White Paper

FPGA and SoC

Intel Agilex® 5 FPGA D-Series - Ideal for Midrange FPGA Applications Requiring Performance, Lower Power, and Smaller Form Factors

Intel 7 technology and monolithic construction deliver advanced Intel Agilex® 5 FPGAs for midrange applications

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Executive Summary

Tremendous market acceptance of the initial Intel Agilex® 5 FPGA families has driven Intel to expand and innovate the Intel Agilex 5 FPGA architecture with new features and densities that suit an even wider range of applications in the communications infrastructure, broadcast, medical, test & measurement and industrial robotics markets.

These capabilities are increasingly important as workloads like those that use artificial intelligence and machine learning algorithms migrate out from data centers to the network's edge, where localized concurrent processing and analysis are needed to meet demanding, system-level latency requirements. At the same time, power is more constrained in many applications which means the implementation technology employed must be power efficient while providing the required performance attributes.

The new Intel Agilex 5 FPGA D-Series devices are manufactured on Intel 7 technology and have a monolithic construction to deliver the excellent performance per watt characteristics needed to meet these varied application requirements.

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Introduction: The Challenges of Data Proliferation at the Edge and in the Core

The world is becoming more digitized and connected every day generating data 24 hours a day 7 days a week. There's a competitive imperative to analyze all this data to extract value from it and to produce actionable insights. We're in the era of big data and that world gets bigger and more complex by the minute. Yet companies analyze only 12% of the available data according to a widely quoted Forrester Research paper[1].

According to IDC, 64.2 zettabytes (ZB) of data were created in 2020 and less than 2% of that data was saved or retained into 2021[2]. From 2020 to 2025, IDC forecasts that new data will be created at a compound annual growth rate (CAGR) of 23%, resulting in approximately 175 ZB of annual data creation by 2025[3]. Clearly, there's more than enough data to analyze. What's needed are better, faster ways to analyze this data, to derive actionable insights, and to create additional value from these analyses. This data analysis demands increased agility and flexibility to handle the exploding diversity in data types and to implement new data-analysis algorithms and methods including artificial intelligence (AI) and machine learning (ML) techniques.

[1] Brandon Purcell, "Q&A: The Secrets of Successful Segmentation Revealed", Forrester, January 1, 2018.

[2] IDC, "Data Creation and Replication Will Grow at a Faster Rate than Installed Storage Capacity, According to the IDC Global DataSphere and StorageSphere Forecasts", March 24, 2021.

[3] IDC Report, "Worldwide Global DataSphere Forecast, 2021–2025: The World Keeps Creating More Data — Now, What Do We Do with It All?" (Doc #US46410421), March 2021.

Because of their flexible nature and ability to implement nearly any sort of processing architecture, programmable logic devices, namely FPGAs, have been on the forefront of advanced data-processing systems for more than three decades. Along the journey, FPGAs accumulated several useful capabilities such as fast on-chip memory, high-speed serial transceivers, and hardened intellectual property (IP) blocks including digital signal processing (DSP) functions, fast SDRAM memory controllers, and multi-core microprocessor system. This expanding collection of capabilities make Intel® FPGAs ideal implementation platforms for meeting today's toughest data-processing challenges.

Introducing the Intel Agilex 5 FPGAs and SoCs D-Series

The first Intel Agilex 5 FPGA and SoC families were introduced in early 2019. Back then, EEJournal's Founder and Editor-in-Chief Kevin Morris wrote, "Intel Agilex® 5 FPGA is a milestone in the evolution of FPGA technology, and it brings substantial new capabilities to the party." The market realized the advantages of those new capabilities, which have made the Intel Agilex 5 FPGA and SoC families extremely successful. Expending this evolutionary architecture into additional markets where power efficiency (performance per watt) and smaller packaged device size are just as important as raw performance, inspired the development of the Intel Agilex 5 FPGAs and SoCs D-Series family.

The new Intel Agilex 5 FPGAs and SoCs D-Series incorporate many new features such as an upgraded hard processor system (HPS), Enhanced DSP with AI Tensor Blocks, MIPI I/O support, and hardened Time Sensitive Networking (TSN) controller. These features make Intel Agilex 5 FPGAs D-Series ideal for midrange FPGA applications requiring performance, lower power, and smaller board level footprints .

Intel has taken advantage of its in-house manufacturing capabilities for the Intel Agilex 5 FPGA D-Series device family, which extends the Intel Agilex 5 FPGA portfolio to lower logic densities, lower power consumption, and smaller form factors than previously offered. Where the initial Intel Agilex 5 FPGA and SoC families are manufactured with Intel 10 nm SuperFin technology.

The Intel Agilex 5 FPGA D-Series devices are manufactured using Intel 7 technology, which is now a mature process that Intel uses to manufacture CPUs including the 12th generation Intel® Core™ CPUs and 4th Generation Intel® Xeon® Scalable server CPUs. Intel Agilex 5 FPGAs D-Series inherit many strong and proven architectural features from the initial Intel Agilex 5 FPGA families including the second-generation Intel Hyperflex FPGA Architecture and SmartVID power-management technology that significantly improve performance and reduce power consumption within the programmable-logic fabric.

Intel 7 technology permits Intel to create programmable-logic devices that integrate fast I/O circuits including 28 Gbps transceivers and flexible general-purpose I/O banks along with programmable logic and hardened IP blocks, all on one monolithic silicon die. A further advantage of Intel 7 technology is that it allows the Intel Agilex 5 FPGAs D-Series to have both high-speed I/O banks and high-voltage I/O banks that can support 3.3 V operation. All these capabilities help the Intel Agilex 5 FPGA D-Series devices provide excellent power-efficient performance while offering lower densities and smaller package options.

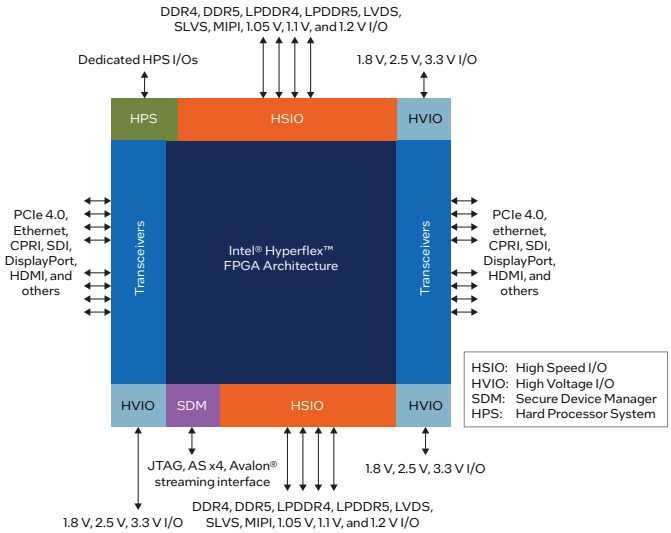

Figure 1. The advanced Intel 7 technology with thick gate oxide allows Intel to manufacture Intel Agilex 5 FPGAs and SoCs D-Series including the programmable-logic fabric, hard processor system, high-speed and high-voltage I/O ports (HSIO and HVIO), and high-speed serial transceivers as a monolithic device.

In addition, Intel Agilex 5 FPGAs and SoCs D-Series incorporate several hard IP blocks that are new to the Intel Agilex 5 FPGA family including Enhanced DSP with AI Tensor Block, a TSN controller, a MIPI interface, and an upgraded HPS that includes two Arm Cortex-A76 processor cores and two Arm Cortex-A55 processor cores. These new hardware features plus the high-performance, low-power programmable-logic fabric make Intel Agilex 5 FPGAs and SoCs D-Series ideal for use in midrange FPGA applications across many markets including wireless and wireline communications, video and audio broadcast equipment, industrial applications, test and measurement products, medical electronics, and military/aerospace applications.

An Architecture Optimized for Edge and Core Applications

The programmable-logic fabric in the Intel Agilex 5 FPGAs D-Series uses essentially the same fabric architecture that is used in the high-performance Intel Agilex 7 FPGA I-Series, F-Series, and M-Series. The same second-generation Intel Hyperflex FPGA Architecture, which uses Hyper-Registers throughout the FPGA to maximize throughput and performance and to minimize power consumption. Intel Agilex 5 FPGAs D-Series bring these advanced capabilities into the midrange FPGA realm.

Intel Agilex 5 FPGAs and SoCs D-Series also feature multiple I/O capabilities that can handle nearly any I/O task needed in equipment used from the edge of the network to its core, including:

- High-speed SerDes transceivers capable of operating at data rates as fast as 28.1 Gbps that support a variety of interface standards including Ethernet and PCI Express (PCIe) 4.0

- High-speed general-purpose I/O banks with single-ended support for a variety of interface standards including 1.05 V, 1.1 V, and 1.2 V LVCMOS; differential I/O support for LVDS and MIPI D-PHY applications; and key I/O functions such as a hard memory controller for DDR4, LPDDR4, DDR5, LPDDR5, DDR-T2 SDRAM, and QDR-IV SRAM
- High-voltage I/O banks that support up to 3.3 V, single-ended LVCMOS voltage levels to support interfaces to legacy devices

In addition, Intel Agilex 5 FPGAs and SoCs D-Series incorporate several hard IP elements that are new to the Intel Agilex 5 FPGA family including:

An upgraded HPS

Intel Agilex 5 FPGAs and SoCs D-Series introduce an upgraded HPS to the Intel Agilex 5 FPGA device families. This upgraded HPS incorporates two 32/64-bit Arm Cortex-A76 and two 32/64-bit Arm Cortex-A55 processor cores. The Arm Cortex-A76 cores in the HPS operate at clock speeds as fast as 1.8 GHz and the Arm Cortex-A55 cores operate at clock speeds as fast as 1.5 GHz. This upgraded HPS includes a system memory management unit that enables system-wide hardware virtualization. The HPS also incorporates many hard peripheral IP blocks to support a wide range of I/O requirements. The processor cores used in the HPS for Intel Agilex 5 FPGAs and SoCs D-Series employ Arm's DynamIQ multi-core processor technology, which allows software to combine the Arm Cortex-A76 and Cortex-A55 CPUs into a single, fully-integrated processor cluster that delivers additional power and performance benefits to applications ranging from portable devices to infrastructure gear from the network's edge to its core.

High-Speed, Monolithic Transceivers

Intel Agilex 5 FPGAs and SoCs D-Series are equipped with high-speed non-return-to-zero (NRZ) transceivers that support data rates ranging from 1 Gbps to 28.1 Gbps. These transceivers exhibit low latency and are optimized for a wide variety of applications, including long-reach backplanes.

Enhanced DSP with AI Tensor Block

The DSP blocks incorporated into the programmable-logic fabric of Intel Agilex 5 FPGAs and SoCs D-Series inherit the design of the variable-precision DSP blocks in the other Intel Agilex 5 FPGA device families, which already offer AI capabilities. In addition to those capabilities, the DSP blocks in Intel Agilex 5 FPGAs and SoCs D-Series add features derived from the tensor block used in the Intel® Stratix® 10 NX FPGAs.

The Enhanced Digital Signal Processing with AI Tensor Block within the FPGA fabric of these new Intel Agilex 5 FPGAs and SoC FPGAs inherit the design of the variable-precision DSP blocks in the earlier Intel Agilex 5 FPGA device families, which already offer AI capabilities. In addition, it adds features derived from the tensor block used in the Intel® Stratix® 10 NX FPGAs. The Enhanced DSP with AI Tensor Block introduces two new important operations: the tensor processing capability for AI and complex number support for signal processing applications such as fast Fourier transform (FFT) and complex finite impulse response (FIR) filters.

The first mode enhances AI with the INT8 tensor mode, which provides twenty INT8 multiplications within one Enhanced DSP with AI Tensor Block, and increases INT8 compute density by 5X versus earlier Intel Agilex 5 FPGA device families. The tensor mode uses a two-column tensor structure with both INT32 and FP32 cascade and accumulation capability, and also supports a block floating exponent for improved inference accuracy and low-precision training. In addition, the AI capability of the variable-precision DSP functionality has also been enhanced. The vector mode has been upgraded from four INT9 multipliers to six INT9 multipliers. These modes are extremely useful for AI-centric tensor math and for various DSP applications.

The second new mode, the complex-number operation, doubles the performances of the tensor block when performing complex-number multiplication. Previously, two DSP blocks were needed for complex-number multiplication, but this new family of Intel Agilex 5 FPGAs and SoC FPGAs can multiply 16-bit, fixed-point, complex numbers within one Enhanced DSP with AI Tensor Block.

Applications	Multiplier	Capabilities per DSP Block		Improvement*
		Earlier Intel Agilex Devices	Enhanced DSP with AI Tensor Block*	
AI, Signal Processing	INT8	4 OPS	20 OPS	5X
	INT9	4 Multipliers	6 Multipliers	50%
Signal Processing	16-bit Complex Multiplier	Needs 2 DSP Blocks	1 DSP Block	2X

Figure 3. Order of magnitude increase in AI and DSP compute density.

*Available in Intel Agilex® 5 FPGAs D-Series and the new Intel Agilex 5 FPGA device family code named Sundance Mesa.

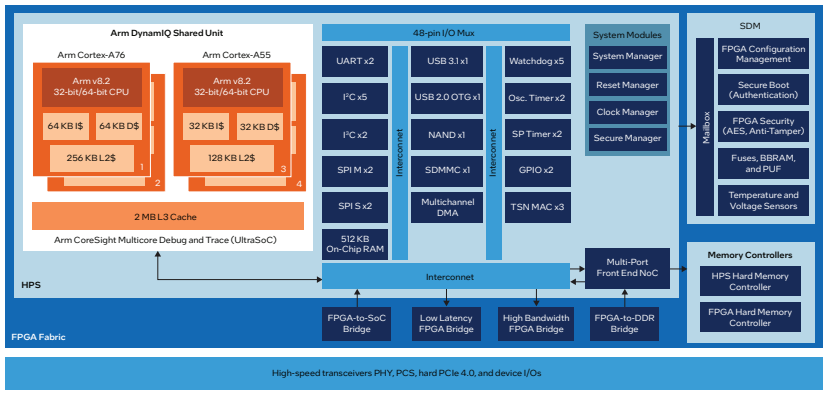

Figure 2. The HPS in Intel Agilex 5 FPGAs and SoCs D-Series incorporates two Arm Cortex-A76 processor cores, two Arm Cortex-A55 processor cores, and many peripheral IP blocks to support varied I/O requirements.

Time Sensitive Networking (TSN)

TSN is a set of standards developed by the Time-Sensitive Networking task group of the IEEE 802.1 working group. These standards define mechanisms for the time-sensitive transmission of data over deterministic Ethernet networks and are needed by applications throughout the network to synchronize systems ranging from Internet of Things (IoT) devices to servers, and everything in between. The hard Ethernet MACs in the Intel Agilex 5 FPGAs and SoCs D-Series implement TSN endpoint functionality compliant to IEEE 802.1AS-2020, Qav, Qbv, Qbu, and IEEE 802.3br standards. Previously, TSN was implemented in programmable logic. However, TSN usage has now become so widespread that it made sense to build TSN capabilities directly into the hard Ethernet MACs of the Intel Agilex 5 FPGA D-Series devices.

MIPI D-PHY

Intel Agilex 5 FPGAs and SoCs D-Series incorporate MIPI IP to support a wide range of video applications. This IP supports MIPI D-PHY v2.5 at data rates as fast as 3.5 Gbps for MIPI's standard reference channel and as fast as 2.5 Gbps for MIPI's long reference channel. The IP also supports MIPI D-PHY high-speed and low-power signaling modes without requiring external components. The MIPI IP's D-PHY implementation supports MIPI's Camera Serial Interface (CSI) version 3.0 and Display Serial Interface (DSI) version 2.0.

Intel Agilex 5 FPGA and SoC D-Series Example Use Cases

Together, Intel Agilex 5 FPGA D-Series device features including the hard IP elements listed above support a very wide range of applications. Some of these applications include:

ORAN–Open RAN for 5G and 6G Communications

Today's wireless infrastructure is built around heterogeneous communications networks assembled from many different-sized radios organized as femtocells, picocells, microcells, and macrocells.

Each of these cells exhibits widely different requirements, including:

- Number of radio bands and frequencies supported
- Modulation technology and protocols (GSM, CDMA, UMTS, 4G LTE/LTE-A, 5G, NB-IOT)
- RF output power level
- Number of antenna elements, ranging from eight antennas for femtocells and picocells to hundreds of antennas for microcell and mmWave implementations
- Number of carriers, covering 4G, 5G, NB-IOT, and legacy standards (2G, 3G)
- Number of supported users per cell
- System configuration (integrated antenna, remote radio head, traditional, active antenna arrays)
- Form factor and power consumption including outdoor vs indoor and with or without power over Ethernet (PoE)

Operators need to draw upon a broad range of radio hardware when developing ORAN solutions. Scalable platform solutions based on Intel FPGAs and SoCs allow operators to quickly adapt to changing standards and to the evolving performance requirements that characterize modern wireless communications. Scalable, flexible platform solutions minimize design effort, lower design and manufacturing costs and reduce time to market.

The key components of digital radio IP are:

- Fronthaul interface and processing (CPRI/eCPRI/ORAN)
- Low Layer 1 (FFT/iFFT/PRACH/CP add/removal)
- Digital up conversion (DUC) and digital down conversion (DDC)
- Crest factor reduction (CFR)
- Digital predistortion (DPD)

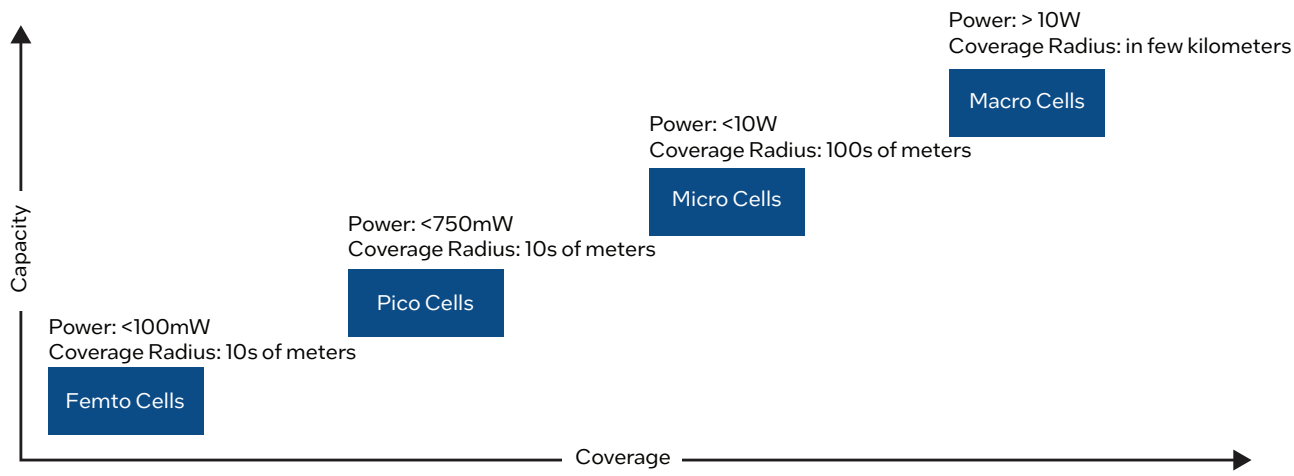

Figure 4. ORAN systems incorporate multiple cellular radios with varying characteristics, ranging from femtocells to macrocells, covering areas from meters to kilometers with MIMO arrays consisting of eight to hundreds of antennas.

Intel Agilex 5 FPGAs and SoCs D-Series provide flexible, cost-effective, and scalable platforms for implementing digital radios. In addition, the flexible I/O capabilities of Intel Agilex 5 FPGAs and SoCs D-Series can easily handle the many interfacing standards used in ORAN systems. One of the key advantages of using programmable logic devices like Intel Agilex 5 FPGAs and SoCs D-Series is that they can accommodate new and evolving standards and new end-product requirements, and they make it easy to propagate design fixes to fielded equipment.

Intel has partnered with various IP and hardware suppliers to deliver ORAN compliant O-RU reference platforms for macrocell, microcell, and picocell radio applications, and has a roadmap toward mMIMO (massive MIMO) and mmWave designs. These ORAN reference platforms can all be leveraged for use with Intel Agilex 5 FPGAs and SoCs D-Series.

8K Broadcast Video Routers, Switches, and Processors

The digital video industry continues to evolve with market trends, adding new technologies along the way such as the increased widespread consumer demand for 8K Ultra High Definition (UHD) video. The continued emergence of new video connectivity standards such as HDMI 2.1 and DisplayPort 2.0 continue to challenge video equipment design teams as do the paradigm shift to video-over-IP solutions, the need for artificial intelligence-based video analytics at the edge, and the diversification of display module form factors.

FPGAs are often used for the design of broadcast because of their flexibility, which enables the adoption of the latest video broadcast standards and is especially helpful while the industry is continuously evolving and improving video quality and is still in the early stages of defining Video-over-IP standards. With a robust portfolio of high quality, video processing and connectivity IP and ready-to-go reference design hardware, Intel is enabling video developers to quickly add and develop new custom features or accommodate other customer-specific requirements today.

Video resolutions have increased over the decades from SD (720x486), through HD (1920x1080), UHD 4K (3840x2160), 8K (7680x4320), and beyond. The clock frequencies required to handle this increasing bandwidth has likewise increased. The pixel clock for SD resolution video was just 27 MHz; easily accomplished today. HD video resolutions require clock frequencies of 74.25 MHz or 148.5 MHz, which again are easily achieved today. However, 4K resolution requires a pixel clock speed of 594 MHz, which start pushing the boundaries of single pixel video pipelines, and 8K video requires a pixel clock speed of 2.376 GHz, which forces a different design approach from video engineers.

To cope with this high pixel clock speed, video IP cores such as scalers or color-space converters must be designed to process multiple pixels during each clock cycle. In most cases, this means replicating the entire video pipeline within the video-processing IP. Moving from video pipelines that process one pixel at a time to two pixels at a time for 4K video doubles the number of FPGA resources required. Early adopters of 8K video design often rely on similar parallel-processing techniques and were forced to process eight pixels at a time to accommodate the fast pixel clock, with predictable increases in FPGA resource usage.

Intel Agilex 5 FPGAs and SoCs D-Series are ideal for low-power video applications. At the same time, they're designed to operate at higher frequencies, which minimize resource usage and power consumption for a given logic function. The ability to reach 600 MHz, often without requiring extensive rewriting of existing RTL code, is of particular interest to video designers because it permits 8K video processing at 60 frames-per-second with a pipeline that handles just four pixels at a time, which cuts FPGA utilization in half.

Robotics

The robotics field encompasses a challenging set of applications including video processing, AI and ML inferencing, sensing, and motion control. Intel Agilex 5 FPGAs and SoCs D-Series are equipped with all the I/O, networking (including TSN), processing, and functional safety capabilities needed to implement a full-spectrum of industrial robots from industrial arms for manufacturing to mobile robots that scan the environment for intruders or other problems.

Many robotics manufacturers have already adopted Intel FPGAs for their designs. For example, one robotics manufacturer selected an Intel FPGA for a safeguard system that allows humans and robots to work together safely and seamlessly in close proximity inside of factory workcells. To ensure safe operation, large industrial robots are usually caged off and require human operators to use tag-out/lock-out procedures for entry into the robot's work area. These procedures significantly slow interaction with the production line and reduce productivity. Allowing robots and humans to work safely alongside each other greatly enhances productivity. This robotics manufacturer chose Intel FPGAs because of their hard real-time and deterministic computational capabilities combined with their functional safety certification, deep portfolio of IP blocks, and development tools.

Conclusion

With the power and performance efficiency of industry-leading Intel 7 technology, Intel Agilex 5 FPGAs and SoCs D-Series are optimized for a wide range of applications that require lower power and higher performance. Devices in the Intel Agilex 5 FPGA D-Series device family include many features needed to develop systems for edge and core applications such as:

- Up to sixteen 28.1 Gbps serial transceivers capable of supporting 25 Gbps Ethernet ports
- High-bandwidth processor interface interconnects, including PCIe 4.0 x8
- Scalable integrated memory controllers with support for DDR4, DDR5, LPDDR4, and LPDDR5 SDRAM
- Variable-precision, AI-enabled DSP or tensor blocks capable of executing as many as 40 TFLOPS
- Hardware support for Advanced Encryption Standard (AES) cryptography
- A HPS with two Arm Cortex-A76 processor cores running at clock speeds to 1.8 GHz and two Arm Cortex-A55 processor cores running at clock speeds 1.5 GHz
- Second-generation Intel Hyperflex FPGA Architecture for faster implementations in the FPGA fabric
- Support for multiple high-speed video I/O standards including MIPI D-PHY v2.5 at up to 3.5 Gbps per lane, serial digital interface (SDI), DisplayPort, and high-definition multimedia interface (HDMI)
- High-speed I/O (HSIO) ports supporting voltage levels of 1.05 V to 1.3 V and high-voltage I/O (HVIO) ports supporting voltage levels from 1.8 V to 3.3 V

All these features combined provide developers of systems for edge and network core applications with a comprehensive toolkit of hardware, software, IP, and reference designs that can tackle a tremendous number of design challenges. For more information about Intel Agilex 5 FPGAs and SoCs D-Series, view the resources listed below or contact your local Intel sales representative.

Learn More

- Intel Briefing Sheet: Keeping pace with the ever-changing wireless landscape
- FPGA Video and Vision Solutions
- White Paper: FPGAs for Live Video Production Workflows
- Robotics Technology Is Redefining What's Possible
- Case Study: FPGAs in Veo FreeMove Industrial Robotics

References

Kevin Morris, "Inside Intel Agilex FPGAs," EEJournal.com, April 9, 2019.

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