MAX 10 - DDR3 Memory Test with NIOS II Getting Started Guide

Design Overview

As MAX 10 DDR3 UniPHY controller is not support EMIF v16.0 toolkit. This design example is introduced to demonstrate how to run memory test on particular memory address using NIOS II eclipse memory test template. The purpose of this design example is to ease user to determine which memory address is fail on DDR3 read/write transaction.

Running the memory test

1) Run full compilation on testddr3_nios_ddr3.qar with Quartus 16.0

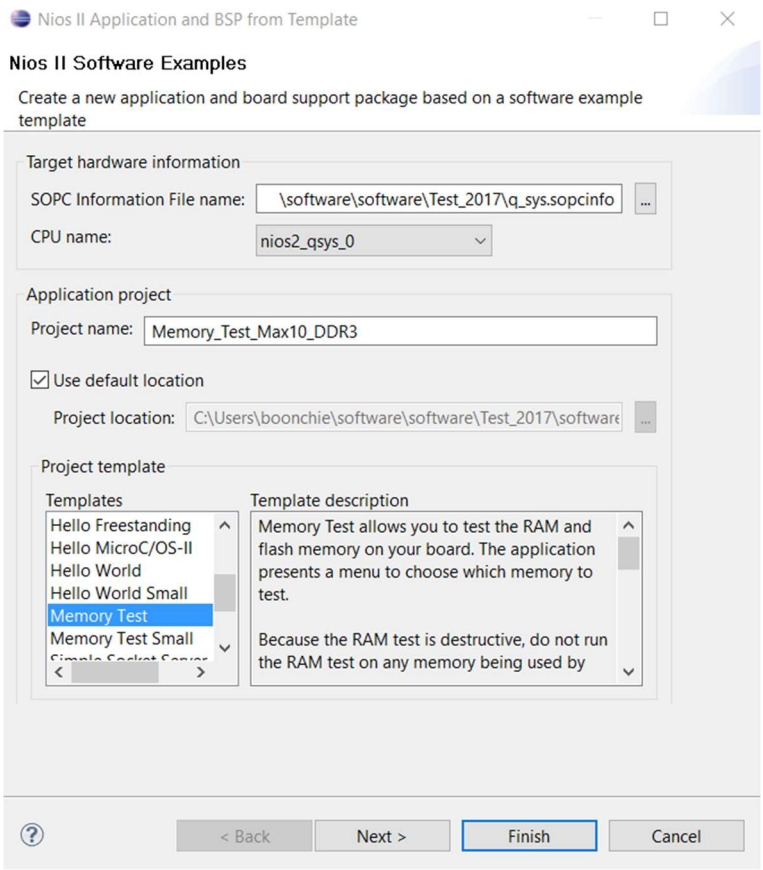
2) Launch Quartus Programmer and program testddr3.sof to the MAX 10 FPGA Development Kit

3) Launch NIOS II 16.0 Software Build Tools for Eclipse

4) Go to File Tab and click *NIOS II Application and BSP from Template*

5) Set as below and click finish:

- SOPC Information File name : q_sys.sopcinfo
- Project name : Memory_Test_MAX10_DDR3
- Project Template: Memory Test



6) Under Project Explorer, right click *Memory_Test_MAX10_DDR3_bsp*. Move to *Nios II* and click *Generate BSP*

7) Under Project Explorer, right click *Memory_Test_MAX10_DDR3*. Move to *Run AS* and click *3 Nios II Hardware*

8) Under *Nios II Console* Tab, type 'a' then 'enter' to select 'Test RAM'

9) Follow the instruction by enter start and end address range to test the RAM. For this Qsys design, the DDR3 address range is 0x0000_0000 to 0X07ff_ffff

Downloads

- Qsys_sopcinfo.zip – *q_sys.qsys* and *q_sys.sopcinfo*
- Output_files.zip – Compilation output files including *testddr3.sof*