Solution Brief

ADC/DAC Cockpit for Intel® Direct RF-Series FPGA

Design Example

Description

Intel® Direct RF-Series FPGA provides unprecedented technological capabilities that allow wideband and SWAP-sensitive systems. Beyond its unrivaled analog/digital front-end sampling capabilities, it includes full flexible signal processing data path that optimizes the system in terms of agility, latency, integration, and power consumption.

To help new users comprehend Intel Direct RF-Series FPGA capabilities quicker and allow out-of-the-box evaluation capability, Intel developed an analog-to-digital converter (ADC) or digital-to-analog converter (DAC) cockpit design example. This design features a graphical user interface (GUI) to explore and configure the analog tile blocks with a variety of settings. These include configuring the decimation or interpolation modes of up/down converters, center frequency of course and fine tuners, setting loopback modes, sample rate, and so on.

On the DAC path, it includes a waveform generator that allows flexible waveform source to be fed to the DAC. On the ADC path, cockpit provides simultaneous capturing capability across two tiles and ports and then visualizing them in waveform viewer. For cases where more accurate evaluation with significantly bigger number of samples required, cockpit can synchronously capture any two ports from any tile into DDR4 external memory. This allows up to 256M samples captures per port.

Phase array systems require coherent data streams, thus gain and timing alignment of data samples is crucial. Intel created an example of how to perform skew and gain measurements and then apply compensation to data stream to reach accurate alignment of data in time and gain.

Features

- ADC and DAC data path configuration
  - Modes, numerically controlled oscillators, tuners, loopback mode
- Synchronous capture across all ports/tiles
- Flexible waveform generation
- Waveform viewer
- Modes: x1, x8H, x8F, x16 - x1024
- Runtime mode switching
- RF calibration flow for ADC and DAC
- Latency alignment flow
- Skew alignment flow
- Sampling rate support: 44–64 GSPS
- Dual-channel deep capture up to 256M samples with external trigger
- Direct register tile control
- Telemetry

Applications

- Radar and electronic countermeasures
- Test and measurement equipment
- Communication systems

For more information about Intel® FPGA design example, contact Intel.