Solution Brief

Multiple Device Synchronization for Intel Agilex® 9 SoC FPGA Direct RF-Series

Design Example

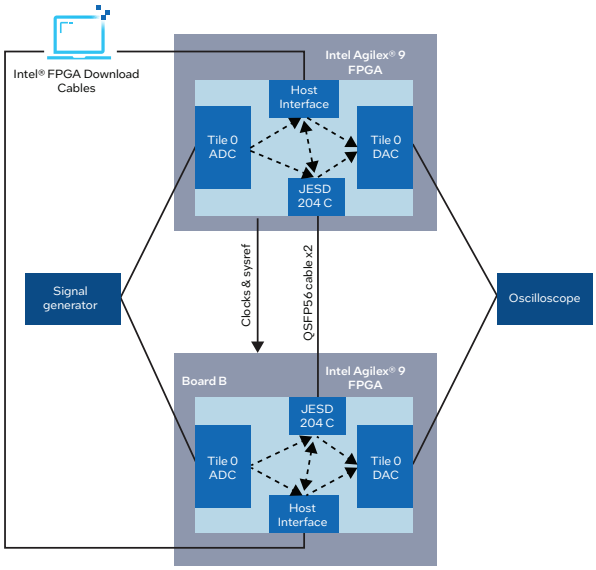
Description

Intel Agilex® 9 SoC FPGA Direct RF-Series provides unprecedented technological capabilities that allow wideband and SWAP-sensitive systems. Its unrivaled analog/digital sampling capabilities can be key enabler in many applications.

To showcase Intel Agilex® 9 SoC FPGA Direct RF-Series synchronization capability, Intel developed a multiple device synchronization design example. This design demonstrates the deterministic latency link between two analog-to-digital converter (ADC) or digital-to-analog converter (DAC) nodes by JESD204C subclass1 protocol, latency alignment, and phase alignment between different ports in local and remote devices.

The Multiple Device Synchronization design example includes a MATLAB-based GUI, which shows the waveforms overlap when the system is synchronized. It also includes the ADC and DAC setting block, latency alignment GUI, and phase alignment GUI.

This design can be used as an out-of-the-box demo to evaluate Intel Agilex® 9 SoC FPGA Direct RF-Series synchronization capability, show the ability of multiple Intel Agilex® 9 SoC FPGA Direct RF-Series devices performing sophisticated processing of data synchronization, and serve as a potential starting point for customer applications.



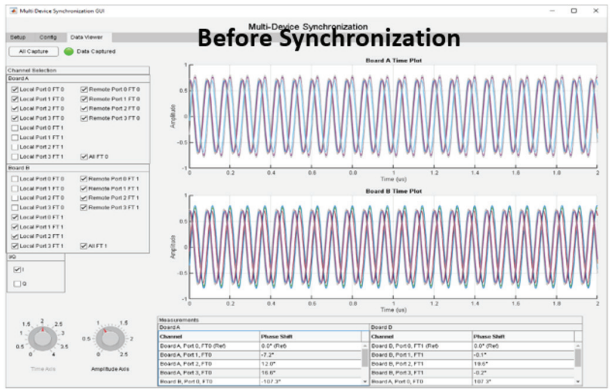
Features

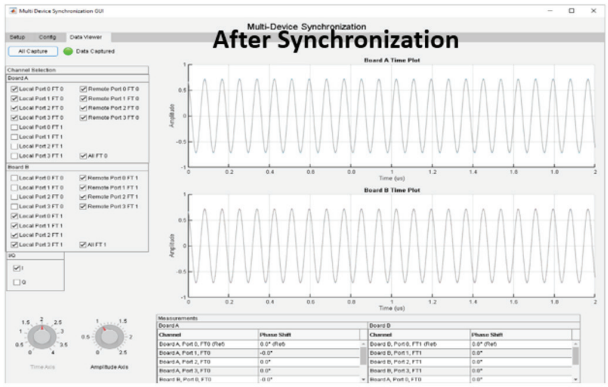
- Mode: x32
- Sampling rate support: 51.2 GSPS
- Latency alignment flow
- Phase alignment flow
- Signal viewer to check waveforms overlap
- Intel® Agilex® 9 Direct RF FPGA Development Kit (014)

Applications

- Radar and electronic countermeasures
- Communication systems

For more information about Intel® FPGA design example, contact Intel.





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