Solution Brief

Time Delay Beamformer for Intel® Direct RF-Series FPGA

Design Example

Description

Intel® Direct RF-Series FPGA provides unprecedented technological capabilities that allow wideband and SWAP-sensitive systems. Its unrivaled analog/digital sampling capabilities can be key enabler in many applications.

Beamforming is an integral part of radar and communications applications where direction of the wavefront can be adjusted accordingly. Digital Time Delay Beamforming offers arbitrary angular resolution, simultaneous beams at different angles, and makes no compromise in quality. Wideband radar signal offers high range resolutions and embeds more details about the reflection for object discrimination. The high sampling rate of the Intel Direct RF-Series FPGA A-tile supports such applications.

This design features a super sample rate fractional delay resampler filter in the time delay engine developed using a DSP Builder for Intel® FPGAs' design tool oriented for DSP developers. There are four instances of the time delay engine to support four simultaneous beams, where each beam is independent and controlled separately. The beam response is stored in a local buffer and displayed on the host through the MATLAB GUI.

The time delay beamformer design includes a channel synchronization flow to support latency and phase alignment for wideband signals.

This design can be used as an out-of-the-box demo to evaluate Intel Direct RF-Series FPGA capabilities, show the ability of FPGA to perform sophisticated processing of data, and serve as a potential starting point for customer applications.

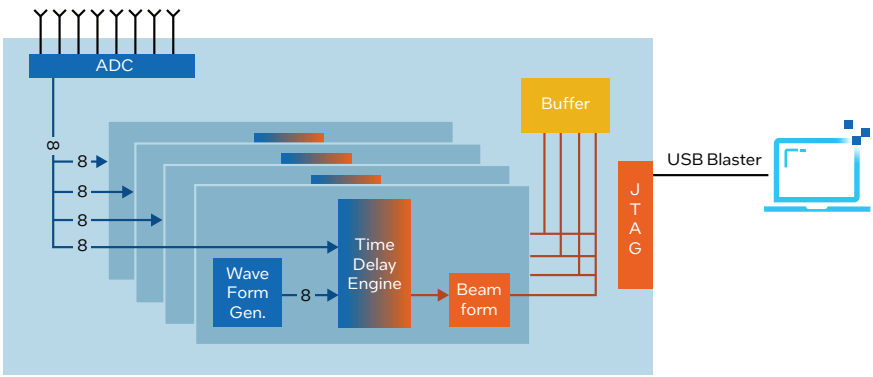
Features

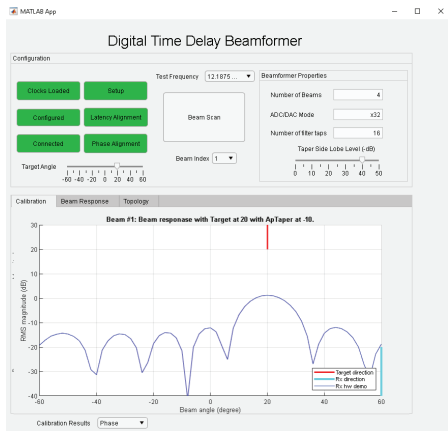
- 8 RX channels in x32 mode at 64 GSPS
- 14 beams, 16-bit complex I, Q at 1.625 GSps
- Bandwidth of 1.6 GHz
- Fractional delay filter with 16-taps, oversampling ratio of 128
- Channel synchronization for wideband signals
- Beam scan range: +/- 60 degrees

Applications

- Active electronically scanned array (AESA)
- Radar and sonar
- Electronic warfare
- Phased array radio telescope

For more information about Intel® FPGA design example, contact Intel.





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