Intel® Processor and Intel® Core™ i3 and Intel® Core™ 3 N-Series

Datasheet - Volume 2 of 2

Revision 003

January 2025

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Contents

Revision History

Revision Number	Description	Revision Date
001	• Initial release	January 2023
002	• Updated Section 13.3.21, "VCCIN AUX CONFIG Register2 (VCCIN_AUX_CFG2)—Offset 11D4h" • Updated Chapter 33, "General Purpose I/O (GPIO)" • Added Section 43.4, "UFSHC MIMO Registers"	June 2023
003	• Added Intel® Core™ 3 N-Series Processor	January 2025

1 Introduction

This is Volume 2 of the Intel® Processor and Intel® Core™ i3 and Intel® Core™ 3 N-Series Datasheet. It provides register information for the processor. Refer #759603 for Datasheet, Volume 1 of 2.

The processor contains one or more PCI devices within a single physical component. The configuration registers for these devices are mapped as devices residing on the PCI Bus assigned for the processor socket. This document describes these configuration space registers or device-specific control and status registers only.

Table 1. Updated Terminology

Existing	Updated Terminology
TDP	Processor Base Power
cTDP Down Power	Minimum Assured Power
cTDP Down Frequency	Minimum Assured Frequency
cTDP Up	Maximum Assured Power
cTDP Up Frequency	Maximum Assured Frequency
P1 Freq	Processor Base Frequency
Small Core	E-core
Big Core	P-core

1.1 Terminology Usage

This document uses the terms ‘initiator’ and ‘target’ (formerly known as ‘master’ and ‘slave’).

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2 Processor Configuration Register Definitions and Address Ranges

This chapter describes the processor configuration register, I/O, memory address ranges and Model Specific Registers (MSRs). The chapter provides register terminology. PCI Devices and Functions are described.

2.1 Register Terminology

Table below lists the register-related terminology and access attributes that are used in this document. Register Attribute Modifiers table provides the attribute modifiers.

Table 2-1. Register Attributes and Terminology

Item	Description
RO	**Read Only:** These bits can only be read by software, writes have no effect. The value of the bits is determined by the hardware only.
RW	**Read / Write:** These bits can be read and written by software.
RW1C	**Read / Write 1 to Clear:** These bits can be read and cleared by software. Writing a '1' to a bit will clear it, while writing a '0' to a bit has no effect. Hardware sets these bits.
RW0C	**Read / Write 0 to Clear:** These bits can be read and cleared by software. Writing a '0' to a bit will clear it, while writing a '1' to a bit has no effect. Hardware sets these bits
RW1S	**Read / Write 1 to Set:** These bits can be read and set by software. Writing a '1' to a bit will set it, while writing a '0' to a bit has no effect. Hardware clears these bits.
RsvdP	**Reserved and Preserved:** These bits are reserved for future RW implementations and their value should not be modified by software. When writing to these bits, software should preserve the value read. When SW updates a register that has RsvdP fields, it should read the register value first so that the appropriate merge between the RsvdP and updated fields will occur.
RsvdZ	**Reserved and Zero:** These bits are reserved for future RW1C implementations. Software should use 0 for writes.
WO	**Write Only:** These bits can only be written by software, reads return zero.
RC	**Read Clear:** These bits can only be read by software, but a read causes the bits to be cleared. Hardware sets these bits
RSW1C	**Read Set / Write 1 to Clear:** These bits can be read and cleared by software. Reading a bit will set the bit to '1'. Writing a '1' to a bit will clear it, while writing a '0' to a bit has no effect.
RCW	**Read Clear / Write:** These bits can be read and written by software, but a read causes the bits to be cleared.

2.2 PCI Devices and Functions

The processor contains multiple PCI devices. The configuration registers for these devices are mapped as devices residing on PCI Bus 0.

- Device 0: Host Bridge / DRAM Controller / LLC Controller 0 – Logically this device appears as a PCI device residing on PCI bus 0. Device 0 contains the standard PCI header registers, PCI Express base address register, DRAM control (including thermal/throttling control), configuration for the DMI, and other processor specific registers.
- Device 2: Processor Graphics – Logically, this device appears as a PCI device residing on PCI Bus 0. Device 2 contains the configuration registers for 3D, 2D, and display functions. In addition, Device 2 is located in two separate physical locations – Processor Graphics (GT) and Display Engine.
- Device 4: Dynamic Tuning Technology (DTT) - Logically, this device appears as a PCI device residing on PCI Bus 0. Device 4 contains the configuration registers for the DTT device.
- Device 8: Gauss Newton Algorithm Device (GNA) – Logically, this device appears as a PCI device residing on PCI Bus 0. Device 8 contains the configuration registers for the Gauss Newton Algorithm Device.
- Device 9: Intel® Trace Hub. Logically, this device appears as a PCI device residing on PCI Bus 0. Device 9 contains the configuration registers for the Trace Hub device. Trace Hub documentation can be found at https://software.intel.com/sites/default/files/managed/f3/47/intel-trace-hub-developers-manual-v2.pdf
- Device 10: Crash Log & Telemetry Device – Logically, this device appears as a PCI device residing on PCI Bus 0. Device 10 contains the configuration registers for the Crash Log & Telemetry Device.
- Device 13: USB-C Device – Logically, this device appears as a PCI device residing on PCI Bus 0. Device 13 contains the following functions:
  - Function 0: USB-C SuperSpeed Host Controller.
  - Function 1: USB-C SuperSpeed Device Controller.
  - Functions 2, 3: DMA Controllers.
- Device 14: Intel® Volume Management Device. Logically, this device appears as a PCI device residing on PCI Bus 0. Device 14 contains the configuration registers for the Volume Management Device.

Table 2-2. Processor PCI Devices and Functions

Description	Device	Function
HOST and DRAM Controller	0	0
Processor Graphics	2	0
Dynamic Tuning Technology	4	0
Image Processing Unit	5	0
Gauss Newton Algorithm Device	8	0
Trace Hub	9	0
Crash Log	10	0

Table 2-2. Processor PCI Devices and Functions

Description	Device	Function
USB-C SuperSpeed Host Controller.	13	0
USB-C SuperSpeed Device Controller		1
DMA Controllers		2,3
Volume Management Device	14	0

From a configuration standpoint, the DMI is logically PCI bus 0. As a result, all devices internal to the processor and the PCH appear to be on PCI Bus 0.

2.3 System Address Map

The processor supports 4 TB (42 bits) of addressable memory space and 64 KB+3 of addressable I/O space.

This section focuses on how the memory space is partitioned and how the separate memory regions are used. I/O address space has simpler mapping and is explained towards the end of this chapter.

DRAM capacity is limited by the number of address pins available. There is no hardware lock to prevent more memory from being inserted than is addressable.

In the following sections, it is assumed that all of the compatibility memory ranges reside on the DMI Interface. The exception to this rule is VGA ranges, which may be mapped to PCI Express*, DMI, or to the Processor Graphics device (Processor Graphics). The processor does not remap APIC or any other memory spaces above TOLUD (Top of Low Usable DRAM). The TOLUD register is set to the appropriate value by BIOS. The remapbase/remaplimit registers remap logical accesses bound for addresses above 4GB onto physical addresses that fall within DRAM.

The Address Map includes a number of programmable ranges that are not configured using standard PCI BAR configuration:

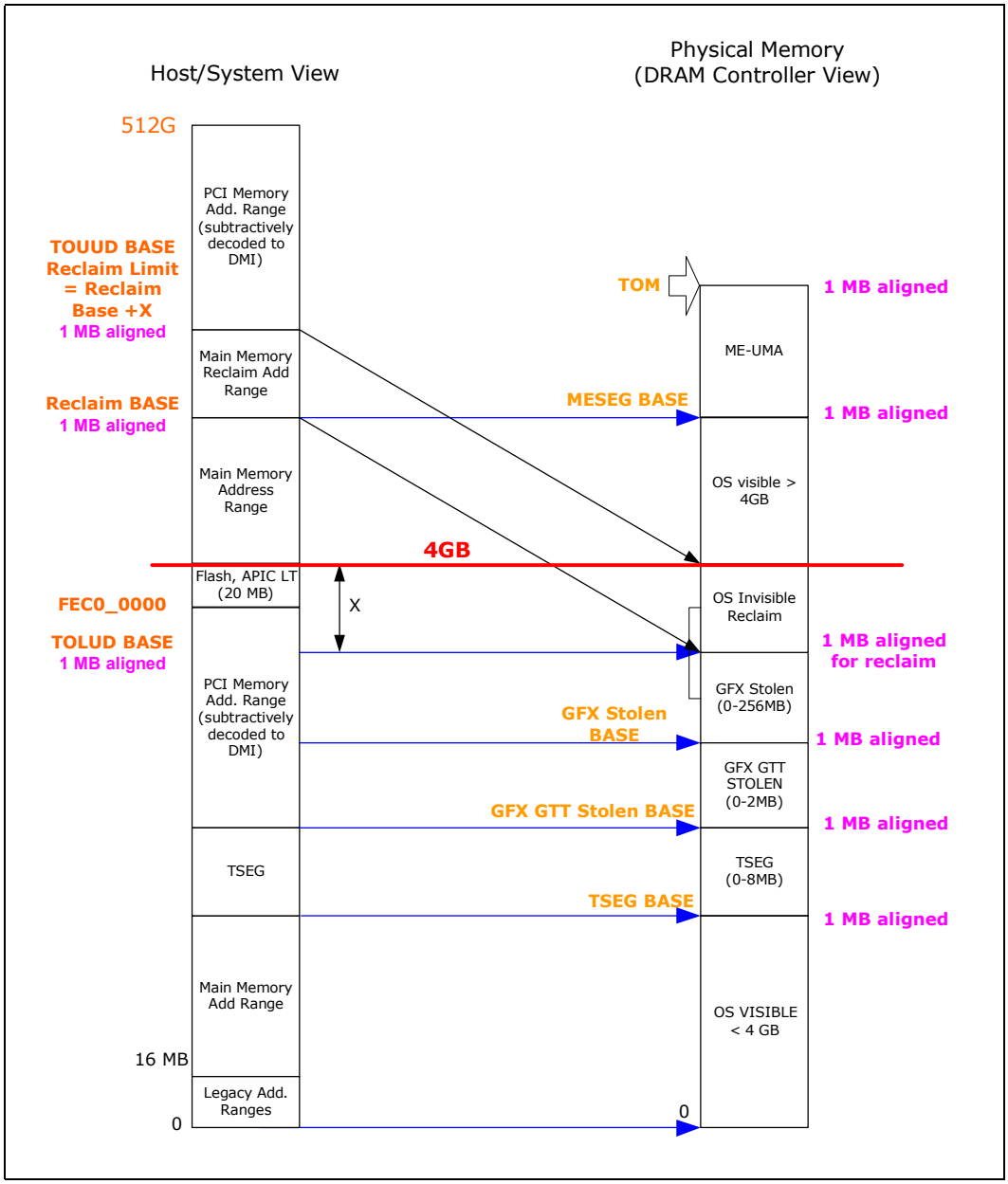
- Device 0:
  - PXPEPBAR – Memory mapped range for PCIe egress port registers. (4 KB window).
  - MCHBAR – Host Memory Mapped Configuration (memory subsystem and power management registers). (128 KB window)
  - DMIBAR – This window is used to access registers associated with the processor/PCH Serial Interconnect (DMI) register memory range. (4 KB window).
  - VTDPVC0BAR - Memory mapped range for VT-d configuration
  - GFXVTBAR - Memory mapped range for VT configuration of the processor graphics device (4KB window).
  - REGBAR - Memory mapped range for System Agent registers (16 MB window).
  - GGC.GMS – Graphics Mode Select. Main memory that is pre-allocated to support the Processor Graphics device in VGA (non-linear) and Native (linear) modes. (0 – 512 MB options).
  - GGC.GGMS – GTT Graphics Memory Size. Main memory that is pre-allocated to support the Processor Graphics Translation Table. (0 – 2 MB options).

- For all other PCI devices within the processor that expose PCI configuration space, the behavior is according to PCI specification.

The rules for the above programmable ranges are:

1. For security reasons, the processor positively decodes (FFE0_0000h to FFFF_FFFFh) to DMI. This ensures the boot vector and BIOS execute off the PCH.
2. ALL of these ranges should be unique and NON-OVERLAPPING. It is the BIOS or system designer's responsibility to limit memory population so that adequate PCI, PCI Express, High BIOS, PCI Express Memory Mapped space, and APIC memory space can be allocated.
3. In the case of overlapping ranges with memory, the memory decode will be given priority. This is an Intel® Trusted Execution Technology (Intel® TXT) requirement. It is necessary to get Intel TXT protection checks, avoiding potential attacks.
4. There are NO Hardware Interlocks to prevent problems in the case of overlapping memory ranges.
5. Accesses to overlapped ranges may produce indeterminate results.
6. Peer-to-peer write cycles are allowed below the Top of Low Usable memory (register TOLUD) for DMI Interface to PCI Express VGA range writes. Peer-to-peer cycles to the Processor Graphics VGA range are not supported.

Figure 2-1. System Address Range Example



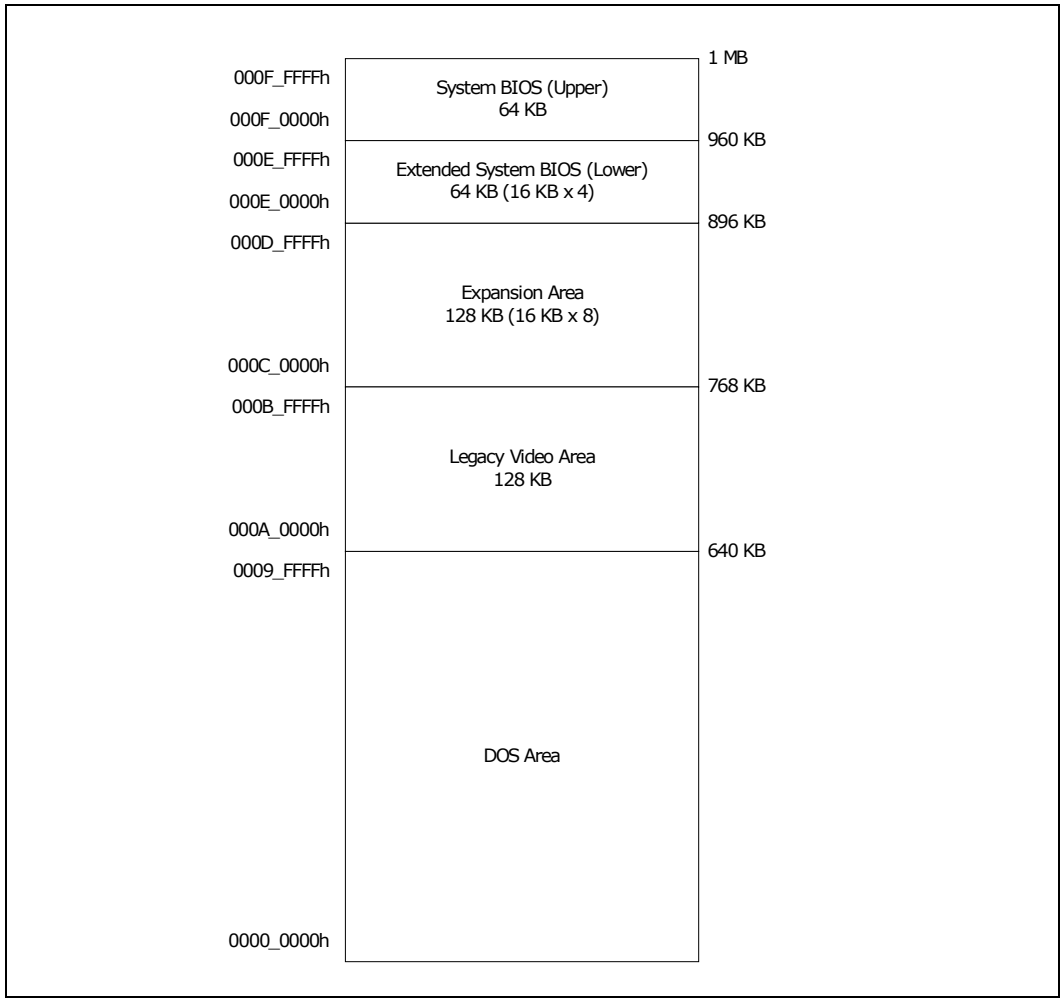
2.4 DOS Legacy Address Range

The memory address range from 0 to 1 MB is known as Legacy Address. This area is divided into the following address regions:

- 0 – 640 KB - DOS Area
- 640 – 768 KB - Legacy Video Buffer Area
- 768 – 896 KB in 16 KB sections (total of 8 sections) – Expansion Area
- 896 – 960 KB in 16 KB sections (total of 4 sections) – Extended System BIOS Area
- 960 KB – 1 MB Memory, System BIOS Area

The area between 768 KB – 1 MB is also collectively referred to as PAM (Programmable Address Memory). All accesses to the DOS and PAM ranges from any device are sent to DRAM. However, access to the legacy video buffer area is treated differently.

Figure 2-2. DOS Legacy Address Range



2.4.1 DOS Range (0h – 9_FFFFh)

The DOS area is 640 KB (0000_0000h – 0009_FFFFh) in size and is always mapped to the main memory.

2.4.2 Legacy Video Area (A_0000h – B_FFFFh)

The same address region is used for both Legacy Video Area.

- Legacy Video Area: The legacy 128 KB VGA memory range, frame buffer, at 000A_0000h – 000B_FFFFh, can be mapped to Processor Graphics (Device 2), to PCI Express (Device 1, 6), and/or to the DMI Interface.
- Monochrome Adapter (MDA) Range: Legacy support for monochrome display adapter

Note: The legacy video area is not available for SMM use.

2.4.2.1 Legacy Video Area

The legacy 128 KB VGA memory range, frame buffer at 000A_0000h – 000B_FFFFh, can be mapped to Processor Graphics (Device 2), to PCI Express (Device 1, 6), and/or to the DMI Interface.

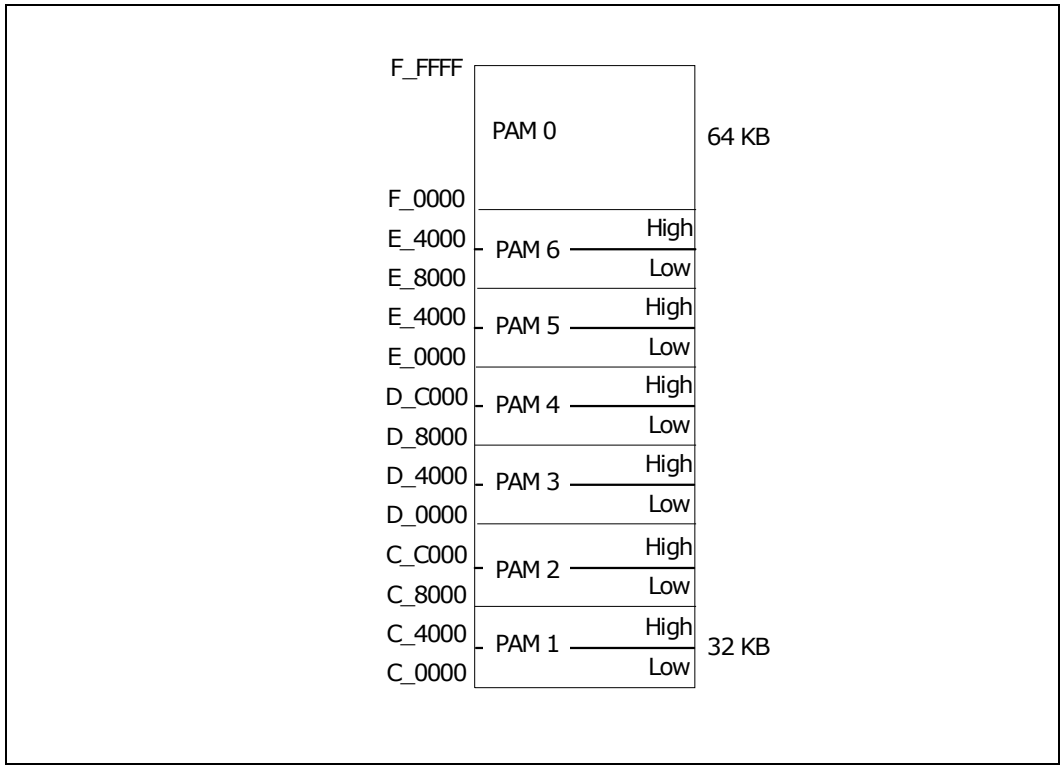
2.4.2.2 Monochrome Adapter (MDA) Range

Legacy support requires the ability to have a second graphics controller (monochrome) in the system. The monochrome adapter may be mapped to Processor Graphics (Device 2), to PCI Express (Device 1, 6), and/or to the DMI Interface.

2.4.3 Programmable Attribute Map (PAM) (C_0000h – F_FFFFh)

PAM is a legacy BIOS ROM area in MMIO. It is overlaid with DRAM and used as a faster ROM storage area. It has a fixed base address (000C_0000h) and fixed size of 256 KB. The 13 sections from 768 KB to 1 MB comprise what is also known as the PAM Memory Area. Each section has Read enable and Write enable attributes.

Figure 2-3. PAM Region Space



The PAM registers are mapped in Device 0 configuration space.

- ISA Expansion Area (C_0000h – D_FFFFh)
- Extended System BIOS Area (E_0000h – E_FFFFh)
- System BIOS Area (F_0000h – F_FFFFh)

The processor decodes the Core request, then routes to the appropriate destination (DRAM or DMI).

Snooped accesses from devices to this region are snooped on processor Caches.

Graphics translated requests to this region are not allowed. If such a mapping error occurs, the request will be routed to C_0000h. Writes will have the byte enables de-asserted.

2.5 Lower Main Memory Address Range (1 MB – TOLUD)

This address range extends from 1 MB to the top of Low Usable physical memory that is permitted to be accessible by the processor (as programmed in the TOLUD register). The processor will route all addresses within this range to the DRAM unless it falls into the optional TSEG, optional ISA Hole or optional Processor Graphics stolen memory.

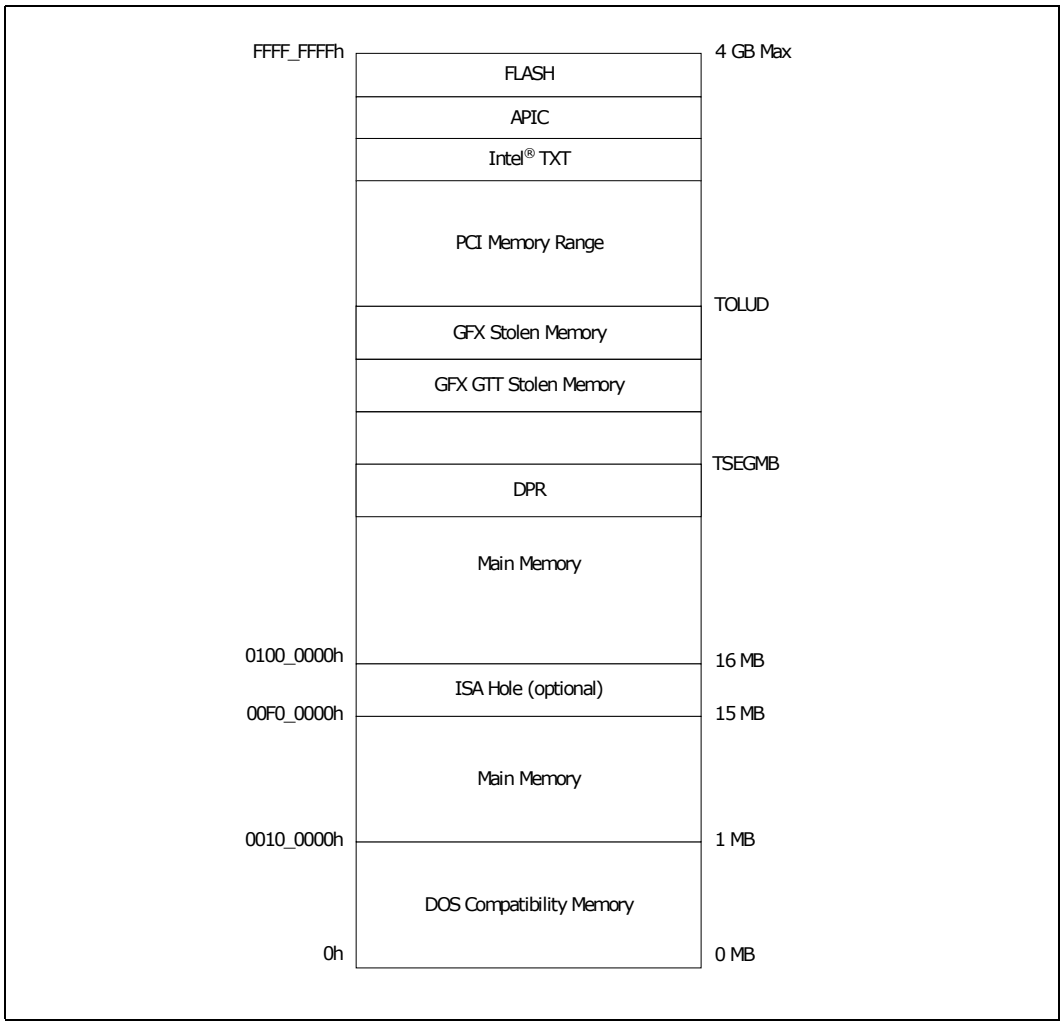
This address range is divided into two sub-ranges:

- 1 MB to TSEGMB

- TSEGMB to TOULUD

TSEGMB indicates the TSEG Memory Base address.

Figure 2-4. Main Memory Address Range



2.5.1 ISA Hole (15 MB –16 MB)

The ISA Hole (starting at address F0_0000h) is enabled in the Legacy Access Control Register in Device 0 configuration space. If no hole is created, the processor will route the request to DRAM. If a hole is created, the processor will route the request to DMI.

Graphics translated requests to the range will always route to DRAM.

2.5.2 1 MB to TSEGMB

Processor access to this range will be directed to memory with the exception of the ISA Hole (when enabled).

2.5.3 TSEG

For processor initiated transactions, the processor relies on correct programming of SMM Range Registers (SMRR) to enforce TSEG protection.

TSEG is below Processor Graphics stolen memory, which is at the Top of Low Usable physical memory (TOLUD). BIOS will calculate and program the TSEG BASE in Device 0 (TSEGMB), used to protect this region from DMA access. Calculation is:

TSEGMB = TOLUD – DSM SIZE – GSM SIZE – TSEG SIZE

SMM-mode processor accesses to TSEG always access the physical DRAM.

When the extended SMRAM space is enabled, processor accesses without SMM attribute or without write-back attribute to the TSEG range are handled as invalid accesses.

Non-processor originated accesses such as PCI Express, DMI or processor graphics to enabled SMM space are handled as invalid cycle type with reads and writes to location C_0000h and byte enables turned off for writes.

2.5.4 Protected Memory Range (PMR) - (Programmable)

For robust and secure launch of the MVMM, the MVMM code and private data need to be loaded to a memory region protected from bus Initiator accesses. Support for protected memory region is required for DMA-remapping hardware implementations on platforms supporting Intel TXT, and is optional for non-Intel TXT platforms. Since the protected memory region needs to be enabled before the MVMM is launched, hardware should support enabling of the protected memory region independently from enabling the DMA-remapping hardware.

As part of the secure launch process, the SINIT-AC module verifies the protected memory regions are properly configured and enabled. Once launched, the MVMM can setup the initial DMA-remapping structures in protected memory (to ensure they are protected while being setup) before enabling the DMA-remapping hardware units.

To optimally support platform configurations supporting varying amounts of main memory, the protected memory region is defined as two non-overlapping regions:

- **Protected Low-memory Region**: This is defined as the protected memory region below 4 GB to hold the MVMM code/private data, and the initial DMA-remapping structures that control DMA to host physical addresses below 4 GB. DMA-remapping hardware implementations on platforms supporting Intel® TXT are required to support protected low-memory region 5.
- **Protected High-memory Region**: This is defined as a variable sized protected memory region above 4 GB, enough to hold the initial DMA-remapping structures for managing DMA accesses to addresses above 4 GB. DMA-remapping hardware implementations on platforms supporting Intel® TXT are required to support protected high-memory region 6, if the platform supports main memory above 4 GB.

Once the protected low/high memory region registers are configured, bus Initiator protection to these regions is enabled through the Protected Memory Enable register. For platforms with multiple DMA-remapping hardware units, each of the DMA-remapping hardware units should be configured with the same protected memory regions and enabled.

2.5.5 DRAM Protected Range (DPR)

This protection range only applies to DMA accesses and GMADR translations. It serves a purpose of providing a memory range that is only accessible to processor streams. The range just below TSEGMB is protected from DMA accesses.

The DPR range works independently of any other range, including the PMRC checks in Intel® VT-d. It occurs post any Intel® VT-d translation. Therefore, incoming cycles are checked against this range after the Intel® VT-d translation and faulted if they hit this protected range, even if they passed the Intel® VT-d translation.

The system will set up:

- 0 to (TSEG_BASE – DPR size – 1) for DMA traffic
- TSEG_BASE to (TSEG_BASE – DPR size) as no DMA.

After some time, software could request more space for not allowing DMA. It will get some more pages and make sure there are no DMA cycles to the new region. DPR size is changed to the new value. When it does this, there should not be any DMA cycles going to DRAM to the new region.

All upstream cycles from 0 to (TSEG_BASE – 1 – DPR size), and not in the legacy holes (VGA), are decoded to DRAM.

2.5.6 Pre-allocated Memory

Voids of physical addresses that are not accessible as general system memory and reside within the system memory address range (< TOLUD) are created for SMM-mode, legacy VGA graphics compatibility, and GFX GTT stolen memory. **It is the responsibility of BIOS to properly initialize these regions**.

2.6 PCI Memory Address Range (TOLUD – 4 GB)

Top of Low Usable DRAM (TOLUD) – TOLUD is restricted to 4 GB memory (1MB granularity), but the System Agent may support up to a much higher capacity, which is limited by DRAM.

This address range from the top of low usable DRAM (TOLUD) to 4 GB is normally mapped to the DMI Interface.

Device 0 exceptions are:

1. Addresses decoded to the egress port registers (PXPEPBAR)
2. Addresses decoded to the memory mapped range for Host Memory Mapped Configuration Space registers (MCHBAR)
3. Addresses decoded to the registers associated with the PCH Serial Interconnect (DMI) register memory range. (DMIBAR)

For each PCI Express* port, there are two exceptions to this rule:

4. Addresses decoded to the PCI Express Memory Window defined by the MBASE, MLIMIT registers are mapped to PCI Express.
5. Addresses decoded to the PCI Express prefetchable Memory Window defined by the PMBASE, PMLIMIT registers are mapped to PCI Express.

In Processor Graphics configurations, there are exceptions to this rule:

6. Addresses decode to the Processor Graphics translation window (GMADR)
7. Addresses decode to the Processor Graphics translation table or Processor Graphics registers. (GTTMMADR)

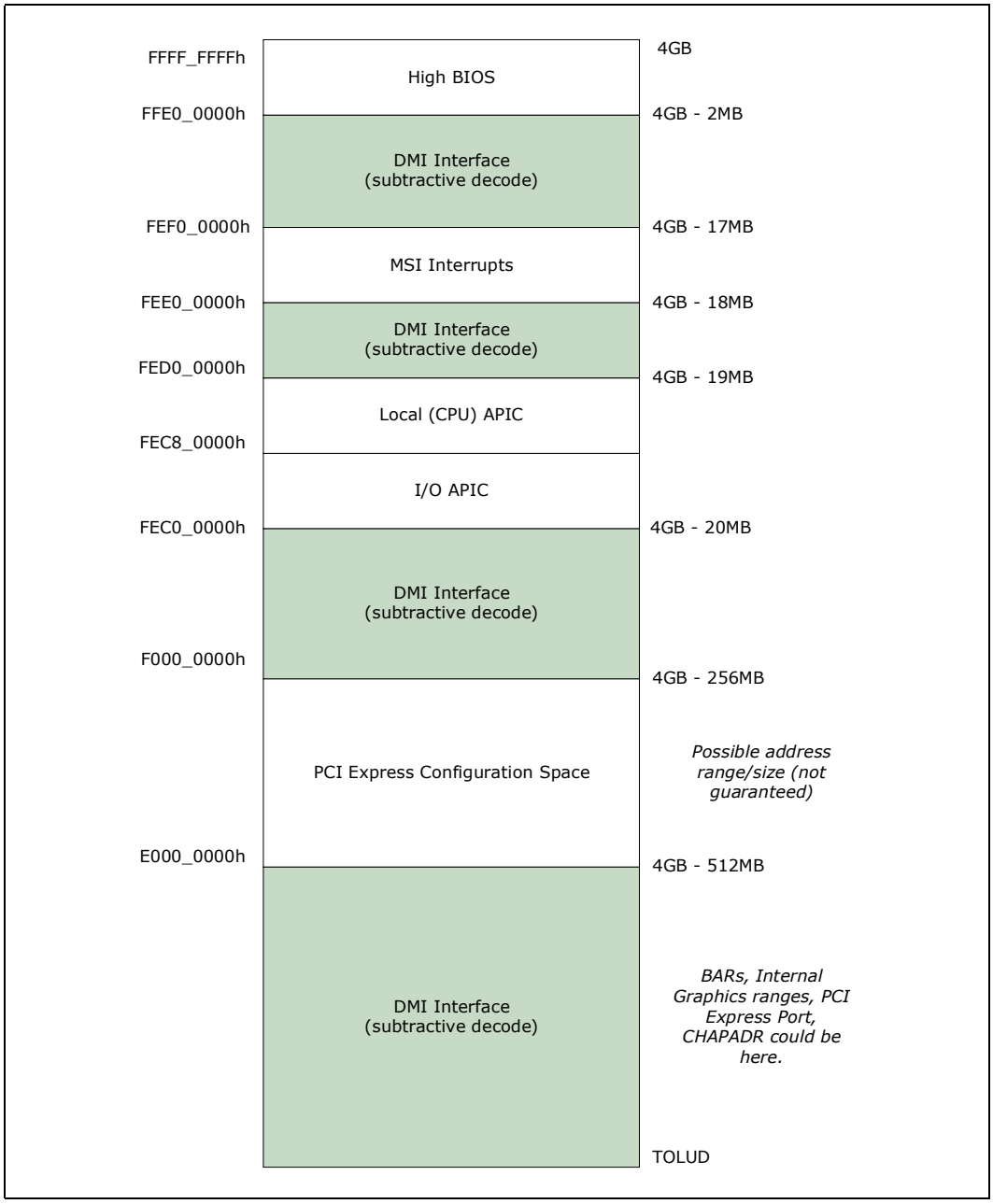
In an Intel® VT enable configuration, there are exceptions to this rule:

8. Addresses decoded to the memory mapped window to Graphics Intel® VT remap engine registers (GFXVTBAR)
9. Addresses decoded to the memory mapped window to PEG/DMI VC0 Intel® VT remap engine registers (VTDPVC0BAR)
10. TCm accesses (to Intel ME stolen memory) from PCH do not go through Intel® VT remap engines.

Some of the MMIO Bars may be mapped to this range or to the range above TOUUD.

There are sub-ranges within the PCI memory address range defined as APIC Configuration Space, MSI Interrupt Space, and High BIOS address range. The exceptions listed above for Processor Graphics and the PCI Express ports ***should NOT overlap with these ranges***.

Figure 2-5. PCI Memory Address Range



2.6.1 APIC Configuration Space (FEC0_0000h – FECF_FFFFh)

This range is reserved for APIC configuration space. The I/O APIC(s) usually reside in the PCH portion of the chipset, but may also exist as stand-alone components like PXH.

The IOAPIC spaces are used to communicate with IOAPIC interrupt controllers that may be populated in the system. Since it is difficult to relocate an interrupt controller using plug-and-play software, fixed address decode regions have been allocated for them. Processor accesses to the default IOAPIC region (FEC0_0000h to FEC7_FFFFh) are always forwarded to DMI.

The processor optionally supports additional I/O APICs behind the PCI Express* "Graphics" port. When enabled using the APIC_BASE and APIC_LIMIT registers (mapped PCI Express* Configuration space offset 240h and 244h), the PCI Express* port(s) will positively decode a subset of the APIC configuration space.

Memory requests to this range would then be forwarded to the PCI Express* port. This mode is intended for the entry Workstation/Server SKU of the PCH, and would be disabled in typical Desktop systems. When disabled, any access within the entire APIC Configuration space (FEC0_0000h to FECF_FFFFh) is forwarded to DMI.

2.6.2 HSEG (FEDA_0000h – FEDB_FFFFh)

This decode range is not supported on this processor platform.

2.6.3 MSI Interrupt Memory Space (FEE0_0000h – FEEF_FFFFh)

Any PCI Express* or DMI device may issue a Memory Write to 0FEEx_xxxxh. This Memory Write cycle does not go to DRAM. The system agent will forward this Memory Write along with the data to the processor as an Interrupt Message Transaction.

2.6.4 High BIOS Area

For security reasons, the processor will positively decode this range to DMI. This positive decode ensures any overlapping ranges will be ignored. This ensures that the boot vector and BIOS execute off the PCH.

The top 2 MB (FFE0_0000h – FFFF_FFFFh) of the PCI Memory Address Range is reserved for System BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS.

The processor begins execution from the High BIOS after reset. This region is positively decoded to DMI. The actual address space required for the BIOS is less than 2 MB. However, the minimum processor MTRR range for this region is 2 MB; thus, the full 2 MB should be considered.

2.7 Upper Main Memory Address Space (4 GB to TOUUD)

The maximum main memory size supported is 64 GB total DRAM memory.

A hole between TOLUD and 4 GB occurs when main memory size approaches 4 GB or larger. As a result, TOM and TOUUD registers and REMAPBASE/REMAPLIMIT registers become relevant.

The remap configuration registers exist to remap lost main memory space. The greater than 32-bit remap handling will be handled similar to other MCHs.

Upstream read and write accesses above 42-bit addressing will be treated as invalid cycles by PEG and DMI.

2.7.1 Top of Memory (TOM)

The "Top of Memory" (TOM) register reflects the total amount of populated physical memory. This is NOT necessarily the highest main memory address (holes may exist in main memory address map due to addresses allocated for memory mapped IO above TOM).

The TOM was used to allocate the Intel Management Engine (Intel ME) stolen memory. The Intel ME stolen size register reflects the total amount of physical memory stolen by the Intel ME. The Intel ME stolen memory is located at the top of physical memory. The Intel ME stolen memory base is calculated by subtracting the amount of memory stolen by the Intel ME from TOM.

2.7.2 Top of Upper Usable DRAM (TOUUD)

The Top of Upper Usable DRAM (TOUUD) register reflects the total amount of addressable DRAM. If remap is disabled, TOUUD will reflect TOM minus Intel ME stolen size. If remap is enabled, then it will reflect the remap limit. When there is more than 4 GB of DRAM and reclaim is enabled, the reclaim base will be the same as TOM minus Intel ME stolen memory size to the nearest 1 MB alignment.

2.7.3 Top of Low Usable DRAM (TOLUD)

TOLUD register is restricted to 4 GB memory (A[31:20]), but the processor can support up to 64 GB, limited by DRAM pins. For physical memory greater than 4 GB, the TOUUD register helps identify the address range between the 4 GB boundary and the top of physical memory. This identifies memory that can be directly accessed (including remap address calculation) that is useful for memory access indication and early path indication. TOLUD can be 1 MB aligned.

2.7.4 TSEG_BASE

The "TSEG_BASE" register reflects the total amount of low addressable DRAM, below TOLUD. BIOS will calculate memory size and program this register; thus, the system agent has knowledge of where (TOLUD) – (Gfx stolen) – (Gfx GTT stolen) – (TSEG) is located. I/O blocks use this minus DPR for upstream DRAM decode.

2.7.5 Memory Re-claim Background

The following are examples of Memory Mapped IO devices that are typically located below 4 GB:

- High BIOS
- TSEG
- GFX stolen
- GTT stolen
- XAPIC
- Local APIC
- MSI Interrupts
- Mbase/Mlimit
- Pmbase/PMlimit
- Memory Mapped IO space that supports only 32B addressing

The processor provides the capability to re-claim the physical memory overlapped by the Memory Mapped IO logical address space. The MCH re-maps physical memory from the Top of Low Memory (TOLUD) boundary up to the 4 GB boundary to an equivalent sized logical address range located just below the Intel ME stolen memory.

2.7.6 Indirect Accesses to MCHBAR Registers

Similar to prior chipsets, MCHBAR registers can be indirectly accessed using:

- Direct MCHBAR access decode:
  - Cycle to memory from processor
  - Hits MCHBAR base, AND
  - MCHBAR is enabled, AND
  - Within MMIO space (above and below 4 GB)
- GTTMMADR (10000h – 13FFFh) range -> MCHBAR decode:
  - Cycle to memory from processor, AND
  - Device 2 (Processor Graphics) is enabled, AND
  - Memory accesses for device 2 is enabled, AND
  - Targets GFX MMIO Function 0, AND
  - MCHBAR is enabled or cycle is a read. If MCHBAR is disabled, only read access is allowed.
- MCHTMBAR -> MCHBAR (Thermal Monitor)
  - Cycle to memory from processor, AND
  - Targets MCHTMBAR base
- IOBAR -> GTTMMADR -> MCHBAR.
  - Follows IOBAR rules. See GTTMMADR information above as well.

2.7.7 Memory Remapping

An incoming address (referred to as a logical address) is checked to see if it falls in the memory re-map window. The bottom of the re-map window is defined by the value in the REMAPBASE register. The top of the re-map window is defined by the value in the REMAPLIMIT register. An address that falls within this window is re-mapped to the physical memory starting at the address defined by the TOLUD register. The TOLUD register should be 1 MB aligned.

2.7.8 Hardware Remap Algorithm

The following pseudo-code defines the algorithm used to calculate the DRAM address to be used for a logical address above the top of physical memory made available using re-claiming.

```
IF (ADDRESS_IN[38:20] >= REMAP_BASE[35:20]) AND
(ADDRESS_IN[38:20] <= REMAP_LIMIT[35:20]) THEN
    ADDRESS_OUT[38:20] = (ADDRESS_IN[38:20] - REMAP_BASE[35:20]) +
0000000b & TOLUD[31:20]
    ADDRESS_OUT[19:0] = ADDRESS_IN[19:0]
```

2.8 Graphics Memory Address Ranges

The integrated memory controller can be programmed to direct memory accesses to the Processor Graphics when addresses are within any of the ranges specified using registers in MCH Device 2 configuration space.

- The Graphics Memory Aperture Base Register (GMADR) is used to access graphics memory allocated using the graphics translation table.
- The Graphics Translation Table Base Register (GTTADR) is used to access the translation table and graphics control registers. This is part of the GTTMMADR register.

These ranges can reside above the Top-of-Low-DRAM and below High BIOS and APIC address ranges. They should reside above the top of memory (TOLUD) and below 4 GB so they do not take any physical DRAM memory space.

Alternatively, these ranges can reside above 4 GB, similar to other BARs that are larger than 32 bits in size.

GMADR is a Prefetchable range in order to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

2.8.1 IOBAR Mapped Access to Device 2 MMIO Space

Device 2, Processor Graphics, contains an IOBAR register. If Device 2 is enabled, Processor Graphics registers or the GTT table can be accessed using this IOBAR. The IOBAR is composed of an index register and a data register.

MMIO_Index: MMIO_INDEX is a 32-bit register. A 32-bit (all bytes enabled) I/O write to this port loads the offset of the MMIO register or offset into the GTT that needs to be accessed. An I/O Read returns the current value of this register. I/O read/write accesses less than 32 bits in size (all bytes enabled) will not target this register.

MMIO_Data: MMIO_DATA is a 32-bit register. A 32-bit (all bytes enabled) I/O write to this port is re-directed to the MMIO register pointed to by the MMIO-index register. An I/O read to this port is re-directed to the MMIO register pointed to by the MMIO-index register. I/O read/write accesses less than 32 bits in size (all bytes enabled) will not target this register.

The result of accesses through IOBAR can be:

- Accesses directed to the GTT table. (that is, route to DRAM)
- Accesses to Processor Graphics registers with the device.
- Accesses to Processor Graphics display registers now located within the PCH. (that is, route to DMI).

Note: GTT table space writes (GTTADR) are supported through this mapping mechanism.

This mechanism to access Processor Graphics MMIO registers should NOT be used to access VGA I/O registers that are mapped through the MMIO space. VGA registers should be accessed directly through the dedicated VGA I/O ports.

2.8.2 Trusted Graphics Ranges

Trusted graphics ranges are NOT supported.

2.9 System Management Mode (SMM)

The Core handles all SMM mode transaction routing. The processor does not allow I/O devices access to the CSEG/TSEG/HSEG ranges.

DMI Interface and PCI Express* Initiators are Not allowed to access the SMM space.

Table 2-3. SMM Regions

SMM Space Enabled	Transaction Address Space	DRAM Space (DRAM)
TSEG (T)	(TOLUD – STOLEN – TSEG) to TOLUD – STOLEN	(TOLUD – STOLEN – TSEG) to TOLUD – STOLEN

2.10 SMM and VGA Access Through GTT TLB

Accesses through GTT TLB address translation SMM DRAM space are not allowed. Writes will be routed to memory address 000C_0000h with byte enables de-asserted and reads will be routed to Memory address 000C_0000h. If a GTT TLB translated address hits VGA space, an error is recorded.

PCI Express* and DMI Interface originated accesses are **never** allowed to access SMM space directly or through the GTT TLB address translation. If a GTT TLB translated address hits enabled SMM DRAM space, an error is recorded.

PCI Express and DMI Interface write accesses through the GMADR range will not be snooped. Only PCI Express and DMI assesses to GMADR linear range (defined using fence registers) are supported. PCI Express and DMI Interface tileY and tileX writes to GMADR are not supported. If, when translated, the resulting physical address is to enable SMM DRAM space, the request will be remapped to address 000C_0000h with de-asserted byte enables.

PCI Express and DMI Interface read accesses to the GMADR range are not supported. Therefore, there are no address translation concerns. PCI Express and DMI Interface reads to GMADR will be remapped to address 000C_0000h. The read will complete with UR (unsupported request) completion status.

GTT fetches are always decoded (at fetch time) to ensure fetch is not in SMM (actually, anything above base of TSEG or 640 KB - 1 MB). Thus, the fetches will be invalid and go to address 000C_0000h. This is not specific to PCI Express or DMI; it also applies to processor or Processor Graphics engines.

2.11 I/O Address Space

The system agent generates either DMI Interface or PCI Express* bus cycles for all processor I/O accesses that it does not claim. The Configuration Address Register (CONFIG_ADDRESS) and the Configuration Data Register (CONFIG_DATA) are used to generate PCI configuration space access.

The processor allows 64K+3 bytes to be addressed within the I/O space. The upper 3 locations can be accessed only during I/O address wrap-around.

A set of I/O accesses are consumed by the Processor Graphics device if it is enabled. The mechanisms for Processor Graphics I/O decode and the associated control is explained in following sub-sections.

The I/O accesses are forwarded normally to the DMI Interface bus unless they fall within the PCI Express I/O address range as defined by the mechanisms explained below. I/O writes are NOT posted. Memory writes to PCH or PCI Express are posted. The PCI Express devices have a register that can disable the routing of I/O cycles to the PCI Express device.

The processor responds to I/O cycles initiated on PCI Express or DMI with an UR status. Upstream I/O cycles and configuration cycles should never occur. If one does occur, the transaction will complete with an UR completion status.

I/O reads that lie within 8-byte boundaries but cross 4-byte boundaries are issued from the processor as one transaction. The reads will be split into two separate transactions. I/O writes that lie within 8-byte boundaries but cross 4-byte boundaries will be split into two transactions by the processor.

2.11.1 PCI Express* I/O Address Mapping

The processor can be programmed to direct non-memory (I/O) accesses to the PCI Express bus interface when processor initiated I/O cycle addresses are within the PCI Express I/O address range. This range is controlled using the I/O Base Address (IOBASE) and I/O Limit Address (IOLIMIT) registers in Device 1 Functions 0, 1, 2 configuration space.

Address decoding for this range is based on the following concept. The top 4 bits of the respective I/O Base and I/O Limit registers correspond to address bits A[15:12] of an I/O address. For the purpose of address decoding, the device assumes that the lower 12 address bits A[11:0] of the I/O base are zero and that address bits A[11:0] of the I/O limit address are FFFh. This forces the I/O address range alignment to a 4 KB boundary and produces a size granularity of 4 KB.

The processor positively decodes I/O accesses to PCI Express I/O address space as defined by the following equation:

```
I/O_Base_Address ≤ processor I/O Cycle Address ≤ I/O_Limit_Address
```

The effective size of the range is programmed by the plug-and-play configuration software and it depends on the size of I/O space claimed by the PCI Express device.

The processor also forwards accesses to the Legacy VGA I/O ranges according to the settings in the PEG configuration registers BCTRL (VGA Enable) and PCICMD (IOAE), unless a second adapter (monochrome) is present on the DMI Interface/PCI (or ISA). The presence of a second graphics adapter is determined by the MDAP configuration bit. When MDAP is set to 1, the processor will decode legacy monochrome I/O ranges and forward them to the DMI Interface. The I/O ranges decoded for the monochrome adapter are 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, and 3BFh.

The PEG I/O address range registers defined above are used for all I/O space allocation for any devices requiring such a window on PCI-Express.

The PCICMD register can disable the routing of I/O cycles to PCI Express.

2.12 Direct Media Interface (DMI) Interface Decode Rules

Note: DMI does not apply to P Processors.

All "SNOOP semantic" PCI Express* transactions are kept coherent with processor caches.

All "Snoop not required semantic" cycles reference the main DRAM address range. PCI Express non-snoop initiated cycles are not snooped.

The processor accepts accesses from the DMI Interface to the following address ranges:

- All snoop memory read and write accesses to Main DRAM including PAM region (except stolen memory ranges, TSEG, A0000h – BFFFFh space)
- Write accesses to enabled VGA range, MBASE/MLIMIT, and PMBASE/PMLIMIT will be routed as peer cycles to the PCI Express interface.
- Write accesses above the top of usable DRAM and below 4 GB (not decoding to PCI Express or GMADR space) will be treated as Initiator aborts.
- Read accesses above the top of usable DRAM and below 4 GB (not decoding to PCI Express) will be treated as unsupported requests.
- Reads and accesses above the TOUUD will be treated as unsupported requests on VC0.

DMI Interface memory read accesses that fall between TOLUD and 4 GB are considered invalid and will Initiator abort. These invalid read accesses will be reassigned to address 000C_0000h and dispatch to DRAM. Reads will return unsupported request completion. Writes targeting PCI Express space will be treated as peer-to-peer cycles.

There is a known usage model for peer writes from DMI to PEG. A video capture card can be plugged into the PCH PCI bus. The video capture card can send video capture data (writes) directly into the frame buffer on an external graphics card (writes to the PEG port). As a result, peer writes from DMI to PEG should be supported.

I/O cycles and configuration cycles are not supported in the upstream direction. The result will be an unsupported request completion status.

2.12.1 DMI Accesses to the Processor that Cross Device Boundaries

The processor does not support transactions that cross device boundaries. This should not occur because PCI Express transactions are not allowed to cross a 4 KB boundary.

For reads, the processor will provide separate completion status for each naturally-aligned 64-byte block or, if chaining is enabled, each 128-byte block. If the starting address of a transaction hits a valid address, the portion of a request that hits that target device (PCI Express or DRAM) will complete normally.

If the starting transaction address hits an invalid address, the entire transaction will be remapped to address 000C_0000h and dispatched to DRAM. A single unsupported request completion will result.

2.12.2 Traffic Class (TC) / Virtual Channel (VC) Mapping Details

- VC0 (enabled by default)
  - Snoop port and Non-snoop Asynchronous transactions are supported.
  - Internal Graphics GMADR writes can occur. These writes will NOT be snooped regardless of the snoop not required (SNR) bit.
  - Processor Graphics GMADR reads (unsupported).
  - Peer writes can occur. The SNR bit is ignored.
  - MSI can occur. These will route and be sent to the cores as Intlogical/ IntPhysical interrupts regardless of the SNR bit.
  - VLW messages can occur. These will route and be sent to the cores as VLW messages regardless of the SNR bit.
  - MCTP messages can occur. These are routed in a peer fashion.
- VC1 (Optionally enabled)
  - Supports non-snoop transactions only. (Used for isochronous traffic). The PCI Express* Egress port (PXPEPBAR) should also be programmed appropriately.
  - The snoop not required (SNR) bit should be set. Any transaction with the SNR bit not set will be treated as an unsupported request.
  - MSI and peer transactions are treated as unsupported requests.
  - No “pacer” arbitration or TWRR arbitration will occur. Never remaps to different port. (PCH takes care of Egress port remapping). The PCH meters TCm Intel ME accesses and Intel® High Definition Audio (Intel® HD Audio) TC1 access bandwidth.
  - Processor Graphics GMADR writes and GMADR reads are not supported.
- VCm accesses

— VCm access only map to Intel ME stolen DRAM. These transactions carry the direct physical DRAM address (no redirection or remapping of any kind will occur). This is how the PCH Intel ME accesses its dedicated DRAM stolen space.

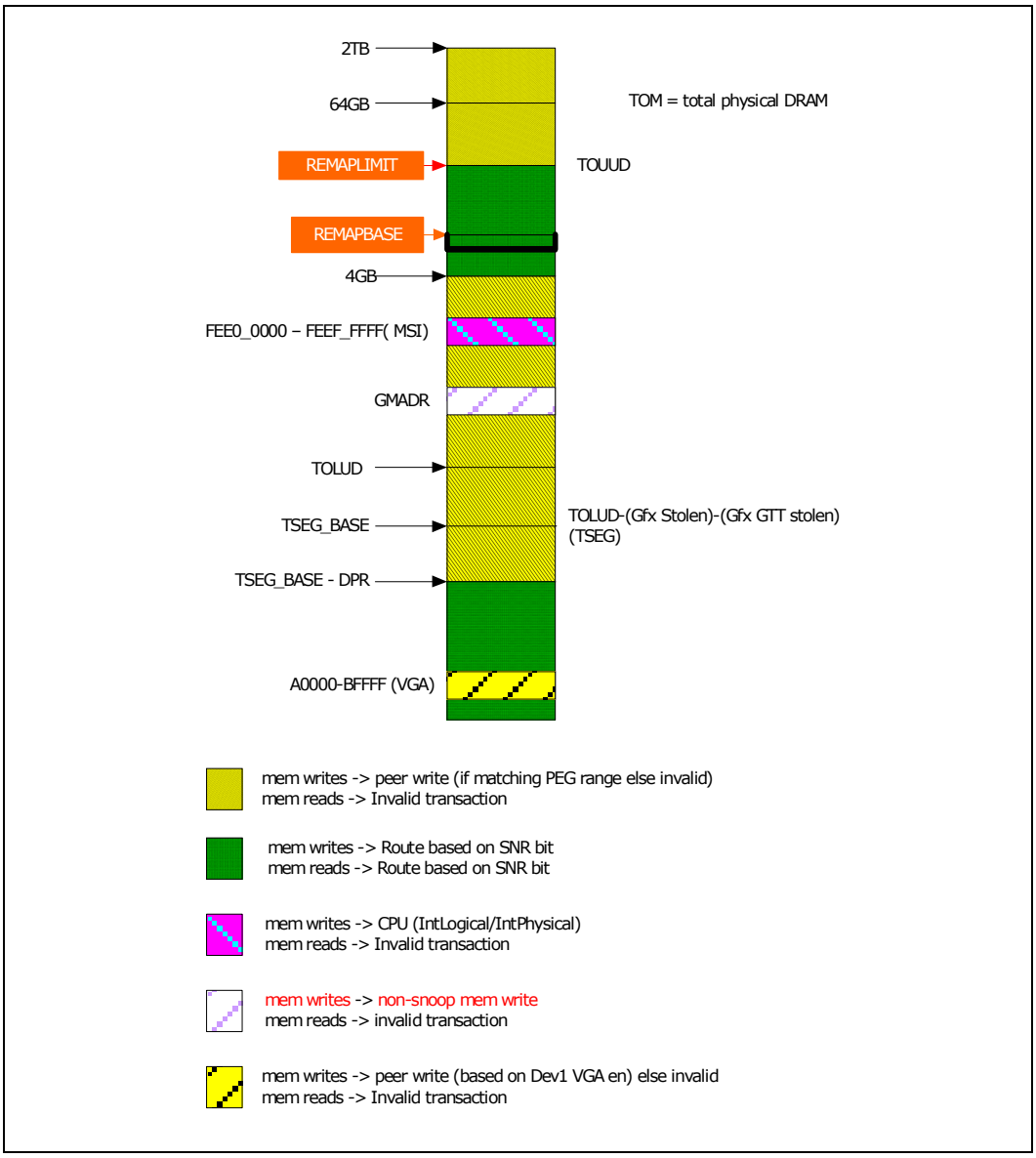
— DMI block will decode these transactions to ensure only Intel ME stolen memory is targeted, and abort otherwise.

— VCm transactions will only route non-snoop.

— VCm transactions will not go through VTd remap tables.

— The remapbase/remaplimit registers to not apply to VCm transactions.

Figure 2-6. Example: DMI Upstream VC0 Memory Map



2.13 PCI Express* Interface Decode Rules

All "SNOOP semantic" PCI Express* transactions are kept coherent with processor caches. All "Snoop not required semantic" cycles should reference the direct DRAM address range. PCI Express non-snoop initiated cycles are not snooped. If a "Snoop not required semantic" cycle is outside of the address range mapped to system memory, then it will proceed as follows:

- Reads: Sent to DRAM address 000C_0000h (non-snooped) and will return "unsuccessful completion".
- Writes: Sent to DRAM address 000C_0000h (non-snooped) with byte enables all disabled Peer writes from PEG to DMI are not supported.

If PEG bus Initiator enable is not set, all reads and writes are treated as unsupported requests.

2.13.1 TC/VC Mapping Details

- VC0 (enabled by default)

  —Snoop port and Non-snoop Asynchronous transactions are supported.

  — Processor Graphics GMADR writes can occur. Unlike FSB chipsets, these will NOT be snooped regardless of the snoop not required (SNR) bit.

  — Processor Graphics GMADR reads (unsupported).

  — Peer writes are only supported between PEG ports. PEG to DMI peer write accesses are NOT supported.

  — MSI can occur. These will route to the cores (IntLogical/IntPhysical) regardless of the SNR bit.
- VC1 is not supported.
- VCm is not supported.

2.14 Legacy VGA and I/O Range Decode Rules

The legacy 128 KB VGA memory range 000A_0000h – 000B_FFFFh can be mapped to Processor Graphics (Device 2), PCI Express (Device 1 Functions), and/or to the DMI interface depending on the programming of the VGA steering bits. Priority for VGA mapping is constant in that the processor always decodes internally mapped devices first. Internal to the processor, decode precedence is always given to Processor Graphics. The processor always positively decodes internally mapped devices, namely the Processor Graphics. Subsequent decoding of regions mapped to either PCI Express port or the DMI Interface depends on the Legacy VGA configurations bits (VGA Enable and MDAP).

For the remainder of this section, PCI Express can refer to either the device 1 port functions.

VGA range accesses will always be mapped as UC type memory.

Accesses to the VGA memory range are directed to Processor Graphics depend on the configuration. The configuration is specified by:

- Processor Graphics controller in Device 2 is enabled (DEVEN.D2EN bit 4)

- Processor Graphics VGA in Device 0 Function 0 is enabled through register GGC bit 1.
- Processor Graphics's memory accesses (PCICMD2 04h – 05h, MAE bit 1) in Device 2 configuration space are enabled.
- VGA compatibility memory accesses (VGA Miscellaneous Output register – MSR Register, bit 1) are enabled.
- Software sets the proper value for VGA Memory Map Mode register (VGA GR06 Register, bits 3:2). See the following table for translations.

Table 2-4. Processor Graphics Frame Buffer Accesses

Memory Access GR06(3:2)	A0000h - AFFFFh	B0000h - B7FFFh MDA	B8000h - BFFFFh
00	Processor Graphics	Processor Graphics	Processor Graphics
01	Processor Graphics	PCI Express bridge or DMI interface	PCI Express bridge or DMI interface
10	PCI Express bridge or DMI interface	Processor Graphics	PCI Express bridge or DMI interface
11	PCI Express bridge or DMI interface	PCI Express bridge or DMI interface	Processor Graphics

Note: Additional qualification within Processor Graphics comprehends internal MDA support. The VGA and MDA enabling bits detailed below control segments not mapped to Processor Graphics.

VGA I/O range is defined as addresses where A[15:0] are in the ranges 03B0h to 03BBh, and 03C0h to 03DFh. VGA I/O accesses are directed to Processor Graphics depends on the following configuration:

- Processor Graphics controller in Device 2 is enabled through register DEVEN.D2EN bit 4.
- Processor Graphics VGA in Device 0 Function 0 is enabled through register GGC bit 1.
- Processor Graphics's I/O accesses (PCICMD2 04 – 05h, IOAE bit 0) in Device 2 are enabled.
- VGA I/O decodes for Processor Graphics uses 16 address bits (15:0) there is no aliasing. This is different when compared to a bridge device (Device 1) that used only 10 address bits (A 9:0) for VGA I/O decode.
- VGA I/O input/output address select (VGA Miscellaneous Output register - MSR Register, bit 0) is used to select mapping of I/O access as defined in the following table.

Table 2-5. Processor Graphics VGA I/O Mapping

I/O Access MSRb0	3CX	3DX	3B0h – 3BBh	3BCh – 3BFh
0	Processor Graphics	PCI Express bridge or DMI interface	Processor Graphics	PCI Express bridge or DMI interface
1	Processor Graphics	Processor Graphics	PCI Express bridge or DMI interface	PCI Express bridge or DMI interface

Note: Additional qualification within Processor Graphics comprehends internal MDA support. The VGA and MDA enabling bits detailed below control ranges not mapped to Processor Graphics.

For regions mapped outside of the Processor Graphics (or if Processor Graphics is disabled), the legacy VGA memory range A0000h – BFFFFh are mapped to the DMI Interface or PCI Express depending on the programming of the VGA Enable bit in the BCTRL configuration register in the PEG configuration space, and the MDAPxx bits in the Legacy Access Control (LAC) register in Device 0 configuration space. The same register controls mapping VGA I/O address ranges. The VGA I/O range is defined as addresses where A[9:0] are in the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases – A[15:10] are not decoded). The function and interaction of these two bits is described below:

VGA Enable: Controls the routing of processor initiated transactions targeting VGA compatible I/O and memory address ranges. When this bit is set, the following processor accesses will be forwarded to the PCI Express:

- Memory accesses in the range 0A0000h to 0BFFFFh
- I/O addresses where A[9:0] are in the ranges 3B0h to 3BBh and 3C0h to 3DFh (including ISA address aliases – A[15:10] are not decoded)

When this bit is set to a "1":

- Forwarding of these accesses issued by the processor is independent of the I/O address and memory address ranges defined by the previously defined base and limit registers.
- Forwarding of these accesses is also independent of the settings of the ISA Enable settings if this bit is "1".
- Accesses to I/O address range x3BCh – x3BFh are forwarded to the DMI Interface.

When this bit is set to a "0":

- Accesses to I/O address range x3BCh – x3BFh are treated like any other I/O accesses; the cycles are forwarded to PCI Express if the address is within IOBASE and IOLIMIT and ISA enable bit is not set. Otherwise, these accesses are forwarded to the DMI interface.
- VGA compatible memory and I/O range accesses are not forwarded to PCI Express but rather they are mapped to the DMI Interface, unless they are mapped to PCI Express using I/O and memory range registers defined above (IOBASE, IOLIMIT)

The following table shows the behavior for all combinations of MDA and VGA.

Table 2-6. VGA and MDA IO Transaction Mapping

VGA_en	MDAP	Range	Destination	Exceptions / Notes
0	0	VGA, MDA	DMI interface	
0	1	Illegal		Undefined behavior results
1	0	VGA	PCI Express	
1	1	VGA	PCI Express	
1	1	MDA	DMI interface	x3BCh – x3BEh will also go to DMI interface

The same registers control mapping of VGA I/O address ranges. The VGA I/O range is defined as addresses where A[9:0] are in the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases – A[15:10] are not decoded). The function and interaction of these two bits is described below.

MDA Present (MDAP): This bit works with the VGA Enable bit in the BCTRL register of Device 1 to control the routing of processor-initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set when the VGA Enable bit is not set. If the VGA enable bit is set, accesses to I/O address range x3BCh – x3BFh are forwarded to the DMI Interface. If the VGA enable bit is not set, accesses to I/O address range x3BCh – x3BFh are treated just like any other I/O accesses; that is, the cycles are forwarded to PCI Express if the address is within IOBASE and IOLIMIT and the ISA enable bit is not set; otherwise, the accesses are forwarded to the DMI Interface. MDA resources are defined as the following:

Table 2-7. MDA Resources

Range Type	Address
Memory	0B0000h – 0B7FFFh
I/O	3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh (Including ISA address aliases, A[15:10] are not used in decode)

Any I/O reference that includes the I/O locations listed above, or their aliases, will be forwarded to the DMI interface even if the reference includes I/O locations not listed above.

For I/O reads that are split into multiple DWord accesses, this decode applies to each DWord independently. For example, a read to x3B3h and x3B4h (quadword read to x3B0h with BE#=E7h) will result in a DWord read from PEG at 3B0h (BE#=Eh), and a DWord read from DMI at 3B4h (BE=7h). Since the processor will not issue I/O writes crossing the DWord boundary, this case does not exist for writes.

Summary of decode priority:

- Processor Graphics VGA, if enabled, gets:
  - 03C0h – 03CFh: always
  - 03B0h – 03BBh: if MSR[0]=0 (MSR is I/O register 03C2h)
  - 03D0h – 03DFh: if MSR[0]=1

Note: 03BCh – 03BFh never decodes to Processor Graphics; 3BCh – 3BEh are parallel port I/Os, and 3BFh is only used by true MDA devices.

- Else, if MDA Present (if VGA on PEG is enabled), DMI gets:
  - x3B4,5,8,9,A,F (any access with any of these bytes enabled, regardless of the other BEs)
- Else, if VGA on PEG is enabled, PEG gets:
  - x3B0h – x3BBh
  - x3C0h – x3CFh
  - x3D0h – x3DFh
- Else, if ISA Enable=1, DMI gets:
  - upper 768 bytes of each 1K block
- Else, IOBASE/IOLIMIT apply.

2.15 I/O Mapped Registers

The processor contains two registers that reside in the processor I/O address space - the Configuration Address (CONFIG_ADDRESS) Register and the Configuration Data (CONFIG_DATA) Register. The Configuration Address Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

§ §

3 Host Bridge and DRAM Controller (D0:F0)

This chapter documents the Host Bridge and DRAM Controller.

Some of the registers in this chapter has a new nomenclature. Refer Table 1, "Updated Terminology" for more information.

Table 3-1. Summary of Host Bridge and DRAM Controller (D0:F0)

"Host Bridge/DRAM Registers (D0:F0)"
"Processor Memory Controller (MCHBAR) Registers"
"Power Management (MCHBAR) Registers"
"Host Controller (MCHBAR) Registers"
"Direct Media Interface BAR (DMIBAR) Registers"
"REGBAR Registers"
"PCI Express Egress Port BAR (PXPEPBAR) Registers"
"VTDPVC0BAR Registers"

3.1 Host Bridge/DRAM Registers (D0:F0)

Host Bridge/DRAM Controller. This section contains the registers in: Bus 0, Device 0, Function 0.

3.1.1 Summary of Registers

Table 3-2. Summary of Bus: 0, Device: 0, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	2	VID_0_0_0_PCI	8086h
2h	2	DID_0_0_0_PCI	9A00h
4h	2	PCICMD_0_0_0_PCI	0006h
6h	2	PCISTS_0_0_0_PCI	0090h
8h	1	RID_0_0_0_PCI	00h
9h	1	CC_PI_0_0_0_PCI	00h
Ah	2	CC_BCC_0_0_0_PCI	0600h
Eh	1	HDR_0_0_0_PCI	00h
2Ch	2	SVID_0_0_0_PCI	0000h
2Eh	2	SID_0_0_0_PCI	0000h
34h	1	CAPPTR_0_0_0_PCI	E0h
40h	8	PXPEPBAR PCI (PXPEPBAR_0_0_0_PCI)	0000000000000000h
48h	8	MCHBAR PCI (MCHBAR_0_0_0_PCI)	0000000000000000h
50h	2	GGC PCI (GGC_0_0_0_PCI)	0500h

Table 3-2. Summary of Bus: 0, Device: 0, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
54h	4	DEVEN PCI (DEVEN_0_0_0_PCI)	0003D4DFh
58h	4	PAVPC PCI (PAVPC_0_0_0_PCI)	00000001h
5Ch	4	DPR PCI (DPR_0_0_0_PCI)	00000000h
60h	8	PCIEXBAR PCI (PCIEXBAR_0_0_0_PCI)	0000000000000000h
68h	8	DMIBAR PCI (DMIBAR_0_0_0_PCI)	0000000000000000h
80h	1	PAM0 PCI (PAM0_0_0_0_PCI)	00h
81h	1	PAM1 PCI (PAM1_0_0_0_PCI)	00h
82h	1	PAM2 PCI (PAM2_0_0_0_PCI)	00h
83h	1	PAM3 PCI (PAM3_0_0_0_PCI)	00h
84h	1	PAM4 PCI (PAM4_0_0_0_PCI)	00h
85h	1	PAM5 PCI (PAM5_0_0_0_PCI)	00h
86h	1	PAM6 PCI (PAM6_0_0_0_PCI)	00h
87h	1	LAC PCI (LAC_0_0_0_PCI)	10h
A0h	8	TOM PCI (TOM_0_0_0_PCI)	0000007FFFF00000h
A8h	8	TOUUD PCI (TOUUD_0_0_0_PCI)	0000000000000000h
B0h	4	BDSM PCI (BDSM_0_0_0_PCI)	00000000h
B4h	4	Base of GTT Stolen Memory (BGSM_0_0_0_PCI)	00100000h
B8h	4	TSEGMB PCI (TSEGMB_0_0_0_PCI)	00000000h
BCh	4	TOLUD PCI (TOLUD_0_0_0_PCI)	00100000h
C8h	2	ERRSTS PCI (ERRSTS_0_0_0_PCI)	0000h
CAh	2	ERRCMD PCI (ERRCMD_0_0_0_PCI)	0000h
CCh	2	SMICMD PCI (SMICMD_0_0_0_PCI)	0000h
CEh	2	SCICMD PCI (SCICMD_0_0_0_PCI)	0000h
DCh	4	SKPD PCI (SKPD_0_0_0_PCI)	00000000h
E4h	4	CAPID0_A PCI (CAPID0_A_0_0_0_PCI)	00000000h
E8h	4	CAPID0_B PCI (CAPID0_B_0_0_0_PCI)	00000000h
ECh	4	CAPID0_C PCI (CAPID0_C_0_0_0_PCI)	00000000h
F0h	4	(CAPID0_E_0_0_0_PCI)	00000000h

3.1.2 VID_0_0_0_PCI — Offset 0h

This register combined with the Device Identification register uniquely identifies any PCI device.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:0, F:0] + 0h	8086h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RO	**VID:** Vendor Identification Number: PCI standard identification for Intel.

3.1.3 DID_0_0_0_PCI — Offset 2h

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:0, F:0] + 2h	9A00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	9Ah RW/Fuse	**DID_MSB:** Device Identification Number MSB: This is the upper part of device identification.
7:0	00h RW/Fuse	**DID_SKU:** Device Identification Number SKU: This is the lower part of device identification.

3.1.4 PCICMD_0_0_0_PCI — Offset 4h

Since Device #0 does not physically reside on PCI_A many of the bits are not implemented.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:0, F:0] + 4h	0006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RO	**Reserved**
9	0h RO	**FB2B:** Fast Back-to-Back Enable: This bit controls whether or not the Initiator can do fast back-to-back write. Since device 0 is strictly a target this bit is not implemented and is hardwired to 0. Writes to this bit position have no effect.
8	0h RW	**SERRE:** SERR Enable: This bit is a global enable bit for Device 0 SERR messaging. The CPU communicates the SERR condition by sending an SERR message over DMI to the PCH. 1: The CPU is enabled to generate SERR messages over DMI for specific Device 0 error conditions that are individually enabled in the ERRCMD and DMIUEMSK registers. The error status is reported in the ERRSTS, PCISTS, and DMIUEST registers. 0: The SERR message is not generated by the Host for Device 0. This bit only controls SERR messaging for Device 0. Other integrated devices have their own SERRE bits to control error reporting for error conditions occurring in each device. The control bits are used in a logical OR manner to enable the SERR DMI message mechanism. OPI N/A
7	0h RO	**ADSTEP:** Address/Data Stepping Enable: Address/data stepping is not implemented in the CPU, and this bit is hardwired to 0. Writes to this bit position have no effect.
6	0h RW	**PERRE:** OPI - N/A Parity Error Enable: Controls whether or not the Initiator Data Parity Error bit in the PCI Status register can bet set. 0: Initiator Data Parity Error bit in PCI Status register can NOT be set. 1: Initiator Data Parity Error bit in PCI Status register CAN be set.
5	0h RO	**VGASNOOP:** VGA Palette Snoop Enable: The CPU does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
4	0h RO	**MWIE:** Memory Write and Invalidate Enable: The CPU will never issue memory write and invalidate commands. This bit is therefore hardwired to 0. Writes to this bit position will have no effect.
3	0h RO	**SCE:** Special Cycle Enable: The CPU does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
2	1h RO	**BME:** Bus Initiator Enable: The CPU is always enabled as a Initiator on the backbone. This bit is hardwired to a 1. Writes to this bit position have no effect.
1	1h RO	**MAE:** Memory Access Enable: The CPU always allows access to main memory, except when such access would violate security principles. Such exceptions are outside the scope of PCI control. This bit is not implemented and is hardwired to 1. Writes to this bit position have no effect.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**IOAE:** I/O Access Enable: This bit is not implemented in the CPU and is hardwired to a 0. Writes to this bit position have no effect.

3.1.5 PCISTS_0_0_0_PCI — Offset 6h

This status register reports the occurrence of error events on Device 0s PCI interface. Since Device 0 does not physically reside on PCI_A many of the bits are not implemented.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:0, F:0] + 6h	0090h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C/V	**DPE:** Detected Parity Error: This bit is set when this Device receives a Poisoned TLP.
14	0h RW/1C/V	**SSE:** Signaled System Error: This bit is set to 1 when Device 0 generates an SERR message over DMI for any enabled Device 0 error condition. Device 0 error conditions are enabled in the PCICMD, ERRCMD, and DMIUEMSK registers. Device 0 error flags are read/reset from the PCISTS, ERRSTS, or DMIUEST registers. Software clears this bit by writing a 1 to it.
13	0h RW/1C/V	**RMAS:** Received Initiator Abort Status: This bit is set when the CPU generates a DMI request that receives an Unsupported Request completion packet. Software clears this bit by writing a 1 to it.
12	0h RW/1C/V	**RTAS:** Received Target Abort Status: This bit is set when the CPU generates a DMI request that receives a Completer Abort completion packet. Software clears this bit by writing a 1 to it.
11	0h RO	**STAS:** Signaled Target Abort Status: The CPU will not generate a Target Abort DMI completion packet or Special Cycle. This bit is not implemented and is hardwired to a 0. Writes to this bit position have no effect.
10:9	0h RO	**DEVT:** DEVSEL Timing: These bits are hardwired to 00. Writes to these bit positions have no affect. Device 0 does not physically connect to PCI_A. These bits are set to 00 (fast decode) so that optimum DEVSEL timing for PCI_A is not limited by the Host.
8	0h RW/1C/V	**DPD:** Initiator Data Parity Error Detected: This bit is set when DMI received a Poisoned completion from PCH. This bit can only be set when the Parity Error Enable bit in the PCI Command register is set.

Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**FB2B:** Fast Back-to-Back: This bit is hardwired to 1. Writes to these bit positions have no effect. Device 0 does not physically connect to PCI_A. This bit is set to 1 (indicating fast back-to-back capability) so that the optimum setting for PCI_A is not limited by the Host.
6	0h RO	**Reserved**
5	0h RO	**MC66:** 66 MHz Capable: Does not apply to PCI Express. Must be hardwired to 0.
4	1h RO	**CLIST:** Capability List: This bit is hardwired to 1 to indicate to the configuration software that this device/function implements a list of new capabilities. A list of new capabilities is accessed via register CAPPTR at configuration address offset 34h. Register CAPPTR contains an offset pointing to the start address within configuration space of this device where the Capability Identification register resides.
3:0	0h RO	**Reserved**

3.1.6 RID_0_0_0_PCI — Offset 8h

This register contains the revision number of Device #0.

These bits are read only and writes to this register have no effect.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:0, F:0] + 8h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RW/L	**RID_MSB:** Revision Identification Number MSB: Four MSB of RID
3:0	0h RW/Strap	**RID:** Revision Identification Number: Four LSB of RID

3.1.7 CC_PI_0_0_0_PCI — Offset 9h

This register (split from original CC) identifies a register-specific programming interface.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:0, F:0] + 9h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**PI:** Programming Interface: This is an 8-bit value that indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

3.1.8 CC_BCC_0_0_0_PCI — Offset Ah

This register (split from original CC) identifies the basic function of the device and a more specific sub-class.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:0, F:0] + Ah	0600h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	06h RO	**BCC:** Base Class Code: This is an 8-bit value that indicates the base class code for the Host Bridge device. This code has the value 06h, indicating a Bridge device.
7:0	00h RO	**SUBCC:** Sub-Class Code: This is an 8-bit value that indicates the category of Bridge into which the Host Bridge device falls. The code is 00h indicating a Host Bridge.

3.1.9 HDR_0_0_0_PCI — Offset Eh

This register identifies the header layout of the configuration space. No physical register exists at this location.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:0, F:0] + Eh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**HDR:** PCI Header: This field always returns 0 to indicate that the Host Bridge is a single function device with standard header layout. Reads and writes to this location have no effect.

3.1.10 SVID_0_0_0_PCI — Offset 2Ch

This value is used to identify the vendor of the subsystem.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:0, F:0] + 2Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/L	**SUBVID:** Subsystem Vendor ID: This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only. **Locked by:** TLDMIREGS.WO_STATUS0_0_0_0_DMIBAR.SUBVIDWOS

3.1.11 SID_0_0_0_PCI — Offset 2Eh

This value is used to identify a particular subsystem.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:0, F:0] + 2Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/L	**SUBID:** Subsystem ID: This field should be programmed during BIOS initialization. After it has been written once, it becomes read only. **Locked by:** TLDMIREGS.WO_STATUS0_0_0_0_DMIBAR.SUBIDWOS

3.1.12 CAPPTR_0_0_0_PCI — Offset 34h

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:0, F:0] + 34h	E0h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	E0h RO	**CAPPTR:** Capabilities Pointer: Pointer to the offset of the first capability ID register block. In this case the first capability is the product-specific Capability Identifier (CAPID0).

3.1.13 PXPEPBAR PCI (PXPEPBAR_0_0_0_PCI) — Offset 40h

This is the base address for the PCI Express Egress Port MMIO Configuration space. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the EGRESS port MMIO configuration space is disabled and must be enabled by writing a 1 to PXPEPBAREN [Dev 0, offset 40h, bit 0].

All the bits in this register are locked in Intel TXT mode.

Type	Size	Offset	Default
PCI	64 bit	[B:0, D:0, F:0] + 40h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RO	**Reserved**
41:12	00000000h RW	**PXPEPBAR:** This field corresponds to bits 41 to 12 of the base address PCI Express Egress Port MMIO configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the PCI Express Egress Port MMIO register set. All the bits in this register are locked in Intel TXT mode.
11:1	0h RO	**Reserved**
0	0h RW	**PXPEPBAREN:** 0: PXPEPBAR is disabled and does not claim any memory 1: PXPEPBAR memory mapped accesses are claimed and decoded appropriately This register is locked by Intel TXT.

3.1.14 MCHBAR PCI (MCHBAR_0_0_0_PCI) — Offset 48h

This is the base address for the Host Memory Mapped Configuration space. There is no physical memory within this 32KB window that can be addressed. The 32KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the Host MMIO Memory Mapped Configuation space is disabled and must be enabled by writing a 1 to MCHBAREN [Dev 0, offset48h, bit 0].

All the bits in this register are locked in intel TXT mode.

The register space contains memory control, initialization, timing, and buffer strength registers; clocking registers; and power and thermal management registers.

Type	Size	Offset	Default
PCI	64 bit	[B:0, D:0, F:0] + 48h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RO	**Reserved**
41:17	0000000h RW	**MCHBAR:** This field corresponds to bits 41 to 17 of the base address Host Memory Mapped configuration space. BIOS will program this register resulting in a base address for a 128KB block of contiguous memory address space. This register ensures that a naturally aligned 128KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the Host Memory Mapped register set. All the bits in this register are locked in Intel TXT mode.
16:1	0h RO	**Reserved**
0	0h RW	**MCHBAREN:** 0: MCHBAR is disabled and does not claim any memory 1: MCHBAR memory mapped accesses are claimed and decoded appropriately This register is locked in Intel TXT mode.

3.1.15 GGC PCI (GGC_0_0_0_PCI) — Offset 50h

All the bits in this register are Intel TXT lockable.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:0, F:0] + 50h	0500h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	05h RW/L	**GMS:** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. This register is also Intel TXT lockable. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0. **Locked by:** GGC_0_0_0_PCI.GGCLCK

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RW/L	**GGMS:** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register. Hardware functionality in case of programming this value to Reserved is not guaranteed. **Locked by:** GGC_0_0_0_PCI.GGCLCK
5:3	0h RO	**Reserved**
2	0h RW/L	**VAMEN:** Enables the use of the iGFX enbines for Versatile Acceleration. 1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h. **Locked by:** GGC_0_0_0_PCI.GGCLCK
1	0h RW/L	**IVD:** 0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field (bits 7:3 of this register) pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0_A[IGD] = 1) or via a register (DEVEN[3] = 0). This register is locked by Intel TXT lock. **Locked by:** GGC_0_0_0_PCI.GGCLCK
0	0h RW/L	**GGCLCK:** When set to 1b, this bit will lock all bits in this register. **Locked by:** GGC_0_0_0_PCI.GGCLCK

3.1.16 DEVEN PCI (DEVEN_0_0_0_PCI) — Offset 54h

Allows for enabling/disabling of PCI devices and functions that are within the CPU package. The table below the bit definitions describes the behavior of all combinations of transactions to devices controlled by this register. All the bits in this register are Intel TXT Lockable.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:0, F:0] + 54h	0003D4DFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW/L	**D6F1EN:** 0: Bus 0 Device 6 Function 1 is disabled and not visible. 1: Bus 0 Device 6 Function 1 is enabled and visible. This bit will be set to 0b and remain 0b if Device 6 Function 1 capability is disabled. **Locked by:** CAPID0_C_0_0_0_PCI.PEG61D
17	1h RW/L	**D10EN:** 0: Bus 0 Device 10 is disabled and not visible. 1: Bus 0 Device 10 is enabled and visible. This bit will be set to 0b and remain 0b if Device 10 capability is disabled. **Locked by:** CAPID0_B_0_0_0_PCI.DEV10_DISABLED
16	1h RW/L	**D6F2EN:** 0: Bus 0 Device 6 Function 2 is disabled and not visible. 1: Bus 0 Device 6 Function 2 is enabled and visible. This bit will be set to 0b and remain 0b if Device 6 Function 2 capability is disabled. **Locked by:** CAPID0_C_0_0_0_PCI.PEG62D
15	1h RW/L	**D8EN:** 0: Bus 0 Device 8 is disabled and not visible. 1: Bus 0 Device 8 is enabled and visible. This bit will be set to 0b and remain 0b if Device 8 capability is disabled. **Locked by:** CAPID0_B_0_0_0_PCI.GMM_DIS
14	1h RW/L	**D14F0EN:** VMD Enable - 0: Bus 0 Device 14 Function 0 is disabled and hidden. 1: Bus 0 Device 14 Function 0 is enabled and visible. **Locked by:** CAPID0_B_0_0_0_PCI.VMD_DIS
13	0h RW/L	**D6F0EN:** 0: Bus 0 Device 6 Function 0 is disabled and not visible. 1: Bus 0 Device 6 Function 0 is enabled and visible. This bit will be set to 0b and remain 0b if Device 6 Function 0 capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.PEG60D
12	1h RW/L	**D9EN:** 0: Bus 0 Device 9 is disabled and not visible. 1: Bus 0 Device 9 is enabled and visible. This bit will be set to 0b and remain 0b if Device 9 capability is disabled. **Locked by:** CAPID0_B_0_0_0_PCI.NPK_DIS
11	0h RO	**Reserved**
10	1h RW/L	**D5EN:** 0: Bus 0 Device 5 is disabled and not visible. 1: Bus 0 Device 5 is enabled and visible. This bit will be set to 0b and remain 0b if Device 5 capability is disabled. **Locked by:** CAPID0_B_0_0_0_PCI.IMGU_DIS
9:8	0h RO	**Reserved**
7	1h RW/L	**D4EN:** 0: Bus 0 Device 4 is disabled and not visible. 1: Bus 0 Device 4 is enabled and visible. This bit will be set to 0b and remain 0b if Device 4 capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.CDD

Bit Range	Default & Access	Field Name (ID): Description
6	1h RW/L	**D3F7EN:** NVMe - Device 3 function 7 enable 0: Bus 0 Device 3 function 7 is disabled and hidden 1: Bus 0 Device 3 function 7 is enabled and visible This bit will be set to 0b and remain 0b if Device 3 capability is disabled. Locked with CAPID0_A_0_0_0_PCI[0].NVME_F7D **Locked by:** CAPID0_A_0_0_0_PCI.NVME_F7D
5	0h RW/L	**D3F0EN:** NVMe - Device 3 function 0 enable 0: Bus 0 Device 3 function 0 is disabled and hidden 1: Bus 0 Device 3 function 0 is enabled and visible This bit will be set to 0b and remain 0b if Device 3 capability is disabled. Locked with CAPID0_A_0_0_0_PCI[31].NVME_F0D **Locked by:** CAPID0_A_0_0_0_PCI.NVME_F0D
4	1h RW/L	**D2EN:** 0: Bus 0 Device 2 is disabled and hidden 1: Bus 0 Device 2 is enabled and visible This bit will be set to 0b and remain 0b if Device 2 capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.IGD
3	1h RW/L	**D1F0EN:** 0: Bus 0 Device 1 Function 0 is disabled and hidden. 1: Bus 0 Device 1 Function 0 is enabled and visible. This bit will be set to 0b and remain 0b if PEG10 capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.PEG10D
2	1h RW/L	**D1F1EN:** 0: Bus 0 Device 1 Function 1 is disabled and hidden. 1: Bus 0 Device 1 Function 1 is enabled and visible. This bit will be set to 0b and remain 0b if: - PEG11 capability is disabled by fuses, OR - PEG11 is disabled by strap (PEG0CFGSEL) **Locked by:** CAPID0_A_0_0_0_PCI.PEG11D
1	1h RW/L	**D1F2EN:** 0: Bus 0 Device 1 Function 2 is disabled and hidden. 1: Bus 0 Device 1 Function 2 is enabled and visible. This bit will be set to 0b and remain 0b if: - PEG12 capability is disabled by fuses, OR - PEG12 is disabled by strap (PEG0CFGSEL) **Locked by:** CAPID0_A_0_0_0_PCI.PEG12D
0	1h RO	**D0EN:** Bus 0 Device 0 Function 0 may not be disabled and is therefore hardwired to 1.

3.1.17 PAVPC PCI (PAVPC_0_0_0_PCI) — Offset 58h

All the bits in this register are locked by Intel TXT. When locked the R/W bits are RO.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:0, F:0] + 58h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/L	**PCMBASE:** Sizes supported: 1M, 2M, 4M and 8M. Base value programmed (from Top of Stolen Memory) itself defines the size of the WOPCM. Separate WOPCM size programming is redundant information and not required. Default 1M size programming. 4M recommended. This register is locked (becomes read-only) when PAVPE = 1b. **Locked by:** PAVPC_0_0_0_PCI.PAVPLCK
19:7	0h RO	**Reserved**
6	0h RW/L	**ASMFEN:** ASMF method enabled 0b Disabled (default). 1b Enabled. This register is locked when PAVPLCK is set. **Locked by:** PAVPC_0_0_0_PCI.PAVPLCK
5	0h RO	**Reserved**
4	0h RW/L	**OVTATTACK:** Override of Unsolicited Connection State Attack and Terminate. 0: Disable Override. Attack Terminate allowed. 1: Enable Override. Attack Terminate disallowed. This register bit is locked when PAVPE is set. **Locked by:** PAVPC_0_0_0_PCI.PAVPLCK
3	0h RW/L	**HVYMODSEL:** This bit is applicable only for PAVP2 operation mode with also set, or for PAVP3 mode only if the per-App memory config is disabled due to the clearing of an additional 9 in the Crypto Function Control_1 register (address 0x320F0). 0: Lite Mode (Non-Serpent mode) 1: Serpent Mode To enabled PAVP3 mode, this one type boot time programming has been replaced by per-App programming (through the Media Crypto Copy command). Note that PAVP2 or PAVP3 mode selection is done by programming bit 8 of the MFX_MODE - Video Mode register. **Locked by:** PAVPC_0_0_0_PCI.PAVPLCK
2	0h RW/L	**PAVPLCK:** This bit locks all writeable contents in this register when set (including itself). Only a hardware reset can unlock the register again. This lock bit needs to be set only if PAVP is enabled (bit 1 of this register is asserted). **Locked by:** PAVPC_0_0_0_PCI.PAVPLCK

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW/L	**PAVPE:** 0: PAVP functionality is disabled. 1: PAVP functionality is enabled. This register is locked when PAVPLCK is set. **Locked by:** PAVPC_0_0_0_PCI.PAVPLCK
0	1h RW/L	**PCME:** This field enables Protected Content Memory within Graphics Stolen Memory. This memory is the same as the WOPCM area, whose size is defined by bit 5 of this register. This register is locked when PAVPLOCK is set. A value of 0 in this field indicates that Protected Content Memory is disabled, and cannot be programmed in this manner when PAVP is enabled. A value of 1 in this field indicates that Protected Content Memory is enabled, and is the only programming option available when PAVP is enabled. (Note that the legacy Lite mode programming of PCME bit = 0 is not supported. For non-PAVP3 Mode, even for Lite mode configuration, this bit should be programmed to 1 and HVYMODESEL = 0). This bit should always be programmed to 1 if bits 1 and 2 (PAVPE and PAVP lock bits) are both set. With per-App Memory configuration support, the range check for the WOPCM memory area should always happen when this bit is set, regardless of Lite or Serpent mode, or PAVP2 or PAVP3 mode programming. **Locked by:** PAVPC_0_0_0_PCI.PAVPLCK

3.1.18 DPR PCI (DPR_0_0_0_PCI) — Offset 5Ch

DMA protected range register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:0, F:0] + 5Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/V/L	**TOPOFDPR:** Top address + 1 of DPR. This is the base of TSEG. Bits 19:0 of the BASE reported here are 0x0_0000.
19:12	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
11:4	00h RW/L	**DPRSIZE:** This is the size of memory, in MB, that will be protected from DMA accesses. A value of 0x00 in this field means no additional memory is protected. The maximum amount of memory that will be protected is 255 MB. The amount of memory reported in this field will be protected from all DMA accesses, including translated CPU accesses and graphics. The top of the protected range is the BASE of TSEG -1. Note: If TSEG is not enabled, then the top of this range becomes the base of stolen graphics, or ME stolen space or TOLUD, whichever would have been the location of TSEG, assuming it had been enabled. The DPR range works independently of any other range, including the NoDMA.TABLE protection or the PMRC checks in VTd, and is done post any VTd translation or Intel TXT NoDMA lookup. Therefore incoming cycles are checked against this range after the VTd translation and faulted if they hit this protected range, even if they passed the VTd translation or were clean in the NoDMA lookup. All the memory checks are ORed with respect to NOT being allowed to go to memory. So if either PMRC, DPR, NoDMA table lookup, NoDMA.TABLE.PROTECT OR a VTd translation disallows the cycle, then the cycle is not allowed to go to memory. Or in other words, all the above checks must pass before a cycle is allowed to DRAM. **Locked by:** DPR_0_0_0_PCI.LOCK
3	0h RO	**Reserved**
2	0h RW/L	**EPM:** This field controls DMA accesses to the DMA Protected Range (DPR) region. 0: DPR is disabled 1: DPR is enabled. All DMA requests accessing DPR region are blocked. HW reports the status of DPR enable/disable through the PRS field in this register. When this bit change, one must have to wait till status (prs) has updated before changing it again. **Locked by:** DPR_0_0_0_PCI.LOCK
1	0h RW/V/L	**PRS:** This field indicates the status of DPR. 0: DPR protection disabled 1: DPR protection enabled
0	0h RW/L	**LOCK:** All bits which may be updated by SW in this register are locked down when this bit is set. **Locked by:** DPR_0_0_0_PCI.LOCK

3.1.19 PCIEXBAR PCI (PCIEXBAR_0_0_0_PCI) — Offset 60h

This register define the PCIEXBAR.

Type	Size	Offset	Default
PCI	64 bit	[B:0, D:0, F:0] + 60h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RO	**Reserved**
41:31	000h RW	**PCIEXBAR:** This field corresponds to bits 41 to 32 of the base address for PCI Express enhanced configuration space including bus segments. BIOS will program this register resulting in a base address for a contiguous memory address space. The size of the range is defined by bits [3:1] of this register. This Base address shall be assigned on a boundary consistent with the number of buses (defined by the Length field in this register) above TOLUD and still within the 39-bit addressable memory space. The address bits decoded depend on the length of the region defined by this register. The address used to access the PCI Express configuration space for a specific device can be determined as follows: PCI Express Base Address +Segment Number*256MB+ Bus Number * 1MB + Device Number * 32KB + Function Number * 4KB This address is the beginning of the 4KB space that contains both the PCI compatible configuration space and the PCI Express extended configuration space.
30	0h RW/V	**ADMSK1024:** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits [3:1] in this register.
29	0h RW/V	**ADMSK512:** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits [3:1] in this register.
28	0h RW/V	**ADMSK256:** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits [3:1] in this register.
27	0h RW/V	**ADMSK128:** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits [3:1] in this register.
26	0h RW/V	**ADMSK64:** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits [3:1] in this register.
25:4	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
3:1	0h RW	**LENGTH:** This field describes the length of this region. 000: 256MB (buses 0-255). Bits 38:28 are decoded in the PCI Express Base Address Field. 001: 128MB (buses 0-127). Bits 38:27 are decoded in the PCI Express Base Address Field. 010: 64MB (buses 0-63). Bits 38:26 are decoded in the PCI Express Base Address Field. 011: 512MB (buses 0-512). Bits 38:29 are decoded in the PCI Express Base Address Field. 100: 1024MB (buses 0-1024). Bits 38:30 are decoded in the PCI Express Base Address Field. 101: 2048MB (buses 0-2048). Bits 38:31 are decoded in the PCI Express Base Address Field. 110: 4096MB (buses 0-4096). Bits 38:32 are decoded in the PCI Express Base Address Field. 111:Rreserved.
0	0h RW	**PCIEXBAREN:** PCIEX BAR Enable

3.1.20 DMIBAR PCI (DMIBAR_0_0_0_PCI) — Offset 68h

This is the base address for the Root Complex configuration space. This window of addresses contains the Root Complex Register set for the PCI Express Hierarchy associated with the Host Bridge. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the Root Complex configuration space is disabled and must be enabled by writing a 1 to DMIBAREN [Dev 0, offset 68h, bit 0] All the bits in this register are locked in Intel TXT mode.

Type	Size	Offset	Default
PCI	64 bit	[B:0, D:0, F:0] + 68h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RO	**Reserved**
41:12	00000000h RW	**DMIBAR:** This field corresponds to bits 41 to 12 of the base address DMI configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the DMI register set. All the Bits in this register are locked in Intel TXT mode.
11:1	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**DMIBAREN:** 0: DMIBAR is disabled and does not claim any memory 1: DMIBAR memory mapped accesses are claimed and decoded appropriately This register is locked by Intel TXT.

3.1.21 PAM0 PCI (PAM0_0_0_0_PCI) — Offset 80h

This register controls the read, write and shadowing attributes of the BIOS range from F_0000h to F_FFFFh. The Uncore allows programmable memory attributes on 13 legacy memory segments of various sizes in the 768KB to 1MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cacheability of these areas is controlled via the MTRR register in the core.

Two bits are used to specify memory attributes for each memory segment. These bits apply to host accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE=1, the host read accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when RE=0, the host read accesses are directed to DMI.

WE - Write Enable. When WE=1, the host write accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when WE=0, the host read accesses are directed to DMI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write or Disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:0, F:0] + 80h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5:4	0h RW/L	**HIENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0F_0000h to 0F_FFFFh. 00: DRAM Disabled. All accesses are directed to DMI. 01: Read Only. All reads are sent to DRAM, all writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM, all reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK
3:1	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/L	**LOCK:** If this bit is set, all of the PAM* registers are locked (cannot be written) **Locked by:** PAM0_0_0_PCI.LOCK

3.1.22 PAM1 PCI (PAM1_0_0_PCI) — Offset 81h

This register controls the read, write and shadowing attributes of the BIOS range from C_0000h to C_7FFFh. The Uncore allows programmable memory attributes on 13 legacy memory segments of various sizes in the 768KB to 1MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cacheability of these areas is controlled via the MTRR register in the core.

Two bits are used to specify memory attributes for each memory segment. These bits apply to host accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE=1, the host read accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when RE=0, the host read accesses are directed to DMI.

WE - Write Enable. When WE=1, the host write accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when WE=0, the host read accesses are directed to DMI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write or Disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:0, F:0] + 81h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5:4	0h RW/L	**HIENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0C_4000h to 0C_7FFFh. 00: DRAM Disabled. All accesses are directed to DMI. 01: Read Only. All reads are sent to DRAM, all writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM, all reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_PCI.LOCK
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW/L	**LOENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0C0000h to 0C3FFFh. 00: DRAM Disabled. All reads are sent to DRAM. All writes are forwarded to DMI. 01: Read Only. All reads are sent to DRAM. All writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM. All reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK

3.1.23 PAM2 PCI (PAM2_0_0_0_PCI) — Offset 82h

This register controls the read, write and shadowing attributes of the BIOS range from C_8000h to C_FFFFh. The Uncore allows programmable memory attributes on 13 legacy memory segments of various sizes in the 768KB to 1MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cacheability of these areas is controlled via the MTRR register in the core.

Two bits are used to specify memory attributes for each memory segment. These bits apply to host accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE=1, the host read accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when RE=0, the host read accesses are directed to DMI.

WE - Write Enable. When WE=1, the host write accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when WE=0, the host read accesses are directed to DMI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write or Disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:0, F:0] + 82h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW/L	**HIENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0CC000h to 0CFFFFh. 00: DRAM Disabled. All accesses are directed to DMI. 01: Read Only. All reads are sent to DRAM, all writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM, all reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK
3:2	0h RO	**Reserved**
1:0	0h RW/L	**LOENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0C8000h to 0CBFFFh. 00: DRAM Disabled. All reads are sent to DRAM. All writes are forwarded to DMI. 01: Read Only. All reads are sent to DRAM. All writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM. All reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK

3.1.24 PAM3 PCI (PAM3_0_0_0_PCI) — Offset 83h

This register controls the read, write and shadowing attributes of the BIOS range from D0000h to D7FFFh. The Uncore allows programmable memory attributes on 13 legacy memory segments of various sizes in the 768KB to 1MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cacheability of these areas is controlled via the MTRR register in the core.

Two bits are used to specify memory attributes for each memory segment. These bits apply to host accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE=1, the host read accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when RE=0, the host read accesses are directed to DMI.

WE - Write Enable. When WE=1, the host write accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when WE=0, the host read accesses are directed to DMI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write or Disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:0, F:0] + 83h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5:4	0h RW/L	**HIENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0D4000h to 0D7FFFh. 00: DRAM Disabled. All accesses are directed to DMI. 01: Read Only. All reads are sent to DRAM, all writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM, all reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK
3:2	0h RO	**Reserved**
1:0	0h RW/L	**LOENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0D0000h to 0D3FFFh. 00: DRAM Disabled. All reads are sent to DRAM. All writes are forwarded to DMI. 01: Read Only. All reads are sent to DRAM. All writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM. All reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK

3.1.25 PAM4 PCI (PAM4_0_0_0_PCI) — Offset 84h

This register controls the read, write and shadowing attributes of the BIOS range from D8000h to DFFFFh. The Uncore allows programmable memory attributes on 13 legacy memory segments of various sizes in the 768KB to 1MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cacheability of these areas is controlled via the MTRR register in the core.

Two bits are used to specify memory attributes for each memory segment. These bits apply to host accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE=1, the host read accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when RE=0, the host read accesses are directed to DMI.

WE - Write Enable. When WE=1, the host write accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when WE=0, the host read accesses are directed to DMI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write or Disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:0, F:0] + 84h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5:4	0h RW/L	**HIENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0DC000h to 0DFFFFh. 00: DRAM Disabled. All accesses are directed to DMI. 01: Read Only. All reads are sent to DRAM, all writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM, all reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK
3:2	0h RO	**Reserved**
1:0	0h RW/L	**LOENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0D8000h to 0DBFFFh. 00: DRAM Disabled. All accesses are directed to DMI. 01: Read Only. All reads are sent to DRAM. All writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM. All reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK

3.1.26 PAM5 PCI (PAM5_0_0_0_PCI) — Offset 85h

This register controls the read, write and shadowing attributes of the BIOS range from E_0000h to E_7FFFh. The Uncore allows programmable memory attributes on 13 legacy memory segments of various sizes in the 768KB to 1MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cacheability of these areas is controlled via the MTRR register in the core.

Two bits are used to specify memory attributes for each memory segment. These bits apply to host accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE=1, the host read accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when RE=0, the host read accesses are directed to DMI.

WE - Write Enable. When WE=1, the host write accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when WE=0, the host read accesses are directed to DMI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write or Disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:0, F:0] + 85h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5:4	0h RW/L	**HIENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0E4000h to 0E7FFFh. 00: DRAM Disabled. All accesses are directed to DMI. 01: Read Only. All reads are sent to DRAM, all writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM, all reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK
3:2	0h RO	**Reserved**
1:0	0h RW/L	**LOENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0E0000h to 0E3FFFh. 00: DRAM Disabled. All reads are sent to DRAM. All writes are forwarded to DMI. 01: Read Only. All reads are sent to DRAM. All writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM. All reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK

3.1.27 PAM6 PCI (PAM6_0_0_0_PCI) — Offset 86h

This register controls the read, write and shadowing attributes of the BIOS range from E_8000h to E_FFFFh. The Uncore allows programmable memory attributes on 13 legacy memory segments of various sizes in the 768KB to 1MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cacheability of these areas is controlled via the MTRR register in the core.

Two bits are used to specify memory attributes for each memory segment. These bits apply to host accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE=1, the host read accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when RE=0, the host read accesses are directed to DMI.

WE - Write Enable. When WE=1, the host write accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when WE=0, the host read accesses are directed to DMI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write or Disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:0, F:0] + 86h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5:4	0h RW/L	**HIENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0EC000h to 0EFFFFh. 00: DRAM Disabled. All accesses are directed to DMI. 01: Read Only. All reads are sent to DRAM, all writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM, all reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK
3:2	0h RO	**Reserved**
1:0	0h RW/L	**LOENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0E8000h to 0EBFFFh. 00: DRAM Disabled. All reads are sent to DRAM. All writes are forwarded to DMI. 01: Read Only. All reads are sent to DRAM. All writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM. All reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK

3.1.28 LAC PCI (LAC_0_0_0_PCI) — Offset 87h

This 8-bit register controls steering of MDA cycles and a fixed DRAM hole from 15-16MB.

There can only be at most one MDA device in the system.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:0, F:0] + 87h	10h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**HEN:** This field enables a memory hole in DRAM space. The DRAM that lies behind this space is not remapped. 0: No memory hole. 1: Memory hole from 15MB to 16MB. This bit is Intel TXT lockable.
6:5	0h RO	**Reserved**
4	1h RW	**MDAPCIE:** This bit works with the VGA Enable bits in the BCTRL register of Non PEG devices to control the routing of CPU initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should be set to 1 by default. It is assumed that these devices will not need to support legacy MDA graphics. However this single bit is added just to support this rare case of using MDA over these devices. The behavior of this bit field is identical to bits [3:0]
3	0h RW	**MDAP60:** This bit works with the VGA Enable bits in the BCTRL register of Device 1 Function 2 to control the routing of CPU initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if device 1 function 2 VGA Enable bit is not set. If device 1 function 2 VGA enable bit is not set, then accesses to IO address range x3BCh-x3BFh remain on the backbone. If the VGA enable bit is set and MDA is not present, then accesses to IO address range x3BCh-x3BFh are forwarded to PCI Express through device 1 function 2 if the address is within the corresponding IOBASE and IOLIMIT, otherwise they remain on the backbone. MDA resources are defined as the following: Memory: 0B0000h - 0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will remain on the backbone even if the reference also includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: VGAEN MDAP Description 0 0 All References to MDA and VGA space are not claimed by Device 1 Function 2. 0 1 Illegal combination 1 0 All VGA and MDA references are routed to PCI Express Graphics Attach device 1 function 2. 1 1 All VGA references are routed to PCI Express Graphics Attach device 1 function 2. MDA references are not claimed by device 1 function 2. VGA and MDA memory cycles can only be routed across PEG12 when MAE (PCICMD12[1]) is set. VGA and MDA I/O cycles can only be routed across PEG12 if IOAE (PCICMD12[0]) is set.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**MDAP12:** This bit works with the VGA Enable bits in the BCTRL register of Device 1 Function 2 to control the routing of CPU initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if device 1 function 2 VGA Enable bit is not set. If device 1 function 2 VGA enable bit is not set, then accesses to IO address range x3BCh-x3BFh remain on the backbone. If the VGA enable bit is set and MDA is not present, then accesses to IO address range x3BCh-x3BFh are forwarded to PCI Express through device 1 function 2 if the address is within the corresponding IOBASE and IOLIMIT, otherwise they remain on the backbone. MDA resources are defined as the following: Memory: 0B0000h - 0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will remain on the backbone even if the reference also includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: VGAEN MDAP Description 0 0 All References to MDA and VGA space are not claimed by Device 1 Function 2. 0 1 Illegal combination 1 0 All VGA and MDA references are routed to PCI Express Graphics Attach device 1 function 2. 1 1 All VGA references are routed to PCI Express Graphics Attach device 1 function 2. MDA references are not claimed by device 1 function 2. VGA and MDA memory cycles can only be routed across PEG12 when MAE (PCICMD12[1]) is set. VGA and MDA I/O cycles can only be routed across PEG12 if IOAE (PCICMD12[0]) is set.
1	0h RW	**MDAP11:** This bit works with the VGA Enable bits in the BCTRL register of Device 1 Function 1 to control the routing of CPU initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if device 1 function 1 VGA Enable bit is not set. If device 1 function 1 VGA enable bit is not set, then accesses to IO address range x3BCh-x3BFh remain on the backbone. If the VGA enable bit is set and MDA is not present, then accesses to IO address range x3BCh-x3BFh are forwarded to PCI Express through device 1 function 1 if the address is within the corresponding IOBASE and IOLIMIT, otherwise they remain on the backbone. MDA resources are defined as the following: Memory: 0B0000h - 0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will remain on the backbone even if the reference also includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: VGAEN MDAP Description 0 0 All References to MDA and VGA space are not claimed by Device 1 Function 1. 0 1 Illegal combination 1 0 All VGA and MDA references are routed to PCI Express Graphics Attach device 1 function 1. 1 1 All VGA references are routed to PCI Express Graphics Attach device 1 function 1. MDA references are not claimed by device 1 function 1. VGA and MDA memory cycles can only be routed across PEG11 when MAE (PCICMD11[1]) is set. VGA and MDA I/O cycles can only be routed across PEG11 if IOAE (PCICMD11[0]) is set.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**MDAP10:** This bit works with the VGA Enable bits in the BCTRL register of Device 1 Function 0 to control the routing of CPU initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if device 1 function 0 VGA Enable bit is not set. If device 1 function 0 VGA enable bit is not set, then accesses to IO address range x3BCh-x3BFh remain on the backbone. If the VGA enable bit is set and MDA is not present, then accesses to IO address range x3BCh-x3BFh are forwarded to PCI Express through device 1 function 0 if the address is within the corresponding IOBASE and IOLIMIT, otherwise they remain on the backbone. MDA resources are defined as the following: Memory: 0B0000h - 0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will remain on the backbone even if the reference also includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: VGAEN MDAP Description 0 0 All References to MDA and VGA space are not claimed by Device 1 Function 0. 0 1 Illegal combination 1 0 All VGA and MDA references are routed to PCI Express Graphics Attach device 1 function 0. 1 1 All VGA references are routed to PCI Express Graphics Attach device 1 function 0. MDA references are not claimed by device 1 function 0. VGA and MDA memory cycles can only be routed across PEG10 when MAE (PCICMD10[1]) is set. VGA and MDA I/O cycles can only be routed across PEG10 if IOAE (PCICMD10[0]) is set.

3.1.29 TOM PCI (TOM_0_0_0_PCI) — Offset A0h

This Register contains the size of physical memory. BIOS determines the memory size reported to the OS using this Register.

Type	Size	Offset	Default
PCI	64 bit	[B:0, D:0, F:0] + A0h	0000007FFFF00000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RO	**Reserved**
41:20	07FFFFh RW/L	**TOM:** This register reflects the total amount of populated physical memory. This is NOT necessarily the highest main memory address (holes may exist in main memory address map due to addresses allocated for memory mapped IO). These bits correspond to address bits 41:20 (1MB granularity). Bits 19:0 are assumed to be 0. All the bits in this register are locked in Intel TXT mode. **Locked by:** TOM_0_0_0_PCI.LOCK

Bit Range	Default & Access	Field Name (ID): Description
19:1	0h RO	**Reserved**
0	0h RW/L	**LOCK:** This bit will lock all writeable settings in this register, including itself. **Locked by:** TOM_0_0_0_PCI.LOCK

3.1.30 TOUUD PCI (TOUUD_0_0_0_PCI) — Offset A8h

This 64 bit register defines the Top of Upper Usable DRAM.

Configuration software must set this value to TOM minus all ME stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to reclaim limit + 1byte, 1MB aligned, since reclaim limit is 1MB aligned. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than or equal to 4GB.

BIOS Restriction: Minimum value for TOUUD is 4GB.

These bits are Intel TXT lockable.

Type	Size	Offset	Default
PCI	64 bit	[B:0, D:0, F:0] + A8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RO	**Reserved**
41:20	000000h RW/L	**TOUUD:** This register contains bits 41 to 20 of an address one byte above the maximum DRAM memory above 4G that is usable by the operating system. Configuration software must set this value to TOM minus all ME stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to reclaim limit 1MB aligned since reclaim limit + 1byte is 1MB aligned. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than 4GB. All the bits in this register are locked in Intel TXT mode. **Locked by:** TOUUD_0_0_0_PCI.LOCK
19:1	0h RO	**Reserved**
0	0h RW/L	**LOCK:** This bit will lock all writeable settings in this register, including itself. **Locked by:** TOUUD_0_0_0_PCI.LOCK

3.1.31 BDSM PCI (BDSM_0_0_0_PCI) — Offset B0h

This register contains the base address of graphics data stolen DRAM memory. BIOS determines the base of graphics data stolen memory by subtracting the graphics data stolen memory size (PCI Device 0 offset 52 bits 7:4) from TOLUD (PCI Device 0 offset BC bits 31:20).

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:0, F:0] + B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/L	**BDSM:** This register contains bits 31 to 20 of the base address of stolen DRAM memory. BIOS determines the base of graphics stolen memory by subtracting the graphics stolen memory size (PCI Device 0 offset 50 bits 15:8) from TOLUD (PCI Device 0 offset BC bits 31:20). **Locked by:** BDSM_0_0_0_PCI.LOCK
19:1	0h RO	**Reserved**
0	0h RW/L	**LOCK:** This bit will lock all writeable settings in this register, including itself. **Locked by:** BDSM_0_0_0_PCI.LOCK

3.1.32 Base of GTT Stolen Memory (BGSM_0_0_0_PCI) — Offset B4h

This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 52 bits 9:8) from the Graphics Base of Data Stolen Memory (PCI Device 0 offset B0 bits 31:20).

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:0, F:0] + B4h	00100000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	001h RW/L	**BGSM:** This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 50 bits 7:6) from the Graphics Base of Data Stolen Memory (PCI Device 0 offset B0 bits 31:20). **Locked by:** BGSM_0_0_0_PCI.LOCK
19:1	0h RO	**Reserved**
0	0h RW/L	**LOCK:** This bit will lock all writeable settings in this register, including itself. **Locked by:** BGSM_0_0_0_PCI.LOCK

3.1.33 TSEGMB PCI (TSEGMB_0_0_0_PCI) — Offset B8h

This register contains the base address of TSEG DRAM memory. BIOS determines the base of TSEG memory which must be at or below Graphics Base of GTT Stolen Memory (PCI Device 0 Offset B4 bits 31:20).

NOTE: BIOS must program TSEGMB to a 8MB naturally aligned boundary.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:0, F:0] + B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW/L	**TSEGMB:** This register contains the base address of TSEG DRAM memory. BIOS determines the base of TSEG memory which must be at or below Graphics Base of GTT Stolen Memory (PCI Device 0 Offset B4 bits 31:20). BIOS must program the value of TSEGMB to be the same as BGSM when TSEG is disabled. **Locked by:** TSEGMB_0_0_0_PCI.LOCK
19:1	0h RO	**Reserved**
0	0h RW/L	**LOCK:** This bit will lock all writeable settings in this register, including itself. **Locked by:** TSEGMB_0_0_0_PCI.LOCK

3.1.34 TOLUD PCI (TOLUD_0_0_0_PCI) — Offset BCh

This 32 bit register defines the Top of Low Usable DRAM. TSEG, GTT Graphics memory and Graphics Stolen Memory are within the DRAM space defined. From the top, the Host optionally claims 1 to 64MBs of DRAM for internal graphics if enabled, 1or 2MB of DRAM for GTT Graphics Stolen Memory (if enabled) and 1, 2, or 8 MB of DRAM for TSEG if enabled.

Programming Example:

C1DRB3 is set to 4GB

TSEG is enabled and TSEG size is set to 1MB

Internal Graphics is enabled, and Graphics Mode Select is set to 32MB

GTT Graphics Stolen Memory Size set to 2MB

BIOS knows the OS requires 1G of PCI space.

BIOS also knows the range from 0_FEC0_0000h to 0_FFFF_FFFFh is not usable by the system. This 20MB range at the very top of addressable memory space is lost to APIC and Intel TXT.

According to the above equation, TOLUD is originally calculated to: 4GB = 1_0000_0000h

The system memory requirements are: 4GB (max addressable space) - 1GB (pci space) - 35MB (lost memory) = 3GB - 35MB (minimum granularity) = 0_ECB0_0000h

Since 0_ECB0_0000h (PCI and other system requirements) is less than 1_0000_0000h, TOLUD should be programmed to ECBh.

These bits are Intel TXT lockable.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:0, F:0] + BCh	00100000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	001h RW/L	**TOLUD:** This register contains bits 31 to 20 of an address one byte above the maximum DRAM memory below 4G that is usable by the operating system. Address bits 31 down to 20 programmed to 01h implies a minimum memory size of 1MB. Configuration software must set this value to the smaller of the following 2 choices: maximum amount memory in the system minus ME stolen memory plus one byte or the minimum address allocated for PCI memory. Address bits 19:0 are assumed to be 0_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register. The Top of Low Usable DRAM is the lowest address above both Graphics Stolen memory and Tseg. BIOS determines the base of Graphics Stolen Memory by subtracting the Graphics Stolen Memory Size from TOLUD and further decrements by Tseg size to determine base of Tseg. All the Bits in this register are locked in Intel TXT mode. This register must be 1MB aligned when reclaim is enabled. **Locked by:** TOLUD_0_0_0_PCI.LOCK
19:1	0h RO	**Reserved**
0	0h RW/L	**LOCK:** This bit will lock all writeable settings in this register, including itself. **Locked by:** TOLUD_0_0_0_PCI.LOCK

3.1.35 ERRSTS PCI (ERRSTS_0_0_0_PCI) — Offset C8h

This register is used to report various error conditions via the SERR DMI messaging mechanism. An SERR DMI message is generated on a zero to one transition of any of these flags (if enabled by the ERRCMD and PCICMD registers).

These bits are set regardless of whether or not the SERR is enabled and generated. After the error processing is complete, the error logging mechanism can be unlocked by clearing the appropriate status bit by software writing a 1 to it.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:0, F:0] + C8h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**
11	0h RW/1C/V/P	**MC1 DDR5 CRC (MC1_DDR5_CRC):** If this bit is set to 1, a memory read data or write transfer had an uncorrectable DDR5 CRC error. The purpose of this feature is just for debug and error isolation and NOT a RAS feature that would be enabled in normal operation. If a CRC error occurs, the system should machine check and BSOD.
10	0h RW/1C/V/P	**MC0 DDR5 CRC (MC0_DDR5_CRC):** If this bit is set to 1, a memory read data or write transfer had an uncorrectable DDR5 CRC error. The purpose of this feature is just for debug and error isolation and NOT a RAS feature that would be enabled in normal operation. If a CRC error occurs, the system should machine check and BSOD.
9	0h RW/1C/V/P	**MC1 DMERR (MC1_DMERR):** If this bit is set to 1, a memory read data transfer had an uncorrectable multiple-bit error. When this bit is set, the column, row, bank, and rank that caused the error, and the error syndrome, are logged in the ECC Error Log register in the channel where the error occurred. Once this bit is set, the ECCERRLOGx fields are locked until the CPU clears this bit by writing a 1. Software uses bits [1:0] to detect whether the logged error address is for a Single-bit or a Multiple-bit error.
8	0h RW/1C/V/P	**MC1 DSERR (MC1_DSERR):** If this bit is set to 1, a memory read data transfer had a single-bit correctable error and the corrected data was returned to the requesting agent. When this bit is set the column, row, bank, and rank where the error occurred and the syndrome of the error are logged in the ECC Error Log register in the channel where the error occurred. Once this bit is set the ECCERRLOGx fields are locked to further single-bit error updates until the CPU clears this bit by writing a 1. A multiple bit error that occurs after this bit is set will overwrite the ECCERRLOGx fields with the multiple-bit error signature and the DMERR bit will also be set. A single bit error that occurs after a multibit error will set this bit but will not overwrite the other fields.
7	0h RO	**IBECC UC (IBECC_UC):** This bit is reserved. Now IOP does not support error messages from IBECC on legacy path. IBECC err messages are logged in the MCA bank. Previously, When this bit is set to 1 it indicates a uncorrectable error occurred in IBECC.
6	0h RO	**IBECC COR (IBECC_COR):** This bit is reserved. Now IOP does not support error messages from IBECC on legacy path. IBECC err messages are logged in the MCA bank. Previously, When this bit is set to 1 it indicates a correctable error occurred in IBECC.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C/V/P	**FMUR:** When this bit is set to 1 it indicates a un-supported request event occurred in FMHC (received from PCIE to SXP).
4	0h RW/1C/V/P	**FMCA:** When this bit is set to 1 it indicates a completer abort occurred in FMHC (received from PCIE to SXP).
3	0h RW/1C/V/P	**FMIAN:** When this bit is set to 1 FMI Asynchronous Notification error event with Media dead or Health log critical notification has occurred in FMHC.
2	0h RW/1C/V/P	**FMITHERMERR:** When this bit is set to 1 it indicates a thermal event occurred in FMHC.
1	0h RW/1C/V/P	**MC0 DMERR (MC0_DMERR):** If this bit is set to 1, a memory read data transfer had an uncorrectable multiple-bit error. When this bit is set, the column, row, bank, and rank that caused the error, and the error syndrome, are logged in the ECC Error Log register in the channel where the error occurred. Once this bit is set, the ECCERRLOGx fields are locked until the CPU clears this bit by writing a 1. Software uses bits [1:0] to detect whether the logged error address is for a Single-bit or a Multiple-bit error.
0	0h RW/1C/V/P	**MC0 DSERR (MC0_DSERR):** If this bit is set to 1, a memory read data transfer had a single-bit correctable error and the corrected data was returned to the requesting agent. When this bit is set the column, row, bank, and rank where the error occurred and the syndrome of the error are logged in the ECC Error Log register in the channel where the error occurred. Once this bit is set the ECCERRLOGx fields are locked to further single-bit error updates until the CPU clears this bit by writing a 1. A multiple bit error that occurs after this bit is set will overwrite the ECCERRLOGx fields with the multiple-bit error signature and the DMERR bit will also be set. A single bit error that occurs after a multibit error will set this bit but will not overwrite the other fields.

3.1.36 ERRCMD PCI (ERRCMD_0_0_0_PCI) — Offset CAh

This register controls the Host Bridge responses to various system errors. Since the Host Bridge does not have an SERRB signal, SERR messages are passed from the CPU to the PCH over DMI.

When a bit in this register is set, a SERR message will be generated on DMI whenever the corresponding flag is set in the ERRSTS register. The actual generation of the SERR message is globally enabled for Device #0 via the PCI Command register.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:0, F:0] + CAh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**
11	0h RW	**MC1 DDR5 CRC (MC1_DDR5_CRC):** 1: The Host Bridge generates an SERR message over DMI when it detects a CRC error reported by the DRAM controller. 0: Reporting of this condition via SERR messaging is disabled. For systems not supporting DDR5 CRC this bit must be disabled.
10	0h RW	**MC0 DDR5 CRC (MC0_DDR5_CRC):** 1: The Host Bridge generates an SERR message over DMI when it detects a CRC error reported by the DRAM controller. 0: Reporting of this condition via SERR messaging is disabled. For systems not supporting DDR5 CRC this bit must be disabled.
9	0h RW	**MC1 DMERR (MC1_DMERR):** 1: The Host Bridge generates an SERR message over DMI when it detects a multiple-bit error reported by the DRAM controller. 0: Reporting of this condition via SERR messaging is disabled. For systems not supporting ECC this bit must be disabled.
8	0h RW	**MC1 DSERR (MC1_DSERR):** 1: The Host Bridge generates an SERR special cycle over DMI when the DRAM controller detects a single bit error. 0: Reporting of this condition via SERR messaging is disabled. For systems that do not support ECC this bit must be disabled.
7	0h RO	**IBECC UC (IBECC_UC):** This bit is reserved. Now IOP does not support error messages from IBECC on legacy path. IBECC err messages are logged in the MCA bank. Previously, SERR on IBECC uncorrectable error event 1: The Host Bridge generates an SERR special cycle over DMI when IBECC reports uncorrectable error. 0: Reporting of this condition via SERR messaging is disabled.
6	0h RO	**IBECC COR (IBECC_COR):** This bit is reserved. Now IOP does not support error messages from IBECC on legacy path. IBECC err messages are logged in the MCA bank. Previously, SERR on IBECC correctable error event 1: The Host Bridge generates an SERR special cycle over DMI when IBECC reports correctable error. 0: Reporting of this condition via SERR messaging is disabled.
5	0h RW	**FMUR:** SERR on FMHC un-supported request event 1: The Host Bridge generates an SERR special cycle over DMI when FMHC reports an un-supported request event. 0: Reporting of this condition via SERR messaging is disabled.
4	0h RW	**FMCA:** SERR on FMHC CA event 1: The Host Bridge generates an SERR special cycle over DMI when FMHC reports a CA event. 0: Reporting of this condition via SERR messaging is disabled.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**FMIAN:** SERR on FMI Asynchronous Notification error event 1: The Host Bridge generates an SERR special cycle over DMI when FMHC reports a Asynchronous Notification error event with Media dead or Health log critical notification. 0: Reporting of this condition via SERR messaging is disabled.
2	0h RW	**FMITHERMERR:** SERR on FMHC thermal event 1: The Host Bridge generates an SERR special cycle over DMI when FMHC reports a thermal event. 0: Reporting of this condition via SERR messaging is disabled.
1	0h RW	**MC0 DMERR (MC0_DMERR):** 1: The Host Bridge generates an SERR message over DMI when it detects a multiple-bit error reported by the DRAM controller. 0: Reporting of this condition via SERR messaging is disabled. For systems not supporting ECC this bit must be disabled.
0	0h RW	**MC0 DSERR (MC0_DSERR):** 1: The Host Bridge generates an SERR special cycle over DMI when the DRAM controller detects a single bit error. 0: Reporting of this condition via SERR messaging is disabled. For systems that do not support ECC this bit must be disabled.

3.1.37 SMICMD PCI (SMICMD_0_0_0_PCI) — Offset CCh

This register enables various errors to generate an SMI DMI special cycle. When an error flag is set in the ERRSTS register, it can generate an SERR, SMI, or SCI DMI special cycle when enabled in the ERRCMD, SMICMD, or SCICMD registers, respectively. Note that one and only one message type can be enabled.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:0, F:0] + CCh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**
11	0h RW	**MC1 DDR5 CRC (MC1_DDR5_CRC):** 1: The Host generates an SMI DMI message when it detects a CRC error reported by the DRAM controller. 0: Reporting of this condition via SMI messaging is disabled. For systems not supporting DDR5 CRC this bit must be disabled.
10	0h RW	**MC0 DDR5 CRC (MC0_DDR5_CRC):** 1: The Host generates an SMI DMI message when it detects a CRC error reported by the DRAM controller. 0: Reporting of this condition via SMI messaging is disabled. For systems not supporting DDR5 CRC this bit must be disabled.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**MC1 DMEDMI (MC1_DMESMI):** 1: The Host generates an SMI DMI message when it detects a multiple-bit error reported by the DRAM controller. 0: Reporting of this condition via SMI messaging is disabled. For systems not supporting ECC this bit must be disabled.
8	0h RW	**MC1 DSESMI (MC1_DSESMI):** 1: The Host generates an SMI DMI special cycle when the DRAM controller detects a single bit error. 0: Reporting of this condition via SMI messaging is disabled. For systems that do not support ECC this bit must be disabled.
7	0h RO	**IBECC UC (IBECC_UC):** This bit is reserved. Now IOP does not support error messages from IBECC on legacy path. IBECC err messages are logged in the MCA bank. Previously, SMI on IBECC uncorrectable error event 1: The Host Bridge generates an SMI special cycle over DMI when IBECC reports uncorrectable error. 0: Reporting of this condition via SMI messaging is disabled.
6	0h RO	**IBECC COR (IBECC_COR):** This bit is reserved. Now IOP does not support error messages from IBECC on legacy path. IBECC err messages are logged in the MCA bank. Previously, SMI on IBECC correctable error event 1: The Host Bridge generates an SMI special cycle over DMI when IBECC reports correctable error. 0: Reporting of this condition via SMI messaging is disabled.
5	0h RW	**FMUR:** SMI on FMHC un-supported request event 1: The Host Bridge generates an SMI special cycle over DMI when FMHC reports an un-supported request event. 0: Reporting of this condition via SMI messaging is disabled.
4	0h RW	**FMCA:** SMI on FMHC CA event 1: The Host Bridge generates an SMI special cycle over DMI when FMHC reports a CA event. 0: Reporting of this condition via SMI messaging is disabled.
3	0h RW	**FMIAN:** SMI on FMI Asynchronous Notification error event 1: The Host Bridge generates an SMI special cycle over DMI when FMHC reports a Asynchronous Notification error event with Media dead or Health log critical notification. 0: Reporting of this condition via SMI messaging is disabled.
2	0h RW	**FMITHERMERR:** SMI on FMHC thermal event 1: The Host Bridge generates an SMI special cycle over DMI when FMHC reports a thermal event. 0: Reporting of this condition via SMI messaging is disabled.
1	0h RW	**MC0 DMESMI (MC0_DMESMI):** 1: The Host generates an SMI DMI message when it detects a multiple-bit error reported by the DRAM controller. 0: Reporting of this condition via SMI messaging is disabled. For systems not supporting ECC this bit must be disabled.
0	0h RW	**MC0 DSESMI (MC0_DSESMI):** 1: The Host generates an SMI DMI special cycle when the DRAM controller detects a single bit error. 0: Reporting of this condition via SMI messaging is disabled. For systems that do not support ECC this bit must be disabled.

3.1.38 SCICMD PCI (SCICMD_0_0_0_PCI) — Offset CEh

This register enables various errors to generate an SMI DMI special cycle. When an error flag is set in the ERRSTS register, it can generate an SERR, SMI, or SCI DMI special cycle when enabled in the ERRCMD, SMICMD, or SCICMD registers, respectively. Note that one and only one message type can be enabled.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:0, F:0] + CEh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**
11	0h RW	**MC1 DDR5 CRC (MC1_DDR5_CRC):** 1: The Host generates an SCI DMI message when it detects a CRC error reported by the DRAM controller. 0: Reporting of this condition via SCI messaging is disabled. For systems not supporting DDR5 CRC this bit must be disabled.
10	0h RW	**MC0 DDR5 CRC (MC0_DDR5_CRC):** 1: The Host generates an SCI DMI message when it detects a CRC error reported by the DRAM controller. 0: Reporting of this condition via SCI messaging is disabled. For systems not supporting DDR5 CRC this bit must be disabled.
9	0h RW	**MC1 DMESCI (MC1_DMESCI):** 1: The Host generates an SCI DMI message when it detects a multiple-bit error reported by the DRAM controller. 0: Reporting of this condition via SCI messaging is disabled. For systems not supporting ECC this bit must be disabled.
8	0h RW	**MC1 DSESCI (MC1_DSESCI):** 1: The Host generates an SCI DMI special cycle when the DRAM controller detects a single bit error. 0: Reporting of this condition via SCI messaging is disabled. For systems that do not support ECC this bit must be disabled.
7	0h RO	**IBECC UC (IBECC_UC):** This bit is reserved. Now IOP does not support error messages from IBECC on legacy path. IBECC err messages are logged in the MCA bank. Previously, SCI on IBECC uncorrectable error event 1: The Host Bridge generates an SCI special cycle over DMI when IBECC reports uncorrectable error. 0: Reporting of this condition via SCI messaging is disabled.
6	0h RO	**IBECC COR (IBECC_COR):** This bit is reserved. Now IOP does not support error messages from IBECC on legacy path. IBECC err messages are logged in the MCA bank. Previously, SCI on IBECC correctable error event 1: The Host Bridge generates an SCI special cycle over DMI when IBECC reports correctable error. 0: Reporting of this condition via SCI messaging is disabled.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**FMUR:** SCI on FMHC un-supported request event 1: The Host Bridge generates an SCI special cycle over DMI when FMHC reports an un-supported request event. 0: Reporting of this condition via SCI messaging is disabled.
4	0h RW	**FMCA:** SCI on FMHC CA event 1: The Host Bridge generates an SCI special cycle over DMI when FMHC reports a CA event. 0: Reporting of this condition via SCI messaging is disabled.
3	0h RW	**FMIAN:** SCI on FMI Asynchronous Notification error event 1: The Host Bridge generates an SCI special cycle over DMI when FMHC reports a Asynchronous Notification error event with Media dead or Health log critical notification. 0: Reporting of this condition via SCI messaging is disabled.
2	0h RW	**FMITHERMERR:** SCI on FMHC thermal event 1: The Host Bridge generates an SCI special cycle over DMI when FMHC reports a thermal event. 0: Reporting of this condition via SCI messaging is disabled.
1	0h RW	**MC0 DMESCI (MC0_DMESCI):** 1: The Host generates an SCI DMI message when it detects a multiple-bit error reported by the DRAM controller. 0: Reporting of this condition via SCI messaging is disabled. For systems not supporting ECC this bit must be disabled.
0	0h RW	**MC0 DSESCI (MC0_DSESCI):** 1: The Host generates an SCI DMI special cycle when the DRAM controller detects a single bit error. 0: Reporting of this condition via SCI messaging is disabled. For systems that do not support ECC this bit must be disabled.

3.1.39 SKPD PCI (SKPD_0_0_0_PCI) — Offset DCh

This register holds 32 writable bits with no functionality behind them. It is for the convenience of BIOS and graphics drivers.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:0, F:0] + DCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SKPD:** 1 DWORD of data storage.

3.1.40 CAPID0_A PCI (CAPID0_A_0_0_0_PCI) — Offset E4h

Control of bits in this register are only required for customer visible SKU differentiation.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:0, F:0] + E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**NVME F0D (NVME_F0D):** 0: Device 3 Function 0 and associated memory spaces are accessible. 1: Device 3 Function 0 (NVMe F0) and associated memory space are disabled by hardwiring the D3F0EN field, bit 5 of the SoC Device Enable register
30	0h RW/L	**PEG12D:** 0: Device 1 Function 2 and associated memory spaces are accessible. 1: Device 1 Function 2 and associated memory and IO spaces are disabled by hardwiring the D1F2EN field, bit 1 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.
29	0h RW/L	**PEG11D:** 0: Device 1 Function 1 and associated memory spaces are accessible. 1: Device 1 Function 1 and associated memory and IO spaces are disabled by hardwiring the D1F1EN field, bit 2 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.
28	0h RW/L	**PEG10D:** 0: Device 1 Function 0 and associated memory spaces are accessible. 1: Device 1 Function 0 and associated memory and IO spaces are disabled by hardwiring the D1F0EN field, bit 3 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.
27	0h RW/L	**PELWUD:** 0: Link width upconfig is supported. The CPU advertises upconfig capability using the data rate symbol in its TS2 training ordered sets during Configuration.Complete. The CPU responds to link width upconfigs initiated by the downstream device. 1: Link width upconfig is NOT supported. The CPU does not advertise upconfig capability using the data rate field in TS2 training ordered sets during Configuration.Complete. The CPU does not respond to link width upconfigs initiated by the downstream device.
26	0h RW/L	**DW:** 0: DMI x4 1: DMI x2
25	0h RW/L	**ECCDIS:** 0b ECC capable 1b Not ECC capable
24	0h RW/L	**FDEE:** 0: DRAM ECC optional via software. 1: DRAM ECC enabled. MCHBAR C0MISCCTL bit [0] and C1MISCCTL bit [0] are forced to 1 and Read-Only. Note that FDEE and ECCDIS must not both be set to 1.
23	0h RW/L	**VTDD:** 0: Enable VTd 1: Disable VTd

Bit Range	Default & Access	Field Name (ID): Description
22	0h RW/L	**DMIG2DIS:** 0: Capable of running DMI in Gen 2 mode 1: Not capable of running DMI in Gen 2 mode
21	0h RO	**Reserved**
20:19	0h RW/L	**DDRSZ:** This field defines the maximum allowed memory size per channel. 00b Unlimited (64GB per channel) 01b Maximum 8GB per channel 10b Maximum 4GB per channel 11b Maximum 2GB per channel
18	0h RW/L	**PEG60D:** Spare
17	0h RW/L	**D1NM:** 0: Part is capable of supporting 1n mode timings on the DDR interface. 1: Part is not capable of supporting 1n mode. Only supported timings are 2n or greater.
16	0h RW/L	**FUFRD:** Controls how much ULT information is available to debugging software via configuration transactions. 0: Full ULT information is available, including Wafer, X, and Y location. 1: ULT information is hidden. All ULT information will read out as zeros.
15	0h RW/L	**CDD:** 0: Camarillo Device enabled. 1: Camarillo Device disabled.
14	0h RW/L	**DDPCD:** Allows Dual Channel operation but only supports 1 DIMM per channel. 0: 2 DIMMs per channel enabled 1: 2 DIMMs per channel disabled. This setting hardwires bits 2 and 3 of the rank population field for each channel to zero. (MCHBAR offset 260h, bits 22-23 for channel 0 and MCHBAR offset 660h, bits 22-23 for channel 1)
13	0h RW/L	**X2APIC ENABLE (X2APIC_EN):** Extended Interrupt Mode. 0b: Hardware does not support Extended APIC mode. 1b: Hardware supports Extended APIC mode.
12	0h RW/L	**PDCD:** 0: Capable of Dual Channels 1: Not Capable of Dual Channel - only single channel capable.
11	0h RW/L	**IGD:** 0: There is a graphics engine within this CPU. Internal Graphics Device (Device 2) is enabled and all of its memory and I/O spaces are accessable. Configuration cycles to Device 2 will be completed within the CPU. All non-SMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2 and IO registers within Device 2 and VGA Enable of the PCI to PCI bridge control register in Devices 1 and 6 (If PCI Express GFX attach is supported). A selected amount of Graphics Memory space is pre-allocated from the main memory based on Graphics Mode Select (GMS in the GGC Register). Graphics Memory is pre-allocated above TSEG Memory. 1: There is no graphics engine within this CPU. Internal Graphics Device (Device 2) and all of its memory and I/O functions are disabled. Configuration cycle targeted to Device 2 will be passed on to DMI. In addition, all clocks to internal graphics logic are turned off. All non-SMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control register in Devices 1 and 6. DEVEN [4:3] (Device 0, offset 54h) have no meaning. Device 2 Functions 0 and 1 are disabled and hidden.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/L	**DID0OE:** 0b Disable ability to override DID0 - For production 1b Enable ability to override DID - For debug and samples only
9	0h RO	**Reserved**
8	0h RW/L	**SXP 2LM SUPPORTED (SXP_2LM_SUPPORTED):** 2LM is supported by this product.
7:4	0h RW/L	**CRID:** Compatibility Rev ID: PCODE will update this field with the value of FUSE_CRID.
3	0h RW/L	**DDR OVERCLOCK (DDR_OVERCLOCK):** DDR overclocking. PCODE will update this field with the value of FUSE_DDR_OC_EN.
2	0h RO	**Reserved**
1	0h RW/L	**NVME F7D (NVME_F7D):** 0: Device 3 Function 7 and associated memory spaces are accessible. 1: Device 3 Function 7 (NVMe F7) and associated memory space are disabled by hardwiring the D3F7EN field, bit 6 of the SoC Device Enable register
0	0h RO	**Reserved**

3.1.41 CAPID0_B PCI (CAPID0_B_0_0_0_PCI) — Offset E8h

Control of bits in this register are only required for customer visible SKU differentiation.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:0, F:0] + E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**IMGU DISABLE (IMGU_DIS):** 0: Device 5 associated memory spaces are accessible. 1: Device 5 associated memory and IO spaces are disabled by hardwiring the D1F2EN field, bit 1 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.
30	0h RW/L	**NPK DISABLE (NPK_DIS):** 0: NPK associated memory spaces are accessible. 1: NPK associated memory and IO spaces are disabled by hardwiring the D1F2EN field, bit 1 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.

Bit Range	Default & Access	Field Name (ID): Description
29	0h RW/L	**OC ENABLED (OC_ENABLED):** PCODE will update this field with the value of FUSE_OC_ENABLED. 0b Over-clocking is Disabled 1b Over-clocking is Enabled If over-clocking is enabled, FUSE_OC_BINS contains how many bits of over-clocking are supported. The encoding is as follows: 0h Overclocking is Disabled 1h Max 1 bin of overclocking is supported 2h Max 2 bin of overclocking is supported 3h Max 3 bin of overclocking is supported 4h Max 4 bin of overclocking is supported 5h Max 5 bin of overclocking is supported 6h Max 6 bin of overclocking is supported 7h Unlimited If overclocking is not enabled, FUSE_OC_BINS is meaningless, and should be 0.
28	0h RW/L	**SMT:** This setting indicates whether or not the CPU is SMT capable.
27:25	0h RW/L	**CACHESZ:** This setting indicates the supporting cache sizes.
24	0h RW/L	**SVM DISABLE (SVM_DISABLE):** Consumed by Display.
23:21	0h RW/L	**PLL REF100 CFG (PLL_REF100_CFG):** DDR3 Maximum Frequency Capability with 100 Memory. PCODE will update this field with the value of FUSE_PLL_REF100_CFG and then apply SSKU overrides. Maximum allowed memory frequency with 100 MHz ref clk. Also serves as defeature. Unlike 133 MHz ref fuses, these are normal 3 bit field 0 - 100 MHz ref disabled 1 - upto DDR-1400 (7 x 200) 2 - upto DDR-1600 (8 x 200) 3 - upto DDR-1800 (8 x 200) 4 - upto DDR-2000 (10 x 200) 5 - upto DDR-2200 (11 x 200) 6 - upto DDR-2400 (12 x 200) 7 - no limit (but still limited by _DDR_FREQ200 to 2600)
20	0h RW/L	**PEGG3 DISABLE (PEGG3_DIS):** PCIe Gen 3 Disable fuse. This fuse will be strap selectable/modifiable to enable SSKU capabilities. This is a defeature fuse -- an un-programmed device should have PCIe Gen 3 capabilities enabled. 0: Capable of running any of the Gen 3-compliant PEG controllers in Gen 3 mode (Devices 0/1/0, 0/1/1, 0/1/2) 1: Not capable of running any of the PEG controllers in Gen 3 mode
19	0h RW/L	**PKGTYP:** This setting indicates the CPU Package Type.
18:17	0h RO	**Reserved**
16	0h RW/L	**PEGX16D:** 0: Capable of x16 PEG Port 1: Not Capable of x16 PEG port, instead PEG limited to x8 and below. Causes PEG port to enable and train logical lanes 7:0 only. Logical lanes 15:8 are powered down (unless in use by the other PEG port or the embedded Display Port), and the Max Link Width field of the Link Capability register reports x8 instead of x16. (In the case of lane reversal, lanes 15:8 are active and lanes 7:0 are powered down.)
15	0h RW/L	**DMIG3DIS:** DMI Gen 3 Disable fuse.
14:12	0h RW/L	**LTECH:** 2L Technology. 3'b000 - 1LM; 3'b001 - EDRAM0; 3'b011 - EDRAM0+1; 3'b100 - 2LM

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/L	**HDCPD:** 0 - Capable of HDCP 1 - HDCP Disabled
10	0h RW/L	**DEV10 DISABLED (DEV10_DISABLED):** Device 10 Disable. 0 - Device 10 Enable 1- Device 10 Disable
9	0h RO	**Reserved**
8	0h RW/L	**GMM DISABLE (GMM_DIS):** 0: Device 8 associated memory spaces are accessible. 1: Device 8 associated memory and IO spaces are disabled by hardwiring the D8EN field, bit 1 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.
7	0h RW/L	**DDD:** 0 - Debug mode 1 - Production mode
6:4	0h RO	**Reserved**
3	0h RW/L	**SH_OPI ENABLE (SH_OPI_EN):** Switch hitter, OPI enabled. 1 - OPI is enabled for H SKU 0 - DMI is enabled for H SKU
2	0h RW/L	**VMD DISABLE (VMD_DIS):** Only for S&H, Indicates if VMD is disabled.
1	0h RW/L	**DPEGFX1:** This bit has no effect on Device 1 unless Device 1 is configured for at least two ports via PEG0CFGSEL strap. 0b All PEG port widths do not depend on their respective BCTRL[VGAEN]. 1b Each PEG port width is limited to x1 operation when its respective BCTRL[VGAEN] is set to 1b.
0	0h RW/L	**SPEGFX1:** This bit has no effect on Device 1 unless Device 1 is configured for a single port via PEG0CFGSEL strap. 0b PEG10 width does not depend on its BCTRL[VGAEN]. 1b PEG10 width is limited to x1 operation when its respective BCTRL[VGAEN] is set to 1b.

3.1.42 CAPID0_C PCI (CAPID0_C_0_0_0_PCI) — Offset ECh

Control of bits in this register are only required for customer visible SKU differentiation.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:0, F:0] + ECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**PEG62D:** 0: Device 6 Function 2 and associated memory spaces are accessible. 1: Device 6 Function 2 and associated memory space are disabled by hardwiring the D6F2EN field
30	0h RW/L	**PEG61D:** 0: Device 6 Function 1 and associated memory spaces are accessible. 1: Device 6 Function 1 and associated memory space are disabled by hardwiring the D6F1EN field
29	0h RW/L	**PEGG5 DISABLE (PEGG5_DIS):** PCIe Gen 5 is disabled 0: Capable of running gen 5-compliant PEG controllers in Gen 5 mode 1: Not capable of running gen 5-compliant PEG controllers in Gen 5 mode
28	0h RW/L	**PEGG4 DISABLE (PEGG4_DIS):** PCIe Gen 4 Disable fuse. This fuse will be strap selectable/modifiable to enable DSKU capabilities. This is a defeature fuse -- an un-programmed device should have PCIe Gen 4 capabilities enabled. 0: Capable of running any of the Gen 4-compliant PEG controllers in Gen 4 mode (Devices 0/1/0, 0/1/1, 0/1/2, 60) 1: Not capable of running any of the PEG controllers in Gen 4 mode
27:23	00h RW/L	**MAX DATA RATE DDR4 (MAX_DATA_RATE_DDR4):** DDR4 Maximum Frequency Capability in 266Mhz units. (0 means unlimited). PCODE will update this field with the value of FUSE_MAX_F_DDR4.
22	0h RW/L	**DDR4 ENABLE (DDR4_EN):** Allow DDR4 operation. PCODE will update this field with the value of FUSE_DDR4_EN.
21:17	00h RW/L	**Reserved**
16	0h RW/L	**Reserved**
15	0h RO	**Reserved**
14	0h RW/L	**QCLK GV DISABLE (QCLK_GV_DIS):** 0: Qclk GV Enable 1: Qclk GV Disable
13:10	0h RW/L	**FDSKUFP:** Placeholders for future DSKUs, combination of DSKU and FUSE_FDSKUFP.
9	0h RW/L	**SE DISABLE (SE_DIS):** Secure Enclave Disable: PCODE will update this field with the value of FUSE_SE_DIS.
8:7	0h RW/L	**BCLKOCRANGE:** Bclk OC range - Combination of DSKU and FUSE_BCLKOCRANGE * 00 Bclk can't exceed 100MHz * 01 Bclk can't exceed [Threshold 1] MHz * 10 Bclk can't exceed [Threshold 2] MHz * 11 unlimited Bclk range * Threshold 1 = 115MHz - Hard coded in pCode (298D) * Threshold 2 = 130MHz - Hard coded in pCode (338D).

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/L	**IDD:** Disable Internal Display: PCODE will update this field with the value of FUSE_DE_INTRNL_DSPLY_DIS.
5	0h RW/L	**DISPLAY PIPE3 (DISPLAY_PIPE3):** Display Pipe3 Enable: PCODE will update this field with the value of FUSE_DISPLAY_PIPE3.
4:0	0h RO	**Reserved**

3.1.43 (CAPID0_E_0_0_0_PCI) — Offset F0h

Control of bits in this register are only required for customer visible SKU differentiation.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:0, F:0] + F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW/L	**CRASHLOG DISABLE (CRASHLOG_DIS):** 0: Device 10 associated memory spaces are accessible. 1: Device 10 associated memory and IO spaces are disabled by hardwiring the D10EN field, bit 17 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.
23:13	000h RW/L	**VDDQ VOLTAGE MAX (VDDQ_VOLTAGE_MAX):** VDDQ_TX MAX VID value. PCODE will update this field with the value from 11b fuse
12	0h RW/L	**IBECC DISABLE (IBECC_DIS):** Disable IBECC operation. PCODE will update this field with the value of FUSE_IBECC_DIS.
11:7	00h RW/L	**MAX DATA RATE DDR5 (MAX_DATA_RATE_DDR5):** DDR5 Maximum frequency capability in 400Mhz units. (0 means unlimited).
6	0h RW/L	**DDR5 ENABLE (DDR5_EN):** Allow DDR5 operation. PCODE will update this field with the value of FUSE_DDR5_EN.
5:1	00h RW/L	**MAX DATA RATE LPDDR5 (MAX_DATA_RATE_LPDDR5):** LPDDR5 Maximum frequency capability in 400Mhz units. (0 means unlimited).
0	0h RW/L	**LPDDR5 ENABLE (LPDDR5_EN):** Allow LPDDR5 operation. PCODE will update this field with the value of FUSE_LPDDR5_EN.

3.2 Processor Memory Controller (MCHBAR) Registers

This section contains the Memory Controller MCHBAR registers.

Base address of these registers are defined in the MCHBAR_0_0_0_PCI register in Bus: 0, Device: 0, Function: 0.

The processor has 1 memory controllers. Each memory controller has 2 channels. Each channel can drive up to 2 sub channels depending on the memory type:

- LPDDR5:
  - — 1 Memory controller
  - — 2 Channels per memory controller (total 2)
  - — 2 sub channels per channel (total 4)
- DDR4:
  - — 1 Memory controller
  - — 1 Channel per memory controller (total 1)
  - — No sub channels
- DDR5:
  - — 1 Memory controllers
  - — 2 Channels per memory controller (total 2)
  - — No sub channels

The MCHBAR exposes 3 sets of memory controller registers per controller for channel 0, channel 1 as well as broadcast.

- Memory Controller 0 (MC0)
  - — Channel 0 offset range: E000h-E7FFh
  - — Channel 1 offset range: E800h-EFFFh
  - — Broadcast offset range: F000h-F7FFh
  - — Shared registers: D800h-DFFFh

Memory Controller Broadcast register behavior is to write to all channels of the same memory controller and read from channel 0.

Note: **NOTE:** For brevity, only Channel 0 and the shared registers of MC0 are documented:

- MC0 Channel 1: MC0 Channel 0 + 0800h
- MC0 Broadcast: MC0 Channel 0 + 1000h

3.2.1 Summary of Registers

Table 3-3. Summary of MCHBAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
D400h	4	Register IBECC ACTIVATE (IBECC_ACTIVATE_0_0_0_MCHBAR)	00000000h
D404h	4	Register IBECC_ECC_STORAGE_START_ADDR type (IBECC_STORAGE_ADDR_0_0_0_MCHBAR)	00000000h
D408h	8	8 registers holding the protected address ranges (IBECC_PROTECT_ADDR_RANGE_0_0_0_0_MCHBAR)	0000000000000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
D410h	8	8 registers holding the protected address ranges (IBECC_PROTECT_ADDR_RANGE_1_0_0_0_MCHBAR)	0000000000000000h
D418h	8	8 registers holding the protected address ranges (IBECC_PROTECT_ADDR_RANGE_2_0_0_0_MCHBAR)	0000000000000000h
D420h	8	8 registers holding the protected address ranges (IBECC_PROTECT_ADDR_RANGE_3_0_0_0_MCHBAR)	0000000000000000h
D428h	8	8 registers holding the protected address ranges (IBECC_PROTECT_ADDR_RANGE_4_0_0_0_MCHBAR)	0000000000000000h
D430h	8	8 registers holding the protected address ranges (IBECC_PROTECT_ADDR_RANGE_5_0_0_0_MCHBAR)	0000000000000000h
D438h	8	8 registers holding the protected address ranges (IBECC_PROTECT_ADDR_RANGE_6_0_0_0_MCHBAR)	0000000000000000h
D440h	8	8 registers holding the protected address ranges (IBECC_PROTECT_ADDR_RANGE_7_0_0_0_MCHBAR)	0000000000000000h
D450h	8	Register IBECC_INJ_ADDR_COMPARE_type (IBECC_INJ_ADDR_COMPARE_0_0_0_MCHBAR)	0000000000000000h
D458h	8	Register IBECC_INJ_ADDR_MASK_type (IBECC_INJ_ADDR_MASK_0_0_0_MCHBAR)	0000000000000000h
D460h	4	Register IBECC_INJ_COUNT_type (IBECC_INJ_COUNT_0_0_0_MCHBAR)	00000000h
D464h	4	Register IBECC_INJ_CONTROL_type (IBECC_INJ_CONTROL_0_0_0_MCHBAR)	00000000h
D468h	8	Register IBECC_ECC_ERROR_LOG_type (IBECC_ERROR_LOG_0_0_0_MCHBAR)	0000000000000000h
D800h	4	MAD INTER CHANNEL 0 0 0 MCHBAR (MAD_INTER_CHANNEL_0_0_0_MCHBAR)	00000000h
D804h	4	MAD INTRA CHANNEL 0 0 0 MCHBAR (MAD_INTRA_CH0_0_0_0_MCHBAR)	00000000h
D808h	4	MAD INTRA CHANNEL 0 0 0 MCHBAR (MAD_INTRA_CH1_0_0_0_MCHBAR)	00000000h
D80Ch	4	MAD DIMM CHANNEL 0 0 0 MCHBAR (MAD_DIMM_CH0_0_0_0_MCHBAR)	10001800h
D810h	4	MAD DIMM CHANNEL 0 0 0 MCHBAR (MAD_DIMM_CH1_0_0_0_MCHBAR)	10001800h
D824h	4	CHANNEL HASH 0 0 0 MCHBAR (CHANNEL_HASH_0_0_0_MCHBAR)	03000000h
D828h	4	CHANNEL EHASH 0 0 0 MCHBAR (CHANNEL_EHASH_0_0_0_MCHBAR)	00000000h
D83Ch	4	PWM PROGRAMMABLE REQCOUNT CONFIG 0 0 0 MCHBAR (PWM_PROGRAMMABLE_REQCOUNT_CONFIG_0_0_0_MCHBAR)	00010820h
D840h	8	PWM TOTAL REQCOUNT 0 0 0 MCHBAR (PWM_TOTAL_REQCOUNT_0_0_0_MCHBAR)	0000000000000000h
D848h	8	PWM PROGRAMMABLE REQCOUNT 0 0 0 MCHBAR (PWM_PROGRAMMABLE_REQCOUNT_0_0_0_MCHBAR[0])	0000000000000000h
D850h	8	PWM PROGRAMMABLE REQCOUNT 0 0 0 MCHBAR (PWM_PROGRAMMABLE_REQCOUNT_0_0_0_MCHBAR[1])	0000000000000000h
D858h	8	PWM RDCAS COUNT 0 0 0 MCHBAR (PWM_RDCAS_COUNT_0_0_0_MCHBAR)	0000000000000000h
D860h	4	PM SREF config 0 0 0 MCHBAR (PM_SREF_CONFIG_0_0_0_MCHBAR)	00000200h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
D888h	8	ECC Inj Addr Compare 0 0 0 MCHBAR (ECC_INJ_ADDR_COMPARE_0_0_0_MCHBAR)	0000000000000000h
D890h	8	REMAPBASE 0 0 0 MCHBAR (REMAPBASE_0_0_0_MCHBAR)	0000007FFFF00000h
D898h	8	REMAPLIMIT 0 0 0 MCHBAR (REMAPLIMIT_0_0_0_MCHBAR)	0000000000000000h
D8A0h	8	PWM WRCAS COUNT 0 0 0 MCHBAR (PWM_WRCAS_COUNT_0_0_0_MCHBAR)	0000000000000000h
D8A8h	8	PWM COMMAND COUNT 0 0 0 MCHBAR (PWM_COMMAND_COUNT_0_0_0_MCHBAR)	0000000000000000h
D958h	8	ECC Inj Addr Mask 0 0 0 MCHBAR (ECC_INJ_ADDR_MASK_0_0_0_MCHBAR)	00000001FFFFFFFFh
D9B8h	4	MAD MC HASH 0 0 0 MCHBAR (MAD_MC_HASH_0_0_0_MCHBAR)	00000006h
D9C0h	4	PMON GLOBAL CONTROL 0 0 0 MCHBAR (PMON_GLOBAL_CONTROL_0_0_0_MCHBAR)	00000000h
D9C4h	4	PMON UNIT CONTROL 0 0 0 MCHBAR (PMON_UNIT_CONTROL_0_0_0_MCHBAR)	00000000h
D9D0h	4	PMON COUNTER CONTROL 0 0 0 MCHBAR (PMON_COUNTER_CONTROL_0_0_0_MCHBAR[0])	00000000h
D9D4h	4	PMON COUNTER CONTROL 0 0 0 MCHBAR (PMON_COUNTER_CONTROL_0_0_0_MCHBAR[1])	00000000h
D9D8h	4	PMON COUNTER CONTROL 0 0 0 MCHBAR (PMON_COUNTER_CONTROL_0_0_0_MCHBAR[2])	00000000h
D9DCh	4	PMON COUNTER CONTROL 0 0 0 MCHBAR (PMON_COUNTER_CONTROL_0_0_0_MCHBAR[3])	00000000h
D9E0h	4	PMON COUNTER CONTROL 0 0 0 MCHBAR (PMON_COUNTER_CONTROL_0_0_0_MCHBAR[4])	00000000h
D9E8h	8	PMON COUNTER DATA 0 0 0 MCHBAR (PMON_COUNTER_DATA_0_0_0_MCHBAR[0])	0000000000000000h
D9F0h	8	PMON COUNTER DATA 0 0 0 MCHBAR (PMON_COUNTER_DATA_0_0_0_MCHBAR[1])	0000000000000000h
D9F8h	8	PMON COUNTER DATA 0 0 0 MCHBAR (PMON_COUNTER_DATA_0_0_0_MCHBAR[2])	0000000000000000h
DA00h	8	PMON COUNTER DATA 0 0 0 MCHBAR (PMON_COUNTER_DATA_0_0_0_MCHBAR[3])	0000000000000000h
DA08h	8	PMON COUNTER DATA 0 0 0 MCHBAR (PMON_COUNTER_DATA_0_0_0_MCHBAR[4])	0000000000000000h
DA10h	4	OS TELEMETRY CONTROL 0 0 0 MCHBAR (OS_TELEMETRY_CONTROL_0_0_0_MCHBAR)	00000000h
E000h	8	TC PRE 0 0 0 MCHBAR (TC_PRE_0_0_0_MCHBAR)	104070180040C008h
E008h	4	TC ACT 0 0 0 MCHBAR (TC_ACT_0_0_0_MCHBAR)	18020810h
E00Ch	4	TC RDRD 0 0 0 MCHBAR (TC_RDRD_0_0_0_MCHBAR)	04040484h
E010h	4	TC RDWR 0 0 0 MCHBAR (TC_RDWR_0_0_0_MCHBAR)	04040404h
E014h	4	TC WRRD 0 0 0 MCHBAR (TC_WRRD_0_0_0_MCHBAR)	08100804h
E018h	4	TC WRWR 0 0 0 MCHBAR (TC_WRWR_0_0_0_MCHBAR)	04040404h
E020h	8	SC Roundtrip latency 0 0 0 MCHBAR (SC_ROUNDTRIP_LATENCY_0_0_0_MCHBAR)	1919191919191919h
E048h	4	ECCERRLOG0 0 0 0 MCHBAR (ECCERRLOG0_0_0_0_MCHBAR)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
E04Ch	4	ECCERRLOG1 0 0 0 MCHBAR (ECCERRLOG1_0_0_0_MCHBAR)	00000000h
E050h	8	TC PWRDN 0 0 0 MCHBAR (TC_PWRDN_0_0_0_MCHBAR)	0804100400810204h
E070h	8	TC ODT 0 0 0 MCHBAR (TC_ODT_0_0_0_MCHBAR)	0000000006050000h
E080h	4	SC ODT MATRIX 0 0 0 MCHBAR (SC_ODT_MATRIX_0_0_0_MCHBAR)	00000000h
E088h	8	SC GS CFG 0 0 0 MCHBAR (SC_GS_CFG_0_0_0_MCHBAR)	0100000000000020h
E0B8h	4	SPID LOW POWER CTL 0 0 0 MCHBAR (SPID_LOW_POWER_CTL_0_0_0_MCHBAR)	08104426h
E104h	4	TR RRDVALID ctrl 0 0 0 MCHBAR (TR_RRDVALID_CTRL_0_0_0_MCHBAR)	00000000h
E108h	8	TR RRDVALID data 0 0 0 MCHBAR (TR_RRDVALID_DATA_0_0_0_MCHBAR)	0000000000000000h
E40Ch	4	TC REFm 0 0 0 MCHBAR (TC_REFM_0_0_0_MCHBAR)	00000000h
E424h	4	MR4 RANK TEMPERATURE 0 0 0 MCHBAR (MR4_RANK_TEMPERATURE_0_0_0_MCHBAR)	03030303h
E428h	4	DDR4 MPR RANK TEMPERATURE 0 0 0 MCHBAR (DDR4_MPR_RANK_TEMPERATURE_0_0_0_MCHBAR)	01010101h
E438h	4	TC RFP 0 0 0 MCHBAR (TC_RFP_0_0_0_MCHBAR)	2356980Fh
E43Ch	4	TC RFTP 0 0 0 MCHBAR (TC_RFTP_0_0_0_MCHBAR)	02D01004h
E440h	4	TC SRFTP 0 0 0 MCHBAR (TC_SRFTP_0_0_0_MCHBAR)	00000200h
E444h	4	MC REFRESH STAGGER 0 0 0 MCHBAR (MC_REFRESH_STAGGER_0_0_0_MCHBAR)	00000000h
E448h	8	TC ZQCAL 0 0 0 MCHBAR (TC_ZQCAL_0_0_0_MCHBAR)	0000032000010000h
E454h	4	MC Init State 0 0 0 MCHBAR (MC_INIT_STATE_0_0_0_MCHBAR)	0000000Fh
E460h	4	PM DIMM IDLE ENERGY 0 0 0 MCHBAR (PM_DIMM_IDLE_ENERGY_0_0_0_MCHBAR)	00000000h
E464h	4	PM DIMM PD ENERGY 0 0 0 MCHBAR (PM_DIMM_PD_ENERGY_0_0_0_MCHBAR)	00000000h
E468h	4	PM DIMM ACT ENERGY 0 0 0 MCHBAR (PM_DIMM_ACT_ENERGY_0_0_0_MCHBAR)	00000000h
E46Ch	4	PM DIMM RD ENERGY 0 0 0 MCHBAR (PM_DIMM_RD_ENERGY_0_0_0_MCHBAR)	00000000h
E470h	4	PM DIMM WR ENERGY 0 0 0 MCHBAR (PM_DIMM_WR_ENERGY_0_0_0_MCHBAR)	00000000h
E478h	4	SC WR Delay 0 0 0 MCHBAR (SC_WR_DELAY_0_0_0_MCHBAR)	00000003h
E488h	4	SC PBR 0 0 0 MCHBAR (SC_PBR_0_0_0_MCHBAR)	0000F011h
E494h	4	TC LPDDR4 MISC 0 0 0 MCHBAR (TC_LPDDR4_MISC_0_0_0_MCHBAR)	04081056h
E4C0h	8	TC SREXITTP 0 0 0 MCHBAR (TC_SREXITTP_0_0_0_MCHBAR)	0200000000000000h
E4E8h	4	reg MBIST 0 0 0 MCHBAR (WDB_MBIST_0_0_0_MCHBAR[0])	00000000h
E4ECh	4	reg MBIST 0 0 0 MCHBAR (WDB_MBIST_0_0_0_MCHBAR[1])	00000000h
E4F8h	4	reg MBIST 0 0 0 MCHBAR (RDB_MBIST_0_0_0_MCHBAR)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
E4FCh	4	ECC Inject count 0 0 0 MCHBAR (ECC_INJECT_COUNT_0_0_0_MCHBAR)	FFFFFFFFh
E5F8h	4	MCMNTS SPARE2 0 0 0 MCHBAR (MCMNTS_SPARE2_0_0_0_MCHBAR)	00000000h
E5FCh	4	MCMNTS SPARE 0 0 0 MCHBAR (MCMNTS_SPARE_0_0_0_MCHBAR)	00000000h

3.2.2 Register IBECC ACTIVATE (IBECC_ACTIVATE_0_0_0_MCHBAR) — Offset D400h

Register activating IBECC

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D400h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**When set, enables IBECC functionality (IBECC_EN):**

3.2.3 Register IBECC_ECC_STORAGE_START_ADDR type (IBECC_STORAGE_ADDR_0_0_0_MCHBAR) — Offset D404h

Register IBECC_ECC_STORAGE_START_ADDR type

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D404h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:0	0000000h RW	**ECC storage start address (START_ADDR):** ECC storage start address (bits 45:20 of the CMI address)

3.2.4 8 registers holding the protected address ranges (IBECC_PROTECT_ADDR_RANGE_0_0_0_0_MCHBAR) — Offset D408h

8 registers holding the protected address ranges

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + D408h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	None	None

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**Enable field (ENABLE):** Enable field for thr protec address range register
62:58	0h RO	**Reserved**
57:32	0000000h RW	**Mask field (MASK):** Mask field for using protected address range
31:26	0h RO	**Reserved**
25:0	0000000h RW	**Base address of protected range (BASE):** Base address of protected range. If (ADDRESS[45:20] & MASK == BASE), then ADDRESS is part of range

3.2.5 8 registers holding the protected address ranges (IBECC_PROTECT_ADDR_RANGE_1_0_0_0_MCHBAR) — Offset D410h

8 registers holding the protected address ranges

Note: **NOTE:** Bit definitions are the same as IBECC_PROTECT_ADDR_RANGE_0_0_0_0_MCHBAR, offset D408h.

3.2.6 8 registers holding the protected address ranges (IBECC_PROTECT_ADDR_RANGE_2_0_0_0_MCHBAR) — Offset D418h

8 registers holding the protected address ranges

Note: **NOTE:** Bit definitions are the same as IBECC_PROTECT_ADDR_RANGE_0_0_0_0_MCHBAR, offset D408h.

3.2.7 8 registers holding the protected address ranges (IBECC_PROTECT_ADDR_RANGE_3_0_0_0_MCHBAR) — Offset D420h

8 registers holding the protected address ranges

Note: **NOTE:** Bit definitions are the same as IBECC_PROTECT_ADDR_RANGE_0_0_0_0_MCHBAR, offset D408h.

3.2.8 8 registers holding the protected address ranges (IBECC_PROTECT_ADDR_RANGE_4_0_0_0_MCHBAR) — Offset D428h

8 registers holding the protected address ranges

Note: **NOTE:** Bit definitions are the same as IBECC_PROTECT_ADDR_RANGE_0_0_0_0_MCHBAR, offset D408h.

3.2.9 8 registers holding the protected address ranges (IBECC_PROTECT_ADDR_RANGE_5_0_0_0_MCHBAR) — Offset D430h

8 registers holding the protected address ranges

Note: **NOTE:** Bit definitions are the same as IBECC_PROTECT_ADDR_RANGE_0_0_0_0_MCHBAR, offset D408h.

3.2.10 8 registers holding the protected address ranges (IBECC_PROTECT_ADDR_RANGE_6_0_0_0_MCHBAR) — Offset D438h

8 registers holding the protected address ranges

Note: **NOTE:** Bit definitions are the same as IBECC_PROTECT_ADDR_RANGE_0_0_0_0_MCHBAR, offset D408h.

3.2.11 8 registers holding the protected address ranges (IBECC_PROTECT_ADDR_RANGE_7_0_0_0_MCHBAR) — Offset D440h

8 registers holding the protected address ranges

Note: **NOTE:** Bit definitions are the same as IBECC_PROTECT_ADDR_RANGE_0_0_0_0_MCHBAR, offset D408h.

3.2.12 Register IBECC_INJ_ADDR_COMPARE_type (IBECC_INJ_ADDR_COMPARE_0_0_0_MCHBAR) — Offset D450h

Address to mask/match against for ECC error injection

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + D450h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:6	00000000 00h RW	**Register ADDR (ADDR):** Address to mask/match against for ECC error injection
5:0	0h RO	**Reserved**

3.2.13 Register IBECC_INJ_ADDR_MASK_type (IBECC_INJ_ADDR_MASK_0_0_0_MCHBAR) — Offset D458h

Address to mask/match against for ECC error injection

Note: **NOTE:** Bit definitions are the same as IBECC_INJ_ADDR_COMPARE_0_0_0_MCHBAR, offset D450h.

3.2.14 Register IBECC_INJ_COUNT_type (IBECC_INJ_COUNT_0_0_0_MCHBAR) — Offset D460h

Number of transactions between ECC error injection

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D460h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Register ADDR (COUNT):** Number of transactions between ECC error injection

3.2.15 Register IBECC_INJ_CONTROL_type (IBECC_INJ_CONTROL_0_0_0_MCHBAR) — Offset D464h

000b - No ECC error injection.

001b - Inject a correctable ECC error on the ECC_INJ_ADDR_COMPARE register match.

011b - Inject a correctable ECC error on the ECC error insertion counter.

101b - Inject a non-recoverable ECC error on the ECC_INJ_ADDR_COMPARE register match.

111b - Inject a non-recoverable ECC error on the ECC error insertion counter.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D464h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2:0	0h RW	**Register ECC_Inj (ECC_INJ):** 000b - No ECC error injection. 001b - Inject a correctable ECC error on the ECC_INJ_ADDR_COMPARE register match. 011b - Inject a correctable ECC error on the ECC error insertion counter. 101b - Inject a non-recoverable ECC error on the ECC_INJ_ADDR_COMPARE register match. 111b - Inject a non-recoverable ECC error on the ECC error insertion counter.

3.2.16 Register IBECC_ECC_ERROR_LOG_type (IBECC_ERROR_LOG_0_0_0_MCHBAR) — Offset D468h

This register is used to store the CMI address information for the address block of main memory in which an error (single bit or multi-bit error) has occurred. Note that the address fields represent the address of the first single or the first multiple bit error occurrence after the error flag bits in the ERRSTS register have been cleared by software. An uncorrectable error will overwrite a correctable error. Else, once the error flag bits are set as a result of an error, this bit field is locked and doesn't change as a result of a new similar error until the error flag is cleared by software.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + D468h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	RW

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/1C/V/P	**Register Multi-bit error status (MERRSTS):** This bit is set when an uncorrectable multiple-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked until this bit is cleared. Software clears this bit after processing the error (by writing 1 via SB).
62	0h RW/1C/V/P	**Register correctable error status (CERRSTS):** This bit is set when a correctable single-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked to further single bit errors, until this bit is cleared. But, a multiple bit error that occurs after this bit is set will over-write the address/error syndrome info. Software clears this bit after processing the error (by writing 1 via SB).
61:46	0000h RO/V/P	**Register error syndrome (ERRSYND):** Error Syndrome that describes the is associated with the failing Cache Line
45:5	00000000000h RO/V/P	**Register error address (ERRADD):** CMI address of the address block of main memory of which an error (single bit or multi-bit error) has occurred.
4	0h RW/1C/V/P	**Milti-Bit Error overflow (MERR_OVERFLOW):** This bit is set when an uncorrectable multiple-bit error occurs on a memory read data transfer and the MERRSTS bit is already set, indicating that more than one error has occurred. Software clears this bit after processing the error (by writing 1 via SB).

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V/P	**Correctable error overflow (CERR_OVERFLOW):** This bit is set when a correctable single-bit error occurs on a memory read data transfer and the MERRSTS bit is already set, indicating that more than one error has occurred. Software clears this bit after processing the error (by writing 1 via SB).
2:0	0h RO	**Reserved**

3.2.17 MAD INTER CHANNEL 0 0 0 MCHBAR (MAD_INTER_CHANNEL_0_0_0_MCHBAR) — Offset D800h

This register holds parameters used by the channel decode stage. It defines virtual channel L mapping, as well as channel S size.

Also defined is the DDR type installed in the system (what DDR/LPDDR type is used).

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D800h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**HalfCachelineMode reg (HALFCACHELINEMODE):** In this mode MC returns only 32B on CMI to CPGC or the CMF fabric.
30:29	0h RO	**Reserved**
28:27	0h RW	**CH WIDTH (CH_WIDTH):** CH_WIDTH defines the width of DRAM Channel 00: x16 01: x32 10: x64 11: RSVD
26:20	0h RO	**Reserved**
19:12	00h RW	**CH S SIZE (CH_S_SIZE):** Channel S size in multiplies of 0.5GB . Supported range is 0GB - 64GB.
11:5	0h RO	**Reserved**
4	0h RW	**CH L MAP (CH_L_MAP):** Channel L mapping to physical channel. 0: Channel 0 1: Channel 1
3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2:0	0h RW	**DDR TYPE (DDR_TYPE):** DDR_TYPE - defines the DDR type in system: 000: DDR4 001: DDR5 010: LPDDR5 100-111: RSVD

3.2.18 MAD INTRA CHANNEL 0 0 0 MCHBAR (MAD_INTRA_CH0_0_0_0_MCHBAR) — Offset D804h

This register holds parameters used by the DRAM decode stage.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D804h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14	0h RW	**CRC reg (CRC):** CRC mode enable bit 0 - Disabled 1 - Enabled
13:12	0h RW	**ECC reg (ECC):** ECC configuration in the channel: 00: No ECC active in the channel. 01: ECC is active in IO, ECC logic is not active. 10: ECC is disabled in IO, but ECC logic is enabled. 11: ECC active in both IO and ECC logic. Note: This field must be programmed identically for all populated channels. Note 2: In a system with ECC this field must be programmed to 2'b01 during training and then 2'b11 before transitioning from training mode to Normal mode
11:9	0h RO	**Reserved**
8	0h RW	**EIM reg (EIM):** Enhanced interleaving mode enable bit 0 - Disabled 1 - Enabled
7:1	0h RO	**Reserved**
0	0h RW	**DIMM L MAP (DIMM_L_MAP):** Virtual DIMM L mapping to physical DIMM 0 - DIMM0 1 - DIMM1

3.2.19 MAD INTRA CHANNEL 0 0 0 MCHBAR (MAD_INTRA_CH1_0_0_0_MCHBAR) — Offset D808h

This register holds parameters used by the DRAM decode stage.

Note: **NOTE:** Bit definitions are the same as MAD_INTRA_CH0_0_0_0_MCHBAR, offset D804h.

3.2.20 MAD DIMM CHANNEL 0 0 0 MCHBAR (MAD_DIMM_CH0_0_0_0_MCHBAR) — Offset D80Ch

This register defines the channel DIMM characteristics - number of DIMMs, number of ranks, size and type.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D80Ch	10001800h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Decoder EBH (DECODER_EBH):** Enable address decoder Extended bank hashing. Bit 0 - Enable XaB Bit 1 - Enable XbB
29:28	1h RW	**BG0 bit options (BG0_BIT_OPTIONS):** depending on value, BG[0] will be replaced with C[5] or C[6]. for DDR5- 0- CAS[5] = zoneaddr[8] , BG[0] = zoneaddr[6] 1- CAS[5] = zoneaddr[6] , BG[0] = zoneaddr[8] 2- CAS[6] = zoneaddr[6] , BG[0] = zoneaddr[9] 3- reserved for DDR4- 0- CAS[5] = zoneaddr[9] , BG[0] = zoneaddr[6] 1- CAS[5] = zoneaddr[6] , BG[0] = zoneaddr[9] 2- CAS[6] = zoneaddr[6] , BG[0] = zoneaddr[10] 3- reserved for LPDDR5 BGMode only- 1 - swap BG[1]/CAS[6] else - keep original BG[1]/CAS[6] 3- reserved
27:26	0h RW	**DSNOR reg (DSNOR):** DIMM S number of ranks 0 - 1 Rank 1 - 2 Ranks
25:24	0h RW	**DSW reg (DSW):** DSW: DIMM S width of DDR chips 00 - X8 chips 01 - X16 chips 10 - X32 chips 11 - Reserved

Bit Range	Default & Access	Field Name (ID): Description
23	0h RO	**Reserved**
22:16	00h RW	**DIMM S SIZE (DIMM_S_SIZE):** Size of DIMM S in 0.5GB multiples
15:13	0h RO	**Reserved**
12	1h RW	**ddr5 dl 8Gb (DDR5_DL_8GB):** 0- DDR5 DIMM L capacity is more than 8Gb; 1- DDR5 DIMM L capacity is 8Gb;
11	1h RW	**ddr5 ds 8Gb (DDR5_DS_8GB):** 0- DDR5 DIMM S capacity is more than 8Gb; 1- DDR5 DIMM S capacity is 8Gb;
10:9	0h RW	**DLNOR reg (DLNOR):** DIMM L number of ranks 00 - 1 Rank 01 - 2 Ranks In ERM (enhanced rank mode): 10 - 3 ranks 11 - 4 ranks
8:7	0h RW	**DLW reg (DLW):** DLW: DIMM L width of DDR chips 00 - X8 chips 01 - X16 chips 10 - X32 chips 11 - Reserved
6:0	00h RW	**DIMM L SIZE (DIMM_L_SIZE):** Size of DIMM L in 0.5GB multiples

3.2.21 MAD DIMM CHANNEL 0 0 0 MCHBAR (MAD_DIMM_CH1_0_0_0_MCHBAR) — Offset D810h

This register defines the channel DIMM characteristics - number of DIMMs, number of ranks, size and type.

Note: **NOTE:** Bit definitions are the same as MAD_DIMM_CH0_0_0_0_MCHBAR, offset D80Ch.

3.2.22 CHANNEL HASH 0 0 0 MCHBAR (CHANNEL_HASH_0_0_0_MCHBAR) — Offset D824h

This register defines the MC channel selection function.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D824h	03000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**HASH MODE (HASH_MODE):** Encoding: 0: Use address bit-6 for channel selection. 1: Use the channel hash function as defined in the other fields of this register
27	0h RO	**Reserved**
26:24	3h RW	**HASH LSB MASK BIT (HASH_LSB_MASK_BIT):** This field specifies the MC Channel interleave bit. The following encoding is used: 000 - Addr[6] 001 - Addr[7] 010 - Addr[8] 011 - Addr[9] 100 - Addr[10] 101 - Addr[11] 110 - Addr[12/ 111 - Addr[13] For example, setting this field to 10b will interleave the channels at a 4 cacheline granularity. BIOS should set this field same as the lowest selected bit in the Mask field of this CR. Note that if the Mask field does not include the corresponding interleave bit, it will still be included in the XOR function by the MC decoding logic.
23:20	0h RO	**Reserved**
19:6	0000h RW	**HASH MASK (HASH_MASK):** The 14-bit mask corresponds to memory request Addr[19:6]. Setting a mask bit to 1 will include that particular address bit in the channel XOR function. For example, if the mask is set to 14'h0C04, then Channel = Addr[17] Addr[16] Addr[8]
5:0	0h RO	**Reserved**

3.2.23 CHANNEL EHASH 0 0 0 MCHBAR (CHANNEL_EHASH_0_0_0_MCHBAR) — Offset D828h

This register defines the MC Enhanced channel selection function.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D828h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**Sub Channels EHASH MODE (EHASH_MODE):** Encoding address bit for sub channel selection (LPDDR): 0: Use address bit-6 for sub channel selection. 1: Use the channel Ehash function as defined in the other fields of this register This mode Should be only used when we have 2 Sub channels per channel - LPDDR
27	0h RO	**Reserved**
26:24	0h RW	**Sub Channels EHASH LSB MASK BIT (EHASH_LSB_MASK_BIT):** This specifies the MC Enhanced Channel interleave bit, to set different address bit for sub channel selection than bit-6. The following encoding is used: • 000: Addr[6] • 001: Addr[7] • 010: Addr[8] • 011: Addr[9] • 100: Addr[10] • 101: Addr[11] • 110: Addr[12] • 111: Addr[13] For example, setting this field to 10b will interleave the sub channels at a 4 cache line granularity. BIOS should set this field same as the lowest selected bit in the Mask field of this register. Note that if the Mask field does not include the corresponding interleave bit, it will still be included in the XOR function by the MC decoding logic. The addresses above refer to channel addresses. When both channels are populated with sub-channels, addresses in this field that are higher than the HASH_LSB_MASK_BIT (defined in CHANNEL_HASH register) are one bit higher in physical address. Examples: • HASH_LSB_MASK_BIT = 0x2: physical Addr[8] • EHASH_LSB_MASK_BIT=0x2: channel address[8], physical address [9]
23:20	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
19:6	0000h RW	**Sub Channels EHASH MASK (EHASH_MASK):** The 14 bit mask corresponds to memory request Addr[19:6]. Setting a mask bit to 1 will include that particular address bit in the channel XOR function. For example, if the mask is set to 14'h0C04, then Channel = Addr[17] Addr[16] Addr[8] The addresses above refer to channel addresses. When both channels are populated with sub-channels, addresses in this field that are higher than the HASH_LSB_MASK_BIT (defined in CHANNEL_HASH register) are one bit higher in physical address. Examples: • HASH_LSB_MASK_BIT = 0x2: physical Addr[8] • EHASH_LSB_MASK_BIT=0x2: channel address[8], physical address [9]
5:0	0h RO	**Reserved**

3.2.24 PWM PROGRAMMABLE REQCOUNT CONFIG 0 0 0 MCHBAR (PWM_PROGRAMMABLE_REQCOUNT_CONFIG_0_0_0_MCHBAR) — Offset D83Ch

Configuration register for PWM_PROGRAMMABLE_REQCOUNT_0_0_0_MCHBAR[1:0] counters.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D83Ch	00010820h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:15	02h RW	**CMI Source ID3 (CMI_SOURCE_ID3):** Holds 1 of 2 CMI Source IDs that will increment the PWM_PROGRAMMABLE_REQCOUNT_0_0_0_MCHBAR[1] counter. When a new CMI request enters MC that has a Source ID matching either CMI_Source_ID2 or CMI_Source_ID3 the counter will be incremented by 1. The default is the CMI Source ID of IOP (IO Port).
14:10	02h RW	**CMI Source ID2 (CMI_SOURCE_ID2):** Holds 1 of 2 CMI Source IDs that will increment the PWM_PROGRAMMABLE_REQCOUNT_0_0_0_MCHBAR[1] counter. When a new CMI request enters MC that has a Source ID matching either CMI_Source_ID2 or CMI_Source_ID3 the counter will be incremented by 1. The default is the CMI Source ID of IOP (IO Port).
9:5	01h RW	**CMI Source ID1 (CMI_SOURCE_ID1):** Holds 1 of 2 CMI Source IDs that will increment the PWM_PROGRAMMABLE_REQCOUNT_0_0_0_MCHBAR[0] counter. When a new CMI request enters MC that has a Source ID matching either CMI_Source_ID0 or CMI_Source_ID1 the counter will be incremented by 1. The default is the CMI Source ID of IDP1 (IDI Port 1).

Bit Range	Default & Access	Field Name (ID): Description
4:0	00h RW	**CMI Source ID0 (CMI_SOURCE_ID0):** Holds 1 of 2 CMI Source IDs that will increment the PWM_PROGRAMMABLE_REQCOUNT_0_0_0_MCHBAR[0] counter. When a new CMI request enters MC that has a Source ID matching either CMI_Source_ID0 or CMI_Source_ID1 the counter will be incremented by 1. The default is the CMI Source ID of IDP0 (IDI Port 0).

3.2.25 PWM TOTAL REQCOUNT 0 0 0 MCHBAR (PWM_TOTAL_REQCOUNT_0_0_0_MCHBAR) — Offset D840h

Counts every 64B CMI read and write request entering the Memory Controller to DRAM (sum of all channels). Each write request counts as a new request incrementing this counter. However, same-cache-line write requests (both full and partial) are combined to a single 64-byte data transfer to DRAM. Therefore multiplying the number of requests by 64-bytes will lead to inaccurate memory bandwidth. The inaccuracy is proportional to the number of same-cache-line writes. If a SOC has multiple MCs instantiated all instances of this counter will need to be added together to get total CMI request bandwidth.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + D840h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000h RW/V	**count reg (COUNT):** Count of the total number of 64B CMI read and write requests entering this MC.

3.2.26 PWM PROGRAMMABLE REQCOUNT 0 0 0 MCHBAR (PWM_PROGRAMMABLE_REQCOUNT_0_0_0_MCHBAR[0]) — Offset D848h

Counts every 64B CMI read and write request entering the Memory Controller to DRAM (sum of all channels) from up to two programmable CMI Source IDs, contained in PWM_PROGRAMMABLE_REQCOUNT_CONFIG_0_0_0_MCHBAR CR. Each write request counts as a new request incrementing this counter. However, same-cache-line write requests (both full and partial) are combined to a single 64-byte data transfer to DRAM. Therefore multiplying the number of requests by 64-bytes will lead to inaccurate

memory bandwidth. The inaccuracy is proportional to the number of same-cache-line writes. If a SOC has multiple MCs instantiated all instances of this counter will need to be added together to get the sum of the requests from the programmable sources.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + D848h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000h RW/V	**count reg (COUNT):** Count of the number of 64B CMI read and write requests entering this MC from up to two programmable CMI Source IDs, contained in PWM_PROGRAMMABLE_REQCOUNT_CONFIG_0_0_0_MCHBAR CR.

3.2.27 PWM PROGRAMMABLE REQCOUNT 0 0 0 MCHBAR (PWM_PROGRAMMABLE_REQCOUNT_0_0_0_MCHBAR[1]) — Offset D850h

Counts every 64B CMI read and write request entering the Memory Controller to DRAM (sum of all channels) from up to two programmable CMI Source IDs, contained in PWM_PROGRAMMABLE_REQCOUNT_CONFIG_0_0_0_MCHBAR CR. Each write request counts as a new request incrementing this counter. However, same-cache-line write requests (both full and partial) are combined to a single 64-byte data transfer to DRAM. Therefore multiplying the number of requests by 64-bytes will lead to inaccurate memory bandwidth. The inaccuracy is proportional to the number of same-cache-line writes. If a SOC has multiple MCs instantiated all instances of this counter will need to be added together to get the sum of the requests from the programmable sources.

Note: **NOTE:** Bit definitions are the same as PWM_PROGRAMMABLE_REQCOUNT_0_0_0_MCHBAR[0], offset D848h.

3.2.28 PWM RDCAS COUNT 0 0 0 MCHBAR (PWM_RDCAS_COUNT_0_0_0_MCHBAR) — Offset D858h

Counts every read (RdCAS) issued by the Memory Controller to DRAM (sum of all channels). All requests result in 64-byte data transfers from DRAM. Use for accurate memory bandwidth calculations.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + D858h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RW/V	**count reg (COUNT):** Number of accesses

3.2.29 PM SREF config 0 0 0 MCHBAR (PM_SREF_CONFIG_0_0_0_MCHBAR) — Offset D860h

Self refresh mode control register - defines if and when DDR can go into SR

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D860h	00000200h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0200h RW/V	**Idle timer (IDLE_TIMER):** This value is used when the SREF_enable field is set. It defines the number of cycles that there should not be any transaction in order to enter self-refresh. Supported range is 512 to 64K-1

3.2.30 ECC Inj Addr Compare 0 0 0 MCHBAR (ECC_INJ_ADDR_COMPARE_0_0_0_MCHBAR) — Offset D888h

Address compare for ECC error inject. Error injection is issued when

ECC_Inj_Addr_Compare[32:0] = ADDR[38:6] AND ECC_Inj_Addr_Mask[32:0]

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + D888h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:33	0h RO	**Reserved**
32:0	000000000h RW	**Address reg (ADDRESS):** Inject error when ECC_Inj_Addr_Compare[32:0] = ADDR[38:6] AND ECC_Inj_Addr_Mask[31:0]

3.2.31 REMAPBASE 0 0 0 MCHBAR (REMAPBASE_0_0_0_MCHBAR) — Offset D890h

MMIO copy of REMAPBASE_0_0_0_PCI

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + D890h	0000007FFFF00000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:20	7FFFFh RW	**REMAPBASE reg (REMAPBASE):** The value in this register defines the lower boundary of the Remap window. The Remap window is inclusive of this address. In the decoder A[19:0] of the Remap Base Address are assumed to be 0's. Thus the bottom of the defined memory range will be aligned to a 1MB boundary. When the value in this register is greater than the value programmed into the Remap Limit register, the Remap window is disabled. These bits are Intel TXT lockable.

Bit Range	Default & Access	Field Name (ID): Description
19:0	0h RO	**Reserved**

3.2.32 REMAPLIMIT 0 0 0 MCHBAR (REMAPLIMIT_0_0_0_MCHBAR) — Offset D898h

MMIO copy of REMAPLIMIT_0_0_0_PCI

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + D898h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:20	00000h RW	**REMAPLMT reg (REMAPLMT):** The value in this register defines the upper boundary of the Remap window. The Remap window is inclusive of this address. In the decoder A[19:0] of the remap limit address are assumed to be F's. Thus the top of the defined range will be one byte less than a 1MB boundary. When the value in this register is less than the value programmed into the Remap Base register, the Remap window is disabled. These Bits are Intel TXT lockable.
19:0	0h RO	**Reserved**

3.2.33 PWM WRCAS COUNT 0 0 0 MCHBAR (PWM_WRCAS_COUNT_0_0_0_MCHBAR) — Offset D8A0h

Counts every write (WrCAS) issued by the Memory Controller to DRAM (sum of all channels). All requests result in 64-byte data transfers from DRAM. Use for accurate memory bandwidth calculations.

Note: **NOTE:** Bit definitions are the same as PWM_RDCAS_COUNT_0_0_0_MCHBAR, offset D858h.

3.2.34 PWM COMMAND COUNT 0 0 0 MCHBAR (PWM_COMMAND_COUNT_0_0_0_MCHBAR) — Offset D8A8h

Request counter used by PCU for estimation of MC & MCIO power consumption and its sources. There are 3 registers for sources and three registers for MC Operations. Sources:

GT

IA

IO

MC Operations:

RD data

WR data

Command

Note: **NOTE:** Bit definitions are the same as PWM_RDCAS_COUNT_0_0_0_MCHBAR, offset D858h.

3.2.35 ECC Inj Addr Mask 0 0 0 MCHBAR (ECC_INJ_ADDR_MASK_0_0_0_MCHBAR) — Offset D958h

Address compare for ECC error inject. Error injection is issued when

ECC_Inj_Addr_Compare[32:0] = ADDR[38:6] AND ECC_Inj_Addr_Mask[32:0]

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + D958h	00000001FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:33	0h RO	**Reserved**
32:0	1FFFFFFFFh RW	**Address reg (ADDRESS):** Inject error when ECC_Inj_Addr_Compare[32:0] = ADDR[38:6] AND ECC_Inj_Addr_Mask[32:0]

3.2.36 MAD MC HASH 0 0 0 MCHBAR (MAD_MC_HASH_0_0_0_MCHBAR) — Offset D9B8h

This register holds parameters used by the CMI slice selection. transforming from HPA (Host Physical Address)-->CCA (CMI compresed address)

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D9B8h	00000006h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RW	**Stacked Mode (STACKED_MODE):** Working in stacked mode, this MC handles the high address bits and will decrement Zone1_start/2 from the recived address
12:4	000h RW	**Zone1 start (ZONE1_START):** Address in GB of the non-interleaved portion of non-symmetric memory. i.e. in case slice 0 has 32 GB and slice 1 has 8 G, then start of non-symmetric memory is 16GB so Zone1_start=0x10. if the memory is symmetric, Zone1_start is set to memory size (i.e. for total capacity of 64GB Zone1_start=0x40)
3:1	3h RW	**Hash LSB (HASH_LSB):** LSB used in MCI hashing between the two MCs. the Hash bit should be removed from the address in order to get a conseutive address in the MC space. Encoding: 000 - address bit 6 001 - address bit 7 ... 111 - address bit 13
0	0h RW	**Hash enabled (HASH_ENABLED):** Hasing in Zone0 between the two MC is enabled

3.2.37 PMON GLOBAL CONTROL 0 0 0 MCHBAR (PMON_GLOBAL_CONTROL_0_0_0_MCHBAR) — Offset D9C0h

Configuration register for chasis PMON. no central Pmon unit implemented so this register is also a part of MC.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D9C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW/V	**Global reset ctrs (GLOBAL_RESET_CTRS):** when set to 1, the counter registers of all units will be reseted to 0. This bit is self clearing.
1	0h RW/V	**Global reset ctrl (GLOBAL_RESET_CTRL):** when set to 1, the counter control registers of all pmons will be reseted to 0. This bit is self clearing.
0	0h RW	**global freeze (GLOBAL_FREEZE):** Freeze. if set to 1, the counters in all units will stop counting and keep their value.

3.2.38 PMON UNIT CONTROL 0 0 0 MCHBAR (PMON_UNIT_CONTROL_0_0_0_MCHBAR) — Offset D9C4h

Configuration register for PMON Unit (holds several coutners)

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D9C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9	0h RW/V	**reset ctrs (RESET_CTRS):** when set to 1, the counter registers will be reseted to 0. This bit is self clearing.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/V	**reset ctrl (RESET_CTRL):** when set to 1, the counter control registers will be reseted to 0. This bit is self clearing.
7:1	0h RO	**Reserved**
0	0h RW	**frz reg (FRZ):** Freeze. if set to 1, the counters in this unit will stop counting and keep their value.

3.2.39 PMON COUNTER CONTROL 0 0 0 MCHBAR (PMON_COUNTER_CONTROL_0_0_0_MCHBAR[0]) — Offset D9D0h

Configuration register for PMON_COUNTER_DATA

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + D9D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW/V	**edge det (EDGE_DET):** Edge Detect. when set to 1, rather than measuring the event in each cycle it's asserted, the corrosponding counter will increment when a 0 to 1 transition (i.e. rising edge) is detected.
17	0h RW/V	**rst reg (RST):** Reset when set to 1, the corrosponding coutner will be cleared to 0. this bit is self clearing
16:12	0h RO	**Reserved**
11:8	0h RW/V	**ch mask (CH_MASK):** select which channel or sub channel is counted, or both. In channel events bits [9:8] (lsb) mask the channel, in sub-channel events bits [11:8] mask [ch1-subch1, ch1-subch0, ch0-subch1, ch1-subch0]. To mask out a channel (or sub channel) set the according bit to 0x1. Events that can increment by more than 1 per cycle should set mask to 0x0.
7:0	00h RW/V	**ev sel (EV_SEL):** Event select. Select which of the available events should be recorded in the paired data register. additional bits in the control register may also be required to select from the available events. 0x0 --> disable counter 0x1 --> count local clock ticks

3.2.40 PMON COUNTER CONTROL 0 0 0 MCHBAR (PMON_COUNTER_CONTROL_0_0_0_MCHBAR[1]) — Offset D9D4h

Configuration register for PMON_COUNTER_DATA

Note: **NOTE:** Bit definitions are the same as PMON_COUNTER_CONTROL_0_0_0_MCHBAR[0], offset D9D0h.

3.2.41 PMON COUNTER CONTROL 0 0 0 MCHBAR (PMON_COUNTER_CONTROL_0_0_0_MCHBAR[2]) — Offset D9D8h

Configuration register for PMON_COUNTER_DATA

Note: **NOTE:** Bit definitions are the same as PMON_COUNTER_CONTROL_0_0_0_MCHBAR[0], offset D9D0h.

3.2.42 PMON COUNTER CONTROL 0 0 0 MCHBAR (PMON_COUNTER_CONTROL_0_0_0_MCHBAR[3]) — Offset D9DCh

Configuration register for PMON_COUNTER_DATA

Note: **NOTE:** Bit definitions are the same as PMON_COUNTER_CONTROL_0_0_0_MCHBAR[0], offset D9D0h.

3.2.43 PMON COUNTER CONTROL 0 0 0 MCHBAR (PMON_COUNTER_CONTROL_0_0_0_MCHBAR[4]) — Offset D9E0h

Configuration register for PMON_COUNTER_DATA

Note: **NOTE:** Bit definitions are the same as PMON_COUNTER_CONTROL_0_0_0_MCHBAR[0], offset D9D0h.

3.2.44 PMON COUNTER DATA 0 0 0 MCHBAR (PMON_COUNTER_DATA_0_0_0_MCHBAR[0]) — Offset D9E8h

performance monitor counter

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + D9E8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000h RW/V	**event count (EVENT_COUNT):** number of event occurrences

3.2.45 PMON COUNTER DATA 0 0 0 MCHBAR (PMON_COUNTER_DATA_0_0_0_MCHBAR[1]) — Offset D9F0h

performance monitor counter

Note: **NOTE:** Bit definitions are the same as PMON_COUNTER_DATA_0_0_0_MCHBAR[0], offset D9E8h.

3.2.46 PMON COUNTER DATA 0 0 0 MCHBAR (PMON_COUNTER_DATA_0_0_0_MCHBAR[2]) — Offset D9F8h

performance monitor counter

Note: **NOTE:** Bit definitions are the same as PMON_COUNTER_DATA_0_0_0_MCHBAR[0], offset D9E8h.

3.2.47 PMON COUNTER DATA 0 0 0 MCHBAR (PMON_COUNTER_DATA_0_0_0_MCHBAR[3]) — Offset DA00h

performance monitor counter

Note: **NOTE:** Bit definitions are the same as PMON_COUNTER_DATA_0_0_0_MCHBAR[0], offset D9E8h.

3.2.48 PMON COUNTER DATA 0 0 0 MCHBAR (PMON_COUNTER_DATA_0_0_0_MCHBAR[4]) — Offset DA08h

performance monitor counter

Note: **NOTE:** Bit definitions are the same as PMON_COUNTER_DATA_0_0_0_MCHBAR[0], offset D9E8h.

3.2.49 OS TELEMETRY CONTROL 0 0 0 MCHBAR (OS_TELEMETRY_CONTROL_0_0_0_MCHBAR) — Offset DA10h

This Register enable telemetry counters:

PWM_DDR_SUBCHx_ACT_COUNTER_0_0_0_MCHBAR

PWM_DDR_SUBCHx_RRDATA_COUNTER_0_0_0_MCHBAR

PWM_DDR_SUBCHx_WRDATA_COUNTER_0_0_0_MCHBAR

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + DA10h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**Enable OS Telemetry (ENABLEOSTELEMETRY):** Enable OS Telemetry of : PWM_DDR_SUBCHx_ACT_COUNTER_0_0_0_MCHBAR PWM_DDR_SUBCHx_RDDATA_COUNTER_0_0_0_MCHBAR PWM_DDR_SUBCHx_WRDATA_COUNTER_0_0_0_MCHBAR

3.2.50 TC PRE 0 0 0 MCHBAR (TC_PRE_0_0_0_MCHBAR) — Offset E000h

DDR timing constraints related to PRE commands

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + E000h	104070180040C008h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63	0h RO	**Reserved**
62:59	2h RW	**derating ext (DERATING_EXT):** Holds LPDDR timing parameters derating tRAS, tRRD, tRP and tRCD in tCK (WCK for LPDDR5) cycles. When LPDDR is hot, this value is added to the appropriate timing parameters. For non LP devices program the field to 0. Supported range is 0-4.
58:51	08h RW	**tRCD reg (TRCD):** Holds DDR timing parameter tRCD ACT to CAS (RD or WR) same bank minimum delay in tCK (WCK for LPDDR5) cycles. Supported range is 8-59.
50:42	01Ch RW	**tRAS reg (TRAS):** Holds DDR timing parameter tRAS. ACT to PRE same bank minimum delay in tCK (WCK for LPDDR5) cycles. For DDR/LPDDR Supported range is 28-136
41:32	018h RW	**tWRPRE reg (TWRPRE):** Holds DDR timing parameter tWRPRE. WR to PRE same bank minimum delay in tCK (WCK for LPDDR5) cycles. Supported range is 18-200.
31:24	0h RO	**Reserved**
23:20	4h RW	**tPPD reg (TPPD):** Holds DDR timing parameter tPPD. PRE/PREALL to PRE/PREALL (same rank) minimum delay in tCK (WCK for LPDDR5) cycles. Supported range is 4-7. Note this register is not used in DDR5";
19:13	06h RW	**tRDPRE reg (TRDPRE):** Holds DDR timing parameter tRDPRE. RD to PRE same bank minimum delay in tCK (WCK for LPDDR5) cycles. Supported range is 4-32.

Bit Range	Default & Access	Field Name (ID): Description
12:8	00h RW	**tRPab ext (TRPAB_EXT):** Holds the value of tRPab-tRPpb for LPDDR in tCK (WCK for LPDDR5) cycles. LPDDR technologies requires a longer time from PREALL to ACT vs. PRE to ACT, the offset between the two should be programmed to this field. When using DDR4 this field should be programmed to 0. For LPDDR4 the following restrictions apply: For single/dual rank sub channels tRP-tRPab_ext > 6. For three/four ranks sub channels tRP-tRPab_ext > 8. Supported range is 0-6.
7:0	08h RW	**tRP reg (TRP):** Holds DDR timing parameter tRP (and tRCD). PRE to ACT same bank minimum delay in tCK (WCK for LPDDR5) cycles. ACT to CAS (RD or WR) same bank minimum delay in tCK (WCK for LPDDR5) cycles. Supported range is 8-60.

3.2.51 TC ACT 0 0 0 MCHBAR (TC_ACT_0_0_0_MCHBAR) — Offset E008h

DDR timing constraints related to ACT commands

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E008h	18020810h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	18h RW	**trefsbrd reg (TREFSBRD):** enforces min delay from refsb to act. specified in tCK
23:22	0h RO	**Reserved**
21:15	04h RW	**tRRD dg (TRRD_DG):** Holds DDR timing parameter tRRD. ACT to ACT (different bank group in DDR4/DDR5) minimum delay in tCK (WCK for LPDDR5) cycles. Supported range is 4-32.
14:9	04h RW	**tRRD sg (TRRD_SG):** Holds DDR timing parameter tRRD/tRRD_L. For LPDDR5 program tRRD, for DDR4/DDR5 program tRRD_L. ACT to ACT (same bank group in DDR4/DDR5) minimum delay in tCK (WCK for LPDDR5) cycles. Supported range is 4-32.
8:0	010h RW	**tFAW reg (TFAW):** Holds DDR timing parameter tFAW (four activates window). In tCK (WCK for LPDDR5) cycles Supported range is 16-88.

3.2.52 TC RDRD 0 0 0 MCHBAR (TC_RDRD_0_0_0_MCHBAR) — Offset E00Ch

DDR timing constraints related to timing between read and read transactions

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E00Ch	04040484h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	04h RW	**tRDRD dd (TRDRD_DD):** Minimum delay from RD to RD to the other DIMM in tCK (WCK for LPDDR5) cycles. Supported range is 4-54.
23:16	04h RW	**tRDRD dr (TRDRD_DR):** Minimum delay from RD to RD to the other rank in the same DIMM in tCK (WCK for LPDDR5) cycles. Supported range is 4-54.
15	0h RO	**Reserved**
14:8	04h RW	**tRDRD dg (TRDRD_DG):** LPDDR5: Minimum delay from RD to RD to different banks in tCK (WCK for LPDDR5) cycles. DDR4/DDR5: Minimum delay from RD to RD to different bank groups in tCK cycles. Supported range is 4-54.
7	1h RW	**Allow 2cyc B2B LPDDR (ALLOW_2CYC_B2B_LPDDR):** LPDDR5: in MPR mode reads are working on BL16. in Gear4 that means 2Dclks apart reads. this bit enable this clearing this bit will prevent LPDDR from schedule a read 2 Dclks after anotehr Read
6:0	04h RW	**tRDRD sg (TRDRD_SG):** LPDDR5: Minimum delay from RD to RD to the same bank in tCK (WCK for LPDDR5) cycles. DDR4/DDR5: Minimum delay from RD to RD to the same bank group in tCK cycles. Supported range is 4-54.

3.2.53 TC RDWR 0 0 0 MCHBAR (TC_RDWR_0_0_0_MCHBAR) — Offset E010h

DDR timing constraints related to timing between read and write transactions

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E010h	04040404h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	04h RW	**tRDWR dd (TRDWR_DD):** Minimum delay from RD to WR to the other DIMM in tCK (WCK for LPDDR5) cycles. Supported range is 4-54.
23:16	04h RW	**tRDWR dr (TRDWR_DR):** Minimum delay from RD to WR to the other rank in the same DIMM in tCK (WCK for LPDDR5) cycles. Supported range is 4-54.
15:8	04h RW	**tRDWR dg (TRDWR_DG):** LPDDR5: Minimum delay from RD to WR to different banks in tCK (WCK for LPDDR5) cycles. DDR4/DDR5: Minimum delay from RD to WR to different bank groups in tCK cycles. Supported range is 4-54.
7:0	04h RW	**tRDWR sg (TRDWR_SG):** LPDDR5: Minimum delay from RD to WR to the same bank in tCK (WCK for LPDDR5) cycles. DDR4/DDR5: Minimum delay from RD to WR to the same bank group in tCK cycles. Supported range is 4-54.

3.2.54 TC WRRD 0 0 0 MCHBAR (TC_WRRD_0_0_0_MCHBAR) — Offset E014h

DDR timing constraints related to timing between write and read transactions

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E014h	08100804h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:25	04h RW	**tWRRD dd (TWRRD_DD):** Minimum delay from WR to RD to the other DIMM in tCK (WCK for LPDDR5) cycles. Supported range is 4-54.
24:18	04h RW	**tWRRD dr (TWRRD_DR):** Minimum delay from WR to RD to the other rank in the same DIMM in tCK (WCK for LPDDR5) cycles. Supported range is 4-54.
17:9	004h RW	**tWRRD dg (TWRRD_DG):** LPDDR5: Minimum delay from WR to RD to different banks in tCK (WCK for LPDDR5) cycles. DDR4/DDR5: Minimum delay from WR to RD to different bank groups in tCK cycles. Supported range is 4-65.
8:0	004h RW	**tWRRD sg (TWRRD_SG):** LPDDR5: Minimum delay from WR to RD to the same bank in tCK (WCK for LPDDR5) cycles. DDR4/DDR5: Minimum delay from WR to RD to the same bank group in tCK cycles. Supported range is 4-145.

3.2.55 TC WRWR 0 0 0 MCHBAR (TC_WRWR_0_0_0_MCHBAR) — Offset E018h

DDR timing constraints related to timing between write and write transactions

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E018h	04040404h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	04h RW	**tWRWR dd (TWRWR_DD):** Minimum delay from WR to WR to the other DIMM in tCK (WCK for LPDDR5) cycles. Supported range is 4-54.
23	0h RO	**Reserved**
22:16	04h RW	**tWRWR dr (TWRWR_DR):** Minimum delay from WR to WR to the other rank in the same DIMM in tCK (WCK for LPDDR5) cycles. Supported range is 4-54.
15	0h RO	**Reserved**
14:8	04h RW	**tWRWR dg (TWRWR_DG):** LPDDR5: Minimum delay from WR to WR to different banks in tCK (WCK for LPDDR5) cycles. DDR4/DDR5: Minimum delay from WR to WR to different bank groups in tCK cycles. Supported range is 4-54.
7	0h RO	**Reserved**
6:0	04h RW	**tWRWR sg (TWRWR_SG):** LPDDR5: Minimum delay from WR to WR to the same bank in tCK (WCK for LPDDR5) cycles. DDR4/DDR5: Minimum delay from WR to WR to the same bank group in tCK cycles. Supported range is 4-54.

3.2.56 SC Roundtrip latency 0 0 0 MCHBAR (SC_ROUNDTRIP_LATENCY_0_0_0_MCHBAR) — Offset E020h

Read Round-trip latency per rank

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + E020h	1919191919191919h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:56	19h RW	**Rank 7 latency (RANK_7_LATENCY):** Latency from read command to rank 7 until first data chunk return to MC in QCLK cycles This field is used for LPDDR4 Sub channel 1 rank 3 (which is indicated by rank = 3 BG[1]=1) Supported range is 19-120.
55:48	19h RW	**Rank 6 latency (RANK_6_LATENCY):** Latency from read command to rank 6 until first data chunk return to MC in QCLK cycles This field is used for LPDDR Sub channel 1 rank 2 (which is indicated by rank = 2 BG[1]=1) Supported range is 19-120.
47:40	19h RW	**Rank 5 latency (RANK_5_LATENCY):** Latency from read command to rank 5 until first data chunk return to MC in QCLK cycles This field is used for LPDDR Sub channel 0 rank 3 (which is indicated by rank = 1 BG[1]=1) Supported range is 19-120.
39:32	19h RW	**Rank 4 latency (RANK_4_LATENCY):** Latency from read command to rank 4 until first data chunk return to MC in QCLK cycles This field is used for LPDDR Sub channel 0 rank 2 (which is indicated by rank = 0 BG[1]=1) Supported range is 19-120.
31:24	19h RW	**Rank 3 latency (RANK_3_LATENCY):** Latency from read command to rank 3 until first data chunk return to MC in QCLK cycles Supported range is 19-120.
23:16	19h RW	**Rank 2 latency (RANK_2_LATENCY):** Latency from read command to rank 2 until first data chunk return to MC in QCLK cycles Supported range is 19-120.
15:8	19h RW	**Rank 1 latency (RANK_1_LATENCY):** Latency from read command to rank 1 until first data chunk return to MC in QCLK cycles Supported range is 19-120.

Bit Range	Default & Access	Field Name (ID): Description
7:0	19h RW	**Rank 0 latency (RANK_0_LATENCY):** Latency from read command to rank 0 until first data chunk return to MC in QCLK cycles Supported range is 19-120.

3.2.57 ECCERRLOG0 0 0 0 MCHBAR (ECCERRLOG0_0_0_0_MCHBAR) — Offset E048h

This register logs ECC error information.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E048h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO/V/P	**ERRBANK reg (ERRBANK):** This field holds the Bank Address of the read transaction that had the ECC error.
28:27	0h RO/V/P	**ERRRANK reg (ERRRANK):** This field holds the Rank ID of the read transaction that had the ECC error. if ddr_1dpc_split_ranks_on_subch feature is enabled then rank 1 is actually logged as rank 3.
26:24	0h RO/V/P	**ERRCHUNK reg (ERRCHUNK):** Holds the chunk number of the error stored in the register.
23:16	00h RO/V/P	**ERRSYND reg (ERRSYND):** This field contains the error syndrome. A value of 0xFF indicates that the error is due to poisoning.
15:4	0h RO	**Reserved**
3	0h RW/1C/V/P	**MERR OVERFLOW (MERR_OVERFLOW):** This bit is set when a correctable single-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked to further single bit errors, until this bit is cleared. A multiple bit error that occurs after this bit is set will override the address/error syndrome information. This bit is cleared when the corresponding bit in 0.0.0.PCI.ERRSTS is cleared.
2	0h RW/1C/V/P	**MERRSTS reg (MERRSTS):** This bit is set when an uncorrectable multiple-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked until this bit is cleared. This bit is cleared when the corresponding bit in 0.0.0.PCI.ERRSTS is cleared.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW/1C/V/P	**CERR OVERFLOW (CERR_OVERFLOW):** This bit is set when a correctable single-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked to further single bit errors, until this bit is cleared. A multiple bit error that occurs after this bit is set will override the address/error syndrome information. This bit is cleared when the corresponding bit in 0.0.0.PCI.ERRSTS is cleared.
0	0h RW/1C/V/P	**CERRSTS reg (CERRSTS):** This bit is set when a correctable single-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked to further single bit errors, until this bit is cleared. A multiple bit error that occurs after this bit is set will override the address/error syndrome information. This bit is cleared when the corresponding bit in 0.0.0.PCI.ERRSTS is cleared.

3.2.58 ECCERRLOG1 0 0 0 MCHBAR (ECCERRLOG1_0_0_0_MCHBAR) — Offset E04Ch

This register logs ECC error information.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E04Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO/V/P	**ERRBANKGROUP reg (ERRBANKGROUP):** This field holds the DRAM bank group address of the read transaction that had the ECC error.
28:18	000h RO/V/P	**ERRCOL reg (ERRCOL):** This field holds the DRAM column address of the read transaction that had the ECC error.
17:0	00000h RO/V/P	**ERRROW reg (ERRROW):** This field holds the DRAM row (page) address of the read transaction that had the ECC error.

3.2.59 TC PWRDN 0 0 0 MCHBAR (TC_PWRDN_0_0_0_MCHBAR) — Offset E050h

DDR timing constraints related to power down

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + E050h	0804100400810204h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:59	01h RW	**tPRPDEN reg (TPRPDEN):** This this CR covers Any CMD --> PDE timing in tCK (WCK for LPDDR5) Note this CR must be programmed to a minimum of 4 in Gear2 and a minimum of 2 in Gear1 Note for LP5 we need to program as follows LPDDR5: tCMDPDE +4
58:54	0h RO	**Reserved**
53:48	04h RW	**tCSL reg (TCSL):** Chip Select low pulse width on power down exit (specified in DCLKs) :this is a fixed spec value (and in LPDDR5 this value is in resolution of tCK or multiples of 4WCK) and the value programmed in the register is in MC DCLKs / WCK Note: it should also be noted that tCSL covers for both tCSL and tCSCAL in LPDDR5.
47:42	04h RW	**tCSH reg (TCSH):** Chip Select high pulse width on power down exit (specified in DCLKs) : this is a fixed spec value (and LPDDR5 this value is in resolution of tCK or multiples of 4WCK) .The Final value programmed in the register is in MC DCLKs/WCK
41:32	004h RW	**tWRPDEN reg (TWRPDEN):** Holds DDR timing parameter tWRPDEN. WR to power down minimum delay in tCK (WCK for LPDDR5) cycles. Supported range is 4-204.
31:29	0h RO	**Reserved**
28:21	04h RW	**tRDPDEN reg (TRDPDEN):** Holds DDR timing parameter for tRDPDEN. RD to power down minimum delay in tCK (WCK for LPDDR5) cycles. Supported range is 4-100. Notes: because CKE power down is asynchrnous CKE may drop on the negedge of the clock so we need to add +1 in LPDDR4 in LPDDR4 need to pad an additional +1 to the formula
20:14	04h RW	**tXPDLL reg (TXPDLL):** Holds DDR timing parameter tXP. Power up to RD/WR minimum delay in tCK (WCK for LPDDR5) cycles. Applicable for DDR4 in case of exit from PPD when DRAM is configured to slow-exit mode. Supported range is 4-63.

Bit Range	Default & Access	Field Name (ID): Description
13:7	04h RW	**tXP reg (TXP):** Holds DDR timing parameter tXP. Power up to any command minimum delay in tCK /WCK cycles. Supported range is 4-24.
6:0	04h RW	**tCKE reg (TCKE):** Holds DDR timing parameter tCKE. Power down to power up (and vice versa) minimum delay in tCK (WCK for LPDDR5) cycles. Note that for LPDDR4 this value is also used for tCKCKEL and tCKELCMD. Supported range is 4-24.

3.2.60 TC ODT 0 0 0 MCHBAR (TC_ODT_0_0_0_MCHBAR) — Offset E070h

ODT timing related parameters

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + E070h	0000000006050000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:32	0h RO	**Reserved**
31:24	06h RW	**tCWL reg (TCWL):** Holds DDR timing parameter tCWL (sometimes referred to as tWCL). Write command to data delay in tCK (WCK for LPDDR5) cycles. Supported range is 4-64 (maximum is for 1N mode) For LPDDR4 the minimum supported value is 4. For DDR4 the minimum supported value is 5.
23	0h RO	**Reserved**
22:16	05h RW	**tCL reg (TCL):** Holds DDR timing parameter tCL. Read command to data delay in tCK (WCK for LPDDR5) cycles. Supported range is 4-72.
15:0	0h RO	**Reserved**

3.2.61 SC ODT MATRIX 0 0 0 MCHBAR (SC_ODT_MATRIX_0_0_0_MCHBAR) — Offset E080h

ODT matrix (enabled using SC_GS_CFG_0_0_0_MCHBAR.enable_odt_matrix)

Note : In DDR5 this matrix should only be used for non target ODT (target ODT should not be specified in this register)

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Write Rank 3 (WRITE_RANK_3):** Indicate which ranks should terminate when writing to rank 3 (bits 3:0 correspond to ODT pins 3:0). Note : In DDR5 this register should only be used for non target ODT (target ODT should not be specified in this register)
27:24	0h RW	**Write Rank 2 (WRITE_RANK_2):** Indicate which ranks should terminate when writing to rank 2 (bits 3:0 correspond to ODT pins 3:0). Note : In DDR5 this register should only be used for non target ODT (target ODT should not be specified in this register)
23:20	0h RW	**Write Rank 1 (WRITE_RANK_1):** Indicate which ranks should terminate when writing to rank 1 (bits 3:0 correspond to ODT pins 3:0). Note : In DDR5 this register should only be used for non target ODT (target ODT should not be specified in this register)
19:16	0h RW	**Write Rank 0 (WRITE_RANK_0):** Indicate which ranks should terminate when writing to rank 0 (bits 3:0 correspond to ODT pins 3:0). Note : In DDR5 this register should only be used for non target ODT
15:12	0h RW	**Read Rank 3 (READ_RANK_3):** Indicate which ranks should terminate when reading from rank 3 (bits 3:0 correspond to ODT pins 3:0) Note that according to DRAM spec the target rank should not be terminated.
11:8	0h RW	**Read Rank 2 (READ_RANK_2):** Indicate which ranks should terminate when reading from rank 2 (bits 3:0 correspond to ODT pins 3:0) Note that according to DRAM spec the target rank should not be terminated.
7:4	0h RW	**Read Rank 1 (READ_RANK_1):** Indicate which ranks should terminate when reading from rank 1 (bits 3:0 correspond to ODT pins 3:0) Note that according to DRAM spec the target rank should not be terminated.
3:0	0h RW	**Read Rank 0 (READ_RANK_0):** Indicate which ranks should terminate when reading from rank 0 (bits 3:0 correspond to ODT pins 3:0) Note that according to DRAM spec the target rank should not be terminated.

3.2.62 SC GS CFG 0 0 0 MCHBAR (SC_GS_CFG_0_0_0_MCHBAR) — Offset E088h

Regsiter for Scheduler configuration

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + E088h	0100000000000020h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:61	0h RO	**Reserved**
60:56	01h RW	**Used for tCPDED timing parameter (TCPDED):** Holds DDR timing parameter tCPDED. Power down to command bus tri-state delay in tCK cycles (for DDR4 only) Supported range is 0-7 in 1N mode.
55	0h RO	**Reserved**
54	0h RW	**Used for WCKDiffLowInIdle (WCKDIFFLOWINIDLE):** PHY holds WCK to a differential value instead of turning it off. This register is a shaow copy of the DDRPHY register and should match the POR value of the DDRPHY register. scram_regfile.MCMISCS_DDRWCKCONTROL_0_0_0_MCHBAR.WCkDiffLowInIdle.cfg_val
53:50	0h RO	**Reserved**
49	0h RW	**enable write zero (WRITE0_ENABLE):** enable write0 for power saving. This bit should only be set in normal mode
48:34	0h RO	**Reserved**
33:32	0h RW	**ddr 1dpc split ranks on subch (DDR_1DPC_SPLIT_RANKS_ON_SUBCH):** Performance optimization for 1 DIMM Per Channel (1DPC) with dual rank. To be used only with Intel Memory reference Code as there are couple of low level configurations to enable it. For DDR5 : the only legal configuration is 0x1,0x2. This CR can never be set to '0 for DDR5
31	0h RW	**Work in gear2 mode (GEAR2):** Indicate that MC is working in Gear-2 (Qclk is half the data transfer clock of the DRAM)
30	0h RW	**no gear2 param divide (NO_GEAR2_PARAM_DIVIDE):** Don't do RU[param/2] for DRAM timing parameters when in gear-2, treat the value given in them in DCLKs instead of tCK clocks. For extending the existing ranges (mainly for Overclocking).
29:28	0h RW	**Define a x8 device (X8_DEVICE):** DIMM is made out of X8 devices LSB is for DIMM 0, MSB is for DIMM 1. In DDR5 1DPC, need to configure x8 same for both subch.

Bit Range	Default & Access	Field Name (ID): Description
27:17	0h RO	**Reserved**
16	0h RW	**no gear4 param divide (NO_GEAR4_PARAM_DIVIDE):** Don't do RU[param/4] for DRAM timing paramters when in gear-4, divide only by 2 (RU[param/2]). For extending the existing ranges (mainly OC)
15	0h RW	**Work in gear4 mode (GEAR4):** Indicate that MC is working in Gear-4 (Qclk is quarter the data transfer clock of the DRAM)
14:12	0h RO	**Reserved**
11:8	0h RW	**Used for Define Address mirroring (ADDRESS_MIRROR):** DIMM routing causes address mirroring For DDR4: bit 0: DIMM 0 (rank 1 bus is mirrored) bit 1: DIMM 1 (rank 3 bus is mirrored) For DDR5 bit 0: Rank0 on Dimm0 is mirrored bit 1: Rank1 on Dimm0 is mirrored bit 2: Rank0 on Dimm1 is mirrored (Rank 2) bit 3: Rank1 on Dimm1 is mirrored (Rank 3) For LPDDR4 bit 0: Sub channel 0 ranks 0 and 2 CA bus is mirrored. bit 1: Sub channel 1 ranks 0 and 2 CA bus is mirrored. bit 2: Sub channel 0 ranks 1 and 3 CA bus is mirrored. bit 3: Sub channel 1 ranks 1 and 3 CA bus is mirrored.
7:5	1h RW	**N to 1 ratio (N_TO_1_RATIO):** When using N:1 command stretch mode, every how many B2B valid command cycles a bubble is required Supported range is 1 to 7
4:3	0h RW	**Used for CMD stretch (CMD_STRETCH):** Command stretch mode: 00 - 1N 01 - 2N 10 - 3N 11 - N:1 Notice that in Gear2 MC uses only the low phase of Dclk for commands, effectively doing a 2N by default. setting 2N in Gear2 will result in 4N at DDR interface
2:0	0h RO	**Reserved**

3.2.63 SPID LOW POWER CTL 0 0 0 MCHBAR (SPID_LOW_POWER_CTL_0_0_0_MCHBAR) — Offset E0B8h

This register holds DDRIO timing constraints regarding power modes latnecies.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E0B8h	08104426h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**selfrefresh enable (SELFREFRESH_ENABLE):** allow sending DDRIO self refresh mode indication
30	0h RW	**powerdown enable (POWERDOWN_ENABLE):** allow sending DDRIO CKE power down mode indication
29	0h RW	**idle enable (IDLE_ENABLE):** allow sending DDRIO idle mode indication. Note: LPMODE-1 is not supported in MC
28	0h RW	**ckevalid enable (CKEVALID_ENABLE):** Allow deasserting cke_valid when not toggling CKE pins
27:24	8h RW	**ckevalid length (CKEVALID_LENGTH):** cke_valid pulse length in DCLK cycles
23:20	1h RW	**selfrefresh length (SELFREFRESH_LENGTH):** Minimum time allowed in self refresh mode Units is MC DCLKs (which means gearing is not handled in hardware)
19:14	01h RW	**selfrefresh latency (SELFREFRESH_LATENCY):** Exit latency from self refresh mode till command can be sent in 8xtCK cycles Need to program to a value of 1 as self refresh latency is hidden behind tXSR. This CR should never be programmed to '0
13:10	1h RW	**powerdown length (POWERDOWN_LENGTH):** Minimum time allowed in CKE power down mode. Units is MC DCLKs (which means gearing is not handled in hardware)
9:5	01h RW	**powerdown latency (POWERDOWN_LATENCY):** Exit latency from CKE power down mode till command can be sent in 1xtCK cycles Refer to DDRIO HAS for values to program for this register. This CR should never be programmed to '0
4:1	3h RW	**idle length (IDLE_LENGTH):** Minimum time allowed in idle mode
0	0h RW	**raise cke after exit latency (RAISE_CKE_AFTER_EXIT_LATENCY):** Delay raising of CKE on exit from powerdown and selfrefresh power modes until required latency has passed. If this bit is clear then CKE exit (and tXP) happens in parallel of waking up the PHY, otherwise they happen back to back.

3.2.64 TR RRDVALID ctrl 0 0 0 MCHBAR (TR_RRDVALID_CTRL_0_0_0_MCHBAR) — Offset E104h

This register holds the rrd_valid feature bits

1 trigger signal

1 overflow indication

In 1DPC rank0 of subCh0 and rank3 of subCh1 is used than Trigger signal should be sent to rank0 and rank3 instead of rank and rank1

ERM is not supported

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E104h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW/V	**Rank 7 overflow (RANK_7_OVERFLOW):** Rank 7 overflow indication
22	0h RW	**Rank 7 wr en (RANK_7_WR_EN):** Rank 7 fix enable
21	0h RW/V	**Rank 7 trigger (RANK_7_TRIGGER):** Rank 7 trigger
20	0h RW/V	**Rank 6 overflow (RANK_6_OVERFLOW):** Rank 6 overflow indication
19	0h RW	**Rank 6 wr en (RANK_6_WR_EN):** Rank 6 fix enable
18	0h RW/V	**Rank 6 trigger (RANK_6_TRIGGER):** Rank 6 trigger
17	0h RW/V	**Rank 5 overflow (RANK_5_OVERFLOW):** Rank 5 overflow indication
16	0h RW	**Rank 5 wr en (RANK_5_WR_EN):** Rank 5 fix enable
15	0h RW/V	**Rank 5 trigger (RANK_5_TRIGGER):** Rank 5 trigger
14	0h RW/V	**Rank 4 overflow (RANK_4_OVERFLOW):** Rank 4 overflow indication
13	0h RW	**Rank 4 wr en (RANK_4_WR_EN):** Rank 4 fix enable
12	0h RW/V	**Rank 4 trigger (RANK_4_TRIGGER):** Rank 4 trigger

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/V	**Rank 3 overflow (RANK_3_OVERFLOW):** Rank 3 overflow indication
10	0h RW	**Rank 3 wr en (RANK_3_WR_EN):** Rank 3 fix enable
9	0h RW/V	**Rank 3 trigger (RANK_3_TRIGGER):** Rank 2 trigger
8	0h RW/V	**Rank 2 overflow (RANK_2_OVERFLOW):** Rank 2 overflow indication
7	0h RW	**Rank 2 wr en (RANK_2_WR_EN):** Rank 2 fix enable
6	0h RW/V	**Rank 2 trigger (RANK_2_TRIGGER):** Rank 2 trigger
5	0h RW/V	**Rank 1 overflow (RANK_1_OVERFLOW):** Rank 1 overflow indication
4	0h RW	**Rank 1 wr en (RANK_1_WR_EN):** Rank 1 fix enable
3	0h RW/V	**Rank 1 trigger (RANK_1_TRIGGER):** Rank 1 trigger
2	0h RW/V	**Rank 0 overflow (RANK_0_OVERFLOW):** Rank 0 overflow indication
1	0h RW	**Rank 0 wr en (RANK_0_WR_EN):** Rank 0 fix enable
0	0h RW/V	**Rank 0 trigger (RANK_0_TRIGGER):** Rank 0 trigger

3.2.65 TR RRDVALID data 0 0 0 MCHBAR (TR_RRDVALID_DATA_0_0_0_MCHBAR) — Offset E108h

This register holds the rrd_Valid feature counter sign and value bits

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + E108h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:57	00h RW/V	**Rank 7 value (RANK_7_VALUE):** Rank 7 value
56	0h RW/V	**Rank 6 sign (RANK_7_SIGN):** Rank 7 sign bit
55:49	00h RW/V	**Rank 6 value (RANK_6_VALUE):** Rank 6 value

Bit Range	Default & Access	Field Name (ID): Description
48	0h RW/V	**Rank 6 sign (RANK_6_SIGN):** Rank 6 sign bit
47:41	00h RW/V	**Rank 5 value (RANK_5_VALUE):** Rank 5 value
40	0h RW/V	**Rank 5 sign (RANK_5_SIGN):** Rank 5 sign bit
39:33	00h RW/V	**Rank 4 value (RANK_4_VALUE):** Rank 4 value
32	0h RW/V	**Rank 4 sign (RANK_4_SIGN):** Rank 4 sign bit
31:25	00h RW/V	**Rank 3 value (RANK_3_VALUE):** Rank 3 value
24	0h RW/V	**Rank 3 sign (RANK_3_SIGN):** Rank 3 sign bit
23:17	00h RW/V	**Rank 2 value (RANK_2_VALUE):** Rank 2 value
16	0h RW/V	**Rank 2 sign (RANK_2_SIGN):** Rank 2 sign bit
15:9	00h RW/V	**Rank 1 value (RANK_1_VALUE):** Rank 1 value
8	0h RW/V	**Rank 1 sign (RANK_1_SIGN):** Rank 1 sign bit
7:1	00h RW/V	**Rank 0 value (RANK_0_VALUE):** Rank 0 value
0	0h RW/V	**Rank 0 sign (RANK_0_SIGN):** Rank 0 sign bit

3.2.66 TC REFm 0 0 0 MCHBAR (TC_REFM_0_0_0_MCHBAR) — Offset E40Ch

Per Bank Refresh parameters

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E40Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

3.2.67 MR4 RANK TEMPERATURE 0 0 0 MCHBAR (MR4_RANK_TEMPERATURE_0_0_0_MCHBAR) — Offset E424h

This register holds the latest MR4 read per rank and used to determine the required refresh rate and thermal conditions of the DRAMs.

It should be noted in if the register DDR5_1DPC_split_ranks_across_subch is set then: rank_0 -- holds rank0 temperature and rank_3 holds rank1 temperature

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E424h	03030303h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:24	03h RW/V	**Rank 3 (RANK_3):** Rank 3 refresh rate (MRC should program the temperature appropriately as the reset default may not apply to all techs : for example LPDDR5 1x ref rate is 0xa)
23:21	0h RO	**Reserved**
20:16	03h RW/V	**Rank 2 (RANK_2):** Rank 2 refresh rate, (MRC should program the temperature appropriately as the reset default may not apply to all techs : for example LPDDR5 1x ref rate is 0xa)
15:13	0h RO	**Reserved**
12:8	03h RW/V	**Rank 1 (RANK_1):** Rank 1 refresh rate, (MRC should program the temperature appropriately as the reset default may not apply to all techs : for example LPDDR5 1x ref rate is 0xa)
7:5	0h RO	**Reserved**
4:0	03h RW/V	**Rank 0 (RANK_0):** Rank 0 refresh rate, (MRC should program the temperature appropriately as the reset default may not apply to all techs : for example LPDDR5 1x ref rate is 0xa)

3.2.68 DDR4 MPR RANK TEMPERATURE 0 0 0 MCHBAR (DDR4_MPR_RANK_TEMPERATURE_0_0_0_MCHBAR) — Offset E428h

This register holds the latest temperature read per rank and used to determine the required refresh rate and thermal conditions of the DRAMs.

Encodings are:

00 - Cold (below 45C), single refresh rate required, DRAM may drop refreshes if allowed

01 - Normal operating temperature (45C-85C), single refresh rate, DRAM may drop refreshes if double rate refreshes are given

10 - Hot (Above 85C), double refresh rate

11 - Reserved

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E428h	01010101h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25:24	1h RW/V	**Rank 3 (RANK_3):** Rank 3 refresh rate
23:18	0h RO	**Reserved**
17:16	1h RW/V	**Rank 2 (RANK_2):** Rank 2 refresh rate
15:10	0h RO	**Reserved**
9:8	1h RW/V	**Rank 1 (RANK_1):** Rank 1 refresh rate
7:2	0h RO	**Reserved**
1:0	1h RW/V	**Rank 0 (RANK_0):** Rank 0 refresh rate

3.2.69 TC RFP 0 0 0 MCHBAR (TC_RFP_0_0_0_MCHBAR) — Offset E438h

Register for Refresh parameters

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E438h	2356980Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	23h RW	**Used to define tREFIx9 (TREFIX9):** Maximum time allowed between refreshes to a rank (in intervals of 1024 DCLK cycles). Should be programmed to 8*tREFI/1024 (to allow for possible delays from ZQ or isoc).
23:20	5h RW	**RAISE BLK WAIT for MNT (RAISE_BLK_WAIT):** Number of clocks the Main refresh FSM blocks the rank and waits before it progresses to any mantainance operations. Notes this register defined to allow enough time for MC safe logic to indicate to all downstream agents whether it is safe to issue MNT operations. the pipeline latency is 5 clocks in all cases except for LP5 Gear1 where it can be 7 clocks due to longer autosync read/wriite commands. So this register is specified in MC dclks and hardware will not change it based on gear.
19:18	1h RW	**Used to define SRX Ref Debits (SRX_REF_DEBITS):** Number of Refresh debits to be given on Self refresh exit. Configurable - POR value is 1 for DDR4 and 2 for LPDDR5, DDR5.
17	1h RW	**setting this bit will enable MRS refresh at the begining of MRS flow if the rank reached HP refresh WM (HPREFONMRS):** should be set by default, it's intended for SAGV as MC can enter SR while owing refreshes.
16	0h RW	**setting this bit will enable tREFI counter while MC refresh enable is not set (COUNTTREFIWHILEREFENOFF):** Sometimes refresh enable bit is cleared in order to block maintenance operetions. MC may want to accumulate refresh debt at that time, setting this bit enable it.
15:12	9h RW	**Used to define Refresh panic wm (REFRESH_PANIC_WM):** tREFI count level in which the refresh priority is panic (default is 9). The Maximum value for this field is 9.
11:8	8h RW	**Used to define Refresh HP WM (REFRESH_HP_WM):** tREFI count level that turns the refresh priority to high (default is 8)
7:0	0Fh RW	**Used for OREF RI (OREF_RI):** Rank idle period that defines an opportunity for refresh, in DCLK cycles

3.2.70 TC RFTP 0 0 0 MCHBAR (TC_RFTP_0_0_0_MCHBAR) — Offset E43Ch

Refresh timing parameters

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E43Ch	02D01004h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**

30:18	00B4h
	RW
		tRFC reg (TRFC):
		Time of refresh - from beginning of refresh until next ACT or refresh is allowed (in tCK (WCK for LPDDR5) cycles, default is 180).
		Note:
		// MC hardware has a hardcoded delay of 10 pipeline stages for setting cke to 0 after REFRESH gets issued,
		// and MC asserts cke after tRFC-(tXP+8), so the minimum value of tRFC must be (tXP + 8) + (11*Gear)

17:0	01004h RW	**tREFI reg (TREFI):** Defines the average period between refreshes, and the rate that tREFI counter is incremented (in tCK (WCK for LPDDR5) cycles, default is 4100).

3.2.71 TC SRFTP 0 0 0 MCHBAR (TC_SRFTP_0_0_0_MCHBAR) — Offset E440h

Self-refresh timing parameters

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E440h	00000200h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12:0	0200h RW	**tXSDLL reg (TXSDLL):** Delay between DDR SR exit and the first command that requires data RD/WR from DDR.

3.2.72 MC REFRESH STAGGER 0 0 0 MCHBAR (MC_REFRESH_STAGGER_0_0_0_MCHBAR) — Offset E444h

Refresh stagger control

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E444h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RW	**Trefipulse Stagger Disable (TREFIPULSE_STAGGER_DISABLE):** When set - disables staggering of trefi debits accross ranks
16	0h RW	**Ref Stagger Mode (REF_STAGGER_MODE):** This bit sets the refresh staggering mode, 0 = per DIMM refresh stagger, 1 = per channel refresh stagger
15	0h RW	**Ref Stagger En (REF_STAGGER_EN):** When set this bit enables refresh staggering
14	0h RW	**En Ref Type Display (EN_REF_TYPE_DISPLAY):** This bit when set displays refresh type on the following address pins (DDR4 BG[0],BA[1:0], DDR5 CA[7:6], LPDDR5 CA_1[2:0], 00 = Stolen refresh 01 = Opportunistic Refresh 10 = Hi Priority Refresh 11 = Panic Refresh
13	0h RW	**Disable Stolen Refresh (DISABLE_STOLEN_REFRESH):** This bit when set disables stolen refreshes
12:0	0000h RW	**Ref Interval (REF_INTERVAL):** Refresh Interval period in DCLKS

3.2.73 TC ZQCAL 0 0 0 MCHBAR (TC_ZQCAL_0_0_0_MCHBAR) — Offset E448h

Register for ZQCAL control

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + E448h	0000032000010000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:45	0h RO	**Reserved**
44:32	0320h RW	**Used to define tZQCAL (TZQCAL):** tZQCAL in 2xtCK (2xWCK for LPDDR5) cycles. Used for LP4/5 and DDR5.
31:21	0h RO	**Reserved**
20:10	040h RW	**Used to define tZQCS (TZQCS):** For DDR4 this field tracks tZQCS timing, programmed in units of tCK. For all other DRAM techs this field tracks tZQLAT timing. In LPDDR5 this field is programmed in units of WCK, otherwise it is programmed in units of tCK.
9:0	0h RO	**Reserved**

3.2.74 MC Init State 0 0 0 MCHBAR (MC_INIT_STATE_0_0_0_MCHBAR) — Offset E454h

Holds information on available ranks

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E454h	0000000Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
7:0	0Fh RW	**Rank occupancy (RANK_OCCUPANCY):** Indicates which ranks are occupied in the system. Non-enhanced channels (DDR4 and DDR5): • Bit 0: Rank 0 • Bit 1: Rank 1 • Bit 2: Rank 2 • Bit 3: Rank 3 Enhanced channels (LPDDR5): • Bit 0: Rank 0 = Sub channel 0 Rank 0 • Bit 1: Rank 1 = Sub channel 0 Rank 1 • Bit 2: Rank 2 = Sub channel 1 Rank 0 • Bit 3: Rank 3 = Sub channel 1 Rank 1 • Bit 4: Sub channel 0 Rank 2 • Bit 5: Sub channel 0 Rank 3 • Bit 6: Sub channel 1 Rank 2 • Bit 7: Sub channel 1 Rank 3 Note: Default on reset is all ranks enabled due to DDRIO requirements, BIOS MRC will write these bits to the proper values after reset based on the actual rank configuration.

3.2.75 PM DIMM IDLE ENERGY 0 0 0 MCHBAR (PM_DIMM_IDLE_ENERGY_0_0_0_MCHBAR) — Offset E460h

This register defines the energy of an idle DIMM with CKE on. Each 6-bit field corresponds to an integer multiple of the base DRAM command energy for that DIMM. There are 2 6-bit fields, one per DIMM.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E460h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:8	00h RW	**DIMM1 IDLE ENERGY (DIMM1_IDLE_ENERGY):** This register defines the energy consumed by DIMM1 for one clock cycle when the DIMM is idle with CKE on.
7:6	0h RO	**Reserved**
5:0	00h RW	**DIMM0 IDLE ENERGY (DIMM0_IDLE_ENERGY):** This register defines the energy consumed by DIMM0 for one clock cycle when the DIMM is idle with CKE on.

3.2.76 PM DIMM PD ENERGY 0 0 0 MCHBAR (PM_DIMM_PD_ENERGY_0_0_0_MCHBAR) — Offset E464h

This register defines the energy of an idle DIMM with CKE off. Each 6-bit field corresponds to an integer multiple of the base DRAM command energy for that DIMM. There are 2 6-bit fields, one per DIMM.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E464h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:8	00h RW	**DIMM1 PD ENERGY (DIMM1_PD_ENERGY):** This register defines the energy consumed by DIMM1 for one clock cycle when the DIMM is idle with CKE off.
7:6	0h RO	**Reserved**
5:0	00h RW	**DIMM0 PD ENERGY (DIMM0_PD_ENERGY):** This register defines the energy consumed by DIMM0 for one clock cycle when the DIMM is idle with CKE off.

3.2.77 PM DIMM ACT ENERGY 0 0 0 MCHBAR (PM_DIMM_ACT_ENERGY_0_0_0_MCHBAR) — Offset E468h

This register defines the combined energy contribution of activate and precharge commands. Each 8-bit field corresponds to an integer multiple of the base DRAM command energy for that DIMM. There are 2 8-bit fields, one per DIMM.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E468h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RW	**DIMM1 ACT ENERGY (DIMM1_ACT_ENERGY):** This register defines the combined energy contribution of activate and precharge commands.
7:0	00h RW	**DIMM0 ACT ENERGY (DIMM0_ACT_ENERGY):** This register defines the combined energy contribution of activate and precharge commands.

3.2.78 PM DIMM RD ENERGY 0 0 0 MCHBAR (PM_DIMM_RD_ENERGY_0_0_0_MCHBAR) — Offset E46Ch

This register defines the energy contribution of a read CAS command. Each 8-bit field corresponds to an integer multiple of the base DRAM command energy for that DIMM. There are 2 8-bit fields, one per DIMM.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E46Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RW	**DIMM1 RD ENERGY (DIMM1_RD_ENERGY):** This register defines the energy contribution of a read CAS command.
7:0	00h RW	**DIMM0 RD ENERGY (DIMM0_RD_ENERGY):** This register defines the energy contribution of a read CAS command.

3.2.79 PM DIMM WR ENERGY 0 0 0 MCHBAR (PM_DIMM_WR_ENERGY_0_0_0_MCHBAR) — Offset E470h

This register defines the energy contribution of a write CAS command. Each 8-bit field corresponds to an integer multiple of the base DRAM command energy for that DIMM. There are 2 8-bit fields, one per DIMM.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E470h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RW	**DIMM1 WR ENERGY (DIMM1_WR_ENERGY):** This register defines the energy contribution of a write CAS command.
7:0	00h RW	**DIMM0 WR ENERGY (DIMM0_WR_ENERGY):** This register defines the energy contribution of a write CAS command.

3.2.80 SC WR Delay 0 0 0 MCHBAR (SC_WR_DELAY_0_0_0_MCHBAR) — Offset E478h

This register defines the number of cycles decresed/increased from tCWL (TC_ODT_0_0_0_MCHBAR.tCWL) in Dclks.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E478h	00000003h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RW	**Add 1Qclk delay (ADD_1QCLK_DELAY):** in Gear2, MC Qclk is actually 1xclk of the DDR, the regular MC register can only set even number of cycles (working in Dclk == 2*1xclk), this bit gives an option to delay the write data by one 1xclk

Bit Range	Default & Access	Field Name (ID): Description
11:6	00h RW	**Add tCWL (ADD_TCWL):** the number of cycles (Dclk) increased to tCWL, make sure tCWL + Add_tCWL doesn't overflow
5:0	03h RW	**Dec tCWL (DEC_TCWL):** the number of cycles (Dclk) decreased from tCWL, configuring this number to be larger than tCWL is forbidden

3.2.81 SC PBR 0 0 0 MCHBAR (SC_PBR_0_0_0_MCHBAR) — Offset E488h

Per Bank Refresh parameters

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E488h	0000F011h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:10	03Ch RW	**tRFCpb reg (TRFCPB):** Refresh time in tCK (WCK for LPDDR5) for REFpb
9:4	01h RW	**PBR Exit on Idle Cnt (PBR_EXIT_ON_IDLE_CNT):** Number of tREFI cycles to count before switching PBR off for better clock gating. Value of 0 means no Idle exit
3	0h RW	**PBR Disable on hot (PBR_DISABLE_ON_HOT):** Disable PBR when LP4 is at 0.25xtREFI condition
2	0h RO	**Reserved**
1	0h RW	**PBR OOO Dis (PBR_OOO_DIS):** Disable out of order scheduling of banks for LP4. When using NoPanicPBR, this should be 0, otherwise will initiate PBR when there is high priority bank but might take low priority bank instead.
0	1h RW	**PBR Disable (PBR_DISABLE):** Disable PBR (per bank refresh) for LP4 (DDR4 force PBR off)

3.2.82 TC LPDDR4 MISC 0 0 0 MCHBAR (TC_LPDDR4_MISC_0_0_0_MCHBAR) — Offset E494h

Miscellaneous timing constrains

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E494h	04081056h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW	**Manual DQS MR READ (MANUAL_DQS_MR_READ):** This bit when set allows software to manually issue a DQS oscillator Mode register read For example : in LP4 : MR18, MR19 will be read, in LP5 : MR35, MR36 will be read
28:22	10h RW	**tMRR reg (TMRR):** Time from MRR to MRR or MRR to any other command (specified in tCK) Note for LP5 it is specified in WCK For LP5: the formula here is : RL + (BL/N_max) + RD (tWCKPST/tCK) + 2 For LP4 : this needs to be programmed to 16 For DDR5 : max (14ns , 16 clocks)
21:15	10h RW	**tMRRMRW reg (TMRRMRW):** MRR --> MRW timing (in DCLKs) (Note in LP5 specifiied in WCK) //MRR to MRW command minimum timing //NOTE: `DDR_TIMING_tDQSCK_max = RU(tDQSCK(max)/tCK) for LP4 // = RU(tWCKDQ0(max)/tCK) for LP5 // `DDR_TIMING_tBL = BL/2 for LP4 // = BL/n_max for LP5 //LP4 - RL + BL/2 + RU(tDQSCK(max)/tCK) + 3 DDR_LPDDR4 ==> `DDR_TIMING_tCL + `DDR_TIMING_tBL + `DDR_TIMING_tDQSCK_max + 3; //LP5 - RL + BL/n_max + RU(tWCKDQ0(max)/tCK) + 2 DDR_LPDDR5== >`DDR_TIMING_tCL + `DDR_TIMING_tBL + `DDR_TIMING_tDQSCK_max + 2;
14:8	10h RW	**tPREMRR reg (TPREMRR):** enforces safety /timing of any cmd to MRR (specified in tCKs in LP4 , WCK in LP5) For LP5: the formula here is : RL + (BL/N_max) + RD (tWCKPST/tCK) + 2 [READ --> MRR] For Other techs : this needs to be programmed to 16
7:0	56h RW	**tOSCO reg (TOSCO):** Delay between DQS_OSC counter stop to MR18/19 read

3.2.83 TC SREXITTP 0 0 0 MCHBAR (TC_SREXITTP_0_0_0_MCHBAR) — Offset E4C0h

Self-refresh exit timing parameters

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + E4C0h	0200000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:58	0h RO	**Reserved**
57:52	20h RW	**tSR reg (TSR):** minimum time that we are in self refresh In LP5 and LP4 it is tSR In DDR4 it is tCKESR In DDR5 it is tCSL
51:13	0h RO	**Reserved**
12:0	0000h RW	**tXSR reg (TXSR):** Exit self refresh to valid commands delay. in LP4 configure this parameter for tXSR or tXSR abort in terms of tCK (WCK for LPDDR5) cycles if used.

3.2.84 reg MBIST 0 0 0 MCHBAR (WDB_MBIST_0_0_0_MCHBAR[0]) — Offset E4E8h

This register holds the MBIST fields for the WDB and RDB.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E4E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**RUN BUSY (RUN_BUSY):** Pcode sets to start PBIST engine. HW clears when done. This bit should keep clocks running in the RF/SRAMs
30:9	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Inject Failure (INJECT_FAILURE):** MBIST Failure Injection
7:2	0h RO	**Reserved**
1	0h RO/V	**Complete reg (COMPLETE):** The MBIST Test has Completed
0	0h RO/V	**PASS reg (PASS):** The MBIST Test has Passed

3.2.85 reg MBIST 0 0 0 MCHBAR (WDB_MBIST_0_0_0_MCHBAR[1]) — Offset E4ECh

This register holds the MBIST fields for the WDB and RDB.

Note: **NOTE:** Bit definitions are the same as WDB_MBIST_0_0_0_MCHBAR[0], offset E4E8h.

3.2.86 reg MBIST 0 0 0 MCHBAR (RDB_MBIST_0_0_0_MCHBAR) — Offset E4F8h

This register holds the MBIST fields for the WDB and RDB.

Note: **NOTE:** Bit definitions are the same as WDB_MBIST_0_0_0_MCHBAR[0], offset E4E8h.

3.2.87 ECC Inject count 0 0 0 MCHBAR (ECC_INJECT_COUNT_0_0_0_MCHBAR) — Offset E4FCh

This register defines the count of write chunks (64-bit data packets) until the next ECC error injection in case ECC_inject field in ECC_DFT_config is 110 or 111. The count is of chunks in order to allow creating ECC errors on different 64-bit chunks

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E4FCh	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**Count reg (COUNT):** Chunk count for error inject

3.2.88 MCMNTS SPARE2 0 0 0 MCHBAR (MCMNTS_SPARE2_0_0_0_MCHBAR) — Offset E5F8h

Second Spare control register for MCMNTS

Note: **NOTE:** Bit definitions are the same as TC_REFM_0_0_0_MCHBAR, offset E40Ch.

3.2.89 MCMNTS SPARE 0 0 0 MCHBAR (MCMNTS_SPARE_0_0_0_MCHBAR) — Offset E5FCh

Spare control register

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + E5FCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW	**ForceX8Ref reg (FORCEX8REF):** Force accelerated refreshes, eight times the refresh number. Should be mutexed with ForceX2Ref and ForceX4Ref. Constant X8 refreshes may block channel from entering self refresh. In case of staggered refreshes and fully occupied channel it can cause performance degradation. Use with caution.
15:11	0h RO	**Reserved**
10	0h RW	**DisLowRefRate reg (DISLOWREFRATE):** Don't allow refresh rate lower than 1X
9	0h RW	**ForceX4Ref reg (FORCEX4REF):** Force accelerated refreshes, four times the refresh number. Should be mutexed with ForceX2Ref and ForceX8Ref. Constant X4 refreshes may block channel from entering self refresh. In case of staggered refreshes and fully occupied channel it can cause performance degradation. Use with caution.
8	0h RW	**ForceX2Ref reg (FORCEX2REF):** Force accelerated refreshes, twice the refresh number. Should be mutexed with ForceX4Ref and ForceX8Ref. Constant X2 refreshes may block channel from entering self refresh. In case of staggered refreshes and fully occupied channel it can cause a performance degradation. Use with caution.
7:0	0h RO	**Reserved**

3.3 Power Management (MCHBAR) Registers

This section contains the power management MCHBAR registers.

Base address of these registers are defined in the MCHBAR_0_0_0_PCI register in Bus: 0, Device: 0, Function: 0.

3.3.1 Summary of Registers

Table 3-4. Summary of MCHBAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
5824h	4	BIOS_POST_CODE_0_0_0_MCHBAR_PCU	00000000h
5828h	8	PKG_IA_C0_ANY_SUM_0_0_0_MCHBAR_PCU	0000000000000000h
5830h	8	PKG_IA_C0_ANY_0_0_0_MCHBAR_PCU	0000000000000000h
5838h	8	PKG_GT_C0_ANY_0_0_0_MCHBAR_PCU	0000000000000000h
5840h	8	PKG_GT_AND_IA_OVERLAP_0_0_0_MCHBAR_PCU	0000000000000000h
5848h	8	PKG_GT_C0_ANY_SLICE_0_0_0_MCHBAR_PCU	0000000000000000h
5850h	8	PKG_GT_C0_SLICES_SUM_0_0_0_MCHBAR_PCU	0000000000000000h
5858h	8	PKG_GT_C0_ANY_MEDIA_0_0_0_MCHBAR_PCU	0000000000000000h
5860h	8	PKG_IA_C0_ANY_RATIO_0_0_0_MCHBAR_PCU	0000000000000000h
5868h	8	PKG_GT_C0_ANY_RATIO_0_0_0_MCHBAR_PCU	0000000000000000h
5870h	8	PKG_GT_C0_ANY_SLICE_RATIO_0_0_0_MCHBAR_PCU	0000000000000000h
58E0h	8	DDR_RAPL_LIMIT_0_0_0_MCHBAR_PCU	0000000000000000h
58F0h	4	PACKAGE_RAPL_PERF_STATUS_0_0_0_MCHBAR_PCU	00000000h
5918h	8	SA_PERF_STATUS_0_0_0_MCHBAR_PCU	0000002000000000h
5920h	4	PRIP_TURBO_PLCY_0_0_0_MCHBAR_PCU	00000000h
5924h	4	SECP_TURBO_PLCY_0_0_0_MCHBAR_PCU	00000010h
5928h	4	PRIP_NRG_STTS_0_0_0_MCHBAR_PCU	00000000h
592Ch	4	SECP_NRG_STTS_0_0_0_MCHBAR_PCU	00000000h
5938h	4	PACKAGE_POWER_SKU_UNIT_0_0_0_MCHBAR_PCU	000A0E03h
593Ch	4	PACKAGE_ENERGY_STATUS_0_0_0_MCHBAR_PCU	00000000h
5948h	4	GT_PERF_STATUS_0_0_0_MCHBAR_PCU	00000000h
5968h	4	PP0_EFFICIENT_CYCLES_0_0_0_MCHBAR_PCU	00000000h
596Ch	4	PP0_THREAD_ACTIVITY_0_0_0_MCHBAR_PCU	00000000h
597Ch	4	PP0_TEMPERATURE_0_0_0_MCHBAR_PCU	00000000h
5984h	4	PCU_REFERENCE_CLOCK_0_0_0_MCHBAR_PCU	00000000h
5994h	4	RP_STATE_LIMITS_0_0_0_MCHBAR_PCU	000000FFh

Table 3-4. Summary of MCHBAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
5998h	4	RP_STATE_CAP_0_0_0_MCHBAR_PCU	00000000h
599Ch	4	TEMPERATURE_TARGET_0_0_0_MCHBAR_PCU	00000000h
59A0h	8	PACKAGE_RAPL_LIMIT_0_0_0_MCHBAR_PCU	0000000000000000h
59C0h	4	THERM_STATUS_GT_0_0_0_MCHBAR_PCU	08000000h
59C4h	4	THERM_INTERRUPT_GT_0_0_0_MCHBAR_PCU	00000000h
59C8h	4	DEVICE_IDLE_DURATION_OVERRIDE_0_0_0_MCHBAR_PCU	00000000h
59F0h	8	PKG_GT_C0_EUS_SUM	0000000000000000h
59F8h	8	PKG_GT_C0_MEDIA_SUM	0000000000000000h
5A08h	4	FFFC_EMI_CONTROL_0_0_0_MCHBAR_PCU	00000000h
5A0Ch	4	FFFC_RFI_CONTROL_0_0_0_MCHBAR_PCU	00000000h
5A18h	4	FFFC_RFI_CONTROL2_0_0_0_MCHBAR_PCU	00000000h
5DA0h	4	BIOS_MAILBOX_DATA_0_0_0_MCHBAR_PCU	00000000h
5DA4h	4	BIOS_MAILBOX_INTERFACE_0_0_0_MCHBAR_PCU	00000000h
5DA8h	4	BIOS_RESET_CPL_0_0_0_MCHBAR_PCU	00000000h
5E00h	4	MC_BIOS_REQ_0_0_0_MCHBAR_PCU	00000000h
5E04h	4	MC_BIOS_DATA_0_0_0_MCHBAR_PCU	00000000h
5F00h	4	SAPMCTL_0_0_0_MCHBAR_PCU	00002106h
5F3Ch	4	CONFIG_TDP_NOMINAL_0_0_0_MCHBAR_PCU	00000000h
5F40h	8	CONFIG_TDP_LEVEL1_0_0_0_MCHBAR_PCU	0000000000000000h
5F48h	8	CONFIG_TDP_LEVEL2_0_0_0_MCHBAR_PCU	0000000000000000h
5F50h	4	CONFIG_TDP_CONTROL_0_0_0_MCHBAR_PCU	00000000h
5F54h	4	TURBO_ACTIVATION_RATIO_0_0_0_MCHBAR_PCU	00000000h
5F58h	4	OC_STATUS_0_0_0_MCHBAR_PCU	00000000h
5F60h	8	BCLK_FREQ_0_0_0_MCHBAR	0000000000000000h

3.3.2 BIOS_POST_CODE_0_0_0_MCHBAR_PCU — Offset 5824h

This register holds 32 writable bits with no functionality behind them. BIOS will write here the current POST code (port 80).

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5824h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**POSTCODE:** BIOS will write the current POST code in this field

3.3.3 PKG_IA_C0_ANY_SUM_0_0_0_MCHBAR_PCU — Offset 5828h

Sum the cycles per number of active cores

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5828h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	0000000000000000h RO/V	**DATA:** RO: The counter value is incremented as a function of the number of cores that reside in C0 and active. If N cores are simultaneously in C0, then the number of clock ticks that are incremented is N. Counter rate is the Max Non-Turbo frequency (same as TSC).

3.3.4 PKG_IA_C0_ANY_0_0_0_MCHBAR_PCU — Offset 5830h

C0.Any - Sum the cycles of any active cores.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5830h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000h RO/V	**DATA:** RO, This counter increments whenever one or more IA cores are active and in C0 state. Counter rate is the Max Non-Turbo frequency (same as TSC).

3.3.5 PKG_GT_C0_ANY_0_0_0_MCHBAR_PCU — Offset 5838h

Sum the cycles of active GT

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5838h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000h RO/V	**DATA:** RO, This counter increments whenever GT slices or un slices are active and in C0 state. Counter rate is the Max Non-Turbo frequency (same as TSC).

3.3.6 PKG_GT_AND_IA_OVERLAP_0_0_0_MCHBAR_PCU — Offset 5840h

Sum the cycles of overlap time between any IA cores and GT

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5840h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RO/V	**DATA:** This counter increments whenever GT slices or un slices are active and in C0 state and in overlap with one of the IA cores that is active and in C0 state. Counter rate is the Max Non-Turbo frequency (same as TSC).

3.3.7 PKG_GT_C0_ANY_SLICE_0_0_0_MCHBAR_PCU — Offset 5848h

Sum the cycles of any active GT slice.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5848h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RO/V	**DATA:** RO, This counter increments whenever any GT slice is active. Counter rate is in Xtal (24/19.2Mhz) clock.

3.3.8 PKG_GT_C0_SLICES_SUM_0_0_0_MCHBAR_PCU — Offset 5850h

Sum the cycles of the sum of active GT slices.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5850h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	0000000000000000h RO	**DATA:** RO, This counter increments by the sum of active GT slices. Counter rate is in 24MHz.

3.3.9 PKG_GT_C0_ANY_MEDIA_0_0_0_MCHBAR_PCU — Offset 5858h

Sum the cycles of any media GT engine.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5858h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	0000000000000000h RO	**DATA:** RO, This counter increments whenever any GT media engine is active. Counter rate is in 24MHz.

3.3.10 PKG_IA_C0_ANY_RATIO_0_0_0_MCHBAR_PCU — Offset 5860h

new counter, follow exactly the PKG_IA_C0_ANY_0_0_0_MCHBAR_PCU

The only change is that they do +N instead of +1 on the relevant clock edge and conditions:

PCU_CR_PKG_IA_C0_ANY_RATIO_0_0_0_MCHBAR_PCU

+IO_WP_CV_P_STATE[IA_RATIO]

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5860h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RO/V	**DATA:** RO, This counter increments whenever one or more IA cores are active and in C0 state. Counter rate is the Max Non-Turbo frequency (same as TSC)

3.3.11 PKG_GT_C0_ANY_RATIO_0_0_0_MCHBAR_PCU — Offset 5868h

new counter, follow exactly the PKG_GT_C0_ANY_0_0_0_MCHBAR_PCU

The only change is that they do +N instead of +1 on the relevant clock edge and conditions:

PCU_CR_PKG_GT_C0_ANY_RATIO_0_0_0_MCHBAR_PCU

+ 3 * IO_WP_CV_P_STATE[GT_UNSLICE_RATIO] - IO_WP_CV_GT_CONFIG[UNSLICE_SQUASH_DELTA]

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5868h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	0000000000000000h RO/V	**DATA:** RO, This counter increments whenever GT slices or un slices are active and in C0 state. Counter rate is the Max Non-Turbo frequency (same as TSC)

3.3.12 PKG_GT_C0_ANY_SLICE_RATIO_0_0_0_MCHBAR_PCU — Offset 5870h

new counter, follow exactly the PKG_GT_C0_ANY_SLICEU

The only change is that they do +N instead of +1 on the relevant clock edge and conditions:

PCU_CR_PKG_GT_C0_ANY_SLICE_RATIO_0_0_0_MCHBAR_PCU

+ 3 * IO_WP_CV_P_STATE[GT_SLICE_RATIO] - IO_WP_CV_GT_CONFIG[SLICE_SQUASH_DELTA]

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5870h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	0000000000000000h RO/V	**DATA:** RO, This counter increments whenever any GT slice is active. Counter rate is in Xtal (24/19.2Mhz) clock

3.3.13 DDR_RAPL_LIMIT_0_0_0_MCHBAR_PCU — Offset 58E0h

Allows software to set running average power limits (RAPL) for the DRAM domain and measurement attributes associated with each limit.

The DDR RAPL algorithm uses the minimum of the values from this register and the DDR_RAPL_LIMIT MSR.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 58E0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/L	**LOCKED:** When set, this entire register becomes read-only. This bit will typically be set by BIOS during boot. **Locked by:** DDR_RAPL_LIMIT_0_0_0_MCHBAR_PCU.LOCKED
62:56	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
55:54	0h RW/L	**LIMIT2_TIME_WINDOW_X:** Power Limit 2 (PL2) time window X value, for DDR domain. Actual time window for RAPL is: (1/1024 seconds) * (1+(X/4)) * (2Y) **Locked by:** DDR_RAPL_LIMIT_0_0_0_MCHBAR_PCU.LOCKED
53:49	00h RW/L	**LIMIT2_TIME_WINDOW_Y:** Power Limit 2 (PL2) time window Y value, for DDR domain. Actual time window for RAPL is: (1/1024 seconds) * (1+(X/4)) * (2Y) **Locked by:** DDR_RAPL_LIMIT_0_0_0_MCHBAR_PCU.LOCKED
48	0h RO	**Reserved**
47	0h RW/L	**LIMIT2_ENABLE:** Power Limit 2 (PL2) enable bit for DDR domain. **Locked by:** DDR_RAPL_LIMIT_0_0_0_MCHBAR_PCU.LOCKED
46:32	0000h RW/L	**LIMIT2_POWER:** Power Limit 2 (PL2) for DDR domain in Watts. Format is U11.3: Resolution 0.125W, Range 0-2047.875W. **Locked by:** DDR_RAPL_LIMIT_0_0_0_MCHBAR_PCU.LOCKED
31:24	0h RO	**Reserved**
23:22	0h RW/L	**LIMIT1_TIME_WINDOW_X:** Power Limit 1 (PL1) time window X value, for DDR domain. Actual time window for RAPL is: (1/1024 seconds) * (1+(X/4)) * (2Y) **Locked by:** DDR_RAPL_LIMIT_0_0_0_MCHBAR_PCU.LOCKED
21:17	00h RW/L	**LIMIT1_TIME_WINDOW_Y:** Power Limit 1 (PL1) time window Y value, for DDR domain. Actual time window for RAPL is: (1/1024 seconds) * (1+(X/4)) * (2Y) **Locked by:** DDR_RAPL_LIMIT_0_0_0_MCHBAR_PCU.LOCKED
16	0h RO	**Reserved**
15	0h RW/L	**LIMIT1_ENABLE:** Power Limit 1 (PL1) enable bit for DDR domain. **Locked by:** DDR_RAPL_LIMIT_0_0_0_MCHBAR_PCU.LOCKED
14:0	0000h RW/L	**LIMIT1_POWER:** Power Limit 1 (PL1) for DDR domain in Watts. Format is U11.3: Resolution 0.125W, Range 0-2047.875W. **Locked by:** DDR_RAPL_LIMIT_0_0_0_MCHBAR_PCU.LOCKED

3.3.14 PACKAGE_RAPL_PERF_STATUS_0_0_0_MCHBAR_PCU — Offset 58F0h

Package RAPL Performance Status Register. This register provides information on the performance impact of the RAPL power limit and indicates the duration for processor went below the requested P-state due to package power constraint.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 58F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V/P	**COUNTS:** Counter of the time units within which RAPL was limiting P-states. If limitation occurred anywhere within the time window of 1/1024 seconds, the count will be incremented (limitation on accuracy). This data can serve as a proxy for the potential performance impacts of RAPL on cores performance.

3.3.15 SA_PERF_STATUS_0_0_0_MCHBAR_PCU — Offset 5918h

System Agent Performance status. Indicates current various System Agent PLL ratios.

Operting frequency needs to be calculated according to reference clock (BCLK).

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5918h	0000002000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RO	**Reserved**
55:40	0000h RO/V	**SA_VOLTAGE:** This register holds the System Agent voltage. This voltage value is valid only if the System Agent VR is SVID based. The precision is U3.13 (1/8192V resolution).
39:32	20h RO/V	**PSF0_RATIO:** Reports the PSF0 PLL ratio. The PSF0 frequency is: ratio * 16.67MHz. The supported ratios are {32, 48, 64} = {533MHz, 800MHz, 1067MHz}.
31:24	00h RO/V	**UCLK_RATIO:** RING UCLK RATIO. Reference=100Mhz

Bit Range	Default & Access	Field Name (ID): Description
23:18	00h RO/V	**IPU_PS_RATIO:** IPU PS RATIO. The frequency is 25MHz * Ratio.
17:12	00h RO/V	**IPU_IS_DIVISOR:** IPU IS divisor. The frequency is 1600MHz/Divisor.
11	0h RO/V	**OPI_LINK_SPEED:** OPI link speed. 0 - 2Gb/s, 1 - 4Gb/s
10	0h RO/V	**QCLK_REFERENCE:** DDR QCLK REFERENCE. 0=133Mhz, 1=100Mhz
9:2	00h RO/V	**QCLK_RATIO:** DDR QCLK RATIO. Reference determined by the QCLK_REFERENCE field.
1:0	0h RO/V	**LAST_DE_WP_REQ_SERVED:** Last DE workpoint request served by Pcode

3.3.16 PRIP_TURBO_PLCY_0_0_0_MCHBAR_PCU — Offset 5920h

The PRIMARY_PLANE_TURBO_POWER_POLICY and SECONDARY_PLANE_TURBO_POWER_POLICY are used together to balance the power budget betwen the two power planes.

The power plane with the higher policy will get a higher priority. The default value will aim to maintain same ratio for IA and GT.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5920h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RW	**PRIPTP:** Priority Level. A higher number implies a higher priority.

3.3.17 SECP_TURBO_PLCY_0_0_0_MCHBAR_PCU — Offset 5924h

The PRIMARY_PLANE_TURBO_POWER_POLICY and SECONDARY_PLANE_TURBO_POWER_POLICY are used together to balance the power budget betwen the two power planes.

The power plane with the higher policy will get a higher priority. The default value will aim to maintain same ratio for IA and GT.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5924h	00000010h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	10h RW	**SECPTP:** Priority Level. A higher number implies a higher priority.

3.3.18 PRIP_NRG_STTS_0_0_0_MCHBAR_PCU — Offset 5928h

Reports total energy consumed. The counter will wrap around and continue counting when it reaches its limit.

The energy status is reported in units which are defined in PACKAGE_POWER_SKU_UNIT_MSR[ENERGY_UNIT].

SW will read this value and subtract the difference from last value read. The value of this register is updated every 1mSec.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5928h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**DATA:** Energy Value

3.3.19 SECP_NRG_STTS_0_0_0_MCHBAR_PCU — Offset 592Ch

Reports total energy consumed. The counter will wrap around and continue counting when it reaches its limit.

The energy status is reported in units which are defined in PACKAGE_POWER_SKU_UNIT_MSR[ENERGY_UNIT].

SW will read this value and subtract the difference from last value read. The value of this register is updated every 1mSec.

Note: **NOTE:** Bit definitions are the same as PRIP_NRG_STTS_0_0_0_MCHBAR_PCU, offset 5928h.

3.3.20 PACKAGE_POWER_SKU_UNIT_0_0_0_MCHBAR_PCU — Offset 5938h

Defines units for calculating SKU power and timing parameters.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5938h	000A0E03h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	Ah RO/V	**TIME_UNIT:** Time Units used for power control registers. The actual unit value is calculated by 1 s / Power(2,TIME_UNIT). The default value of Ah corresponds to 976 usec.
15:13	0h RO	**Reserved**
12:8	0Eh RO/V	**ENERGY_UNIT:** Energy Units used for power control registers. The actual unit value is calculated by 1 J / Power(2,ENERGY_UNIT). The default value of 14 corresponds to Ux.14 number.
7:4	0h RO	**Reserved**
3:0	3h RO/V	**PWR_UNIT:** Power Units used for power control registers. The actual unit value is calculated by 1 W / Power(2,PWR_UNIT). The default value of 0011b corresponds to 1/8 W.

3.3.21 PACKAGE_ENERGY_STATUS_0_0_0_MCHBAR_PCU — Offset 593Ch

Package energy consumed by the entire CPU (including IA, GT and uncore). The counter will wrap around and continue counting when it reaches its limit.

The energy status is reported in units which are defined in PACKAGE_POWER_SKU_UNIT_MSR[ENERGY_UNIT].

Note: **NOTE:** Bit definitions are the same as PRIP_NRG_STTS_0_0_0_MCHBAR_PCU, offset 5928h.

3.3.22 GT_PERF_STATUS_0_0_0_MCHBAR_PCU — Offset 5948h

P-state encoding for the Secondary Power Planes current PLL frequency and the current VID.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5948h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:20	000h RO/V	**SLICES_RATIO:** GT Slices frequency, in granularity of 16.666Mhz. When GT is in RC6, or when all slices are disabled, this frequency is ZERO.
19:11	000h RO/V	**UNSLICE_RATIO:** GT Unslice frequency, in granularity of 16.666Mhz. When GT is in RC6 this frequency is ZERO.
10:8	0h RO	**Reserved**
7:0	00h RO/V/P	**SLICES_VOLTAGE:** GT voltage, in VID units according to SVID spec format.

3.3.23 PP0_EFFICIENT_CYCLES_0_0_0_MCHBAR_PCU — Offset 5968h

This register will store a value equal to the product of the number of BCLK cycles in which at least one of the IA cores was active and the efficiency score calculated by the PCODE. The efficiency score is a number between 0 and 1 that indicates the IAs efficiency.

This is a 32 bit accumulation done by P-code to this register out of the PUSH-BUS. Values exceeding 32b will wrap around.

This value is used in conjunction with PP0_ANY_THREAD_ACTIVITY to generate statistics for SW.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5968h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**DATA:** Number of Cycles

3.3.24 PP0_THREAD_ACTIVITY_0_0_0_MCHBAR_PCU — Offset 596Ch

This register will store a value equal to the product of the number of BCLK cycles and the number of IA threads that are running. This is a 32 bit accumulation done by PCU HW. Values exceeding 32b will wrap around.

This value is used in conjunction with PP0_ANY_THREAD_ACTIVITY to generate statistics for SW.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 596Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**DATA:** Number of Cycles.

3.3.25 PP0_TEMPERATURE_0_0_0_MCHBAR_PCU — Offset 597Ch

PP0 (IA) temperature in degrees (C). This field is updated by FW.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 597Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO/V	**DATA:** Temperature in degrees (C).

3.3.26 PCU_REFERENCE_CLOCK_0_0_0_MCHBAR_PCU — Offset 5984h

This register will count BCLK cycles. Values exceeding 32b will wrap around. This value is used for energy and power calculations.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5984h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TIME_VAL:** Number of Cycles

3.3.27 RP_STATE_LIMITS_0_0_0_MCHBAR_PCU — Offset 5994h

This register allows SW to limit the maximum base frequency for the Integrated GFX Engine (GT) allowed during run-time.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5994h	000000FFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	FFh RW	**RPSTT_LIM:** This field indicates the maximum base frequency limit for the Integrated GFX Engine (GT) allowed during run-time.

3.3.28 RP_STATE_CAP_0_0_0_MCHBAR_PCU — Offset 5998h

This register contains the maximum base frequency capability for the Integrated GFX Engine (GT).

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5998h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RO	**RPN_CAP:** This field indicates the maximum RPN base frequency capability for the Integrated GFX Engine (GT). Values are in units of 50 MHz.
15:8	00h RO	**RP1_CAP:** This field indicates the maximum RP1 base frequency capability for the Integrated GFX Engine (GT). Values are in units of 50 MHz.
7:0	00h RO	**RP0_CAP:** This field indicates the maximum RP0 base frequency capability for the Integrated GFX Engine (GT). Values are in units of 50 MHz.

3.3.29 TEMPERATURE_TARGET_0_0_0_MCHBAR_PCU — Offset 599Ch

Legacy register holding temperature related constants for Platform use.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 599Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**LOCKED:** When set, this entire register becomes read-only. **Locked by:** TEMPERATURE_TARGET.LOCKED
30:24	00h RO/V	**TJ_MAX_TCC_OFFSET:** Temperature offset in degrees (C) from the TJ Max. Used for throttling temperature. Will not impact temperature reading. If offset is allowed and set - the throttle will occur and reported at lower then Tj_max. **Locked by:** TEMPERATURE_TARGET.LOCKED
23:16	00h RO/V	**REF_TEMP:** This field indicates the maximum junction temperature, also referred to as the Throttle Temperature, TCC Activation Temperature or Prochot Temperature. This is the temperature at which the Adaptive Thermal Monitor is activated.
15:8	00h RO/V	**FAN_TEMP_TARGET_OFST:** Fan Temperature Target Offset (a.k.a. T-Control) indicates the relative offset from the Thermal Monitor Trip Temperature at which fans should be engaged.
7	0h RO/V	**TCC_OFFSET_CLAMPING_BIT:** When enabled will allow RATL throttling below P1 **Locked by:** TEMPERATURE_TARGET.LOCKED
6:0	00h RO/V	**TCC_OFFSET_TIME_WINDOW:** Describes the RATL averaging time window **Locked by:** TEMPERATURE_TARGET.LOCKED

3.3.30 PACKAGE_RAPL_LIMIT_0_0_0_MCHBAR_PCU — Offset 59A0h

The Integrated Graphics driver, CPM driver, BIOS and OS can balance the power budget between the Primary Power Plane (IA) and the Secondary Power Plane (GT) via PRIMARY_PLANE_TURBO_POWER_LIMIT_MSR and SECONDARY_PLANE_TURBO_POWER_LIMIT_MSR.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 59A0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/L	**PKG_PWR_LIM_LOCK:** When set, all settings in this register are locked and are treated as Read Only. This bit will typically set by BIOS during boot time or resume from Sx. **Locked by:** PACKAGE_RAPL_LIMIT_0_0_0_MCHBAR_PCU.PKG_PWR_LIM_LOCK
62:56	0h RO	**Reserved**
55:49	00h RW/L	**PKG_PWR_LIM_2_TIME:** x = PKG_PWR_LIM_2_TIME[55:54] y = PKG_PWR_LIM_2_TIME[53:49] The timing interval window is Floating Point number given by 1.x * power(2,y). The unit of measurement is defined in PACKAGE_POWER_SKU_UNIT_MSR[TIME_UNIT]. The maximal time window is bounded by PACKAGE_POWER_SKU_MSR[PKG_MAX_WIN]. The minimum time window is 1 unit of measurement (as defined above). **Locked by:** PACKAGE_RAPL_LIMIT_0_0_0_MCHBAR_PCU.PKG_PWR_LIM_LOCK
48	0h RW/L	**PKG_CLMP_LIM_2:** Package Clamping limitation #2 - Allow going below P1. 0b PBM is limited between P1 and P0. 1b PBM can go below P1. **Locked by:** PACKAGE_RAPL_LIMIT_0_0_0_MCHBAR_PCU.PKG_PWR_LIM_LOCK
47	0h RW/L	**PKG_PWR_LIM_2_EN:** This bit enables/disables PKG_PWR_LIM_2. 0b Package Power Limit 2 is Disabled 1b Package Power Limit 2 is Enabled **Locked by:** PACKAGE_RAPL_LIMIT_0_0_0_MCHBAR_PCU.PKG_PWR_LIM_LOCK
46:32	0000h RW/L	**PKG_PWR_LIM_2:** This field indicates the power limitation #2. The unit of measurement is defined in PACKAGE_POWER_SKU_UNIT_MSR[PWR_UNIT]. **Locked by:** PACKAGE_RAPL_LIMIT_0_0_0_MCHBAR_PCU.PKG_PWR_LIM_LOCK
31:24	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
23:17	00h RW/L	**PKG_PWR_LIM_1_TIME:** x = PKG_PWR_LIM_1_TIME[23:22] y = PKG_PWR_LIM_1_TIME[21:17] The timing interval window is Floating Point number given by 1.x * power(2,y). The unit of measurement is defined in PACKAGE_POWER_SKU_UNIT_MSR[TIME_UNIT]. The maximal time window is bounded by PACKAGE_POWER_SKU_MSR[PKG_MAX_WIN]. The minimum time window is 1 unit of measurement (as defined above). **Locked by:** PACKAGE_RAPL_LIMIT_0_0_0_MCHBAR_PCU.PKG_PWR_LIM_LOCK
16	0h RW/L	**PKG_CLMP_LIM_1:** Package Clamping limitation #1 - Allow going below P1. 0b PBM is limited between P1 and P0. 1b PBM can go below P1. **Locked by:** PACKAGE_RAPL_LIMIT_0_0_0_MCHBAR_PCU.PKG_PWR_LIM_LOCK
15	0h RW/L	**PKG_PWR_LIM_1_EN:** This bit enables/disables PKG_PWR_LIM_1. 0b Package Power Limit 1 is Disabled 1b Package Power Limit 1 is Enabled **Locked by:** PACKAGE_RAPL_LIMIT_0_0_0_MCHBAR_PCU.PKG_PWR_LIM_LOCK
14:0	0000h RW/L	**PKG_PWR_LIM_1:** This field indicates the power limitation #1. The unit of measurement is defined in PACKAGE_POWER_SKU_UNIT_MSR[PWR_UNIT]. **Locked by:** PACKAGE_RAPL_LIMIT_0_0_0_MCHBAR_PCU.PKG_PWR_LIM_LOCK

3.3.31 THERM_STATUS_GT_0_0_0_MCHBAR_PCU — Offset 59C0h

Contains status information about the processors thermal sensor and automatic thermal monitoring facilities.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 59C0h	08000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**VALID:** This bit indicates that the TEMPERATURE field is valid. It is set by PCODE if the temperature is within valid thermal sensor range.
30:27	1h RO	**RESOLUTION:** Supported resolution in degrees C.
26:24	0h RO	**Reserved**
23:16	00h RO/V	**TEMPERATURE:** This is a temperature offset in degrees C below theTJ Max temperature. This number is meaningful only if VALID bit in this register is set.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/0C/V	**CROSS_DOMAIN_LIMIT_LOG:** R/WC0 - If set (1), indicates another hardware domain (e.g. processor graphics) has limited energy efficiency optimizations in the processor core domain since the last clearing of this bit or a reset. This bit is sticky, software may clear this bit by writing a zero (0).
14	0h RO/V	**CROSS_DOMAIN_LIMIT_STATUS:** RO - If set (1), indicates another hardware domain (e.g. processor graphics) is currently limiting energy efficiency optimizations in the processor core domain.
13	0h RW/0C/V	**CURRENT_LIMIT_LOG:** R/WC0 - If set (1), an electrical current limit has been exceeded that has adversely impacted energy efficiency optimizations since the last clearing of this bit or a reset. This bit is sticky, software may clear this bit by writing a zero (0).
12	0h RO/V	**CURRENT_LIMIT_STATUS:** RO - If set (1), indicates an electrical current limit (e.g. Electrical Design Point/IccMax) is being exceeded and is adversely impacting energy efficiency optimizations.
11	0h RW/0C/V	**POWER_LIMITATION_LOG:** R/WC0 - Sticky bit which indicates whether the current P-state is limited by power limitation since the last clearing of this bit or a reset. SW may clear this bit by writing a zero (0). For legacy P state method, this bit will be set only if the P-state is limit below the guaranty level
10	0h RO/V	**POWER_LIMITATION_STATUS:** RO - Indicates whether the current P-state is limited by power limitation. For legacy P state method, this bit will be set only if the P-state is limit below the guaranty level.
9	0h RW/0C/V	**THRESHOLD2_LOG:** Sticky log bit that asserts on a 0 to 1 or a 1 to 0 transition of the THRESHOLD2_STATUS bit. This bit is set by HW and cleared by SW.
8	0h RO/V	**THRESHOLD2_STATUS:** Indicates that the current temperature is higher than or equal to Threshold 2 temperature.
7	0h RW/0C/V	**THRESHOLD1_LOG:** Sticky log bit that asserts on a 0 to 1 or a 1 to 0 transition of the THRESHOLD1_STATUS bit. This bit is set by HW and cleared by SW.
6	0h RO/V	**THRESHOLD1_STATUS:** Indicates that the current temperature is higher than or equal to Threshold 1 temperature.
5	0h RW/0C/V	**OUT_OF_SPEC_LOG:** Sticky log bit indicating that the processor operating out of its thermal specification since the last time this bit was cleared. This bit is set by HW on a 0 to 1 transition of OUT_OF_SPEC_STATUS.
4	0h RO/V	**OUT_OF_SPEC_STATUS:** Status bit indicating that the processor is operating out of its thermal specification. Once set, this bit should only clear on a reset.
3	0h RW/0C/V	**PROCHOT_LOG:** Sticky log bit indicating that xxPROCHOT# has been asserted since the last time this bit was cleared by SW. This bit is set by HW on a 0 to 1 transition of PROCHOT_STATUS.
2	0h RO/V	**PROCHOT_STATUS:** Status bit indicating that xxPROCHOT# is currently being asserted.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW/0C/V	**THERMAL_MONITOR_LOG:** Sticky log bit indicating that the core has seen a thermal monitor event since the last time SW cleared this bit. This bit is set by HW on a 0 to 1 transition of THERMAL_MONITOR_STATUS.
0	0h RO/V	**THERMAL_MONITOR_STATUS:** Status bit indicating that the Thermal Monitor has tripped and is currently thermally throttling.

3.3.32 THERM_INTERRUPT_GT_0_0_0_MCHBAR_PCU — Offset 59C4h

Enables and disables the generation of an interrupt on temperature transitions detected with the processors thermal sensors and thermal monitor.

.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 59C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**POWER_INT_ENABLE:** When this bit is set, a thermal interrupt will be sent upon throttling due to power limitations.
23	0h RW	**THRESHOLD_2_INT_ENABLE:** Controls the generation of a thermal interrupt whenever the Thermal Threshold 2 Temperature is crossed.
22:16	00h RW	**THRESHOLD_2_REL_TEMP:** This value indicates the offset in degrees below TJ Max Temperature that should trigger a Thermal Threshold 2 trip.
15	0h RW	**THRESHOLD_1_INT_ENABLE:** Controls the generation of a thermal interrupt whenever the Thermal Threshold 1 Temperature is crossed.
14:8	00h RW	**THRESHOLD_1_REL_TEMP:** This value indicates the offset in degrees below TJ Max Temperature that should trigger a Thermal Threshold 1 trip.
7:5	0h RO	**Reserved**
4	0h RW	**OUT_OF_SPEC_INT_ENABLE:** Thermal interrupt enable for the critical temperature condition which is stored in the Critical Temperature Status bit in IA32_THERM_STATUS.
3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**PROCHOT_INT_ENABLE:** Bidirectional PROCHOT# assertion interrupt enable. If set, a thermal interrupt is delivered on the rising edge of xxPROCHOT#.
1	0h RW	**LOW_TEMP_INT_ENABLE:** Enables a thermal interrupt to be generated on the transition from a high-temperature to a low-temperature when set, where high temperature is dictated by the thermal monitor trip temperature.
0	0h RW	**HIGH_TEMP_INT_ENABLE:** Enables a thermal interrupt to be generated on the transition from a low-temperature to a high-temperature when set, where high temperature is dictated by the thermal monitor trip temperature.

3.3.33 DEVICE_IDLE_DURATION_OVERRIDE_0_0_0_MCHBAR_PCU — Offset 59C8h

MDID override register to be used by OS/SW/post-si for debug purposes.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 59C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	0h RW	**FORCE_MDID_OVERRIDE:** When this bit is set, and bit 1 (the valid bit) is set, the value specified in this field will be used for MDID purposes. If this bit is clear, and bit 1 (the valid bit) is set, this value should be consumed along with the other MDID registers to determine which value is expiring next and reporting that value.
29	0h RW	**DISABLE_MDID_EVALUATION:** Send a value of disabled to the PCH for the MDID field.
28:8	000000h RW	**NEXT_DEVICE_ACTIVITY:** These are in 1us increments and can report a max. value of approximately 2 seconds
7	0h RW	**IM:** 0: Interrupt. This is a hint for the idle duration time to the next interrupt. 1: Memory. This is a hint for the idle duration time to the next snoop cycle.
6	0h RW	**OD:** 0: Opportunistic. This is an opportunistic hint as suggested by the sub-system. 1: Deterministic. This is a deterministic hint as suggested by the sub-system.
5:2	0h RO	**Reserved**
1	0h RW	**VALID:** 0: This Idle Duration Override CSR is not valid 1: This Idle Duration Override CSR is valid

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**Reserved**

3.3.34 PKG_GT_C0_EUS_SUM — Offset 59F0h

GT EUS MCNT

The counter value is incremented when PKG_GT_C0_ANY_SLICE icrements.

Counts in 24Mhz units.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 59F0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RO/V	**DATA:** mmio for software pcode interaface

3.3.35 PKG_GT_C0_MEDIA_SUM — Offset 59F8h

GT MEDIA MCNT

The counter value is incremented when PKG_GT_C0_ANY_SLICE icrements.

Counts in 24Mhz units.

Note: **NOTE:** Bit definitions are the same as PKG_GT_C0_EUS_SUM, offset 59F0h.

3.3.36 FFFC_EMI_CONTROL_0_0_0_MCHBAR_PCU — Offset 5A08h

Fivr FFFC Control Register

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5A08h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DATA:** Data field SW write pcode read

3.3.37 FFFC_RFI_CONTROL_0_0_0_MCHBAR_PCU — Offset 5A0Ch

Fivr FFFC Control Register

Note: **NOTE:** Bit definitions are the same as FFFC_EMI_CONTROL_0_0_0_MCHBAR_PCU, offset 5A08h.

3.3.38 FFFC_RFI_CONTROL2_0_0_0_MCHBAR_PCU — Offset 5A18h

Fivr FFFC Control Register

Note: **NOTE:** Bit definitions are the same as FFFC_EMI_CONTROL_0_0_0_MCHBAR_PCU, offset 5A08h.

3.3.39 BIOS_MAILBOX_DATA_0_0_0_MCHBAR_PCU — Offset 5DA0h

Data register for the BIOS-to-Firmware mailbox.

This register is used in conjunction with BIOS_MAILBOX_INTERFACE.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5DA0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**DATA:** This field contains the data associated with specific commands.

3.3.40 BIOS_MAILBOX_INTERFACE_0_0_0_MCHBAR_PCU — Offset 5DA4h

Control and Status register for the BIOS-to-Firmware mailbox.

This register is used in conjunction with BIOS_MAILBOX_DATA.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5DA4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**RUN_BUSY:** SW may write to the two mailbox registers only when RUN_BUSY is cleared (0b). After setting this bit, SW will poll this bit until it is cleared. Firmware will clear RUN_BUSY after updating the mailbox registers with the result and error code.
30:29	0h RO	**Reserved**
28:16	0000h RW/V	**PARAM2:** This field contains additional parameters associated with specific commands. These are documented in the BIOS Writers Guide
15:8	00h RW/V	**PARAM1:** This field contains additional parameters associated with specific commands. These are documented in the BIOS Writers Guide

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW/V	**COMMAND:** On RUN_BUSY assertion this field should contain the SW request command, on RUN_BUSY deassrtion this field will contain the Firmware response code

3.3.41 BIOS_RESET_CPL_0_0_0_MCHBAR_PCU — Offset 5DA8h

This register is used as interface between BIOS and PCODE. It is written by BIOS and read by PCODE.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5DA8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW	**C7_ALLOWED:** BIOS/driver will set this bit when only discrete graphics is being used and the PCIe lanes will be down. BIOS/driver will clear this bit when discrete graphics is being used. THIS FIELD IS OBSOLETE. NOT USED ANYWHERE. (Nov-2013)
1	0h RW	**PCIE_ENUMERATION_DONE:** This will be set after PCIe enumeration is done. This bit will be read by pcode. If it is set, pcode will look at the following register bits: MPVTDTRK_CR_DEVEN_0_0_0_PCI Bit Bit Name 1 D1F2EN 2 D1F1EN 3 D1F0EN If all of these bits are set to a 0x0, this means that there is nothing connected to the PEG devices and the Gen3 PLL can be shut off. Note - implicit assumption - this bit is asserted prior to (or with) asserting RST_CPL.
0	0h RW/1S	**RST_CPL:** This bit is set by BIOS to indicate to the CPU Power management function that it has completed to set up all PM relevant configuration and allow CPU Power management function to digest the configuration data and start active PM operation. It is expected that this bit will be set just before BIOS transfer of control to the OS. 0b Not ready 1b BIOS PM configuration complete

3.3.42 MC_BIOS_REQ_0_0_0_MCHBAR_PCU — Offset 5E00h

This register allows BIOS to request Memory Controller clock frequency.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5E00h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RUN_BUSY:** This bit indicates that the BIOS request is pending. BIOS sets this bit together with a command in the lower bits of this register. Firmware may only clear this bit after the BIOS request has been served or observed.
30:27	0h RW	**REQ_VDDQ_TX_ICCMAX:** Peak current on VDDQTX rail at this clock frequency and gear configuration. Described in 0.25A resolution. Max: 32 * 0.25 = 8A;
26:17	000h RW	**REQ_VDDQ_TX_VOLTAGE:** Voltage of the VDDQTX rail at this clock frequency and gear configuration. Described in 5mV resolution.
16:14	0h RO	**Reserved**
13:12	0h RW	**GEAR:** 0h - Gear1 (Default) - DDR bus clock is the same as QCLK 1h - Gear2 - DDR PHY bus clock is double of QCLK 2h - Gear4 - DDR PHY bus clock is quad of QCLK
11:8	0h RW	**MC_PLL_REF:** Request Type: 0h - MC frequency request for 133MHz Qclk granularity. 1h - MC frequency request for 100MHz Qclk granularity. All other values are reserved.
7:0	00h RW	**MC_PLL_RATIO:** This field holds the memory controller frequency request (QCLK). Each bin is 133/100MHz and not 266/200MHz. This interface replaces the usage of DCLK ratios and Odd Ratio. QCLK frequency is determined by the MC reference clock (MC_FREQ_TYPE) as well as BCLK. Binary Dec DCLK Equation DCLK Freq QCLK Equation QCLK Freq 0000b 0d ---------- MC PLL - shutdown ---------- ... 0011b 3d 3 * 66.66 200.00 MHz 3 * 133.33 400.00 MHz 0100b 4d 4 * 66.66 266.66 MHz 4 * 133.33 533.33 MHz 0101b 5d 5 * 66.66 333.33 MHz 5 * 133.33 666.67 MHz 0110b 6d 6 * 66.66 400.00 MHz 6 * 133.33 800.00 MHz 0111b 7d 7 * 66.66 466.66 MHz 7 * 133.33 933.33 MHz 1000b 8d 8 * 66.66 533.33 MHz 8 * 133.33 1066.67 MHz ...

3.3.43 MC_BIOS_DATA_0_0_0_MCHBAR_PCU — Offset 5E04h

Memory Controller Frequency information for BIOS, during MRC flow. Reflects the last frequency requested in MC_BIOS_REQ_0_0_0_MCHBAR_PCU.

Incase of Dual MRC for SAGV, the value will change according to the MRC requests. Post MRC will hold the last MRC request and not the current MC frequency.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5E04h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:27	0h RW	**VDDQ_TX_ICCMAX:** Peak current on VDDQTX rail at this clock frequency and gear configuration. Described in 0.25A resolution. Max: 32 * 0.25 = 8A;
26:17	000h RW	**VDDQ_TX_VOLTAGE:** Voltage of the VDDQTX rail at this clock frequency and gear configuration. Described in 5mV resolution.
16:14	0h RO	**Reserved**
13:12	0h RW/L	**GEAR:** 0 - Gear1 (Default) - DDR bus clock is the same as QCLK 1 - Gear2 - DDR PHY bus clock is double of QCLK 2h - Gear4 - DDR PHY bus clock is quad of QCLK
11:8	0h RW/L	**MC_PLL_REF:** This field holds the memory controller frequency Type. • 0h: MC frequency request for 133MHz Qclk granularity. • 1h: MC frequency request for 100MHz Qclk granularity. All other values are reserved.

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW/L	**MC_PLL_RATIO:** This field holds the memory controller frequency (QCLK). Each bin is 133/100MHz and not 266/200MHz. This interface replaces the usage of DCLK ratios and Odd Ratio. QCLK frequency is determined by the MC reference clock (MC_FREQ_TYPE) as well as BCLK. Binary Dec DCLK Equation DCLK Freq QCLK Equation QCLK Freq 0000b 0d ---------- MC PLL - shutdown ---------- ... 0011b 3d 3 * 66.66 200.00 MHz 3 * 133.33 400.00 MHz 0100b 4d 4 * 66.66 266.66 MHz 4 * 133.33 533.33 MHz 0101b 5d 5 * 66.66 333.33 MHz 5 * 133.33 666.67 MHz 0110b 6d 6 * 66.66 400.00 MHz 6 * 133.33 800.00 MHz 0111b 7d 7 * 66.66 466.66 MHz 7 * 133.33 933.33 MHz 1000b 8d 8 * 66.66 533.33 MHz 8 * 133.33 1066.67 MHz ... The values above are given in units of 133.33MHz (400/3). A value of zero implies that the memory controller PLL is shut down.

3.3.44 SAPMCTL_0_0_0_MCHBAR_PCU — Offset 5F00h

PCODE will sample this register at the end of Phase 4.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5F00h	00002106h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**MDLL_ON_DE:** Force memory Initiator DLL on when the Display Engine is active. This includes cases where memory is not accessed. This bit has to be set only if there are issues with the memory DLL wakeup based on the Self Refresh exit indication from Display Engine. 0b Display Engine wakes up memory DLL using the Self Refresh exit indication only 1b Force Memory DLL on when the Display Engine is active
14	0h RW	**MPLL_ON_DE:** Force Memory PLLs (MCPLL and GDPLL) on when the Display Engine is active. This includes cases where memory is not accessed. This bit has to be set only if there are issues with the Memory PLL wakeup based on the Self Refresh exit indication from Display Engine. 0b Display Engine wakes up Memory PLLs using the Self Refresh exit indication only 1b Force Memory PLLs on when the Display Engine is active
13	1h RW	**SACG_MPLL:** When this bit is set to 1b, FCLK will never be gated when the memory controller PLL is ON. Otherwise, FCLK gating policies are not affected by the locking of the memory controller PLLs.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**NSWAKE_SREXIT:** When this bit is set to 1b, a Non-Snoop wakeup signal from PCH sideband indication will cause the PCU to force the MC to exit from Self-Refresh. Otherwise, the Non-Snoop indication will not affect the Self Refresh exit policy.
11	0h RW	**SACG_SREXIT:** The Display Engine can indicate to the PCU that it wants the Memory Controller to exit self-refresh. When this bit is set to 1b, this request from the Display Engine will cause FCLK to be ungated. Otherwise, this request from the Display Engine has no effect on FCLK gating.
10	0h RW	**MDLL_OFF_SEN:** This bit indicates when the Memory Initiator DLL may be shutdown based on link active power states. 0b Memory DLL may be shut down in L1 and deeper sleep states. 1b Memory DLL may be shut down in L0s and deeper sleep states.
9	0h RW	**MPLL_OFF_SEN:** This bit indicates when the Memory PLLs (MCPLL and GDPLL) may be shutdown based on link active power states. 0b Memory PLLs may be shut down in L1 and deeper sleep states. 1b Memory PLLs may be shut down in L0s and deeper sleep states.
8	1h RW	**SACG_SEN:** This bit indicates when the System Agent clock gating is possible based on link active power states. 0b System Agent clock gating is allowed in L1 and deeper sleep states. 1b System Agent clock gating is allowed in L0s and deeper sleep states.
7:3	0h RO	**Reserved**
2	1h RW	**PPLL_OFF_ENA:** This bit is used to enable shutting down the PCIe/DMI PLL. 0b PLL shutdown is not allowed 1b PLL shutdown is allowed
1	1h RW	**MPLL_OFF_ENA:** This bit is used to enable shutting down the Memory Controller PLLs (MCPLL and GDPLL). 0b PLL shutdown is not allowed 1b PLL shutdown is allowed
0	0h RW	**SACG_ENA:** This bit is used to enable or disable the System Agent Clock Gating (FCLK). 0b SA Clock Gating is Not Allowed 1b SA Clock Gating is Allowed

3.3.45 CONFIG_TDP_NOMINAL_0_0_0_MCHBAR_PCU — Offset 5F3Ch

This register is used to indicate the Nominal Configurable TDP ratio available for this

specific sku. System BIOS must use this value while building the _PSS table if the feature is enabled.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5F3Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO/V	**TDP_RATIO:** Nominal TDP level ratio to be used for this specific processor (in units of 100 MHz). Note: A value of 0 in this field indicates invalid/undefined TDP point

3.3.46 CONFIG_TDP_LEVEL1_0_0_0_MCHBAR_PCU — Offset 5F40h

Level 1 configurable TDP settings

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5F40h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63	0h RO	**Reserved**
62:48	0000h RO/V	**PKG_MIN_PWR:** Min pkg power setting allowed for this config TDP level. Lower values will be clamped up to this value. Units defined in PACKAGE_POWER_SKU_MSR[PWR_UNIT]. Similar to PACKAGE_POWER_SKU[PKG_MIN_PWR].
47	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
46:32	0000h RO/V	**PKG_MAX_PWR:** Max pkg power setting allowed for this config TDP level1. Higher values will be clamped down to this value. Units defined in PACKAGE_POWER_SKU_MSR[PWR_UNIT]. Similar to PACKAGE_POWER_SKU[PKG_MAX_PWR].
31:24	0h RO	**Reserved**
23:16	00h RO/V	**TDP_RATIO:** TDP ratio for config tdp level 1.
15	0h RO	**Reserved**
14:0	0000h RO/V	**PKG_TDP:** Power for this TDP level. Units defined in PACKAGE_POWER_SKU_MSR[PWR_UNIT] Similar to PACKAGE_POWER_SKU[PKG_TDP]

3.3.47 CONFIG_TDP_LEVEL2_0_0_0_MCHBAR_PCU — Offset 5F48h

Level 2 configurable TDP settings

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5F48h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63	0h RO	**Reserved**
62:48	0000h RO/V	**PKG_MIN_PWR:** Min pkg power setting allowed for this config TDP level 2. Lower values will be clamped up to this value. Units defined in PACKAGE_POWER_SKU_MSR[PWR_UNIT]. Similar to PACKAGE_POWER_SKU[PKG_MIN_PWR].
47	0h RO	**Reserved**
46:32	0000h RO/V	**PKG_MAX_PWR:** Max pkg power setting allowed for config TDP level 2. Higher values will be clamped down to this value. Units defined in PACKAGE_POWER_SKU_MSR[PWR_UNIT]. Similar to PACKAGE_POWER_SKU[PKG_MAX_PWR].
31:24	0h RO	**Reserved**
23:16	00h RO/V	**TDP_RATIO:** TDP ratio for level 2.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14:0	0000h RO/V	**PKG_TDP:** Power for this TDP level. Units defined in PACKAGE_POWER_SKU_MSR[PWR_UNIT] Similar to PACKAGE_POWER_SKU[PKG_TDP].

3.3.48 CONFIG_TDP_CONTROL_0_0_0_MCHBAR_PCU — Offset 5F50h

Rd/Wr register to allow platform SW to select TDP point and set lock

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5F50h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**CONFIG_TDP_LOCK:** Config TDP level select lock 0 - unlocked. 1 - locked till next reset. **Locked by:** CONFIG_TDP_CONTROL.CONFIG_TDP_LOCK
30:2	0h RO	**Reserved**
1:0	0h RW/L	**TDP_LEVEL:** Config TDP level selected 0 = nominal TDP level (default) 1 = Level from CONFIG_TDP_LEVEL_1 2 = Level from CONFIG_TDP_LEVEL_2 3 = reserved **Locked by:** CONFIG_TDP_CONTROL.CONFIG_TDP_LOCK

3.3.49 TURBO_ACTIVATION_RATIO_0_0_0_MCHBAR_PCU — Offset 5F54h

Read/write register to allow MSR/MMIO access to ACPI P-state notify (PCS 33).

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5F54h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**TURBO_ACTIVATION_RATIO_LOCK:** Lock this MSR until next reset 0 - unlocked 1 - locked **Locked by:** TURBO_ACTIVATION_RATIO.TURBO_ACTIVATION_RATIO_LOCK
30:8	0h RO	**Reserved**
7:0	00h RW/L	**MAX_NON_TURBO_RATIO:** CPU will treat any P-state request above this ratio as a request for max turbo 0 is special encoding which disables the feature. **Locked by:** TURBO_ACTIVATION_RATIO.TURBO_ACTIVATION_RATIO_LOCK

3.3.50 OC_STATUS_0_0_0_MCHBAR_PCU — Offset 5F58h

give overclockers the ability to adjust memory timing values. We need to expose to SW when the ability to modify these registers is enabled, so that secure features can react appropriately

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 5F58h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO	**MC_TIMING_RUNTIME_OC_ENABLED:** Adjusting memory timing values for overclocking is enabled.

3.3.51 BCLK_FREQ_0_0_0_MCHBAR — Offset 5F60h

This MMIO register will be written by pcode to report the BCLK frequency.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5F60h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:32	00000000h RO	**PCIECLK_FREQ:** Reported PCIE BCLK Frequency in Khz
31:0	00000000h RO	**BCLK_FREQ:** Reported BCLK Frequency in Khz

3.4 Host Controller (MCHBAR) Registers

This section contains the Host Controller MCHBAR registers.

Base address of these registers are defined in the MCHBAR_0_0_0_PCI register in Bus: 0, Device: 0, Function: 0.

3.4.1 Summary of Registers

Table 3-5. Summary of MCHBAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
7090h	4	TCSS_DEVEN MCHBAR_IMPH (TCSS_DEVEN_0_0_0_MCHBAR_IMPH)	00003FFFh
7094h	4	CAPID0_D MCHBAR (CAPID0_D_0_0_0_MCHBAR)	00000000h
7098h	4	CAPID0_F PCI (CAPID0_F_0_0_0_PCI)	00000000h
7110h	8	REGBAR MCHBAR_IMPH (REGBAR_0_0_0_MCHBAR_IMPH)	0000000000000000h

3.4.2 TCSS_DEVEN MCHBAR_IMPH (TCSS_DEVEN_0_0_0_MCHBAR_IMPH) — Offset 7090h

Allows for enabling/disabling of Type-C PCI devices and functions that are within the CPU package. The table below the bit definitions describes the behavior of all combinations of transactions to devices controlled by this register. All the bits in this register are Intel TXT Lockable.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7090h	00003FFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	1h RW/L	**Reserved**
12	1h RW/L	**Reserved**
11	1h RW/L	**Reserved**
10	1h RW/L	**Reserved**
9	1h RW/L	**xDCI EN (XDCI_EN):** xDCI Enable - 0: xDCI is disabled and hidden. 1: xDCI is enabled and visible. **Locked by:** CAPID0_D_0_0_0_MCHBAR.TC_XDCI_DIS
8	1h RW/L	**xHCI EN (XHCI_EN):** xHCI Enable - 0: xHCI is disabled and hidden. 1: xHCI is enabled and visible. **Locked by:** CAPID0_D_0_0_0_MCHBAR.TC_XHCI_DIS
7	1h RW/L	**PCIE7 EN (PCIE7_EN):** PCIE7 Enable 0: TypeC PCIE RP7 is disabled 1: TypeC PCIE RP7 is enabled **Locked by:** CAPID0_D_0_0_0_MCHBAR.TC_PCIE7_DIS
6	1h RW/L	**PCIE6 EN (PCIE6_EN):** PCIE6 Enable 0: TypeC PCIE RP6 is disabled 1: TypeC PCIE RP6 is enabled **Locked by:** CAPID0_D_0_0_0_MCHBAR.TC_PCIE6_DIS

Bit Range	Default & Access	Field Name (ID): Description
5	1h RW/L	**PCIE5 EN (PCIE5_EN):** PCIE5 Enable 0: TypeC PCIE RP5 is disabled 1: TypeC PCIE RP5 is enabled **Locked by:** CAPID0_D_0_0_0_MCHBAR.TC_PCIE5_DIS
4	1h RW/L	**PCIE4 EN (PCIE4_EN):** PCIE4 Enable 0: TypeC PCIE RP4 is disabled 1: TypeC PCIE RP4 is enabled **Locked by:** CAPID0_D_0_0_0_MCHBAR.TC_PCIE4_DIS
3	1h RW/L	**PCIE3 EN (PCIE3_EN):** PCIE3 Enable 0: TypeC PCIE RP3 is disabled 1: TypeC PCIE RP3 is enabled **Locked by:** CAPID0_D_0_0_0_MCHBAR.TC_PCIE3_DIS
2	1h RW/L	**PCIE2 EN (PCIE2_EN):** PCIE2 Enable 0: TypeC PCIE RP2 is disabled 1: TypeC PCIE RP2 is enabled **Locked by:** CAPID0_D_0_0_0_MCHBAR.TC_PCIE2_DIS
1	1h RW/L	**PCIE1 EN (PCIE1_EN):** PCIE1 Enable 0: TypeC PCIE RP1 is disabled 1: TypeC PCIE RP1 is enabled **Locked by:** CAPID0_D_0_0_0_MCHBAR.TC_PCIE1_DIS
0	1h RW/L	**PCIE0 EN (PCIE0_EN):** PCIE0 Enable 0: TypeC PCIE RP0 is disabled 1: TypeC PCIE RP0 is enabled **Locked by:** CAPID0_D_0_0_0_MCHBAR.TC_PCIE0_DIS

3.4.3 CAPID0_D MCHBAR (CAPID0_D_0_0_0_MCHBAR) — Offset 7094h

Control of bits in this register are only required for customer visible SKU differentiation.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7094h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:17	0h RW/L	**DPIN PORT COUNT (DPIN_PORT_COUNT):** This field indicates the max number of DPin ports enabled by fuses

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW/L	**IOM DISABLE (IOM_DIS):** 1 - Type C IOM is Disabled 0 - Type C IOM is Enabled
15:13	0h RO	**Reserved**
12	0h RW/L	**Reserved**
11	0h RW/L	**Reserved**
10	0h RW/L	**Reserved**
9	0h RW/L	**TC XDCI DIS (TC_XDCI_DIS):** Indicates if Type-C XDCI device is disabled.
8	0h RW/L	**TC XHCI DIS (TC_XHCI_DIS):** Indicates if Type-C XHCI device is disabled.
7	0h RW/L	**TC PCIE7 DIS (TC_PCIE7_DIS):** Indicates if Type-C PCIE7 device is disabled.
6	0h RW/L	**TC PCIE6 DIS (TC_PCIE6_DIS):** Indicates if Type-C PCIE6 device is disabled.
5	0h RW/L	**TC PCIE5 DIS (TC_PCIE5_DIS):** Indicates if Type-C PCIE5 device is disabled.
4	0h RW/L	**TC PCIE4 DIS (TC_PCIE4_DIS):** Indicates if Type-C PCIE4 device is disabled.
3	0h RW/L	**TC PCIE3 DIS (TC_PCIE3_DIS):** Indicates if Type-C PCIE3 device is disabled.
2	0h RW/L	**TC PCIE2 DIS (TC_PCIE2_DIS):** Indicates if Type-C PCIE2 device is disabled.
1	0h RW/L	**TC PCIE1 DIS (TC_PCIE1_DIS):** Indicates if Type-C PCIE1 device is disabled.
0	0h RW/L	**TC PCIE0 DIS (TC_PCIE0_DIS):** Indicates if Type-C PCIE0 device is disabled.

3.4.4 CAPID0_F PCI (CAPID0_F_0_0_0_PCI) — Offset 7098h

Control of bits in this register are only required for customer visible SKU differentiation.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + 7098h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW/L	**MAX DATA RATE AT GEAR1 (MAX_DATA_RATE_AT_GEAR1):** This field controls the max DDR data rate at gear1 (it is equal to the QCLK ratio) in 33MHz granularity. 0 means unlimited

3.4.5 REGBAR MCHBAR_IMPH (REGBAR_0_0_0_MCHBAR_IMPH) — Offset 7110h

This register define the REGBAR.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 7110h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RO	**Reserved**
41:24	00000h RW	**REGFBAR:** This field corresponds to bits 41 to 24 of the base address IOSF MMIO (CR) space. BIOS will program this register resulting in a base address for a 16MB block of contiguous memory address space.
23:1	0h RO	**Reserved**
0	0h RW	**REGBAREN:** 0: REGBAR is disabled and does not claim any memory 1: REGBAR memory mapped accesses are claimed and decoded appropriately.

3.5 Direct Media Interface BAR (DMIBAR) Registers

This section contains the DMIBAR registers. Base address of these registers are defined in the DMIBAR_0_0_0_PCI register in Bus: 0, Device: 0, Function: 0.

3.5.1 Summary of Registers

Table 3-6. Summary of DMIBAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	DMIVCECH_0_0_0_DMIBAR	04010002h
4h	4	DMIPVCCAP1_0_0_0_DMIBAR	00000000h
8h	4	DMIPVCCAP2_0_0_0_DMIBAR	00000000h
Ch	2	DMIPVCCTL_0_0_0_DMIBAR	0000h
10h	4	DMIVC0RCAP_0_0_0_DMIBAR	00000001h
1Ch	4	DMIVC1RCAP_0_0_0_DMIBAR	00000001h
26h	2	DMIVC1RSTS_0_0_0_DMIBAR	0002h
34h	4	DMIVCMRCAP_0_0_0_DMIBAR	00008000h
38h	4	DMIVCMRCTL_0_0_0_DMIBAR	07000180h
3Eh	2	DMIVCMRSTS_0_0_0_DMIBAR	0002h
40h	4	DMIRCLDECH_0_0_0_DMIBAR	08010005h
44h	4	DMIESD_0_0_0_DMIBAR	01000202h
50h	4	DMILE1D_0_0_0_DMIBAR	00000000h
5Ch	4	DMILUE1A_0_0_0_DMIBAR	00000000h
60h	4	DMILE2D_0_0_0_DMIBAR	00000000h
68h	4	DMILE2A_0_0_0_DMIBAR	00000000h
88h	2	LCTL_0_0_0_DMIBAR	0000h
1C4h	4	DMIUESTS_0_0_0_DMIBAR	00000000h
1C8h	4	DMIUEMSK_0_0_0_DMIBAR	00000000h
1CCh	4	DMIUESEV_0_0_0_DMIBAR	00060010h
1D0h	4	DMICESTS_0_0_0_DMIBAR	00000000h
1D4h	4	DMICEMSK_0_0_0_DMIBAR	00002000h

3.5.2 DMIVCECH_0_0_0_DMIBAR — Offset 0h

Indicates DMI Virtual Channel capabilities.

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 0h	04010002h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	040h RO	**PNC:** Pointer to Next Capability: This field contains the offset to the next PCI Express capability structure in the linked list of capabilities (Link Declaration Capability).
19:16	1h RO	**PCIEVCCV:** PCI Express Virtual Channel Capability Version: Hardwired to 1 to indicate compliances with the 1.1 version of the PCI Express specification. Note: This version does not change for 2.0 compliance.
15:0	0002h RO	**ECID:** Extended Capability ID: Value of 0002h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.

3.5.3 DMIPVCCAP1_0_0_0_DMIBAR — Offset 4h

Describes the configuration of PCI Express Virtual Channels associated with this port.

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:4	0h RO	**LPEVCC:** Low Priority Extended VC Count: Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2:0	0h RW/L	**EVCC:** Extended VC Count: Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. The Private Virtual Channel, VC1 and the Manageability Virtual Channel are not included in this count. **Locked by:** TLDMIREGS.WO_STATUS0_0_0_0_DMIBAR.EVCCDWOS

3.5.4 DMIPVCCAP2_0_0_0_DMIBAR — Offset 8h

Describes the configuration of PCI Express Virtual Channels associated with this port.

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**VCATO:** Reserved
23:8	0h RO	**Reserved**
7:0	00h RO	**VCAC:** Reserved

3.5.5 DMIPVCCTL_0_0_0_DMIBAR — Offset Ch

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:4	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
3:1	0h RW	**VCAS:** VC Arbitration Select: This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. The value 000b when written to this field will indicate the VC arbitration scheme is hardware fixed (in the root complex). This field cannot be modified when more than one VC in the LPVC group is enabled. 000: Hardware fixed arbitration scheme. E.G. Round Robin Others: Reserved See the PCI express specification for more details.
0	0h RO	**LVCAT:** Reserved

3.5.6 DMIVC0RCAP_0_0_0_DMIBAR — Offset 10h

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 10h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**PATO:** Reserved
23	0h RO	**Reserved**
22:16	00h RO	**MTS:** Reserved
15	0h RO	**REJSNPT:** Reject Snoop Transactions: 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: Any transaction for which the No Snoop attribute is applicable but is not set within the TLP Header will be rejected as an Unsupported Request.
14:8	0h RO	**Reserved**
7:0	01h RO	**PAC:** Port Arbitration Capability: Having only bit 0 set indicates that the only supported arbitration scheme for this VC is non-configurable hardware-fixed.

3.5.7 DMIVC1RCAP_0_0_0_DMIBAR — Offset 1Ch

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 1Ch	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**PATO:** Reserved
23	0h RO	**Reserved**
22:16	00h RO	**MTS:** Reserved
15	0h RO	**REJSNPT:** Reject Snoop Transactions: 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: When Set, any transaction for which the No Snoop attribute is applicable but is not Set within the TLP Header will be rejected as an Unsupported Request.
14:8	0h RO	**Reserved**
7:0	01h RO	**PAC:** Port Arbitration Capability: Having only bit 0 set indicates that the only supported arbitration scheme for this VC is non-configurable hardware-fixed.

3.5.8 DMIVC1RSTS_0_0_0_DMIBAR — Offset 26h

Reports the Virtual Channel specific status.

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + 26h	0002h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1	1h RO/V	**VC1NP:** Virtual Channel 1 Negotiation Pending: 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). Software may use this bit when enabling or disabling the VC. This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	0h RO	**Reserved**

3.5.9 DMIVCMRCAP_0_0_0_DMIBAR — Offset 34h

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 34h	00008000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	1h RO	**REJSNPT:** Reject Snoop Transactions: 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on the VC. 1: When Set, any transaction for which the No Snoop attribute is applicable but is not Set within the TLP Header will be rejected as an Unsupported Request
14:0	0h RO	**Reserved**

3.5.10 DMIVCMRCTL_0_0_0_DMIBAR — Offset 38h

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 38h	07000180h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**VCMEN:** Virtual Channel enable: 0: Virtual Channel is disabled. 1: Virtual Channel is enabled. See exceptions below. Software must use the VC Negotiation Pending bit to check whether the VC negotiation is complete. When VC Negotiation Pending bit is cleared, a 1 read from this VC Enable bit indicates that the VC is enabled (Flow Control Initialization is completed for the PCI Express port). A 0 read from this bit indicates that the Virtual Channel is currently disabled. BIOS Requirement: 1. To enable a Virtual Channel, the VC Enable bits for that Virtual Channel must be set in both Components on a Link. 2. To disable a Virtual Channel, the VC Enable bits for that Virtual Channel must be cleared in both Components on a Link. 3. Software must ensure that no traffic is using a Virtual Channel at the time it is disabled. 4. Software must fully disable a Virtual Channel in both Components on a Link before re-enabling the Virtual Channel.
30:27	0h RO	**Reserved**
26:24	7h RW	**VCID:** Virtual Channel ID: Assigns a VC ID to the VC resource. Assigned value must be non-zero. This field can not be modified when the VC is already enabled.
23:13	0h RO	**Reserved**
12:8	01h RW/V/L	**FC_FSM_STATE:** This register is for Save Restore to restore the FC fsm
7:0	80h RO	**TCVCMMAP:** Traffic Class/Virtual Channel Map: Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.

3.5.11 DMIVCMRSTS_0_0_0_DMIBAR — Offset 3Eh

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + 3Eh	0002h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**
1	1h RO/V	**VCNEGPND:** Virtual Channel Negotiation Pending: 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). Software may use this bit when enabling or disabling the VC. This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	0h RO	**Reserved**

3.5.12 DMIRCLDECH_0_0_0_DMIBAR — Offset 40h

This capability declares links from the respective element to other elements of the root complex component to which it belongs and to an element in another root complex component. See PCI Express specification for link/topology declaration requirements.

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 40h	08010005h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	080h RO	**PNC:** Pointer to Next Capability: This field contains the offset to the next PCI Express capability structure in the linked list of capabilities (Internal Link Control Capability).
19:16	1h RO	**LDCV:** Link Declaration Capability Version: Hardwired to 1 to indicate compliances with the 1.1 version of the PCI Express specification. Note: This version does not change for 2.0 compliance.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0005h RO	**ECID:** Extended Capability ID: Value of 0005h identifies this linked list item (capability structure) as being for PCI Express Link Declaration Capability.

3.5.13 DMIESD_0_0_0_DMIBAR — Offset 44h

Provides information about the root complex element containing this Link Declaration Capability.

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 44h	01000202h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	01h RO	**PORTNUM:** Port Number: Specifies the port number associated with this element with respect to the component that contains this element. This port number value is utilized by the egress port of the component to provide arbitration to this Root Complex Element.
23:16	00h RW/L	**CID:** Component ID: Identifies the physical component that contains this Root Complex Element. BIOS Requirement: Must be initialized according to guidelines in the PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS). **Locked by:** TLDMIREGS.WO_STATUS0_0_0_0_DMIBAR.CIDDWOS
15:8	02h RO	**NLE:** Number of Link Entries: Indicates the number of link entries following the Element Self Description. This field reports 2 (one for MCH egress port to main memory and one to egress port belonging to ICH on other side of internal link).
7:4	0h RO	**Reserved**
3:0	2h RO	**ETYP:** Element Type: Indicates the type of the Root Complex Element. Value of 2h represents an Internal Root Complex Link (DMI).

3.5.14 DMILE1D_0_0_0_DMIBAR — Offset 50h

First part of a Link Entry which declares an internal link to another Root Complex Element.

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 50h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW/L	**TPN:** Target Port Number: Specifies the port number associated with the element targeted by this link entry (egress port of PCH). The target port number is with respect to the component that contains this element as specified by the target component ID. This can be programmed by BIOS, but the default value will likely be correct because the DMI RCRB in the PCH will likely be associated with the default egress port for the PCH meaning it will be assigned port number 0. **Locked by:** TLDMIREGS.WO_STATUS0_0_0_0_DMIBAR.TPNWOS
23:16	00h RW/L	**TCID:** Target Component ID: Identifies the physical component that is targeted by this link entry. BIOS Requirement: Must be initialized according to guidelines in the PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS). **Locked by:** TLDMIREGS.WO_STATUS0_0_0_0_DMIBAR.TCIDE1DWOS
15:2	0h RO	**Reserved**
1	0h RO	**LTYP:** Link Type: Indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	0h RW/L	**LV:** Link Valid: 0: Link Entry is not valid and will be ignored. 1: Link Entry specifies a valid link. **Locked by:** TLDMIREGS.WO_STATUS0_0_0_0_DMIBAR.LVE1DWOS

3.5.15 DMILUE1A_0_0_0_DMIBAR — Offset 5Ch

Second part of a Link Entry which declares an internal link to another Root Complex Element.

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 5Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW/L	**ULA:** Upper Link Address: Memory mapped base address of the RCRB that is the target element (egress port of PCH) for this link entry. **Locked by:** TLDMIREGS.WO_STATUS0_0_0_0_DMIBAR.ULAE1DWOS

3.5.16 DMILE2D_0_0_0_DMIBAR — Offset 60h

First part of a Link Entry which declares an internal link to another Root Complex Element.

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 60h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**TPN:** Target Port Number: Specifies the port number associated with the element targeted by this link entry (Egress Port). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	00h RW/L	**TCID:** Target Component ID: Identifies the physical or logical component that is targeted by this link entry. BIOS Requirement: Must be initialized according to guidelines in the PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS). **Locked by:** TLDMIREGS.WO_STATUS0_0_0_0_DMIBAR.TCIDE2DWOS
15:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1	0h RO	**LTYP:** Link Type: Indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	0h RW/L	**LV:** Link Valid: 0: Link Entry is not valid and will be ignored. 1: Link Entry specifies a valid link. **Locked by:** TLDMIREGS.WO_STATUS0_0_0_0_DMIBAR.LVE2DWOS

3.5.17 DMILE2A_0_0_0_DMIBAR — Offset 68h

Second part of a Link Entry which declares an internal link to another Root Complex Element.

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 68h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW/L	**LA:** Link Address: Memory mapped base address of the RCRB that is the target element (Egress Port) for this link entry. **Locked by:** TLDMIREGS.WO_STATUS0_0_0_0_DMIBAR.LAE2DWOS
11:0	0h RO	**Reserved**

3.5.18 LCTL_0_0_0_DMIBAR — Offset 88h

Allows control of PCI Express link.

Type	Size	Offset	Default
MMIO	16 bit	DMIBAR + 88h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**HAWD:** OPI - N/A Hardware Autonomous Width Disable: Hardware Autonomous Width Disable - When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Devices that do not implement the ability autonomously to change Link width are permitted to hardwire this bit to 0b.
8	0h RO	**Reserved**
7	0h RW	**ES:** OPI - N/A Extended Synch: Extended synch 0: Standard Fast Training Sequence (FTS). 1: Forces the transmission of additional ordered sets when exiting the L0s state and when in the Recovery state. This mode provides external devices (e.g., logic analyzers) monitoring the Link time to achieve bit and symbol lock before the link enters L0 and resumes communication. This is a test mode only and may cause other undesired side effects such as buffer overflows or underruns.
6	0h RO	**Reserved**
5	0h RO	**RL:** Retrain Link: 0: Normal operation. 1: Full Link retraining is initiated by directing the Physical Layer LTSSM from L0, L0s, or L1 states to the Recovery state. This bit always returns 0 when read. This bit is cleared automatically (no need to write a 0).
4:2	0h RO	**Reserved**
1:0	0h RO	**ASPM:** Active State PM: Controls the level of active state power management supported on the given link. 00: Disabled 01: L0s Entry Supported 10: L1 Entry Supported 11: L0s and L1 Entry Supported

3.5.19 DMIUESTS_0_0_0_DMIBAR — Offset 1C4h

DMI Uncorrectable Error Status register. This register is for test and debug purposes only.

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 1C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RW/1C/V/P	**URES:** Unsupported Request Error Status:
19	0h RO	**Reserved**
18	0h RW/1C/V/P	**MTLPS:** Malformed TLP Status:
17	0h RW/1C/V/P	**ROS:** Receiver Overflow Status:
16	0h RW/1C/V/P	**UCS:** Unexpected Completion Status:
15	0h RO	**Reserved**
14	0h RW/1C/V/P	**CTS:** Completion Timeout Status:
13	0h RO	**Reserved**
12	0h RW/1C/V/P	**PTLPS:** Poisoned TLP Status:
11:5	0h RO	**Reserved**
4	0h RW/1C/V/P	**DLPES:** Data Link Protocol Error Status:
3:0	0h RO	**Reserved**

3.5.20 DMIUEMSK_0_0_0_DMIBAR — Offset 1C8h

DMI Uncorrectable Error Mask register. This register is for test and debug purposes only.

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 1C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22	0h RW/P	**ECCERRM:** 2 Bit Error Mask:
21	0h RO	**Reserved**
20	0h RW/P	**UREM:** Unsupported Request Error Mask:
19	0h RO	**Reserved**
18	0h RW/P	**MTLPM:** Malformed TLP Mask:
17	0h RW/P	**ROM:** Receiver Overflow Mask:
16	0h RW/P	**UCM:** Unexpected Completion Mask:
15	0h RO	**Reserved**
14	0h RW/P	**CPLTM:** Completion Timeout Mask:
13	0h RO	**Reserved**
12	0h RW/P	**PTLPM:** Poisoned TLP Mask:
11:5	0h RO	**Reserved**
4	0h RW/P	**DLPEM:** Data Link Protocol Error Mask:
3:0	0h RO	**Reserved**

3.5.21 DMIUESEV_0_0_0_DMIBAR — Offset 1CCh

DMI Uncorrectable Error Severity register. This register controls whether an individual error is reported as a non-fatal or fatal error. An error is reported as fatal when the corresponding error bit in the severity register is set. If the bit is cleared, the corresponding error is considered nonfatal. It is for test and debug purposes only.

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 1CCh	00060010h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22	0h RW/P	**ECCERRS:** 2 Bit Error Mask:
21	0h RO	**Reserved**
20	0h RW/P	**URES:** Unsupported Request Error Severity:
19	0h RO	**ECRCES:** Reserved
18	1h RW/P	**MTLPES:** Malformed TLP Error Severity:
17	1h RW/P	**ROEV:** Receiver Overflow Error Severity:
16	0h RW/P	**UCES:** Unexpected Completion Error Severity:
15	0h RO	**CAES:** Reserved
14	0h RW/P	**CTES:** Completion Timeout Error Severity:
13	0h RO	**FCPES:** Reserved
12	0h RW/P	**PTLPES:** Poisoned TLP Error Severity:
11:5	0h RO	**Reserved**
4	1h RW/P	**DLPES:** Data Link Protocol Error Severity:
3:0	0h RO	**Reserved**

3.5.22 DMICESTS_0_0_0_DMIBAR — Offset 1D0h

DMI Correctable Error Status Register. This register is for test and debug purposes only.

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 1D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RW/1C/V/P	**ANFES:** Advisory Non-Fatal Error Status: When set, indicates that an Advisory Non-Fatal Error occurred.
12	0h RW/1C/V/P	**RTTS:** Replay Timer Timeout Status:
11:9	0h RO	**Reserved**
8	0h RW/1C/V/P	**RNRS:** REPLAY_NUM Rollover Status:
7	0h RW/1C/V/P	**BDLLPS:** Bad DLLP Status:
6	0h RW/1C/V/P	**BTLPS:** Bad TLP Status:
5:1	0h RO	**Reserved**
0	0h RW/1C/V/P	**RES:** Receiver Error Status: Physical layer receiver Error occurred. These errors include: elastic Buffer Collision, 8b/10b error, De-skew Timeout Error.

3.5.23 DMICEMSK_0_0_0_DMIBAR — Offset 1D4h

DMI Correctable Error Mask register. This register is for test and debug purposes only.

Type	Size	Offset	Default
MMIO	32 bit	DMIBAR + 1D4h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	1h RW/P	**ANFEM:** Advisory Non-Fatal Error Mask: When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register, and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.
12:0	0h RO	**Reserved**

3.6 REGBAR Registers

This section contains the REGBAR registers. Base address of these registers are defined in the REGBAR_0_0_0_MCHBAR_IMPH register which resides in the MCHBAR register collection.

3.6.1 Summary of Registers

Table 3-7. Summary of REGBAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
C10010h	4	IOM CSME IMR MG STATUS REG (IOM_CSME_IMR_MG_STATUS)	00000000h
C10160h	4	IOM PORT STATUS (IOM_PORT_STATUS[0])	00000000h
C10164h	4	IOM PORT STATUS (IOM_PORT_STATUS[1])	00000000h
C10168h	4	IOM PORT STATUS (IOM_PORT_STATUS[2])	00000000h
C1016Ch	4	IOM PORT STATUS (IOM_PORT_STATUS[3])	00000000h
C10098h	4	IOM_TYPEC_SW_CONFIGURATION 4 (IOM_TYPEC_SW_CONFIGURATION_4)	00000000h
C1102Ch	4	IOM DP RESOURCE MNG REG (IOM_DP_RESOURCE_MNG[0])	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
C11030h	4	IOM DP RESOURCE MNG REG (IOM_DP_RESOURCE_MNG[1])	00000000h
C11038h	4	IOM DP HW RESOURCE SEMAPHORE (IOM_DP_HW_RESOURCE_SEMAPHORE[0])	00000000h
C1103Ch	4	IOM DP HW RESOURCE SEMAPHORE (IOM_DP_HW_RESOURCE_SEMAPHORE[1])	00000000h
C118F8h	4	IOM FW CURRENT STATUS REG (IOM_FW_CURRENT_STATUS)	00000000h
C118FCh	4	IOM FW CURRENT TASK REG (IOM_FW_CURRENT_TASK)	00000000h

3.6.2 IOM CSME IMR MG STATUS REG (IOM_CSME_IMR_MG_STATUS) — Offset C10010h

PHY Image Status in IMR

Type	Size	Offset	Default
MMIO	32 bit	REGBAR + C10010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/P	**FW Download Done (DONE):** FW download to IMR is done
30	0h RW/P	**Valid Authentication (VALID):** Valid: although the FW is in the IMR, it failed authentication and therefore shouldn't be trusted. 0 - untrusted FW, 1 - successful authentication -it is ok to use the code
29:22	00h RW/P	**ERROR CODE (ERROR_CODE):** ERROR CODE Logged by CSME while populating PHY IMR.
21:16	0h RO	**Reserved**
15:0	0000h RW/P	**Firmware Version (FW_VERSION):** The version of firmware that MG is using.

3.6.3 IOM PORT STATUS (IOM_PORT_STATUS[0]) — Offset C10160h

TypeC port (PHY) status and control. Note that 'Port' and 'PHY' are used interchangeably

Type	Size	Offset	Default
MMIO	32 bit	REGBAR + C10160h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/P	**Port Is Connected (PORT_IS_CONNECTED):** Status indication that the port is connected. Maintained by IOM FW. 0x0: Port is not connected. 0x1: Port is connected (IOM FW is done configuring the port).
30:29	0h RO	**Reserved**
28	0h RW/P	**Aux Orientation (AUX_ORI):** Aux orientation status Status. Maintained by IOM FW. 1'b0: Orientation is not flipped. 1'b1: Orientation is flipped.
27:20	00h RW/P	**Mode Type (MODE_TYPE):** Mode Type. Maintained by IOM FW. Various usage models. Example is to specify the NiDnT overlay mode or Intel debug overlay mode.
19:12	00h RW/P	**HPD Status (DHPD):** HPD status. Maintained by IOM FW DHPD[1:0] - HPD current state. 0x0: No HPD. 0x1: HPD asserted. 0x2: HPD deasserted. 0x3 Invalid. DHPD[2:2] - HPD current state source. 0x0: PCH. 0x1: Reserved DHPD[3:3] - HPD current state destination. 0x0: DP. 0x1: DPin. DHPD[5:4] - Deferred HPD current state. 0x0: No HPD. 0x1: HPD asserted. 0x2: HPD deasserted. 0x3 Invalid. DHPD[6:6] - Deferred HPD current state source. 0x0: PCH. 0x1: Reserved DHPD[7:7] - Reserved.
11	0h RW/P	**High Speed Link Orientation Status (HSL_ORI):** High-Speed Link Orientation Status. Maintained by IOM FW. 1'b0: Orientation is not flipped. 1'b1: Orientation is flipped.
10	0h RW/P	**Upstream Facing Port Status (UFP):** UFP: Upstream Facing Port Status. Maintained by IOM FW. 1'b0: Downstream facing port. TCSS USB is configured to be the Host. 1'b1: Upstream facing port. TCSS USB is configured to be the Device.

Bit Range	Default & Access	Field Name (ID): Description
9:6	0h RW/P	**Port activity type (ACTIVITY_TYPE):** Port activity type. The TypeC PHY is flexible thus it can be configured for various possible connections. Maintained by IOM FW. 0x0: Undefined 0x1: Fixed connection 0x2: DPin 0x3: USB3 0x4: Safe mode 0x5: Alt mode DP 0x6: Alt mode DP MFD (Multi Function Device) 0x7: **Reserved** 0x8: HTI (High-speed Trace Interface - used for debug) 0x9: Alt mode NiDNT (Debug mode) 0xA: DBGACC (Debug Acessory) 0xB: HTI direct 0xC: Alt mode USB3 0xD: Reserved 0xE: Reserved
5	0h RW/P	**Configuration Done (CFG_DONE):** Control / Status bit to indicate that the port configuration is complete. This bit is also tied to the PHY common lane reset. Maintained by IOM FW. 1'b1: Port configuration is complete. Deassert TypeC PHY (port) common lane reset. 1'b0: Port configuration is not complete. Assert TypeC PHY (port) common lane reset.
4	0h RW/P	**Port in Transition (PORT_IN_TRANSITION):** Indicator that the port bringup is in progress. Maintained by IOM FW.
3	0h RW/P	**Port Enabled (PORT_EN):** Status indicator if the PHY is enabled by BIOS. Maintained by IOM FW.
2:0	0h RW/P	**PHY Command (CMD):** PHY Command: 0x0: NO-OP, 0x1: Wake PHY, 0x2: VNN OFF prep, 0x3: VNNAON OFF prep

3.6.4 IOM PORT STATUS (IOM_PORT_STATUS[1]) — Offset C10164h

TypeC port (PHY) status and control. Note that 'Port' and 'PHY' are used interchangeably

Note: **NOTE:** Bit definitions are the same as IOM_PORT_STATUS[0], offset C10160h.

3.6.5 IOM PORT STATUS (IOM_PORT_STATUS[2]) — Offset C10168h

TypeC port (PHY) status and control. Note that 'Port' and 'PHY' are used interchangeably

Note: **NOTE:** Bit definitions are the same as IOM_PORT_STATUS[0], offset C10160h.

3.6.6 IOM PORT STATUS (IOM_PORT_STATUS[3]) — Offset C1016Ch

TypeC port (PHY) status and control. Note that 'Port' and 'PHY' are used interchangeably

Note: **NOTE:** Bit definitions are the same as IOM_PORT_STATUS[0], offset C10160h.

3.6.7 IOM_TYPEC_SW_CONFIGURATION 4 (IOM_TYPEC_SW_CONFIGURATION_4) — Offset C10098h

define high speed lane orientation - if HSL Orientation override is enabled and set, the HSL orientation is flipped

Type	Size	Offset	Default
MMIO	32 bit	REGBAR + C10098h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**LOCK:** LOCK **Locked by:** IOM_TYPEC_SW_CONFIGURATION_4.LOCK
30:12	00000h RW	**BFFI:** BFFI **Locked by:** IOM_TYPEC_SW_CONFIGURATION_4.LOCK
11	0h RW/L	**PORT6 HSL ORIENTATION (PORT6_HSL_ORIENTATION):** High Speed Lane Orientation. **Locked by:** IOM_TYPEC_SW_CONFIGURATION_4.LOCK
10	0h RW/L	**PORT6 HSL ORIENTATION_OVERIDE ENABLE (PORT6_HSL_ORIENTATION_OVRRD_EN):** HSL Orientation Override enable **Locked by:** IOM_TYPEC_SW_CONFIGURATION_4.LOCK
9	0h RW/L	**PORT5 HSL ORIENTATION (PORT5_HSL_ORIENTATION):** High Speed Lane Orientation. **Locked by:** IOM_TYPEC_SW_CONFIGURATION_4.LOCK
8	0h RW/L	**PORT5 HSL ORIENTATION_OVERIDE ENABLE (PORT5_HSL_ORIENTATION_OVRRD_EN):** HSL Orientation Override enable **Locked by:** IOM_TYPEC_SW_CONFIGURATION_4.LOCK
7	0h RW/L	**PORT4 HSL ORIENTATION (PORT4_HSL_ORIENTATION):** High Speed Lane Orientation. **Locked by:** IOM_TYPEC_SW_CONFIGURATION_4.LOCK
6	0h RW/L	**PORT4 HSL ORIENTATION_OVERIDE ENABLE (PORT4_HSL_ORIENTATION_OVRRD_EN):** HSL Orientation Override enable **Locked by:** IOM_TYPEC_SW_CONFIGURATION_4.LOCK

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/L	**PORT3 HSL ORIENTATION (PORT3_HSL_ORIENTATION):** High Speed Lane Orientation. **Locked by:** IOM_TYPEC_SW_CONFIGURATION_4.LOCK
4	0h RW/L	**PORT3 HSL ORIENTATION_OVERIDE ENABLE (PORT3_HSL_ORIENTATION_OVRRD_EN):** HSL Orientation Override enable **Locked by:** IOM_TYPEC_SW_CONFIGURATION_4.LOCK
3	0h RW/L	**PORT2 HSL ORIENTATION (PORT2_HSL_ORIENTATION):** High Speed Lane Orientation. **Locked by:** IOM_TYPEC_SW_CONFIGURATION_4.LOCK
2	0h RW/L	**PORT2 HSL ORIENTATION_OVERIDE ENABLE (PORT2_HSL_ORIENTATION_OVRRD_EN):** HSL Orientation Override enable **Locked by:** IOM_TYPEC_SW_CONFIGURATION_4.LOCK
1	0h RW/L	**PORT1 HSL ORIENTATION (PORT1_HSL_ORIENTATION):** High Speed Lane Orientation. **Locked by:** IOM_TYPEC_SW_CONFIGURATION_4.LOCK
0	0h RW/L	**PORT1 HSL ORIENTATION_OVERIDE ENABLE (PORT1_HSL_ORIENTATION_OVRRD_EN):** HSL Orientation Override enable **Locked by:** IOM_TYPEC_SW_CONFIGURATION_4.LOCK

3.6.8 IOM DP RESOURCE MNG REG (IOM_DP_RESOURCE_MNG[0]) — Offset C1102Ch

IOM DP Resource Management Reg

Type	Size	Offset	Default
MMIO	32 bit	REGBAR + C1102Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:4	0h RW	**DP1 Ownership (DP1_ALLOC):** DP1 Ownership: 0x0 Free 0x1 CM 0x2 IOM 0xF:0x3 Reserved"

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RW	**DP0 Ownership (DP0_ALLOC):** DP0 Ownership: 0x0 Free 0x1 CM 0x2 IOM 0xF:0x3 Reserved";

3.6.9 IOM DP RESOURCE MNG REG (IOM_DP_RESOURCE_MNG[1]) — Offset C11030h

IOM DP Resource Management Reg

Note: **NOTE:** Bit definitions are the same as IOM_DP_RESOURCE_MNG[0], offset C1102Ch.

3.6.10 IOM DP HW RESOURCE SEMAPHORE (IOM_DP_HW_RESOURCE_SEMAPHORE[0]) — Offset C11038h

IOM DP HW Resource Semaphore reg

Type	Size	Offset	Default
MMIO	32 bit	REGBAR + C11038h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Semaphore Lock (SEMLOCK):** SemLock: Semaphore lock bit- Initiator write this bit with its iD, If successfully written Initiator Owns this resource. Initiator Should clear the lock as soon as possible
30:4	0h RO	**Reserved**
3:0	0h RO/V	**REQUESTOR ID (REQESTOR_ID):** Requestor ID: 0x0: CM. 0x1: IOM 0x2-0xF Reserved

3.6.11 IOM DP HW RESOURCE SEMAPHORE (IOM_DP_HW_RESOURCE_SEMAPHORE[1]) — Offset C1103Ch

IOM DP HW Resource Semaphore reg

Note: **NOTE:** Bit definitions are the same as IOM_DP_HW_RESOURCE_SEMAPHORE[0], offset C11038h.

3.6.12 IOM FW CURRENT STATUS REG (IOM_FW_CURRENT_STATUS) — Offset C118F8h

FW current staus

Type	Size	Offset	Default
MMIO	32 bit	REGBAR + C118F8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**FW CURRENT STATUS (FW_CURRENT_STATUS):** FW Current Status

3.6.13 IOM FW CURRENT TASK REG (IOM_FW_CURRENT_TASK) — Offset C118FCh

At the beginning of every task management. FW update this Register. For more information on this structure.

Type	Size	Offset	Default
MMIO	32 bit	REGBAR + C118FCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:27	0h RW	**STAGE:** stage of the execution. Always starts with 0. Progrees according to the progress of the thread
26:24	0h RW	**GROUP:** Group: internal use. 000 - PCH initiated 001 - IOM_FW initiated 010 - IOM_HW 011 - PM
23:16	00h RW	**DATA:** Data
15:12	0h RW	**Command Parameter (PARAMS):** IOMFW command parameter.
11:8	0h RW	**USB2 Port Number (USB2_PORT_NUM):** usb2_port_num: USB2 Port Number: 1s based number (first port = port 1). Up to 16 ports can be encoded. A value of '0h' means port 16

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RW	**USB3 Port Number (USB3_PORT_NUM):** usb3_port_num: USB3 Port Number: 1s based number (first port = port 1). Up to 16 ports can be encoded. A value of '0h' means port 16
3:0	0h RW	**OPCODE:** opcode

3.7 PCI Express Egress Port BAR (PXPEPBAR) Registers

This section contains the PXPEPBAR registers. Base address of these registers are defined in the PXPEPBAR_0_0_0_PCI register in Bus: 0, Device: 0, Function: 0.

3.7.1 Summary of Registers

Table 3-8. Summary of PXPEPBAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
Ch	2	EPPVCCTL_0_0_0_PXPEPBAR	0000h
44h	4	EPESD_0_0_0_PXPEPBAR	00000501h

3.7.2 EPPVCCTL_0_0_0_PXPEPBAR — Offset Ch

Type	Size	Offset	Default
MMIO	16 bit	PXPEPBAR + Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:4	0h RO	**Reserved**
3:1	0h RW	**VCAS:** VC Arbitration Select: This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. The value 000b when written to this field will indicate the VC arbitration scheme is hardware fixed (in the root complex). This field cannot be modified when more than one VC in the LPVC group is enabled.
0	0h RO	**LVCAT:** Reserved

3.7.3 EPESD_0_0_0_PXPEPBAR — Offset 44h

Provides information about the root complex element containing this Link Declaration Capability.

Type	Size	Offset	Default
MMIO	32 bit	PXPEPBAR + 44h	00000501h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**PN:** Port Number: This field specifies the port number associated with this element with respect to the component that contains this element. Value of 00 h indicates to configuration software that this is the default egress port.
23:16	00h RW/L	**CID:** Component ID: Identifies the physical component that contains this Root Complex Element. BIOS Requirement: Must be initialized according to guidelines in the PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS). **Locked by:** TLDMIREGS.WO_STATUS0_0_0_0_DMIBAR.CIDPWOS
15:8	05h RO	**NLE:** Number of Link Entries: Indicates the number of link entries following the Element Self Description. This field reports 5 (one each for PEG0, PEG11 PEG12 , PEG1 and DMI).
7:4	0h RO	**Reserved**
3:0	1h RO	**ET:** Element Type: Indicates the type of the Root Complex Element. Value of 1 h represents a port to system memory.

3.8 VTDPVC0BAR Registers

This section contains the VC0PREMAP BAR registers. Base address of these registers are defined in the VTDPVC0BAR_0_0_0_MCHBAR_NCU register which resides in the MCHBAR register collection.

3.8.1 Summary of Registers

Table 3-9. Summary of VTDPVC0BAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Version Register (VER_REG_0_0_0_VTDBAR)	00000050h
8h	8	Capability Register (CAP_REG_0_0_0_VTDBAR)	08D2008C40690462h
10h	8	Extended Capability Register (ECAP_REG_0_0_0_VTDBAR)	0000060000F050DAh
18h	4	Global Command Register (GCMD_REG_0_0_0_VTDBAR)	00000000h
1Ch	4	Global Status Register (GSTS_REG_0_0_0_VTDBAR)	00000000h
20h	8	Root Table Address Register (RTADDR_REG_0_0_0_VTDBAR)	0000000000000000h

Table 3-9. Summary of VTDPVC0BAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
28h	8	Context Command Register (CCMD_REG_0_0_0_VTDBAR)	0800000000000000h
34h	4	Fault Status Register (FSTS_REG_0_0_0_VTDBAR)	00000000h
38h	4	Fault Event Control Register (FECTL_REG_0_0_0_VTDBAR)	80000000h
3Ch	4	Fault Event Data Register (FEDATA_REG_0_0_0_VTDBAR)	00000000h
40h	4	Fault Event Address Register (FEADDR_REG_0_0_0_VTDBAR)	00000000h
44h	4	Fault Event Upper Address Register (FEUADDR_REG_0_0_0_VTDBAR)	00000000h
58h	8	Advanced Fault Log Register (AFLOG_REG_0_0_0_VTDBAR)	0000000000000000h
64h	4	Protected Memory Enable Register (PMEN_REG_0_0_0_VTDBAR)	00000000h
68h	4	Protected Low Memory Base Register (PLMBASE_REG_0_0_0_VTDBAR)	00000000h
6Ch	4	Protected Low-Memory Limit Register (PLMLIMIT_REG_0_0_0_VTDBAR)	00000000h
70h	8	Protected High-Memory Base Register (PHMBASE_REG_0_0_0_VTDBAR)	0000000000000000h
78h	8	Protected High-Memory Limit Register (PHMLIMIT_REG_0_0_0_VTDBAR)	0000000000000000h
80h	8	Invalidation Queue Head Register (IQH_REG_0_0_0_VTDBAR)	0000000000000000h
88h	8	Invalidation Queue Tail Register (IQT_REG_0_0_0_VTDBAR)	0000000000000000h
90h	8	Invalidation Queue Address Register (IQA_REG_0_0_0_VTDBAR)	0000000000000000h
9Ch	4	Invalidation Completion Status Register (ICS_REG_0_0_0_VTDBAR)	00000000h
A0h	4	Invalidation Event Control Register (IECTL_REG_0_0_0_VTDBAR)	80000000h
A4h	4	Invalidation Event Data Register (IEDATA_REG_0_0_0_VTDBAR)	00000000h
A8h	4	Invalidation Event Address Register (IEADDR_REG_0_0_0_VTDBAR)	00000000h
ACh	4	Invalidation Event Upper Address Register (IEUADDR_REG_0_0_0_VTDBAR)	00000000h
B8h	8	Interrupt Remapping Table Address Register (IRTA_REG_0_0_0_VTDBAR)	0000000000000000h
C0h	8	Page Request Queue Head Register (PQH_REG_0_0_0_VTDBAR)	0000000000000000h
C8h	8	Page Request Queue Tail Register (PQT_REG_0_0_0_VTDBAR)	0000000000000000h
D0h	8	Page Request Queue Address Register (PQA_REG_0_0_0_VTDBAR)	0000000000000000h
DCh	4	Page Request Status Register (PRS_REG_0_0_0_VTDBAR)	00000000h
E0h	4	Page Request Event Control Register (PECTL_REG_0_0_0_VTDBAR)	80000000h
E4h	4	Page Request Event Data Register (PEDATA_REG_0_0_0_VTDBAR)	00000000h
E8h	4	Page Request Event Address Register (PEADDR_REG_0_0_0_VTDBAR)	00000000h

Table 3-9. Summary of VTDPVC0BAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
ECh	4	Page Request Event Upper Address Register (PEUADDR_REG_0_0_0_VTDBAR)	00000000h
100h	8	MTRR Capability Register (MTRRCAP_0_0_0_VTDBAR)	0000000000000000h
108h	8	MTRR Default Type Register (MTRRDEFAULT_0_0_0_VTDBAR)	0000000000000000h
120h	8	Fixed-Range MTRR Format 64K-00000 (MTRR_FIX64K_00000_REG_0_0_0_VTDBAR)	0000000000000000h
128h	8	Fixed-Range MTRR Format 16K-80000 (MTRR_FIX16K_80000_REG_0_0_0_VTDBAR)	0000000000000000h
130h	8	Fixed-Range MTRR Format 16K-A0000 (MTRR_FIX16K_A0000_REG_0_0_0_VTDBAR)	0000000000000000h
138h	8	Fixed-Range MTRR Format 4K-C0000 (MTRR_FIX4K_C0000_REG_0_0_0_VTDBAR)	0000000000000000h
140h	8	Fixed-Range MTRR Format 4K-C8000 (MTRR_FIX4K_C8000_REG_0_0_0_VTDBAR)	0000000000000000h
148h	8	Fixed-Range MTRR Format 4K-D0000 (MTRR_FIX4K_D0000_REG_0_0_0_VTDBAR)	0000000000000000h
150h	8	Fixed-Range MTRR Format 4K-D8000 (MTRR_FIX4K_D8000_REG_0_0_0_VTDBAR)	0000000000000000h
158h	8	Fixed-Range MTRR Format 4K-E0000 (MTRR_FIX4K_E0000_REG_0_0_0_VTDBAR)	0000000000000000h
160h	8	Fixed-Range MTRR Format 4K-E8000 (MTRR_FIX4K_E8000_REG_0_0_0_VTDBAR)	0000000000000000h
168h	8	Fixed-Range MTRR Format 4K-F0000 (MTRR_FIX4K_F0000_REG_0_0_0_VTDBAR)	0000000000000000h
170h	8	Fixed-Range MTRR Format 4K-F8000 (MTRR_FIX4K_F8000_REG_0_0_0_VTDBAR)	0000000000000000h
180h	8	Variable-Range MTRR Format Physical Base 0 (MTRR_PHYSBASE0_REG_0_0_0_VTDBAR)	0000000000000000h
188h	8	Variable-Range MTRR Format Physical Mask 0 (MTRR_PHYSMASK0_REG_0_0_0_VTDBAR)	0000000000000000h
190h	8	Variable-Range MTRR Format Physical Base 1 (MTRR_PHYSBASE1_REG_0_0_0_VTDBAR)	0000000000000000h
198h	8	Variable-Range MTRR Format Physical Mask 1 (MTRR_PHYSMASK1_REG_0_0_0_VTDBAR)	0000000000000000h
1A0h	8	Variable-Range MTRR Format Physical Base 2 (MTRR_PHYSBASE2_REG_0_0_0_VTDBAR)	0000000000000000h
1A8h	8	Variable-Range MTRR Format Physical Mask 2 (MTRR_PHYSMASK2_REG_0_0_0_VTDBAR)	0000000000000000h
1B0h	8	Variable-Range MTRR Format Physical Base 3 (MTRR_PHYSBASE3_REG_0_0_0_VTDBAR)	0000000000000000h
1B8h	8	Variable-Range MTRR Format Physical Mask 3 (MTRR_PHYSMASK3_REG_0_0_0_VTDBAR)	0000000000000000h
1C0h	8	Variable-Range MTRR Format Physical Base 4 (MTRR_PHYSBASE4_REG_0_0_0_VTDBAR)	0000000000000000h
1C8h	8	Variable-Range MTRR Format Physical Mask 4 (MTRR_PHYSMASK4_REG_0_0_0_VTDBAR)	0000000000000000h
1D0h	8	Variable-Range MTRR Format Physical Base 5 (MTRR_PHYSBASE5_REG_0_0_0_VTDBAR)	0000000000000000h

Table 3-9. Summary of VTDPVC0BAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1D8h	8	Variable-Range MTRR Format Physical Mask 5 (MTRR_PHYSMASK5_REG_0_0_0_VTDBAR)	0000000000000000h
1E0h	8	Variable-Range MTRR Format Physical Base 6 (MTRR_PHYSBASE6_REG_0_0_0_VTDBAR)	0000000000000000h
1E8h	8	Variable-Range MTRR Format Physical Mask 6 (MTRR_PHYSMASK6_REG_0_0_0_VTDBAR)	0000000000000000h
1F0h	8	Variable-Range MTRR Format Physical Base 7 (MTRR_PHYSBASE7_REG_0_0_0_VTDBAR)	0000000000000000h
1F8h	8	Variable-Range MTRR Format Physical Mask 7 (MTRR_PHYSMASK7_REG_0_0_0_VTDBAR)	0000000000000000h
200h	8	Variable-Range MTRR Format Physical Base 8 (MTRR_PHYSBASE8_REG_0_0_0_VTDBAR)	0000000000000000h
208h	8	Variable-Range MTRR Format Physical Mask 8 (MTRR_PHYSMASK8_REG_0_0_0_VTDBAR)	0000000000000000h
210h	8	Variable-Range MTRR Format Physical Base 9 (MTRR_PHYSBASE9_REG_0_0_0_VTDBAR)	0000000000000000h
218h	8	Variable-Range MTRR Format Physical Mask 9 (MTRR_PHYSMASK9_REG_0_0_0_VTDBAR)	0000000000000000h
400h	8	Fault Recording Register Low [0] (FRCDL_REG_0_0_0_VTDBAR)	0000000000000000h
408h	8	Fault Recording Register High [0] (FRCDH_REG_0_0_0_VTDBAR)	0000000000000000h
500h	8	Invalidate Address Register (IVA_REG_0_0_0_VTDBAR)	0000000000000000h
508h	8	IOTLB Invalidate Register (IOTLB_REG_0_0_0_VTDBAR)	0200000000000000h

3.8.2 Version Register (VER_REG_0_0_0_VTDBAR) — Offset 0h

Register to report the architecture version supported. Backward compatibility for the architecture is maintained with new revision numbers, allowing software to load remapping hardware drivers written for prior architecture versions.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + 0h	00000050h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:4	5h RO/V	**Major Version Number (MAJOR):** Indicates supported architecture version.

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RO/V	**Minor Version Number (MINOR):** Indicates supported architecture minor version.

3.8.3 Capability Register (CAP_REG_0_0_0_VTDBAR) — Offset 8h

Register to report general remapping hardware capabilities.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 8h	08D2008C40690462h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:61	0h RO	**Reserved**
60	0h RO/V	**First Level 5-level Paging (FL5LP):** • 0: Hardware does not support 5-level paging for requests-with-PASID subject to first-level translation. • 1: Hardware supports 5-level paging for requests-with-PASID subject to first-level translation.
59	1h RO/V	**Posted Interrupt Support (PI):** • 0 = Hardware does not support Posting of Interrupts. • 1 = Hardware supports Posting of Interrupts. Hardware implementations reporting this field as Set must also report Interrupt Remapping support (IR field in Extended Capability Register)
58:57	0h RO	**Reserved**
56	0h RO/V	**First Level 1-GByte Page Support (FL1GP):** A value of 1 in this field indicates 1-GByte page size is supported for first-level translation.
55	1h RO/V	**Read Draining (DRD):** • 0 = Hardware does not support draining of DMA read requests. • 1 = Hardware supports draining of DMA read requests.
54	1h RO/V	**Write Draining (DWD):** • 0 = Hardware does not support draining of DMA write requests. • 1 = Hardware supports draining of DMA write requests.
53:48	12h RO/V	**Maximum Address Mask Value (MAMV):** The value in this field indicates the maximum supported value for the Address Mask (AM) field in the Invalidation Address register (IVA_REG) and IOTLB Invalidation Descriptor (iotlb_inv_dsc) used for invalidations of second-level translation. This field is valid only when the PSI field in Capability register is reported as Set.

Bit Range	Default & Access	Field Name (ID): Description
47:40	00h RO/V	**Number of Fault-Recording Registers (NFR):** Number of fault recording registers is computed as N+1, where N is the value reported in this field. Implementations must support at least one fault recording register (NFR = 0) for each remapping hardware unit in the platform. The maximum number of fault recording registers per remapping hardware unit is 256.
39	1h RO/V	**Page Selective Invalidation (PSI):** • 0 = Hardware supports only domain and global invalidates for IOTLB. • 1 = Hardware supports page selective, domain and global invalidates for IOTLB. Hardware implementations reporting this field as set are recommended to support a Maximum Address Mask Value (MAMV) value of at least 9 (or 18 if supporting 1GB pages with second level translation).
38	0h RO	**Reserved**
37:34	3h RO/V	**Second Level Large Page Support (SLLPS):** This field indicates the super page sizes supported by hardware. A value of 1 in any of these bits indicates the corresponding super-page size is supported. The super-page sizes corresponding to various bit positions within this field are: • 0 = 21-bit offset to page frame (2MB) • 1 = 30-bit offset to page frame (1GB) • 2 = 39-bit offset to page frame (512GB) • 3 = 48-bit offset to page frame (1TB) Hardware implementations supporting a specific super-page size must support all smaller super-page sizes, i.e. only valid values for this field are 0000b, 0001b, 0011b, 0111b, 1111b.
33:24	040h RO/V	**Fault-Recording Register Offset (FRO):** This field specifies the location to the first fault recording register relative to the register base address of this remapping hardware unit. If the register base address is X, and the value reported in this field is Y, the address for the first fault recording register is calculated as X+(16*Y).
23	0h RO	**Reserved**
22	1h RO/V	**Zero Length Read (ZLR):** • 0 = Indicates the remapping hardware unit blocks (and treats as fault) zero length DMA read requests to write-only pages. • 1 = Indicates the remapping hardware unit supports zero length DMA read requests to write-only pages. DMA remapping hardware implementations are recommended to report ZLR field as Set.
21:16	29h RO/V	**Maximum Guest Address Width (MGAW):** This field indicates the maximum DMA virtual addressability supported by remapping hardware. The Maximum Guest Address Width (MGAW) is computed as (N+1), where N is the value reported in this field. For example, a hardware implementation supporting 48-bit MGAW reports a value of 47 (101111b) in this field. If the value in this field is X, untranslated and translated DMA requests to addresses above 2(x+1)-1 are always blocked by hardware. Translations requests to address above 2(x+1)-1 from allowed devices return a null Translation Completion Data Entry with R=W=0. Guest addressability for a given DMA request is limited to the minimum of the value reported through this field and the adjusted guest address width of the corresponding page-table structure. (Adjusted guest address widths supported by hardware are reported through the SAGAW field). Implementations are recommended to support MGAW at least equal to the physical addressability (host address width) of the platform.
15:13	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
12:8	04h RO/V	**Supported Adjusted Guest Address Widths (SAGAW):** This 5-bit field indicates the supported adjusted guest address widths (which in turn represents the levels of page-table walks for the 4KB base page size) supported by the hardware implementation. A value of 1 in any of these bits indicates the corresponding adjusted guest address width is supported. The adjusted guest address widths corresponding to various bit positions within this field are: • 0 = 30-bit AGAW (2-level page table) • 1 = 39-bit AGAW (3-level page table) • 2 = 48-bit AGAW (4-level page table) • 3 = 57-bit AGAW (5-level page table) • 4 = Reserved Software must ensure that the adjusted guest address width used to setup the page tables is one of the supported guest address widths reported in this field.
7	0h RO/V	**Caching Mode (CM):** • 0 = Not-present and erroneous entries are not cached in any of the renmapping caches. Invalidations are not required for modifications to individual not present or invalid entries. However, any modifications that result in decreasing the effective permissions or partial permission increases require invalidations for them to be effective. • 1 = Not-present and erroneous mappings may be cached in the remapping caches. Any software updates to the remapping structures (including updates to not-present or erroneous entries) require explicit invalidation. Hardware implementations of this architecture must support a value of 0 in this field.
6	1h RO/V	**Protected High-Memory Region (PHMR):** • 0 = Indicates protected high-memory region is not supported. • 1 = Indicates protected high-memory region is supported.
5	1h RO/V	**Protected Low-Memory Region (PLMR):** • 0 = Indicates protected low-memory region is not supported. • 1 = Indicates protected low-memory region is supported.
4	0h RO/V	**Required Write-Buffer Flushing (RWBF):** • 0 = Indicates no write-buffer flushing is needed to ensure changes to memory-resident structures are visible to hardware. • 1 = Indicates software must explicitly flush the write buffers to ensure updates made to memory-resident remapping structures are visible to hardware.
3	0h RO/V	**Advanced Fault Logging (AFL):** • 0 = Indicates advanced fault logging is not supported. Only primary fault logging is supported. • 1 = Indicates advanced fault logging is supported.
2:0	2h RO/V	**Number of Domains Supported (ND):** • 000b = Hardware supports 4-bit domain-ids with support for up to 16 domains. • 001b = Hardware supports 6-bit domain-ids with support for up to 64 domains. • 010b = Hardware supports 8-bit domain-ids with support for up to 256 domains. • 011b = Hardware supports 10-bit domain-ids with support for up to 1024 domains. • 100b = Hardware supports 12-bit domain-ids with support for up to 4K domains. • 100b = Hardware supports 14-bit domain-ids with support for up to 16K domains. • 110b = Hardware supports 16-bit domain-ids with support for up to 64K domains. • 111b = Reserved.

3.8.4 Extended Capability Register (ECAP_REG_0_0_0_VTDBAR) — Offset 10h

Register to report remapping hardware extended capabilities.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 10h	0000060000F050DAh

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:44	0h RO	**Reserved**
43	0h RO/V	**PASID Support Limitation (PSL):** This field is valid only when Process Address Space ID Support (PASID) field (bit 40) is reported as Set. When this field is reported as Set, extendedcontext-entries with PASID Enable (PASIDE) field Set do not support Requests-withoutPASID. Hardware implementations must report a value of 0 in this field. Virtual implementations may report a value of 1 in this field to disallow guest software from using an extended-context-entry for both Virtual Address (VA) and I/O Virtual Address (IOVA) concurrently.
42	1h RO/V	**Page Request Draining Support (PDS):** • 0 = Hardware does not support Page-Request Drain (PD) flag in Inv_wait_dsc. • 1 = Hardware supports Page-Request Drain (PD) flag in Inv_wait_dsc. This field is valid only when Device-TLB support field is reported as Set.
41	1h RO/V	**Device-TLB Invalidation Throttle (DIT):** • 0 = Hardware does not support Device-TLB Invalidation Throttling. • 1 = Hardware supports Device-TLB Invalidation Throttling. This field is valid only when Page Request Support (PRS) field is reported as Set.
40	0h RO/V	**Process Address Space ID Support (PASID):** • 0 = Hardware does not support requests tagged with Process Address Space IDs. • 1 = Hardware supports requests tagged with Process Address Space IDs.
39:35	00h RO/V	**PASID Size Supported (PSS):** This field reports the PASID size supported by the remapping hardware for requests-with-PASID. A value of N in this field indicates hardware supports PASID field of N+1 bits (For example, value of 7 in this field, indicates 8-bit PASIDs are supported). Requests-with-PASID with PASID value beyond the limit specified by this field are treated as error by the remapping hardware. This field is valid only when PASID field is reported as Set.
34	0h RO/V	**Extended Accessed Flag Support (EAFS):** • 0 = Hardware does not support the extended-accessed (EA) bit in first-level paging-structure entries. • 1 = Hardware supports the extended accessed (EA) bit in first-level paging-structure entries. This field is valid only when PASID field is reported as Set.
33	0h RO/V	**No Write Flag Support (NWFS):** • 0 = Hardware ignores the No Write (NW) flag in Device-TLB translationrequests, and behaves as if NW is always 0. • 1 = Hardware supports the No Write (NW) flag in Device-TLB translationrequests. This field is valid only when Device-TLB support (DT) field is reported as Set.

Bit Range	Default & Access	Field Name (ID): Description
32	0h RO	**Reserved**
31	0h RO/V	**Supervisor Request Support (SRS):** • 0 = H/W does not support requests-with-PASID seeking supervisor privilege. • 1 = H/W supports requests-with-PASID seeking supervisor privilege. The field is valid only when PASID field is reported as Set.
30	0h RO/V	**Execute Request Support (ERS):** • 0 = H/W does not support requests-with-PASID seeking execute permission. • 1 = H/W supports requests-with-PASID seeking execute permission. This field is valid only when PASID field is reported as Set.
29	0h RO/V	**Page Request Support (PRS):** • 0 = Hardware does not support Page Requests. • 1 = Hardware supports Page Requests This field is valid only when Device-TLB (DT) field is reported as Set.
28	0h RO/V	**Ignore ECAP (IGN):** Ignore this field
27	0h RO/V	**Deferred Invalidate Support (DIS):** • 0 = Hardware does not support deferred invalidations of IOTLB and Device-TLB. • 1 = Hardware supports deferred invalidations of IOTLB and Device-TLB. This field is valid only when PASID field is reported as Set.
26	0h RO/V	**Nested Translation Support (NEST):** • 0 = Hardware does not support nested translations. • 1 = Hardware supports nested translations. This field is valid only when PASID field is reported as Set.
25	0h RO/V	**Memory Type Support (MTS):** • 0 = Hardware does not support Memory Type in first-level translation and Extended Memory type in second-level translation. • 1 = Hardware supports Memory Type in first-level translation and Extended Memory type in second-level translation. This field is valid only when PASID and ECS fields are reported as Set. Remapping hardware units with, one or more devices that operate in processor coherency domain, under its scope must report this field as Set.
24	0h RO/V	**Extended Context Support (ECS):** • 0 = Hardware does not support extended-root-entries and extended-context-entries. • 1 = Hardware supports extended-root-entries and extended-context-entries. Implementations reporting PASID or PRS fields as Set, must report this field as Set.
23:20	Fh RO/V	**Maximum Handle Mask Value (MHMV):** The value in this field indicates the maximum supported value for the Handle Mask (HM) field in the interrupt entry cache invalidation descriptor (iec_inv_dsc). This field is valid only when the IR field in Extended Capability register is reported as Set.
19:18	0h RO	**Reserved**
17:8	050h RO/V	**IOTLB Register Offset (IRO):** This field specifies the offset to the IOTLB registers relative to the register base address of this remapping hardware unit. If the register base address is X, and the value reported in this field is Y, the address for the first IOTLB invalidation register is calculated as X+(16*Y).
7	1h RO/V	**Snoop Control (SC):** • 0 = Hardware does not support 1-setting of the SNP field in the page-table entries. • 1 = Hardware supports the 1-setting of the SNP field in the page-table entries.

Bit Range	Default & Access	Field Name (ID): Description
6	1h RO/V	**Pass Through (PT):** • 0 = Hardware does not support pass-through translation type in context entries and extended-context-entries. • 1 = Hardware supports pass-through translation type in context entries and extended-context-entries. Pass-through translation is specified through Translation-Type (T) field value of 10b in context-entries, or T field value of 010b in extended-context-entries. Hardware implementations supporting PASID must report a value of 1b in this field.
5	0h RO	**Reserved**
4	1h RO/V	**Extended Interrupt Mode (EIM):** • 0 = On Intel64 platforms, hardware supports only 8-bit APIC-IDs (xAPIC mode). • 1 = On Intel64 platforms, hardware supports 32-bit APIC-IDs (x2APIC mode). This field is valid only on Intel64 platforms reporting Interrupt Remapping support (IR field Set).
3	1h RO/V	**Interrupt Remapping Suport (IR):** • 0 = Hardware does not support interrupt remapping. • 1 = Hardware supports interrupt remapping. Implementations reporting this field as Set must also support Queued Invalidation (QI).
2	0h RO/V	**Device-TLB Support (DT):** • 0 = Hardware does not support device-IOTLBs. • 1 = Hardware supports Device-IOTLBs. Implementations reporting this field as Set must also support Queued Invalidation (QI). Hardware implementations supporting I/O Page Requests (PRS field Set in Extended Capability register) must report a value of 1b in this field.
1	1h RO/V	**Queued Invalidation Support (QI):** • 0 = Hardware does not support queued invalidations. • 1 = Hardware supports queued invalidations.
0	0h RO/V	**Page-Walk Coherency (C):** This field indicates if hardware access to the root, context, extended-context and interrupt-remap tables, and second-level paging structures for requests-without-PASID, are coherent (snooped) or not. • 0 = Indicates hardware accesses to remapping structures are non-coherent. • 1 = Indicates hardware accesses to remapping structures are coherent. Hardware access to advanced fault log, invalidation queue, invalidation semaphore, page-request queue, PASID-table, PASID-state table, and first-level page-tables are always coherent.

3.8.5 Global Command Register (GCMD_REG_0_0_0_VTDBAR) — Offset 18h

Register to control remapping hardware. If multiple control fields in this register need to be modified, software must serialize the modifications through multiple writes to this register

Register to control r mapping hardware. If multiple control fields in this register need to be modified, software must serialize the modifications through multiple writes to this register

- 1. Tmp = Read GSTS_REG
- 2. Status = (Tmp & 96FFFFFFh) // Reset the one-shot bits
- 3. Command = (Status | (Y << X))
- 4. Write Command to GCMD_REG
- 5. Wait until GSTS_REG[X] indicates command is serviced.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + 18h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h WO	**Translation Enable (TE):** Software writes to this field to request hardware to enable/disable DMA-remapping: • 0 = Disable DMA remapping. • 1 = Enable DMA remapping. Hardware reports the status of the translation enable operation through the TES field in the Global Status register. There may be active DMA requests in the platform when software updates this field. Hardware must enable or disable remapping logic only at determinstic transaction boundaries, so that any in-flight transaction is either subject to remapping or not at all. Hardware implementations supporting DMA draining must drain any in-flight DMA read/write requests queued within the Root-Complex before completing the translation enable command and reflecting the status of the command through the TES field in the Global Status register. The value returned on a read of this field is undefined.
30	0h WO	**Set Root Table Pointer (SRTP):** Software sets this field to set/update the root-entry table pointer used by hardware. The root-entry table pointer is specified through the Root-entry Table Address (RTA_REG) register. Hardware reports the status of the Set Root Table Pointer operation through the RTPS field in the Global Status register. The Set Root Table Pointer operation must be performed before enabling or re-enabling (after disabling) DMA remapping through the TE field. .After a Set Root Table Pointer operation, software must globally invalidate the context cache and then globally invalidate of IOTLB. This is required to ensure hardware uses only the remapping structures referenced by the new root table pointer, and not stale cached entries. While DMA remapping hardware is active, software may update the root table pointer through this field. However, to ensure valid in-flight DMA requests are deterministically remapped, software must ensure that the structures referenced by the new root table pointer are programmed to provide the same remapping results as the structures referenced by the previous root-table pointer. Clearing this bit has no effect. The value returned on read of this field is undefined.
29	0h RO	**Set Fault Log (SFL):** This field is valid only for implementations supporting advanced fault logging. Software sets this field to request hardware to set/update the fault-log pointer used by hardware. The fault-log pointer is specified through Advanced Fault Log register. Hardware reports the status of the Set Fault Log operation through the FLS field in the Global Status register. The fault log pointer must be set before enabling advanced fault logging (through EAFL field). Once advanced fault logging is enabled, the fault log pointer may be updated through this field while DMA remapping is active. Clearing this bit has no effect. The value returned on read of this field is undefined.

Bit Range	Default & Access	Field Name (ID): Description
28	0h RO	**Enable Advanced Fault Logging (EAFL):** This field is valid only for implementations supporting advanced fault logging. Software writes to this field to request hardware to enable or disable advanced fault logging: • 0 = Disable advanced fault logging. In this case, translation faults are reported through the Fault Recording registers. • 1 = Enable use of memory-resident fault log. When enabled, translation faults are recorded in the memory-resident log. The fault log pointer must be set in hardware (through the SFL field) before enabling advaned fault logging. Hardware reports the status of the advaned fault logging enable operation through the AFLS field in the Global Status register. The value returned on read of this field is undefined.
27	0h RO	**Write Buffer Flush (WBF):** This bit is valid only for implementations requiring write buffer flushing. Software sets this field to request that hardware flush the Root-Complex internal write buffers. This is done to ensure any updates to the memory-resident remapping structures are not held in any internal write posting buffers. Hardware reports the status of the write buffer flushing operation through the WBFS field in the Global Status register. Clearing this bit has no effect. The value returned on a read of this field is undefined.
26	0h WO	**Queued Invalidation Enable (QIE):** This field is valid only for implementations supporting queued invalidations. Software writes to this field to enable or disable queued invalidations. • 0 = Disable queued invalidations. • 1 = Enable use of queued invalidations. Hardware reports the status of queued invalidation enable operation through QIES field in the Global Status register. The value returned on a read of this field is undefined.
25	0h WO	**Interrupt Remapping Enable (IRE):** This field is valid only for implementations supporting interrupt remapping. • 0 = Disable interrupt-remapping hardware. • 1 = Enable interrupt-remapping hardware. Hardware reports the status of the interrupt remapping enable operation through the IRES field in the Global Status register. There may be active interrupt requests in the platform when software updates this field. Hardware must enable or disable interrupt-remapping logic only at deterministic transaction boundaries, so that any in-flight interrupts are either subject to remapping or not at all. Hardware implementations must drain any in-flight interrupts requests queued in the Root-Complex before completing the interrupt-remapping enable command and reflecting the status of the command through the IRES field in the Global Status register. The value returned on a read of this field is undefined.

Bit Range	Default & Access	Field Name (ID): Description
24	0h WO	**Set Interrupt Remap Table Pointer (SIRTP):** This field is valid only for implementations supporting interrupt-remapping. Software sets this field to set/update the interrupt remapping table pointer used by hardware. The interrupt remapping table pointer is specified through the Interrupt Remapping Table Address (IRTA_REG) register. Hardware reports the status of the Set Interrupt Remap Table Pointer operation through the IRTPS field in the Global Status register. The Set Interrupt Remap Table Pointer operation must be performed before enabling or re-enabling (after disabling) interrupt-remapping hardware through the IRE field. After a Set Interrupt Remap Table Pointer operation, software must globally invalidate the interrupt entry cache. This is required to ensure hardware uses only the interrupt-remapping entries referenced by the new interrupt remap table pointer, and not any stale cached entries. While interrupt remapping is active, software may update the interrupt remapping table pointer through this field. However, to ensure valid in-flight interrupt requests are deterministically remapped, software must ensure that the structures referenced by the new interrupt remap table pointer are programmed to provide the same remapping results as the structures referenced by the previous interrupt remap table pointer. Clearing this bit has no effect. The value returned on a read of this field is undefined.
23	0h WO	**Compatibility Format Interrupt (CFI):** This field is valid only for Intel64 implementations supporting interrupt-remapping. Software writes to this field to enable or disable Compatibility Format interrupts on Intel64 platforms. The value in this field is effective only when interrupt-remapping is enabled and Extended Interrupt Mode (x2APIC mode) is not enabled. • 0 = Block Compatibility format interrupts. • 1 = Process Compatibility format interrupts as pass-through (bypass interrupt remapping). Hardware reports the status of updating this field through the CFIS field in the Global Status register. The value returned on a read of this field is undefined.
22:0	0h RO	**Reserved**

3.8.6 Global Status Register (GSTS_REG_0_0_0_VTDBAR) — Offset 1Ch

Register to report general remapping hardware status.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + 1Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Translation Enable Status (TES):** This field indicates the status of DMA-remapping hardware. • 0 = DMA-remapping hardware is not enabled. • 1 = DMA-remapping hardware is enabled

Bit Range	Default & Access	Field Name (ID): Description
30	0h RO/V	**Root Table Pointer Status (RTPS):** This field indicates the status of the root- table pointer in hardware. This field is cleared by hardware when software sets the SRTP field in the Global Command register. This field is set by hardware when hardware completes the Set Root Table Pointer operation using the value provided in the Root-Entry Table Address register.
29	0h RO	**Fault Log Status (FLS):** This field: • Is cleared by hardware when software Sets the SFL field in the Global Command register. • Is Set by hardware whn hardware completes the Set Fault Log Pointer operation using the value provided in the Advanced Fault Log register.
28	0h RO	**Adavanced Fault Logging Status (AFLS):** This field is valid only for implementations supporting advanced fault logging. It indicates the advanced fault logging status: • 0 = Advanced Fault Logging is not enabled. • 1 = Advanced Fault Logging is enabled.
27	0h RO	**Write Buffer Flush Status (WBFS):** This field is valid only for implementations requiring write buffer flushing. This field indicates the status of the write buffer flush command. It is: • Set by hardware when software sets the WBF field in the Global Command register. • Cleared by hardware when hardware completes the write buffer flushing operation.
26	0h RO/V	**Queued Invalidation Enable Status (QIES):** This field indicates queued invalidation enable status. • 0 = queued invalidation is not enabled. • 1 = queued invalidation is enabled
25	0h RO/V	**Interrupt Remapping Enable Status (IRES):** This field indicates the status of Interrupt-remapping hardware. • 0 = Interrupt-remapping hardware is not enabled. • 1 = Interrupt-remapping hardware is enabled
24	0h RO/V	**Interrupt Remapping Pointer Status (IRTPS):** This field indicates the status of the interrupt remapping table pointer in hardware. This field is cleared by hardware when software sets the SIRTP field in the Global Command register. This field is Set by hardware when hardware completes the set interrupt remap table pointer operation using the value provided in the Interrupt Remapping Table Address register.
23	0h RO/V	**Compatibility Format Interrupt Status (CFIS):** This field indicates the status of Compatibility format interrupts on Intel64 implementations supporting interrupt-remapping. The value reported in this field is applicable only when interrupt-remapping is enabled and Extended Interrupt Mode (x2APIC mode) is not enabled. • 0 = Compatibility format interrupts are blocked. • 1 = Compatibility format interrupts are processed as pass-through (bypassing interrupt remapping).
22:0	0h RO	**Reserved**

3.8.7 Root Table Address Register (RTADDR_REG_0_0_0_VTDBAR) — Offset 20h

Register providing the base address of root-entry table.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 20h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:52	0h RO	**Reserved**
51:12	0000000000h RW	**Root Table Address (RTA):** This register points to base of page aligned, 4KB-sized root-entry table in system memory. Hardware ignores and not implements bits 63:HAW, where HAW is the host address width. Software specifies the base address of the root-entry table through this register, and programs it in hardware through the SRTP field in the Global Command register. Reads of this register returns value that was last programmed to it.
11	0h RW/V	**Root Table Type (RTT):** This field specifies the type of root-table referenced by the Root Table Address (RTA) field: • 0 = Root Table. • 1 = Extended Root Table
10:0	0h RO	**Reserved**

3.8.8 Context Command Register (CCMD_REG_0_0_0_VTDBAR) — Offset 28h

Register to manage context cache. The act of writing the uppermost byte of the CCMD_REG with the ICC field Set causes the hardware to perform the context-cache invalidation.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 28h	0800000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/V	**Invalidate Context Cache (ICC):** Software requests invalidation of context-cache by setting this field. Software must also set the requested invalidation granularity by programming the CIRG field. Software must read back and check the ICC field is Clear to confirm the invalidation is complete. Software must not update this register when this field is set. Hardware clears the ICC field to indicate the invalidation request is complete. Hardware also indicates the granularity at which the invalidation operation was performed through the CAIG field. Software must submit a context-cache invalidation request through this field only when there are no invalidation requests pending at this remapping hardware unit. Since information from the context-cache may be used by hardware to tag IOTLB entries, software must perform domain-selective (or global) invalidation of IOTLB after the context cache invalidation has completed. Hardware implementations reporting write-buffer flushing requirement (RWBF=1 in Capability register) must implicitly perform a write buffer flush before invalidating the context cache.
62:61	0h RW	**Context Invalidation Request Granularity (CIRG):** Software provides the requested invalidation granularity through this field when setting the ICC field: • 00: Reserved. • 01: Global Invalidation request. • 10: Domain-selective invalidation request. The target domain-id must be specified in the DID field. • 11: Device-selective invalidation request. The target source-id(s) must be specified through the SID and FM fields, and the domain-id (that was programmed in the context-entry for these device(s)) must be provided in the DID field. Hardware implementations may process an invalidation request by performing invalidation at a coarser granularity than requested. Hardware indicates completion of the invalidation request by clearing the ICC field. At this time, hardware also indicates the granularity at which the actual invalidation was performed through the CAIG field.

Bit Range	Default & Access	Field Name (ID): Description
60:59	1h RO/V	**Context Actual Invalidation Granularity (CAIG):** Hardware reports the granularity at which an invalidation request was processed through the CAIG field at the time of reporting invalidation completion (by clearing the ICC field). The following are the encodings for this field: • 00: Reserved. • 01: Global Invalidation performed. This could be in response to a global, domain-selective or device-selective invalidation request. • 10: Domain-selective invalidation performed using the domain-id specified by software in the DID field. This could be in response to a domain-selective or device-selective invalidation request. • 11: Device-selective invalidation performed using the source-id and domain-id specified by software in the SID and FM fields. This can only be in response to a device-selective invalidation request.
58:34	0h RO	**Reserved**
33:32	0h WO	**Function Mask (FM):** Software may use the Function Mask to perform device-selective invalidations on behalf of devices supporting PCI Express Phantom Functions...This field specifies which bits of the function number portion (least significant three bits) of the SID field to mask when performing device-selective invalidations. The following encodings are defined for this field: • 00: No bits in the SID field masked. • 01: Mask most significant bit of function number in the SID field. • 10: Mask two most significant bit of function number in the SID field. • 11: Mask all three bits of function number in the SID field. The context-entries corresponding to all the source-ids specified through the FM and SID fields must have to the domain-id specified in the DID field.
31:16	0000h WO	**Source ID (SID):** Indicates the source-id of the device whose corresponding context-entry needs to be selectively invalidated. This field along with the FM field must be programmed by software for device-selective invalidation requests.
15:0	0000h RW	**Domain ID (DID):** Indicates the id of the domain whose context-entries need to be selectively invalidated. This field must be programmed by software for both domain-selective and device-selective invalidation requests. The Capability register reports the domain-id width supported by hardware. Software must ensure that the value written to this field is within this limit. Hardware may ignore and not implement bits15:N, where N is the supported domain-id width reported in the Capability register.

3.8.9 Fault Status Register (FSTS_REG_0_0_0_VTDBAR) — Offset 34h

Register indicating the various error status.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + 34h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RO/V	**Fault Record Index (FRI):** This field is valid only when the PPF field is Set. The FRI field indicates the index (from base) of the fault recording register to which the first pending fault was recorded when the PPF field was Set by hardware. The value read from this field is undefined when the PPF field is clear.
7	0h RW/1C/V/P	**Page Request Overflow (PRO):** Hardware detected a Page Request Overflow error. Hardware implementations not supporting the Page Request Queue implement this bit as RsvdZ.
6	0h RW/1C/V/P	**Invalidation Time-out Error (ITE):** Hardware detected a Device-IOTLB invalidation completion time-out. At this time, a fault event may be generated based on the programming of the Fault Event Control register. Hardware implementations not supporting device Device-IOTLBs implement this bit as RsvdZ.
5	0h RW/1C/V/P	**Invalidation Completion Error (ICE):** Hardware received an unexpected or invalid Device-IOTLB invalidation completion. This could be due to either an invalid ITag or invalid source-id in an invalidation completion response. At this time, a fault event may be generated based on the programming of hte Fault Event Control register. Hardware implementations not supporting Device-IOTLBs implement this bit as RsvdZ.
4	0h RW/1C/V/P	**Invalidation Queue Error (IQE):** Hardware detected an error associated with the invalidation queue. This could be due to either a hardware error while fetching a descriptor from the invalidation queue, or hardware detecting an erroneous or invalid descriptor in the invalidation queue. At this time, a fault event may be generated based on the programming of the Fault Event Control register. Hardware implementations not supporting queued invalidations implement this bit as RsvdZ.
3	0h RO/V	**Advanced Pending Fault (APF):** When this field is Clear, hardware sets this field when the first fault record (at index 0) is written to a fault log. At this time, a fault event is generated based on the programming of the Fault Event Control register. Software writing 1 to this field clears it. Hardware implementations not supporting advanced fault logging implement this bit as RsvdZ.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO/V	**Advanced Fault Overflow (AFO):** Hardware sets this field to indicate advanced fault log overflow condition. At this time, a fault event is generated based on the programming of the Fault Event Control register. Software writing 1 to this field clears it. Hardware implementations not supporting advanced fault logging implement this bit as RsvdZ.
1	0h RO/V/P	**Primary Pending Fault (PPF):** This field indicates if there are one or more pending faults logged in the fault recording registers. Hardware computes this field as the logical OR of Fault (F) fields across all the fault recording registers of this remapping hardware unit. • 0 = No pending faults in any of the fault recording registers. • 1 = One or more fault recording registers has pending faults. The FRI field is updated by hardware whenever the PPF field is set by hardware. Also, depending on the programming of Fault Event Control register, a fault event is generated when hardware sets this field.
0	0h RW/1C/V/P	**Primary Fault Overflow (PFO):** Hardware sets this field to indicate overflow of fault recording registers. Software writing 1 clears this field. When this field is Set, hardware does not record any new faults until software clears this field.

3.8.10 Fault Event Control Register (FECTL_REG_0_0_0_VTDBAR) — Offset 38h

Register specifying the fault event interrupt message control bits.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + 38h	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**Interrupt Mask (IM):** • 0 = No masking of interrupt. When an interrupt condition is detected, hardware issues an interrupt message (using the Fault Event Data and Fault Event Address register values). • 1 = This is the value on reset. Software may mask interrupt message generation by setting this field. Hardware is prohibited from sending the interrupt message when this field is set.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RO/V	**Interrupt Pending (IP):** Hardware sets the IP field whenever it detects an interrupt condition, which is defined as: • When primary fault logging is active, an interrupt condition occurs when hardware records a fault through one of the Fault Recording registers and sets the PPF field in Fault Status register. • When advanced fault logging is active, an interrupt condition occurs when hardware records a fault in the first fault record (at index 0) of the current fault log and sets the APF field in the Fault Status register. • Hardware detected error associated with the Invalidation Queue, setting the IQE field in the Fault Status register. • Hardware detected invalid Device-IOTLB invalidation completion, setting the ICE field in the Fault Status register. • Hardware detected Device-IOTLB invalidation completion time-out, setting the ITE field in the Fault Status register. If any of the status fields in the Fault Status register was already Set at the time of setting any of these fields, it is not treated as a new interrupt condition. The IP field is kept set by hardware while the interrupt message is held pending. The interrupt message could be held pending due to interrupt mask (IM field) being Set or other transient hardware conditions. The IP field is cleared by hardware as soon as the interrupt message pending condition is serviced. This could be due to either: • Hardware issuing the interrupt message due to either change in the transient hardware condition that caused interrupt message to be held pending, or due to software clearing the IM field. • Software servicing all the pending interrupt status fields in the Fault Status register as follows: — When primary fault logging is active, software clearing the Fault (F) field in all the Fault Recording registers with faults, causing the PPF field in Fault Status register to be evaluated as clear. — Software clearing other status fields in the Fault Status register by writing back the value read from the respective fields.
29:0	0h RO	**Reserved**

3.8.11 Fault Event Data Register (FEDATA_REG_0_0_0_VTDBAR) — Offset 3Ch

Register specifying the interrupt message data

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + 3Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Extended Interrupt Message Data (EIMD):** This field is valid only for implementations supporting 32-bit interrupt data fields. Hardware implementations supporting only 16-bit interrupt data may treat this field as RsvdZ.
15:0	0000h RW	**Interrupt Message Data (IMD):** Data value in the interrupt request.

3.8.12 Fault Event Address Register (FEADDR_REG_0_0_0_VTDBAR) — Offset 40h

Register specifying the interrupt message address.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + 40h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**Message Address (MA):** When fault events are enabled, the contents of this register specify the DWORD-aligned address (bits 31:2) for the interrupt request.
1:0	0h RO	**Reserved**

3.8.13 Fault Event Upper Address Register (FEUADDR_REG_0_0_0_VTDBAR) — Offset 44h

Register specifying the interrupt message upper address.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + 44h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Message Upper Address (MUA):** Hardware implementations supporting Extended Interrupt Mode are required to implement this register. Hardware implementations not supporting Extended Interrupt Mode may treat this field as RsvdZ.

3.8.14 Advanced Fault Log Register (AFLOG_REG_0_0_0_VTDBAR) — Offset 58h

Register to specify the base address of the memory-resident fault-log region. This register is treated as RsvdZ for implementations not supporting advanced translation fault logging (AFL field reported as 0 in the Capability register).

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 58h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:12	0000000000000h RO	**Fault Log Address (FLA):** This field specifies the base of 4KB aligned fault-log region in system memory. Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width. Software specifies the base address and size of the fault log region through this register, and programs it in hardware through the SFL field in the Global Command register. When implemented, reads of this field return the value that was last programmed to it.
11:9	0h RO	**Fault Log Size (FLS):** This field specifies the size of the fault log region pointed by the FLA field. The size of the fault log region is 2X * 4KB, where X is the value programmed in this register. When implemented, reads of this field return the value that was last programmed to it.
8:0	0h RO	**Reserved**

3.8.15 Protected Memory Enable Register (PMEN_REG_0_0_0_VTDBAR) — Offset 64h

Register to enable the DMA-protected memory regions setup through the PLMBASE,..PLMLIMT, PHMBASE, PHMLIMIT registers. This register is always treated as RO for implementations not supporting protected memory regions (PLMR and PHMR fields reported as Clear in the Capability register).

Protected memory regions may be used by software to securely initialize remapping structures in memory. To avoid impact to legacy BIOS usage of memory, software is recommended to not overlap protected memory regions with any reserved memory regions of the platform reported through the Reserved Memory Region Reporting (RMRR) structures.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + 64h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Protected Memory (EPM):** This field controls DMA accesses to the protected low-memory and protected high-memory regions. • 0 = Protected memory regions are disabled. • 1 = Protected memory regions are enabled.DMA requests accessing protected memory regions are handled as follows: — When DMA remapping is not enabled, all DMA requests accessing protected memory regions are blocked. — When DMA remapping is enabled: — DMA requests processed as pass-through (Translation Type value of 10b in Context-Entry) and accessing the protected memory regions are blocked. — DMA requests with translated address (AT=10b) and accessing the protected memory regions are blocked. — DMA requests that are subject to address remapping, and accessing the protected memory regions may or may not be blocked by hardware. For such requests, software must not depend on hardware protection of the protected memory regions, and instead program the DMA-remapping page-tables to not allow DMA to protected memory regions. Remapping hardware access to the remapping structures are not subject to protected memory region checks. DMA requests blocked due to protected memory region violation are not recorded or reported as remapping faults. Hardware reports the status of the protected memory enable/disable operation through the PRS field in this register.Hardware implementations supporting DMA draining must drain any in-flight translated DMA requests queued within the Root-Complex before indicating the protected memory region as enabled through the PRS field. After writing to this field software must wait for the operation to be completed and reflected in the PRS status field (bit 0) before changing the value of this field again.
30:1	0h RO	**Reserved**
0	0h RO/V	**Protected Region Status (PRS):** This field indicates the status of protected memory region(s): • 0 = Protected memory region(s) disabled. • 1 = Protected memory region(s) enabled.

3.8.16 Protected Low Memory Base Register (PLMBASE_REG_0_0_0_VTDBAR) — Offset 68h

Register to set up the base address of DMA-protected low-memory region below 4GB. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled.

This register is always treated as RO for implementations not supporting protected low memory region (PLMR field reported as Clear in the Capability register).

The alignment of the protected low memory region base depends on the number of reserved bits (N:0) of this register. Software may determine N by writing all 1s to this register, and finding the most significant zero bit position with 0 in the value read back from the register. Bits N:0 of this register is decoded by hardware as all 0s...Software must setup the protected low memory region below 4GB.

Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + 68h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW	**Protected Low-Memory Base (PLMB):** This register specifies the base of protected low-memory region in system memory.
19:0	0h RO	**Reserved**

3.8.17 Protected Low-Memory Limit Register (PLMLIMIT_REG_0_0_0_VTDBAR) — Offset 6Ch

Register to set up the limit address of DMA-protected low-memory region below 4GB. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled

This register is always treated as RO for implementations not supporting protected low memory region (PLMR field reported as Clear in the Capability register)

The alignment of the protected low memory region limit depends on the number of reserved bits (N:0) of this register. Software may determine N by writing all 1s to this register, and finding most significant zero bit position with 0 in the value read back from the register. Bits N:0 of the limit register is decoded by hardware as all 1s

The Protected low-memory base and limit registers functions as follows:

- Programming the protected low-memory base and limit registers with the same value in bits 31: (N+1) specifies a protected low-memory region of size 2(N+1) bytes

- Programming the protected low-memory limit register with a value less than the protected low-memory base register disables the protected low-memory region

Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + 6Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW	**Protected Low-Memory Limit (PLML):** This register specifies the last host physical address of the DMA-protected low-memory region in system memory.
19:0	0h RO	**Reserved**

3.8.18 Protected High-Memory Base Register (PHMBASE_REG_0_0_0_VTDBAR) — Offset 70h

Register to set up the base address of DMA-protected high-memory region. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled

This register is always treated as RO for implementations not supporting protected high memory region (PHMR field reported as Clear in the Capability register)

The alignment of the protected high memory region base depends on the number of reserved bits (N:0) of this register. Software may determine N by writing all 1s to this register, and finding most significant zero bit position below host address width (HAW) in the value read back from the register. Bits N:0 of this register are decoded by hardware as all 0s

Software may setup the protected high memory region either above or below 4GB

Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 70h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RO	**Reserved**
41:20	000000h RW	**Protected High-Memory Base (PHMB):** This register specifies the base of protected (high) memory region in system memory Hardware ignores, and does not implement, bits 63:HAW, where HAW is the host address width.
19:0	0h RO	**Reserved**

3.8.19 Protected High-Memory Limit Register (PHMLIMIT_REG_0_0_0_VTDBAR) — Offset 78h

Register to set up the limit address of DMA-protected high-memory region. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled

This register is always treated as RO for implementations not supporting protected high memory region (PHMR field reported as Clear in the Capability register)

The alignment of the protected high memory region limit depends on the number of reserved bits (N:0) of this register. Software may determine the value of N by writing all 1s to this register, and finding most significant zero bit position below host address width (HAW) in the value read back from the register. Bits N:0 of the limit register is decoded by hardware as all 1s

The protected high-memory base & limit registers functions as follows

- Programming the protected low-memory base and limit registers with the same value in bits HAW:(N+1) specifies a protected low-memory region of size 2(N+1) bytes
- Programming the protected high-memory limit register with a value less than the protected high-memory base register disables the protected high-memory region

Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 78h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RO	**Reserved**
41:20	000000h RW	**Protected High-Memory Limit (PHML):** This register specifies the last host physical address of the DMA-protected high-memory region in system memory Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width.
19:0	0h RO	**Reserved**

3.8.20 Invalidation Queue Head Register (IQH_REG_0_0_0_VTDBAR) — Offset 80h

Register indicating the invalidation queue head. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 80h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:19	0h RO	**Reserved**
18:4	0000h RO/V	**Queue Head (QH):** Specifies the offset (128-bit aligned) to the invalidation queue for the command that will be fetched next by hardware Hardware resets this field to 0 whenever the queued invalidation is disabled (QIES field Clear in the Global Status register).
3:0	0h RO	**Reserved**

3.8.21 Invalidation Queue Tail Register (IQT_REG_0_0_0_VTDBAR) — Offset 88h

Register indicating the invalidation tail head. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 88h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:19	0h RO	**Reserved**
18:4	0000h RW	**Queue Tail (QT):** Specifies the offset (128-bit aligned) to the invalidation queue for the command that will be written next by software.

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RO	**Reserved**

3.8.22 Invalidation Queue Address Register (IQA_REG_0_0_0_VTDBAR) — Offset 90h

Register to configure the base address and size of the invalidation queue. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 90h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	00000000 0h RW	**Invalidation Queue Base Address (IQA):** This field points to the base of 4KB aligned invalidation request queue. Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width Reads of this field return the value that was last programmed to it.
11:3	0h RO	**Reserved**
2:0	0h RW	**Queue Size (QS):** This field specifies the size of the invalidation request queue. A value of X in this field indicates an invalidation request queue of (2^X) 4KB pages. The number of entries in the invalidation queue is 2^(X + 8).

3.8.23 Invalidation Completion Status Register (ICS_REG_0_0_0_VTDBAR) — Offset 9Ch

Register to report completion status of invalidation wait descriptor with Interrupt Flag (IF) Set

This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + 9Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/1C/V/P	**Invalidation Wait Descriptor Complete (IWC):** Indicates completion of Invalidation Wait Descriptor with Interrupt Flag (IF) field Set. Hardware implementations not supporting queued invalidations implement this field as RsvdZ.

3.8.24 Invalidation Event Control Register (IECTL_REG_0_0_0_VTDBAR) — Offset A0h

Register specifying the invalidation event interrupt control bits

This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + A0h	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**Interrupt Mask (IM):** • 0= No masking of interrupt. When a invalidation event condition is detected, hardware issues an interrupt message (using the Invalidation Event Data & Invalidation Event Address register values) • 1= This is the value on reset. Software may mask interrupt message generation by setting this field. Hardware is prohibited from sending the interrupt message when this field is Set.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RO/V	**Interrupt Pending (IP):** Hardware sets the IP field whenever it detects an interrupt condition. Interrupt condition is defined as: • An Invalidation Wait Descriptor with Interrupt Flag (IF) field Set completed, setting the IWC field in the Invalidation Completion Status register • If the IWC field in the Invalidation Completion Status register was already Set at the time of setting this field, it is not treated as a new interrupt condition The IP field is kept Set by hardware while the interrupt message is held pending. The interrupt message could be held pending due to interrupt mask (IM field) being Set, or due to other transient hardware conditions. The IP field is cleared by hardware as soon as the interrupt message pending condition is serviced. This could be due to either: • 0= Hardware issuing the interrupt message due to either change in the transient hardware condition that caused interrupt message to be held pending or due to software clearing the IM field • 1= Software servicing the IWC field in the Invalidation Completion Status register.
29:0	0h RO	**Reserved**

3.8.25 Invalidation Event Data Register (IEDATA_REG_0_0_0_VTDBAR) — Offset A4h

Register specifying the Invalidation Event interrupt message data

This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Extended Interrupt Message Data (EIMD):** This field is valid only for implementations supporting 32-bit interrupt data fields Hardware implementations supporting only 16-bit interrupt data treat this field as Rsvd.
15:0	0000h RW	**Interrupt Message Data (IMD):** Data value in the interrupt request.

3.8.26 Invalidation Event Address Register (IEADDR_REG_0_0_0_VTDBAR) — Offset A8h

Register specifying the Invalidation Event Interrupt message address

This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Note: **NOTE:** Bit definitions are the same as FEADDR_REG_0_0_0_VTDBAR, offset 40h.

3.8.27 Invalidation Event Upper Address Register (IEUADDR_REG_0_0_0_VTDBAR) — Offset ACh

Register specifying the Invalidation Event interrupt message upper address.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Message Upper Address (MUA):** Hardware implementations supporting Queued Invalidations and Extended Interrupt Mode are required to implement this register Hardware implementations not supporting Queued Invalidations or Extended Interrupt Mode may treat this field as RsvdZ.

3.8.28 Interrupt Remapping Table Address Register (IRTA_REG_0_0_0_VTDBAR) — Offset B8h

Register providing the base address of Interrupt remapping table. This register is treated as RsvdZ by implementations reporting Interrupt Remapping (IR) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + B8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:52	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
51:12	0000000000h RW/V	**Interrupt Remapping Table Address (IRTA):** This field points to the base of 4KB aligned interrupt remapping table Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width Reads of this field returns value that was last programmed to it.
11	0h RW/V	**Extended Interrupt Mode Enable (EIME):** This field is used by hardware on Intel64 platforms as follows: • 0=xAPIC mode is active. Hardware interprets only low 8-bits of Destination-ID field in the IRTEs. The high 24-bits of the Destination-ID field are treated as reserved • 1= x2APIC mode is active. Hardware interprets all 32-bits of Destination-ID field in the IRTEs This field is implemented as RsvdZ on implementations reporting Extended Interrupt Mode (EIM) field as Clear in Extended Capability register.
10:4	0h RO	**Reserved**
3:0	0h RW/V	**Size IRTA (S):** This field specifies the size of the interrupt remapping table. The number of entries in the interrupt remapping table is 2(X+1), where X is the value programmed in this field.

3.8.29 Page Request Queue Head Register (PQH_REG_0_0_0_VTDBAR) — Offset C0h

Register indicating the page request queue head. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + C0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:19	0h RO	**Reserved**
18:4	0000h RO	**Page Queue Head (PQH):** Specifies the offset (16-bytes aligned) to the page request queue for the request that will be processed next by software.
3:0	0h RO	**Reserved**

3.8.30 Page Request Queue Tail Register (PQT_REG_0_0_0_VTDBAR) — Offset C8h

Register indicating the page request queue tail. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + C8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:19	0h RO	**Reserved**
18:4	0000h RO/V	**Page Queue Tail (PQT):** Specifies the offset (16-bytes aligned) to the page request queue for the request that will be written next by hardware.
3:0	0h RO	**Reserved**

3.8.31 Page Request Queue Address Register (PQA_REG_0_0_0_VTDBAR) — Offset D0h

Register to configure the base address and size of the page request queue. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + D0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RO	**Page Request Queue Base Address (PQA):** This field points to the base of 4KB aligned page request queue. Hardware may ignore and not implement bits 63:HAW, where HAW is the host address width. Software must configure this register before enabling page requests in any extended-context-entries.

Bit Range	Default & Access	Field Name (ID): Description
11:3	0h RO	**Reserved**
2:0	0h RO	**Page Request Queue Size (PQS):** This field specifies the size of the page request queue. A value of X in this field indicates an invalidation request queue of (2^X) 4KB pages. The number of entries in the page request queue is 2^(X + 8)

3.8.32 Page Request Status Register (PRS_REG_0_0_0_VTDBAR) — Offset DCh

Register to report pending page request in page request queue. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + DCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V/P	**Pending Page Request (PPR):** Pending Page Request: Indicates pending page requests to be serviced by software in the page request queue. This field is Set by hardware when a streaming page request entry (page_stream_reg_dsc) or a page group request (page_grp_req_dsc) with Last Page in Group (LPG) field Set, is added to the page request queue.

3.8.33 Page Request Event Control Register (PECTL_REG_0_0_0_VTDBAR) — Offset E0h

Register specifying the page request event interrupt control bits. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + E0h	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**Interrupt Mask (IM):** Interrupt Mask • 0=No masking of interrupt. When a page request event condition is detected, hardware issues an interrupt message (using the Page Request Event Data and Page Request Event Address register values) • 1=This is the value on reset. Software may mask interrupt message generation by setting this field. Hardware is prohibited from sending the interrupt message when this field is Set.
30	0h RO/V	**Interrupt Pending (IP):** Interrupt Pending: Hardware sets the IP field whenever it detects an interrupt condition. Interrupt condition is defined as: • A streaming page request entry (page_stream_req_dsc) or a page group request (page_grp_req_dsc) with Last Page in Group (LPG) field Set, was added to page request queue, resulting in hardware setting the Pending Page Request (PPR) field in Page Request Status register • If the PPR field in the Page Request Event Status register was already Set at the time of setting this field, it is not treated as a new interrupt condition The IP field is kept Set by hardware while the interrupt message is held pending. The interrupt message could be held pending due to interrupt mask (IM field) being Set, or due to other transient hardware conditions. The IP field is cleared by hardware as soon as the interrupt message pending condition is serviced. This could be due to either: • Hardware issuing the interrupt message due to either change in the transient hardware condition that caused interrupt message to be held pending or due to software clearing the IM field • Software servicing the PPR field in the Page Request Event Status register.
29:0	0h RO	**Reserved**

3.8.34 Page Request Event Data Register (PEDATA_REG_0_0_0_VTDBAR) — Offset E4h

Register specifying the Page Request Event interrupt message data. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Extended Interrupt Message Data (EIMD):** Extended Interrupt Message Data
15:0	0000h RO	**Interrupt Message Data (IMD):** Interrupt Message Data: Data value in the interrupt request. Software requirements for programming this register are described in VTd Spec

3.8.35 Page Request Event Address Register (PEADDR_REG_0_0_0_VTDBAR) — Offset E8h

Register specifying the Page Request Event Interrupt message address. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RO	**Message Address (MA):** Message Address: When fault events are enabled, the contents of this register specify the DWORD-aligned address (bits 31:2) for the interrupt request.
1:0	0h RO	**Reserved**

3.8.36 Page Request Event Upper Address Register (PEUADDR_REG_0_0_0_VTDBAR) — Offset ECh

Register specifying the Page Request Event interrupt message upper address.

Type	Size	Offset	Default
MMIO	32 bit	VTDPVC0BAR + ECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Message Upper Address (MUA):** Message Upper Address: This field specifies the upper address (bits.. 63:32) for the page request event interrupt.

3.8.37 MTRR Capability Register (MTRRCAP_0_0_0_VTDBAR) — Offset 100h

Register reporting the Memory Type Range Register Capability. This register is treated as RsvdZ by implementations reporting Memory Type Support (MTS) as not supported in the Extended Capability register.

When implemented, value reported in this register must match IA32_MTRRCAP Model Specific Register (MSR) value reported by the host IA-32 processor(s).

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 100h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:11	0h RO	**Reserved**
10	0h RO	**Write Combining (WC):** • 0 = Write-combining (WC) memory type is not supported. • 1 = Write-combining (WC) memory type is supported.Indicates whether the Write Combining memory type is supported.
9	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**Fixed Range MTRRs Supported (FIX):** • 0 = No fixed range MTRRs are supported • 1 = Fixed range MTRRs (MTRR_FIX64K_00000 through MTRR_FIX4K_0F8000) are supported
7:0	00h RO	**Variable MTRR Count (VCNT):** Indicates number of variable range MTRRs are supported.

3.8.38 MTRR Default Type Register (MTRRDEFAULT_0_0_0_VTDBAR) — Offset 108h

Register for enabling/configuring Memory Type Range Registers. This register is treated as RsvdZ by implementations reporting Memory Type Support (MTS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 108h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:12	0h RO	**Reserved**
11	0h RO	**MTRR Enable (E):** • 0 = Disable MTRRs; UC memory type is applied. FE field has no effect. • 1 = Enable MTRRs. FE field can disable the fixed-range MTRRs. Type specified in the default memory type field is used for areas of memory not already mapped by either fixed or variable MTRR
10	0h RO	**Fixed Range MTRR Enable (FE):** • 0 = Disable fixed range MTRRs. • 1 = Enable fixed range MTRRs. When fixed range MTRRs are enabled, they take priority over the variable range MTRRs when overlaps in ranges occur. If the fixed-range MTRRs are disabled, the variable range MTRRs can still be used and can map the range ordinarily covered by the fixed range MTRRs.
9:8	0h RO	**Reserved**
7:0	00h RO	**Default Memory Type (MEMTYPE):** Indicates default memory type used for physical memory address ranges that do not have a memory type specified for them by an MTRR. Legal values for this field are 0,1,4, 5 and 6.

3.8.39 Fixed-Range MTRR Format 64K-00000 (MTRR_FIX64K_00000_REG_0_0_0_VTDBAR) — Offset 120h

Fixed Range MTRR covering the 64K memory space from 0x00000 - 0x7FFFF.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 120h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RO	**R7 IOMMU (R7):** Register Field 7
55:48	00h RO	**R6 IOMMU (R6):** Register Field 6
47:40	00h RO	**R5 IOMMU (R5):** Register Field 5
39:32	00h RO	**R4 IOMMU (R4):** Register Field 4
31:24	00h RO	**R3 IOMMU (R3):** Register Field 3
23:16	00h RO	**R2 IOMMU (R2):** Register Field 2
15:8	00h RO	**R1 IOMMU (R1):** Register Field 1
7:0	00h RO	**R0 IOMMU (R0):** Register Field 0

3.8.40 Fixed-Range MTRR Format 16K-80000 (MTRR_FIX16K_80000_REG_0_0_0_VTDBAR) — Offset 128h

Fixed Range MTRR covering the 16K memory space from 0x80000 - 0x9FFFF.

Note: **NOTE:** Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.8.41 Fixed-Range MTRR Format 16K-A0000 (MTRR_FIX16K_A0000_REG_0_0_0_VTDBAR) — Offset 130h

Fixed Range MTRR covering the 16K memory space from 0xA0000 - 0xBFFFF.

Note: **NOTE:** Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.8.42 Fixed-Range MTRR Format 4K-C0000 (MTRR_FIX4K_C0000_REG_0_0_0_VTDBAR) — Offset 138h

Fixed Range MTRR covering the 4K memory space 0xC0000 - 0xC7FFF.

Note: **NOTE:** Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.8.43 Fixed-Range MTRR Format 4K-C8000 (MTRR_FIX4K_C8000_REG_0_0_0_VTDBAR) — Offset 140h

Fixed Range MTRR covering the 4K memory space from 0xC8000 - 0xCFFFF.

Note: **NOTE:** Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.8.44 Fixed-Range MTRR Format 4K-D0000 (MTRR_FIX4K_D0000_REG_0_0_0_VTDBAR) — Offset 148h

Fixed Range MTRR covering the 4K memory space from 0xD0000 - 0xD7FFF.

Note: **NOTE:** Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.8.45 Fixed-Range MTRR Format 4K-D8000 (MTRR_FIX4K_D8000_REG_0_0_0_VTDBAR) — Offset 150h

Fixed Range MTRR covering the 4K memory space from 0xD80000 - 0xDFFFF.

Note: **NOTE:** Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.8.46 Fixed-Range MTRR Format 4K-E0000 (MTRR_FIX4K_E0000_REG_0_0_0_VTDBAR) — Offset 158h

Fixed Range MTRR covering the 4K memory space from 0xE0000 - 0xE7FFF.

Note: **NOTE:** Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.8.47 Fixed-Range MTRR Format 4K-E8000 (MTRR_FIX4K_E8000_REG_0_0_0_VTDBAR) — Offset 160h

Fixed Range MTRR covering the 4K memory space from 0xE8000 - 0xEFFFF.

Note: **NOTE:** Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.8.48 Fixed-Range MTRR Format 4K-F0000 (MTRR_FIX4K_F0000_REG_0_0_0_VTDBAR) — Offset 168h

Fixed Range MTRR covering the 4K memory space from 0xF0000 - 0xF7FFF.

Note: **NOTE:** Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.8.49 Fixed-Range MTRR Format 4K-F8000 (MTRR_FIX4K_F8000_REG_0_0_0_VTDBAR) — Offset 170h

Fixed Range MTRR covering the 4K memory space from 0xF8000 - 0xFFFFF.

Note: **NOTE:** Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

3.8.50 Variable-Range MTRR Format Physical Base 0 (MTRR_PHYSBASE0_REG_0_0_0_VTDBAR) — Offset 180h

Variable-Range MTRR BASE0

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 180h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	00000000 0h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 0
11:8	0h RO	**Reserved**
7:0	00h RO	**Memtype PHYSBASE (MEMTYPE):** Memory type for variable memory type range 0

3.8.51 Variable-Range MTRR Format Physical Mask 0 (MTRR_PHYSMASK0_REG_0_0_0_VTDBAR) — Offset 188h

Variable-Range MTRR MASK0

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 188h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	00000000 0h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 0
11	0h RO	**Valid PHYSMASK (VALID):** Valid bit for variable range 0 mask
10:0	0h RO	**Reserved**

3.8.52 Variable-Range MTRR Format Physical Base 1 (MTRR_PHYSBASE1_REG_0_0_0_VTDBAR) — Offset 190h

Variable-Range MTRR BASE1

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 190h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	00000000 0h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 1
11:8	0h RO	**Reserved**
7:0	00h RO	**Memtype PHYSBASE (MEMTYPE):** Memory type for variable memory type range 1

3.8.53 Variable-Range MTRR Format Physical Mask 1 (MTRR_PHYSMASK1_REG_0_0_0_VTDBAR) — Offset 198h

Variable-Range MTRR MASK1

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 198h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 1
11	0h RO	**Valid PHYSMASK (VALID):** Valid bit for variable range 1 mask
10:0	0h RO	**Reserved**

3.8.54 Variable-Range MTRR Format Physical Base 2 (MTRR_PHYSBASE2_REG_0_0_0_VTDBAR) — Offset 1A0h

Variable-Range MTRR BASE2

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 1A0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 2
11:8	0h RO	**Reserved**
7:0	00h RO	**Memtype PHYSBASE (MEMTYPE):** Memory type for variable memory type range 2

3.8.55 Variable-Range MTRR Format Physical Mask 2 (MTRR_PHYSMASK2_REG_0_0_0_VTDBAR) — Offset 1A8h

Variable-Range MTRR MASK2

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 1A8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	00000000 0h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 2
11	0h RO	**Valid PHYSMASK (VALID):** Valid bit for variable range 2 mask
10:0	0h RO	**Reserved**

3.8.56 Variable-Range MTRR Format Physical Base 3 (MTRR_PHYSBASE3_REG_0_0_0_VTDBAR) — Offset 1B0h

Variable-Range MTRR BASE3

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 1B0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	00000000 0h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 3
11:8	0h RO	**Reserved**
7:0	00h RO	**Memtype PHYSBASE (MEMTYPE):** Memory type for variable memory type range 3

3.8.57 Variable-Range MTRR Format Physical Mask 3 (MTRR_PHYSMASK3_REG_0_0_0_VTDBAR) — Offset 1B8h

Variable-Range MTRR MASK3

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 1B8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	00000000 0h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 3
11	0h RO	**Valid PHYSMASK (VALID):** Valid bit for variable range 3 mask
10:0	0h RO	**Reserved**

3.8.58 Variable-Range MTRR Format Physical Base 4 (MTRR_PHYSBASE4_REG_0_0_0_VTDBAR) — Offset 1C0h

Variable-Range MTRR BASE4

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 1C0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	00000000 0h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 4
11:8	0h RO	**Reserved**
7:0	00h RO	**Memtype PHYSBASE (MEMTYPE):** Memory type for variable memory type range 4

3.8.59 Variable-Range MTRR Format Physical Mask 4 (MTRR_PHYSMASK4_REG_0_0_0_VTDBAR) — Offset 1C8h

Variable-Range MTRR MASK4

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 1C8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	00000000 0h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 4
11	0h RO	**Valid PHYSMASK (VALID):** Valid bit for variable range 4 mask
10:0	0h RO	**Reserved**

3.8.60 Variable-Range MTRR Format Physical Base 5 (MTRR_PHYSBASE5_REG_0_0_0_VTDBAR) — Offset 1D0h

Variable-Range MTRR BASE5

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 1D0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	00000000 0h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 5
11:8	0h RO	**Reserved**
7:0	00h RO	**Memtype PHYSBASE (MEMTYPE):** Memory type for variable memory type range 5

3.8.61 Variable-Range MTRR Format Physical Mask 5 (MTRR_PHYSMASK5_REG_0_0_0_VTDBAR) — Offset 1D8h

Variable-Range MTRR MASK5

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 1D8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 5
11	0h RO	**Valid PHYSMASK (VALID):** Valid bit for variable range 5 mask
10:0	0h RO	**Reserved**

3.8.62 Variable-Range MTRR Format Physical Base 6 (MTRR_PHYSBASE6_REG_0_0_0_VTDBAR) — Offset 1E0h

Variable-Range MTRR BASE6

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 1E0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 6
11:8	0h RO	**Reserved**
7:0	00h RO	**Memtype PHYSBASE (MEMTYPE):** Memory type for variable memory type range 6

3.8.63 Variable-Range MTRR Format Physical Mask 6 (MTRR_PHYSMASK6_REG_0_0_0_VTDBAR) — Offset 1E8h

Variable-Range MTRR MASK6

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 1E8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	00000000 0h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 6
11	0h RO	**Valid PHYSMASK (VALID):** Valid bit for variable range 6 mask
10:0	0h RO	**Reserved**

3.8.64 Variable-Range MTRR Format Physical Base 7 (MTRR_PHYSBASE7_REG_0_0_0_VTDBAR) — Offset 1F0h

Variable-Range MTRR BASE7

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 1F0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	00000000 0h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 7
11:8	0h RO	**Reserved**
7:0	00h RO	**Memtype PHYSBASE (MEMTYPE):** Memory type for variable memory type range 7

3.8.65 Variable-Range MTRR Format Physical Mask 7 (MTRR_PHYSMASK7_REG_0_0_0_VTDBAR) — Offset 1F8h

Variable-Range MTRR MASK7

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 1F8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 7
11	0h RO	**Valid PHYSMASK (VALID):** Valid bit for variable range 7 mask
10:0	0h RO	**Reserved**

3.8.66 Variable-Range MTRR Format Physical Base 8 (MTRR_PHYSBASE8_REG_0_0_0_VTDBAR) — Offset 200h

Variable-Range MTRR BASE8

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 200h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 8
11:8	0h RO	**Reserved**
7:0	00h RO	**Memtype PHYSBASE (MEMTYPE):** Memory type for variable memory type range 8

3.8.67 Variable-Range MTRR Format Physical Mask 8 (MTRR_PHYSMASK8_REG_0_0_0_VTDBAR) — Offset 208h

Variable-Range MTRR MASK8

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 208h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	00000000 0h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 8
11	0h RO	**Valid PHYSMASK (VALID):** Valid bit for variable range 8 mask
10:0	0h RO	**Reserved**

3.8.68 Variable-Range MTRR Format Physical Base 9 (MTRR_PHYSBASE9_REG_0_0_0_VTDBAR) — Offset 210h

Variable-Range MTRR BASE9

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 210h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	00000000 0h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 9
11:8	0h RO	**Reserved**
7:0	00h RO	**Memtype PHYSBASE (MEMTYPE):** Memory type for variable memory type range 9

3.8.69 Variable-Range MTRR Format Physical Mask 9 (MTRR_PHYSMASK9_REG_0_0_0_VTDBAR) — Offset 218h

Variable-Range MTRR MASK9

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 218h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	00000000 0h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 9
11	0h RO	**Valid PHYSMASK (VALID):** Valid bit for variable range 9 mask
10:0	0h RO	**Reserved**

3.8.70 Fault Recording Register Low [0] (FRCDL_REG_0_0_0_VTDBAR) — Offset 400h

Register to record fault information when primary fault logging is active. Hardware reports the number and location of fault recording registers through the Capability register. This register is relevant only for primary fault logging

This register is sticky and can be cleared only through power good reset or by software clearing the RW1C fields by writing a 1.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 400h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:12	0000000000000h RO/V/P	**Fault Info (FI):** When the Fault Reason (FR) field indicates one of the address translation fault conditions, bits 63:12 of this field contains the page address in the faulted request. When PASID Present field is 0 (i.e, faulted request is a request without PASID), hardware treat bits 63:N as reserved (0), where N is the maximum guest address width (MGAW) supported. For requests-withPASID (PASID Present field = 1), hardware treats bits 63:N as reserved (0), where N corresponds to the largest AGAW value supported by hardware. When the Fault Reason (FR) field indicates interrupt-remapping fault conditions other than Fault Reason 25h, bits 63:48 of this field indicate the interrupt_index computed for the faulted interrupt request, and bits 47:12 are cleared. When the Fault Reason (FR) field indicates interrupt-remapping fault condition of blocked Compatibility mode interrupt (Fault Reason 25h), contents of this field is undefined. This field is relevant only when the F field is Set.
11:0	0h RO	**Reserved**

3.8.71 Fault Recording Register High [0] (FRCDH_REG_0_0_0_VTDBAR) — Offset 408h

Register to record fault information when primary fault logging is active. Hardware reports the number and location of fault recording registers through the Capability register. This register is relevant only for primary fault logging

This register is sticky and can be cleared only through power good reset or by software clearing the RW1C fields by writing a 1.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 408h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/1C/V/P	**Fault FRCDH (F):** Hardware sets this field to indicate a fault is logged in this Fault Recording register. The F field is set by hardware after the details of the fault is recorded in other fields When this field is Set, hardware may collapse additional faults from the same source-id (SID) Software writes the value read from this field to Clear it.
62	0h RO/V/P	**Type FRCDH (T):** Type of the faulted request: • 0=0: Write request or Page (PRS) Request • 1=1: Read request or AtomicOp request This field is relevant only when the F field is Set, and when the fault reason (FR) indicates one of the DMA-remapping fault conditions.
61:60	0h RO/V/P	**Address Type (AT):** This field captures the AT field from the faulted DMA request Hardware implementations not supporting Device-IOTLBs (DI field Clear in Extended Capability register) treat this field as RsvdZ When supported, this field is valid only when the F field is Set, and when the fault reason (FR) indicates one of the DMA-remapping fault conditions.
59:40	00000h RO/V/P	**PASID Value (PV):** PASID value in the faulted request. This field is relevant only when the PP field is set. Hardware implementations not supporting PASID (PASID field Clear in Extended Capability register) implement this field as RsvdZ.
39:32	00h RO/V/P	**Fault Reason (FR):** Reason for the fault This field is relevant only when the F field is set.
31	0h RO/V/P	**PASID Present (PP):** When set, indicates the faulted request has a PASID tag. The value of the PASID field is reported in the PASID Value (PV) field. This field is relevant only when the F field is Set, and when the fault reason (FR) indicates one of the non-recoverable address translation fault conditions. Hardware implementations not supporting PASID (PASID field Clear in Extended Capability register) implement this field as RsvdZ.
30	0h RO/V/P	**Execute Permission Requested (EXE):** When set, indicates Execute permission was requested by the faulted read request. This field is relevant only when the PP field and T field are both Set. Hardware implementations not supporting PASID (PASID field Clear in Extended Capability register) implement this field as RsvdZ.

Bit Range	Default & Access	Field Name (ID): Description
29	0h RO/V/P	**Privilege Mode Requested (PRIV):** When set, indicates Supervisor privilege was requested by the faulted request. This field is relevant only when the PP field is Set. Hardware implementations not supporting PASID (PASID field Clear in Extended Capability register) implement this field as RsvdZ.
28:16	0h RO	**Reserved**
15:0	0000h RO/V/P	**Source Identifier (SID):** Requester-id associated with the fault condition This field is relevant only when the F field is set.

3.8.72 Invalidate Address Register (IVA_REG_0_0_0_VTDBAR) — Offset 500h

Register to provide the DMA address whose corresponding IOTLB entry needs to be invalidated through the corresponding IOTLB Invalidate register. This register is a write-only register.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 500h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:12	00000000 00000h WO	**Address IVA (ADDR):** Software provides the DMA address that needs to be page-selectively invalidated. To make a page-selective invalidation request to hardware, software must first write the appropriate fields in this register, and then issue the appropriate page-selective invalidate command through the IOTLB_REG. Hardware ignores bits 63:N, where N is the maximum guest address width (MGAW) supported. A value retuned on a read of this field is undefined A value returned on a read of this field is undefined
11:7	0h RO	**Reserved**
6	0h WO	**Invalidation Hint (IH):** The field provides hint to hardware about preserving or flushing the non-leaf (page-directory) entries that may be cached in hardware: • 0 = Software may have modified both leaf and non-leaf page-table entries corresponding to mappings specified in the ADDR and AM fields. On a page-selective invalidation request, hardware must flush both the cached leaf and non-leaf page-table entries corresponding to the mappings specified by ADDR and AM fields. • 1 = Software has not modified any non-leaf page-table entries corresponding to mappings specified in the ADDR and AM fields. On a page-selective invalidation request, hardware may preserve the cached non-leaf page-table entries corresponding to mappings specified by ADDR and AM fields. A value returned on a read of this field is undefined

Bit Range	Default & Access	Field Name (ID): Description
5:0	00h WO	**Address Mask (AM):** The value in this field specifies the number of low order bits of the ADDR field that must be masked for the invalidation operation. This field enables software to request invalidation of contiguous mappings for size-aligned regions. For example:..Mask ADDR bits Pages..Value masked invalidated.. 0 None 1.. 1 12 2.. 2 13:12 4.. 3 14:12 8.. 4 15:12 16 When invalidating mappings for super-pages, software must specify the appropriate mask value. For example, when invalidating mapping for a 2MB page, software must specify an address mask value of at least 9...Hardware implementations report the maximum supported mask value through the Capability register.

3.8.73 IOTLB Invalidate Register (IOTLB_REG_0_0_0_VTDBAR) — Offset 508h

Register to invalidate IOTLB. The act of writing the upper byte of the IOTLB_REG with IVT field Set causes the hardware to perform the IOTLB invalidation.

Type	Size	Offset	Default
MMIO	64 bit	VTDPVC0BAR + 508h	0200000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/V	**Invalidate IOTLB (IVT):** Software requests IOTLB invalidation by setting this field. Software must also set the requested invalidation granularity by programming the IIRG field Hardware clears the IVT field to indicate the invalidation request is complete. Hardware also indicates the granularity at which the invalidation operation was performed through the IAIG field. Software must not submit another invalidation request through this register while the IVT field is Set, nor update the associated Invalidate Address register Software must not submit IOTLB invalidation requests when there is a context-cache invalidation request pending at this remapping hardware unit. Hardware implementations reporting write-buffer flushing requirement (RWBF=1 in Capability register) must implicitly perform a write buffer flushing before invalidating the IOTLB.
62	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
61:60	0h RW	**IOTLB Invalidation Request Granularity (IIRG):** When requesting hardware to invalidate the IOTLB (by setting the IVT field), software writes the requested invalidation granularity through this field. The following are the encodings for the field • 00 = Reserved • 01 = Global invalidation request • 10 = Domain-selective invalidation request. The target domain-id must be specified in the DID field • 11 = Page-selective invalidation request. The target address, mask and invalidation hint must be specified in the Invalidate Address register, and the domain-id must be provided in the DID field Hardware implementations may process an invalidation request by performing invalidation at a coarser granularity than requested. Hardware indicates completion of the invalidation request by clearing the IVT field. At this time, the granularity at which actual invalidation was performed is reported through the IAIG field
59	0h RO	**Reserved**
58:57	1h RO/V	**IOTLB Actual Invalidation Granularity (IAIG):** Hardware reports the granularity at which an invalidation request was processed through this field when reporting invalidation completion (by clearing the IVT field). The following are the encodings for this field • 00 = Reserved. This indicates hardware detected an incorrect invalidation request and ignored the request. Examples of incorrect invalidation requests include detecting an unsupported address mask value in Invalidate Address register for page-selective invalidation requests • 01 = Global Invalidation performed. This could be in response to a global, domain-selective, or page-selective invalidation request • 10 = Domain-selective invalidation performed using the domain-id specified by software in the DID field. This could be in response to a domain-selective or a page-selective invalidation request • 11 = Domain-page-selective invalidation performed using the address, mask and hint specified by software in the Invalidate Address register and domain-id specified in DID field. This can be in response to a page-selective invalidation request.
56:50	0h RO	**Reserved**
49	0h RW	**Drain Reads (DR):** This field is ignored by hardware if the DRD field is reported as clear in the Capability register. When the DRD field is reported as Set in the Capability register, the following encodings are supported for this field: • 0 = Hardware may complete the IOTLB invalidation without draining any translated DMA read requests • 1 = Hardware must drain DMA read requests.
48	0h RW	**Drain Writes (DW):** This field is ignored by hardware if the DWD field is reported as Clear in the Capability register. When the DWD field is reported as Set in the Capability register, the following encodings are supported for this field: • 0 = Hardware may complete the IOTLB invalidation without draining DMA write requests • 1 = Hardware must drain relevant translated DMA write requests.
47:32	0000h RW	**Domain ID (DID):** Indicates the ID of the domain whose IOTLB entries need to be selectively invalidated. This field must be programmed by software for domain-selective and page-selective invalidation requests. The Capability register reports the domain-id width supported by hardware. Software must ensure that the value written to this field is within this limit. Hardware ignores and not implements bits 47:(32+N), where N is the supported domain-id width reported in the Capability register.
31:0	0h RO	**Reserved**

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4 Processor Graphics (D2:F0)

This chapter documents the Processor Graphics Registers.

Table 4-1. Summary of Processor Graphics (D2:F0)

"Processor Graphics Registers (D2:F0)"
"Graphics VT BAR (GFXVTBAR) Registers"

4.1 Processor Graphics Registers (D2:F0)

Processor Graphics device. This section contains the registers in: Bus 0, Device 2, Function 0.

4.1.1 Summary of Registers

Table 4-2. Summary of Bus: 0, Device: 2, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	2	Vendor Identification (VID2_0_2_0_PCI)	8086h
2h	2	Device Identification (DID2_0_2_0_PCI)	9A40h
4h	2	PCI Command (PCICMD_0_2_0_PCI)	0000h
6h	2	PCI Status (PCISTS2_0_2_0_PCI)	0010h
8h	4	Revision Identification and Class Code register (RID2_CC_0_2_0_PCI)	03000000h
Ch	1	Cache Line Size (CLS_0_2_0_PCI)	00h
Dh	1	INITIATOR Latency Timer (MLT2_0_2_0_PCI)	00h
Eh	1	Header Type (HDR2_0_2_0_PCI)	00h
Fh	1	Built In Self Test (BIST_0_2_0_PCI)	00h
10h	4	Graphics Translation Table Memory Mapped Range Address (GTTMMADR0_0_2_0_PCI)	00000004h
14h	4	Graphics Translation Table Memory Mapped Range Address (GTTMMADR1_0_2_0_PCI)	00000000h
18h	4	Graphics Memory Range Address (GMADR0_0_2_0_PCI)	0000000Ch
1Ch	4	Graphics Memory Range Address (GMADR1_0_2_0_PCI)	00000000h
20h	4	I/O Base Address (IOBAR_0_2_0_PCI)	00000001h
2Ch	2	Subsystem Vendor Identification (SVID2_0_2_0_PCI)	0000h
2Eh	2	Subsystem Identification (SID2_0_2_0_PCI)	0000h
30h	4	Video BIOS ROM Base Address (ROMADR_0_2_0_PCI)	00000000h
34h	1	Capabilities Pointer (CAPPOINT_0_2_0_PCI)	40h
3Ch	1	Interrupt Line (INTRLINE_0_2_0_PCI)	00h
3Dh	1	Interrupt Pin (INTRPIN_0_2_0_PCI)	01h
3Eh	1	Minimum Grant (MINGNT_0_2_0_PCI)	00h
3Fh	1	Maximum Latency (MAXLAT_0_2_0_PCI)	00h
40h	2	Capability Identifier (CAPID0_0_2_0_PCI)	7009h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
42h	2	Capabilities Control (CAPCTRL0_0_2_0_PCI)	010Ch
44h	4	Capabilities A (CAPID0_A_0_2_0_PCI)	00000000h
48h	4	Capabilities B (CAPID0_B_0_2_0_PCI)	00000000h
50h	2	PCI Mirror of GMCH Graphics Control (MGGC0_0_2_0_PCI)	0500h
54h	2	Mirror of Device Enable (DEVEN0_0_2_0_PCI)	00BFh
58h	1	Device 2 Control (DEV2CTL_0_2_0_PCI)	00h
60h	4	Multi Size Aperture Control (MSAC_0_2_0_PCI)	00000000h
68h	4	PUSHAP_0_2_0_PCI	00000000h
6Ch	1	VTd Status (VTD_STATUS_0_2_0_PCI)	00h
70h	2	PCI Express Capability Header (PCIECAPHDR_0_2_0_PCI)	AC10h
72h	2	PCI Express Capability (PCIECAP_0_2_0_PCI)	0092h
74h	4	Device Capabilities (DEVICECAP_0_2_0_PCI)	10008000h
78h	2	PCI Express Device Control (DEVICECTL_0_2_0_PCI)	0000h
7Ah	2	PCI Express Capability Structure (DEVICESTS_0_2_0_PCI)	0000h
ACh	2	Message Signaled Interrupts Capability ID (MSI_CAPID_0_2_0_PCI)	D005h
AEh	2	Message Control (MC_0_2_0_PCI)	0100h
B0h	4	Message Address (MA_0_2_0_PCI)	00000000h
B4h	2	Message Data (MD_0_2_0_PCI)	0000h
B8h	4	MSI Mask Bits (MSI_MASK_0_2_0_PCI)	00000000h
BCh	4	MSI Pending Bits (MSI_PEND_0_2_0_PCI)	00000000h
C0h	4	Mirror of Base Data of Stolen Memory (BDSM0_0_2_0_PCI)	00000000h
C4h	4	Mirror of Base Data of Stolen Memory (BDSM1_0_2_0_PCI)	00000000h
C8h	4	GFXVTDBAR_LSB_0_2_0_PCI	00000000h
CCh	4	GFXVTDBAR_MSB_0_2_0_PCI	00000000h
D0h	2	Power Management Capabilities ID (PMCAPID_0_2_0_PCI)	0001h
D2h	2	Power Management Capabilities (PMCAP_0_2_0_PCI)	0022h
D4h	2	Power Management Control and Status (PMCS_0_2_0_PCI)	0000h
E0h	2	Software SMI (SWSMI_0_2_0_PCI)	0000h
E4h	4	Graphics System Event (GSE_0_2_0_PCI)	00000000h
E8h	2	Software SCI (SWSCI_0_2_0_PCI)	0000h
F0h	4	Dev2 Mirror of Protected Audio Video Path Control (PAVPC0_0_2_0_PCI)	00000000h
F4h	4	Dev2 Mirror of Protected Audio Video Path Control (PAVPC1_0_2_0_PCI)	00000000h
F8h	4	Stepping Revision ID (SRID_0_2_0_PCI)	00000000h
FCh	4	ASL Storage (ASLS_0_2_0_PCI)	00000000h
100h	4	PASID Extended Capability Header (PASID_EXTCAP_0_2_0_PCI)	2001001Bh
104h	2	PASID Capability (PASID_CAP_0_2_0_PCI)	1400h
106h	2	PASID Control (PASID_CTRL_0_2_0_PCI)	0000h
200h	4	ATS Extended Capability Header (ATS_EXTCAP_0_2_0_PCI)	3001000Fh
204h	2	ATS Capability (ATS_CAP_0_2_0_PCI)	0060h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
206h	2	ATS Control (ATS_CTRL_0_2_0_PCI)	0000h
300h	4	Page Request Extended Capability Header (PR_EXTCAP_0_2_0_PCI)	00010013h
304h	2	Page Request Control (PR_CTRL_0_2_0_PCI)	0000h
306h	2	Page Request Status (PR_STATUS_0_2_0_PCI)	8100h
308h	4	Outstanding Page Request Capacity (OPRC_0_2_0_PCI)	00008000h
30Ch	4	Outstanding Page Request Allocation (OPRA_0_2_0_PCI)	00000000h
320h	4	SRIOV Extended Capability Header (SRIOV_ECAPHDR_0_2_0_PCI)	00010010h
324h	4	SRIOV Capabilities (SRIOV_CAP_0_2_0_PCI)	00000000h
32Ah	2	SRIOV Status (SRIOV_STS_0_2_0_PCI)	0000h
32Ch	2	SRIOV Initial VFs (SRIOV_INITVFS_0_2_0_PCI)	0007h
32Eh	2	SRIOV Total VFs (SRIOV_TOTVFS_0_2_0_PCI)	0007h
334h	2	First VF Offset (FIRST_VF_OFFSET_0_2_0_PCI)	0001h
336h	2	VF Stride (VF_STRIDE_0_2_0_PCI)	0001h
33Ah	2	VF Device ID (VF_DEVICEID_0_2_0_PCI)	9A40h
33Ch	4	Supported Page Sizes (SUPPORTED_PAGE_SIZES_0_2_0_PCI)	00000553h
340h	4	System Page Sizes (SYSTEM_PAGE_SIZES_0_2_0_PCI)	00000001h
344h	4	VF BAR0 LDW (VF_BAR0_LDW_0_2_0_PCI)	00000004h
348h	4	VF BAR0 UDW (VF_BAR0_UDW_0_2_0_PCI)	00000000h
34Ch	4	VF BAR1 LDW (VF_BAR1_LDW_0_2_0_PCI)	0000000Ch
350h	4	VF BAR1 UDW (VF_BAR1_UDW_0_2_0_PCI)	00000000h
354h	4	VF BAR2 LDW (VF_BAR2_LDW_0_2_0_PCI)	00000000h
358h	4	VF BAR2 UDW (VF_BAR2_UDW_0_2_0_PCI)	00000000h
35Ch	4	VF Migration State Array Offset (VF_MIGST_OFFSET_0_2_0_PCI)	00000000h

4.1.2 Vendor Identification (VID2_0_2_0_PCI) — Offset 0h

This register combined with the Device Identification register uniquely identifies any PCI device.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 0h	8086h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RO	**VENDOR IDENTIFICATION NUMBER (VID):** PCI standard identification for Intel.

4.1.3 Device Identification (DID2_0_2_0_PCI) — Offset 2h

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 2h	9A40h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:7	134h RO	**DEVICE IDENTIFICATION NUMBER MSB (DID_MSB):** All 16 bits of Device ID is acquired through fuse pull as per Chassis 2.1 updates. SetIDValue message would continue to be supported. SetIDValue message will only update bits[15:7] of Device ID
6:0	40h RO/V	**DEVICE IDENTIFICATION NUMBER SKU (DID_SKU):** All 16 bits of Device ID is acquired through fuse pull as per Chassis 2.1 updates.

4.1.4 PCI Command (PCICMD_0_2_0_PCI) — Offset 4h

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant Initiator accesses to main memory.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 4h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**Reserved**
10	0h RW/V	**INTERRUPT DISABLE (INTDIS):** This bit disables the device from asserting INTx#. 0: Enable the assertion of this device's INTx# signal. 1: Disable the assertion of this device's INTx# signal. DO_INTx messages will not be sent to DMI.
9	0h RO	**FAST BACK-TO-BACK (FB2B):** Not Implemented. Hardwired to 0.
8	0h RO	**SERR ENABLE (SEN):** Not Implemented. Hardwired to 0.
7	0h RO	**WAIT CYCLE CONTROL (WCC):** Not Implemented. Hardwired to 0.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**PARITY ERROR ENABLE (PER):** Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	0h RO	**VIDEO PALETTE SNOOPING (VPS):** This bit is hardwired to 0 to disable snooping.
4	0h RO	**MEMORY WRITE AND INVALIDATE ENABLE (MWIE):** Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	0h RO	**SPECIAL CYCLE ENABLE (SCE):** This bit is hardwired to 0. The IGD ignores Special cycles.
2	0h RW/V	**BUS INITIATOR ENABLE (BME):** 0: Disable IGD bus Initiator. 1: Enable the IGD to function as a PCI compliant Initiator.
1	0h RW/V	**MEMORY ACCESS ENABLE (MAE):** This bit controls the IGD's response to memory space accesses. 0: Disable. 1: Enable.
0	0h RW/V/L	**I/O ACCESS ENABLE (IOAE):** This bit controls the IGD's response to I/O space accesses. 0: Disable. 1: Enable. This field is RO 1'b0 if DEV2CTL[0] IOBARDIS at offset 0x58 is 1b. **Locked by:** DEV2CTL_0_2_0_PCI.IOBARDIS

4.1.5 PCI Status (PCISTS2_0_2_0_PCI) — Offset 6h

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant Initiator abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 6h	0010h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**DETECTED PARITY ERROR (DPE):** Since the IGD does not detect parity, this bit is always hardwired to 0.
14	0h RO	**SIGNALED SYSTEM ERROR (SSE):** The IGD never asserts SERR#, therefore this bit is hardwired to 0.
13	0h RO	**RECEIVED INITIATOR ABORT STATUS (RMAS):** The IGD never gets a Initiator Abort, therefore this bit is hardwired to 0.
12	0h RO	**RECEIVED TARGET ABORT STATUS (RTAS):** The IGD never gets a Target Abort, therefore this bit is hardwired to 0.
11	0h RO	**SIGNALED TARGET ABORT STATUS (STAS):** Hardwired to 0. The IGD does not use target abort semantics.
10:9	0h RO	**DEVSEL TIMING (DEVT):** Hardwired to 00.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**INITIATOR DATA PARITY ERROR DETECTED (DPD):** Since Parity Error Response is hardwired to disabled, and the IGD does not do any parity detection, this bit is hardwired to 0.
7	0h RO	**FAST BACK-TO-BACK (FB2B):** Hardwired to 0 to be compliant to PCI Express Base Spec (rev 3.0).
6	0h RO	**USER DEFINED FORMAT (UDF):** Hardwired to 0.
5	0h RO	**66 MHZ PCI CAPABLE (C66):** Hardwired to 0.
4	1h RO	**CAPABILITY LIST (CLIST):** This bit is hardwired to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.
3	0h RO/V	**INTERRUPT STATUS (INTSTS):** This bit reflects the state of the interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the devices INTx# signal be asserted.
2:0	0h RO	**Reserved**

4.1.6 Revision Identification and Class Code register (RID2_CC_0_2_0_PCI) — Offset 8h

This register contains the revision number for Device #2 Functions 0 and contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 8h	03000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	03h RO/V	**BASE CLASS CODE (BCC):** This is an 8-bit value that indicates the base class code. When MGGC0[VAMEN] is 0 this code has the value 03h, indicating a Display Controller. When MGGC0[VAMEN] is 1 this code has the value 03h, indicating a Display Controller Device.
23:16	00h RO/V	**SUB-CLASS CODE (SUBCC):** When MGGC0[VAMEN] is 0, this value is 00h. When MGGC0[VAMEN] is 1, this value is 80h, indicating other display device.
15:8	00h RO	**PROGRAMMING INTERFACE (PI):** When MGGC0[VAMEN] is 0 this value is 00h, indicating a Display Controller.When MGGC0[VAMEN] is 1 this value is 00h, indicating a NOP.

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**REVISION IDENTIFICATION NUMBER (RID):** All 8 bits of Revision ID is acquired through fuse pull as per Chassis 2.1 updates SetIDValue message would continue to be supported. SetIDValue message will update bits[7:0] of Revision ID

4.1.7 Cache Line Size (CLS_0_2_0_PCI) — Offset Ch

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:2, F:0] + Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**CACHE LINE SIZE VALUE (CLS):** This field is implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no effect on any PCI Express device behavior.

4.1.8 INITIATOR Latency Timer (MLT2_0_2_0_PCI) — Offset Dh

The IGD does not support the programmability of the initiator latency timer because it does not perform bursts.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:2, F:0] + Dh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**INITIATOR LATENCY TIMER COUNT VALUE (MLTCV):** Hardwired to 0s.

4.1.9 Header Type (HDR2_0_2_0_PCI) — Offset Eh

This register contains the Header Type of the IGD.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:2, F:0] + Eh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**MULTI FUNCTION STATUS (MFUNC):** Indicates if the device is a Multi-Function Device. The Value of this register is hardwired to 0, internal graphics is a single function.
6:0	00h RO	**HEADER CODE (H):** This is a 7-bit value that indicates the Header Code for the IGD. This code is hardwired to the value 00h, indicating a type 0 configuration space format.

4.1.10 Built In Self Test (BIST_0_2_0_PCI) — Offset Fh

This register is used for control and status of Built In Self Test (BIST).

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:2, F:0] + Fh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**BIST SUPPORTED (BISTS):** BIST is not supported. This bit is hardwired to 0.
6:0	0h RO	**Reserved**

4.1.11 Graphics Translation Table Memory Mapped Range Address (GTTMMADR0_0_2_0_PCI) — Offset 10h

This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 16 MB combined for MMIO and Global GTT aperture, with 2MB of that used by MMIO, 6MB reserved, and 8MB used by GTT. GTTADR will begin at (GTTMMADR + 8 MB) while the MMIO base address will be the same as GTTMMADR. The region between (GTTMMADR + 2MB) - (GTTMMADR + 8MB) is reserved. For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT

memory area. The device snoops writes to this region in order to invalidate any cached translations within the various TLB's implemented on-chip. The allocation is for 16MB and the base address is defined by bits [38:24].

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 10h	00000004h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW/V	**MEMORY BASE ADDRESS (MBA_0):** Set by the OS, these bits correspond to address signals [63:24].
23:4	00000h RO	**ADDRESS MASK (ADM):** Hardwired to 0s to indicate at least 16MB address range.
3	0h RO	**PREFETCHABLE MEMORY (PREFMEM):** Hardwired to 0 to prevent prefetching.
2:1	2h RO	**MEMORY TYPE (MEMTYP):** Hardwired to 2h to indicate 64 bit base address.
0	0h RO	**MEMORY/IO SPACE (MIOS):** Hardwired to 0 to indicate memory space.

4.1.12 Graphics Translation Table Memory Mapped Range Address (GTTMMADR1_0_2_0_PCI) — Offset 14h

This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 16 MB combined for MMIO and Global GTT aperture, with 2MB of that used by MMIO, 6MB reserved, and 8MB used by GTT. GTTADR will begin at (GTTMMADR + 8 MB) while the MMIO base address will be the same as GTTMMADR. The region between (GTTMMADR + 2MB) - (GTTMMADR + 8MB) is reserved. For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area. The device snoops writes to this region in order to invalidate any cached translations within the various TLB's implemented on-chip. The allocation is for 16MB and the base address is defined by bits [38:24].

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 14h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**MEMORY BASE ADDRESS (MBA_1):** Set by the OS, these bits correspond to address signals [63:24].

4.1.13 Graphics Memory Range Address (GMADR0_0_2_0_PCI) — Offset 18h

GMADR is the PCI aperture used by S/W to access tiled GFX surfaces in a linear fashion.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 18h	0000000Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V/L	**4096 MB ADDRESS MASK (ADMSK4096):** This bit is either part of the Memory Base Address (R/W) or part of Address Mask (RO) depending on the value of MSAC.APSZ.RO and forced to 0 when MSAC.APSZ >= 4096MB. (i.e. MSAC.APSZ[4]=1) **Locked by:** MSAC_0_2_0_PCI.APSZ4
30	0h RW/V/L	**2048 MB ADDRESS MASK (ADMSK2048):** This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ.RO and forced to 0 when MSAC.APSZ >= 2048MB. (i.e. MSAC.APSZ[3]=1) **Locked by:** MSAC_0_2_0_PCI.APSZ3
29	0h RW/V/L	**1024 MB ADDRESS MASK (ADMSK1024):** This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ.RO and forced to 0 when MSAC.APSZ >= 1024MB. (i.e. MSAC.APSZ[2]=1) **Locked by:** MSAC_0_2_0_PCI.APSZ2
28	0h RW/V/L	**512MB ADDRESS MASK (ADMSK512):** This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ.RO and forced to 0 when MSAC.APSZ >= 512MB. (i.e. MSAC.APSZ[1]=1) **Locked by:** MSAC_0_2_0_PCI.APSZ1

Bit Range	Default & Access	Field Name (ID): Description
27	0h RW/V/L	**256 MB ADDRESS MASK (ADMSK256):** This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ.RO and forced to 0 when MSAC.APSZ >= 256MB. (i.e. MSAC.APSZ[0]=1) **Locked by:** MSAC_0_2_0_PCI.APSZ0
26:4	000000h RO	**ADDRESS MASK (ADM):** Hardwired to 0s to indicate at least 128MB address range.
3	1h RO	**PREFETCHABLE MEMORY (PREFMEM):** Hardwired to 1 to enable prefetching.
2:1	2h RO	**MEMORY TYPE (MEMTYP):** Hardwired to 2h to indicate 64 bit base address.
0	0h RO	**MEMORY/IO SPACE (MIOS):** Hardwired to 0 to indicate memory space.

4.1.14 Graphics Memory Range Address (GMADR1_0_2_0_PCI) — Offset 1Ch

GMADR is the PCI aperture used by S/W to access tiled GFX surfaces in a linear fashion.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 1Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**MEMORY BASE ADDRESS (MBA):** Set by the OS, these bits correspond to address signals [63:32].

4.1.15 I/O Base Address (IOBAR_0_2_0_PCI) — Offset 20h

This register provides the Base offset of the I/O registers within Device #2. Bits 15:6 are programmable allowing the I/O Base to be located anywhere in 16bit I/O Address Space. Bits 2:1 are fixed and return zero; bit 0 is hardwired to a one indicating that 8 bytes of I/O space are decoded. Access to the 8Bs of IO space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set. Access is disallowed in PM states D1-D3 or if IO Enable is clear or if Device #2 is turned off or if Internal graphics is disabled through the fuse or fuse override mechanisms.Note that access to this IO BAR is independent of VGA functionality within Device #2. If accesses to this IO bar is allowed then all 8, 16 or 32 bit IO cycles from IA cores that falls within the 8B are claimed. This IO BAR can be disabled and hidden from system software via DEV2CTL[0] IOBARDIS at offset 0x58.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 20h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:6	000h RW/V/L	**IO BASE ADDRESS (IOBASE):** Set by the OS, these bits correspond to address signals [15:6]. Note: This field is RO 0's if DEV2CTL[0] IOBARDIS is 1b. **Locked by:** DEV2CTL_0_2_0_PCI.IOBARDIS
5:3	0h RO	**Reserved**
2:1	0h RO	**MEMORY TYPE (MEMTYPE):** Hardwired to 0s to indicate 32-bit address.
0	1h RO	**MEMORY/IO SPACE (MIOS):** Hardwired to '1' to indicate IO space. Note: This field is RO 0's if DEV2CTL[0] IOBARDIS is 1b.

4.1.16 Subsystem Vendor Identification (SVID2_0_2_0_PCI) — Offset 2Ch

This register is used to uniquely identify the subsystem where the PCI device resides.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 2Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**SUBSYSTEM VENDOR ID (SUBVID):** This value is used to identify the vendor of the subsystem.

4.1.17 Subsystem Identification (SID2_0_2_0_PCI) — Offset 2Eh

This register is used to uniquely identify the subsystem where the PCI device resides.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 2Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**SUBSYSTEM IDENTIFICATION (SUBID):** This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up.

4.1.18 Video BIOS ROM Base Address (ROMADR_0_2_0_PCI) — Offset 30h

The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0s.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 30h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0000h RO	**ROM BASE ADDRESS (RBA):** Hardwired to 0's.
17:11	00h RO	**ADDRESS MASK (ADMSK):** Hardwired to 0s to indicate 256 KB address range.
10:1	0h RO	**Reserved**
0	0h RO	**ROM BIOS ENABLE (RBE):** Hardwired to 0 to indicate ROM not accessible.

4.1.19 Capabilities Pointer (CAPPOINT_0_2_0_PCI) — Offset 34h

This register points to a linked list of capabilities implemented by this device.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:2, F:0] + 34h	40h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	40h RO	**CAPABILITIES POINTER VALUE (CPV):** This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List, the CAPID0 register at offset 40h.

4.1.20 Interrupt Line (INTRLINE_0_2_0_PCI) — Offset 3Ch

This register is used to communicate interrupt line routing information. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:2, F:0] + 3Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**INTERRUPT CONNECTION (INTCON):** Used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates to which input of the system interrupt controller the device's interrupt pin is connected.

4.1.21 Interrupt Pin (INTRPIN_0_2_0_PCI) — Offset 3Dh

This register tells which interrupt pin the device uses.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:2, F:0] + 3Dh	01h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	01h RO	**INTERRUPT PIN VALUE (INTPIN):** As a single function device, the IGD specifies INTA# as its interrupt pin. Hardwired to 01h = INTA#.

4.1.22 Minimum Grant (MINGNT_0_2_0_PCI) — Offset 3Eh

The Integrated Graphics Device has no requirement for the settings of Latency Timers.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:2, F:0] + 3Eh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**MINIMUM GRANT VALUE (MGV):** Hardwired to 0s because the IGD does not burst as a PCI compliant initiator.

4.1.23 Maximum Latency (MAXLAT_0_2_0_PCI) — Offset 3Fh

The Integrated Graphics Device has no requirement for the settings of Latency Timers.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:2, F:0] + 3Fh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**MAXIMUM LATENCY VALUE (MLV):** Hardwired to 0s because the IGD has no specific requirements for how often it needs to access the PCI bus.

4.1.24 Capability Identifier (CAPID0_0_2_0_PCI) — Offset 40h

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 40h	7009h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	70h RO	**NEXT CAPABILITY POINTER (NEXT_CAP):** This field is hardwired to point to the next PCI Capability structure, the PCIe Capabilities structure at 70h.
7:0	09h RO	**CAPABILITY IDENTIFIER (CAP_ID):** This field is hardwired to the value 09h to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

4.1.25 Capabilities Control (CAPCTRL0_0_2_0_PCI) — Offset 42h

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 42h	010Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
11:8	1h RO	**CAPID VERSION (CAPID_VER):** This field is hardwired to the value 1h to identify the first revision of the CAPID register definition.
7:0	0Ch RO	**CAPID LENGTH (CAPIDLEN):** This field is hardwired to the value 0Ch to indicate the structure length (12 bytes).

4.1.26 Capabilities A (CAPID0_A_0_2_0_PCI) — Offset 44h

Populated by pulling relevant fuses.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 44h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO/V	**DISPLAY FUSA DISABLE (DISPLAY_FUSA_DIS):** Fuse to disable FuSa
23:4	0h RO	**Reserved**
3	0h RO/V	**VGT ENABLE FUSE (VGT_EN_FUSE):**
2	0h RO	**Reserved**
1	0h RO/V	**SVM DISABLE FUSE (SVMD):**
0	0h RO/V	**VTD DISABLE FUSE (VTDD):**

4.1.27 Capabilities B (CAPID0_B_0_2_0_PCI) — Offset 48h

Populated by pulling relevant fuses.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 48h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

4.1.28 PCI Mirror of GMCH Graphics Control (MGGC0_0_2_0_PCI) — Offset 50h

Mirror of GGC register from GTTMMADR Space at offset 0x108040.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 50h	0500h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:8	05h RO/V	**GMS:** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. It corresponds to DSM (Data Stolen Memory region) region. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0. BIOS Requirement: Given new sizes allow down to 8MB allocation, BIOS has to ensure there is sufficient space for WOPCM and basic GFX Stolen functions. 00h:0MB 01h:32MB 02h:64MB 03h:96MB 04h:128MB 05h:160MB 06h:192MB 07h:224MB 08h:256MB 09h:288MB 0Ah:320MB 0Bh:352MB 0Ch:384MB 0Dh:416MB 0Eh:448MB 0Fh:480MB 10h:512MB 11h - 1Fh: Reserved 20h:1024MB 21h - 2Fh: Reserved 30h:1536MB 31h - 3Fh: Reserved 40h: 2048MB 41h - EFh: Reserved F0h: 4MB F1h: 8MB F2h: 12MB F3h: 16MB F4h: 20MB F5h: 24MB F6h: 28MB F7h: 32MB F8h: 36MB F9h: 40MB FAh: 44MB FBh: 48MB FCh: 52MB FDh: 56MB FEh: 60MB FFh: Reserved Hardware functionality in case of programming this value to Reserved is not guaranteed.
7:6	0h RO/V	**GGMS:** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register. Hardware functionality in case of programming this value to Reserved is not guaranteed. 0x0:No Preallocated Memory 0x1:2MB of Preallocated Memory 0x2:4MB of Preallocated Memory 0x3:8MB of Preallocated Memory

Bit Range	Default & Access	Field Name (ID): Description
5:3	0h RO	**Reserved**
2	0h RO/V	**VAMEN:** Enables the use of the iGFX engines for Versatile Acceleration. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h. 1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 038000h.
1	0h RO/V	**IVD:** 0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field (bits 7:3 of this register) pre-allocates no memory.
0	0h RO	**Reserved**

4.1.29 Mirror of Device Enable (DEVEN0_0_2_0_PCI) — Offset 54h

Mirror of DEVEN_0_0_0_PCI.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 54h	00BFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RO/V	**CHAP ENABLE (D7EN):**
13	0h RO	**DEVICE 6 ENABLE (D6EN):**
12:11	0h RO	**Reserved**
10	0h RO	**DEVICE 5 ENABLE (D5EN):**
9:8	0h RO	**Reserved**
7	1h RO/V	**DEVICE 4 ENABLE (D4EN):**
6	0h RO	**Reserved**
5	1h RO/V	**DEVICE 3 ENABLE FOR DISPLAY HD AUDIO (D3EN):**

Bit Range	Default & Access	Field Name (ID): Description
4	1h RO/V	**INTERNAL GRAPHICS ENGINE (D2EN):** 0: Bus 0 Device 2 is disabled and hidden1: Bus 0 Device 2 is enabled and visibleThis bit will be set to 0b and remain 0b if Device 2 capability is disabled.
3	1h RO/V	**PEG10 ENABLE (D1F0EN):**
2	1h RO/V	**PEG11 ENABLE (D1F1EN):**
1	1h RO/V	**PEG12 ENABLE (D1F2EN):**
0	1h RO	**HOST BRIDGE (D0EN):**

4.1.30 Device 2 Control (DEV2CTL_0_2_0_PCI) — Offset 58h

This register implements a control bit to disable and hide the IOBAR register in systems that do not require legacy IOBAR access to Gfx MMIO registers.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:2, F:0] + 58h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RO	**Reserved**
0	0h RW	**IOBAR DISABLE (IOBARDIS):** System BIOS can choose to disable and hide the IOBAR for systems that do not require legacy IOBAR access to Gfx MMIO registers.0b: IOBAR is enabled and exposed at offset 0x20 in Device 2 Configuration space. (Default)1b: IOBAR is disabled and not visible in PCI Configuration Space. Behaves as if hardwired to zeros.

4.1.31 Multi Size Aperture Control (MSAC_0_2_0_PCI) — Offset 60h

This register contains MSAC register which determines the size of the graphics memory aperture (GMADR) in function 0 and in the trusted space, and affects certain bits of the GMADR register. Bits [20:16] 00000b: 128MB, GMADR[26:4] is hardwired to all 0 Bits [20:16] 00001b: 256MB, GMADR[27:4] overriden to all 0 Bits [20:16] 00010b: illegal (hardware will treat this as 00011b) Bits [20:16] 00011b: 512MB, GMADR[28:27] overriden to all 0 Bits [20:16] 00100-00110b: illegal (hardware will treat this as 00111b) Bits [20:16] 00111b: 1024MB, GMADR[29:27] overriden to all 0 Bits [20:16] 01000-01110b: illegal (hardware will treat this as 01111b) Bits [20:16] 01111b: 2048MB, GMADR[30:27] overriden to all 0 Bits [20:16] 10000-11110b: illegal (hardware will treat this as 11111b) Bits [20:16] 11111b: 4096MB, GMADR[31:27] overriden to all 0

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 60h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RW/V	**UNTRUSTED APERTURE SIZE BIT 4 (APSZ4):**
19	0h RW/V	**UNTRUSTED APERTURE SIZE BIT 3 (APSZ3):**
18	0h RW/V	**UNTRUSTED APERTURE SIZE BIT 2 (APSZ2):**
17	0h RW/V	**UNTRUSTED APERTURE SIZE BIT 1 (APSZ1):**
16	0h RW/V	**UNTRUSTED APERTURE SIZE BIT 0 (APSZ0):**
15:0	0h RO	**Reserved**

4.1.32 PUSHAP_0_2_0_PCI — Offset 68h

GT writes this Push Aperture register to ensure aperture writes have been pushed to DRAM.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 68h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**TOKEN_VALUE:** 32 bit Token Value. GT (GuC) writes a Dword Token value to this field. A write to this register triggers a write response to GT. The response write will use the value written into this register.

4.1.33 VTd Status (VTD_STATUS_0_2_0_PCI) — Offset 6Ch

This register contains indicator bits for Graphics VTd mode.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:2, F:0] + 6Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RO	**Reserved**
0	0h RO	**GFX VTD ACTIVE (VTACT):** Reflects GFX VTd Mode is active. 1 - if active, 0 if inactive. Acts as R/W register only during Punit restore - when iommu freeze bit is set. RO otherwise

4.1.34 PCI Express Capability Header (PCIECAPHDR_0_2_0_PCI) — Offset 70h

PCI Express Capability Header

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 70h	AC10h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	ACh RO	**NEXT CAPABILITY POINTER (NEXT_PTR):** This field is hardwired to point to the next PCI Capability structure, the MSI Capabilities at ACh.
7:0	10h RO	**CAPABILITY IDENTIFIER (CAP_ID):** This field is hardwired to 10h to indicate that this is a PCI Express Capability structure.

4.1.35 PCI Express Capability (PCIECAP_0_2_0_PCI) — Offset 72h

PCI Express Capability

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 72h	0092h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**Reserved**
13:9	00h RO	**INTERRUPT MESSAGE NUMBER (INTRMSG):** This field indicates which MSI vector is used for the interrupt message generated in association with any of the status bits of this Capability structure.Since this device only supports one MSI vector, this field is hardwired to 0.
8	0h RO	**SLOT IMPLEMENTED (SLOTIMP):** This field is hardwired to 0 for an endpoint device.
7:4	9h RO	**DEVICE TYPE (DEV_TYPE):** This field is hardwired to 9h to indicate a Root Complex Integrated Endpoint.
3:0	2h RO	**CAPABILITY VERSION (CAP_VER):** This field is hardwired to 2h to indicate Functions compliant to PCI Express 3.0 Base Specification.

4.1.36 Device Capabilities (DEVICECAP_0_2_0_PCI) — Offset 74h

PCI Express Device Capabilities

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 74h	10008000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	1h RO	**FUNCTIONAL LEVEL RESET CAPABILITY (FLRCAP):** Hardwired to 1b to indicate the Function supports the optional Function Level Reset mechanism.
27:26	0h RO	**CAPTURED SLOT POWER LIMIT SCALE (PWR_LIM_SCALE):** Not applicable for a Root Complex Integrated Endpoint with no Link or Slot. Hardwired to 00b
25:18	00h RO	**CAPTURED SLOT POWER LIMIT VALUE (CSPLS):** Not applicable for a Root Complex Integrated Endpoint with no Link or Slot. Hardwired to 00h

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RO	**Reserved**
15	1h RO	**ROLE-BASED ERROR REPORTING (RBER):** When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1.Hardwired to 1b as this bit must be Set by all Functions conforming to the ECN, PCI Express Base Specification, Revision 1.1, or subsequent PCI Express Base Specification revisions.
14:12	0h RO	**Reserved**
11:9	0h RO	**ENDPOINT L1 ACCEPTABLE LATENCY (EPL1AL):** This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from the L1 state to the L0 state.This does not apply to the integrated graphics device, so it is hardwired to 000b (Maximum of 1 us).
8:6	0h RO	**ENDPOINT L0S ACCEPTABLE LATENCY (EPL0AL):** This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from the L0s state to the L0 state.This does not apply to the integrated graphics device, so it is hardwired to 000b (Maximum of 64 ns).
5	0h RO	**EXTENDED TAG FIELD SUPPORTED (ETFS):** This bit indicates the maximum supported size of the Tag field as a Requester.This does not apply to the integrated graphics device, so it is hardwired to 0b (5-bit Tag field supported).
4:3	0h RO	**PHANTOM FUNCTIONS SUPPORTED (PFS):** This field indicates the support for use of unclaimed Function Numbers to extend the number of outstanding transactions for PCIe devices.This does not apply to the integrated graphics device, so it is hardwired to 00b to indicate no Function Number bits are used for Phantom Functions.
2:0	0h RO	**MAX PAYLOAD SIZE SUPPORTED (MPSS):** This field indicates the maximum payload size that the Function can support for TLPs.Hardwired to 000b to represents 128 bytes, the minimum allowed value.

4.1.37 PCI Express Device Control (DEVICECTL_0_2_0_PCI) — Offset 78h

PCI Express Device Control

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 78h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/V	**INITIATE FUNCTION LEVEL RESET (INIT_FLR):** A write of 1b initiates Function Level Reset to the Function.During FLR, a read will return 1b since device 2 reads abort. If a local panel is powered on and configured to power down on reset, the FLR will typically take several hundred milliseconds to complete. The worst possible, although unrealistic, delay is 5 seconds.

Bit Range	Default & Access	Field Name (ID): Description
14:12	0h RO	**MAX READ REQUEST SIZE (MRRS):** Functions that do not generate Read Requests larger than 128 bytes and Functions that do not generate Read Requests on their own behalf are permitted to implement this field as Read Only (RO) with a value of 000b.
11	0h RO	**ENABLE NO SNOOP (ENS):** This bit is permitted to be hardwired to 0b if a Function would never Set the No Snoop attribute in transactions it initiates.The graphics device never generates a PCI Express TLP.
10	0h RO	**AUX POWER PM ENABLE (APPME):** Functions that do not implement this capability hardwire this bit to 0b.
9	0h RO	**PHANTOM FUNCTIONS ENABLE (PFE):** Functions that do not implement this capability hardwire this bit to 0b.
8	0h RO	**EXTENDED TAG FIELD ENABLE (ETFE):** Functions that do not implement this capability hardwire this bit to 0b.
7:5	0h RO	**MAX PAYLOAD SIZE (MPS):** Functions that support only the 128-byte max payload size are permitted to hardwire this field to 000b.
4	0h RO	**ENABLE RELAXED ORDERING (ERO):** A Function is permitted to hardwire this bit to 0b if it never sets the Relaxed Ordering attribute in transactions it initiates as a Requester.The graphics device never generates a PCI Express TLP.
3	0h RO	**UNSUPPORTED REQUEST RESPONSE ENABLE (URRE):** A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.
2	0h RW/V	**FATAL ERROR ENABLE (FEE):** This bit, in conjunction with other bits, controls sending ERR_FATAL Messages.
1	0h RW/V	**NON-FATAL ERROR ENABLE (NFEE):** This bit, in conjunction with other bits, controls sending ERR_NONFATAL Messages.
0	0h RW/V	**CORRECTABLE ERROR ENABLE (CEE):** This bit, in conjunction with other bits, controls sending ERR_COR Messages.

4.1.38 PCI Express Capability Structure (DEVICESTS_0_2_0_PCI) — Offset 7Ah

PCI Express Capability Structure

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 7Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**TRANSACTIONS PENDING (TP):** When Set, this bit indicates that the Function has issued Non-Posted Requests that have not been completed.A Function reports this bit is cleared only when all outstanding Non-Posted Requests have completed or have been terminated by the Completion Timeout mechanism. This bit must also be cleared upon the completion of an FLR.
4	0h RO	**AUX POWER DETECTED (APD):** Functions that require Aux power report this bit as Set if Aux power is detected by the Function. Hardwired to 0b, the integrated graphics device does not require Aux power.
3	0h RO	**UNSUPPORTED REQUEST DETECTED (URD):** This bit indicates the Function received an Unsupported Request.Hardwired to 0b, the Root Complex Integrated Endpoint graphics device does not use the PCI Express error reporting mechanism.
2	0h RW/V	**FATAL ERROR DETECTED (FED):** This bit indicates status of fatal errors detected. Errors are logged in this regsiter regardless of whether error reporting is enabled or not in the Device Control Register.
1	0h RW/V	**NON-FATAL ERROR DETECTED (NFED):** This bit indicates status of non fatal errors detected. Errors are logged in this regsiter regardless of whether error reporting is enabled or not in the Device Control Register.
0	0h RW/V	**CORRECTABLE ERROR DETECTED (CED):** This bit indicates status of correctable errors detected. Errors are logged in this regsiter regardless of whether error reporting is enabled or not in the Device Control Register.

4.1.39 Message Signaled Interrupts Capability ID (MSI_CAPID_0_2_0_PCI) — Offset ACh

When a device supports MSI it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + ACh	D005h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	D0h RO	**POINTER TO NEXT CAPABILITY (POINTNEXT):** This is a hardwired pointer to the next item in the capabilities list.
7:0	05h RO	**CAPABILITY ID (CAPID):** This field is hardwired to the value 05h to identify the CAP_ID as being for MSI registers.

4.1.40 Message Control (MC_0_2_0_PCI) — Offset AEh

Message Signaled Interrupt control register. System software can modify bits in this register, but the device is prohibited from doing so. If the device writes the same message multiple times, only one of those messages is guaranteed to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + AEh	0100h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	**Reserved**
8	1h RO	**PER VECTOR MASK CAPABLE (PVMASKCAP):** SR-IOV requires this capability.
7	0h RO	**64 BIT CAPABLE (CAP64B):** Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message address register and is incapable of generating a 64-bit memory address.
6:4	0h RW/V	**MULTIPLE MESSAGE ENABLE (MME):** System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested.Value: Number of requests000: 1001: 2010: 4011: 8100: 16101: 32110: Reserved111: Reserved
3:1	0h RO	**MULTIPLE MESSAGE CAPABLE (MMC):** System Software reads this field to determine the number of messages being requested by this device. Hardwired to 000b to indicate number of requests is 1.
0	0h RW/V	**MSI ENABLE (MSIEN):** Controls the ability of this device to generate MSIs.

4.1.41 Message Address (MA_0_2_0_PCI) — Offset B0h

This register contains the Message Address for MSIs sent by the device.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW/V	**MESSAGE ADDRESS FIELD (MESSADD):** Used by system software to assign an MSI address to the device.The device handles an MSI by writing the padded contents of the MD register to this address.
1:0	0h RO	**FORCE DWORD ALIGN (FDWORD):** Hardwired to 0 so that addresses assigned by system software are always aligned on a DWORD address boundary.

4.1.42 Message Data (MD_0_2_0_PCI) — Offset B4h

This register contains the Message Data for MSIs sent by the device.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + B4h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/V	**MESSDATA:** Base message data pattern assigned by system software and used to handle an MSI from the device.When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.

4.1.43 MSI Mask Bits (MSI_MASK_0_2_0_PCI) — Offset B8h

This register contains the MSI Mask Bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/V	**MASK BIT FOR VECTOR 0 (MASKBIT):** For each Mask bit that is set, the function is prohibited from sending the associated message.

4.1.44 MSI Pending Bits (MSI_PEND_0_2_0_PCI) — Offset BCh

This register contains the MSI Pending Bits

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + BCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**PENDING BIT FOR VECTOR 0 (PENDBIT):** For each Pending bit that is set, the function has a pending associated message. If this bit is set when the corresponding vector's Mask bit is cleared, the function will send an MSI and then clear the Pending bit.

4.1.45 Mirror of Base Data of Stolen Memory (BDSM0_0_2_0_PCI) — Offset C0h

Mirror of BSDM from GTTMMADR space. This register contains the base address of graphics data stolen DRAM memory.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RO/V	**GRAPHICS BASE OF STOLEN MEMORY LSB (BDSM_LSB):** This register contains bits 63 to 20 of the base address of stolen DRAM memory. BIOS is now able to allocate GDSM above 4GB.
19:0	0h RO	**Reserved**

4.1.46 Mirror of Base Data of Stolen Memory (BDSM1_0_2_0_PCI) — Offset C4h

Mirror of BSDM from GTTMMADR space. This register contains the base address of graphics data stolen DRAM memory.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**GRAPHICS BASE OF STOLEN MEMORY MSB (BDSM_MSB):** This register contains bits 63 to 20 of the base address of stolen DRAM memory. BIOS is now able to allocate GDSM above 4GB.

4.1.47 GFXVTDBAR_LSB_0_2_0_PCI — Offset C8h

This is the base address for the Graphics VTD configuration space. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the GFX-VTD configuration space is disabled and must be enabled by writing a 1 to GFXVTDBAREN. None of the bits in this register are writeable in Intel TXT mode. This enforcement is based on SAI policy registers. BIOS programs this register, after which the register cannot be altered. This register is only written via an SAI in the appropriate policy group.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**GFXVTDBAR:** This field corresponds to bits 31 to 12 of the base address GFX-VTD configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the GFX-VTD register set. All the Bits in this register are included in an SAI policy group for Intel TXT mode purposes.
11:1	0h RO	**Reserved**
0	0h RW/V	**GFXVTDBAREN:** 0: GFX-VTBAR is disabled and does not claim any memory. 1: GFX-VTBAR memory mapped accesses are claimed and decoded appropriately This bit will remain 0 if VTd capability is disabled.

4.1.48 GFXVTDBAR_MSB_0_2_0_PCI — Offset CCh

This is the base address for the Graphics VTD configuration space. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the GFX-VTD configuration space is disabled and must be enabled by writing a 1 to GFXVTDBAREN. All the bits in this register are included in an SAI protection group for Intel TXT mode. BIOS programs this register, after which the register cannot be altered.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GFXVTDBAR:** This field corresponds to bits 63 to 32 of the base address GFX-VTD configuration space. BIOS will program this register, resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the GFX-VTD register set. All the Bits in this register are included in an SAI policy group for Intel TXT mode.

4.1.49 Power Management Capabilities ID (PMCAPID_0_2_0_PCI) — Offset D0h

This register contains the PCI Power Management Capability ID and the next capability pointer.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + D0h	0001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RO	**NEXT CAPABILITY POINTER (NEXT_PTR):** This is a hardwired pointer to the next item in the capabilities list.
7:0	01h RO	**CAPABILITY IDENTIFIER (CAP_ID):** Hardwired to 01h for power management.

4.1.50 Power Management Capabilities (PMCAP_0_2_0_PCI) — Offset D2h

This register provides information on the capabilities of the function related to powermanagement.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + D2h	0022h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:11	00h RO	**PME SUPPORT (PMES):** This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.
10	0h RO	**D2 SUPPORT (D2):** Hardwired to 0 to indicate the D2 power management state is not supported.
9	0h RO	**D1 SUPPORT (D1):** Hardwired to 0 to indicate that the D1 power management state is not supported.
8:6	0h RO	**Reserved**
5	1h RO	**DEVICE SPECIFIC INITIALIZATION (DSI):** Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**Reserved**
3	0h RO	**PME CLOCK (PMECLK):** Hardwired to 0 to indicate IGD does not support PME# generation.
2:0	2h RO	**VER:** Hardwired to 010b to indicate that there are 4 bytes of power management registers implemented and that this device complies with revision 1.1 of the PCI Power Management Interface Specification.

4.1.51 Power Management Control and Status (PMCS_0_2_0_PCI) — Offset D4h

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + D4h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**PME STATUS (PMESTS):** This bit is hardwired to 0 to indicate that IGD does not support PME# generation from D3 (cold).
14:13	0h RO	**DATA SCALE (DSCALE):** This field is hardwired to 00 to indicate IGD does not support data register.
12:9	0h RO	**DATA SELECT (DSEL):** This field is hardwired to 0h to indicate IGD does not support data register.
8	0h RO	**PME ENABLE (PMEEN):** This bit is hardwired to 0 to indicate that PME# assertion from D3 (cold) is disabled.
7:2	0h RO	**Reserved**
1:0	0h RW/V	**POWER STATE (PWRSTAT):** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. Behavior of the graphics controller in supported states is detailed in the power management section of the Bspec.Bits[1:0]Power state00:D0Default01:D1Not Supported10:D2Not Supported11:D3

4.1.52 Software SMI (SWSMI_0_2_0_PCI) — Offset E0h

As long as there is the potential that DVO port legacy drivers exist which expect this register at this address, Dev#2F0address E0h-E1h must be reserved for this register.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + E0h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RW	**SOFTWARE SCRATCH BITS (SWSB):**
7:1	00h RW	**SOFTWARE FLAG (SWF):** Used to indicate caller and SMI function desired, as well as return result.
0	0h RW	**GMCH SOFTWARE SMI EVENT (GSSMIE):** When Set this bit will trigger an SMI. Software must write a '0' to clear this bit.SMI will be triggered only if SWSCI[SMISCISEL] is set to select SMI.

4.1.53 Graphics System Event (GSE_0_2_0_PCI) — Offset E4h

This register can be accessed by either Byte, Word, or Dword PCI config cycles. A write to this register will cause the Graphics System Event display interrupt if it is enabled and unmasked in the display interrupt registers.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**GSE SCRATCH TRIGGER 3 (GSE3):**
23:16	00h RW	**GSE SCRATCH TRIGGER 2 (GSE2):**
15:8	00h RW	**GSE SCRATCH TRIGGER 1 (GSE1):**
7:0	00h RW	**GSE SCRATCH TRIGGER 0 (GSE0):**

4.1.54 Software SCI (SWSCI_0_2_0_PCI) — Offset E8h

This register serves 2 purposes: 1) Support selection of SMI or SCI event source (SMISCISEL - bit15) 2) SCI Event trigger (GSSCIE - bit 0). To generate a SW SCI event, software should program bit 15 (SMISCISEL) to 1. This is typically programmed once (assuming SMIs are never triggered). On a '0' to '1' subsequent transition in bit 0

of this register (caused by a software write operation), a SCI message will be sent to cause the TCOSCI_STS bit in GPE0 register to be set to 1. The corresponding SCI event handler in BIOS is to be defined as a _Lxx method, indicating level trigger to the operating system. Once written as 1, software must write a '0' to this bit to clear it, and all other write transitions (1-0, 0-0, 1-1) will not cause a SCI message to be sent. To generate a SW SMI event, software should program bit 15 to 0 and trigger SMI via writes to SWSMI register (See SWSMI register for programming details).

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + E8h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**SMI OR SCI EVENT SELECT (SMISCISEL):** 0 = SMI (default)1 = SCI If selected event source is SMI, SMI trigger and associated scratch bits accesses are performed via SWSMI register. If SCI event source is selected, the rest of the bits in this register provide SCI trigger capability and associated SW scratch pad area.
14:1	0000h RW	**SOFTWARE SCRATCH BITS (SCISB):** Read/write bits not used by hardware.
0	0h RW	**SOFTWARE SCI EVENT (GSSCIE):** If SCI event is selected (SMISCISEL = 1), on a 0 to 1 transition of GSSCIE bit, a SCI message will be sent to cause the TCOSCI_STS bit in GPE0 register to be set to 1. Software must write a 0 to clear this bit.

4.1.55 Dev2 Mirror of Protected Audio Video Path Control (PAVPC0_0_2_0_PCI) — Offset F0h

Device 2 Mirror of Protected Audio Video Control.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RO/V	**WOPCM BASE LSB (WOPCMBASE_LSB):** Base value programmed (from Top of Stolen Memory). The programmed value must be consistent with the WOPCM Size programming.
19:9	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RO/V	**WOPCM SIZE (WOPCMSIZE):** This register determines the WOPCM size. The programmed value must be consistent with the WOPCM base programming. 00b: 1MB (default) 01b: 2MB 10b: 4MB 11b: 8MB
6	0h RO/V	**ASMF METHOD ENABLE (ASMFEN):** 0: Disable ASMF 1: Enable ASMF
5	0h RO	**Reserved**
4	0h RO/V	**OVERRIDE TERMINATE ATTACK (OVTATTACK):** Override of unsolicited connection state attack and terminate 0: Disable override; attack terminate allowed 1: Enable override; attack terminate disallowed
3	0h RO/V	**HEAVY MODE SELECT (HVYMODSEL):** Heavy/light encryption mode select 0: Surface encryption is disabled - Light mode 1: Surface encryption is enabled
2	0h RO/V	**LOCK:** BIOS will set this bit with bit 0 and/or bit 1.
1	0h RO/V	**PAVP ENABLE (PAVPE):** 0: PAVP functionality disabled 1: PAVP functionality enabled
0	0h RO/V	**PCM ENABLE (PCME):** Protected content memory enable.

4.1.56 Dev2 Mirror of Protected Audio Video Path Control (PAVPC1_0_2_0_PCI) — Offset F4h

Device 2 Mirror of Protected Audio Video Control.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + F4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**WOPCM BASE MSB (WOPCMBASE_MSB):** Base value programmed (from Top of Stolen Memory). The programmed value must be consistent with the WOPCM Size programming.

4.1.57 Stepping Revision ID (SRID_0_2_0_PCI) — Offset F8h

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + F8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RO	**STEPPING REVISION ID MSB (SRID_MSB):** The four MSB of the stepping revision ID
19:16	0h RO	**STEPPING REVISION ID LSB (SRID_LSB):** Those are the four LSB of SRID as set by fuses
15:0	0h RO	**Reserved**

4.1.58 ASL Storage (ASLS_0_2_0_PCI) — Offset FCh

This is a software scratch register. The exact bit register usage must be worked out in common between System BIOS and driver software. For each device, the ASL control method requires two bits for DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for DGS (enable/disable requested), and two bits for DCS (enabled now/disabled now, connected or not).

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + FCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**DEVICE SWITCHING STORAGE (DSS):** Software controlled usage to support device switching.

4.1.59 PASID Extended Capability Header (PASID_EXTCAP_0_2_0_PCI) — Offset 100h

PASID capability reports support for Process Address Space ID(PASID) on Device-2, compliant to PCI-Express PASID ECN.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 100h	2001001Bh

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	200h RO	**NEXT CAPABILITY OFFSET (NCO):** This is a hardwired pointer to the next item in the capabilities list.
19:16	1h RO	**V:** Hardwired to capability version 1.
15:0	001Bh RO	**CAPABILITY ID (CAPID):** Hardwired to the PASID Extended Capability ID

4.1.60 PASID Capability (PASID_CAP_0_2_0_PCI) — Offset 104h

PASID capability reports support for Process Address Space ID(PASID) on Device-2, compliant to PCI-Express PASID ECN.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 104h	1400h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	**Reserved**
12:8	14h RO	**MAXIMUM PASID WIDTH (MPW):** Indicates the width of the PASID field supported by the Endpoint. Hardwired to 14h to indicate support for all PASID values (20 bits).
7:3	0h RO	**Reserved**
2	0h RO	**PRIVILEGE MODE SUPPORTED (PMS):** Hardwired to 0, the Endpoint supports operating in Non-privileged mode only, and will never request privileged mode in requests-with-PASID.
1	0h RO	**EXECUTE PERMISSION SUPPORTED (EPS):** Hardwired to 0, the Endpoint supports requests-with-PASID that requests execute permission.
0	0h RO	**Reserved**

4.1.61 PASID Control (PASID_CTRL_0_2_0_PCI) — Offset 106h

Process Address Space ID (PASID) control for Device-2.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 106h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2	0h RO	**PRIVILEGED MODE ENABLE (PME):** Hardwired to 0, the Endpoint is not permitted to request privileged mode in requests-with-PASID.
1	0h RW	**EXECUTE PERMISSION ENABLE (EPE):** If Set, the Endpoint is permitted to request execute permission in requests-with-PASID. If Clear, the Endpoint is not permitted to do so. Behavior is undefined if this bit changes value when ATS Enable field in ATS Capability is Set.Processor graphics does not use this field. Software is expected to Set this field before configuring extended-context-entry for Device-2 with the Execute Request Enable field Set.
0	0h RW	**PASID ENABLE (PE):** If Set, the Endpoint is permitted to generate requests-with-PASID. If Clear, the Endpoint is not permitted to do so. Behavior is undefined if this bit changes value when ATS Enable field in ATS Capability is Set. If Priviliged Mode Supported field in PASID Capability register is Clear, then this field is treated as Reserved(0).Processor graphics does not use this field. Software is expected to Set this field before configuring extended-context-entry for Device-2 with Supervisor Request Enable field Set. For compatibility reasons, this field is implemented as RW.

4.1.62 ATS Extended Capability Header (ATS_EXTCAP_0_2_0_PCI) — Offset 200h

ATS Capability reports support for Device-TLBs on Device-2, compliant to PCI Express ats specification.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 200h	3001000Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	300h RO	**NEXT CAPABILITY OFFSET (NCO):** This is a hardwired pointer to the next item in the capabilities list. Value 300h in this field provides the offset for Page-Request Capability.
19:16	1h RO	**V:** Hardwired to capability version 1.
15:0	000Fh RO	**CAPABILITY ID (CAPID):** Hardwired to the ATS Extended Capability ID

4.1.63 ATS Capability (ATS_CAP_0_2_0_PCI) — Offset 204h

ATS Capability reports support for Device-TLBs on Device-2, compliant to PCI Express ATS specification.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 204h	0060h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:7	0h RO	**Reserved**
6	1h RO	**GLOBAL INVALIDATE SUPPORTED (GIS):** If Set, the Function supports Invalidation Requests that have the Global Invalidate bit Set. If Clear, the Function ignores the Global Invalidate bit in all Invalidate requests.Reserved
5	1h RO	**PAGE ALIGNED REQUEST (PAR):** Hardwired to 1, the Untranslated Address is always aligned to a 4096 byte boundary. Processor Graphics reports value of 1b indicating all VT-d and SVM translations are page-aligned.
4:0	00h RO	**INVALIDATE QUEUE DEPTH (IQE):** The number of Invalidate Requests that the endpoint can accept before putting back pressure on the upstream connection. Hardwired to 0h, the function can accept 32 Invalidate Requests.

4.1.64 ATS Control (ATS_CTRL_0_2_0_PCI) — Offset 206h

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 206h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**ATS ENABLE (AE):** When Set, the function is enabled to cache translations. Processor graphics ignores this field, as GT uses GTLB as IOTLB and only pretends to software that it has a Device-TLB. Software is expected to Set this field before configuring extended context-entry for Device2 with Page Request Enable field Set. For compatibility, this field is implemeted as RW as software can read it to determine ATS enable status.
14:5	0h RO	**Reserved**
4:0	00h RW	**SMALLEST TRANSLATION UNIT (STU):** This value indicates to the Endpoint the minimum number of 4096-byte blocks that is indicated in a Translation Completion or Invalidate Request. This is a power of 2 multiple and the number of blocks is 2^STU. A value of 0 indicates one block and value 1F indicates 2^31 blocks. For IGD this must be programmed to 0h for 4KB as smallest translation unit.

4.1.65 Page Request Extended Capability Header (PR_EXTCAP_0_2_0_PCI) — Offset 300h

Page Request Extended Capability reports support for page-faults on Device-2, compliant to PCI-Express ATS 1.1 Specification

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 300h	00010013h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RO/V	**NEXT CAPABILITY OFFSET (NCO):** This is a hardwired pointer to the next item in the capabilities list. Value 000h (Default) indicates that this is the end of the PCI-Express Extended capability Linked List. When Graphics Virtualization is enabled, this field is hardwired to point to the next PCI Capability structure, the SRIOV Extended Capability Header at 320h. When Graphics Virtualization is disabled, this field will be hardwired to 000h to indicate the end of PCI-Express Extended capability Linked List.
19:16	1h RO	**V:** Hardwired to capability version 1.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0013h RO	**CAPABILITY ID (CAPID):** Hardwired to the Page Request Extended Capability ID

4.1.66 Page Request Control (PR_CTRL_0_2_0_PCI) — Offset 304h

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 304h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**
1	0h RO	**RST:** When the Enable field is clear, or is being cleared in the same register update that sets this field, writing a 1b to this field, clears the associated implementation dependent page request credit Counter and pending request state for the associated Page Request Interface. No action is initiated if this field is written to 0b or if this field is written with any value when the PRE field is set. Processor graphics does not use this field, and hardwires it as read-only (0).
0	0h RW	**PAGE-REQUEST ENABLE (PRE):** When Set, indicates that the page request interface on the endpoint is allowed to make page requests. If both this field and the Stopped field in Page Request Status register are Clear, then the Page request interface will not issue new page requests, but has outstanding page requests for which page responses is not yet received. When this field transitions from 0 to 1, all the status fields in the Page-Request Status register are cleared. Enabling a page request interface that has not successfully stopped has indeterminate results.

4.1.67 Page Request Status (PR_STATUS_0_2_0_PCI) — Offset 306h

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 306h	8100h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	1h RO	**PRG RESPONSE PASID REQUIRED (PRPR):** If set, the Function expects a PASID TLP Prefix on PRG Response Messages when the corresponding page requests had a PASID TLP Prefix. If Clear, the function does not expect PASID TLP Prefixes on any PRG Response Message. Function behavior is undefined if this bit is Clear and the Function receives a PRG Response Message with a PASID TLP Prefix. Function behavior is undefined if this bit is Set and the Function receives a PRG Response Message with no PASID TLP Prefix when the corresponding Page Requests had a PASID TLP Prefix. This bit is RsvdZ if the Function does not support the PASID TLP Prefix.
14:9	0h RO	**Reserved**
8	1h RO	**S:** When this field is Set, the associated page request interface has stopped issuing additional Page requests and that all previously issued Page requests have completed. When this field is clear the associate Page request interface either has not stopped or has stopped issuing new Page requests but has outstanding Page requests.
7:2	0h RO	**Reserved**
1	0h RW/V	**UNEXPECTED PAGE REQUEST GROUP INDEX (UPGRI):** When Set, indicates the function received a PRG response message containing a PRG index that has no matching request, a response failure. This field is Set by the Function and cleared when a 1b is written to the field.
0	0h RW/V	**RESPONSE FAILURE (RF):** When Set, indicates the function received a PRG response message indicating a response failure. The function expects no further response from the host (any received are ignored). This field is Set by the Function and cleared when a 1b is written to this field.

4.1.68 Outstanding Page Request Capacity (OPRC_0_2_0_PCI) — Offset 308h

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 308h	00008000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00008000h RO	**OUTSTANDING PAGE REQUEST CAPACITY (OPRC):** This register contains the number of outstanding page request messages the associated Page Request Interface physically supports. This is the upper limit on the number of pages that can be usefully allocated to the Page Request Interface. Hardwired to 32,768 requests.

4.1.69 Outstanding Page Request Allocation (OPRA_0_2_0_PCI) — Offset 30Ch

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 30Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**OUTSTANDING PAGE REQUEST ALLOCATION (OPRA):** This register contains the number of outstanding page request messages the associated Page Request Interface is allowed to issue.

4.1.70 SRIOV Extended Capability Header (SRIOV_ECAPHDR_0_2_0_PCI) — Offset 320h

SR-IOV Extended Capability Header.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 320h	00010010h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RO	**NEXT CAPABILITY OFFSET (NEXT_0):** Next capability Offset. Value = 0x000 to indicate the end of the Extended Capability List
19:16	1h RO	**CAPABILITY VERSION (CAP_VER):** Capability Version
15:0	0010h RO	**PCIE EXTENDED CAPABLITY ID (PCIE_ECAP_ID):** PCIE Extended Capablity ID

4.1.71 SRIOV Capabilities (SRIOV_CAP_0_2_0_PCI) — Offset 324h

Defines SR-IOV Capabilities

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 324h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:21	000h RO	**VF MIGRATION INTERRUPT MESSAGE NUMBER (VF_MIG_INTR_MSG_NUM):** Value: 0. VF Migration is not supported.
20:2	0h RO	**Reserved**
1	0h RO	**ARI CAPABLE HIERARCHY PRESERVED (ARI_CAP_HIER_PRESERVED):** Value: 0. ARI not supported.
0	0h RO	**VF MIGRATION CAPABLE (VF_MIG_CAP):** Value:0. VF Migration not supported.

4.1.72 SRIOV Status (SRIOV_STS_0_2_0_PCI) — Offset 32Ah

SR-IOV Status Register.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 32Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:1	0h RO	**Reserved**
0	0h RO	**VF MIGRATION STATUS (VF_MIG_STS):** VF Migration Status

4.1.73 SRIOV Initial VFs (SRIOV_INITVFS_0_2_0_PCI) — Offset 32Ch

Defines Initial number of VFs available to the VMM.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 32Ch	0007h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	0007h RO/V	**INITIAL VFS (INITIAL_VFS):** For SR-IOV implementation, this value must exactly match the Total VFs

4.1.74 SRIOV Total VFs (SRIOV_TOTVFS_0_2_0_PCI) — Offset 32Eh

Defines the Total number of VFs available to the VMM.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 32Eh	0007h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	0007h RO	**TOTAL VFS (TOTAL_VFS):** Indicates the maximum number of VFs that could be associated with the PF

4.1.75 First VF Offset (FIRST_VF_OFFSET_0_2_0_PCI) — Offset 334h

Defines the offset of the function number from the PF to the first VF.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 334h	0001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	0001h RO	**FIRST VF OFFSET VALUE (FIRST_VF_OFFSET):** Defines the routing ID offset of the first VF that is associated with the PF that contains this Capability structure. The first VFs 16-bit Routing ID is calculated by adding the contents of this field to the Routing ID of the PF containing this field ignoring any carry, using unsigned, 16-bit arithmetic. The value of this field is hardwired to 0001h.

4.1.76 VF Stride (VF_STRIDE_0_2_0_PCI) — Offset 336h

Defines the stride of the function number from one VF to the next.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 336h	0001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	0001h RO	**VF STRIDE VALUE (VF_STRIDE):** Defines the Routing ID offset from one VF to the next one for all VFs associated with the PF that contains this Capability structure. The next VFs 16-bit Routing ID is calculated by adding the contents of this field to the Routing ID of the current VF, ignoring any carry, using unsigned 16-bit arithmetic. The value of this field is hardwired to 0001h.

4.1.77 VF Device ID (VF_DEVICEID_0_2_0_PCI) — Offset 33Ah

Defines the Device ID to be used by all Virtual Functions

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:2, F:0] + 33Ah	9A40h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	9A40h RO/V	**VF DEVICE ID VALUE (VF_DEVICEID):** Mirror the same device ID as the PF

4.1.78 Supported Page Sizes (SUPPORTED_PAGE_SIZES_0_2_0_PCI) — Offset 33Ch

Defines the System Page Sizes supported by this SR-IOV implementation.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 33Ch	00000553h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000553h RO	**SUPPORTED PAGE SIZES VALUE (PAGE_SIZES):** This field indicates the page sizes supported by the PF. This PF supports a page size of 2^(n+12) if bit n is Set. For example, if bit 0 is Set, the PF supports 4-KB page sizes. PFs are required to support 4-KB, 8-KB, 64-KB, 256-KB, 1-MB, and 4-MB page sizes. All other page sizes are optional, and not supported in this implementation.

4.1.79 System Page Sizes (SYSTEM_PAGE_SIZES_0_2_0_PCI) — Offset 340h

Defines the System Page Size chosen by the VMM.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 340h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000001h RO	**SYSTEM PAGE SIZES VALUE (SYS_PAGE_SIZES):** This field defines the page size the system will useto map the VFs memory addresses. Software must set the value of the System Page Size to one of the page sizes set in the Supported Page Sizes field. As with Supported Page Sizes, if bit nis Set in System Page Size, the VFs associated with this PF are required to support a page size of 2^(n+12). For example, if bit 1 is Set, the system is using an 8-KB page size. The results are undefined if System Page Size is zero. The results are undefined if more than one bit is set in System Page Size. The results are undefined if a bit is Set in System Page Size that is not Set in Supported Page Sizes. When System Page Size is set, the VF associated with this PF is required to align all BAR resources 20 on a System Page Size boundary. Each VF BARn or VF BARn pair shall be aligned on a System Page Size boundary. Each VF BARn or VF BARn pair defining a non-zero address space shall be sized to consume an integer multiple of System Page Size bytes. All data structures requiring page size alignment within a VF shall be aligned on a System Page Size boundary. VF Enable must be zero when System Page Size is written. The results are undefined if System Page Size is written when VF Enable is Set. Default value is 1h (i.e., 4 KB), and that is the only value allowed for this implementation

4.1.80 VF BAR0 LDW (VF_BAR0_LDW_0_2_0_PCI) — Offset 344h

Lower DW of the BAR that defines the base Host Physical Address (HPA) of GTTMMADR for all VFs. The HPA of the GTTMMADR for Virtual Function n = VF GTTMMADDR (Upper and Lower DW) + (n - 1) * (16MB * num Tiles)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 344h	00000004h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW/V	**VF GTTMMADDR LOWER DW (VF_GTTMMADDR_LDW):** VF GTTMMADDR Lower DW
23:4	00000h RO	**VF GTTMMADDR LOWER DW MASK (VF_GTTMMADDR_LDW_MASK):** VF GTTMMADDR Lower DW Mask
3	0h RO	**PREFETCHABLE:** Prefetchable
2:1	2h RO	**BAR_TYPE:** Type. Value 10 indicates 64 bit BAR
0	0h RO	**MEMORY SPACE INDICATOR (MEM_SPACE_IND):** Memory space Indicator. Value 0 indicates memory space.

4.1.81 VF BAR0 UDW (VF_BAR0_UDW_0_2_0_PCI) — Offset 348h

Upper DW of the BAR that defines the base Host Physical Address of the GTTMMADR for all VFs

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 348h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**VF GTTMMADDR UPPER DWORD (VF_GTTMMADDR_UDW):** VF GTTMMADDR Upper DW

4.1.82 VF BAR1 LDW (VF_BAR1_LDW_0_2_0_PCI) — Offset 34Ch

Lower DW of the BAR that defines the base Host Physical Address of GMADR for all VFs.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 34Ch	0000000Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW/V	**VF GMADDR LOWER DW (VF_GMADDR_LDW):** VF GMADDR Lower DW
28:4	0000000h RO	**VF GMADDR LOWER DW MASK (VF_GMADDR_LDW_MASK):** VF GMADDR Lower DW Mask
3	1h RO	**PREFETCHABLE:** Prefetchable
2:1	2h RO	**BAR_TYPE:** Type. Value 10 indicates 64 bit BAR
0	0h RO	**MEMORY SPACE INDICATOR (MEM_SPACE_IND):** Memory space Indicator. Value 0 indicates memory space.

4.1.83 VF BAR1 UDW (VF_BAR1_UDW_0_2_0_PCI) — Offset 350h

Upper DW of the BAR that defines the base Host Physical Address of GMADR for all VFs

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:2, F:0] + 350h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW/V	**VF GMADDR UPPER DWORD (VF_GMADDR_UDW):** VF GMADDR Upper DW

4.1.84 VF BAR2 LDW (VF_BAR2_LDW_0_2_0_PCI) — Offset 354h

Lower DW of Unused BAR

Note: **NOTE:** Bit definitions are the same as CAPID0_B_0_2_0_PCI, offset 48h.

4.1.85 VF BAR2 UDW (VF_BAR2_UDW_0_2_0_PCI) — Offset 358h

Upper DW of Unused BAR

Note: **NOTE:** Bit definitions are the same as CAPID0_B_0_2_0_PCI, offset 48h.

4.1.86 VF Migration State Array Offset (VF_MIGST_OFFSET_0_2_0_PCI) — Offset 35Ch

Defines offset from a PF BAR to the VF Migration State Array. VF Migration not supported in this implementation

Note: Bit definitions are the same as CAPID0_B_0_2_0_PCI, offset 48h.

4.2 Graphics VT BAR (GFXVTBAR) Registers

This section contains the GFXVTBAR registers. Base address of these registers are defined in the GFXVTBAR_0_0_0_MCHBAR_NCU register which resides in the MCHBAR register collection.

4.2.1 Summary of Registers

Table 4-3. Summary of GFXVTBAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Version Register (VER_REG_0_0_0_VTDBAR)	00000040h
8h	8	Capability Register (CAP_REG_0_0_0_VTDBAR)	09C0000C406F0466h
10h	8	Extended Capability Register (ECAP_REG_0_0_0_VTDBAR)	0000079E2FF050DFh
18h	4	Global Command Register (GCMD_REG_0_0_0_VTDBAR)	00000000h
1Ch	4	Global Status Register (GSTS_REG_0_0_0_VTDBAR)	00000000h
20h	8	Root Table Address Register (RTADDR_REG_0_0_0_VTDBAR)	0000000000000000h
28h	8	Context Command Register (CCMD_REG_0_0_0_VTDBAR)	0800000000000000h
34h	4	Fault Status Register (FSTS_REG_0_0_0_VTDBAR)	00000000h
38h	4	Fault Event Control Register (FECTL_REG_0_0_0_VTDBAR)	80000000h
3Ch	4	Fault Event Data Register (FEDATA_REG_0_0_0_VTDBAR)	00000000h
40h	4	Fault Event Address Register (FEADDR_REG_0_0_0_VTDBAR)	00000000h
44h	4	Fault Event Upper Address Register (FEUADDR_REG_0_0_0_VTDBAR)	00000000h
58h	8	Advanced Fault Log Register (AFLOG_REG_0_0_0_VTDBAR)	0000000000000000h
64h	4	Protected Memory Enable Register (PMEN_REG_0_0_0_VTDBAR)	00000000h
68h	4	Protected Low Memory Base Register (PLMBASE_REG_0_0_0_VTDBAR)	00000000h
6Ch	4	Protected Low-Memory Limit Register (PLMLIMIT_REG_0_0_0_VTDBAR)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
70h	8	Protected High-Memory Base Register (PHMBASE_REG_0_0_0_VTDBAR)	0000000000000000h
78h	8	Protected High-Memory Limit Register (PHMLIMIT_REG_0_0_0_VTDBAR)	0000000000000000h
80h	8	Invalidation Queue Head Register (IQH_REG_0_0_0_VTDBAR)	0000000000000000h
88h	8	Invalidation Queue Tail Register (IQT_REG_0_0_0_VTDBAR)	0000000000000000h
90h	8	Invalidation Queue Address Register (IQA_REG_0_0_0_VTDBAR)	0000000000000000h
9Ch	4	Invalidation Completion Status Register (ICS_REG_0_0_0_VTDBAR)	00000000h
A0h	4	Invalidation Event Control Register (IECTL_REG_0_0_0_VTDBAR)	80000000h
A4h	4	Invalidation Event Data Register (IEDATA_REG_0_0_0_VTDBAR)	00000000h
A8h	4	Invalidation Event Address Register (IEADDR_REG_0_0_0_VTDBAR)	00000000h
ACh	4	Invalidation Event Upper Address Register (IEUADDR_REG_0_0_0_VTDBAR)	00000000h
B8h	8	Interrupt Remapping Table Address Register (IRTA_REG_0_0_0_VTDBAR)	0000000000000000h
C0h	8	Page Request Queue Head Register (PQH_REG_0_0_0_VTDBAR)	0000000000000000h
C8h	8	Page Request Queue Tail Register (PQT_REG_0_0_0_VTDBAR)	0000000000000000h
D0h	8	Page Request Queue Address Register (PQA_REG_0_0_0_VTDBAR)	0000000000000000h
DCh	4	Page Request Status Register (PRS_REG_0_0_0_VTDBAR)	00000000h
E0h	4	Page Request Event Control Register (PECTL_REG_0_0_0_VTDBAR)	80000000h
E4h	4	Page Request Event Data Register (PEDATA_REG_0_0_0_VTDBAR)	00000000h
E8h	4	Page Request Event Address Register (PEADDR_REG_0_0_0_VTDBAR)	00000000h
ECh	4	Page Request Event Upper Address Register (PEUADDR_REG_0_0_0_VTDBAR)	00000000h
100h	8	MTRR Capability Register (MTRRCAP_0_0_0_VTDBAR)	0000000000000000h
108h	8	MTRR Default Type Register (MTRRDEFAULT_0_0_0_VTDBAR)	0000000000000000h
120h	8	Fixed-Range MTRR Format 64K-00000 (MTRR_FIX64K_00000_REG_0_0_0_VTDBAR)	0000000000000000h
128h	8	Fixed-Range MTRR Format 16K-80000 (MTRR_FIX16K_80000_REG_0_0_0_VTDBAR)	0000000000000000h
130h	8	Fixed-Range MTRR Format 16K-A0000 (MTRR_FIX16K_A0000_REG_0_0_0_VTDBAR)	0000000000000000h
138h	8	Fixed-Range MTRR Format 4K-C0000 (MTRR_FIX4K_C0000_REG_0_0_0_VTDBAR)	0000000000000000h
140h	8	Fixed-Range MTRR Format 4K-C8000 (MTRR_FIX4K_C8000_REG_0_0_0_VTDBAR)	0000000000000000h
148h	8	Fixed-Range MTRR Format 4K-D0000 (MTRR_FIX4K_D0000_REG_0_0_0_VTDBAR)	0000000000000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
150h	8	Fixed-Range MTRR Format 4K-D8000 (MTRR_FIX4K_D8000_REG_0_0_0_VTDBAR)	0000000000000000h
158h	8	Fixed-Range MTRR Format 4K-E0000 (MTRR_FIX4K_E0000_REG_0_0_0_VTDBAR)	0000000000000000h
160h	8	Fixed-Range MTRR Format 4K-E8000 (MTRR_FIX4K_E8000_REG_0_0_0_VTDBAR)	0000000000000000h
168h	8	Fixed-Range MTRR Format 4K-F0000 (MTRR_FIX4K_F0000_REG_0_0_0_VTDBAR)	0000000000000000h
170h	8	Fixed-Range MTRR Format 4K-F8000 (MTRR_FIX4K_F8000_REG_0_0_0_VTDBAR)	0000000000000000h
180h	8	Variable-Range MTRR Format Physical Base 0 (MTRR_PHYSBASE0_REG_0_0_0_VTDBAR)	0000000000000000h
188h	8	Variable-Range MTRR Format Physical Mask 0 (MTRR_PHYSMASK0_REG_0_0_0_VTDBAR)	0000000000000000h
190h	8	Variable-Range MTRR Format Physical Base 1 (MTRR_PHYSBASE1_REG_0_0_0_VTDBAR)	0000000000000000h
198h	8	Variable-Range MTRR Format Physical Mask 1 (MTRR_PHYSMASK1_REG_0_0_0_VTDBAR)	0000000000000000h
1A0h	8	Variable-Range MTRR Format Physical Base 2 (MTRR_PHYSBASE2_REG_0_0_0_VTDBAR)	0000000000000000h
1A8h	8	Variable-Range MTRR Format Physical Mask 2 (MTRR_PHYSMASK2_REG_0_0_0_VTDBAR)	0000000000000000h
1B0h	8	Variable-Range MTRR Format Physical Base 3 (MTRR_PHYSBASE3_REG_0_0_0_VTDBAR)	0000000000000000h
1B8h	8	Variable-Range MTRR Format Physical Mask 3 (MTRR_PHYSMASK3_REG_0_0_0_VTDBAR)	0000000000000000h
1C0h	8	Variable-Range MTRR Format Physical Base 4 (MTRR_PHYSBASE4_REG_0_0_0_VTDBAR)	0000000000000000h
1C8h	8	Variable-Range MTRR Format Physical Mask 4 (MTRR_PHYSMASK4_REG_0_0_0_VTDBAR)	0000000000000000h
1D0h	8	Variable-Range MTRR Format Physical Base 5 (MTRR_PHYSBASE5_REG_0_0_0_VTDBAR)	0000000000000000h
1D8h	8	Variable-Range MTRR Format Physical Mask 5 (MTRR_PHYSMASK5_REG_0_0_0_VTDBAR)	0000000000000000h
1E0h	8	Variable-Range MTRR Format Physical Base 6 (MTRR_PHYSBASE6_REG_0_0_0_VTDBAR)	0000000000000000h
1E8h	8	Variable-Range MTRR Format Physical Mask 6 (MTRR_PHYSMASK6_REG_0_0_0_VTDBAR)	0000000000000000h
1F0h	8	Variable-Range MTRR Format Physical Base 7 (MTRR_PHYSBASE7_REG_0_0_0_VTDBAR)	0000000000000000h
1F8h	8	Variable-Range MTRR Format Physical Mask 7 (MTRR_PHYSMASK7_REG_0_0_0_VTDBAR)	0000000000000000h
200h	8	Variable-Range MTRR Format Physical Base 8 (MTRR_PHYSBASE8_REG_0_0_0_VTDBAR)	0000000000000000h
208h	8	Variable-Range MTRR Format Physical Mask 8 (MTRR_PHYSMASK8_REG_0_0_0_VTDBAR)	0000000000000000h
210h	8	Variable-Range MTRR Format Physical Base 9 (MTRR_PHYSBASE9_REG_0_0_0_VTDBAR)	0000000000000000h
218h	8	Variable-Range MTRR Format Physical Mask 9 (MTRR_PHYSMASK9_REG_0_0_0_VTDBAR)	0000000000000000h
400h	8	Fault Recording Register Low [0] (FRCDL_REG_0_0_0_VTDBAR)	0000000000000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
408h	8	Fault Recording Register High [0] (FRCDH_REG_0_0_0_VTDBAR)	0000000000000000h
500h	8	Invalidate Address Register (IVA_REG_0_0_0_VTDBAR)	0000000000000000h
508h	8	IOTLB Invalidate Register (IOTLB_REG_0_0_0_VTDBAR)	0200000000000000h

4.2.2 Version Register (VER_REG_0_0_0_VTDBAR) — Offset 0h

Register to report the architecture version supported. Backward compatibility for the architecture is maintained with new revision numbers, allowing software to load remapping hardware drivers written for prior architecture versions.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + 0h	00000040h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:4	4h RO	**Major Version Number (MAJOR):** Indicates supported architecture version.
3:0	0h RO	**Minor Version Number (MINOR):** Indicates supported architecture minor version.

4.2.3 Capability Register (CAP_REG_0_0_0_VTDBAR) — Offset 8h

Register to report general remapping hardware capabilities.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 8h	09C0000C406F0466h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:61	0h RO	**Reserved**
60	0h RO	**First Level 5-level Paging (FL5LP):** • 0: Hardware does not support 5-level paging for requests-with-PASID subject to first-level translation. • 1: Hardware supports 5-level paging for requests-with-PASID subject to first-level translation.
59	1h RO	**Posted Interrupt Support (PI):** • 0 = Hardware does not support Posting of Interrupts. • 1 = Hardware supports Posting of Interrupts. Hardware implementations reporting this field as Set must also report Interrupt Remapping support (IR field in Extended Capability Register)
58:57	0h RO	**Reserved**
56	1h RO	**First Level 1-GByte Page Support (FL1GP):** A value of 1 in this field indicates 1-GByte page size is supported for first-level translation.
55	1h RO	**Read Draining (DRD):** • 0 = Hardware does not support draining of DMA read requests. • 1 = Hardware supports draining of DMA read requests.
54	1h RO	**Write Draining (DWD):** • 0 = Hardware does not support draining of DMA write requests. • 1 = Hardware supports draining of DMA write requests.
53:48	00h RO	**Maximum Address Mask Value (MAMV):** The value in this field indicates the maximum supported value for the Address Mask (AM) field in the Invalidation Address register (IVA_REG) and IOTLB Invalidation Descriptor (iotlb_inv_dsc) used for invalidations of second-level translation. This field is valid only when the PSI field in Capability register is reported as Set.
47:40	00h RO	**Number of Fault-Recording Registers (NFR):** Number of fault recording registers is computed as N+1, where N is the value reported in this field. Implementations must support at least one fault recording register (NFR = 0) for each remapping hardware unit in the platform. The maximum number of fault recording registers per remapping hardware unit is 256.
39	0h RO	**Page Selective Invalidation (PSI):** • 0 = Hardware supports only domain and global invalidates for IOTLB. • 1 = Hardware supports page selective, domain and global invalidates for IOTLB. Hardware implementations reporting this field as set are recommended to support a Maximum Address Mask Value (MAMV) value of at least 9 (or 18 if supporting 1GB pages with second level translation).
38	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
37:34	3h RO	**Second Level Large Page Support (SLLPS):** This field indicates the super page sizes supported by hardware. A value of 1 in any of these bits indicates the corresponding super-page size is supported. The super-page sizes corresponding to various bit positions within this field are: • 0 = 21-bit offset to page frame (2MB) • 1 = 30-bit offset to page frame (1GB) • 2 = 39-bit offset to page frame (512GB) • 3 = 48-bit offset to page frame (1TB) Hardware implementations supporting a specific super-page size must support all smaller super-page sizes, i.e. only valid values for this field are 0000b, 0001b, 0011b, 0111b, 1111b.
33:24	040h RO	**Fault-Recording Register Offset (FRO):** This field specifies the location to the first fault recording register relative to the register base address of this remapping hardware unit. If the register base address is X, and the value reported in this field is Y, the address for the first fault recording register is calculated as X+(16*Y).
23	0h RO	**Reserved**
22	1h RO	**Zero Length Read (ZLR):** • 0 = Indicates the remapping hardware unit blocks (and treats as fault) zero length DMA read requests to write-only pages. • 1 = Indicates the remapping hardware unit supports zero length DMA read requests to write-only pages. DMA remapping hardware implementations are recommended to report ZLR field as Set.
21:16	2Fh RO	**Maximum Guest Address Width (MGAW):** This field indicates the maximum DMA virtual addressability supported by remapping hardware. The Maximum Guest Address Width (MGAW) is computed as (N+1), where N is the value reported in this field. For example, a hardware implementation supporting 48-bit MGAW reports a value of 47 (101111b) in this field. If the value in this field is X, untranslated and translated DMA requests to addresses above 2(x+1)-1 are always blocked by hardware. Translations requests to address above 2(x+1)-1 from allowed devices return a null Translation Completion Data Entry with R=W=0. Guest addressability for a given DMA request is limited to the minimum of the value reported through this field and the adjusted guest address width of the corresponding page-table structure. (Adjusted guest address widths supported by hardware are reported through the SAGAW field). Implementations are recommended to support MGAW at least equal to the physical addressability (host address width) of the platform.
15:13	0h RO	**Reserved**
12:8	04h RO	**Supported Adjusted Guest Address Widths (SAGAW):** This 5-bit field indicates the supported adjusted guest address widths (which in turn represents the levels of page-table walks for the 4KB base page size) supported by the hardware implementation. A value of 1 in any of these bits indicates the corresponding adjusted guest address width is supported. The adjusted guest address widths corresponding to various bit positions within this field are: • 0 = 30-bit AGAW (2-level page table) • 1 = 39-bit AGAW (3-level page table) • 2 = 48-bit AGAW (4-level page table) • 3 = 57-bit AGAW (5-level page table) • 4 = Reserved Software must ensure that the adjusted guest address width used to setup the page tables is one of the supported guest address widths reported in this field.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Caching Mode (CM):** • 0 = Not-present and erroneous entries are not cached in any of the renmapping caches. Invalidations are not required for modifications to individual not present or invalid entries. However, any modifications that result in decreasing the effective permissions or partial permission increases require invalidations for them to be effective. • 1 = Not-present and erroneous mappings may be cached in the remapping caches. Any software updates to the remapping structures (including updates to not-present or erroneous entries) require explicit invalidation. Hardware implementations of this architecture must support a value of 0 in this field.
6	1h RO	**Protected High-Memory Region (PHMR):** • 0 = Indicates protected high-memory region is not supported. • 1 = Indicates protected high-memory region is supported.
5	1h RO	**Protected Low-Memory Region (PLMR):** • 0 = Indicates protected low-memory region is not supported. • 1 = Indicates protected low-memory region is supported.
4	0h RO	**Required Write-Buffer Flushing (RWBF):** • 0 = Indicates no write-buffer flushing is needed to ensure changes to memory-resident structures are visible to hardware. • 1 = Indicates software must explicitly flush the write buffers to ensure updates made to memory-resident remapping structures are visible to hardware.
3	0h RO	**Advanced Fault Logging (AFL):** • 0 = Indicates advanced fault logging is not supported. Only primary fault logging is supported. • 1 = Indicates advanced fault logging is supported.
2:0	6h RO	**Number of Domains Supported (ND):** • 000b = Hardware supports 4-bit domain-ids with support for up to 16 domains. • 001b = Hardware supports 6-bit domain-ids with support for up to 64 domains. • 010b = Hardware supports 8-bit domain-ids with support for up to 256 domains. • 011b = Hardware supports 10-bit domain-ids with support for up to 1024 domains. • 100b = Hardware supports 12-bit domain-ids with support for up to 4K domains. • 100b = Hardware supports 14-bit domain-ids with support for up to 16K domains. • 110b = Hardware supports 16-bit domain-ids with support for up to 64K domains. • 111b = Reserved.

4.2.4 Extended Capability Register (ECAP_REG_0_0_0_VTDBAR) — Offset 10h

Register to report remapping hardware extended capabilities.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 10h	0000079E2FF050DFh

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:44	0h RO	**Reserved**
43	0h RO	**PASID Support Limitation (PSL):** This field is valid only when Process Address Space ID Support (PASID) field (bit 40) is reported as Set. When this field is reported as Set, extendedcontext-entries with PASID Enable (PASIDE) field Set do not support Requests-withoutPASID. Hardware implementations must report a value of 0 in this field. Virtual implementations may report a value of 1 in this field to disallow guest software from using an extended-context-entry for both Virtual Address (VA) and I/O Virtual Address (IOVA) concurrently.
42	1h RO	**Page Request Draining Support (PDS):** • 0 = Hardware does not support Page-Request Drain (PD) flag in Inv_wait_dsc. • 1 = Hardware supports Page-Request Drain (PD) flag in Inv_wait_dsc. This field is valid only when Device-TLB support field is reported as Set.
41	1h RO	**Device-TLB Invalidation Throttle (DIT):** • 0 = Hardware does not support Device-TLB Invalidation Throttling. • 1 = Hardware supports Device-TLB Invalidation Throttling. This field is valid only when Page Request Support (PRS) field is reported as Set.
40	1h RO	**Process Address Space ID Support (PASID):** • 0 = Hardware does not support requests tagged with Process Address Space IDs. • 1 = Hardware supports requests tagged with Process Address Space IDs.
39:35	13h RO	**PASID Size Supported (PSS):** This field reports the PASID size supported by the remapping hardware for requests-with-PASID. A value of N in this field indicates hardware supports PASID field of N+1 bits (For example, value of 7 in this field, indicates 8-bit PASIDs are supported). Requests-with-PASID with PASID value beyond the limit specified by this field are treated as error by the remapping hardware. This field is valid only when PASID field is reported as Set.
34	1h RO	**Extended Accessed Flag Support (EAFS):** • 0 = Hardware does not support the extended-accessed (EA) bit in first-level paging-structure entries. • 1 = Hardware supports the extended accessed (EA) bit in first-level paging-structure entries. This field is valid only when PASID field is reported as Set.
33	1h RO	**No Write Flag Support (NWFS):** • 0 = Hardware ignores the No Write (NW) flag in Device-TLB translationrequests, and behaves as if NW is always 0. • 1 = Hardware supports the No Write (NW) flag in Device-TLB translationrequests. This field is valid only when Device-TLB support (DT) field is reported as Set.
32	0h RO	**Reserved**
31	0h RO	**Supervisor Request Support (SRS):** • 0 = H/W does not support requests-with-PASID seeking supervisor privilege. • 1 = H/W supports requests-with-PASID seeking supervisor privilege. The field is valid only when PASID field is reported as Set.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RO	**Execute Request Support (ERS):** • 0 = H/W does not support requests-with-PASID seeking execute permission. • 1 = H/W supports requests-with-PASID seeking execute permission. This field is valid only when PASID field is reported as Set.
29	1h RO	**Page Request Support (PRS):** • 0 = Hardware does not support Page Requests. • 1 = Hardware supports Page Requests This field is valid only when Device-TLB (DT) field is reported as Set.
28	0h RO	**IGN:** Ignore this field
27	1h RO	**Deferred Invalidate Support (DIS):** • 0 = Hardware does not support deferred invalidations of IOTLB and Device-TLB. • 1 = Hardware supports deferred invalidations of IOTLB and Device-TLB. This field is valid only when PASID field is reported as Set.
26	1h RO	**Nested Translation Support (NEST):** • 0 = Hardware does not support nested translations. • 1 = Hardware supports nested translations. This field is valid only when PASID field is reported as Set.
25	1h RO	**Memory Type Support (MTS):** • 0 = Hardware does not support Memory Type in first-level translation and Extended Memory type in second-level translation. • 1 = Hardware supports Memory Type in first-level translation and Extended Memory type in second-level translation. This field is valid only when PASID and ECS fields are reported as Set. Remapping hardware units with, one or more devices that operate in processor coherency domain, under its scope must report this field as Set.
24	1h RO	**Extended Context Support (ECS):** • 0 = Hardware does not support extended-root-entries and extended-context-entries. • 1 = Hardware supports extended-root-entries and extended-context-entries. Implementations reporting PASID or PRS fields as Set, must report this field as Set.
23:20	Fh RO	**Maximum Handle Mask Value (MHMV):** The value in this field indicates the maximum supported value for the Handle Mask (HM) field in the interrupt entry cache invalidation descriptor (iec_inv_dsc). This field is valid only when the IR field in Extended Capability register is reported as Set.
19:18	0h RO	**Reserved**
17:8	050h RO	**IOTLB Register Offset (IRO):** This field specifies the offset to the IOTLB registers relative to the register base address of this remapping hardware unit. If the register base address is X, and the value reported in this field is Y, the address for the first IOTLB invalidation register is calculated as X+(16*Y).
7	1h RO	**Snoop Control (SC):** • 0 = Hardware does not support 1-setting of the SNP field in the page-table entries. • 1 = Hardware supports the 1-setting of the SNP field in the page-table entries.
6	1h RO	**Pass Through (PT):** • 0 = Hardware does not support pass-through translation type in context entries and extended-context-entries. • 1 = Hardware supports pass-through translation type in context entries and extended-context-entries. Pass-through translation is specified through Translation-Type (T) field value of 10b in context-entries, or T field value of 010b in extended-context-entries. Hardware implementations supporting PASID must report a value of 1b in this field.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**Reserved**
4	1h RO	**Extended Interrupt Mode (EIM):** • 0 = On Intel64 platforms, hardware supports only 8-bit APIC-IDs (xAPIC mode). • 1 = On Intel64 platforms, hardware supports 32-bit APIC-IDs (x2APIC mode). This field is valid only on Intel64 platforms reporting Interrupt Remapping support (IR field Set).
3	1h RO	**Interrupt Remapping Suport (IR):** • 0 = Hardware does not support interrupt remapping. • 1 = Hardware supports interrupt remapping. Implementations reporting this field as Set must also support Queued Invalidation (QI).
2	1h RO	**Device-TLB Support (DT):** • 0 = Hardware does not support device-IOTLBs. • 1 = Hardware supports Device-IOTLBs. Implementations reporting this field as Set must also support Queued Invalidation (QI). Hardware implementations supporting I/O Page Requests (PRS field Set in Extended Capability register) must report a value of 1b in this field.
1	1h RO	**Queued Invalidation Support (QI):** • 0 = Hardware does not support queued invalidations. • 1 = Hardware supports queued invalidations.
0	1h RO	**Page-Walk Coherency (C):** This field indicates if hardware access to the root, context, extended-context and interrupt-remap tables, and second-level paging structures for requests-without-PASID, are coherent (snooped) or not. • 0 = Indicates hardware accesses to remapping structures are non-coherent. • 1 = Indicates hardware accesses to remapping structures are coherent. Hardware access to advanced fault log, invalidation queue, invalidation semaphore, page-request queue, PASID-table, PASID-state table, and first-level page-tables are always coherent.

4.2.5 Global Command Register (GCMD_REG_0_0_0_VTDBAR) — Offset 18h

Register to control remapping hardware. If multiple control fields in this register need to be modified, software must serialize the modifications through multiple writes to this register

Register to control r mapping hardware. If multiple control fields in this register need to be modified, software must serialize the modifications through multiple writes to this register

- 1. Tmp = Read GSTS_REG
- 2. Status = (Tmp & 96FFFFFFh) // Reset the one-shot bits
- 3. Command = (Status | (Y << X))
- 4. Write Command to GCMD_REG
- 5. Wait until GSTS_REG[X] indicates command is serviced.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + 18h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Translation Enable (TE):** Software writes to this field to request hardware to enable/disable DMA-remapping: • 0 = Disable DMA remapping. • 1 = Enable DMA remapping. Hardware reports the status of the translation enable operation through the TES field in the Global Status register. There may be active DMA requests in the platform when software updates this field. Hardware must enable or disable remapping logic only at determinstic transaction boundaries, so that any in-flight transaction is either subject to remapping or not at all. Hardware implementations supporting DMA draining must drain any in-flight DMA read/write requests queued within the Root-Complex before completing the translation enable command and reflecting the status of the command through the TES field in the Global Status register. The value returned on a read of this field is undefined.
30	0h WO	**Set Root Table Pointer (SRTP):** Software sets this field to set/update the root-entry table pointer used by hardware. The root-entry table pointer is specified through the Root-entry Table Address (RTA_REG) register. Hardware reports the status of the Set Root Table Pointer operation through the RTPS field in the Global Status register. The Set Root Table Pointer operation must be performed before enabling or re-enabling (after disabling) DMA remapping through the TE field. .After a Set Root Table Pointer operation, software must globally invalidate the context cache and then globally invalidate of IOTLB. This is required to ensure hardware uses only the remapping structures referenced by the new root table pointer, and not stale cached entries. While DMA remapping hardware is active, software may update the root table pointer through this field. However, to ensure valid in-flight DMA requests are deterministically remapped, software must ensure that the structures referenced by the new root table pointer are programmed to provide the same remapping results as the structures referenced by the previous root-table pointer. Clearing this bit has no effect. The value returned on read of this field is undefined.
29	0h RO	**Set Fault Log (SFL):** This field is valid only for implementations supporting advanced fault logging. Software sets this field to request hardware to set/update the fault-log pointer used by hardware. The fault-log pointer is specified through Advanced Fault Log register. Hardware reports the status of the Set Fault Log operation through the FLS field in the Global Status register. The fault log pointer must be set before enabling advanced fault logging (through EAFL field). Once advanced fault logging is enabled, the fault log pointer may be updated through this field while DMA remapping is active. Clearing this bit has no effect. The value returned on read of this field is undefined.

Bit Range	Default & Access	Field Name (ID): Description
28	0h RO	**Enable Advanced Fault Logging (EAFL):** This field is valid only for implementations supporting advanced fault logging. Software writes to this field to request hardware to enable or disable advanced fault logging: • 0 = Disable advanced fault logging. In this case, translation faults are reported through the Fault Recording registers. • 1 = Enable use of memory-resident fault log. When enabled, translation faults are recorded in the memory-resident log. The fault log pointer must be set in hardware (through the SFL field) before enabling advaned fault logging. Hardware reports the status of the advaned fault logging enable operation through the AFLS field in the Global Status register. The value returned on read of this field is undefined.
27	0h RO	**Write Buffer Flush (WBF):** This bit is valid only for implementations requiring write buffer flushing. Software sets this field to request that hardware flush the Root-Complex internal write buffers. This is done to ensure any updates to the memory-resident remapping structures are not held in any internal write posting buffers. Hardware reports the status of the write buffer flushing operation through the WBFS field in the Global Status register. Clearing this bit has no effect. The value returned on a read of this field is undefined.
26	0h RW	**Queued Invalidation Enable (QIE):** This field is valid only for implementations supporting queued invalidations. Software writes to this field to enable or disable queued invalidations. • 0 = Disable queued invalidations. • 1 = Enable use of queued invalidations. Hardware reports the status of queued invalidation enable operation through QIES field in the Global Status register. The value returned on a read of this field is undefined.
25	0h RW	**Interrupt Remapping Enable (IRE):** This field is valid only for implementations supporting interrupt remapping. • 0 = Disable interrupt-remapping hardware. • 1 = Enable interrupt-remapping hardware. Hardware reports the status of the interrupt remapping enable operation through the IRES field in the Global Status register. There may be active interrupt requests in the platform when software updates this field. Hardware must enable or disable interrupt-remapping logic only at deterministic transaction boundaries, so that any in-flight interrupts are either subject to remapping or not at all. Hardware implementations must drain any in-flight interrupts requests queued in the Root-Complex before completing the interrupt-remapping enable command and reflecting the status of the command through the IRES field in the Global Status register. The value returned on a read of this field is undefined.

Bit Range	Default & Access	Field Name (ID): Description
24	0h WO	**Set Interrupt Remap Table Pointer (SIRTP):** This field is valid only for implementations supporting interrupt-remapping. Software sets this field to set/update the interrupt remapping table pointer used by hardware. The interrupt remapping table pointer is specified through the Interrupt Remapping Table Address (IRTA_REG) register. Hardware reports the status of the Set Interrupt Remap Table Pointer operation through the IRTPS field in the Global Status register. The Set Interrupt Remap Table Pointer operation must be performed before enabling or re-enabling (after disabling) interrupt-remapping hardware through the IRE field. After a Set Interrupt Remap Table Pointer operation, software must globally invalidate the interrupt entry cache. This is required to ensure hardware uses only the interrupt-remapping entries referenced by the new interrupt remap table pointer, and not any stale cached entries. While interrupt remapping is active, software may update the interrupt remapping table pointer through this field. However, to ensure valid in-flight interrupt requests are deterministically remapped, software must ensure that the structures referenced by the new interrupt remap table pointer are programmed to provide the same remapping results as the structures referenced by the previous interrupt remap table pointer. Clearing this bit has no effect. The value returned on a read of this field is undefined.
23	0h RW	**Compatibility Format Interrupt (CFI):** This field is valid only for Intel64 implementations supporting interrupt-remapping. Software writes to this field to enable or disable Compatibility Format interrupts on Intel64 platforms. The value in this field is effective only when interrupt-remapping is enabled and Extended Interrupt Mode (x2APIC mode) is not enabled. • 0 = Block Compatibility format interrupts. • 1 = Process Compatibility format interrupts as pass-through (bypass interrupt remapping). Hardware reports the status of updating this field through the CFIS field in the Global Status register. The value returned on a read of this field is undefined.
22:0	0h RO	**Reserved**

4.2.6 Global Status Register (GSTS_REG_0_0_0_VTDBAR) — Offset 1Ch

Register to report general remapping hardware status.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + 1Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Translation Enable Status (TES):** This field indicates the status of DMA-remapping hardware. • 0 = DMA-remapping hardware is not enabled. • 1 = DMA-remapping hardware is enabled

Bit Range	Default & Access	Field Name (ID): Description
30	0h RO/V	**Root Table Pointer Status (RTPS):** This field indicates the status of the root- table pointer in hardware. This field is cleared by hardware when software sets the SRTP field in the Global Command register. This field is set by hardware when hardware completes the Set Root Table Pointer operation using the value provided in the Root-Entry Table Address register.
29	0h RO	**Fault Log Status (FLS):** This field: • Is cleared by hardware when software Sets the SFL field in the Global Command register. • Is Set by hardware whn hardware completes the Set Fault Log Pointer operation using the value provided in the Advanced Fault Log register.
28	0h RO	**Adavanced Fault Logging Status (AFLS):** This field is valid only for implementations supporting advanced fault logging. It indicates the advanced fault logging status: • 0 = Advanced Fault Logging is not enabled. • 1 = Advanced Fault Logging is enabled.
27	0h RO	**Write Buffer Flush Status (WBFS):** This field is valid only for implementations requiring write buffer flushing. This field indicates the status of the write buffer flush command. It is: • Set by hardware when software sets the WBF field in the Global Command register. • Cleared by hardware when hardware completes the write buffer flushing operation.
26	0h RO/V	**Queued Invalidation Enable Status (QIES):** This field indicates queued invalidation enable status. • 0 = queued invalidation is not enabled. • 1 = queued invalidation is enabled
25	0h RO/V	**Interrupt Remapping Enable Status (IRES):** This field indicates the status of Interrupt-remapping hardware. • 0 = Interrupt-remapping hardware is not enabled. • 1 = Interrupt-remapping hardware is enabled
24	0h RO/V	**Interrupt Remapping Pointer Status (IRTPS):** This field indicates the status of the interrupt remapping table pointer in hardware. This field is cleared by hardware when software sets the SIRTP field in the Global Command register. This field is Set by hardware when hardware completes the set interrupt remap table pointer operation using the value provided in the Interrupt Remapping Table Address register.
23	0h RO/V	**Compatibility Format Interrupt Status (CFIS):** This field indicates the status of Compatibility format interrupts on Intel64 implementations supporting interrupt-remapping. The value reported in this field is applicable only when interrupt-remapping is enabled and Extended Interrupt Mode (x2APIC mode) is not enabled. • 0 = Compatibility format interrupts are blocked. • 1 = Compatibility format interrupts are processed as pass-through (bypassing interrupt remapping).
22:0	0h RO	**Reserved**

4.2.7 Root Table Address Register (RTADDR_REG_0_0_0_VTDBAR) — Offset 20h

Register providing the base address of root-entry table.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 20h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:52	0h RO	**Reserved**
51:12	0000000000h RW	**Root Table Address (RTA):** This register points to base of page aligned, 4KB-sized root-entry table in system memory. Hardware ignores and not implements bits 63:HAW, where HAW is the host address width. Software specifies the base address of the root-entry table through this register, and programs it in hardware through the SRTP field in the Global Command register. Reads of this register returns value that was last programmed to it.
11	0h RW	**Root Table Type (RTT):** This field specifies the type of root-table referenced by the Root Table Address (RTA) field: • 0 = Root Table. • 1 = Extended Root Table
10:0	0h RO	**Reserved**

4.2.8 Context Command Register (CCMD_REG_0_0_0_VTDBAR) — Offset 28h

Register to manage context cache. The act of writing the uppermost byte of the CCMD_REG with the ICC field Set causes the hardware to perform the context-cache invalidation.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 28h	0800000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/V	**Invalidate Context Cache (ICC):** Software requests invalidation of context-cache by setting this field. Software must also set the requested invalidation granularity by programming the CIRG field. Software must read back and check the ICC field is Clear to confirm the invalidation is complete. Software must not update this register when this field is set. Hardware clears the ICC field to indicate the invalidation request is complete. Hardware also indicates the granularity at which the invalidation operation was performed through the CAIG field. Software must submit a context-cache invalidation request through this field only when there are no invalidation requests pending at this remapping hardware unit. Since information from the context-cache may be used by hardware to tag IOTLB entries, software must perform domain-selective (or global) invalidation of IOTLB after the context cache invalidation has completed. Hardware implementations reporting write-buffer flushing requirement (RWBF=1 in Capability register) must implicitly perform a write buffer flush before invalidating the context cache.
62:61	0h RW	**Context Invalidation Request Granularity (CIRG):** Software provides the requested invalidation granularity through this field when setting the ICC field: • 00: Reserved. • 01: Global Invalidation request. • 10: Domain-selective invalidation request. The target domain-id must be specified in the DID field. • 11: Device-selective invalidation request. The target source-id(s) must be specified through the SID and FM fields, and the domain-id (that was programmed in the context-entry for these device(s)) must be provided in the DID field. Hardware implementations may process an invalidation request by performing invalidation at a coarser granularity than requested. Hardware indicates completion of the invalidation request by clearing the ICC field. At this time, hardware also indicates the granularity at which the actual invalidation was performed through the CAIG field.
60:59	1h RO/V	**Context Actual Invalidation Granularity (CAIG):** Hardware reports the granularity at which an invalidation request was processed through the CAIG field at the time of reporting invalidation completion (by clearing the ICC field). The following are the encodings for this field: • 00: Reserved. • 01: Global Invalidation performed. This could be in response to a global, domain-selective or device-selective invalidation request. • 10: Domain-selective invalidation performed using the domain-id specified by software in the DID field. This could be in response to a domain-selective or device-selective invalidation request. • 11: Device-selective invalidation performed using the source-id and domain-id specified by software in the SID and FM fields. This can only be in response to a device-selective invalidation request.
58:34	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
33:32	0h RW	**Function Mask (FM):** Software may use the Function Mask to perform device-selective invalidations on behalf of devices supporting PCI Express Phantom Functions...This field specifies which bits of the function number portion (least significant three bits) of the SID field to mask when performing device-selective invalidations. The following encodings are defined for this field: • 00: No bits in the SID field masked. • 01: Mask most significant bit of function number in the SID field. • 10: Mask two most significant bit of function number in the SID field. • 11: Mask all three bits of function number in the SID field. The context-entries corresponding to all the source-ids specified through the FM and SID fields must have to the domain-id specified in the DID field.
31:16	0000h RW	**SID:** Indicates the source-id of the device whose corresponding context-entry needs to be selectively invalidated. This field along with the FM field must be programmed by software for device-selective invalidation requests.
15:0	0000h RW	**DID:** Indicates the id of the domain whose context-entries need to be selectively invalidated. This field must be programmed by software for both domain-selective and device-selective invalidation requests. The Capability register reports the domain-id width supported by hardware. Software must ensure that the value written to this field is within this limit. Hardware may ignore and not implement bits15:N, where N is the supported domain-id width reported in the Capability register.

4.2.9 Fault Status Register (FSTS_REG_0_0_0_VTDBAR) — Offset 34h

Register indicating the various error status.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + 34h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RO	**Fault Record Index (FRI):** This field is valid only when the PPF field is Set. The FRI field indicates the index (from base) of the fault recording register to which the first pending fault was recorded when the PPF field was Set by hardware. The value read from this field is undefined when the PPF field is clear.
7	0h RW/1C	**Page Request Overflow (PRO):** Hardware detected a Page Request Overflow error. Hardware implementations not supporting the Page Request Queue implement this bit as RsvdZ.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/1C	**Invalidation Time-out Error (ITE):** Hardware detected a Device-IOTLB invalidation completion time-out. At this time, a fault event may be generated based on the programming of the Fault Event Control register. Hardware implementations not supporting device Device-IOTLBs implement this bit as RsvdZ.
5	0h RW/1C	**Invalidation Completion Error (ICE):** Hardware received an unexpected or invalid Device-IOTLB invalidation completion. This could be due to either an invalid ITag or invalid source-id in an invalidation completion response. At this time, a fault event may be generated based on the programming of hte Fault Event Control register. Hardware implementations not supporting Device-IOTLBs implement this bit as RsvdZ.
4	0h RW/1C	**Invalidation Queue Error (IQE):** Hardware detected an error associated with the invalidation queue. This could be due to either a hardware error while fetching a descriptor from the invalidation queue, or hardware detecting an erroneous or invalid descriptor in the invalidation queue. At this time, a fault event may be generated based on the programming of the Fault Event Control register. Hardware implementations not supporting queued invalidations implement this bit as RsvdZ.
3	0h RO	**Advanced Pending Fault (APF):** When this field is Clear, hardware sets this field when the first fault record (at index 0) is written to a fault log. At this time, a fault event is generated based on the programming of the Fault Event Control register. Software writing 1 to this field clears it. Hardware implementations not supporting advanced fault logging implement this bit as RsvdZ.
2	0h RO	**Advanced Fault Overflow (AFO):** Hardware sets this field to indicate advanced fault log overflow condition. At this time, a fault event is generated based on the programming of the Fault Event Control register. Software writing 1 to this field clears it. Hardware implementations not supporting advanced fault logging implement this bit as RsvdZ.
1	0h RO/V	**Primary Pending Fault (PPF):** This field indicates if there are one or more pending faults logged in the fault recording registers. Hardware computes this field as the logical OR of Fault (F) fields across all the fault recording registers of this remapping hardware unit. • 0 = No pending faults in any of the fault recording registers. • 1 = One or more fault recording registers has pending faults. The FRI field is updated by hardware whenever the PPF field is set by hardware. Also, depending on the programming of Fault Event Control register, a fault event is generated when hardware sets this field.
0	0h RW/1C	**Primary Fault Overflow (PFO):** Hardware sets this field to indicate overflow of fault recording registers. Software writing 1 clears this field. When this field is Set, hardware does not record any new faults until software clears this field.

4.2.10 Fault Event Control Register (FECTL_REG_0_0_0_VTDBAR) — Offset 38h

Register specifying the fault event interrupt message control bits.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + 38h	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**Interrupt Mask (IM):** • 0 = No masking of interrupt. When an interrupt condition is detected, hardware issues an interrupt message (using the Fault Event Data and Fault Event Address register values). • 1 = This is the value on reset. Software may mask interrupt message generation by setting this field. Hardware is prohibited from sending the interrupt message when this field is set.
30	0h RO/V	**Interrupt Pending (IP):** Hardware sets the IP field whenever it detects an interrupt condition, which is defined as: • When primary fault logging is active, an interrupt condition occurs when hardware records a fault through one of the Fault Recording registers and sets the PPF field in Fault Status register. • When advanced fault logging is active, an interrupt condition occurs when hardware records a fault in the first fault record (at index 0) of the current fault log and sets the APF field in the Fault Status register. • Hardware detected error associated with the Invalidation Queue, setting the IQE field in the Fault Status register. • Hardware detected invalid Device-IOTLB invalidation completion, setting the ICE field in the Fault Status register. • Hardware detected Device-IOTLB invalidation completion time-out, setting the ITE field in the Fault Status register. If any of the status fields in the Fault Status register was already Set at the time of setting any of these fields, it is not treated as a new interrupt condition. The IP field is kept set by hardware while the interrupt message is held pending. The interrupt message could be held pending due to interrupt mask (IM field) being Set or other transient hardware conditions. The IP field is cleared by hardware as soon as the interrupt message pending condition is serviced. This could be due to either: • Hardware issuing the interrupt message due to either change in the transient hardware condition that caused interrupt message to be held pending, or due to software clearing the IM field. • Software servicing all the pending interrupt status fields in the Fault Status register as follows: — When primary fault logging is active, software clearing the Fault (F) field in all the Fault Recording registers with faults, causing the PPF field in Fault Status register to be evaluated as clear. — Software clearing other status fields in the Fault Status register by writing back the value read from the respective fields.
29:0	0h RO	**Reserved**

4.2.11 Fault Event Data Register (FEDATA_REG_0_0_0_VTDBAR) — Offset 3Ch

Register specifying the interrupt message data

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + 3Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Extended Interrupt Message Data (EIMD):** This field is valid only for implementations supporting 32-bit interrupt data fields. Hardware implementations supporting only 16-bit interrupt data may treat this field as RsvdZ.
15:0	0000h RW	**Interrupt Message Data (IMD):** Data value in the interrupt request.

4.2.12 Fault Event Address Register (FEADDR_REG_0_0_0_VTDBAR) — Offset 40h

Register specifying the interrupt message address.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + 40h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**Message Address (MA):** When fault events are enabled, the contents of this register specify the DWORD-aligned address (bits 31:2) for the interrupt request.
1:0	0h RO	**Reserved**

4.2.13 Fault Event Upper Address Register (FEUADDR_REG_0_0_0_VTDBAR) — Offset 44h

Register specifying the interrupt message upper address.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + 44h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Message Upper Address (MUA):** Hardware implementations supporting Extended Interrupt Mode are required to implement this register. Hardware implementations not supporting Extended Interrupt Mode may treat this field as RsvdZ.

4.2.14 Advanced Fault Log Register (AFLOG_REG_0_0_0_VTDBAR) — Offset 58h

Register to specify the base address of the memory-resident fault-log region. This register is treated as RsvdZ for implementations not supporting advanced translation fault logging (AFL field reported as 0 in the Capability register).

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 58h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:12	0000000000000h RO	**Fault Log Address (FLA):** This field specifies the base of 4KB aligned fault-log region in system memory. Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width. Software specifies the base address and size of the fault log region through this register, and programs it in hardware through the SFL field in the Global Command register. When implemented, reads of this field return the value that was last programmed to it.
11:9	0h RO	**Fault Log Size (FLS):** This field specifies the size of the fault log region pointed by the FLA field. The size of the fault log region is 2X * 4KB, where X is the value programmed in this register. When implemented, reads of this field return the value that was last programmed to it.
8:0	0h RO	**Reserved**

4.2.15 Protected Memory Enable Register (PMEN_REG_0_0_0_VTDBAR) — Offset 64h

Register to enable the DMA-protected memory regions setup through the PLMBASE,..PLMLIMT, PHMBASE, PHMLIMIT registers. This register is always treated as RO for implementations not supporting protected memory regions (PLMR and PHMR fields reported as Clear in the Capability register).

Protected memory regions may be used by software to securely initialize remapping structures in memory. To avoid impact to legacy BIOS usage of memory, software is recommended to not overlap protected memory regions with any reserved memory regions of the platform reported through the Reserved Memory Region Reporting (RMRR) structures.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + 64h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Protected Memory (EPM):** This field controls DMA accesses to the protected low-memory and protected high-memory regions. • 0 = Protected memory regions are disabled. • 1 = Protected memory regions are enabled.DMA requests accessing protected memory regions are handled as follows: — When DMA remapping is not enabled, all DMA requests accessing protected memory regions are blocked. — When DMA remapping is enabled: — DMA requests processed as pass-through (Translation Type value of 10b in Context-Entry) and accessing the protected memory regions are blocked. — DMA requests with translated address (AT=10b) and accessing the protected memory regions are blocked. — DMA requests that are subject to address remapping, and accessing the protected memory regions may or may not be blocked by hardware. For such requests, software must not depend on hardware protection of the protected memory regions, and instead program the DMA-remapping page-tables to not allow DMA to protected memory regions. Remapping hardware access to the remapping structures are not subject to protected memory region checks. DMA requests blocked due to protected memory region violation are not recorded or reported as remapping faults. Hardware reports the status of the protected memory enable/disable operation through the PRS field in this register.Hardware implementations supporting DMA draining must drain any in-flight translated DMA requests queued within the Root-Complex before indicating the protected memory region as enabled through the PRS field. After writing to this field software must wait for the operation to be completed and reflected in the PRS status field (bit 0) before changing the value of this field again.
30:1	0h RO	**Reserved**
0	0h RO/V	**Protected Region Status (PRS):** This field indicates the status of protected memory region(s): • 0 = Protected memory region(s) disabled. • 1 = Protected memory region(s) enabled.

4.2.16 Protected Low Memory Base Register (PLMBASE_REG_0_0_0_VTDBAR) — Offset 68h

Register to set up the base address of DMA-protected low-memory region below 4GB. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled.

This register is always treated as RO for implementations not supporting protected low memory region (PLMR field reported as Clear in the Capability register).

The alignment of the protected low memory region base depends on the number of reserved bits (N:0) of this register. Software may determine N by writing all 1s to this register, and finding the most significant zero bit position with 0 in the value read back from the register. Bits N:0 of this register is decoded by hardware as all 0s...Software must setup the protected low memory region below 4GB.

Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + 68h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW	**Protected Low-Memory Base (PLMB):** This register specifies the base of protected low-memory region in system memory.
19:0	0h RO	**Reserved**

4.2.17 Protected Low-Memory Limit Register (PLMLIMIT_REG_0_0_0_VTDBAR) — Offset 6Ch

Register to set up the limit address of DMA-protected low-memory region below 4GB. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled

This register is always treated as RO for implementations not supporting protected low memory region (PLMR field reported as Clear in the Capability register)

The alignment of the protected low memory region limit depends on the number of reserved bits (N:0) of this register. Software may determine N by writing all 1s to this register, and finding most significant zero bit position with 0 in the value read back from the register. Bits N:0 of the limit register is decoded by hardware as all 1s

The Protected low-memory base and limit registers functions as follows:

- Programming the protected low-memory base and limit registers with the same value in bits 31: (N+1) specifies a protected low-memory region of size 2(N+1) bytes

- Programming the protected low-memory limit register with a value less than the protected low-memory base register disables the protected low-memory region

Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + 6Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RW	**Protected Low-Memory Limit (PLML):** This register specifies the last host physical address of the DMA-protected low-memory region in system memory.
19:0	0h RO	**Reserved**

4.2.18 Protected High-Memory Base Register (PHMBASE_REG_0_0_0_VTDBAR) — Offset 70h

Register to set up the base address of DMA-protected high-memory region. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled

This register is always treated as RO for implementations not supporting protected high memory region (PHMR field reported as Clear in the Capability register)

The alignment of the protected high memory region base depends on the number of reserved bits (N:0) of this register. Software may determine N by writing all 1s to this register, and finding most significant zero bit position below host address width (HAW) in the value read back from the register. Bits N:0 of this register are decoded by hardware as all 0s

Software may setup the protected high memory region either above or below 4GB

Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 70h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:20	00000h RW	**Protected High-Memory Base (PHMB):** This register specifies the base of protected (high) memory region in system memory Hardware ignores, and does not implement, bits 63:HAW, where HAW is the host address width.
19:0	0h RO	**Reserved**

4.2.19 Protected High-Memory Limit Register (PHMLIMIT_REG_0_0_0_VTDBAR) — Offset 78h

Register to set up the limit address of DMA-protected high-memory region. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled

This register is always treated as RO for implementations not supporting protected high memory region (PHMR field reported as Clear in the Capability register)

The alignment of the protected high memory region limit depends on the number of reserved bits (N:0) of this register. Software may determine the value of N by writing all 1s to this register, and finding most significant zero bit position below host address width (HAW) in the value read back from the register. Bits N:0 of the limit register is decoded by hardware as all 1s

The protected high-memory base & limit registers functions as follows

- Programming the protected low-memory base and limit registers with the same value in bits HAW:(N+1) specifies a protected low-memory region of size 2(N+1) bytes
- Programming the protected high-memory limit register with a value less than the protected high-memory base register disables the protected high-memory region

Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 78h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:20	00000h RW	**Protected High-Memory Limit (PHML):** This register specifies the last host physical address of the DMA-protected high-memory region in system memory Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width.
19:0	0h RO	**Reserved**

4.2.20 Invalidation Queue Head Register (IQH_REG_0_0_0_VTDBAR) — Offset 80h

Register indicating the invalidation queue head. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 80h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:19	0h RO	**Reserved**
18:4	0000h RO/V	**Queue Head (QH):** Specifies the offset (128-bit aligned) to the invalidation queue for the command that will be fetched next by hardware Hardware resets this field to 0 whenever the queued invalidation is disabled (QIES field Clear in the Global Status register).
3:0	0h RO	**Reserved**

4.2.21 Invalidation Queue Tail Register (IQT_REG_0_0_0_VTDBAR) — Offset 88h

Register indicating the invalidation tail head. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 88h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:19	0h RO	**Reserved**
18:4	0000h RW	**Queue Tail (QT):** Specifies the offset (128-bit aligned) to the invalidation queue for the command that will be written next by software.
3:0	0h RO	**Reserved**

4.2.22 Invalidation Queue Address Register (IQA_REG_0_0_0_VTDBAR) — Offset 90h

Register to configure the base address and size of the invalidation queue. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 90h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RW	**Invalidation Queue Base Address (IQA):** This field points to the base of 4KB aligned invalidation request queue. Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width Reads of this field return the value that was last programmed to it.

Bit Range	Default & Access	Field Name (ID): Description
11:3	0h RO	**Reserved**
2:0	0h RW	**Queue Size (QS):** This field specifies the size of the invalidation request queue. A value of X in this field indicates an invalidation request queue of (2^X) 4KB pages. The number of entries in the invalidation queue is 2^(X + 8).

4.2.23 Invalidation Completion Status Register (ICS_REG_0_0_0_VTDBAR) — Offset 9Ch

Register to report completion status of invalidation wait descriptor with Interrupt Flag (IF) Set

This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + 9Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/1C	**Invalidation Wait Descriptor Complete (IWC):** Indicates completion of Invalidation Wait Descriptor with Interrupt Flag (IF) field Set. Hardware implementations not supporting queued invalidations implement this field as RsvdZ.

4.2.24 Invalidation Event Control Register (IECTL_REG_0_0_0_VTDBAR) — Offset A0h

Register specifying the invalidation event interrupt control bits

This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + A0h	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**Interrupt Mask (IM):** • 0= No masking of interrupt. When a invalidation event condition is detected, hardware issues an interrupt message (using the Invalidation Event Data & Invalidation Event Address register values) • 1= This is the value on reset. Software may mask interrupt message generation by setting this field. Hardware is prohibited from sending the interrupt message when this field is Set.
30	0h RO/V	**Interrupt Pending (IP):** Hardware sets the IP field whenever it detects an interrupt condition. Interrupt condition is defined as: • An Invalidation Wait Descriptor with Interrupt Flag (IF) field Set completed, setting the IWC field in the Invalidation Completion Status register • If the IWC field in the Invalidation Completion Status register was already Set at the time of setting this field, it is not treated as a new interrupt condition The IP field is kept Set by hardware while the interrupt message is held pending. The interrupt message could be held pending due to interrupt mask (IM field) being Set, or due to other transient hardware conditions. The IP field is cleared by hardware as soon as the interrupt message pending condition is serviced. This could be due to either: • 0= Hardware issuing the interrupt message due to either change in the transient hardware condition that caused interrupt message to be held pending or due to software clearing the IM field • 1= Software servicing the IWC field in the Invalidation Completion Status register.
29:0	0h RO	**Reserved**

4.2.25 Invalidation Event Data Register (IEDATA_REG_0_0_0_VTDBAR) — Offset A4h

Register specifying the Invalidation Event interrupt message data

This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Extended Interrupt Message Data (EIMD):** This field is valid only for implementations supporting 32-bit interrupt data fields Hardware implementations supporting only 16-bit interrupt data treat this field as Rsvd.
15:0	0000h RW	**Interrupt Message Data (IMD):** Data value in the interrupt request.

4.2.26 Invalidation Event Address Register (IEADDR_REG_0_0_0_VTDBAR) — Offset A8h

Register specifying the Invalidation Event Interrupt message address

This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Note: **NOTE:** Bit definitions are the same as FEADDR_REG_0_0_0_VTDBAR, offset 40h.

4.2.27 Invalidation Event Upper Address Register (IEUADDR_REG_0_0_0_VTDBAR) — Offset ACh

Register specifying the Invalidation Event interrupt message upper address.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Message Upper Address (MUA):** Hardware implementations supporting Queued Invalidations and Extended Interrupt Mode are required to implement this register Hardware implementations not supporting Queued Invalidations or Extended Interrupt Mode may treat this field as RsvdZ.

4.2.28 Interrupt Remapping Table Address Register (IRTA_REG_0_0_0_VTDBAR) — Offset B8h

Register providing the base address of Interrupt remapping table. This register is treated as RsvdZ by implementations reporting Interrupt Remapping (IR) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + B8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:12	00000000 00000h RW	**Interrupt Remapping Table Address (IRTA):** This field points to the base of 4KB aligned interrupt remapping table Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width Reads of this field returns value that was last programmed to it.
11	0h RW	**Extended Interrupt Mode Enable (EIME):** This field is used by hardware on Intel64 platforms as follows: • 0=xAPIC mode is active. Hardware interprets only low 8-bits of Destination-ID field in the IRTEs. The high 24-bits of the Destination-ID field are treated as reserved • 1= x2APIC mode is active. Hardware interprets all 32-bits of Destination-ID field in the IRTEs This field is implemented as RsvdZ on implementations reporting Extended Interrupt Mode (EIM) field as Clear in Extended Capability register.
10:4	0h RO	**Reserved**
3:0	0h RW	**S:** This field specifies the size of the interrupt remapping table. The number of entries in the interrupt remapping table is 2(X+1), where X is the value programmed in this field.

4.2.29 Page Request Queue Head Register (PQH_REG_0_0_0_VTDBAR) — Offset C0h

Register indicating the page request queue head. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + C0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:19	0h RO	**Reserved**
18:4	0000h RW	**Page Queue Head (PQH):** Specifies the offset (16-bytes aligned) to the page request queue for the request that will be processed next by software.
3:0	0h RO	**Reserved**

4.2.30 Page Request Queue Tail Register (PQT_REG_0_0_0_VTDBAR) — Offset C8h

Register indicating the page request queue tail. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + C8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:19	0h RO	**Reserved**
18:4	0000h RW/V	**Page Queue Tail (PQT):** Specifies the offset (16-bytes aligned) to the page request queue for the request that will be written next by hardware.
3:0	0h RO	**Reserved**

4.2.31 Page Request Queue Address Register (PQA_REG_0_0_0_VTDBAR) — Offset D0h

Register to configure the base address and size of the page request queue. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + D0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	000000000h RW	**Page Request Queue Base Address (PQA):** This field points to the base of 4KB aligned page request queue. Hardware may ignore and not implement bits 63:HAW, where HAW is the host address width. Software must configure this register before enabling page requests in any extended-context-entries.
11:3	0h RO	**Reserved**
2:0	0h RW	**Page Request Queue Size (PQS):** This field specifies the size of the page request queue. A value of X in this field indicates an invalidation request queue of (2^X) 4KB pages. The number of entries in the page request queue is 2^(X + 8)

4.2.32 Page Request Status Register (PRS_REG_0_0_0_VTDBAR) — Offset DCh

Register to report pending page request in page request queue. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + DCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/1C	**Pending Page Request (PPR):** Pending Page Request: Indicates pending page requests to be serviced by software in the page request queue. This field is Set by hardware when a streaming page request entry (page_stream_reg_dsc) or a page group request (page_grp_req_dsc) with Last Page in Group (LPG) field Set, is added to the page request queue.

4.2.33 Page Request Event Control Register (PECTL_REG_0_0_0_VTDBAR) — Offset E0h

Register specifying the page request event interrupt control bits. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + E0h	80000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**Interrupt Mask (IM):** Interrupt Mask • 0=No masking of interrupt. When a page request event condition is detected, hardware issues an interrupt message (using the Page Request Event Data and Page Request Event Address register values) • 1=This is the value on reset. Software may mask interrupt message generation by setting this field. Hardware is prohibited from sending the interrupt message when this field is Set.
30	0h RO/V	**Interrupt Pending (IP):** Interrupt Pending: Hardware sets the IP field whenever it detects an interrupt condition. Interrupt condition is defined as: • A streaming page request entry (page_stream_req_dsc) or a page group request (page_grp_req_dsc) with Last Page in Group (LPG) field Set, was added to page request queue, resulting in hardware setting the Pending Page Request (PPR) field in Page Request Status register • If the PPR field in the Page Request Event Status register was already Set at the time of setting this field, it is not treated as a new interrupt condition The IP field is kept Set by hardware while the interrupt message is held pending. The interrupt message could be held pending due to interrupt mask (IM field) being Set, or due to other transient hardware conditions. The IP field is cleared by hardware as soon as the interrupt message pending condition is serviced. This could be due to either: • Hardware issuing the interrupt message due to either change in the transient hardware condition that caused interrupt message to be held pending or due to software clearing the IM field • Software servicing the PPR field in the Page Request Event Status register.
29:0	0h RO	**Reserved**

4.2.34 Page Request Event Data Register (PEDATA_REG_0_0_0_VTDBAR) — Offset E4h

Register specifying the Page Request Event interrupt message data. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Extended Interrupt Message Data (EIMD):** Extended Interrupt Message Data
15:0	0000h RW	**Interrupt Message Data (IMD):** Interrupt Message Data: Data value in the interrupt request. Software requirements for programming this register are described in VTd Spec

4.2.35 Page Request Event Address Register (PEADDR_REG_0_0_0_VTDBAR) — Offset E8h

Register specifying the Page Request Event Interrupt message address. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**Message Address (MA):** Message Address: When fault events are enabled, the contents of this register specify the DWORD-aligned address (bits 31:2) for the interrupt request.
1:0	0h RO	**Reserved**

4.2.36 Page Request Event Upper Address Register (PEUADDR_REG_0_0_0_VTDBAR) — Offset ECh

Register specifying the Page Request Event interrupt message upper address.

Type	Size	Offset	Default
MMIO	32 bit	GFXVTBAR + ECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Message Upper Address (MUA):** Message Upper Address: This field specifies the upper address (bits.. 63:32) for the page request event interrupt.

4.2.37 MTRR Capability Register (MTRRCAP_0_0_0_VTDBAR) — Offset 100h

Register reporting the Memory Type Range Register Capability. This register is treated as RsvdZ by implementations reporting Memory Type Support (MTS) as not supported in the Extended Capability register.

When implemented, value reported in this register must match IA32_MTRRCAP Model Specific Register (MSR) value reported by the host IA-32 processor(s).

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 100h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:11	0h RO	**Reserved**
10	0h RO	**Write Combining (WC):** • 0 = Write-combining (WC) memory type is not supported. • 1 = Write-combining (WC) memory type is supported.Indicates whether the Write Combining memory type is supported.
9	0h RO	**Reserved**
8	0h RO	**Fixed Range MTRRs Supported (FIX):** • 0 = No fixed range MTRRs are supported • 1 = Fixed range MTRRs (MTRR_FIX64K_00000 through MTRR_FIX4K_0F8000) are supported
7:0	00h RO	**Variable MTRR Count (VCNT):** Indicates number of variable range MTRRs are supported.

4.2.38 MTRR Default Type Register (MTRRDEFAULT_0_0_0_VTDBAR) — Offset 108h

Register for enabling/configuring Memory Type Range Registers. This register is treated as RsvdZ by implementations reporting Memory Type Support (MTS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 108h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:12	0h RO	**Reserved**
11	0h RO	**MTRR Enable (E):** • 0 = Disable MTRRs; UC memory type is applied. FE field has no effect. • 1 = Enable MTRRs. FE field can disable the fixed-range MTRRs. Type specified in the default memory type field is used for areas of memory not already mapped by either fixed or variable MTRR
10	0h RO	**Fixed Range MTRR Enable (FE):** • 0 = Disable fixed range MTRRs. • 1 = Enable fixed range MTRRs. When fixed range MTRRs are enabled, they take priority over the variable range MTRRs when overlaps in ranges occur. If the fixed-range MTRRs are disabled, the variable range MTRRs can still be used and can map the range ordinarily covered by the fixed range MTRRs.
9:8	0h RO	**Reserved**
7:0	00h RO	**Default Memory Type (MEMTYPE):** Indicates default memory type used for physical memory address ranges that do not have a memory type specified for them by an MTRR. Legal values for this field are 0,1,4, 5 and 6.

4.2.39 Fixed-Range MTRR Format 64K-00000 (MTRR_FIX64K_00000_REG_0_0_0_VTDBAR) — Offset 120h

Fixed Range MTRR covering the 64K memory space from 0x00000 - 0x7FFFF.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 120h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RO	**R7:** Register Field 7
55:48	00h RO	**R6:** Register Field 6
47:40	00h RO	**R5:** Register Field 5
39:32	00h RO	**R4:** Register Field 4
31:24	00h RO	**R3:** Register Field 3
23:16	00h RO	**R2:** Register Field 2
15:8	00h RO	**R1:** Register Field 1
7:0	00h RO	**R0:** Register Field 0

4.2.40 Fixed-Range MTRR Format 16K-80000 (MTRR_FIX16K_80000_REG_0_0_0_VTDBAR) — Offset 128h

Fixed Range MTRR covering the 16K memory space from 0x80000 - 0x9FFFF.

Note: **NOTE:** Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

4.2.41 Fixed-Range MTRR Format 16K-A0000 (MTRR_FIX16K_A0000_REG_0_0_0_VTDBAR) — Offset 130h

Fixed Range MTRR covering the 16K memory space from 0xA0000 - 0xBFFFF.

Note: **NOTE:** Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

4.2.42 Fixed-Range MTRR Format 4K-C0000 (MTRR_FIX4K_C0000_REG_0_0_0_VTDBAR) — Offset 138h

Fixed Range MTRR covering the 4K memory space 0xC0000 - 0xC7FFF.

Note: **NOTE:** Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

4.2.43 Fixed-Range MTRR Format 4K-C8000 (MTRR_FIX4K_C8000_REG_0_0_0_VTDBAR) — Offset 140h

Fixed Range MTRR covering the 4K memory space from 0xC8000 - 0xCFFFF.

Note: **NOTE:** Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

4.2.44 Fixed-Range MTRR Format 4K-D0000 (MTRR_FIX4K_D0000_REG_0_0_0_VTDBAR) — Offset 148h

Fixed Range MTRR covering the 4K memory space from 0xD0000 - 0xD7FFF.

Note: **NOTE:** Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

4.2.45 Fixed-Range MTRR Format 4K-D8000 (MTRR_FIX4K_D8000_REG_0_0_0_VTDBAR) — Offset 150h

Fixed Range MTRR covering the 4K memory space from 0xD80000 - 0xDFFFF.

Note: **NOTE:** Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

4.2.46 Fixed-Range MTRR Format 4K-E0000 (MTRR_FIX4K_E0000_REG_0_0_0_VTDBAR) — Offset 158h

Fixed Range MTRR covering the 4K memory space from 0xE0000 - 0xE7FFF.

Note: **NOTE:** Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

4.2.47 Fixed-Range MTRR Format 4K-E8000 (MTRR_FIX4K_E8000_REG_0_0_0_VTDBAR) — Offset 160h

Fixed Range MTRR covering the 4K memory space from 0xE8000 - 0xEFFFF.

Note: **NOTE:** Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

4.2.48 Fixed-Range MTRR Format 4K-F0000 (MTRR_FIX4K_F0000_REG_0_0_0_VTDBAR) — Offset 168h

Fixed Range MTRR covering the 4K memory space from 0xF0000 - 0xF7FFF.

Note: **NOTE:** Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

4.2.49 Fixed-Range MTRR Format 4K-F8000 (MTRR_FIX4K_F8000_REG_0_0_0_VTDBAR) — Offset 170h

Fixed Range MTRR covering the 4K memory space from 0xF8000 - 0xFFFFF.

Note: **NOTE:** Bit definitions are the same as MTRR_FIX64K_00000_REG_0_0_0_VTDBAR, offset 120h.

4.2.50 Variable-Range MTRR Format Physical Base 0 (MTRR_PHYSBASE0_REG_0_0_0_VTDBAR) — Offset 180h

Variable-Range MTRR BASE0

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 180h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 0
11:8	0h RO	**Reserved**
7:0	00h RO	**MEMTYPE:** Memory type for variable memory type range 0

4.2.51 Variable-Range MTRR Format Physical Mask 0 (MTRR_PHYSMASK0_REG_0_0_0_VTDBAR) — Offset 188h

Variable-Range MTRR MASK0

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 188h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 0
11	0h RO	**VALID:** Valid bit for variable range 0 mask
10:0	0h RO	**Reserved**

4.2.52 Variable-Range MTRR Format Physical Base 1 (MTRR_PHYSBASE1_REG_0_0_0_VTDBAR) — Offset 190h

Variable-Range MTRR BASE1

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 190h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 1
11:8	0h RO	**Reserved**
7:0	00h RO	**MEMTYPE:** Memory type for variable memory type range 1

4.2.53 Variable-Range MTRR Format Physical Mask 1 (MTRR_PHYSMASK1_REG_0_0_0_VTDBAR) — Offset 198h

Variable-Range MTRR MASK1

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 198h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 1
11	0h RO	**VALID:** Valid bit for variable range 1 mask
10:0	0h RO	**Reserved**

4.2.54 Variable-Range MTRR Format Physical Base 2 (MTRR_PHYSBASE2_REG_0_0_0_VTDBAR) — Offset 1A0h

Variable-Range MTRR BASE2

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 1A0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 2
11:8	0h RO	**Reserved**
7:0	00h RO	**MEMTYPE:** Memory type for variable memory type range 2

4.2.55 Variable-Range MTRR Format Physical Mask 2 (MTRR_PHYSMASK2_REG_0_0_0_VTDBAR) — Offset 1A8h

Variable-Range MTRR MASK2

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 1A8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 2
11	0h RO	**VALID:** Valid bit for variable range 2 mask
10:0	0h RO	**Reserved**

4.2.56 Variable-Range MTRR Format Physical Base 3 (MTRR_PHYSBASE3_REG_0_0_0_VTDBAR) — Offset 1B0h

Variable-Range MTRR BASE3

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 1B0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 3
11:8	0h RO	**Reserved**
7:0	00h RO	**MEMTYPE:** Memory type for variable memory type range 3

4.2.57 Variable-Range MTRR Format Physical Mask 3 (MTRR_PHYSMASK3_REG_0_0_0_VTDBAR) — Offset 1B8h

Variable-Range MTRR MASK3

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 1B8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 3
11	0h RO	**VALID:** Valid bit for variable range 3 mask
10:0	0h RO	**Reserved**

4.2.58 Variable-Range MTRR Format Physical Base 4 (MTRR_PHYSBASE4_REG_0_0_0_VTDBAR) — Offset 1C0h

Variable-Range MTRR BASE4

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 1C0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 4
11:8	0h RO	**Reserved**
7:0	00h RO	**MEMTYPE:** Memory type for variable memory type range 4

4.2.59 Variable-Range MTRR Format Physical Mask 4 (MTRR_PHYSMASK4_REG_0_0_0_VTDBAR) — Offset 1C8h

Variable-Range MTRR MASK4

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 1C8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 4
11	0h RO	**VALID:** Valid bit for variable range 4 mask
10:0	0h RO	**Reserved**

4.2.60 Variable-Range MTRR Format Physical Base 5 (MTRR_PHYSBASE5_REG_0_0_0_VTDBAR) — Offset 1D0h

Variable-Range MTRR BASE5

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 1D0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 5
11:8	0h RO	**Reserved**
7:0	00h RO	**MEMTYPE:** Memory type for variable memory type range 5

4.2.61 Variable-Range MTRR Format Physical Mask 5 (MTRR_PHYSMASK5_REG_0_0_0_VTDBAR) — Offset 1D8h

Variable-Range MTRR MASK5

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 1D8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 5
11	0h RO	**VALID:** Valid bit for variable range 5 mask
10:0	0h RO	**Reserved**

4.2.62 Variable-Range MTRR Format Physical Base 6 (MTRR_PHYSBASE6_REG_0_0_0_VTDBAR) — Offset 1E0h

Variable-Range MTRR BASE6

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 1E0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 6
11:8	0h RO	**Reserved**
7:0	00h RO	**MEMTYPE:** Memory type for variable memory type range 6

4.2.63 Variable-Range MTRR Format Physical Mask 6 (MTRR_PHYSMASK6_REG_0_0_0_VTDBAR) — Offset 1E8h

Variable-Range MTRR MASK6

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 1E8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 6
11	0h RO	**VALID:** Valid bit for variable range 6 mask
10:0	0h RO	**Reserved**

4.2.64 Variable-Range MTRR Format Physical Base 7 (MTRR_PHYSBASE7_REG_0_0_0_VTDBAR) — Offset 1F0h

Variable-Range MTRR BASE7

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 1F0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 7
11:8	0h RO	**Reserved**
7:0	00h RO	**MEMTYPE:** Memory type for variable memory type range 7

4.2.65 Variable-Range MTRR Format Physical Mask 7 (MTRR_PHYSMASK7_REG_0_0_0_VTDBAR) — Offset 1F8h

Variable-Range MTRR MASK7

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 1F8h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 7
11	0h RO	**VALID:** Valid bit for variable range 7 mask
10:0	0h RO	**Reserved**

4.2.66 Variable-Range MTRR Format Physical Base 8 (MTRR_PHYSBASE8_REG_0_0_0_VTDBAR) — Offset 200h

Variable-Range MTRR BASE8

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 200h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 8
11:8	0h RO	**Reserved**
7:0	00h RO	**MEMTYPE:** Memory type for variable memory type range 8

4.2.67 Variable-Range MTRR Format Physical Mask 8 (MTRR_PHYSMASK8_REG_0_0_0_VTDBAR) — Offset 208h

Variable-Range MTRR MASK8

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 208h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 8
11	0h RO	**VALID:** Valid bit for variable range 8 mask
10:0	0h RO	**Reserved**

4.2.68 Variable-Range MTRR Format Physical Base 9 (MTRR_PHYSBASE9_REG_0_0_0_VTDBAR) — Offset 210h

Variable-Range MTRR BASE9

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 210h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 9
11:8	0h RO	**Reserved**
7:0	00h RO	**MEMTYPE:** Memory type for variable memory type range 9

4.2.69 Variable-Range MTRR Format Physical Mask 9 (MTRR_PHYSMASK9_REG_0_0_0_VTDBAR) — Offset 218h

Variable-Range MTRR MASK9

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 218h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 9
11	0h RO	**VALID:** Valid bit for variable range 9 mask
10:0	0h RO	**Reserved**

4.2.70 Fault Recording Register Low [0] (FRCDL_REG_0_0_0_VTDBAR) — Offset 400h

Register to record fault information when primary fault logging is active. Hardware reports the number and location of fault recording registers through the Capability register. This register is relevant only for primary fault logging

This register is sticky and can be cleared only through power good reset or by software clearing the RW1C fields by writing a 1.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 400h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:12	00000000 00000h RO/V	**Fault Info (FI):** When the Fault Reason (FR) field indicates one of the address translation fault conditions, bits 63:12 of this field contains the page address in the faulted request. When PASID Present field is 0 (i.e, faulted request is a request without PASID), hardware treat bits 63:N as reserved (0), where N is the maximum guest address width (MGAW) supported. For requests-withPASID (PASID Present field = 1), hardware treats bits 63:N as reserved (0), where N corresponds to the largest AGAW value supported by hardware. When the Fault Reason (FR) field indicates interrupt-remapping fault conditions other than Fault Reason 25h, bits 63:48 of this field indicate the interrupt_index computed for the faulted interrupt request, and bits 47:12 are cleared. When the Fault Reason (FR) field indicates interrupt-remapping fault condition of blocked Compatibility mode interrupt (Fault Reason 25h), contents of this field is undefined. This field is relevant only when the F field is Set.
11:0	0h RO	**Reserved**

4.2.71 Fault Recording Register High [0] (FRCDH_REG_0_0_0_VTDBAR) — Offset 408h

Register to record fault information when primary fault logging is active. Hardware reports the number and location of fault recording registers through the Capability register. This register is relevant only for primary fault logging

This register is sticky and can be cleared only through power good reset or by software clearing the RW1C fields by writing a 1.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 408h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/1C	**F:** Hardware sets this field to indicate a fault is logged in this Fault Recording register. The F field is set by hardware after the details of the fault is recorded in other fields When this field is Set, hardware may collapse additional faults from the same source-id (SID) Software writes the value read from this field to Clear it.

Bit Range	Default & Access	Field Name (ID): Description
62	0h RO/V	**T:** Type of the faulted request: • 0=0: Write request or Page (PRS) Request • 1=1: Read request or AtomicOp request This field is relevant only when the F field is Set, and when the fault reason (FR) indicates one of the DMA-remapping fault conditions.
61:60	0h RO/V	**Address Type (AT):** This field captures the AT field from the faulted DMA request Hardware implementations not supporting Device-IOTLBs (DI field Clear in Extended Capability register) treat this field as RsvdZ When supported, this field is valid only when the F field is Set, and when the fault reason (FR) indicates one of the DMA-remapping fault conditions.
59:40	00000h RO/V	**PASID Value (PV):** PASID value in the faulted request. This field is relevant only when the PP field is set. Hardware implementations not supporting PASID (PASID field Clear in Extended Capability register) implement this field as RsvdZ.
39:32	00h RO/V	**Fault Reason (FR):** Reason for the fault This field is relevant only when the F field is set.
31	0h RO/V	**PASID Present (PP):** When set, indicates the faulted request has a PASID tag. The value of the PASID field is reported in the PASID Value (PV) field. This field is relevant only when the F field is Set, and when the fault reason (FR) indicates one of the non-recoverable address translation fault conditions. Hardware implementations not supporting PASID (PASID field Clear in Extended Capability register) implement this field as RsvdZ.
30	0h RO/V	**Execute Permission Requested (EXE):** When set, indicates Execute permission was requested by the faulted read request. This field is relevant only when the PP field and T field are both Set. Hardware implementations not supporting PASID (PASID field Clear in Extended Capability register) implement this field as RsvdZ.
29	0h RO/V	**Privilege Mode Requested (PRIV):** When set, indicates Supervisor privilege was requested by the faulted request. This field is relevant only when the PP field is Set. Hardware implementations not supporting PASID (PASID field Clear in Extended Capability register) implement this field as RsvdZ.
28:16	0h RO	**Reserved**
15:0	0000h RO/V	**Source Identifier (SID):** Requester-id associated with the fault condition This field is relevant only when the F field is set.

4.2.72 Invalidate Address Register (IVA_REG_0_0_0_VTDBAR) — Offset 500h

Register to provide the DMA address whose corresponding IOTLB entry needs to be invalidated through the corresponding IOTLB Invalidate register. This register is a write-only register.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 500h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:12	00000000 00000h RW	**ADDR:** Software provides the DMA address that needs to be page-selectively invalidated. To make a page-selective invalidation request to hardware, software must first write the appropriate fields in this register, and then issue the appropriate page-selective invalidate command through the IOTLB_REG. Hardware ignores bits 63:N, where N is the maximum guest address width (MGAW) supported. A value retuned on a read of this field is undefined A value returned on a read of this field is undefined
11:7	0h RO	**Reserved**
6	0h RW	**Invalidation Hint (IH):** The field provides hint to hardware about preserving or flushing the non-leaf (page-directory) entries that may be cached in hardware: • 0 = Software may have modified both leaf and non-leaf page-table entries corresponding to mappings specified in the ADDR and AM fields. On a page-selective invalidation request, hardware must flush both the cached leaf and non-leaf page-table entries corresponding to the mappings specified by ADDR and AM fields. • 1 = Software has not modified any non-leaf page-table entries corresponding to mappings specified in the ADDR and AM fields. On a page-selective invalidation request, hardware may preserve the cached non-leaf page-table entries corresponding to mappings specified by ADDR and AM fields. A value returned on a read of this field is undefined
5:0	00h RW	**Address Mask (AM):** The value in this field specifies the number of low order bits of the ADDR field that must be masked for the invalidation operation. This field enables software to request invalidation of contiguous mappings for size-aligned regions. For example:..Mask ADDR bits Pages..Value masked invalidated.. 0 None 1.. 1 12 2.. 2 13:12 4.. 3 14:12 8.. 4 15:12 16 When invalidating mappings for super-pages, software must specify the appropriate mask value. For example, when invalidating mapping for a 2MB page, software must specify an address mask value of at least 9...Hardware implementations report the maximum supported mask value through the Capability register.

4.2.73 IOTLB Invalidate Register (IOTLB_REG_0_0_0_VTDBAR) — Offset 508h

Register to invalidate IOTLB. The act of writing the upper byte of the IOTLB_REG with IVT field Set causes the hardware to perform the IOTLB invalidation.

Type	Size	Offset	Default
MMIO	64 bit	GFXVTBAR + 508h	0200000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/V	**Invalidate IOTLB (IVT):** Software requests IOTLB invalidation by setting this field. Software must also set the requested invalidation granularity by programming the IIRG field Hardware clears the IVT field to indicate the invalidation request is complete. Hardware also indicates the granularity at which the invalidation operation was performed through the IAIG field. Software must not submit another invalidation request through this register while the IVT field is Set, nor update the associated Invalidate Address register Software must not submit IOTLB invalidation requests when there is a context-cache invalidation request pending at this remapping hardware unit. Hardware implementations reporting write-buffer flushing requirement (RWBF=1 in Capability register) must implicitly perform a write buffer flushing before invalidating the IOTLB.
62	0h RO	**Reserved**
61:60	0h RW	**IOTLB Invalidation Request Granularity (IIRG):** When requesting hardware to invalidate the IOTLB (by setting the IVT field), software writes the requested invalidation granularity through this field. The following are the encodings for the field • 00 = Reserved • 01 = Global invalidation request • 10 = Domain-selective invalidation request. The target domain-id must be specified in the DID field • 11 = Page-selective invalidation request. The target address, mask and invalidation hint must be specified in the Invalidate Address register, and the domain-id must be provided in the DID field Hardware implementations may process an invalidation request by performing invalidation at a coarser granularity than requested. Hardware indicates completion of the invalidation request by clearing the IVT field. At this time, the granularity at which actual invalidation was performed is reported through the IAIG field
59	0h RO	**Reserved**
58:57	1h RO/V	**IOTLB Actual Invalidation Granularity (IAIG):** Hardware reports the granularity at which an invalidation request was processed through this field when reporting invalidation completion (by clearing the IVT field). The following are the encodings for this field • 00 = Reserved. This indicates hardware detected an incorrect invalidation request and ignored the request. Examples of incorrect invalidation requests include detecting an unsupported address mask value in Invalidate Address register for page-selective invalidation requests • 01 = Global Invalidation performed. This could be in response to a global, domain-selective, or page-selective invalidation request • 10 = Domain-selective invalidation performed using the domain-id specified by software in the DID field. This could be in response to a domain-selective or a page-selective invalidation request • 11 = Domain-page-selective invalidation performed using the address, mask and hint specified by software in the Invalidate Address register and domain-id specified in DID field. This can be in response to a page-selective invalidation request.

Bit Range	Default & Access	Field Name (ID): Description
56:50	0h RO	**Reserved**
49	0h RW	**Drain Reads (DR):** This field is ignored by hardware if the DRD field is reported as clear in the Capability register. When the DRD field is reported as Set in the Capability register, the following encodings are supported for this field: • 0 = Hardware may complete the IOTLB invalidation without draining any translated DMA read requests • 1 = Hardware must drain DMA read requests.
48	0h RW	**Drain Writes (DW):** This field is ignored by hardware if the DWD field is reported as Clear in the Capability register. When the DWD field is reported as Set in the Capability register, the following encodings are supported for this field: • 0 = Hardware may complete the IOTLB invalidation without draining DMA write requests • 1 = Hardware must drain relevant translated DMA write requests.
47:32	0000h RW	**DID:** Indicates the ID of the domain whose IOTLB entries need to be selectively invalidated. This field must be programmed by software for domain-selective and page-selective invalidation requests. The Capability register reports the domain-id width supported by hardware. Software must ensure that the value written to this field is within this limit. Hardware ignores and not implements bits 47:(32+N), where N is the supported domain-id width reported in the Capability register.
31:0	0h RO	**Reserved**

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5 Dynamic Tuning Technology Registers (D4:F0)

Dynamic Tuning Technology device. This section contains the registers in Bus: 0, Device: 4, Function: 0.

5.1 Summary of Registers

Table 5-1. Summary of Bus: 0, Device: 4, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	2	VID PCI (VID_0_4_0_PCI)	8086h
2h	2	DID PCI (DID_0_4_0_PCI)	461Dh
4h	2	PCICMD PCI (PCICMD_0_4_0_PCI)	0000h
6h	2	PCISTS PCI (PCISTS_0_4_0_PCI)	0090h
8h	1	RID PCI (RID_0_4_0_PCI)	00h
9h	1	CC PCI (CC_0_4_0_PCI)	00h
Ah	2	CC NOPI PCI (CC_0_4_0_NOPI_PCI)	1180h
Ch	1	CLS PCI (CLS_0_4_0_PCI)	00h
Dh	1	MLT PCI (MLT_0_4_0_PCI)	00h
Eh	1	HDR PCI (HDR_0_4_0_PCI)	00h
Fh	1	BIST PCI (BIST_0_4_0_PCI)	00h
10h	8	TMBAR PCI (TMBAR_0_4_0_PCI)	0000000000000004h
2Ch	2	SVID PCI (SVID_0_4_0_PCI)	0000h
2Eh	2	SID PCI (SID_0_4_0_PCI)	0000h
34h	1	CAPPOINT PCI (CAPPOINT_0_4_0_PCI)	90h
3Ch	1	INTRLINE PCI (INTRLINE_0_4_0_PCI)	00h
3Dh	1	INTRPIN PCI (INTRPIN_0_4_0_PCI)	01h
3Eh	1	MINGNT PCI (MINGNT_0_4_0_PCI)	00h
3Fh	1	MAXLAT PCI (MAXLAT_0_4_0_PCI)	00h
54h	4	DEVEN PCI (DEVEN_0_4_0_PCI)	0003D4DFh
E4h	4	CAPID0_A PCI (CAPID0_A_0_4_0_PCI)	00000000h
E8h	4	CAPID0_B PCI (CAPID0_B_0_4_0_PCI)	00000000h

5.1.1 VID PCI (VID_0_4_0_PCI) — Offset 0h

This register combined with the Device Identification register uniquely identifies any PCI

device.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:4, F:0] + 0h	8086h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RO	**VID:** PCI standard identification for Intel.

5.1.2 DID PCI (DID_0_4_0_PCI) — Offset 2h

This register combined with the Vendor Identification register uniquely identifies any PCI

device.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:4, F:0] + 2h	461Dh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	461Dh RW/V/L	**DID:** Identifier assigned to the Thermal Management Controller.

5.1.3 PCICMD PCI (PCICMD_0_4_0_PCI) — Offset 4h

This register provides basic control over the Camarillo devices ability to respond to PCI cycles.

The PCICMD Register in the Camarillo disables the Camarillo PCI compliant initiator accesses to main

memory.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:4, F:0] + 4h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**Reserved**
10	0h RW	**INTDIS:** This bit, when set, disables the device from asserting INTA#.
9	0h RO	**FB2B:** The Camarillo device does not implement this bit and it is hardwired to a 0.
8	0h RO	**SERRE:** The Camarillo device does not implement this bit and it is hardwired to a 0.
7	0h RO	**ADSTEP:** The Camarillo device does not implement this bit and it is hardwired to a 0.
6	0h RO	**PERRE:** This bit is hardwired to 0. The Camarillo Device belongs to the category of devices that does not corrupt programs or data in system memory or hard drives. It therefore ignores any parity error that it detects and continues with normal operation.
5	0h RO	**VGASNOOP:** The Camarillo device does not implement this bit and it is hardwired to a 0.
4	0h RO	**MWIE:** This bit is hardwired to 0. The Camarillo Device will never issue memory write and invalidate commands, and therefore has no need to implement this bit.
3	0h RO	**SCE:** The Camarillo device does not implement this bit and it is hardwired to a 0.
2	0h RW	**BME:** The Camarillo Device is enabled to function as a PCI-compliant bus initiator when this bit is set. If it is not set, bus initiator is disabled.
1	0h RW	**MAE:** The Camarillo Device will allow access to thermal registers when this bit is set. If it is not set, access to memory mapped thermal registers is disabled.
0	0h RO	**IOAE:** The Camarillo device does not implement this bit and it is hardwired to a 0.

5.1.4 PCISTS PCI (PCISTS_0_4_0_PCI) — Offset 6h

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant Initiator Abort (MA)

and PCI compliant Target Abort (TA). PCISTS also indicates the DEVSEL# timing that has been set by the Camarillo

Device.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:4, F:0] + 6h	0090h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**DPE:** The Camarillo device does not implement this bit and it is hardwired to a 0.
14	0h RO	**SSE:** This bit is hardwired to zero. The Camarillo Device never asserts SERR#, and therefore it has no need to implement this bit.
13	0h RO	**RURS:** The Camarillo device does not implement this bit and it is hardwired to a 0.
12	0h RO	**RCAS:** The Camarillo device does not implement this bit and it is hardwired to a 0.
11	0h RO	**STAS:** his bit is hardwired to 0. The Camarillo Device will not generate a Target Abort DMI completion packet or Special Cycle, and therefore it has no need to implement this bit.
10:9	0h RO	**DEVT:** These bits are hardwired to 0. Device 4 does not physically connect to PCI_A.
8	0h RO	**DPD:** This bit is hardwired to 0. PERR signaling and messaging are not implemented by the Camarillo Device, and therefore it has no need to implement this bit.
7	1h RO	**FB2B:** This bit is hardwired to 1. Device 4 does not physically connect to PCI_A, so this bit is set to 1 (indicating fast back-to-back capability) so that the optimum setting for PCI_A is not limited by the Camarillo Device.
6	0h RO	**Reserved**
5	0h RO	**PCI66M:** The Camarillo device does not implement this bit and it is hardwired to a 0.
4	1h RO	**CLIST:** This bit is set to 1 to indicate that the register at 34h provides an offset into the function. PCI Configuration Space containing a pointer to the location of the first item in the list.
3	0h RW/V/L	**IS:** Reflects the state of the INTA# signal at the input of the enable/disable circuit. This bit is set by HW to 1 when the INTA# is asserted and reset by HW to 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the 0.4.0.PCICMD register).

Bit Range	Default & Access	Field Name (ID): Description
2:0	0h RO	**Reserved**

5.1.5 RID PCI (RID_0_4_0_PCI) — Offset 8h

This register contains the revision number of the Camarillo Device. This is an 8-bit value that

indicates the revision identification number for the device. For the A-0 Stepping, this value is

00h.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:4, F:0] + 8h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RW/L	**RID MSB (RID_MSB):** Revision ID MSB.
3:0	0h RW/L	**RID:** Camarilo device Revision ID.

5.1.6 CC PCI (CC_0_4_0_PCI) — Offset 9h

This register contains the device programming interface information related to the Sub-Class Code and

Base Class Code definition for the Camarillo Device. This register also contains the Base Class Code and the

function sub-class in relation to the Base Class Code.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:4, F:0] + 9h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**PI:** This is an 8-bit value that indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

5.1.7 CC NOPI PCI (CC_0_4_0_NOPI_PCI) — Offset Ah

This register contains the device programming interface information related to the Sub-Class Code and

Base Class Code definition for the Camarillo Device. This register also contains the Base Class Code and the

function sub-class in relation to the Base Class Code.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:4, F:0] + Ah	1180h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	11h RO	**BCC:** This is an 8-bit value that indicates the base class code for the Camarillo Thermal Controller. This code has the value 11h, indicating a device that is used for data acquisition and signal processing.
7:0	80h RO	**SUBCC:** The code is 80h which indicates Other Data Acquisition and Signal Processing Controllers.

5.1.8 CLS PCI (CLS_0_4_0_PCI) — Offset Ch

The Camarillo Device does not support this register as a PCI target.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:4, F:0] + Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**CLS:** This field is hardwired to 0. The Camarillo as a PCI compliant initiator does not use the Memory Write and Invalidate command and, in general, does not perform operations based on cache line size.

5.1.9 MLT PCI (MLT_0_4_0_PCI) — Offset Dh

The Camarillo Device does not support the programmability of the initiator latency timer because it does

not perform bursts.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:4, F:0] + Dh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**MLT:** This field is hardwired to 0. The Camarillo Device does not support perform bursts.

5.1.10 HDR PCI (HDR_0_4_0_PCI) — Offset Eh

This register identifies the header layout of the configuration space. No physical register exists at

this location.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:4, F:0] + Eh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**HDR:** This field always returns 0 to indicate that the Camarillo device is a single function device with standard header layout.

5.1.11 BIST PCI (BIST_0_4_0_PCI) — Offset Fh

This register is used for control and status of Built In Self Test (BIST).

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:4, F:0] + Fh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**BS:** This bit is hardwired to zero. The Camarillo Device does not support BIST.
6:0	0h RO	**Reserved**

5.1.12 TMBAR PCI (TMBAR_0_4_0_PCI) — Offset 10h

This is the base address for the Thermal Controller Memory Mapped space. There is no physical memory

within this 32KB window that can be addressed. The 32KB reserved by this register does not alias to any PCI 2.2

compliant memory mapped space. All TMBAR space maps the access to this memory space towards MCHBAR space. For

details of this BAR, refer to the MCHBAR specifications.

Type	Size	Offset	Default
PCI	64 bit	[B:0, D:4, F:0] + 10h	0000000000000004h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:43	0h RO	**Reserved**
42:17	0000000h RW	**TMMBA:** This field corresponds to bits 41 to 16 of the base address TMBAR address space. BIOS will program this register resulting in a base address for a 64KB block of contiguous memory address space. This register ensures that a naturally aligned 64KB space is allocated within total addressable memory space. The Camarillo driver uses this base address to program all Thermal and Throttling control register set.
16:4	0000h RO	**ADM:** Hardwired to 0s to indicate at least 128KB address range.
3	0h RO	**PM:** Hardwired to 0 to prevent prefetching.
2:1	2h RO	**MT:** Hardwired to 10 to indicate 64-bit address.
0	0h RO	**MIOS:** Hardwired to 0 to indicate memory space.

5.1.13 SVID PCI (SVID_0_4_0_PCI) — Offset 2Ch

This value is used to identify the vendor of the subsystem.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:4, F:0] + 2Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/L	**SUBVID:** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only. **Locked by:** WRITE_ONCE_LOCK.SUBVID_WOL

5.1.14 SID PCI (SID_0_4_0_PCI) — Offset 2Eh

This value is used to identify a particular subsystem.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:4, F:0] + 2Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/L	**SUBID:** This field should be programmed during BIOS initialization. After it has been written once, it becomes read only. **Locked by:** WRITE_ONCE_LOCK.SUBID_WOL

5.1.15 CAPPOINT PCI (CAPPOINT_0_4_0_PCI) — Offset 34h

CAPPOINT provides the offset that is the pointer to the location of the first device capability in

the capability list.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:4, F:0] + 34h	90h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	90h RW/V/L	**CAPPV:** This field contains an offset into the functions PCI Configuration Space for the first item in the New Capabilities Linked List which is the MSI Capabilities ID register at address 90h or the Power Management Capabilities ID registers at address D0h. The value is determined by CAPL[0].

5.1.16 INTRLINE PCI (INTRLINE_0_4_0_PCI) — Offset 3Ch

This register specifies which interrupt line this device uses.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:4, F:0] + 3Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**INTCON:** Used to communicate interrupt line routing information. BIOS Requirement: POST software writes the routing information into this register as it initializes and configures the system. The value indicates to which input of the system interrupt controller this devices interrupt pin is connected.

5.1.17 INTRPIN PCI (INTRPIN_0_4_0_PCI) — Offset 3Dh

This register specifies which interrupt pin this device uses.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:4, F:0] + 3Dh	01h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	01h RO	**INTPIN:** As a single function device, the Camarillo device specifies INTA as its interrupt pin. 01h = INTA.

5.1.18 MINGNT PCI (MINGNT_0_4_0_PCI) — Offset 3Eh

This register are hardwired to zero. The Camarillo Device does not burst as a PCI compliant initiator.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:4, F:0] + 3Eh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**MGV:** These bits are hardwired to zero. The Camarillo Device does not burst as a PCI compliant initiator.

5.1.19 MAXLAT PCI (MAXLAT_0_4_0_PCI) — Offset 3Fh

This register are hardwired to zero. The Camarillo Device has no specific requirements for how often it needs to access the PCI bus.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:4, F:0] + 3Fh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**MLV:** These bits are hardwired to zero. The Camarillo Device has no specific requirements for how often it needs to access the PCI bus.

5.1.20 DEVEN PCI (DEVEN_0_4_0_PCI) — Offset 54h

Allows for enabling/disabling of PCI devices and functions that are within the CPU package. The table below the bit definitions describes the behavior of all combinations of transactions to devices controlled by this register. All the bits in this register are Intel TXT Lockable.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:4, F:0] + 54h	0003D4DFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW/L	**D6F1EN:** 0: Bus 0 Device 6 Function 1 is disabled and not visible. 1: Bus 0 Device 6 Function 1 is enabled and visible. This bit will be set to 0b and remain 0b if Device 6 Function 1 capability is disabled. **Locked by:** CAPID0_C_0_0_0_PCI.PEG61D
17	1h RW/L	**D10EN:** 0: Bus 0 Device 10 is disabled and not visible. 1: Bus 0 Device 10 is enabled and visible. This bit will be set to 0b and remain 0b if Device 10 capability is disabled. **Locked by:** CAPID0_B_0_0_0_PCI.DEV10_DISABLED
16	1h RW/L	**D6F2EN:** 0: Bus 0 Device 6 Function 2 is disabled and not visible. 1: Bus 0 Device 6 Function 2 is enabled and visible. This bit will be set to 0b and remain 0b if Device 6 Function 2 capability is disabled. **Locked by:** CAPID0_C_0_0_0_PCI.PEG62D
15	1h RW/L	**D8EN:** 0: Bus 0 Device 8 is disabled and not visible. 1: Bus 0 Device 8 is enabled and visible. This bit will be set to 0b and remain 0b if Device 8 capability is disabled. **Locked by:** CAPID0_B_0_0_0_PCI.GMM_DIS
14	1h RW/L	**D14F0EN:** VMD Enable - 0: Bus 0 Device 14 Function 0 is disabled and hidden. 1: Bus 0 Device 14 Function 0 is enabled and visible. **Locked by:** CAPID0_B_0_0_0_PCI.VMD_DIS
13	0h RW/L	**D6F0EN:** 0: Bus 0 Device 6 Function 0 is disabled and not visible. 1: Bus 0 Device 6 Function 0 is enabled and visible. This bit will be set to 0b and remain 0b if Device 6 Function 0 capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.PEG60D
12	1h RW/L	**D9EN:** 0: Bus 0 Device 9 is disabled and not visible. 1: Bus 0 Device 9 is enabled and visible. This bit will be set to 0b and remain 0b if Device 9 capability is disabled. **Locked by:** CAPID0_B_0_0_0_PCI.NPK_DIS
11	0h RO	**Reserved**
10	1h RW/L	**D5EN:** 0: Bus 0 Device 5 is disabled and not visible. 1: Bus 0 Device 5 is enabled and visible. This bit will be set to 0b and remain 0b if Device 5 capability is disabled. **Locked by:** CAPID0_B_0_0_0_PCI.IMGU_DIS

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RO	**Reserved**
7	1h RW/L	**D4EN:** 0: Bus 0 Device 4 is disabled and not visible. 1: Bus 0 Device 4 is enabled and visible. This bit will be set to 0b and remain 0b if Device 4 capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.CDD
6	1h RW/L	**D3F7EN:** NVMe - Device 3 function 7 enable 0: Bus 0 Device 3 function 7 is disabled and hidden 1: Bus 0 Device 3 function 7 is enabled and visible This bit will be set to 0b and remain 0b if Device 3 capability is disabled. Locked with CAPID0_A_0_0_0_PCI[0].NVME_F7D **Locked by:** CAPID0_A_0_0_0_PCI.NVME_F7D
5	0h RW/L	**D3F0EN:** NVMe - Device 3 function 0 enable 0: Bus 0 Device 3 function 0 is disabled and hidden 1: Bus 0 Device 3 function 0 is enabled and visible This bit will be set to 0b and remain 0b if Device 3 capability is disabled. Locked with CAPID0_A_0_0_0_PCI[31].NVME_F0D **Locked by:** CAPID0_A_0_0_0_PCI.NVME_F0D
4	1h RW/L	**D2EN:** 0: Bus 0 Device 2 is disabled and hidden 1: Bus 0 Device 2 is enabled and visible This bit will be set to 0b and remain 0b if Device 2 capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.IGD
3	1h RW/L	**D1F0EN:** 0: Bus 0 Device 1 Function 0 is disabled and hidden. 1: Bus 0 Device 1 Function 0 is enabled and visible. This bit will be set to 0b and remain 0b if PEG10 capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.PEG10D
2	1h RW/L	**D1F1EN:** 0: Bus 0 Device 1 Function 1 is disabled and hidden. 1: Bus 0 Device 1 Function 1 is enabled and visible. This bit will be set to 0b and remain 0b if: - PEG11 capability is disabled by fuses, OR - PEG11 is disabled by strap (PEG0CFGSEL) **Locked by:** CAPID0_A_0_0_0_PCI.PEG11D
1	1h RW/L	**D1F2EN:** 0: Bus 0 Device 1 Function 2 is disabled and hidden. 1: Bus 0 Device 1 Function 2 is enabled and visible. This bit will be set to 0b and remain 0b if: - PEG12 capability is disabled by fuses, OR - PEG12 is disabled by strap (PEG0CFGSEL) **Locked by:** CAPID0_A_0_0_0_PCI.PEG12D
0	1h RO	**D0EN:** Bus 0 Device 0 Function 0 may not be disabled and is therefore hardwired to 1.

5.1.21 CAPID0_A PCI (CAPID0_A_0_4_0_PCI) — Offset E4h

Control of bits in this register are only required for customer visible SKU differentiation.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:4, F:0] + E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**NVME F0D (NVME_F0D):** 0: Device 3 Function 0 and associated memory spaces are accessible. 1: Device 3 Function 0 (NVMe F0) and associated memory space are disabled by hardwiring the D3F0EN field, bit 5 of the SoC Device Enable register
30	0h RW/L	**PEG12D:** 0: Device 1 Function 2 and associated memory spaces are accessible. 1: Device 1 Function 2 and associated memory and IO spaces are disabled by hardwiring the D1F2EN field, bit 1 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.
29	0h RW/L	**PEG11D:** 0: Device 1 Function 1 and associated memory spaces are accessible. 1: Device 1 Function 1 and associated memory and IO spaces are disabled by hardwiring the D1F1EN field, bit 2 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.
28	0h RW/L	**PEG10D:** 0: Device 1 Function 0 and associated memory spaces are accessible. 1: Device 1 Function 0 and associated memory and IO spaces are disabled by hardwiring the D1F0EN field, bit 3 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.
27	0h RW/L	**PELWUD:** 0: Link width upconfig is supported. The CPU advertises upconfig capability using the data rate symbol in its TS2 training ordered sets during Configuration.Complete. The CPU responds to link width upconfigs initiated by the downstream device. 1: Link width upconfig is NOT supported. The CPU does not advertise upconfig capability using the data rate field in TS2 training ordered sets during Configuration.Complete. The CPU does not respond to link width upconfigs initiated by the downstream device.
26	0h RW/L	**DW:** 0: DMI x4 1: DMI x2
25	0h RW/L	**ECCDIS:** 0b ECC capable 1b Not ECC capable
24	0h RW/L	**FDEE:** 0: DRAM ECC optional via software. 1: DRAM ECC enabled. MCHBAR C0MISCCTL bit [0] and C1MISCCTL bit [0] are forced to 1 and Read-Only. Note that FDEE and ECCDIS must not both be set to 1.
23	0h RW/L	**VTDD:** 0: Enable VTd 1: Disable VTd
22	0h RW/L	**DMIG2DIS:** 0: Capable of running DMI in Gen 2 mode 1: Not capable of running DMI in Gen 2 mode

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**Reserved**
20:19	0h RW/L	**DDRSZ:** This field defines the maximum allowed memory size per channel. 00b Unlimited (64GB per channel) 01b Maximum 8GB per channel 10b Maximum 4GB per channel 11b Maximum 2GB per channel
18	0h RW/L	**PEG60D:** Spare
17	0h RW/L	**D1NM:** 0: Part is capable of supporting 1n mode timings on the DDR interface. 1: Part is not capable of supporting 1n mode. Only supported timings are 2n or greater.
16	0h RW/L	**FUFRD:** Controls how much ULT information is available to debugging software via configuration transactions. 0: Full ULT information is available, including Wafer, X, and Y location. 1: ULT information is hidden. All ULT information will read out as zeros.
15	0h RW/L	**CDD:** 0: Camarillo Device enabled. 1: Camarillo Device disabled.
14	0h RW/L	**DDPCD:** Allows Dual Channel operation but only supports 1 DIMM per channel. 0: 2 DIMMs per channel enabled 1: 2 DIMMs per channel disabled. This setting hardwires bits 2 and 3 of the rank population field for each channel to zero. (MCHBAR offset 260h, bits 22-23 for channel 0 and MCHBAR offset 660h, bits 22-23 for channel 1)
13	0h RW/L	**X2APIC ENABLE (X2APIC_EN):** Extended Interrupt Mode. 0b: Hardware does not support Extended APIC mode. 1b: Hardware supports Extended APIC mode.
12	0h RW/L	**PDCD:** 0: Capable of Dual Channels 1: Not Capable of Dual Channel - only single channel capable.
11	0h RW/L	**IGD:** 0: There is a graphics engine within this CPU. Internal Graphics Device (Device 2) is enabled and all of its memory and I/O spaces are accessable. Configuration cycles to Device 2 will be completed within the CPU. All non-SMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2 and IO registers within Device 2 and VGA Enable of the PCI to PCI bridge control register in Devices 1 and 6 (If PCI Express GFX attach is supported). A selected amount of Graphics Memory space is pre-allocated from the main memory based on Graphics Mode Select (GMS in the GGC Register). Graphics Memory is pre-allocated above TSEG Memory. 1: There is no graphics engine within this CPU. Internal Graphics Device (Device 2) and all of its memory and I/O functions are disabled. Configuration cycle targeted to Device 2 will be passed on to DMI. In addition, all clocks to internal graphics logic are turned off. All non-SMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control register in Devices 1 and 6. DEVEN [4:3] (Device 0, offset 54h) have no meaning. Device 2 Functions 0 and 1 are disabled and hidden.
10	0h RW/L	**DID0OE:** 0b Disable ability to override DID0 - For production 1b Enable ability to override DID - For debug and samples only

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**Reserved**
8	0h RW/L	**SXP 2LM SUPPORTED (SXP_2LM_SUPPORTED):** 2LM is supported by this product.
7:4	0h RW/L	**CRID:** Compatibility Rev ID: PCODE will update this field with the value of FUSE_CRID.
3	0h RW/L	**DDR OVERCLOCK (DDR_OVERCLOCK):** DDR overclocking. PCODE will update this field with the value of FUSE_DDR_OC_EN.
2	0h RO	**Reserved**
1	0h RW/L	**NVME F7D (NVME_F7D):** 0: Device 3 Function 7 and associated memory spaces are accessible. 1: Device 3 Function 7 (NVMe F7) and associated memory space are disabled by hardwiring the D3F7EN field, bit 6 of the SoC Device Enable register
0	0h RO	**Reserved**

5.1.22 CAPID0_B PCI (CAPID0_B_0_4_0_PCI) — Offset E8h

Control of bits in this register are only required for customer visible SKU differentiation.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:4, F:0] + E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**IMGU DISABLE (IMGU_DIS):** 0: Device 5 associated memory spaces are accessible. 1: Device 5 associated memory and IO spaces are disabled by hardwiring the D1F2EN field, bit 1 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.
30	0h RW/L	**NPK DISABLE (NPK_DIS):** 0: NPK associated memory spaces are accessible. 1: NPK associated memory and IO spaces are disabled by hardwiring the D1F2EN field, bit 1 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.

Bit Range	Default & Access	Field Name (ID): Description
29	0h RW/L	**OC ENABLED (OC_ENABLED):** PCODE will update this field with the value of FUSE_OC_ENABLED. 0b Over-clocking is Disabled 1b Over-clocking is Enabled If over-clocking is enabled, FUSE_OC_BINS contains how many bits of over-clocking are supported. The encoding is as follows: 0h Overclocking is Disabled 1h Max 1 bin of overclocking is supported 2h Max 2 bin of overclocking is supported 3h Max 3 bin of overclocking is supported 4h Max 4 bin of overclocking is supported 5h Max 5 bin of overclocking is supported 6h Max 6 bin of overclocking is supported 7h Unlimited If overclocking is not enabled, FUSE_OC_BINS is meaningless, and should be 0.
28	0h RW/L	**SMT:** This setting indicates whether or not the CPU is SMT capable.
27:25	0h RW/L	**CACHESZ:** This setting indicates the supporting cache sizes.
24	0h RW/L	**SVM DISABLE (SVM_DISABLE):** Consumed by Display.
23:21	0h RW/L	**PLL REF100 CFG (PLL_REF100_CFG):** DDR3 Maximum Frequency Capability with 100 Memory. PCODE will update this field with the value of FUSE_PLL_REF100_CFG and then apply SSKU overrides. Maximum allowed memory frequency with 100 MHz ref clk. Also serves as defeature. Unlike 133 MHz ref fuses, these are normal 3 bit field 0 - 100 MHz ref disabled 1 - upto DDR-1400 (7 x 200) 2 - upto DDR-1600 (8 x 200) 3 - upto DDR-1800 (8 x 200) 4 - upto DDR-2000 (10 x 200) 5 - upto DDR-2200 (11 x 200) 6 - upto DDR-2400 (12 x 200) 7 - no limit (but still limited by _DDR_FREQ200 to 2600)
20	0h RW/L	**PEGG3 DISABLE (PEGG3_DIS):** PCIe Gen 3 Disable fuse. This fuse will be strap selectable/modifiable to enable SSKU capabilities. This is a defeature fuse -- an un-programmed device should have PCIe Gen 3 capabilities enabled. 0: Capable of running any of the Gen 3-compliant PEG controllers in Gen 3 mode (Devices 0/1/0, 0/1/1, 0/1/2) 1: Not capable of running any of the PEG controllers in Gen 3 mode
19	0h RW/L	**PKGTYP:** This setting indicates the CPU Package Type.
18:17	0h RO	**Reserved**
16	0h RW/L	**PEGX16D:** 0: Capable of x16 PEG Port 1: Not Capable of x16 PEG port, instead PEG limited to x8 and below. Causes PEG port to enable and train logical lanes 7:0 only. Logical lanes 15:8 are powered down (unless in use by the other PEG port or the embedded Display Port), and the Max Link Width field of the Link Capability register reports x8 instead of x16. (In the case of lane reversal, lanes 15:8 are active and lanes 7:0 are powered down.)
15	0h RW/L	**DMIG3DIS:** DMI Gen 3 Disable fuse.
14:12	0h RW/L	**LTECH:** 2L Technology. 3'b000 - 1LM; 3'b001 - EDRAM0; 3'b011 - EDRAM0+1; 3'b100 - 2LM

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/L	**HDCPD:** 0 - Capable of HDCP 1 - HDCP Disabled
10	0h RW/L	**DEV10 DISABLED (DEV10_DISABLED):** Device 10 Disable. 0 - Device 10 Enable 1- Device 10 Disable
9	0h RO	**Reserved**
8	0h RW/L	**GMM DISABLE (GMM_DIS):** 0: Device 8 associated memory spaces are accessible. 1: Device 8 associated memory and IO spaces are disabled by hardwiring the D8EN field, bit 1 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to 0.
7	0h RW/L	**DDD:** 0 - Debug mode 1 - Production mode
6:4	0h RO	**Reserved**
3	0h RW/L	**SH_OPI ENABLE (SH_OPI_EN):** Switch hitter, OPI enabled. 1 - OPI is enabled for H SKU 0 - DMI is enabled for H SKU
2	0h RW/L	**VMD DISABLE (VMD_DIS):** Only for S&H, Indicates if VMD is disabled.
1	0h RW/L	**DPEGFX1:** This bit has no effect on Device 1 unless Device 1 is configured for at least two ports via PEG0CFGSEL strap. 0b All PEG port widths do not depend on their respective BCTRL[VGAEN]. 1b Each PEG port width is limited to x1 operation when its respective BCTRL[VGAEN] is set to 1b.
0	0h RW/L	**SPEGFX1:** This bit has no effect on Device 1 unless Device 1 is configured for a single port via PEG0CFGSEL strap. 0b PEG10 width does not depend on its BCTRL[VGAEN]. 1b PEG10 width is limited to x1 operation when its respective BCTRL[VGAEN] is set to 1b.

6 Image Processing Unit Registers (D5:F0)

This chapter documents the registers in Bus: 0, Device: 5, Function: 0.

6.1 Summary of Registers

Table 6-1. Summary of Bus: 0, Device: 5, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	VID DID (VID_DID)	00008086h
4h	4	PCICMD PCISTS (PCICMD_PCISTS)	00100000h
8h	4	RID CC (RID_CC)	04800000h
Ch	4	CLS MLT HT BIST (CLS_MLT_HT_BIST)	00000000h
10h	4	ISPMMADR LOW (ISPMMADR_LOW)	00000004h
14h	4	ISPMMADR HIGH (ISPMMADR_HIGH)	00000000h
2Ch	4	SVID SID (SVID_SID)	00000000h
34h	4	CAPPOINT reg (CAPPOINT)	00000070h
3Ch	4	INTR reg (INTR)	00000100h
70h	4	PCIECAPHDR PCIECAP (PCIECAPHDR PCIECAP) — Offset 70h	0092D010h
74h	4	Device CAP (DEVICECAP)	10008020h
78h	4	DEVICECTL DEVICESTS (DEVICECTL_DEVICESTS)	00000000h
ACh	4	MSI CAPID (MSI_CAPID)	0080D005h
B0h	4	MSI Address low (MSI_ADDRESS_LO)	00000000h
B4h	4	MSI Address high (MSI_ADDRESS_HI)	00000000h
B8h	4	MSI Data (MSI_DATA)	00000000h
D0h	4	PMCAP reg (PMCAP)	00030001h
D4h	4	PMCS reg (PMCS)	00000008h
F0h	4	IPUVTDBAR LOW (IPUVTDBAR_LOW)	00000000h
F4h	4	IPUVTDBAR HIGH (IPUVTDBAR_HIGH)	00000000h

6.1.1 VID DID (VID_DID) — Offset 0h

VID_DID - Vendor ID and Device ID Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:5, F:0] + 0h	00008086h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO/V	**DID:** Device Identification Number Low (DID_LOW): Lower 2 bits of Iunit Device ID. Connected to fuse isp_device_id
15:0	8086h RO	**VENDOR_ID:** Vendor Identification Number (VID): PCI standard identification for Intel.

6.1.2 PCICMD PCISTS (PCICMD_PCISTS) — Offset 4h

CMD_STS- Command and Status Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:5, F:0] + 4h	00100000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	0h RO/V	**SERR_STS:** SERR status
29	0h RW/1C/V	**RMA:** Received Initiator Abort (MA): Set when IUNIT recieve UR
28	0h RW/1C/V	**RTA:** Received Target Abort (RTA): Set when IUNIT recieve CA
27	0h RW/1C/V	**STA:** Signaled Target Abort (STA): Set when IUNIT recieve P/NP transaction which is CA
26:21	0h RO	**Reserved**
20	1h RO	**CAPLIST:** Capability List (CAP): Indicates that the CAPPOINT register at 34h provides an offset into PCI Configuration Space containing a pointer to the location of the first item in the list.
19	0h RO/V	**INTA_STATUS:** Interrupt Status (IS): Reflects the state of the interrupt in the camera device. Is set to 1 if IER and IIR are both set. Otherwise is set to 0.

Bit Range	Default & Access	Field Name (ID): Description
18:11	0h RO	**Reserved**
10	0h RW	**INTA_DISABLE:** Interrupt Disable (ID): When 1, blocks the sending of ASSERT_INTA and DEASSERT_INTA messages to the Intel Legacy Block (ILB). The interrupt status is not blocked from being reflected in PCICMDSTS.IS. When 0, permits the sending of ASSERT_INTA and DEASSERT_INTA messages to the ILB.
9	0h RO	**FASTB2B:**
8	0h RO	**SERR_EN:**
7	0h RO	**Reserved**
6	0h RO	**PARITY_ERR:**
5	0h RO	**VGA_SNP:**
4	0h RO	**MWRINV:**
3	0h RO	**SPECIAL_CYCLE:**
2	0h RW	**BME:** Bus Initiator Enable (BME): Enables ISP to function as a PCI compliant initiator. When 0, blocks the sending of MSI interrupts. When 1, permits the sending of MSI interrupts.
1	0h RW	**MSE:** Memory Space Enable (MSE): When set, accesses to this device's memory space is enabled. When 1, the ISP will compare the incoming address on the IOSF bus with ISPMMADR_BAR(31:22). If there is a match and if the IOSF command is either a MEMRD or MEMWR, the ISP will select the command and direct it to internally addressed entity. When 0, the ISP will not claim MEMRD or MEMWR IOSF commands.
0	0h RO	**IOAE:** IO Space Enable - IUNIT doesn't expect to get IO commands.

6.1.3 RID CC (RID_CC) — Offset 8h

RID_CC - Revision ID and Class Code Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:5, F:0] + 8h	04800000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	04h RO	**BASECLASS_CODE:** Base-Class Code (BCC): 04h indicates a multimedia device

Bit Range	Default & Access	Field Name (ID): Description
23:16	80h RO	**SUBCLASS_CODE:** Sub-Class Code: (SCC): 80h indicates a video device
15:8	00h RO	**PROGRAMMING_INTERFACE:** Programming Interface (PI): Default programming interface
7:0	00h RO/V	**REVISION_ID:** Revision ID (RID): The value in this field is set by the setIDValue message

6.1.4 CLS MLT HT BIST (CLS_MLT_HT_BIST) — Offset Ch

CLS_MLT_HT_BIST - Cache Line Size, Initiator Latency Timer, Header Type and BIST Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:5, F:0] + Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**BIST:** Built In Self Test
23:16	00h RO	**HEADER_TYPE:** Header Type (HDR): Indicates a type 0 header format.
15:8	00h RO	**LATENCY_TIMER:** Latency Timer
7:0	00h RW	**CACHELINE_SIZE:** Cache Line Size: Value is ignored. This field is implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no effect on any PCI Express device behavior.

6.1.5 ISPMMADR LOW (ISPMMADR_LOW) — Offset 10h

BAR_LOW - Low Part of Base Address Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:5, F:0] + 10h	00000004h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**BASE_ADDR:** Base Address (BA): Set by the OS, these bits correspond to address signals (31:24). The ISP will compare the IOSF address (38:24) with {ISPMMADR_BAR_HI(6:0), ISPMMADR_BAR_LO(31:24)}. If there is a match, and PCICMDSTS(1) = MSE = 1 and the IOSF command is either a MEMRD or MEMWR, the ISP will select the command and direct it to internally addressed entity.
23:4	00000h RO	**ADDR_MASK:** Address Mask: Hardwired to 0s to indicate at least 16MB address range
3	0h RO	**PREFETCHABLE:** Prefetchable Memory: Hardwired to 0 to prevent prefetching
2:1	2h RO	**TYPE:** Memory Type - 2h indicates 64 bit wide addressing
0	0h RO	**MESSAGE_SPACE:** Message Space - 0h indicates memory space

6.1.6 ISPMMADR HIGH (ISPMMADR_HIGH) — Offset 14h

BAR_HIGH - High Part of Base Address Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:5, F:0] + 14h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**BASE_ADDR:** Base Address MSB

6.1.7 SVID SID (SVID_SID) — Offset 2Ch

SVID_SID - Subsystem Vendor ID and Subsystem ID Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:5, F:0] + 2Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**SUBSYSTEM_ID:** Subsystem ID (SSID): Written by BIOS after reset, can be changed only after a reset cycle
15:0	0000h RW/O	**SUBSYSTEM_VENDOR_ID:** Subsystem Vendor ID (SSVID):Written by BIOS after reset, can be changed only after a reset cycle

6.1.8 CAPPOINT reg (CAPPOINT) — Offset 34h

CAPPTR - Capabilities Pointer Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:5, F:0] + 34h	00000070h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	70h RO	**CAPABILITY_PTR:** Capabilities Pointer (CAP): CAPABILITIES_POINTER: This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List, the CAPID0 register at offset 70h

6.1.9 INTR reg (INTR) — Offset 3Ch

INTR - Interrupt Properties Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:5, F:0] + 3Ch	00000100h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**MAXLAT:** MaxLat
23:16	00h RO	**MINLAT:** MinLat
15:8	01h RO	**INTERRUPT_PIN:** Interrupt Pin (IPIN): PCI Device 0/3/0 (IUNIT) is a single function device. If INTx is used, the PCI spec requires that it use INTA# this pin is hardcoded yo 8'h01 - signifies inta is used.
7:0	00h RW	**INTERRUPT_LINE:** Interrupt Line (ILIN): BIOS written value to communicate interrupt line routing information to the ISP device driver.

6.1.10 PCIECAPHDR PCIECAP (PCIECAPHDR PCIECAP) — Offset 70h

PCIE Capabilities Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:5, F:0] + 70h	0092D010h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0092h RO	**PCIE_CAP:** PCIE_CAP: Bits 31:30: Reserved, 0 Bits 29:25: Interrupt Message Number (INTMSG): Since this device only supports one MSI vector, this field is hardwired to 0. Bit 24: Slot Implemented (SLOTIMP): Hardwired to 0 for any endpoint device. Bits 23:20: DevicePort Type: Indicates the specific type of this PCI Express function. 1001b indicates a Root Complex Integrated Endpoint Bits 19:16 Capability Version: Must be hardwired to 2h for Functions compliant to PCI Express 3.0 Base Specification.

Bit Range	Default & Access	Field Name (ID): Description
15:8	D0h RO/V	**NEXT_PTR:** Next Capability Pointer: (PCIE_NEXT_CAP): Indicates the next item in the capabilities list or 00h if no other items exist in the linked list of capabilities. actual value will set by PCI_CTRL_type register
7:0	10h RO	**CAPABILITY_ID:** Capability ID (PCIE_CAPID): Indicates the PCI Express Capability structure. This field must return a Capability ID of 10h indicating that this is a PCI Express Capability structure

6.1.11 Device CAP (DEVICECAP) — Offset 74h

Capabilities Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:5, F:0] + 74h	10008020h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	1h RO/V	**FLRCAP:** FLRCAP: A value of 1b indicates the Function supports the optional Function Level Reset mechanism. set by fuse.
27:0	0008020h RO	**DEVICECAP:** DEVICECAP: Bits 31:29: Reserved, 0 Bits 27:26: Power Limit Scale: Not applicable , hardwired to 00b Bits 25:18: Power Limit Value: Not applicable , hardwired to 00b Bits 17:16: Reserved, 0. Bit 15: Role-base Error Reporting (RBER): When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1 Bits 14:12: Reserved, 0. Bits 11:9: Endpoint L1 Acceptable Latency: This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from the L1 state to the L0 state. Bits 8:6: Endpoint L0s Acceptable Latency: This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from the L0s state to the L0 state. Bit 5: Extended Tag Field Supported: This bit indicates the maximum supported size of the Tag field as a Requester. Bits 4:3: Phantom Functions Supported: This field indicates the support for use of unclaimed Function Numbers to extend the number of outstanding transactions for PCIe devices. Bits 2:0: Max_Payload_Size Supported: This field indicates the maximum payload size that the Function can support for TLPs. 000b represents 128 bytes, the minimum allowed value.

6.1.12 DEVICECTL DEVICESTS (DEVICECTL_DEVICESTS) — Offset 78h

PCI Express Device Capabilities and Control Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:5, F:0] + 78h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RO/V	**DEVICESTS:** Transaction Pending bit: When Set, this bit indicates that the Function has issued Non-Posted Requests that have not been completed. A Function reports this bit is cleared only when all outstanding Non-Posted Requests have completed or have been terminated by the Completion Timeout mechanism. This bit must also be cleared upon the completion of an FLR.
20	0h RO	**RELAX_ORD_EN:** AUX Power Detected: Not used, 0
19	0h RW/1C/V	**UR_REQ_DET:** Unsupported Request Detected - set when IUNIT recieve P/NP transaction which is UR
18:16	0h RO	**DEVICECTL_MISC_STS:** DEVICESTS Bits 2:0: Various error detected bits: The Root Complex Integrated Endpoint does not use the PCI Express error reporting mechanism. Always return 0.
15	0h RW	**INIT_FLR:** Initiate Function Level Reset: A write of 1b initiates Function Level Reset to the Function. The value read by software from this bit is always 0b.
14:0	0000h RO	**DEVICECTL_MISC_CTRL:** DEVICECTL - Misc RO ctrl bits. the only bit set reflect Unsupported-Request-Reporting Enable

6.1.13 MSI CAPID (MSI_CAPID) — Offset ACh

MSI_CAPID - MSI Capabilities and MSI Control Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:5, F:0] + ACh	0080D005h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	1h RO	**AC64:** 64-bit Address Capable (C64): PCIe devices must support 64b MSI addressing.
22:20	0h RW	**MME:** Multiple Message Enable (MME): This field is RW for software compatibility, but only a single message is ever generated.
19:17	0h RO	**MMC:** Multiple Message Capable (MMC)- 3'h0 indicates one outstanding message is supported
16	0h RW	**MSIEN:** MSI Enable (MSIE): If set, MSI is enabled. PCICMDSTS.BME must be set for an MSI to be generated. When 0, blocks the sending of a MSI interrupt. The interrupt status is not blocked from being reflected in the PCICMDSTS.IS bit. When 1, permits sending of a MSI interrupt.
15:8	D0h RO	**NEXT_PTR:** Next Capability Pointer (MSI_NEXT_CAP): This contains a pointer to the next item in the capabilities list which is the Power Management capability
7:0	05h RO	**CAPABILITY_ID:** MSI Capability (MSI_CAPID): Indicates an MSI capability.

6.1.14 MSI Address low (MSI_ADDRESS_LO) — Offset B0h

MSI Address Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:5, F:0] + B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**MSI_ADDR:** MSI Address: System specified message address, always DW aligned.
1:0	0h RO	**Reserved**

6.1.15 MSI Address high (MSI_ADDRESS_HI) — Offset B4h

MSI Address Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:5, F:0] + B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**MSI_ADDR:** MSI Address: Upper 32 bits of the system specified message address.

6.1.16 MSI Data (MSI_DATA) — Offset B8h

MSI Data Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:5, F:0] + B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**MSI_DATA:** MSI Data (MD): This 16-bit field is programmed by system software and is driven onto the lower word of data during the data phase of the MSI write transaction. When the ISP issues an MSI interrupt as a MEMWR on the IOSF, the write data corresponds to the value of this field.

6.1.17 PMCAP reg (PMCAP) — Offset D0h

Power Management Capabilities

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:5, F:0] + D0h	00030001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0003h RO	**PMCAP:** PM Capability: Bits 31:27: PME Support (PMES): The camera controller does not generate PME#. Bit 26: D2_SUPPORT (D2S): The D2 power management state is not supported. Bit 25: D1_SUPPORT (D1S): The D1 power management state is not supported. Bits 24:22: Reserved Bit 21: Device Specific Initialization (DSI): Hardwired to 0 to indicate that no special initialization of the camera controller is required before generic class device driver is to use it. Bits 20:19: Reserved Bits 18:16: Version (VS): Indicates compliance with revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**NEXT_PTR:** Next Capability Pointer (PM_NEXT_CAP): End of List
7:0	01h RO	**CAPABILITY_ID:** PM Capability ID (PM_CAPID): SIG defines this ID is 01h for power management

6.1.18 PMCS reg (PMCS) — Offset D4h

Power Management Control/Status

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:5, F:0] + D4h	00000008h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/V	**PMES:** Power Management Event Status: Not used; No PME from D3cold. we put it as RW1C just to be complient w/ PCI spec
14:13	0h RO	**DS:** Data Scale: Not used
12:9	0h RO	**DSEL:** Data Select: Not used

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**PMEEN:** Power Management Event Enable
7:4	0h RO	**Reserved**
3	1h RO	**NSR:** No Soft Reset (NSR): This read-only bit indicates that the device does not lose internal state on a D3hot to D0 transition. This means: The internal state is not reset on a D3 (D3hot actually) to D0 transition and no additional operating system intervention is required to preserve the state A transition from D3 to D0 will NOT cause the IP to return to D0uninitialized. The Iunit+PUnit will restore the state of the IP configuration and MMIO registers.
2	0h RO	**Reserved**
1:0	0h RW/V	**PS:** Power State (PS): : Power management is implemented by writing to control registers in the PUNIT. This field may be programmed by the software driver, but no action is taken based on writing to this field

6.1.19 IPUVTDBAR LOW (IPUVTDBAR_LOW) — Offset F0h

VTDBAR

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:5, F:0] + F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**VTD_BAR_LOW:** VTD BAR bits 31:12
11:1	0h RO	**Reserved**
0	0h RW/L	**VTD_ENABLE:** BIOS can write VTD_ENABLE only if VTD_ENABLE_LOCK is set to '0 by fuse

6.1.20 IPUVTDBAR HIGH (IPUVTDBAR_HIGH) — Offset F4h

VTD_BAR

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:5, F:0] + F4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**VTD_BAR_HIGH:** VTD BAR bits 38:32

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7 Gaussian & Neural Network Accelerator (D8:F0)

Gaussian and Neural Network Accelerator. This chapter contains the registers in: Bus 0, Device 8, Function 0.

7.1 Summary of Registers

Table 7-1. Summary of Bus: 0, Device: 8, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	GNA Identifiers (IDENTIFICATION)	00008086h
4h	2	Device Control (DCTRL)	0000h
6h	2	Device Status (DSTS)	0010h
8h	4	RID: Revision ID DLCO: Class Code (RID_DLCO)	08800000h
Ch	1	Cache Line Size (CLS)	00h
Eh	1	Header Type (HTYPE)	00h
Fh	1	Built-in Self Test (BIST)	00h
10h	4	GNA Base Address Low (GNABAL)	00000004h
14h	4	GNA Base Address High (GNABAH)	00000000h
2Ch	2	Sub System Vendor Identifiers (SSVI)	0000h
2Eh	2	Sub System Identifiers (SSI)	0000h
34h	4	Capabilities Pointers (CAPP)	00000090h
3Ch	1	Interrupt Line (INTL)	00h
3Dh	1	Interrupt Pin Register (INTP)	01h
3Eh	2	Min Grant And Min Latency Register (MINGNTLAT)	0000h
40h	4	Override Configuration Control (OVRCFGCTL)	00000000h
90h	2	Message Signaled Interrupt Capability ID (MSICAPID)	A005h
92h	2	Message Signaled Interrupt Message Control (MC)	0000h
94h	4	Message Signaled Interrupt Message Address (MA)	00000000h
98h	4	Message Signaled Interrupt Message Data (MD)	00000000h
A0h	2	D0i3 Capability ID (D0I3CAPID)	DC09h
A2h	2	D0i3 Capability (D0I3CAP)	F014h
A4h	4	D0i3 Vendor Extended Capability Register (D0I3VSEC)	01400010h
A8h	4	D0i3 SW LTR Pointer Register (D0I3SWLTRPTR)	00000000h
ACh	4	D0i3 DevIdle Pointer Register (D0I3DEVIDLEPTR)	00000A81h
B0h	2	D0i3 DevIdle Power On Latency (D0I3DEVIDLEPOL)	0800h
B2h	2	D0i3 Power Control Enables Register (PCE)	0028h
DCh	2	Power Management Capability ID (PMCAPID)	F001h
DEh	2	Power Management Capability (PMCAP)	0002h
E0h	2	Power Management Control Status (PMCS)	0000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
F0h	2	FLR Capability ID (FLRCAPID)	0013h
F2h	2	FLR Capability Length And Version (FLRMISC)	0306h
F4h	1	FLR Control Register (FLRCTL)	00h
F5h	1	FLR Status Register (FLRSTS)	00h

7.1.1 GNA Identifiers (IDENTIFICATION) — Offset 0h

Device ID assigned to GNA and Vendor ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 0h	00008086h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO/V	**Device Identification Number (DID):** Indicates the device ID assigned to the GNA [6:0] set by straps [15:7] This field is set to the module via IOSF SB message received during device reset.
15:0	8086h RO	**Vendor Identification Number (VID):** Inidicates Intels identification

7.1.2 Device Control (DCTRL) — Offset 4h

The Command register provides coarse control over GMM's abilities like Unsupported Request Error Reporting Enable, Poisoned TLP Error Reporting Enable, Interrupt Disable, Max Aligned Payload Size, Max Aligned Read Request Size, Special Cycle Enable, Bus Initiator Enable, Memory Space Enable

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + 4h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO	**Unsupported Request Error Reporting Enable (UNSPREQERREN):** Unsupported Request Error Reporting Enable
13	0h RO	**Poisoned TLP Error Reporting Enable (PTLPERREN):** Poisoned TLP Error Reporting Enable
12:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable (INTDIS):** Interrupt Disable: Controls the ability of the function to generate INTx interrupts. 0: INTx allowed 1: INTx disabled
9:6	0h RO	**Reserved**
5	0h RO	**Max Aligned Payload Size (MXAPAYLDSZ):** Max Aligned Payload Size - Reserved
4	0h RO	**Max Aligned Read Request Size (MXARDREQSZ):** Max Aligned Read Request Size - Reserved
3	0h RO	**Special Cycle Enable (SCEN):** Special Cycle Enable - Reserved
2	0h RW	**Bus Initiator Enable (BME):** Bus Initiator Enable: 0: Disable (default) 1: Enabled. Device may generate bus initiator transactions depending on its mode of operation.
1	0h RW	**Memory Space Enable (MSE):** Memory Space Enable Controls the GMM devices response to memory space accesses 0: Disabled (default) 1: Enabled. Device will respond to memory space accesses.
0	0h RO	**IO Space Enable (IOSE):** IO Space Enable. Not implemented.

7.1.3 Device Status (DSTS) — Offset 6h

The Status register to record status information for PCI/IOSF related events

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + 6h	0010h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Detected Parity Error (DPE):** This bit is Set by a Function whenever it receives a Poisoned TLP, regardless of the state the Parity Error Response bit in the Command register. On a Function with a Type 1 Configuration header, the bit is Set when the Poisoned TLP is received by its Primary Side. Note : some implementations use this error type as non-fatal error indication This bit is typically RWC. Change to RO as this bit is not in use
14	0h RO	**Signaled System Error (SSE):** This bit is Set when a Function sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR# Enable bit in the Command register is 1. Note: some implementations use this error for fatal. When received all operations are aborted. This bit is typically RWC. Change to RO as this bit is not in use
13	0h RW/1C/V	**Received Initiator Abort (RMA):** This bit is Set when a Requester receives a Completion with Unsupported Request Completion Status. On a Function with a Type 1 Configuration header, the bit is Set when the Unsupported Request is received by its Primary Side.
12	0h RW/1C/V	**Received Target Abort (RTA):** This bit is set when a transaction abort is received to a GMM initiated transaction
11	0h RW/1C/V	**Signaled Target Abort (STA):** This bit is Set when a Function completes a Posted or Non-Posted Request as a Completer Abort error. This applies to a Function with a Type 1 Configuration header when the Completer Abort was generated by its Primary Side.
10:8	0h RO	**Reserved**
7	0h RO	**Fast Back-to-Back (FB2B):** Fast Back-to_Back (ignored by SW)
6:5	0h RO	**Reserved**
4	1h RO	**Capability List (CLIST):** Capability List 0 : no capability list 1 : the GMM contains a linked list of capabilities which is accessed via the CAPPTR register at offset 34h
3	0h RO/V	**Interrupt Status (INTSTS):** Interrupt Status Reflects the state of the interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will this device send a virtual INTA. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit is controlled by HW. 0 : No interrupt pending 1 : Interrupt pending

Bit Range	Default & Access	Field Name (ID): Description
2:0	0h RO	**Reserved**

7.1.4 RID: Revision ID DLCO: Class Code (RID_DLCO) — Offset 8h

RID:

DLCO: This register identify the type of device. The values are as defined in PCI 3.0 bus specification in Appendix D. The GMM is identified as an Other system Peripheral

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 8h	08800000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	08h RO	**Base Class Code (BCC):** Base Class (Generic system Peripherals)
23:16	80h RO	**Sub Class Code (SCC):** Code for Sub Class
15:8	00h RO	**Peripheral Interface (PROGINTERFACE):** Interface (other system peripheral)
7:0	8'hxx RO	**Revision ID (RID):** Indicates stepping of this device. This register is set by side-band. All RID registers are sourced from a fuse/settings incremented for each stepping.

7.1.5 Cache Line Size (CLS) — Offset Ch

The system cacheline size in units of DWORDS

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:8, F:0] + Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Cache Line Size (CLS):** Implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no impact on any PCI Express device functionality

7.1.6 Header Type (HTYPE) — Offset Eh

This byte identifies the layout of the second part of the predefined header and whether or not the device contains multiple functions (GMM is a single-function device of basic configuration space format, so this register is Read-Only and hardwired to 0)

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:8, F:0] + Eh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Multi Function Device (MFD):** Hardwired to 0 indicating this device is not a multi-function device.
6:0	00h RO	**Header Type (HT):** The value 00h, indicates a basic (i.e., single function) configuration space format.

7.1.7 Built-in Self Test (BIST) — Offset Fh

This register describes the BIST capability of GMM and since GMM doesnt support BIST, the register is configured as Read Only

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:8, F:0] + Fh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**BIST Capable (BISTCAP):** BIST Capable. Hardwired to 0 since this device does not implement BIST.
6	0h RO	**Start BIST (BISTST):** Start BIST. Hardwired to 0 since this device does not implement BIST
5:4	0h RO	**Reserved**
3:0	0h RO	**BIST Completion Code (BISTCC):** Hardwired to 0 since this device does not implement BIST.

7.1.8 GNA Base Address Low (GNABAL) — Offset 10h

GNA Base Address Low:

Lower 32-bits of the GNA Base Address register.

The GMM Base Address register may be accessed with Double Word (32bit) read/write operations.

In 32-bit OS, the address specified may be limited by 32-bit of space, and the renaming bits must stay with their default values

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 10h	00000004h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Memory Base Address Low (BAL):** Memory Base Address Low Base address of this device's memory mapped IO space. A page of 4KB of address is used
11:4	00h RO	**Address Mask (ADDRMSK):** Address Mask Hardwired to 0s to indicate at least 4KB address range

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**Prefetchable Memory (PREF):** Hardwired to 0 indicating that this range is not prefetchable
2:1	2h RO	**Memory Type (MEMTY):** Memory Type: 00: 32 bit base address 01: reserved 10: 64-bit base address 11: reserved
0	0h RO	**Space Type (SPTY):** Space Type: Memory/IO Space Hardwired to 0 indicating that this is a Memory BAR

7.1.9 GNA Base Address High (GNABAH) — Offset 14h

GNA Base Address High:

Upper 32-bits of the GNA Base Address register.

The GNA Base Address register may be accessed with Double Word (32bit) read/write operations.

In 32-bit OS, the address specified may be limited by 32-bit of space, and the renaming bits must stay with their default values

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 14h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RO	**Memory Base Address High (Reserved) (BAR):** These bits must be loaded with zeros
6:0	00h RW	**Memory Base Address High (BAH):** Memory Base Address High - bits Includes the high bits of the base address used by 64-bit OS. Must hold zero for 32-bit OS

7.1.10 Sub System Vendor Identifiers (SSVI) — Offset 2Ch

This register is initialized to logic 0 by the assertion of reset. This register can be written only once after reset de-assertion it is locked for writes after that.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + 2Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/O	**Subsystem Vendor ID (SSVID):** Subsystem Vendor ID (SSVID): This is written by BIOS. No hardware action taken on this value.

7.1.11 Sub System Identifiers (SSI) — Offset 2Eh

This register is initialized to logic 0 by the assertion of reset. This register can be written only once after reset de-assertion it is locked for writes after that.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + 2Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/O	**Subsystem ID (SSID):** Subsystem ID (SSID): This is written by BIOS. No hardware action taken on this value.

7.1.12 Capabilities Pointers (CAPP) — Offset 34h

This register gives MSI capability pointer offset

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 34h	00000090h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	90h RO	**Capability Pointer (CAPP):** Indicates that the MSI capability pointer offset is offset 90h

7.1.13 Interrupt Line (INTL) — Offset 3Ch

This register contains interrupt line routing information. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:8, F:0] + 3Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Interrupt Connection (INTCON):** Interrupt Connection Communicate interrupt line routing information. BIOS Requirement: POST software writes the routing information into this register as it initializes and configures the system. The value indicates to which input of the system interrupt controller this device's interrupt pin is connected

7.1.14 Interrupt Pin Register (INTP) — Offset 3Dh

tells which PCI legacy interrupt pin a device will use (GMM uses only IntA).

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:8, F:0] + 3Dh	01h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved**
2:0	1h RO	**Legacy Interrupt (LEGINT):** When Legacy interrupts are used, function use legacy interrupt INTA.

7.1.15 Min Grant And Min Latency Register (MINGNTLAT) — Offset 3Eh

specifies a device's desired settings for Latency Timer values

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + 3Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RO	**Min Latency (MINLAT):** Reserved
7:0	00h RO	**Min Grant (MINGNT):** Reserved

7.1.16 Override Configuration Control (OVRCFGCTL) — Offset 40h

This register holds bits that may be used internal mechanisms in the GMM during debug operations. Special notes will be made to BIOS writers, if any 5 of these bits will need to be set to value other than default.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 40h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	15'h0 RO	**Reserved**
17	1'b0 RW	**Narrow-Mem Residue Fix Dis (NMEMRFXDIS):** This bit influences the Narrow-Mem control logic. In conditions where I/F bandwidth is high and the Narrow-Mem holds some residue data which is not used for computation (such as incomplete convolution stride), the Narrow-Mem control logic can hang. By setting this bit to 1'b1, the HW fix is disabled. Refer to Narrow-Mem Residue Hang (2D-CNN). Note: Value of this bit is not impact by OVR_FORCE_PWR_ON
16	1'b0 RW	**Scoring Underrun/Overrun Error Check Disable (SUOECD):** Disables consistency checks in GNA setup (SW calculated values GNASCRLEN & GNATELST) that are based on too-few or toomany elements in the DMA setup. Scoring Under-run is a scenario where DMA is out of data for scoring to proceed. Note: [Value of this bit is not impact by OVR_FORCE_PWR_ON] 1'b0 : Error Check is enabled 1'b1 : Error Check is disabled
15	1'b1 RW	**PM_REQ NACK before Drain Enable (CXNBDEN):** PM_REQ IOSF-SB massage is used in 'Package C state transition' flow. 1'b0: NACK PM_REQ is sent only after all outstanding completion have returned, and after Initiator cycles are blocked. 1'b1: NACK PM_REQ is sent before waiting for return of any outstanding completion. This is critical to mitigate GNA In/out dependencies, and prevent platform hang, refer to GNA In/Out Dependencies in Pkg-Cx Flows
14	1'b0 RW	**FLR_NP_Disable (FLRNPDIS):** Function Level Reset Non-Posted Disable. 1'b0 : FLR operates normally. 1'b1 : FLR This also disable new path.
13	1'b0 RW	**FLR_Disable (FLRDIS):** Function Level Reset Disable. 1'b0 : FLR operates normally. 1'b1 : FLR is disabled. Writes to start FLR will be ignored. FLR data structure is reported as usual.
12:11	1'b0 RO	**Reserved**
10	1'b0 RO/V	**Clock Wake Glitch Patch Disable (CWGPD):** 1'b0 : Patch fix Enabled 1'b1 : Patch fix Disables
9	1'b0 RW	**PGCB Clock Trunk Clock Gating Enable (PGCBCGEN):** This bit, when set, allows the PGCB interface clock for GNA from SoC (pgcb_clk) to be gated when conditions are met by de-asserting GNA's clock request (pgcb_clkreq). When clear, GNA will always assert its clock request.
8	0h RW	**Sideband Clock Gating Enable (SBDCGEN):** This bit, when set, enables the sideband interface clock used for GMM bus interface operations (gated_side_clk) to be gated when conditions are met. When clear, clock gating is disabled.

Bit Range	Default & Access	Field Name (ID): Description
7	1'b0 RW	**Side-Band Clock Trunk Clock Gating Enable (SBTCGEN):** This bit, when set, allows the sideband interface clock for GNA from SoC (iosfsf_clk) to be gated when conditions are met by de-asserting GNA's clock request (iosfst_side_clkreq). When clear, GNA will always assert its clock request.
6	1'b0 RW	**Sideband Clock Partition Clock Gating Enable (SBPCGEN):** This bit, when set, enables the IOSF-SB interface clock for GNA (side_clk) to be gated when conditions are met. When clear, clock gating is disabled.
5	1'b0 RW	**GNA Core Clock Gating Enable (GM_BB_GNAC_DCGEN):**This bit, when set, enables the primary interface clock used for GNA core operations (gmm_core_clk) to be gated when conditions are met. When clear, dynamic clock gating is disabled.
4	1'b0 RW	**DMA engine Clock Gating Enable (GM_BB_DMA_DCGEN):**This bit, when set, enables the primary interface clock used for DMA and MMU operations (gmm_bb_clk_dma) to be gated when conditions are met. When clear, clock gating is disabled.
3	1'b0 RW	**Register Access Clock Gating Enable (GM_BB_RA_DCGEN):**This bit, when set, enables the primary interface clock used for GNA register access operations (gmm_bb_clk_ra) to be gated when conditions are met. When clear, clock gating is disabled.
2	1'b0 RW	**Host interface Clock Gating Enable (GM_BB_HOST_DCGEN):** This bit, when set, enables the primary interface clock used for GNA bus interface operations (gmm_bb_clk_host) to be gated when conditions are met. When clear, clock gating is disabled
1	1'b0 RW	**Partition Clock Gating Enable (PCGEN):** This bit, when set, enables the primary interface clock for GNA (gmm_bb_clk) to be gated when conditions are met. When clear, clock gating is disabled
0	1'b0 RW	**Trunk Clock Gating Enable (TCGEN):** This bit, when set, allows the primary interface clock for GNA from SoC (iosfpf_clk) to be gated when conditions are met by de-asserting GNA's clock request (iosfpt_prim_clkreq). When clear, GNA will always assert its clock request.

7.1.17 Message Signaled Interrupt Capability ID (MSICAPID) — Offset 90h

This register contains a pointer to the next item in the capabilities list which is the Power Management Capability and also helps to identify linked list item (capability structure) as being for MSI registers.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + 90h	A005h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	A0h RO	**Pointer to Next Capability (NXTPTR):** Pointer to Next Capability This contains a pointer to the next item in the capabilities list which is the Power Management Capability

Bit Range	Default & Access	Field Name (ID): Description
7:0	05h RO	**Capability ID (CAPID):** Capability ID Value of 05h identifies this linked list item (capability structure) as being for MSI registers.

7.1.18 Message Signaled Interrupt Message Control (MC) — Offset 92h

This register is defined to meet PCI Local Bus Specification 3.0 Section 6.8 definition of MSI messages.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + 92h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	**Reserved**
8	0h RO	**Per-Vector Masking Capable (PVMCAP):** Per-Vector Masking Capable. 0- not supported by GMM
7	0h RO	**64-bit Address Capable (ADDR64CAP):** 64-bit Address Capable Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message Address register and is incapable of generating a 64-bit memory address. This may need to change in future implementations when addressable system memory exceeds the 32bit/4GB limit.
6:4	0h RW	**Multiple Message Enable (MMEN):** Multiple Message Enable System software program this field to indicate the number of vectors allocated to the GMM. At least one vector must be allocated when the MSI interrupts are enabled. This value is ignored by HW as only a single vector is in use by GMM.
3:1	0h RO	**Multiple Message Capable (MMCAP):** Indicates to SW the number of vectors that the GMM module is requesting for use Value Number of Messages requested 000 1 001 2 (reserved) 010 4 (reserved) 011 8 (reserved) 100 16(reserved) 101 32(reserved) Other reserved
0	0h RW	**MSI Enable (MSIEN):** MSI Enable Controls the ability of GMM to generate MSI Messages. A device driver is prohibited from writing this bit to mask a functions service request. 0: MSI will not be generated 1: MSI will be generated. INTA will not be generated and INTA status is not set.

7.1.19 Message Signaled Interrupt Message Address (MA) — Offset 94h

This register is defined to meet PCI Local Bus Specification 3.0 Section 6.8 definition of MSI messages

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 94h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**Message Address (MADDR):** Message Address Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address
1:0	0h RO	**Reserved**

7.1.20 Message Signaled Interrupt Message Data (MD) — Offset 98h

This register is defined to meet PCI Local Bus Specification 3.0 Section 6.8 definition of MSI messages

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 98h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Message Data (MDAT):** Message Data Base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.

7.1.21 D0i3 Capability ID (D0I3CAPID) — Offset A0h

Pointer to next capability and capability ID

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + A0h	DC09h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	DCh RO	**Pointer to Next Capability (NXTPTR):** This contains a pointer to the next item in the capabilities list which is the Power Management Capability
7:0	09h RO	**Capability ID (CAPID):** Value of 09h identifies this linked list item (capability structure) is a vendor specific capability.

7.1.22 D0i3 Capability (D0I3CAP) — Offset A2h

Vendor-Specific Capability ID

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + A2h	F014h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:12	8'hF RO	**Vendor-Specific Capability ID (VSID):** Indicates that this Vendor Specific Capability is an Extended Capability, which use a VSEC 16-bit Externded VCapaiblity in the subsequent 4B., differentiating this from other vendor specific capabilities.
11:8	0h RO	**Vendor Specific Capability Revision (VSREV):** Reserved
7:0	4'h0 RO	**Vendor Specific Capability Length (VSLEN):** This field indicates the number of bytes in this capability including the CapID and Cap registers.

7.1.23 D0i3 Vendor Extended Capability Register (D0I3VSEC) — Offset A4h

Vendor Specific Extended Capability Length

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + A4h	01400010h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	12'h14 RO	**Vendor Specific Extended Capability Length (VSECLEN):** Indicates that this Vendor Specific Capability is an Extended Capability, which use a VSEC 16-bit Externded VCapaiblity in the subsequent 4B., differentiating this from other vendor specific capabilities.
19:16	0h RO	**Vendor Specific Extended Capability Revision (VSREV):** For this revision of DevIdle, this field is 0h
15:0	0010h RO	**Vendor Specific Extended Capability ID (VSECID):** DevIdle has been assigned the Intel VSEC ID of 10h

7.1.24 D0i3 SW LTR Pointer Register (D0I3SWLTRPTR) — Offset A8h

SW LTR Update MMIO Offset Location

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**SW LTR Update MMIO Offset Location (SWLTRLOC):** The value in this field is ignored as GMM does not support SW LTR
3:1	0h RO	**Base Address Register Number (BARNUM):** The value in this field is ignored as GMM does not support SW LTR
0	0h RO	**Valid Indicator (VALID):** Indicates the use of SW LTR by the function.GMM does not use SW LTR

7.1.25 D0i3 DevIdle Pointer Register (D0I3DEVIDLEPTR) — Offset ACh

DevIdle MMIO Offset Location

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + ACh	00000A81h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:4	28'hA8 RO	**DevIdle MMIO Offset Location (DEVIDLELOC):** This location pointer to the DevIdle register in MMIO space, as an offset from the BAR base.
3:1	0h RO	**Base Address Register Number (BARNUM):** The DevIdle is located in BAR0
0	1h RO	**Valid Indicator (VALID):** GMM has a DevIdle register

7.1.26 D0i3 DevIdle Power On Latency (D0I3DEVIDLEPOL) — Offset B0h

D0idle_5 Max_Power_On_Latency is set by BIOS at boot and read by device driver SW to calculate approximate cost of a D0idle entry + exit cycle. This allows driver to avoid idle entry in cases where device duty cycle is larger than D0idle entry + exit cycle.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + B0h	0800h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	**Reserved**
12:10	2h RO	**Power On Latency Scale (POLS):** Latency Scale multiplier: 010: 1us 011: 32us All other settings are reserved. This field is a RO as there is no need for BIOS programing of it.
9:0	000h RO	**Power On Latency Value (POLV):** A value of 0 indicates a power on latency of less than 1us. This field is a RO as there is no need for BIOS programing of it.

7.1.27 D0i3 Power Control Enables Register (PCE) — Offset B2h

This register controls the D0i3 features like Hardware Autonomous Enable,sleep enable, D3-Hot Enable, I3 Enable and PMC Request Enable

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + B2h	0028h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	1h RW	**Hardware Autonomous Enable (HAE):** If set, then the IP may request a PG whenever it is idle. NOTE: If this bit is set, then bits[2:0] must be 000.
4	0h RO	**Reserved**
3	1h RW	**Sleep Enable (SE):** if clear, then IP will never asset Sleep to the retention flops. If set, then IP may assert Sleep during PGing. Note that some platforms may default this bit to 0, others to 1.
2	0h RW	**D3-Hot Enable (D3HE):** If set, then IP will PG when idle and the PMCSR[1:0] register in the IP =11.
1	0h RW	**I3 Enable (I3E):** If set, then IP will PG when idle and the D0i3 register (D0i3C[2] = 1) is set. NOTE: If bits [2:1] = 11, then the IP would PG whenever either PMCSR = 11 or the D0i3C.i3 bit is set.
0	0h RW	**PMC Request Enable (PMCRE):** If set, then IP will PG when idle and the PMC requests power gating by asserting the pmc_*_sw_pg_req_b signal.

7.1.28 Power Management Capability ID (PMCAPID) — Offset DCh

This register contains a pointer to next item in capabilities list and also helps to identify linked list item as being for

PCI Power Management registers

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + DCh	F001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	F0h RO	**Next Pointer (NXTPTR):** Next Pointer This contains a pointer to next item in capabilities list. This is the final capability in the list and must be set to 00h.
7:0	8'h05 RO	**Capability Identifier (CAPID):** Capability Identifier Identifies this linked list item as being for PCI Power Management registers. This is compliant with the PCI Power Management Interface Specification (section 3.2).

7.1.29 Power Management Capability (PMCAP) — Offset DEh

This register describes the Power Management Capability of GMM

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + DEh	0002h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:11	00h RO	**PME Support (PMES):** PME Support This device does not support PMEB signal
10	0h RO	**D2 Support (D2S):** D2 This device does not support D2
9	0h RO	**D1 Support (D1S):** D1 This device does not support D1
8:6	0h RO	**Auxiliary Current (AUXC):** Auxiliary Current Reserved. Not applicable for GMM
5	0h RO	**Device Specific Initialization (DSI):** Device specific Initialization Indicates that this device requires device specific initialization before generic class device driver is to use it

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**Auxiliary Power (AUXP):** Aux Power This device does not use Aux power
3	0h RO	**PME Clock (PMEC):** PME Clock indicate this device does NOT support PMEB generation
2:0	2h RO	**Version for PM (VER):** Version Hardwired to 010b to indicate there are 4 bytes of power management registers implemented and that this device complies with revision 1.1 of the PCI Power Management Interface Specification.

7.1.30 Power Management Control Status (PMCS) — Offset E0h

This register has the status of PME Generation from D3(cold), Data Scale, Data Select, PME Enable and Power State

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + E0h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**PME Generation from D3 (cold) (PMEGD3):** PME Generation from D3 (cold) Not supported
14:13	0h RO	**Data Scale (DATSC):** Data Scale No support for Power Management Data register
12:9	0h RO	**Data Select (DATSEL):** Data Select No support for Power Management Data register
8	0h RO	**PME Enable (PMEE):** PME Enable PMEB is not supported
7:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Power State (PS):** Indicates the current power state of this device and can be used to set the device into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. 00: D0 01: D1 (Not supported in this device.) 10: D2 (Not supported in this device.) 11: D3 Write of reserved values is ignored and state will not change. Support of D3cold does not require any special action. While in the D3hot state, this device can only act as the target of PCI configuration transactions (for power management control). This device also cannot generate interrupts or respond to MMR cycles in the D3 state. The device must return to the D0 state in order to be fully-functional.

7.1.31 FLR Capability ID (FLRCAPID) — Offset F0h

This register contains a pointer to next item in capabilities list and capablity of Advanced Features

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + F0h	0013h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RO	**Next Pointer (NXTPTR):** Next Pointer This contains a pointer to next item in capabilities list. This is the final capability in the list and must be set to 00h.
7:0	13h RO	**Capability Identifier (CAPID):** Capability Identifier A value that indicates FLR (Vendor specific value) 0 : 09h (FLR in use) A value of 09h in this register indicates that this is a FLR capabilities field.

7.1.32 FLR Capability Length And Version (FLRMISC) — Offset F2h

This register descibest the FLR Capability, TXP Capability and Capability Length

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + F2h	0306h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RO	**Reserved**
9	1h RO	**FLR Capability (FLRCAP):** Indicates support for Function Level Reset (FLR).
8	1h RO	**TXP Capability (TXPCAP):** Indicates that TP bit is supported
7:0	06h RO	**Capability Length (CAPLEN):** Capability Length This bit indicates the number of bytes this vendor specified capability requires. it has a value of 06h for the FLR capability

7.1.33 FLR Control Register (FLRCTL) — Offset F4h

This register controls the Functional Level reset operation of gmm

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:8, F:0] + F4h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RO	**Reserved**
0	0h WO/V	**Initiate FLR (INITFLR):** Writing 1 to this field starts the Functional Level Reset.This will act similar to the Abort + will bring all non-CFG registers to their reset value. The FLR is completed when the FLR status bit is cleared

7.1.34 FLR Status Register (FLRSTS) — Offset F5h

This register helps to identify whether FLR is in progress

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:8, F:0] + F5h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RO	**Reserved**
0	0h RO/V	**Transaction Pending (XPEND):** Transaction Pending 0 : FLR not in progress 1 : FLR is in progress (due to internal operation or waiting for the completion of a non-posted transaction)

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8 CrashLog Registers (D10:F0)

CrashLog device registers. The CrashLog is an SRAM within the processor that records the system information during a crash/hang. This chapter documents the registers in Bus: 0, Device: 10, Function: 0.

8.1 Summary of Registers

Table 8-1. Summary of Bus: 0, Device: 10, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	VENDOR_ID_DEVICE_ID	9A0D8086h
4h	4	COMMAND_STATUS	00100000h
8h	4	REVISION_ID	11800001h
Ch	4	CACHE_LINE_SIZE	00000000h
10h	8	PM_BAR	0000000000000004h
2Ch	4	SUBSYSTEM_VENDOR_ID	00000000h
34h	4	CAPABILITIES_POINTER	00000070h
3Ch	4	INTERRUPT_LINE	00000000h
70h	4	PCIE_CAPID	0092D010h
74h	4	DEV_CAP	00000FE0h
78h	4	DEV_CTL_STS	00000000h
D0h	4	PM_CAPID	00030001h
D4h	4	PM_CONTROL_STATUS	00000008h
100h	4	TELEM_CAPABILITY_HEADER	11010023h
104h	4	TELEM_VSEC_0	01018086h
108h	4	TELEM_VSEC_1	04040002h
10Ch	4	TELEM_VSEC_2	000326C0h
110h	4	WATCHER_CAPABILITY_HEADER	12010023h
114h	4	WATCHER_VSEC_0	01018086h
118h	4	WATCHER_VSEC_1	04020003h
11Ch	4	WATCHER_VSEC_2	00030080h
120h	4	CRASHLOG_CAPABILITY_HEADER	00010023h
124h	4	CRASHLOG_VSEC_0	01018086h
128h	4	CRASHLOG_VSEC_1	0A010004h
12Ch	4	CRASHLOG_VSEC_2	00030180h

8.1.1 VENDOR_ID_DEVICE_ID — Offset 0h

Vendor and Device ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 0h	9A0D8086h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	9A0Dh RO	**DEVICE_ID:** Device ID: The value that uniquely identifies the the power management device from all other PCI devices.
15:0	8086h RO	**VENDOR_ID:** Vendor ID: 8086 is Intel Vendor Identification code

8.1.2 COMMAND_STATUS — Offset 4h

Command and Status

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 4h	00100000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**DETECTED_PARITY_ERROR:** The Camarillo device does not implement this bit and it is hardwired to a 0.
30	0h RO	**SIGNALED_SYSTEM_ERROR:** This bit is set when the device has detected an un-correctable error and reported it via SERR message over sideband. This requires SERR Enable bit to be set in Command register. The Camarillo device does not implement this bit and it is hardwired to a 0.
29	0h RO	**RECEIVED_INITIATOR_ABORT_STATUS:** This bit is set when device receives a Completion transaction with Unsupported Request completion status. No error will be reported.
28	0h RO	**RECEIVED_TARGET_ABORT_STATUS:** This bit is set when device receives a Completion transaction with Completer Abort completion status. No error will be reported

Bit Range	Default & Access	Field Name (ID): Description
27	0h RO	**SIGNALED_TARGET_ABORT_STATUS:** Set by the device when aborting a request that violates the device programming model. When SERR Enable is set SERR message will be send over sideband. Device will not generate a Target Abort DMI completion packet or Special Cycle, and therefore it has no need to implement this bit.
26:25	0h RO	**Reserved**
24	0h RO	**INITIATOR_DATA_PARITY_ERROR:** This bit is Set by a Requester if the Parity Error Response bit in the Command register is 1b and either of the following two conditions occurs: * Requester receives a Completion marked poisoned * Requester poisons a write Request If the Parity Error Response bit is 0b, this bit is never Set.
23:21	0h RO	**Reserved**
20	1h RO	**CAPABILITIES_LIST:** This optional read-only bit indicates whether or not this device implements the pointer for a New Capabilities linked list at offset 34h. A value of zero indicates that no New Capabilities linked list is available. A value of one indicates that the value read at offset 34h is a pointer in Configuration Space to a linked list of new capabilities. This device does support capabilities.
19	0h RO	**INTERRUPT_STATUS:** Reflects the state of the interrupt pin at the input of the enable/disable circuit. When the interrupt is asserted, and cleared when the interrupt is cleared (independent of the state of Interrupt Disable bit in command register. This bit is only associated with the INTx messages and has no meaning if the device is using MSI.
18:11	0h RO	**Reserved**
10	0h RO	**INTERRUPT_DISABLE:** Disables the function to generate INTx interrupt. A value of 0 enables the function to generate INTA messages on IOSF sideband. Note: this bit has no effect on MSI generation. Since this device does not generate interrupts, this bit is set to 0x0.
9	0h RO	**Reserved**
8	0h RO	**SERR_ENABLE:** Setting this bit enables the generation of System Error message, when required through sideband interface. Not implemented by this device.
7	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**PARITY_ERROR_RESPONSE:** This bit controls the logging of poisoned TLPs in the Initiator Data Parity Error bit in the Status register. A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.
5:3	0h RO	**Reserved**
2	0h RO	**BUS_INITIATOR_ENABLE:** Controls the ability of a PCI Express Endpoint to issue Memory and I/O Read/Write Requests, and the ability of a Root or Switch Port to forward Memory and I/O Read/Write Requests in the Upstream direction. *Endpoints:* * When this bit is Set, the PCI Express Function is allowed to issue Memory or I/O Requests. * When this bit is Clear, the PCI Express Function is not allowed to issue any Memory or I/O Requests. * Note that as MSI/MSI-X interrupt Messages are in-band memory writes, setting the Bus Initiator Enable bit to 0b disables MSI/MSI-X interrupt Messages as well. Requests other than Memory or I/O Requests are not controlled by this bit. Default value of this bit is 0b. This bit is hardwired to 0b if a Function does not generate Memory or I/O Requests.
1	0h RW	**MEMORY_SPACE_ENABLE:** When set, Memory Space Decoding is enabled and memory transactions targeting the device are accepted Note: The MSE has to be set to accept any memory transaction on the primary interface targeting any of this device.
0	0h RO	**Reserved**

8.1.3 REVISION_ID — Offset 8h

Revision ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 8h	11800001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	11h RO	**CLASS_CODE:** This is an 8-bit value that indicates the base class code for the Power Management Controller. This code has the value 11h, indicating a device that is used for data acquisition and signal processing.
23:16	80h RO	**SUB_CLASS_CODE:** The code is 80h which indicates Other Data Acquisition and Signal Processing Controllers.
15:8	00h RO	**PROGRAMMING_INTERFACE:** Indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.
7:0	01h RO	**REVISION_ID:** Indicates the device specific revision identifier derived from and input strap

8.1.4 CACHE_LINE_SIZE — Offset Ch

Cache Line Size

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**BIST:** Hardwired to 0x0. This device does not support BIST
30:24	0h RO	**Reserved**
23:16	00h RO	**HEADER_TYPE:** This device implements a Type 0 configuration header
15:8	00h RO	**INITIATOR_LATENCY_TIMER:** This register is also referred to as Primary Latency Timer for Type 1 Configuration Space header Functions. The Latency Timer does not apply to PCI Express. This register must be hardwired to 00h.

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**CACHE_LINE_SIZE:** The Cache Line Size register is set by the system firmware or the operating system to system cache line size. However, note that legacy PCI 3.0 software may not always be able to program this field correctly especially in the case of Hot-Plug devices. This field is implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no effect on any PCI Express device behavior.

8.1.5 PM_BAR — Offset 10h

Base address register.

Type	Size	Offset	Default
PCI	64 bit	[B:0, D:8, F:0] + 10h	0000000000000004h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:15	000000h RW	**PMBAR:** This field corresponds to bits 38 to 15 of the base address PMBAR address space. BIOS will program this register resulting in a base address for a 32KB block of contiguous memory address space. This register ensures that a naturally aligned 32KB space is allocated within total addressable memory space.
14:4	000h RO	**ADDRESS_MASK:** Hardwired to 0s to indicate at least 32KB address range. Software typically writes all 1's to the BAR and then reads back the resulting value to assess the size of the BAR. Since bits 14:4 are read-only and zero, that indicates that the device is 32KB.
3	0h RO	**PREFETCHABLE:** Value of 0 indicates the BAR cannot be prefetched
2:1	2h RO	**ADDRESS_RANGE:** Address Range: Value of 0x2 indicates that the BAR is located anywhere system memory space (i.e. 64-bit addressing). This also indicates that the size of the BAR register is 64b.
0	0h RO	**SPACE_TYPE:** Value of 0 indicates the BAR is located in memory space

8.1.6 SUBSYSTEM_VENDOR_ID — Offset 2Ch

This value is used to identify a particular subsystem.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 2Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**SUBSYSTEM_ID:** This field should be programmed during BIOS initialization. After it has been written once, it becomes read only.
15:0	0000h RW/O	**SUBSYSTEM_VENDOR_ID:** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only.

8.1.7 CAPABILITIES_POINTER — Offset 34h

Capabilities pointer

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 34h	00000070h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	70h RO	**CAP_PTR:** Pointer to first capability structure.

8.1.8 INTERRUPT_LINE — Offset 3Ch

Interrupt line

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 3Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RO	**INTERRUPT_PIN:** A value of 00h indicates that the Function uses no legacy interrupt Message(s).
7:0	00h RO	**INTERRUPT_LINE:** Hardware does not use this field. Rather it is programmed by system software and device drivers to communicate interrupt line routing information

8.1.9 PCIE_CAPID — Offset 70h

Indicates the PCI Express Capability

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 70h	0092D010h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:25	00h RO	**INTERRUPT_MESSAGE_NUMBER:** This field indicates which MSI/MSI-X vector is used for the interrupt message generated in association with any of the status bits of this Capability structure. Telemetry Aggregator doesn't currently generate interrupts, so this value is hardwired to 0.
24	0h RO	**SLOT_IMPLEMENTED:** Hardwired to 0 for any endpoint device
23:20	9h RO	**DEV_TYPE:** Device/Port Type Indicates the specific type of this PCI Express Function. 0x9 is Root Complex Integrated Endpoint.
19:16	2h RO	**CAP_VERSION:** Indicates PCI Express Capability structure version number. Must be hardwired to 0x2.
15:8	D0h RO	**NEXT_CAPABILITY_POINTER:** Pointer to next capability in the capabilities linked list

Bit Range	Default & Access	Field Name (ID): Description
7:0	10h RO	**CAPABILITY_ID:** 0x10 indicates that this is a PCI express capability structure

8.1.10 DEV_CAP — Offset 74h

Identifies PCI Express device Function specific capabilities

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 74h	00000FE0h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RO	**FLR_CAP:** Function Level Reset Capability A value of 1b indicates the Function supports the optional Function Level Reset mechanism.
27:12	0000h RO	**MISC:** Miscellaneous fields not relevant for Telemetry Aggregator device.
11:9	7h RO	**L1_LAT:** Endpoint L1 Acceptable Latency. 0x7 == No limit.
8:6	7h RO	**L0_LAT:** Endpoint L0 Acceptable Latency. 0x7 == No limit.
5	1h RO	**EXT_TAG:** Extended Tag Field Supported This bit indicates the maximum supported size of the Tag field as a Requester. 0x1 == 8-bit Tag field supported.
4:3	0h RO	**FANTOM_FUNC:** Phantom Functions Supported. 0x0 == No Function Number bits are used for Pha Functions.
2	0h RO	**Reserved**
1:0	0h RO	**MAX_PAYLOAD_SIZE:** Max_Payload_Size Supported This field indicates the maximum payload size that the Function can support for TLPs. 0x0 == 128 bytes max payload size.

8.1.11 DEV_CTL_STS — Offset 78h

PCIE Device Control and Status register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 78h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**MISC_STATUS:** Miscellaneous reserved and status bits. Telemetry Aggregator doesn't set any of the status bits.
15	0h RO	**INIT_FLR:** Initiates FLR for FLR-supporting devices. FLR not supported for Telemetry Aggregator. Hardwire to 0.
14:0	0000h RO	**MISC_CONTROL:** Miscellaneous PCIE device control settings. Telemetry Aggregator doesn't implement any of the contolled functionality and as such will not respond to the writes.

8.1.12 PM_CAPID — Offset D0h

The Power Management Capabilities register is a read-only register which provides information on the capabilities of the function related to power management. The information in this register is generally static and known at design time.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + D0h	00030001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**PME_SUPPORT:** This field indicates the power states in which the device may assert PME#. It is hardwired to 0 to indicate that the device does not support nor assert the PME# signal.
26	0h RO	**D2:** Hardwired to 0 to indicate that the D2 power management state is not supported.
25	0h RO	**D1:** Hardwired to 0 to indicate that the D1 power management state is not supported.
24:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**DEVICE_SPECIFIC_INITIALIZATION:** Indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. This bit is not used by some operating systems. Windows and Windows NT, for instance, do not use this bit to determine whether to use D3. Instead, they use the driver's capabilities to determine this. 1b indicates that the function requires a device specific initialization sequence following transition to the D0 uninitialized state.
20	0h RO	**Reserved**
19	0h RO	**PME_CAPABILITY:** When this bit is a "1", it indicates that the function relies on the presence of the PCI clock for PME# operation. When this bit is a "0", it indicates that no PCI clock is required for the function to generate PME#. Functions that do not support PME# generation in any state must return "0" for this field. Hardwired to 0 to indicate the device does not support PME# generation.
18:16	3h RO	**VERSION:** This device complies with revision 1.2 of the PCI Power Management Interface Specification.
15:8	00h RO	**NEXT_CAPABILITY_POINTER:** This field is hardwired to 00h, indicating the end of the capabilities linked list.
7:0	01h RO	**CAPABILITY_ID:** 01h indicates that this is a power management capability

8.1.13 PM_CONTROL_STATUS — Offset D4h

The Data register is an optional, 8-bit read-only register that provides a mechanism for the function to report state dependent operating data such as power consumed or heat dissipation. Typically the data returned through the Data register is a static copy (look up table, for example) of the function's worst case 'DC characteristics' data sheet. This data, when made available to system software, could then be used to intelligently make decisions about power budgeting, cooling requirements, etc.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + D4h	00000008h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**DATA:** The data register, data scale and data select registers are not supported. Hardwired to zero.
23:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**PME_STATUS:** PME# Status. This bit is set when the function would normally assert the PME# signal independent of the state of the PME_En bit. This bit is hardwired to 0b to indicate that PME# assertion from D3 (cold) is not supported.
14:13	0h RO	**DATA_SCALE:** The data register, data scale and data select registers are not supported
12:9	0h RO	**DATA_SELECT:** The data register, data scale and data select registers are not supported
8	0h RO	**PME_ENABLE:** This bit is hardwired to 0b to indicate that PME# assertion from D3 (cold) is disabled.
7:4	0h RO	**Reserved**
3	1h RO	**NO_SOFT_RESET:** No Soft Reset. When set to 1 this bit indicates that the device is transitioning from D3hot to D0 because the power state commands do not perform a internal reset. Config context is preserved. Upon transition no additional operating system intervention is required to preserve configuration context beyond writing the power state bits. When clear the devices do not perform an internal reset upon transitioning from D3hot to D0 via software control of the power state bits. Regardless of this bit the devices that transition from a D3hot to D0 by a system or bus segment reset will return to the device state D0 uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	**Reserved**
1:0	0h RW	**POWER_STATE:** This field indicates the current power state of the device and can be used to set the device into a new power state. If software attempts to write an unsupported state to this field, the write operation must complete normally on the bus, but the data is discarded and no state change occurs.

8.1.14 TELEM_CAPABILITY_HEADER — Offset 100h

DVSEC header for telemetry capability.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 100h	11010023h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	110h RO	**NEXT_CAPABILITY_OFFSET:** Points to the location of the next capability, unless this is the last one then the value is either 000h or a value within CFG range or greater than 0xFF if in the extended config space

Bit Range	Default & Access	Field Name (ID): Description
19:16	1h RO	**CAPABILITY_VERSION:** Indicates that this is version 1 of the PCIe capability header
15:0	0023h RO	**PCIE_EXTENDED_CAPID:** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for the Designated Vendor-Specific Capability is 0023h

8.1.15 TELEM_VSEC_0 — Offset 104h

Telemetry VSEC 0

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 104h	01018086h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	010h RO	**DVSEC_LEN:** DVSEC number of bytes including this field and the PCIe Capability field
19:16	1h RO	**DVSEC_VER:** Indicates the revision of this header
15:0	8086h RO	**DVSEC_VENDOR_ID:** 0x8086 Intel

8.1.16 TELEM_VSEC_1 — Offset 108h

Telemetry VSEC 1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 108h	04040002h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	04h RO	**ENTRY_SIZE:** Entry Size in DWORDS.

Bit Range	Default & Access	Field Name (ID): Description
23:16	04h RO	**NUM_ENTRIES:** Number of entries, describes the number of telemetry aggregators that would exist in this capability lookup table.
15:0	0002h RO	**DVSEC_ID:** Indicates the type of discovery entry. This is a telemetry capability.

8.1.17 TELEM_VSEC_2 — Offset 10Ch

Telemetry VSEC 2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 10Ch	000326C0h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:3	000064D8h RO	**DISCOVERY_TABLE_OFFSET:** Base address of the discovery list for this capability space. This offset is relative to the device's MMIO address space (relative to the BAR)
2:0	0h RO	**BAR_ID:** The BAR to be used: 0 == 0x10 (BAR0)

8.1.18 WATCHER_CAPABILITY_HEADER — Offset 110h

DVSEC header for watcher capability.

Note: **NOTE:** Bit definitions are the same as TELEM_CAPABILITY_HEADER, offset 100h.

8.1.19 WATCHER_VSEC_0 — Offset 114h

Watcher VSEC 0

Note: **NOTE:** Bit definitions are the same as TELEM_VSEC_0, offset 104h.

8.1.20 WATCHER_VSEC_1 — Offset 118h

Watcher VSEC 1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 118h	04020003h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	04h RO	**ENTRY_SIZE:** Entry Size in DWORDS.
23:16	02h RO	**NUM_ENTRIES:** Number of entries, describes the number of telemetry aggregators that would exist in this capability lookup table.
15:0	0003h RO	**DVSEC_ID:** Indicates the type of discovery entry. This is a watcher capability.

8.1.21 WATCHER_VSEC_2 — Offset 11Ch

Watcher VSEC 2

Note: **NOTE:** Bit definitions are the same as TELEM_VSEC_2, offset 10Ch.

8.1.22 CRASHLOG_CAPABILITY_HEADER — Offset 120h

DVSEC header for crashlog capability.

Note: **NOTE:** Bit definitions are the same as TELEM_CAPABILITY_HEADER, offset 100h.

8.1.23 CRASHLOG_VSEC_0 — Offset 124h

Crashlog VSEC 0

Note: **NOTE:** Bit definitions are the same as TELEM_VSEC_0, offset 104h.

8.1.24 CRASHLOG_VSEC_1 — Offset 128h

Crashlog VSEC 1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 128h	0A010004h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	0Ah RO	**ENTRY_SIZE:** Entry Size in DWORDS.
23:16	01h RO	**NUM_ENTRIES:** Number of entries, describes the number of telemetry aggregators that would exist in this capability lookup table.
15:0	0004h RO	**DVSEC_ID:** Indicates the type of discovery entry. This is a crashlog capability.

8.1.25 CRASHLOG_VSEC_2 — Offset 12Ch

Crashlog VSEC 2

Note: Bit definitions are the same as TELEM_VSEC_2, offset 10Ch.

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9 Volume Management Device (D14:F0)

This chapter documents the Volume Management Device Registers.

Summary of Volume Management Device (D14:F0)

"Volume Management Device (D14:F0)"
"Volume Management Device MEMBAR2 Registers"

9.1 Volume Management Device (D14:F0)

This section contains the registers in Bus: 0, Device: 14, Function: 0.

9.1.1 Summary of Registers

Table 9-1. Summary of Bus: 0, Device: 14, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	2	Vendor ID (VID_0_14_0_PCI)	8086h
2h	2	Device ID (DID_0_14_0_PCI)	0000h
4h	2	PCI Command (PCICMD_0_14_0_PCI)	0000h
6h	2	PCI Status (PCISTS_0_14_0_PCI)	0010h
8h	1	RID PCI (RID_0_14_0_PCI)	00h
9h	1	CCRIF PCI (CCRIF_0_14_0_PCI)	00h
Ah	2	CCRC PCI (CCRC_0_14_0_PCI)	0104h
Ch	1	CLSR PCI (CLSR_0_14_0_PCI)	00h
Eh	1	HDR PCI (HDR_0_14_0_PCI)	80h
10h	8	CFGBAR PCI (CFGBAR_0_14_0_PCI)	000000000000000Ch
18h	8	MEMBAR1 PCI (MEMBAR1_0_14_0_PCI)	000000000000000Ch
20h	8	MEMBAR2 PCI (MEMBAR2_0_14_0_PCI)	000000000000000Ch
2Ch	2	SVID PCI (SVID_0_14_0_PCI)	8086h
2Eh	2	SSID PCI (SSID_0_14_0_PCI)	0000h
34h	1	CAPPTR PCI (CAPPTR_0_14_0_PCI)	80h
3Ch	1	INTL PCI (INTL_0_14_0_PCI)	00h
3Dh	1	INTPIN PCI (INTPIN_0_14_0_PCI)	00h

9.1.2 Vendor ID (VID_0_14_0_PCI) — Offset 0h

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:14, F:0] + 0h	8086h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RO	**Vendor Identification Number (VENDOR_IDENTIFICATION_NUMBER):** The value is assigned by PCI-SIG to Intel.

9.1.3 Device ID (DID_0_14_0_PCI) — Offset 2h

This register combined with the Device Identification register uniquely identifies any PCI device.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:14, F:0] + 2h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**Device Identification Number (DEVICE_IDENTIFICATION_NUMBER):** The value in this register specifies the Device ID for the Volumne Management Device. This value is the same for all instances of the VMD. The value of this register is selected by the DEVID_SELECT field in the VMCONFIG register. Volume Management Device v2.0 for Server uses Device ID values 0x28C0 to 0x28CF.

9.1.4 PCI Command (PCICMD_0_14_0_PCI) — Offset 4h

This register provides basic control over the VMD devices ability to respond to PCI cycles.

The PCICMD Register in the VMD disables the VMD PCI compliant initiator accesses to main memory.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:14, F:0] + 4h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable (INTERRUPT_DISABLE):** Interrupt_Disable INTx Interrupt Disable VMD does not support the generation of INTx, but VMD-owned devices may. This bit has no effect in hardware. 1: INTx Legacy Interrupt generation is disabled 0: INTx Legacy Interrupt generation is enabled Notes: INTx message received from VMD-owned Root Ports will be routed to the system using the same rules defined in the Root Ports as though they were not VMD-owned. If the VMD driver expects INTx, then the INTPIN registers in the VMD-owned Root Ports and Switches must be programmed by the VMD driver. A write to this register will trigger an interrupt to the VMD driver using the MSI table entry 0.
9	0h RO	**Fast B2B Enable (FAST_BACK_TO_BACK_ENABLE):** Not applicable to PCI Express and is hardwired to 0
8	0h RO	**SERRE PCICMD (SERRE):** SERR Reporting Enable Not supported for VMD. VMD-Owned Root Ports may be programmed by the VMD driver to signal a system error.
7	0h RO	**IDSEL Stepping Wait Cycle Control (IDSEL_STEPPING_WAIT_CYCLE_CONTROL):** Not applicable to internal IIO devices. Hardwired to 0.
6	0h RO	**PERRE PCICMD (PERRE):** Parity Error Reporting Enable Not supported for VMD. VMD-Owned Root Ports still report parity errors separately.
5	0h RO	**VGA Palette Snoop Enable (VGA_PALETTE_SNOOP_ENABLE):** Not applicable to internal IIO devices. Hardwired to 0.
4	0h RO	**MWIE PCICMD (MWIE):** Memory Write and Invalidate Enable Not applicable to internal IIO devices. Hardwired to 0.
3	0h RO	**SCE PCICMD (SCE):** Special Cycle Enable Not applicable to DMI/PCI Express devices. Hardwired to 0

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**BME PCICMD (BME):** Bus Initiator Enable Virtually, this bit is meant to enable the VMD to initiator requests to the system. This bit has no effect in hardware. The VMD driver reads this bit to decide how to set corresponding BME bits in the VMD-Owned Root Ports and Endpoint devices. 1: If this bit is set, the VMD driver may allow VMD-Owned Root Ports and Endpoint devices to initiator requests to the Root Complex. 0: If this bit is clear, the VMD driver must prevent VMD-Owned Root Ports and Endpoint devices from initiator requests to the Root Complex. Notes: A write to this register will trigger an interrupt to the VMD driver using the MSI table entry 0.
1	0h RW	**MSE PCICMD (MSE):** Memory Space Enable Virtually, this bit is meant to enable the VMD memory BAR's. In hardware, this bit will enable CFGBAR and the MEMBAR2 MSI-X table. It has no effect on MEMBAR1 and the rest of MEMBAR2 (which are decoded by the VMD-Owned Root Ports). The VMD driver reads this bit to decide how to set corresponding MSE bits in the VMD-Owned Root Ports and/or Endpoint devices. 1: If this bit is set, CFGBAR and MSI-X tables are enabled for access. The VMD driver may enable VMD-Owned Root Port and Endpoint device BAR regions. 0: If this bit is clear, CFGBAR and MSI-X tables are disabled and inaccessible. The VMD driver must disable VMD-Owned Root Port and Endpoint device BAR regions. Notes: A write to this register will trigger an interrupt to the VMD driver using the MSI table entry 0.
0	0h RO	**IOSE PCICMD (IOSE):** I/O Space Enable Not supported by VMD. VMD driver must not enable I/O regions in VMD-Owned Root Port or Endpoint devices.

9.1.5 PCI Status (PCISTS_0_14_0_PCI) — Offset 6h

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant Initiator Abort (MA) and PCI compliant Target Abort (TA).

PCISTS also indicates the DEVSEL# timing that has been set by the VMD.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:14, F:0] + 6h	0010h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**DPE PCISTS (DPE):** Detected Parity Error. Not used by VMD.
14	0h RO	**SSE PCISTS (SSE):** Signalled System Error. Not used by VMD.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	**RMA PCISTS (RMA):** Received Initiator Abort. Not used by VMD.
12	0h RO	**RTA PCISTS (RTA):** Received Target Abort. Not used by VMD.
11	0h RO	**STA PCISTS (STA):** Signalled Target Abort. Not used by VMD.
10:9	0h RO	**DEVSEL Timing (DEVSEL_TIMING):** Not applicable to PCI Express. Hardwired to 0.
8	0h RO	**MDPE PCISTS (MDPE):** Initiator Data Parity Error. Not used by VMD.
7	0h RO	**Fast B2B (FAST_BACK_TO_BACK):** Not applicable to VMD. Hardwired to 0.
6	0h RO	**Reserved**
5	0h RO	**pci66MHz capable (PCI66MHZ_CAPABLE):** Not applicable to VMD. Hardwired to 0.
4	1h RO	**Capabilities List (CAPABILITIES_LIST):** This bit indicates the presence of a capabilities list structure.
3	0h RO	**INTx Status (INTX_STATUS):** Indicates a pending INTx interrupt. Not used by VMD.
2:0	0h RO	**Reserved**

9.1.6 RID PCI (RID_0_14_0_PCI) — Offset 8h

This register contains the revision number of the VMD Device. This is an 8-bit value that indicates the revision identification number for the device.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:14, F:0] + 8h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO/V	**Revision ID (REVISION_ID):** Reflects the Uncore Revision ID after reset. Reflects the Compatibility Revision ID after BIOS writes 0x69 to this register.

9.1.7 CCRIF PCI (CCRIF_0_14_0_PCI) — Offset 9h

Class Code Register Interface

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:14, F:0] + 9h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW/L	**Interface CCRIF (INTERFACE_F):** VMD can be any value. **Locked by:** VMCONFIG_0_14_0_PCI.VMDLOCK

9.1.8 CCRC PCI (CCRC_0_14_0_PCI) — Offset Ah

Class Code Register Classes

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:14, F:0] + Ah	0104h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:8	01h RW/L	**Base Class (BASE_CLASS):** VMD can represent itself as any Base Class. Initial Base Class is Mass Storage Device. **Locked by:** VMCONFIG_0_14_0_PCI.VMDLOCK
7:0	04h RW/L	**Sub Class (SUB_CLASS):** VMD can be represented with any Sub Class. Initial Sub Class is RAID device. **Locked by:** VMCONFIG_0_14_0_PCI.VMDLOCK

9.1.9 CLSR PCI (CLSR_0_14_0_PCI) — Offset Ch

Cacheline Size Register

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:14, F:0] + Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Cacheline Size (CACHELINE_SIZE):** This register is set as RW for compatibility reasons only. Cacheline size is 64B.

9.1.10 HDR PCI (HDR_0_14_0_PCI) — Offset Eh

This register identifies the header layout of the configuration space.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:14, F:0] + Eh	80h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Multi function Device (MULTI_FUNCTION_DEVICE):** Set to 1b to indicate functions 1-7 may exist for the device
6:0	00h RO	**Configuration Layout (CONFIGURATION_LAYOUT):** This field identifies the format of the configuration header layout. It is Type 0 for all this device. The default is 00h, indicating a 'endpoint device'.

9.1.11 CFGBAR PCI (CFGBAR_0_14_0_PCI) — Offset 10h

VMD Configuration Base Address

Type	Size	Offset	Default
PCI	64 bit	[B:0, D:14, F:0] + 10h	000000000000000Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RO	**Reserved**
41:20	000000h RW/V	**Memory Base Address (MEMORY_BASE_ADDRESS):** Sets the location of the CFGBAR in memory space. The size is programmed in CFGBARSZ by BIOS. CFGBARSZ specifies the lowest order address bit that is writeable. The minimum granularity is 1MB. If CFGBAR.Type = 10b, then bits 63:32 are writeable. If CFGBAR.Type = 01b, then bits 63:32 are read-only.
19:4	0h RO	**Reserved**
3	1h RW/L	**Prefetchable CFGBAR (PREFETCHABLE):** BAR points to Prefetchable memory. **Locked by:** VMCONFIG_0_14_0_PCI.VMDLOCK
2:1	2h RW/L	**Type CFGBAR (TYPE_F):** Memory type claimed by this BAR is 64-bit addressable **Locked by:** VMCONFIG_0_14_0_PCI.VMDLOCK
0	0h RO	**Memory Space Indicator (MEMORY_SPACE_INDICATOR):** BAR resource is memory (as opposed to I/O).

9.1.12 MEMBAR1 PCI (MEMBAR1_0_14_0_PCI) — Offset 18h

VMD Memory Base Address Range x

Type	Size	Offset	Default
PCI	64 bit	[B:0, D:14, F:0] + 18h	000000000000000Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
41:12	00000000h RW/V	**Memory Base Address (MEMORY_BASE_ADDRESS):** Sets the location of the MEMBARx in memory space. The size is programmed in MEMBARxSZ by BIOS. MEMBARxSZ specifies the lowest order address bit that is writeable. The minimum granularity is 4kB. If MEMBARx.Type = 10b, then bits 63:32 are writeable. If MEMBARx.Type = 01b, then bits 63:32 are read-only. If MEMBARxSZ = 0, then all address bits are read-only. If MEMBARxSZ < 12, then the effective value is 12.
11:4	0h RO	**Reserved**
3	1h RW/L	**Prefetchable MEMBAR1 (PREFETCHABLE):** BAR points to Prefetchable memory. **Locked by:** VMCONFIG_0_14_0_PCI.VMDLOCK
2:1	2h RW/L	**Type MEMBAR1 (TYPE_F):** Memory type claimed by this BAR is 64-bit addressable **Locked by:** VMCONFIG_0_14_0_PCI.VMDLOCK
0	0h RO	**Memory Space Indicator (MEMORY_SPACE_INDICATOR):** BAR resource is memory (as opposed to I/O).

9.1.13 MEMBAR2 PCI (MEMBAR2_0_14_0_PCI) — Offset 20h

VMD Memory Base Address Range x

Note: **NOTE:** Bit definitions are the same as MEMBAR1_0_14_0_PCI, offset 18h.

9.1.14 SVID PCI (SVID_0_14_0_PCI) — Offset 2Ch

Subsystem Vendor ID

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:14, F:0] + 2Ch	8086h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RW/L	**Subsystem Vendor ID (SUBSYSTEM_VENDOR_ID):** The default value specifies Intel but can be set to any value once after reset. **Locked by:** IOP_WRITE_ONCE_LOCK_0_14_0_CR.VMD_SVID_WOL

9.1.15 SSID PCI (SSID_0_14_0_PCI) — Offset 2Eh

This register contain the VMD Subsystem ID

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:14, F:0] + 2Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/L	**Subsystem_ ID (SUBSYSTEM_ID):** The default value specifies Intel but can be set to any value once after reset. **Locked by:** IOP_WRITE_ONCE_LOCK_0_14_0_CR.VMD_SID_WOL

9.1.16 CAPPTR PCI (CAPPTR_0_14_0_PCI) — Offset 34h

This register contain the VMD Capability Pointer

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:14, F:0] + 34h	80h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	80h RO	**Capability Pointer (CAPABILITY_POINTER):** Points to the first capability structure for the device which is the PCIe capability (for devices that support 4kB extended configuration space). A value of zero indicates there are no capability structures (and no extended configuration space).

9.1.17 INTL PCI (INTL_0_14_0_PCI) — Offset 3Ch

Interrupt Line Register

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:14, F:0] + 3Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**Interrupt Line (INTERRUPT_LINE):** N/A for these devices

9.1.18 INTPIN PCI (INTPIN_0_14_0_PCI) — Offset 3Dh

Interrupt Pin Register

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:14, F:0] + 3Dh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

9.2 Volume Management Device MEMBAR2 Registers

This section contains the Volume Management Device's MEMBAR2 registers.

Base address of these registers are defined in the MEMBAR2_0_14_0_PCI register in Bus: 0, Device: 14, Function: 0.

9.2.1 Summary of Registers

Table 9-2. Summary of MEMBER2 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	8	MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[0])	0000000000000000h
8h	4	MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[0])	00000000h
Ch	4	MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[0])	00000001h
10h	8	MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[1])	0000000000000000h
18h	4	MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[1])	00000000h
1Ch	4	MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[1])	00000001h
20h	8	MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[2])	0000000000000000h
28h	4	MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[2])	00000000h
2Ch	4	MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[2])	00000001h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
30h	8	MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[3])	0000000000000000h
38h	4	MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[3])	00000000h
3Ch	4	MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[3])	00000001h
40h	8	MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[4])	0000000000000000h
48h	4	MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[4])	00000000h
4Ch	4	MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[4])	00000001h
50h	8	MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[5])	0000000000000000h
58h	4	MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[5])	00000000h
5Ch	4	MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[5])	00000001h
60h	8	MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[6])	0000000000000000h
68h	4	MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[6])	00000000h
6Ch	4	MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[6])	00000001h
70h	8	MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[7])	0000000000000000h
78h	4	MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[7])	00000000h
7Ch	4	MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[7])	00000001h
80h	8	MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[8])	0000000000000000h
88h	4	MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[8])	00000000h
8Ch	4	MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[8])	00000001h
90h	8	MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[9])	0000000000000000h
98h	4	MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[9])	00000000h
9Ch	4	MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[9])	00000001h
A0h	8	MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[10])	0000000000000000h
A8h	4	MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[10])	00000000h
ACh	4	MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[10])	00000001h
B0h	8	MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[11])	0000000000000000h
B8h	4	MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[11])	00000000h
BCh	4	MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[11])	00000001h
C0h	8	MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[12])	0000000000000000h
C8h	4	MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[12])	00000000h
CCh	4	MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[12])	00000001h
D0h	8	MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[13])	0000000000000000h
D8h	4	MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[13])	00000000h
DCh	4	MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[13])	00000001h
E0h	8	MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[14])	0000000000000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
E8h	4	MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[14])	00000000h
ECh	4	MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[14])	00000001h
F0h	8	MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[15])	0000000000000000h
F8h	4	MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[15])	00000000h
FCh	4	MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[15])	00000001h
100h	8	MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[16])	0000000000000000h
108h	4	MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[16])	00000000h
10Ch	4	MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[16])	00000001h
110h	8	MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[17])	0000000000000000h
118h	4	MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[17])	00000000h
11Ch	4	MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[17])	00000001h
120h	8	MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[18])	0000000000000000h
128h	4	MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[18])	00000000h
12Ch	4	MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[18])	00000001h
1000h	8	MSIXPBA MEMBAR2 (MSIXPBA_0_14_0_MEMBAR2)	0000000000000000h

9.2.2 MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[0]) — Offset 0h

MSI-X Table Address Register

Type	Size	Offset	Default
MMIO	64 bit	MEMBER2 + 0h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:32	00000000h RW	**MSIX Upper Address (MSI_X_UPPER_ADDRESS):** Upper address bits used when generating an MSI.
31:2	00000000h RW	**MSIX Address (MSI_X_ADDRESS):** System-specified message lower address. For MSI-X messages, the contents of this field from an MSI-X Table entry specifies the lower portion of the DWORD-aligned address (AD[31:02]) for the memory write transaction.
1:0	0h RO	**MSG ADD10 (MSG_ADD10):** For proper DWORD alignment, these bits need to be 0's.

9.2.3 MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[0]) — Offset 8h

MSI-X Message Data Register

Type	Size	Offset	Default
MMIO	32 bit	MEMBER2 + 8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Message Data (MESSAGE_DATA):** System-specified message data.

9.2.4 MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[0]) — Offset Ch

MSI-X Vector Control Register

Type	Size	Offset	Default
MMIO	32 bit	MEMBER2 + Ch	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	1h RW	**MSIX Mask (MSI_X_MASK):** When this bit is set, the NTB is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked.

9.2.5 MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[1]) — Offset 10h

MSI-X Table Address Register

Note: **NOTE:** Bit definitions are the same as MSIXADDR_0_14_0_MEMBAR2[0], offset 0h.

9.2.6 MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[1]) — Offset 18h

MSI-X Message Data Register

Note: **NOTE:** Bit definitions are the same as MSIXDATA_0_14_0_MEMBAR2[0], offset 8h.

9.2.7 MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[1]) — Offset 1Ch

MSI-X Vector Control Register

Note: **NOTE:** Bit definitions are the same as MSIXVCTL_0_14_0_MEMBAR2[0], offset Ch.

9.2.8 MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[2]) — Offset 20h

MSI-X Table Address Register

Note: **NOTE:** Bit definitions are the same as MSIXADDR_0_14_0_MEMBAR2[0], offset 0h.

9.2.9 MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[2]) — Offset 28h

MSI-X Message Data Register

Note: **NOTE:** Bit definitions are the same as MSIXDATA_0_14_0_MEMBAR2[0], offset 8h.

9.2.10 MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[2]) — Offset 2Ch

MSI-X Vector Control Register

Note: **NOTE:** Bit definitions are the same as MSIXVCTL_0_14_0_MEMBAR2[0], offset Ch.

9.2.11 MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[3]) — Offset 30h

MSI-X Table Address Register

Note: **NOTE:** Bit definitions are the same as MSIXADDR_0_14_0_MEMBAR2[0], offset 0h.

9.2.12 MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[3]) — Offset 38h

MSI-X Message Data Register

Note: **NOTE:** Bit definitions are the same as MSIXDATA_0_14_0_MEMBAR2[0], offset 8h.

9.2.13 MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[3]) — Offset 3Ch

MSI-X Vector Control Register

Note: **NOTE:** Bit definitions are the same as MSIXVCTL_0_14_0_MEMBAR2[0], offset Ch.

9.2.14 MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[4]) — Offset 40h

MSI-X Table Address Register

Note: **NOTE:** Bit definitions are the same as MSIXADDR_0_14_0_MEMBAR2[0], offset 0h.

9.2.15 MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[4]) — Offset 48h

MSI-X Message Data Register

Note: **NOTE:** Bit definitions are the same as MSIXDATA_0_14_0_MEMBAR2[0], offset 8h.

9.2.16 MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[4]) — Offset 4Ch

MSI-X Vector Control Register

Note: **NOTE:** Bit definitions are the same as MSIXVCTL_0_14_0_MEMBAR2[0], offset Ch.

9.2.17 MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[5]) — Offset 50h

MSI-X Table Address Register

Note: **NOTE:** Bit definitions are the same as MSIXADDR_0_14_0_MEMBAR2[0], offset 0h.

9.2.18 MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[5]) — Offset 58h

MSI-X Message Data Register

Note: **NOTE:** Bit definitions are the same as MSIXDATA_0_14_0_MEMBAR2[0], offset 8h.

9.2.19 MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[5]) — Offset 5Ch

MSI-X Vector Control Register

Note: **NOTE:** Bit definitions are the same as MSIXVCTL_0_14_0_MEMBAR2[0], offset Ch.

9.2.20 MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[6]) — Offset 60h

MSI-X Table Address Register

Note: **NOTE:** Bit definitions are the same as MSIXADDR_0_14_0_MEMBAR2[0], offset 0h.

9.2.21 MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[6]) — Offset 68h

MSI-X Message Data Register

Note: **NOTE:** Bit definitions are the same as MSIXDATA_0_14_0_MEMBAR2[0], offset 8h.

9.2.22 MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[6]) — Offset 6Ch

MSI-X Vector Control Register

Note: **NOTE:** Bit definitions are the same as MSIXVCTL_0_14_0_MEMBAR2[0], offset Ch.

9.2.23 MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[7]) — Offset 70h

MSI-X Table Address Register

Note: **NOTE:** Bit definitions are the same as MSIXADDR_0_14_0_MEMBAR2[0], offset 0h.

9.2.24 MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[7]) — Offset 78h

MSI-X Message Data Register

Note: **NOTE:** Bit definitions are the same as MSIXDATA_0_14_0_MEMBAR2[0], offset 8h.

9.2.25 MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[7]) — Offset 7Ch

MSI-X Vector Control Register

Note: **NOTE:** Bit definitions are the same as MSIXVCTL_0_14_0_MEMBAR2[0], offset Ch.

9.2.26 MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[8]) — Offset 80h

MSI-X Table Address Register

Note: **NOTE:** Bit definitions are the same as MSIXADDR_0_14_0_MEMBAR2[0], offset 0h.

9.2.27 MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[8]) — Offset 88h

MSI-X Message Data Register

Note: **NOTE:** Bit definitions are the same as MSIXDATA_0_14_0_MEMBAR2[0], offset 8h.

9.2.28 MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[8]) — Offset 8Ch

MSI-X Vector Control Register

Note: **NOTE:** Bit definitions are the same as MSIXVCTL_0_14_0_MEMBAR2[0], offset Ch.

9.2.29 MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[9]) — Offset 90h

MSI-X Table Address Register

Note: **NOTE:** Bit definitions are the same as MSIXADDR_0_14_0_MEMBAR2[0], offset 0h.

9.2.30 MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[9]) — Offset 98h

MSI-X Message Data Register

Note: **NOTE:** Bit definitions are the same as MSIXDATA_0_14_0_MEMBAR2[0], offset 8h.

9.2.31 MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[9]) — Offset 9Ch

MSI-X Vector Control Register

Note: **NOTE:** Bit definitions are the same as MSIXVCTL_0_14_0_MEMBAR2[0], offset Ch.

9.2.32 MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[10]) — Offset A0h

MSI-X Table Address Register

Note: **NOTE:** Bit definitions are the same as MSIXADDR_0_14_0_MEMBAR2[0], offset 0h.

9.2.33 MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[10]) — Offset A8h

MSI-X Message Data Register

Note: **NOTE:** Bit definitions are the same as MSIXDATA_0_14_0_MEMBAR2[0], offset 8h.

9.2.34 MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[10]) — Offset ACh

MSI-X Vector Control Register

Note: **NOTE:** Bit definitions are the same as MSIXVCTL_0_14_0_MEMBAR2[0], offset Ch.

9.2.35 MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[11]) — Offset B0h

MSI-X Table Address Register

Note: **NOTE:** Bit definitions are the same as MSIXADDR_0_14_0_MEMBAR2[0], offset 0h.

9.2.36 MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[11]) — Offset B8h

MSI-X Message Data Register

Note: **NOTE:** Bit definitions are the same as MSIXDATA_0_14_0_MEMBAR2[0], offset 8h.

9.2.37 MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[11]) — Offset BCh

MSI-X Vector Control Register

Note: **NOTE:** Bit definitions are the same as MSIXVCTL_0_14_0_MEMBAR2[0], offset Ch.

9.2.38 MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[12]) — Offset C0h

MSI-X Table Address Register

Note: **NOTE:** Bit definitions are the same as MSIXADDR_0_14_0_MEMBAR2[0], offset 0h.

9.2.39 MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[12]) — Offset C8h

MSI-X Message Data Register

Note: **NOTE:** Bit definitions are the same as MSIXDATA_0_14_0_MEMBAR2[0], offset 8h.

9.2.40 MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[12]) — Offset CCh

MSI-X Vector Control Register

Note: **NOTE:** Bit definitions are the same as MSIXVCTL_0_14_0_MEMBAR2[0], offset Ch.

9.2.41 MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[13]) — Offset D0h

MSI-X Table Address Register

Note: **NOTE:** Bit definitions are the same as MSIXADDR_0_14_0_MEMBAR2[0], offset 0h.

9.2.42 MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[13]) — Offset D8h

MSI-X Message Data Register

Note: **NOTE:** Bit definitions are the same as MSIXDATA_0_14_0_MEMBAR2[0], offset 8h.

9.2.43 MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[13]) — Offset DCh

MSI-X Vector Control Register

Note: **NOTE:** Bit definitions are the same as MSIXVCTL_0_14_0_MEMBAR2[0], offset Ch.

9.2.44 MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[14]) — Offset E0h

MSI-X Table Address Register

Note: **NOTE:** Bit definitions are the same as MSIXADDR_0_14_0_MEMBAR2[0], offset 0h.

9.2.45 MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[14]) — Offset E8h

MSI-X Message Data Register

Note: **NOTE:** Bit definitions are the same as MSIXDATA_0_14_0_MEMBAR2[0], offset 8h.

9.2.46 MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[14]) — Offset ECh

MSI-X Vector Control Register

Note: **NOTE:** Bit definitions are the same as MSIXVCTL_0_14_0_MEMBAR2[0], offset Ch.

9.2.47 MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[15]) — Offset F0h

MSI-X Table Address Register

Note: **NOTE:** Bit definitions are the same as MSIXADDR_0_14_0_MEMBAR2[0], offset 0h.

9.2.48 MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[15]) — Offset F8h

MSI-X Message Data Register

Note: **NOTE:** Bit definitions are the same as MSIXDATA_0_14_0_MEMBAR2[0], offset 8h.

9.2.49 MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[15]) — Offset FCh

MSI-X Vector Control Register

Note: **NOTE:** Bit definitions are the same as MSIXVCTL_0_14_0_MEMBAR2[0], offset Ch.

9.2.50 MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[16]) — Offset 100h

MSI-X Table Address Register

Note: **NOTE:** Bit definitions are the same as MSIXADDR_0_14_0_MEMBAR2[0], offset 0h.

9.2.51 MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[16]) — Offset 108h

MSI-X Message Data Register

Note: **NOTE:** Bit definitions are the same as MSIXDATA_0_14_0_MEMBAR2[0], offset 8h.

9.2.52 MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[16]) — Offset 10Ch

MSI-X Vector Control Register

Note: **NOTE:** Bit definitions are the same as MSIXVCTL_0_14_0_MEMBAR2[0], offset Ch.

9.2.53 MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[17]) — Offset 110h

MSI-X Table Address Register

Note: **NOTE:** Bit definitions are the same as MSIXADDR_0_14_0_MEMBAR2[0], offset 0h.

9.2.54 MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[17]) — Offset 118h

MSI-X Message Data Register

Note: **NOTE:** Bit definitions are the same as MSIXDATA_0_14_0_MEMBAR2[0], offset 8h.

9.2.55 MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[17]) — Offset 11Ch

MSI-X Vector Control Register

Note: **NOTE:** Bit definitions are the same as MSIXVCTL_0_14_0_MEMBAR2[0], offset Ch.

9.2.56 MSIXADDR MEMBAR2 (MSIXADDR_0_14_0_MEMBAR2[18]) — Offset 120h

MSI-X Table Address Register

Note: **NOTE:** Bit definitions are the same as MSIXADDR_0_14_0_MEMBAR2[0], offset 0h.

9.2.57 MSIXDATA MEMBAR2 (MSIXDATA_0_14_0_MEMBAR2[18]) — Offset 128h

MSI-X Message Data Register

Note: **NOTE:** Bit definitions are the same as MSIXDATA_0_14_0_MEMBAR2[0], offset 8h.

9.2.58 MSIXVCTL MEMBAR2 (MSIXVCTL_0_14_0_MEMBAR2[18]) — Offset 12Ch

MSI-X Vector Control Register

Note: **NOTE:** Bit definitions are the same as MSIXVCTL_0_14_0_MEMBAR2[0], offset Ch.

9.2.59 MSIXPBA MEMBAR2 (MSIXPBA_0_14_0_MEMBAR2) — Offset 1000h

MSI-X Pending Bit Array

Type	Size	Offset	Default
MMIO	64 bit	MEMBER2 + 1000h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
63:19	0h RO	**Reserved**
18	0h RO/V	**IntPending 18 (INTPENDING_18):** Represents MSI entry 18
17	0h RO/V	**IntPending 17 (INTPENDING_17):** Bit 17 represents MSI entry 17

Bit Range	Default & Access	Field Name (ID): Description
16	0h RO/V	**IntPending 16 (INTPENDING_16):** Bit 16 represents MSI entry 16
15	0h RO/V	**IntPending 15 (INTPENDING_15):** Bit 15 represents MSI entry 15
14	0h RO/V	**IntPending 14 (INTPENDING_14):** Bit 14 represents MSI entry 14
13	0h RO/V	**IntPending 13 (INTPENDING_13):** Bit 13 represents MSI entry 13
12	0h RO/V	**IntPending 12 (INTPENDING_12):** Bit 12 represents MSI entry 12
11	0h RO/V	**IntPending 11 (INTPENDING_11):** Bit 11 represents MSI entry 11
10	0h RO/V	**IntPending 10 (INTPENDING_10):** Bit 10 represents MSI entry 10
9	0h RO/V	**IntPending 9 (INTPENDING_9):** Bit 9 represents MSI entry 9
8	0h RO/V	**IntPending 8 (INTPENDING_8):** Bit 8 represents MSI entry 8
7	0h RO/V	**IntPending 7 (INTPENDING_7):** Bit 7 represents MSI entry 7
6	0h RO/V	**IntPending 6 (INTPENDING_6):** Bit 6 represents MSI entry 6
5	0h RO/V	**IntPending 5 (INTPENDING_5):** Bit 5 represents MSI entry 5
4	0h RO/V	**IntPending 4 (INTPENDING_4):** Bit 4 represents MSI entry 4
3	0h RO/V	**IntPending 3 (INTPENDING_3):** Bit 3 represents MSI entry 3
2	0h RO/V	**IntPending 2 (INTPENDING_2):** Bit 2 represents MSI entry 2
1	0h RO/V	**IntPending 1 (INTPENDING_1):** Bit 1 represents MSI entry 1
0	0h RO/V	**IntPending 0 (INTPENDING_0):** Bit 0 represents MSI entry 0

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**INTP INTPIN (INTP):** Interrupt Pin. N/A since these devices do not generate any interrupt on their own

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10 USB Subsystem Registers (D13:F0/F1)

This chapter documents the Subsystem Registers.

Table 10-1. Summary of Subsystem (SS)

"USB Host Controller (xHCI) Registers (D13:F0)"
"USB Host Controller MBAR Registers (D13:F0)"
"USB Device Controller (xDCI) Configuration Registers (D13:F1)"

10.1 USB Host Controller (xHCI) Registers (D13:F0)

This section contains the registers in Bus: 0, Device: 13, Function: 0.

10.1.1 Summary of Registers

Table 10-2. Summary of Bus: 0, Device: 13, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	2	Vendor ID (VID)	8086h
2h	2	Device ID (DID)	8C31h
4h	2	Command Reg (CMD)	0000h
6h	2	Device Status (STS)	0290h
8h	1	Revision ID (RID)	00h
9h	1	Programming Interface (PI)	30h
Ah	1	Sub Class Code (SCC)	03h
Bh	1	Base Class Code (BCC)	0Ch
Ch	1	Cache Line Size (CLS)	00h
Dh	1	INITIATOR Latency Timer (MLT)	00h
Eh	1	Header Type (HT)	80h
10h	8	Memory Base Address (MBAR)	0000000000000004h
2Ch	2	USB Subsystem Vendor ID (SSVID)	0000h
2Eh	2	USB Subsystem ID (SSID)	0000h
34h	1	Capabilities Pointer (CAP_PTR)	70h
3Ch	1	Interrupt Line (ILINE)	00h
3Dh	1	Interrupt Pin (IPIN)	00h
58h	4	Audio Time Synchronization (AUDSYNC)	00000000h
60h	1	Serial Bus Release Number (SBRN)	32h
61h	1	Frame Length Adjustment (FLADJ)	60h
62h	1	Best Effort Service Latency (BESL)	00h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
70h	1	PCI Power Management Capability ID (PM_CID)	01h
71h	1	Next Item Pointer 1 (PM_NEXT)	80h
72h	2	Power Management Capabilities (PM_CAP)	C1C2h
74h	2	Power Management Control/Status (PM_CS)	0008h
80h	1	Message Signaled Interrupt CID (MSI_CID)	05h
81h	1	Next Item Pointer (MSI_NEXT)	90h
82h	2	Message Signaled Interrupt Message Control (MSI_MCTL)	0086h
84h	4	Message Signaled Interrupt Message Address (MSI_MAD)	00000000h
88h	4	Message Signaled Interrupt Upper Address (MSI_MUAD)	00000000h
8Ch	2	Message Signaled Interrupt Message Data (MSI_MD)	0000h
A4h	4	High Speed Configuration 2 (HSCFG2)	00003800h

10.1.2 Vendor ID (VID) — Offset 0h

Vendor ID

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:13, F:0] + 0h	8086h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RO	**Vendor ID (VID):** Vendor ID

10.1.3 Device ID (DID) — Offset 2h

Device ID

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:13, F:0] + 2h	8C31h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
15:0	8C31h RO/V	**Device ID (DID):** See Global Device ID table in Chap. 6 for value

10.1.4 Command Reg (CMD) — Offset 4h

Command Reg

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:13, F:0] + 4h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable (INTR_DIS):** When cleared to 0, the function is capable of generating interrupts. When 1, the function can not generate its interrupt to the interrupt controller. Note that the corresponding Interrupt Status bit is not affected by the interrupt enable.
9	0h RO	**Fast Back to Back Enable (FBE):** Fast Back to Back Enable
8	0h RW	**SERR Enable (SERR):** When set to 1, the XHC is capable of generating (internally) SERR#.
7	0h RO	**Wait Cycle Control (WCC):** Wait Cycle Control
6	0h RW	**Parity Error Response (PER):** When set to 1, the XHCI Host Controller will check for correct parity (on its internal interface) and halt operation when bad parity is detected during the data phase as recommended by the XHCI specification. Note that this applies to both requests and completions from the system interface. This bit must be set in order for the parity errors to generate SERR#.
5	0h RO	**VGA Palette Snoop (VPS):** VGA Palette Snoop
4	0h RO	**Memory Write Invalidate (MWI):** Memory Write Invalidate

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**Special Cycle Enable (SCE):** Special Cycle Enable
2	0h RW	**Bus Initiator Enable (BME):** When set, it allows XHC to act as a bus initiator. When cleared, it disable XHC from initiating transactions on the system bus.
1	0h RW	**Memory Space Enable (MSE):** This bit controls access to the XHC Memory Space registers. If this bit is set, accesses to the XHC registers are enabled. The Base Address register for the XHC should be programmed before this bit is set.
0	0h RO	**I/O Space Enable (IOSE):** Reserved

10.1.5 Device Status (STS) — Offset 6h

Device Status

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:13, F:0] + 6h	0290h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**Detected Parity Error (DPE):** This bit is set by the PCH whenever a parity error is seen on the internal interface to the XHC host controller, regardless of the setting of bit 6 or bit 8 in the Command register or any other conditions. Software clears this bit by writing a 1 to this bit location.
14	0h RW/1C	**Signaled System Error (SSE):** This bit is set by the PCH whenever it signals SERR# (internally). The SERR_EN bit (bit 8 in the Command Register) must be 1 for this bit to be set.
13	0h RW/1C	**Received Initiator-Abort Status (RMA):** This bit is set when XHC, as a Initiator, receives a initiator-abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location.
12	0h RW/1C	**Received Target Abort Status (RTA):** This bit is set when XHC, as a initiator, receives a target abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location.
11	0h RW/1C	**Signaled Target-Abort Status (STA):** This bit is used to indicate when the XHC function responds to a cycle with a target abort.
10:9	1h RO	**DEVSEL Timing Status (DEVT):** This 2-bit field defines the timing for DEVSEL# assertion. Read-Only.
8	0h RW/1C	**Initiator Data Parity Error Detected (MDPED):** This bit is set by the PCH whenever a data parity error is detected on a XHC read completion packet on the internal interface to the XHC host controller and bit 6 of the Command register is set to 1. Software clears this bit by writing a 1 to this bit location.

Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Fast Back-to-Back Capable (FBBC):** Reserved
6	0h RO	**User Definable Features (UDF):** Reserved
5	0h RO	**66 MHz Capable (MC):** Reserved
4	1h RO	**Capabilities List (CL):** Hardwired to 1 indicating that offset 34h contains a valid capabilities pointer.
3	0h RO/V	**Interrupt Status (INTR_STS):** This read-only bit reflects the state of this function's interrupt at the input of the enable/disable logic. This bit is a 1 when the interrupt is asserted. This bit will be 0 when the interrupt is deasserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
2:0	0h RO	**Reserved**

10.1.6 Revision ID (RID) — Offset 8h

Revision ID

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:13, F:0] + 8h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO/V	**Revision ID (RID):** See Chap 6 for value.

10.1.7 Programming Interface (PI) — Offset 9h

Programming Interface

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:13, F:0] + 9h	30h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	30h RO	**Programming Interface (PI):** A value of 30h indicates that this USB Host Controller conforms to the XHCI specification.

10.1.8 Sub Class Code (SCC) — Offset Ah

Sub Class Code

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:13, F:0] + Ah	03h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	03h RO	**Sub Class Code (SCC):** A value of 03h indicates that this is a Universal Serial Bus Host Controller.

10.1.9 Base Class Code (BCC) — Offset Bh

Base Class Code

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:13, F:0] + Bh	0Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	0Ch RO	**Base Class Code (BCC):** A value of 0Ch indicates that this is a Serial Bus controller.

10.1.10 Cache Line Size (CLS) — Offset Ch

Cache Line Size

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:13, F:0] + Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Cache Line Size (CLS):** Cache Line Size

10.1.11 Initiator Latency Timer (MLT) — Offset Dh

Initiator Latency Timer

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:13, F:0] + Dh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**Initiator Latency Timer (MLT):** Because the XHC controller is internally implemented with arbitration on an internal interface, it does not need a initiator latency timer. The bits will be fixed at 0.

10.1.12 Header Type (HT) — Offset Eh

Header Type

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:13, F:0] + Eh	80h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Multi-Function Bit (MFB):** Read only indicating single function device.
6:0	00h RO	**Configuration layout (CL):** Hardwired to 0 to indicate a standard PCI configuration layout.

10.1.13 Memory Base Address (MBAR) — Offset 10h

Value in this register will be different after the enumeration process.

Type	Size	Offset	Default
PCI	64 bit	[B:0, D:13, F:0] + 10h	0000000000000004h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:16	00000000 0000h RW	**Base Address (BA):** Bits (63:16) correspond to memory address signals (63:16), respectively. This gives 64 KB of relocatable memory space aligned to 64 KB boundaries.
15:4	0h RO	**Reserved**
3	0h RO	**Prefetchable Indication (PREFETCHABLE):** This bit is hardwired to 0 indicating that this range should not be prefetched.
2:1	2h RO	**Type Indication (MBAR_TYPE):** If this field is hardwired to 00 it indicates that this range can be mapped anywhere within 32-bit address space. If this field is hardwired to 10 it indicates that this range can be mapped anywhere within 64-bit address space.
0	0h RO	**Resource Type Indicator (RTE):** This bit is hardwired to 0 indicating that the base address field in this register maps to memory space

10.1.14 USB Subsystem Vendor ID (SSVID) — Offset 2Ch

This register is modified and maintained by BIOS

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:13, F:0] + 2Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/L	**USB Subsystem Vendor ID (SSVID):** This register, in combination with the USB Subsystem ID register, enables the operating system to distinguish each subsystem from the others.

10.1.15 USB Subsystem ID (SSID) — Offset 2Eh

This register is modified and maintained by BIOS

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:13, F:0] + 2Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/L	**USB Subsystem ID (SSID):** BIOS sets the value in this register to identify the Subsystem ID. This register, in combination with the Subsystem Vendor ID register, enables the operating system to distinguish each subsystem from other(s).

10.1.16 Capabilities Pointer (CAP_PTR) — Offset 34h

Capabilities Pointer

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:13, F:0] + 34h	70h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	70h RO	**Capabilities Pointer (CAP_PTR):** This register points to the starting offset of the capabilities ranges.

10.1.17 Interrupt Line (ILINE) — Offset 3Ch

Interrupt Line

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:13, F:0] + 3Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Interrupt Line (ILINE):** This data is not used by the PCH. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to.

10.1.18 Interrupt Pin (IPIN) — Offset 3Dh

This register is modified and maintained by BIOS

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:13, F:0] + 3Dh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW/L	**Interrupt pin (IPIN):** Bits 7:0 reflect the Interrupt Pin assigned to the host controller by the platform (and are hardwired). **Locked by:** XHCC1.ACCTRL

10.1.19 Audio Time Synchronization (AUDSYNC) — Offset 58h

This 32 bit register is used for audio stream synchronization across different devices. Global signal sample_now captures a value in AUDSYNC register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:13, F:0] + 58h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:16	0000h RO/V	**Captured Frame List Current Index/Frame Number (CMFI):** The value in this register is updated in response to sample_now signal. Bits (29:16) reflect state of bits (13:0) of FRINDEX
15:13	0h RO	**Reserved**
12:0	0000h RO/V	**Captured Micro-frame BLIF (CMFB):** The value is updated in response to sample_now signal and provides information about offset within micro-frame. Captured value represents number of 8 high-speed bit time units from start of micro-frame. At the beginning of micro-frame captured value will be 0 and increase to maximum value at the end. Default maximum value is 7499 but it may be changed as result of adjustment done in FLA.

10.1.20 Serial Bus Release Number (SBRN) — Offset 60h

Serial Bus Release Number

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:13, F:0] + 60h	32h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	32h RW/L	**Serial Bus Release Number (SBRN):** A value of 32h indicates that this controller follows USB release 3.2. **Locked by:** XHCC1.ACCTRL

10.1.21 Frame Length Adjustment (FLADJ) — Offset 61h

This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written into these six bits, the length of the frame is adjusted. Its initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system BIOS. This register should only be modified when the HChalted bit in the USBSTS register is a one. Changing value of this register while the host controller is operating yields undefined results.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:13, F:0] + 61h	60h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6	1h RO	**No Frame Length Timing Capability (NO_FRAME_LENGTH_TIMING_CAP):** This flag is set to 1 to indicate that the host controller does not support a programmable Frame Length Timing Value field.

Bit Range	Default & Access	Field Name (ID): Description
5:0	20h RO	**Frame Length Timing Value (FLTV):** SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (number of High Speed bit times) FLADJ Value (decimal) (decimal) 59488 0 (00h) 59504 1 (01h) 59520 2 (02h) ... 59984 31 (1Fh) 60000 32 (20h) ... 60480 62 (3Eh) 60496 63 (3Fh) Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (# High Speed bit times) FLADJ Value

10.1.22 Best Effort Service Latency (BESL) — Offset 62h

Bset Effort Service Latency.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:13, F:0] + 62h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RW/L	**Default Best Effort Service Latency Deep (DBESLD):** Default Best Effort Service Latency (DBESLD) If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESLD field. This is programmed by BIOS based on platform parameters. **Locked by:** XHCC1.ACCTRL
3:0	0h RW/L	**Default Best Effort Service Latency (DBESL):** If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESL field. This is programmed by BIOS based on platform parameters. **Locked by:** XHCC1.ACCTRL

10.1.23 PCI Power Management Capability ID (PM_CID) — Offset 70h

PCI Power Management Capability ID

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:13, F:0] + 70h	01h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	01h RO	**PCI Power Management Capability ID (PM_CID):** A value of 01h indicates that this is a PCI Power Management capabilities field.

10.1.24 Next Item Pointer 1 (PM_NEXT) — Offset 71h

This register is modified and maintained by BIOS

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:13, F:0] + 71h	80h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	80h RW/L	**Next Item Pointer 1 (PM_NEXT):** This register defaults to 80h, which indicates that the next capability registers begin at configuration offset 80h. This register is writable when the Access Control bit is set to '0'. This allows BIOS to effectively hide the next capability registers, if necessary. This register should only be written during system initialization before the plug-and-play software has enabled any initiator-initiated traffic. Values of: 80h implies next capability is MSI 00h implies that MSI capability is hidden. Note: This value is never expected to be programmed. **Locked by:** XHCC1.ACCTRL

10.1.25 Power Management Capabilities (PM_CAP) — Offset 72h

Normally, this register is read-only to report capabilities to the power management software. In order to report different power management capabilities depending on the system in which the PCH is used, the write access to this register is controlled by the Access Control bit (ACCTRL). The value written to this register does not affect the hardware other than changing the value returned during a read.

This register is modified and maintained by BIOS

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:13, F:0] + 72h	C1C2h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:11	18h RW/L	**PME Support (PME_SUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. The PCH XHC does not support the D1 or D2 states. For all other states, the PCH XHC is capable of generating PME#. Software should never need to modify this field.
10	0h RW/L	**D2 Support (D2_SUPPORT):** The D2 state is not supported. **Locked by:** XHCC1.ACCTRL
9	0h RW/L	**D1 Support (D1_SUPPORT):** The D1 state is not supported. **Locked by:** XHCC1.ACCTRL
8:6	7h RW/L	**Aux Current (AUX_CURRENT):** The PCH XHC reports 375mA maximum Suspend well current required when in the D3cold state. This value can be written by BIOS when a more accurate value is known. **Locked by:** XHCC1.ACCTRL
5	0h RW/L	**Device Specific Initialization (DSI):** The PCH reports 0, indicating that no device-specific initialization is required. **Locked by:** XHCC1.ACCTRL
4	0h RO	**Reserved**
3	0h RW/L	**PME Clock (PMECLOCK):** The PCH reports 0, indicating that no PCI clock is required to generate PME#. **Locked by:** XHCC1.ACCTRL
2:0	2h RW/L	**Version Indication (VERSION):** The PCH reports 010, indicating that it complies with Revision 1.1 of the PCI Power Management Specification. **Locked by:** XHCC1.ACCTRL

10.1.26 Power Management Control/Status (PM_CS) — Offset 74h

Power Management Control/Status

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:13, F:0] + 74h	0008h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**PME Status (PME_STATUS):** This bit is set when the PCH XHC would normally assert the PME# signal independent of the state of the PME_En bit. Writing a 1 to this bit will clear it and cause the internal PME to deassert (if enabled). Writing a 0 has no effect. This bit must be explicitly cleared by the operating system each time the operating system is loaded.
14:13	0h RO	**Data Scale (DATA_SCALE):** The PCH hardwires these bits to 00 because it does not support the associated Data register.
12:9	0h RO	**Data Select (DATA_SELECT):** The PCH hardwires these bits to 0000 because it does not support the associated Data register.
8	0h RW	**PME Enable (PME_EN):** A 1 enables the PCH XHC to generate an internal PME signal when PME_Status is 1. This bit must be explicitly cleared by the operating system each time it is initially loaded.
7:4	0h RO	**Reserved**
3	1h RW/L	**No Soft Reset (NSR):** No_Soft_Reset - When set ("1"), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. Transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled. **Locked by:** XHCC1.ACCTRL
2	0h RO	**Reserved**
1:0	0h RW	**Power State (POWERSTATE):** This 2-bit field is used both to determine the current power state of XHC function and to set a new power state. The definition of the field values are: 00b - D0 state 11b - D3hot state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally, however, the data is discarded and no state change occurs. When in the D3hot state, the PCH must not accept accesses to the XHC memory range, but the configuration space must still be accessible.

10.1.27 Message Signaled Interrupt CID (MSI_CID) — Offset 80h

Message Signaled Interrupt CID

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:13, F:0] + 80h	05h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	05h RO	**Capability ID (CID):** Indicates that this is an MSI capability

10.1.28 Next Item Pointer (MSI_NEXT) — Offset 81h

Next Item Pointer

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:13, F:0] + 81h	90h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	90h RW/L	**Next Pointer (NEXT_POINTER):** Indicates that this is the last item on the capability list **Locked by:** XHCC1.ACCTRL

10.1.29 Message Signaled Interrupt Message Control (MSI_MCTL) — Offset 82h

Message Signaled Interrupt Message Control

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:13, F:0] + 82h	0086h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	**Reserved**
8	0h RO	**Per-Vector Masking Capable (PVM):** Specifies whether controller supports MSI per vector masking. Not supported
7	1h RO	**64 Bit Address Capable (C64):** Specifies whether capable of generating 64-bit messages. This device is 64-bit capable.
6:4	0h RW	**Multiple Message Enable (MME):** Indicates the number of messages the controller should assert. This device supports multiple message MSI.
3:1	3h RO	**Multiple Message Capable (MMC):** Indicates the number of messages the controller wishes to assert. This field must be set by HW to reflect the number of Interrupters supported. Encoding number of Vectors requested (number of Interrupters) 000 1 001 2 010 4 011 8 100 16 101 32 110-111 Reserved
0	0h RW	**MSI Enable (MSIE):** If set to 1, MSI is enabled and the traditional interrupt pins are not used to generate interrupts. If cleared to 0, MSI operation is disabled and the traditional interrupt pins are used.

10.1.30 Message Signaled Interrupt Message Address (MSI_MAD) — Offset 84h

Message Signaled Interrupt Message Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:13, F:0] + 84h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**Lower DW Address (ADDR):** Lower DW of system specified message address, always DWORD aligned
1:0	0h RO	**Reserved**

10.1.31 Message Signaled Interrupt Upper Address (MSI_MUAD) — Offset 88h

Message Signaled Interrupt Upper Address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:13, F:0] + 88h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Upper Addr (UPPERADDR):** Upper DW of system specified message address.

10.1.32 Message Signaled Interrupt Message Data (MSI_MD) — Offset 8Ch

Message Signaled Interrupt Message Data

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:13, F:0] + 8Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**Data Field (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD(15:0)) during the data phase of the MSI memory write transaction. The Multiple Message Enable field (bits 6-4 of the Message Control register) defines the number of low order message data bits the function is permitted to modify to generate its system software allocated vectors. For example, a Multiple Message Enable encoding of 010 indicates the function has been allocated four vectors and is permitted to modify message data bits 1 and 0 (a function modifies the lower message data bits to generate the allocated number of vectors). If the Multiple Message Enable field is 000, the function is not permitted to modify the message data.

10.1.33 High Speed Configuration 2 (HSCFG2) — Offset A4h

High Speed Configuration 2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:13, F:0] + A4h	00003800h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW	**PORT1 Host Mode Override (PORT1_HOST_MODE_OVERRIDE):** When set, this bit causes the Host_Device mux on port 1 to be forced into the Host mode.
17:16	0h RW	**EUSB2SEL:** The two bits are associate with USB2 ports 1 - bit 16 and 2 - bit 2 0: Port is mapped to USB2 1: Port is mapped to eUSB2
15	0h RW	**HS ASYNC Active IN Mask (HSAAIM):** Determines if the Async Active will mask/ignore IN EP s. 0 HS ASYNC Active will include IN EP s. 1 HS ASYNC Active will mask/ignore IN EP s.
14	0h RW	**HS OUT ASYNC Active Polling EP Mask (HSOAAPEPM):** Determines if the Async Active for OUT HS/FS/LS masks/ignores EP s that are polling/PINGing (HS) due to NAK. 0 HS OUT ASYNC Active will include EP s that are polling. 1 HS OUT ASYNC Active will mask/ignore EP s that are polling.
13	1h RW	**HS IN ASYNC Active Polling EP Mask (HSIAAPEPM):** Determines if the Async Active for IN HS/FS/LS masks/ignores EP s that are polling due to NAK. 0 HS IN ASYNC Active will include EP s that are polling. 1 HS IN ASYNC Active will mask/ignore EP s that are polling.
12:11	3h RW	**HS INTR IN Periodic Active Policy Control (HSIIPAPC):** Controls how the HS INTR IN periodic active is used to generate the global periodic active. This will determine how the smallest service interval among active EP s and number of active EP s are used. 0 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold OR Numb of EP Threshold values meet the requirement. 1 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold AND Numb of EP Threshold values meet the requirement. 2 Always allow HS INTR EP s to be used in the generation of the global Periodic Active indication. 3 Never allow HS INTR EP s to be used in the generation of the global Periodic Active indicaiton
10:4	00h RW	**HS INTR IN Periodic Active Num of EP Threshold (HSIIPANEPT):** Defines the threshold used to determine if Periodic Acive may include HS/FS/LS INTR IN EP active indication. If there are more than NumEPThreshold active HS/FS/LS INTR EP s then they may be included as part of the periodic active generation.
3:0	0h RW	**HS INTR IN Periodic Active Service Interval Threshold (HSIIPASIT):** Defines the Service Interval threshold used to determine if Periodic Acive will include HS/FS/LS INTR IN EP active indication. If there are any active HS/FS/LS INTR EP s with a service interval less than or equal to this threshold then they may be included as part of the periodic active generation.

10.2 USB Host Controller MBAR Registers (D13:F0)

This section contains the USB Host Controller MBAR registers. The Base address of these registers is defined in the MBAR register which resides in the USB Host Controller register collection (D13:F0).

10.2.1 Summary of Registers

Table 10-3. Summary of MBAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	1	Capability Registers Length (CAPLENGTH)	80h
2h	2	Host Controller Interface Version Number (HCIVERSION)	0110h
4h	4	Structural Parameters 1 (HCSPARAMS1)	05000840h
8h	4	Structural Parameters 2 (HCSPARAMS2)	14200054h
Ch	4	Structural Parameters 3 (HCSPARAMS3)	00A0000Ah
10h	4	Capability Parameters (HCCPARAMS)	20007FC1h
14h	4	Doorbell Offset (DBOFF)	00003000h
18h	4	Runtime Register Space Offset (RTSOFF)	00002000h
80h	4	USB Command (USBCMD)	00000000h
84h	4	USB Status (USBSTS)	00000001h
88h	4	Page Size (PAGESIZE)	00000001h
94h	4	Device Notification Control (DNCTRL)	00000000h
98h	4	Command Ring Low (CRCR_LO)	00000000h
9Ch	4	Command Ring High (CRCR_HI)	00000000h
B0h	4	Device Context Base Address Array Pointer Low (DCBAAP_LO)	00000000h
B4h	4	Device Context Base Address Array Pointer High (DCBAAP_HI)	00000000h
B8h	4	Configure Reg (CONFIG)	00000000h
480h	4	Port Status AndControl USB2 (PORTSC1)	000002A0h
484h	4	Port Power Management Status Aand Control USB2 (PORTPMSC1)	00000000h
48Ch	4	Port X Hardware LPM Control Register (PORTHLPMC1)	00000000h
490h	4	Port Status And Control USB3 (PORTSC2)	000002A0h
494h	4	Port Power Management Status And Control USB3 (PORTPMSC2)	00000000h
498h	4	USB3 Port Link Info (PORTLI2)	00000000h
4A0h	4	Port Status And Control USB3 (PORTSC3)	000002A0h
4A4h	4	Port Power Management Status And Control USB3 (PORTPMSC3)	00000000h
4A8h	4	USB3 Port Link Info (PORTLI3)	00000000h
4B0h	4	Port Status And Control USB3 (PORTSC4)	000002A0h
4B4h	4	Port Power Management Status And Control USB3 (PORTPMSC4)	00000000h
4B8h	4	USB3 Port Link Info (PORTLI4)	00000000h
4C0h	4	Port Status And Control USB3 (PORTSC5)	000002A0h
4C4h	4	Port Power Management Status And Control USB3 (PORTPMSC5)	00000000h
4C8h	4	USB3 Port Link Info (PORTLI5)	00000000h
2000h	4	Microframe Index (RTMFINDEX)	00000000h
2020h	4	Interrupter Management (IMAN0)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
2024h	4	Interrupter Moderation (IMOD0)	00000FA0h
2028h	4	Event Ring Segment Table Size (ERSTSZ0)	00000000h
2030h	4	Event Ring Segment Table Base Address Low (ERSTBA_LO0)	00000000h
2034h	4	Event Ring Segment Table Base Address High (ERSTBA_HI0)	00000000h
2038h	4	Event Ring Dequeue Pointer Low (ERDP_LO0)	00000000h
203Ch	4	Event Ring Dequeue Pointer High (ERDP_HI0)	00000000h
2040h	4	Interrupter Management (IMAN1)	00000000h
2044h	4	Interrupter Moderation (IMOD1)	00000FA0h
2048h	4	Event Ring Segment Table Size (ERSTSZ1)	00000000h
2050h	4	Event Ring Segment Table Base Address Low (ERSTBA_LO1)	00000000h
2054h	4	Event Ring Segment Table Base Address High (ERSTBA_HI1)	00000000h
2058h	4	Event Ring Dequeue Pointer Low (ERDP_LO1)	00000000h
205Ch	4	Event Ring Dequeue Pointer High (ERDP_HI1)	00000000h
2060h	4	Interrupter Management (IMAN2)	00000000h
2064h	4	Interrupter Moderation (IMOD2)	00000FA0h
2068h	4	Event Ring Segment Table Size (ERSTSZ2)	00000000h
2070h	4	Event Ring Segment Table Base Address Low (ERSTBA_LO2)	00000000h
2074h	4	Event Ring Segment Table Base Address High (ERSTBA_HI2)	00000000h
2078h	4	Event Ring Dequeue Pointer Low (ERDP_LO2)	00000000h
207Ch	4	Event Ring Dequeue Pointer High (ERDP_HI2)	00000000h
2080h	4	Interrupter Management (IMAN3)	00000000h
2084h	4	Interrupter Moderation (IMOD3)	00000FA0h
2088h	4	Event Ring Segment Table Size (ERSTSZ3)	00000000h
2090h	4	Event Ring Segment Table Base Address Low (ERSTBA_LO3)	00000000h
2094h	4	Event Ring Segment Table Base Address High (ERSTBA_HI3)	00000000h
2098h	4	Event Ring Dequeue Pointer Low (ERDP_LO3)	00000000h
209Ch	4	Event Ring Dequeue Pointer High (ERDP_HI3)	00000000h
20A0h	4	Interrupter Management (IMAN4)	00000000h
20A4h	4	Interrupter Moderation (IMOD4)	00000FA0h
20A8h	4	Event Ring Segment Table Size (ERSTSZ4)	00000000h
20B0h	4	Event Ring Segment Table Base Address Low (ERSTBA_LO4)	00000000h
20B4h	4	Event Ring Segment Table Base Address High (ERSTBA_HI4)	00000000h
20B8h	4	Event Ring Dequeue Pointer Low (ERDP_LO4)	00000000h
20BCh	4	Event Ring Dequeue Pointer High (ERDP_HI4)	00000000h
20C0h	4	Interrupter Management (IMAN5)	00000000h
20C4h	4	Interrupter Moderation (IMOD5)	00000FA0h
20C8h	4	Event Ring Segment Table Size (ERSTSZ5)	00000000h
20D0h	4	Event Ring Segment Table Base Address Low (ERSTBA_LO5)	00000000h
20D4h	4	Event Ring Segment Table Base Address High (ERSTBA_HI5)	00000000h
20D8h	4	Event Ring Dequeue Pointer Low (ERDP_LO5)	00000000h
20DCh	4	Event Ring Dequeue Pointer High (ERDP_HI5)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
20E0h	4	Interrupter Management (IMAN6)	00000000h
20E4h	4	Interrupter Moderation (IMOD6)	00000FA0h
20E8h	4	Event Ring Segment Table Size (ERSTSZ6)	00000000h
20F0h	4	Event Ring Segment Table Base Address Low (ERSTBA_LO6)	00000000h
20F4h	4	Event Ring Segment Table Base Address High (ERSTBA_HI6)	00000000h
20F8h	4	Event Ring Dequeue Pointer Low (ERDP_LO6)	00000000h
20FCh	4	Event Ring Dequeue Pointer High (ERDP_HI6)	00000000h
2100h	4	Interrupter Management (IMAN7)	00000000h
2104h	4	Interrupter Moderation (IMOD7)	00000FA0h
2108h	4	Event Ring Segment Table Size (ERSTSZ7)	00000000h
2110h	4	Event Ring Segment Table Base Address Low (ERSTBA_LO7)	00000000h
2114h	4	Event Ring Segment Table Base Address High (ERSTBA_HI7)	00000000h
2118h	4	Event Ring Dequeue Pointer Low (ERDP_LO7)	00000000h
211Ch	4	Event Ring Dequeue Pointer High (ERDP_HI7)	00000000h
3000h	4	Door Bell (DB0)	00000000h
3004h	4	Door Bell (DB1)	00000000h
3008h	4	Door Bell (DB2)	00000000h
300Ch	4	Door Bell (DB3)	00000000h
3010h	4	Door Bell (DB4)	00000000h
3014h	4	Door Bell (DB5)	00000000h
3018h	4	Door Bell (DB6)	00000000h
301Ch	4	Door Bell (DB7)	00000000h
3020h	4	Door Bell (DB8)	00000000h
3024h	4	Door Bell (DB9)	00000000h
3028h	4	Door Bell (DB10)	00000000h
302Ch	4	Door Bell (DB11)	00000000h
3030h	4	Door Bell (DB12)	00000000h
3034h	4	Door Bell (DB13)	00000000h
3038h	4	Door Bell (DB14)	00000000h
303Ch	4	Door Bell (DB15)	00000000h
3040h	4	Door Bell (DB16)	00000000h
3044h	4	Door Bell (DB17)	00000000h
3048h	4	Door Bell (DB18)	00000000h
304Ch	4	Door Bell (DB19)	00000000h
3050h	4	Door Bell (DB20)	00000000h
3054h	4	Door Bell (DB21)	00000000h
3058h	4	Door Bell (DB22)	00000000h
305Ch	4	Door Bell (DB23)	00000000h
3060h	4	Door Bell (DB24)	00000000h
3064h	4	Door Bell (DB25)	00000000h
3068h	4	Door Bell (DB26)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
306Ch	4	Door Bell (DB27)	00000000h
3070h	4	Door Bell (DB28)	00000000h
3074h	4	Door Bell (DB29)	00000000h
3078h	4	Door Bell (DB30)	00000000h
307Ch	4	Door Bell (DB31)	00000000h
3080h	4	Door Bell (DB32)	00000000h
3084h	4	Door Bell (DB33)	00000000h
3088h	4	Door Bell (DB34)	00000000h
308Ch	4	Door Bell (DB35)	00000000h
3090h	4	Door Bell (DB36)	00000000h
3094h	4	Door Bell (DB37)	00000000h
3098h	4	Door Bell (DB38)	00000000h
309Ch	4	Door Bell (DB39)	00000000h
30A0h	4	Door Bell (DB40)	00000000h
30A4h	4	Door Bell (DB41)	00000000h
30A8h	4	Door Bell (DB42)	00000000h
30ACh	4	Door Bell (DB43)	00000000h
30B0h	4	Door Bell (DB44)	00000000h
30B4h	4	Door Bell (DB45)	00000000h
30B8h	4	Door Bell (DB46)	00000000h
30BCh	4	Door Bell (DB47)	00000000h
30C0h	4	Door Bell (DB48)	00000000h
30C4h	4	Door Bell (DB49)	00000000h
30C8h	4	Door Bell (DB50)	00000000h
30CCh	4	Door Bell (DB51)	00000000h
30D0h	4	Door Bell (DB52)	00000000h
30D4h	4	Door Bell (DB53)	00000000h
30D8h	4	Door Bell (DB54)	00000000h
30DCh	4	Door Bell (DB55)	00000000h
30E0h	4	Door Bell (DB56)	00000000h
30E4h	4	Door Bell (DB57)	00000000h
30E8h	4	Door Bell (DB58)	00000000h
30ECh	4	Door Bell (DB59)	00000000h
30F0h	4	Door Bell (DB60)	00000000h
30F4h	4	Door Bell (DB61)	00000000h
30F8h	4	Door Bell (DB62)	00000000h
30FCh	4	Door Bell (DB63)	00000000h
3100h	4	Door Bell (DB64)	00000000h
8000h	4	XECP SUPP USB2_0 (XECP_SUPP_USB2_0)	02000802h
8004h	4	XECP SUPP USB2_1 (XECP_SUPP_USB2_1)	20425355h
8008h	4	XECP SUPP USB2_2 (XECP_SUPP_USB2_2)	30180101h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
800Ch	4	XECP SUPP USB3_3 (XECP_SUPP_USB2_3)	00000000h
8010h	4	XECP SUPP USB2_4 Full Speed (XECP_SUPP_USB2_4)	000C0021h
8014h	4	XECP_SUPP USB2_5 Low Speed (XECP_SUPP_USB2_5)	05DC0012h
8018h	4	XECP SUPP USB2_6 High Speed (XECP_SUPP_USB2_6)	01E00023h
8020h	4	XECP SUPP USB3_0 (XECP_SUPP_USB3_0)	03201402h
8024h	4	XECP SUPP USB3_1 (XECP_SUPP_USB3_1)	20425355h
8028h	4	XECP SUPP USB3_2 (XECP_SUPP_USB3_2)	40000402h
802Ch	4	XECP SUPP USB3_3 (XECP_SUPP_USB3_3)	00000000h
8030h	4	XECP SUPP USB3_4 (XECP_SUPP_USB3_4)	00050134h
8034h	4	XECP SUPP USB3_5 (XECP_SUPP_USB3_5)	000A4135h
8038h	4	XECP SUPP USB3_6 (XECP_SUPP_USB3_6)	000A0136h
803Ch	4	XECP SUPP USB3_7 (XECP_SUPP_USB3_7)	00140137h
8094h	4	Host Control Scheduler (HOST_CTRL_SCH_REG)	00C08140h
80A4h	4	Power Management Control (PMCTRL_REG)	492D5094h
80B0h	4	Host Controller Misc Reg (HOST_CTRL_MISC_REG)	0080037Fh
80B4h	4	Host Controller Misc Reg2 (HOST_CTRL_MISC_REG2)	10800184h
80B8h	4	Super Speed Port Enable (SSPE_REG)	C0000000h
80E0h	4	AUX Power Management Control (AUX_CTRL_REG1)	8080BCE0h
80ECh	4	SuperSpeed Port Link Control (HOST_CTRL_PORT_LINK_REG)	18020000h
80F0h	4	USB2 Port Link Control 1 (USB2_LINK_MGR_CTRL_REG1)	314803A0h
80F4h	4	USB2 Port Link Control 2 (USB2_LINK_MGR_CTRL_REG2)	80C40620h
80F8h	4	USB2 Port Link Control 3 (USB2_LINK_MGR_CTRL_REG3)	F865EB6Bh
80FCh	4	USB2 Port Link Control 4 (USB2_LINK_MGR_CTRL_REG4)	02008003h
8140h	4	Power Scheduler Control-0 (PWR_SCHED_CTRL0)	0A019132h
8144h	4	Power Scheduler Control-1 (PWR_SCHED_CTRL2)	0000023Fh
8154h	4	AUX Power Management Control (AUX_CTRL_REG2)	81192206h
8164h	4	USB2 PHY Power Management Control (USB2_PHY_PMC)	000000FCh
816Ch	4	XHCI Aux Clock Control Register (XHCI_AUX_CCR)	000F403Ch
8174h	4	XHC Latency Tolerance Parameters LTV Control (XLTP_LTV1)	01400C01h
8178h	4	XHC Latency Tolerance Parameters LTV Control 2 (XLTP_LTV2)	000017FFh
817Ch	4	XHC Latency Tolerance Parameters High Idle Time Control (XLTP_HITC)	00050002h
8180h	4	XHC Latency Tolerance Parameters Medium Idle Time Control (XLTP_MITC)	00050002h
8184h	4	XHC Latency Tolerance Parameters Low Idle Time Control (XLTP_LITC)	00050002h
81B8h	4	LFPS On Count (LFPSONCOUNT_REG)	000420C8h
81C4h	4	USB2 Power Management Control (USB2PMCTRL_REG)	00822908h
846Ch	4	USB Legacy Support Capability (USBLEGSUP)	00002201h
8470h	4	USB Legacy Support Control Status (USBLEGCTLSTS)	00000000h
84F4h	4	Port Disable Override Capability Register (PDO_CAPABILITY)	000003C6h
8604h	2	Command Reg (CMD_MMIO)	0000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8606h	2	Device Status (STS_MMIO)	0290h
8608h	1	Revision ID (RID_MMIO)	00h
8609h	1	Programming Interface (PI_MMIO)	30h
860Ah	1	Sub Class Code (SCC_MMIO)	03h
860Bh	1	Base Class Code (BCC_MMIO)	0Ch
860Ch	1	Cache Line Size (CLS_MMIO)	00h
860Dh	1	Initiator Latency Timer (MLT_MMIO)	00h
860Eh	1	Header Type (HT_MMIO)	80h
8610h	8	Memory Base Address (MBAR_MMIO)	0000000000000004h
862Ch	2	USB Subsystem Vendor ID (SSVID_MMIO)	0000h
862Eh	2	USB Subsystem ID (SSID_MMIO)	0000h
8634h	1	Capabilities Pointer (CAP_PTR_MMIO)	70h
863Ch	1	Interrupt Line (ILINE_MMIO)	00h
863Dh	1	Interrupt Pin (IPIN_MMIO)	00h
8660h	1	Serial Bus Release Number (SBRN_MMIO)	32h
8661h	1	Frame Length Adjustment (FLADJ_MMIO)	60h
8662h	1	Best Effort Service Latency (BESL_MMIO)	00h
8670h	1	PCI Power Management Capability ID (PM_CID_MMIO)	01h
8671h	1	Next Item Pointer 1 (PM_NEXT_MMIO)	80h
8672h	2	Power Management Capabilities (PM_CAP_MMIO)	C1C2h
8674h	2	Power Management Control/Status (PM_CS_MMIO)	0008h
8680h	1	Message Signaled Interrupt CID (MSI_CID_MMIO)	05h
8681h	1	Next Item Pointer (MSI_NEXT_MMIO)	90h
8682h	2	Message Signaled Interrupt Message Control (MSI_MCTL_MMIO)	0086h
8684h	4	Message Signaled Interrupt Message Address (MSI_MAD_MMIO)	00000000h
8688h	4	Message Signaled Interrupt Upper Address (MSI_MUAD_MMIO)	00000000h
868Ch	2	Message Signaled Interrupt Message Data (MSI_MD_MMIO)	0000h
86A4h	4	High Speed Configuration 2 (HSCFG2_MMIO)	00003800h
8700h	4	Debug Capability ID Register (DCID)	0005100Ah
8704h	4	Debug Capability Doorbell Register (DCDB)	00000000h
8708h	4	Debug Capability Event Ring Segment Table Size Register (DCERSTSZ)	00000000h
8710h	8	Debug Capability Event Ring Segment Table Base Address Register (DCERSTBA)	0000000000000000h
8718h	8	Debug Capability Event Ring Dequeue Pointer Register (DCERDP)	0000000000000000h
8720h	4	Debug Capability Control Register (DCCTRL)	00000000h
8724h	4	Debug Capability Status Register (DCST)	00000000h
8728h	4	Debug Capability Port Status And Control Register (DCPORTSC)	00000080h
8730h	8	Debug Capability Context Pointer Register (DCCP)	0000000000000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8800h	4	Fuse and Strap Mirror Capability Register (FUSE_AND_STRAP_MIRROR_CAP_REG)	000040D1h
8E10h	4	GLOBAL TIME SYNC CAP REG (GLOBAL_TIME_SYNC_CAP_REG)	000012C9h
8E14h	4	GLOBAL TIME SYNC CTRL REG (GLOBAL_TIME_SYNC_CTRL_REG)	00000000h
8E18h	4	MICROFRAME TIME REG (MICROFRAME_TIME_REG)	00000000h
8E20h	4	Global Time Value (Low Register) (GLOBAL_TIME_LOW_REG)	00000000h
8E24h	4	GLOBAL TIME HI REG (GLOBAL_TIME_HI_REG)	00000000h
8E60h	4	Dublin HOST_CTRL_USB3_LOCAL_LPBK_RPTR (HOST_CTRL_USB3_LOCAL_LPBK_RPTR)	00000000h
8EC8h	4	Host Ctrl Usb3 Initiator Loopback Register (HOST_CTRL_USB3_MSTR_LPBK)	00000000h
8ECCh	4	Host Ctrl Usb3 Blr Comp Register (HOST_CTRL_USB3_BLR_COMP)	00000000h
8ED0h	4	Host Ctrl Ssp Dis Register (HOST_CTRL_SSP_DIS)	00000000h
90A4h	4	XHCI USB2 Overcurrent Pin Mapping (U2OCM1)	00000000h
90A8h	4	XHCI USB2 Overcurrent Pin Mapping (U2OCM2)	00000000h
90ACh	4	XHCI USB2 Overcurrent Pin Mapping (U2OCM3)	00000000h
90B0h	4	XHCI USB2 Overcurrent Pin Mapping (U2OCM4)	00000000h
9124h	4	XHCI USB3 Overcurrent Pin Mapping (U3OCM1)	00000000h
9128h	4	XHCI USB3 Overcurrent Pin Mapping (U3OCM2)	00000000h
912Ch	4	XHCI USB3 Overcurrent Pin Mapping (U3OCM3)	00000000h
9130h	4	XHCI USB3 Overcurrent Pin Mapping (U3OCM4)	00000000h

10.2.2 Capability Registers Length (CAPLENGTH) — Offset 0h

This register is modified and maintained by BIOS

Type	Size	Offset	Default
MMIO	8 bit	MBAR + 0h	80h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	80h RW/L	**Capability Registers Length (CAPLENGTH):** Capability Registers Length (CAPLENGTH) **Locked by:** XHCC1.ACCTRL

10.2.3 Host Controller Interface Version Number (HCIVERSION) — Offset 2h

This register is modified and maintained by BIOS

Type	Size	Offset	Default
MMIO	16 bit	MBAR + 2h	0110h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0110h RW/L	**Host Controller Interface Version Number (HCIVERSION):** Host Controller Interface Version Number (HCIVERSION) **Locked by:** XHCC1.ACCTRL

10.2.4 Structural Parameters 1 (HCSPARAMS1) — Offset 4h

This register is modified and maintained by BIOS

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 4h	05000840h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	05h RW/L	**Number of Ports (MAXPORTS):** Number of Ports (MaxPorts): The value in this field reflects the highest numbered port in the controller, not the actual count of the number of ports. This allows for gaps in the port numbering, between USB2 and USB3 protocol capabilities. **Locked by:** XHCC1.ACCTRL
23:19	0h RO	**Reserved**
18:8	008h RW/L	**Number of Interrupters (MAXINTRS):** Number of Interrupters (MaxInt) **Locked by:** XHCC1.ACCTRL
7:0	40h RW/L	**Number of Device Slots (MAXSLOTS):** Number of Device Slots (MaxSlots) **Locked by:** XHCC1.ACCTRL

10.2.5 Structural Parameters 2 (HCSPARAMS2) — Offset 8h

This register is modified and maintained by BIOS

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8h	14200054h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	02h RW/L	**Max Scratchpad Buffers LO (MAXSCRATCHPADBUFS):** Max Scratchpad Buffers Lo (MaxScratchpadBufs) **Locked by:** XHCC1.ACCTRL
26	1h RW/L	**Scratchpad Restore (SPR):** Scratchpad Restore (SPR) **Locked by:** XHCC1.ACCTRL
25:21	01h RW/L	**Max Scratchpad Buffers HI (MAXSCRATCHPADBUFS_HI):** Max Scratchpad Buffers Hi (MaxScratchpadBufs) **Locked by:** XHCC1.ACCTRL
20:8	0h RO	**Reserved**
7:4	5h RW/L	**Event Ring Segment Table Max (ERSTMAX):** Event Ring Segment Table Max (ERSTMax) **Locked by:** XHCC1.ACCTRL
3:0	4h RW/L	**Isochronous Scheduling Threshold (IST):** Isochronous Scheduling Threshold (IST) **Locked by:** XHCC1.ACCTRL

10.2.6 Structural Parameters 3 (HCSPARAMS3) — Offset Ch

This register is modified and maintained by BIOS

Type	Size	Offset	Default
MMIO	32 bit	MBAR + Ch	00A0000Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	00A0h RW/L	**U2 Device Exit Latency (U2DEL):** U2 Device Exit Latency (U2DEL): **Locked by:** XHCC1.ACCTRL

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7:0	0Ah RW/L	**U1 Device Exit Latency (U1DEL):** U1 Device Exit Latency (U1DEL): **Locked by:** XHCC1.ACCTRL

10.2.7 Capability Parameters (HCCPARAMS) — Offset 10h

This register is modified and maintained by BIOS

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 10h	20007FC1h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	2000h RW/L	**xHCI Extended Capabilities Pointer (XECP):** xHCI Extended Capabilities Pointer (xECP): The Default value should be 2008h if NumUSB2 = 0 **Locked by:** XHCC1.ACCTRL
15:12	7h RW/L	**Maximum Primary Stream Array Size (MAXPSASIZE):** Maximum Primary Stream Array Size (MaxPSASize): **Locked by:** XHCC1.ACCTRL
11	1h RW/L	**Contiguous Frame ID Capability (CFC):** Contiguous Frame ID Capability (CFC) **Locked by:** XHCC1.ACCTRL
10	1h RW/L	**Stopped EDLTA Capabilty (SEC):** Stopped EDLTA Capabilty (SEC) **Locked by:** XHCC1.ACCTRL
9	1h RW/L	**Stopped - Short Packet Capability (SPC):** Stopped - Short Packet Capability (SPC) **Locked by:** XHCC1.ACCTRL
8	1h RW/L	**Parst All Event Data (PAE):** Parse All Event Data (PAE) **Locked by:** XHCC1.ACCTRL
7	1h RW/L	**No Secondary SID Support (NSS):** No Secondary SID Support (NSS) **Locked by:** XHCC1.ACCTRL
6	1h RW/L	**Latency Tolerance Messaging Capability (LTC):** Latency Tolerance Messaging Capability (LTC): **Locked by:** XHCC1.ACCTRL
5	0h RW/L	**Light HC Reset Capability (LHRC):** Light HC Reset Capability (LHRC) **Locked by:** XHCC1.ACCTRL

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/L	**Port Indicators (PIND):** Port Indicators (PIND): **Locked by:** XHCC1.ACCTRL
3	0h RW/L	**Port Power Control (PPC):** Port Power Control (PPC): **Locked by:** XHCC1.ACCTRL
2	0h RW/L	**Context Size (CSZ):** Context Size (CSZ): **Locked by:** XHCC1.ACCTRL
1	0h RW/L	**BW Negotiation Capability (BNC):** BW Negotiation Capability (BNC): **Locked by:** XHCC1.ACCTRL
0	1h RW/L	**64-bit Addressing Capability (AC64):** 64-bit Addressing Capability (AC64) **Locked by:** XHCC1.ACCTRL

10.2.8 Doorbell Offset (DBOFF) — Offset 14h

Doorbell Offset

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 14h	00003000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000C00h RO	**Doorbell Array Offset (DBAO):** Doorbell Array Offset (DBAO)
1:0	0h RO	**Reserved**

10.2.9 Runtime Register Space Offset (RTSOFF) — Offset 18h

Runtime Register Space Offset

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 18h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:5	0000100h RO	**Runtime Register Space Offset (RTRSO):** Runtime Register Space Offset (RTRSO):
4:0	0h RO	**Reserved**

10.2.10 USB Command (USBCMD) — Offset 80h

USB Command

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 80h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14	0h RW	**Extended TCB Enable (ETE):** This flag indicates that the host controller implementation is enabled to support Transfer Burst Count values greater than 4 in Isoch TDs. This bit may be set only if ETC = 1.
13	0h RW	**CEM Enable (CEM):** Default = '0'. when set to '1', a Max Exit Latency Too Large Capability Error may be returned by a Configure Endpoint Command. When Cleared to '0', a Max Exit latency Too Large Capability Error shall not be returned by a Configure Endpoint Command. This bit is Reserved if CMC='0'.
12	0h RO	**Reserved**
11	0h RW	**Enable U3 MFINDEX Stop (EU3S):** Enable U3 MFINDEX Stop

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**Enable Wrap Event (EWE):** Enable Wrap Event
9	0h RW	**Controller Restore State (CRS):** Controller Restore State
8	0h RW	**Controller Save State (CSS):** Controller Save State
7	0h RW	**Light Host Controller Reset (LHCRST):** Light Host Controller Reset
6:4	0h RO	**Reserved**
3	0h RW	**Host System Error Enable (HSEE):** Host System Error Enable
2	0h RW	**Interrupter Enable (INTE):** Interrupter Enable
1	0h RW	**Host Controller Reset (HCRST):** Host Controller Reset
0	0h RW	**Run/Stop Host Controller (RS):** Run/Stop

10.2.11 USB Status (USBSTS) — Offset 84h

USB Status

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 84h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RO	**Host Controller Error (HCE):** This bit is not preset in HC, this is deviation from XHCI 1.0 spec.
11	0h RO	**Controller Not Ready (CNR):** This is deviation from XHCI 1.0 spec.
10	0h RW/1C	**Save/Restore Error (SRE):** Save/Restore Error
9	0h RO	**Restore State Status (RSS):** Restore State Status
8	0h RO	**Save State Status (SSS):** Save State Status
7:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/1C	**Port Change Detect (PCD):** Port Change Detect
3	0h RW/1C	**Event Interrupt (EINT):** Event Interrupt
2	0h RW/1C	**Host System Error (HSE):** Host System Error
1	0h RO	**Reserved**
0	1h RO	**Host Controller Halted (HCH):** HCHalted

10.2.12 Page Size (PAGESIZE) — Offset 88h

Page Size

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 88h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0001h RO	**Page Size (PAGESIZE):** Page Size

10.2.13 Device Notification Control (DNCTRL) — Offset 94h

Device Notification Control

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 94h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**Notification Enable (N0_N15):** Notification Enable

10.2.14 Command Ring Low (CRCR_LO) — Offset 98h

Command Ring Low

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 98h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h WO	**Command Ring Pointer (CRP):** Command Ring Pointer
5:4	0h RO	**Reserved**
3	0h RO	**Command Ring Running (CRR):** Command Ring Running
2	0h WO	**Command Abort (CA):** Command Abort
1	0h WO	**Command Stop (CS):** Command Stop
0	0h WO	**Ring Cycle State (RCS):** Ring Cycle State

10.2.15 Command Ring High (CRCR_HI) — Offset 9Ch

Command Ring High

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 9Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WO	**Command Ring Pointer (CRP):** Command Ring Pointer

10.2.16 Device Context Base Address Array Pointer Low (DCBAAP_LO) — Offset B0h

Device Context Base Address Array Pointer Low

Type	Size	Offset	Default
MMIO	32 bit	MBAR + B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h RW	**Device Context Base Address Array Pointer (DCBAAP):** Device Context Base Address Array Pointer
5:0	0h RO	**Reserved**

10.2.17 Device Context Base Address Array Pointer High (DCBAAP_HI) — Offset B4h

Device Context Base Address Array Pointer High

Type	Size	Offset	Default
MMIO	32 bit	MBAR + B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Device Context Base Address Array Pointer (DCBAAP):** Device Context Base Address Array Pointer High

10.2.18 Configure Reg (CONFIG) — Offset B8h

Configure Reg

Type	Size	Offset	Default
MMIO	32 bit	MBAR + B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9	0h RW	**Configuration Information Enable (CIE):** Configuration Information Enable
8	0h RW	**U3 Entry Enable (U3E):** U3 Entry Enable
7:0	00h RW	**Max Device Slots Enabled (MAXSLOTSEN):** Max Device Slots Enabled

10.2.19 Port Status AndControl USB2 (PORTSC1) — Offset 480h

There are NumUSB2 USB2 PORTSC registers at offsets :

480h, 490h, ... (480h + (NumUSB2-1)*10h)

The USB PORTSC registers should be accessed via DW writes for any modification.

Byte Writes have unintended behavior.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 480h	000002A0h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S	**Warm Port Reset (WPR):** Warm Port Reset
30	0h RW/L	**Device Removable (DR):** Device Removable **Locked by:** XHCC1.ACCTRL
29:28	0h RO	**Reserved**
27	0h RW/P	**Wake on Over-current Enable (WOE):** Note: This register is sticky.
26	0h RW/P	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0h RW/P	**Wake on Connect Enable (WCE):** Note: This register is sticky.
24	0h RO	**Cold Attach Status (CAS):** Cold Attach Status
23	0h RW/1C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0h RW/1C	**Port Link State Change (PLC):** Note: This register is sticky.
21	0h RW/1C	**Port Reset Change (PRC):** Note: This register is sticky.
20	0h RW/1C	**Over-current Change (OCC):** Note: This register is sticky.
19	0h RW/1C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0h RW/1C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.
17	0h RW/1C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0h RW	**Port Link State Write Strobe (LWS):** Port Link State Write Strobe

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RW/P	**Port Indicator Control (PIC):** Note: This register is sticky.
13:10	0h RO	**Port Speed (PORTSPEED):** Note: This register is sticky.
9	1h RW/P	**Port Power (PP):** Note: This register is sticky.
8:5	5h RW/P	**Port Link State (PLS):** Note: This register is sticky.
4	0h RW/1S	**Port Reset (PR):** Port Reset
3	0h RO	**Over-current Active (OCA):** Note: This register is sticky.
2	0h RO	**Reserved**
1	0h RW/1C	**Port Enabled Disabled (PED):** Note: This register is sticky.
0	0h RO	**Current Connect Status (CCS):** Note: This register is sticky.

10.2.20 Port Power Management Status Aand Control USB2 (PORTPMSC1) — Offset 484h

There are 6 USB2 PORTPMSC registers at offsets:

484h, 494h, ... (484h + (NumUSB2-1)*10h)

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 484h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW/P	**Port Test Control (PTC):** Note: This register is sticky.
27:17	0h RO	**Reserved**
16	0h RW	**Hardware LPM Enable (HLE):** Hardware LPM Enable
15:8	00h RW/P	**Device Address (DA):** Note: This register is sticky.
7:4	0h RW/P	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/P	**Remote Wake Enable (RWE):** Note: This register is sticky.
2:0	0h RW	**L1 Status (L1S):** Note: This register is sticky.

10.2.21 Port X Hardware LPM Control Register (PORTHLPMC1) — Offset 48Ch

There are 9 PORTHLPMC registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch

This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST).

The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 48Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value.
9:2	00h RW/P	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky.

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW/P	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky.

10.2.22 Port Status And Control USB3 (PORTSC2) — Offset 490h

The USB3 PORTSC registers are at offsets:

First USB3 port: 480h+NumUSB2*10h

Next USB3 port : First USB3 Port + 10h

and so on...

Final USB3 Port : First USB3 Port + (NumUSB3-1)*10h)

The USB PORTSC registers should be accessed via DW writes for any modification.

Byte Writes have unintended behavior.

Note: **NOTE:** Bit definitions are the same as PORTSC1, offset 480h.

10.2.23 Port Power Management Status And Control USB3 (PORTPMSC2) — Offset 494h

Port Power Management Status And Control USB3

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 494h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW	**Force Link PM Accept (FLA):** Force Link PM Accept
15:8	00h RW/P	**U2 Timeout (U2T):** U2 Timeout
7:0	00h RW/P	**U1 Timeout (U1T):** U1 Timeout

10.2.24 USB3 Port Link Info (PORTLI2) — Offset 498h

The USB3 PORTLI registers are at offsets:

First USB3 port: 488h+NumUSB2*10h

Next USB3 port : First USB3 Port + 10h

and so on...

Final USB3 Port : First USB3 Port + (NumUSB3-1)*10h)

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 498h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RO/V	**Tx Lane Count (TLC):** Tx Lane Count
19:16	0h RO/V	**Rx Lane Count (RLC):** Rx Lane Count
15:0	0000h RW	**Link Error Count (LEC):** Link Error Count

10.2.25 Port Status And Control USB3 (PORTSC3) — Offset 4A0h

The USB3 PORTSC registers are at offsets:

First USB3 port: 480h+NumUSB2*10h

Next USB3 port : First USB3 Port + 10h

and so on...

Final USB3 Port : First USB3 Port + (NumUSB3-1)*10h)

The USB PORTSC registers should be accessed via DW writes for any modification.

Byte Writes have unintended behavior.

Note: **NOTE:** Bit definitions are the same as PORTSC1, offset 480h.

10.2.26 Port Power Management Status And Control USB3 (PORTPMSC3) — Offset 4A4h

Port Power Management Status And Control USB3

Note: **NOTE:** Bit definitions are the same as PORTPMSC2, offset 494h.

10.2.27 USB3 Port Link Info (PORTLI3) — Offset 4A8h

The USB3 PORTLI registers are at offsets:

First USB3 port: 488h+NumUSB2*10h

Next USB3 port : First USB3 Port + 10h

and so on...

Final USB3 Port : First USB3 Port + (NumUSB3-1)*10h)

Note: **NOTE:** Bit definitions are the same as PORTLI2, offset 498h.

10.2.28 Port Status And Control USB3 (PORTSC4) — Offset 4B0h

The USB3 PORTSC registers are at offsets:

First USB3 port: 480h+NumUSB2*10h

Next USB3 port : First USB3 Port + 10h

and so on...

Final USB3 Port : First USB3 Port + (NumUSB3-1)*10h)

The USB PORTSC registers should be accessed via DW writes for any modification.

Byte Writes have unintended behavior.

Note: **NOTE:** Bit definitions are the same as PORTSC1, offset 480h.

10.2.29 Port Power Management Status And Control USB3 (PORTPMSC4) — Offset 4B4h

Port Power Management Status And Control USB3

Note: **NOTE:** Bit definitions are the same as PORTPMSC2, offset 494h.

10.2.30 USB3 Port Link Info (PORTLI4) — Offset 4B8h

The USB3 PORTLI registers are at offsets:

First USB3 port: 488h+NumUSB2*10h

Next USB3 port : First USB3 Port + 10h

and so on...

Final USB3 Port : First USB3 Port + (NumUSB3-1)*10h)

Note: **NOTE:** Bit definitions are the same as PORTLI2, offset 498h.

10.2.31 Port Status And Control USB3 (PORTSC5) — Offset 4C0h

The USB3 PORTSC registers are at offsets:

First USB3 port: 480h+NumUSB2*10h

Next USB3 port : First USB3 Port + 10h

and so on...

Final USB3 Port : First USB3 Port + (NumUSB3-1)*10h)

The USB PORTSC registers should be accessed via DW writes for any modification.

Byte Writes have unintended behavior.

Note: **NOTE:** Bit definitions are the same as PORTSC1, offset 480h.

10.2.32 Port Power Management Status And Control USB3 (PORTPMSC5) — Offset 4C4h

Port Power Management Status And Control USB3

Note: **NOTE:** Bit definitions are the same as PORTPMSC2, offset 494h.

10.2.33 USB3 Port Link Info (PORTLI5) — Offset 4C8h

The USB3 PORTLI registers are at offsets:

First USB3 port: 488h+NumUSB2*10h

Next USB3 port : First USB3 Port + 10h

and so on...

Final USB3 Port : First USB3 Port + (NumUSB3-1)*10h)

Note: **NOTE:** Bit definitions are the same as PORTLI2, offset 498h.

10.2.34 Microframe Index (RTMFINDEX) — Offset 2000h

Microframe Index

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:0	0000h RO	**Microframe Index (IMAN0):** Microframe Index

10.2.35 Interrupter Management (IMAN0) — Offset 2020h

There are 8 IMAN registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**Interrupt Enable (IE):** Interrupt Enable
0	0h RW/1C	**Interrupt Pending (IP):** Interrupt Pending

10.2.36 Interrupter Moderation (IMOD0) — Offset 2024h

There are 8 IMOD registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2024h	00000FA0h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Interrupt Moderation Counter (IMODC):** Interrupt Moderation Counter
15:0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Interrupt Moderation Interval

10.2.37 Event Ring Segment Table Size (ERSTSZ0) — Offset 2028h

There are 8 ERSTSZ register.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2028h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Event Ring Segment Table Size (ERSTS):** Event Ring Segment Table Size

10.2.38 Event Ring Segment Table Base Address Low (ERSTBA_LO0) — Offset 2030h

There are 8 ERSTBA_LO registers

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2030h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Event Ring Segment Table Base Address Register
5:0	0h RO	**Reserved**

10.2.39 Event Ring Segment Table Base Address High (ERSTBA_HI0) — Offset 2034h

Event Ring Segment Table Base Address High

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2034h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA):** Event Ring Segment Table Base Address

10.2.40 Event Ring Dequeue Pointer Low (ERDP_LO0) — Offset 2038h

There are 8 ERDP_LO registers.

x = 1, 2, ...,8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 2038h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** Event Ring Dequeue Pointer
3	0h RW/1C	**Event Handler Busy (EHB):** Event Handler Busy
2:0	0h RW	**Dequeue ERST Segment Index (DESI):** Dequeue ERST Segment Index

10.2.41 Event Ring Dequeue Pointer High (ERDP_HI0) — Offset 203Ch

There are 8 ERDP_HI registers.

x = 1, 2, ..., 8

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 203Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** Event Ring Dequeue Pointer

10.2.42 Interrupter Management (IMAN1) — Offset 2040h

There are 8 IMAN registers.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as IMAN0, offset 2020h.

10.2.43 Interrupter Moderation (IMOD1) — Offset 2044h

There are 8 IMOD registers.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as IMOD0, offset 2024h.

10.2.44 Event Ring Segment Table Size (ERSTSZ1) — Offset 2048h

There are 8 ERSTSZ register.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as ERSTSZ0, offset 2028h.

10.2.45 Event Ring Segment Table Base Address Low (ERSTBA_LO1) — Offset 2050h

There are 8 ERSTBA_LO registers

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as ERSTBA_LO0, offset 2030h.

10.2.46 Event Ring Segment Table Base Address High (ERSTBA_HI1) — Offset 2054h

Event Ring Segment Table Base Address High

Note: **NOTE:** Bit definitions are the same as ERSTBA_HI0, offset 2034h.

10.2.47 Event Ring Dequeue Pointer Low (ERDP_LO1) — Offset 2058h

There are 8 ERDP_LO registers.

x = 1, 2, ...,8

Note: **NOTE:** Bit definitions are the same as ERDP_LO0, offset 2038h.

10.2.48 Event Ring Dequeue Pointer High (ERDP_HI1) — Offset 205Ch

There are 8 ERDP_HI registers.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as ERDP_HI0, offset 203Ch.

10.2.49 Interrupter Management (IMAN2) — Offset 2060h

There are 8 IMAN registers.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as IMAN0, offset 2020h.

10.2.50 Interrupter Moderation (IMOD2) — Offset 2064h

There are 8 IMOD registers.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as IMOD0, offset 2024h.

10.2.51 Event Ring Segment Table Size (ERSTSZ2) — Offset 2068h

There are 8 ERSTSZ register.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as ERSTSZ0, offset 2028h.

10.2.52 Event Ring Segment Table Base Address Low (ERSTBA_LO2) — Offset 2070h

There are 8 ERSTBA_LO registers

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as ERSTBA_LO0, offset 2030h.

10.2.53 Event Ring Segment Table Base Address High (ERSTBA_HI2) — Offset 2074h

Event Ring Segment Table Base Address High

Note: **NOTE:** Bit definitions are the same as ERSTBA_HI0, offset 2034h.

10.2.54 Event Ring Dequeue Pointer Low (ERDP_LO2) — Offset 2078h

There are 8 ERDP_LO registers.

x = 1, 2, ...,8

Note: **NOTE:** Bit definitions are the same as ERDP_LO0, offset 2038h.

10.2.55 Event Ring Dequeue Pointer High (ERDP_HI2) — Offset 207Ch

There are 8 ERDP_HI registers.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as ERDP_HI0, offset 203Ch.

10.2.56 Interrupter Management (IMAN3) — Offset 2080h

There are 8 IMAN registers.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as IMAN0, offset 2020h.

10.2.57 Interrupter Moderation (IMOD3) — Offset 2084h

There are 8 IMOD registers.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as IMOD0, offset 2024h.

10.2.58 Event Ring Segment Table Size (ERSTSZ3) — Offset 2088h

There are 8 ERSTSZ register.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as ERSTSZ0, offset 2028h.

10.2.59 Event Ring Segment Table Base Address Low (ERSTBA_LO3) — Offset 2090h

There are 8 ERSTBA_LO registers

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as ERSTBA_LO0, offset 2030h.

10.2.60 Event Ring Segment Table Base Address High (ERSTBA_HI3) — Offset 2094h

Event Ring Segment Table Base Address High

Note: **NOTE:** Bit definitions are the same as ERSTBA_HI0, offset 2034h.

10.2.61 Event Ring Dequeue Pointer Low (ERDP_LO3) — Offset 2098h

There are 8 ERDP_LO registers.

x = 1, 2, ...,8

Note: **NOTE:** Bit definitions are the same as ERDP_LO0, offset 2038h.

10.2.62 Event Ring Dequeue Pointer High (ERDP_HI3) — Offset 209Ch

There are 8 ERDP_HI registers.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as ERDP_HI0, offset 203Ch.

10.2.63 Interrupter Management (IMAN4) — Offset 20A0h

There are 8 IMAN registers.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as IMAN0, offset 2020h.

10.2.64 Interrupter Moderation (IMOD4) — Offset 20A4h

There are 8 IMOD registers.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as IMOD0, offset 2024h.

10.2.65 Event Ring Segment Table Size (ERSTSZ4) — Offset 20A8h

There are 8 ERSTSZ register.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as ERSTSZ0, offset 2028h.

10.2.66 Event Ring Segment Table Base Address Low (ERSTBA_LO4) — Offset 20B0h

There are 8 ERSTBA_LO registers

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as ERSTBA_LO0, offset 2030h.

10.2.67 Event Ring Segment Table Base Address High (ERSTBA_HI4) — Offset 20B4h

Event Ring Segment Table Base Address High

Note: **NOTE:** Bit definitions are the same as ERSTBA_HI0, offset 2034h.

10.2.68 Event Ring Dequeue Pointer Low (ERDP_LO4) — Offset 20B8h

There are 8 ERDP_LO registers.

x = 1, 2, ...,8

Note: **NOTE:** Bit definitions are the same as ERDP_LO0, offset 2038h.

10.2.69 Event Ring Dequeue Pointer High (ERDP_HI4) — Offset 20BCh

There are 8 ERDP_HI registers.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as ERDP_HI0, offset 203Ch.

10.2.70 Interrupter Management (IMAN5) — Offset 20C0h

There are 8 IMAN registers.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as IMAN0, offset 2020h.

10.2.71 Interrupter Moderation (IMOD5) — Offset 20C4h

There are 8 IMOD registers.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as IMOD0, offset 2024h.

10.2.72 Event Ring Segment Table Size (ERSTSZ5) — Offset 20C8h

There are 8 ERSTSZ register.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as ERSTSZ0, offset 2028h.

10.2.73 Event Ring Segment Table Base Address Low (ERSTBA_LO5) — Offset 20D0h

There are 8 ERSTBA_LO registers

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as ERSTBA_LO0, offset 2030h.

10.2.74 Event Ring Segment Table Base Address High (ERSTBA_HI5) — Offset 20D4h

Event Ring Segment Table Base Address High

Note: **NOTE:** Bit definitions are the same as ERSTBA_HI0, offset 2034h.

10.2.75 Event Ring Dequeue Pointer Low (ERDP_LO5) — Offset 20D8h

There are 8 ERDP_LO registers.

x = 1, 2, ...,8

Note: **NOTE:** Bit definitions are the same as ERDP_LO0, offset 2038h.

10.2.76 Event Ring Dequeue Pointer High (ERDP_HI5) — Offset 20DCh

There are 8 ERDP_HI registers.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as ERDP_HI0, offset 203Ch.

10.2.77 Interrupter Management (IMAN6) — Offset 20E0h

There are 8 IMAN registers.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as IMAN0, offset 2020h.

10.2.78 Interrupter Moderation (IMOD6) — Offset 20E4h

There are 8 IMOD registers.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as IMOD0, offset 2024h.

10.2.79 Event Ring Segment Table Size (ERSTSZ6) — Offset 20E8h

There are 8 ERSTSZ register.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as ERSTSZ0, offset 2028h.

10.2.80 Event Ring Segment Table Base Address Low (ERSTBA_LO6) — Offset 20F0h

There are 8 ERSTBA_LO registers

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as ERSTBA_LO0, offset 2030h.

10.2.81 Event Ring Segment Table Base Address High (ERSTBA_HI6) — Offset 20F4h

Event Ring Segment Table Base Address High

Note: **NOTE:** Bit definitions are the same as ERSTBA_HI0, offset 2034h.

10.2.82 Event Ring Dequeue Pointer Low (ERDP_LO6) — Offset 20F8h

There are 8 ERDP_LO registers.

x = 1, 2, ...,8

Note: **NOTE:** Bit definitions are the same as ERDP_LO0, offset 2038h.

10.2.83 Event Ring Dequeue Pointer High (ERDP_HI6) — Offset 20FCh

There are 8 ERDP_HI registers.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as ERDP_HI0, offset 203Ch.

10.2.84 Interrupter Management (IMAN7) — Offset 2100h

There are 8 IMAN registers.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as IMAN0, offset 2020h.

10.2.85 Interrupter Moderation (IMOD7) — Offset 2104h

There are 8 IMOD registers.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as IMOD0, offset 2024h.

10.2.86 Event Ring Segment Table Size (ERSTSZ7) — Offset 2108h

There are 8 ERSTSZ register.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as ERSTSZ0, offset 2028h.

10.2.87 Event Ring Segment Table Base Address Low (ERSTBA_LO7) — Offset 2110h

There are 8 ERSTBA_LO registers

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as ERSTBA_LO0, offset 2030h.

10.2.88 Event Ring Segment Table Base Address High (ERSTBA_HI7) — Offset 2114h

Event Ring Segment Table Base Address High

Note: **NOTE:** Bit definitions are the same as ERSTBA_HI0, offset 2034h.

10.2.89 Event Ring Dequeue Pointer Low (ERDP_LO7) — Offset 2118h

There are 8 ERDP_LO registers.

x = 1, 2, ...,8

Note: **NOTE:** Bit definitions are the same as ERDP_LO0, offset 2038h.

10.2.90 Event Ring Dequeue Pointer High (ERDP_HI7) — Offset 211Ch

There are 8 ERDP_HI registers.

x = 1, 2, ..., 8

Note: **NOTE:** Bit definitions are the same as ERDP_HI0, offset 203Ch.

10.2.91 Door Bell (DB0) — Offset 3000h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 3000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	**Reserved**
7:0	00h RW	**DB Target (DT):** DB Target

10.2.92 Door Bell (DB1) — Offset 3004h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.93 Door Bell (DB2) — Offset 3008h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.94 Door Bell (DB3) — Offset 300Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.95 Door Bell (DB4) — Offset 3010h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.96 Door Bell (DB5) — Offset 3014h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.97 Door Bell (DB6) — Offset 3018h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.98 Door Bell (DB7) — Offset 301Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.99 Door Bell (DB8) — Offset 3020h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.100 Door Bell (DB9) — Offset 3024h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.101 Door Bell (DB10) — Offset 3028h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.102 Door Bell (DB11) — Offset 302Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.103 Door Bell (DB12) — Offset 3030h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.104 Door Bell (DB13) — Offset 3034h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.105 Door Bell (DB14) — Offset 3038h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.106 Door Bell (DB15) — Offset 303Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.107 Door Bell (DB16) — Offset 3040h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.108 Door Bell (DB17) — Offset 3044h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.109 Door Bell (DB18) — Offset 3048h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.110 Door Bell (DB19) — Offset 304Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.111 Door Bell (DB20) — Offset 3050h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.112 Door Bell (DB21) — Offset 3054h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.113 Door Bell (DB22) — Offset 3058h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.114 Door Bell (DB23) — Offset 305Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.115 Door Bell (DB24) — Offset 3060h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.116 Door Bell (DB25) — Offset 3064h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.117 Door Bell (DB26) — Offset 3068h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.118 Door Bell (DB27) — Offset 306Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.119 Door Bell (DB28) — Offset 3070h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.120 Door Bell (DB29) — Offset 3074h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.121 Door Bell (DB30) — Offset 3078h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.122 Door Bell (DB31) — Offset 307Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.123 Door Bell (DB32) — Offset 3080h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.124 Door Bell (DB33) — Offset 3084h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.125 Door Bell (DB34) — Offset 3088h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.126 Door Bell (DB35) — Offset 308Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.127 Door Bell (DB36) — Offset 3090h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.128 Door Bell (DB37) — Offset 3094h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.129 Door Bell (DB38) — Offset 3098h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.130 Door Bell (DB39) — Offset 309Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.131 Door Bell (DB40) — Offset 30A0h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.132 Door Bell (DB41) — Offset 30A4h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.133 Door Bell (DB42) — Offset 30A8h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.134 Door Bell (DB43) — Offset 30ACh

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.135 Door Bell (DB44) — Offset 30B0h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.136 Door Bell (DB45) — Offset 30B4h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.137 Door Bell (DB46) — Offset 30B8h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.138 Door Bell (DB47) — Offset 30BCh

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.139 Door Bell (DB48) — Offset 30C0h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.140 Door Bell (DB49) — Offset 30C4h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.141 Door Bell (DB50) — Offset 30C8h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.142 Door Bell (DB51) — Offset 30CCh

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.143 Door Bell (DB52) — Offset 30D0h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.144 Door Bell (DB53) — Offset 30D4h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.145 Door Bell (DB54) — Offset 30D8h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.146 Door Bell (DB55) — Offset 30DCh

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.147 Door Bell (DB56) — Offset 30E0h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.148 Door Bell (DB57) — Offset 30E4h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.149 Door Bell (DB58) — Offset 30E8h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.150 Door Bell (DB59) — Offset 30ECh

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.151 Door Bell (DB60) — Offset 30F0h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.152 Door Bell (DB61) — Offset 30F4h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.153 Door Bell (DB62) — Offset 30F8h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.154 Door Bell (DB63) — Offset 30FCh

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.155 Door Bell (DB64) — Offset 3100h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Note: **NOTE:** Bit definitions are the same as DB0, offset 3000h.

10.2.156 XECP SUPP USB2_0 (XECP_SUPP_USB2_0) — Offset 8000h

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8000h	02000802h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	02h RO	**USB Major Revision: 2.0 (USB2_MAJ_REV):** USB Major Revision: 2.0
23:16	00h RO	**USB Minor Revision (USB_MIN_REV):** USB Minor Revision

Bit Range	Default & Access	Field Name (ID): Description
15:8	08h RO	**Next Capability Pointer (NCP):** Next Capability Pointer.
7:0	02h RO	**Supported Protocol ID (SPID):** Supported Protocol ID

10.2.157 XECP SUPP USB2_1 (XECP_SUPP_USB2_1) — Offset 8004h

XECP SUPP USB2_1

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8004h	20425355h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	20425355h RO	**XECP SUPP USB2 1 (XECP_SUPP_USB2_1):** Namestring USB

10.2.158 XECP SUPP USB2_2 (XECP_SUPP_USB2_2) — Offset 8008h

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8008h	30180101h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	3h RO	**Protocol Speed ID Count (PROT_SPD_ID_CNT):** 3 USB 2.0 Speed (High, Full, Low)
27:21	0h RO	**Reserved**
20	1h RW/L	**BESL LPM Capability (BLC):** Bit is set to 1 to indicate that the the ports described by this xHCI Supported Protocol Capability will apply BESL timing to BESL and BESLD fields of the PORTPMSC and PORTHLPMCC registers. **Locked by:** XHCC1.ACCTRL

Bit Range	Default & Access	Field Name (ID): Description
19	1h RW/L	**Protocol Defined - Hardware LMP Capability (HLC):** This field can be modified and maintained by BIOS under Access Control **Locked by:** XHCC1.ACCTRL
18	0h RO	**Protocol Defined - Integrated Hub Implementation (IHI):** Protocol Defined - Integrated Hub Implementation
17	0h RO	**Protocol Defined - High SPeed Only (HSO):** Protocol Defined - High SPeed Only
16	0h RO	**Reserved**
15:8	01h RO	**Compatible Port Count (CPC):** This field can be modified and maintained by BIOS under Access Control
7:0	01h RO	**Compatible Port Offset (CPO):** Compatible Port Offset

10.2.159 XECP SUPP USB3_3 (XECP_SUPP_USB2_3) — Offset 800Ch

XECP SUPP USB3_3

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 800Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RO	**XECP SUPP USB3 3 (PROTOCOL_SLOT_TYPE):** Protocol Slot Type

10.2.160 XECP SUPP USB2_4 Full Speed (XECP_SUPP_USB2_4) — Offset 8010h

XECP SUPP USB2_4 Full Speed

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8010h	000C0021h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	000Ch RO	**Protocol Speed ID Mantissa (PSIM):** Protocol Speed ID Mantissa
15:9	0h RO	**Reserved**
8	0h RO	**PSI Full Duplex (PFD):** PSI Full Duplex
7:6	0h RO	**PSI Type (PLT):** PSI Type
5:4	2h RO	**Protocol Speed ID Exponent (PSIE):** Protocol Speed ID Exponent
3:0	1h RO	**Protocol Speed ID Value (PSIV):** Protocol Speed ID Value

10.2.161 XECP_SUPP USB2_5 Low Speed (XECP_SUPP_USB2_5) — Offset 8014h

XECP_SUPP USB2_5 Low Speed

Note: **NOTE:** Bit definitions are the same as XECP_SUPP_USB2_4, offset 8010h.

10.2.162 XECP SUPP USB2_6 High Speed (XECP_SUPP_USB2_6) — Offset 8018h

XECP SUPP USB2_6 High Speed

Note: **NOTE:** Bit definitions are the same as XECP_SUPP_USB2_4, offset 8010h.

10.2.163 XECP SUPP USB3_0 (XECP_SUPP_USB3_0) — Offset 8020h

XECP SUPP USB3_0

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8020h	03201402h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	03h RO	**USB Major Revision: 3.0 (USB3_MAJ_REV):** USB Major Revision: 3.0
23:16	20h RW/L	**USB Minor Revision (USB3_MIN_REV):** USB Minor Revision:0.2 **Locked by:** XHCC1.ACCTRL
15:8	14h RW/L	**Next Capability Pointer (NCP):** Next Capability Pointer **Locked by:** XHCC1.ACCTRL
7:0	02h RO	**Supported Protocol ID (SPID):** Supported Protocol ID

10.2.164 XECP SUPP USB3_1 (XECP_SUPP_USB3_1) — Offset 8024h

XECP SUPP USB3_1

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8024h	20425355h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	20425355h RO	**XECP SUPP USB3 1 (XECP_SUPP_USB3_1):** Namestring USB

10.2.165 XECP SUPP USB3_2 (XECP_SUPP_USB3_2) — Offset 8028h

XECP SUPP USB3_2

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8028h	40000402h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:28	4h RO	**Protocol Speed ID Count (PROT_SPD_ID_CNT):** 1 USB 3.0 Speed (Supper Speed)
27:16	0h RO	**Reserved**
15:8	04h RO	**Compatible Port Count (CPC):** The compatible port count varies based on SKU - controlled by the USB3 Port config fuses
7:0	02h RO	**Compatible Port Offset (CPO):** Compatible Port Offset

10.2.166 XECP SUPP USB3_3 (XECP_SUPP_USB3_3) — Offset 802Ch

XECP SUPP USB3_3

Note: **NOTE:** Bit definitions are the same as XECP_SUPP_USB2_3, offset 800Ch.

10.2.167 XECP SUPP USB3_4 (XECP_SUPP_USB3_4) — Offset 8030h

XECP SUPP USB3_4

Note: **NOTE:** Bit definitions are the same as XECP_SUPP_USB2_4, offset 8010h.

10.2.168 XECP SUPP USB3_5 (XECP_SUPP_USB3_5) — Offset 8034h

XECP SUPP USB3_5

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8034h	000A4135h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	000Ah RO	**Protocol Speed ID Mantissa (PSIM):** Protocol Speed ID Mantissa
15:14	1h RO	**link Protocol (LP):** link Protocol
13:9	0h RO	**Reserved**
8	1h RO	**PSI Full Duplex (PFD):** PSI Full Duplex
7:6	0h RO	**PSI Type (PLT):** PSI Type
5:4	3h RO	**Protocol Speed ID Exponent (PSIE):** Protocol Speed ID Exponent
3:0	5h RO	**Protocol Speed ID Value (PSIV):** Protocol Speed ID Value

10.2.169 XECP SUPP USB3_6 (XECP_SUPP_USB3_6) — Offset 8038h

XECP SUPP USB3_6

Note: **NOTE:** Bit definitions are the same as XECP_SUPP_USB2_4, offset 8010h.

10.2.170 XECP SUPP USB3_7 (XECP_SUPP_USB3_7) — Offset 803Ch

XECP SUPP USB3_7

Note: **NOTE:** Bit definitions are the same as XECP_SUPP_USB2_4, offset 8010h.

10.2.171 Host Control Scheduler (HOST_CTRL_SCH_REG) — Offset 8094h

Host Control Scheduler

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8094h	00C08140h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Disable repeat scheduler service of usb2 periodic (SCH_USB2_PRDC):** Disable repeat scheduler service of usb2 periodic
30:27	0h RW	**Enable scheduler limiter functions to block async. traffic types across ports while periodic pending (SCH_BLOCK_ASYNC):** Enable scheduler limiter functions to block async. traffic types across ports while periodic pending
26	0h RW	**Enable pkt pending notification to usb3 ports (EN_PP_NTFC_USB3):** Enable pkt pending notification to usb3 ports
25	0h RW	**disable async. burst limitation while periodic in progress (DIS_ASYNC_BURST):** disable async. burst limitation while periodic in progress
24	0h RW	**Disable marking overlap flag on all TT periodic INs. (DIS_OVERLAP_TT_PERIODIC):** Disable marking overlap flag on all TT periodic INs.
23	1h RW	**disable blocking of async. scheduling while periodic active to same port (DIS_BLOCK_ASYNC_PER_ACT):** disable blocking of async. scheduling while periodic active to same port
22	1h RW	**Setting this bit enables pipelining of multiple OUT EPs (EN_PIPELINE_MULTIPLE_OUT):** Setting this bit enables pipelining of multiple OUT EPs (across diff ports). This will help boost the performance for multiple ports OUT test case
21	0h RW	**Enable stop serving packets to disabled port (EN_STOP_SERVE_DIS_PORT):** Enable stop serving packets to disabled port
20:17	0h RW	**TTE Host Control (TTE_HOST_CTRL):** (0): disable interrupt complete split limit to 3 microframes (1): disable checking of missed microframes (2): disable split error request w/NULL pointer on speculative INs with data payload and no TRB. (3): disable deferred split error request on speculative IN with data payload and no TRB. (7:4): reserved
16	0h RW	**disable deferred split error request on speculative IN with data payload and no TRB. (DIS_DEFFER_SPLIT_ERR):** disable deferred split error request on speculative IN with data payload and no TRB.
15	1h RW	**TTE: disable split error request w/NULL pointer on speculative INs with data payload and no TRB. (TTE_DIS_SPLIT_ERR_IN_DATA_NO_TRB):** TTE: disable split error request w/NULL pointer on speculative INs with data payload and no TRB.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**TTE: Disable checking of missed microframes (DIS_MISSED_UFRAME_CHECK):** TTE: Disable checking of missed microframes
13	0h RW	**TTE: Disable interrupt complete split limit to 3 micro frames (DIS_INTER_SPLIT_LIMIT):** TTE: Disable interrupt complete split limit to 3 micro frames
12:11	0h RW	**Cache Size Control Reg (CACHE_SZ_CTRL):** 0: 64 1: 32 2,3: 16
10:9	0h RW	**Maximum EP Per Slot (MAX_EP_SLOT):** 0: 32 1: 16 2: 8 3: 4
8	1h RW	**Turn on scratch_pad_en (TO_SCRATCH_PAD_EN):** Cmd Mgr: Enables scratch pad function
7	0h RW	**Scheduler Host Control Reg (STOP_SCH_UNCON):** enable check to stop scheduling on port that are not connected
6	1h RW	**disable 1 pack scheduling limit when ISO pending in present microframe (DIS_SCH_LIMIT):** disable 1 pack scheduling limit when ISO pending in present microframe
5:4	0h RW	**scheduler sort pattern (SCH_SORT_PATTERN):** 00 (default) search ISO ahead of interrupt within each service interval 01 - search USB2-ISO, USB3-ISO, USB2-Interrupt, USB3-Interrupt within each service interval 10 - search strictly by interval 11 - search all ISO intervals ahead interrupt intervals and within each interval, USB2 ahead of USB3
3	0h RW	**enable TTE overlap prevention on interrupt OUT EPs (at cost of possible service interval slip (EN_TTE_OVERLAP_PREV_OUT):** enable TTE overlap prevention on interrupt OUT EPs (at cost of possible service interval slip
2	0h RW	**enable TTE overlap prevention on interrupt IN EPs (at cost of possible service interval slip (EN_TTE_OVERLAP_PREV_IN):** enable TTE overlap prevention on interrupt IN EPs (at cost of possible service interval slip
1	0h RW	**Disable TRM active IN EP valid check function (DIS_TRM_ACT_IN_VALID):** Disable TRM active IN EP valid check function
0	0h RW	**Disable poll delay function (DIS_POLL_DELAY):** Scheduler: Disable poll delay function

10.2.172 Power Management Control (PMCTRL_REG) — Offset 80A4h

Power Management Control

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 80A4h	492D5094h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Async PME Source Enable (ASYNC_PME_SRC_EN):** This field allows the async PME source to be allowed to generate PME. This is specifically required for SOCs that do not allow for any clock other than RTC to be available during RTD3.
30	1h RW	**Legacy PME Source Enable (LEGACY_PME_SRC_EN):** This field allows the legacy PME source to be used in PME generation. The legacy source in in reference to the source prior to the RTD3 changes.
29	0h RW	**Reset Warn Power Gate Trigger Disable (RESET_WARN_PWR_GATE_TRIGGER_DISABLE):** This field controls the actions taken for due to reset warn. 0 - Reset Warn will trigger a HW autonomous Power Gate 1 - Reset Warn will not trigger a HW autonomous Power Gate
28	0h RW	**Clear PME Flag (CLR_PME_FLAG_PULSE_AUX_CCLK):** Internal PME flag Clear This Write-Only bit can be used to clear the internal PME flag. SW write to 1 will clear the PME flag. SW write to 0 will have no effect and be ignored by the controller. Read always return 0
27	1h RW	**Disable RTD3 power gating when in D3 (DIS_D3_PG):** Disable RTD3 power gating when in D3 and context save operation is not performed
26	0h RW	**XLFPS Count Source (XLFPSCOUNTSRC):** XLFPSCOUNTSRC (Source for LFPS OFF Counter) 0: Central RTC Counter for LFPS detection 1: Local Counter for LFPS detection
25	0h RW	**X Enable LFPS Filtering on RTC (XELFPSRTC):** XELFPSRTC (Enable LFPS Filtering on RTC) 0: Use Oscillator clock for LFPS Filtering during P3 1: Use RTC Clock for LFPS Filtering during P3
24	1h RW	**X ModPhy Sus Well Power Gate Disable for D0I2 (XMPHYSPGDD0I2):** XMPHYSPGDD0I2 (ModPhy Sus Well Power Gate Disable for D0I2) 0 : Modphy sus well power gating enabled 1 : Modphy sus well power gating disabled
23	0h RW	**X ModPhy Sus Well Power Gate Disable for D0I3 (XMPHYSPGDD0I3):** XMPHYSPGDD0I3 (ModPhy Sus Well Power Gate Disable for D0I3) 0 : Modphy sus well power gating enabled 1 : Modphy sus well power gating disabled

Bit Range	Default & Access	Field Name (ID): Description
22	0h RW	**X ModPhy Sus Well Power Gate Disable for RTD3 (XMPHYSPGDRTD3):** XMPHYSPGDRTD3 (ModPhy Sus Well Power Gate Disable for RTD3) 0 : Modphy sus well power gating enabled 1 : Modphy sus well power gating disabled
21:18	Bh RW	**D3 RTC Port Timer Tick Multiplier (XD3RTCPTTM):** XD3RTCPTTM (D3 RTC Port Timer Tick Multiplier) This register will be the multiplication factor for determining SSIC Wake Detection Frequency and RXDET based on the XD3RTCPTTC value. If XD3RTCPTTC is 9h and this register is Bh, frequency for RXDET and SSIC H8EXIT detection while MODPHY SUS Power gating is enabled would be 99ms.
17	0h RW	**U3 LFPS Periodic Sampling ON Time Control (U3_LFPS_PRDC_SAMPLING_ON_TIME_CTRL):** This field controls the ON time for the LFPS periodic sampling for USB3/SSIC ports. 0 ON time is 2 rtc clocks 1 ON time is 3 rtc clocks Note: This field is ignored if USB3/SSIC PHY SUS Well Power Gating is enabled.
16	1h RW	**AON LFPS Detector Enable Mode (AON_LFPS_DETECTOR_EN_MODE):** 1 - Allow the LFSP Detector in AON to own LFPS detection when the port is in PS3 for U2/U3 - not RxD regardless of port ownership. 0 - Allow the LFPS Detector in AON to own the LFPS detection only when the AON owns the port and in U2/U3 - not RxD
15:8	50h RW	**SS U3 LFPS Detection Threshold (SS_U3_LFPS_DETECTION_THRESHOLD):** This field controls the threshold used to determine when a valid U3 Wake is detected through when using the unfiltered LFPS source. The value on this field will reflect the binary count required to have been detected on the counter being clocked by the unfiltered lfps source to result in a valid U3 wake detection.
7:4	9h RW	**SS U3 LFPS Periodic Sampling OFF Time Control (SS_U3_LFPS_PRDC_SAMPLING_OFFTIME_CTRL):** This field controls the OFF time for the LFPS periodic sampling for USB3 Ports 0x0 periodic sampling is disabled. 0x1 OFF time is 1ms 0x2 OFF time is 2ms 0xF OFF time is 15ms The ON Time is determined by the amount of time required to reliably determine if there is a valid LFPS and is HW implementation specific. A speed up mode shall be implemented where this field is in units of us. i.e. 0x1 = 1 us OFF time, 0x2 = 2 us OFF time, etc.
3	0h RW	**PS3 LFPS Source Select (PS3_LFPS_SRC_SEL):** 0 LFPS Source is unfiltered 1 LFPS Source is filtered (Rx-Elec-Idle) LFPS Source is Rx-Elec-Idle for any non PS3 state.
2	1h RW	**XHCI Engine Autonomous Power Gate Exit Reset Policy (XHC_AUTO_PWRGATE_EXITRST_POLICY):** Controls when the xHCI engine is brought out of reset due to a power ungate. 0 Engine is brought out of reset when D3 to D0 is triggered. This allows for a quick power up sequence while leaving the virtual PCIe LTSSM in L23 is power ungate is not due to D3 to D0. 1 Engine is brought out of reset along with the rest of the IP. This is required for PMC save/restore flow.
1	0h RW	**USB2 Port Wake Unit Coupling Policy (USB2_PORT_WAKE_COUPLING_POLICY):** Controls the trigger for USB2 Port Wake Units to initiate Port Level Power Off Preparation. 0 RTD3 triggered 1 - Port Triggered when in L1, L2 or Disabled, Disconnected

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**USB3 Port Wake Unit Coupling Policy (USB3_PORT_WAKE_COUPLING_POLICY):** Controls the trigger for USB3 Port Wake Units to initiate Port Level Power Off Preparation. 0 - RTD3 Triggered 1 - Port Triggered when in PS3 due to RxDetect, U3, U2 or Disabled

10.2.173 Host Controller Misc Reg (HOST_CTRL_MISC_REG) — Offset 80B0h

Host Controller Misc Reg

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 80B0h	0080037Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**USB2 LTR Update Disable (USB2_LTRUPDT_DIS):** This controls the inclusion of the USB2 LTR based on link state as defined in the LTR HAS. Setting this bit will disable USB2 LTR and will expose a NO Requirement from USB2 thus not impacting the aggregated LTR vaule for the controller.
30	0h RW	**USB2 Line State Debounce During Port Reset Policy (USB2_LINE_STATE_DEBOUNCE_DURING_PORT_RESET_POLICY):** This register controls how the debounce is enforced during the Port Reset phase. 0 do not enable the line state debounce during port reset. 1 enable the line state debounce during port reset.
29	0h RW	**TTE PEXE Credit Fix Disable (TTE_PEXE_CREDIT_FIX_DISABLE):** When set, it disables a fix implemented to re-deem PEXE credits when a port is disconnected
28	0h RW	**TTE Scheduling policy (TTE_SCHEDULING_POLICY):** This register controls a fix made to prevent over-scheduling by not account for 188B in each uFrame. Setting this bit will disable the fix and allow for over-scheduling.
27	0h RW	**USB3 ITP Delta Timer Source Select (USB3_ITP_DELTA_TIMER_SOURCE_SELECT):** This register selects the source for the delta timer tracking used for ITP generation. 0 the source is a 16.666 ns tick generated from a crystal reference clock 1 - the source is a 16.666 ns tick generated from the aux_cclk. This field needs to remain in sync with Frame Timer Source Select to ensure the are both set or both cleared. There is no support for any other combination.
26	0h RW	**Frame Timer Source Select (FRAME_TIMER_SOURCE_SELECT):** This register controls the source for the frame timer. 0 the source for the frame timer is a crystal reference clock 1 the source for the frame timer is the aux_cclk.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RW	**uFrame Masking Enable (UFRAME_MASKING_ENABLE):** If set, enables the uFrame tick to be masked due to ports being in U3/NC. This controls a fix made to disable the auto masking of uFrame tick due to port state w/o any pipeline idle condition. When cleared, we rely on gating of frame timer due to proper port state and idleness tracking from the pipeline.
24	0h RW	**Late FID Check Disable (LATE_FID_CHECK_DISABLE):** This register disables the Late FID Check performed when starting an ISOCH stream.
23	1h RW	**Late FID TTE count adjust Disable (DIS_LATE_FID_TTE_CNT_ADJ):** 0 the value of frame late skip count starts at 1 for TTE eps and 0 for non tte eps. this represents an adjustment for the number of SI missed 1 the value of frame late skip count starts at 0 for both TTE eps and non tte eps
22	0h RW	**Late FID difference calculation legacy (DIS_DIF_CAL_LEGACY):** 0 late uframeid uses the new difference calculation to compute how may SI the TD is late 1 late uframeid uses the legacy difference calculation to compute how may SI the TD is late
21	0h RW	**ERDY flag Disable (ERDY_FLAG_DIS):** 0 An ERDY received on any interrupt EP will force the backbone clock high untill the next uframe to allow that eps trm pending mask to be cleared 1 operation this flag is disabled
20	0h RW	**enable ltr DB device clear (EN_LTR_DB_DEV_CLR):** 1 TDB 0 Operation
19	0h RW	**USB2 Resume Cx Inhibit Disable (USB2_RESUME_CX_INHIBIT_DISABLE):** Controls if USB2 L1 Resume is allowed to contribute to DMA Active which will inhibit Cx state. 0 USB2 L1 Resume is allowed to inhibit Cx via DMA Active 1 USB2 L1 Resume is NOT allowed to inhibit Cx via DMA Active When cleared, Cx will only be inhibited when the DMA traffic for the port begins.
18	0h RW	**Late FID TTE Disable (LATE_FID_TTE_DIS):** 0: Late Frame ID Check is enabled for TTE Endpoints 1: Late Frame ID Check is disabled for TTE Endpoints
17	0h RW	**Late FID uframe Check Disable (LATE_FID_UFRAME_CHK_DIS):** 0 Frame ID Match only asserts in uframe 7 for non-TTE Endpoints Frame before match 1 Frame ID Match can assert in any uframe
16	0h RW	**Late FID Extra Interval (LATE_FID_EXTRA_INTER):** This register controls the extra number of intervals added onto the advancing of late FID check escentially a bias used to correct for possible errors in implementation
15:0	037Fh RW	**Valid Isoch Scheduling Range (VALID_ISOCH_SCHEDULING_RANGE):** This register defines the window in miliseconds from the current Frame that will be considered for scheduling in an upcoming Frame. Anything scheduled outside of this window will be considered as late and will trigger the Missed Service Error.

10.2.174 Host Controller Misc Reg2 (HOST_CTRL_MISC_REG2) — Offset 80B4h

Host Controller Misc Reg2

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 80B4h	10800184h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**MAX_SHORT_PKT_ADV_CNT:** Short Packet Advance Throttling 0 - Limit SPA to 4 TRB's 1 - Limit SPA to 16 TRB's 2 - limit SPA to 64 TRB's 3 - limit SPA to 128 TRB's 4 - limit SPA to 512 TRB's 5 - limit SPA to 1024 TRB's 6 - limit SPA to 2048 TRB's 7 - Disabled
28	1h RW	**DIS_SCH_FRAMEID_CHK:** To disable Schedular FrameID check. 0-SCH frameid check is enabled. 1- SCH frameid check disabled
27	0h RW	**DISABLE_ISOC_BUF_OVERRUN_DETECT:** To disable ISOC buff overrun error code reporting. 0-Enables the reporting of ISOC buffer Overrun Error code. 1- Disabled ISOC buffer Overrun Error Code and reports Babble instead
26	0h RW	**DISABLE_CPL_NODMA_TRB_WALK:** To walk NON-DMA TRB at the end of TD. 0-Enables the walk of NON-DMA TRB on encountering TRB Cache Invalidation scenario for TTE EP. 1-Disables the NON_DMA TRB walk on encountering TRB Cache Invalidation Scenario
25	0h RW	**LTM_BELT_VALID_CLR:** ltm_belt_valid_clr
24	0h RW	**CFG_TRM_DROP_SCH_REQ_DIS:** cfg_trm_drop_sch_req_dis
23	1h RW	**CFG_TRM_DROP_TTE_REQ_DIS:** cfg_trm_drop_tte_req_dis
22	0h RW	**CFG_TRM_EDTLA_CLR_DIS:** cfg_trm_edtla_clr_dis
21	0h RW	**CFG_XFER_IS_SERVE_CHK_EN:** Enable checking is_serve condition in XFER, mainly for undoing fix if needed
20	0h RW	**CFG_CPL_NPKT0_FC_DIS:** Set low to allow receiving ACK with NUMP>0 to bring the TRM out of Remote Flow Control
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Disable IDT credit leak fix (CFG_DIS_ODMA_IDT_CRD_LEAK_FIX):** Disable the IDT credit leak fix in odma. 0 Fix is enabled 1 Fix is disabled
16	0h RW	**CFG_IDMA_TTYPE_CHK_DIS:** Set to disable packet Transfer Type checking in IDMA
15	0h RW	**HC Reset Controller Isolation Disable (HCRST_CTRL_ISOL_DISABLE):** Setting this bit to 1 will disable the HC Reset based quiescing/isolation flow
14	0h RW	**DISABLE_IDMA_PERF_FIX:** Fix is enabled by default 0 - fix is enabled 1 - fix is disabled
13	0h RW	**EN_HH_FRINDEX_NOT_RUN:** enable_hh_frindex_not_run
12	0h RW	**DISABLE_IDT_FIX_ODMA:** To disable DMA_RD_WAIT_IDT arc fix 0:enable the fix 1:disable the fix
11	0h RW	**DISABLE_PING_FIX_ODMA:** To disable ping fix 0:enable the fix 1:disable the fix
10	0h RW	**Disable CERR (Consecutive Errors) Fix (DISABLE_CERR_FIX_IDMA):** 0: Fix is enabled 1: Fix is disabled
9	0h RW	**EN_100MS_WATCH_DOG_TIMER:** 100ms Watch Dog Timer When set, it will enable 100ms Watch Dog Timer for Aux PM FSM for phystatus assertion else watch dog timer is 300ms.
8	1h RW	**EN_WATCH_DOG_TIMER:** Enable Watch Dog Timer:When set, it will enable 100/300ms watch dog timer for AUX PM FSM for phystatus assertion
7	1h RW	**EN_SSP_ISOC_PIPELINING:** enable isoc pipelining feature for ssp devices 1:enable the feature 0:disable the feature
6	0h RW	**DISABLE_TCG_UNGATE_ON_FLUSH:** When set, it will ungate the trunk clock gating for PIPE clock when there is flush whe DBC/EXI HHH is not idle.
5	0h RW	**DISABLE_VNN_FRAME_TIMER:** Frame Timer Select This register defines the frame timer used for all frame timer derived ticks. 0 - Frame timer in the VNN is the source for all frame timer related tracking. 1 - Frame timer in the Gated VNN is the source for all frame timer related tracking.
4	0h RW	**DISABLE_CLR_CCS_ON_CAS_SET:** Clear CCS on CAS When set, XHCI port will not clear the CAS when CCS is set. (BUGDE 5076358)
3	0h RW	**DISABLE_RHUB_PARK_AT_DBCDISC:** On Default Enables Root Hub s/m to arc to DBC_DISCONNECTED from ERROR and RESET states if the reason to enter into those state was a prior connection failure to exchange Link Capabilities Set 1 Keep the Root hub s/m in ERROR or RESET as the case may be , on a successful connection as a DBC if the first attempt was failed due to PortConfigTimeout
2	1h RW	**DISABLE_BLOCK_WPR_ON_DISPORTS:** Warm Port Reset on Disconnected Port Disable When set, disables the generation of a WPR on a disconnected port.

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RO	**Reserved**

10.2.175 Super Speed Port Enable (SSPE_REG) — Offset 80B8h

Super Speed Port Enable

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 80B8h	C0000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**SS_CFG_BLOCK_PWRDWN_4_ACT_LFPS:** Delay power down entry if Rx LFPS is active. Setting this bit will block the controllers power down entry seq (for Sx/D3/D0i2 etc) if Rx LFPS is active. The power down entry will happen once a device stops sending LFPS.
30	1h RW	**DIS_CLR_CCS_4_HCRESET:** Enable Clearing of CCS for HCReset - Setting this bit clears the USB3 ports PORTSC.CCS bit upon HCReset.
29	0h RW	**DISABLE_RAWLFPS_BASED_WAKE_FIX:** Disable Raw Lfps Detection Based Wake from P3 This bit is used to disable RTL fix provided to separate RawLFPS and RxElecIDle detection 0: Transition port to RESUME based on raw LFPS detection 1 : Transition port to RESUME based Filtered RxElecIdle detection
28	0h RW	**EXI OVERRIDE DISABLE (EXI_OVERRIDE_DIS):** EXI Override Disable
27:4	0h RO	**Reserved**
3:0	0h RW	**SuperSpeed Port Enable Register (SSPE_REG):** USB3 Port Enable This field controls whether SuperSpeed capability is enabled for a given USB3 port. When set to 1, Enables SS termination Enables PORTSC to to see the connects on the ports. When set to 0, Disables SS termination Blocks PORTSC from reporting attach/connect. Places port in the lowest power state.

10.2.176 AUX Power Management Control (AUX_CTRL_REG1) — Offset 80E0h

AUX Power Management Control

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 80E0h	8080BCE0h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**D3 Hot function enable register (D3_HOT_FXN_EN):** This bit is from pin input which is set 1. But we allow software to alter it if it is needed. 1: D3 hot enabled 0: D3 hot not abled.
30	0h RW	**Allow L1 Core Clock Gating (ALL_L1_CORE_CG):** When set to 1 allows core clock being gated during L1 state.
29	0h RW	**Allow Engine PHY Status Extension (AL_EP_SEXT):** When set to 1 allows the engine to extend PHY status of PCIe PIPE for one more cycle. This is due to the fact that our rate change function has a potential of not being able to sample the phystatus signal.
28	0h RW	**Allow Engine PCIe Rate Change Passing (ALL_EP_RCP):** When set to 1 allows the engine to pass PCIe rate change signal as it is from PCIe core to PCIe PHY.
27	0h RW	**Allow Engine PERST Fundamental Reset (AL_PERST_FRST):** When set to 1 allow engine to treat PERST# as a foundamental reset
26	0h RW	**Overwrite PCIe P2 to P1 (OVR_PCIE_P2_P1):** When set to 1 will overwrite a PCIe powerdown state of P2 to P1.
25	0h RW	**Set Internal SSV 1 (SET_ISSV_1):** When set to 1 set the internal SSV to 1.
24	0h RW	**Clear Internal SSV 0 (CLR_ISSV_0):** When set to 1 clear the internal SSV to 0.
23	1h RW	**Enable save_restore_enable SW Loading (EN_SRE_SW_LD):** This is a bit that enables the save_restore_enable signal being loaded when a software command has set Save bit. This is a debug function.
22	0h RO	**Reserved**
21	0h RW	**Force save_restore 1 (FORCE_SR1):** When set to 1, it will force the save_restore flag to 1. This flag is an bit to ensure that we have masked the update during low power state. If software write this bit to 1, it must write it to 0 in order to resume the normal save and restore function.
20	0h RW	**CFG DISABLE_WARM_RST_DET_specUpPorts (CFG_DIS_WRSTDET_SPECU):** 0: Speculative upstream for Debug and SS/SSP port will detect WPR 1: No speculative upstream till port configuration is completed
19	0h RW	**cfg iob drivestrength[1] (CIDS1):** Controls the drive strength of the IO buffer

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**cfg iob drivestrength[0] (CIDS0):** Controls the drive strength of the IO buffer
17	0h RW	**CFG_DIS_ARC_RXDP3:** When set to '1' DIsables arc to RXDET_p3 on disc from U2P3/U3
16	0h RW	**cfg clk gate dis (CCGD):** 1: Disable USB3 port clock gating 0: Enable USB3 port clock gating
15	1h RW	**Enable CFG RXDET P3 (EN_CFG_RDP3):** When set to '1' enable cfg rxdet p3
14	0h RW	**Enable CFG PIPE Reset (EN_CFG_PIPE_RST):** When set to '1' enable cfg pipe rst
13	1h RW	**Enable Filter TX Idle (EN_FILT_TX_IDLE):** When set to 1 enables a filter function to TX electrical idle signal at PCie PIPE. We have a filter that will set TXelecidle signal of PCIe PIPE to 1 whenever we are in isolation state or power down transition states.
12	1h RW	**Enable Host Engine Generate PME (EN_HE_GEN_PME):** This is a global switch to whether or not eable this host engine to generate PME message.
11	1h RW	**Enable Isolation (EN_ISOL):** When set to '1' enable isolation
10	1h RW	**Enable L1 Caused P2 Overwrite (EN_L1_P2_OVR):** Set 1 to enable a new feature. This new feature is designed to use L1 as a state to identify whether we should do P2 Overwrite or not. We used to use P1 state to identify whether or not to invoke P2 overwrite function.
9	0h RW	**Enable Core Clock Gating (EN_CORE_CG):** When set to '1' disable core clock gating based on low power state entered
8	0h RW	**Enable PHY Status Timeout (EN_PHY_STS_TO):** When set to '1' enable PHY status timeout function which is designed to cover the PCIePHY issue that we may have not able to detect the PHY status toggle.
7	1h RW	**Ignore aux_pm_en PCIe Core (IGN_APE_PC):** When set to '1' ignore the aux_pm_en reg from PCIe core to continue the remote wake/clock switching support
6	1h RW	**Enable P2 Overwrite P1 (EN_P2_OVR_P1):** When set to '1' enable P2 overwrite P1 when PCIe core has indicated the transition from P0 to P1. This is to enable entering the even lower power state.
5	1h RW	**Enable P2 Remote Wake (EN_P2_REM_WAKE):** When set 1 '1' enable the remote wake function by allowing P2 clock/switching and P2 entering
4:1	0h RW	**Forced PM State (FORCED_PM_STATE):** Forced PM state
0	0h RW	**Initiate Force PM State (INIT_FPMS):** When set to '1' force PM state to go to the state indicated in bit 4:1

10.2.177 SuperSpeed Port Link Control (HOST_CTRL_PORT_LINK_REG) — Offset 80ECh

SuperSpeed Port Link Control

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 80ECh	18020000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	03h RW	**Force LTSSM State (FORCE_LTSSM_ST):** LTSSM state to be forced
26	0h RW	**Direct Link LTSSM State (DL_LTSSM_ST):** 0: Normal operation mode 1: Direct link to a specific state specified by bit 31:27
25	0h RW	**Direct Link To U0 (DL_U0):** 0: Normal operation mode 1: Direct link to U0
24:21	0h RW	**Forced Compliance Pattern (FORCED_CMP_PAT):** Compliance pattern to be forced to enter compliance mode
20	0h RW	**Enable Link Error Target Count (EN_LES_CNT):** 0: Disable link error target count 1: Enable link error target count
19	0h RW	**TS rcv to complete U1/U2/U3 exit LFPS handshake (TS_RCV_UX_EXIT_LFPS_HS):** 1: enable TS receive to complete U1/U2/U3 exit LFPS handshake 0: disable TS receive to complete U1/U2/U3 exit LFPS handshake
18	0h RW	**Enable IDLE Receive to exit Polling.Config and Recov.Config (EN_LOGIC_TO_EXIT_POLLCONF_AND_RECCONF):** 1: enable logic idle receive to exit Polling.Configuration and Recovery.Configuration 0: disable logic idle receive to exit Polling.Configuration and Recovery.Configuration
17	1h RW	**Port Initialization Timeout Value (PORT_INTIL_TIMEOUT_VAL):** This bit specifies the port initialization timeout value. 1: 20us - 21us 0: 19us - 20us
16:15	0h RW	**PHY Low Power Latency (PHY_LP_LAT):** This field defines the latency to drive the PHY to enter low power mode 0: 4 cycles 1: 8 cycles 2: 16 cycles 3: 32 cycles
14:12	0h RW	**Link Recovery Minimum Time (LR_MIN_TM):** This value defines the minimum time for the link to stay in Recovery.Active other than from U3. The granuity is 128us.
11:9	0h RW	**Link Polling Minimum Time (LP_MIN_TM):** This value defines the minimum time for the link to stay in Polling.Active and Recovery.Active from U3. The granuity is 128us.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Force Link Accept PM Command (FORCE_LA_PMC):** 0: Normal operation mode 1: Force link to accept power management command
7	0h RW	**Direct Link Recovery U0 (DL_REC_U0):** 0: Normal operation mode 1: Direct link to Recovery from U0
6	0h RW	**Link Fast Training Mode (LINK_FTM):** 0: Normal operation mode 1: Link fast training mode This bit should be written 0 in normal operation.
5	0h RW	**Disable Link Scrambler (DIS_LINK_SCRAM):** 0: Enable link scrambler 1: Disable link scramber
4	0h RW	**Direct Link U3 From U0 (DL_U3_U0):** 0: Normal operation mode 1: Direct link to U3 from U0
3	0h RW	**Direct Link U3 From U0 (DL_U2_U0):** 0: Normal operation mode 1: Direct link to U2 from U0
2	0h RW	**Direct Link U3 From U0 (DL_U1_U0):** 0: Normal operation mode 1: Direct link to U1 from U0
1	0h RW	**Enable Link Loopback Initiator Mode (EN_LINK_LB_MAST):** 0: Disable link loopback initiator mode 1: Enable link loopback initiator mode
0	0h RW	**Disable Link Compliance Mode (DIS_LINK_CM):** 0: Enable link compliance mode 1: Disable link compliance mode

10.2.178 USB2 Port Link Control 1 (USB2_LINK_MGR_CTRL_REG1) — Offset 80F0h

These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 80F0h	314803A0h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	31h RW	**FS/LS Mode SE0 Disconnect Delay[7:0] (FSLS_SE0_DIS_DEL_7_0):** # of microseconds of SE0 in FS/LS mode to register disconnect had occurred.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**Enable SNPS PHY Fix (EN_SNPS_PHY_FIX):** Enable SNPS PHY Fix: 1: When set, termselect will assert at the start of EOR. Fslsserialmode will also deassert at the same clock as txenb. 0: Legacy behavior for Intel PHY.
22	1h RW	**Enable L1 Disconnect in L0 (EN_L1_DISC_IN_L0):** Enable Pseudo L0 state when transition from L1 to L2 due to disconnect: 1: When set, {L1 suspendm, L2 suspendm} will go from 01->11->10 to allow the USB2 PHY to exit L1 and enter L2 for deeper PM 0: Legacy behavior (01->10)
21	0h RW	**Disable Purge On SETUP Fix (DIS_PURGE_ON_SETUP_FIX):** To disable the fix for SETUP purge that match for both device address and endpoint number: 0: Only allow purge for SETUP when both device address and endpoint number are matched. 1: Revert back to old behaviour that purge is allowed when either device address or endpoint number is matched.
20	0h RW	**L1 Exit Recovery Mode (L1_EXIT_RECOVERY_MODE):** Mode for extended L1 Exit recovery delay: 0: 12us 1: 50us
19	1h RW	**L1 Timeout Increment Mode (L1_TO_INCR_MODE):** Mode select for L1 Timeout increments: 0: time out increments are in 125us 1: L1 Timeout increments are in 256us. Refer to USB2 PORTHLPMC.L1 Timeout in XHCI Spec for additional details
18	0h RO	**Reserved**
17	0h RW	**Enable Detect Minimal Packet EOP (EN_DETECT_NOMINAL_PKT_EOP):** 0: Detect minimal packet EOP. 1: Detect nominal packet EOP.
16	0h RW	**Disable Chirp Response (DIS_CHIRP_RESPONSE):** 0: Normal 1: Force full speed on host ports (disable chirp response)
15	0h RW	**Disable 192 Byte Limit Check (DIS_192B_LIM):** 0: Enforce 192 byte limit on complete-split INs. Treat any packet) 192 as babble case. 1: Disable 192 byte limit check.
14	0h RW	**External Provided FS/LS Disconnect (EXT_FSLS_DIS):** 0: Internal FS/LS Disconnect from linestate(1:0) 1: External provided FS/LS Disconnect from hostdisconnect input
13:12	0h RW	**UTMI Reset Source Select (UTMI_RST_SEL):** Select UTMI Reset Source (FRD UTMI Reset Only) 00: HCReset or Force PHY Reset or internal reset after disconnect/suspend for restart (default) 01,11: UTMI reset = ~UTMI suspendm 10: UTMI reset = ~UTMI suspendm and synchronization to port clk.
11	0h RW	**Disable HS Disconnect Window (DIS_HS_DIS_WIN):** 0: Enable HS Disconnect Window Function 1: Disable HS Disconnect Window Function
10	0h RW	**Disable Port Error Detection (DIS_PERR_DET):** 0: Enable Port Error Detection (default) 1: Disable Port Error Detection

Bit Range	Default & Access	Field Name (ID): Description
9	1h RW	**Disable Peek Function for ISO-OUT (DIS_PF_IOUT):** 0: Enable Peek function for ISO-OUT (default) 1: Disable Peek function for ISO-OUT
8	1h RW	**Drive Resume-K FS/LS Serial Interface (DRV_RESK_FSLS_SER):** 0: Drive Resume-K on parallel Interface 1: Drive Resume-K directly on FS/LS Serial Interface (default)
7	1h RW	**Enable USB2 Drop-Ping (EN_U2_DROP_PING):** 0: Disable Drop-Ping Function in USB2 Protocol (default) 1: Enable Drop-Ping Function in USB2 Protocol
6	0h RW	**Enable USB2 Force-Ping (EN_U2_FORCE_PING):** 0: Disable Force-Ping Function in USB2 Protocol (default) 1: Enable Force-Ping Function in USB2 Protocol
5	1h RW	**Enable USB2 Auto-Ping (EN_U2_AUTO_PING):** 0: Disable Auto-Ping Function 1: Enable Auto-Ping Function in USB2 Protocol (default)
4	0h RW	**Disable PHY SuspendM (DIS_PHY_SUSM):** 0: PHY is suspend=U3,U2,disconnect (default) 1: Disable PHY SuspendM in All States
3	0h RW	**UTMI Internal Clock Gate Disable (UTMI_INT_CG_DIS):** 0: Normal operation (internal clock gated in U2,U3,disconnect) 1: UTMI Internal Clock Gate Disable
2	0h RW	**Disable PHY SuspendM in Disconnect State (DIS_PSUSM_DS):** 0: PHY is suspendM=0 in Disconnect State (default) 1: Disable PHY SuspendM in Disconnect State
1	0h RW	**Force PHY Reset (FORCE_PHY_RST):** 0: Normal Operation (default) 1: Force PHY Reset
0	0h RW	**USB2 Accelerated Simulation Timing (U2_ACC_SIM_TIM):** 0: Normal Operation (default - FPGA/ASIC) 1: USB2 Accelerated Simulation Timing (default - simulation)

10.2.179 USB2 Port Link Control 2 (USB2_LINK_MGR_CTRL_REG2) — Offset 80F4h

These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 80F4h	80C40620h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**Total Reset Duration[0] (TOT_RST_DUR_0):** # of microseconds for total reset duration

Bit Range	Default & Access	Field Name (ID): Description
30:18	0031h RW	**Chirp-K Duration (CHIRPK_DUR):** # of microseconds of Chirp-K to register that a device is chirping
17:5	0031h RW	**K/J Disconnect Connect Delay (KJ_DIS_CON_DEL):** # of microseconds of K/J in disconnected state to register connect has occurred.
4:0	00h RW	**FS/LS Mode SE0 Disconnect Delay[12:8] (FSLS_SE0_DIS_DEL_12_8):** # of microseconds of SE0 in FS/LS mode to register disconnect had occurred.

10.2.180 USB2 Port Link Control 3 (USB2_LINK_MGR_CTRL_REG3) — Offset 80F8h

These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 80F8h	F865EB6Bh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RW	**U2 Entry Ignore Linestate Changes Duration[3:0] (U2_IGN_LS_DUR_3_0):** # of microseconds after entering U2, linestate changes are ignored as bus settles
27:15	10CBh RW	**U3 Entry Ignore Linestate Changes Duration (U3_IGN_LS_DUR):** # of microseconds after entering U3, linestate changes are ignored as bus settles
14:0	6B6Bh RW	**Total Reset Duration[15:1] (TOT_RST_DUR_15_1):** # of microseconds for total reset duration

10.2.181 USB2 Port Link Control 4 (USB2_LINK_MGR_CTRL_REG4) — Offset 80FCh

These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 80FCh	02008003h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:27	0h RW	**Additional Guardband for L1 Advance Prewake (ADD_GB_4_L1_PREWAKE):** 00 = +0 us 01 = +1uF 10 = +2uF 11 = +4uF
26	0h RW	**select L1 min idle duration that will be driven to Scheduler. Either drive '0' or based on L1 Timeout value (SEL_L1_MIN_IDLE):** select L1 min idle duration that will be driven to Scheduler. Either drive '0' or based on L1 Timeout value
25	1h RW	**Enable periodic_prewake to prevent L1 entry if in U0, or wake from L1 if already in U2. (EN_PER_PREWAKE):** Enable periodic_prewake to prevent L1 entry if in U0, or wake from L1 if already in U2.
24:22	0h RO	**Reserved**
21:9	0040h RW	**U2 Detect Remote Wake Delay (U2D_RWAKE_DEL):** #of microseconds after detecting U2 remote wake condition to reflect K
8:0	003h RW	**U2 Entry Ignore Linestate Changes Duration[12:4] (U2_IGN_LS_DUR_12_4):** # of microseconds after entering U2, linestate changes are ignored as bus settles

10.2.182 Power Scheduler Control-0 (PWR_SCHED_CTRL0) — Offset 8140h

Power Scheduler Control-0

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8140h	0A019132h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0Ah RW	**Engine Idle Hysteresis (EIH):** This register controls the min. idle span that has to be observed from the engine idle indicators before the power state flags (xhc_*_idle) will indicate a 1.
23:12	019h RW	**Backbone PLL Shutdown Advance Wake (BPSAW):** This register controls the time before the next scheduled transaction where the Backbone PLL request will assert. Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124)
11:0	132h RW	**Backbone PLL Shutdown Min. Idle Duration (BPSMID):** The sum of this register plus the Backbone PLL Shutdown Advance Wake form to a Total Idle time. When the next scheduled periodic transaction is after present time + Total Idle, the Backbone PLL request will de-assert, allowing the PLL to shutdwon. Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124)

10.2.183 Power Scheduler Control-1 (PWR_SCHED_CTRL2) — Offset 8144h

These bit enable by EP type those EPs classes that are considered for determining next periodic active interval for pre-wake of

the periodic_active signal. EP classes that are disabled may never be observed in setting of the periodic_active signal.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8144h	0000023Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26	0h RW	**Disable Power Scheduler wait for inprogress NDE (DISABLE_INPROG_NDE_WAIT):** Policy for controlling transition of LTR_STATE_* FSM to move from ACTIVE to *_INACTIVE states 0: LTR_STATE_* FSM will wait for inprogress NDE message to complete before transitioning to one of the INACTIVE states 1: LTR_STATE_* FSM will not wait for inprogress NDE message to complete before transitioning to one of the INACTIVE states
25	0h RW	**Disable sending NDE sideband messages with NoREQ (NDE_SBMSG_NOREQ_DIS):** Policy to disable sending NOREQ NDE sideband messages 0: Controller will send NOREQ NDE sideband messages 1: Controller will not send NOREQ NDE sideband messages
24	0h RW	**Enable NDE sideband messaging (NDE_SBMSG_EN):** Policy to enable NDE Sideband messaging. 0: Controller is not allowed to send NDE sideband messages 1: Controller is allowed to send NDE Sideband messages
23:21	0h RO	**Reserved**
20	0h RW	**Revert LPM Hysteresis Clear (RVRT_LPM_HYS_CLR):** 0: The per-port periodic active signal from the Scheduler is used to reset the per-port hysteresis loop for the LPMs. 1: The global pwr_sch_xhc_engine_prdc_idle signal is used to reset all of the per-port hysteresis loops for LPM. This is the legacy behavior.
19	0h RO	**Reserved**
18	0h RW	**Flow-Controlled SS INTR 2SI Mode (FLOW_CTRL_2SI_MODE):** 0: The Power Scheduler will Schedule all Flow-Controlled SS INTR Endpoint's alarm to the SI determined by the Endpoint's Interval value. 1: The Power Scheduler will Schedule all Flow-Controlled SS INTR Endpoint's alarm to twice the SI determined by the Endpoint's Interval value.
17	0h RW	**d0i2 Clear Alarm Fix Disable (D0I2_CLR_ALARM_FIX_DISAB):** d0i2 Clear Alarm Fix Disable

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**No Doorbell Clear Valid Disable (NO_DB_CLR_VAL_DISAB):** No Doorbell Clear Valid Disable
15	0h RW	**Disable BELT Latch (DISAB_BELT_LATCH):** 1: The Power Scheduler's interface to the LTR Manager signals BELT and No_Requirement are not latched with the Request signal and can change before Halt is deasserted. 0: The Power Scheduler's interface to the LTR Manager signals BELT and No_Requirement are latched when the Request signal is asserted and will remain latched until Halt is deasserted.
14	0h RW	**LPM Prewake Interrupt NAK Disable (LPM_PREWAKE_INTR_NAK_DIS):** LPM Prewake Naked Interrupt Enable 0: Ignore the Naked INTR for LPM. 1: Do not ignore the Naked INTR for LPM.
13:12	0h RW	**LPM Prewake Interrupt Enable (LPM_PREWAKE_INTR_EN):** LPM Prewake Interrupt Enable 11: Disable interrupt prewake for LPM. 01: Enable interrupt OUT prewake for LPM. 10: Enable interrupt IN prewake for LPM. 00: Enable both interrupt IN/OUT prewake for LPM.
11:10	0h RW	**Idle Scale (IDLE_SCALE):** Engine Idle Hysteresis Scale Controls the Engine Idle Hysteresis scale. 0 - clock 1 - 1 us 2 - 125 us
9	1h RW	**HS Interrupt-OUT Alarm (HS_INT_OUT_ALRM):** HS Interrupt OUT Alarm
8	0h RW	**HS Interrupt-IN Alarm (HS_INT_IN_ALRM):** HS Interrupt IN Alarm (HSII): Note: This is required to be set to enable the functionality behind the PCICFG.HSCFG2.HSIIPAPC method of tracking HS Intr IN EP's for Periodic Active.
7	0h RW	**SS Interrupt-OUT FC Alarm (SS_INT_OUT_FC_ALRM):** SS Interrupt OUT Alarm
6	0h RW	**SS Interrupt-IN Alarm (SS_INT_IN_FC_ALRM):** SS Interrupt IN Alarm
5	1h RW	**SS Interrupt-OUT and not in FC Alarm (SS_INT_OUT_ALRM):** SS Interrupt OUT and not in FC Frame Alarm
4	1h RW	**SS Interrupt-IN and not in FC Alarm (SS_INT_IN_ALRM):** SS Interrupt IN and not in FC Frame Alarm
3	1h RW	**HS ISO-OUT Alarm (HS_ISO_OUT_ALRM):** HS ISO-OUT Alarm
2	1h RW	**HS ISO-IN Alarm (HS_ISO_IN_ALRM):** HS ISO-IN Alarm
1	1h RW	**SS ISO-OUT Alarm (SS_ISO_OUT_ALRM):** SS ISO-OUT Alarm
0	1h RW	**SS ISO-IN Alarm (SS_ISO_IN_ALRM):** SS ISO-IN Alarm

10.2.184 AUX Power Management Control (AUX_CTRL_REG2) — Offset 8154h

AUX Power Management Control Register2

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8154h	81192206h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**Disable L1P2 Exit on Wake Enable (DIS_L1P2_EXIT_ON_WAKE_EN):** This bit disables the dependency on Wake Enables defined in PORTSC for L1P2 exit when in D0
30	0h RW	**Link Fast Training Mode (CFG_FAST_TRAINING):** 0: Normal operation mode 1: Link fast training mode This bit should be written 0 in normal operation
29	0h RW	**SNPS_PHYSTATUS_DONE_L1_DIS:** snps_phystatus_done_l1_dis
28	0h RW	**SHADOW_DECODE_DIS:** shadow_decode_dis_reg
27	0h RW	**BATT_CHARGE_D3_EN:** batt_charge_d3_en
26	0h RW	**CFG_DEBOUNCE_EN:** cfg_debounce_en
25	0h RW	**PCIE_P0_EXIT_L1_EN:** pcie_p0_exit_l1_en_reg
24	1h RW	**Enable L1 exit notification to SNPS PCIe core (EN_L1_EXIT_NOTIF_PCIE):** This bit enables a L1 exit notification to SNPS PCIe core. There is a case where USB ports have waked up and AUX PM module has started the wakeup process. The AUX PM control state got into a wait for P0 state because it needs to wait until PCie core to signal powerdown state change. Due to the fact that the core is in D3Hot, there is no run_stop bit set such that no internal interrupt will be fired. This causes the LTSSM of PCIe stayed in L1 even though AUX PM has known that it needs an L1 exit. This bit works together with bit21 of this register. 1: enables this feature 0: disables this feature.
23	0h RW	**DISABLE PLC ON DISCONNECT (DIS_PLC_ON_DISCONNECT):** 1: do not assert PLC for disconnection 0: assert PLC for disconnection
22	0h RW	**Treat IDLE as TS2 when LTSSM in Wait for TS2 (TREAT_IDLE_AS_TS2_IN_LTSSM_WAIT_4_TS2):** This bit enables a feature in PCie core LTSSM to treat IDLE received as TS2 when LTSSM is in wait for TS2 receive state. This is a function requested from PHY where it is possible to not able to receive TS2 without error. 1: treat Logic IDLE as TS2 received when in some PCIe LTSSM state. 0: disable this feature.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**Disable p2 overwrite due to the D3HOT where PCIe core enters the L1 (DIS_P2_OVERWRITE_DUE2_D3HOT):** We added a feature where if PCIe core LTSSM enters L1 due to the D3hot, the aux PM control will not start a P2 overwrite function in anticipating for the next L23 enter. 1: disables p2 overwrite due to the D3HOT where PCIe core enters the L1. 0: enables P2 overwrite even if we are in D3Hot.
20	1h RW	**Enable the port to enter U3 automatically when in U1/U2 (ENABLE_AUTO_U3_ENTRY_FROM_U2_U3):** 1: enables the port to enter U3 automatically when in U1/U2 0: disables the port to enter U3 automatically when in U1/U2
19	1h RW	**No linkdown reset is issue during low power state (DIS_LINKDOWN_RST_DURING_LOW_POWER):** No linkdown reset is issue during low power state
18	0h RW	**Enable Exit Deep Sleep If PCIE in P0 (EN_EXIT_DEEP_SLEEP_IF_PCIE_IN_P0):** This bit enables a feature in AUX PM module where if PCIe core LTSSM is in P0 for a duration of time, we will exit the deep sleep state. This is for failure control in case. 1: enables this feature 0: disable this feature
17	0h RW	**U2 Exit LFPS Timer Value (U2_EXIT_LFPS_TIMER_VALUE):** This bit selects U2 exit LFPS timer value 0: 320ns 400ns in 25MHz domain 1: 240ns 320ns in 25MHz domain
16	1h RW	**Enable Exit Deep Sleep on USB Port Wakeup (EN_EXIT_DEEP_SLEEP_ON_USB_PORT_WAKEUP):** This bit enables a function that AUX PM module exits from the deep sleep state due to the USB ports wakeup level signal. We have added this feature where USB ports will generated a wakeup level signal to wakeup the AUX PM module if it is in deep sleep state and this level signal will be cleared if the change bits are updated by software. 1: enables this function 0: disables this function which means that a wakeup pulse generated from each USB PortSC event will wake up the AUX PM module from deep sleep if the D3 state is programmed.
15:14	0h RW	**P3 Entry Timeout (P3_ENTRY_TIMEOUT):** This field defines the timeout value to enter P3 mode in U2. 00: 7us 8us 01: 511us 512us 10: disables the timer (0us) 11: disables the timer (0us)
13	1h RW	**Enable U2 P3 Mode (EN_U2_P3):** 0: Disable U2 P3 mode 1: Enable U2 P3 mode
12:11	0h RW	**Fine Debug Mode Select (FINE_DM_SEL):** Fine Debug Mode Select
10	0h RW	**Enable Low Power State Based Core Clock Gating (EN_LP_CORE_CG):** When set to '1' enable core clock gating based on low power state entered
9	1h RW	**Disable USB3 Port Status Changed Event (DIS_U3_PORT_SCE):** 0: Enable USB3 port status change event generation if any change bit is not cleared 1: Disable USB3 port status change event generation if any change bit is not cleared Bit 12 default 0
8:4	00h RW	**Debug Mode Select Register (DEB_MODE_SEL):** Debug Mode Select Register
3	0h RW	**Enable Auto Wakeup Non-IDLE (EN_AWAK_NIDLE):** When set to 1 enables the auto wakeup function when engine has identified non IDLE condition.

Bit Range	Default & Access	Field Name (ID): Description
2	1h RW	**Enable PM Control P1 Exit P2 (EN_PMC_P1_EXIT_P2):** When set 1 enables the PM control module to transition to P1 instead of P0 when exit P2.
1	1h RW	**Enable PCIe PIPE CLK Isolation (EN_PP_CLK_ISOL):** When set to 1 enables the PCIe PIPE CLK to be isolated when main power is removed.
0	0h RW	**Enable P2 Overwrite P1 Allowed Detect (EN_P2OVRP1_ADET):** When set to 1 enables a function that can detect whether or not enable P2 overwrite P1 function. The condition to get to P2 overwrite is when engine is in idle conditions. This means that there is no ISO EP pending.

10.2.185 USB2 PHY Power Management Control (USB2_PHY_PMC) — Offset 8164h

USB2 PHY Power Management Control

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8164h	000000FCh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**125us Frame Tick Sync Selection (FRAMETICK_SYNC_SEL):** 0: Selects 125us tick synched from Frame Clock. 1: Selects 125us tick synched from aux_clk.
30:8	0h RO	**Reserved**
7	1h RW	**Enable Command Manager Active Indication for Tx/Rx Bias (EN_CMDM_TXRXB):** Enable Command Manager Active indication for Tx/Rx Bias circuit HS Phy PM Policy
6	1h RW	**Enable TTE Tx/Rx Bias (EN_TTE_TXRXB):** Enable TTE Active indication for Tx/Rx Bias circuit HS Phy PM Policy
5	1h RW	**Enable IDMA Tx/Rx Bias (EN_IDMA_TXRXB):** Enable IDMA Active indication for Tx/Rx Bias circuit HS Phy PM Policy
4	1h RW	**Enable ODMA Tx/Rx Bias (EN_ODMA_TXRXB):** Enable ODMA Active indication for Tx/Rx Bias circuit HS Phy PM Policy
3	1h RW	**Enable TRM Tx/Rx Bias (EN_TRM_TXRXB):** Enable Transfer Manager Active indication for Tx/Rx Bias circuit HS Phy PM Policy
2	1h RW	**Enable Scheduler Tx/Rx Bias (EN_SCH_TXRXB):** Enable Scheduler Active indication for Tx/Rx Bias circuit HS Phy PM Policy
1	0h RW	**Enable Rx Bias ckt disable (EN_RXB_CD):** When set enables the Rx bias ckt to be disabled when conditions met (as described by the HS phy PM policy bits)

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Enable Tx Bias ckt disable (EN_TXB_CD):** When set enables the Tx bias ckt to be disabled when conditions met (as described by the HS phy PM policy bits)

10.2.186 XHCI Aux Clock Control Register (XHCI_AUX_CCR) — Offset 816Ch

XHCI Aux Clock Control Register

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 816Ch	000F403Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	1h RW	**USB3 Partition Engine/Link trunk gating Enable (PARUSB3_ENG_GEN):** When set to 1 enables gating of the SOSC trunk to the XHCI engine and link in the PARUSB3 partition.
18	1h RW	**USB3 Partition Frame Timer trunk gating Enable (PARUSB3_LINK_GEN):** When set to 1 enables gating of the SOSC trunk to the Frame timer in the PARUSB3 partition.
17	1h RW	**USB2 link partition clock gating enable (PARUSB2_CLK_GEN):** When set to 1 enables gating of the SOSC trunk to the USB2 link and Phy logic in the PARUSB2 partition.
16	1h RW	**USB2/USHIP 12.5 MHz partition clock gating enable (USHIP_PCGEN):** When set to 1 enables gating of the 12.5 MHz SOSC trunk to the USB2 and USHIP logic in the PARUSB2 partition.
15	0h RO	**Reserved**
14	1h RW	**USB3 Port Aux/Core clock gating enable (USB3_AC_CGE):** When set, allows the aux_cclk clock into the USB3 port to be gated when conditions are met. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
13:12	0h RW	**Rx Detect Timer when port Aux Clock is Gated (RX_DT_ACG):** This field defines the value of the timer used to perform Rx Detect when port Aux Clock has been gated. 0x0: 100ms 0x1: 12ms Others: Reserved Note: This timer shall use the Fast Training Timer Tick (about 1us tick) for simulation purposes. For Fast Training mode, the above timeouts will become about 11us and about 100us, +/- implementation uncertainty, respectively.

Bit Range	Default & Access	Field Name (ID): Description
11:10	0h RO	**Reserved**
9	0h RW	**Aux Clock Gating Counter PipeStage Enable (AUXCLKGT_CNTEN_PIPE_STGEN):** Policy to enable pipe stage on cnten of aux_clk and frame_clk gating logic
8	0h RO	**Reserved**
7	0h RW	**Frame Timer Clock Gating Ports in U2 Enable (FTCGPU2E):** This bit, when set, allows Host Controller to gate the clock to the Frame Timer when ports are in U2.
6	0h RW	**USB2 port clock throttle enable (USB2_PC_TE):** When set, allows the Aux clock into the USB2 ports to be throttled when conditions allow.
5	1h RW	**XHCI Engine Aux clock gating enable (XHCI_AC_GE):** When set, allows the aux clock into the XHCI engine to be gated when idle. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
4	1h RW	**XHCI Aux PM block clock gating enable (XHCI_APMB_CGE):** When set, allows the aux clock into the Aux PM block to be gated when idle. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
3	1h RW	**USB3 Aux Clock Trunk Gating Enable (USB3_AC_TGE):** When set, allows Aux Clock Trunk feeding to USB3.0 ports to be gated when port Aux clock is gated at all USB3.0 ports and all USB3.0 modPHY instances. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
2	1h RW	**USB3 Port Aux/Port clock gating enable (USB3_AP_CGE):** When set, allows the aux_pclk clock into the USB3 port to be gated when conditions are met. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
1	0h RW	**ModPHY port Aux clock gating enable in U2 (MPP_AC_GEU2):** When set, allows the aux clock into the ModPhy to be gated when Link is in U2 and pipe has been in PS3 for at least the time defined by U2 Residency Before ModPHY Clock Gating field. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
0	0h RW	**ModPHY port Aux clock gating enable in Disconnected, U3 or Disabled (MPP_AC_GE_DDU3):** When set, allows the aux clock into the ModPHY to be gated when Link is in Disconnected, U3 or Disabled state. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.

10.2.187 XHC Latency Tolerance Parameters LTV Control (XLTP_LTV1) — Offset 8174h

XHC Latency Tolerance Parameters LTV Control

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8174h	01400C01h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Disable scheduler direct transition from IDLE to NO requirement (DIS_SDT_IDL_NR):** 0: (default) allow scheduler direct transition from IDLE to NO requirement 1: Disable scheduler direct transition from IDLE to NO requirement
30	0h RW	**XHCI LTR Transition Policy (XLTRTP) (LTR_TRANS_POL):** When 0, the LTR messaging state machine transitions through High Med Low Active states assuming enough latency is available for each transition. When 1, LTR messaging state machine transitions from High, Medium, or Low LTR states to Active state upon the Alarm Timer timeout and stays in Active until the next service boundary.
29	0h RW	**Include Scheduler First Round in Active Signal Disable (INCL_ROUND1_DIS):** 0: xHC Engine Idle from the Power Scheduler will not assert if the Scheduler is performing its first round pass through periodic endpoints. 1: Revert to previous behavior. Scheduler's first round checks not included in xHC Engine Idle equation.
28	0h RW	**XHCI LTR Active Enable (XLTRAE) (XLTRAE):** 0: The Power Scheduler will not request an LTR message on a transition to ACTIVE. 1: The Power Scheduler will request an LTR message on a transition to ACTIVE.
27	0h RW	**Power Scheduler Local Clock Gating Enable (PWRLCGE) (PWRLCGE):** 0: Power Scheduler does not use local clock gating 1: Power Scheduler's local clock gating enabled. Note: This functionality is no longer required. This LCG existed previous to the inclusion of Aux clock gating.
26	0h RW	**LTR EVM Hysteresis Max Count (LTR_HYS_MAX):** Power Scheduler's Periodic IDLE residency before we assert Periodic Complete 0: Hysteresis set to 127 clock ticks. (.64us) 1: Hysteresis set to 31 clock ticks (.16us)
25	0h RW	**Enable USB2 Port L0 LTV based on active async (EN_USB2_LTV_U0_PORT_ASYNC_ACTIVE):** 0 - USB2 Port L0 LTV is used regardless of whether there is active async EPs being present or not (Legacy mode) 1 - USB2 LTR L0 LTV is used only when there is active async EPs being present on that port. In the absence of active async EPs on given port, the L0 LTR value is NoRequirement for that port.
24	1h RW	**XHCI LTR Enable (XLTRE):** This bit must be set to enable LTV messaging from XHCI to the PMC.

Bit Range	Default & Access	Field Name (ID): Description
23:12	400h RW	**Periodic Active LTV (PA_LTV):** 23:22 Latency Scale 00b : Reserved 01b : Latency Value to be multiplied by 1024 10b : Latency Value to be multiplied by 32,768 11b : Latency Value to be multiplied by 1,048,576 21:12 Latency Value (ns) Defaults to 0 micro seconds
11:0	C01h RW	**USB2 Port L0 LTV (USB2_PL0_LTV):** 11:10 Latency Scale 00b : Reserved 01b : Latency Value to be multiplied by 1024 10b : Latency Value to be multiplied by 32,768 11b : Latency Value to be multiplied by 1,048,576 9:0 Latency Value (ns) Defaults to 128 Micro Seconds

10.2.188 XHC Latency Tolerance Parameters LTV Control 2 (XLTP_LTV2) — Offset 8178h

XHC Latency Tolerance Parameters LTV Control 2

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8178h	000017FFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RW	**Enable Sending Zero LTR message based on run125 (RUN125_IN_LTR_EN):** When set, LTR manager will send Zero LTR message upon run125 assertion. And, recomputes and send another LTR upon run125 deassertion
16	0h RW	**Non Offload Active Periodic TTE Counter Clearing Disable (NONOFLD_ACTV_PRDC_TTE_CNT_CLR_DIS):** Setting this bit will disable clearing Non-offload active periodic TTE counter based on TTE Idle indicator
15	0h RW	**xHC Engine active Propogation into ux_pmcm_run125 (ENAB_NON_DMA_ENGINE_ACTIVE):** This register enables/disables the non DMA related memory traffic to PMC via the xHC active indication. 0 - xHC Engine non DMA active is NOT propogated to PMC 1 - xHC Engine non DMA active is propogated to PMC

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Audio Offload USB2 Resume to DMA Active Mapping Enable (ADO_USB2RES_DMAACTV_MAP_EN):** Enables USB2 Port Resume Influence on 'XHCI DMA Active' indication (i.e. Run 125) for Ports Handling Audio Offload. 0 - A USB2 port involved with Audio Offload will NOT influence the XHCI DMA Active indication through USB2 Resume (i.e. USB2 resume for the associated port is not consumed when generating XHCI DMA Active). 1 - A USB2 port involved with Audio Offload will influence (legacy mode) the XHCI DMA Active indication through USB2 Resume (i.e. USB2 resume for the associated port is not consumed when generating XHCI DMA Active). Note: When this field is '0' will allow for a different field to determine what constitutes Audio Offload involvemen The different field is located at 0x8174[13]
13	0h RW	**Audio Offload USB2 Resume to DMA Active Mask Policy (ADO_USB2RES_DMAACTV_MASK_POLICY):** Defines the conditions required for what constitutes Audio Offload involvement for appropriate masking of USB2 Resume on 'XHCI DMA Active' indication (i.e. Run 125) for Ports Handling Audio Offload. 0 - Mask USB2 Resume from asserting the XHCI DMA Active if the particular port going through resume is engaged in Audio Offload while an Audio Offload DB is active (i.e. Audio Offload is connected and active). 1 - Mask USB2 Resume from asserting the XHCI DMA Active if the particular port going through resume is engaged in Audio Offload (i.e. Audio Offload is connected) irrespective of a DB being active/idle.
12:0	17FFh RW	**LTV Limit (LTV_LMT):** This register defines a maximum LTR value that is allowed to be advertised to the PMC. This is meant to be used as a mitigation if issues are discovered with the LTR values generated by the XHC using the defined algorithms. If the LTR value of the XHC is larger than the value in this register field, the value in this field is sent to the PMC instead. Default value is the highest possible - 101b 12:10: Latency Multiplier Field 000b - Value times 1 ns 001b - Value times 32 ns 010b - Value times 1,024 ns 011b - Value times 32,768 ns 100b - Value times 1,048,576 ns 101b - Value times 33,554,432 ns 110b-111b - Not Permitted 9:0: Latency Value Default = 3FFh

10.2.189 XHC Latency Tolerance Parameters High Idle Time Control (XLTP_HITC) — Offset 817Ch

XHC Latency Tolerance Parameters High Idle Time Control

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 817Ch	00050002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:16	0005h RW	**Minimum High Idle Time (MHIT):** This is the minimum schedule idle time that must be available before a "High" LTR value can be indicated. This value must be larger than HIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)
15:13	0h RO	**Reserved**
12:0	0002h RW	**High Idle Wake Latency (HIWL):** This is the latency to access memory from the High Idle Latency state. This value must be larger than MIWL and LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)

10.2.190 XHC Latency Tolerance Parameters Medium Idle Time Control (XLTP_MITC) — Offset 8180h

XHC Latency Tolerance Parameters Medium Idle Time Control

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8180h	00050002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
28:16	0005h RW	**Minimum Medium Idle Time (MMIT):** This is the minimum schedule idle time that must be available before a "Medium" LTR value can be indicated. This value must be larger than MIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)
15:13	0h RO	**Reserved**
12:0	0002h RW	**Medium Idle Wake Latency (MIWL):** This is the latency to access memory from the Medium Idle Latency state. This value must be larger than LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)

10.2.191 XHC Latency Tolerance Parameters Low Idle Time Control (XLTP_LITC) — Offset 8184h

XHC Latency Tolerance Parameters Low Idle Time Control

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8184h	00050002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:16	0005h RW	**Minimum Low Idle Time (MLIT):** This is the minimum schedule idle time that must be available before a "Low" LTR value can be indicated. This value must be larger than LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)
15:13	0h RO	**Reserved**
12:0	0002h RW	**Low Idle Wake Latency (LIWL):** This is the latency to access memory from the Medium Idle Latency state. 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)

10.2.192 LFPS On Count (LFPSONCOUNT_REG) — Offset 81B8h

LFPS On Count

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 81B8h	000420C8h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22	0h RW	**EN LFPS RX CONSOLIDATION (EN_LFPS_RX_CONSOLIDATION):** When set, port will start comprehending LFPS on either of lane for the Resume Exits
21	0h RW	**RTC Clock Generation Override (RTCCLKGENOVERRIDE):** when set it will Disable the RTC tick generation unconditionally.This will be used by software to disable the tick and CRO if WDE/WCE is disabled du ring D3
20	0h RW	**Disable U3 Wait for Ownership (DISABLE_U3_WAIT_FOROWNERSHIP):** When set will allow Gated SS Link to send the LFPS even though AON owns the LFPS detection
19	0h RW	**Rx LFPS Filter 8us Enable (RXLFPSFILT_8US_EN):** 0- RXLFPS detection filter for U3 Exit is 4 ticks of 128ns 1- RXLFPS Filter will remain at 8us
18	1h RW	**Disable RTC Polling (XDISRTCPOLLING):** 1: Disable the RTC tick generation which is consumed for the RxDet Polling, LFPS Polling and Aux Clock PCG Wakup to enable this. 0: RTC tick generation based on the defined interval
17:16	0h RW	**U2P3 LFPS Periodic Sampling Control (XU2P3LPSC):** This field controls the OFF time for the LFPS periodic sampling for SS and SSIC ports in U2P3. If LFPSPM for a port is 1, it will override the OFF time and LFPS receiver will remain OFF permanently. For Fast Sim mode, 500us will be equivalent to 5us. 0x0 Polling Disable. (RXDET Polling will become 100ms.) 0x1 500us OFF Time 0x2 1ms OFF Time 0x3 1.5ms OFF Time
15:10	08h RW	**X LFPS On Count SSIC (XLFPSONCNTSSIC):** This time would describe the number of clocks SSIC LFPS will remain ON. SSIC LFPS detection operation may be carried out on using RTC clock or Oscillator clock. The value of this register should be adjusted accordingly. For RTC recommended value is 2. For Oscillator clock, recommended value is 8.
9:0	0C8h RW	**X LFPS On Count SS (XLFPSONCNTSS):** This time would describe the number of clocks LFPS will remain ON. LFPS detection operation may be carried out on using RTC clock or Oscillator clock. The value of this register should be adjusted accordingly. For RTC recommended value is 2. For Oscillator clock, recommended value is 200.

10.2.193 USB2 Power Management Control (USB2PMCTRL_REG) — Offset 81C4h

USB2 Power Management Control

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 81C4h	00822908h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RF PG Fix Disable (DIS_RFPGFIX):** 0 - Enable RF Power gating fix (Default) 1 - Disable RF Power gating fix
30:25	0h RO	**Reserved**
24	0h RW	**SNPS PHY OPMODE Normal Enable (SNPSPHYOPNORMEN):** 1: Enables OPMODE == Normal during suspendm/sleepm assertion 0: OPMODE == Disable Bit Stuff/NRZI during suspendm/sleepm assertion
23	1h RW	**SNPS PHY Resume Bypass Path Disable (SNPSPHYRESBYPDIS):** 1: Disables the resume signaling through the bypass path 0: Enables the resume signaling through the bypass path
22:21	0h RW	**L1 Timeout Override (L1TOUTOVR):** Overrides and ignores SW programmed values for L1 Timeout on all ports to 11: 60 us 10: 40 us 01: 20 us 00: Accepts L1 Timeout value from SW (no override)
20	0h RW	**L1 BESL/BESLD Override (L1BESLOVR):** 1: Overrides BESL/BESLD to zero on all ports and ignores SW programmed values 0: Accept BESL/BESLD values from SW (no override)
19	0h RW	**Disable RTC Sus Power Gating Control (DISRTCSPGC):** 1: Disables the RTC Sus PG SM from asserting sus_pwr_req to PMC, legacy path is used instead 0: Enables the RTC Sus PG SM to assert sus_pwr_req to PMC
18:16	2h RW	**L1 USB2 PLL Spin Up Time (L1USB2PLLSUT):** 111: 70us 110: 60us ... 001: 10us 000: 0us
15	0h RO	**Reserved**
14	0h RW	**RTC Resume Disable (DIS_RTCRSM):** 1: When set, RTC resume will be disable and fallback to use portmgr for resumes 0: When cleared, RTC resume will take over portmgr's U3 resume

Bit Range	Default & Access	Field Name (ID): Description
13	1h RW	**Bypass Suspend SM (BYPSUSSM):** 1: When set, Suspend SM is bypassed and L1/L2 suspendm from the controller goes directly to the PHY 0: When cleared, Suspend SM controls the L1/L2 suspendm to the PHY
12	0h RW	**USB2 HOST PHY UTMI Clock Gate Disable Policy (U2HPUCGDP):** This controls the policy for Host PHY UTMI Clock Gating. When Set HOST PHY UTMI Clock Gating is disabled else Host PHY UTMI Clock Gating is enable
11	1h RW	**USB2 PHY SUS Power Gate PORTSC Block Policy (U2PSPGPSCBP):** This controls the policy for blocking PORTSC Updates while the USB2 PHY SUS Well is power gated. When set, the controller will block any updates to the PORTSC caused by port status change if the USB2 PHY SUS is power gated. 0 Do not
10:8	1h RW	**USB2 PHY SUS Well Power Gate Entry Hysteresis Count (U2PSPGEHC):** This controls the amount of hysteresis time the controller will enforce after detecting the USB2 PHY SUS Power Gate entry condition. 0h 0 clocks 1h 32 clocks 2h 64 clocks 3h 128 clocks 4h 256 clocks 5h 512 clocks 6h 1024 clocks 7h 2048 clocks
7:4	0h RW	**USB2 PHY SUS Power Gate PORTSC Block Policy (U2CLPGLAT):** This field represents the worst case latency for the USB2 Common Lane to enter and exit its power gate state. This fields is required to be compared to a ports HIRD/HIRD value for the ports that have allowed L1 to L2 mapping to determine if the Common Lane can be allowed to power off. If the power gate entry/exit latency is greater than the HIRD/HIRDD then the common lane should not be allowed to power gate as this will result in a L1 exit violation. 0h 100 us 1h 200 us 2h 300 us Eh 1500us Fh 1600 us
3:2	2h RW	**USB2 PHY SUS Well Power Gate Policy (U2PSUSPGP):** This field controls when to enable the USB2 PHY SUS Well Power Gating when the proper conditions are met. 00 USB2 PHY SUS Power Gating is Disabled. 01 USB2 PHY SUS Power Gating is Enabled in Only D0 and D0i2 (Excludes D0i3 and D3) 10 USB2 PHY SUS Power Gating is Eanabled in only in D0, D0i2 and D0i3 (Excludes D3) 11 USB2 PHY SUS Power Gating is Eanabled in D0/D0i2/D0i3/D3
1:0	0h RO	**Reserved**

10.2.194 USB Legacy Support Capability (USBLEGSUP) — Offset 846Ch

This register is modified and maintained by BIOS

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 846Ch	00002201h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**HC OS Owned Semaphore (HCOSOS):** HC OS Owned Semaphore
23:17	0h RO	**Reserved**
16	0h RW	**HC BIOS Owned Semaphore (HCBIOSOS):** HC BIOS Owned Semaphore
15:8	22h RW/L	**Next Capability Pointer (NEXTCP):** Next Capability Pointer **Locked by:** XHCC1.ACCTRL
7:0	01h RW/L	**Capability ID (CID):** Capability ID **Locked by:** XHCC1.ACCTRL

10.2.195 USB Legacy Support Control Status (USBLEGCTLSTS) — Offset 8470h

USB Legacy Support Control Status

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8470h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**SMI on BAR (SMIBAR):** SMI on BAR

Bit Range	Default & Access	Field Name (ID): Description
30	0h RW/1C	**SMI on PCI Command (SMIPCIC):** SMI on PCI Command
29	0h RW/1C	**SMI on OS Ownership Change (SMIOSOC):** SMI on OS Ownership Change
28:21	0h RO	**Reserved**
20	0h RO	**SMI on Host System Error (SMIHSE):** SMI on Host System Error
19:17	0h RO	**Reserved**
16	0h RO	**SMI on Event Interrupt (SMIEI):** SMI on Event Interrupt
15	0h RW	**SMI on BAR Enable (SMIBARE):** SMI on BAR Enable
14	0h RW	**SMI on PCI Command Enable (SMIPCICE):** SMI on PCI Command Enable
13	0h RW	**SMI on OS Ownership Enable (SMIOSOE):** SMI on OS Ownership Enable
12:5	0h RO	**Reserved**
4	0h RW	**SMI on Host System Error Enable (SMIHSEE):** SMI on Host System Error Enable
3:1	0h RO	**Reserved**
0	0h RW	**USB SMI Enable (USBSMIE):** USB SMI Enable

10.2.196 Port Disable Override Capability Register (PDO_CAPABILITY) — Offset 84F4h

Port Disable Override Capability Register

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 84F4h	000003C6h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	03h RW/L	**Next Capability Pointer (NCP):** Next Capability Pointer **Locked by:** XHCC1.ACCTRL

Bit Range	Default & Access	Field Name (ID): Description
7:0	C6h RW/L	**Capability ID (CID):** Capability ID **Locked by:** XHCC1.ACCTRL

10.2.197 Command Reg (CMD_MMIO) — Offset 8604h

Type	Size	Offset	Default
MMIO	16 bit	MBAR + 8604h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable (INTR_DIS):** When cleared to 0, the function is capable of generating interrupts. When 1, the function can not generate its interrupt to the interrupt controller. Note that the corresponding Interrupt Status bit is not affected by the interrupt enable.
9	0h RO	**Fast Back to Back Enable (FBE):** Fast Back to Back Enable
8	0h RW	**SERR Enable (SERR):** When set to 1, the XHC is capable of generating (internally) SERR#.
7	0h RO	**Wait Cycle Control (WCC):** Wait Cycle Control
6	0h RW	**Parity Error Response (PER):** When set to 1, the XHCI Host Controller will check for correct parity (on its internal interface) and halt operation when bad parity is detected during the data phase as recommended by the XHCI specification. Note that this applies to both requests and completions from the system interface. This bit must be set in order for the parity errors to generate SERR#.
5	0h RO	**VGA Palette Snoop (VPS):** VGA Palette Snoop
4	0h RO	**Memory Write Invalidate (MWI):** Memory Write Invalidate
3	0h RO	**Special Cycle Enable (SCE):** Special Cycle Enable
2	0h RW	**Bus Initiator Enable (BME):** When set, it allows XHC to act as a bus initiator. When cleared, it disable XHC from initiating transactions on the system bus.
1	0h RW	**Memory Space Enable (MSE):** This bit controls access to the XHC Memory Space registers. If this bit is set, accesses to the XHC registers are enabled. The Base Address register for the XHC should be programmed before this bit is set.
0	0h RO	**I/O Space Enable (IOSE):** Reserved

10.2.198 Device Status (STS_MMIO) — Offset 8606h

Device Status

Type	Size	Offset	Default
MMIO	16 bit	MBAR + 8606h	0290h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**Detected Parity Error (DPE):** This bit is set by the PCH whenever a parity error is seen on the internal interface to the XHC host controller, regardless of the setting of bit 6 or bit 8 in the Command register or any other conditions. Software clears this bit by writing a 1 to this bit location.
14	0h RW/1C	**Signaled System Error (SSE):** This bit is set by the PCH whenever it signals SERR# (internally). The SERR_EN bit (bit 8 in the Command Register) must be 1 for this bit to be set.
13	0h RW/1C	**Received Initiator-Abort Status (RMA):** This bit is set when XHC, as a initiator, receives a initiator-abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location.
12	0h RW/1C	**Received Target Abort Status (RTA):** This bit is set when XHC, as a initiator, receives a target abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location.
11	0h RW/1C	**Signaled Target-Abort Status (STA):** This bit is used to indicate when the XHC function responds to a cycle with a target abort.
10:9	1h RO	**DEVSEL Timing Status (DEVT):** This 2-bit field defines the timing for DEVSEL# assertion. Read-Only.
8	0h RW/1C	**Initiator Data Parity Error Detected (MDPED):** This bit is set by the PCH whenever a data parity error is detected on a XHC read completion packet on the internal interface to the XHC host controller and bit 6 of the Command register is set to 1. Software clears this bit by writing a 1 to this bit location.
7	1h RO	**Fast Back-to-Back Capable (FBBC):** Reserved
6	0h RO	**User Definable Features (UDF):** Reserved
5	0h RO	**66 MHz Capable (MC):** Reserved
4	1h RO	**Capabilities List (CL):** Hardwired to 1 indicating that offset 34h contains a valid capabilities pointer.
3	0h RO/V	**Interrupt Status (INTR_STS):** This read-only bit reflects the state of this function's interrupt at the input of the enable/disable logic. This bit is a 1 when the interrupt is asserted. This bit will be 0 when the interrupt is deasserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.

Bit Range	Default & Access	Field Name (ID): Description
2:0	0h RO	**Reserved**

10.2.199 Revision ID (RID_MMIO) — Offset 8608h

Revision ID

Type	Size	Offset	Default
MMIO	8 bit	MBAR + 8608h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO/V	**Revision ID (RID):** See Chap 6 for value.

10.2.200 Programming Interface (PI_MMIO) — Offset 8609h

Programming Interface

Type	Size	Offset	Default
MMIO	8 bit	MBAR + 8609h	30h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	30h RO	**Programming Interface (PI):** A value of 30h indicates that this USB Host Controller conforms to the XHCI specification.

10.2.201 Sub Class Code (SCC_MMIO) — Offset 860Ah

Sub Class Code

Type	Size	Offset	Default
MMIO	8 bit	MBAR + 860Ah	03h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	03h RO	**Sub Class Code (SCC):** A value of 03h indicates that this is a Universal Serial Bus Host Controller.

10.2.202 Base Class Code (BCC_MMIO) — Offset 860Bh

Base Class Code

Type	Size	Offset	Default
MMIO	8 bit	MBAR + 860Bh	0Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	0Ch RO	**Base Class Code (BCC):** A value of 0Ch indicates that this is a Serial Bus controller.

10.2.203 Cache Line Size (CLS_MMIO) — Offset 860Ch

Cache Line Size

Type	Size	Offset	Default
MMIO	8 bit	MBAR + 860Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Cache Line Size (CLS):** Cache Line Size

10.2.204 Initiator Latency Timer (MLT_MMIO) — Offset 860Dh

Initiator Latency Timer

Type	Size	Offset	Default
MMIO	8 bit	MBAR + 860Dh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**Initiator Latency Timer (MLT):** Because the XHC controller is internally implemented with arbitration on an internal interface, it does not need a initiator latency timer. The bits will be fixed at 0.

10.2.205 Header Type (HT_MMIO) — Offset 860Eh

Header Type

Type	Size	Offset	Default
MMIO	8 bit	MBAR + 860Eh	80h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Multi-Function Bit (MFB):** Read only indicating single function device.
6:0	00h RO	**Configuration layout (CL):** Hardwired to 0 to indicate a standard PCI configuration layout.

10.2.206 Memory Base Address (MBAR_MMIO) — Offset 8610h

Type	Size	Offset	Default
MMIO	64 bit	MBAR + 8610h	0000000000000004h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:16	00000000 0000h RW	**Base Address (BA):** Bits (63:16) correspond to memory address signals (63:16), respectively. This gives 64 KB of relocatable memory space aligned to 64 KB boundaries.
15:4	0h RO	**Reserved**
3	0h RO	**Prefetchable Indication (PREFETCHABLE):** This bit is hardwired to 0 indicating that this range should not be prefetched.
2:1	2h RO	**Type Indication (MBAR_TYPE):** If this field is hardwired to 00 it indicates that this range can be mapped anywhere within 32-bit address space. If this field is hardwired to 10 it indicates that this range can be mapped anywhere within 64-bit address space.
0	0h RO	**Resource Type Indicator (RTE):** This bit is hardwired to 0 indicating that the base address field in this register maps to memory space

10.2.207 USB Subsystem Vendor ID (SSVID_MMIO) — Offset 862Ch

Type	Size	Offset	Default
MMIO	16 bit	MBAR + 862Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/L	**USB Subsystem Vendor ID (SSVID):** This register, in combination with the USB Subsystem ID register, enables the operating system to distinguish each subsystem from the others.

10.2.208 USB Subsystem ID (SSID_MMIO) — Offset 862Eh

Type	Size	Offset	Default
MMIO	16 bit	MBAR + 862Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/L	**USB Subsystem ID (SSID):** BIOS sets the value in this register to identify the Subsystem ID. This register, in combination with the Subsystem Vendor ID register, enables the operating system to distinguish each subsystem from other(s).

10.2.209 Capabilities Pointer (CAP_PTR_MMIO) — Offset 8634h

This register points to the starting offset of the capabilities ranges.

Type	Size	Offset	Default
MMIO	8 bit	MBAR + 8634h	70h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	70h RO	**Capabilities Pointer (CAP_PTR):** This register points to the starting offset of the capabilities ranges.

10.2.210 Interrupt Line (ILINE_MMIO) — Offset 863Ch

Type	Size	Offset	Default
MMIO	8 bit	MBAR + 863Ch	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Interrupt Line (ILINE):** This data is not used by the PCH. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to.

10.2.211 Interrupt Pin (IPIN_MMIO) — Offset 863Dh

Type	Size	Offset	Default
MMIO	8 bit	MBAR + 863Dh	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW/L	**Interrupt pin (IPIN):** Bits 7:0 reflect the Interrupt Pin assigned to the host controller by the platform (and are hardwired). **Locked by:** XHCC1.ACCTRL

10.2.212 Serial Bus Release Number (SBRN_MMIO) — Offset 8660h

Serial Bus Release Number

Type	Size	Offset	Default
MMIO	8 bit	MBAR + 8660h	32h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	32h RW/L	**Serial Bus Release Number (SBRN):** A value of 32h indicates that this controller follows USB release 3.2. **Locked by:** XHCC1.ACCTRL

10.2.213 Frame Length Adjustment (FLADJ_MMIO) — Offset 8661h

This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written into these six bits, the length of the frame is adjusted. Its initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system BIOS. This register

should only be modified when the HChalted bit in the USBSTS register is a one. Changing value of this register while the host controller is operating yields undefined results.

Type	Size	Offset	Default
MMIO	8 bit	MBAR + 8661h	60h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6	1h RO	**No Frame Length Timing Capability (NO_FRAME_LENGTH_TIMING_CAP):** This flag is set to 1 to indicate that the host controller does not support a programmable Frame Length Timing Value field.
5:0	20h RO	**Frame Length Timing Value (FLTV):** SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (number of High Speed bit times) FLADJ Value (decimal) (decimal) 59488 0 (00h) 59504 1 (01h) 59520 2 (02h) ... 59984 31 (1Fh) 60000 32 (20h) ... 60480 62 (3Eh) 60496 63 (3Fh) Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (# High Speed bit times) FLADJ Value

10.2.214 Best Effort Service Latency (BESL_MMIO) — Offset 8662h

Type	Size	Offset	Default
MMIO	8 bit	MBAR + 8662h	00h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RW/L	**Default Best Effort Service Latency Deep (DBESLD):** Default Best Effort Service Latency (DBESLD) If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESLD field. This is programmed by BIOS based on platform parameters. **Locked by:** XHCC1.ACCTRL
3:0	0h RW/L	**Default Best Effort Service Latency (DBESL):** If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESL field. This is programmed by BIOS based on platform parameters. **Locked by:** XHCC1.ACCTRL

10.2.215 PCI Power Management Capability ID (PM_CID_MMIO) — Offset 8670h

PCI Power Management Capability ID

Type	Size	Offset	Default
MMIO	8 bit	MBAR + 8670h	01h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	01h RO	**PCI Power Management Capability ID (PM_CID):** A value of 01h indicates that this is a PCI Power Management capabilities field.

10.2.216 Next Item Pointer 1 (PM_NEXT_MMIO) — Offset 8671h

Type	Size	Offset	Default
MMIO	8 bit	MBAR + 8671h	80h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	80h RW/L	**Next Item Pointer 1 (PM_NEXT):** This register defaults to 80h, which indicates that the next capability registers begin at configuration offset 80h. This register is writable when the Access Control bit is set to '0'. This allows BIOS to effectively hide the next capability registers, if necessary. This register should only be written during system initialization before the plug-and-play software has enabled any initiator-initiated traffic. Values of: 80h implies next capability is MSI 00h implies that MSI capability is hidden. Note: This value is never expected to be programmed. **Locked by:** XHCC1.ACCTRL

10.2.217 Power Management Capabilities (PM_CAP_MMIO) — Offset 8672h

Normally, this register is read-only to report capabilities to the power management software. In order to report different power management capabilities depending on the system in which the PCH is used, the write access to this register is controlled by the Access Control bit (ACCTRL). The value written to this register does not affect the hardware other than changing the value returned during a read.

This register is modified and maintained by BIOS

Type	Size	Offset	Default
MMIO	16 bit	MBAR + 8672h	C1C2h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:11	18h RW/L	**PME Support (PME_SUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. The PCH XHC does not support the D1 or D2 states. For all other states, the PCH XHC is capable of generating PME#. Software should never need to modify this field.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/L	**D2 Support (D2_SUPPORT):** The D2 state is not supported. **Locked by:** XHCC1.ACCTRL
9	0h RW/L	**D1 Support (D1_SUPPORT):** The D1 state is not supported. **Locked by:** XHCC1.ACCTRL
8:6	7h RW/L	**Aux Current (AUX_CURRENT):** The PCH XHC reports 375mA maximum Suspend well current required when in the D3cold state. This value can be written by BIOS when a more accurate value is known. **Locked by:** XHCC1.ACCTRL
5	0h RW/L	**Device Specific Initialization (DSI):** The PCH reports 0, indicating that no device-specific initialization is required. **Locked by:** XHCC1.ACCTRL
4	0h RO	**Reserved**
3	0h RW/L	**PME Clock (PMECLOCK):** The PCH reports 0, indicating that no PCI clock is required to generate PME#. **Locked by:** XHCC1.ACCTRL
2:0	2h RW/L	**Version Indication (VERSION):** The PCH reports 010, indicating that it complies with Revision 1.1 of the PCI Power Management Specification. **Locked by:** XHCC1.ACCTRL

10.2.218 Power Management Control/Status (PM_CS_MMIO) — Offset 8674h

Type	Size	Offset	Default
MMIO	16 bit	MBAR + 8674h	0008h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**PME Status (PME_STATUS):** This bit is set when the PCH XHC would normally assert the PME# signal independent of the state of the PME_En bit. Writing a 1 to this bit will clear it and cause the internal PME to deassert (if enabled). Writing a 0 has no effect. This bit must be explicitly cleared by the operating system each time the operating system is loaded.
14:13	0h RO	**Data Scale (DATA_SCALE):** The PCH hardwires these bits to 00 because it does not support the associated Data register.
12:9	0h RO	**Data Select (DATA_SELECT):** The PCH hardwires these bits to 0000 because it does not support the associated Data register.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**PME Enable (PME_EN):** A 1 enables the PCH XHC to generate an internal PME signal when PME_Status is 1. This bit must be explicitly cleared by the operating system each time it is initially loaded.
7:4	0h RO	**Reserved**
3	1h RW/L	**No Soft Reset (NSR):** No_Soft_Reset - When set ("1"), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. Transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled. **Locked by:** XHCC1.ACCTRL
2	0h RO	**Reserved**
1:0	0h RW	**Power State (POWERSTATE):** This 2-bit field is used both to determine the current power state of XHC function and to set a new power state. The definition of the field values are: 00b - D0 state 11b - D3hot state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally, however, the data is discarded and no state change occurs. When in the D3hot state, the PCH must not accept accesses to the XHC memory range, but the configuration space must still be accessible.

10.2.219 Message Signaled Interrupt CID (MSI_CID_MMIO) — Offset 8680h

Message Signaled Interrupt CID

Type	Size	Offset	Default
MMIO	8 bit	MBAR + 8680h	05h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
7:0	05h RO	**Capability ID (CID):** Indicates that this is an MSI capability

10.2.220 Next Item Pointer (MSI_NEXT_MMIO) — Offset 8681h

Type	Size	Offset	Default
MMIO	8 bit	MBAR + 8681h	90h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
7:0	90h RW/L	**Next Pointer (NEXT_POINTER):** Indicates that this is the last item on the capability list **Locked by:** XHCC1.ACCTRL

10.2.221 Message Signaled Interrupt Message Control (MSI_MCTL_MMIO) — Offset 8682h

Type	Size	Offset	Default
MMIO	16 bit	MBAR + 8682h	0086h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	**Reserved**
8	0h RO	**Per-Vector Masking Capable (PVM):** Specifies whether controller supports MSI per vector masking. Not supported
7	1h RO	**64 Bit Address Capable (C64):** Specifies whether capable of generating 64-bit messages. This device is 64-bit capable.
6:4	0h RW	**Multiple Message Enable (MME):** Indicates the number of messages the controller should assert. This device supports multiple message MSI.
3:1	3h RO	**Multiple Message Capable (MMC):** Indicates the number of messages the controller wishes to assert. This field must be set by HW to reflect the number of Interrupters supported. Encoding number of Vectors requested (number of Interrupters) 000 1 001 2 010 4 011 8 100 16 101 32 110-111 Reserved

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**MSI Enable (MSIE):** If set to 1, MSI is enabled and the traditional interrupt pins are not used to generate interrupts. If cleared to 0, MSI operation is disabled and the traditional interrupt pins are used.

10.2.222 Message Signaled Interrupt Message Address (MSI_MAD_MMIO) — Offset 8684h

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8684h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**Lower DW Address (ADDR):** Lower DW of system specified message address, always DWORD aligned
1:0	0h RO	**Reserved**

10.2.223 Message Signaled Interrupt Upper Address (MSI_MUAD_MMIO) — Offset 8688h

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8688h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Upper DW Address (UPPERADDR):** Upper DW of system specified message address.

10.2.224 Message Signaled Interrupt Message Data (MSI_MD_MMIO) — Offset 868Ch

Type	Size	Offset	Default
MMIO	16 bit	MBAR + 868Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**Data Field (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD(15:0)) during the data phase of the MSI memory write transaction. The Multiple Message Enable field (bits 6-4 of the Message Control register) defines the number of low order message data bits the function is permitted to modify to generate its system software allocated vectors. For example, a Multiple Message Enable encoding of 010 indicates the function has been allocated four vectors and is permitted to modify message data bits 1 and 0 (a function modifies the lower message data bits to generate the allocated number of vectors). If the Multiple Message Enable field is 000, the function is not permitted to modify the message data.

10.2.225 High Speed Configuration 2 (HSCFG2_MMIO) — Offset 86A4h

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 86A4h	00003800h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW	**PORT1 Host Mode Override (PORT1_HOST_MODE_OVERRIDE):** When set, this bit causes the Host_Device mux on port 1 to be forced into the Host mode.
17:16	0h RW	**EUSB2SEL:** The two bits are associate with USB2 ports 1 - bit 16 and 2 - bit 2 0: Port is mapped to USB2 1: Port is mapped to eUSB2

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**HS ASYNC Active IN Mask (HSAAIM):** Determines if the Async Active will mask/ignore IN EP s. 0 HS ASYNC Active will include IN EP s. 1 HS ASYNC Active will mask/ignore IN EP s.
14	0h RW	**HS OUT ASYNC Active Polling EP Mask (HSOAAPEPM):** Determines if the Async Active for OUT HS/FS/LS masks/ignores EP s that are polling/PINGing (HS) due to NAK. 0 HS OUT ASYNC Active will include EP s that are polling. 1 HS OUT ASYNC Active will mask/ignore EP s that are polling.
13	1h RW	**HS IN ASYNC Active Polling EP Mask (HSIAAPEPM):** Determines if the Async Active for IN HS/FS/LS masks/ignores EP s that are polling due to NAK. 0 HS IN ASYNC Active will include EP s that are polling. 1 HS IN ASYNC Active will mask/ignore EP s that are polling.
12:11	3h RW	**HS INTR IN Periodic Active Policy Control (HSIIPAPC):** Controls how the HS INTR IN periodic active is used to generate the global periodic active. This will determine how the smallest service interval among active EP s and number of active EP s are used. 0 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold OR Numb of EP Threshold values meet the requirement. 1 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold AND Numb of EP Threshold values meet the requirement. 2 Always allow HS INTR EP s to be used in the generation of the global Periodic Active indication. 3 Never allow HS INTR EP s to be used in the generation of the global Periodic Active indicaiton
10:4	00h RW	**HS INTR IN Periodic Active Num of EP Threshold (HSIIPANEPT):** Defines the threshold used to determine if Periodic Acive may include HS/FS/LS INTR IN EP active indication. If there are more than NumEPThreshold active HS/FS/LS INTR EP s then they may be included as part of the periodic active generation.
3:0	0h RW	**HS INTR IN Periodic Active Service Interval Threshold (HSIIPASIT):** Defines the Service Interval threshold used to determine if Periodic Acive will include HS/FS/LS INTR IN EP active indication. If there are any active HS/FS/LS INTR EP s with a service interval less than or equal to this threshold then they may be included as part of the periodic active generation.

10.2.226 Debug Capability ID Register (DCID) — Offset 8700h

This register is modified and maintained by BIOS

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8700h	0005100Ah

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
20:16	05h RW/L	**Debug Capability Event Ring Segment Table Max (DCERSTM):** Note: This register is sticky. **Locked by:** XHCC1.ACCTRL
15:8	10h RW/L	**Next Capability Pointer (NCP):** Note: This register is sticky. **Locked by:** XHCC1.ACCTRL
7:0	0Ah RW/L	**Capability ID (CID):** Note: This register is sticky. **Locked by:** XHCC1.ACCTRL

10.2.227 Debug Capability Doorbell Register (DCDB) — Offset 8704h

Debug Capability Doorbell Register

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8704h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RW	**Doorbell Target (DBTGT):** This field defines the target of the doorbell reference. The table below defines the Debug Capability notification that is generated by ringing the doorbell. Value Definition 0 Data EP 1 OUT Enqueue Pointer Update 1 Data EP 1 IN Enqueue Pointer Update 2:255 Reserved This field returns '0' when read and the value should be treated as undefined by software.
7:0	0h RO	**Reserved**

10.2.228 Debug Capability Event Ring Segment Table Size Register (DCERSTSZ) — Offset 8708h

Debug Capability Event Ring Segment Table Size Register

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8708h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Event Ring Segment Table Size (ERSTS):** This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Debug Capability Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the DCERST Max field in the DCID register Software shall initialize this register before setting the Debug Capability Enable field in the DCCTRL register to '1'.

10.2.229 Debug Capability Event Ring Segment Table Base Address Register (DCERSTBA) — Offset 8710h

Debug Capability Event Ring Segment Table Base Address Register

Type	Size	Offset	Default
MMIO	64 bit	MBAR + 8710h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:4	00000000 0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBAR):** This field defines the high order bits of the start address of the Debug Capability Event Ring Segment Table. Software shall initialize this register before setting the Debug Capability Enable field in the DCCTRL register to '1'.
3:0	0h RO	**Reserved**

10.2.230 Debug Capability Event Ring Dequeue Pointer Register (DCERDP) — Offset 8718h

Debug Capability Event Ring Dequeue Pointer Register

Type	Size	Offset	Default
MMIO	64 bit	MBAR + 8718h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:4	00000000 0000000h RW	**Dequeue Pointer (DQP):** This field defines the high order bits of the 64-bit address of the current Debug Capability Event Ring Dequeue Pointer. Software shall initialize this register before setting the Debug Capability Enable field in the DCCTRL register to '1'.
3	0h RO	**Reserved**
2:0	0h RW	**Dequeue ERST Segment Index (DESI):** This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in.

10.2.231 Debug Capability Control Register (DCCTRL) — Offset 8720h

Debug Capability Event Ring Dequeue Pointer Register

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8720h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Debug Capability Enable (DCE):** Debug Capability Enable
30:24	00h RO	**Device Address (DADDR):** Device Address
23:16	00h RO	**Debug Max Burst Size (DMBS):** LPT-LP USB Debug Device does not support bursting.

Bit Range	Default & Access	Field Name (ID): Description
15:5	0h RO	**Reserved**
4	0h RW/1C	**DbC Run Change (DRC):** DbC Run Change
3	0h RW/1S	**Halt IN TR (HIT):** Halt IN TR
2	0h RW/1S	**Halt OUT TR (HOT):** Halt OUT TR
1	0h RW	**Link Status Event Enable (LSE):** Link Status Event Enable
0	0h RO	**DbC Run (DCR):** DbC Run

10.2.232 Debug Capability Status Register (DCST) — Offset 8724h

Debug Capability Status Register

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8724h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Debug Port Number (DPNUM):** This field provides the ID of the Root Hub port that the Debug Capability has been automatically attached to. The value is '0' when the Debug Capability is not attached to a Root Hub port.
23:1	0h RO	**Reserved**
0	0h RO	**Event Ring Not Empty (ERNE):** When '1', this field indicates that the Debug Capability Event Ring has a Transfer Event on it. It is automatically cleared to '0' by the xHC when the Debug Capability Event Ring is empty, i.e. the Debug Capability Enqueue Pointer is equal to the Debug Capability Event Ring Dequeue Pointer register.

10.2.233 Debug Capability Port Status And Control Register (DCPORTSC) — Offset 8728h

Debug Capability Port Status And Control Register

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8728h	00000080h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW/1C	**USB3-Port Config Error Change. USB2-Reserved for USB2 Debug Capability (CEC):** USB3-This flag indicates that the port failed to configure its link partner. 0 = No change. 1 = Port Config Error detected. Software shall clear this bit by writing a '1' to it. USB2-This bit shall never be set when operating in USB2 Kernel Debug mode.
22	0h RW/1C	**Port Link Status Change (PLC):** This flag is set to '1' due to the following PLS transitions: U0 -) U3 Suspend signaling detected from Debug Host U3 -) U0 Resume complete Polling -) Disabled Training Error Ux or Recovery -) Inactive Error Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'
21	0h RW/1C	**Port Reset Change (PRC):** This bit is set when reset processing on this port is complete (i.e. a '1' to '0' transition of PR). '0' = No change. '1' = Reset complete.Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'.
20:18	0h RO	**Reserved**
17	0h RW/1C	**Connect Status Change (CSC):** '1' = Change in Current Connect Status. '0' = No change. Indicates a change has occurred in the port's Current Connect Status. The xHC sets this bit to '1' for all changes to the Debug Device connect status, even if system software has not cleared an existing DbC Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, hardware will be "setting" an already-set bit (i.e., the bit will remain '1'). Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'.
16:14	0h RO	**Reserved**
13:10	0h RO	**Port Speed (PSPD):** This field identifies the speed of the port. This field is only relevant when a Debug Host is attached (CCS = '1') in all other cases this field shall indicate Undefined Speed. 0 Undefined Speed 1-15 Protocol Speed ID (PSI) Note: The Debug Capability onlydoes not supports LS, FS, or HS operation.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**Reserved**
8:5	4h RO	**Port Link State (PLS):** This field reflects its current link state. This field is only relevant when a Debug Host is attached (Debug Port Number) '0'). Value Meaning 0 Link is in the U0 State 1 Link is in the U1 State 2 Link is in the U2 State 3 Link is in the U3 State (Device Suspended) 4 Link is in the Disabled State 5 Link is in the RxDetect State 6 Link is in the Inactive State 7 Link is in the Polling State 8 Link is in the Recovery State 9 Link is in the Hot Reset State 15:10 Reserved Note: Transitions between different states are not reflected until the transition is complete.
4	0h RO	**Port Reset (PR):** '1' = Port is in Reset. '0' = Port is not in Reset. This bit is set to '1' when the bus reset sequence as defined in the USB Specification is detected on the Root Hub port assigned to the Debug capability. It is cleared when the bus reset sequence is completed by the Debug Host, and the DbC shall transition to the USB Default state. A '0' to '1' transition of this bit shall clear DCPORTSC PED ('0'). This field is '0' if DCE or CCS are '0'.
3:2	0h RO	**Reserved**
1	0h RW	**Port Enabled/Disabled (PED):** Default = '0'. '1' = Enabled. '0' = Disabled. This flag shall be set to '1' by a '0' to '1' transition of CCS or a '1' to '0' transition of the PR. When PED transitions from '1' to '0' due to the assertion of PR, the port's link shall transition to the Rx.Detect state. This flag may be used by software to enable or disable the operation of the Root Hub port assigned to the Debug Capability. The Debug Capability Root Hub port operation may be disabled by a fault condition (disconnect event or other fault condition, e.g. a LTSSM Polling substate timeout, tPortConfiguration timeout error, etc.), the assertion of DCPORTSC PR, or by software. 0 = Debug Capability Root Hub port is disabled. 1 = Debug Capability Root Hub port is enabled. When the port is disabled (PED = '0') the port's link shall enter the SS.Disabled state and remain there until PED is reasserted ('1') or DCE is negated ('0'). Note that the Root Hub port is remains mapped to Debug Capability while PED = '0'. While PED = '0' the Debug Capability will appear to be disconnected to the Debug Host. Note, this bit is not affected by PORTSC PR bit transitions. This field is '0' if DCE or CCS are '0'.
0	0h RO	**Current Connect Status (CCS):** '1' = A Root Hub port is connected to a Debug Host and assigned to the Debug Capability. '0' = No Debug Host is present. This value reflects the current state of the port, and may not correspond to the value reported by the Connect Status Change (CSC) field in the Port Status Change Event. Port Status Change Event is generated when both PED and CSC are set to 1. This is a change compared to USB3 because for USB2, the Port Speed field is only valid after PED is set to 1, which only happens some time after CSC is set to 1. This flag is '0' if Debug Capability Enable (DCE) is '0'.

10.2.234 Debug Capability Context Pointer Register (DCCP) — Offset 8730h

Debug Capability Context Pointer Register

Type	Size	Offset	Default
MMIO	64 bit	MBAR + 8730h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:4	00000000 0000000h RW	**Debug Capability Context Pointer Register (DCCPR):** This field defines the high order bits of the start address of the Debug Capability Context data structure associated with the Debug Capability. Software shall initialize this register before setting the Debug Capability Enable bit in the Debug Capability Control Register to '1'.
3:0	0h RO	**Reserved**

10.2.235 Fuse and Strap Mirror Capability Register (FUSE_AND_STRAP_MIRROR_CAP_REG) — Offset 8800h

Fuse and Strap Mirror Capability Register.

Note: **NOTE:** Bit definitions are the same as PDO_CAPABILITY, offset 84F4h.

10.2.236 GLOBAL TIME SYNC CAP REG (GLOBAL_TIME_SYNC_CAP_REG) — Offset 8E10h

GLOBAL TIME SYNC CAP REG

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8E10h	000012C9h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	12h RW/L	**Next Capability pointer (NCP):** Next Capability pointer **Locked by:** XHCC1.ACCTRL

Bit Range	Default & Access	Field Name (ID): Description
7:0	C9h RW/L	**Capability ID (CID):** Capability ID **Locked by:** XHCC1.ACCTRL

10.2.237 GLOBAL TIME SYNC CTRL REG (GLOBAL_TIME_SYNC_CTRL_REG) — Offset 8E14h

GLOBAL TIME SYNC CTRL REG

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8E14h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/1S	**Time Stamp Counter Capture Initiate (TIME_STAMP_CNTR_CAPTURE_INITIATE):** SW sets this bit to initiate a time capture. Once the time capture is complete and the time values are valid in the Local and Global time capture registers, HW clears the bit.

10.2.238 MICROFRAME TIME REG (MICROFRAME_TIME_REG) — Offset 8E18h

MICROFRAME TIME REG

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8E18h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:16	0000h RO	**Captured Frame List Current Index/Frame Number (CMFI):** The value in this register is updated in response to sample_now signal. Bits [29:16] reflect state of bits [13:0] of FRINDEX

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	**Reserved**
12:0	0000h RO	**Captured Micro-frame BLIF (CMFB):** The value is updated in response to sample_now signal and provides information about offset within micro-frame. Captured value represents number of 8 high-speed bit time units from start of micro-frame. At the beginning of micro-frame captured value will be 0 and increase to maximum value at the end. Default maximum value is 7499 but it may be changed as result of adjustment done via Bus Interval Adjust (BIA).

10.2.239 Global Time Value (Low Register) (GLOBAL_TIME_LOW_REG) — Offset 8E20h

Global Time Value (Low):

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8E20h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**GLOBAL_TIME_LOW:** Global Time Value (Low):

10.2.240 GLOBAL TIME HI REG (GLOBAL_TIME_HI_REG) — Offset 8E24h

Global Time Value (High):

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8E24h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Global Time Value (High Register) (GLOBAL_TIME_HI):** Global Time Value (High):

10.2.241 Dublin HOST_CTRL_USB3_LOCAL_LPBK_RPTR (HOST_CTRL_USB3_LOCAL_LPBK_RPTR) — Offset 8E60h

This register is updated by BIOS

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8E60h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**USB3 Local Loopback Repeater (CFG_USB3_LOCAL_LPBK_RPTR):** This will set the local loopback in repeater bit (Bit 4) set in Symbol 5 of TS1/TS2. (Bit2 and Bit3 will be controlled by HOST_CTRL_PORT_LINK_REG)

10.2.242 Host Ctrl Usb3 Initiator Loopback Register (HOST_CTRL_USB3_MSTR_LPBK) — Offset 8EC8h

This register is to provide initiator loopback information

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8EC8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**USB3 Initiator Loopback (CFG_USB3_MSTR_LPBK_EN):** This will set the Initiator Loopback Bit (Bit 2) set in Symbol 5 of TS1/TS2.

10.2.243 Host Ctrl Usb3 Blr Comp Register (HOST_CTRL_USB3_BLR_COMP) — Offset 8ECCh

This register is to provide initiator loopback information

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8ECCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**USB3 BLR COMP (CFG_USB3_BLR_COMP):** This will set the Initiator Loopback Bit (Bit 5) set in Symbol 5 of TS1/TS2.

10.2.244 Host Ctrl Ssp Dis Register (HOST_CTRL_SSP_DIS) — Offset 8ED0h

This register is to disable ssp capability of usb3 link

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 8ED0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**SSP Disable (CFG_SSP_DIS):** When set, it will disable the SSP protocol preventing the XHCI to transmit SCD.

10.2.245 XHCI USB2 Overcurrent Pin Mapping (U2OCM1) — Offset 90A4h

The RW/L property of this register is controlled by OCCFDONE bit.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 90A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/L	**OC Mapping (OCM):** USB2 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB2 std. port 1 Bit 1 maps the OC pin N to USB2 std port 2 ... Bit (NumUSB2std-1) maps the OC pin N to USB2 Std port NumUSB2std Note: The USB-R port which is the most significant USB2 port does not have an OC pin. Thus the OC assignment for the USB-R port is ignored. **Locked by:** XHCC2.OCCFGDONE

10.2.246 XHCI USB2 Overcurrent Pin Mapping (U2OCM2) — Offset 90A8h

The RW/L property of this register is controlled by OCCFDONE bit.

Note: **NOTE:** Bit definitions are the same as U2OCM1, offset 90A4h.

10.2.247 XHCI USB2 Overcurrent Pin Mapping (U2OCM3) — Offset 90ACh

The RW/L property of this register is controlled by OCCFDONE bit.

Note: **NOTE:** Bit definitions are the same as U2OCM1, offset 90A4h.

10.2.248 XHCI USB2 Overcurrent Pin Mapping (U2OCM4) — Offset 90B0h

The RW/L property of this register is controlled by OCCFDONE bit.

Note: **NOTE:** Bit definitions are the same as U2OCM1, offset 90A4h.

10.2.249 XHCI USB3 Overcurrent Pin Mapping (U3OCM1) — Offset 9124h

The RW/L property of this register is controlled by OCCFDONE bit.

Type	Size	Offset	Default
MMIO	32 bit	MBAR + 9124h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW/L	**OC Mapping (OCM):** USB3 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB3 std. port 1 Bit 1 maps the OC pin N to USB3 std. port 2 ... Bit (NumUSB3std-1) maps the OC pin N to USB3 Std port NumUSB3std **Locked by:** XHCC2.OCCFGDONE

10.2.250 XHCI USB3 Overcurrent Pin Mapping (U3OCM2) — Offset 9128h

The RW/L property of this register is controlled by OCCFDONE bit.

Note:

NOTE: Bit definitions are the same as U3OCM1, offset 9124h.

10.2.251 XHCI USB3 Overcurrent Pin Mapping (U3OCM3) — Offset 912Ch

The RW/L property of this register is controlled by OCCFDONE bit.

Note:

NOTE: Bit definitions are the same as U3OCM1, offset 9124h.

10.2.252 XHCI USB3 Overcurrent Pin Mapping (U3OCM4) — Offset 9130h

The RW/L property of this register is controlled by OCCFDONE bit.

Note:

NOTE: Bit definitions are the same as U3OCM1, offset 9124h.

10.3 USB Device Controller (xDCI) Configuration Registers (D13:F1)

This section documents the registers in Bus: 0, Device: 13, Function: 1.

Table 10-4. Summary of Bus: 0, Device: 13, Function: 1 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device Id And Vendor Id Register (DEVVENDID)	0AAA8086h
4h	4	Status And Command (STATUSCOMMAND)	00100000h
8h	4	Revision Id And Class Code (REVCLASSCODE)	0C03FE00h
Ch	4	Cache Line Latency Header And Bist (CLLATHEADERBIST)	00000000h
10h	4	Base Address Register (BAR)	00000004h
14h	4	Base Address Register High (BAR_HIGH)	00000000h
18h	4	Base Address Register1 (BAR1)	00000004h
1Ch	4	Base Address Register1 High (BAR1_HIGH)	00000000h
2Ch	4	Subsystem Vendor And Subsystem Id (SUBSYSTEMID)	00000000h
30h	4	Expansion Rom Base Address (EXPANSION_ROM_BASEADDR)	00000000h
34h	4	Capabilities Pointer Register (CAPABILITYPTR)	00000080h
3Ch	4	Interrupt Register (INTERRUPTREG)	00000100h
80h	4	Power Management Capability Id (POWERCAPID)	48039001h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
84h	4	Power Management Control And Status Register (PMECTRLSTATUS)	00000008h
90h	4	Pci Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD)	F0140009h
94h	4	Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG)	01400010h
98h	4	Software Ltr Update Mmio Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)	00000000h
9Ch	4	Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG)	010F8301h
A0h	4	D0i3 And Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG)	00080800h
F8h	4	Manufacturers Id (MANID)	04000F1Ch

10.3.1 Device Id And Vendor Id Register (DEVVENDID) — Offset 0h

Device ID and Vendor ID provided by this register uniquely identifies the XXX Device

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:13, F:1] + 0h	0AAA8086h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0AAAh RO/P	**Device Id Field (DEVICEID):** Device ID identifies the particular PCI device
15:0	8086h RO	**Vendor Id Field (VENDORID):** Vendor ID is a unique ID provided by the PCI SIG which identifies the manufacturer of the device

10.3.2 Status And Command (STATUSCOMMAND) — Offset 4h

Command register to programme interrupt disable bus initiator enable and Memory space enable. Status register to read the errors and aborts

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:13, F:1] + 4h	00100000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW/1C	**Rma Field (RMA):** Received initiator Abort
28	0h RW/1C	**Rta Field (RTA):** Received Target Abort
27:21	0h RO	**Reserved**
20	1h RO	**Cap List Field (CAPLIST):** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**Intrerrupt Status Field (INTR_STATUS):** Interrupt Status: This bit reflects state of interrupt in the device
18:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** This field is Interrupt Disable
9	0h RO	**Reserved**
8	0h RW	**Serr Enable Field (SERR_ENABLE):** SERR Enable Not implemented
7:3	0h RO	**Reserved**
2	0h RW	**Bme Field (BME):** Bus Initiator Enable
1	0h RW	**Mse Field (MSE):** Memory Space Enable
0	0h RO	**Reserved**

10.3.3 Revision Id And Class Code (REVCLASSCODE) — Offset 8h

Revision ID register identifies revision of particular device and Class Code register is used to identify generic function of the device

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:13, F:1] + 8h	0C03FE00h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:8	0C03FEh RO	**Revision Id Field (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	00h RO/P	**Class Code Field (RID):** Revision ID identifies the revision of particular PCI device.

10.3.4 Cache Line Latency Header And Bist (CLLATHEADERBIST) — Offset Ch

Cache Line size as RW with def 0 Latency timer RW with def 0 Header type with Type 0 configuration header and Reserved BIST register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:13, F:1] + Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**Multi Function Device Field (MULFNDEV):** This field is Multi Function Device
22:16	00h RO	**Header Type Field (HEADERTYPE):** Header Type: Implements Type 0 Configuration header
15:8	00h RO	**Latency Timer Field (LATTIMER):** Latency Timer:. This register is implemented as R/W with default as 0
7:0	00h RW/P	**Cache Line Size Field (CACHELINE_SIZE):** This field is Cacheline Size

10.3.5 Base Address Register (BAR) — Offset 10h

Base Address Register low [31:2] type[2:1] in 32bit or 64bit addr range and memory space indicator [0]

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:13, F:1] + 10h	00000004h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:21	000h RW	**Base Address Field (BASEADDR):** Base Address Register Low Base address of the OCP fabric memory space. Taken from Strap values as ones
20:12	0h RO	**Reserved**
11:4	00h RO	**Size Field (SIZEINDICATOR):** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**Prefetchable Field (PREFETCHABLE):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	2h RO	**Type Field (TYPE0):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** Memory Space Indicator: 0 indicates this BAR is present in the memory space.

10.3.6 Base Address Register High (BAR_HIGH) — Offset 14h

Base Address Register High enabled if [2:1] of BAR_type_LOW is 10

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:13, F:1] + 14h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR_HIGH):** Base Address high - MSB

10.3.7 Base Address Register1 (BAR1) — Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K type in [2:1] and memory space indicator in [0]

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:13, F:1] + 18h	00000004h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR1):** Base Address1 This field is present if BAR1 is enabled through private configuration space.
11:4	00h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	2h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

10.3.8 Base Address Register1 High (BAR1_HIGH) — Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1 register is 10

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:13, F:1] + 1Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR1_HIGH):** Base Address: Base address of the OCP fabric memory space. Taken from Strap values as ones

10.3.9 Subsystem Vendor And Subsystem Id (SUBSYSTEMID) — Offset 2Ch

SVID register along with SID register is to distinguish subsystem from another

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:13, F:1] + 2Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O/P	**Subsystem Id Field (SUBSYSTEMID):** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system.
15:0	0000h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

10.3.10 Expansion Rom Base Address (EXPANSION_ROM_BASEADDR) — Offset 30h

EXPANSION ROM base address register is a RO indicates support for expansion ROMs

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:13, F:1] + 30h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Expansion Rom Base Address Field (EXPANSION_ROM_BASE):** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

10.3.11 Capabilities Pointer Register (CAPABILITYPTR) — Offset 34h

Capabilities Pointer register indicates what the next capability is

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:13, F:1] + 34h	00000080h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Capabilities Pointer: Indicates what the next capability is.

10.3.12 Interrupt Register (INTERRUPTREG) — Offset 3Ch

Interrupt line Register isn't used in Bridge directly Interrupt Pin register reflects the IPIN value in private config space. Min_gnt register indicating the req of latency timers and max_lat register max latenc

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:13, F:1] + 3Ch	00000100h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	**Min Gnt Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved**
11:8	1h RO	**Interrupt Pin Field (INTPIN):** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW/P	**Int Line Field (INTLINE):** Interrupt Line: It is used to communicate to software the interrupt line to which the interrupt pin is connected

10.3.13 Power Management Capability Id (POWERCAPID) — Offset 80h

PowerManagement Capability ID register points to next capability structure and power mgmnt capability with Power management capabilities register for PME support and version

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:13, F:1] + 80h	48039001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:27	09h RO	**Pme Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved**
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	90h RO	**Next Cap Field (NXTCAP):** Next Capability: Points to the next capability structure.
7:0	01h RO	**Power Capability Id Field (POWER_CAP):** Power Management Capability: Indicates this is power management capability

10.3.14 Power Management Control And Status Register (PMECTRLSTATUS) — Offset 84h

power management control and status register to set and read PME status PME enable No Soft reset and power state

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:13, F:1] + 84h	00000008h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/P	**Pme Status Field (PMESTATUS):** This field is PME Status

Bit Range	Default & Access	Field Name (ID): Description
14:9	0h RO	**Reserved**
8	0h RW/P	**Pme Enable Field (PMEENABLE):** This field is PME Enable
7:4	0h RO	**Reserved**
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	0h RO	**Reserved**
1:0	0h RW	**Power State Field (POWERSTATE):** Power State: This field is used both to determine the current power state and to set a new power state

10.3.15 Pci Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) — Offset 90h

PCI Device Vendor Specific Capability register defines Vendor specific Capability ID revision length next capability and CAPID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:13, F:1] + 90h	F0140009h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision Id Field (REVID):** Revision ID of capability structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	00h RO	**Next Capability Field (NEXT_CAP):** This field is Next Capability
7:0	09h RO	**Capability Id Field (CAPID):** This field is Capability ID

10.3.16 Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) — Offset 94h

Extended Vendor capability register for VSEC Length revision and ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:13, F:1] + 94h	01400010h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**Vendor Specific Id Field (VSEC_LENGTH):** Vendor Specific Extended Capability Length
19:16	0h RO	**Vendor Specific Revision Field (VSEC_REV):** Vendor specific Extended Capability revision
15:0	0010h RO	**Vendor Specific Length Field (VSECID):** Vendor Specific Extended Capability ID

10.3.17 Software Ltr Update Mmio Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) — Offset 98h

Software location pointer in MMIO space as an offset specified by BAR

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:13, F:1] + 98h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**Swltr Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**Swltr Bar Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**Swltr Valid Field (SW_LAT_VALID):** This value is reflected from the SW LTR valid strap at the top level

10.3.18 Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) — Offset 9Ch

Device IDLE pointer register giving details on Device MMIO offset location BAR NUM and D0i3 Valid Strap

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:13, F:1] + 9Ch	010F8301h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:4	010F830h RO	**D0i3 Dword Offset Field (DWORD_OFFSET):** contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**Bar Num Field (BAR_NUM):** Bar num: Indicates that the D0i3 MMIO location is always at BAR0
0	1h RO	**D0i3 Valid Field (VALID):** Valid: This value is reflected from the D0i3 valid strap at the top level.

10.3.19 D0i3 And Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) — Offset A0h

D0idle_Max_Power_On_Latency register set at boot and Power control enable register to enable communication with the PGCB block below the Bridge

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:13, F:1] + A0h	00080800h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW/P	**Hae Field (HAE):** Hardware Autonomous Enable
20	0h RO	**Reserved**
19	1h RW/P	**Sleep Enable Field (SLEEP_EN):** This field is Sleep Enable

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW/P	**D3 Hen Field (D3HEN):** D3-Hot Enable (D3HEN): If 1 then function will power gate when idle and the PMCSR[1:0] register in the function =11 (D3).
17	0h RW/P	**Device Idle En Field (DEVIDLEN):** DEVIDLE Enable (DEVIDLEN): If 1 then the function will power gate when idle and the DevIdle register (DevIdleC[2] = 1) is set.
16	0h RW/P	**Pmc Request Enable Field (PMCRE):** PMCRE: PMC Request Enable
15:13	0h RO	**Reserved**
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** Power On Latency Scale
9:0	000h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** Power On Latency value

10.3.20 Manufacturers Id (MANID) — Offset F8h

Manufacturers ID register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:13, F:1] + F8h	04000F1Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	04000F1Ch RO/P	**Manufacturers Id Field (MANID):** Manufacturer ID: Default value comes from straps.

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11 Enhanced SPI Interface (D31:F0)

11.1 eSPI PCI Configuration Registers

Table 11-1. Summary of eSPI PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device and Vendor Identifiers (ESPI_DID_VID)—Offset 0h	XXXX8086h
4h	7h	Device Status and Command (ESPI_STS_CMD)—Offset 4h	3h
8h	Bh	Class Code and Revision ID (ESPI_CC_RID)—Offset 8h	60100XXh
2Ch	2Fh	Sub System Identifiers (ESPI_SS)—Offset 2Ch	0h
34h	37h	Capability List Pointer (ESPI_CAPP)—Offset 34h	0h
80h	83h	I/O Decode Ranges and I/O Enables (ESPI_IOD_IOE)—Offset 80h	0h
84h	87h	eSPI Generic IO Range 1 (ESPI_LGIR1)—Offset 84h	0h
88h	8Bh	eSPI Generic IO Range 2 (ESPI_LGIR2)—Offset 88h	0h
8Ch	8Fh	eSPI Generic IO Range 3 (ESPI_LGIR3)—Offset 8Ch	0h
90h	93h	eSPI Generic IO Range 4 (ESPI_LGIR4)—Offset 90h	0h
94h	97h	USB Legacy Keyboard/Mouse Control (ESPI_ULKMC)—Offset 94h	0h
98h	9Bh	eSPI Generic Memory Range (ESPI_LGMR)—Offset 98h	0h
A0h	A3h	eSPI CS1 IO Routing Enables (ESPI_CS1IORE)—Offset A0h	0h
A4h	A7h	eSPI CS1 Generic IO Range 1 (ESPI_CS1GIR1)—Offset A4h	0h
A8h	ABh	eSPI CS1 Generic Memory Range 1 (ESPI_CS1GMR1)—Offset A8h	0h
D8h	DBh	BIOS Decode Enable (ESPI_BDE)—Offset D8h	FFCFh
DCh	DFh	BIOS Control (ESPI_BC)—Offset DCh	20h

11.1.1 Device and Vendor Identifiers (ESPI_DID_VID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: XXXX8086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	-- RO/V	**Device Identification (DID):** Indicates the Device ID of the controller. Refer to the Device and Revision ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor Identification (VID)**

11.1.2 Device Status and Command (ESPI_STS_CMD)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 3h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Detected Parity Error (DPE):** Set when the bridge detects a parity error. This bit gets set even if CMD.PERE is not set.
30	0h RW/1C/V	**Signaled System Error (SSE):** Set when the bridge signals a system error to the internal SERR# logic.
29	0h RW/1C/V	**Received Initiator Abort (RMA):** Set when the bridge receives a completion with unsupported request.
28	0h RW/1C/V	**Received Target Abort (RTA):** Set when the bridge receives a completion with completer abort status.
27	0h RW/1C/V	**Signaled Target Abort (STA):** Set when the bridge generates a completion packet with target abort status.
26:25	0h RO	**DEVSEL# Timing Status (DTS):** Indicates medium timing, although this has no meaning on the HW.
24	0h RW/1C/V	**Data Parity Error Detected (DPD):** Set when the bridge receives a completion packet from a previous request, and detects a parity error, and CMD.PERE is set.
23:21	0h RO	Reserved.
20	0h RO	**Capabilities List (CLIST):** There is a capabilities list in the eSPI bridge.
19:9	0h RO	Reserved.
8	0h RW	**SERR# Enable (SEE):** Enable SERR# to be generated if this bit is set.
7	0h RO	Reserved.
6	0h RW	**Parity Error Response Enable (PERE):** When this bit is set to 1, it enables the HW to response to parity errors detected on the interface.
5:3	0h RO	Reserved.
2	0h RW	**Bus Initiator Enable (BME):** Controls a device's ability to act as a Initiator on the bus. A value of 0 disables the device from generating traffic. A value of 1 allows the device to behave as a bus Initiator.
1	1h RO	**Memory Space Enable (MSE):** Memory space cannot be disabled.
0	1h RO	**I/O Space Enable (IOSE):** I/O space cannot be disabled.

11.1.3 Class Code and Revision ID (ESPI_CC_RID)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 60100XXh

Bit Range	Default & Access	Field Name (ID): Description
31:24	6h RO	**Base Class Code (BCC):** Indicates the device is a bridge device.
23:16	1h RO	**Sub-Class Code (SCC):** Indicates the device a PCI to ISA bridge.
15:8	0h RO	**Programming Interface (PI):** Hardwired to 0. The bridge has no programming interface.
7:0	-- RO/V	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

11.1.4 Sub System Identifiers (ESPI_SS)—Offset 2Ch

This register is initialized to logic 0 by the assertion of PLTRST#. This register can be written only once after PLTRST# de-assertion.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SSID):** This is written by BIOS. No hardware action taken on this value.
15:0	0h RW/O	**Subsystem Vendor ID (SSVID):** This is written by BIOS. No hardware action taken on this value.

11.1.5 Capability List Pointer (ESPI_CAPP)—Offset 34h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Capability Pointer (CP):** Indicates the offset of the first Capability Item.

11.1.6 I/O Decode Ranges and I/O Enables (ESPI_IOD_IOE)—Offset 80h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW	**Microcontroller Enable #2 (ME2):** Enables decoding of I/O locations 4Eh and 4Fh.
28	0h RW	**SuperI/O Enable (SE):** Enables decoding of I/O locations 2Eh and 2Fh.
27	0h RW	**Microcontroller Enable #1 (ME1):** Enables decoding of I/O locations 62h and 66h.
26	0h RW	**Keyboard Enable (KE):** Enables decoding of the keyboard I/O locations 60h and 64h.
25	0h RW	**High Gameport Enable (HGE):** Enables decoding of the I/O locations 208h to 20Fh.
24	0h RW	**Low Gameport Enable (LGE):** Enables decoding of the I/O locations 200h to 207h.
23:20	0h RO	Reserved.
19	0h RW	**Floppy Drive Enable (FDE):** Enables decoding of the FDD range. Range is selected by FDD bit.
18	0h RW	**Parallel Port Enable (PPE):** Enables decoding of the LPT range. Range is selected by LPT bit.
17	0h RW	**Com Port B Enable (CBE):** Enables decoding of the COMB range. Range is selected CB bit.
16	0h RW	**Com Port A Enable (CAE):** Enables decoding of the COMA range. Range is selected CA bit.
15:13	0h RO	Reserved.
12	0h RW	**FDD Range (FDD):** The following table describes which range to decode for the FDD Port Bits Decode Range 0 3F0h - 3F5h, 3F7h (Primary) 1 370h - 375h, 377h (Secondary)
11:10	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**LPT Range (LPT):** The following table describes which range to decode for the LPT Port: Bits Decode Range 00 378h - 37Fh and 778h - 77Fh 01 278h - 27Fh (port 279h is read only) and 678h - 67Fh 10 3BCh - 3BEh and 7BCh - 7BEh 11 Reserved
7	0h RO	Reserved.
6:4	0h RW	**ComB Range (CB):** The following table describes which range to decode for the COMB Port Bits Decode Range 000 3F8h - 3FFh (COM 1) 001 2F8h - 2FFh (COM 2) 010 220h - 227h 011 228h - 22Fh 100 238h - 23Fh 101 2E8h - 2EFh (COM 4) 110 338h - 33Fh 111 3E8h - 3EFh (COM 3)
3	0h RO	Reserved.
2:0	0h RW	**ComA Range (CA):** The following table describes which range to decode for the COMA Port Bits Decode Range 000 3F8h - 3FFh (COM 1) 001 2F8h - 2FFh (COM 2) 010 220h - 227h 011 228h - 22Fh 100 238h - 23Fh 101 2E8h - 2EFh (COM 4) 110 338h - 33Fh 111 3E8h - 3EFh (COM 3)

11.1.7 eSPI Generic IO Range 1 (ESPI_LGIR1)—Offset 84h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 31
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address[7:2] Mask (ADDR_MASK):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW	**Address[15:2] (ADDR):** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RO	Reserved.
0	0h RW	**eSPI Decode Enable (LDE):** When this bit is set to 1, then the range specified in this register is enabled for decoding to eSPI.

11.1.8 eSPI Generic IO Range 2 (ESPI_LGIR2)—Offset 88h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address[7:2] Mask (ADDR_MASK):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW	**Address[15:2] (ADDR):** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
1	0h RO	Reserved.
0	0h RW	**eSPI Decode Enable (LDE):** When this bit is set to 1, then the range specified in this register is enabled for decoding to eSPI.

11.1.9 eSPI Generic IO Range 3 (ESPI_LGIR3)—Offset 8Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
23:18	0h RW	**Address[7:2] Mask (ADDR_MASK):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW	**Address[15:2] (ADDR):** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
1	0h RO	Reserved.
0	0h RW	**eSPI Decode Enable (LDE):** When this bit is set to 1, then the range specified in this register is enabled for decoding to eSPI.

11.1.10 eSPI Generic IO Range 4 (ESPI_LGIR4)—Offset 90h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address[7:2] Mask (ADDR_MASK):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW	**Address[15:2] (ADDR):** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
1	0h RO	Reserved.
0	0h RW	**eSPI Decode Enable (LDE):** When this bit is set to 1, then the range specified in this register is enabled for decoding to eSPI.

11.1.11 USB Legacy Keyboard/Mouse Control (ESPI_ULKMC)—Offset 94h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C/V	**SMI Caused by End of Pass-through (SMIBYENDPS):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 7, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
14:12	0h RO	Reserved.
11	0h RW/1C/V	**SMI Caused by Port 64 Write (TRAPBY64W):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 3, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch. Note that the A20Gate Pass-Through Logic allows specific port 64h Writes to complete without setting this bit.
10	0h RW/1C/V	**SMI Caused by Port 64 Read (TRAPBY64R):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 2, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
9	0h RW/1C/V	**SMI Caused by Port 60 Write (TRAPBY60W):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 1, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch. Note that the A20Gate Pass-Through Logic allows specific port 60h Writes to complete without setting this bit.
8	0h RW/1C/V	**SMI Caused by Port 60 Read (TRAPBY60R):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 0, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
7	0h RW	**SMI at End of Pass-through Enable (SMIATENDPS):** May need to cause SMI at the end of a pass-through. Can occur if an SMI is generated in the middle of a pass through, and needs to be serviced later.
6	0h RO/V	**Pass Through State (PSTATE):** This read-only bit indicates that the state machine is in the middle of an A20GATE pass-through sequence. If software needs to reset this bit, it should set Bit 5 0.
5	0h RW	**A20Gate Pass-Through Enable (A20PASSEN):** When enabled, allows A20GATE sequence Pass-Through function. When enabled, a specific cycle sequence involving writes to port 60h and port 64h does not result in the setting of the SMI status bits. SMI# will not be generated, even if the various enable bits are set.
4	0h RO	Reserved.
3	0h RW	**SMI on Port 64 Writes Enable (S64WEN):** When set, a 1 in bit 11 will cause an SMI event.
2	0h RW	**SMI on Port 64 Reads Enable (S64REN):** When set, a 1 in bit 10 will cause an SMI event.
1	0h RW	**SMI on Port 60 Writes Enable (S60WEN):** When set, a 1 in bit 9 will cause an SMI event.
0	0h RW	**SMI on Port 60 Reads Enable (S60REN):** When set, a 1 in bit 8 will cause an SMI event.

11.1.12 eSPI Generic Memory Range (ESPI_LGMR)—Offset 98h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Memory Address[31:16] (MADDR):** This field specifies a 64KB memory block anywhere in the 4GB memory space that will be decoded to eSPI if enabled.
15:1	0h RO	Reserved.
0	0h RW	**eSPI Memory Range Decode Enable (LGMRD_EN):** When this bit is set to 1, then the range specified in this register is enabled for decoding to eSPI.

11.1.13 eSPI CS1 IO Routing Enables (ESPI_CS1IORE)—Offset A0h

This register is used to route fixed I/O transactions from the Host to the second Target device (CS1# if supported) over the Peripheral Channel on the eSPI bus. Register Lock:This register is locked in a single Target configuration (soft-strap espi_cs1_en = 0b).

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14	0h RO	**Debug Port CS1# Routing Enable (DPRE):** Enables routing of I/O locations 80h, 84h-86h, 88h, 8Ch-8Eh, 90h, 94h-96h, 98h, 9Ch-9Eh to eSPI CS1#. This field is only writeable if the eSPI CS1 is enabled and is RO when eSPI CS1 is disabled.
13	0h RO	**Microcontroller #2 CS1# Routing Enable (MRE2):** Enables routing of I/O locations 4Eh and 4Fh to eSPI CS1#. This field is only writeable if the eSPI CS1 is enabled and is RO when eSPI CS1 is disabled.
12	0h RO	**SuperI/O CS1# Routing Enable (SRE):** Enables routing of I/O locations 2Eh and 2Fh to eSPI CS1#. This field is only writeable if the eSPI CS1 is enabled and is RO when eSPI CS1 is disabled.
11	0h RO	**Microcontroller #1 CS1# Routing Enable (MRE1):** Enables routing of I/O locations 62h and 66h to eSPI CS1#. This field is only writeable if the eSPI CS1 is enabled and is RO when eSPI CS1 is disabled.
10	0h RO	**Keyboard CS1# Routing Enable (KRE):** Enables routing of the keyboard I/O locations 60h and 64h to eSPI CS1#. This field is only writeable if the eSPI CS1 is enabled and is RO when eSPI CS1 is disabled.
9	0h RO	**High Gameport CS1# Routing Enable (HGRE):** Enables routing of the I/O locations 208h to 20Fh to eSPI CS1#. This field is only writeable if the eSPI CS1 is enabled and is RO when eSPI CS1 is disabled.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**Low Gameport CS1# Routing Enable (LGRE):** Enables routing of the I/O locations 200h to 207h to eSPI CS1#. This field is only writeable if the eSPI CS1 is enabled and is RO when eSPI CS1 is disabled.
7:4	0h RO	Reserved.
3	0h RO	**Floppy Drive CS1# Routing Enable (FDRE):** Enables routing of the FDD range to eSPI CS1#. Range is selected by FDD bit. This field is only writeable if the eSPI CS1 is enabled and is RO when eSPI CS1 is disabled.
2	0h RO	**Parallel Port CS1# Routing Enable (PPRE):** Enables routing of the LPT range to eSPI CS1#. Range is selected by LPT bit. This field is only writeable if the eSPI CS1 is enabled and is RO when eSPI CS1 is disabled.
1	0h RO	**Com Port B CS1# Routing Enable (CBRE):** Enables routing of the COMB range to eSPI CS1#. Range is selected by CB bit. This field is only writeable if the eSPI CS1 is enabled and is RO when eSPI CS1 is disabled.
0	0h RO	**Com Port A CS1# Routing Enable (CARE):** Enables routing of the COMA range to eSPI CS1#. Range is selected by CA bit. This field is only writeable if the eSPI CS1 is enabled and is RO when eSPI CS1 is disabled.

11.1.14 eSPI CS1 Generic IO Range 1 (ESPI_CS1GIR1)—Offset A4h

This register has the same bit definitions as LGIR1. This register is used to route variable IO transactions from the Host to the second Target device (CS1#) over the Peripheral Channel on the eSPI bus.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address[7:2] Mask (ADDR_MASK):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW	**Address[15:2] (ADDR):** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
1	0h RO	Reserved.
0	0h RW	**LPC Decode Enable (LDE):** When this bit is set to 1, then the range specified in this register is enabled for decoding to eSPI.

11.1.15 eSPI CS1 Generic Memory Range 1 (ESPI_CS1GMR1)—Offset A8h

This register has the same bit definitions as LGMR. This register is used to route memory transactions from the Host to the second Target device (CS1#) over the Peripheral Channel on the eSPI bus.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Memory Address[31:16] (MADDR):** This field specifies a 64KB memory block anywhere in the 4GB memory space that will be decoded to eSPI as Memory Cycle if enabled.
15:1	0h RO	Reserved.
0	0h RW	**eSPI Memory Range Decode Enable (LGMRD_EN):** When this bit is set to 1, then the range specified in this register is enabled for decoding to eSPI.

11.1.16 BIOS Decode Enable (ESPI_BDE)—Offset D8h

The concept of Feature Space does not apply to SPI-based flash. PCH simply decodes these ranges as memory accesses when enabled for the SPI flash interface.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 0

Default: FFCFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**BDE Lock Enable (BLE):** When this bit is set, the RW bits of this BDE register are locked down. Once set, this bit can only be cleared by PLTRST#.
30:16	0h RO	Reserved.
15	1h RO	**F8-FF Enable (EF8):** Enables decoding of 512K of the following BIOS range: Data space: FFF80000h - FFFFFFFFh Feature space: FFB80000h - FFBFFFFFh
14	1h RW/L	**F0-F8 Enable (EF0):** Enables decoding of 512K of the following BIOS range: Data space: FFF00000h - FFF7FFFFh{br] Feature space: FFB00000h - FFB7FFFFh
13	1h RW/L	**E8-EF Enable (EE8):** Enables decoding of 512K of the followingBIOS range: Data space: FFE80000h - FFEFFFFFh Feature space: FFA80000h - FFAFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
12	1h RW/L	**E0-E8 Enable (EE0):** Enables decoding of 512K of the followingBIOS range: Data space: FFE00000h - FFE7FFFFh Feature Space: FFA00000h - FFA7FFFFh
11	1h RW/L	**D8-DF Enable (ED8):** Enables decoding of 512K of the following BIOS range: Data space: FFD80000h - FFDFFFFFh Feature space: FF980000h - FF9FFFFFh
10	1h RW/L	**D0-D7 Enable (ED0):** Enables decoding of 512K of the followingBIOS range: Data space: FFD00000h - FFD7FFFFh Feature space: FF900000h - FF97FFFFh
9	1h RW/L	**C8-CF Enable (EC8):** Enables decoding of 512K of the following BIOS range: Data space: FFC80000h - FFCFFFFFh Feature space: FF880000h - FF8FFFFFh
8	1h RW/L	**C0-C7 Enable (EC0):** Enables decoding of 512K of the following BIOS range: Data space: FFC00000h - FFC7FFFFh Feature space: FF800000h - FF87FFFFh
7	1h RW/L	**Legacy F Segment Enable (LFE):** This enables the decoding of thelegacy 64KB range at F0000h - FFFFFh Note that decode for the BIOS legacy F segment is enabled by theLFE bit only, it is not affected by the GEN_PMCON_1.iA64_EN bit.
6	1h RW/L	**Legacy E Segment Enable (LEE):** This enables the decoding of thelegacy 64KB range at E0000h - EFFFFh Note that decode for the BIOS legacy E segment is enabled by the LEE bit only, it is not affected by the GEN_PMCON_1.iA64_EN bit.
5:4	0h RO	Reserved.
3	1h RW/L	**70-7F Enable (E70):** Enables decoding of 1MB of the followingBIOS range: Data space: FF700000h - FF7FFFFFh Feature space: FF300000h - FF3FFFFFh
2	1h RW/L	**60-6F Enable (E60):** Enables decoding of 1MB of the followingBIOS range: Data space: FF600000h - FF6FFFFFh Feature Space: FF200000h - FF2FFFFFh
1	1h RW/L	**50-5F Enable (E50):** Enables decoding of 1MB of the followingBIOS range: Data space: FF500000h - FF5FFFFFh Feature space: FF100000h - FF1FFFFFh
0	1h RW/L	**40-4F Enable (E40):** Enables decoding of 1MB of the following BIOS range: Data space: FF400000h - FF4FFFFFh Feature space: FF000000h - FF0FFFFFh

11.1.17 BIOS Control (ESPI_BC)—Offset DCh

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 20h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW/L	**BIOS Write Reporting (Async-SMI) Enable (BWRE):** 1'b0: Disable reporting of BIOS Write event. 1'b1: Enable reporting of BIOS Write event (BWRS bit = 1) using Async-SMI.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/1C/V	**BIOS Write Status (BWRS):** HW sets this bit if a memory write access is detected to a protected BIOS range. 1'b0: Memory write to BIOS region not attempted or attempted with WPD bit = 1. 1'b1: A memory write transaction to BIOS region has been received with WPD bit = 0. Note: An Async-SMI message is generated to report this event if BWRE bit is set. Note: SW must write a 1 to this bit to clear it, which will also deassert the Async-SMI, if BWRE is set.
9	0h RO	Reserved.
8	0h RW/1C/V	**BIOS Write Protect Disable Status (BWPDS):** HW sets this bit if configuration write access is detected to protected WPD bit. 1'b0: No attempt has been made to set WPD bit with LE bit = 1. 1'b1: A configuration write request has been received to set WPD bit (0 or 1) with LE bit = 1. Note: An SB Sync-SMI (Assert_SSMI) message is generated to report this event if HW sets this bit. The unsuccessful completion for the configuration write is returned upon receiving the SMI_Ack message response. Note: SW must write a 1 to this bit to clear it, which will also deassert the Sync-SMI Note: The Sync-SMI sets the PMC SMI_STS.TCO_STS register.
7	0h RW/L	**BIOS Interface Lock-Down (BILD):** When set, prevents TS and BBS bits from being changed. This bit can only be written from 0 to 1 once. BIOS Note: This bit is not backed up in the RTC well. This bit should also be set in the BUC register in the RTC device to record the last state of this value following a cold reset.
6	0h RW/V/L	**Boot BIOS Strap (BBS):** This field determines the destination of accesses to the BIOS memory range. For the default see the strap section in Vol1 for details. 0: SPI 1: eSPI When SPI or eSPI is selected, the range that is decoded is further qualified by other configuration bits described in the respective sections. The value in this field can be overwritten by software as long as the BIOS Interface Lock-Down is not set.
5	1h RW/L	**Enable InSMM.STS (EISS):** When this bit is set, the BIOS region is not writable until SMM sets the InSMM.STS bit. Today BIOS Flash is writable if WPD is a 1. If this bit is set, then WPD must be a 1 and InSMM.STS (0xFED3_0880(0)) must be 1 also. If this bit is clear, then BIOS is writable based only on WPD = 1 and the InSMM.STS is a dont care.
4	0h RO/V	**Top Swap (TS):** When set, PCH will invert either A16, A17, or A18 for cycles going to the BIOS space (but not the Feature space). When cleared, PCH will not invert A16. If booting from eSPI, then the Boot Block Size is fixed at 64KB and A16 is inverted if Top Swap is enabled. If booting from SPI, then the BOOT_BLOCK_SIZE soft strap determines if A16, A17, orA18 should be inverted if Top Swap is enabled. Note: If the Top-Swap strap is asserted, then this bit cannot be cleared by software. The strap jumper should be removed and the system rebooted. BIOS Note: This bit provides a read-only path to view the state of the Top Swap strap. It is backed up and driven from the RTC well. BIOS will need to program the corresponding register in the RTC well, which will be reflected in this register.
3	0h RO	Reserved.
2	0h RO/V	**eSPI Enable Pin Strap (ESPI):** This field determines the destination of accesses to the D31:F0 and related Fixed and Variable IO and Memory decode ranges, including BIOS memory range. 1'b0: Reserved 1'b1: eSPI is the D31:F0 target. Notes: 1. This field, along with the BBS field setting, determines PCH configuration. 2. This field cannot be overwritten by software (unlike the BBS field). 3. This bit is also reflected in the SPI Flash PCI Configuration register Offset DCh.
1	0h RW/L	**Lock Enable (LE):** When set, setting the WP bit will cause SMI. When cleared, setting the WP bit will not cause SMI. Once set, this bit can only be cleared by a PLTRST#. When this bit is set, EISS - bit (5) of this register is locked down.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Write Protect Disable (WPD):** When set, access to the BIOS space is enabled for both read and write cycles to BIOS. When cleared, only read cycles are permitted to the FWH or SPI flash. When this bit is written from a 0 to a 1 and the LE bit is also set, an SMI# is generated. This ensures that only SMM code can update BIOS.

11.2 eSPI PCR Registers

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 11-2. Summary of eSPI PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4000h	4003h	eSPI Target Configuration And Link Control (SLV_CFG_REG_CTL)—Offset 4000h	0h
4004h	4007h	eSPI Target Configuration Register Data (SLV_CFG_REG_DATA)—Offset 4004h	0h
4020h	4023h	Peripheral Channel Error for Target 0 (PCERR_SLV0)—Offset 4020h	80h
4024h	4027h	Peripheral Channel Error for Target 1 (PCERR_SLV1)—Offset 4024h	0h
4030h	4033h	Virtual Wire Channel Error for Target 0 (VWERR_SLV0)—Offset 4030h	0h
4034h	4037h	Virtual Wire Channel Error for Target 1 (VWERR_SLV1)—Offset 4034h	0h
4040h	4043h	Flash Access Channel Error for Target 0 (FCERR_SLV0)—Offset 4040h	40080h
4050h	4053h	Link Error for Target 0 (LNKERR_SLV0)—Offset 4050h	FF00h
4054h	4057h	Link Error for Target 1 (LNKERR_SLV1)—Offset 4054h	0h

11.2.1 eSPI Target Configuration And Link Control (SLV_CFG_REG_CTL)—Offset 4000h

Along with SLV_CFG_REG_DATA, this register controls Rd/Wr access to Target Configuration registers using eSPI Get/Set_Configuration, Get_Status and In-Band Reset cycles.

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Target Configuration Register Access Enable (SCRE):** Writing a 1 to this field triggers an access (SCRT) to a Target Config Register ('Go'). Note: Hardware clears this bit to 0 (& sets the SCRS field) when the transaction has completed on the eSPI bus. In the case of a configuration/status register read, the data is valid only after this bit has been cleared by HW. Note: The SCRE is effective only if SCRS is clear.

Bit Range	Default & Access	Field Name (ID): Description
30:28	0h RW/1C/V	**Target Configuration Register Access Status (SCRS):** This field is set upon the completion of a configuration register access (SCRE). Software must clear this field by writing all 1s before initiating another Target configuration register access (SCRE). 0h: Status not valid 1h: Target No_Response 2h: Target Response CRC Error 3h: Target Response Fatal Error 4h: Target Response Non-Fatal Error 5h – 6h: Reserved 7h: No errors (transaction completed successfully)
27	0h RW/1S	**SB eSPI Link Configuration Lock (SBLCL):** When set, eSPI controller prevents writes (i.e., SET_CONFIGURATION) to any eSPI Specification defined Target Capabilities and Configuration registers in the reserved register address range (0h – 7FFh). Access to Target implementation specific configuration registers outside this range are not impacted by this lock bit and are always available – access protections to such registers are Target implementation dependent. Notes: 1. This bit cannot be written to 0 once it has been set to 1. It can only be cleared by PLTRST# assertion. The lock is automatically disabled if and while the LNKERR_SLV0.SLCRR register bit is asserted (upon an eSPI link Fatal Error condition) to allow BIOS (or another SW agent) to attempt to recover the link. 2. This bit has no effect when PLTRST# is asserted. BIOS Note: BIOS must ensure that this bit is set to 1 after initial eSPI link configuration is over to prevent any further (unintentional or malicious) changes to the eSPI link configuration.
26:21	0h RO	Reserved.
20:19	0h RW	**Target ID (SID):** eSPI Target ID (CS#) to which the Target Configuration Register Access (SCRT) is directed. 00: eSPI Target 0 (EC/BMC) 01: eSPI Target 1 (only support when a second eSPI Target device is present) 10 – 2'b11: Reserved
18	0h RO	Reserved.
17:16	0h RW	**Target Configuration Register Access Type (SCRT):** 00: Target Configuration register read from address SCRA[11:0] (GET_CONFIG) 01: Target Configuration register write to address SCRA[11:0] (SET_CONFIG) 10: Target Status register read (GET_STATUS) 11: In-Band Reset Notes: 1. Writes to Target Configuration registers in the reserved address range (0h – 7FFh) are gated by the SBLCL bit. 2. Setting this field to 10 triggers a Get_Status command to the Target. In this case, the SCRA field is ignored and only the lower 16-bits of the returned data (SLV_CFG_REG_DATA[15:0]) are valid. 3. Setting this field to 11 triggers an In-Band Reset command to the Target. In this case, the SCRA field is ignored and no data is returned. This command resets the link for the targeted Target to a default configuration. Software is responsible for reinitializing the link to optimized (higher performance) settings using these registers.
15:12	0h RO	Reserved.
11:0	0h RW	**Target Configuration Register Address (SCRA):** Per eSPI Spec / eSPI Compatibility Spec.

11.2.2 eSPI Target Configuration Register Data (SLV_CFG_REG_DATA)—Offset 4004h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Target Configuration Register for Read and Write data (SCRD):** Configuration register Write data from software or read data from the Target. For writes, this register must be programmed before the CTL register. For reads, data in this register is valid after the CTL.SCRE bit has been cleared by HW and the CTL.SCRS field indicates a successful transaction.

11.2.3 Peripheral Channel Error for Target 0 (PCERR_SLV0)—Offset 4020h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RW	**Target Host Reset Ack Override (SLV_HOST_RST_ACK_OVRD):** A 1 in this bit will cause the eSPI-MC to not wait for the Target HOST_RESET_ACK Virtual Wire before (immediately) asserting the ResetPrepAck (Host space, GenPrep). The Host_Reset_Warn VW will be transmitted to the Target independent of the setting for this bit.
27:26	0h RW	**Peripheral Channel Received Initiator or Target Abort Reporting Enable (PCRMTARE):** 00: Disable RMA or RTA Reporting 01: Reserved 10: Enable RMA or RTA Reporting as SERR 11: Enable RMA or RTA Reporting as SMI Notes: 1. SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. 2. SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted.
25	0h RW	**Peripheral Channel Unsupported Request Reporting Enable (PCURRE):** If set to 1 by software, it allows reporting of an Unsupported Request (UR) as a System Error (SERR). If eSPI controller decodes a Posted transaction that is not supported, it sets the PCURD bit. If PCCMD.SEE (SERR enable) is also set to 1, then eSPI controller sets the PCSTS.SSE (Signaled System Error) bit and sends a Do_SErr message. Note: If the transaction was a Non-Posted request, then the agent handles the transaction as an Advisory Non-Fatal error, and no error logging or signaling is done. The Completion with UR Completion Status serves the purpose of error reporting.
24	0h RW/1C/V	**Peripheral Channel Unsupported Request Detected (PCURD):** Set to 1 by hardware upon detecting an Unsupported Request (UR) that is not considered an Advisory Non-Fatal error and PCERR.PCURRE is set. Cleared to 0 when software writes a 1 to this register.
23:15	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RW	**Peripheral Channel Non-Fatal Error Reporting Enable (PCNFEE):** 00: Disable Non-Fatal Error Reporting 01: Reserved 10: Enable Non-Fatal Error Reporting as SERR 11: Enable Non-Fatal Error Reporting as SMI Note: SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. Notes: 1. SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. 2. SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
12	0h RW/1C/V	**Peripheral Channel Non-Fatal Status (PCNFES):** This field is set by hardware if a Non-Fatal Error condition is detected on the Peripheral Channel. Software must clear this bit. 0: No Non-Fatal Error detected 1: Non-Fatal Error detected (PCNFEC has a non-zero value) Notes: 1. Clearing this unlocks the PCNFEC field and triggers a SB Deassert_SMI message if PCNFEE is set to SMI. 2. Setting of this bit is independent of the enable to generate a SMI/SERR (PCNFEE)
11:8	0h RO/V	**Peripheral Channel Non-Fatal Cause (PCNFEC):** 0h: No error 1h: Target Response Code: NONFATAL_ERROR 2h: Target Response Code: Unsuccessful Completion 3h: Unexpected completion received from Target (i.e. completion without non-posted request or completion with invalid tag or completion with invalid length) 4h: Unsupported Cycle Type (w.r.t. Command) 5h: Unsupported Message Code 6h: Unsupported Address/Length alignment (upstream only): Memory: Address + Length > 64 B (aligned) [for both Posted and Non-Posted transactions] 7h: Unsupported Address/Length alignment (upstream only): Memory: 64-bit Address with Addr[63:32] = 0h [for both Posted and Non-Posted transactions] 8h – Fh: Reserved Note: This field is updated after a Peripheral channel transaction is completed if the PCNFES bit is not set.
7	1h RW	**PLCC Misaligned Memory Access (PMMA):** Applies to only posted and non-posted memory transactions directed towards D31:f0 to be sent over the eSPI Peripheral Channel to an eSPI Target. 1'b0: Requests with a length of 3 bytes or requests with a length of 1/2/4 bytes whose Address+Length is not DWord aligned will be rejected. 1'b1: Requests with a length of 3 bytes or requests with a length of 1/2/4 bytes whose Address+Length is not DWord aligned will be sent to the Target using the memory write/read format.
6:5	0h RW	**Peripheral Channel Fatal Error Reporting (PCFEE):** 00: Disable Fatal Error Reporting 01: Reserved 10: Enable Fatal Error Reporting as SERR (IOSF-SB Do_SErr message) 11: Enable Fatal Error Reporting as SMI (IOSF-SB Assert_SMI message) Notes: 1. SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. 2. SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. 3. SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
4	0h RW/1C/V	**Peripheral Channel Fatal Error Reporting (PCFES):** This field is set by hardware if a Fatal Error condition is detected on the Peripheral Channel. Software must clear this bit by writing a 1 to it. 0: No Fatal Error detected 1: Fatal Error Type 2 detected (PCFEC has a non-zero value) Notes: 1. Clearing this unlocks the PCFEC field and triggers an SB Deassert_SMI message if PCFEE is set to SMI. 2. Setting of this bit is independent of the enable to generate a SMI/SERR (PCFEE).

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RO/V	**Peripheral Channel Fatal Error Cause (PCFEC):** 0h: No error 1h – 7h: Reserved 8h: Malformed Target Response Payload: Payload length > Max Payload Size (aligned) [Type 2] 9h: Malformed Target Response Payload: Read request size > Max Read Request Size (aligned) [Type 2] Ah: Malformed Target Response Payload: Address + Length > 4KB (aligned) [Type 2] Bh – Fh: Reserved Note: This field is updated after a Peripheral channel transaction is completed if the PCFES bit is not set.

11.2.4 Peripheral Channel Error for Target 1 (PCERR_SLV1)—Offset 4024h

This register is used to control error reporting for the eSPI Peripheral Channel for the second eSPI Target device.
The register definition is identical to that of PCERR_SLV0, with the following exception:
SLV_HOST_RST_ACK_OVRD (bit [28]): This bit has no impact since the Host_Reset_Ack VW from CS1# is not supported by eSPI-MC (Host partition reset flow is gated only for CS0#).

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RW	**Target Host Reset Ack Override (SLV_HOST_RST_ACK_OVRD):** This bit has no impact since the Host_Reset_Ack VW from CS1# is not supported by eSPI-MC (Host partition reset flow is gated only for CS0#).
27:26	0h RW	**Peripheral Channel Received Initiator or Target Abort Reporting Enable (PCRMTARE):** Not used by the design. The field in the Target 0 register is used.
25	0h RW	**Peripheral Channel Unsupported Request Reporting Enable (PCURRE):** See PCERR_SLV0.PCURRE.
24	0h RW/1C/V	**Peripheral Channel Unsupported Request Detected (PCURD):** See PCERR_SLV0.PCURD
23:15	0h RO	Reserved.
14:13	0h RW	**Peripheral Channel Non-Fatal Error Reporting Enable (PCNFEE):** See PCERR_SLV0.PCNFEE.
12	0h RW/1C/V	**Peripheral Channel Non-Fatal Status (PCNFES):** See PCERR_SLV0.PCNFES.
11:8	0h RO/V	**Peripheral Channel Non-Fatal Cause (PCNFEC):** See PCERR_SLV0.PCNFEC.
7	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
6:5	0h RW	**Peripheral Channel Fatal Error Reporting (PCFEE):** See PCERR_SLV0.PCFEE.
4	0h RW/1C/V	**Peripheral Channel Fatal Error Reporting (PCFES):** See PCERR_SLV0.PCFES.
3:0	0h RO/V	**Peripheral Channel Fatal Error Cause (PCFEC):** See PCERR_SLV0.PCFEC.

11.2.5 Virtual Wire Channel Error for Target 0 (VWERR_SLV0)—Offset 4030h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27	0h RW/L	**Initiator NMIOUT (Virtual Wire) to Target Enable (VWNMIOE):** 1'b0: Disable NMIOUT# reporting (NMI#_Sent indication from ITSS is ignored) 1'b1: Enable NMIOUT# reporting to Target via eSPI Virtual Wire (upon receiving a NMI#_Sent indication from ITSS)**Note:** This bit is locked when VWNSMIEL = 1.
26	0h RW/L	**Initiator SMIOUT (Virtual Wire) to Target Enable (VWSMIOE):** 1'b0: Disable SMIOUT# reporting (SMI#_Sent indication from PMC is ignored) 1'b1: Enable SMIOUT# reporting to Target via eSPI Virtual Wire (upon receiving a SMI#_Sent indication from PMC)**Note:** This bit is locked when VWNSMIEL = 1.
25:15	0h RO	Reserved.
14:13	0h RW	**Virtual Wire Channel Non-Fatal Error Reporting Enable (VWNFEE):** 00: Disable Non-Fatal Error Reporting 01: Reserved 10: Enable Non-Fatal Error Reporting as SERR (SB Do_SErr message) 11: Enable Non-Fatal Error Reporting as SMI (SB Assert_SMI message) Notes: 1. SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. 2. SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. 3. SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
12	0h RW/1C/V	**Virtual Wire Channel Non-Fatal Error Status (VWNFES):** This field is set by hardware if a Non-Fatal Error condition is detected on the Virtual Wire Channel. Software must clear this bit. 0: No Non-Fatal Error detected 1: Non-Fatal Error detected (VWNFEC has a non-zero value) Notes: 1. Clearing this unlocks the VWNFEC field and triggers an SB Deassert_SMI message if VWNFEE is set to SMI. 2. Setting of this bit is independent of the enable to generate a SMI/SERR (VWNFEE).

Bit Range	Default & Access	Field Name (ID): Description
11:8	0h RO/V	**Virtual Wire Channel Non-Fatal Error Cause (VWNFEC):** 0h: No error 1h: Target Response Code: NONFATAL_ERROR 2h – Dh: Reserved Eh: Target Virtual Wire: NON_FATAL_ERROR: 0 to 1 transition (1 to 0 transition on this VW is ignored) Fh: Reserved Note: This field is updated after a Virtual Wire Channel transaction is completed if the VWNFES bit is not set.
7	0h RO	Reserved.
6:5	0h RW	**Virtual Wire Channel Fatal Error Reporting Enable (VWFEE):** 00: Disable Fatal Error Reporting 01: Reserved 10: Enable Fatal Error Reporting as SERR (IOSF-SB Do_SErr message) 11: Enable Fatal Error Reporting as SMI (SB Assert_SMI message) Notes: 1. SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. 2. SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. 3. SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
4	0h RW/1C/V	**Virtual Wire Channel Fatal Error Status (VWFES):** This field is set by hardware if a Fatal Error condition is detected on the Virtual Wire Channel. Software must clear this bit by writing all 1s to it. 0: No Fatal Error detected 1: Fatal Error Type 2 detected (VWFEC has a non-zero value) Notes: 1. Clearing this unlocks the VWFEC field and triggers an SB Deassert_SMI message if VWFEE is set to SMI. 2. Setting of this bit is independent of the enable to generate a SMI/SERR (VWFEE).
3:0	0h RO/V	**Virtual Wire Channel Fatal Error Cause (VWFEC):** 0h: No error 1h – 7h: Reserved 8h: Malformed Target Response Payload: VW Count > Max. VW Count [Type 2] 9h – 4'hD: Reserved Eh: Target Virtual Wire: FATAL_ERROR 0 to 1 transition (1 to 0 transition on this VW is ignored) [Type 2] Fh: Reserved Note: This field is updated after a Virtual Wire Channel transaction is completed if the VWFES bit is not set.

11.2.6 Virtual Wire Channel Error for Target 1 (VWERR_SLV1)—Offset 4034h

This register is used to control error reporting for the eSPI Virtual Wire Channel for the second eSPI Target device.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
27	0h RO	**Initiator NMIOUT (Virtual Wire) to Target Enable (VWNMIOE):** These bits are not supported. The corresponding bits for Target0 in VWERR_SLV0 register cover NMI# and SMI# transmission to both Targets.
26	0h RO	**Initiator SMIOUT (Virtual Wire) to Target Enable (VWSMIOE):** These bits are not supported. The corresponding bits for Target0 in VWERR_SLV0 register cover NMI# and SMI# transmission to both Targets.
25:15	0h RO	Reserved.
14:13	0h RW	**Virtual Wire Channel Non-Fatal Error Reporting Enable (VWNFEE):** See VWERR_SLV0.VWNFEE.
12	0h RW/1C/V	**Virtual Wire Channel Non-Fatal Error Status (VWNFES):** See VWERR_SLV0.VWNFES.
11:8	0h RO/V	**Virtual Wire Channel Non-Fatal Error Cause (VWNFEC):** See VWERR_SLV0.VWNFEC.
7	0h RO	Reserved.
6:5	0h RW	**Virtual Wire Channel Fatal Error Reporting Enable (VWFEE):** See VWERR_SLV0.VWFEE.
4	0h RW/1C/V	**Virtual Wire Channel Fatal Error Status (VWFES):** See VWERR_SLV0.VWFES.
3:0	0h RO/V	**Virtual Wire Channel Fatal Error Cause (VWFEC):** See VWERR_SLV0.VWFEC.

11.2.7 Flash Access Channel Error for Target 0 (FCERR_SLV0)—Offset 4040h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 40080h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
17	0h RO	Reserved.
15	0h RO	Reserved.
14:13	0h RW	**Flash Access Channel Non-Fatal Error Reporting Enable (FCNFEE):** 00: Disable Non-Fatal Error Reporting 01: Reserved 10: Enable Non-Fatal Error Reporting as SERR (SB Do_SErr message) 11: Enable Non-Fatal Error Reporting as SMI (SB Assert_SMI message) Notes: 1. SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. 2. SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. 3. SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C/V	**Flash Access Channel Non-Fatal Error Status (FCNFES):** This field is set by hardware if a Non-Fatal Error condition is detected on the Flash Access Channel. Software must clear this bit. 0: No Non-Fatal Error detected 1: Non-Fatal Error detected (FCNFEC has a non-zero value) Notes: 1. Clearing this unlocks the FCNFEC field and triggers an SB Deassert_SMI message if FCNFEE is set to SMI. 2. Setting of this bit is independent of the enable to generate a SMI/SERR (FCNFEE).
11:8	0h RO/V	**Flash Access Channel Non-Fatal Error Cause (FCNFEC):** 0h: No error 1h: Target Response Code: NONFATAL_ERROR received in response to GET_FLASH_NP, PUT_FLASH_C [for Initiator-Attached Flash accesses only] 2h: Reserved 3h: Reserved 4h: Unsupported Cycle Type (w.r.t. Command) 5h: Reserved 6h: Unsupported Address (i.e., address > Flash linear address range) [for Initiator-Attached Flash accesses only] set to Flash Access Error 7h: Reserved 8h-Fh: Reserved Note: This field is updated after a Flash Access Channel transaction is completed if the FCNFES bit is not set
7	1h RW	**Initiator Attached Flash Request Priority (MAFRP)**
6:5	0h RW	**Flash Access Channel Fatal Error Reporting Enable (FCFEE):** 00: Disable Fatal Error Reporting 01: Reserved 10: Enable Fatal Error Reporting as SERR (SB Do_SErr message) 11: Enable Fatal Error Reporting as SMI (SB Assert_SMI message) Notes: 1. SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. 2. SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. 3. SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
4	0h RW/1C/V	**Flash Access Channel Fatal Error Status (FCFES):** This field is set by hardware if a Fatal Error condition is detected on the Flash Access Channel. Software must clear this bit by writing a 1 to it. 0: No Fatal Error detected 1: Fatal Error Type 2 detected (FCFEC has a non-zero value) Notes: 1. Clearing this unlocks the FCFEC field and triggers an IOSF-SB Deassert_SMI message if FCFEE is set to SMI. 2. Setting of this bit is independent of the enable to generate a SMI/SERR (FCFEE).
3:0	0h RO/V	**Flash Access Channel Fatal Error Cause (FCFEC):** 0h: No error 1h – 7h: Reserved 8h: Malformed Target Response Payload: Payload length > Max Payload Size [Type 2] 9h: Malformed Target Response Payload: Read request size > Max Read Request Size [for Initiator-Attached Flash accesses only] [Type 2] Ah – Fh: Reserved Note: This field is updated after a Flash Access Channel transaction is completed if the FCFES bit is not set.

11.2.8 Link Error for Target 0 (LNKERR_SLV0)—Offset 4050h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: FF00h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**eSPI Link and Target Channel Recovery Required (SLCRR):** HW sets this bit when it has detected a Type 1 Fatal Error condition, for any channel (LFET1C is non-zero). Setting of this bit will trigger an error handling sequence by the eSPI-MC, followed by the suspension of all HW initiated transactions on the eSPI link with the Target. SW must clear this bit (by writing a 1 to it) after it has taken all necessary actions to recover the link. This indicates the eSPI-MC to resume HW initiated transactions with the Target.
30:23	0h RO	Reserved.
22:21	0h RW	**Fatal Error Type 1 Reporting Enable (LFET1E):** 00: Disable Fatal Error Type 1 Reporting 01: Reserved 10: Enable Fatal Error Type 1 Reporting as SERR (IOSF-SB Do_SErr message) 11: Enable Fatal Error Type 1 Reporting as SMI (IOSF-SB Assert_SMI message) Notes: 1. SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. 2. SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. 3. SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted). 4. When this error is reported, SW must also inspect and handle the SLCRR field.
20	0h RW/1C/V	**Fatal Error Type 1 Reporting Status (LFET1S):** This field is set by hardware if a Link Fatal Error Type 1 condition is detected on the eSPI link (any transaction). Software must clear this bit by writing a 1 to it. 0: No Link Fatal Error Type 1 detected 1: Fatal Error Type 1 detected (LFET1C has a non-zero value) Note: 1. Clearing this unlocks the LFET1C field and triggers an IOSF-SB Deassert_SMI message if LFET1E is set to SMI. 2. Setting of this bit is independent of the enable to generate a SMI/SERR (LFET1E).
19:16	0h RO/V	**Link Fatal Type 1 cause (LFET1C):** 4'h0: No error 4'h1: Target Response Code: NO_RESPONSE [Type 1] 4'h2: Target Response Code: FATAL_ERROR [Type 1] 4'h3: Target Response Code: CRC_ERROR [Type 1] 4'h4: Invalid Target Response Code (w.r.t. to Command) [Type 1] 4'h5: Invalid Target Cycle Type (w.r.t. to Command) [Type 1] 4'h6 - 4'hF: Reserved Note: 1. This field is updated after a transaction (any channel) is completed if the LFET1S bit is clear. 2. A non-zero value in this field also causes the SLCRR bit to be set.
15:8	FFh RO/V	**Link Fatal Error Type 1 Cycle Type (LFET1CTYP)**
7:0	0h RO/V	**Link Fatal Error Type 1 Command (LFET1CMD)**

11.2.9 Link Error for Target 1 (LNKERR_SLV1)—Offset 4054h

This register is used to log and control link error reporting for the second eSPI Target device.
The register definition is identical to that of LNKERR_SLV0.

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12 P2SB Bridge (D31:F1)

12.1 P2SB PCI Configuration Registers

Table 12-1. Summary of P2SB PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	PCI Identifier (PCIID)—Offset 0h	XXXX8086h
4h	5h	PCI Command (PCICMD)—Offset 4h	4h
Eh	Eh	PCI Header Type (PCIHTYPE)—Offset Eh	0h
10h	13h	Sideband Register Access BAR (SBREG_BAR)—Offset 10h	4h
14h	17h	Sideband Register BAR High DWORD (SBREG_BARH)—Offset 14h	0h
2Ch	2Fh	PCI Subsystem Identifiers (PCIHSS)—Offset 2Ch	0h
50h	51h	VLW Bus:Device:Function (VBDF)—Offset 50h	F8h
52h	53h	ERROR Bus:Device:Function (EBDF)—Offset 52h	F8h
54h	57h	Routing Configuration (RCFG)—Offset 54h	C700h
60h	60h	High Performance Event Timer Configuration (HPTC)—Offset 60h	0h
64h	65h	IOxAPIC Configuration (IOAC)—Offset 64h	0h
6Ch	6Dh	IOxAPIC Bus:Device:Function (IBDF)—Offset 6Ch	F8h
70h	71h	HPET Bus:Device:Function (HBDF)—Offset 70h	F8h
C0h	C3h	Display Bus:Device:Function (DISPBDF)—Offset C0h	60010h
C4h	C5h	ICC Register Offsets (ICCOS)—Offset C4h	0h
D0h	D3h	SBI Address (SBIADDR)—Offset D0h	0h
D4h	D7h	SBI Data (SBIDATA)—Offset D4h	0h
D8h	D9h	SBI Status (SBISTAT)—Offset D8h	0h
DAh	DBh	SBI Routing Identification (SBIRID)—Offset DAh	0h
DCh	DFh	SBI Extended Address (SBIEXTADDR)—Offset DCh	0h
E0h	E3h	P2SB Control (P2SBC)—Offset E0h	0h
E4h	E4h	Power Control Enable (PCE)—Offset E4h	1h
200h	203h	Sideband Register Posted 0 (SBREGPOSTED0)—Offset 200h	0h
204h	207h	Sideband Register Posted 1 (SBREGPOSTED1)—Offset 204h	0h
208h	20Bh	Sideband Register Posted 2 (SBREGPOSTED2)—Offset 208h	0h
20Ch	20Fh	Sideband Register Posted 3 (SBREGPOSTED3)—Offset 20Ch	0h
210h	213h	Sideband Register Posted 4 (SBREGPOSTED4)—Offset 210h	0h
214h	217h	Sideband Register Posted 5 (SBREGPOSTED5)—Offset 214h	0h
218h	21Bh	Sideband Register Posted 6 (SBREGPOSTED6)—Offset 218h	0h
21Ch	21Fh	Sideband Register Posted 7 (SBREGPOSTED7)—Offset 21Ch	0h
220h	223h	Endpoint Mask 0 (EPMASK0)—Offset 220h	0h
224h	227h	Endpoint Mask 1 (EPMASK1)—Offset 224h	0h
228h	22Bh	Endpoint Mask 2 (EPMASK2)—Offset 228h	0h
22Ch	22Fh	Endpoint Mask 3 (EPMASK3)—Offset 22Ch	0h

Table 12-1. Summary of P2SB PCI Configuration Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
230h	233h	Endpoint Mask 4 (EPMASK4)—Offset 230h	0h
234h	237h	Endpoint Mask 5 (EPMASK5)—Offset 234h	0h
238h	23Bh	Endpoint Mask 6 (EPMASK6)—Offset 238h	0h
23Ch	23Fh	Endpoint Mask 7 (EPMASK7)—Offset 23Ch	0h

12.1.1 PCI Identifier (PCIID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: XXXX8086h

Bit Range	Default and Access	Field Name (ID): Description
31:16	-- RO/V	**Device Identification (DID):** Indicates the device identification.
15:0	8086h RO	**Vendor Identification (VID):** Indicates Intel

12.1.2 PCI Command (PCICMD)—Offset 4h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 1

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RO	**Interrupt Disable (INTD):** P2SB does not issue any interrupts on its own behalf
9	0h RO	**Fast Back to Back Enable (FB2BE):** Not applicable
8:6	0h RO	Reserved.
5	0h RO	**VGA Palette Snoop (VGA):** Not applicable.
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** Not applicable.
3	0h RO	**Special Cycle Enable (SCE):** Not applicable.

Bit Range	Default and Access	Field Name (ID): Description
2	1h RO	**Bus Initiator Enable (BME):** Bus Initiatoring cannot be disabled as this device acts as a proxy for non-PCI devices.
1	0h RW	**Memory Space Enable (MSE):** Will control the P2SB acceptance of PCI MMIO BARs only. Other legacy regions are unaffected by this bit.
0	0h RW	**I/O Space Enable (IOSE):** Legacy regions are unaffected by this bit.

12.1.3 PCI Header Type (PCIHTYPE)—Offset Eh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7	0h RO	**Multi-Function Device (MFD):** Indicates that this is part of a multi-function device.
6:0	0h RO	**Header Type (HTYPE):** Indicates a generic device header.

12.1.4 Sideband Register Access BAR (SBREG_BAR)—Offset 10h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RW	**Register Base Address (RBA):** Lower DWORD of the base address for the sideband register access BAR.
23:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PREF):** Indicates this is not prefetchable.
2:1	2h RO	**Address Type (ATYPE):** Indicates that this can be placed anywhere in 64b space.
0	0h RO	**Space Type (STYPE):** Indicates memory space

12.1.5 Sideband Register BAR High DWORD (SBREG_BARH)—Offset 14h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Register Base Address (RBAH):** Upper DWORD of the base address for the sideband register access BAR.

12.1.6 PCI Subsystem Identifiers (PCIHSS)—Offset 2Ch

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SSID):** Written by BIOS. Not used by hardware.
15:0	0h RW/O	**Subsystem Vendor ID (SSVID):** Written by BIOS. Not used by hardware.

12.1.7 VLW Bus:Device:Function (VBDF)—Offset 50h

This register specifies the bus:device:function ID that will be used for its Requester ID. This field is default to Bus 0: Device 31: Function 0 after reset. BIOS shall program this field accordingly if unique bus:device:function number is required.

Access Method

Type: CFG Register (Size: 16 bits)
Device: 31
Function: 1

Default: F8h

Bit Range	Default and Access	Field Name (ID): Description
15:8	0h RW	**Bus Number (BUS):** VLW Bus Number
7:3	1Fh RW	**Device Number (DEV):** VLW Device Number

Bit Range	Default and Access	Field Name (ID): Description
2:0	0h RW	**Function Number (FUNC):** VLW Function Number

12.1.8 ERROR Bus:Device:Function (EBDF)—Offset 52h

This register specifies the bus:device:function ID that the Error Signaling messages will use for its Requester ID. This field is default to Bus 0: Device 31: Function 0 after reset. BIOS shall program this field accordingly if unique bus:device:function number is required.

Access Method

Type: CFG Register (Size: 16 bits)
Device: 31
Function: 1

Default: F8h

Bit Range	Default and Access	Field Name (ID): Description
15:8	0h RW	**Bus Number (BUS):** ERROR Bus Number
7:3	1Fh RW	**Device Number (DEV):** ERROR Device Number
2:0	0h RW	**Function Number (FUNC):** ERROR Function Number

12.1.9 Routing Configuration (RCFG)—Offset 54h

This register contains information used for routing transactions between primary and sideband interfaces.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: C700h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	C7h RW	**Reserved Page Register Destination ID (RPRID):** Specifies the IOSF-SB destination ID for sending Reserved Page Register cycles (e.g. Port 80h). By default this will load to the ID of eSPI device if it's enabled by pin strap.
7:1	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
0	0h RW	**RTC Shadow Enable (RSE):** When set, all IO writes to the RTC will be also sent to the PMC. This allows cases where the battery backed storage is in an external PMIC.

12.1.10 High Performance Event Timer Configuration (HPTC)—Offset 60h

HPET configuration register

Access Method

Type: CFG Register (Size: 8 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7	0h RW	**Address Enable (AE):** When set, the P2SB will decode the High Performance Timer memory address range selected by bits 1:0 below.
6:2	0h RO	Reserved.
1:0	0h RW	**Address Select (AS):** This 2-bit field selects 1 of 4 possible memory address ranges for the High Performance Timer functionality. The encodings are: 00 : FED0_0000h - FED0_03FFFh 01 : FED0_1000h - FED0_13FFFh 10 : FED0_2000h - FED0_23FFFh 11 : FED0_3000h - FED0_33FFFh

12.1.11 IOxAPIC Configuration (IOAC)—Offset 64h

IOAPIC configuration register

Access Method

Type: CFG Register (Size: 16 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:9	0h RO	Reserved.
8	0h RW	**Address Enable (AE):** When set, the P2SB will decode the IOxAPIC memory address range selected by bits 7:0 below.
7:0	0h RW	**APIC Range Select (ASEL):** These bits define address bits 19:12 for the IOxAPIC range. The default value of 00h enables compatibility with prior products as an initial value. This value must not be changed unless the IOxAPIC Enable bit is cleared.

12.1.12 IOxAPIC Bus:Device:Function (IBDF)—Offset 6Ch

This register specifies the bus:device:function ID that the IOxAPIC will use in the following : As the Requester ID when initiating Interrupt Messages to the CPU As the Completer ID when responding to the reads targeting the IOxAPICs Memory-Mapped I/O registers This field is default to Bus 0: Device 31: Function 0 after reset. BIOS shall program this field accordingly if unique bus:device:function number is required for the internal IOxAPIC.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 1

Default: F8h

Bit Range	Default and Access	Field Name (ID): Description
15:8	0h RW	**Bus Number (BUS):** IOxAPIC Bus Number
7:3	1Fh RW	**Device Number (DEV):** IOxAPIC Device Number
2:0	0h RW	**Function Number (FUNC):** IOxAPIC Function Number

12.1.13 HPET Bus:Device:Function (HBDF)—Offset 70h

This register specifies the bus:device:function ID that the HPET device will use in the following : As the Requester ID when initiating Interrupt Messages to the CPU As the Completer ID when responding to the reads targeting the corresponding HPETs Memory-Mapped I/O registers This field is default to Bus 0: Device 31: Function 0 after reset. BIOS shall program this field accordingly if unique bus:device:function number is required for the corresponding HPET.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 1

Default: F8h

Bit Range	Default and Access	Field Name (ID): Description
15:8	0h RW	**Bus Number (BUS):** HPET Bus Number
7:3	1Fh RW	**Device Number (DEV):** HPET Device Number
2:0	0h RW	**Function Number (FUNC):** HPET Function Number

12.1.14 Display Bus:Device:Function (DISPBDF)—Offset C0h

This register specifies the bus:device:function ID that the Display initiated upstream RAVDMs will use for its Requester ID. This will also be used for the claiming these Route-by-ID RAVDMs downstream.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 60010h

Bit Range	Default and Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18:16	6h RW	**Display Target Block (DTBLK):** This register contains the Target BLK field that will be used when sending RAVDM messages to the CPU Complex North Display.
15:8	0h RW	**Bus Number (BUS):** The bus number of the Display in the CPU Complex.
7:3	2h RW	**Device Number (DEV):** The bus number of the Display in the CPU Complex.
2:0	0h RW	**Function Number (FUNC):** The function number of the Display in the CPU Complex

12.1.15 ICC Register Offsets (ICCOS)—Offset C4h

This register contains the offsets to be used when sending RAVDMs to the Integrated Clock Controller. Each of the two spaces decoded for the ICC have a separate base address that will be used when sending those transactions on IOSF-SB to the ICC.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:8	0h RW	**Modulator Control Address Offset (MODBASE):** This specifies the upper 8b for the 16b address that will be used for sending RAVDM access that target the Modulator Control range of the ICC (FFF00h - FFFFFh).
7:0	0h RW	**Buffer Address Offset (BUFBASE):** This specifies the upper 8b for the 16b address that will be used for sending RAVDM access that target the Buffer range of the ICC (FFE00h - FFEFFh).

12.1.16 SBI Address (SBIADDR)—Offset D0h

Provides mechanism to send message on IOSF-SB.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RW	**Destination Port ID (DESTID):** The content of this register field is sent in the IOSF Sideband Message Register Access dest field.
23:16	0h RO	Reserved.
15:0	0h RW	**Address Offset (OFFSET):** Register address offset. The content of this register field is sent in the IOSF Sideband Message Register Access address(15:0) field.

12.1.17 SBI Data (SBIDATA)—Offset D4h

Provides mechanism to send message on IOSFSB

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Data (DATA):** The content of this register field is sent on the IOSF sideband Message Register Access data(31:0) field.

12.1.18 SBI Status (SBISTAT)—Offset D8h

Provides mechanism to send message on IOSFSB

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:8	0h RW	**Opcode (OPCODE):** This is the Opcode sent in the IOSF sideband message.
7	0h RW	**Posted (POSTED):** When set to 1, the message will be sent as a posted message instead of non-posted. This should only be used if the receiver is known to support posted operations for the specified operation.
6:3	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
2:1	0h RW/V	**Response Status (RESPONSE):** 00 - Successful 01 - Unsuccessful / Not Supported 10 - Powered Down 11 - Multi-cast Mixed This register reflects the response status for the previously completed transaction. The value of this register is only meaningful if SBISTAT.INITRDY is zero.
0	0h RW/1S	**Initiate/ Ready# (INITRDY):** 0: The IOSF sideband interface is ready for a new transaction 1: The IOSF sideband interface is busy with the previous transaction. A write to set this register bit to 1 will trigger an IOSF sideband message on the private IOSF sideband interface. The message will be formed based on the values programmed in the Sideband Message Interface Register Access registers. Software needs to ensure that the interface is not busy (SBISTAT.INITRDY is clear) before writing to this register.

12.1.19 SBI Routing Identification (SBIRID)—Offset DAh

Provides mechanism to send message on IOSFSB

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:12	0h RW	**First Byte Enable (FBE):** The content of this field is sent in the IOSF Sideband Register Access FBE field.
11	0h RO	Reserved.
10:8	0h RW	**Base Address Register (BAR):** The contents of this field are sent in the IOSF Sideband Register Access BAR field. This should be zero performing a Memory Mapped operation to a PCI compliant device.
7:0	0h RW	**Function ID (FID):** The contents of this field are sent in the IOSF Sideband Register access FID field. This field should generally remain at zero unless specifically required by a particular application.

12.1.20 SBI Extended Address (SBIEXTADDR)—Offset DCh

Provides mechanism to send message on IOSFSB

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Extended Address (ADDR):** The content of this register field is sent on the IOSF sideband Message Register Access address(48:32) field. This must be set to all 0 if 16b addressing is desired.

12.1.21 P2SB Control (P2SBC)—Offset E0h

P2SB general configuration register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW/O	**SBI register Lock (SBILOCK):** Once written, it will not be writable until reset. When 1, the bit will lock down access to the P2SB SBI register (P2SB PCI offsets D0h - DFh)
30:18	0h RO	Reserved.
17	0h RW/1L	**Endpoint Mask Lock (MASKLOCK):** Locks the value of the EPMASK[0-7] registers. Once this value is written to a one it may only be cleared by a reset.
16:9	0h RO	Reserved.
8	0h RW	**Hide Device (HIDE):** When this bit is set, the P2SB will return 1s on any PCI Configuration Read on IOSF-P. All other transactions including PCI Configuration Writes are unaffected by this. This does not affect reads performed on the IOSF-SB interface.
7:0	0h RO	Reserved.

12.1.22 Power Control Enable (PCE)—Offset E4h

Power Control Enable register

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 1

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
7:6	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
5	0h RW	**Hardware Autonomous Enable (HAE):** When set, the P2SB will automatically engage power gating when it has reached its idle condition.
4:3	0h RO	Reserved.
2	0h RO	**D3-Hot Enable (D3HE):** No support for D3 Hot power gating.
1	0h RO	**I3 Enable (I3E):** No support for S0i3 power gating.
0	1h RW	**PMC Power Gating Enable (PMCPG_EN):** When set to 1, the P2SB will engage power gating if it is idle (and an internal PMC power gating signal is asserted.)

12.1.23 Sideband Register Posted 0 (SBREGPOSTED0)—Offset 200h

Provides a mechanism to send MMIO writes as posted writes on the IOSFSB space.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register Posted 0 (SBREGPOSTED0):** One hot masks for setting SBREG to posted posted for IOSF-SB endpoint IDs 31-0.

12.1.24 Sideband Register Posted 1 (SBREGPOSTED1)—Offset 204h

Provides an mechanism to send MMIO writes as posted writes on the IOSFSB space.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register Posted 1 (SBREGPOSTED1):** One hot masks for setting SBREG to posted posted for IOSF-SB endpoint IDs 63-32.

12.1.25 Sideband Register Posted 2 (SBREGPOSTED2)—Offset 208h

Provides an mechanism to send MMIO writes as posted writes on the IOSFSB space.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register Posted 0 (SBREGPOSTED2):** One hot masks for setting SBREG to posted posted for IOSF-SB endpoint IDs 95-64.

12.1.26 Sideband Register Posted 3 (SBREGPOSTED3)—Offset 20Ch

Provides a mechanism to send MMIO writes as posted writes on the IOSFSB space.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register Posted 3 (SBREGPOSTED3):** One hot masks for setting SBREG to posted posted for IOSF-SB endpoint IDs 127-96.

12.1.27 Sideband Register Posted 4 (SBREGPOSTED4)—Offset 210h

Provides a mechanism to send MMIO writes as posted writes on the IOSFSB space.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register Posted 4 (SBREGPOSTED4):** One hot masks for setting SBREG to posted posted for IOSF-SB endpoint IDs 159-128.

12.1.28 Sideband Register Posted 5 (SBREGPOSTED5)—Offset 214h

Provides a mechanism to send MMIO writes as posted writes on the IOSFSB space.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register Posted 5 (SBREGPOSTED5):** One hot masks for setting SBREG to posted posted for IOSF-SB endpoint IDs 191-160.

12.1.29 Sideband Register Posted 6 (SBREGPOSTED6)—Offset 218h

Provides a mechanism to send MMIO writes as posted writes on the IOSFSB space.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register Posted 6 (SBREGPOSTED6):** One hot masks for setting SBREG to posted posted for IOSF-SB endpoint IDs 223-192.

12.1.30 Sideband Register Posted 7 (SBREGPOSTED7)—Offset 21Ch

Provides a mechanism to send MMIO writes as posted writes on the IOSFSB space.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register Posted 7 (SBREGPOSTED7):** One hot masks for setting SBREG to posted posted for IOSF-SB endpoint IDs 255-224.

12.1.31 Endpoint Mask 0 (EPMASK0)—Offset 220h

Provides a mechanism for disabling particular IOSF-SB endpoints from being allowed to targeted by transactions from the P2SB.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 0 (EPMASK0):** One hot masks for disabling IOSF-SB endpoint IDs 31-0.

12.1.32 Endpoint Mask 1 (EPMASK1)—Offset 224h

Provides a mechanism for disabling particular IOSF-SB endpoints from being allowed to targeted by transactions from the P2SB.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 1 (EPMASK1):** One hot masks for disabling IOSF-SB endpoint IDs 63-32.

12.1.33 Endpoint Mask 2 (EPMASK2)—Offset 228h

Provide a mechanism for disabling particular IOSF-SB endpoints from being allowed to targeted by transactions from the P2SB.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 2 (EPMASK2):** One hot masks for disabling IOSF-SB endpoint IDs 95-64

12.1.34 Endpoint Mask 3 (EPMASK3)—Offset 22Ch

Provides a mechanism for disabling particular IOSF-SB endpoints from being allowed to targeted by transactions from the P2SB.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 3 (EPMASK3):** One hot masks for disabling IOSF-SB endpoint IDs 127-96

12.1.35 Endpoint Mask 4 (EPMASK4)—Offset 230h

Provides a mechanism for disabling particular IOSF-SB endpoints from being allowed to targeted by transactions from the P2SB.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 4 (EPMASK4):** One hot masks for disabling IOSF-SB endpoint IDs 128-159

12.1.36 Endpoint Mask 5 (EPMASK5)—Offset 234h

Provides a mechanism for disabling particular IOSF-SB endpoints from being allowed to targeted by transactions from the P2SB.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 5 (EPMASK5):** One hot masks for disabling IOSF-SB endpoint IDs 191-160

12.1.37 Endpoint Mask 6 (EPMASK6)—Offset 238h

Provides a mechanism for disabling particular IOSF-SB endpoints from being allowed to targeted by transactions from the P2SB.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 6 (EPMASK6):** One hot masks for disabling IOSF-SB endpoint IDs 223-192

12.1.38 Endpoint Mask 7 (EPMASK7)—Offset 23Ch

Provides a mechanism for disabling particular IOSF-SB endpoints from being allowed to targeted by transactions from the P2SB.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 7 (EPMASK7):** One hot masks for disabling IOSF-SB endpoint IDs 255-224

13 PMC Controller (D31:F2)

13.1 Power Management Configuration

The power management registers are distributed within the PCI Device 31: Function 2 space, with dedicated I/O and memory-mapped spaces. Bits not explicitly defined in each register are assumed to be reserved. Writes to reserved bits must retain their previous values. Other than a read/modify/write, software should not attempt to use the value read from a reserved bit, as it may not be consistently 1 or 0.

Table 13-1. Summary of Bus: 0, Device: 31, Function: 2 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device Vendor ID (DEVVENDID)	00008086h
4h	4	STATUSCOMMAND Status and Command (STATUSCOMMAND)	00100000h
8h	4	Revision Class Codes (REVCLASSCODE)	00000000h
Ch	4	CLLATHEADERBIST Cache Line Latency Header And BIST (CLLATHEADERBIST)	00000000h
10h	4	32-bit Base Address Register (BAR)	00000004h
14h	4	BAR HIGH (BAR_HIGH)	00000000h
18h	4	32-bit Base Address Register1 (BAR1)	00000004h
1Ch	4	BAR1 HIGH (BAR1_HIGH)	00000000h
20h	4	BAR2	00000001h
2Ch	4	Subsystem Identifiers (SUBSYSTEMID)	00000000h
30h	4	EXPANSION ROM BASEADDR (EXPANSION_ROM_BASEADDR)	00000000h
34h	4	CAPABILITY PTR (CAPABILITYPTR)	00000080h
3Ch	4	INTERRUPT REG Interrupt Register (INTERRUPTREG)	00000000h
80h	4	POWER CAP ID PowerManagement Capability ID (POWERCAPID)	48030001h
84h	4	PME CTRL STATUS (PMECTRLSTATUS)	00000008h
90h	4	PCIDEVIDLE CAP RECORD (PCIDEVIDLE_CAP_RECORD)	F0140009h
94h	4	DEVID VEND SPECIFIC REG (DEVID_VEND_SPECIFIC_REG)	01400010h
98h	4	D0I3 CONTROL SW LTR MMIO REG (D0I3_CONTROL_SW_LTR_MMIO_REG)	00000000h
9Ch	4	DEVICE IDLE POINTER REG (DEVICE_IDLE_POINTER_REG)	00000000h
A0h	4	D0I3 MAX POW LAT PG CONFIG (D0I3_MAX_POW_LAT_PG_CONFIG)	00000800h
B0h	4	GEN REGRW1 (GEN_REGRW1)	00000000h
B4h	4	GEN REGRW2 (GEN_REGRW2)	00000000h
B8h	4	GEN REGRW3 (GEN_REGRW3)	00000000h
BCh	4	GEN REGRW4 (GEN_REGRW4)	00000000h
C0h	4	GEN INPUT REG (GEN_INPUT_REG)	00000000h

13.1.1 Device Vendor ID (DEVVENDID) — Offset 0h

Device Vendor ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 0h	00008086h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Device Identification (DEVICEID):** These bits are controlled as follows: Bits [15:10]: hardwired (101111 for SPT-LP) Bits [9:7]: fuses (global device ID - 000 by default) Bits [6:5]: hardwired (10 for SPT) Bits [4:0]: DID fuses (00 to 1F - variable).
15:0	8086h RO	**Vendor Identification (VENDORID):** Indicates Intel

13.1.2 STATUSCOMMAND Status and Command (STATUSCOMMAND) — Offset 4h

Status and Command

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 4h	00100000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW/1C	**RMA:** Received Initiator Abort
28	0h RW/1C	**RTA:** Received Target Abort
27:21	0h RO	**Reserved**
20	1h RO	**CAPLIST:** Capabilities List

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**INTR_STATUS:** Interrupt Status
18:11	0h RO	**Reserved**
10	0h RW	**INTR_DISABLE:** Interrupt Disable
9	0h RO	**Reserved**
8	0h RW	**SERR_ENABLE:** System Error Enable
7:3	0h RO	**Reserved**
2	0h RW	**BME:** Bus Initiator Enable
1	0h RW	**MSE:** Memory Space Enable
0	0h RO	**Reserved**

13.1.3 Revision Class Codes (REVCLASSCODE) — Offset 8h

Revision Class Codes

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**CLASS_CODES:** Class Codes
7:0	00h RO	**RID:** Revision ID

13.1.4 CLLATHEADERBIST Cache Line Latency Header And BIST (CLLATHEADERBIST) — Offset Ch

Cache Line Latency Header And BIST

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**MULFNDEV:** Multi Function Device
22:16	00h RO	**HEADERTYPE:** Header Type
15:8	00h RO	**LATTIMER:** Latency Timer
7:0	00h RW	**CACHELINE_SIZE:** Cacheline Size

13.1.5 32-bit Base Address Register (BAR) — Offset 10h

Base Address Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 10h	00000004h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:13	00000h RW	**BASEADDR:** Software programs this register with the base address of the device's memory region
12:4	000h RO	**Size Indicator (SIZEINDICATOR):** Hardwired to 0 to indicate 8KB of memory space
3	0h RO	**PREFETCHABLE:** A device can mark a range as prefetchable if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables. Hardwired to 0 to indicate the device's memory space as notprefetchable.
2:1	2h RO	**TYPE:** Hardwired to 10 to indicate that Base register is 64 bits wide and mapping can be done anywhere in the 64-bit Memory Space.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** Hardwired to 0 to identify a Memory BAR.

13.1.6 BAR HIGH (BAR_HIGH) — Offset 14h

BAR -Base Address Register High

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 14h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address HIGH (BASEADDR_HIGH):** Base Address

13.1.7 32-bit Base Address Register1 (BAR1) — Offset 18h

Base Address Register1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 18h	00000004h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**BASEADDR1:** Software programs this register with the base address of the device's memory region
11:4	00h RO	**Size Indicator (SIZEINDICATOR1):** Hardwired to 0 to indicate 4KB of memory space
3	0h RO	**PREFETCHABLE1:** A device can mark a range as prefetchable if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables. Hardwired to 0 to indicate the device's memory space as notprefetchable.
2:1	2h RO	**TYPE1:** Hardwired to 10 to indicate that Base register is 64 bits wide and mapping can be done anywhere in the 64-bit Memory Space.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** Hardwired to 0 to identify a Memory BAR.

13.1.8 BAR1 HIGH (BAR1_HIGH) — Offset 1Ch

BAR1 -Base Address Register High

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 1Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address HIGH (BASEADDR1_HIGH):** Base Address HIGH

13.1.9 BAR2 — Offset 20h

BAR -Base Address Register2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 20h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RW	**Base Address (BASEADDR):** Base Address
6:1	0h RO	**Reserved**
0	1h RO	**Message Space (MESSAGE_SPACE):** Hardwired to 1 to identify an IO BAR.

13.1.10 Subsystem Identifiers (SUBSYSTEMID) — Offset 2Ch

Subsystem Identifiers

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 2Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** Written by BIOS. Not used by hardware.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** Written by BIOS.Not used by hardware.

13.1.11 EXPANSION ROM BASEADDR (EXPANSION_ROM_BASEADDR) — Offset 30h

EXPANSION ROM base address

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 30h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Expansion ROM Base

13.1.12 CAPABILITY PTR (CAPABILITYPTR) — Offset 34h

CAPABILITYPTR - Capabilities Pointer

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 34h	00000080h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**CAPPTR_POWER:** Capabilities Pointer

13.1.13 INTERRUPT REG Interrupt Register (INTERRUPTREG) — Offset 3Ch

Interrupt Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 3Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**MAX_LAT:** Maximum Latency
23:16	00h RO	**MIN_GNT:** Minimum Gnt
15:12	0h RO	**Reserved**
11:8	0h RO	**INTPIN:** Interrupt Pin
7:0	00h RW	**INTLINE:** Interrupt Line

13.1.14 POWER CAP ID PowerManagement Capability ID (POWERCAPID) — Offset 80h

PowerManagement Capability ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 80h	48030001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	09h RO	**PMESUPPORT:** PME Support
26:19	0h RO	**Reserved**
18:16	3h RO	**VERSION:** Version
15:8	00h RO	**NXTCAP:** Next Capability
7:0	01h RO	**POWER_CAP:** Power Management Capability

13.1.15 PME CTRL STATUS (PMECTRLSTATUS) — Offset 84h

Power Management Control and Status Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 84h	00000008h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C	**PMESTATUS:** PME Status
14:9	0h RO	**Reserved**
8	0h RW	**PMEENABLE:** PME Enable
7:4	0h RO	**Reserved**
3	1h RO	**NO_SOFT_RESET:** NO SOFT RESET

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**Reserved**
1:0	0h RW	**POWERSTATE:** Power State

13.1.16 PCIDEVIDLE CAP RECORD (PCIDEVIDLE_CAP_RECORD) — Offset 90h

PCI DEVICE IDLE CAPABILITY RECORD

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 90h	F0140009h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**VEND_CAP:** Vendor Specific Capability ID
27:24	0h RO	**REVID:** Vendor Specific Capability Revision
23:16	14h RO	**CAP_LENGTH:** Vendor Specific Capability Length
15:8	00h RO	**NEXT_CAP:** NEXT Capability
7:0	09h RO	**CAPID:** Capability ID

13.1.17 DEVID VEND SPECIFIC REG (DEVID_VEND_SPECIFIC_REG) — Offset 94h

DEVID VENDOR SPECIFIC REG

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 94h	01400010h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**VSEC_LENGTH:** Vendor Specific Extended Capability Length
19:16	0h RO	**VSEC_REV:** Vendor Specific Extended Capability Revision
15:0	0010h RO	**VSECID:** Vendor Specific Extended Capability ID

13.1.18 D0I3 CONTROL SW LTR MMIO REG (D0I3_CONTROL_SW_LTR_MMIO_REG) — Offset 98h

SW LTR Update MMIO Location Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 98h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**SW_LAT_DWORD_OFFSET:** SW LTR Update MMIO Offset Location
3:1	0h RO	**SW_LAT_BAR_NUM:** SW LTR Bar Num
0	0h RO	**SW_LAT_VALID:** SW LTR Valid Strap

13.1.19 DEVICE IDLE POINTER REG (DEVICE_IDLE_POINTER_REG) — Offset 9Ch

Device IDLE pointer register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + 9Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**DWORD_OFFSET:** Device MMIO Offset Location
3:1	0h RO	**BAR_NUM:** D0i3 MMIO Location
0	0h RO	**VALID:** D0i3 Valid Strap

13.1.20 D0I3 MAX POW LAT PG CONFIG (D0I3_MAX_POW_LAT_PG_CONFIG) — Offset A0h

DEVICE PG CONFIG

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + A0h	00000800h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW	**HAE:** Hardware Autonomous Enable
20	0h RO	**Reserved**
19	0h RW	**SLEEP_EN:** Sleep Enable
18	0h RW	**PGE:** Power Gate Enable
17	0h RW	**I3_ENABLE:** I3 Enable
16	0h RW	**PMCRE:** PMC Request Enable
15:13	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
12:10	2h RW/O	**POW_LAT_SCALE:** Power On Latency Scale
9:0	000h RW/O	**POW_LAT_VALUE:** Power On Latency Value

13.1.21 GEN REGRW1 (GEN_REGRW1) — Offset B0h

General Purpose Read Write Register1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW1:** General Purpose PCI Register

13.1.22 GEN REGRW2 (GEN_REGRW2) — Offset B4h

General Purpose Read Write Register2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW2:** General Purpose PCI Register

13.1.23 GEN REGRW3 (GEN_REGRW3) — Offset B8h

General Purpose Read Write Register3

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW3:** General Purpose PCI Register

13.1.24 GEN REGRW4 (GEN_REGRW4) — Offset BCh

General Purpose Read Write Register4

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + BCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW4:** General Purpose PCI Register

13.1.25 GEN INPUT REG (GEN_INPUT_REG) — Offset C0h

General Purpose Input Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:31, F:2] + C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN REG INPUT_RW (GEN_REG_INPUT_RW):** General Purpose Input Register

13.2 PMC I/O Based Registers

The ACPI power management I/O registers are accessed based upon offsets from PM Base Address, BAR2, defined in PCI Device 31: Function 2.

Table 13-2. Summary of PMC I/O Based Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Power Management 1 Enables and Status (PM1_EN_STS)—Offset 0h	0h
4h	7h	Power Management 1 Control (PM1_CNT)—Offset 4h	0h
8h	Bh	Power Management 1 Timer (PM1_TMR)—Offset 8h	0h
20h	23h	Thermal Timer Delay (THERM_TIMER_DELAY)—Offset 20h	0h
30h	33h	SMI Control and Enable (SMI_EN)—Offset 30h	2h
34h	37h	SMI Status Register (SMI_STS)—Offset 34h	0h
40h	43h	General Purpose Event Control (GPE_CTRL)—Offset 40h	0h
50h	53h	PM2a Control Block (PM2A_CNT_BLK)—Offset 50h	0h
54h	57h	Over-Clocking WDT Control (OC_WDT_CTL)—Offset 54h	2000h
60h	63h	General Purpose Event 0 Status [31:0] (GPE0_STS_31_0)—Offset 60h	0h
64h	67h	General Purpose Event 0 Status [63:32] (GPE0_STS_63_32)—Offset 64h	0h
68h	6Bh	General Purpose Event 0 Status [95:64] (GPE0_STS_95_64)—Offset 68h	0h
6Ch	6Fh	General Purpose Event 0 Status [127:96] (GPE0_STS[127:96])—Offset 6Ch	0h
70h	73h	General Purpose Event 0 Enable [31:0] (GPE0_EN_31_0)—Offset 70h	0h
74h	77h	General Purpose Event 0 Enable [63:32] (GPE0_EN_63_32)—Offset 74h	0h
78h	7Bh	General Purpose Event 0 Enable [95:64] (GPE0_EN_95_64)—Offset 78h	0h
7Ch	7Fh	General Purpose Event 0 Enable [127:96] (GPE0_EN[127:96])—Offset 7Ch	0h

13.2.1 Power Management 1 Enables and Status (PM1_EN_STS)—Offset 0h

Power Management 1 Enables and Status

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30	0h RW	**PCI Express Wake Disable (PCIEXP_WAKE_DIS):** This bit disables the inputs to the PCIEXP_WAKE_STS bit in the PM1 Status register from waking the system. Modification of this bit has no impact on the value of the PCIEXP_WAKE_STS bit. This bit is reset by DSW_PWROK de-assertion.

Bit Range	Default & Access	Field Name (ID): Description
29:27	0h RO	Reserved.
26	0h RW/V	**RTC Alarm Enable (RTC_EN):** This is the RTC alarm enable bit. It works in conjunction with the SCI_EN bit as described below. RTC_EN: SCI_EN: Effect when RTC_STS is set 0: X: No SMI# or SCI. If system was in S3-S5, no wake even occurs. 1: 0: SMI#. If system was in S3-S5, then a wake event occurs before the SMI#. 1: 1: SCI. If system was in S3-S5, then a wake event occurs before the SCI. Note: This bit is in the RTC well and is reset by RTCRST# assertion, to allow an RTC event to wake after a power failure.
25	0h RO	Reserved.
24	0h RW/V	**Power Button Enable (PWRBTN_EN):** This bit is the power button enable. It works in conjunction with the SCI_EN bit as described below: PWRBTN_EN: SCI_EN: Effect when PWRBTN_STS is set 0: X: No SMI# or SCI 1: 0: SMI#. 1: 1: SCI. NOTE: PWRBTN_EN has no effect on the PWRBTN_STS bit being set by the assertion of the power button. The Power Button is always enabled as a Wake event.
23:22	0h RO	Reserved.
21	0h RW	**Global Enable (GBL_EN):** Global enable bit. When both the GBL_EN and the GBL_STS are set, PCH generates an SCI. This bit is reset by PLTRST# assertion.
20:17	0h RO	Reserved.
16	0h RW	**Timer Overflow Interrupt Enable (TMROF_EN):** This is the timer overflow interrupt enable bit. It works in conjunction with the SCI_EN bit as described below: TMROF_EN: SCI_EN: Effect when TMROF_STS is set 0: X: No SMI# or SCI. 1: 0: SMI#. 1: 1: SCI. This bit is reset by PLTRST# assertion.
15	0h RW/1C/V	**Wake Status (WAK_STS):** This bit is set when the system is in one of the Sleep states (via the SLP_EN bit) and an enabled PCH Wake event occurs. Upon setting this bit, the PCH will transition the system to the ON state. This bit can only be set by hardware and can only be cleared by writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST#. If a power failure occurs (such as removed batteries) without the SLP_EN bit set, the WAK_STS bit will not be set when the power returns if the AFTER_G3 bit is 0. If the AFTER_G3 bit is 1, then the WAK_STS bit will be set after waking from a power failure. If necessary, the BIOS can clear the WAK_STS bit in this case.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/1C/V	**PCI Express Wake Status (PCIEXP_WAKE_STS):** This bit is set by hardware to indicate that the system woke due to a PCI Express wakeup event. This event can be caused by the PCI Express WAKE# pin being active, or one or more of the PCI Express ports being in beacon state, or receipt of a PCI Express PME message at root port. This bit should only be set when one of these events causes the system to transition from a non-S0 system power state to the S0 system power state. This bit is set independant of the PCIEXP_WAKE_DIS bit. Software writes a 1 to clear this bit. If WAKE# pin is still active during the write or one or more PCI Express ports is in the beacon state or PME message received indication is not cleared in the root port, then the bit will remain active (i.e. all inputs to this bit are level sensitive) Note: This bit does not itself cause a wake event or prevent entry to a sleeping state. Thus if the bit is 1 and the system is put into a sleeping state, the system will not automatically wake.
13:12	0h RO	Reserved.
11	0h RW/1C/V	**Power Button Override (PWRBTNOR_STS):** This bit is set any time a Power Button Override Event occurs (i.e. the power button is pressed for at least 4 consecutive seconds), the corresponding bit is received in the SMBus Target message, the Intel(R)CSME-Initiated Power Button Override bit is set, the Intel(R)CSME-Initiated Host Reset with Power Down is set, or due to an internal thermal sensor catastrophic condition. These events cause an unconditional transition to the S5 state. The BIOS or SCI handler clears this bit by writing a 1 to it. This bit is not affected by hard resets via CF9h writes, and is not reset by RSMRST#. Thus, this bit is on RTC well and is preserved through power failures (reset by RTCRST#). Note that this bit is still asserted when the global SCI_EN is set to '1' then an SCI will be generated.
10	0h RW/1C/V	**RTC Status (RTC_STS):** This bit is set when the RTC generates an alarm (assertion of the IRQ8# signal), and is not affected by any other enable bit. See RTC_EN for the effect when RTC_STS goes active. This bit is only set by hardware and can only be reset by writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by DSW_PWROK de-assertion.
9	0h RO	Reserved.
8	0h RW/1C/V	**Power Button Status (PWRBTN_STS):** This bit is set when the PWRBTN# signal is asserted (low), independent of any other enable bit. See PWRBTN_EN for the effect when PWRBTN_STS goes active. PWRBTN_STS is always a wake event. This bit is only set by hardware and can be cleared by software writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by DSW_PWROK de-assertion. If the PWRBTN# signal is held low for more than 4 seconds, the PCH clears the PWRBTN_STS bit, sets the PWRBTNOR_STS bit, the system transitions to the S5 state, and only PWRBTN# is enabled as a wake event. If PWRBTN_STS bit is cleared by software while the PWRBTN# pin is still held low, this will not cause the PWRBTN_STS bit to be set. The PWRBTN# signal must go inactive and active again to set the PWRBTN_STS bit. Note that the SMBus Unconditional Powerdown message, the CPU Thermal Trip and the Internal Thermal Sensors' Catastrophic Condition result in behavior matching the Powerbutton Override, which includes clearing this bit.
7:6	0h RO	Reserved.
5	0h RW/1C/V	**GBL Status (GBL_STS):** This bit is set when an SCI is generated due to the BIOS wanting the attention of the SCI handler. BIOS has a corresponding bit, BIOS_RLS, which will cause an SCI and set this bit. The SCI handler should then clear this bit by writing a 1 to it. This bit will not cause wake events or SMI#. This bit is not effected by SCI_EN. Note: GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (which causes GBL_STS to be set) if the SCI handler is not in place. This bit is reset by PLTRST# assertion.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/1C/V	**Bus Initiator Status (BM_STS):** This bit is set to 1 by the PCH when a PCH-visible bus Initiator requests access to memory or the BM_BUSY# signal is active. This bit is cleared by the Processor writing a 1 to this bit position. This bit will not cause a wake event, SCI, or SMI. This bit is reset by PLTRST# assertion.
3:1	0h RO	Reserved.
0	0h RW/1C/V	**Timer Overflow Status (TMROF_STS):** This is the timer overflow status bit. This bit gets set anytime bit 22 of the 24 bit timer goes low (bits are counted from 0 to 23). This will occur every 2.3435 seconds. See TMROF_EN for the effect when TMROF_STS goes active. Software clears this bit by writing a 1 to it. This bit is reset by PLTRST# assertion.

13.2.2 Power Management 1 Control (PM1_CNT)—Offset 4h

Lockable: No Usage: ACPI or Legacy Power Well: Bits 0-9, 13-31: Primary, Bits 10-12: RTC Available: Desktop, Mobile

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	0h WO	**Sleep Enable (SLP_EN):** This is a write-only bit and reads to it always return a zero. Setting this bit causes the system to sequence into the Sleep state defined by the SLP_TYP field. This bit is reset by PLTRST# assertion.
12:10	0h RW	**Sleep Type (SLP_TYP):** This 3-bit field defines the type of Sleep the system should enter when the SLP_EN bit is set to 1. Bits Mode Typical Mapping 000 ON S0 001 Reserved 010 Reserved 011 Reserved 100 Reserved 101 Suspend-To-RAM S3 110 Suspend-To-Disk S4 111 Soft Off S5 These bits are reset by RTCRST# only.
9:3	0h RO	Reserved.
2	0h WO	**GBL_RLS (GBL_RLS):** This bit always reads as 0. ACPI software writes a '1' to this bit to raise an event to the BIOS. BIOS software has corresponding enable and status bits to control its ability to receive ACPI events.
1	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**SCI Enable (SCI_EN):** Selects the SCI interrupt or the SMI# for various events. 0 = These events will generate an SMI#. 1 = These events will generate an SCI. This bit is reset by PLTRST# assertion.

13.2.3 Power Management 1 Timer (PM1_TMR)—Offset 8h

Lockable: No
Usage: ACPI
Power Well: Primary

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:0	0h RO/V	**Timer Value (TMR_VAL):** This read-only field returns the running count of the PM timer. This counter runs off a 3.579545 MHz clock (derived from 14.31818 MHz divided by 4). It is reset (to 0) during a PCI reset, and then continues counting as long as the system is in the S0 state. Anytime bit 22 of the timer goes HIGH to LOW (bits referenced from 0 to 23), the TMROF_STS bit is set. The High-to-Low transition will occur every 2.3435 seconds. Writes to this register have no effect.

13.2.4 Thermal Timer Delay (THERM_TIMER_DELAY)—Offset 20h

Thermal timer delay register

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:0	0h RW	**Thermal Timer Delay (THERM_TIMER_DELAY_VALUE):** Thermal Timer Delay

13.2.5 SMI Control and Enable (SMI_EN)—Offset 30h

Lockable: No
Usage: ACPI or Legacy
Power Well: Primary
Note: This register is symmetrical to the SMI Status Register.

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 2h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**xHCI SMI Enable (xHCI_SMI_EN):** Software sets this bit to enable xHCI SMI events. This bit is reset by PLTRST# assertion.
30	0h RW	**Intel(R) CSME SMI Enable (ME_SMI_EN):** Software sets this bit to enable Intel(R)CSME SMI# events. This bit is reset by PLTRST# assertion.
29	0h RO	Reserved.
28	0h RW/L	**eSPI SMI Enable (ESPI_SMI_EN):** Software sets this bit to enable eSPI SMI events. This bit is reset by PLTRST# assertion.
27	0h RW/1S	**GPIO Unlock SMI Enable (GPIO_UNLOCK_SMI_EN):** Setting this bit will cause the PCH to generate an SMI# when the GPIO_UNLOCK_SMI_STS bit is set in the SMI_STS register. Once written to '1', this bit can only be cleared by PLTRST# assertion.
26:18	0h RO	Reserved.
17	0h RW	**Legacy USB 2 Enable (LEGACY_USB2_EN):** Enables legacy USB2 logic to cause SMI#.
16:15	0h RO	Reserved.
14	0h RW	**Periodic Enable (PERIODIC_EN):** Setting this bit will cause the PCH to generate an SMI# when the PERIODIC_STS bit is set in the SMI_STS register. This bit is reset by PLTRST# assertion.
13	0h RW/L	**TCO Enable (TCO_EN):** 1 = Enables the TCO logic to generate SMI#. 0 = Disables TCO logic from generating an SMI#. If the NMI2SMI_EN bit is set, then SMI's that are caused by NMI's (i.e. rerouted) will not be gated by the TCO_EN bit. Even if the TCO_EN bit is 0, the NMI's will still be routed to cause the SMI#. NOTE: This bit can not be written once the TCO_LOCK bit (at offset 08h of TCO I/O Space) is set. This prevents unauthorized software from disabling the generation of TCO-based SMI's. This bit is reset by PLTRST# assertion.
12	0h RO	Reserved.
11	0h RW	**Microcontroller SMI Enable (MCSMI_EN):** Software sets this bit to 1 to enables PCH to trap access to the microcontroller range (62h or 66h). A 'trapped' cycles will be claimed by PCH, but not forwarded to eSPI. An SMI# will also be generated. This bit is reset by PLTRST# assertion.

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RO	Reserved.
7	0h WO	**BIOS Release (BIOS_RLS):** Enables the generation of an SCI interrupt for ACPI software when a '1' is written to this bit position by BIOS software. This bit always reads a '0'. NOTE: GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (which causes GBL_STS to be set) if the SCI handler is not in place. This bit is reset by PLTRST# assertion.
6	0h RW	**Software SMI Timer Enable (SWSMI_TMR_EN):** Software sets this bit to a '1' to start the Software SMI# Timer. When the timer expires (depending on the SWSMI_RATE_SEL bits), it will generate an SMI# and set the SWSMI_TMR_STS bit. The SWSMI_TMR_EN bit will remain at 1 until software sets it back to 0. Clearing the SWSMI_TMR_EN bit before the timer expires will reset the timer and the SMI# will not be generated. The default for this bit is 0. This bit is reset by PLTRST# assertion.
5	0h RW	**APMC Enable (APMC_EN):** If set, this enables writes to the APM_CNT register to cause an SMI#. This bit is reset by PLTRST# assertion.
4	0h RW	**SMI On Sleep Enable (SMI_ON_SLP_EN):** If this bit is set, the PCH will generate an SMI# when a write access attempts to set the SLP_EN bit (in the PM1_CNT register). Furthermore, the PCH will not put the system to a sleep state. It is expected that the SMI# handler will turn off the SMI_ON_SLP_EN bit before actually setting the SLP_EN bit. This bit is reset by PLTRST# assertion.
3	0h RW	**Legacy USB Enable (LEGACY_USB_EN):** Enables legacy USB circuit to cause SMI#. This bit is reset by PLTRST# assertion.
2	0h RW	**BIOS Enable (BIOS_EN):** Enables the generation of SMI# when ACPI software writes a 1 to the GBL_RLS bit. Note that if the BIOS_STS bit, which gets set when software writes a 1 to GBL_RLS bit, is already a 1 at the time that BIOS_EN becomes 1, an SMI# will be generated when BIOS_EN gets set. This bit is reset by PLTRST# assertion.
1	1h RW/1S/V	**End of SMI (EOS):** This bit controls the arbitration of the SMI signal to the processor. This bit must be set in order for PCH to assert SMI# low to the processor after SMI# has been asserted previously. Once Intel ICH asserts SMI# low, the EOS bit is automatically cleared. In the SMI handler, the CPU should clear all pending SMIs (by servicing them and then clearing their respective status bits), set the EOS bit, and exit SMM. This will allow the SMI arbiter to reassert SMI upon detection of an SMI event and the setting of a SMI status bit. The SMI# signal will go inactive for 4 PCI clocks. This bit is reset by PLTRST# assertion.
0	0h RW/L	**Global SMI Enable (GBL_SMI_EN):** 0 = No SMI# will be generated by PCH. 1 = Enables the generation of SMI# in the system upon any enabled SMI event. NOTE: When the SMI_LOCK bit is set, this bit cannot be changed. This bit is reset by PLTRST# assertion.

13.2.6 SMI Status Register (SMI_STS)—Offset 34h

Lockable: No
Usage: ACPI or Legacy
Power Well: Primary
Note: If the corresponding _EN bit is set when the _STS bit is set, the PCH will cause an SMI# (except bits 8-10, which don't cause SMI#)

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**xHCI SMI Status (xHCI_SMI_STS):** This bit will be set when any USB3 (xHCI) Host Controller is requesting an SMI.
30	0h RO/V	**Intel(R) CSME SMI Status (ME_SMI_STS):** This bit will be set when Intel(R)CSME is requesting an SMI#.
29	0h RO	Reserved.
28	0h RO/V	**eSPI SMI Status (ESPI_SMI_STS):** This bit is set if an eSPI agent is requesting an SMI#. This bit is set by hardware and cleared when the PCH receives an eSPI SMI deassertion from an eSPI device.
27	0h RW/1C/V	**GPIO Unlock SMI Status (GPIO_UNLOCK_SMI_STS):** This bit will be set of the GPIO registers lockdown logic is requesting an SMI#. Writing a '1' to this bit position clears this bit to '0'. This bit is reset by PLTRST# assertion.
26	0h RO/V	**SPI_SMI Status (SPI_SMI_STS):** This bit will be set when the SPI logic is requesting an SMI#. This bit is read only because the sticky status and enable bits associated with this function are located in the SPI registers.
25:22	0h RO	Reserved.
21	0h RO/V	**Monitor Status (MONITOR_STS):** This bit will be set if the Trap/SMI logic has caused the SMI. This will occur when the CPU or a bus Initiator accesses an assigned register (or a sequence of accesses).
20	0h RO/V	**PCI_EXP_SMI Status (PCI_EXP_SMI_STS):** 1- PCI Express SMI event occurred. This could be due to a PCI Express PME event or Hot Plug Event.
19:17	0h RO	Reserved.
16	0h RW/1C/V	**SMBUS_SMI Status (SMBUS_SMI_STS):** 0 = This bit is set from the 64 KHz clock domain used by the SMBus. Software must wait at least 15.63 microseconds after initial assertion of this bit before clearing it. This bit is sticky and is cleared by writing a 1 to this bit position. 1 = Indicates that the SMI# was caused by: 1.The SMBus Target receiving a message that an SMI# should be caused, or 2. The SMBALERT# signal goes active and the SMB_SMI_EN bit is set and the SMBALERT_DIS bit is cleared, or 3. The SMBus Target receiving a HOST_NOTIFY message and the HOST_NOTIFY_INTREN and the SMB_SMI_EN bits are set, or 4. The SMBus Target receiving a “SMI in S0“msage. This bit is reset by PLTRST# assertion.
15	0h RO/V	**SERIRQ_SMI Status (SERIRQ_SMI_STS):** 1 = Indicates the SMI# was caused by the SERIRQ decoder. 0 = SMI# not caused by SERIRQ decoder. NOTE: this bit is not sticky. Writes to this bit will have no effect.
14	0h RW/1C/V	**Periodic Status (PERIODIC_STS):** This bit will be set at the rate determined by the PER_SMI_SEL bits. If the PERIODIC_EN bit is also set, the PCH will generate an SMI#. This bit is cleared by writing a 1 to this bit position. This bit is reset by PLTRST# assertion.
13	0h RW/1C/V	**TCO Status (TCO_STS):** 0 = SMI not caused by TCO logic. 1 = Indicates SMI was caused by the TCO logic. NOTE: Will not cause wake event. This bit is cleared by writing a 1 to this bit position. This bit is reset by PLTRST# assertion.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO/V	**DEVMON Status (DEVMON_STS):** This read-only bit is set when bit 0 in the DEVTRAP_STS register is set. It is not sticky, so writes to this bit will have no effect.
11	0h RW/1C/V	**MCSMI Status (MCSMI_STS):** This bit is set if there is an access to the power management microcontroller range (62h or 66h). If this bit is set, and the MCSMI_EN bit is also set, the PCH will generate an SMI#. This bit is set by hardware and cleared by software writing a 1 to its bit position. This bit is reset by PLTRST# assertion.
10	0h RO/V	**GPIO SMI Status (GPIO_SMI_STS):** This bit will be a 1 if any GPIO that is enabled to trigger SMI is asserted. GPIOs that are not routed to cause an SMI will have no effect on this bit. This bit is NOT sticky. Writes to this bit will have no effect. Note: See the GPIO chapter for the individual GPIO SMI status, enable, and routing bit definitions.
9	0h RO/V	**GPE0 Status (GPE0_STS):** There are several status/enable bit pairs in GPE0_STS/EN_127_96 that are capable of triggering SMI#s. This bit is a logical OR of all of those pairs (i.e. this bit is asserted whenever at least one of those pairs has both the status and enable bit asserted). This bit is NOT sticky. Writes to this bit will have no effect. Note: The setting of this bit does not cause the SMI#. The following bit pairs are included in this logical OR: - GPE0_STS/EN_127_96 [18, 17, 16, 13, 11, 10, 8, 2]
8	0h RO/V	**PM1 Status Register (PM1_STS_REG):** This is an OR of the bits (except for bits 5 and 4) in the ACPI PM1 Status Reg. Not sticky. Writes to this bit have no effect. Note: The setting of this bit does not cause the SMI#.
7	0h RO	Reserved.
6	0h RW/1C/V	**Software SMI Timer Status (SWSMI_TMR_STS):** This bit will be set to 1 by the hardware when the Software SMI# Timer expires. This bit will remain 1 until the software writes a 1 to this bit. This bit is reset by PLTRST# assertion.
5	0h RW/1C/V	**APM Status (APM_STS):** SMI# was generated by a write access to the APM control register and if the APMC_EN bit is set. This bit is cleared by writing a one to its bit position. This bit is reset by PLTRST# assertion.
4	0h RW/1C/V	**SMI_ON_SLP_EN Status (SMI_ON_SLP_EN_STS):** This bit will be set by the PCH when a write access attempts to set the SLP_EN bit. This bit is cleared by writing a 1 to this bit position. This bit is reset by PLTRST# assertion.
3	0h RO/V	**Legacy USB Status (LEGACY_USB_STS):** This non-sticky read-only bit is a logical OR of each of the SMI status bits in the USB Legacy Keybd Register ANDed with the corresponding enable bits. This bit will not be active if the enable bits are not set. Writes to this bit will have no effect.
2	0h RW/1C/V	**BIOS Status (BIOS_STS):** This bit gets set by hardware when a 1 is written by software to the GBL_RLS bit. When both BIOS_EN and the BIOS_STS bit are set, an SMI# will be generated. The BIOS_STS bit is cleared when software writes a 1 to this bit position. This bit is reset by PLTRST# assertion.
1:0	0h RO	Reserved.

13.2.7 General Purpose Event Control (GPE_CTRL)—Offset 40h

Lockable: No
Usage: ACPI or Legacy
Power Well: Primary

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW/V	**Software GPE Control (SWGPE_CTRL):** This bit allows software to control the assertion of SWGPE_STS bit. This bit is used by hardware as the level input signal for the SWGPE_STS bit in the GPE0_STS register. When SWGPE_CTRL is 1, SWGPE_STS will be set to 1, and writes to SWGPE_STS with a value of 1 to clear SWGPE_STS will result in SWGPE_STS being set back to 1 by hardware. When SWGPE_CTRL is 0, writes to SWGPE_STS with a value of 1 will clear SWGPE_STS to 0. This bit is reset by RSMRST# assertion.
16:0	0h RO	Reserved.

13.2.8 PM2a Control Block (PM2A_CNT_BLK)—Offset 50h

Lockable: No Usage
Usage: ACPI or Legacy
Power Well: Primary
Note: BIOS must describe this register as 1 byte wide to the OS

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**Arbiter Disable (ARB_DIS):** This bit is a scratchpad bit for legacy software compatibility. This bit is reset by PLTRST# assertion.

13.2.9 Over-Clocking WDT Control (OC_WDT_CTL)—Offset 54h

This register controls the operation of the PCH Over-Clocking Watchdog Timer.

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 2000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h WO	**Over-Clocking WDT Reload (OC_WDT_RLD):** Software can write a '1' to this bit to reload ("ping") the PCH over-clocking watchdog timer while it is running. A write of '0' to this bit has no effect. A write of '1' to this bit while OC_WDT_EN=0, or with the clearing of OC_WDT_EN, does not start or reload the WDT (i.e. OC_WDT_EN takes precedence). The value in OC_WDT_TOV may be changed by software along with its setting of this bit. On a WDT reload, the current (potentially new) value in OC_WDT_TOV is loaded into the WDT as the new timeout value.
30:26	0h RO	Reserved.
25	0h RW/1C/V	**Over-Clocking WDT ICC Survivability Mode Timeout Status (OC_WDT_ICCSURV_STS):** This bit is set to '1' if the over-clocking WDT has timed out and triggered a global reset while running in a mode that has ICC survivability impact (OC_WDT_ICCSURV=1). It is cleared by a software write of '1' or by RSMRST# assertion.
24	0h RW/1C/V	**Over-Clocking WDT Non-ICC Survivability Mode Timeout Status (OC_WDT_NO_ICCSURV_STS):** This bit is set to '1' if the over-clocking WDT has timed out and triggered a global reset while running in a mode that does not have ICC survivability impact (OC_WDT_ICCSURV=0). It is cleared by a software write of '1' or by RSMRST# assertion.
23:16	0h RW	**Over-Clocking WDT Scratchpad (OC_WDT_SCRATCH):** This field is available as scratchpad space for software and has no effect on PCH HW operation. This bit is reset by RSMRST# assertion.
15	0h RW/L	**Over-Clocking WDT Force All (OC_WDT_FORCE_ALL):** GATE_BIT:OC_WDT_CTL.OC_WDT_CTL_LCK.HIGH When this bit is set to '1' and the OC_WDT is running, any included global reset source will behave as though the OC_WDT expired. This bit is reset by RSMRST# assertion or CF9 reset.
14	0h RW/V/L	**Over-Clocking WDT Enable (OC_WDT_EN):** Software sets this bit to '1' to enable the PCH over-clocking watchdog timer. While the counter is running, if it expires before being reloaded by software via the OC_WDT_RLD bit or halted by software clearing this bit, then one of the status bits will be set (which one depends on the WDT operating mode at the time - see the OC_WDT_ICCSURV bit description), and a global reset will be triggered. This bit is also set by the hardware when conditions allow the OC_WDT to self-start at power cycle reboot (effectively changes the default of this bit as seen by software).
13	1h RW/L	**Over-Clocking WDT ICC Survivability Impact (OC_WDT_ICCSURV):** This bit determines whether OC_WDT expiration will have an impact on ICC (Integrated Clock Controller) bootstrap survivability. OC_WDT_ICCSURV=1 (default) An OC_WDT timeout while operating in this mode causes certain ICC hardware auto-recovery actions to take place. A timeout in this mode will set OC_WDT_ICCSURV_STS.OC_WDT_ICCSURV=0 Software should configure the OC_WDT to this mode if no ICC hardware auto-recovery actions are desired in the event of a timeout. A timeout in this mode will set OC_WDT_NO_ICCSURV_STS
12	0h RW/L	**OC_WDT_CTL Register Lock (OC_WDT_CTL_LCK):** This bit controls write-ability to this register. Encodings: 0: All fields of register OC_WDT_CTL operate as normal and can be updated by software. Reads to the register operate as normal. 1: All RW/L fields of register OC_WDT_CTL, including this lock control bit, are locked. Writes to these register fields have no effect and the register fields retain their current states. Reads to the register operate as normal. Once this bit is set, it can only be cleared by Primary well power loss (via RSMRST# assertion).
11:10	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
9:0	0h RW/V/L	**Over-Clocking WDT Timeout Value (OC_WDT_TOV):** Software programs the desired over-clocking WDT timeout value into this register. This timer is zero-based and has a granularity of 1 second. Example timeout values: 000h: 1 second 001h: 2 seconds ... 3FFh: ~17 minutes (1024 seconds) The value of OC_WDT_TOV may be changed by software along with its setting of the OC_WDT_RLD bit. On a WDT reload, the current (potentially new) value in OC_WDT_TOV is loaded into the WDT as the new timeout value. This field is also updated by the hardware when conditions allow the OC_WDT to self-start at power cycle reboot (effectively changes the default of this field as seen by software).

13.2.10 General Purpose Event 0 Status [31:0] (GPE0_STS_31_0)—Offset 60h

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/1C/V	**General Purpose Event 0 Status [31:0] (GPE0_STS_31_0):** These bits are set any time the corresponding GPIO is setup as an input and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPE0_EN_31_0 register, then when the GPE0_STS_31_0 bit is set: - If system is in an S3-S5 state, the event will also wake the system. - If system is in an S0 state (or upon waking back to S0), an SCI will be caused, depending on the GPIROUTSCI bit for the corresponding GPI. These bits are sticky bits and are cleared by writing a 1 back to this bit position. Note: The GPP/GPD group mapped to this GPE0_STS_31_0 is configured via GPIO_CFG.DW0 and MISCCFG.DW0. Both GPIO_CFG.DW0 and MISCCFG.DW0 must be programmed to the same GPIO group.

13.2.11 General Purpose Event 0 Status [63:32] (GPE0_STS_63_32)—Offset 64h

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/1C/V	**General Purpose Event 0 Status [63:32] (GPE0_STS_63_32):** These bits are set any time the corresponding GPIO is setup as an input and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPE0_EN_63_32 register, then when the GPE0_STS_63_32 bit is set: - If system is in an S3-S5 state, the event will also wake the system. - If system is in an S0 state (or upon waking back to S0), an SCI will be caused, depending on the GPIROUTSCI bit for the corresponding GPI. These bits are sticky bits and are cleared by writing a 1 back to this bit position. Note: The GPP/GPD group mapped to this GPE0_STS_63_32 is configured via GPIO_CFG.DW1 and MISCCFG.DW1. Both GPIO_CFG.DW1 and MISCCFG.DW1 must be programmed to the same GPIO group.

13.2.12 General Purpose Event 0 Status [95:64] (GPE0_STS_95_64)—Offset 68h

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/1C/V	**General Purpose Event 0 Status [95:64] (GPE0_STS_95_64):** These bits are set any time the corresponding GPIO is setup as an input and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPE0_EN_95_64 register, then when the GPE0_STS_95_64 bit is set: - If system is in an S3-S5 state, the event will also wake the system. - If system is in an S0 state (or upon waking back to S0), an SCI will be caused, depending on the GPIROUTSCI bit for the corresponding GPI. These bits are sticky bits and are cleared by writing a 1 back to this bit position. Note: The GPP/GPD group mapped to this GPE0_STS_95_64 is configured via GPIO_CFG.DW2 and MISCCFG.DW2. Both GPIO_CFG.DW2 and MISCCFG.DW2 must be programmed to the same GPIO group.

13.2.13 General Purpose Event 0 Status [127:96] (GPE0_STS[127:96])—Offset 6Ch

Note: This register is symmetrical to the General Purpose Event 0 Enable [127:96] Register. Unless indicated otherwise below, if the corresponding _EN bit is set, then when the STS bit get set, the PCH will generate a Wake Event. Once back in an S0 state (or if already in an S0 state when the event occurs), the PCH will also generate an SCI if the SCI_EN bit is set, or an SMI# if the SCI_EN bit is not set and GBL_SMI_EN is set.
Note that GPE0_STS bits 95:0 are claimed by the GPIO register block.

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18	0h RW/1C/V	**Wake Alarm Device Timer Status (WADT_STS):** This bit is set whenever the any of the wake alarm device timers signal a timer expiration. This bit is reset by RSMRST# assertion.
17:16	0h RO	Reserved.
15	0h RW/1C/V	**GPIO Tier2 SCI Status (GPIO_TIER2_SCI_STS):** This bit is a logical OR of sci_wake from tier 2 GPIO's.
14	0h RW/1C/V	**eSPI SCI Status (ESPI_SCI_STS):** This bit will be set when an agent attached to eSPI is requesting an SCI. Note: This source is not able to cause a wake event. This bit is reset by RSMRST# assertion.
13	0h RW/1C/V	**Power Management Event Bus 0 Status (PME_B0_STS):** This bit will be set to 1 by the PCH when any internal device with PCI Power Management capabilities on bus 0 asserts the equivalent of the PME# signal. Additionally, if the PME_B0_EN and SCI_EN bits are set, and the system is in an S0 state, then the setting of the PME_B0_STS bit will generate an SCI (or SMI# if SCI_EN is not set). If the PME_B0_EN bit is set, and the system is in an S3-S4 state (or S5 state due to SLP_TYP and SLP_EN), then the setting of the PME_B0_STS bit will generate a wake event. If the system is in an S5 state due to power button override, then the PME_B0_STS bit will not cause a wake event or SCI. This bit is cleared by a software write of '1'. Internal devices which can set this bit: - Integrated LAN - HD Audio/Audio DSP - SATA - xHCI - CNVi - Intel (R)CSME Maskable Host Wake This bit is reset by RSMRST# assertion.
12	0h RW/1C/V	**Intel(R)CSME SCI Status (ME_SCI_STS):** This bit will be set when Intel(R)CSME is requesting an SCI. Software must clear the Intel(R)CSME source of the SCI before clearing this bit. Note: This source is not able to cause a wake event. This bit is reset by RSMRST# assertion.
11	0h RW/1C/V	**Power Management Event Status (PME_STS):** This bit will be set to 1 by hardware when the PME# signal goes active. Additionally, if the PME_EN and SCI_EN bits are set, and system is in an S0 state, then the setting of the PME_STS bit will generate an SCI (or SMI# if SCI_EN is not set). If the PME_EN bit is set, and the system is in an S3-S4 state (or S5 state due to SLP_TYP and SLP_EN), then the setting of the PME_STS bit will generate a wake event. If the system is in an S5 state due to power button override, then PME_STS will not cause a wake event or SCI. This bit is cleared by writing a 1 to this bit position or RSMRST# assertion.
10	0h RW/1C/V	**Battery Low Status (BATLOW_STS):** In Mobile Mode this bit will be set to 1 by hardware when the BATLOW# signal goes low. Software clears the bit by writing a 1 to the bit position. In Desktop Mode, this bit will be treated as Reserved. This bit is reset by RSMRST# assertion.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/1C/V	**PCI Express Status (PCI_EXP_STS):** This bit will be set to 1 by hardware to indicate that: - The PME event message was received on one or more of the PCI-Express Ports - An Assert PMEGPE message received from the MCH via DMI Note: The PCI WAKE# pin and the PCI-Express Beacons have no impact on this bit. Software attempts to clear this bit by writing a 1 to this bit position. If the PCI_EXP_STS bit went active due to an Assert PMEGPE message, then a Deassert PMEGPE message must be received prior to the software write in order for the bit to be cleared. If the bit is not cleared and the corresponding PCI_EXP_EN bit is set, the leveltriggered SCI will remain active. Note that a race condition exists where the PCI Express device sends another PME message because the PCI Express device was not serviced within the time when it must resend the message. This may result in a spurious interrupt, and this is comprehended and approved by the PCI Express specification. The window for this race condition is approximately 95-105 milliseconds. This bit is reset by RSMRST# assertion.
8	0h RO	Reserved.
7	0h RW/1C/V	**SMBus Wake Status (SMB_WAK_STS):** This bit is set to 1 by the hardware to indicate that the wake event was caused by the PCH's SMBus logic. This could be due to either the SM Bus Target unit receiving a message or the SMBALERT# signal going active. NOTES: 1. The SMBus controller will independently cause an SMI# so this bit does not need to do so (unlike the other bits in this register). 2. This bit is set by the SMBus Target command 01h (Wake/SMI#) even when the system is in the S0 state. Therefore, to avoid an instant wake on subsequent transitions to sleep states, software must clear this bit after each reception of the Wake/SMI# command or just prior to entering the sleep state. 3. The SMBALERT_STS bit (D31:F3:I/O Offset 00h:bit 5) should be cleared by software before clearing this bit. This bit is reset by RSMRST# assertion.
6	0h RW/1C/V	**TCOSCI Status (TCOSCI_STS):** This bit will be set to 1 by hardware when the TCO logic or Thermal Sensor logic causes an SCI. This bit can be reset by writing a one to this bit position or by RSMRST# assertion.
5	0h RO	Reserved.
4	0h RW/1C/V	**Thermal SCI Status (THERM_SCI_STS):** This bit will be set to 1 by hardware when the firmware sets the DRV_THERM_SMI_SCI_STS.DRV_SCI_STS. This bit can be cleared by writing a one to this bit position.
3	0h RO	Reserved.
2	0h RW/1C/V	**Software GPE Status (SWGPE_STS):** The SWGPE_CTRL bit(bit 1 of GPE_CTRL reg) acts as a level input to this bit. This bit is reset by RSMRST# assertion.
1	0h RW/1C/V	**Hot Plug Status (HOT_PLUG_STS):** Enables PCH to cause an SCI when the HOT_PLUG_STS bit is set. This is used to allow the PCI Express ports to cause an SCI due to hot-plug events. The following events cause HOT_PLUG_STS bit to set - Assert GPE message received from any of the PCIE ports in PCH - Assert HPGPE message received from any of the PCIE ports in PCH - Assert GPE message received downstream from processor - Assert HPGPE message received downstream from processor. This bit is reset by RSMRST# assertion.
0	0h RO	Reserved.

13.2.14 General Purpose Event 0 Enable [31:0] (GPE0_EN_31_0)—Offset 70h

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Event 0 Enable [31:0] (GPE0_EN_31_0):** These bits enable the corresponding GPE0_STS[31:0] bits being set to cause an SCI and/or wake event. Note: The GPP/GPD group mapped to this GPE0_EN_31_0 is configured via GPIO_CFG.DW0 and MISCCFG.DW0. Both GPIO_CFG.DW0 and MISCCFG.DW0 must be programmed to the same value.

13.2.15 General Purpose Event 0 Enable [63:32] (GPE0_EN_63_32)—Offset 74h

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Event 0 Enable [63:32] (GPE0_EN_63_32):** These bits enable the corresponding GPE0_STS[63:32] bits being set to cause an SCI and/or wake event. Note: The GPP/GPD group mapped to this GPE0_EN_63_32 is configured via GPIO_CFG.DW1 and MISCCFG.DW1. Both GPIO_CFG.DW1 and MISCCFG.DW1 must be programmed to the same value.

13.2.16 General Purpose Event 0 Enable [95:64] (GPE0_EN_95_64)—Offset 78h

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Event 0 Enable [95:64] (GPE0_EN_95_64):** These bits enable the corresponding GPE0_STS[95:64] bits being set to cause an SCI and/or wake event. Note: The GPP/GPD group mapped to this GPE0_EN_95_64 is configured via GPIO_CFG.DW2 and MISCCFG.DW2. Both GPIO_CFG.DW2 and MISCCFG.DW2 must be programmed to the same value.

13.2.17 General Purpose Event 0 Enable [127:96] (GPE0_EN[127:96])—Offset 7Ch

Note: This register is symmetrical to the General Purpose Event 0 Status [127:96] Register.
Note that GPE0_STS bits 95:0 are claimed by the GPIO register block.

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18	0h RW	**Wake Alarm Device Timer Enable (WADT_EN):** Used to enable the setting of the WADT_STS bit to generate Wake/SMI#/SCI. This bit is reset by DSW_PWROK de-assertion.
17	0h RO	Reserved.
16	0h RW	**LAN WAKE Enable (LAN_WAKE_EN):** Used to enable the setting of the LANWAKE_STS bit to generate wake/SMI#/SCI. Host wake events from the PHY through LANWAKE cannot be disabled by clearing this bit. Note that GPIO[27] is a valid host wake event from Deep-Sx. But the wake enable configuration must persist even after a G3. So this bit is in the RTC well.
15	0h RW/V	**GPIO Tier2 SCI EN (GPIO_TIER2_SCI_EN):** Used to enable the setting of GPIO_TIER2_SCI_STS to generate wake/SCI#.
14	0h RW/V	**eSPI SCI Enable (ESPI_SCI_EN):** Used to enable the setting of the ESPI_SCI_STS bit to generate a SCI.
13	0h RW/V	**PME_B0 Enable (PME_B0_EN):** Enables the setting of the PME_B0_STS bit to generate a wake event and/or an SCI or SMI#. This bit is reset by RTCRST# assertion.
12	0h RW/V	**Intel (R) CSME SCI Enable (ME_SCI_EN):** Used to enable the setting of the ME_SCI_STS bit to generate a SCI.
11	0h RW/V	**Power Management Event Enable (PME_EN):** Enables the setting of the PME_STS to generate a wake event and/or an SCI. This bit is reset by RTCRST# assertion.
10	0h RW/V	**Low Battery Enable (BATLOW_EN):** In Mobile Mode, this bit enables the BATLOW# signal to cause an SMI# or SCI (depending on the SCI_EN bit) when it goes low.This bit does not prevent the BATLOW# signal from inhibiting the wake event. In Desktop Mode this bit will be treated as Reserved. This bit is reset by RTCRST# assertion.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/V	**PCI Express Enable (PCI_EXP_EN):** Enables PCH to cause an SCI when PCI_EXP_STS bit is set. This is used to allow the PCI Express ports to cause an SCI due to wake/PME events.
8:7	0h RO	Reserved.
6	0h RW/V	**TCOSCI Enable (TCOSCI_EN):** When TCOSCI_EN and TCOSCI_STS are both set, an SCI will be generated. This bit is reset by RSMRST# assetion.
5	0h RO	Reserved.
4	0h RW	**Thermal SCI Enable (THERM_EN):** When THERM_EN and THERM_SCI_STS are both set, an SCI will be generated.
3	0h RO	Reserved.
2	0h RW/V	**Software GPE Enable (SWGPE_EN):** This bit, when set to 1, enables the SW GPE function. If SWGPE_CTRL is written to a 1, hardware will set SWGPE_STS (acts as a level input) If SWGPE_STS, SWGPE_EN, and SCI_EN are all 1's, an SCI will be generated If SWGPE_STS = 1, SWGPE_EN = 1, SCI_EN = 0, and GBL_SMI_EN = 1 then an SMI# will be generated
1	0h RW/V	**Hot Plug Enable (HOT_PLUG_EN):** Enables PCH to cause an SCI when the HOT_PLUG_STS bit is set. This is used to allow the PCI Express ports to cause an SCI due to hot-plug events. The following events cause HOT_PLUG_STS bit to set - Assert GPE message received from any of the PCIE ports in PCH - Assert HPGPE message received from any of the PCIE ports in PCH - Assert GPE message received downstream from MCH - Assert HPGPE message received downstream from MCH
0	0h RO	Reserved.

13.3 PMC Memory Mapped Registers Summary

The PMC memory mapped registers are accessed based upon offsets from PM Base Address (PWRMBASE) defined in PCI Device 31: Function 2.

Table 13-3. Summary of PMC Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1020h	1023h	General PM Configuration A (GEN_PMCON_A)—Offset 1020h	20014000h
1024h	1027h	General PM Configuration B (GEN_PMCON_B)—Offset 1024h	4h
1030h	1033h	Configured Revision ID (CRID)—Offset 1030h	0h
1048h	104Bh	Extended Test Mode Register 3 (ETR3)—Offset 1048h	0h
104Ch	104Fh	SET STRAP MSG LOCK (SSML)—Offset 104Ch	0h
1050h	1053h	SET STRAP MSG CONTROL (SSMC)—Offset 1050h	0h
1054h	1057h	SET STRAP MSG DATA (SSMD)—Offset 1054h	0h
10B0h	10B3h	Configured Revision ID (CRID_UIP)—Offset 10B0h	0h
10C0h	10C3h	HSIO Power Management Configuration 1 (MODPHY_PM_CFG1)—Offset 10C0h	0h
10C4h	10C7h	HSIO Power Management Configuration 2 (MODPHY_PM_CFG2)—Offset 10C4h	FFFh

Table 13-3. Summary of PMC Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
10C8h	10CBh	HSIO Power Management Configuration 3 (MODPHY_PM_CFG3)—Offset 10C8h	5000000h
10CCh	10CFh	HSIO Power Management Configuration 4 (MODPHY_PM_CFG4)—Offset 10CCh	0h
10D0h	10D3h	HSIO Power Management Configuration 5 (MODPHY_PM_CFG5)—Offset 10D0h	0h
10D4h	10D7h	HSIO Power Management Configuration 6 (MODPHY_PM_CFG6)—Offset 10D4h	0h
11B8h	11BBh	External Rail Config (EXT_RAIL_CONFIG)—Offset 11B8h	0h
11C0h	11C3h	External Rail Config (EXT_V1P05_VR_CONFIG)—Offset 11C0h	0h
11C4h	11C7h	External Rail Config (EXT_VNN_VR_CONFIG0)—Offset 11C4h	0h
11C8h	11CBh	VNN V1p05 Control Hold Off (VNN_V1P05_CTRL_HOLD_OFF)—Offset 11C8h	101h
11CCh	11CFh	EXT FET RAMP CFG (EXT_FET_RAMP_CFG)—Offset 11CCh	40004h
11D0h	11D3h	VCCIN AUX CONFIG Register1 (VCCIN_AUX_CFG1)—Offset 11D0h	0h
11D4h	11D7h	VCCIN AUX CONFIG Register2 (VCCIN_AUX_CFG2)—Offset 11D4h	0h
1200h	1203h	Always Running Timer Value 31:0 (ARTV_31_0)—Offset 1200h	0h
1204h	1207h	Always Running Timer Value 31:0 (ARTV_63_32)—Offset 1204h	0h
1210h	1213h	Timed GPIO Control 0 (TGPIOCTL0)—Offset 1210h	0h
1220h	1223h	Timed GPIO 0 Comparator Value 31:0 (TGPIOCOMPV0_31_0)—Offset 1220h	0h
1224h	1227h	Timed GPIO Comparator Value 63:32 (TGPIOCOMPV0_63_32)—Offset 1224h	0h
1228h	122Bh	Timed GPIO0 Periodic Interval Value 31_0 (TGPIOPIV0_31_0)—Offset 1228h	0h
122Ch	122Fh	Timed GPIO 0 Periodic Interval Value 63_32 (TGPIOPIV0_63_32)—Offset 122Ch	0h
1230h	1233h	Timed GPIO Time Capture Register 31_0 (TGPIOTCV0_31_0)—Offset 1230h	0h
1234h	1237h	Timed GPIO0 Time Capture Register 63_32 (TGPIOTCV0_63_32)—Offset 1234h	0h
1238h	123Bh	Timed GPIO0 Event Counter Capture Register 31_0 (TGPIOECCV0_31_0)—Offset 1238h	0h
123Ch	123Fh	Timed GPIO0 Event Counter Capture Register 63_32 (TGPIOECCV0_63_32)—Offset 123Ch	0h
1240h	1243h	Timed GPIO0 Event Counter Register 31_0 (TGPIOEC0_31_0)—Offset 1240h	0h
1244h	1247h	Timed GPIO0 Event Counter Register 63_32 (TGPIOEC0_63_32)—Offset 1244h	0h
1310h	1313h	Timed GPIO Control 1 (TGPIOCTL1)—Offset 1310h	0h
1320h	1323h	Timed GPIO 1 Comparator Value 31:0 (TGPIOCOMPV1_31_0)—Offset 1320h	0h
1324h	1327h	Timed GPIO Comparator Value 63:32 (TGPIOCOMPV1_63_32)—Offset 1324h	0h
1328h	132Bh	Timed GPIO1 Periodic Interval Value 31_0 (TGPIOPIV1_31_0)—Offset 1328h	0h
132Ch	132Fh	Timed GPIO 1 Periodic Interval Value 63_32 (TGPIOPIV1_63_32)—Offset 132Ch	0h

Table 13-3. Summary of PMC Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1330h	1333h	Timed GPIO Time Capture Register 31_0 (TGPIOTCV1_31_0)—Offset 1330h	0h
1334h	1337h	Timed GPIO Time Capture Register 63_32 (TGPIOTCV1_63_32)—Offset 1334h	0h
1338h	133Bh	Timed GPIO0 Event Counter Capture Register 31_0 (TGPIOECCV1_31_0)—Offset 1338h	0h
133Ch	133Fh	Timed GPIO0 Event Counter Capture Register 63_32 (TGPIOECCV1_63_32)—Offset 133Ch	0h
1340h	1343h	Timed GPIO1 Event Counter Register 31_0 (TGPIOEC1_31_0)—Offset 1340h	0h
1344h	1347h	Timed GPIO Event Counter Register 63_32 (TGPIOEC1_63_32)—Offset 1344h	0h
150Ch	150Fh	Catastrophic Trip Point Enable (CTEN)—Offset 150Ch	1h
1510h	1513h	EC Thermal Sensor Reporting Enable (ECRPTEN)—Offset 1510h	0h
1520h	1523h	Throttle Level (TL)—Offset 1520h	FF3FCFFh
1528h	152Bh	Throttle Levels Enable (TLEN)—Offset 1528h	0h
1530h	1533h	Thermal Sensor Alert High Value (TSAHV)—Offset 1530h	FFh
1534h	1537h	Thermal Sensor Alert Low Value (TSALV)—Offset 1534h	0h
1538h	153Bh	Thermal Alert Trip Status (TAS)—Offset 1538h	0h
1540h	1543h	PCH Hot Level Control (PHLC)—Offset 1540h	0h
1560h	1563h	Temperature Sensor Control and Status (TSS0)—Offset 1560h	0h
1800h	1803h	Wake Alarm Device Timer: AC (WADT_AC)—Offset 1800h	FFFFFFFFh
1804h	1807h	Wake Alarm Device Timer: DC (WADT_DC)—Offset 1804h	FFFFFFFFh
1808h	180Bh	Wake Alarm Device Expired Timer: AC (WADT_EXP_AC)—Offset 1808h	FFFFFFFFh
180Ch	180Fh	Wake Alarm Device Expired Timer: DC (WADT_EXP_DC)—Offset 180Ch	FFFFFFFFh
1810h	1813h	Power and Reset Status (PRSTS)—Offset 1810h	0h
1818h	181Bh	Power Management Configuration Reg 1 (PM_CFG)—Offset 1818h	20h
1828h	182Bh	S3 Power Gating Policies (S3_PWRGATE_POL)—Offset 1828h	0h
182Ch	182Fh	S4 Power Gating Policies (S4_PWRGATE_POL)—Offset 182Ch	0h
1830h	1833h	S5 Power Gating Policies (S5_PWRGATE_POL)—Offset 1830h	0h
1834h	1837h	DeepSx Configuration (DSX_CFG)—Offset 1834h	0h
183Ch	183Fh	Power Management Configuration Reg 2 (PM_CFG2)—Offset 183Ch	0h
18C8h	18CBh	PM_SYNC Miscellaneous Configuration (PM_SYNC_MISC_CFG)—Offset 18C8h	0h
18E0h	18E3h	Chipset Initialization Register E0 (CIRE0)—Offset 18E0h	0h
18ECh	18EFh	CPU Early Power-on Configuration (CPU_EPOC)—Offset 18ECh	0h
18FCh	18FFh	ACPI Timer Control (ACPI_TMR_CTL)—Offset 18FCh	0h
1910h	1913h	Last TSC Alarm Value[31:0] (TSC_ALARM_LO)—Offset 1910h	0h
1914h	1917h	Last TSC Alarm Value[63:32] (TSC_ALARM_HI)—Offset 1914h	0h
1920h	1923h	GPIO Configuration (GPIO_CFG)—Offset 1920h	432h
1924h	1927h	Global Reset Causes (GBLRST_CAUSE0)—Offset 1924h	0h
1928h	192Bh	Global Reset Causes Register 1 (GBLRST_CAUSE1)—Offset 1928h	0h
192Ch	192Fh	Host Partition Reset Causes (HPR_CAUSE0)—Offset 192Ch	0h

Table 13-3. Summary of PMC Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1930h	1933h	LATENCY_LIMIT_RESIDENCY_0 (LAT_LIM_RES_0)—Offset 1930h	0h
1934h	1937h	LATENCY_LIMIT_RESIDENCY_1 (LAT_LIM_RES_1)—Offset 1934h	0h
1938h	193Bh	LATENCY_LIMIT_RESIDENCY_2 (LAT_LIM_RES_2)—Offset 1938h	0h
193Ch	193Fh	SLP S0 RESIDENCY (SLP_S0_RES)—Offset 193Ch	0h
1940h	1943h	Latency Limit Control (LLC)—Offset 1940h	0h
1B1Ch	1B1Fh	Chipset Initialization Register B1C (CPPMVRIC)—Offset 1B1Ch	0h
1B24h	1B27h	Chipset Initialization Register B24 (CIRB24)—Offset 1B24h	0h
1B40h	1B43h	Chipset Initialization Register 340 (CIRB40)—Offset 1B40h	0h
1B44h	1B47h	Chipset Initialization Register B44 (CIRB44)—Offset 1B44h	0h
1B4Ch	1B4Fh	Chipset Initialization Register 34C (CIR34C)—Offset 1B4Ch	2000000h
1BD4h	1BD7h	CWB MDID Status Register (CWBMDIDSTATUS)—Offset 1BD4h	0h
1BD8h	1BDBh	ACPI Control (ACTL)—Offset 1BD8h	0h
1C34h	1C37h	Low Power Mode Status Latch Enable (LPM_STS_LATCH_EN)—Offset 1C34h	0h
1C3Ch	1C3Fh	Low Power Mode Status Reg 0 (LPM_STS_0)—Offset 1C3Ch	0h
1C40h	1C43h	Low Power Mode Status Reg 1 (LPM_STS_1)—Offset 1C40h	0h
1C44h	1C47h	Low Power Mode Status Reg 2 (LPM_STS_2)—Offset 1C44h	0h
1C48h	1C4Bh	Low Power Mode Status Reg 3 (LPM_STS_3)—Offset 1C48h	0h
1C4Ch	1C4Fh	Low Power Mode Status Reg 4 (LPM_STS_4)—Offset 1C4Ch	0h
1C50h	1C53h	Low Power Mode Status Reg 5 (LPM_STS_5)—Offset 1C50h	0h
1C5Ch	1C5Fh	Live Status of the Low Power Mode Status Reg 0 (LPM_LIVE_STS_0)—Offset 1C5Ch	0h
1C60h	1C63h	Live Status of the Low Power Mode Status Reg 1 (LPM_LIVE_STS_1)—Offset 1C60h	0h
1C64h	1C67h	Live Status of the Low Power Mode Status Reg 2 (LPM_LIVE_STS_2)—Offset 1C64h	0h
1C68h	1C6Bh	Live Status of the Low Power Mode Status Reg 3 (LPM_LIVE_STS_3)—Offset 1C68h	0h
1C6Ch	1C6Fh	Live Status of the Low Power Mode Status Reg 4 (LPM_LIVE_STS_4)—Offset 1C6Ch	0h
1C70h	1C73h	Live Status of the Low Power Mode Status Reg 5 (LPM_LIVE_STS_5)—Offset 1C70h	0h
1C78h	1C7Bh	Low Power Mode Enable (LPM_EN)—Offset 1C78h	0h
1C80h	1C83h	Low Power Mode 0 Residency Counter (LPM_0_RES)—Offset 1C80h	0h
1C84h	1C87h	Low Power Mode 1 Residency Counter (LPM_1_RES)—Offset 1C84h	0h
1C88h	1C8Bh	Low Power Mode 2 Residency Counter (LPM_2_RES)—Offset 1C88h	0h
1C8Ch	1C8Fh	Low Power Mode 3 Residency Counter (LPM_3_RES)—Offset 1C8Ch	0h
1C90h	1C93h	Low Power Mode 4 Residency Counter (LPM_4_RES)—Offset 1C90h	0h
1C94h	1C97h	Low Power Mode 5 Residency Counter (LPM_5_RES)—Offset 1C94h	0h
1C98h	1C9Bh	Low Power Mode 6 Residency Counter (LPM_6_RES)—Offset 1C98h	0h
1C9Ch	1C9Fh	Low Power Mode 7 Residency Counter (LPM_7_RES)—Offset 1C9Ch	0h
1D80h	1D83h	Power Gated ACK Status Register 0 (PPASR0)—Offset 1D80h	0h
1D84h	1D87h	Power Gated ACK Status Register 1 (PPASR1)—Offset 1D84h	0h

Table 13-3. Summary of PMC Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1D90h	1D93h	PFET Enable Ack Register 0 (PPFEAR0)—Offset 1D90h	0h
1D94h	1D97h	PFET Enable Ack Register 1 (PPFEAR1)—Offset 1D94h	0h
1DE0h	1DE3h	Chipset Initialization Register 5E0 (CIR5E0)—Offset 1DE0h	0h
1DE4h	1DE7h	Chipset Initialization Register 5E4 (CIR5E4)—Offset 1DE4h	0h
1E20h	1E23h	Static PG Function Disable 1 (ST_PG_FDIS1)—Offset 1E20h	0h
1E24h	1E27h	Static Function Disable Control 2 (ST_PG_FDIS2)—Offset 1E24h	0h
1E28h	1E2Bh	Chipset Initialization Register (NST_PG_FDIS_1)—Offset 1E28h	0h
1E40h	1E43h	PCIe Controller Disable Read (N_STPG_FUSE_SS_DIS_RD_1)—Offset 1E40h	0h
1E44h	1E47h	Capability Disable Read Register (STPG_FUSE_SS_DIS_RD_2)—Offset 1E44h	0h

13.3.1 General PM Configuration A (GEN_PMCON_A)—Offset 1020h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 20014000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30	0h RW	**DC PHY Power Disable (DC_PP_DIS):** This bit determines the Host software contribution to whether the LAN PHY remains powered in Sx/MOFF or DeepSx while on battery.
29	1h RW	**Deep-Sx PHY Power Disable (DSX_PP_DIS):** This bit determines the Host software contribution to whether the LAN PHY remains powered in DeepSx. If this bit is cleared, for the PHY to be powered in deep-Sx state, SX_PP_EN must be set to 1.
28	0h RW	**After G3 PHY Power Enable (AG3_PP_EN):** This bit determines the Host software contribution to whether the LAN PHY is powered up after exiting G3 (to either Sx/MOFF or DeepSx).
27	0h RW	**Sx PHY Power Enable (SX_PP_EN):** This bit determines the Host software contribution to whether the LAN PHY remains powered in an Sx/MOFF state that was entered from S0 (rather than from G3).
26:25	0h RO	Reserved.
24	0h RW/1C/V	**Global Reset Status (GBL_RST_STS):** This bit is set after a global reset (not G3 or DeepSx) occurs. See the GEN_PMCON_B.HOST_RST_STS bit for potential usage models.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**DRAM Initialization Scratchpad Bit (DISB):** This bit does not effect hardware functionality in any way. It is provided as a scratchpad bit that is maintained through main power well resets and CF9h-initiated resets. BIOS is expected to set this bit prior to starting the DRAM initialization sequence and to clear this bit after completing the DRAM initialization sequence. BIOS can detect that a DRAM initialization sequence was interrupted by a reset by reading this bit during the boot sequence. If the bit is 1, then the DRAM initialization was interrupted. This bit is reset by the assertion of the RSMRST# pin.
22	0h RO	Reserved.
21	0h RO/V	**Memory Placed in Self-Refresh (MEM_SR):** This bit will be set to 1 if DRAM should have remained powered and held in Self-Refresh through the last power state transition (i.e. the last time the system left S0). The scenarios where this should be the case are: - successful S3 entry & exit - successful Host partition reset without power cycle These scenarios both involve a handshake between the PCH and the CPU/MCH. The acknowledge from the CPU/MCH back to the PCH is assumed to imply that memory was successfully placed into Self-Refresh (the PCH has no way to verify whether that actually occurred). This bit will be cleared whenever the PCH begins a transition out of S0. Note: This bit should not be consulted upon wake from S1, as that state does not involve the same type of handshake or placing memory into Self-Refresh. It is assumed that software is already aware that memory context is not impacted by S1 and therefore does not need to check this bit.
20:19	0h RO	Reserved.
18	0h RW/1C/V	**Minimum SLP_S4# Assertion Width Violation Status (MS4V):** Hardware sets this bit when the SLP_S4# assertion width is less than the time programmed in the SLP_S4# Minimum Assertion Width field (D31.F0.A4h.5:4). The PCH begins the timer when SLP_S4# pin (including Intel (R) CSME override logic) is asserted during S4/S5 entry, or when the RSMRST# input is deasserted during SUS well power-up. The status bit is cleared by software writing a 1 to the bit. Note that this bit is functional regardless of the value in the SLP_S4# Assertion Stretch Enable and the Disable SLP_X Stretching After SUS Power Failure bits. This bit is reset by the assertion of the RSMRST# pin, but can be set in some cases before the default value is readable.
17	0h RO	Reserved.
16	1h RW/1C	**SUS Well Power Failure (SUS_PWR_FLR):** This bit is set to '1' whenever SUS well power is lost, as indicated by RSMRST# assertion. Software writes a 1 to this bit to clear it.
15	0h RW	**PME B0 S5 Disable (PME_B0_S5_DIS):** When set to '1', this bit blocks wake events from PME_B0_STS in S5, regardless of the state of PME_B0_EN. When cleared (default), wake events from PME_B0_STS are allowed in S5 if PME_B0_EN = '1'. Wakes from power states other than S5 are not affected by this policy bit. The net effect of setting PME_B0_S5_DIS = '1' is described by the truth table below: Y = Wake N = Don't wake B0 = PME_B0_EN OV = WOL Enable Override B0/OV | S1/S3/S4 | S5 00 | N | N 01 | N | Y (LAN only) 11 | Y (all PME B0 sources) | Y (LAN only) 10 | Y (all PME B0 sources) | N This bit is cleared by the RTCRST# pin.
14	1h RW/1C	**PWR_FLR (PF):** 1 = Indicates that the trickle current (from the main battery or trickle supply) was removed or failed. 0 = Indicates that the trickle current has not failed since the last time the bit was cleared. Software writes a 1 to this bit to clear it. This bit is in the DSW well, and defaults to '1' based on DSW_PWROK deassertion (not cleared by any type of reset).

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	Reserved.
12	0h RW/L	**Disable SLP_X Stretching After SUS Well Power Up (DIS_SLP_X_STRCH_SUS_UP):** When this bit is set to 1, all SLP_* pin stretching is disabled when powering up after a SUS well power loss. When this bit is left at 0, SLP_* stretching will be performed after SUS power failure as enabled in various other fields. Note that if this bit is a 0, SLP_* stretch timers start on SUS well power up (the PCH has no ability to count stretch time while the SUS well is powered down). Setting this bit can therefore prevent long delays after SUS power loss which may be common in mobile platforms and in manufacturing flow testing, while still allowing for the full power cycling during S3, S4 and S5 states. If the platform guarantees minimum SUS power down residence in other ways, an additional PCH-induced delay is not needed or wanted. Note: This policy bit has a different effect on SLP_SUS# stretching than on the other SLP_* pins, since SLP_SUS# is the control signal for one of the scenarios where SUS well power is lost (DeepSx). The effect of setting this bit to '1' on: - SLP_S3#, SLP_S4#, SLP_A# and SLP_LAN# stretching: disabled after any SUS power loss - SLP_SUS# stretching: disabled after G3, but no impact on DeepSx This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. This bit is cleared by the RTCRST# pin.
11:10	0h RW/L	**SLP_S3# Minimum Assertion Width (SLP_S3_MIN_ASST_WDTH):** This 2-bit value indicates the minimum assertion width of the SLP_S3# signal to guarantee that the Main power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power failure detection circuits, etc. Settings are: 00: 60 usec 01: 1 ms 10: 50 ms 11: 2 sec This field is not writable when the SLP_Sx# Stretching Policy Lock- Down bit is set. This bit is cleared by the RSMRST# pin.
9	0h RW/1C/V	**Host Reset Status (HOST_RST_STS):** This bit is set by hardware when a host partition reset (not a global reset, DeepSx, or G3) occurs. This bit is an optional tool to help BIOS determine when a host partition reset might have collided with a wake from a valid sleep state. A possible usage model would be to consult and then write a '1' to clear this bit during the boot flow before determining what action to take based on reading PM1_STS.WAK_STS = '1'. If HOST_RST_STS = '1' and/or GEN_PMCON_A.GBL_RST_STS = '1', the cold reset boot path could be followed rather than the resume path, regardless of the setting of WAK_STS. This bit does not affect PCH operation in any way, and can therefore be left set if BIOS chooses not to use it.
8	0h RW/L	**ESPI SMI Lock (ESPI_SMI_LOCK):** When this bit is set, writes to the ESPI_SMI_EN bit will have no effect. Once the ESPI_SMI_LOCK bit is set, writes of 0 to ESPI_SMI_LOCK bit will have no effect (i.e. once set, this bit can only be cleared by RSMRST#).
7:6	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW/L	**SLP_S4# Minimum Assertion Width (S4MAW):** This 2-bit value indicates the minimum assertion width of the SLP_S4# signal to guarantee that the DRAMs have been safely power-cycled. This value may be modified per platform depending on DRAM types, power supply capacitance, etc. Valid values are: 11: 1 second 10: 2 seconds 01: 3 seconds 00: 4 seconds This value is used in two ways: 1. If the SLP_S4# assertion width is ever shorter than this time, a status bit (D31.F0.A2h.2) is set for BIOS to read when S0 is entered 2. If enabled by bit 3 in this register, the hardware will prevent the SLP_S4# signal from deasserting within this minimum time period after asserting. Note that the logic that measures this time is in the suspend power well. Therefore, when leaving a G3 or DeepSx state, the minimum time is measured from the deassertion of the internal suspend well reset (unless the Disable SLP_X Stretching After SUS Power Failure bit is set). This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. RTCRST# forces this field to the conservative default state (00b).
3	0h RW/L	**SLP_S4# Assertion Stretch Enable (S4ASE):** When set to 1, the SLP_S4# pin will minimally assert for the time specified in bits 5:4 of this register. When 0, the minimum assertion time for SLP_S4# is the same as the timing defined in the Platform Design Guide. This bit is provided so that all DIMMs in the system can deterministically detect a power-cycle event for proper initialization. Note that there are behavioral changes that may be noticeable when this bit is set. Resume times from S4 and S5 and power-up times from G3 or DeepSx may be delayed by several seconds. This bit is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. This bit is cleared by RTCRST#.
2:1	0h RW	**Period SMI Select (PER_SMI_SEL):** Software sets these bits to control the rate at which the periodic SMI# is generated: 00 = 64 seconds (default), 01 = 32 seconds, 10 = 16 seconds, 11 = 8 seconds Tolerance for the timer is +/- 1 second.
0	0h RW	**AFTERG3_EN (AG3E):** Determines what state to go to when power is reapplied after a power failure (G3 state). 0 = System will return to an S0 state (boot) after power is re-applied. 1 = System will return to the S5 state (except if it was in S4, in which case it will return to S4-like state). In the S5 state, the only enabled wake-up event is the Power Button or any enabled wake event that was preserved through the power failure. This bit is in the RTC well and is only cleared by RTCRST#.

13.3.2 General PM Configuration B (GEN_PMCON_B)—Offset 1024h

General PM configuration B

Access Method

Type: MEM Register (Size: 32 bits)

Device:

Function:

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18	0h RW/L	**SLP_Sx# Stretching Policy Lock-Down (SLPSX_STR_POL_LOCK):** When set to 1, this bit locks down the following fields: - GEN_PMCON_3.DIS_SLP_X_STRCH_SUSPF - GEN_PMCON_3.SLP_S3_MIN_ASST_WDTH - GEN_PMCON_3.S4MAW - GEN_PMCON_3.S4ASE - PM_CFG.SLP_A_MIN_ASST_WDTH - PM_CFG.SLP_LAN_MIN_ASST_WDTH - PM_CFG.PWR_CYC_DUR Those bits become read-only. This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a platform reset. This lockdown bit is available in both desktop and mobile.
17	0h RW/L	**VR Config Lock (VR_CONFIG_LOCK):** When set to 1, this bit locks down the enable bits in the EXT_RAIL_CONFIG register such that the enable becomes read-only. This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a platform reset. This lockdown bit is available in both desktop and mobile.
16:14	0h RO	Reserved.
13	0h RW	**WOL Enable Override (WOL_EN_OVRD):** When this bit is set to 1, the integrated LAN is enabled to wake the system from S5 regardless of the value in the PME_B0_EN bit in the GPE0_EN register. This allows the system BIOS to enable Wake-On-LAN regardless of the policies selected through the operating system. This bit is maintained in the RTC power well, therefore permitting WOL following a surprise power failure even in cases in which the system may have been running in S0 without the PME Enables set. (Note that the LAN NVRAM configuration must support WOL after SUS power loss.) When this bit is cleared to 0, the wake-on-LAN policies are determined by OS-visible bits. This bit has no effect on wakes from S1, S3, or S4. This bit is cleared by RSMRST# pin
12:11	0h RO	Reserved.
10	0h RW	**BIOS PCI Express Enable (BIOS_PCI_EXP_EN):** This bit acts as a global enable for the SCI associated with the PCI express ports. If this bit is not set, then the various PCI Express ports and MCH cannot cause the PCI_EXP_STS bit to go active.
9	0h RO/V	**Power Button Level (PWRBTN_LVL):** This read-only bit indicates the current state of the PWRBTN# signal. 1= High, 0 = Low. The value reflected in this bit is dependent upon PM_CFG1.PB_DB_MODE. The PB_DB_MODE bit's value causes the following behavior: - '0': PWRBTN_LVL is taken from the debounced PWRBTN# pin value that is seen at the output of a 16ms debouncer. - '1': PWRBTN_LVL is taken from the raw PWRBTN# pin (before the debouncer).
8:5	0h RO	Reserved.
4	0h RW/L	**SMI Lock (SMI_LOCK):** When this bit is set, writes to the GLB_SMI_EN bit will have no effect. Once the SMI_LOCK bit is set, writes of 0 to SMI_LOCK bit will have no effect (i.e. once set, this bit can only be cleared by RSMRST#).
3	0h RO	Reserved.
2	1h RW	**RTC_PWR_STS (RPS):** The PCH will set this bit to 1 when rtc_pwrgood_rst indicates a weak or missing battery. The bit will remain set until the software clears it by writing a 0 back to this bit position. This bit is not cleared by any type of reset.
1:0	0h RO	Reserved.

13.3.3 Configured Revision ID (CRID)—Offset 1030h

Configured revision ID Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**CRID Lock (CRID_LK):** BIOS writes to this bit to lock this register (a specific lock bit is preferable over a write-based self-lock for the RID_SEL field). When this bit is written to 1, the entire register becomes RO (writes have no effect, reads return actual value) until the next assertion of RMSRST#.
30:2	0h RO	Reserved.
1:0	0h RW/L	**RID Select(RID_SEL) (rid_sel):** Software writes this field to select Revision ID reflected in PCI Config space. The decoding is: 00 - Revision ID 01 - CRID 0 10 - CRID 1 11 - CRID 2 Once written, this field can only be cleared by RSMRST#. BIOS should write to this bit on all boots, (HOST_RST/platform.)

13.3.4 Extended Test Mode Register 3 (ETR3)—Offset 1048h

This register resides in the primary well.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V/L	**CF9h Lockdown (CF9LOCK):** When set, this bit will lock the CF9h Global Reset bit and this register. This register is reset by a CF9h reset.
30:21	0h RO	Reserved.
20	0h RW/L	**CF9h Global Reset (CF9GR):** 1 = a CF9h write of 6h or Eh will cause a Global Reset of both the Host and the Intel (R) ME partitions. 0 = a CF9h write of 6h or Eh will only reset the Host partition. It is recommended that BIOS should set this bit early on in the boot sequence, and then clear it and set the CF9LOCK bit prior to loading the OS in both an Intel CSME Enabled and a Intel CSME Disabled system. This register is locked by the CF9 Lockdown (CF9LOCK) bit. This register is not reset by a CF9h reset.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW	**ModPHY Lane S0 SUS Well Power Gating Policy [1] (MLS0SWPGP):** 1: Lane power gating is permitted in S0. Note that strap information/PCIe Lane reversal information will be factored by BIOS when programming these bits in the configuration registers. Note that it is illegal SW programming to have a bit location to be 1 in this field and the corresponding bit position to be 0 in MLSXSWPGP
0	0h	Reserved

13.3.5 SET STRAP MSG LOCK (SSML)—Offset 104Ch

SET STRAP MSG LOCK

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW/L	**Set_Strap Lock (SSL):** When set to 1, all of SSML, SSMC and SSMD is locked, including this Lock bit. Note that this bit is reset on host partition reset

13.3.6 SET STRAP MSG CONTROL (SSMC)—Offset 1050h

SET STRAP Message Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW/L	**Set_Strap Mux Select (SSMS):** When set to 1, the Set strap message bits [47:32] come from the Set_Strap Msg Data register. This bit is reset by the RSMRST# pin only. When 0, the Set-Strap data continues to come from the soft straps themselves.This register field is locked by the Set Strap Lock (SSML.SSL) bit.

13.3.7 SET STRAP MSG DATA (SSMD)—Offset 1054h

This register is used to provide a BIOS programmable sticky register which contains data that will be used in the Set-Strap type 1 msg on subsequent resets. The bits in the message control certain CPU features, for which see the CPU spec. These bits are in the resume well, so only reset on G3. The usage model is that on each reset BIOS will check the state of the CPU. If the state is correct, then BIOS continues. If not, then BIOS writes the SSMD and SSMC registers and does a CF9 reset. On the reset the value of what was written to SSMD takes effect. Note that some mobile platforms force G3 on S5 requests. For those platforms, if the user/BIOS wants to have these bits set, there will be 2 resets on every power-on. If the platform accepts the default of 0 for these controls, then there is only one reset. The bits are in DSW and not RTC well because this allows a user upgrade, assuming the user unplugged the system before doing the upgrade, to revert to a setting of 0. This should reduce any interoperability concerns regarding user upgrades. The DSW bits are all cleared by DSW_PWROK, and must not be cleared by CF9h resets.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW/L	**Set_Strap DATA (SSD):** When SSMS is 1, then this data is sent in the Set-Strap msg Type 1 upon reset. This data is sent i//n the 2nd DW of data, bits 15:0. This register field is locked by the Set Strap Lock SSML.SSL bit.

13.3.8 Configured Revision ID (CRID_UIP)—Offset 10B0h

Configured revision ID Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW/V	**CRID Update in Progress (CRID_UIP):** PMC HW sets this bit to indicate that SetID broadcast flow has been requested by BIOS. This bit is cleared by PMC FW only when the completion/s for the multicast non-posted SetIDVal message is received by PMC. BIOS is required to read this bit as cleared before writing to the CRID register (to request a CRID update). BIOS is also required to poll on reads to this bit until it sees the bit as cleared after BIOS has written to the CRID register. 0 Any previously requested CRID Update is complete. 1 the most recently requested CRID update is still in progress.

13.3.9 HSIO Power Management Configuration 1 (MODPHY_PM_CFG1)—Offset 10C0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11:0	0h RW	**HSIO Lane S0 SUS Well Power Gating Policy (MLS0SWPGP):** This is a bit per lane that controls SUS Well Power Gating for a HSIO lane to be used for S0 and S0ix. Bit 0: Corresponds to HSIO Lane 0 Bit 1: Corresponds to HSIO Lane 1 Bit 2: Corresponds to HSIO Lane 2 : : Bit 11: Corresponds to HSIO Lane 11 For each lane: 0: Lane power gating not permitted in S0. 1: Lane power gating is permitted in S0. Note that strap information/PCIe Lane reversal information will be factored by BIOS when programming these bits in the configuration registers. Note that it is not allowed for SW programming to have a bit location to be 1 in this field and the corresponding bit position to be 0 in MLSXSWPGP

13.3.10 HSIO Power Management Configuration 2 (MODPHY_PM_CFG2)—Offset 10C4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: FFFh

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11:0	FFFh RW	**HSIO Lane Sx SUS Well Power Gating Policy [11:0] (MLSXSWPGP):** This is a bit per lane that controls SUS Well Power Gating for a HSIO lane when system is in Sx. Bit 0: Corresponds to HSIO Lane 0 Bit 1: Corresponds to HSIO Lane 1 Bit 2: Corresponds to HSIO Lane 2 : : Bit 11: Corresponds to HSIO Lane 11 For each lane: 0: Lane power gating not permitted in Sx. 1: Lane power gating is permitted in Sx. Note that strap information/PCIe Lane reversal information will be factored by BIOS when programming these bits in the configuration registers. This field will be used to manage Sx policies even in S0. In other words, the earlier restriction that BIOS does not have to program this field if MLSPDDGE is 1 does not apply any more. BIOS shall set this field appropriately for all cases.

13.3.11 HSIO Power Management Configuration 3 (MODPHY_PM_CFG3)—Offset 10C8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 5000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30	0h RW	**HSIO Lane SUS Power Domain Dynamic Gating Enable (MLSPDDGE):** When this bit is set to 1, HSIO Lane SUS Well Dynamic Gating is enabled. When this bit is 0, HSIO Lane SUS Well Gating can still be done at a more coarse level using MLSXSWPGP and MLS0SWPGP fields.
29	0h RW	**Enable HSIO FET Control (EMFC):** This bit enables PMC dynamic control of HSIO lane external FET. When this bit is 0 and MLSPDDGE is 1, PMC goes through all of the HSIO lane power gating flows except that the external FET is not turned off. This bit is being provided primarily to prevent External FET gating during EXI debug
28:24	5h RW/L	**External FET Ramp Time (EFRT):** This field defines the ramp time of HSIO FET. 00000b: 00us 00001b: 20us 00010b: 40us ... 00101b: 100us ... 11111b: 620us This bit is locked while PM_SYNC_MISC_CFG.PM_SYNC_LOCK = '1'

Bit Range	Default & Access	Field Name (ID): Description
23:2	0h RO	Reserved.
1	0h RW	**HSIO Per-Lane SUS Power Domain Dynamic Gating Enable (MPLSPDDGE):** When this bit is set to 1, HSIO Per-Lane SUS Well Dynamic Gating is enabled. When this bit is 0, if HSIO lane SUS power domain dynamic gating is enabled, all lanes are gated/ungated together. This bit has no impact if HSIO lane SUS power domain dynamic gating is disabled.
0	0h RO	Reserved.

13.3.12 HSIO Power Management Configuration 4 (MODPHY_PM_CFG4)—Offset 10CCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**ASL Over-rides [26:0] (ASLOR):** This field provides BIOS code to take over SPD power gating control. If BIOS code sets a bit corresponding to a controller, it implies that PMC shall ignore any other inputs from that controller and assume that the controller is ready for SPD power gating. 0 in a bit position: Use HW interfaces for the controller to manage SPD gating/wake-up. 1 in a bit position: Ignore HW interfaces for the controller, rely only on MSPDRTReq field thats managed by BIOS code. Bit 0: Corresponds to PCIe Controller A, Function 0 Bit 1: Corresponds to PCIe Controller A, Function 1 Bit 2: Corresponds to PCIe Controller A, Function 2 Bit 3: Corresponds to PCIe Controller A, Function 3 Bit 4: Corresponds to PCIe Controller B, Function 0 Bit 5: Corresponds to PCIe Controller B, Function 1 Bit 6: Corresponds to PCIe Controller B, Function 2 Bit 7: Corresponds to PCIe Controller B, Function 3 Bit 8: Corresponds to PCIe Controller C, Function 0 Bit 9: Corresponds to PCIe Controller C, Function 1 Bit 10: Corresponds to PCIe Controller C, Function 2 Bit 11: Corresponds to PCIe Controller C, Function 3 Bit 12: Corresponds to SATA Controller Bit 13: Corresponds to Gbe Controller Bit 14: Corresponds to xHCI Controller Bit 15: Corresponds to xDCI Controller Bit 16-24: Reserved Bit 25: Corresponds to DMI Controller Bit 26: Reserved This field is going to be used in conjunction with MSPDRTReq and MSPDRTRAck fields above. If BIOS code intends to over-ride HW decisions, it will set the corresponding bit for a controller/function to 1 in ASLOR and use MSPDRTReq bits to power-up/power-down SPD.

13.3.13 HSIO Power Management Configuration 5 (MODPHY_PM_CFG5)—Offset 10D0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Controller SPD RTD3 Request [26:0] (MSPDRTREQ):** This field provides BIOS code to take over SPD power gating control. If BIOS code sets a bit corresponding to a controller, it implies that PMC shall ignore any other inputs from that controller and assume that the controller is ready for SPD power gating. 0 in a bit position: Use HW interfaces for the controller to manage SPD gating/wake-up. 1 in a bit position: Ignore HW interfaces for the controller, rely only on MSPDRTReq field thats managed by BIOS code. Bit 0: Corresponds to PCIe Controller A, Function 0 Bit 1: Corresponds to PCIe Controller A, Function 1 Bit 2: Corresponds to PCIe Controller A, Function 2 Bit 3: Corresponds to PCIe Controller A, Function 3 Bit 4: Corresponds to PCIe Controller B, Function 0 Bit 5: Corresponds to PCIe Controller B, Function 1 Bit 6: Corresponds to PCIe Controller B, Function 2 Bit 7: Corresponds to PCIe Controller B, Function 3 Bit 8: Corresponds to PCIe Controller C, Function 0 Bit 9: Corresponds to PCIe Controller C, Function 1 Bit 10: Corresponds to PCIe Controller C, Function 2 Bit 11: Corresponds to PCIe Controller C, Function 3 Bit 12: Corresponds to SATA Controller Bit 13: Corresponds to Gbe Controller Bit 14: Corresponds to xHCI Controller Bit 15: Corresponds to xDCI Controller Bit 16-24: Reserved Bit 25: Corresponds to DMI Controller Bit 26: Reserved

13.3.14 HSIO Power Management Configuration 6 (MODPHY_PM_CFG6)—Offset 10D4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Controller SPD RTD3 Request Acknowledge [19:0] (MSPDRTRACK):** This field provides BIOS code to take over SPD power gating control. If BIOS code sets a bit corresponding to a controller, it implies that PMC shall ignore any other inputs from that controller and assume that the controller is ready for SPD power gating. 0 in a bit position: Use HW interfaces for the controller to manage SPD gating/wake-up. 1 in a bit position: Ignore HW interfaces for the controller, rely only on MSPDRTReq field thats managed by BIOS code. Bit 0: Corresponds to PCIe Controller A, Function 0 Bit 1: Corresponds to PCIe Controller A, Function 1 Bit 2: Corresponds to PCIe Controller A, Function 2 Bit 3: Corresponds to PCIe Controller A, Function 3 Bit 4: Corresponds to PCIe Controller B, Function 0 Bit 5: Corresponds to PCIe Controller B, Function 1 Bit 6: Corresponds to PCIe Controller B, Function 2 Bit 7: Corresponds to PCIe Controller B, Function 3 Bit 8: Corresponds to PCIe Controller C, Function 0 Bit 9: Corresponds to PCIe Controller C, Function 1 Bit 10: Corresponds to PCIe Controller C, Function 2 Bit 11: Corresponds to PCIe Controller C, Function 3 Bit 12: Corresponds to SATA Controller Bit 13: Corresponds to Gbe Controller Bit 14: Corresponds to xHCI Controller Bit 15: Corresponds to xDCI Controller Bit 16-24: Reserved Bit 25: Corresponds to DMI Controller Bit 26: Reserved

13.3.15 External Rail Config (EXT_RAIL_CONFIG)—Offset 11B8h

External Rail Configuration

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	0h RW/L	**Enable External V1P05 Rail in S5 (ENABLE_EXT_V1P05_RAIL_S5):** Enable External V1P05 Rail in S5
11	0h RW/L	**Enable External V1P05 Rail in S4 (ENABLE_EXT_V1P05_RAIL_S4):** Enable External V1P05 Rail in S4
10	0h RW/L	**Enable External V1P05 Rail in S3 (ENABLE_EXT_V1P05_RAIL_S3):** Enable External V1P05 Rail in S3
9	0h RW/L	**Enable External V1P05 Rail in S0i3 (ENABLE_EXT_V1P05_RAIL_S0I3):** Enable External V1P05 Rail in S0i3
8	0h RW	**Enable External V1P05 Rail in S0i1/S0i2 (ENABLE_EXT_V1P05_RAIL_S0I1_I2)**
7:5	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/L	**Enable External VNN Rail in S5 (ENABLE_EXT_VNN_RAIL_S5):** Enable External Vnn Rail in S5
3	0h RW/L	**Enable External VNN Rail in S4 (ENABLE_EXT_VNN_RAIL_S4):** Enable External Vnn Rail in S4
2	0h RW/L	**Enable External VNN Rail in S3 (ENABLE_EXT_VNN_RAIL_S3):** Enable External Vnn Rail in S3
1	0h RW/L	**Enable External VNN Rail in S0i3 (ENABLE_EXT_VNN_RAIL_S0I3):** Enable External Vnn Rail in S0i3
0	0h RW	**Enable External VNN Rail in S0i1/S0i2 (ENABLE_EXT_VNN_RAIL_S0I1_I2)**

13.3.16 External Rail Config (EXT_V1P05_VR_CONFIG)—Offset 11C0h

External Rail Configuration

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26:24	0h RW	**External V1P05 Voltage Value - Upper (EXT_V1P05_VOLTAGE1)**
23:16	0h RW	**External V1P05 Voltage Value - Lower (EXT_V1P05_VOLTAGE0)**
15:8	0h RW/L	**External V1P05 Icc Max Value - Upper (EXT_V1P05_ICC_MAX_VAL1):** This register houses the Icc max for the external V1p05 rail in granularity of ma in U2.14 format.
7:0	0h RW/L	**External V1P05 Icc Max Value - Lower (EXT_V1P05_ICC_MAX_VAL0):** This register houses the Icc max for the external V1p05 rail in granularity of ma in U2.14 format.

13.3.17 External Rail Config (EXT_VNN_VR_CONFIG0)—Offset 11C4h

External Rail Configuration

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26:24	0h RW	**External VNN Voltage Value - Upper (EXT_VNN_VOLTAGE1):** This register houses the voltage for the external VNN rail that will be used in S0i2/S0i3 states. Expectation is that SW will update this based on if we are in S0i2 or S0i3. This value is given in 2.5mV increments. The value of the PMIC voltage cannot be changed during idle windows in which this supply is being used.
23:16	0h RW	**External VNN Voltage Value - Lower (EXT_VNN_VOLTAGE0):** This register houses the voltage for the external VNN rail that will be used in S0i2/S0i3 states. Expectation is that SW will update this based on if we are in S0i2 or S0i3. This value is given in 2.5mV increments. The value of the PMIC voltage cannot be changed during idle windows in which this supply is being used.
15:8	0h RW/L	**External VNN Icc Max Value - Upper (EXT_VNN_ICC_MAX_VAL1):** This register houses the Icc max for the external VNN rail in granularity of ma in U2.14 format.
7:0	0h RW/L	**External VNN Icc Max Value - Lower (EXT_VNN_ICC_MAX_VAL0):** This register houses the Icc max for the external VNN rail in granularity of ma in U2.14 format.

13.3.18 VNN V1p05 Control Hold Off (VNN_V1P05_CTRL_HOLD_OFF)—Offset 11C8h

Hold Off Control for V1p05

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 101h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	1h RW/L	**V1p05 Control Ramp Timer (V1P05_CTRL_RAMP_TMR):** This register holds the V1P05 control hold off values to be used when changing the v1p05_ctrl for external bypass value in us
7:0	1h RW/L	**VNN Control Ramp Timer (VNN_CTRL_RAMP_TMR):** This register holds the VNN control hold off values to be used when changing the vnn_ctrl for external bypass value in us

13.3.19 EXT FET RAMP CFG (EXT_FET_RAMP_CFG)—Offset 11CCh

External FET Ramp Time Configuration

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 40004h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**V1p05-IS FET Ramp Time Lock (V1P05_IS_FRT_LOCK):** The bit is used to lock V1P05_IS_FET_RAMP_TIME. This bit is self-locking (i.e. once written to '1', it can only be cleared by RSMRST#).
30:24	0h RO	Reserved.
23:16	4h RW/L	**V1p05-IS FET Ramp Time (V1P05_IS_FET_RAMP_TIME):** This field defines the ramp time of the external V1p05-IS FET. Each increment is 10us (ie. 0x4=40us). This field is locked by V1P05_IS_FRT_LOCK.
15	0h RW/L	**V1P05-PHY FET Ramp Time Lock (V1P05_PHY_FRT_LOCK):** The bit is used to lock V1P05_PHY_FET_RAMP_TIME. This bit is self-locking (i.e. once written to '1', it can only be cleared by RSMRST#).
14:8	0h RO	Reserved.
7:0	4h RW/L	**V1p05-PHY FET Ramp Time (V1P05_PHY_FET_RAMP_TIME):** This field defines the ramp time of the external V1p05-PHY FET. Each increment is 10us (ie. 0x4=40us). This field is locked by V1P05_PHY_FRT_LOCK.

13.3.20 VCCIN AUX CONFIG Register1 (VCCIN_AUX_CFG1)—Offset 11D0h

This register defines the characteristics of the VCCIN_AUX voltage rail

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:16	0h RW/L	**Low Current Mode Voltage to High Current Mode Voltage Transition Time (LCM_HCM_VOLT_TRANS_TIME):** Voltage transition time required by motherboard voltage regulator when PCH changes the VCCIN_AUX regulator set point from the low current mode voltage and high current mode voltage. This field has 1us resolution. 8'h00 = Transition from low current mode voltage retention mode VID disabled. (default) 8'h01 = 1us 8'h02 = 2us ... 8'hFF = 255us Note: When [23:16]=8'h00 PCH will not transition VCCIN_AUX to low current mode voltage.
15:8	0h RW/L	**Retention Mode Voltage to High Current Mode Voltage Transition Mode (RMV_HCM_VOLT_TRANS_TIME):** Voltage transition time required by motherboard voltage regulator when PCH changes the VCCIN_AUX regulator set point from the retention mode voltage and low current mode voltage. This field has 1us resolution. 8'h00 = Transition from retention mode voltage to high current mode voltage is disabled (default) 8'h01 = 1us 8'h02 = 2us ... 8'hFF = 255us Note: When [7:0]=8'h00 and [15:8]=8'h00 PCH will not transition VCCIN_AUX to retention voltage.
7:0	0h RW/L	**Retention Mode Voltage to Low Current Mode Voltage Transition Mode (RMV_LCM_VOLT_TRANS_TIME):** Voltage transition time required by motherboard voltage regulator when PCH changes the VCCIN_AUX regulator set point from the retention mode voltage and low current mode voltage.This field has 1us resolution. 8'h00 = Transition from retention mode voltage to low current mode voltage is disabled (default) 8'h01 = 1us 8'h02 = 2us ... 8'hFF = 255us Note: When [7:0]=8'h00 and [15:8]=8'h00 PCH will not transition VCCIN_AUX to retention voltage.

13.3.21 VCCIN AUX CONFIG Register2 (VCCIN_AUX_CFG2)—Offset 11D4h

This register defines the characteristics of the VCCIN_AUX voltage rail

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	Reserved.
10:8	0h RW/L	**OFF to High Current Mode Voltage Transition Mode 10_8 (OFF_HCM_VOLT_TRANS_TIME_10_8):** Voltage transition time required by motherboard voltage regulator when PCH changes the VCCIN_AUX regulator set point from 0V to the high current mode voltage. 11'h000 = Transition to 0V in S0 & Sx states is disabled (default) 11'h001 = 1us 11'h002 = 2us ... 11'hFFF = 2048us Note: Setting this field to 11'h000 sets VCCIN_AUX as a fixed rail that stays on in all S0 & Sx power states after initial start up on G3 exit
7:0	0h RW/L	**OFF to High Current Mode Voltage Transition Mode 7_0 (OFF_HCM_VOLT_TRANS_TIME_7_0):** Voltage transition time required by motherboard voltage regulator when PCH changes the VCCIN_AUX regulator set point from 0V to the high current mode voltage. 11'h000 = Transition to 0V in S0 & Sx states is disabled (default) 11'h001 = 1us 11'h002 = 2us ... 11'hFFF = 2048us Note: Setting this field to 11'h000 sets VCCIN_AUX as a fixed rail that stays on in all S0 & Sx power states after initial start up on G3 exit

13.3.22 Always Running Timer Value 31:0 (ARTV_31_0)—Offset 1200h

Note: This register is intended for debug purposes. To obtain the most accurate timer reading, customers are recommended to read the PCH ART through the CPU TSC register and apply CPUID conversion.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**ART Value (ARTV):** Reads return current value of the ART timer [31:0]. Writes to this register has no effect Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

13.3.23 Always Running Timer Value 31:0 (ARTV_63_32)—Offset 1204h

Note: This register is intended for debug purposes. To obtain the most accurate timer reading, customers are recommended to read the PCH ART through the CPU TSC register and apply CPUID conversion.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**ART Value (ARTV):** Reads return current value of the ART timer [63:32]. Writes to this register has no effect Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

13.3.24 Timed GPIO Control 0 (TGPIOCTL0)—Offset 1210h

Timed GPIO COntrol 0

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RW	**Periodic Mode (PM):** 0:Periodic mode is disabled 1:periodic mode is enabled This bit is only applicable when Timed GPIO is configured as an output
3:2	0h RW	**Event Polarity (EP):** 00:Rising Edge 01:Falling Edge 10:Toggle Edge 11:Reserved
1	0h RW	**Direction (DIR):** 0: Output 1: Input
0	0h RW	**Enable (EN):** 0: Timed GPIO is disabled 1: Timed GPIO is enabled Note: a. When Enabled, xtal clock turnoff is disabled. This may also disable SLP_S0 assertion b. All other Timed GPIO configuration bits must be programmed before enable bit is set and must not change while the enable is 1

13.3.25 Timed GPIO 0 Comparator Value 31:0 (TGPIOCOMPV0_31_0)—Offset 1220h

Timed GPIO 0 comparator Value 31:0

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Comparator Value (COMPV):** This register is only applicable when Timed GPIO is configured as an output. If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. For example, in periodic mode if the value written to this register is 00000100h, and Periodic Interval register has the value of 200h. 1. A Timed GPIO event will be generated when ART reaches 00000100h. 2. The value in this register will then be adjusted by the hardware to 00000300h. 3. Another Timed GPIO event will be generated when the ART reaches 00000300h. 4. The value in this register will then be adjusted by the hardware to 00000500h As such when periodic Timed GPIO event occurs, the value in this register will increment. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

13.3.26 Timed GPIO Comparator Value 63:32 (TGPIOCOMPV0_63_32)—Offset 1224h

Timed GPIO Comparator Value

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Comparator Value (COMPV):** Refer to Comparator Value [31:0] for description.

13.3.27 Timed GPIO0 Periodic Interval Value 31_0 (TGPIOPIV0_31_0)—Offset 1228h

Timed GPIO0 Periodic Interval Value 31_0

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Periodic Interval Value [31:0] (PIV):** This register is only applicable when Timed GPIO is configured as an output, and Periodic Mode is enabled. The value in this register is written by SW to set the interval for the periodic Timed GPIO event

13.3.28 Timed GPIO 0 Periodic Interval Value 63_32 (TGPIOPIV0_63_32)—Offset 122Ch

Timed GPIO 0 Periodic Interval Value 63_32

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Periodic Interval Value [63:32] (PIV):** Refer to Periodic Interval Value [31:0] for description.

13.3.29 Timed GPIO Time Capture Register 31_0 (TGPIOTCV0_31_0)—Offset 1230h

Timed GPIO Time Cpature Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Time Capture Value [31:0] (TCV):** When Timed GPIO event triggers, HW captures the current ART time into this register. This register is applicable to both when Timed GPIO is configured as an input or an output. When Timed GPIO is configured as an output, the Time Capture Value in this register is the Comparator Value (COMPV) when a match with ART time happens and a Timed GPIO output event generated. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

13.3.30 Timed GPIO0 Time Capture Register 63_32 (TGPIOTCV0_63_32)—Offset 1234h

Timed GPIO Time Capture Register 63_32

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Time Capture Value [63:32] (TCV):** Refer to Time Capture Value [31:0] for description.

13.3.31 Timed GPIO0 Event Counter Capture Register 31_0 (TGPIOECCV0_31_0)—Offset 1238h

Timed GPIO0 Event Counter Capture Register 31_0

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Event Counter Capture Value [31:0] (ECCV):** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register. A read to the Time Capture Value (TGPIOTCV0_31_0) register triggers HW to load the Event Counter value into this register. Note: The 'load' signal is the same register read signal that returns the Time Capture Value to the SW. SW must first perform a read to the Time Capture Value (TGPIOTCV0_31_0) register, followed by a read to this Event Counter Capture Value (ECCV) register such that these two values are associated with each others, despite they are obtained thru 2 separate register read operations one after another. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

13.3.32 Timed GPIO0 Event Counter Capture Register 63_32 (TGPIOECCV0_63_32)—Offset 123Ch

Timed GPIO0 Event Counter Capture Register 63_32

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Event Counter Capture Value [63:32] (ECCV):** Refer to Event Counter Capture Value [31:0] for description.

13.3.33 Timed GPIO0 Event Counter Register 31_0 (TGPIOEC0_31_0)—Offset 1240h

Timed GPIO0 Event Counter Register 31_0

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Event Counter Register [31:0] (EC):** Event Counter (EC): After Timed GPIO is enabled, event counter operates as follow: ' When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. ' When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. Note: The signal to increment the count is the same signal that captures the ART time into the TCV register. For Timed GPIO configured as output with Periodic Mode enabled, it is also the same signal that updates the Comparator Value for the subsequent match. When Timed GPIO is disabled, event counter is reset to 0x0. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

13.3.34 Timed GPIO0 Event Counter Register 63_32 (TGPIOEC0_63_32)—Offset 1244h

Timed GPIO0 Event Counter Register 63_32

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Event Counter Register [31:0] (EC):** Refer to Event Counter Register [31:0] for description.

13.3.35 Timed GPIO Control 1 (TGPIOCTL1)—Offset 1310h

Timed GPIO Control 1

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RW	**Periodic Mode (PM):** 0:Periodic mode is disabled 1:periodic mode is enabled This bit is only applicable when Timed GPIO is configured as an output
3:2	0h RW	**Event Polarity (EP):** 00:Rising Edge 01:Falling Edge 10:Toggle Edge 11:Reserved
1	0h RW	**Direction (DIR):** 0: Output 1: Input
0	0h RW	**Enable (EN):** 0: Timed GPIO is disabled 1: Timed GPIO is enabled Note: a. When Enabled, xtal clock turnoff is disabled. This may also disable SLP_S0 assertion b. All other Timed GPIO configuration bits must be programmed before enable bit is set and must not change while the enable is 1

13.3.36 Timed GPIO 1 Comparator Value 31:0 (TGPIOCOMPV1_31_0)—Offset 1320h

Timed GPIO 1 comparator Value 31:0

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Comparator Value (COMPV):** This register is only applicable when Timed GPIO is configured as an output. If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. For example, in periodic mode if the value written to this register is 00000100h, and Periodic Interval register has the value of 200h. 1. A Timed GPIO event will be generated when ART reaches 00000100h. 2. The value in this register will then be adjusted by the hardware to 00000300h. 3. Another Timed GPIO event will be generated when the ART reaches 00000300h. 4. The value in this register will then be adjusted by the hardware to 00000500h As such when periodic Timed GPIO event occurs, the value in this register will increment. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

13.3.37 Timed GPIO Comparator Value 63:32 (TGPIOCOMPV1_63_32)—Offset 1324h

Timed GPIO Comparator Value 63:32

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Comparator Value (COMPV):** Refer to Comparator Value [31:0] for description.

13.3.38 Timed GPIO1 Periodic Interval Value 31_0 (TGPIOPIV1_31_0)—Offset 1328h

Timed gPIO Periodic Interval Value 31_0

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Periodic Interval Value [31:0] (PIV):** This register is only applicable when Timed GPIO is configured as an output, and Periodic Mode is enabled. The value in this register is written by SW to set the interval for the periodic Timed GPIO event

13.3.39 Timed GPIO 1 Periodic Interval Value 63_32 (TGPIOPIV1_63_32)—Offset 132Ch

Timed GPIO 1 Periodic Interval Value 63_32

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Periodic Interval Value [63:32] (PIV):** Refer to Periodic Interval Value [31:0] for description.

13.3.40 Timed GPIO Time Capture Register 31_0 (TGPIOTCV1_31_0)—Offset 1330h

Timed GPIO Time Capture Register 31_0

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Time Capture Value [31:0] (TCV):** When Timed GPIO event triggers, HW captures the current ART time into this register. This register is applicable to both when Timed GPIO is configured as an input or an output. When Timed GPIO is configured as an output, the Time Capture Value in this register is the Comparator Value (COMPV) when a match with ART time happens and a Timed GPIO output event generated. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

13.3.41 Timed GPIO Time Capture Register 63_32 (TGPIOTCV1_63_32)—Offset 1334h

Timed GPIO Time Capture Register 63_32

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Time Capture Value [63:32] (TCV):** Refer to Time Capture Value [31:0] for description.

13.3.42 Timed GPIO0 Event Counter Capture Register 31_0 (TGPIOECCV1_31_0)—Offset 1338h

Timed GPIO0 Event Counter Capture Register 31_0

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Event Counter Capture Value [31:0] (ECCV):** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register. A read to the Time Capture Value (TCV1_31_0) register triggers HW to load the Event Counter value into this register. Note: The 'load' signal is the same register read signal that returns the Time Capture Value to the SW. SW must first perform a read to the Time Capture Value (TCV1_31_0) register, followed by a read to this Event Counter Capture Value (ECCV) register such that these two values are associated with each others, despite they are obtained thru 2 separate register read operations one after another. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

13.3.43 Timed GPIO0 Event Counter Capture Register 63_32 (TGPIOECCV1_63_32)—Offset 133Ch

Timed GPIO0 Event Counter Capture Register 63_32

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Event Counter Capture Value [63:32] (ECCV):** Refer to Event Counter Capture Value [31:0] for description.

13.3.44 Timed GPIO1 Event Counter Register 31_0 (TGPIOEC1_31_0)—Offset 1340h

Timed GPIO1 Event Counter Register 31_0

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Event Counter Register [31:0] (EC):** Event Counter (EC): After Timed GPIO is enabled, event counter operates as follow: ' When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. ' When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. Note: The signal to increment the count is the same signal that captures the ART time into the TCV register. For Timed GPIO configured as output with Periodic Mode enabled, it is also the same signal that updates the Comparator Value for the subsequent match. When Timed GPIO is disabled, event counter is reset to 0x0. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

13.3.45 Timed GPIO Event Counter Register 63_32 (TGPIOEC1_63_32)—Offset 1344h

Timed GPIO Event Counter Register 63_32

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Event Counter Register [31:0] (EC):** Refer to Event Counter Register [31:0] for description.

13.3.46 Catastrophic Trip Point Enable (CTEN)—Offset 150Ch

This register is used to enable Catastrophic Trip point assertion into S5 state on a Cattrip event. This bit should always be set in all functional cases.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Policy Lock-Down Bit (CTENLOCK):** When written to 1, this bit prevents any more writes to this register.
30:1	0h RO	Reserved.
0	1h RW/L	**Catastrophic Power-Down Enable (CPDEN):** 1 = the power management logic (PMC) transitions to the S5 state when a catastrophic temperature is detected by any of the sensor. The transition to the S5 state is unconditional (like the Power Button Override Function). 0 = Disable going into S5 state on a CatTrip detection. This bit should only be set to 0 for debug purposes. Note: Thermal sensor and response logic are in the core/main power well; therefore, detection of a catastrophic temperature is limited to times when this well is powered and out of reset.

13.3.47 EC Thermal Sensor Reporting Enable (ECRPTEN)—Offset 1510h

This is a BIOS programmable register used to enable reporting of temperature by PMC to EC over eSPI. Setting bit 0 will cause a GCR interrupt to PMC FW through generic GCR mechanism. FW needs to enable the periodic reporting task accordingly. Bit 31 is uses as a lock bit to prevent any further writes to bit 0.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Lock-Down Bit (ECRPTENLOCK):** When written to 1, this bit prevents any more writes to this register.
30:1	0h RO	Reserved.
0	0h RW/L	**Enable PMC to EC Temperature Reporting (EN_PMC_TO_EC_TEMP_RPT):** 0x1 : Enables the reporting of the PCH temperature to the EC (via SMBUS or eSPI). Note that this must also be set if Intel (R) CSME needs access to the PCH temperature. Once enabled this bit should not be cleared by SW. If it is cleared then the EC may get an undefined value. SW has no need to dynamically disable and then re-enable this bit. 0x0 (Default) : Disables temperature reporting (default)

13.3.48 Throttle Level (TL)—Offset 1520h

Throttle Level.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: FF3FCFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**TLLOCK (TLLOCK):** When set to 1, this entire register (TL) is locked and remains locked until the next platform reset
30	0h RW/L	**TT State 13 Enable (TT13EN):** When set to 1 and the programmed GPIO pin is a 1, then PMSync state 13 (now called GPIO_A) will force at least T2 state.
29	0h RW/L	**TT Enable (TTEN):** This is the enable bit associated with the FW control of the throttle state. This bit needs to be set in order for the FW to be able to update the throttle state based on the comparison of the T2L/T1L/T0L with the temperature. At reset, BIOS must set bits 28:0 and then do a separate write to set bit 29 to enable throttling. SW may set bit 31 at the same time it sets bit 29 if it wishes to lock the register. If SW wishes to change the values of 28:0, it must first clear the TTEN bit, then change the values in 28:0; and then re-enable TTEN. It is legal to set bits 31, 30 and 29 with the same write This bit must not be set by SW until SW has already enabled atleast one of the thermal sensor(setting TSENx.ETS bits to 1) If TTEN is written to 0, after having been enabled, then the PCH may stay in the throttling state it was in at the moment TTEN is disabled. There is no intent that the sensor be enabled for a while and then disabled and left off. It may be disabled temporarily while changing the register values, but it should not be left in the disabled state
28:20	FFh RW/L	**T2 Level (T2L):** Determines the temp level for T2 state. If TTEN = 1 AND TSEN = 1 AND T2L >= TEMP.MAXTEMP[8:0] > T1L, then the system is in T2 state. If TTEN = 1 AND TSE = 1 AND TEMP.MAXTEMP [8:0] > T2L, then the system is in T3 state.SW Note: When TTEN =1 condition to satisfy is T2L > T1L > T0L NOTE: the T3 condition overrides PMSync[13] and forces the system to T3 if both cases are true

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	Reserved.
18:10	FFh RW/L	**T1 Level (T1L):** Determines the temp level for T1 state. If TTEN = 1 AND (|TSEN) = 1 AND T1L >= TEMP.MAXTEMP[8:0] > T0L, then the system is in T1 state. SW Note: When TTEN =1 condition to satisfy is T2L > T1L > T0L
9	0h RO	Reserved.
8:0	FFh RW/L	**T0 Level (T0L):** Determines the temp level for T0 state. If TEMP.MAXTEMP[8:0] <= T0L or TTEN = 0 OR (|TSEN) = 0, then the system is in T0 state SW Note: When TTEN =1 condition to satisfy is T2L> T1L > T0L

13.3.49 Throttle Levels Enable (TLEN)—Offset 1528h

Throttle Levels Enable

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**TLENLOCK (TLENLOCK):** When set to 1, this entire register (TLEN) is locked and remains locked until the next platform reset
30:0	0h RO	Reserved.

13.3.50 Thermal Sensor Alert High Value (TSAHV)—Offset 1530h

This register is used to set the Thermal Alert High Value for all Thermal Sensors on the chip. PMC HW should compare the aggregated MAXTEMP against these values to cause an SMI or SCI Interrupt

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: FFh

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8:0	FFh RW	**Alert High Value (AHV):** Sets the high value for the alert indication. Temperature programmed in S9.8.0 2s complement format This register is not lockable, so that SW can change the values during runtime. NOTE: it is unsupported for SW to program TSAHV.AHV to a value lower than TSAL.ALV

13.3.51 Thermal Sensor Alert Low Value (TSALV)—Offset 1534h

This register is used to set the Thermal Alert Low Value for all Thermal Sensors on the chip. PMC HW should compare the aggregated MINTEMP against these values to cause an SMI or SCI Interrupt

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8:0	0h RW	**Alert Low Value (ALV):** Sets the low value for the alert indication. Temperature programmed in S9.8.0 2s complement format This register is not lockable, so that SW can change the values during runtime. NOTE: it is unsupported for SW to program TSALV.ALV to a value higher than TSAH.AHV

13.3.52 Thermal Alert Trip Status (TAS)—Offset 1538h

SW uses this register to determine the Thermal Alert Trip event (Low-to-High or High-to-Low) along with the Thermal Sensor ID that caused this event.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C/V	**TS Alert High-to-Low Event (AHLE):** 0x1: Indicates that an Thermal Sensor trip event occurred based on a higher to lower temperature transition thru the trip point 0x0: No trip for this event Software must write a 1 to clear this status bit Note: AHLE will not be set until there has been one occurrence of a Low to High event (ALHE must have been set once). This prevents the case where the system power up at a reasonably high temperature and starts to cool off while booting and causing an interrupt before there is SW loaded to handle it
14:12	0h RO	Reserved.
11:8	0h RO/V	**High-to-Low trip TS (HLTTS):** 0xF 0x3 : Reserved 0x2 : TS2 0x1 : TS1 0x0 : TS0
7	0h RW/1C/V	**TS Alert Low-to-High Event (ALHE):** 0x1: Indicates that an Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point 0x0: No trip for this event Software must write a 1 to clear this status bit Note: AHLE will not be set until there has been one occurrence of a Low to High event (ALHE must have been set once). This prevents the case where the system power up at a reasonably high temperature and starts to cool off while booting and causing an interrupt before there is SW loaded to handle it
6:4	0h RO	Reserved.
3:0	0h RO/V	**Low-to-High trip TS (LHTTS):** 0xF 0x3 : Reserved 0x2 : TS2 0x1 : TS1 0x0 : TS0

13.3.53 PCH Hot Level Control (PHLC)—Offset 1540h

PCH Hot Level Control

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**PHL Lock (PHLCLOCK):** When written to a 1, this entire register is locked and remains locked until next platform reset
30:16	0h RO	Reserved.
15	0h RW/L	**PHL Enable (PHLE):** When set and the current temperature reading, MaxTSR is greater than PHLL, then the PCHHOT# pin will be asserted (active low)
14:9	0h RO	Reserved.
8:0	0h RW/L	**PHL Level (PHLL):** Temperature value used for PCHHOT# pin assertion based on 2s complement format 0x001 positive 1oC 0x000 0oC 0x1FF negative 1oC 0x1D8 negative 40oC and so on

13.3.54 Temperature Sensor Control and Status (TSS0)—Offset 1560h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Policy Lock-Down Bit (TSS0LOCK):** When set to 1, this bit locks down the following fields: - TSS0.TSMASKEN The other bits in TSSx are anyway RO and hence do not need a lock bit set for them.Those bits become read-only . This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a global reset.
30:17	0h RO	Reserved.
16	0h RW/L	**TS MASK for MAXTEMP calculation (TSMASKEN):** 0 (Default) = Temperature reported from TS is used for temperature comparison with PMC. 1 = Temperature reported from the TS is masked for TEMP comparison within PMC. This in turn will also enable/disable SMI/SCI assertions for alert thermal events from this TS.
15:10	0h RO	Reserved.
9	0h RO/V	**TS Reading Valid (TSRV):** This bit indicates if the TS die temperature reported in valid or not.
8:0	0h RO/V	**TS Reading (TSR):** The TS die temperature with resolution of 1oC in S9.8.0 2s complement format 0x001 positive 1oC 0x000 0oC 0x1FF negative 1oC 0x1D8 negative 40oC and so on

13.3.55 Wake Alarm Device Timer: AC (WADT_AC)—Offset 1800h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/V	**Wake Alarm Device Timer Value for AC Mode (WADT_AC_VAL):** This field contains the 32-bit wake alarm device timer value (granularity 1s) for AC power. The timer begins decrementing when written to a value other than FFFFFFFFh (regardless of the power source when the write occurs). Upon counting down to 0: - If on AC power, GPE0b_STS.WADT_STS will be set. This status bit being set will generate a host wake if GPE0b_EN.WADT_EN is 1. - If the power source is DC at this time, the status bit is not set. However, if AC power subsequently returns to the platform, the AC Expired Timer begins running. See the WADT_EXP_AC register for details. - The timer returns to its default value of FFFFFFFFh. This bit is reset by DSW_PWROK de-assertion.

13.3.56 Wake Alarm Device Timer: DC (WADT_DC)—Offset 1804h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/V	**Wake Alarm Device Timer Value for DC Mode (WADT_DC_VAL):** This field contains the 32-bit wake alarm device timer value (granularity 1s) for DC power. The timer begins decrementing when written to a value other than FFFFFFFFh (regardless of the power source when the write occurs). Upon counting down to 0: - If on DC power, GPE0b_STS.WADT_STS will be set. This status bit being set will generate a host wake if GPE0b_EN.WADT_EN is 1. - If the power source is AC at this time, the status bit is not set. However, if DC power subsequently returns to the platform, the DC Expired Timer begins running. See the WADT_EXP_DC register for details. - The timer returns to its default value of FFFFFFFFh. This bit is reset by DSW_PWROK de-assertion.

13.3.57 Wake Alarm Device Expired Timer: AC (WADT_EXP_AC)—Offset 1808h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/V	**Wake Alarm Device Expired Timer Value for AC Mode (WADT_EXP_AC_VAL):** This field contains the 32-bit wake alarm device "Expired Timer" value (granularity 1s) for AC power. The timer begins decrementing after switching from DC to AC power. In the case where the WADT_AC timer has already expired while the platform was on DC power, this timer only decrements while operating on AC power. So if the power source switches back to DC power, the timer will stop (but not reset). When AC power returns, the timer will again begin decrementing. Note: This timer will only begin decrementing under the conditions described above if this field has been configured for something other than its default value of FFFFFFFFh (i.e. FFFFFFFFh = disabled). Upon expiration of this timer: - If on AC power, GPE0b_STS.WADT_STS will be set. This status bit being set will generate a host wake if GPE0b_EN.WADT_EN is 1. - BOTH the AC and DC Expired Timers return to their defaults value of FFFFFFFFh. This bit is reset by DSW_PWROK de-assertion.

13.3.58 Wake Alarm Device Expired Timer: DC (WADT_EXP_DC)—Offset 180Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/V	**Wake Alarm Device Expired Timer Value for DC Mode (WADT_EXP_DC_VAL):** This field contains the 32-bit wake alarm device "Expired Timer" value (granularity 1s) for DC power.The timer begins decrementing after switching from AC to DC power. In the case where the WADT_DC timer has already expired while the platform was on AC power, this timer only decrements while operating on DC power. So if the power source switches back to AC power, the timer will stop (but not reset). When DC power returns, the timer will again begin decrementing. Note: This timer will only begin decrementing under the conditions described above if this field has been configured for something other than its default value of FFFFFFFFh (i.e. FFFFFFFFh = disabled). Upon expiration of this timer: - If on DC power, GPE0b_STS.WADT_STS will be set. This status bit being set will generate a host wake if GPE0b_EN.WADT_EN is 1. - BOTH the AC and DC Expired Timers return to their defaults value of FFFFFFFFh. This bit is reset by DSW_PWROK de-assertion.

13.3.59 Power and Reset Status (PRSTS)—Offset 1810h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5	0h RW/1C/V	**Wake On LAN Override Wake Status (WOL_OVR_WK_STS):** This bit gets set when integrated LAN Signals a Power Management Event AND the system is in S5. BIOS can read this status bit to determine this wake source. Software clears this bit by writing a 1 to it.
4:1	0h RO	Reserved.
0	0h RW/1C/V	**ME_HOST_WAKE_STS (ME_HOST_WAKE_STS):** This bit is set when the ME generates a non-maskable wake event and is not affected by any other enable bit. When this bit is set, the host power management logic wakes to S0.

13.3.60 Power Management Configuration Reg 1 (PM_CFG)—Offset 1818h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 20h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	Reserved.
25	0h RW	**Allow USB2 PHY Core Power Gating (ALLOW_USB2_CORE_PG):** When this bit is '0' (default), USB2 PHY power gating is disabled. When this bit is '1', USB2 PHY power gating can occur if all other required conditions are met.
24	0h RW/L	**Energy Reporting Lock (ER_LOCK):** When this bit is written to 1, it will remain 1 until the next host_prim_rst_b assertion. While this bit is 1, GEN_PMCON_A.ER_EN value cannot be changed. BIOS should write 1b1 to this bit only AFTER writing to GEN_PMCON_A.ER_EN.
23:22	0h RO	Reserved.
21	0h RW	**RTC Wake from DeepSx Disable (RTC_DSX_WAKE_DIS):** When set, this bit disables RTC wakes from waking the system from DeepSx. This bit is reset by RTCRST# assertion.
20	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
19:18	0h RW/L	**SLP_SUS# Minimum Assertion Width (SLP_SUS_MIN_ASST_WDTH):** This 2-bit value indicates the minimum assertion width of the SLP_SUS# signal to guarantee that the SUS well power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power failure detection circuits, etc. Settings are: 00 = 0 ms (i.e. stretching disabled - default) 01 = 500ms 10 = 1s 11 = 4s This field is not writable when the SLP_Sx# Stretching Policy Lock- Down bit is set. This field is ignored when exiting a G3 state if the "Disable SLP_X Stretching After SUS Power Failure" bit is set. Note that unlike with all other SLP_* pin stretching, this disable bit only impacts SLP_SUS# stretching during G3 exit rather than both G3 and DeepSx exit. SLP_SUS# stretching always applies to DeepSx regardless of the disable bit. Programming Note: For platforms that enable DeepSx, BIOS must program SLP_SUS# stretching to be greater than or equal to the largest stretching value on any other SLP_* pin (SLP_S3#, SLP_S4#, SLP_LAN#, or SLP_A#). This bit is cleared by the RTCRST# pin.
17:16	0h RW/L	**SLP_A# Minimum Assertion Width (SLP_A_MIN_ASST_WDTH):** This 2-bit value indicates the minimum assertion width of the SLP_A# signal to guarantee that the ASW power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power failure detection circuits, etc. Settings are: 00 = 0 ms (i.e. stretching disabled - default) 01 = 4 s 10 = 98 ms 11 = 2 s This field is not writable when the SLP_Sx# Stretching Policy Lock- Down bit is set. This field is ignored when exiting a G3 or Deep Sx state if the "Disable SLP_X Stretching After SUS Power Failure" bit is set. This bit is cleared by the RTCRST# pin.
15:14	0h RW/L	**SLP_LAN# Minimum Assertion Width (SLP_LAN_MIN_ASST_WDTH):** This 2-bit value indicates the minimum assertion width of the SLP_LAN# signal to guarantee that the power to the PHY has been fully power-cycled. This value may be modified per platform depending on power supply, capacitance, board capacitance, power failure detection circuits, etc. This field is not writable when the SLP_Sx# Stretching Policy Lock Down bit is set to 1. This bit is reset by RTCRST# assertion.
13	0h RW	**After G3 Last State Enable (AG3_LS_EN):** When PM_CFG.AG3E is '0', AG3_LS_EN determines whether the PCH will consider the platform's previous state when determining whether to power-up after G3. Encodings: 0: PCH power-up policies after G3 do not depend on the platform's state when the G3 occurred. (default) 1: PCH power-up policies after G3 depend on the platform's state when the G3 occurred. - If the power failure occurred while the platform was in S0 or while in the process of going to S0, the platform will power-up to S0 upon exiting G3. - If the power failure occurred while the platform was in Sx or while in the process of going to Sx, the platform will stay in S4/S5 upon exiting G3. Note: This bit applies only when GEN_PMCON_3.AG3E is '0'. If AG3E is '1', the platform will always stay in S4/S5 after G3 regardless of the value of AG3_LS_EN.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**After Type 8 Global Reset Last State Enable (A8GR_LS_EN):** AGR_LS_EN determines whether the PCH will consider the platform's previous state when determining whether to power-up after non-thermal and non-explicitly requested type 8 global resets. Encodings: 0 (default): PCH power-up policies after a global reset do not depend on the platform's state when the reset occurred. 1: PCH power-up policies after a global reset depend on the platform's state when the reset occurred. If the global reset occurred while the platform was in S0 or while in the process of going to S0, the platform will power-up to S0 after the reset. If the global reset occurred while the platform was in Sx or while in the process of going to Sx, the platform will stay in S5 upon exiting G3.
11	0h RO	Reserved.
10	0h RW	**Power Button Debounce Mode (PB_DB_MODE):** This bit controls when interrupts (SMI#, SCI) are generated in response to assertion of the PWRBTN# pin. This bit's values cause the following behavior: - '0': The 16ms debounce period applies to all usages of the PWRBTN# pin (legacy behavior). - '1': When a falling edge occurs on the PWRBTN# pin, an interrupt is generated and the 16ms debounce timer starts. Subsequent interrupts are masked while the debounce timer is running. Note: Power button override logic always samples the post-debounce version of the pin. This bit is reset by RTCRST# assertion.
9:8	0h RW/L	**Reset Power Cycle Duration (PWR_CYC_DUR):** The value in this register determines the minimum time a platform will stay in reset (SLP_S3#, SLP_S4#, SLP_S5# asserted and also SLP_A# and SLP_LAN# asserted if applicable) during a host partition reset with power cycle or a global reset. The duration programmed in this register takes precedence over the applicable SLP_# stretch timers in these reset scenarios. This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. Note that the duration programmed in this register should never be smaller than the stretch duration programmed in the following registers - - GEN_PMCON_3.SLP_S3_MIN_ASST_WDTH - GEN_PMCON_3.S4MAW - PM_CFG.SLP_A_MIN_ASST_WDTH - PM_CFG.SLP_LAN_MIN_ASST_WDTH This bit is reset by RTCRST# assertion. 00 = 4 - 5 seconds 01 = 3 - 4 seconds 10 = 2 - 3 seconds 11 = 1 - 2 seconds
7:6	0h RO	Reserved.
5	1h RW/V	**CPU OC Strap (COCS):** SW programs this pin with the value that should be reflected to the GPIO8_OCS pin, when the pin is in native mode. Hardware also sets this bit when the over-clocking watchdog timer expires. This bit is reset by RSMRST# assertion.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RO	Reserved.
2	0h RW/L	**Energy Reporting Enable (ER_EN):** When this bit is 1, the PCH will periodically calculate and report its energy consumption to the CPU via PM_SYNC. When this bit is 0, the PCH will neither calculate nor report its energy consumption.
1:0	0h RW/V	**Timing t581 (TIMING_T581):** This field configures the t581 timing involved in the power down flow (CPUPWRGD inactive to ICC_ICLK_INIT inactive). Encodings (all min timings): 00: 10 us (default) 01: 100 us 10: 1 ms 11: 10 ms reset_type=host_deep_rst_b

13.3.61 S3 Power Gating Policies (S3_PWRGATE_POL)—Offset 1828h

This register contains policy bits to configure various power gating options while the system is in S3. Note that setting any of these policies to "enabled" may not directly result in power gating - in some cases other HW qualifications may be dynamically applied.
This register is in the RTC power well and is reset by RTCRST# assertion.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW	**S3 Power Gate Enable in DC Mode: SUS Well (S3DC_GATE_SUS):** A '1' in this bit enables power gating of the SUS well in S3 while operating on DC power (based on the AC_PRESENT pin value).
0	0h RW	**S3 Power Gate Enable in AC Mode: SUS Well (S3AC_GATE_SUS):** A '1' in this bit enables power gating of the SUS well in S3 while operating on AC power (based on the AC_PRESENT pin value).

13.3.62 S4 Power Gating Policies (S4_PWRGATE_POL)—Offset 182Ch

This register contains policy bits to configure various power gating options while the system is in S4. Note that setting any of these policies to "enabled" may not directly result in power gating - in some cases other HW qualifications may be dynamically applied.
This register is in the RTC power well and is reset by RTCRST# assertion.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW	**S4 Power Gate Enable in DC Mode: SUS Well (S4DC_GATE_SUS):** A '1' in this bit enables power gating of the SUS well in S4 while operating on DC power (based on the AC_PRESENT pin value).
0	0h RW	**S4 Power Gate Enable in AC Mode: SUS Well (S4AC_GATE_SUS):** A '1' in this bit enables power gating of the SUS well in S4 while operating on AC power (based on the AC_PRESENT pin value).

13.3.63 S5 Power Gating Policies (S5_PWRGATE_POL)—Offset 1830h

This register contains policy bits to configure various power gating options while the system is in S5. Note that setting any of these policies to "enabled" may not directly result in power gating - in some cases other HW qualifications may be dynamically applied.
This register is in the RTC power well and is reset by RTCRST# assertion.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**S5 Power Gate Enable in DC Mode: SUS Well (S5DC_GATE_SUS):** A '1' in this bit enables power gating of the SUS well in S5 while operating on DC power (based on the AC_PRESENT pin value).
14	0h RW	**S5 Power Gate Enable in AC Mode: SUS Well (S5AC_GATE_SUS):** A '1' in this bit enables power gating of the SUS well in S5 while operating on AC power (based on the AC_PRESENT pin value).
13:0	0h RO	Reserved.

13.3.64 DeepSx Configuration (DSX_CFG)—Offset 1834h

This register contains misc. fields used to configure the PCH's power management behavior.
This register is in the RTC power well and is reset by RTCRST# assertion.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RW	**Require CNV Wake Disabled for DeepSx Entry/SUSPWRDNACK (REQ_CNV_NOWAKE_DSX):** If this bit is 0, the state of connectivity wake enable is not considered when making DeepSx entry decisions. If this bit is 1, connectivity wake must be disabled to allow DeepSx entry or SUSPWRDNACK assertion, and even then all other conditions must be satisfied.
3	0h RW	**Require BATLOW# Assertion for DeepSx Entry/SUSPWRDNACK (REQ_BATLOW_DSX):** If this bit is 0, the state of the BATLOW# pin is not considered when making DeepSx entry and SUSPWRDNACK decisions. If this bit is 1, BATLOW# must be asserted to allow DeepSx entry or SUSPWRDNACK assertion, and even then all other entry conditions must be satisfied.
2	0h RW	**WAKE# Pin DeepSx Enable (WAKE_PIN_DSX_EN):** When this bit is 1, the PCI Express WAKE# pin is monitored while in Deep Sx, supporting waking from Deep Sx due to assertion of this pin. In this case, the platform must externally pull up the pin to the DSW (instead of pulling up to the SUS as has historically been the case). When this bit is 0: - DeepSx enabled configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time. -Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled Note: Deep Sx disabled configurations must leave this bit at 0.
1	0h RW	**AC_PRESENT Pin Pulldown in DeepSx Disable (ACPRES_PD_DSX_DIS):** When this bit is 1, the internal pull-down on the ACPRESENT pin is disabled. However, the pulldown is not necessarily enabled if the bit is '0'. This bit must be left at '0' for Deep Sx disabled configurations, and the pulldown is disabled for those configurations even though the bit is '0'. To support Intel (R) CSME wakes from Deep Sx, the pin is always monitored regardless of the value of this host policy bit. When this bit is '0': DeepSx enabled configurations: The PCH internal pull-down on ACPRESENT is enabled in Deep Sx and during G3 exit. Deep Sx disabled configurations: The PCH internal pull-down on ACPRESENT is always disabled.
0	0h RW	**LANWAKE Pin DeepSx Enable (LANWAKE_PIN_DSX_EN):** When this bit is 1, the LANWAKE pin is monitored while in DeepSx, supporting waking from DeepSx due to assertion of this pin. In this case, the platform must drive the pin to the correct value while in DeepSx. DeepSx disabled configurations must leave this bit at 0. When this bit is 0: DeepSx enabled configurations: The PCH internal pull-down on LANWAKE pin is enabled in deep-Sx and during G3 exit and the pin is not monitored during this time. DeepSx disabled configurations: The PCH internal pull-down is never enabled

13.3.65 Power Management Configuration Reg 2 (PM_CFG2)—Offset 183Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**Power Button Override Period (PBOP):** This field determines, while the power button remains asserted, how long the PMC will wait before initiating a global reset. Encoding: 000b - 4 seconds 001b - 6 seconds 010b - 8 seconds 011b - 10 seconds 100b - 12 seconds 101b - 14 seconds Others - Reserved This bit is reset by DSW_PWROK de-assertion.
28	0h RW/L	**Power Button Native Mode Disable (PB_DIS):** When this bit is '0' (default), the PMC's power button logic will act upon the input value from the GPIO unit, as normal. When this bit is set to '1', the PMC must force its internal version of the power button pin to '1'. This will result in the PMC logic constantly seeing the pin as de-asserted. This bit is reset by RTCRST# assertion.
27	0h RO	Reserved.
26	0h RW/V	**DRAM_RESET# Control (DRAM_RESET_CTL):** BIOS uses this bit to control the DRAM_RESET# pin from the PCH, which is routed to the reset pin on the DRAM. Encoding: 0 = DRAM_RESET# output is asserted (driven low) 1 = DRAM_RESET# output is tri-stated. Note: This bit is cleared to '0' by HW when SLP_S4# goes low. This bit is reset by DSW_PWROK de-assertion.
25:0	0h RO	Reserved.

13.3.66 PM_SYNC Miscellaneous Configuration (PM_SYNC_MISC_CFG)—Offset 18C8h

This register is used to configure miscellaneous aspects of the PM_SYNC pin.
This register is in the CORE power well and is reset by PLTRST#.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW/L	**GPIO_D Pin Selection (GPIO_D_SEL):** There are two possible GPIOs that can be routed to the GPIO_D PM_SYNC state. This bit selects between them: 0: CPU_GP_3 (default) 1: CPU_GP_2 This field is not writeable when PM_SYNC_LOCK=1.
10	0h RW/L	**GPIO_C Pin Selection (GPIO_C_SEL):** There are two possible GPIOs that can be routed to the GPIO_C PM_SYNC state. This bit selects between them: 0: CPU_GP_0 (default) 1: CPU_GP_1 This field is not writeable when PM_SYNC_LOCK=1.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/L	**GPIO_B Pin Selection (GPIO_B_SEL):** There are two possible GPIOs that can be routed to the GPIO_B PM_SYNC state. This bit selects between them: 0: CPU_GP_2 (default) 1: CPU_GP_0 This field is not writeable when PM_SYNC_LOCK=1.
8	0h RW/L	**GPIO_A Pin Selection (GPIO_A_SEL):** There are two possible GPIOs that can be routed to the GPIO_A PM_SYNC state. This bit selects between them: 0: CPU_GP_1 (default) 1: CPU_GP_3 This field is not writeable when PM_SYNC_LOCK=1.
7:0	0h RO	Reserved.

13.3.67 Chipset Initialization Register E0 (CIRE0)—Offset 18E0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW	**Host Wireless LAN Phy Power Enable (HOST_WLAN_PP_EN):** This policy bit is set by Host software when it desires the wireless LAN PHY to be powered in Sx power states for wakes over wireless LAN (WoWLAN). This bit is reset by DSW_PWROK de-assertion.
16	0h RW	**Deep-Sx WLAN Phy Power Enable (DSX_WLAN_PP_EN):** When set to '1, PMC will keep SLP_WLAN# high in deep-Sx to enable WoWLAN. Note: 1. This policy bit will be applied for Deep Sx entry from S3, S4 and S5. 2. This bit does not affect SLP_WLAN# behaviour in Sx after G3 or after a global reset 3. HOST_WLAN_PP_EN must be set when this bit is set. This bit is reset by DSW_PWROK de-assertion.
15:0	0h RO	Reserved.

13.3.68 CPU Early Power-on Configuration (CPU_EPOC)—Offset 18ECh

CPU Early Power on Configuration

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21:20	0h RO/V	**Crystal Frequency[2:1] (XTAL_FREQ_MSB):** Along with XTAL_FREQ_LSB the 3 bit field reflects the frequency of the crystal (aka NSSC) clock used by the CPU and PCH Encoding: 000b -24MHz 001b -19.Mhz 010b -38.4 Mhz Others - Reserved
19:18	0h RO	Reserved.
17	0h RO/V	**Crystal Frequency [0] (XTAL_FREQ_LSB):** See XTAL_FREQ_MSB
16:8	0h RO	Reserved.
7:3	0h RW/L	**EPOC Data [7:3] (EPOC_DATA_7_3):** EPOC Data [7:3]
2	0h RO	Reserved.
1:0	0h RW/L	**EPOC Data [1:0] (EPOC_DATA_1_0):** EPOC Data [1:0]

13.3.69 ACPI Timer Control (ACPI_TMR_CTL)—Offset 18FCh

This register allows software to disable the ACPI Timer, which could result in power savings for the PCH.
This register is in the CORE power well and is reset by PLTRST#

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW	**ACPI Timer Disable (ACPI_TIM_DIS):** This bit determines whether the ACPI Timer is enabled to run. - 0: ACPI Timer is enabled (default) - 1: ACPI Timer is disabled (halted at the current value) Even when enabled, the timer only runs during S0. This bit must only be set to "1" if the operating system can tolerate disabling the 14.31818 MHz ACPI PM Timer. Note: 1.Some operating systems may only tolerate disabling the timer during entry into deep idle states. In such cases, the bit must be set to "1" during entry into those states and cleared to "0" during exit. This bit is reset by PLTRST# assertion.
0	0h RW/1S/V	**ACPI Timer Clear (ACPI_TIM_CLR):** Writing a 1 to this bit will clear the ACPI Timer to all 0s. Hardware will automatically clear the bit back to 0 once the timer clear operation has completed. Writing a 0 to this bit has no effect. The PCH is capable of honoring this bit even while ACPI_TIM_DIS=1. This bit is reset by PLTRST# assertion.

13.3.70 Last TSC Alarm Value[31:0] (TSC_ALARM_LO)—Offset 1910h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Last TSC Alarm Value [31:0] (TSC_ALARM_VAL_LO):** This field contains bits 31:0 of the last TSC alarm value received from the CPU. This field is reset by PLTRST# assertion.

13.3.71 Last TSC Alarm Value[63:32] (TSC_ALARM_HI)—Offset 1914h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Last TSC Alarm Value [63:32] (TSC_ALARM_VAL_HI):** This field contains bits 63:32 of the last TSC alarm value received from the CPU. This field is reset by PLTRST# assertion.

13.3.72 GPIO Configuration (GPIO_CFG)—Offset 1920h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 432h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11:8	4h RW	**GPIO Group to GPE_DW2 assignment encoding (GPE0_DW2):** This register assigns a specific GPIO Group to the ACPI GPE0[95:64]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_B[23:0] mapped to GPE[87:64]; other GPE bits not used. 1h = GPP_T[3:2] mapped to GPE[67:66]; other GPE bits not used. 2h = GPP_A[23:0] mapped to GPE[87:64]; other GPE bits not used. 3h = GPP_R[7:0] mapped to GPE[71:64]; other GPE bits not used. 4h = GPD[11:0] mapped to GPE[75:64]; other GPE bits not used. 5h = GPP_S[7:0] mapped to GPE[71:64]; other GPE bits not used. 6h = GPP_H[23:0] mapped to GPE[87:64]; other GPE bits not used. 7h = GPP_D[19:0] mapped to GPE[83:64]; other GPE bits not used. 8h-9h = Reserved Ah = GPP_F[23:0] mapped to GPE[87:64]; other GPE bits not used. Bh = GPP_C[23:0] mapped to GPE[87:64]; other GPE bits not used. Ch = GPP_E[23:0] mapped to GPE[87:64]; other GPE bits not used. Dh - Fh = Reserved
7:4	3h RW	**GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1):** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_B[23:0] mapped to GPE[55:32]; other GPE bits not used. 1h = GPP_T[3:2] mapped to GPE[35:34]; other GPE bits not used. 2h = GPP_A[23:0] mapped to GPE[55:32]; other GPE bits not used. 3h = GPP_R[7:0] mapped to GPE[39:32]; other GPE bits not used. 4h = GPD[11:0] mapped to GPE[43:32]; other GPE bits not used. 5h = GPP_S[7:0] mapped to GPE[39:32]; other GPE bits not used. 6h = GPP_H[23:0] mapped to GPE[55:32]; other GPE bis not used. 7h = GPP_D[19:0] mapped to GPE[41:32]; other GPE bits not used. 8h-9h = Reserved Ah = GPP_F[23:0] mapped to GPE[55:32]; other GPE bits not used. Bh = GPP_C[23:0] mapped to GPE[55:32]; other GPE bits not used. Ch = GPP_E[23:0] mapped to GPE[55:32]; other GPE bits not used. Dh - Fh = Reserved
3:0	2h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0):** This register assigns a specific GPIO Group to the ACPI GPE0[31:0]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_B[23:0] mapped to GPE[23:0]; other GPE bits not used. 1h = GPP_T[3:2] mapped to GPE[3:2]; other GPE bits not used 2h = GPP_A[23:0] mapped to GPE[23:0]; other GPE bits not used. 3h = GPP_R[7:0] mapped to GPE[7:0]; other GPE bits not used. 4h = GPD[11:0] mapped to GPE[11:0]; other GPE bits not used. 5h = GPP_S[7:0] mapped to GPE[7:0]; other GPE bits not used. 6h = GPP_H[23:0] mapped to GPE[23:0]; other GPE bits not used. 7h = GPP_D[19:0] mapped to GPE[19:0]; other GPE bits not used. 8h-9h = Reserved Ah = GPP_F[23:0] mapped to GPE[23:0]; other GPE bits not used. Bh = GPP_C[23:0] mapped to GPE[23:0]; other GPE bits not used. Ch = GPP_E[23:0] mapped to GPE[23:0]; other GPE bits not used. Dh - Fh = Reserved

13.3.73 Global Reset Causes (GBLRST_CAUSE0)—Offset 1924h

This register logs causes of host partition resets.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RW/1C/V	**PMC RF FUSA Error Global Reset (PMC_RF_FUSA_ERROR):** This bit is set to 1 by hardware if an MBIST error is detected from any RFs during FUSA Power-On Self Test.
23:17	0h RO	Reserved.
16	0h RW/1C/V	**CPU Thermal Runaway Watchdog Timer (CPU_THRM_WDT):** This bit is set to '1' by hardware when a global reset is triggered by the expiration of the CPU Thermal Runaway Watchdog Timer.
15:13	0h RO	Reserved.
12	0h RW/1C/V	**SYS_PWROK Failure (SYSPWR_FLR):** This bit is set to '1' by hardware when a global reset is triggered by an unexpected loss of SYS_PWROK. This bit is reset by DSW_PWROK de-assertion.
11	0h RW/1C/V	**PCH_PWROK Failure (PCHPWR_FLR):** This bit is set to '1' by hardware when a global reset is triggered by an unexpected loss of PCH_PWROK. This bit is reset by DSW_PWROK de-assertion.
10	0h RW/1C/V	**PMC Firmware Global Reset (PMC_FW):** This bit is set to '1' by hardware when a global reset is triggered by a request from PMC firmware (i.e. a write of '1' to the GBLRST_CTL.TRIG_GBL bit).
9:6	0h RO	Reserved.
5	0h RW/1C/V	**CPU Thermal Trip (CPU_TRIP):** This bit is set to '1' by hardware when a global reset is triggered by a CPU thermal trip event (i.e. an assertion of the THRMTRIP# pin).
4	0h RO	Reserved.
3	0h RW/1C/V	**PCH Catastrophic Temperature Event (ICH_CAT_TMP):** This bit is set to '1 by hardware when a global reset is triggered by a catastrophic temperature event from the ICH internal thermal sensor.
2	0h RO	Reserved.
1	0h RW/1C/V	**Power Button Override (PB_OVR):** This bit is set to '1' by hardware when a global reset is triggered by a power button override (i.e. an assertion of the PWRBTN# pin for 5 seconds). This bit is reset by DSW_PWROK de-assertion.
0	0h RO	Reserved.

13.3.74 Global Reset Causes Register 1 (GBLRST_CAUSE1)—Offset 1928h

This register logs causes of host partition resets.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9	0h RW/1C/V	**eSPI Initiated Type 8 Global Reset (ESPI_TYPE8):** This bit is set to '1' by hardware when a shutdown is requested via eSPI
8	0h RW/1C/V	**eSPI Initiated Type 7 Global Reset (ESPI_TYPE7):** This bit is set to '1' by hardware when a global reset is requested via eSPI
7:6	0h RO	Reserved.
5	0h RW/1C/V	**Intel (R) CSME Set Power Button Status (ME_SET_PBO_STS):** If this bit is set, the cause of the previous global reset was Intel (R) CSME FW setting the power button override status. This bit is reset by DSW_PWROK de-assertion.
4	0h RO	Reserved.
3	0h RW/1C/V	**Host SMBus Message (HSMB_MSG):** If this bit is set, the cause of the previous global reset was a global reset request received over the host SMBus interface.
2	0h RW/1C/V	**Host Partition Reset Promotion (HOST_RST_PROM):** If this bit is set, the cause of the previous global reset was a host partition reset that was promoted to a global reset either due to Intel CSME or host policy. This bit is reset by DSW_PWROK de-assertion.
1	0h RO	Reserved.
0	0h RW/1C/V	**Host Partition Reset Timeout (HOST_RESET_TIMEOUT):** If this bit is set, the cause of the previous global reset was an expiration of the timer that runs during host partition resets. This bit is reset by DSW_PWROK de-assertion.

13.3.75 Host Partition Reset Causes (HPR_CAUSE0)—Offset 192Ch

This register logs causes of host partition resets.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RO/V	**eSPI Host Reset With Power Cycle (ESPI_HRWPC):** eSPI requested host partition reset with power cycle.
16	0h RO/V	**eSPI Host Reset Without Power Cycle (ESPI_HRWOPC):** eSPI requested host partition reset without power cycle
15:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO/V	**Host SMBUS Host Reset With Power Cycle (HSMB_HRPC):** SMBus initiated host partition reset with power cycle.
12	0h RO/V	**Host SMBUS Host Reset Without Power Cycle (HSMB_HR):** SMBus initiated host partition reset without power cycle.
11	0h RO	Reserved.
10	0h RO/V	**Intel CSME-Initiated Host Reset With Power Down (MI_HRPD):** Intel CSME initiated host reset with power down.
9	0h RO/V	**Intel (R) CSME-Initiated Host Reset With Power Cycle (MI_HRPC):** Intel CSME initiated host reset with power cycle.
8	0h RO/V	**Intel CSME-Initiated Host Reset Without Power Cycle (MI_HR):** Intel CSME initiated host reset without power cycle.
7	0h RO	Reserved.
6	0h RO/V	**Host TCO Watchdog Timer Second Expiration (TCO_WDT):** Host TCO watchdog timer reached zero for the second time.
5:3	0h RO	Reserved.
2	0h RO/V	**SYS_RESET# (SYSRST_ES):** Assertion of the SYS_RESET# pin after the 16 ms HW debounce.
1	0h RO/V	**Write to CF9 (CF9_ES):** This bit will be set when Host software writes a value of 6h or Eh to the CF9 register. Note: The shutdown special cycle from the CPU will also set this bit.
0	0h RO	Reserved.

13.3.76 LATENCY_LIMIT_RESIDENCY_0 (LAT_LIM_RES_0)—Offset 1930h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**LATENCY_LIMIT_RESIDENCY (LLR0):** This field contains the amount of time (in 120us granularity) for the corresponding 0/1/2 counter in the LATENCY_LIMIT_CONTROL register that the appropriate counter is limiting the memory LTR request to the CPU. Note that this counter can wrap and that should not be of any concern. This register will reset to 0 anytime the corresponding enable for the register transitions from a 0->1. Note that on a 1->0 transition, the counter should hold its previous value

13.3.77 LATENCY_LIMIT_RESIDENCY_1 (LAT_LIM_RES_1)—Offset 1934h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**LATENCY_LIMIT_RESIDENCY (LLR1):** This field contains the amount of time (in 120us granularity) for the corresponding 0/1/2 counter in the LATENCY_LIMIT_CONTROL register that the appropriate counter is limiting the memory LTR request to the CPU. Note that this counter can wrap and that should not be of any concern. This register will reset to 0 anytime the corresponding enable for the register transitions from a 0->1. Note that on a 1->0 transition, the counter should hold its previous value

13.3.78 LATENCY_LIMIT_RESIDENCY_2 (LAT_LIM_RES_2)—Offset 1938h

LATENCY_LIMIT_RESIDENCY_2

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**LATENCY_LIMIT_RESIDENCY (LLR2):** This field contains the amount of time (in 120us granularity) for the corresponding 0/1/2 counter in the LATENCY_LIMIT_CONTROL register that the appropriate counter is limiting the memory LTR request to the CPU. Note that this counter can wrap and that should not be of any concern. This register will reset to 0 anytime the corresponding enable for the register transitions from a 0->1. Note that on a 1->0 transition, the counter should hold its previous value

13.3.79 SLP S0 RESIDENCY (SLP_S0_RES)—Offset 193Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Residency In S0 (RESIDENCY_IN_S0):** This field contains the amount of time that the SLP_S0# has been asserted. Note that this counter can wrap. The timer counts with 122 us granularity.

13.3.80 Latency Limit Control (LLC)—Offset 1940h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22	0h RW	**CTR2_ENABLE (CTR2_ENABLE):** Control for counting only if EA=0 0 Count always (EA=0 or 1) 1 Count only if in a state where EA=0
21	0h RW	**CTR2_EA_CTL (CTR2_EA_CTL):** Control for counting only if EA=0 0 Count always (EA=0 or 1) 1 Count only if in a state where EA=0
20:16	0h RW	**CTR2_DEVICE (CTR2_DEVICE):** Encoding of the LTR device to be monitored 0 - PCIe SPA 1 - PCIe SPB 2 - PCIe SPC 3 - SATA 4 - GbE 5 - xHCI 6 - Intel CSME 7 - Reserved 8 - Intel HD Audio 9 - eSPI 10 - I2C, UART, GSPI 11 - PCIe SPD 12:13 - Reserved 14 - SDXC 15 - ISH 16 - CNVi 17 - eMMC
15	0h RO	Reserved.
14	0h RW	**CTR1_ENABLE (CTR1_ENABLE):** Control for counting only if EA=0 0 Count always (EA=0 or 1) 1 Count only if in a state where EA=0
13	0h RW	**CTR1_EA_CTL (CTR1_EA_CTL):** Control for counting only if EA=0 0 Count always (EA=0 or 1) 1 Count only if in a state where EA=0

Bit Range	Default & Access	Field Name (ID): Description
12:8	0h RW	**CTR1_DEVICE (CTR1_DEVICE):** Encoding of the LTR device to be monitored 0 - PCIe SPA 1 - PCIe SPB 2 - PCIe SPC 3 - SATA 4 - GbE 5 - xHCI 6 - Intel CSME 7 - Reserved 8 - Intel HD Audio 9 - eSPI 10 - I2C, UART, GSPI 11 - PCIe SPD 12:13 - Reserved 14 - SDXC 15 - ISH 16 - CNVi 17 - eMMC
7	0h RO	Reserved.
6	0h RW	**CTR0_ENABLE (CTR0_ENABLE):** Control for counting only if EA=0 0 Count always (EA=0 or 1) 1 Count only if in a state where EA=0
5	0h RW	**CTR0_EA_CTL (CTR0_EA_CTL):** Control for counting only if EA=0 0 Count always (EA=0 or 1) 1 Count only if in a state where EA=0
4:0	0h RW	**CTR0_DEVICE (CTR0_DEVICE):** Encoding of the LTR device to be monitored 0 - PCIe SPA 1 - PCIe SPB 2 - PCIe SPC 3 - SATA 4 - GbE 5 - xHCI 6 - Intel CSME 7 - Reserved 8 - Intel HD Audio 9 - eSPI 10 - I2C, UART, GSPI 11 - PCIe SPD 12:13 - Reserved 14 - SDXC 15 - ISH 16 - CNVi 17 - eMMC

13.3.81 Chipset Initialization Register B1C (CPPMVRIC)—Offset 1B1Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**CSME Power Gated Qualification Disable (MEPGQDIS):** 0 = SLP_S0# assertion requires CSME to be power gated 1 = SLP_S0# assertion does not require CSME to be power gated
30	0h RW	**GbE Disconnected Qualification Disable (GBEDISCQDIS):** 0 = SLP_S0# assertion requires GbE LAN to be disconnected 1 = SLP_S0# assertion does not require GbE LAN to be disconnected
29	0h RW	**Audio DSP is in D3 Qualification Disable (ADSPD3QDIS):** 0 = SLP_S0# assertion requires the Audio DSP controller to be in D3 1 = SLP_S0# assertion does not require the Audio DSP controller to be in D3
28	0h RW	**XHCI is in D3 Qualification Disable (XHCID3QDIS):** 0 = SLP_S0# assertion requires the XHCI controller to be in D3 1 = SLP_S0# assertion does not require the XHCI controller to be in D3
27	0h RW	**LPIO is in D3 Qualification Disable (LPIOD3QDIS):** 0 = SLP_S0# assertion requires LPIO controllers to be in D3 1 = SLP_S0# assertion does not require LPIO controllers to be in D3
26	0h RW	**Thermal Sensor Disable Qualification Disable (TSDQDIS):** 0 = SLP_S0# assertion requires the thermal sensor to be disabled 1 = SLP_S0# assertion does not require the thermal sensor to be disabled
25	0h RW	**ICC PLL Wake Block Enable (ICCPLLWBE):** 0 = PMC HW never blocks ICLK PLL from being re-enabled during a dynamic ICC PLL shutdown event. 1 = PMC HW blocks ICLK PLL from being re-enabled for any reason following a dynamic ICC PLL shutdown event while SLP_S0# assertion conditions are met and until VR idle mode exit timer expires after SLP_S0# de-assertion.
24	0h RO	Reserved.
23	0h RW	**Power Ungate Block Enable (PUGBEN):** 0 = PMC HW does not block Intel(R)CSME and HSIO Power from being restored upon being requested to do so while SLP_S0# assertion conditions are met and until VR idle mode exit timer expires after SLP_S0# de-assertion. 1 = PMC HW blocks Intel(R)CSME and HSIO Power from being restored upon being requested to do so while SLP_S0# assertion conditions are met and until VR idle mode exit timer expires after SLP_S0# de-assertion.
22	0h RW	**24MHz Crystal Shutdown Qualification Disable (XTALSDQDIS):** 0 = SLP_S0# assertion requires the 24MHz Crystal Oscillator to be shutdown. Once SLP_S0# is asserted, the Crystal oscillator should be kept off until PMC notifies it is allowed to be re-enabled. 1 = SLP_S0# assertion does not require the 24MHz Crystal to be shutdown.
21:16	0h RW	**SRC[5:0]CLKRQ# VR Idle Enable (CLKRQ_VRI_EN):** Each bit in this register deterimes whether the corresponding PCIe clock request pin (SRC[bit #]CLKRQ#) is enabled as a VR Idle break event / entry inhibitor. For example, if CLKRQ_VRI_EN[0] = '1' then SRC0CLKRQ# must be a '1' in order for SLP_S0# to be asserted and if SRC0CLKRQ# goes to '0' then it will cause SLP_S0# to be deasserted. On the other hand, if CLKRQ_VRI_EN[0] = '0' then the state of SRC0CLKRQ# has no impact on SLP_S0#.
15	0h RW/V	**Global SLP_S0# (VR Idle) Enable (GSLPS0EN):** 0 = CPPMVRIC-based SLP_S0# HW functionality is disabled (controlled by the LPM*_ACT_*.ASSERT_SLPS0 bits). 1 = CPPMVRIC-based SLP_S0# HW functionality is enabled (the LPM*_ACT_*.ASSERT_SLPS0 bits have no impact on the SLP_S0# pin). When GSLPS0EN = 0, SLP_S0# is always driven based on the 'Low power mode actions' registers, except if being overridden by PMC FW.
14	0h RO	Reserved.
13	0h RW	**SLP_S0# Low Voltage Mode Enable (SLPS0LVEN):** 0 = high speed ring oscillator (>24 MHz) clocks are allowed to run when SLP_S0#=0 1 = high speed ring oscillator (>24 MHz) clocks are not allowed to run when SLP_S0#=0. The PMC prevent ungating of these clock domains while SLP_S0#=0.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**Intel (R) Trace Hub AON Active Request Qualification Disable (NPKAONACTREQQDIS):** 0 = SLP_S0# assertion requires Intel(R) Trace Hub not to be requesting AON active 1 =SLP_S0# assertion does not require Intel(R) Trace Hub not to be requesting AON active.
11:9	0h RW	**SLP_S0# Minimum Assertion Width (SLP_S0_MIN_ASST_WDTH):** 000 = 30.5us 001 = 61us 010 = 91.5us 011 = 122us 100 = 152.5us 101 = 183us 110 = 500us 111 = 1ms
8:0	0h RW	**SLP_S0# De-assertion Exit Latency (SLP_S0_EXIT_LAT):** This value is used in the SLP_S0# exit timer and has an RTC clk period (30.5us) granularity. 000h = 0us (reserved) 001h = 30.5us 002h = 61us 003h = 91.5us 1FFh = 15.6ms

13.3.82 Chipset Initialization Register B24 (CIRB24)—Offset 1B24h

BIOS may program this register.

13.3.83 Chipset Initialization Register 340 (CIRB40)—Offset 1B40h

BIOS may program this register.

13.3.84 Chipset Initialization Register B44 (CIRB44)—Offset 1B44h

BIOS may program this register.

13.3.85 Chipset Initialization Register 34C (CIR34C)—Offset 1B4Ch

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 2000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**PCIe Root Ports Low Voltage Qualification Disable (PCIELVQDIS):** 0 = SLP_S0# assertion requires all PCIe ports and their controllers to allow for Low Voltage mode entry. 1 = SLP_S0# assertion does not require all PCIe ports and their controllers to allow for Low Voltage mode entry
30	0h RW	**SATA Controller in D3 Qualification Disable (SATAD3QDIS):** 0 = SLP_S0# assertion requires the SATA controller to be in D3 1 = SLP_S0# assertion does not require the SATA controller to be in D3
29	0h RW	**USB Device in D3 Qualification Disable (USBDEVD3QDIS):** 0 = SLP_S0# assertion requires the USB Device controller to be in D3 1 = SLP_S0# assertion does not require the USB Device controller to be in D3
28:26	0h RO	Reserved.
25	1h RW	**Connectivity Vnn Request Qualification Disable (CNVIVNNREQQDIS):** 0 = SLP_S0# assertion requires CNVi not to be requesting Vnn active 1 = SLP_S0# assertion does not require CNVi not to be requesting Vnn active
24	0h RW	**LPC Clk Request Qualification Disable (LPCCLKREQQDIS):** 0 = SLP_S0# assertion requires the CLKOUT_LPC output clocks to be gated and CLKRUN# is low 1 = SLP_S0# assertion does not require the CLKOUT_LPC output clocks to be gated
23	0h RW	**HPET 24MHz Clk Request Qualification Disable (HPET24CLKREQQDIS):** 0 = SLP_S0# assertion requires the HPET 24MHz clkreq to be low 1 = SLP_S0# assertion does not require the HPET 24MHz clkreq to be low
22	0h RW	**Audio DSP ROSC Off Qualification Disable (ADSPROSCOFFQDIS):** 0 = SLP_S0# assertion requires the Audio DSP ROSC to be off 1 = SLP_S0# assertion does not require the Audio DSP ROSC to be off
21	0h RW	**HSIO Core Power Gated Qualification Disable (HSIOCPGQDIS):** 0 = SLP_S0# assertion requires all lanes of the HSIO Core Power Domain to be gated. 1 = SLP_S0# assertion does not require all lanes of the HSIO Core Power Domain to be gated.
20	0h RW	**USB2 PLL is off Qualification Disable (USB2PLLSDQDIS):** 0 = SLP_S0# assertion requires the USB2 PLL to be shut down. 1 = SLP_S0# assertion does not require the USB2 PLL to be shut down.
19	0h RW	**Audio PLL is off Qualification Disable (APLLSDQDIS):** 0 = SLP_S0# assertion requires the Audio PLL to be shut down. 1 = SLP_S0# assertion does not require the Audio PLL to be shut down.
18	0h RW	**IsCLK PLL Shutdown Qualification Disable (ICCPLLSDQDIS):** 0 = SLP_S0# assertion requires the IsCLK PLL to be shut down. 1 = SLP_S0# assertion does not require the IsCLK PLL to be shut down.
17	0h RW	**CPU in C10 Qualification Disable (CPUC10QDIS):** 0 = SLP_S0# assertion requires the CPU to be in a C10 state. 1 = SLP_S0# assertion does not require the CPU to be in a C10 state.
16:0	0h RO	Reserved.

13.3.86 CWB MDID Status Register (CWBMDIDSTATUS)—Offset 1BD4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**CWB Status (CWB_STS):** When set , DMI Central Write Buffer is enabled. 1: CWB on 0: CWB off
30:18	0h RO	Reserved.
17:9	0h RW/V	**DMI MDID Value (DMI_MDID):** DMI sent MDID value.
8:0	0h RW/V	**CNVi MDID Value (CNVI_MDID):** CNVi sent MDID value. Note: this is used for CNVi WIFI

13.3.87 ACPI Control (ACTL)—Offset 1BD8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RW	**ACPI Enable (EN):** When set, decode of the I/O range pointed to by the ACPI base register is enabled and the ACPI power management function is enabled.
6:3	0h RO	Reserved.
2:0	0h RW	**SCI IRQ Select (SCIS):** Specifies on which IRQ the SCI will internally appear. If not using the APIC, the SCI must be routed to IRQ[9-11], and that interrupt is not sharable with the SERIRQ stream, but is shareable with other PCI interrupts. If using the APIC, the SCI can also be mapped to IRQ20-23, and can be shared with other interrupts. Bits - SCI Map ---- - ------- 000 - IRQ9 001 - IRQ10 010 - IRQ11 011 - Reserved 100 - IRQ20 (only if APIC is enabled) 101 - IRQ21 (only if APIC is enabled) 110 - IRQ22 (only if APIC is enabled) 111 - IRQ23 (only if APIC is enabled) When the interrupt is mapped to APIC interrupts 9, 10 or 11, the APIC should be programmed for active-high reception. When the interrupt is mapped to APIC interrupts 20 through 23, the APIC should be programmed for active-low reception.

13.3.88 Low Power Mode Status Latch Enable (LPM_STS_LATCH_EN)—Offset 1C34h

Control whether the low power mode requirements are latched when attempting to enter and when exiting the given state.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RW	**S0i3.4 Status Latch Enable (LPM7_STS_LATCH_EN):** Latch the low power mode requirements when attempting to enter this low power state and when exiting.
6	0h RW	**S0i3.3 Status Latch Enable (LPM6_STS_LATCH_EN):** Latch the low power mode requirements when attempting to enter this low power state and when exiting.
5	0h RW	**S0i3.2 Status Latch Enable (LPM5_STS_LATCH_EN):** Latch the low power mode requirements when attempting to enter this low power state and when exiting.
4	0h RW	**S0i3.1 Status Latch Enable (LPM4_STS_LATCH_EN):** Latch the low power mode requirements when attempting to enter this low power state and when exiting.
3	0h RW	**S0i3.0 Status Latch Enable (LPM3_STS_LATCH_EN):** Latch the low power mode requirements when attempting to enter this low power state and when exiting.
2	0h RW	**S0i2.2 Status Latch Enable (LPM2_STS_LATCH_EN):** Latch the low power mode requirements when attempting to enter this low power state and when exiting.
1	0h RW	**S0i2.1 Status Latch Enable (LPM1_STS_LATCH_EN):** Latch the low power mode requirements when attempting to enter this low power state and when exiting.
0	0h RW	**S0i2.0 Status Latch Enable (LPM0_STS_LATCH_EN):** Latch the low power mode requirements when attempting to enter this low power state and when exiting.

13.3.89 Low Power Mode Status Reg 0 (LPM_STS_0)—Offset 1C3Ch

Status of the low power mode requirements. The registers are latched on every C10 entry or exit (configurable) and on every s0ix.x entry/exit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**XTAL_USB2PLL Off Status (CS31_OFF_STS):** Reflects the value of the associated clock source. A value of 1 means that the clock source is OFF.
30	0h RO	Reserved.
29	0h RO/V	**SATA PLL Off Status (CS29_OFF_STS):** Reflects the value of the associated clock source. A value of 1 means that the clock source is OFF.

Bit Range	Default & Access	Field Name (ID): Description
28	0h RO	Reserved.
27	0h RO/V	**Main Calibrated Ring Oscillator Off Status (CS27_OFF_STS):** Reflects the value of the associated clock source. A value of 1 means that the clock source is OFF.
26	0h RO/V	**Audio Calibrated Ring Oscillator Off Status (CS26_OFF_STS):** Reflects the value of the associated clock source. A value of 1 means that the clock source is OFF.
25	0h RO/V	**Fast Crystal Oscillator (excludes USB_XTAL clkreq, XTAL_USB2PLL, Clock partition 6) Off Status (CS25_OFF_STS):** Reflects the value of the associated clock source. A value of 1 means that the clock source is OFF.
24	0h RO/V	**MIPI PLL Off Status (CS24_OFF_STS):** Reflects the value of the associated clock source. A value of 1 means that the clock source is OFF.
23	0h RO/V	**Audio PLL Off Status (CS23_OFF_STS):** Reflects the value of the associated clock source. A value of 1 means that the clock source is OFF.
22	0h RO/V	**Over Clocking PLL Off Status (CS22_OFF_STS):** Reflects the value of the associated clock source. A value of 1 means that the clock source is OFF.
21	0h RO/V	**OPIO PLL Off Status (CS21_OFF_STS):** Reflects the value of the associated clock source. A value of 1 means that the clock source is OFF.
20	0h RO/V	**PCIe Gen3 PLL Off Status (CS20_OFF_STS):** Reflects the value of the associated clock source. A value of 1 means that the clock source is OFF.
19	0h RO/V	**PCIe/USB3.1 Gen2 PLL Off Status (CS19_OFF_STS):** Reflects the value of the associated clock source. A value of 1 means that the clock source is OFF.
18	0h RO/V	**USB2 PLL Off Status (CS18_OFF_STS):** Reflects the value of the associated clock source. A value of 1 means that the clock source is OFF.
17:0	0h RO	Reserved.

13.3.90 Low Power Mode Status Reg 1 (LPM_STS_1)—Offset 1C40h

Status of the low power mode requirements. The registers are latched on every C10 entry or exit (configurable) and on every s0ix.x entry/exit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**CSME_SPL Power Gate Status (AGENT31_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
30	0h RO/V	**CLINK_V1P05 Power Gate Status (AGENT30_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
29	0h RO/V	**Audio Power Gate Status (AGENT29_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.

Bit Range	Default & Access	Field Name (ID): Description
28	0h RO/V	**CSME_KVM Power Gate Status (AGENT28_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
27	0h RO/V	**ISH Power Gate Status (AGENT27_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
26	0h RO/V	**PSF6 Power Gate Status (AGENT26_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
25	0h RO/V	**FIA Power Gate Status (AGENT25_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
24	0h RO/V	**MMP_UFSX2B Power Gate Status (AGENT24_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
23	0h RO/V	**MMP_UFSX2 Power Gate Status (AGENT23_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
22	0h RO/V	**Intel Serial IO Power Gate Status (AGENT22_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
21	0h RO/V	**GBE Power Gate Status (AGENT21_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
20	0h RO	Reserved.
19	0h RO/V	**TH1 Power Gate Status (AGENT19_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
18	0h RO/V	**TH0 Power Gate Status (AGENT18_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
17	0h RO/V	**OPDMI Power Gate Status (AGENT17_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
16	0h RO/V	**SBR Power Gate Status (AGENT16_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
15	0h RO/V	**PSF Power Gate Status (AGENT15_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
14	0h RO/V	**P2SB Power Gate Status (AGENT14_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
13	0h RO/V	**LSX Power Gate Status (AGENT13_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
12	0h RO	Reserved.
11	0h RO/V	**PCIe Controller F Power Gate Status (AGENT11_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
10	0h RO/V	**PCIe Controller E Power Gate Status (AGENT10_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
9	0h RO/V	**PCIe Controller D Power Gate Status (AGENT9_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
8	0h RO/V	**PCIe Controller C Power Gate Status (AGENT8_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
7	0h RO/V	**PCIe Controller B Power Gate Status (AGENT7_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
6	0h RO/V	**PCIe Controller A Power Gate Status (AGENT6_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
5	0h RO/V	**OTG Controller B Power Gate Status (AGENT5_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	Reserved.
3	0h RO/V	**UFSX2 Power Gating Status (AGENT3_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
2	0h RO/V	**xHCI Power Gate Status (AGENT2_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
1	0h RO/V	**SATA Power Gate Status (AGENT1_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
0	0h RO/V	**CSME Power Gate Status (AGENT0_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.

13.3.91 Low Power Mode Status Reg 2 (LPM_STS_2)—Offset 1C44h

Status of the low power mode requirements. The registers are latched on every C10 entry or exit (configurable) and on every s0ix.x entry/exit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	0h RO/V	**GBE TSN D3 Status (IP12_D3_STS):** Reflects the value of the associated D3 status. A value of 1 means that the IP is in D3.
11	0h RO/V	**GBE D3 Status (IP11_D3_STS):** Reflects the value of the associated D3 status. A value of 1 means that the IP is in D3.
10	0h RO/V	**THC1 D3 Status (IP10_D3_STS):** Reflects the value of the associated D3 status. A value of 1 means that the IP is in D3.
9	0h RO/V	**THC0 D3 Status (IP9_D3_STS):** Reflects the value of the associated D3 status. A value of 1 means that the IP is in D3.
8	0h RO/V	**Intel(R) Serial IO D3 Status (IP8_D3_STS):** Reflects the value of the associated D3 status. A value of 1 means that the IP is in D3.
7	0h RO/V	**EMMC D3 Status (IP7_D3_STS):** Reflects the value of the associated D3 status. A value of 1 means that the IP is in D3.
6	0h RO/V	**SDX D3 Status (IP6_D3_STS):** Reflects the value of the associated D3 status. A value of 1 means that the IP is in D3.
5	0h RO/V	**xDCI D3 Status (IP5_D3_STS):** Reflects the value of the associated D3 status. A value of 1 means that the IP is in D3.
4:3	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO/V	**xHCI D3 Status (IP2_D3_STS):** Reflects the value of the associated D3 status. A value of 1 means that the IP is in D3.
1	0h RO/V	**SATA D3 Status (IP1_D3_STS):** Reflects the value of the associated D3 status. A value of 1 means that the IP is in D3.
0	0h RO/V	**ADSP D3 Status (IP0_D3_STS):** Reflects the value of the associated D3 status. A value of 1 means that the IP is in D3.

13.3.92 Low Power Mode Status Reg 3 (LPM_STS_3)—Offset 1C48h

Status of the low power mode requirements. The registers are latched on every C10 entry or exit (configurable) and on every s0ix.x entry/exit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	Reserved.
25	0h RO/V	**GBE Request Status (IP25_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
24	0h RO/V	**CSME Request Status (IP24_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
23	0h RO	Reserved.
22	0h RO/V	**Intel Trace Hub Request Status (IP22_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
21	0h RO/V	**DCI Request Status (IP21_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
20	0h RO/V	**Controller Link Request Status (IP20_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
19:18	0h RO	Reserved.
17	0h RO/V	**SMLINK1 Request Status (IP17_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
16	0h RO/V	**SMLINK0 Request Status (IP16_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high
15	0h RO/V	**CSME Request Status (IP15_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
14	0h RO/V	**SMBUS Request Status (IP14_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	Reserved.
12	0h RO/V	**DTS Request Status (IP12_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
11	0h RO/V	**Display Request Status (IP11_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
10	0h RO/V	**eSPI Request Status (IP10_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
9	0h RO/V	**CNVI Request Status (IP9_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
8	0h RO/V	**ISH Request Status (IP8_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
7	0h RO/V	**Audio Request Status (IP7_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
6	0h RO/V	**GPIO_COM5 Request Status (IP6_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
5	0h RO/V	**GPIO_COM4 Request Status (IP5_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
4	0h RO/V	**GPIO_COM3 Request Status (IP4_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
3	0h RO/V	**GPIO_COM2 Request Status (IP3_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
2	0h RO/V	**GPIO_COM1 Request Status (IP2_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
1	0h RO/V	**GPIO_COM0 Request Status (IP1_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
0	0h RO	Reserved.

13.3.93 Low Power Mode Status Reg 4 (LPM_STS_4)—Offset 1C4Ch

Status of the low power mode requirements. The registers are latched on every C10 entry or exit (configurable) and on every s0ix.x entry/exit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RO/V	**xDCI attached Requirement Status (MISC_REQ_STS_24):** Reflects the value of the associated MISC request status. A value of 1 means that the IP MISC request is high.
23	0h RO	Reserved.
22	0h RO/V	**MPHY SUS Requirement Status (MISC_REQ_STS_22):** Reflects the value of the associated MISC request status. A value of 1 means that the IP MISC request is high.
21:19	0h RO	Reserved.
18	0h RO/V	**Auto-demotion enable status (MISC_REQ_STS_18):** Reflects the value of the associated MISC request status. A value of 1 means that the IP MISC request is high.
17	0h RO/V	**Break-even enable status (MISC_REQ_STS_17):** Reflects the value of the associated MISC request status. A value of 1 means that the IP MISC request is high.
16	0h RO/V	**MPHY Core Data Lanes Requirement Status (MISC_REQ_STS_16):** Reflects the value of the associated MISC request status. A value of 1 means that the IP MISC request is high.
15:13	0h RO	Reserved.
12	0h RO/V	**PCIe Clock Request Deasserted Status (MISC_REQ_STS_12):** Reflects the value of the associated MISC request status. A value of 1 means that the IP MISC request is high.
11	0h RO	Reserved.
10	0h RO/V	**USB2_SUS Power Gating System Requirement Status (MISC_REQ_STS_10):** Reflects the value of the associated MISC request status. A value of 1 means that the IP MISC request is high.
9:8	0h RO	Reserved.
7	0h RO/V	**ISH Requirement Status (MISC_REQ_STS_7):** Reflects the value of the associated MISC request status. A value of 1 means that the IP MISC request is high.
6	0h RO/V	**CNVI Requirement Status (MISC_REQ_STS_6):** Reflects the value of the associated MISC request status. A value of 1 means that the IP MISC request is high.
5	0h RO/V	**Intel Trace Hub Requirement Status (MISC_REQ_STS_5):** Reflects the value of the associated MISC request status. A value of 1 means that the IP MISC request is high.
4	0h RO	Reserved.
3	0h RO/V	**PCIe LPM Enable Requirement Status (MISC_REQ_STS_3):** Reflects the value of the associated MISC request status. A value of 1 means that the IP MISC request is high.
2:1	0h RO	Reserved.
0	0h RO/V	**CPU_C10 Requirement Status (MISC_REQ_STS_0):** Reflects the value of the associated MISC request status. A value of 1 means that the IP MISC request is high.

13.3.94 Low Power Mode Status Reg 5 (LPM_STS_5)—Offset 1C50h

Status of the low power mode requirements. The registers are latched on every C10 entry or exit (configurable) and on every s0ix.x entry/exit.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Interrupt and Timer Subsystem Wake 5 Polarity (SIG15_LIVE_STS):** Reflects the wake of the associated signal requirement status.
30	0h RO/V	**Interrupt and Timer Subsystem Wake 5 Enable (SIG15_WAKE_STS):** Reflects the wake of the associated signal requirement status.
29	0h RO/V	**Interrupt and Timer Subsystem Wake 4 Polarity (SIG14_LIVE_STS):** Reflects the wake of the associated signal requirement status.
28	0h RO/V	**Interrupt and Timer Subsystem Wake 4 Enable (SIG14_WAKE_STS):** Reflects the wake of the associated signal requirement status.
27	0h RO/V	**Interrupt and Timer Subsystem Wake 3 Polarity (SIG13_LIVE_STS):** Reflects the wake of the associated signal requirement status.
26	0h RO/V	**Interrupt and Timer Subsystem Wake 3 Enable (SIG13_WAKE_STS):** Reflects the wake of the associated signal requirement status.
25	0h RO/V	**Interrupt and Timer Subsystem Wake 2 Polarity (SIG12_LIVE_STS):** Reflects the wake of the associated signal requirement status.
24	0h RO/V	**Interrupt and Timer Subsystem Wake 2 Enable (SIG12_WAKE_STS):** Reflects the wake of the associated signal requirement status.
23	0h RO/V	**Interrupt and Timer Subsystem Wake 1 Polarity (SIG11_LIVE_STS):** Reflects the wake of the associated signal requirement status.
22	0h RO/V	**Interrupt and Timer Subsystem Wake 1 Enable (SIG11_WAKE_STS):** Reflects the wake of the associated signal requirement status.
21	0h RO/V	**Interrupt and Timer Subsystem Wake 0 Polarity (SIG10_LIVE_STS):** Reflects the wake of the associated signal requirement status.
20	0h RO/V	**Interrupt and Timer Subsystem Wake 0 Enable (SIG10_WAKE_STS):** Reflects the wake of the associated signal requirement status.
19	0h RO/V	**Intel(R) Serial IO 1 Wake Polarity (SIG9_LIVE_STS):** Reflects the wake of the associated signal requirement status.
18	0h RO/V	**Intel(R) Serial IO 1 Wake Enable (SIG9_WAKE_STS):** Reflects the wake of the associated signal requirement status.
17	0h RO/V	**Intel(R) Serial IO 0 Wake Polarity (SIG8_LIVE_STS):** Reflects the wake of the associated signal requirement status.
16	0h RO/V	**Intel(R) Serial IO 0 Wake Enable (SIG8_WAKE_STS):** Reflects the wake of the associated signal requirement status.
15	0h RO/V	**LSX Wake 7 Polarity (SIG7_LIVE_STS):** Reflects the wake of the associated signal requirement status.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO/V	**LSX Wake 7 Enable (SIG7_WAKE_STS):** Reflects the wake of the associated signal requirement status.
13	0h RO/V	**LSX Wake 6 Polarity (SIG6_LIVE_STS):** Reflects the wake of the associated signal requirement status.
12	0h RO/V	**LSX Wake 6 Enable (SIG6_WAKE_STS):** Reflects the wake of the associated signal requirement status.
11	0h RO/V	**LSX Wake 5 Polarity (SIG5_LIVE_STS):** Reflects the wake of the associated signal requirement status.
10	0h RO/V	**LSX Wake 5 Enable (SIG5_WAKE_STS):** Reflects the wake of the associated signal requirement status.
9	0h RO/V	**LSX Wake 4 Polarity (SIG4_LIVE_STS):** Reflects the wake of the associated signal requirement status.
8	0h RO/V	**LSX Wake 4 Enable (SIG4_WAKE_STS):** Reflects the wake of the associated signal requirement status.
7	0h RO/V	**LSX Wake 3 Polarity (SIG3_LIVE_STS):** Reflects the wake of the associated signal requirement status.
6	0h RO/V	**LSX Wake 3 Enable (SIG3_WAKE_STS):** Reflects the wake of the associated signal requirement status.
5	0h RO/V	**LSX Wake 2 Polarity (SIG2_LIVE_STS):** Reflects the wake of the associated signal requirement status.
4	0h RO/V	**LSX Wake 2 Enable (SIG2_WAKE_STS):** Reflects the wake of the associated signal requirement status.
3	0h RO/V	**LSX Wake 1 Polarity (SIG1_LIVE_STS):** Reflects the wake of the associated signal requirement status.
2	0h RO/V	**LSX Wake 1 Enable (SIG1_WAKE_STS):** Reflects the wake of the associated signal requirement status.
1	0h RO/V	**LSX Wake 0 Polarity (SIG0_LIVE_STS):** Reflects the wake of the associated signal requirement status.
0	0h RO/V	**LSX Wake 0 Enable (SIG0_WAKE_STS):** Reflects the wake of the associated signal requirement status.

13.3.95 Live Status of the Low Power Mode Status Reg 0 (LPM_LIVE_STS_0)—Offset 1C5Ch

Live status of the low power mode requirements. The registers are latched on every C10 entry or exit (configurable) and on every s0ix.x entry/exit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**XTAL_USB2 PLL Off Status (CS31_OFF_STS):** Reflects the value of the associated clock source. A value of 1 means that the clock source is OFF.
30	0h RO	Reserved.
29	0h RO/V	**SATA PLL Off Status (CS29_OFF_STS):** Reflects the value of the associated clock source. A value of 1 means that the clock source is OFF.
28	0h RO	Reserved.
27	0h RO/V	**Main Calibrated Ring Oscillator Off Status (CS27_OFF_STS):** Reflects the value of the associated clock source. A value of 1 means that the clock source is OFF.
26	0h RO/V	**Audio Calibrated Ring Oscillator Off Status (CS26_OFF_STS):** Reflects the value of the associated clock source. A value of 1 means that the clock source is OFF.
25	0h RO/V	**Fast Crystal Oscillator (Excludes USB_XTAL clkreq, XTAL_USB2PLL, Clock source 6 XTAL) Off Status (CS25_OFF_STS):** Reflects the value of the associated clock source. A value of 1 means that the clock source is OFF.
24	0h RO/V	**MIPI PLL Off Status (CS24_OFF_STS):** Reflects the value of the associated clock source. A value of 1 means that the clock source is OFF.
23	0h RO/V	**Audio PLL Off Status (CS23_OFF_STS):** Reflects the value of the associated clock source. A value of 1 means that the clock source is OFF.
22	0h RO/V	**Over Clocking Off Status (CS22_OFF_STS):** Reflects the value of the associated clock source. A value of 1 means that the clock source is OFF.
21	0h RO/V	**OPIO PLL Off Status (CS21_OFF_STS):** Reflects the value of the associated clock source. A value of 1 means that the clock source is OFF.
20	0h RO/V	**PCIe PLL Gen 3 Off Status (CS20_OFF_STS):** Reflects the value of the associated clock source. A value of 1 means that the clock source is OFF.
19	0h RO/V	**PCIe/USB3.1 Gen 2 PLL Off Status (CS19_OFF_STS):** Reflects the value of the associated clock source. A value of 1 means that the clock source is OFF.
18	0h RO/V	**USB2 PLL Off Status (CS18_OFF_STS):** Reflects the value of the associated clock source. A value of 1 means that the clock source is OFF.
17:0	0h RO	Reserved.

13.3.96 Live Status of the Low Power Mode Status Reg 1 (LPM_LIVE_STS_1)—Offset 1C60h

Live status of the low power mode requirements. The registers are latched on every C10 entry or exit (configurable) and on every s0ix.x entry/exit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**CSME Power Gate Status (AGENT31_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
30	0h RO/V	**CSME_CLINK Power Gate Status (AGENT30_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
29	0h RO/V	**CSME Power Gate Status (AGENT29_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
28	0h RO/V	**CSME_KVM Power Gate Status (AGENT28_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
27	0h RO/V	**CSME Power Gate Status (AGENT27_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
26	0h RO/V	**DCI Power Gate Status (AGENT26_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
25	0h RO/V	**xDCI Power Gate Status (AGENT25_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
24:21	0h RO	Reserved.
20	0h RO/V	**SDX Power Gate Status (AGENT20_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
19	0h RO/V	**Intel(R) Trace Hub Power Gate Status (AGENT19_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
18	0h RO	Reserved.
17	0h RO/V	**ISH Power Gate Status (AGENT17_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
16	0h RO/V	**SMB Power Gate Status (AGENT16_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
15	0h RO	Reserved.
14	0h RO/V	**Intel (R) Serial IO Power Gate Status (AGENT14_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
13	0h RO/V	**PCIe Controller D Power Gate Status (AGENT13_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
12	0h RO/V	**HDA Power Gate Status (AGENT12_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
11	0h RO/V	**HDA Power Gate Status (AGENT11_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
10	0h RO/V	**HDA Power Gate Status (AGENT10_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
9	0h RO/V	**HDA Power Gate Status (AGENT9_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
8	0h RO/V	**SATA Power Gate Status (AGENT8_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
7	0h RO/V	**GBE Power Gate Status (AGENT7_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
6	0h RO/V	**PCIe Controller C Power Gate Status (AGENT6_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO/V	**PCIe Controller B Power Gate Status (AGENT5_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
4	0h RO/V	**PCIe Controller A Power Gate Status (AGENT4_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
3	0h RO/V	**xHCI Power Gate Status (AGENT3_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
2	0h RO/V	**SPI Power Gate Status (AGENT2_PG_STS):** Reflects the value of the associated agent pg. A value of 1 means that the agent is power gated.
1:0	0h RO	Reserved.

13.3.97 Live Status of the Low Power Mode Status Reg 2 (LPM_LIVE_STS_2)—Offset 1C64h

Live status of the low power mode requirements. The registers are latched on every C10 entry or exit (configurable) and on every s0ix.x entry/exit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	0h RO/V	**GBE D3 Status (IP12_D3_STS):** Reflects the value of the associated D3 status. A value of 1 means that the IP is in D3.
11	0h RO/V	**GBE D3 Status (IP11_D3_STS):** Reflects the value of the associated D3 status. A value of 1 means that the IP is in D3.
10	0h RO/V	**THC1 D3 Status (IP10_D3_STS):** Reflects the value of the associated D3 status. A value of 1 means that the IP is in D3.
9	0h RO/V	**THC0 D3 Status (IP9_D3_STS):** Reflects the value of the associated D3 status. A value of 1 means that the IP is in D3.
8	0h RO/V	**Intel (R) Serial IO D3 Status (IP8_D3_STS):** Reflects the value of the associated D3 status. A value of 1 means that the IP is in D3.
7	0h RO/V	**eMMC D3 Status (IP7_D3_STS):** Reflects the value of the associated D3 status. A value of 1 means that the IP is in D3.
6	0h RO/V	**SDX D3 Status (IP6_D3_STS):** Reflects the value of the associated D3 status. A value of 1 means that the IP is in D3.
5	0h RO/V	**xDCI D3 Status (IP5_D3_STS):** Reflects the value of the associated D3 status. A value of 1 means that the IP is in D3.
4:3	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO/V	**xHCI D3 Status (IP2_D3_STS):** Reflects the value of the associated D3 status. A value of 1 means that the IP is in D3.
1	0h RO/V	**SATA D3 Status (IP1_D3_STS):** Reflects the value of the associated D3 status. A value of 1 means that the IP is in D3.
0	0h RO/V	**ADSP D3 Status (IP0_D3_STS):** Reflects the value of the associated D3 status. A value of 1 means that the IP is in D3.

13.3.98 Live Status of the Low Power Mode Status Reg 3 (LPM_LIVE_STS_3)—Offset 1C68h

Live status of the low power mode requirements. The registers are latched on every C10 entry or exit (configurable) and on every s0ix.x entry/exit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	Reserved.
25	0h RO/V	**GBE Request Status (IP25_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
24	0h RO/V	**CSME Request Status (IP24_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
23	0h RO	Reserved.
22	0h RO/V	**Intel(R) Trace Hub Request Status (IP22_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
21	0h RO/V	**DCI Request Status (IP21_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
20	0h RO/V	**Controller Link Request Status (IP20_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
19:18	0h RO	Reserved.
17	0h RO/V	**SMLINK 1 Request Status (IP17_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
16	0h RO/V	**SMLINK 0 Request Status (IP16_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
15	0h RO/V	**CSME Request Status (IP15_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
14	0h RO/V	**SMBUS Request Status (IP14_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	Reserved.
12	0h RO/V	**DTS Request Status (IP12_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
11	0h RO/V	**Display Request Status (IP11_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
10	0h RO/V	**eSPI Request Status (IP10_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
9	0h RO/V	**CNVI Request Status (IP9_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
8	0h RO/V	**ISH Request Status (IP8_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
7	0h RO/V	**Audio Request Status (IP7_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
6	0h RO/V	**GPIO_COM5 Request Status (IP6_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
5	0h RO/V	**GPIO_COM4 Request Status (IP5_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
4	0h RO/V	**GPIO_COM3 Request Status (IP4_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
3	0h RO/V	**GPIO_COM2 Request Status (IP3_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
2	0h RO/V	**GPIO_COM1 Request Status (IP2_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
1	0h RO/V	**GPIO_COM0 Request Status (IP1_VNN_REQ_STS):** Reflects the value of the associated IP VNN request. A value of 1 means that the IP VNN request is high.
0	0h RO	Reserved.

13.3.99 Live Status of the Low Power Mode Status Reg 4 (LPM_LIVE_STS_4)—Offset 1C6Ch

Live status of the low power mode requirements. The registers are latched on every C10 entry or exit (configurable) and on every s0ix.x entry/exit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RO/V	**xDCI attached Requirement Status (MISC_REQ_STS_24):** Reflects the value of the associated MISC request status. A value of 1 means that the IP MISC request is high.
23	0h RO	Reserved.
22	0h RO/V	**MPHY SUS Requirement Status (MISC_REQ_STS_22):** Reflects the value of the associated MISC request status. A value of 1 means that the IP MISC request is high.
21:18	0h RO	Reserved.
17	0h RO/V	**Break-even enable status (MISC_REQ_STS_17):** Reflects the value of the associated MISC request status. A value of 1 means that the IP MISC request is high.
16	0h RO/V	**MPHY Core Data Lanes Off Requirement Status (MISC_REQ_STS_16):** Reflects the value of the associated MISC request status. A value of 1 means that the IP MISC request is high.
15:13	0h RO	Reserved.
12	0h RO/V	**PCIe Clock Request Deasserted Status (MISC_REQ_STS_12):** Reflects the value of the associated MISC request status. A value of 1 means that the IP MISC request is high.
11	0h RO	Reserved.
10	0h RO/V	**USB2_SUS Power Gating System Requirement Status (MISC_REQ_STS_10):** Reflects the value of the associated MISC request status. A value of 1 means that the IP MISC request is high.
9:8	0h RO	Reserved.
7	0h RO/V	**ISH Requirement Status (MISC_REQ_STS_7):** Reflects the value of the associated MISC request status. A value of 1 means that the IP MISC request is high.
6	0h RO/V	**CNVI Requirement Status (MISC_REQ_STS_6):** Reflects the value of the associated MISC request status. A value of 1 means that the IP MISC request is high.
5	0h RO/V	**Intel Trace Hub Requirement Status (MISC_REQ_STS_5):** Reflects the value of the associated MISC request status. A value of 1 means that the IP MISC request is high.
4	0h RO	Reserved.
3	0h RO/V	**PCIe LPM Enable Requirement Status (MISC_REQ_STS_3):** Reflects the value of the associated MISC request status. A value of 1 means that the IP MISC request is high.
2:1	0h RO	Reserved.
0	0h RO/V	**CPU_C10 Requirement Status (MISC_REQ_STS_0):** Reflects the value of the associated MISC request status. A value of 1 means that the IP MISC request is high.

13.3.100 Live Status of the Low Power Mode Status Reg 5 (LPM_LIVE_STS_5)—Offset 1C70h

Live status of the low power mode requirements. The registers are latched on every C10 entry or exit (configurable) and on every s0ix.x entry/exit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Interrupt and Timer Subsystem 5 Wake Polarity (SIG15_LIVE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
30	0h RO/V	**Interrupt and Timer Subsystem 5 Wake Enable (SIG15_WAKE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
29	0h RO/V	**Interrupt and Timer Subsystem 4 Wake Polarity (SIG14_LIVE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
28	0h RO/V	**Interrupt and Timer Subsystem 4 Wake Enable (SIG14_WAKE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
27	0h RO/V	**Interrupt and Timer Subsystem 3 Wake Polarity (SIG13_LIVE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
26	0h RO/V	**Interrupt and Timer Subsystem 3 Wake Enable (SIG13_WAKE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
25	0h RO/V	**Interrupt and Timer Subsystem 2 Wake Polarity (SIG12_LIVE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
24	0h RO/V	**Interrupt and Timer Subsystem 2 Wake Enable (SIG12_WAKE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
23	0h RO/V	**Interrupt and Timer Subsystem 1 Wake Polarity (SIG11_LIVE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
22	0h RO/V	**Interrupt and Timer Subsystem 1 Wake Enable (SIG11_WAKE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
21	0h RO/V	**Interrupt and Timer Subsystem 0 Wake Polarity (SIG10_LIVE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
20	0h RO/V	**Interrupt and Timer Subsystem 0 Wake Enable (SIG10_WAKE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
19	0h RO/V	**Intel (R) Serial IO 1 Wake Polarity (SIG9_LIVE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
18	0h RO/V	**Intel (R) Serial IO 1 Wake Enable (SIG9_WAKE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
17	0h RO/V	**Intel (R) Serial IO 0 Wake Polarity (SIG8_LIVE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
16	0h RO/V	**Intel (R) Serial IO 0 Wake Enable (SIG8_WAKE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO/V	**LSX Wake 7 Polarity (SIG7_LIVE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
14	0h RO/V	**LSX Wake 7 Enable (SIG7_WAKE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
13	0h RO/V	**SIG6 Live Status (SIG6_LIVE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
12	0h RO/V	**LSX Wake 6 Enable (SIG6_WAKE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
11	0h RO/V	**LSX Wake 5 Polarity (SIG5_LIVE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
10	0h RO/V	**LSX Wake 5 Enable (SIG5_WAKE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
9	0h RO/V	**LSX Wake 4 Polarity (SIG4_LIVE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
8	0h RO/V	**LSX Wake 4 Enable (SIG4_WAKE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
7	0h RO/V	**LSX Wake 3 Polarity (SIG3_LIVE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
6	0h RO/V	**LSX Wake 3 Enable (SIG3_WAKE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
5	0h RO/V	**LSX Wake 2 Polarity (SIG2_LIVE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
4	0h RO/V	**LSX Wake 2 Enable (SIG2_WAKE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
3	0h RO/V	**LSX Wake 1 Polarity (SIG1_LIVE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
2	0h RO/V	**LSX Wake 1 Enable (SIG1_WAKE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
1	0h RO/V	**LSX Wake 0 Polarity (SIG0_LIVE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.
0	0h RO/V	**LSX Wake 0 Enable (SIG0_WAKE_STS):** Reflects the value of the associated signal requirement status. A value of 1 means that the IP signal requirement is high.

13.3.101 Low Power Mode Enable (LPM_EN)—Offset 1C78h

Enable for each low power mode.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RW	**S0i3.4 Enable (LPM7_EN):** If this bit is 1, the associated low power mode is enabled.
6	0h RW	**S0i3.3 Enable (LPM6_EN):** If this bit is 1, the associated low power mode is enabled.
5	0h RW	**S0i3.2 Enable (LPM5_EN):** If this bit is 1, the associated low power mode is enabled.
4	0h RW	**S0i3.1 Enable (LPM4_EN):** If this bit is 1, the associated low power mode is enabled.
3	0h RW	**S0i3.0 Enable (LPM3_EN):** If this bit is 1, the associated low power mode is enabled.
2	0h RW	**S0i2.2 Enable (LPM2_EN):** If this bit is 1, the associated low power mode is enabled.
1	0h RW	**S0i2.1 Enable (LPM1_EN):** If this bit is 1, the associated low power mode is enabled.
0	0h RW	**S0i2.0 Enable (LPM0_EN):** If this bit is 1, the associated low power mode is enabled.

13.3.102 Low Power Mode 0 Residency Counter (LPM_0_RES)—Offset 1C80h

Residency, in XXus increments.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**S0i2.0 Residency Counter (LPM_0_RES):** Residency, in XXus increments.

13.3.103 Low Power Mode 1 Residency Counter (LPM_1_RES)—Offset 1C84h

Residency, in XXus increments.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**S0i2.1 Residency Counter (LPM_1_RES):** Residency, in XXus increments.

13.3.104 Low Power Mode 2 Residency Counter (LPM_2_RES)—Offset 1C88h

Residency, in XXus increments.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**S0i2.2 Residency Counter (LPM_2_RES):** Residency, in XXus increments.

13.3.105 Low Power Mode 3 Residency Counter (LPM_3_RES)—Offset 1C8Ch

Residency, in XXus increments.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**S0i3.0 Residency Counter (LPM_3_RES):** Residency, in XXus increments.

13.3.106 Low Power Mode 4 Residency Counter (LPM_4_RES)—Offset 1C90h

Residency, in XXus increments.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**S0i3.1 Residency Counter (LPM_4_RES):** Residency, in XXus increments.

13.3.107 Low Power Mode 5 Residency Counter (LPM_5_RES)—Offset 1C94h

Residency, in XXus increments.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**S0i3.2 Residency Counter (LPM_5_RES):** Residency, in XXus increments.

13.3.108 Low Power Mode 6 Residency Counter (LPM_6_RES)—Offset 1C98h

Residency, in XXus increments.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**S0i3.3 Residency Counter (LPM_6_RES):** Residency, in XXus increments.

13.3.109 Low Power Mode 7 Residency Counter (LPM_7_RES)—Offset 1C9Ch

Residency, in XXus increments.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**S0i3.4 Residency Counter (LPM_7_RES):** Residency, in XXus increments.

13.3.110 Power Gated ACK Status Register 0 (PPASR0)—Offset 1D80h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**CSME Power Gate Ack Status (AGT31_PG_ACK_STS):** Same description as bit 2.
30	0h RO/V	**Controller Link Power Gate Ack Status (AGT30_PG_ACK_STS):** Same description as bit 2.
29	0h RO/V	**CSME Power Gate Ack Status (AGT29_PG_ACK_STS):** Same description as bit 2.
28	0h RO/V	**CSME_KVM Power Gate Ack Status (AGT28_PG_ACK_STS):** Same description as bit 2.
27	0h RO/V	**CSME Power Gate Ack Status (AGT27_PG_ACK_STS):** Same description as bit 2.
26	0h RO/V	**DCI Power Gate Ack Status (AGT26_PG_ACK_STS):** Same description as bit 2.
25	0h RO/V	**XDCI Power Gate Ack Status (AGT25_PG_ACK_STS):** Same description as bit 2.
24:21	0h RO	Reserved.
20	0h RO/V	**SDXC Power Gate Ack Status (AGT20_PG_ACK_STS):** Same description as bit 2.
19	0h RO/V	**Intel Trace Hub Power Gate Ack Status (AGT19_PG_ACK_STS):** Same description as bit 2.
18	0h RO	Reserved.
17	0h RO/V	**ISH Power Gate Ack Status (AGT17_PG_ACK_STS):** Same description as bit 2.
16	0h RO/V	**SMBus Power Gate Ack Status (AGT16_PG_ACK_STS):** Same description as bit 2.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RO/V	**Intel Serial I/O Power Gate Ack Status (AGT14_PG_ACK_STS):** Same description as bit 2.
13	0h RO/V	**PCIe Controller D Power Gate Ack Status (AGT13_PG_ACK_STS):** Same description as bit 2.
12	0h RO/V	**HDA Power Gate Ack Status (AGT12_PG_ACK_STS):** Same description as bit 2.
11	0h RO/V	**HDA Power Gate Ack Status (AGT11_PG_ACK_STS):** Same description as bit 2.
10	0h RO/V	**HDA Power Gate Ack Status (AGT10_PG_ACK_STS):** Same description as bit 2.
9	0h RO/V	**HDA_PGD0 Power Gate Ack Status (AGT9_PG_ACK_STS):** Same description as bit 2.
8	0h RO/V	**SATA Power Gate Ack Status (AGT8_PG_ACK_STS):** Same description as bit 2.
7	0h RO/V	**GbE Power Gate Ack Status (AGT7_PG_ACK_STS):** Same description as bit 2.
6	0h RO/V	**PCIe Controller C Power Gate Ack Status (AGT6_PG_ACK_STS):** Same description as bit 2.
5	0h RO/V	**PCIe Controller B Power Gate Ack Status (AGT5_PG_ACK_STS):** Same description as bit 2.
4	0h RO/V	**PCIe Controller A Power Gate Ack Status (AGT4_PG_ACK_STS):** Same description as bit 2.
3	0h RO/V	**xHCI Power Gate Ack Status (AGT3_PG_ACK_STS):** Same description as bit 2.
2	0h RO/V	**SPI Power Gate Ack Status (AGT2_PG_ACK_STS):** This indicates the current status of the controller. 0: Controller may be power gated 1: Controller may not be power gated
1:0	0h RO	Reserved.

13.3.111 Power Gated ACK Status Register 1 (PPASR1)—Offset 1D84h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RO/V	**HDA Power Gate Ack Status (AGT60_PG_ACK_STS):** Same description as bit 0.
27	0h RO/V	**HDA Power Gate Ack Status (AGT59_PG_ACK_STS):** Same description as bit 0.
26	0h RO/V	**HDA Power Gate Ack Status (AGT58_PG_ACK_STS):** Same description as bit 0.
25:20	0h RO	Reserved.
19	0h RO/V	**CNVI_WIFI Power Gate Ack Status (AGT51_PG_ACK_STS):** Same description as bit 0.
18:8	0h RO	Reserved.
7	0h RO/V	**CSME Power Gate Ack Status (AGT39_PG_ACK_STS):** Same description as bit 0.
6	0h RO/V	**CSME Power Gate Ack Status (AGT38_PG_ACK_STS):** Same description as bit 0.
5	0h RO/V	**CSME Power Gate Ack Status (AGT37_PG_ACK_STS):** Same description as bit 0.
4	0h RO/V	**CSME Power Gate Ack Status (AGT36_PG_ACK_STS):** Same description as bit 0.
3	0h RO	Reserved.
2	0h RO/V	**CSME Power Gate Ack Status (AGT34_PG_ACK_STS):** Same description as bit 0.
1	0h RO/V	**CSME Power Gate Ack Status (AGT33_PG_ACK_STS):** Same description as bit 0.
0	0h RO/V	**CSME_USBR Power Gate Ack Status (AGT32_PG_ACK_STS):** This indicates the current status of the controller. 0: Controller may be power gated 1: Controller may not be power gated

13.3.112 PFET Enable Ack Register 0 (PPFEAR0)—Offset 1D90h

Intel(R) IP is power gated when the corresponding bit in PPFEAR0 or PPFEAR1 is set to 1

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**CSME PFET Enable Ack Status (AGT31_PFET_EN_ACK_STS):** Same definition as bit 2.
30	0h RO/V	**CSME_CLINK PFET Enable Ack Status (AGT30_PFET_EN_ACK_STS):** Same definition as bit 2.
29	0h RO/V	**CSME PFET Enable Ack Status (AGT29_PFET_EN_ACK_STS):** Same definition as bit 2.
28	0h RO/V	**CSME_KVM PFET Enable Ack Status (AGT28_PFET_EN_ACK_STS):** Same definition as bit 2.
27	0h RO/V	**CSME PFET Enable Ack Status (AGT27_PFET_EN_ACK_STS):** Same definition as bit 2.
26	0h RO/V	**DCI PFET Enable Ack Status (AGT26_PFET_EN_ACK_STS):** Same definition as bit 2.
25	0h RO/V	**XDCI PFET Enable Ack Status (AGT25_PFET_EN_ACK_STS):** Same definition as bit 2.
24:20	0h RO	Reserved.
19	0h RO/V	**Intel Trace Hub PFET Enable Ack Status (AGT19_PFET_EN_ACK_STS):** Same definition as bit 2.
18	0h RO	Reserved.
17	0h RO/V	**ISH PFET Enable Ack Status (AGT17_PFET_EN_ACK_STS):** Same definition as bit 2.
16	0h RO/V	**SMBus PFET Enable Ack Status (AGT16_PFET_EN_ACK_STS):** Same definition as bit 2.
15	0h RO	Reserved.
14	0h RO/V	**Intel Serial I/O PFET Enable Ack Status (AGT14_PFET_EN_ACK_STS):** Same definition as bit 2.
13	0h RO/V	**PCIe Controller D PFET Enable Ack Status (AGT13_PFET_EN_ACK_STS):** Same definition as bit 2.
12	0h RO/V	**HDA PFET Enable Ack Status (AGT12_PFET_EN_ACK_STS):** Same definition as bit 2.
11	0h RO/V	**HDA PFET Enable Ack Status (AGT11_PFET_EN_ACK_STS):** Same definition as bit 2.
10	0h RO/V	**HDA PFET Enable Ack Status (AGT10_PFET_EN_ACK_STS):** Same definition as bit 2.
9	0h RO/V	**HDA PFET Enable Ack Status (AGT9_PFET_EN_ACK_STS):** Same definition as bit 2.
8	0h RO/V	**SATA PFET Enable Ack Status (AGT8_PFET_EN_ACK_STS):** Same definition as bit 2.
7	0h RO/V	**GbE PFET Enable Ack Status (AGT7_PFET_EN_ACK_STS):** Same definition as bit 2.
6	0h RO/V	**PCIe Controller C PFET Enable Ack Status (AGT6_PFET_EN_ACK_STS):** Same definition as bit 2.
5	0h RO/V	**PCIe Controller B PFET Enable Ack Status (AGT5_PFET_EN_ACK_STS):** Same definition as bit 2.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO/V	**PCIe Controller A PFET Enable Ack Status (AGT4_PFET_EN_ACK_STS):** Same definition as bit 2.
3	0h RO/V	**xHCI PFET Enable Ack Status (AGT3_PFET_EN_ACK_STS):** Same definition as bit 2.
2	0h RO/V	**SPI PFET Enable Ack Status (AGT2_PFET_EN_ACK_STS):** 0: PFET is turned on 1: PFET is turned off
1:0	0h RO	Reserved.

13.3.113 PFET Enable Ack Register 1 (PPFEAR1)—Offset 1D94h

Intel(R) CSME is power gated when PPFEAR0[31..24]=0xF9 and PPFEAR1[7..0]=0xFF

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RO/V	**HDA PFET Enable Ack Status (AGT60_PFET_EN_ACK_STS):** Same definition as bit 0.
27	0h RO/V	**HDA PFET Enable Ack Status (AGT59_PFET_EN_ACK_STS):** Same definition as bit 0.
26	0h RO/V	**HDA PFET Enable Ack Status (AGT58_PFET_EN_ACK_STS):** Same definition as bit 0.
25:20	0h RO	Reserved.
19	0h RO/V	**CNVI_WIFI PFET Enable Ack Status (AGT51_PFET_EN_ACK_STS):** Same definition as bit 0.
18:8	0h RO	Reserved.
7	0h RO/V	**CSME PFET Enable Ack Status (AGT39_PFET_EN_ACK_STS):** Same definition as bit 0.
6	0h RO/V	**CSME PFET Enable Ack Status (AGT38_PFET_EN_ACK_STS):** Same definition as bit 0.
5	0h RO/V	**CSME PFET Enable Ack Status (AGT37_PFET_EN_ACK_STS):** Same definition as bit 0.
4	0h RO/V	**CSME PFET Enable Ack Status (AGT36_PFET_EN_ACK_STS):** Same definition as bit 0.
3	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO/V	**CSME PFET Enable Ack Status (AGT34_PFET_EN_ACK_STS):** Same definition as bit 0.
1	0h RO/V	**CSME PFET Enable Ack Status (AGT33_PFET_EN_ACK_STS):** Same definition as bit 0.
0	0h RO/V	**CSME__USBR PFET Enable Ack Status (AGT32_PFET_EN_ACK_STS):** 0: PFET is turned on 1: PFET is turned off

13.3.114 Chipset Initialization Register 5E0 (CIR5E0)—Offset 1DE0h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**CSME Power Gate Req Status (AGT31_PG_REQ_STS):** Same definition as bit 2.
30	0h RO/V	**CSME_CLINK Power Gate Req Status (AGT30_PG_REQ_STS):** Same definition as bit 2.
29	0h RO/V	**CSME Power Gate Req Status (AGT29_PG_REQ_STS):** Same definition as bit 2.
28	0h RO/V	**CSME_KVM Power Gate Req Status (AGT28_PG_REQ_STS):** Same definition as bit 2.
27	0h RO/V	**CSME Power Gate Req Status (AGT27_PG_REQ_STS):** Same definition as bit 2.
26	0h RO/V	**DCI Power Gate Req Status (AGT26_PG_REQ_STS):** Same definition as bit 2.
25	0h RO/V	**XDCI Power Gate Req Status (AGT25_PG_REQ_STS):** Same definition as bit 2.
24:21	0h RO	Reserved.
20	0h RO/V	**SDXC Power Gate Req Status (AGT20_PG_REQ_STS):** Same definition as bit 2.
19	0h RO/V	**Intel Trace Hub Power Gate Req Status (AGT19_PG_REQ_STS):** Same definition as bit 2.
18	0h RO	Reserved.
17	0h RO/V	**ISH Power Gate Req Status (AGT17_PG_REQ_STS):** Same definition as bit 2.
16	0h RO/V	**SMBus Power Gate Req Status (AGT16_PG_REQ_STS):** Same definition as bit 2.
15	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO/V	**Intel Serial I/O Power Gate Req Status (AGT14_PG_REQ_STS):** Same definition as bit 2.
13	0h RO	Reserved.
12	0h RO/V	**HDA Power Gate Req Status (AGT12_PG_REQ_STS):** Same definition as bit 2.
11	0h RO/V	**HDA Power Gate Req Status (AGT11_PG_REQ_STS):** Same definition as bit 2.
10	0h RO/V	**HDA Power Gate Req Status (AGT10_PG_REQ_STS):** Same definition as bit 2.
9	0h RO/V	**HDA Power Gate Req Status (AGT9_PG_REQ_STS):** Same definition as bit 2.
8	0h RO/V	**SATA Power Gate Req Status (AGT8_PG_REQ_STS):** Same definition as bit 2.
7	0h RO/V	**GbE Power Gate Req Status (AGT7_PG_REQ_STS):** Same definition as bit 2.
6	0h RO/V	**PCIe Controller C Power Gate Req Status (AGT6_PG_REQ_STS):** Same definition as bit 2.
5	0h RO/V	**PCIe Controller B Power Gate Req Status (AGT5_PG_REQ_STS):** Same definition as bit 2.
4	0h RO/V	**PCIe Controller A Power Gate Req Status (AGT4_PG_REQ_STS):** Same definition as bit 2.
3	0h RO/V	**xHCI Power Gate Req Status (AGT3_PG_REQ_STS):** Same definition as bit 2.
2	0h RO/V	**SPI Power Gate Req Status (AGT2_PG_REQ_STS):** This indicates the current power gating request status of the controller. 0: Controller is requesting to be power-gated 1: Controller is requesting to be powered-on.
1:0	0h RO	Reserved.

13.3.115 Chipset Initialization Register 5E4 (CIR5E4)—Offset 1DE4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RO/V	**HDA Power Gate Req Status (AGT60_PG_REQ_STS):** Same definition as bit 0.
27	0h RO/V	**HDA Power Gate Req Status (AGT59_PG_REQ_STS):** Same definition as bit 0.
26	0h RO/V	**HDA Power Gate Req Status (AGT58_PG_REQ_STS):** Same definition as bit 0.
25:23	0h RO	Reserved.
22	0h RO/V	**SPF Power Gate Req Status (AGT54_PG_REQ_STS):** Same definition as bit 0.
21	0h RO/V	**eMMC Power Gate Req Status (AGT53_PG_REQ_STS):** Same definition as bit 0.
20	0h RO/V	**UFS Power Gate Req Status (AGT52_PG_REQ_STS):** Same definition as bit 0.
19	0h RO/V	**CNVI_WIFI Power Gate Req Status (AGT51_PG_REQ_STS):** Same definition as bit 0.
18:8	0h RO	Reserved.
7	0h RO/V	**CSME Power Gate Req Status (AGT39_PG_REQ_STS):** Same definition as bit 0.
6	0h RO/V	**CSME Power Gate Req Status (AGT38_PG_REQ_STS):** Same definition as bit 0.
5	0h RO/V	**CSME Power Gate Req Status (AGT37_PG_REQ_STS):** Same definition as bit 0.
4	0h RO/V	**CSME_SMS2 Power Gate Req Status (AGT36_PG_REQ_STS):** Same definition as bit 0.
3	0h RO	Reserved.
2	0h RO/V	**CSME Power Gate Req Status (AGT34_PG_REQ_STS):** Same definition as bit 0.
1	0h RO/V	**CSME Power Gate Req Status (AGT33_PG_REQ_STS):** Same definition as bit 0.
0	0h RO/V	**CSME_USBR Power Gate Req Status (AGT32_PG_REQ_STS):** 0: IP may be power gated 1: IP may not be power gated

13.3.116 Static PG Function Disable 1 (ST_PG_FDIS1)—Offset 1E20h

Static PG Related Function Disable Register 1

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Static Function Disable Lock (ST_FDIS_LK):** Lock control for all ST_PG_FDIS* and NST_PG_FDIS_* registers. Also self-locks when written to 1. This bit is reset by RSMRST# assertion.
30:6	0h RO	Reserved.
5	0h RW/L	**ISH Function Disable (PMC Version) (ISH_FDIS_PMC):** BIOS is required to set this bit when ISH function is configured to be function disabled. This bit is reset by RTCRST# assertion.
4:2	0h RO	Reserved.
1	0h RW/L	**CNVI Function Disable (PMC Version) (CNVI_FDIS_PMC):** BIOS is required to set this bit when GBE function is configured to be function disabled.
0	0h RW/L	**GBE Function Disable (PMC Version) (GBE_FDIS_PMC):** BIOS is required to set this bit when GBE function is configured to be function disabled. This bit is reset by RTCRST#

13.3.117 Static Function Disable Control 2 (ST_PG_FDIS2)—Offset 1E24h

Static Function Disable Control 2 Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW/L	**GSPI Controller Device Device 2 Function Disable (PMC Version) (LPSS_GSPI2_FDIS_PMC):** BIOS is required to set this bit when this Device (single function) is configured to be function disabled.
10	0h RW/L	**GSPI Controller Device Device 1 Function Disable (PMC Version) (LPSS_GSPI1_FDIS_PMC):** BIOS is required to set this bit when this Device (single function) is configured to be function disabled.
9	0h RW/L	**GSPI Controller Device Device 0 Function Disable (PMC Version) (LPSS_GSPI0_FDIS_PMC):** BIOS is required to set this bit when this Device (single function) is configured to be function disabled.
8	0h RW/L	**UART Controller Device Device 2 Function Disable (PMC Version) (LPSS_UART2_FDIS_PMC):** BIOS is required to set this bit when this Device (single function) is configured to be function disabled.
7	0h RW/L	**UART Controller Device Device 1 Function Disable (PMC Version) (LPSS_UART1_FDIS_PMC):** BIOS is required to set this bit when this Device (single function) is configured to be function disabled.
6	0h RW/L	**UART Controller Device Device 0 Function Disable (PMC Version) (LPSS_UART0_FDIS_PMC):** BIOS is required to set this bit when this Device (single function) is configured to be function disabled.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/L	**I2C Controller Device 5 Function Disable (PMC Version) (LPSS_I2C5_FDIS_PMC):** BIOS is required to set this bit when this Device (single function) is configured to be function disabled.
4	0h RW/L	**I2C Controller Device 4 Function Disable (PMC Version) (LPSS_I2C4_FDIS_PMC):** BIOS is required to set this bit when this Device (single function) is configured to be function disabled.
3	0h RW/L	**I2C Controller Device 3 Function Disable (PMC Version) (LPSS_I2C3_FDIS_PMC):** BIOS is required to set this bit when this Device (single function) is configured to be function disabled.
2	0h RW/L	**I2C Controller Device 2 Function Disable (PMC Version) (LPSS_I2C2_FDIS_PMC):** BIOS is required to set this bit when this Device (single function) is configured to be function disabled.
1	0h RW/L	**I2C Controller Device 1 Function Disable (PMC Version) (LPSS_I2C1_FDIS_PMC):** BIOS is required to set this bit when this Device (single function) is configured to be function disabled.
0	0h RW/L	**I2C Controller Device 0 Function Disable (PMC Version) (LPSS_I2C0_FDIS_PMC):** BIOS is required to set this bit when this Device (single function) is configured to be function disabled.

13.3.118 Chipset Initialization Register (NST_PG_FDIS_1)—Offset 1E28h

BIOS may need to program this register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27	0h RW/L	**UFSX2 Function Disable (PMC Version) (UFSX2_FDIS_PMC):** BIOS is required to set this bit when this IP block (single function) is configured to be function disabled.
26	0h RW/L	**XDCI Function Disable (PMC Version) (XDCI_FDIS_PMC):** BIOS is required to set this bit when this IP block (single function) is configured to be function disabled.
25	0h RW/L	**SMB Function Disable (PMC Version) (SMB_FDIS_PMC):** BIOS is required to set this bit when this IP block (single function) is configured to be function disabled.
24	0h RW/L	**LPC Function Disable (PMC Version) (LPC_FDIS_PMC):** BIOS is required to set this bit when this IP block (single function) is configured to be function disabled.
23	0h RW/L	**ADSP Function Disable (PMC Version) (ADSP_FDIS_PMC):** BIOS is required to set this bit when this IP block (single function) is configured to be function disabled.
22	0h RW/L	**SATA Controller Function Disable (PMC Version) (ST_FDIS_PMC):** BIOS is required to set this bit when the SATA controller (single function) is configured to be function disabled.
21:18	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW/L	**PCIe Controller D Port 3 Function Disable [PMC Version] (PCIE_D3_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
16	0h RW/L	**PCIe Controller D Port 2 Function Disable [PMC Version] (PCIE_D2_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
15	0h RW/L	**PCIe Controller D Port 1 Function Disable [PMC Version] (PCIE_D1_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
14	0h RW/L	**PCIe Controller D Port 0 Function Disable [PMC Version] (PCIE_D0_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
13	0h RW/L	**PCIe Controller C Port 3 Function Disable (PMC Version) (PCIE_C3_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
12	0h RW/L	**PCIe Controller C Port 2 Function Disable (PMC Version) (PCIE_C2_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
11	0h RW/L	**PCIe Controller C Port 1 Function Disable (PMC Version) (PCIE_C1_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
10	0h RW/L	**PCIe Controller C Port 0 Function Disable (PMC Version) (PCIE_C0_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
9	0h RW/L	**PCIe Controller B Port 3 Function Disable (PMC Version) (PCIE_B3_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
8	0h RW/L	**PCIe Controller B Port 2 Function Disable (PMC Version) (PCIE_B2_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
7	0h RW/L	**PCIe Controller B Port 1 Function Disable (PMC Version) (PCIE_B1_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
6	0h RW/L	**PCIe Controller B Port 0 Function Disable (PMC Version) (PCIE_B0_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
5	0h RW/L	**PCIe Controller A Port 3 Function Disable (PMC Version) (PCIE_A3_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
4	0h RW/L	**PCIe Controller A Port 2 Function Disable (PMC Version) (PCIE_A2_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
3	0h RW/L	**PCIe Controller A Port 1 Function Disable (PMC Version) (PCIE_A1_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
2	0h RW/L	**PCIe Controller A Port 0 Function Disable (PMC Version) (PCIE_A0_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
1	0h RO	Reserved.
0	0h RW/L	**xHCI Function Disable (PMC Version) (xHCI_FDIS_PMC):** BIOS is required to set this bit when this IP block (single logical function) is configured to be function disabled.

13.3.119 PCIe Controller Disable Read (N_STPG_FUSE_SS_DIS_RD_1)—Offset 1E40h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RO/V	**PCIe Controller D Port 3 Disable (PCIE_D3_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
16	0h RO/V	**PCIe Controller D Port 2 Disable (PCIE_D2_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
15	0h RO/V	**PCIe Controller D Port 1 Disable (PCIE_D1_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
14	0h RO/V	**PCIe Controller D Port 0 Disable (PCIE_D0_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
13	0h RO/V	**PCIe Controller C Port 3 Disable (PCIE_C3_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
12	0h RO/V	**PCIe Controller C Port 2 Disable (PCIE_C2_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
11	0h RO/V	**PCIe Controller C Port 1 Disable (PCIE_C1_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
10	0h RO/V	**PCIe Controller C Port 0 Disable (PCIE_C0_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
9	0h RO/V	**PCIe Controller B Port 3 Disable (PCIE_B3_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
8	0h RO/V	**PCIe Controller B Port 2 Disable (PCIE_B2_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
7	0h RO/V	**PCIe Controller B Port 1 Disable (PCIE_B1_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
6	0h RO/V	**PCIe Controller B Port 0 Disable (PCIE_B0_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
5	0h RO/V	**PCIe Controller A Port 3 Disable (PCIE_A3_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
4	0h RO/V	**PCIe Controller A Port 2 Disable (PCIE_A2_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
3	0h RO/V	**PCIe Controller A Port 1 Disable (PCIE_A1_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
2	0h RO/V	**PCIe Controller A Port 0 Disable (PCIE_A0_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
1:0	0h RO	Reserved.

13.3.120 Capability Disable Read Register (STPG_FUSE_SS_DIS_RD_2)—Offset 1E44h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RO/V	**TBT LSX Disable (TBTLSX_FUSE_SS_DIS):** This bit indicates if TBTLSX function is disabled.
28:20	0h RO	Reserved.
19	0h RO/V	**xDCI Disable (XDCI_FUSE_SS_DIS):** RO bit indicating if xDCI function is disabled.
18:17	0h RO	Reserved.
16	0h RO/V	**DSP Disable (DSP_FUSE_SS_DIS):** RO bit indicating if DSP function is disabled.
15:10	0h RO	Reserved.
9	0h RO/V	**SMBus Disable (SMB_FUSE_SS_DIS):** RO bit indicating if SMBus function is disabled.
8:7	0h RO	Reserved.
6	0h RO/V	**Intel Serial I/O Disable (LPSS_FUSE_SS_DIS):** RO bit indicating if Serial IO (I2C, UART, GSPI) function is disabled.
5	0h RO/V	**eMMC Disable (EMMC_FUSE_SS_DIS):** RO bit indicating if eMMC function is disabled.
4	0h RO/V	**CNVi Disable (CNVI_FUSE_SS_DIS):** RO bit indicating if CNVi function is disabled.
3	0h RO	Reserved.
2	0h RO/V	**SD Controller Disable (SDX_FUSE_SS_DIS):** RO bit indicating if SDXC function is disabled.
1	0h RO/V	**ISH Disable (ISH_FUSE_SS_DIS):** RO bit indicating if ISH function is disabled.
0	0h RO/V	**GBE Disable (GBE_FUSE_SS_DIS):** RO bit indicating if GBE function is disabled.

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14 High Definition Audio Interface (D31:F3)

14.1 High Definition Audio PCI Configuration Registers

Table 14-1. Summary of High Definition Audio PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	1h	Vendor Identification (VID)—Offset 0h	8086h
2h	3h	Device ID (DID)—Offset 2h	XXXXh
4h	5h	Command (CMD)—Offset 4h	0h
6h	7h	Status (STS)—Offset 6h	10h
8h	8h	Revision Identification (RID)—Offset 8h	XXh
9h	9h	Programming Interface (PI)—Offset 9h	0h
Ah	Ah	Sub Class Code (SCC)—Offset Ah	3h
Bh	Bh	Base Class Code (BCC)—Offset Bh	4h
Ch	Ch	Cache Line Size (CLS)—Offset Ch	0h
Dh	Dh	Latency Timer (LT)—Offset Dh	0h
Eh	Eh	Header Type (HTYPE)—Offset Eh	0h
10h	13h	Intel HD Audio Base Lower Address (HDALBA)—Offset 10h	4h
14h	17h	Intel HD Audio Base Upper Address (HDAUBA)—Offset 14h	0h
18h	1Bh	Shadowed PCI Configuration Lower Base Address (SPCLBA)—Offset 18h	0h
1Ch	1Fh	Shadowed PCI Configuration Upper Base Address (SPCUBA)—Offset 1Ch	0h
20h	23h	Audio DSP Lower Base Address (ADSPLBA)—Offset 20h	4h
24h	27h	Audio DSP Upper Base Address (ADSPUBA)—Offset 24h	0h
2Ch	2Dh	Subsystem Vendor ID (SVID)—Offset 2Ch	0h
2Eh	2Fh	Subsystem ID (SID)—Offset 2Eh	0h
34h	34h	Capability Pointer (CAPPTR)—Offset 34h	50h
3Ch	3Ch	Interrupt Line (INTLN)—Offset 3Ch	0h
3Dh	3Dh	Interrupt Pin (INTPN)—Offset 3Dh	1h
50h	51h	PCI Power Management Capability ID (PID)—Offset 50h	6001h
52h	53h	Power Management Capabilities (PC)—Offset 52h	C043h
54h	57h	Power Management Control And Status (PCS)—Offset 54h	8h
60h	61h	MSI Capability ID (MID)—Offset 60h	7005h
62h	63h	MSI Message Control (MMC)—Offset 62h	80h
64h	67h	MSI Message Lower Address (MMLA)—Offset 64h	0h
68h	6Bh	MSI Message Upper Address (MMUA)—Offset 68h	0h
6Ch	6Dh	MSI Message Data (MMD)—Offset 6Ch	0h
70h	71h	PCI Express Capability ID (PXID)—Offset 70h	10h
72h	73h	PCI Express Capabilities (PXC)—Offset 72h	91h

Table 14-1. Summary of High Definition Audio PCI Configuration Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
74h	77h	Device Capabilities (DEVCAP)—Offset 74h	10000000h
78h	79h	Device Control (DEVC)—Offset 78h	2800h
7Ah	7Bh	Device Status (DEVS)—Offset 7Ah	10h

14.1.1 Vendor Identification (VID)—Offset 0h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 8086h

Bit Range	Default and Access	Field Name (ID): Description
15:0	8086h RO	**Vendor ID (VID):** Indicates that Intel is the vendor.

14.1.2 Device ID (DID)—Offset 2h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: XXXXh

Bit Range	Default and Access	Field Name (ID): Description
15:0	8C20h RO/V	**Device ID (DID):** Indicates the Device ID of the controller. Refer to the Device and Revision ID Table in Volume 1 for default value.

14.1.3 Command (CMD)—Offset 4h

This register provides coarse control over a device's ability to generate and respond to PCI cycles.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (ID):** Enables the device to assert an INTx#. When set, the Intel(r) HD Audio controller's INTx# signal will be de-asserted. When cleared, the INTx# signal may be asserted. Note that this bit does not affect the generation of MSI's.
9	0h RO	**Fast Back to Back Enable (FBE):** Not implemented. Hardwired to 0.
8	0h RW	**SERR Enable (SEN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
7	0h RO	**Wait Cycle Control (WCC):** Not implemented. Hardwired to 0.
6	0h RW	**Parity Error Response (PER):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
5	0h RO	**VGA Palette Snoop (VPS):** Not implemented. Hardwired to 0.
4	0h RO	**Memory Write and Invalidate Enable (MWI):** Not implemented. Hardwired to 0.
3	0h RO	**Special Cycle Enable (SCE):** Not implemented. Hardwired to 0.
2	0h RW	**Bus Initiator Enable (BME):** 1 = Enable, 0 = Disable. Controls standard PCI Express bus Initiatoring capabilities for Memory and IO, reads and writes. Note that this also controls MSI generation since MSI are essentially Memory writes.
1	0h RW	**Memory Space Enable (MSE):** When set, enables memory space accesses to the Intel HD Audio controller.
0	0h RO	**I/O Space (IOS):** The Intel HD Audio controller does not implement IO Space, therefore this bit is hardwired to 0.

14.1.4 Status (STS)—Offset 6h

This register is used to record status information for PCI bus related events.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 10h

Bit Range	Default and Access	Field Name (ID): Description
15	0h RO	**Detected Parity Error (DPE):** Not implemented. Hardwired to 0.
14	0h RO	**SERR# Status (SERRS):** Not implemented. Hardwired to 0.
13	0h RW/1C/V	**Received Initiator Abort (RMA):** If the completion status received from IOSF is UR, this bit is set. SW writes a 1 to this bit to clear it.
12	0h RW/1C/V	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, this bit is set. SW writes a 1 to this bit to clear it.
11	0h RO	**Signaled Target-Abort (STA):** Not implemented. Hardwired to 0.
10:9	0h RO	**DEVSEL# Timing Status (DEVT):** Does not apply. Hardwired to 0.
8	0h RO	**Initiator Data Parity Error (MDPE):** Not implemented. Hardwired to 0.
7	0h RO	**Fast Back to Back Capable (FBC):** Does not apply. Hardwired to 0.
6	0h RO	Reserved.
5	0h RO	**66 MHz Capable (C66):** Does not apply. Hardwired to 0.
4	1h RO	**Capabilities List Exists (CLIST):** Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h.
3	0h RO/V	**Interrupt Status (IS):** Reflects the state of the INTx# signal at the input of the enable/disable circuit. This bit is a 1 when the INTx# is asserted. This bit is a 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the command register). Note that this bit is not set by an MSI.
2:0	0h RO	Reserved.

14.1.5 Revision Identification (RID)—Offset 8h

This register is not affected by D3HOT to D0 reset or FLR

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: XXh

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RO/V	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Volume 1 for specific value.

14.1.6 Programming Interface (PI)—Offset 9h

This register is not affected by D3HOT to D0 reset or FLR

Access Method

Type: CFG Register (Size: 8 bits)
Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW/L	**Programming Interface (PI):** Value assigned to the Intel HD Audio subsystem. Locked when FNCFG.BCLD = 1.

14.1.7 Sub Class Code (SCC)—Offset Ah

This register is not affected by D3HOT to D0 reset or FLR

Access Method

Type: CFG Register (Size: 8 bits)
Device: 31
Function: 3

Default: 3h

Bit Range	Default and Access	Field Name (ID): Description
7:0	3h RW/L	**Sub Class Code (SCC):** This indicates the device is an Intel HD Audio audio device, in the context of a multimedia device. Locked when FNCFG.BCLD = 1.

14.1.8 Base Class Code (BCC)—Offset Bh

This register is not affected by D3HOT to D0 reset or FLR

Access Method

Type: CFG Register (Size: 8 bits)
Device: 31
Function: 3

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
7:0	4h RW/L	**Base Class Code (BCC):** This register indicates that the function implements a multimedia device. Locked when FNCFG.BCLD = 1.

14.1.9 Cache Line Size (CLS)—Offset Ch

This register specifies the system cache line size in units of DWORDs.

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**Cache Line Size (CLS):** Does not apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the PCH.

14.1.10 Latency Timer (LT)—Offset Dh

This register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus Initiator.

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW/L	**Latency Timer (LT):** Doesn t apply to PCI Express. RO as 00h if PCI Express. If configured to appear as PCI device, maintain RW for Legacy PCI SW compliancy. Locked when FNCFG.HDASPCID = 0

14.1.11 Header Type (HTYPE)—Offset Eh

This register identifies the layout of the second part of the predefined header and also whether or not the device contains multiple functions.

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7	0h RW/L	**Multi Function Device (MFD):** Value of 0 indicates a single function device. Value of 1 indicates a multi function device. Locked when FNCFG.BCLD = 1.
6:0	0h RO	**Header Type (HTYPE):** Implements Type 0 Configuration header.

14.1.12 Intel HD Audio Base Lower Address (HDALBA)—Offset 10h

This BAR creates a selected size of memory space to signify the base address of the Intel HD Audio memory mapped configuration registers depending on implementation.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:14	0h RW	**Lower Base Address (LBA):** Base address for the Intel HD Audio subsystem s memory mapped configuration registers. 16 Kbytes are requested by hardwiring bits 13:4 to 0 s.
13:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PREF):** Indicates that this BAR is NOT pre-fetchable.
2:1	2h RO	**Address Range (ADDRNG):** Indicates that this BAR can be located anywhere in 64-bit address space.
0	0h RO	**Space Type (SPTYP):** Indicates that this BAR is located in memory space.

14.1.13 Intel HD Audio Base Upper Address (HDAUBA)—Offset 14h

This BAR creates a selected size of memory space to signify the base address (upper 32 bits) of the Intel HD Audio memory mapped configuration registers, depending on implementation.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Intel HD Audio Upper Base Address (UBA):** Upper 32 bits of the Base address for the Intel(r) HD Audio controller's memory mapped configuration registers.

14.1.14 Shadowed PCI Configuration Lower Base Address (SPCLBA)—Offset 18h

This BAR creates 4 Kbytes of memory space to signify the base address (lower 32 bits) of the shadowed PCI configuration when used as an ACPI device.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:12	0h RW/L	**Lower Base Address (LBA):** Base address for the PCI Configuration register shadowed to memory mapped. 4 KB is requested by hardwiring bits 11:4 to 0 s. Locked when PCICFGCTL0.SPCBAD = 1.
11:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PREF):** Indicates that this BAR is NOT pre-fetchable.
2:1	0h RO/V	**Address Range (ADDRNG):** Indicates that this BAR can be located anywhere in 64-bit address space.
0	0h RO	**Space Type (SPTYP):** Indicates that this BAR is located in memory space.

14.1.15 Shadowed PCI Configuration Upper Base Address (SPCUBA)—Offset 1Ch

This BAR creates 4 Kbytes of memory space to signify the base address (upper 32 bits) of the shadowed PCI configuration when used as an ACPI device.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/L	**Upper Base Address (UBA):** Upper 32 bits of the Base address for the PCI Configuration register shadowed to memory mapped. Locked when PCICFGCTL0.SPCBAD = 1.

14.1.16 Audio DSP Lower Base Address (ADSPLBA)—Offset 20h

This BAR creates a selected size of memory space to signify the base address of the Audio DSP memory mapped configuration registers depending on implementation. The number of LBA bits in this register is depending on the size of the memory window implemented.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 3

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:20	0h RW	**Lower Base Address (LBA):** Base address for the Audio DSP memory mapped configuration registers.
19:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PREF):** Indicates that this BAR is NOT pre-fetchable.
2:1	2h RO	**Address Range (ADDRNG):** Indicates that this BAR can be located anywhere in 64-bit address space.
0	0h RO	**Space Type (SPTYP):** Indicates that this BAR is located in memory space.

14.1.17 Audio DSP Upper Base Address (ADSPUBA)—Offset 24h

This BAR creates a selected size of memory space to signify the base address (upper 32 bits) of the Audio DSP memory-mapped configuration registers, depending on implementation.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Upper Base Address (UBA):** Upper 32 bits of the Base address for the Audio DSP memory mapped configuration registers.

14.1.18 Subsystem Vendor ID (SVID)—Offset 2Ch

This register should be implemented for any function that could be instantiated more than once in a given system, for example, a system with 2 audio subsystems, one down on the motherboard and the other plugged into a PCI expansion slot, should have the SVID register implemented. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one audio subsystem from the other(s).
Software (BIOS) will write the value to this register. After that, the value can be read, but writes to the register will have no effect. The write to this register should be combined with the write to the SID to create one 32-bit write. This register is not affected by D3HOT to D0 reset or FLR

Access Method

Type: CFG Register (Size: 16 bits)
Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:0	0h RW/L	**SVID (SVID):** These RW bits have no functionality. Locked when FNCFG.BCLD = 1.

14.1.19 Subsystem ID (SID)—Offset 2Eh

This register should be implemented for any function that could be instantiated more than once in a given system, for example, a system with 2 audio subsystems, one down on the motherboard and the other plugged into a PCI expansion slot. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from the other(s). Software (BIOS) will write the value to this register. After that, the value can be read, but writes to the register will have no effect. The write to this register should be combined with the write to the SVID to create one 32-bit write. This register is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register (Size: 16 bits)
Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:0	0h RW/L	**SID (SID):** These RW bits have no functionality. Locked when FNCFG.BCLD = 1.

14.1.20 Capability Pointer (CAPPTR)—Offset 34h

This optional register is used to point to a linked list of new capabilities implemented by this device.

Access Method

Type: CFG Register (Size: 8 bits)
Device: 31
Function: 3

Default: 50h

Bit Range	Default and Access	Field Name (ID): Description
7:0	50h RO	**Capability Pointer (CAPPTR):** Indicates that the first capability pointer offset is offset 50h (Power Management Capability).

14.1.21 Interrupt Line (INTLN)—Offset 3Ch

This register is not affected by FLR.

Access Method

Type: CFG Register (Size: 8 bits)
Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**Interrupt Line (INTLN):** Hardware does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

14.1.22 Interrupt Pin (INTPN)—Offset 3Dh

This register is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register (Size: 8 bits)
Device: 31
Function: 3

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
7:4	0h RO	Reserved.
3:0	1h RW/L	**Interrupt Pin (INTPN):** Identifies the interrupt pin the function uses. 0h: No interrupt pin 1h: INTA 2h: INTB 3h: INTC 4h: INTD 5h - Fh: reserved Locked when FNCFG.BCLD = 1.

14.1.23 PCI Power Management Capability ID (PID)—Offset 50h

This register declares the power management capability structure.

Access Method

Type: CFG Register (Size: 16 bits)
Device: 31
Function: 3

Default: 6001h

Bit Range	Default and Access	Field Name (ID): Description
15:8	60h RW/L	**Next Capability (NEXT):** Points to the next capability structure (MSI). Locked when FNCFG.BCLD = 1.
7:0	1h RO	**Cap ID (CAP):** Indicates that this pointer is a PCI power management capability

14.1.24 Power Management Capabilities (PC)—Offset 52h

This register provides information on the capabilities of the function related to power management.

Access Method

Type: CFG Register (Size: 16 bits)
Device: 31
Function: 3

Default: C043h

Bit Range	Default and Access	Field Name (ID): Description
15:11	18h RW/L	**PME_Support (PMES):** Indicates PME# can be generated from D3 and D0 states. Programmable by BIOS for the option to declare SUS well wake is supported or not: 19h (SUS well wake supported) or 09h (SUS well wake not supported). Locked when FNCFG.BCLD = 1
10	0h RO	**D2_Support (D2S):** The D2 state is not supported.

Bit Range	Default and Access	Field Name (ID): Description
9	0h RO	**D1_Support (D1S):** The D1 state is not supported.
8:6	1h RW/L	**Aux_Current (AC):** Reports 55 mA maximum Suspend well current required when in the D3cold state. Programmable by BIOS for the option to declare SUS well wake is supported or not: 001b (SUS well wake supported) or 000b (SUS well wake not supported). Locked when FNCFG.BCLD = 1.
5	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
4	0h RO	Reserved.
3	0h RO	**PME Clock (PMEC):** Does not apply. Hardwired to 0.
2:0	3h RW/L	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification. Programmable by BIOS to older revision if compatibility issue is found. Locked when FNCFG.BCLD = 1.

14.1.25 Power Management Control And Status (PCS)—Offset 54h

PMES and PMEE bits reside in Resume well, and reset by resume reset.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	**Data (DT):** Does not apply. Hardwired to 0's.
23	0h RO	**Bus Power/Clock Control Enable (BPCCE):** Does not apply. Hardwired to0.
22	0h RO	**B2/B3 Support (B23):** Does not apply. Hardwired to 0.
21:16	0h RO	Reserved.
15	0h RW/1C/V	**PME Status (PMES):** This bit is set when the Intel HD Audio controller would normally assert the PME# signal independent of the state of the PME bit. This bit is cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.
14:9	0h RO	Reserved.
8	0h RW	**PME Enable (PMEE):** When set, and if corresponding PMES is also set, the Intel HD Audio subsystem send PME to PMC. This bit is cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.
7:4	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
3	1h RW/L	**No Soft Reset (NSR):** When set (1), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. When clear (0), devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon transition from the D3hot to the D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled. Locked when FNCFG.BCLD = 1.
2	0h RO	Reserved.
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the Intel HD Audio subsystem and to set a new power state. The values are: 00 D0 state 11 D3HOT state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally, however, the data is discarded and no state change occurs. When in the D3HOT states, the Intel HD Audio subsystem s configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. When software changes this value from the D3HOT state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the function.

14.1.26 MSI Capability ID (MID)—Offset 60h

NEXT field is not affected by D3HOT to D0 reset or FLR

Access Method

Type: CFG Register (Size: 16 bits)
Device: 31
Function: 3

Default: 7005h

Bit Range	Default and Access	Field Name (ID): Description
15:8	70h RO/V	**Next Capability (NEXT):** Points to the PCI Express* capability structure. The value of this field depends on the FNCFG.HDASPCID bit. When FNCFG.HDASPCID is 0 , this field has a value of 70h where it points to the PCI Express capability structure. When FNCFG.HDASPCID bit is 1 , this field has a value of 00h to indicate that this is the last capability structure in the list.
7:0	5h RO	**Cap ID (CAP):** Indicates that this pointer is a MSI capability

14.1.27 MSI Message Control (MMC)—Offset 62h

This register provides system software control over MSI.

Access Method

Type: CFG Register (Size: 16 bits)
Device: 31
Function: 3

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7	1h RO	**64b Address Capability (ADD64):** Indicates the ability to generate a 64-bitmessage address
6:4	0h RO	**Multiple Message Enable (MME):** Normally this is a R/W register. However since only 1 message is supported, these bits are hardwired to 000 = 1 message.
3:1	0h RO	**Multiple Message Capable (MMC):** Hardwired to 0 indicating request for 1message
0	0h RW	**MSI Enable (ME):** If set to 1 an MSI will be generated instead of an INTx#signal. If set to 0, an MSI may not be generated.

14.1.28 MSI Message Lower Address (MMLA)—Offset 64h

This register specifies the MSI message address (lower 32 bits).

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**MSI Message Lower Address (MMLA):** Lower Address used for MSI Message.
1:0	0h RO	Reserved.

14.1.29 MSI Message Upper Address (MMUA)—Offset 68h

This register specifies the MSI message address (upper 32 bits).

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI Message Upper Address (MMUA):** Upper 32 bits of address used for MSIMessage.

14.1.30 MSI Message Data (MMD)—Offset 6Ch

This register specifies the MSI message data.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:0	0h RW	**MSI Message Data (MMD):** Data used for MSI Message.

14.1.31 PCI Express Capability ID (PXID)—Offset 70h

This register declares the PCI Express capability structure.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 10h

Bit Range	Default and Access	Field Name (ID): Description
15:8	0h RO	**Next Capability (NEXT):** Indicates that this is the last capability structure in the list.
7:0	10h RO	**Cap ID (CAP):** Indicates that this pointer is a PCI Express capability structure.

14.1.32 PCI Express Capabilities (PXC)—Offset 72h

This register identifies PCI Express device Function type and associated capabilities.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 91h

Bit Range	Default and Access	Field Name (ID): Description
15:14	0h RO	Reserved.
13:9	0h RO	**Interrupt Message Number (IMN):** Hardwired to 0.
8	0h RO	**Slot Implemented (SI):** Hardwired to 0.
7:4	9h RO	**Device/Port Type (DPT):** Indicates that this is a Root Complex IntegratedEndpoint Device.
3:0	1h RO	**Capability Version (CV):** Indicates version #1 PCI Express capability

14.1.33 Device Capabilities (DEVCAP)—Offset 74h

This register is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 10000000h

Bit Range	Default and Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	1h RW/L	**Functional Level Reset (FLR):** A 1 indicates that the Intel HD Audio subsystem supports the Function Level Reset capability. Locked when FNCFG.BCLD = 1.
27:26	0h RO	**Captured Slot Power Limit Scale (SPLS):** Hardwired to 0.
25:18	0h RO	**Captured Slot Power Limit Value (SPLV):** Hardwired to 0.
17:15	0h RO	Reserved.
14	0h RO	**Power Indicator Present (PIP):** Hardwired to 0.
13	0h RO	**Attention Indicator Present (AIP):** Hardwired to 0.
12	0h RO	**Attention Button Present (ABP):** Hardwired to 0.
11:9	0h RW/L	**Endpoint L1 Acceptable Latency (L1CAP):** This bit field is defined in the PCI Express spec as RO. At this time it is risky to assign a hardwired value to this bit field. Making it RW would cause a WHQL failure. By making it RW/L it will appear as RO to WHQL testing while allowing BIOS to write a value at boot that is determined by post silicon system testing. Locked when FNCFG.BCLD = 1.

Bit Range	Default and Access	Field Name (ID): Description
8:6	0h RW/L	**Endpoint L0s Acceptable Latency (L0SCAP):** This bit field is defined in the PCI Express spec as RO. At this time it is risky to assign a hardwired value to this bit field. Making it RW would cause a WHQL failure. By making it RW/L it will appear as RO to WHQL testing while allowing BIOS to write a value at boot that is determined by post silicon system testing. Locked when FNCFG.BCLD = 1.
5	0h RO	**Extended Tag Field Support (ETCAP):** Indicates 5 bit tag supported.
4:3	0h RO	**Phantom Functions Supported (PFCAP):** Indicates phantom functions notsupported.
2:0	0h RO	**Max Payload Size Supported (MPCAP):** Indicates 128B maximum payloadsize capability.

14.1.34 Device Control (DEVC)—Offset 78h

NSNPEN bit is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 2800h

Bit Range	Default and Access	Field Name (ID): Description
15	0h WO	**Initiate FLR (IF):** Used to initiate FLR transition. A write of 1 initiates FLR transition. Since hardware must not respond to any cycles until FLR completion, the read value by software from this bit is 0 .
14:12	2h RW	**Max Read Request Size (MRRS):** This field sets the maximum Read Request size for the Function as a Requester. The Function must not generate Read Requests with size exceeding the set value. Defined encodings for this field are: 000: 128 B 001: 256 B 010: 512 B 011: 1024 B 100: 2048 B 101: 4096 B 110 111: Reserved
11	1h RW	**Enable No Snoop (NSNPEN):** When set to 1 (or EM2.FNSNPEN = 1) the Intel HD Audio controller is permitted to set the No Snoop bit in the Requester Attributes of a bus Initiator transaction. In this case VC0, VCp, or VC1 may be used for isochronous transfers. When set to 0 (and EM2.FNSNPEN = 0) the Intel HD Audio controller will not set the No Snoop bit. In the case isochronous transfers will not use VC1(VCi) even if it is enabled since VC1 is never snooped. Isochronous transfers will use either VCp or VC0. This bit is not affected by D3HOT to D0 reset or FLR.
10	0h RO	**Auxiliary (AUX) Power PM Enable (AUXPEN):** Hardwired to 0 indicating Intel HD Audio device does not draw AUX power.
9	0h RO	**Phantom Functions Enable (PFEN):** Hardwired to 0 disabling phantom functions.
8	0h RO	**Extended Tag Field Enable (ETEN):** Hardwired to 0 enabling 5-bit tag.

Bit Range	Default and Access	Field Name (ID): Description
7:5	0h RO	**Max Payload Size (MAXPAY):** Hardwired to 000 indicating 128 B.
4	0h RO	**Enable Relaxed Ordering (ROEN):** Hardwired to 0 disabling relaxed ordering.
3	0h RW	**Unsupported Request Reporting Enable (URREN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
2	0h RW	**Fatal Error Reporting Enable (FEREN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
1	0h RW	**Non-Fatal Error Reporting Enable (NFEREN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
0	0h RW	**Correctable Error Reporting Enable (CEREN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.

14.1.35 Device Status (DEVS)—Offset 7Ah

This register provides information about PCI Express device (Function) specific parameters.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 10h

Bit Range	Default and Access	Field Name (ID): Description
15:6	0h RO	Reserved.
5	0h RO/V	**Transactions Pending (TXP):** A 1 indicates that the Intel HD Audio controller has issued Non-Posted requests which have not been completed. A 0 indicates that Completions for all Non-Posted Requests have been received.
4	1h RW/L	**AUX Power Detected (AUXDET):** Hardwired to 1 indicating the device is connected to Suspend power. Programmable by BIOS for the option to declare SUS well wake is supported or not: 1b (SUS well wake supported) or 0b (SUS well wake not supported). Locked when FNCFG.BCLD = 1.
3	0h RO	**Unsupported Request Detected (URDET):** Not implemented. Hardwired to 0.
2	0h RO	**Fatal Error Detected (FEDET):** Not implemented. Hardwired to 0.
1	0h RO	**Non-Fatal Error Detected (NFEDET):** Not implemented. Hardwired to 0.
0	0h RO	**Correctable Error Detected (CEDET):** Not implemented. Hardwired to 0.

14.2 High Definition Audio Memory Mapped I/O Registers Summary

Table 14-2. Summary of High Definition Audio Memory Mapped I/O Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	1h	Global Capabilities (GCAP)—Offset 0h	9701h
2h	2h	Minor Version (VMIN)—Offset 2h	0h
3h	3h	Major Version (VMAJ)—Offset 3h	1h
4h	5h	Output Payload Capability (OUTPAY)—Offset 4h	3Ch
6h	7h	Input Payload Capability (INPAY)—Offset 6h	1Dh
8h	Bh	Global Control (GCTL)—Offset 8h	0h
Ch	Dh	Wake Enable (WAKEEN)—Offset Ch	0h
Eh	Fh	Wake Status (WAKESTS)—Offset Eh	0h
10h	11h	Global Status (GSTS)—Offset 10h	0h
12h	13h	Global Capabilities 2 (GCAP2)—Offset 12h	1h
14h	15h	Linked List Capabilities Header (LLCH)—Offset 14h	C00h
18h	19h	Output Stream Payload Capability (OUTSTRMPAY)—Offset 18h	30h
1Ah	1Bh	Input Stream Payload Capability (INSTRMPAY)—Offset 1Ah	18h
20h	23h	Interrupt Control (INTCTL)—Offset 20h	0h
24h	27h	Interrupt Status (INTSTS)—Offset 24h	0h
30h	33h	Wall Clock Counter (WALCLK)—Offset 30h	0h
38h	3Bh	Stream Synchronization (SSYNC)—Offset 38h	0h
40h	43h	CORB Lower Base Address (CORBLBASE)—Offset 40h	0h
44h	47h	CORB Upper Base Address (CORBUBASE)—Offset 44h	0h
48h	49h	CORB Write Pointer (CORBWP)—Offset 48h	0h
4Ah	4Bh	CORB Read Pointer (CORBRP)—Offset 4Ah	0h
4Ch	4Ch	CORB Control (CORBCTL)—Offset 4Ch	0h
4Dh	4Dh	CORB Status (CORBSTS)—Offset 4Dh	0h
4Eh	4Eh	CORB Size (CORBSIZE)—Offset 4Eh	42h
50h	53h	RIRB Lower Base Address (RIRBLBASE)—Offset 50h	0h
54h	57h	RIRB Upper Base Address (RIRBUBASE)—Offset 54h	0h
58h	59h	RIRB Write Pointer (RIRBWP)—Offset 58h	0h
5Ah	5Bh	Response Interrupt Count (RINTCNT)—Offset 5Ah	0h
5Ch	5Ch	RIRB Control (RIRBCTL)—Offset 5Ch	0h
5Dh	5Dh	RIRB Status (RIRBSTS)—Offset 5Dh	0h
5Eh	5Eh	RIRB Size (RIRBSIZE)—Offset 5Eh	42h
60h	63h	Immediate Command (IC)—Offset 60h	0h
64h	67h	Immediate Response (IR)—Offset 64h	0h
68h	69h	Immediate Command Status (ICS)—Offset 68h	0h
70h	73h	DMA Position Lower Base Address (DPLBASE)—Offset 70h	0h
74h	77h	DMA Position Upper Base Address (DPUBASE)—Offset 74h	0h
80h	83h	Input/Output Stream Descriptor x Control (ISD0CTL)—Offset 80h	40000h

Table 14-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
83h	83h	Input/Output Stream Descriptor x Status (ISD0STS)—Offset 83h	0h
84h	87h	Input/Output Stream Descriptor x Link Position in Buffer (ISD0LPIB)—Offset 84h	0h
88h	8Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD0CBL)—Offset 88h	0h
8Ch	8Dh	Input/Output Stream Descriptor x Last Valid Index (ISD0LVI)—Offset 8Ch	0h
8Eh	8Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD0FIFOW)—Offset 8Eh	4h
90h	91h	Input/Output Stream Descriptor x FIFO Size (ISD0FIFOS)—Offset 90h	0h
92h	93h	Input/Output Stream Descriptor x Format (ISD0FMT)—Offset 92h	0h
94h	95h	Input/Output Stream Descriptor x FIFO Limit (ISD0FIFOL)—Offset 94h	0h
98h	9Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD0BDLPLBA)—Offset 98h	0h
9Ch	9Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD0BDLPUBA)—Offset 9Ch	0h
A0h	A0h	Input/Output Stream Descriptor x Control (ISD1CTLB0)—Offset A0h	0h
A0h	A3h	Input/Output Stream Descriptor x Control (ISD1CTL)—Offset A0h	0h
A2h	A2h	Input/Output Stream Descriptor x Control (ISD1CTLB2)—Offset A2h	0h
A3h	A3h	Input/Output Stream Descriptor x Status (ISD1STS)—Offset A3h	0h
A4h	A7h	Input/Output Stream Descriptor x Link Position in Buffer (ISD1LPIB)—Offset A4h	0h
A8h	ABh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD1CBL)—Offset A8h	0h
ACh	ADh	Input/Output Stream Descriptor x Last Valid Index (ISD1LVI)—Offset ACh	0h
AEh	AFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD1FIFOW)—Offset AEh	0h
B0h	B1h	Input/Output Stream Descriptor x FIFO Size (ISD1FIFOS)—Offset B0h	0h
B2h	B3h	Input/Output Stream Descriptor x Format (ISD1FMT)—Offset B2h	0h
B4h	B5h	Input/Output Stream Descriptor x FIFO Limit (ISD1FIFOL)—Offset B4h	0h
B8h	BBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD1BDLPLBA)—Offset B8h	0h
BCh	BFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD1BDLPUBA)—Offset BCh	0h
C0h	C3h	Input/Output Stream Descriptor x Control (ISD2CTL)—Offset C0h	0h
C3h	C3h	Input/Output Stream Descriptor x Status (ISD2STS)—Offset C3h	0h
C4h	C7h	Input/Output Stream Descriptor x Link Position in Buffer (ISD2LPIB)—Offset C4h	0h
C8h	CBh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD2CBL)—Offset C8h	0h
CCh	CDh	Input/Output Stream Descriptor x Last Valid Index (ISD2LVI)—Offset CCh	0h
CEh	CFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD2FIFOW)—Offset CEh	0h
D0h	D1h	Input/Output Stream Descriptor x FIFO Size (ISD2FIFOS)—Offset D0h	0h
D2h	D3h	Input/Output Stream Descriptor x Format (ISD2FMT)—Offset D2h	0h

Table 14-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
D4h	D5h	Input/Output Stream Descriptor x FIFO Limit (ISD2FIFOL)—Offset D4h	0h
D8h	DBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD2BDLPLBA)—Offset D8h	0h
DCh	DFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD2BDLPUBA)—Offset DCh	0h
E0h	E3h	Input/Output Stream Descriptor x Control (ISD3CTL)—Offset E0h	0h
E0h	E0h	Input/Output Stream Descriptor x Control (ISD3CTLB0)—Offset E0h	0h
E3h	E3h	Input/Output Stream Descriptor x Status (ISD3STS)—Offset E3h	0h
E4h	E7h	Input/Output Stream Descriptor x Link Position in Buffer (ISD3LPIB)—Offset E4h	0h
E8h	EBh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD3CBL)—Offset E8h	0h
ECh	EDh	Input/Output Stream Descriptor x Last Valid Index (ISD3LVI)—Offset ECh	0h
EEh	EFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD3FIFOW)—Offset EEh	0h
F0h	F1h	Input/Output Stream Descriptor x FIFO Size (ISD3FIFOS)—Offset F0h	0h
F2h	F3h	Input/Output Stream Descriptor x Format (ISD3FMT)—Offset F2h	0h
F4h	F5h	Input/Output Stream Descriptor x FIFO Limit (ISD3FIFOL)—Offset F4h	0h
F8h	FBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD3BDLPLBA)—Offset F8h	0h
FCh	FFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD3BDLPUBA)—Offset FCh	0h
100h	103h	Input/Output Stream Descriptor x Control (ISD4CTL)—Offset 100h	0h
103h	103h	Input/Output Stream Descriptor x Status (ISD4STS)—Offset 103h	0h
104h	107h	Input/Output Stream Descriptor x Link Position in Buffer (ISD4LPIB)—Offset 104h	0h
108h	10Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD4CBL)—Offset 108h	0h
10Ch	10Dh	Input/Output Stream Descriptor x Last Valid Index (ISD4LVI)—Offset 10Ch	0h
10Eh	10Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD4FIFOW)—Offset 10Eh	0h
110h	111h	Input/Output Stream Descriptor x FIFO Size (ISD4FIFOS)—Offset 110h	0h
112h	113h	Input/Output Stream Descriptor x Format (ISD4FMT)—Offset 112h	0h
114h	115h	Input/Output Stream Descriptor x FIFO Limit (ISD4FIFOL)—Offset 114h	0h
118h	11Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD4BDLPLBA)—Offset 118h	0h
11Ch	11Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD4BDLPUBA)—Offset 11Ch	0h
120h	123h	Input/Output Stream Descriptor x Control (ISD5CTL)—Offset 120h	0h
123h	123h	Input/Output Stream Descriptor x Status (ISD5STS)—Offset 123h	0h
124h	127h	Input/Output Stream Descriptor x Link Position in Buffer (ISD5LPIB)—Offset 124h	0h
128h	12Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD5CBL)—Offset 128h	0h

Table 14-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
12Ch	12Dh	Input/Output Stream Descriptor x Last Valid Index (ISD5LVI)—Offset 12Ch	0h
12Eh	12Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD5FIFOW)—Offset 12Eh	0h
130h	131h	Input/Output Stream Descriptor x FIFO Size (ISD5FIFOS)—Offset 130h	0h
132h	133h	Input/Output Stream Descriptor x Format (ISD5FMT)—Offset 132h	0h
134h	135h	Input/Output Stream Descriptor x FIFO Limit (ISD5FIFOL)—Offset 134h	0h
138h	13Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD5BDLPLBA)—Offset 138h	0h
13Ch	13Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD5BDLPUBA)—Offset 13Ch	0h
140h	143h	Input/Output Stream Descriptor x Control (ISD6CTL)—Offset 140h	0h
143h	143h	Input/Output Stream Descriptor x Status (ISD6STS)—Offset 143h	0h
144h	147h	Input/Output Stream Descriptor x Link Position in Buffer (ISD6LPIB)—Offset 144h	0h
148h	14Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD6CBL)—Offset 148h	0h
14Ch	14Dh	Input/Output Stream Descriptor x Last Valid Index (ISD6LVI)—Offset 14Ch	0h
14Eh	14Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD6FIFOW)—Offset 14Eh	0h
150h	151h	Input/Output Stream Descriptor x FIFO Size (ISD6FIFOS)—Offset 150h	0h
152h	153h	Input/Output Stream Descriptor x Format (ISD6FMT)—Offset 152h	0h
154h	155h	Input/Output Stream Descriptor x FIFO Limit (ISD6FIFOL)—Offset 154h	0h
158h	15Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD6BDLPLBA)—Offset 158h	0h
15Ch	15Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD6BDLPUBA)—Offset 15Ch	0h
180h	183h	Input/Output Stream Descriptor x Control (OSD1CTL)—Offset 180h	0h
183h	183h	Input/Output Stream Descriptor x Status (OSD1STS)—Offset 183h	0h
184h	187h	Input/Output Stream Descriptor x Link Position in Buffer (OSD1LPIB)—Offset 184h	0h
188h	18Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD1CBL)—Offset 188h	0h
18Ch	18Dh	Input/Output Stream Descriptor x Last Valid Index (OSD1LVI)—Offset 18Ch	0h
18Eh	18Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD1FIFOW)—Offset 18Eh	0h
190h	191h	Input/Output Stream Descriptor x FIFO Size (OSD1FIFOS)—Offset 190h	0h
192h	193h	Input/Output Stream Descriptor x Format (OSD1FMT)—Offset 192h	0h
194h	195h	Input/Output Stream Descriptor x FIFO Limit (OSD1FIFOL)—Offset 194h	0h
198h	19Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD1BDLPLBA)—Offset 198h	0h
19Ch	19Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD1BDLPUBA)—Offset 19Ch	0h
1A0h	1A3h	Input/Output Stream Descriptor x Control (OSD2CTL)—Offset 1A0h	0h
1A3h	1A3h	Input/Output Stream Descriptor x Status (OSD2STS)—Offset 1A3h	0h

Table 14-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1A4h	1A7h	Input/Output Stream Descriptor x Link Position in Buffer (OSD2LPIB)—Offset 1A4h	0h
1A8h	1ABh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD2CBL)—Offset 1A8h	0h
1ACh	1ADh	Input/Output Stream Descriptor x Last Valid Index (OSD2LVI)—Offset 1ACh	0h
1AEh	1AFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD2FIFOW)—Offset 1AEh	0h
1B0h	1B1h	Input/Output Stream Descriptor x FIFO Size (OSD2FIFOS)—Offset 1B0h	0h
1B2h	1B3h	Input/Output Stream Descriptor x Format (OSD2FMT)—Offset 1B2h	0h
1B4h	1B5h	Input/Output Stream Descriptor x FIFO Limit (OSD2FIFOL)—Offset 1B4h	0h
1B8h	1BBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD2BDLPLBA)—Offset 1B8h	0h
1BCh	1BFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD2BDLPUBA)—Offset 1BCh	0h
1C0h	1C0h	Input/Output Stream Descriptor x Control (OSD3CTLB0)—Offset 1C0h	0h
1C0h	1C3h	Input/Output Stream Descriptor x Control (OSD3CTL)—Offset 1C0h	0h
1C2h	1C2h	Input/Output Stream Descriptor x Control (OSD3CTLB2)—Offset 1C2h	0h
1C3h	1C3h	Input/Output Stream Descriptor x Status (OSD3STS)—Offset 1C3h	0h
1C4h	1C7h	Input/Output Stream Descriptor x Link Position in Buffer (OSD3LPIB)—Offset 1C4h	0h
1C8h	1CBh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD3CBL)—Offset 1C8h	0h
1CCh	1CDh	Input/Output Stream Descriptor x Last Valid Index (OSD3LVI)—Offset 1CCh	0h
1CEh	1CFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD3FIFOW)—Offset 1CEh	0h
1D0h	1D1h	Input/Output Stream Descriptor x FIFO Size (OSD3FIFOS)—Offset 1D0h	0h
1D2h	1D3h	Input/Output Stream Descriptor x Format (OSD3FMT)—Offset 1D2h	0h
1D4h	1D5h	Input/Output Stream Descriptor x FIFO Limit (OSD3FIFOL)—Offset 1D4h	0h
1D8h	1DBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD3BDLPLBA)—Offset 1D8h	0h
1DCh	1DFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD3BDLPUBA)—Offset 1DCh	0h
1E0h	1E3h	Input/Output Stream Descriptor x Control (OSD4CTL)—Offset 1E0h	0h
1E3h	1E3h	Input/Output Stream Descriptor x Status (OSD4STS)—Offset 1E3h	0h
1E4h	1E7h	Input/Output Stream Descriptor x Link Position in Buffer (OSD4LPIB)—Offset 1E4h	0h
1E8h	1EBh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD4CBL)—Offset 1E8h	0h
1ECh	1EDh	Input/Output Stream Descriptor x Last Valid Index (OSD4LVI)—Offset 1ECh	0h
1EEh	1EFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD4FIFOW)—Offset 1EEh	0h
1F0h	1F1h	Input/Output Stream Descriptor x FIFO Size (OSD4FIFOS)—Offset 1F0h	0h
1F2h	1F3h	Input/Output Stream Descriptor x Format (OSD4FMT)—Offset 1F2h	0h
1F4h	1F5h	Input/Output Stream Descriptor x FIFO Limit (OSD4FIFOL)—Offset 1F4h	0h

Table 14-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1F8h	1FBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD4BDLPLBA)—Offset 1F8h	0h
1FCh	1FFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD4BDLPUBA)—Offset 1FCh	0h
200h	203h	Input/Output Stream Descriptor x Control (OSD5CTL)—Offset 200h	0h
203h	203h	Input/Output Stream Descriptor x Status (OSD5STS)—Offset 203h	0h
204h	207h	Input/Output Stream Descriptor x Link Position in Buffer (OSD5LPIB)—Offset 204h	0h
208h	20Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD5CBL)—Offset 208h	0h
20Ch	20Dh	Input/Output Stream Descriptor x Last Valid Index (OSD5LVI)—Offset 20Ch	0h
20Eh	20Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD5FIFOW)—Offset 20Eh	0h
210h	211h	Input/Output Stream Descriptor x FIFO Size (OSD5FIFOS)—Offset 210h	0h
212h	213h	Input/Output Stream Descriptor x Format (OSD5FMT)—Offset 212h	0h
214h	215h	Input/Output Stream Descriptor x FIFO Limit (OSD5FIFOL)—Offset 214h	0h
218h	21Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD5BDLPLBA)—Offset 218h	0h
21Ch	21Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD5BDLPUBA)—Offset 21Ch	0h
220h	223h	Input/Output Stream Descriptor x Control (OSD6CTL)—Offset 220h	0h
223h	223h	Input/Output Stream Descriptor x Status (OSD6STS)—Offset 223h	0h
224h	227h	Input/Output Stream Descriptor x Link Position in Buffer (OSD6LPIB)—Offset 224h	0h
228h	22Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD6CBL)—Offset 228h	0h
22Ch	22Dh	Input/Output Stream Descriptor x Last Valid Index (OSD6LVI)—Offset 22Ch	0h
22Eh	22Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD6FIFOW)—Offset 22Eh	0h
230h	231h	Input/Output Stream Descriptor x FIFO Size (OSD6FIFOS)—Offset 230h	0h
232h	233h	Input/Output Stream Descriptor x Format (OSD6FMT)—Offset 232h	0h
234h	235h	Input/Output Stream Descriptor x FIFO Limit (OSD6FIFOL)—Offset 234h	0h
238h	23Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD6BDLPLBA)—Offset 238h	0h
23Ch	23Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD6BDLPUBA)—Offset 23Ch	0h
240h	240h	Input/Output Stream Descriptor x Control (OSD7CTLB0)—Offset 240h	0h
240h	243h	Input/Output Stream Descriptor x Control (OSD7CTL)—Offset 240h	0h
242h	242h	Input/Output Stream Descriptor x Control (OSD7CTLB2)—Offset 242h	0h
243h	243h	Input/Output Stream Descriptor x Status (OSD7STS)—Offset 243h	0h
244h	247h	Input/Output Stream Descriptor x Link Position in Buffer (OSD7LPIB)—Offset 244h	0h
248h	24Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD7CBL)—Offset 248h	0h

Table 14-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
24Ch	24Dh	Input/Output Stream Descriptor x Last Valid Index (OSD7LVI)—Offset 24Ch	0h
24Eh	24Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD7FIFOW)—Offset 24Eh	0h
250h	251h	Input/Output Stream Descriptor x FIFO Size (OSD7FIFOS)—Offset 250h	0h
252h	253h	Input/Output Stream Descriptor x Format (OSD7FMT)—Offset 252h	0h
254h	255h	Input/Output Stream Descriptor x FIFO Limit (OSD7FIFOL)—Offset 254h	0h
258h	25Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD7BDLPLBA)—Offset 258h	0h
25Ch	25Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD7BDLPUBA)—Offset 25Ch	0h
260h	263h	Input/Output Stream Descriptor x Control (OSD8CTL)—Offset 260h	0h
263h	263h	Input/Output Stream Descriptor x Status (OSD8STS)—Offset 263h	0h
264h	267h	Input/Output Stream Descriptor x Link Position in Buffer (OSD8LPIB)—Offset 264h	0h
268h	26Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD8CBL)—Offset 268h	0h
26Ch	26Dh	Input/Output Stream Descriptor x Last Valid Index (OSD8LVI)—Offset 26Ch	0h
26Eh	26Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD8FIFOW)—Offset 26Eh	0h
270h	271h	Input/Output Stream Descriptor x FIFO Size (OSD8FIFOS)—Offset 270h	0h
272h	273h	Input/Output Stream Descriptor x Format (OSD8FMT)—Offset 272h	0h
274h	275h	Input/Output Stream Descriptor x FIFO Limit (OSD8FIFOL)—Offset 274h	0h
278h	27Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD8BDLPLBA)—Offset 278h	0h
27Ch	27Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD8BDLPUBA)—Offset 27Ch	0h
280h	283h	Input/Output Stream Descriptor x Control (ISD7CTL)—Offset 280h	0h
283h	283h	Input/Output Stream Descriptor x Status (ISD7STS)—Offset 283h	0h
284h	287h	Input/Output Stream Descriptor x Link Position in Buffer (ISD7LPIB)—Offset 284h	0h
288h	28Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD7CBL)—Offset 288h	0h
28Ch	28Dh	Input/Output Stream Descriptor x Last Valid Index (ISD7LVI)—Offset 28Ch	0h
28Eh	28Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD7FIFOW)—Offset 28Eh	0h
290h	291h	Input/Output Stream Descriptor x FIFO Size (ISD7FIFOS)—Offset 290h	0h
292h	293h	Input/Output Stream Descriptor x Format (ISD7FMT)—Offset 292h	0h
294h	295h	Input/Output Stream Descriptor x FIFO Limit (ISD7FIFOL)—Offset 294h	0h
298h	29Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD7BDLPLBA)—Offset 298h	0h
29Ch	29Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD7BDLPUBA)—Offset 29Ch	0h
2A0h	2A3h	Input/Output Stream Descriptor x Control (ISD8CTL)—Offset 2A0h	0h
2A3h	2A3h	Input/Output Stream Descriptor x Status (ISD8STS)—Offset 2A3h	0h

Table 14-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
2A4h	2A7h	Input/Output Stream Descriptor x Link Position in Buffer (ISD8LPIB)—Offset 2A4h	0h
2A8h	2ABh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD8CBL)—Offset 2A8h	0h
2ACh	2ADh	Input/Output Stream Descriptor x Last Valid Index (ISD8LVI)—Offset 2ACh	0h
2AEh	2AFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD8FIFOW)—Offset 2AEh	0h
2B0h	2B1h	Input/Output Stream Descriptor x FIFO Size (ISD8FIFOS)—Offset 2B0h	0h
2B2h	2B3h	Input/Output Stream Descriptor x Format (ISD8FMT)—Offset 2B2h	0h
2B4h	2B5h	Input/Output Stream Descriptor x FIFO Limit (ISD8FIFOL)—Offset 2B4h	0h
2B8h	2BBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD8BDLPLBA)—Offset 2B8h	0h
2BCh	2BFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD8BDLPUBA)—Offset 2BCh	0h
2C0h	2C3h	Input/Output Stream Descriptor x Control (ISD9CTL)—Offset 2C0h	0h
2C3h	2C3h	Input/Output Stream Descriptor x Status (ISD9STS)—Offset 2C3h	0h
2C4h	2C7h	Input/Output Stream Descriptor x Link Position in Buffer (ISD9LPIB)—Offset 2C4h	0h
2C8h	2CBh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD9CBL)—Offset 2C8h	0h
2CCh	2CDh	Input/Output Stream Descriptor x Last Valid Index (ISD9LVI)—Offset 2CCh	0h
2CEh	2CFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD9FIFOW)—Offset 2CEh	0h
2D0h	2D1h	Input/Output Stream Descriptor x FIFO Size (ISD9FIFOS)—Offset 2D0h	0h
2D2h	2D3h	Input/Output Stream Descriptor x Format (ISD9FMT)—Offset 2D2h	0h
2D4h	2D5h	Input/Output Stream Descriptor x FIFO Limit (ISD9FIFOL)—Offset 2D4h	0h
2D8h	2DBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD9BDLPLBA)—Offset 2D8h	0h
2DCh	2DFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD9BDLPUBA)—Offset 2DCh	0h
2E0h	2E3h	Input/Output Stream Descriptor x Control (ISD10CTL)—Offset 2E0h	0h
2E3h	2E3h	Input/Output Stream Descriptor x Status (ISD10STS)—Offset 2E3h	0h
2E4h	2E7h	Input/Output Stream Descriptor x Link Position in Buffer (ISD10LPIB)—Offset 2E4h	0h
2E8h	2EBh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD10CBL)—Offset 2E8h	0h
2ECh	2EDh	Input/Output Stream Descriptor x Last Valid Index (ISD10LVI)—Offset 2ECh	0h
2EEh	2EFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD10FIFOW)—Offset 2EEh	0h
2F0h	2F1h	Input/Output Stream Descriptor x FIFO Size (ISD10FIFOS)—Offset 2F0h	0h
2F2h	2F3h	Input/Output Stream Descriptor x Format (ISD10FMT)—Offset 2F2h	0h
2F4h	2F5h	Input/Output Stream Descriptor x FIFO Limit (ISD10FIFOL)—Offset 2F4h	0h
2F8h	2FBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD10BDLPLBA)—Offset 2F8h	0h

Table 14-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
2FCh	2FFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD10BDLPUBA)—Offset 2FCh	0h
300h	303h	Input/Output Stream Descriptor x Control (ISD11CTL)—Offset 300h	0h
303h	303h	Input/Output Stream Descriptor x Status (ISD11STS)—Offset 303h	0h
304h	307h	Input/Output Stream Descriptor x Link Position in Buffer (ISD11LPIB)—Offset 304h	0h
308h	30Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD11CBL)—Offset 308h	0h
30Ch	30Dh	Input/Output Stream Descriptor x Last Valid Index (ISD11LVI)—Offset 30Ch	0h
30Eh	30Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD11FIFOW)—Offset 30Eh	0h
310h	311h	Input/Output Stream Descriptor x FIFO Size (ISD11FIFOS)—Offset 310h	0h
312h	313h	Input/Output Stream Descriptor x Format (ISD11FMT)—Offset 312h	0h
314h	315h	Input/Output Stream Descriptor x FIFO Limit (ISD11FIFOL)—Offset 314h	0h
318h	31Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD11BDLPLBA)—Offset 318h	0h
31Ch	31Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD11BDLPUBA)—Offset 31Ch	0h
320h	323h	Input/Output Stream Descriptor x Control (ISD12CTL)—Offset 320h	0h
323h	323h	Input/Output Stream Descriptor x Status (ISD12STS)—Offset 323h	0h
324h	327h	Input/Output Stream Descriptor x Link Position in Buffer (ISD12LPIB)—Offset 324h	0h
328h	32Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD12CBL)—Offset 328h	0h
32Ch	32Dh	Input/Output Stream Descriptor x Last Valid Index (ISD12LVI)—Offset 32Ch	0h
32Eh	32Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD12FIFOW)—Offset 32Eh	0h
330h	331h	Input/Output Stream Descriptor x FIFO Size (ISD12FIFOS)—Offset 330h	0h
332h	333h	Input/Output Stream Descriptor x Format (ISD12FMT)—Offset 332h	0h
334h	335h	Input/Output Stream Descriptor x FIFO Limit (ISD12FIFOL)—Offset 334h	0h
338h	33Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD12BDLPLBA)—Offset 338h	0h
33Ch	33Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD12BDLPUBA)—Offset 33Ch	0h
340h	343h	Input/Output Stream Descriptor x Control (ISD13CTL)—Offset 340h	0h
343h	343h	Input/Output Stream Descriptor x Status (ISD13STS)—Offset 343h	0h
344h	347h	Input/Output Stream Descriptor x Link Position in Buffer (ISD13LPIB)—Offset 344h	0h
348h	34Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD13CBL)—Offset 348h	0h
34Ch	34Dh	Input/Output Stream Descriptor x Last Valid Index (ISD13LVI)—Offset 34Ch	0h
34Eh	34Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD13FIFOW)—Offset 34Eh	0h
350h	351h	Input/Output Stream Descriptor x FIFO Size (ISD13FIFOS)—Offset 350h	0h

Table 14-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
352h	353h	Input/Output Stream Descriptor x Format (ISD13FMT)—Offset 352h	0h
354h	355h	Input/Output Stream Descriptor x FIFO Limit (ISD13FIFOL)—Offset 354h	0h
358h	35Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD13BDLPLBA)—Offset 358h	0h
35Ch	35Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD13BDLPUBA)—Offset 35Ch	0h
360h	363h	Input/Output Stream Descriptor x Control (ISD14CTL)—Offset 360h	0h
363h	363h	Input/Output Stream Descriptor x Status (ISD14STS)—Offset 363h	0h
364h	367h	Input/Output Stream Descriptor x Link Position in Buffer (ISD14LPIB)—Offset 364h	0h
368h	36Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD14CBL)—Offset 368h	0h
36Ch	36Dh	Input/Output Stream Descriptor x Last Valid Index (ISD14LVI)—Offset 36Ch	0h
36Eh	36Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD14FIFOW)—Offset 36Eh	0h
370h	371h	Input/Output Stream Descriptor x FIFO Size (ISD14FIFOS)—Offset 370h	0h
372h	373h	Input/Output Stream Descriptor x Format (ISD14FMT)—Offset 372h	0h
374h	375h	Input/Output Stream Descriptor x FIFO Limit (ISD14FIFOL)—Offset 374h	0h
378h	37Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD14BDLPLBA)—Offset 378h	0h
37Ch	37Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD14BDLPUBA)—Offset 37Ch	0h
380h	383h	Input/Output Stream Descriptor x Control (OSD9CTL)—Offset 380h	0h
383h	383h	Input/Output Stream Descriptor x Status (OSD9STS)—Offset 383h	0h
384h	387h	Input/Output Stream Descriptor x Link Position in Buffer (OSD9LPIB)—Offset 384h	0h
388h	38Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD9CBL)—Offset 388h	0h
38Ch	38Dh	Input/Output Stream Descriptor x Last Valid Index (OSD9LVI)—Offset 38Ch	0h
38Eh	38Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD9FIFOW)—Offset 38Eh	0h
390h	391h	Input/Output Stream Descriptor x FIFO Size (OSD9FIFOS)—Offset 390h	0h
392h	393h	Input/Output Stream Descriptor x Format (OSD9FMT)—Offset 392h	0h
394h	395h	Input/Output Stream Descriptor x FIFO Limit (OSD9FIFOL)—Offset 394h	0h
398h	39Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD9BDLPLBA)—Offset 398h	0h
39Ch	39Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD9BDLPUBA)—Offset 39Ch	0h
3A0h	3A3h	Input/Output Stream Descriptor x Control (OSD10CTL)—Offset 3A0h	0h
3A3h	3A3h	Input/Output Stream Descriptor x Status (OSD10STS)—Offset 3A3h	0h
3A4h	3A7h	Input/Output Stream Descriptor x Link Position in Buffer (OSD10LPIB)—Offset 3A4h	0h
3A8h	3ABh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD10CBL)—Offset 3A8h	0h

Table 14-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3ACh	3ADh	Input/Output Stream Descriptor x Last Valid Index (OSD10LVI)—Offset 3ACh	0h
3AEh	3AFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD10FIFOW)—Offset 3AEh	0h
3B0h	3B1h	Input/Output Stream Descriptor x FIFO Size (OSD10FIFOS)—Offset 3B0h	0h
3B2h	3B3h	Input/Output Stream Descriptor x Format (OSD10FMT)—Offset 3B2h	0h
3B4h	3B5h	Input/Output Stream Descriptor x FIFO Limit (OSD10FIFOL)—Offset 3B4h	0h
3B8h	3BBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD10BDLPLBA)—Offset 3B8h	0h
3BCh	3BFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD10BDLPUBA)—Offset 3BCh	0h
3C0h	3C3h	Input/Output Stream Descriptor x Control (OSD11CTL)—Offset 3C0h	0h
3C3h	3C3h	Input/Output Stream Descriptor x Status (OSD11STS)—Offset 3C3h	0h
3C4h	3C7h	Input/Output Stream Descriptor x Link Position in Buffer (OSD11LPIB)—Offset 3C4h	0h
3C8h	3CBh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD11CBL)—Offset 3C8h	0h
3CCh	3CDh	Input/Output Stream Descriptor x Last Valid Index (OSD11LVI)—Offset 3CCh	0h
3CEh	3CFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD11FIFOW)—Offset 3CEh	0h
3D0h	3D1h	Input/Output Stream Descriptor x FIFO Size (OSD11FIFOS)—Offset 3D0h	0h
3D2h	3D3h	Input/Output Stream Descriptor x Format (OSD11FMT)—Offset 3D2h	0h
3D4h	3D5h	Input/Output Stream Descriptor x FIFO Limit (OSD11FIFOL)—Offset 3D4h	0h
3D8h	3DBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD11BDLPLBA)—Offset 3D8h	0h
3DCh	3DFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD11BDLPUBA)—Offset 3DCh	0h
3E0h	3E3h	Input/Output Stream Descriptor x Control (OSD12CTL)—Offset 3E0h	0h
3E3h	3E3h	Input/Output Stream Descriptor x Status (OSD12STS)—Offset 3E3h	0h
3E4h	3E7h	Input/Output Stream Descriptor x Link Position in Buffer (OSD12LPIB)—Offset 3E4h	0h
3E8h	3EBh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD12CBL)—Offset 3E8h	0h
3ECh	3EDh	Input/Output Stream Descriptor x Last Valid Index (OSD12LVI)—Offset 3ECh	0h
3EEh	3EFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD12FIFOW)—Offset 3EEh	0h
3F0h	3F1h	Input/Output Stream Descriptor x FIFO Size (OSD12FIFOS)—Offset 3F0h	0h
3F2h	3F3h	Input/Output Stream Descriptor x Format (OSD12FMT)—Offset 3F2h	0h
3F4h	3F5h	Input/Output Stream Descriptor x FIFO Limit (OSD12FIFOL)—Offset 3F4h	0h
3F8h	3FBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD12BDLPLBA)—Offset 3F8h	0h

Table 14-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3FCh	3FFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD12BDLPUBA)—Offset 3FCh	0h
400h	403h	Input/Output Stream Descriptor x Control (OSD13CTL)—Offset 400h	0h
403h	403h	Input/Output Stream Descriptor x Status (OSD13STS)—Offset 403h	0h
404h	407h	Input/Output Stream Descriptor x Link Position in Buffer (OSD13LPIB)—Offset 404h	0h
408h	40Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD13CBL)—Offset 408h	0h
40Ch	40Dh	Input/Output Stream Descriptor x Last Valid Index (OSD13LVI)—Offset 40Ch	0h
40Eh	40Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD13FIFOW)—Offset 40Eh	0h
410h	411h	Input/Output Stream Descriptor x FIFO Size (OSD13FIFOS)—Offset 410h	0h
412h	413h	Input/Output Stream Descriptor x Format (OSD13FMT)—Offset 412h	0h
414h	415h	Input/Output Stream Descriptor x FIFO Limit (OSD13FIFOL)—Offset 414h	0h
418h	41Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD13BDLPLBA)—Offset 418h	0h
41Ch	41Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD13BDLPUBA)—Offset 41Ch	0h
420h	423h	Input/Output Stream Descriptor x Control (OSD14CTL)—Offset 420h	0h
423h	423h	Input/Output Stream Descriptor x Status (OSD14STS)—Offset 423h	0h
424h	427h	Input/Output Stream Descriptor x Link Position in Buffer (OSD14LPIB)—Offset 424h	0h
428h	42Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD14CBL)—Offset 428h	0h
42Ch	42Dh	Input/Output Stream Descriptor x Last Valid Index (OSD14LVI)—Offset 42Ch	0h
42Eh	42Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD14FIFOW)—Offset 42Eh	0h
430h	431h	Input/Output Stream Descriptor x FIFO Size (OSD14FIFOS)—Offset 430h	0h
432h	433h	Input/Output Stream Descriptor x Format (OSD14FMT)—Offset 432h	0h
434h	435h	Input/Output Stream Descriptor x FIFO Limit (OSD14FIFOL)—Offset 434h	0h
438h	43Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD14BDLPLBA)—Offset 438h	0h
43Ch	43Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD14BDLPUBA)—Offset 43Ch	0h
500h	503h	Global Time Synchronization Capability Header (GTSCH)—Offset 500h	11F00h
504h	507h	Global Time Synchronization Capability Declaration (GTSCD)—Offset 504h	0h
520h	523h	Global Time Synchronization Capture Control (GTSCC0)—Offset 520h	0h
524h	527h	Wall Frame Counter Captured (WALFCC0)—Offset 524h	0h
528h	52Bh	Time Stamp Counter Captured Lower (TSCCL0)—Offset 528h	0h
52Ch	52Fh	Time Stamp Counter Captured Upper (TSCCU0)—Offset 52Ch	0h
534h	537h	Linear Link Position Frame Offset Captured (LLPFOC0)—Offset 534h	0h
538h	53Bh	Linear Link Position Captured Lower (LLPCL0)—Offset 538h	0h

Table 14-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
53Ch	53Fh	Linear Link Position Captured Upper (LLPCU0)—Offset 53Ch	0h
540h	543h	Global Time Synchronization Capture Control (GTSCC1)—Offset 540h	0h
544h	547h	Wall Frame Counter Captured (WALFCC1)—Offset 544h	0h
548h	54Bh	Time Stamp Counter Captured Lower (TSCCL1)—Offset 548h	0h
54Ch	54Fh	Time Stamp Counter Captured Upper (TSCCU1)—Offset 54Ch	0h
554h	557h	Linear Link Position Frame Offset Captured (LLPFOC1)—Offset 554h	0h
558h	55Bh	Linear Link Position Captured Lower (LLPCL1)—Offset 558h	0h
55Ch	55Fh	Linear Link Position Captured Upper (LLPCU1)—Offset 55Ch	0h
800h	803h	Processing Pipe Capability Header (PPCH)—Offset 800h	30500h
804h	807h	Processing Pipe Control (PPCTL)—Offset 804h	0h
808h	80Bh	Processing Pipe Status (PPSTS)—Offset 808h	0h
810h	813h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC0LLPL)—Offset 810h	0h
814h	817h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC0LLPU)—Offset 814h	0h
818h	81Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC0LDPL)—Offset 818h	0h
81Ch	81Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC0LDPU)—Offset 81Ch	0h
910h	913h	Input/Output Processing Pipe's Link Connection x Control (IPPLC0CTL)—Offset 910h	0h
914h	915h	Input/Output Processing Pipe's Link Connection x Format (IPPLC0FMT)—Offset 914h	0h
918h	91Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC0LLPL)—Offset 918h	0h
91Ch	91Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC0LLPU)—Offset 91Ch	0h
C00h	C03h	Multiple Links Capability Header (MLCH)—Offset C00h	20800h
C04h	C07h	Multiple Links Capability Declaration (MLCD)—Offset C04h	1h
C40h	C43h	Link 0 Capabilities (LCAP0)—Offset C40h	7h
C44h	C47h	Link Control 0 (LCTL0)—Offset C44h	10002h
C48h	C4Bh	Link 0 Output Stream ID Mapping Valid (LOSIDV0)—Offset C48h	FFFEh
C4Ch	C4Fh	Link 0 SDI Identifier (LSDIID0)—Offset C4Ch	3h
C50h	C50h	Link 0 Per Stream Output Overhead (LPSOO0)—Offset C50h	0h
C52h	C52h	Link 0 Per Stream Input Overhead (LPSIO0)—Offset C52h	0h
C58h	C5Bh	Link 0 Wall Frame Counter (LWALFC0)—Offset C58h	0h
C80h	C83h	Link 1 Capabilities (LCAP1)—Offset C80h	1Fh
C84h	C87h	Link 1 Control (LCTL1)—Offset C84h	10004h
C88h	C8Bh	Link 1 Output Stream ID Mapping Valid (LOSIDV1)—Offset C88h	FFFEh
C8Ch	C8Fh	Link 1 SDI Identifier (LSDIID1)—Offset C8Ch	4h
C90h	C90h	Link 1 Per Stream Output Overhead (LPSOO1)—Offset C90h	0h
C92h	C92h	Link 1 Per Stream Input Overhead (LPSIO1)—Offset C92h	0h
C98h	C9Bh	Link 1 Wall Frame Counter (LWALFC1)—Offset C98h	0h

Table 14-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4A10h	4A13h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC7LLPL)—Offset 4A10h	0h
4A14h	4A17h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC7LLPU)—Offset 4A14h	0h
4A18h	4A1Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC7LDPL)—Offset 4A18h	0h
4A1Ch	4A1Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC7LDPU)—Offset 4A1Ch	0h
4A20h	4A23h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC8LLPL)—Offset 4A20h	0h
4A24h	4A27h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC8LLPU)—Offset 4A24h	0h
4A28h	4A2Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC8LDPL)—Offset 4A28h	0h
4A2Ch	4A2Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC8LDPU)—Offset 4A2Ch	0h
4A30h	4A33h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC9LLPL)—Offset 4A30h	0h
4A34h	4A37h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC9LLPU)—Offset 4A34h	0h
4A38h	4A3Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC9LDPL)—Offset 4A38h	0h
4A3Ch	4A3Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC9LDPU)—Offset 4A3Ch	0h
4A40h	4A43h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC10LLPL)—Offset 4A40h	0h
4A44h	4A47h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC10LLPU)—Offset 4A44h	0h
4A48h	4A4Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC10LDPL)—Offset 4A48h	0h
4A4Ch	4A4Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC10LDPU)—Offset 4A4Ch	0h
4A50h	4A53h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC11LLPL)—Offset 4A50h	0h
4A54h	4A57h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC11LLPU)—Offset 4A54h	0h
4A58h	4A5Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC11LDPL)—Offset 4A58h	0h
4A5Ch	4A5Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC11LDPU)—Offset 4A5Ch	0h
4A60h	4A63h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC12LLPL)—Offset 4A60h	0h
4A64h	4A67h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC12LLPU)—Offset 4A64h	0h
4A68h	4A6Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC12LDPL)—Offset 4A68h	0h
4A6Ch	4A6Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC12LDPU)—Offset 4A6Ch	0h
4A70h	4A73h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC13LLPL)—Offset 4A70h	0h

Table 14-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4A74h	4A77h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC13LLPU)—Offset 4A74h	0h
4A78h	4A7Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC13LDPL)—Offset 4A78h	0h
4A7Ch	4A7Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC13LDPU)—Offset 4A7Ch	0h
4A80h	4A83h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC14LLPL)—Offset 4A80h	0h
4A84h	4A87h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC14LLPU)—Offset 4A84h	0h
4A88h	4A8Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC14LDPL)—Offset 4A88h	0h
4A8Ch	4A8Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC14LDPU)—Offset 4A8Ch	0h
4A90h	4A93h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC9LLPL)—Offset 4A90h	0h
4A94h	4A97h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC9LLPU)—Offset 4A94h	0h
4A98h	4A9Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC9LDPL)—Offset 4A98h	0h
4A9Ch	4A9Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC9LDPU)—Offset 4A9Ch	0h
4AA0h	4AA3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC10LLPL)—Offset 4AA0h	0h
4AA4h	4AA7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC10LLPU)—Offset 4AA4h	0h
4AA8h	4AABh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC10LDPL)—Offset 4AA8h	0h
4AACh	4AAFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC10LDPU)—Offset 4AACh	0h
4AB0h	4AB3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC11LLPL)—Offset 4AB0h	0h
4AB4h	4AB7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC11LLPU)—Offset 4AB4h	0h
4AB8h	4ABBh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC11LDPL)—Offset 4AB8h	0h
4ABCh	4ABFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC11LDPU)—Offset 4ABCh	0h
4AC0h	4AC3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC12LLPL)—Offset 4AC0h	0h
4AC4h	4AC7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC12LLPU)—Offset 4AC4h	0h
4AC8h	4ACBh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC12LDPL)—Offset 4AC8h	0h
4ACCh	4ACFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC12LDPU)—Offset 4ACCh	0h
4AD0h	4AD3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC13LLPL)—Offset 4AD0h	0h
4AD4h	4AD7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC13LLPU)—Offset 4AD4h	0h

Table 14-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4AD8h	4ADBh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC13LDPL)—Offset 4AD8h	0h
4ADCh	4ADFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC13LDPU)—Offset 4ADCh	0h
4AE0h	4AE3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC14LLPL)—Offset 4AE0h	0h
4AE4h	4AE7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC14LLPU)—Offset 4AE4h	0h
4AE8h	4AEBh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC14LDPL)—Offset 4AE8h	0h
4AECh	4AEFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC14LDPU)—Offset 4AECh	0h
4AF0h	4AF3h	Input/Output Processing Pipe's Link Connection x Control (IPPLC7CTL)—Offset 4AF0h	0h
4AF4h	4AF5h	Input/Output Processing Pipe's Link Connection x Format (IPPLC7FMT)—Offset 4AF4h	0h
4AF8h	4AFBh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC7LLPL)—Offset 4AF8h	0h
4AFCh	4AFFh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC7LLPU)—Offset 4AFCh	0h
4B00h	4B03h	Input/Output Processing Pipe's Link Connection x Control (IPPLC8CTL)—Offset 4B00h	0h
4B04h	4B05h	Input/Output Processing Pipe's Link Connection x Format (IPPLC8FMT)—Offset 4B04h	0h
4B08h	4B0Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC8LLPL)—Offset 4B08h	0h
4B0Ch	4B0Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC8LLPU)—Offset 4B0Ch	0h
4B10h	4B13h	Input/Output Processing Pipe's Link Connection x Control (IPPLC9CTL)—Offset 4B10h	0h
4B14h	4B15h	Input/Output Processing Pipe's Link Connection x Format (IPPLC9FMT)—Offset 4B14h	0h
4B18h	4B1Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC9LLPL)—Offset 4B18h	0h
4B1Ch	4B1Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC9LLPU)—Offset 4B1Ch	0h
4B20h	4B23h	Input/Output Processing Pipe's Link Connection x Control (IPPLC10CTL)—Offset 4B20h	0h
4B24h	4B25h	Input/Output Processing Pipe's Link Connection x Format (IPPLC10FMT)—Offset 4B24h	0h
4B28h	4B2Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC10LLPL)—Offset 4B28h	0h
4B2Ch	4B2Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC10LLPU)—Offset 4B2Ch	0h
4B30h	4B33h	Input/Output Processing Pipe's Link Connection x Control (IPPLC11CTL)—Offset 4B30h	0h
4B34h	4B35h	Input/Output Processing Pipe's Link Connection x Format (IPPLC11FMT)—Offset 4B34h	0h
4B38h	4B3Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC11LLPL)—Offset 4B38h	0h

Table 14-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4B3Ch	4B3Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC11LLPU)—Offset 4B3Ch	0h
4B40h	4B43h	Input/Output Processing Pipe's Link Connection x Control (IPPLC12CTL)—Offset 4B40h	0h
4B44h	4B45h	Input/Output Processing Pipe's Link Connection x Format (IPPLC12FMT)—Offset 4B44h	0h
4B48h	4B4Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC12LLPL)—Offset 4B48h	0h
4B4Ch	4B4Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC12LLPU)—Offset 4B4Ch	0h
4B50h	4B53h	Input/Output Processing Pipe's Link Connection x Control (IPPLC13CTL)—Offset 4B50h	0h
4B54h	4B55h	Input/Output Processing Pipe's Link Connection x Format (IPPLC13FMT)—Offset 4B54h	0h
4B58h	4B5Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC13LLPL)—Offset 4B58h	0h
4B5Ch	4B5Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC13LLPU)—Offset 4B5Ch	0h
4B60h	4B63h	Input/Output Processing Pipe's Link Connection x Control (IPPLC14CTL)—Offset 4B60h	0h
4B64h	4B65h	Input/Output Processing Pipe's Link Connection x Format (IPPLC14FMT)—Offset 4B64h	0h
4B68h	4B6Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC14LLPL)—Offset 4B68h	0h
4B6Ch	4B6Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC14LLPU)—Offset 4B6Ch	0h
4B70h	4B73h	Input/Output Processing Pipe's Link Connection x Control (OPPLC9CTL)—Offset 4B70h	0h
4B74h	4B75h	Input/Output Processing Pipe's Link Connection x Format (OPPLC9FMT)—Offset 4B74h	0h
4B78h	4B7Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC9LLPL)—Offset 4B78h	0h
4B7Ch	4B7Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC9LLPU)—Offset 4B7Ch	0h
4B80h	4B83h	Input/Output Processing Pipe's Link Connection x Control (OPPLC10CTL)—Offset 4B80h	0h
4B84h	4B85h	Input/Output Processing Pipe's Link Connection x Format (OPPLC10FMT)—Offset 4B84h	0h
4B88h	4B8Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC10LLPL)—Offset 4B88h	0h
4B8Ch	4B8Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC10LLPU)—Offset 4B8Ch	0h
4B90h	4B93h	Input/Output Processing Pipe's Link Connection x Control (OPPLC11CTL)—Offset 4B90h	0h
4B94h	4B95h	Input/Output Processing Pipe's Link Connection x Format (OPPLC11FMT)—Offset 4B94h	0h
4B98h	4B9Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC11LLPL)—Offset 4B98h	0h
4B9Ch	4B9Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC11LLPU)—Offset 4B9Ch	0h

Table 14-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4BA0h	4BA3h	Input/Output Processing Pipe's Link Connection x Control (OPPLC12CTL)—Offset 4BA0h	0h
4BA4h	4BA5h	Input/Output Processing Pipe's Link Connection x Format (OPPLC12FMT)—Offset 4BA4h	0h
4BA8h	4BABh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC12LLPL)—Offset 4BA8h	0h
4BACh	4BAFh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC12LLPU)—Offset 4BACh	0h
4BB0h	4BB3h	Input/Output Processing Pipe's Link Connection x Control (OPPLC13CTL)—Offset 4BB0h	0h
4BB4h	4BB5h	Input/Output Processing Pipe's Link Connection x Format (OPPLC13FMT)—Offset 4BB4h	0h
4BB8h	4BBBh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC13LLPL)—Offset 4BB8h	0h
4BBCh	4BBFh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC13LLPU)—Offset 4BBCh	0h
4BC0h	4BC3h	Input/Output Processing Pipe's Link Connection x Control (OPPLC14CTL)—Offset 4BC0h	0h
4BC4h	4BC5h	Input/Output Processing Pipe's Link Connection x Format (OPPLC14FMT)—Offset 4BC4h	0h
4BC8h	4BCBh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC14LLPL)—Offset 4BC8h	0h
4BCCh	4BCFh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC14LLPU)—Offset 4BCCh	0h

14.2.1 Global Capabilities (GCAP)—Offset 0h

This register indicates the capabilities of the controller.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 9701h

Bit Range	Default and Access	Field Name (ID): Description
15:12	9h RW/L	**Number of Output Streams Supported (OSS):** 0100b indicates that the Intel HD Audio controller supports four output streams. Reset value is hardcoded to parameter HSTOSC. Locked when FNCFG.BCLD = 1.
11:8	7h RW/L	**Number of Input Streams Supported (ISS):** 0100b indicates that the Intel HD Audio controller supports four input streams. Reset value is hardcoded to parameter HSTISC. Locked when FNCFG.BCLD = 1.

Bit Range	Default and Access	Field Name (ID): Description
7:3	0h RO	**Number of Bidirectional Streams Supported (BSS):** 00000b indicates that the Intel HD Audio controller supports 0 bidirectional streams.
2:1	0h RW/L	**Number of Serial Data Out Signals (NSDO):** 00b indicates that the Intel HD Audio controller supports one Serial Data Output signal. For the case of multiple link segments is supported, this field indicates the number of SDO for link 0. Locked when FNCFG.BCLD = 1.
0	1h RW/L	**64 Bit Address Supported (ADD64OK):** A 1 indicates that the Intel HD Audio controller supports 64 bit addressing for BDL addresses, data buffer addresses, and command buffer addresses. Locked when FNCFG.BCLD = 1.

14.2.2 Minor Version (VMIN)—Offset 2h

This register indicates minor revision number of the High Definition Audio specification.

Access Method

Type: MEM Register (Size: 8 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW/L	**Minor Version (VMIN):** Indicates the Intel HD Audio controller supports minor revision number 00h of the Intel HD Audio specification.

14.2.3 Major Version (VMAJ)—Offset 3h

This register indicates major revision number of the High Definition Audio specification.

Access Method

Type: MEM Register (Size: 8 bits)
Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
7:0	1h RW/L	**Major Version (VMAJ):** Indicates the Intel HD Audio controller supports major revision number 1 of the Intel HD Audio specification.

14.2.4 Output Payload Capability (OUTPAY)—Offset 4h

This register indicates the total output payload available on the link.

Access Method

Type: MEM Register (Size: 16 bits)
Device:
Function:

Default: 3Ch

Bit Range	Default and Access	Field Name (ID): Description
15:0	3Ch RW/L	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. The default link clock speed of 24.000 MHz (the data is double pumped) provides 1000 bits per frame, or 62.5 words in total. 40 bits are used for command and control, leaving 60 words available for data payload. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Note: In the event that multiple links is supported (GCAP2.LCOUNT) 0), the payload advertised will be the lowest common denominator offered by the default clock frequency on each link. Locked when FNCFG.BCLD = 1.

14.2.5 Input Payload Capability (INPAY)—Offset 6h

This register indicates the total input payload available on the link.

Access Method

Type: MEM Register (Size: 16 bits)
Device:
Function:

Default: 1Dh

Bit Range	Default and Access	Field Name (ID): Description
15:0	1Dh RW/L	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link. This does not include bandwidth used for response. This measurement is in 16-bit word quantities per 48 kHz frame. The default link clock speed of 24.000 MHz provides 500 bits per frame, or 31.25 words in total. 36 bits are used for response, leaving 29 words for data payload. Note that this value does not reflect any bandwidth increase due to support for multiple SDI lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Note: In the event that multiple links is supported (GCAP2.LCOUNT) 0), the payload advertised will be the lowest common denominator offered by the default clock frequency on each link. Locked when FNCFG.BCLD = 1.

14.2.6 Global Control (GCTL)—Offset 8h

CRSTB bit is not affected by controller reset.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Accept Unsolicited Response Enable (UNSOL):** If UNSOL is a 1, Unsolicited Responses from the codecs are accepted by the controller and placed into the Response Input Ring Buffer. If UNSOL is a 0, unsolicited responses are not accepted, and dropped on the floor.
7:2	0h RO	Reserved.
1	0h RW/1S/V	**Flush Control (FCNTRL):** Writing a 1 to this bit initiates a flush. When the flush completion is received by the controller, hardware sets the Flush Status bit and clears this Flush Control bit. Before a flush cycle is initiated, the DMA Position Buffer must be programmed with a valid memory address by software, but the DMA Position Buffer bit 0 need not be set to enable the position reporting mechanism. Also, all streams must be stopped (the associated RUN bit must be 0). When the flush is initiated, the controller will flush pipelines to memory to guarantee that the hardware is ready to transition to a D3 state. Setting this bit is not a critical step in the power state transition if the content of the FIFOs is not critical.
0	0h RW/V	**Controller Reset# (CRSTB):** After the hardware has completed sequencing into the reset state, it will report a 0 in this bit. Software must read a 0 from this bit to verify that the controller is in reset. Writing a 1 to this bit causes the controller to exit its reset state and deassert the Intel HD Audio link RESET# signal. Software is responsible for setting/clearing this bit such that the minimum Intel HD Audio link RESET# signal assertion pulse width specification is met. When the controller hardware is ready to begin operation, it will report a 1 in this bit. Software must read a 1 from this bit before accessing any controller registers. The CRST bit defaults to a 0 after hardware reset, therefore software needs to write a 1 to this bit to begin operation. Note that the CORB/RIRB RUN bits and all Stream RUN bits must be verified cleared to zero before CRST bit is written to 0 (asserted) in order to assure a clean re-start. When setting or clearing CRST, software must ensure that minimum link timing requirements (minimum RESET# assertion time, etc.) are met. When CRST is 0 indicating that the controller is in reset, writes to all Intel HD Audio memory mapped registers are ignored as if the device is not present. The only exception is the Global Control register containing the CRST bit itself. The Global Control register is write-able as a DWord, Word, or Byte even when CRST is 0 if the byte enable for the byte containing the CRST bit (Byte Enable 0) is active. If Byte Enable 0 is not active, writes to the Global Control register will be ignored when CRST is 0. When CRST is 0, reads to Intel HD Audio memory mapped registers will return their default value except for registers that are not reset with PLTRST# or on a D3hot to D0 transition.

14.2.7 Wake Enable (WAKEEN)—Offset Ch

This register indicates which bits in the WAKESTS register may cause either a wake event or an interrupt.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:3	0h RO	Reserved.
2:0	0h RW	**SDIN Wake Enable Flags (WAKEEN):** Bits which control which SDI signal(s) may generate a wake event. A 1 bit in the bit mask indicates that the associated SDIN signal is enabled to generate a wake. These bits are cleared on a power-on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.

14.2.8 Wake Status (WAKESTS)—Offset Eh

This register indicates that a Status Change event has occurred on the link, which usually indicates that either the codec has just come out of reset and is requesting an address, or that a codec is signaling a wake event.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:3	0h RO	Reserved.
2:0	0h RW/1C/V	**SDIN State Change Status Flags (WAKESTS):** Flag bits that indicate which SDI signal(s) received a State Change event. The bits are cleared by writing 1's to them. These bits are cleared on a power-on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.

14.2.9 Global Status (GSTS)—Offset 10h

This register provides global level status of the controller.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:2	0h RO	Reserved.
1	0h RW/1C/V	**Flush Status (FSTS):** This bit is set to a 1 by the hardware to indicate that the flush cycle initiated when the FCNTRL bit was set has completed. Software must write a 1to clear this bit before the next time FCNTRL is set.
0	0h RO	Reserved.

14.2.10 Global Capabilities 2 (GCAP2)—Offset 12h

This register indicates the additional capabilities of the controller.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
15:1	0h RO	Reserved.
0	1h RW/V/L	**Energy Efficient Audio Capability (EEAC):** Indicates whether the energy efficient audio with deeper buffering is supported or not. 0 = Not supported. FIFOL register and FIFOLC bit behave as RO. 1 = Supported. FIFOL register and FIFOLC bit behave as RW. Locked when FNCFG.BCLD = 1 or FUSVAL.CPPMD = 1.

14.2.11 Linked List Capabilities Header (LLCH)—Offset 14h

This register provides the pointer to the first capability structure, if exists.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: C00h

Bit Range	Default and Access	Field Name (ID): Description
15:0	C00h RW/L	**First Capability Pointer (PTR):** This field contains the offset to the first capability structure of the linked list capabilities, or 0000h if no linked list capabilities exist. Point to Multiple Links Capability. Locked when FNCFG.BCLD = 1.

14.2.12 Output Stream Payload Capability (OUTSTRMPAY)—Offset 18h

This register indicates the maximum number of Words per frame for any single output stream.

Access Method

Type: MEM Register (Size: 16 bits)
Device:
Function:

Default: 30h

Bit Range	Default and Access	Field Name (ID): Description
15:0	30h RO	**Output Stream Payload Capability (OUTSTRMPAY):** Indicates maximum number of words per frame for any single output stream. This measurement is in 16 bit word quantities per 48 kHz frame. 48 Words (96B) is the maximum supported, therefore a value of 30h is reported in this register. Software must ensure that a format which would cause more words per frame than indicated is not programmed into the Output Stream Descriptor register. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload

14.2.13 Input Stream Payload Capability (INSTRMPAY)—Offset 1Ah

This register indicates the maximum number of Words per frame for any single input stream.

Access Method

Type: MEM Register (Size: 16 bits)
Device:
Function:

Default: 18h

Bit Range	Default and Access	Field Name (ID): Description
15:0	18h RO	**Input Stream Payload Capability (INSTRMPAY):** Indicates maximum number of words per frame for any single input stream. This measurement is in 16 bit word quantities per 48 kHz frame. 24 Words (48B) is the maximum supported, therefore a value of 18h is reported in this register. Software must ensure that a format which would cause more words per frame than indicated is not programmed into the Input Stream Descriptor register. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload

14.2.14 Interrupt Control (INTCTL)—Offset 20h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW	**Global Interrupt Enable (GIE):** Global bit to enable device interrupt generation. When set to 1 the Intel HD Audio function is enabled to generate an interrupt. This control is in addition to any bits in the bus specific address space, such as the Interrupt Enable bit in the PCI Configuration Space.
30	0h RW	**Controller Interrupt Enable (CIE):** Enables the general interrupt for controller functions. When set to 1 (and GIE is enabled), the controller generates an interrupt when the CIS bit gets set.
29:16	0h RO	Reserved.
15:0	0h RW	**Stream Interrupt Enable (SIE):** When set to 1 the individual Streams are enabled to generate an interrupt when the corresponding stream status bits get set. A stream interrupt will be caused as a result of a buffer with IOC=1 in the BDL entry being completed, or as a result of a FIFO error (underrun or overrun) occurring. Control over the generation of each of these sources is in the associated Stream Descriptor. The streams are numbered and the SIE bits assigned sequentially, based on their order in the register set.

14.2.15 Interrupt Status (INTSTS)—Offset 24h

GIS and CIS bits are not affected by controller reset.
The number of SIS bits in this register is depending on the total number of stream DMA implemented.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO/V	**Global Interrupt Status (GIS):** This bit is an OR of all of the interrupt status bits in this register and PPSTS register
30	0h RW/V	**Controller Interrupt Status (CIS):** Status of general controller interrupt. A 1 indicates that an interrupt condition occurred due to a Response Interrupt, a Response Buffer Overrun Interrupt, CORB Memory Error Interrupt, or a SDIN State Change event. The exact cause can be determined by interrogating other registers. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of the stated interrupt status bits for this register.
29:16	0h RO	Reserved.
15:0	0h RW/V	**Stream Interrupt Status (SIS):** A 1 indicates that an interrupt condition occurred on the corresponding Stream. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of an individual stream s interrupt status bits. The streams are numbered and the SIS bits assigned sequentially, based on their order in the register set.

14.2.16 Wall Clock Counter (WALCLK)—Offset 30h

The 32 bit monotonic counter provides a 'wall clock' that can be used by system software to synchronize independent audio controllers.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Wall Clock Counter (WALCLK):** 32 bit counter that is incremented on each link BCLK period and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to zero with a period of approximately 179 seconds. This counter is enabled while the BCLK bit is set to 1. Software uses this counter to synchronize between multiple controllers. Will be reset on controller reset. With the introduction of multiple link segments for the Intel HD Audio controller, and the capability of running each link segment at different clock speed, the BCLK definition for this counter is fixed at 24 MHz equivalent rate always, independent of the physical link clock speed, and reports the link 0 wall clock value.

14.2.17 Stream Synchronization (SSYNC)—Offset 38h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**Stream Synchronization Bits (SSYNC):** The Stream Synchronization bits, when set to 1, block data from being sent on or received from the link. Each bit controls the associated Stream Descriptor, bit 0 corresponds to the first Stream Descriptor, etc. To synchronously start a set of DMA engines, the bits in the SSYNC register are first set to a 1. The RUN bits for the associated Stream Descriptors are then set to a 1 to start the DMA engines. When all streams are ready (FIFORDY=1), the associated SSYNC bits can all be set to 0 at the same time, and transmission or reception of bits to or from the link will begin together at the start of the next full link frame. To synchronously stop streams, first the bits are set in the SSYNC register, and then the individual RUN bits in the Stream Descriptors are cleared by software. The streams are numbered and the SSYNC bits assigned sequentially, based on their order in the register set.

14.2.18 CORB Lower Base Address (CORBLBASE)—Offset 40h

This register specifies the address (lower 32 bits) of the Command Output Ring Buffer.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:7	0h RW	**CORB Lower Base Address (CORBLBASE):** Lower address of the Command Output Ring Buffer, allowing the CORB Base Address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	0h RO	Reserved.

14.2.19 CORB Upper Base Address (CORBUBASE)—Offset 44h

This register specifies the address (upper 32 bits) of the Command Output Ring Buffer.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/L	**CORB Upper Base Address (CORBUBASE):** Upper 32 bits of address of the Command Output Ring Buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted. Locked when GCAP.ADD64OK = 0.

14.2.20 CORB Write Pointer (CORBWP)—Offset 48h

This register specifies the write pointer of the Command Output Ring Buffer.

Access Method

Type: MEM Register (Size: 16 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7:0	0h RW	**CORB Write Pointer (CORBWP):** Software writes the last valid CORB entry offset into this field in Dword granularity. The DMA engine fetches commands from the CORB until the Read Pointer matches the Write Pointer. Supports 256 CORB entries (256 x 4B=1KB). This field may be written while the DMA engine is running.

14.2.21 CORB Read Pointer (CORBRP)—Offset 4Ah

This register reports the read pointer of the Command Output Ring Buffer.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15	0h RW/V	**CORB Read Pointer Reset (CORBRPRST):** Software writes a 1 to this bit to reset the CORB Read Pointer to 0 and clear any residual pre-fetched commands in the CORB hardware buffer within the Intel Audio controller. The hardware will physically update this bit to 1 when the CORB Pointer reset is complete. Software must read a 1 to verify that the reset completed correctly. Software must clear this bit back to 0 and read back the 0 to verify that the clear completed correctly. The CORB DMA engine must be stopped prior to resetting the Read Pointer or else DMA transfer may be corrupted.
14:8	0h RO	Reserved.
7:0	0h RO/V	**CORB Read Pointer (CORBRP):** Software reads this field to determine how many commands it can write to the CORB without over-running. The value read indicates the CORB Read Pointer offset in Dword granularity. The offset entry read from this field has been successfully fetched by the DMA controller and may be over-written by software. Supports 256 CORB entries (256 x 4B=1KB). This field may be read while the DMA engine is running.

14.2.22 CORB Control (CORBCTL)—Offset 4Ch

This register provides the control of the Command Output Ring Buffer.

Access Method

Type: MEM Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:2	0h RO	Reserved.
1	0h RW/V	**Enable CORB DMA Engine (CORBRUN):** 0 = DMA Stop 1 = DMA Run After SW writes a 0 to this bit, the HW may not stop immediately. The hardware will physically update the bit to a 0 when the DMA engine is truly stopped. SW must read a 0 from this bit to verify that the DMA is truly stopped.
0	0h RW	**CORB Memory Error Interrupt Enable (CMEIE):** If this bit is set (and GIE and CIE are enabled), the controller will generate an interrupt if the MEI status bit is set.

14.2.23 CORB Status (CORBSTS)—Offset 4Dh

This register provides the status of the Command Output Ring Buffer.

Access Method

Type: MEM Register (Size: 8 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:1	0h RO	Reserved.
0	0h RW/1C/V	**CORB Memory Error Indication (CMEI):** If this status bit is set, the controller has detected an error in the pathway between the controller and memory. This may be an ECC bit error or any other type of detectable data error which renders the command data fetched invalid. Software can clear this bit by writing a 1 to it. However, this type of error leaves the audio subsystem in an unavailable state and typically requires CRST#.

14.2.24 CORB Size (CORBSIZE)—Offset 4Eh

This register declares the size of the Command Output Ring Buffer.

Access Method

Type: MEM Register (Size: 8 bits)
Device:
Function:

Default: 42h

Bit Range	Default and Access	Field Name (ID): Description
7:4	4h RO	**CORB Size Capability (CORBSZCAP):** 0100b indicates that the ICH9 only supports a CORB size of 256 CORB entries (1024B).
3:2	0h RO	Reserved.
1:0	2h RO	**CORB Size (CORBSIZE):** Hardwired to 10b which sets the CORB size to 256 entries (1024B).

14.2.25 RIRB Lower Base Address (RIRBLBASE)—Offset 50h

This register specifies the address (lower 32 bits) of the Response Input Ring Buffer.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:7	0h RW	**RIRB Lower Base Address (RIRBLBASE):** Lower address of the Response Input Ring Buffer, allowing the RIRB Base Address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	0h RO	Reserved.

14.2.26 RIRB Upper Base Address (RIRBUBASE)—Offset 54h

This register specifies the address (upper 32 bits) of the Response Input Ring Buffer.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/L	**RIRB Upper Base Address (RIRBUBASE):** Upper 32 bits of address of the Command Output Ring Buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0.

14.2.27 RIRB Write Pointer (RIRBWP)—Offset 58h

This register reports the write pointer of the Response Input Ring Buffer.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15	0h WO	**RIRB Write Pointer Reset (RIRBWPRST):** Software writes a 1 to this bit to reset the RIRB Write Pointer to 0's. The RIRB DMA engine must be stopped prior to resetting the Write Pointer or else DMA transfer may be corrupted. This bit will always be read as 0.
14:8	0h RO	Reserved.
7:0	0h RO/V	**RIRB Write Pointer (RIRBWP):** Indicates the last valid RIRB entry written by the DMA controller. Software reads this field to determine how many responses it can read from the RIRB. The value read indicates the RIRB Write Pointer offset in 2 Dword RIRB entry units (since each RIRB entry is 2 Dwords long). Supports up to 256 RIRB entries (256 x 8B=2KB). This field may be read while the DMA engine is running.

14.2.28 Response Interrupt Count (RINTCNT)—Offset 5Ah

This register specifies the threshold of Response Input Ring Buffer that triggers an interrupt.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7:0	0h RW	**N Response Interrupt Count (RINTCNT):** 0000_0001b = 1 Response sent to RIRB ... 1111_1111b = 255 Responses sent to RIRB 0000_0000b = 256 Responses sent to RIRB The DMA engine should be stopped when changing this field or else an interrupt may be lost. Note that each Response occupies 2 Dwords in the RIRB. This is compared to the total number of responses that have been returned, as opposed to the number of frames in which there were responses. If more than one codec responds in one frame, then the count is increased by the number of responses received in the frame.

14.2.29 RIRB Control (RIRBCTL)—Offset 5Ch

This register provides the control of the Response Input Ring Buffer.

Access Method

Type: MEM Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h RW	**Response Overrun Interrupt Control (RIRBOIC):** If this bit is set (and GIE and CIE are enabled), the hardware will generate an interrupt when the Response Overrun Interrupt Status bit is set.
1	0h RW/V	**RIRB DMA Enable (RIRBRUN):** 0 = DMA Stop 1 = DMA Run After SW writes a 0 to this bit, the HW may not stop immediately. The hardware will physically update the bit to a 0 when the DMA engine is truly stopped. SW must read a 0 from this bit to verify that the DMA is truly stopped.
0	0h RW	**Response Interrupt Control (RINTCTL):** 0 = Disable Interrupt 1 = Generate an interrupt (if GIE and CIE are enabled) after N number of Responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI_x inputs (whichever occurs first). The N counter is reset when the interrupt is generated.

14.2.30 RIRB Status (RIRBSTS)—Offset 5Dh

This register provides the status of the Response Input Ring Buffer.

Access Method

Type: MEM Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h RW/1C/V	**Response Overrun Interrupt Status (RIRBOIS):** Hardware sets this bit to a 1 when the RIRB DMA engine is not able to write the incoming responses to memory before additional incoming responses overrun the internal FIFO. When the overrun occurs, the hardware will drop the responses which overrun the buffer. An interrupt may be generated if the Response Overrun Interrupt Control bit is set. Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this flag by writing a 1 to this bit.
1	0h RO	Reserved.
0	0h RW/1C/V	**Response Interrupt (RINTFL):** Hardware sets this bit to a 1 when an interrupt has been generated after N number of Responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI(x) inputs (whichever occurs first). Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this flag by writing a 1 to this bit.

14.2.31 RIRB Size (RIRBSIZE)—Offset 5Eh

This register declares the size of the Response Input Ring Buffer.

Access Method

Type: MEM Register
(Size: 8 bits)

Device:
Function:

Default: 42h

Bit Range	Default and Access	Field Name (ID): Description
7:4	4h RO	**RIRB Size Capability (RIRBSZCAP):** 0100b indicates that the PCH only supports a RIRB size of 256 RIRB entries (2048B).
3:2	0h RO	Reserved.
1:0	2h RO	**RIRB Size (RIRBSIZE):** Hardwired to 10b which sets the RIRB size to 256 entries (2048B).

14.2.32 Immediate Command (IC)—Offset 60h

This register provides the control of the immediate command.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Immediate Command (IC):** The command to be sent to the codec via the Immediate Command mechanism is written to this register. The command stored in this register is sent out over the link during the next available frame after a 1 is written to the ICB bit.

14.2.33 Immediate Response (IR)—Offset 64h

This register reports the response received for the immediate command.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Immediate Response (IR):** This register contains the response received from a codec resulting from a command sent via the Immediate Command mechanism. If multiple codecs responded in the same frame, there is no guarantee as to which response will be latched. Therefore broadcast-type commands must not be issued via the Immediate Command mechanism.

14.2.34 Immediate Command Status (ICS)—Offset 68h

This register provides the status of the immediate command.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:2	0h RO	Reserved.
1	0h RW/1C/V	**Immediate Result Valid (IRV):** This bit is set to a 1 by hardware when a new response is latched into the IR register. This is a status flag indicating that software may read the response from the Immediate Response register. Software must clear this bit (by writing a one to it) before issuing a new command so that the software may determine when a new response has arrived.
0	0h RW/V	**Immediate Command Busy (ICB):** When this bit as read as a 0 it indicates that a new command may be issued using the Immediate Command mechanism. When this bit transitions from a 0 to a 1 (via software writing a 1), the controller issues the command currently stored in the Immediate Command register to the codec over the link. When the corresponding response is latched into the Immediate Response register, the controller hardware sets the IRV flag and clears the ICB bit back to 0. SW may write this bit to a 0 if the bit fails to return to 0 after a reasonable timeout period. Note that an Immediate Command must not be issued while the CORB/RIRB mechanism is operating, otherwise the responses conflict. This must be enforced by software.

14.2.35 DMA Position Lower Base Address (DPLBASE)—Offset 70h

This register specifies the base address (lower 32 bits) of DMA Position Buffer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:7	0h RW	**DMA Position Lower Base Address (DPLBASE):** Lower 32 bits of the DMA Position Buffer Base Address. This register field must not be written when any DMA engine is running or the DMA transfer may be corrupted. This same address is used by the Flush Control, and must be programmed with a valid value before the FLCNRTL bit is set.
6:1	0h RO	Reserved.
0	0h RW	**DMA Position Buffer Enable (DPBE):** When this bit is set to a '1', the controller will write the DMA positions of each of the DMA engines to the buffer in main memory periodically (typically once/frame). Software can use this value to know what data in memory is valid data. The controller must guarantee that the values in the DMA Position Buffer that the software can read represent positions in the stream for which valid data exists in the Stream's DMA buffer. This has particular relevance in systems which support isochronous transfer, the stream positions in the software-visible memory buffer must represent stream data which has reached the Global Observation point.

14.2.36 DMA Position Upper Base Address (DPUBASE)—Offset 74h

This register specifies the base address (upper 32 bits) of DMA Position Buffer.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/L	**DMA Position Upper Base Address (DPUBASE):** Upper 32 bits of address of the DMA Position Buffer Base Address. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted. Locked when GCAP.ADD64OK = 0.

14.2.37 Input/Output Stream Descriptor x Control (ISD0CTL)—Offset 80h

NOTE: This register definition applies to all of the following input and output streams at the corresponding offsets:
Input stream 0: offset 80h
Input stream 1: offset A0h
Input stream 2: offset C0h
Input stream 3: offset E0h
Input stream 4: offset 100h
Input stream 5: offset 120h
Input stream 6: offset 140h
Input stream 7: offset 280h
Input stream 8: offset 2A0h
Input stream 9: offset 2C0h
Input stream 10: offset 2E0h
Input stream 11: offset 300h
Input stream 12: offset 320h

Input stream 13: offset 340h
Input stream 14: offset 360h

Output stream 0: offset 160h
Output stream 1: offset 180h
Output stream 2: offset 1A0h
Output stream 3: offset 1C0h
Output stream 4: offset 1E0h
Output stream 5: offset 200h
Output stream 6: offset 220h
output stream 7: offset 240h
Output stream 8: offset 260h
Output stream 9: offset 380h
Output stream 10: offset 3A0h
Output stream 11: offset 3C0h
Output stream 12: offset 3E0h
Output stream 13: offset 400h
Output stream 14: offset 420h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 40000h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.
19	0h RO	**Bidirectional Direction Control (DIR):** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	1h RO	**Traffic Priority (TP):** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RW/L	**Stripe Control (STRIPE):** Input Stream: This field is meaningless for input streams. Output Stream: For output streams it controls the number of SDO signals to stripe data across. Locked when GCAP.NSDO = 00b.
15:6	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0. If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set). If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set).
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

14.2.38 Input/Output Stream Descriptor x Status (ISD0STS)—Offset 83h

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 83h
Input stream 1: offset A3h
Input stream 2: offset C3h
Input stream 3: offset E3h
Input stream 4: offset 103h
Input stream 5: offset 123h
Input stream 6: offset 143h
Input stream 7: offset 283h
Input stream 8: offset 2A3h
Input stream 9: offset 2C3h
Input stream 10: offset 2E3h
Input stream 11: offset 303h
Input stream 12: offset 323h
Input stream 13: offset 343h
Input stream 14: offset 363h

Output stream 0: offset 163h
Output stream 1: offset 183h
Output stream 2: offset 1A3h

Output stream 3: offset 1C3h
Output stream 4: offset 1E3h
Output stream 5: offset 203h
Output stream 6: offset 223h
output stream 7: offset 243h
Output stream 8: offset 263h
Output stream 9: offset 383h
Output stream 10: offset 3A3h
Output stream 11: offset 3C3h
Output stream 12: offset 3E3h
Output stream 13: offset 403h
Output stream 14: offset 423h

Access Method

Type: MEM Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:6	0h RO	Reserved.
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers do not increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	Reserved.

14.2.39 Input/Output Stream Descriptor x Link Position in Buffer (ISD0LPIB)—Offset 84h

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 84h
Input stream 1: offset A4h
Input stream 2: offset C4h
Input stream 3: offset E4h
Input stream 4: offset 104h
Input stream 5: offset 124h
Input stream 6: offset 144h
Input stream 7: offset 284h
Input stream 8: offset 2A4h
Input stream 9: offset 2C4h
Input stream 10: offset 2E4h
Input stream 11: offset 304h
Input stream 12: offset 324h
Input stream 13: offset 344h
Input stream 14: offset 364h

Output stream 0: offset 164h
Output stream 1: offset 184h
Output stream 2: offset 1A4h
Output stream 3: offset 1C4h
Output stream 4: offset 1E4h
Output stream 5: offset 204h
Output stream 6: offset 224h
output stream 7: offset 244h
Output stream 8: offset 264h
Output stream 9: offset 384h
Output stream 10: offset 3A4h
Output stream 11: offset 3C4h
Output stream 12: offset 3E4h
Output stream 13: offset 404h
Output stream 14: offset 324h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.40 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD0CBL)—Offset 88h

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 88h
Input stream 1: offset A8h
Input stream 2: offset C8h
Input stream 3: offset E8h
Input stream 4: offset 108h
Input stream 5: offset 128h
Input stream 6: offset 148h
Input stream 7: offset 288h
Input stream 8: offset 2A8h
Input stream 9: offset 2C8h
Input stream 10: offset 2E8h
Input stream 11: offset 308h
Input stream 12: offset 328h
Input stream 13: offset 348h
Input stream 14: offset 368h

Output stream 0: offset 168h
Output stream 1: offset 188h
Output stream 2: offset 1A8h
Output stream 3: offset 1C8h
Output stream 4: offset 1E8h
Output stream 5: offset 208h
Output stream 6: offset 228h
output stream 7: offset 248h
Output stream 8: offset 268h
Output stream 9: offset 388h
Output stream 10: offset 3A8h
Output stream 11: offset 3C8h
Output stream 12: offset 3E8h
Output stream 13: offset 408h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

14.2.41 Input/Output Stream Descriptor x Last Valid Index (ISD0LVI)—Offset 8Ch

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 8Ch
Input stream 1: offset ACh
Input stream 2: offset CCh
Input stream 3: offset ECh
Input stream 4: offset 10Ch
Input stream 5: offset 12Ch
Input stream 6: offset 14Ch
Input stream 7: offset 28Ch
Input stream 8: offset 2ACh
Input stream 9: offset 2CCh
Input stream 10: offset 2ECh
Input stream 11: offset 30Ch
Input stream 12: offset 32Ch
Input stream 13: offset 34Ch
Input stream 14: offset 36Ch

Output stream 0: offset 16Ch
Output stream 1: offset 18Ch
Output stream 2: offset 1ACh
Output stream 3: offset 1CCh
Output stream 4: offset 1ECh
Output stream 5: offset 20Ch
Output stream 6: offset 22Ch
output stream 7: offset 24Ch
Output stream 8: offset 26Ch
Output stream 9: offset 38Ch
Output stream 10: offset 3ACh
Output stream 11: offset 3CCh
Output stream 12: offset 3ECh
Output stream 13: offset 40Ch
Output stream 14: offset 42Ch

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7:0	0h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the b uffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'

14.2.42 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD0FIFOW)—Offset 8Eh

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 8Eh
Input stream 1: offset AEh
Input stream 2: offset CEh
Input stream 3: offset EEh
Input stream 4: offset 10Eh
Input stream 5: offset 12Eh
Input stream 6: offset 14Eh
Input stream 7: offset 28Eh
Input stream 8: offset 2AEh
Input stream 9: offset 2CEh
Input stream 10: offset 2EEh
Input stream 11: offset 30Eh
Input stream 12: offset 32Eh
Input stream 13: offset 34Eh
Input stream 14: offset 36Eh

Output stream 0: offset 16Eh
Output stream 1: offset 18Eh
Output stream 2: offset 1AEh
Output stream 3: offset 1CEh
Output stream 4: offset 1EEh
Output stream 5: offset 20Eh
Output stream 6: offset 22Eh
output stream 7: offset 24Eh
Output stream 8: offset 26Eh
Output stream 9: offset 38Eh
Output stream 10: offset 3AEh
Output stream 11: offset 3CEh
Output stream 12: offset 3EEh
Output stream 13: offset 40Eh
Output stream 14: offset 42Eh

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
15:3	0h RO	Reserved.
2:0	4h RO/V	**FIFOW (FIFOW):** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The PCH HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description 000-011 Reserved 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

14.2.43 Input/Output Stream Descriptor x FIFO Size (ISD0FIFOS)—Offset 90h

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 90h
Input stream 1: offset B0h
Input stream 2: offset D0h
Input stream 3: offset F0h
Input stream 4: offset 110h
Input stream 5: offset 130h
Input stream 6: offset 150h
Input stream 7: offset 290h
Input stream 8: offset 2B0h
Input stream 9: offset 2D0h
Input stream 10: offset 2F0h
Input stream 11: offset 310h
Input stream 12: offset 330h
Input stream 13: offset 350h
Input stream 14: offset 370h

Output stream 0: offset 170h
Output stream 1: offset 190h
Output stream 2: offset 1B0h
Output stream 3: offset 1D0h
Output stream 4: offset 1F0h
Output stream 5: offset 210h
Output stream 6: offset 230h
output stream 7: offset 250h
Output stream 8: offset 270h
Output stream 9: offset 390h
Output stream 10: offset 3B0h
Output stream 11: offset 3D0h

Output stream 12: offset 3F0h
Output stream 13: offset 410h
Output stream 14: offset 430h

Access Method

Type: MEM Register (Size: 16 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:0	0h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O)SDxFMT register, the min frame of buffering setting in EM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O)SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum value could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

14.2.44 Input/Output Stream Descriptor x Format (ISD0FMT)—Offset 92h

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 92h
Input stream 1: offset B2h
Input stream 2: offset D2h
Input stream 3: offset F2h
Input stream 4: offset 112h
Input stream 5: offset 132h
Input stream 6: offset 152h
Input stream 7: offset 292h
Input stream 8: offset 2B2h
Input stream 9: offset 2D2h
Input stream 10: offset 2F2h
Input stream 11: offset 312h
Input stream 12: offset 332h
Input stream 13: offset 352h
Input stream 14: offset 372h

Output stream 0: offset 172h
Output stream 1: offset 192h
Output stream 2: offset 1B2h
Output stream 3: offset 1D2h

Output stream 4: offset 1F2h
Output stream 5: offset 212h
Output stream 6: offset 232h
output stream 7: offset 252h
Output stream 8: offset 272h
Output stream 9: offset 392h
Output stream 10: offset 3B2h
Output stream 11: offset 3D2h
Output stream 12: offset 3F2h
Output stream 13: offset 412h
Output stream 14: offset 432h

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8bit containers on 16bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

14.2.45 Input/Output Stream Descriptor x FIFO Limit (ISD0FIFOL)—Offset 94h

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 94h
Input stream 1: offset B4h
Input stream 2: offset D4h
Input stream 3: offset F4h
Input stream 4: offset 114h
Input stream 5: offset 134h
Input stream 6: offset 154h
Input stream 7: offset 294h
Input stream 8: offset 2B4h
Input stream 9: offset 2D4h
Input stream 10: offset 2F4h
Input stream 11: offset 314h
Input stream 12: offset 334h
Input stream 13: offset 354h
Input stream 14: offset 374h

Output stream 0: offset 174h
Output stream 1: offset 194h
Output stream 2: offset 1B4h
Output stream 3: offset 1D4h
Output stream 4: offset 1F4h
Output stream 5: offset 214h
Output stream 6: offset 234h
output stream 7: offset 254h
Output stream 8: offset 274h
Output stream 9: offset 394h
Output stream 10: offset 3B4h
Output stream 11: offset 3D4h
Output stream 12: offset 3F4h
Output stream 13: offset 414h
Output stream 14: offset 434h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW/L	**Granularity (GNL):** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. 0 = 125 us 1 = 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).
13:0	0h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time. 0 = Disabled (FIFOS is the limit) 0001h 3FFFh = 1 16383 units When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).

14.2.46 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD0BDLPLBA)—Offset 98h

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 98h
Input stream 1: offset B8h
Input stream 2: offset D8h
Input stream 3: offset F8h
Input stream 4: offset 118h
Input stream 5: offset 138h
Input stream 6: offset 158h
Input stream 7: offset 298h
Input stream 8: offset 2B8h
Input stream 9: offset 2D8h
Input stream 10: offset 2F8h
Input stream 11: offset 318h
Input stream 12: offset 338h
Input stream 13: offset 358h
Input stream 14: offset 378h

Output stream 0: offset 178h
Output stream 1: offset 198h
Output stream 2: offset 1B8h
Output stream 3: offset 1D8h
Output stream 4: offset 1F8h
Output stream 5: offset 218h
Output stream 6: offset 238h
output stream 7: offset 258h
Output stream 8: offset 278h
Output stream 9: offset 398h
Output stream 10: offset 3B8h
Output stream 11: offset 3D8h

Output stream 12: offset 3F8h
Output stream 13: offset 418h
Output stream 14: offset 438h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:7	0h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:0	0h RO	Reserved.

14.2.47 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD0BDLPUBA)—Offset 9Ch

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 9Ch
Input stream 1: offset BCh
Input stream 2: offset DCh
Input stream 3: offset FCh
Input stream 4: offset 11Ch
Input stream 5: offset 13Ch
Input stream 6: offset 15Ch
Input stream 7: offset 29Ch
Input stream 8: offset 2BCh
Input stream 9: offset 2DCh
Input stream 10: offset 2FCh
Input stream 11: offset 31Ch
Input stream 12: offset 33Ch
Input stream 13: offset 35Ch
Input stream 14: offset 37Ch

Output stream 0: offset 17Ch
Output stream 1: offset 19Ch
Output stream 2: offset 1BCh
Output stream 3: offset 1DCh
Output stream 4: offset 1FCh
Output stream 5: offset 21Ch
Output stream 6: offset 23Ch
output stream 7: offset 25Ch
Output stream 8: offset 27Ch
Output stream 9: offset 39Ch
Output stream 10: offset 3BCh
Output stream 11: offset 3DCh

Output stream 12: offset 4FCh
Output stream 13: offset 41Ch
Output stream 14: offset 43Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0.

14.2.48 Input/Output Stream Descriptor x Control (ISD1CTLB0)—Offset A0h

SRST bit is not affected by stream reset.

14.2.49 Input/Output Stream Descriptor x Control (ISD1CTL)—Offset A0h

Same description as ISD0CTL register at offset 80h.

14.2.50 Input/Output Stream Descriptor x Control (ISD1CTLB2)—Offset A2h

SRST bit is not affected by stream reset.

14.2.51 Input/Output Stream Descriptor x Status (ISD1STS)—Offset A3h

Same description as ISD0STS register at offset 83h.

14.2.52 Input/Output Stream Descriptor x Link Position in Buffer (ISD1LPIB)—Offset A4h

Same description as ISD0LPIB register at offset 84h.

14.2.53 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD1CBL)—Offset A8h

Same description as ISD0CBL register at offset 88h.

14.2.54 Input/Output Stream Descriptor x Last Valid Index (ISD1LVI)—Offset ACh

Same description as ISD0LVI register at offset 8Ch.

14.2.55 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD1FIFOW)—Offset AEh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.56 Input/Output Stream Descriptor x FIFO Size (ISD1FIFOS)—Offset B0h

Same description as ISD0FIFOS register at offset 90h.

14.2.57 Input/Output Stream Descriptor x Format (ISD1FMT)—Offset B2h

Same description as ISD0FMT register at offset 92h.

14.2.58 Input/Output Stream Descriptor x FIFO Limit (ISD1FIFOL)—Offset B4h

Same description as ISD0FIFOL register at offset 94h.

14.2.59 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD1BDLPLBA)—Offset B8h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.60 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD1BDLPUBA)—Offset BCh

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.61 Input/Output Stream Descriptor x Control (ISD2CTL)—Offset C0h

Same description as ISD0CTL register at offset 80h.

14.2.62 Input/Output Stream Descriptor x Status (ISD2STS)—Offset C3h

Same description as ISD0STS register at offset 83h.

14.2.63 Input/Output Stream Descriptor x Link Position in Buffer (ISD2LPIB)—Offset C4h

Same description as ISD0LPIB register at offset 84h.

14.2.64 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD2CBL)—Offset C8h

Same description as ISD0CBL register at offset 88h.

14.2.65 Input/Output Stream Descriptor x Last Valid Index (ISD2LVI)—Offset CCh

Same description as ISD0LVI register at offset 8Ch.

14.2.66 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD2FIFOW)—Offset CEh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.67 Input/Output Stream Descriptor x FIFO Size (ISD2FIFOS)—Offset D0h

Same description as ISD0FIFOS register at offset 90h.

14.2.68 Input/Output Stream Descriptor x Format (ISD2FMT)—Offset D2h

Same description as ISD0FMT register at offset 92h.

14.2.69 Input/Output Stream Descriptor x FIFO Limit (ISD2FIFOL)—Offset D4h

Same description as ISD0FIFOL register at offset 94h.

14.2.70 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD2BDLPLBA)—Offset D8h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.71 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD2BDLPUBA)—Offset DCh

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.72 Input/Output Stream Descriptor x Control (ISD3CTL)—Offset E0h

Same description as ISD0CTL register at offset 80h.

14.2.73 Input/Output Stream Descriptor x Control (ISD3CTLB0)—Offset E0h

SRST bit is not affected by stream reset.

14.2.74 Input/Output Stream Descriptor x Status (ISD3STS)—Offset E3h

Same description as ISD0STS register at offset 83h.

14.2.75 Input/Output Stream Descriptor x Link Position in Buffer (ISD3LPIB)—Offset E4h

Same description as ISD0LPIB register at offset 84h.

14.2.76 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD3CBL)—Offset E8h

Same description as ISD0CBL register at offset 88h.

14.2.77 Input/Output Stream Descriptor x Last Valid Index (ISD3LVI)—Offset ECh

Same description as ISD0LVI register at offset 8Ch.

14.2.78 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD3FIFOW)—Offset EEh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.79 Input/Output Stream Descriptor x FIFO Size (ISD3FIFOS)—Offset F0h

Same description as ISD0FIFOS register at offset 90h.

14.2.80 Input/Output Stream Descriptor x Format (ISD3FMT)—Offset F2h

Same description as ISD0FMT register at offset 92h.

14.2.81 Input/Output Stream Descriptor x FIFO Limit (ISD3FIFOL)—Offset F4h

Same description as ISD0FIFOL register at offset 94h.

14.2.82 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD3BDLPLBA)—Offset F8h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.83 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD3BDLPUBA)—Offset FCh

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.84 Input/Output Stream Descriptor x Control (ISD4CTL)—Offset 100h

Same description as ISD0CTL register at offset 80h.

14.2.85 Input/Output Stream Descriptor x Status (ISD4STS)—Offset 103h

Same description as ISD0STS register at offset 83h.

14.2.86 Input/Output Stream Descriptor x Link Position in Buffer (ISD4LPIB)—Offset 104h

Same description as ISD0LPIB register at offset 84h.

14.2.87 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD4CBL)—Offset 108h

Same description as ISD0CBL register at offset 88h.

14.2.88 Input/Output Stream Descriptor x Last Valid Index (ISD4LVI)—Offset 10Ch

Same description as ISD0LVI register at offset 8Ch.

14.2.89 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD4FIFOW)—Offset 10Eh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.90 Input/Output Stream Descriptor x FIFO Size (ISD4FIFOS)—Offset 110h

Same description as ISD0FIFOS register at offset 90h.

14.2.91 Input/Output Stream Descriptor x Format (ISD4FMT)—Offset 112h

Same description as ISD0FMT register at offset 92h.

14.2.92 Input/Output Stream Descriptor x FIFO Limit (ISD4FIFOL)—Offset 114h

Same description as ISD0FIFOL register at offset 94h.

14.2.93 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD4BDLPLBA)—Offset 118h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.94 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD4BDLPUBA)—Offset 11Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.95 Input/Output Stream Descriptor x Control (ISD5CTL)—Offset 120h

Same description as ISD0CTL register at offset 80h.

14.2.96 Input/Output Stream Descriptor x Status (ISD5STS)—Offset 123h

Same description as ISD0STS register at offset 83h.

14.2.97 Input/Output Stream Descriptor x Link Position in Buffer (ISD5LPIB)—Offset 124h

Same description as ISD0LPIB register at offset 84h.

14.2.98 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD5CBL)—Offset 128h

Same description as ISD0CBL register at offset 88h.

14.2.99 Input/Output Stream Descriptor x Last Valid Index (ISD5LVI)—Offset 12Ch

Same description as ISD0LVI register at offset 8Ch.

14.2.100 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD5FIFOW)—Offset 12Eh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.101 Input/Output Stream Descriptor x FIFO Size (ISD5FIFOS)—Offset 130h

Same description as ISD0FIFOS register at offset 90h.

14.2.102 Input/Output Stream Descriptor x Format (ISD5FMT)—Offset 132h

Same description as ISD0FMT register at offset 92h.

14.2.103 Input/Output Stream Descriptor x FIFO Limit (ISD5FIFOL)—Offset 134h

Same description as ISD0FIFOL register at offset 94h.

14.2.104 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD5BDLPLBA)—Offset 138h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.105 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD5BDLPUBA)—Offset 13Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.106 Input/Output Stream Descriptor x Control (ISD6CTL)—Offset 140h

Same description as ISD0CTL register at offset 80h.

14.2.107 Input/Output Stream Descriptor x Status (ISD6STS)—Offset 143h

Same description as ISD0STS register at offset 83h.

14.2.108 Input/Output Stream Descriptor x Link Position in Buffer (ISD6LPIB)—Offset 144h

Same description as ISD0LPIB register at offset 84h.

14.2.109 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD6CBL)—Offset 148h

Same description as ISD0CBL register at offset 88h.

14.2.110 Input/Output Stream Descriptor x Last Valid Index (ISD6LVI)—Offset 14Ch

Same description as ISD0LVI register at offset 8Ch.

14.2.111 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD6FIFOW)—Offset 14Eh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.112 Input/Output Stream Descriptor x FIFO Size (ISD6FIFOS)—Offset 150h

Same description as ISD0FIFOS register at offset 90h.

14.2.113 Input/Output Stream Descriptor x Format (ISD6FMT)—Offset 152h

Same description as ISD0FMT register at offset 92h.

14.2.114 Input/Output Stream Descriptor x FIFO Limit (ISD6FIFOL)—Offset 154h

Same description as ISD0FIFOL register at offset 94h.

14.2.115 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD6BDLPLBA)—Offset 158h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.116 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD6BDLPUBA)—Offset 15Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.117 Input/Output Stream Descriptor x Control (OSD1CTL)—Offset 180h

Same description as ISD0CTL register at offset 80h.

14.2.118 Input/Output Stream Descriptor x Status (OSD1STS)—Offset 183h

Same description as ISD0STS register at offset 83h.

14.2.119 Input/Output Stream Descriptor x Link Position in Buffer (OSD1LPIB)—Offset 184h

Same description as ISD0LPIB register at offset 84h.

14.2.120 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD1CBL)—Offset 188h

Same description as ISD0CBL register at offset 88h.

14.2.121 Input/Output Stream Descriptor x Last Valid Index (OSD1LVI)—Offset 18Ch

Same description as ISD0LVI register at offset 8Ch.

14.2.122 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD1FIFOW)—Offset 18Eh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.123 Input/Output Stream Descriptor x FIFO Size (OSD1FIFOS)—Offset 190h

Same description as ISD0FIFOS register at offset 90h.

14.2.124 Input/Output Stream Descriptor x Format (OSD1FMT)—Offset 192h

Same description as ISD0FMT register at offset 92h.

14.2.125 Input/Output Stream Descriptor x FIFO Limit (OSD1FIFOL)—Offset 194h

Same description as ISD0FIFOL register at offset 94h.

14.2.126 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD1BDLPLBA)—Offset 198h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.127 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD1BDLPUBA)—Offset 19Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.128 Input/Output Stream Descriptor x Control (OSD2CTL)—Offset 1A0h

Same description as ISD0CTL register at offset 80h.

14.2.129 Input/Output Stream Descriptor x Status (OSD2STS)—Offset 1A3h

Same description as ISD0STS register at offset 83h.

14.2.130 Input/Output Stream Descriptor x Link Position in Buffer (OSD2LPIB)—Offset 1A4h

Same description as ISD0LPIB register at offset 84h.

14.2.131 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD2CBL)—Offset 1A8h

Same description as ISD0CBL register at offset 88h.

14.2.132 Input/Output Stream Descriptor x Last Valid Index (OSD2LVI)—Offset 1ACh

Same description as ISD0LVI register at offset 8Ch.

14.2.133 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD2FIFOW)—Offset 1AEh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.134 Input/Output Stream Descriptor x FIFO Size (OSD2FIFOS)—Offset 1B0h

Same description as ISD0FIFOS register at offset 90h.

14.2.135 Input/Output Stream Descriptor x Format (OSD2FMT)—Offset 1B2h

Same description as ISD0FMT register at offset 92h.

14.2.136 Input/Output Stream Descriptor x FIFO Limit (OSD2FIFOL)—Offset 1B4h

Same description as ISD0FIFOL register at offset 94h.

14.2.137 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD2BDLPLBA)—Offset 1B8h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.138 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD2BDLPUBA)—Offset 1BCh

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.139 Input/Output Stream Descriptor x Control (OSD3CTLB0)—Offset 1C0h

SRST bit is not affected by stream reset.

14.2.140 Input/Output Stream Descriptor x Control (OSD3CTL)—Offset 1C0h

Same description as ISD0CTL register at offset 80h.

14.2.141 Input/Output Stream Descriptor x Control (OSD3CTLB2)—Offset 1C2h

SRST bit is not affected by stream reset.

14.2.142 Input/Output Stream Descriptor x Status (OSD3STS)—Offset 1C3h

Same description as ISD0STS register at offset 83h.

14.2.143 Input/Output Stream Descriptor x Link Position in Buffer (OSD3LPIB)—Offset 1C4h

Same description as ISD0LPIB register at offset 84h.

14.2.144 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD3CBL)—Offset 1C8h

Same description as ISD0CBL register at offset 88h.

14.2.145 Input/Output Stream Descriptor x Last Valid Index (OSD3LVI)—Offset 1CCh

Same description as ISD0LVI register at offset 8Ch.

14.2.146 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD3FIFOW)—Offset 1CEh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.147 Input/Output Stream Descriptor x FIFO Size (OSD3FIFOS)—Offset 1D0h

Same description as ISD0FIFOS register at offset 90h.

14.2.148 Input/Output Stream Descriptor x Format (OSD3FMT)—Offset 1D2h

Same description as ISD0FMT register at offset 92h.

14.2.149 Input/Output Stream Descriptor x FIFO Limit (OSD3FIFOL)—Offset 1D4h

Same description as ISD0FIFOL register at offset 94h.

14.2.150 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD3BDLPLBA)—Offset 1D8h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.151 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD3BDLPUBA)—Offset 1DCh

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.152 Input/Output Stream Descriptor x Control (OSD4CTL)—Offset 1E0h

Same description as ISD0CTL register at offset 80h.

14.2.153 Input/Output Stream Descriptor x Status (OSD4STS)—Offset 1E3h

Same description as ISD0STS register at offset 83h.

14.2.154 Input/Output Stream Descriptor x Link Position in Buffer (OSD4LPIB)—Offset 1E4h

Same description as ISD0LPIB register at offset 84h.

14.2.155 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD4CBL)—Offset 1E8h

Same description as ISD0CBL register at offset 88h.

14.2.156 Input/Output Stream Descriptor x Last Valid Index (OSD4LVI)—Offset 1ECh

Same description as ISD0LVI register at offset 8Ch.

14.2.157 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD4FIFOW)—Offset 1EEh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.158 Input/Output Stream Descriptor x FIFO Size (OSD4FIFOS)—Offset 1F0h

Same description as ISD0FIFOS register at offset 90h.

14.2.159 Input/Output Stream Descriptor x Format (OSD4FMT)—Offset 1F2h

Same description as ISD0FMT register at offset 92h.

14.2.160 Input/Output Stream Descriptor x FIFO Limit (OSD4FIFOL)—Offset 1F4h

Same description as ISD0FIFOL register at offset 94h.

14.2.161 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD4BDLPLBA)—Offset 1F8h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.162 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD4BDLPUBA)—Offset 1FCh

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.163 Input/Output Stream Descriptor x Control (OSD5CTL)—Offset 200h

Same description as ISD0CTL register at offset 80h.

14.2.164 Input/Output Stream Descriptor x Status (OSD5STS)—Offset 203h

Same description as ISD0STS register at offset 83h.

14.2.165 Input/Output Stream Descriptor x Link Position in Buffer (OSD5LPIB)—Offset 204h

Same description as ISD0LPIB register at offset 84h.

14.2.166 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD5CBL)—Offset 208h

Same description as ISD0CBL register at offset 88h.

14.2.167 Input/Output Stream Descriptor x Last Valid Index (OSD5LVI)—Offset 20Ch

Same description as ISD0LVI register at offset 8Ch.

14.2.168 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD5FIFOW)—Offset 20Eh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.169 Input/Output Stream Descriptor x FIFO Size (OSD5FIFOS)—Offset 210h

Same description as ISD0FIFOS register at offset 90h.

14.2.170 Input/Output Stream Descriptor x Format (OSD5FMT)—Offset 212h

Same description as ISD0FMT register at offset 92h.

14.2.171 Input/Output Stream Descriptor x FIFO Limit (OSD5FIFOL)—Offset 214h

Same description as ISD0FIFOL register at offset 94h.

14.2.172 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD5BDLPLBA)—Offset 218h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.173 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD5BDLPUBA)—Offset 21Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.174 Input/Output Stream Descriptor x Control (OSD6CTL)—Offset 220h

Same description as ISD0CTL register at offset 80h.

14.2.175 Input/Output Stream Descriptor x Status (OSD6STS)—Offset 223h

Same description as ISD0STS register at offset 83h.

14.2.176 Input/Output Stream Descriptor x Link Position in Buffer (OSD6LPIB)—Offset 224h

Same description as ISD0LPIB register at offset 84h.

14.2.177 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD6CBL)—Offset 228h

Same description as ISD0CBL register at offset 88h.

14.2.178 Input/Output Stream Descriptor x Last Valid Index (OSD6LVI)—Offset 22Ch

Same description as ISD0LVI register at offset 8Ch.

14.2.179 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD6FIFOW)—Offset 22Eh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.180 Input/Output Stream Descriptor x FIFO Size (OSD6FIFOS)—Offset 230h

Same description as ISD0FIFOS register at offset 90h.

14.2.181 Input/Output Stream Descriptor x Format (OSD6FMT)—Offset 232h

Same description as ISD0FMT register at offset 92h.

14.2.182 Input/Output Stream Descriptor x FIFO Limit (OSD6FIFOL)—Offset 234h

Same description as ISD0FIFOL register at offset 94h.

14.2.183 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD6BDLPLBA)—Offset 238h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.184 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD6BDLPUBA)—Offset 23Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.185 Input/Output Stream Descriptor x Control (OSD7CTLB0)—Offset 240h

SRST bit is not affected by stream reset.

14.2.186 Input/Output Stream Descriptor x Control (OSD7CTL)—Offset 240h

Same description as ISD0CTL register at offset 80h.

14.2.187 Input/Output Stream Descriptor x Control (OSD7CTLB2)—Offset 242h

SRST bit is not affected by stream reset.

14.2.188 Input/Output Stream Descriptor x Status (OSD7STS)—Offset 243h

Same description as ISD0STS register at offset 83h.

14.2.189 Input/Output Stream Descriptor x Link Position in Buffer (OSD7LPIB)—Offset 244h

Same description as ISD0LPIB register at offset 84h.

14.2.190 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD7CBL)—Offset 248h

Same description as ISD0CBL register at offset 88h.

14.2.191 Input/Output Stream Descriptor x Last Valid Index (OSD7LVI)—Offset 24Ch

Same description as ISD0LVI register at offset 8Ch.

14.2.192 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD7FIFOW)—Offset 24Eh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.193 Input/Output Stream Descriptor x FIFO Size (OSD7FIFOS)—Offset 250h

Same description as ISD0FIFOS register at offset 90h.

14.2.194 Input/Output Stream Descriptor x Format (OSD7FMT)—Offset 252h

Same description as ISD0FMT register at offset 92h.

14.2.195 Input/Output Stream Descriptor x FIFO Limit (OSD7FIFOL)—Offset 254h

Same description as ISD0FIFOL register at offset 94h.

14.2.196 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD7BDLPLBA)—Offset 258h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.197 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD7BDLPUBA)—Offset 25Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.198 Input/Output Stream Descriptor x Control (OSD8CTL)—Offset 260h

Same description as ISD0CTL register at offset 80h.

14.2.199 Input/Output Stream Descriptor x Status (OSD8STS)—Offset 263h

Same description as ISD0STS register at offset 83h.

14.2.200 Input/Output Stream Descriptor x Link Position in Buffer (OSD8LPIB)—Offset 264h

Same description as ISD0LPIB register at offset 84h.

14.2.201 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD8CBL)—Offset 268h

Same description as ISD0CBL register at offset 88h.

14.2.202 Input/Output Stream Descriptor x Last Valid Index (OSD8LVI)—Offset 26Ch

Same description as ISD0LVI register at offset 8Ch.

14.2.203 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD8FIFOW)—Offset 26Eh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.204 Input/Output Stream Descriptor x FIFO Size (OSD8FIFOS)—Offset 270h

Same description as ISD0FIFOS register at offset 90h.

14.2.205 Input/Output Stream Descriptor x Format (OSD8FMT)—Offset 272h

Same description as ISD0FMT register at offset 92h.

14.2.206 Input/Output Stream Descriptor x FIFO Limit (OSD8FIFOL)—Offset 274h

Same description as ISD0FIFOL register at offset 94h.

14.2.207 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD8BDLPLBA)—Offset 278h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.208 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD8BDLPUBA)—Offset 27Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.209 Input/Output Stream Descriptor x Control (ISD7CTL)—Offset 280h

Same description as ISD0CTL register at offset 80h.

14.2.210 Input/Output Stream Descriptor x Status (ISD7STS)—Offset 283h

Same description as ISD0STS register at offset 83h.

14.2.211 Input/Output Stream Descriptor x Link Position in Buffer (ISD7LPIB)—Offset 284h

Same description as ISD0LPIB register at offset 84h.

14.2.212 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD7CBL)—Offset 288h

Same description as ISD0CBL register at offset 88h.

14.2.213 Input/Output Stream Descriptor x Last Valid Index (ISD7LVI)—Offset 28Ch

Same description as ISD0LVI register at offset 8Ch.

14.2.214 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD7FIFOW)—Offset 28Eh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.215 Input/Output Stream Descriptor x FIFO Size (ISD7FIFOS)—Offset 290h

Same description as ISD0FIFOS register at offset 90h.

14.2.216 Input/Output Stream Descriptor x Format (ISD7FMT)—Offset 292h

Same description as ISD0FMT register at offset 92h.

14.2.217 Input/Output Stream Descriptor x FIFO Limit (ISD7FIFOL)—Offset 294h

Same description as ISD0FIFOL register at offset 94h.

14.2.218 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD7BDLPLBA)—Offset 298h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.219 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD7BDLPUBA)—Offset 29Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.220 Input/Output Stream Descriptor x Control (ISD8CTL)—Offset 2A0h

Same description as ISD0CTL register at offset 80h.

14.2.221 Input/Output Stream Descriptor x Status (ISD8STS)—Offset 2A3h

Same description as ISD0STS register at offset 83h.

14.2.222 Input/Output Stream Descriptor x Link Position in Buffer (ISD8LPIB)—Offset 2A4h

Same description as ISD0LPIB register at offset 84h.

14.2.223 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD8CBL)—Offset 2A8h

Same description as ISD0CBL register at offset 88h.

14.2.224 Input/Output Stream Descriptor x Last Valid Index (ISD8LVI)—Offset 2ACh

Same description as ISD0LVI register at offset 8Ch.

14.2.225 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD8FIFOW)—Offset 2AEh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.226 Input/Output Stream Descriptor x FIFO Size (ISD8FIFOS)—Offset 2B0h

Same description as ISD0FIFOS register at offset 90h.

14.2.227 Input/Output Stream Descriptor x Format (ISD8FMT)—Offset 2B2h

Same description as ISD0FMT register at offset 92h.

14.2.228 Input/Output Stream Descriptor x FIFO Limit (ISD8FIFOL)—Offset 2B4h

Same description as ISD0FIFOL register at offset 94h.

14.2.229 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD8BDLPLBA)—Offset 2B8h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.230 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD8BDLPUBA)—Offset 2BCh

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.231 Input/Output Stream Descriptor x Control (ISD9CTL)—Offset 2C0h

Same description as ISD0CTL register at offset 80h.

14.2.232 Input/Output Stream Descriptor x Status (ISD9STS)—Offset 2C3h

Same description as ISD0STS register at offset 83h.

14.2.233 Input/Output Stream Descriptor x Link Position in Buffer (ISD9LPIB)—Offset 2C4h

Same description as ISD0LPIB register at offset 84h.

14.2.234 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD9CBL)—Offset 2C8h

Same description as ISD0CBL register at offset 88h.

14.2.235 Input/Output Stream Descriptor x Last Valid Index (ISD9LVI)—Offset 2CCh

Same description as ISD0LVI register at offset 8Ch.

14.2.236 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD9FIFOW)—Offset 2CEh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.237 Input/Output Stream Descriptor x FIFO Size (ISD9FIFOS)—Offset 2D0h

Same description as ISD0FIFOS register at offset 90h.

14.2.238 Input/Output Stream Descriptor x Format (ISD9FMT)—Offset 2D2h

Same description as ISD0FMT register at offset 92h.

14.2.239 Input/Output Stream Descriptor x FIFO Limit (ISD9FIFOL)—Offset 2D4h

Same description as ISD0FIFOL register at offset 94h.

14.2.240 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD9BDLPLBA)—Offset 2D8h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.241 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD9BDLPUBA)—Offset 2DCh

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.242 Input/Output Stream Descriptor x Control (ISD10CTL)—Offset 2E0h

Same description as ISD0CTL register at offset 80h.

14.2.243 Input/Output Stream Descriptor x Status (ISD10STS)—Offset 2E3h

Same description as ISD0STS register at offset 83h.

14.2.244 Input/Output Stream Descriptor x Link Position in Buffer (ISD10LPIB)—Offset 2E4h

Same description as ISD0LPIB register at offset 84h.

14.2.245 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD10CBL)—Offset 2E8h

Same description as ISD0CBL register at offset 88h.

14.2.246 Input/Output Stream Descriptor x Last Valid Index (ISD10LVI)—Offset 2ECh

Same description as ISD0LVI register at offset 8Ch.

14.2.247 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD10FIFOW)—Offset 2EEh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.248 Input/Output Stream Descriptor x FIFO Size (ISD10FIFOS)—Offset 2F0h

Same description as ISD0FIFOS register at offset 90h.

14.2.249 Input/Output Stream Descriptor x Format (ISD10FMT)—Offset 2F2h

Same description as ISD0FMT register at offset 92h.

14.2.250 Input/Output Stream Descriptor x FIFO Limit (ISD10FIFOL)—Offset 2F4h

Same description as ISD0FIFOL register at offset 94h.

14.2.251 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD10BDLPLBA)—Offset 2F8h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.252 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD10BDLPUBA)—Offset 2FCh

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.253 Input/Output Stream Descriptor x Control (ISD11CTL)—Offset 300h

Same description as ISD0CTL register at offset 80h.

14.2.254 Input/Output Stream Descriptor x Status (ISD11STS)—Offset 303h

Same description as ISD0STS register at offset 83h.

14.2.255 Input/Output Stream Descriptor x Link Position in Buffer (ISD11LPIB)—Offset 304h

Same description as ISD0LPIB register at offset 84h.

14.2.256 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD11CBL)—Offset 308h

Same description as ISD0CBL register at offset 88h.

14.2.257 Input/Output Stream Descriptor x Last Valid Index (ISD11LVI)—Offset 30Ch

Same description as ISD0LVI register at offset 8Ch.

14.2.258 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD11FIFOW)—Offset 30Eh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.259 Input/Output Stream Descriptor x FIFO Size (ISD11FIFOS)—Offset 310h

Same description as ISD0FIFOS register at offset 90h.

14.2.260 Input/Output Stream Descriptor x Format (ISD11FMT)—Offset 312h

Same description as ISD0FMT register at offset 92h.

14.2.261 Input/Output Stream Descriptor x FIFO Limit (ISD11FIFOL)—Offset 314h

Same description as ISD0FIFOL register at offset 94h.

14.2.262 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD11BDLPLBA)—Offset 318h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.263 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD11BDLPUBA)—Offset 31Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.264 Input/Output Stream Descriptor x Control (ISD12CTL)—Offset 320h

Same description as ISD0CTL register at offset 80h.

14.2.265 Input/Output Stream Descriptor x Status (ISD12STS)—Offset 323h

Same description as ISD0STS register at offset 83h.

14.2.266 Input/Output Stream Descriptor x Link Position in Buffer (ISD12LPIB)—Offset 324h

Same description as ISD0LPIB register at offset 84h.

14.2.267 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD12CBL)—Offset 328h

Same description as ISD0CBL register at offset 88h.

14.2.268 Input/Output Stream Descriptor x Last Valid Index (ISD12LVI)—Offset 32Ch

Same description as ISD0LVI register at offset 8Ch.

14.2.269 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD12FIFOW)—Offset 32Eh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.270 Input/Output Stream Descriptor x FIFO Size (ISD12FIFOS)—Offset 330h

Same description as ISD0FIFOS register at offset 90h.

14.2.271 Input/Output Stream Descriptor x Format (ISD12FMT)—Offset 332h

Same description as ISD0FMT register at offset 92h.

14.2.272 Input/Output Stream Descriptor x FIFO Limit (ISD12FIFOL)—Offset 334h

Same description as ISD0FIFOL register at offset 94h.

14.2.273 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD12BDLPLBA)—Offset 338h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.274 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD12BDLPUBA)—Offset 33Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.275 Input/Output Stream Descriptor x Control (ISD13CTL)—Offset 340h

Same description as ISD0CTL register at offset 80h.

14.2.276 Input/Output Stream Descriptor x Status (ISD13STS)—Offset 343h

Same description as ISD0STS register at offset 83h.

14.2.277 Input/Output Stream Descriptor x Link Position in Buffer (ISD13LPIB)—Offset 344h

Same description as ISD0LPIB register at offset 84h.

14.2.278 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD13CBL)—Offset 348h

Same description as ISD0CBL register at offset 88h.

14.2.279 Input/Output Stream Descriptor x Last Valid Index (ISD13LVI)—Offset 34Ch

Same description as ISD0LVI register at offset 8Ch.

14.2.280 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD13FIFOW)—Offset 34Eh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.281 Input/Output Stream Descriptor x FIFO Size (ISD13FIFOS)—Offset 350h

Same description as ISD0FIFOS register at offset 90h.

14.2.282 Input/Output Stream Descriptor x Format (ISD13FMT)—Offset 352h

Same description as ISD0FMT register at offset 92h.

14.2.283 Input/Output Stream Descriptor x FIFO Limit (ISD13FIFOL)—Offset 354h

Same description as ISD0FIFOL register at offset 94h.

14.2.284 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD13BDLPLBA)—Offset 358h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.285 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD13BDLPUBA)—Offset 35Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.286 Input/Output Stream Descriptor x Control (ISD14CTL)—Offset 360h

Same description as ISD0CTL register at offset 80h.

14.2.287 Input/Output Stream Descriptor x Status (ISD14STS)—Offset 363h

Same description as ISD0STS register at offset 83h.

14.2.288 Input/Output Stream Descriptor x Link Position in Buffer (ISD14LPIB)—Offset 364h

Same description as ISD0LPIB register at offset 84h.

14.2.289 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD14CBL)—Offset 368h

Same description as ISD0CBL register at offset 88h.

14.2.290 Input/Output Stream Descriptor x Last Valid Index (ISD14LVI)—Offset 36Ch

Same description as ISD0LVI register at offset 8Ch.

14.2.291 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD14FIFOW)—Offset 36Eh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.292 Input/Output Stream Descriptor x FIFO Size (ISD14FIFOS)—Offset 370h

Same description as ISD0FIFOS register at offset 90h.

14.2.293 Input/Output Stream Descriptor x Format (ISD14FMT)—Offset 372h

Same description as ISD0FMT register at offset 92h.

14.2.294 Input/Output Stream Descriptor x FIFO Limit (ISD14FIFOL)—Offset 374h

Same description as ISD0FIFOL register at offset 94h.

14.2.295 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD14BDLPLBA)—Offset 378h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.296 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD14BDLPUBA)—Offset 37Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.297 Input/Output Stream Descriptor x Control (OSD9CTL)—Offset 380h

Same description as ISD0CTL register at offset 80h.

14.2.298 Input/Output Stream Descriptor x Status (OSD9STS)—Offset 383h

Same description as ISD0STS register at offset 83h.

14.2.299 Input/Output Stream Descriptor x Link Position in Buffer (OSD9LPIB)—Offset 384h

Same description as ISD0LPIB register at offset 84h.

14.2.300 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD9CBL)—Offset 388h

Same description as ISD0CBL register at offset 88h.

14.2.301 Input/Output Stream Descriptor x Last Valid Index (OSD9LVI)—Offset 38Ch

Same description as ISD0LVI register at offset 8Ch.

14.2.302 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD9FIFOW)—Offset 38Eh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.303 Input/Output Stream Descriptor x FIFO Size (OSD9FIFOS)—Offset 390h

Same description as ISD0FIFOS register at offset 90h.

14.2.304 Input/Output Stream Descriptor x Format (OSD9FMT)—Offset 392h

Same description as ISD0FMT register at offset 92h.

14.2.305 Input/Output Stream Descriptor x FIFO Limit (OSD9FIFOL)—Offset 394h

Same description as ISD0FIFOL register at offset 94h.

14.2.306 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD9BDLPLBA)—Offset 398h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.307 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD9BDLPUBA)—Offset 39Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.308 Input/Output Stream Descriptor x Control (OSD10CTL)—Offset 3A0h

Same description as ISD0CTL register at offset 80h.

14.2.309 Input/Output Stream Descriptor x Status (OSD10STS)—Offset 3A3h

Same description as ISD0STS register at offset 83h.

14.2.310 Input/Output Stream Descriptor x Link Position in Buffer (OSD10LPIB)—Offset 3A4h

Same description as ISD0LPIB register at offset 84h.

14.2.311 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD10CBL)—Offset 3A8h

Same description as ISD0CBL register at offset 88h.

14.2.312 Input/Output Stream Descriptor x Last Valid Index (OSD10LVI)—Offset 3ACh

Same description as ISD0LVI register at offset 8Ch.

14.2.313 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD10FIFOW)—Offset 3AEh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.314 Input/Output Stream Descriptor x FIFO Size (OSD10FIFOS)—Offset 3B0h

Same description as ISD0FIFOS register at offset 90h.

14.2.315 Input/Output Stream Descriptor x Format (OSD10FMT)—Offset 3B2h

Same description as ISD0FMT register at offset 92h.

14.2.316 Input/Output Stream Descriptor x FIFO Limit (OSD10FIFOL)—Offset 3B4h

Same description as ISD0FIFOL register at offset 94h.

14.2.317 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD10BDLPLBA)—Offset 3B8h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.318 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD10BDLPUBA)—Offset 3BCh

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.319 Input/Output Stream Descriptor x Control (OSD11CTL)—Offset 3C0h

Same description as ISD0CTL register at offset 80h.

14.2.320 Input/Output Stream Descriptor x Status (OSD11STS)—Offset 3C3h

Same description as ISD0STS register at offset 83h.

14.2.321 Input/Output Stream Descriptor x Link Position in Buffer (OSD11LPIB)—Offset 3C4h

Same description as ISD0LPIB register at offset 84h.

14.2.322 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD11CBL)—Offset 3C8h

Same description as ISD0CBL register at offset 88h.

14.2.323 Input/Output Stream Descriptor x Last Valid Index (OSD11LVI)—Offset 3CCh

Same description as ISD0LVI register at offset 8Ch.

14.2.324 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD11FIFOW)—Offset 3CEh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.325 Input/Output Stream Descriptor x FIFO Size (OSD11FIFOS)—Offset 3D0h

Same description as ISD0FIFOS register at offset 90h.

14.2.326 Input/Output Stream Descriptor x Format (OSD11FMT)—Offset 3D2h

Same description as ISD0FMT register at offset 92h.

14.2.327 Input/Output Stream Descriptor x FIFO Limit (OSD11FIFOL)—Offset 3D4h

Same description as ISD0FIFOL register at offset 94h.

14.2.328 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD11BDLPLBA)—Offset 3D8h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.329 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD11BDLPUBA)—Offset 3DCh

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.330 Input/Output Stream Descriptor x Control (OSD12CTL)—Offset 3E0h

Same description as ISD0CTL register at offset 80h.

14.2.331 Input/Output Stream Descriptor x Status (OSD12STS)—Offset 3E3h

Same description as ISD0STS register at offset 83h.

14.2.332 Input/Output Stream Descriptor x Link Position in Buffer (OSD12LPIB)—Offset 3E4h

Same description as ISD0LPIB register at offset 84h.

14.2.333 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD12CBL)—Offset 3E8h

Same description as ISD0CBL register at offset 88h.

14.2.334 Input/Output Stream Descriptor x Last Valid Index (OSD12LVI)—Offset 3ECh

Same description as ISD0LVI register at offset 8Ch.

14.2.335 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD12FIFOW)—Offset 3EEh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.336 Input/Output Stream Descriptor x FIFO Size (OSD12FIFOS)—Offset 3F0h

Same description as ISD0FIFOS register at offset 90h.

14.2.337 Input/Output Stream Descriptor x Format (OSD12FMT)—Offset 3F2h

Same description as ISD0FMT register at offset 92h.

14.2.338 Input/Output Stream Descriptor x FIFO Limit (OSD12FIFOL)—Offset 3F4h

Same description as ISD0FIFOL register at offset 94h.

14.2.339 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD12BDLPLBA)—Offset 3F8h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.340 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD12BDLPUBA)—Offset 3FCh

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.341 Input/Output Stream Descriptor x Control (OSD13CTL)—Offset 400h

Same description as ISD0CTL register at offset 80h.

14.2.342 Input/Output Stream Descriptor x Status (OSD13STS)—Offset 403h

Same description as ISD0STS register at offset 83h.

14.2.343 Input/Output Stream Descriptor x Link Position in Buffer (OSD13LPIB)—Offset 404h

Same description as ISD0LPIB register at offset 84h.

14.2.344 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD13CBL)—Offset 408h

Same description as ISD0CBL register at offset 88h.

14.2.345 Input/Output Stream Descriptor x Last Valid Index (OSD13LVI)—Offset 40Ch

Same description as ISD0LVI register at offset 8Ch.

14.2.346 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD13FIFOW)—Offset 40Eh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.347 Input/Output Stream Descriptor x FIFO Size (OSD13FIFOS)—Offset 410h

Same description as ISD0FIFOS register at offset 90h.

14.2.348 Input/Output Stream Descriptor x Format (OSD13FMT)—Offset 412h

Same description as ISD0FMT register at offset 92h.

14.2.349 Input/Output Stream Descriptor x FIFO Limit (OSD13FIFOL)—Offset 414h

Same description as ISD0FIFOL register at offset 94h.

14.2.350 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD13BDLPLBA)—Offset 418h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.351 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD13BDLPUBA)—Offset 41Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.352 Input/Output Stream Descriptor x Control (OSD14CTL)—Offset 420h

Same description as ISD0CTL register at offset 80h.

14.2.353 Input/Output Stream Descriptor x Status (OSD14STS)—Offset 423h

Same description as ISD0STS register at offset 83h.

14.2.354 Input/Output Stream Descriptor x Link Position in Buffer (OSD14LPIB)—Offset 424h

Same description as ISD0LPIB register at offset 84h.

14.2.355 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD14CBL)—Offset 428h

Same description as ISD0CBL register at offset 88h.

14.2.356 Input/Output Stream Descriptor x Last Valid Index (OSD14LVI)—Offset 42Ch

Same description as ISD0LVI register at offset 8Ch.

14.2.357 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD14FIFOW)—Offset 42Eh

Same description as ISD0FIFOW register at offset 8Eh.

14.2.358 Input/Output Stream Descriptor x FIFO Size (OSD14FIFOS)—Offset 430h

Same description as ISD0FIFOS register at offset 90h.

14.2.359 Input/Output Stream Descriptor x Format (OSD14FMT)—Offset 432h

Same description as ISD0FMT register at offset 92h.

14.2.360 Input/Output Stream Descriptor x FIFO Limit (OSD14FIFOL)—Offset 434h

Same description as ISD0FIFOL register at offset 94h.

14.2.361 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD14BDLPLBA)—Offset 438h

Same description as ISD0BDLPLBA register at offset 98h.

14.2.362 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD14BDLPUBA)—Offset 43Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

14.2.363 Global Time Synchronization Capability Header (GTSCH)—Offset 500h

This register declares the global time synchronization capability structure.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 11F00h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RW/L	**Capability Version (VER):** This field is an Intel HD Audio Specification defined version number that indicates the version of the capability structure present. Locked when FNCFG.BCLD = 1.
27:16	1h RW/L	**Capability Identifier (ID):** This field is an Intel HD Audio Specification defined ID number that indicates the nature and format of the capability. Locked when FNCFG.BCLD = 1.
15:0	1F00h RW/L	**Next Capability Pointer (PTR):** This field contains the offset to the next capability structure or 000h if no other items exist in the linked list of capabilities. Point to DMA resume capability. Locked when FNCFG.BCLD = 1.

14.2.364 Global Time Synchronization Capability Declaration (GTSCD)—Offset 504h

This register identifies the general global time synchronization associated capabilities.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RO	**Controller Based Synchronization Adjust Supported (CTLSAS):** When set, it indicates that the controller based synchronization adjustment is supported. By adjusting the global link clock which is used as reference clock for the codecs DAC / ADC, the codec will indirectly changing the rate of all its active streams. Locked when FNCFG.BCLD = 1.
1:0	0h RO	Reserved.

14.2.365 Global Time Synchronization Capture Control (GTSCC0)—Offset 520h

This register controls the global time synchronization capture operation, and snapshots ART value as the global time stamp counter value.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW/1C/V	**Time Stamp Counter Capture Done (TSCCD):** This bit is set when a valid TSC value has been captured: WALFCC, TSCCL, TSCCU, LLPFOC, LLPCL, and LLPCH contain valid data. The Intel HD Audio driver software must acknowledge the completion by writing 1 to clear this bit.
30	0h RW	**Time Stamp Counter Capture Done Interrupt Enable (TSCCDIE):** If set to 1, TSCCD bit can pass through to cause an interrupt status reported in INTSTS.CIS bit, and cause an interrupt to CPU if INTCTL.CIE = 1 and INTCTL.GIE = 1.
29:6	0h RO	Reserved.
5	0h RW/1S/V	**Time Stamp Counter Capture Initiate (TSCCI):** Write to 1 to initiate Global Time Synchronization capture for measuring TSC offset to local wall frame info. Cleared to 0 by hardware when the process is completed.
4:0	0h RW	**Capture DMA Select (CDMAS):** To select which DMA's LLPL, and LLPU value to be captured together with the TSC value. Bit 4 = 1 for ODMA, 0 for IDMA Bit 3:0 indicates the respective DMA engine index. Programmed before TSCCI = 1.

14.2.366 Wall Frame Counter Captured (WALFCC0)—Offset 524h

This register reports the wall frame counter captured.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:9	0h RO/V	**Frame Number (FN):** Indicates the 23 bit frame number captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.
8:0	0h RO/V	**Clock in Frame (CIF):** Indicates the 9 bit clock in frame value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

14.2.367 Time Stamp Counter Captured Lower (TSCCL0)—Offset 528h

This register reports the ART value snapshot as the global time stamp counter captured (lower 32 bits).

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Counter Captured Lower (CCL):** Indicates the lower 32 bit TSC value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

14.2.368 Time Stamp Counter Captured Upper (TSCCU0)—Offset 52Ch

This register reports the ART value snapshot as the global time stamp counter captured (upper 32 bits).

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Counter Captured Upper (CCU):** Indicates the upper 32 bit TSC value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

14.2.369 Linear Link Position Frame Offset Captured (LLPFOC0)—Offset 534h

This register is to report additional accuracy details for captures made in between of two updates of LLP values, in number of 48 KHz HD Audio frames of the corresponding link. Audio streams with 44.1 KHz base rate and non zero divider FMT value will skip frames periodically on the Intel HD Audio link and Intel iDisplay Audio link in order to normalize its sampling rate to the 48 KHz HD Audio frame rate; hence; the frame offset will be useful in these cases.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RO/V	**Frame Offset Captured (FOC):** When the LLPCL and LLPCU registers are updated, this field records the elapsed number of 48 KHz HD Audio frames since the last LLP value change. Valid and static when GTSCC.TSCCD = 1

14.2.370 Linear Link Position Captured Lower (LLPCL0)—Offset 538h

This register reports the linear link position counter captured (lower 32 bits).

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Linear Link Position Captured Lower (LLPCL):** Indicates the lower 32 bit linear link position value of the link DMA captured as a result of Global Time Synchronization capture request. Note that the LLPCL value that is captured is the LLPL value at the previous HD Audio frame boundary, not the live LLPL register value which may be changing in the middle of the current frame. Valid and static when GTSCC.TSCCD = 1.

14.2.371 Linear Link Position Captured Upper (LLPCU0)—Offset 53Ch

This register reports the time stamp counter captured (upper 32 bits).

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Linear Link Position Captured Upper (LLPCU):** Indicates the upper 32 bit linear link position value of the link DMA captured as a result of Global Time Synchronization capture request. Note that the LLPCU value that is captured is the LLPU value at the previous HD Audio frame boundary, not the live LLPU register value which may be changing in the middle of the current frame. Valid and static when GTSCC.TSCCD = 1.

14.2.372 Global Time Synchronization Capture Control (GTSCC1)—Offset 540h

Same definition as GTSCC0 at offset 520h.

14.2.373 Wall Frame Counter Captured (WALFCC1)—Offset 544h

Same definition as WALFCC0 at offset 524h.

14.2.374 Time Stamp Counter Captured Lower (TSCCL1)—Offset 548h

Same definition as TSCCL0 at offset 528h.

14.2.375 Time Stamp Counter Captured Upper (TSCCU1)—Offset 54Ch

Same definition as TSCCU0 at offset 52Ch.

14.2.376 Linear Link Position Frame Offset Captured (LLPFOC1)—Offset 554h

Same definition as LLPFOC0 at offset 534h.

14.2.377 Linear Link Position Captured Lower (LLPCL1)—Offset 558h

Same definition as LLPCL0 at offset 538h.

14.2.378 Linear Link Position Captured Upper (LLPCU1)—Offset 55Ch

Same definition as LLPCU0 at offset 53Ch.

14.2.379 Processing Pipe Capability Header (PPCH)—Offset 800h

This register declares the processing pipe capability structure.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 30500h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RW/L	**Capability Version (VER):** This field is an Intel HD Audio Specification defined version number that indicates the version of the capability structure present. Locked when FNCFG.BCLD = 1.
27:16	3h RW/L	**Capability Identifier (ID):** This field is an Intel HD Audio Specification defined ID number that indicates the nature and format of the capability. Locked when FNCFG.BCLD = 1.
15:0	500h RW/L	**Next Capability Pointer (PTR):** This field contains the offset to the next capability structure or 000h if no other items exist in the linked list of capabilities. Point to Global Time Synchronization capability. Locked when FNCFG.BCLD = 1.

14.2.380 Processing Pipe Control (PPCTL)—Offset 804h

This register is not affected by stream reset.
Note that the PROCEN bit should only be modified when the corresponding host DMA and link DMA are idle, i.e. RUN bits are cleared, and the DMA contexts have been destroyed through SRST bits if it was previously activated.
Note that GPROCEN bit does not really enable or disable the Audio DSP operation, but mainly to workaround some legacy Intel HD Audio driver software such that if GPROCEN = 0, ADSPxBA (BAR2) is mapped to the Intel HD Audio memory mapped configuration registers, for compliancy with some legacy SW implementation. If GPROCEN = 1, only then ADSPxBA (BAR2) is mapped to the actual Audio DSP memory mapped configuration registers.
The number of PROCEN bits in this register is depending on the total number of stream DMA implemented.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW	**Processing Interrupt Enable (PIE):** Enables the general interrupt for the Audio DSP function. When set to 1 (and GIE is enabled), the Audio DSP generates an interrupt when the PIS bit gets set.
30:16	0h RO	Reserved.
15:0	0h RW	**Processing Enable (PROCEN):** When set to 1 the DMA engine associated with this stream will be enabled to route the audio stream to DSP audio pipes in the Audio DSP for processing. When cleared to 0 the DMA engine associated with this stream will be bypassing the Audio DSP and route the audio stream directly to the audio link.

14.2.381 Processing Pipe Status (PPSTS)—Offset 808h

This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO/V	**Processing Interrupt Status (PIS):** Status of general interrupt for the Audio DSP function. A 1 indicates that an interrupt condition occurred in the Audio DSP function. The exact cause can be determined by interrogating the ADSPIS register. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of the interrupt status bits in ADSPIS register.
30:0	0h RO	Reserved.

14.2.382 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC0LLPL)—Offset 810h

Detail description is in their respective fields. There can be up to 15 input / output processing pipes with each pipe having their own register set. Offset for IPPHCxLLPL for each pipe is below.

Input stream 0: Offset 810h
Input stream 1: Offset 820h
Input stream 2: Offset 830h
Input stream 3: Offset 840h
Input stream 4: Offset 850h
Input stream 5: Offset 860h
Input stream 6: Offset 870h
Input stream 7: Offset 4A10h
Input stream 8: Offset 4A20h
Input stream 9: Offset 4A30h
Input stream 10: Offset 4A40h
Input stream 11: Offset 4A50h
Input stream 12: Offset 4A60h
Input stream 13: Offset 4A70h
Input stream 14: Offset 4A80h

Output stream 0: Offset 880h
Output stream 1: Offset 890h
Output stream 2: Offset 8A0h
Output stream 3: Offset 8B0h
Output stream 4: Offset 8C0h
Output stream 5: Offset 8D0h
output stream 6: Offset 8E0h
Output stream 7: Offset 8F0h
Output stream 8: Offset 900h
Output stream 9: Offset 4A90h
Output stream 10: Offset 4AA0h
Output stream 11: Offset 4AB0h
Output stream 12: Offset 4AC0h
Output stream 13: Offset 4AD0h
Output stream 14: Offset 4AE0h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.383 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC0LLPU)—Offset 814h

Detail description is in their respective fields. There can be up to 15 input / output processing pipes with each pipe having their own register set. Offset for IPPHCxLLPU for each pipe is below.

Input stream 0: Offset 814h
Input stream 1: Offset 824h
Input stream 2: Offset 834h
Input stream 3: Offset 844h
Input stream 4: Offset 854h
Input stream 5: Offset 864h
Input stream 6: Offset 874h
Input stream 7: Offset 4A10h
Input stream 8: Offset 4A24h
Input stream 9: Offset 4A34h
Input stream 10: Offset 4A44h
Input stream 11: Offset 4A54h
Input stream 12: Offset 4A64h
Input stream 13: Offset 4A74h
Input stream 14: Offset 4A84h

Output stream 0: Offset 884h
Output stream 1: Offset 894h
Output stream 2: Offset 8A4h
Output stream 3: Offset 8B4h
Output stream 4: Offset 8C4h
Output stream 5: Offset 8D4h
output stream 6: Offset 8E4h
Output stream 7: Offset 8F4h
Output stream 8: Offset 904h
Output stream 9: Offset 4A94h
Output stream 10: Offset 4AA4h
Output stream 11: Offset 4AB4h
Output stream 12: Offset 4AC4h
Output stream 13: Offset 4AD4h
Output stream 14: Offset 4AE4h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.384 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC0LDPL)—Offset 818h

Detail description is in their respective fields. There can be up to 15 input / output processing pipes with each pipe having their own register set. Offset for IPPHCxLDPL for each pipe is below.

Input stream 0: Offset 818h
Input stream 1: Offset 828h
Input stream 2: Offset 838h
Input stream 3: Offset 848h
Input stream 4: Offset 858h
Input stream 5: Offset 868h
Input stream 6: Offset 878h
Input stream 7: Offset 4A18h
Input stream 8: Offset 4A28h
Input stream 9: Offset 4A38h
Input stream 10: Offset 4A48h
Input stream 11: Offset 4A58h
Input stream 12: Offset 4A60h
Input stream 13: Offset 4A70h
Input stream 14: Offset 4A88h

Output stream 0: Offset 888h
Output stream 1: Offset 898h
Output stream 2: Offset 8A8h
Output stream 3: Offset 8B8h
Output stream 4: Offset 8C8h
Output stream 5: Offset 8D8h
output stream 6: Offset 8E8h
Output stream 7: Offset 8F8h
Output stream 8: Offset 908h
Output stream 9: Offset 4A98h
Output stream 10: Offset 4AA8h
Output stream 11: Offset 4AB8h
Output stream 12: Offset 4AC8h
Output stream 13: Offset 4AD8h
Output stream 14: Offset 4AE8h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.385 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC0LDPU)—Offset 81Ch

Detail description is in their respective fields. There can be up to 15 input / output processing pipes with each pipe having their own register set. Offset for IPPHCxLDPU for each pipe is below.

Input stream 0: Offset 81Ch
Input stream 1: Offset 82Ch
Input stream 2: Offset 83Ch
Input stream 3: Offset 84Ch
Input stream 4: Offset 85Ch
Input stream 5: Offset 86Ch
Input stream 6: Offset 87Ch
Input stream 7: Offset 4A1Ch
Input stream 8: Offset 4A2Ch
Input stream 9: Offset 4A3Ch
Input stream 10: Offset 4A4Ch
Input stream 11: Offset 4A5Ch
Input stream 12: Offset 4A6Ch
Input stream 13: Offset 4A7Ch
Input stream 14: Offset 4A8Ch

Output stream 0: Offset 88Ch
Output stream 1: Offset 89Ch
Output stream 2: Offset 8ACh
Output stream 3: Offset 8BCh
Output stream 4: Offset 8CCh
Output stream 5: Offset 8DCh
output stream 6: Offset 8ECh
Output stream 7: Offset 8FCh
Output stream 8: Offset 90Ch
Output stream 9: Offset 4A9Ch
Output stream 10: Offset 4AACh
Output stream 11: Offset 4ABCh
Output stream 12: Offset 4ACCh
Output stream 13: Offset 4ADCh
Output stream 14: Offset 4AECh

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.386 Input/Output Processing Pipe's Link Connection x Control (IPPLC0CTL)—Offset 910h

Detail description is in their respective fields. There can be up to 15 input / output processing pipes with each pipe having their own register set. Offset for IPPLCxCTL for each pipe is below.

Input stream 0: Offset 910h
Input stream 1: Offset 920h
Input stream 2: Offset 930h
Input stream 3: Offset 940h
Input stream 4: Offset 950h
Input stream 5: Offset 960h
Input stream 6: Offset 970h
Input stream 7: Offset 4AF0h
Input stream 8: Offset 4B00h
Input stream 9: Offset 4B10h
Input stream 10: Offset 4B20h
Input stream 11: Offset 4B30h
Input stream 12: Offset 4B40h
Input stream 13: Offset 4B50h
Input stream 14: Offset 4B60h

Output stream 0: Offset 980h
Output stream 1: Offset 990h
Output stream 2: Offset 9A0h
Output stream 3: Offset 9B0h
Output stream 4: Offset 9C0h
Output stream 5: Offset 9D0h
output stream 6: Offset 9E0h
Output stream 7: Offset 9F0h
Output stream 8: Offset A00h
Output stream 9: Offset 4B70h
Output stream 10: Offset 4B80h
Output stream 11: Offset 4B90h
Output stream 12: Offset 4BA0h
Output stream 13: Offset 4BB0h
Output stream 14: Offset 4BC0h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

14.2.387 Input/Output Processing Pipe's Link Connection x Format (IPPLC0FMT)—Offset 914h

Detail description is in their respective fields. There can be up to 15 input / output processing pipes with each pipe having their own register set. Offset for IPPLCxFMT for each pipe is below.

Input stream 0: Offset 914h
Input stream 1: Offset 924h
Input stream 2: Offset 934h
Input stream 3: Offset 944h
Input stream 4: Offset 954h
Input stream 5: Offset 964h
Input stream 6: Offset 974h
Input stream 7: Offset 4AF4h
Input stream 8: Offset 4B04h
Input stream 9: Offset 4B14h
Input stream 10: Offset 4B24h
Input stream 11: Offset 4B34h
Input stream 12: Offset 4B44h

Input stream 13: Offset 4B54h
Input stream 14: Offset 4B64h

Output stream 0: Offset 984h
Output stream 1: Offset 994h
Output stream 2: Offset 9A4h
Output stream 3: Offset 9B4h
Output stream 4: Offset 9C4h
Output stream 5: Offset 9D4h
output stream 6: Offset 9E4h
Output stream 7: Offset 9F4h
Output stream 8: Offset A04h
Output stream 9: Offset 4B74h
Output stream 10: Offset 4B84h
Output stream 11: Offset 4B94h
Output stream 12: Offset 4BA4h
Output stream 13: Offset 4BB4h
Output stream 14: Offset 4BC4h

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

14.2.388 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC0LLPL)—Offset 918h

Detail description is in their respective fields. There can be up to 15 input / output processing pipes with each pipe having their own register set. Offset for IPPLCxLLPL for each pipe is below.

Input stream 0: Offset 918h
Input stream 1: Offset 928h
Input stream 2: Offset 938h
Input stream 3: Offset 948h
Input stream 4: Offset 958h
Input stream 5: Offset 968h
Input stream 6: Offset 978h
Input stream 7: Offset 4AF8h
Input stream 8: Offset 4B08h
Input stream 9: Offset 4B18h
Input stream 10: Offset 4B28h
Input stream 11: Offset 4B38h
Input stream 12: Offset 4B48h
Input stream 13: Offset 4B58h
Input stream 14: Offset 4B68h

Output stream 0: Offset 988h
Output stream 1: Offset 998h
Output stream 2: Offset 9A8h
Output stream 3: Offset 9B8h
Output stream 4: Offset 9C8h
Output stream 5: Offset 9D8h
output stream 6: Offset 9E8h
Output stream 7: Offset 9F8h
Output stream 8: Offset A08h
Output stream 9: Offset 4B78h
Output stream 10: Offset 4B88h
Output stream 11: Offset 4B98h
Output stream 12: Offset 4BA8h
Output stream 13: Offset 4BB8h
Output stream 14: Offset 4BC8h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.389 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC0LLPU)—Offset 91Ch

Detail description is in their respective fields. There can be up to 15 input / output processing pipes with each pipe having their own register set. Offset for IPPLCxLLPU for each pipe is below.

Input stream 0: Offset 91ch
Input stream 1: Offset 92ch
Input stream 2: Offset 93Ch
Input stream 3: Offset 94Ch
Input stream 4: Offset 95Ch
Input stream 5: Offset 96Ch
Input stream 6: Offset 97Ch
Input stream 7: Offset 4AFCh
Input stream 8: Offset 4B0Ch
Input stream 9: Offset 4B1Ch
Input stream 10: Offset 4B2Ch
Input stream 11: Offset 4B3Ch
Input stream 12: Offset 4B4Ch
Input stream 13: Offset 4B5Ch
Input stream 14: Offset 4B6Ch

Output stream 0: Offset 98Ch
Output stream 1: Offset 99Ch
Output stream 2: Offset 9ACh
Output stream 3: Offset 9BCh
Output stream 4: Offset 9CCh
Output stream 5: Offset 9DCh
output stream 6: Offset 9ECh
Output stream 7: Offset 9FCh
Output stream 8: Offset A0Ch
Output stream 9: Offset 4B7Ch
Output stream 10: Offset 4B8Ch
Output stream 11: Offset 4B9Ch
Output stream 12: Offset 4BACh
Output stream 13: Offset 4BBCh
Output stream 14: Offset 4BCCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.390 Multiple Links Capability Header (MLCH)—Offset C00h

This register declares the multiple links capability structure.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 20800h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RW/L	**Capability Version (VER):** This field is an Intel HD Audio Specification defined version number that indicates the version of the capability structure present. Locked when FNCFG.BCLD = 1.
27:16	2h RW/L	**Capability Identifier (ID):** This field is an Intel HD Audio Specification defined ID number that indicates the nature and format of the capability. Locked when FNCFG.BCLD = 1.
15:0	800h RW/L	**Next Capability Pointer (PTR):** This field contains the offset to the next capability structure or 000h if no other items exist in the linked list of capabilities. Point to Processing Pipe capability. Locked when FNCFG.BCLD = 1.

14.2.391 Multiple Links Capability Declaration (MLCD)—Offset C04h

This register identifies the general multiple links associated capabilities.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	1h RO	**Link Count (LCOUNT):** Indicates the number of links. Up to 15 links can be supported. A '0' indicates 1 link, and '1110' indicates 15 links. Note: '1111' is reserved. Note that this Link Count is the cumulative total number of links where the links can be heterogeneous.

14.2.392 Link 0 Capabilities (LCAP0)—Offset C40h

This register identifies the specific link associated capabilities

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 7h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RW/L	**Audio Link Type (ALT):** Indicates which Link Type this link belongs to. 0001-1111 = Reserved 0000 = Intel HD Audio Link Reset value is hardcoded to parameter LCAPALT[x*4+3:x*4]. Locked when FNCFG.BCLD = 1.
27:26	0h RO	Reserved.
25:24	0h RW/L	**Number of Serial Data Out Signals (NSDO):** 00b indicates that the Intel HD Audio controller supports one Serial Data Output signal. Locked when FNCFG.BCLD = 1.
23:6	0h RO	Reserved.
5	0h RW/L	**192 MHz Supported (S192):** Indicates 192 MHz clock is supported. Reset value is hardcoded to parameter DEFLCAPS192[x]. Locked when FNCFG.BCLD = 1.
4	0h RW/L	**96 MHz Supported (S96):** Indicates 96 MHz clock is supported. Reset value is hardcoded to parameter DEFLCAPS96[x]. Locked when FNCFG.BCLD = 1.
3	0h RW/L	**48 MHz Supported (S48):** Indicates 48 MHz clock is supported. Reset value is hardcoded to parameter DEFLCAPS48[x]. Locked when FNCFG.BCLD = 1.
2	1h RW/L	**24 MHz Supported (S24):** Indicates 24 MHz clock is supported. Reset value is hardcoded to parameter DEFLCAPS24[x]. Locked when FNCFG.BCLD = 1.
1	1h RW/L	**12 MHz Supported (S12):** Indicates 12 MHz clock is supported. Reset value is hardcoded to parameter DEFLCAPS12[x]. Locked when FNCFG.BCLD = 1.
0	1h RW/L	**6 MHz Supported (S6):** Indicates 6 MHz clock is supported. Reset value is hardcoded to parameter DEFLCAPS6[x]. Locked when FNCFG.BCLD = 1.

14.2.393 Link Control 0 (LCTL0)—Offset C44h

Link x Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 10002h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RO/V	**Current Power Active (CPA):** This value changes to the value set by SPA when the power of the link has reached that state. Software sets SPA, then monitors CPA to know when the link has changed state.
22:17	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
16	1h RW	**Set Power Active (SPA):** Software sets this bit to '1' to turn the link on (provided CRSTB = 1), and clears it to '0' when it wishes to turn the link off. When CPA matches the value of this bit, the achieved power state has been reached. Software is expected to wait for CPA to match SPA before it can program SPA again. Any deviation may result in undefined behaviour
15:4	0h RO	Reserved.
3:0	2h RW	**Set Clock Frequency (SCF):** Indicates the frequency that software wishes the link to run at. Changing this value to a value not supported by Link Capabilities shall result in indeterminate results. The possible encodings are: Encoding Frequency 0000 6 MHz 0001 12 MHz 0010 24 MHz 0011 48 MHz 0100 96 MHz 0101 Reserved for 192 MHz 0110-1111 Reserved

14.2.394 Link 0 Output Stream ID Mapping Valid (LOSIDV0)—Offset C48h

This register maps the output stream connection for specific link.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: FFFEh

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	1h RW	**Output Stream ID of 15 is Valid for this Link (L1OSIDV15):** This link will claim / forward output cycles with Stream ID = 1111b.
14	1h RW	**Output Stream ID of 14 is Valid for this Link (L1OSIDV14):** This link will claim / forward output cycles with Stream ID = 1110b.
13	1h RW	**Output Stream ID of 13 is Valid for this Link (L1OSIDV13):** This link will claim / forward output cycles with Stream ID = 1101b.
12	1h RW	**Output Stream ID of 12 is Valid for this Link (L1OSIDV12):** This link will claim / forward output cycles with Stream ID = 1100b.
11	1h RW	**Output Stream ID of 11 is Valid for this Link (L1OSIDV11):** This link will claim / forward output cycles with Stream ID = 1011b.
10	1h RW	**Output Stream ID of 10 is Valid for this Link (L1OSIDV10):** This link will claim / forward output cycles with Stream ID = 1010b.
9	1h RW	**Output Stream ID of 9 is Valid for this Link (L1OSIDV9):** This link will claim / forward output cycles with Stream ID = 1001b.
8	1h RW	**Output Stream ID of 8 is Valid for this Link (L1OSIDV8):** This link will claim / forward output cycles with Stream ID = 1000b.

Bit Range	Default and Access	Field Name (ID): Description
7	1h RW	**Output Stream ID of 7 is Valid for this Link (L1OSIDV7):** This link will claim / forward output cycles with Stream ID = 0111b.
6	1h RW	**Output Stream ID of 6 is Valid for this Link (L1OSIDV6):** This link will claim / forward output cycles with Stream ID = 0110b.
5	1h RW	**Output Stream ID of 5 is Valid for this Link (L1OSIDV5):** This link will claim / forward output cycles with Stream ID = 0101b.
4	1h RW	**Output Stream ID of 4 is Valid for this Link (L1OSIDV4):** This link will claim / forward output cycles with Stream ID = 0100b.
3	1h RW	**Output Stream ID of 3 is Valid for this Link (L1OSIDV3):** This link will claim / forward output cycles with Stream ID = 0011b.
2	1h RW	**Output Stream ID of 2 is Valid for this Link (L1OSIDV2):** This link will claim / forward output cycles with Stream ID = 0010b.
1	1h RW	**Output Stream ID of 1 is Valid for this Link (L1OSIDV1):** This link will claim / forward output cycles with Stream ID = 0001b.
0	0h RO	Reserved.

14.2.395 Link 0 SDI Identifier (LSDIID0)—Offset C4Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 3h

Bit Range	Default and Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14	0h RO	**SDI 14 (SDIID14):** This link uses SDI 14. This bit is hardcoded per parameter LSDIID14 assignment.
13	0h RO	**SDI 13 (SDIID13):** This link uses SDI 13. This bit is hardcoded per parameter LSDIID13 assignment.
12	0h RO	**SDI 12 (SDIID12):** This link uses SDI 12. This bit is hardcoded per parameter LSDIID12 assignment.
11	0h RO	**SDI 11 (SDIID11):** This link uses SDI 11. This bit is hardcoded per parameter LSDIID11 assignment.
10	0h RO	**SDI 10 (SDIID10):** This link uses SDI 10. This bit is hardcoded per parameter LSDIID10 assignment.
9	0h RO	**SDI 9 (SDIID9):** This link uses SDI 9. This bit is hardcoded per parameter LSDIID9 assignment.
8	0h RO	**SDI 8 (SDIID8):** This link uses SDI 8. This bit is hardcoded per parameter LSDIID8 assignment.
7	0h RO	**SDI 7 (SDIID7):** This link uses SDI 7. This bit is hardcoded per parameter LSDIID7 assignment.

Bit Range	Default and Access	Field Name (ID): Description
6	0h RO	**SDI 6 (SDIID6):** This link uses SDI 6. This bit is hardcoded per parameter LSDIID6 assignment.
5	0h RO	**SDI 5 (SDIID5):** This link uses SDI 5. This bit is hardcoded per parameter LSDIID5 assignment.
4	0h RO	**SDI 4 (SDIID4):** This link uses SDI 4. This bit is hardcoded per parameter LSDIID4 assignment.
3	0h RO	**SDI 3 (SDIID3):** This link uses SDI 3. This bit is hardcoded per parameter LSDIID3 assignment.
2	0h RO	**SDI 2 (SDIID2):** This link uses SDI 2. This bit is hardcoded per parameter LSDIID2 assignment.
1	1h RO	**SDI 1 (SDIID1):** This link uses SDI 1. This bit is hardcoded per parameter LSDIID1 assignment.
0	1h RO	**SDI 0 (SDIID0):** This link uses SDI 0. This bit is hardcoded per parameter LSDIID0 assignment.

14.2.396 Link 0 Per Stream Output Overhead (LPSOO0)—Offset C50h

This register reports the output stream overhead for specific link.

Access Method

Type: MEM Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RO/V	**Per Stream Output Overhead (PSOO):** Indicates the SDO Output Overhead on a per stream basis. This does not include bandwidth used for command and control. This measurement is in byte quantities per 48 kHz frame. Software calculates available link bandwidth in bytes with the following formula: (2 * LOUTPAY) - (NumOfStreams * LPSOO).

14.2.397 Link 0 Per Stream Input Overhead (LPSIO0)—Offset C52h

This register reports the input stream overhead for specific link.

Access Method

Type: MEM Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RO/V	**Per Stream Input Overhead (PSIO):** Indicates the SDI Input Overhead on a per stream basis. This does not include bandwidth used for response. This measurement is in byte quantities per 48 kHz frame. Software calculates available link bandwidth in bytes with the following formula: (2 * LINPAY) - (NumOfStreams * LPSIO).

14.2.398 Link 0 Wall Frame Counter (LWALFC0)—Offset C58h

This register reports the wall frame counter for specific link.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:9	0h RO/V	**Frame Number (FN):** 23 bit counter that is incremented when CIF rolls over from 499 to 0. This counter will roll over to zero with a period of approximately 174 seconds.
8:0	0h RO/V	**Clock in Frame (CIF):** 9 bit counter that is incremented on each link BCLK period and rolls over from 499 to 0. This counter will roll over to zero with a period of 48 KHz HD Audio frame. With the introduction of multiple link segments for the Intel HD Audio controller, and the capability of running each link segment at different clock speed, the BCLK definition is fixed at 24 MHz equivalent rate always, independent of the physical link clock speed.

14.2.399 Link 1 Capabilities (LCAP1)—Offset C80h

This register identifies the specific link associated capabilities

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1Fh

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RW/L	**Audio Link Type (ALT):** Indicates which Link Type this link belongs to. 0001-1111 = Reserved 0000 = Intel HD Audio Link Locked when FNCFG.BCLD = 1.
27:26	0h RO	Reserved.
25:24	0h RW/L	**Number of Serial Data Out Signals (NSDO):** 00b indicates that the Intel HD Audio controller supports one Serial Data Output signal. Locked when FNCFG.BCLD = 1.

Bit Range	Default and Access	Field Name (ID): Description
23:6	0h RO	Reserved.
5	0h RW/L	**192 MHz Supported (S192):** Indicates 192 MHz clock is supported. Locked when FNCFG.BCLD = 1.
4	1h RW/L	**96 MHz Supported (S96):** Indicates 96 MHz clock is supported. Locked when FNCFG.BCLD = 1.
3	1h RW/L	**48 MHz Supported (S48):** Indicates 48 MHz clock is supported. Locked when FNCFG.BCLD = 1.
2	1h RW/L	**24 MHz Supported (S24):** Indicates 24 MHz clock is supported. Locked when FNCFG.BCLD = 1.
1	1h RW/L	**12 MHz Supported (S12):** Indicates 12 MHz clock is supported. Locked when FNCFG.BCLD = 1.
0	1h RW/L	**6 MHz Supported (S6):** Indicates 6 MHz clock is supported. Locked when FNCFG.BCLD = 1.

14.2.400 Link 1 Control (LCTL1)—Offset C84h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 10004h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RO/V	**Current Power Active (CPA):** This value changes to the value set by SPA when the power of the link has reached that state. Software sets SPA, then monitors CPA to know when the link has changed state.
22:17	0h RO	Reserved.
16	1h RW	**Set Power Active (SPA):** Software sets this bit to '1' to turn the link on (provided CRSTB = 1), and clears it to '0' when it wishes to turn the link off. When CPA matches the value of this bit, the achieved power state has been reached. Software is expected to wait for CPA to match SPA before it can program SPA again. Any deviation may result in undefined behaviour
15:4	0h RO	Reserved.
3:0	4h RW	**Set Clock Frequency (SCF):** Indicates the frequency that software wishes the link to run at. Changing this value to a value not supported by Link Capabilities shall result in indeterminate results. The possible encodings are: Encoding Frequency 0000 6 MHz 0001 12 MHz 0010 24 MHz 0011 48 MHz 0100 96 MHz 0101 Reserved for 192 MHz 0110-1111 Reserved

14.2.401 Link 1 Output Stream ID Mapping Valid (LOSIDV1)—Offset C88h

This register maps the output stream connection for specific link.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: FFFEh

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	1h RW	**Output Stream ID of 15 is Valid for this Link (L1OSIDV15):** This link will claim / forward output cycles with Stream ID = 1111b.
14	1h RW	**Output Stream ID of 14 is Valid for this Link (L1OSIDV14):** This link will claim / forward output cycles with Stream ID = 1110b.
13	1h RW	**Output Stream ID of 13 is Valid for this Link (L1OSIDV13):** This link will claim / forward output cycles with Stream ID = 1101b.
12	1h RW	**Output Stream ID of 12 is Valid for this Link (L1OSIDV12):** This link will claim / forward output cycles with Stream ID = 1100b.
11	1h RW	**Output Stream ID of 11 is Valid for this Link (L1OSIDV11):** This link will claim / forward output cycles with Stream ID = 1011b.
10	1h RW	**Output Stream ID of 10 is Valid for this Link (L1OSIDV10):** This link will claim / forward output cycles with Stream ID = 1010b.
9	1h RW	**Output Stream ID of 9 is Valid for this Link (L1OSIDV9):** This link will claim / forward output cycles with Stream ID = 1001b.
8	1h RW	**Output Stream ID of 8 is Valid for this Link (L1OSIDV8):** This link will claim / forward output cycles with Stream ID = 1000b.
7	1h RW	**Output Stream ID of 7 is Valid for this Link (L1OSIDV7):** This link will claim / forward output cycles with Stream ID = 0111b.
6	1h RW	**Output Stream ID of 6 is Valid for this Link (L1OSIDV6):** This link will claim / forward output cycles with Stream ID = 0110b.
5	1h RW	**Output Stream ID of 5 is Valid for this Link (L1OSIDV5):** This link will claim / forward output cycles with Stream ID = 0101b.
4	1h RW	**Output Stream ID of 4 is Valid for this Link (L1OSIDV4):** This link will claim / forward output cycles with Stream ID = 0100b.
3	1h RW	**Output Stream ID of 3 is Valid for this Link (L1OSIDV3):** This link will claim / forward output cycles with Stream ID = 0011b.
2	1h RW	**Output Stream ID of 2 is Valid for this Link (L1OSIDV2):** This link will claim / forward output cycles with Stream ID = 0010b.
1	1h RW	**Output Stream ID of 1 is Valid for this Link (L1OSIDV1):** This link will claim / forward output cycles with Stream ID = 0001b.
0	0h RO	Reserved.

14.2.402 Link 1 SDI Identifier (LSDIID1)—Offset C8Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14	0h RO	**SDI 14 (SDIID14):** This link uses SDI 14.
13	0h RO	**SDI 13 (SDIID13):** This link uses SDI 13.
12	0h RO	**SDI 12 (SDIID12):** This link uses SDI 12.
11	0h RO	**SDI 11 (SDIID11):** This link uses SDI 11.
10	0h RO	**SDI 10 (SDIID10):** This link uses SDI 10.
9	0h RO	**SDI 9 (SDIID9):** This link uses SDI 9.
8	0h RO	**SDI 8 (SDIID8):** This link uses SDI 8.
7	0h RO	**SDI 7 (SDIID7):** This link uses SDI 7.
6	0h RO	**SDI 6 (SDIID6):** This link uses SDI 6.
5	0h RO	**SDI 5 (SDIID5):** This link uses SDI 5.
4	0h RO	**SDI 4 (SDIID4):** This link uses SDI 4.
3	0h RO	**SDI 3 (SDIID3):** This link uses SDI 3.
2	1h RO	**SDI 2 (SDIID2):** This link uses SDI 2.
1	0h RO	**SDI 1 (SDIID1):** This link uses SDI 1.
0	0h RO	**SDI 0 (SDIID0):** This link uses SDI 0.

14.2.403 Link 1 Per Stream Output Overhead (LPSOO1)—Offset C90h

This register reports the output stream overhead for specific link.

Access Method

Type: MEM Register (Size: 8 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RO/V	**Per Stream Output Overhead (PSOO):** Indicates the SDO Output Overhead on a per stream basis. This does not include bandwidth used for command and control. This measurement is in byte quantities per 48 kHz frame. Software calculates available link bandwidth in bytes with the following formula: (2 * LOUTPAY) - (NumOfStreams * LPSOO).

14.2.404 Link 1 Per Stream Input Overhead (LPSIO1)—Offset C92h

This register reports the input stream overhead for specific link.

Access Method

Type: MEM Register (Size: 8 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RO/V	**Per Stream Input Overhead (PSIO):** Indicates the SDI Input Overhead on a per stream basis. This does not include bandwidth used for response. This measurement is in byte quantities per 48 kHz frame. Software calculates available link bandwidth in bytes with the following formula: (2 * LINPAY) - (NumOfStreams * LPSIO).

14.2.405 Link 1 Wall Frame Counter (LWALFC1)—Offset C98h

This register reports the wall frame counter for specific link.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:9	0h RO/V	**Frame Number (FN):** 23 bit counter that is incremented when CIF rolls over from 499 to 0. This counter will roll over to zero with a period of approximately 174 seconds.
8:0	0h RO/V	**Clock in Frame (CIF):** 9 bit counter that is incremented on each link BCLK period and rolls over from 499 to 0. This counter will roll over to zero with a period of 48 KHz HD Audio frame. With the introduction of multiple link segments for the Intel HD Audio controller, and the capability of running each link segment at different clock speed, the BCLK definition is fixed at 24 MHz equivalent rate always, independent of the physical link clock speed.

14.2.406 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC7LLPL)—Offset 4A10h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.407 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC7LLPU)—Offset 4A14h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.408 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC7LDPL)—Offset 4A18h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.409 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC7LDPU)—Offset 4A1Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.410 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC8LLPL)—Offset 4A20h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.411 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC8LLPU)—Offset 4A24h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.412 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC8LDPL)—Offset 4A28h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.413 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC8LDPU)—Offset 4A2Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.414 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC9LLPL)—Offset 4A30h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.415 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC9LLPU)—Offset 4A34h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.416 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC9LDPL)—Offset 4A38h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.417 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC9LDPU)—Offset 4A3Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.418 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC10LLPL)—Offset 4A40h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.419 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC10LLPU)—Offset 4A44h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.420 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC10LDPL)—Offset 4A48h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.421 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC10LDPU)—Offset 4A4Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.422 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC11LLPL)—Offset 4A50h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.423 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC11LLPU)—Offset 4A54h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.424 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC11LDPL)—Offset 4A58h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.425 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC11LDPU)—Offset 4A5Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.426 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC12LLPL)—Offset 4A60h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.427 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC12LLPU)—Offset 4A64h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.428 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC12LDPL)—Offset 4A68h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.429 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC12LDPU)—Offset 4A6Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.430 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC13LLPL)—Offset 4A70h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.431 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC13LLPU)—Offset 4A74h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.432 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC13LDPL)—Offset 4A78h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.433 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC13LDPU)—Offset 4A7Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.434 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC14LLPL)—Offset 4A80h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.435 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC14LLPU)—Offset 4A84h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.436 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC14LDPL)—Offset 4A88h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.437 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC14LDPU)—Offset 4A8Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.438 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC9LLPL)—Offset 4A90h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.439 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC9LLPU)—Offset 4A94h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.440 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC9LDPL)—Offset 4A98h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.441 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC9LDPU)—Offset 4A9Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.442 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC10LLPL)—Offset 4AA0h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.443 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC10LLPU)—Offset 4AA4h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.444 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC10LDPL)—Offset 4AA8h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.445 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC10LDPU)—Offset 4AACh

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.446 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC11LLPL)—Offset 4AB0h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.447 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC11LLPU)—Offset 4AB4h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.448 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC11LDPL)—Offset 4AB8h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.449 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC11LDPU)—Offset 4ABCh

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.450 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC12LLPL)—Offset 4AC0h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.451 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC12LLPU)—Offset 4AC4h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.452 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC12LDPL)—Offset 4AC8h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.453 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC12LDPU)—Offset 4ACCh

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.454 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC13LLPL)—Offset 4AD0h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.455 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC13LLPU)—Offset 4AD4h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.456 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC13LDPL)—Offset 4AD8h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.457 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC13LDPU)—Offset 4ADCh

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.458 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC14LLPL)—Offset 4AE0h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.459 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC14LLPU)—Offset 4AE4h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.460 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC14LDPL)—Offset 4AE8h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.461 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC14LDPU)—Offset 4AECh

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

14.2.462 Input/Output Processing Pipe's Link Connection x Control (IPPLC7CTL)—Offset 4AF0h

SRST bit is not affected by stream reset.

14.2.463 Input/Output Processing Pipe's Link Connection x Format (IPPLC7FMT)—Offset 4AF4h

This register specifies the audio format on the link connection end of the processing pipe.

14.2.464 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC7LLPL)—Offset 4AF8h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

14.2.465 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC7LLPU)—Offset 4AFCh

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

14.2.466 Input/Output Processing Pipe's Link Connection x Control (IPPLC8CTL)—Offset 4B00h

SRST bit is not affected by stream reset.

14.2.467 Input/Output Processing Pipe's Link Connection x Format (IPPLC8FMT)—Offset 4B04h

This register specifies the audio format on the link connection end of the processing pipe.

14.2.468 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC8LLPL)—Offset 4B08h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

14.2.469 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC8LLPU)—Offset 4B0Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

14.2.470 Input/Output Processing Pipe's Link Connection x Control (IPPLC9CTL)—Offset 4B10h

SRST bit is not affected by stream reset.

14.2.471 Input/Output Processing Pipe's Link Connection x Format (IPPLC9FMT)—Offset 4B14h

This register specifies the audio format on the link connection end of the processing pipe.

14.2.472 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC9LLPL)—Offset 4B18h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

14.2.473 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC9LLPU)—Offset 4B1Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

14.2.474 Input/Output Processing Pipe's Link Connection x Control (IPPLC10CTL)—Offset 4B20h

SRST bit is not affected by stream reset.

14.2.475 Input/Output Processing Pipe's Link Connection x Format (IPPLC10FMT)—Offset 4B24h

This register specifies the audio format on the link connection end of the processing pipe.

14.2.476 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC10LLPL)—Offset 4B28h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

14.2.477 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC10LLPU)—Offset 4B2Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

14.2.478 Input/Output Processing Pipe's Link Connection x Control (IPPLC11CTL)—Offset 4B30h

SRST bit is not affected by stream reset.

14.2.479 Input/Output Processing Pipe's Link Connection x Format (IPPLC11FMT)—Offset 4B34h

This register specifies the audio format on the link connection end of the processing pipe.

14.2.480 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC11LLPL)—Offset 4B38h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

14.2.481 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC11LLPU)—Offset 4B3Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

14.2.482 Input/Output Processing Pipe's Link Connection x Control (IPPLC12CTL)—Offset 4B40h

SRST bit is not affected by stream reset.

14.2.483 Input/Output Processing Pipe's Link Connection x Format (IPPLC12FMT)—Offset 4B44h

This register specifies the audio format on the link connection end of the processing pipe.

14.2.484 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC12LLPL)—Offset 4B48h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

14.2.485 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC12LLPU)—Offset 4B4Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

14.2.486 Input/Output Processing Pipe's Link Connection x Control (IPPLC13CTL)—Offset 4B50h

SRST bit is not affected by stream reset.

14.2.487 Input/Output Processing Pipe's Link Connection x Format (IPPLC13FMT)—Offset 4B54h

This register specifies the audio format on the link connection end of the processing pipe.

14.2.488 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC13LLPL)—Offset 4B58h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

14.2.489 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC13LLPU)—Offset 4B5Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

14.2.490 Input/Output Processing Pipe's Link Connection x Control (IPPLC14CTL)—Offset 4B60h

SRST bit is not affected by stream reset.

14.2.491 Input/Output Processing Pipe's Link Connection x Format (IPPLC14FMT)—Offset 4B64h

This register specifies the audio format on the link connection end of the processing pipe.

14.2.492 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC14LLPL)—Offset 4B68h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

14.2.493 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC14LLPU)—Offset 4B6Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

14.2.494 Input/Output Processing Pipe's Link Connection x Control (OPPLC9CTL)—Offset 4B70h

SRST bit is not affected by stream reset.

14.2.495 Input/Output Processing Pipe's Link Connection x Format (OPPLC9FMT)—Offset 4B74h

This register specifies the audio format on the link connection end of the processing pipe.

14.2.496 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC9LLPL)—Offset 4B78h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

14.2.497 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC9LLPU)—Offset 4B7Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

14.2.498 Input/Output Processing Pipe's Link Connection x Control (OPPLC10CTL)—Offset 4B80h

SRST bit is not affected by stream reset.

14.2.499 Input/Output Processing Pipe's Link Connection x Format (OPPLC10FMT)—Offset 4B84h

This register specifies the audio format on the link connection end of the processing pipe.

14.2.500 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC10LLPL)—Offset 4B88h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

14.2.501 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC10LLPU)—Offset 4B8Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

14.2.502 Input/Output Processing Pipe's Link Connection x Control (OPPLC11CTL)—Offset 4B90h

SRST bit is not affected by stream reset.

14.2.503 Input/Output Processing Pipe's Link Connection x Format (OPPLC11FMT)—Offset 4B94h

This register specifies the audio format on the link connection end of the processing pipe.

14.2.504 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC11LLPL)—Offset 4B98h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

14.2.505 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC11LLPU)—Offset 4B9Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

14.2.506 Input/Output Processing Pipe's Link Connection x Control (OPPLC12CTL)—Offset 4BA0h

SRST bit is not affected by stream reset.

14.2.507 Input/Output Processing Pipe's Link Connection x Format (OPPLC12FMT)—Offset 4BA4h

This register specifies the audio format on the link connection end of the processing pipe.

14.2.508 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC12LLPL)—Offset 4BA8h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

14.2.509 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC12LLPU)—Offset 4BACh

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

14.2.510 Input/Output Processing Pipe's Link Connection x Control (OPPLC13CTL)—Offset 4BB0h

SRST bit is not affected by stream reset.

14.2.511 Input/Output Processing Pipe's Link Connection x Format (OPPLC13FMT)—Offset 4BB4h

This register specifies the audio format on the link connection end of the processing pipe.

14.2.512 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC13LLPL)—Offset 4BB8h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

14.2.513 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC13LLPU)—Offset 4BBCh

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

14.2.514 Input/Output Processing Pipe's Link Connection x Control (OPPLC14CTL)—Offset 4BC0h

SRST bit is not affected by stream reset.

14.2.515 Input/Output Processing Pipe's Link Connection x Format (OPPLC14FMT)—Offset 4BC4h

This register specifies the audio format on the link connection end of the processing pipe.

14.2.516 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC14LLPL)—Offset 4BC8h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

14.2.517 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC14LLPU)—Offset 4BCCh

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

14.3 HDA PCR Registers

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 14-3. Summary ofHDA PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
530h	533h	Function Configuration (FNCFG)—Offset 530h	2Ah

14.3.1 Function Configuration (FNCFG)—Offset 530h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 2Ah

Bit Range	Default and Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5	1h RW	**Power Gating Disable (PGDIS):** When cleared, it allows power gating to take place per their associated enable and idle conditions. When set, it globally disables all power gating.
4	0h RW/O/L	**BIOS Configuration Lock Down (BCLD):** BIOS Configuration Lock Down (BCLD): When set, it indicates BIOS configuration is done and ready for operations. It also locks down related RW/L bits.
3	1h RW	**Clock Gating Disable (CGD):** Clock Gating Disabled (CGD): When cleared, it allows local / dynamic clock gating and trunk clock gating to take place per their associated enable and idle conditions. When set, it globally disables all clock gating.
2	0h RW/L	**Audio DSP Disable (ADSPD):** Audio DSP Disable (ADSPD): When set, the Audio DSP is disabled and all register access associated with Audio DSP are treated as unsupported request, and return UR response if it is non-posted cycle. This bit does not affect cycles from IOSF Sideband Interface. Locked when FNCFG.BCLD = 1.
1	1h RW/L	**HD Audio Subsystem as PCI Device (HDASPCID):** HD Audio Subsystem as PCI Device (HDASPCID): When this bit is set to 1, the Intel HD Audio subsystem will appear as a PCI device to SW. When this bit is 0, the Intel HD Audio subsystem will appear as a PCI-Express device to SW. Locked when FNCFG.BCLD = 1.
0	0h RW/L	**HD Audio Subsystem Disable (HDASD):** HD Audio Subsystem Disable (HDASD): When set, the Intel HD Audio subsystem (including Audio DSP) is disabled and all register access are treated as unsupported request, and return UR response if it is non-posted cycle. This bit does not affect cycles from IOSF Sideband Interface. Locked when FNCFG.BCLD = 1.

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14.4 High Definition Audio PCI Configuration Registers

Table 14-4. Summary of High Definition Audio PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	1h	Vendor Identification (VID)—Offset 0h	8086h
2h	3h	Device ID (DID)—Offset 2h	XXXXh
4h	5h	Command (CMD)—Offset 4h	0h
6h	7h	Status (STS)—Offset 6h	10h
8h	8h	Revision Identification (RID)—Offset 8h	XXh
9h	9h	Programming Interface (PI)—Offset 9h	0h
Ah	Ah	Sub Class Code (SCC)—Offset Ah	3h
Bh	Bh	Base Class Code (BCC)—Offset Bh	4h
Ch	Ch	Cache Line Size (CLS)—Offset Ch	0h
Dh	Dh	Latency Timer (LT)—Offset Dh	0h
Eh	Eh	Header Type (HTYPE)—Offset Eh	0h
10h	13h	Intel HD Audio Base Lower Address (HDALBA)—Offset 10h	4h
14h	17h	Intel HD Audio Base Upper Address (HDAUBA)—Offset 14h	0h
18h	1Bh	Shadowed PCI Configuration Lower Base Address (SPCLBA)—Offset 18h	0h
1Ch	1Fh	Shadowed PCI Configuration Upper Base Address (SPCUBA)—Offset 1Ch	0h
20h	23h	Audio DSP Lower Base Address (ADSPLBA)—Offset 20h	4h
24h	27h	Audio DSP Upper Base Address (ADSPUBA)—Offset 24h	0h
2Ch	2Dh	Subsystem Vendor ID (SVID)—Offset 2Ch	0h
2Eh	2Fh	Subsystem ID (SID)—Offset 2Eh	0h
34h	34h	Capability Pointer (CAPPTR)—Offset 34h	50h
3Ch	3Ch	Interrupt Line (INTLN)—Offset 3Ch	0h
3Dh	3Dh	Interrupt Pin (INTPN)—Offset 3Dh	1h
50h	51h	PCI Power Management Capability ID (PID)—Offset 50h	6001h
52h	53h	Power Management Capabilities (PC)—Offset 52h	C043h
54h	57h	Power Management Control And Status (PCS)—Offset 54h	8h
60h	61h	MSI Capability ID (MID)—Offset 60h	7005h
62h	63h	MSI Message Control (MMC)—Offset 62h	80h
64h	67h	MSI Message Lower Address (MMLA)—Offset 64h	0h
68h	6Bh	MSI Message Upper Address (MMUA)—Offset 68h	0h
6Ch	6Dh	MSI Message Data (MMD)—Offset 6Ch	0h
70h	71h	PCI Express Capability ID (PXID)—Offset 70h	10h
72h	73h	PCI Express Capabilities (PXC)—Offset 72h	91h
74h	77h	Device Capabilities (DEVCAP)—Offset 74h	10000000h
78h	79h	Device Control (DEVC)—Offset 78h	2800h
7Ah	7Bh	Device Status (DEVS)—Offset 7Ah	10h

14.4.1 Vendor Identification (VID)—Offset 0h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 8086h

Bit Range	Default and Access	Field Name (ID): Description
15:0	8086h RO	**Vendor ID (VID):** Indicates that Intel is the vendor.

14.4.2 Device ID (DID)—Offset 2h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: XXXXh

Bit Range	Default and Access	Field Name (ID): Description
15:0	8C20h RO/V	**Device ID (DID):** Indicates the Device ID of the controller. Refer to the Device and Revision ID Table in Volume 1 for default value.

14.4.3 Command (CMD)—Offset 4h

This register provides coarse control over a device's ability to generate and respond to PCI cycles.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (ID):** Enables the device to assert an INTx#. When set, the Intel(r) HD Audio controller's INTx# signal will be de-asserted. When cleared, the INTx# signal may be asserted. Note that this bit does not affect the generation of MSI's.
9	0h RO	**Fast Back to Back Enable (FBE):** Not implemented. Hardwired to 0.
8	0h RW	**SERR Enable (SEN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
7	0h RO	**Wait Cycle Control (WCC):** Not implemented. Hardwired to 0.
6	0h RW	**Parity Error Response (PER):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
5	0h RO	**VGA Palette Snoop (VPS):** Not implemented. Hardwired to 0.
4	0h RO	**Memory Write and Invalidate Enable (MWI):** Not implemented. Hardwired to 0.
3	0h RO	**Special Cycle Enable (SCE):** Not implemented. Hardwired to 0.
2	0h RW	**Bus Initiator Enable (BME):** 1 = Enable, 0 = Disable. Controls standard PCI Express bus Initiatoring capabilities for Memory and IO, reads and writes. Note that this also controls MSI generation since MSI are essentially Memory writes.
1	0h RW	**Memory Space Enable (MSE):** When set, enables memory space accesses to the Intel HD Audio controller.
0	0h RO	**I/O Space (IOS):** The Intel HD Audio controller does not implement IO Space, therefore this bit is hardwired to 0.

14.4.4 Status (STS)—Offset 6h

This register is used to record status information for PCI bus related events.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 10h

Bit Range	Default and Access	Field Name (ID): Description
15	0h RO	**Detected Parity Error (DPE):** Not implemented. Hardwired to 0.
14	0h RO	**SERR# Status (SERRS):** Not implemented. Hardwired to 0.
13	0h RW/1C/V	**Received Initiator Abort (RMA):** If the completion status received from IOSF is UR, this bit is set. SW writes a 1 to this bit to clear it.
12	0h RW/1C/V	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, this bit is set. SW writes a 1 to this bit to clear it.
11	0h RO	**Signaled Target-Abort (STA):** Not implemented. Hardwired to 0.
10:9	0h RO	**DEVSEL# Timing Status (DEVT):** Does not apply. Hardwired to 0.
8	0h RO	**Initiator Data Parity Error (MDPE):** Not implemented. Hardwired to 0.
7	0h RO	**Fast Back to Back Capable (FBC):** Does not apply. Hardwired to 0.
6	0h RO	Reserved.
5	0h RO	**66 MHz Capable (C66):** Does not apply. Hardwired to 0.
4	1h RO	**Capabilities List Exists (CLIST):** Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h.
3	0h RO/V	**Interrupt Status (IS):** Reflects the state of the INTx# signal at the input of the enable/disable circuit. This bit is a 1 when the INTx# is asserted. This bit is a 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the command register). Note that this bit is not set by an MSI.
2:0	0h RO	Reserved.

14.4.5 Revision Identification (RID)—Offset 8h

This register is not affected by D3HOT to D0 reset or FLR

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: XXh

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RO/V	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Volume 1 for specific value.

14.4.6 Programming Interface (PI)—Offset 9h

This register is not affected by D3HOT to D0 reset or FLR

Access Method

Type: CFG Register (Size: 8 bits)
Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW/L	**Programming Interface (PI):** Value assigned to the Intel HD Audio subsystem. Locked when FNCFG.BCLD = 1.

14.4.7 Sub Class Code (SCC)—Offset Ah

This register is not affected by D3HOT to D0 reset or FLR

Access Method

Type: CFG Register (Size: 8 bits)
Device: 31
Function: 3

Default: 3h

Bit Range	Default and Access	Field Name (ID): Description
7:0	3h RW/L	**Sub Class Code (SCC):** This indicates the device is an Intel HD Audio audio device, in the context of a multimedia device. Locked when FNCFG.BCLD = 1.

14.4.8 Base Class Code (BCC)—Offset Bh

This register is not affected by D3HOT to D0 reset or FLR

Access Method

Type: CFG Register (Size: 8 bits)
Device: 31
Function: 3

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
7:0	4h RW/L	**Base Class Code (BCC):** This register indicates that the function implements a multimedia device. Locked when FNCFG.BCLD = 1.

14.4.9 Cache Line Size (CLS)—Offset Ch

This register specifies the system cache line size in units of DWORDs.

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**Cache Line Size (CLS):** Does not apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the PCH.

14.4.10 Latency Timer (LT)—Offset Dh

This register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus Initiator.

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW/L	**Latency Timer (LT):** Doesn t apply to PCI Express. RO as 00h if PCI Express. If configured to appear as PCI device, maintain RW for Legacy PCI SW compliancy. Locked when FNCFG.HDASPCID = 0

14.4.11 Header Type (HTYPE)—Offset Eh

This register identifies the layout of the second part of the predefined header and also whether or not the device contains multiple functions.

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7	0h RW/L	**Multi Function Device (MFD):** Value of 0 indicates a single function device. Value of 1 indicates a multi function device. Locked when FNCFG.BCLD = 1.
6:0	0h RO	**Header Type (HTYPE):** Implements Type 0 Configuration header.

14.4.12 Intel HD Audio Base Lower Address (HDALBA)—Offset 10h

This BAR creates a selected size of memory space to signify the base address of the Intel HD Audio memory mapped configuration registers depending on implementation.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:14	0h RW	**Lower Base Address (LBA):** Base address for the Intel HD Audio subsystem s memory mapped configuration registers. 16 Kbytes are requested by hardwiring bits 13:4 to 0 s.
13:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PREF):** Indicates that this BAR is NOT pre-fetchable.
2:1	2h RO	**Address Range (ADDRNG):** Indicates that this BAR can be located anywhere in 64-bit address space.
0	0h RO	**Space Type (SPTYP):** Indicates that this BAR is located in memory space.

14.4.13 Intel HD Audio Base Upper Address (HDAUBA)—Offset 14h

This BAR creates a selected size of memory space to signify the base address (upper 32 bits) of the Intel HD Audio memory mapped configuration registers, depending on implementation.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Intel HD Audio Upper Base Address (UBA):** Upper 32 bits of the Base address for the Intel(r) HD Audio controller's memory mapped configuration registers.

14.4.14 Shadowed PCI Configuration Lower Base Address (SPCLBA)—Offset 18h

This BAR creates 4 Kbytes of memory space to signify the base address (lower 32 bits) of the shadowed PCI configuration when used as an ACPI device.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:12	0h RW/L	**Lower Base Address (LBA):** Base address for the PCI Configuration register shadowed to memory mapped. 4 KB is requested by hardwiring bits 11:4 to 0 s. Locked when PCICFGCTL0.SPCBAD = 1.
11:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PREF):** Indicates that this BAR is NOT pre-fetchable.
2:1	0h RO/V	**Address Range (ADDRNG):** Indicates that this BAR can be located anywhere in 64-bit address space.
0	0h RO	**Space Type (SPTYP):** Indicates that this BAR is located in memory space.

14.4.15 Shadowed PCI Configuration Upper Base Address (SPCUBA)—Offset 1Ch

This BAR creates 4 Kbytes of memory space to signify the base address (upper 32 bits) of the shadowed PCI configuration when used as an ACPI device.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/L	**Upper Base Address (UBA):** Upper 32 bits of the Base address for the PCI Configuration register shadowed to memory mapped. Locked when PCICFGCTL0.SPCBAD = 1.

14.4.16 Audio DSP Lower Base Address (ADSPLBA)—Offset 20h

This BAR creates a selected size of memory space to signify the base address of the Audio DSP memory mapped configuration registers depending on implementation. The number of LBA bits in this register is depending on the size of the memory window implemented.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:20	0h RW	**Lower Base Address (LBA):** Base address for the Audio DSP memory mapped configuration registers.
19:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PREF):** Indicates that this BAR is NOT pre-fetchable.
2:1	2h RO	**Address Range (ADDRNG):** Indicates that this BAR can be located anywhere in 64-bit address space.
0	0h RO	**Space Type (SPTYP):** Indicates that this BAR is located in memory space.

14.4.17 Audio DSP Upper Base Address (ADSPUBA)—Offset 24h

This BAR creates a selected size of memory space to signify the base address (upper 32 bits) of the Audio DSP memory-mapped configuration registers, depending on implementation.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Upper Base Address (UBA):** Upper 32 bits of the Base address for the Audio DSP memory mapped configuration registers.

14.4.18 Subsystem Vendor ID (SVID)—Offset 2Ch

This register should be implemented for any function that could be instantiated more than once in a given system, for example, a system with 2 audio subsystems, one down on the motherboard and the other plugged into a PCI expansion slot, should have the SVID register implemented. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one audio subsystem from the other(s).
Software (BIOS) will write the value to this register. After that, the value can be read, but writes to the register will have no effect. The write to this register should be combined with the write to the SID to create one 32-bit write. This register is not affected by D3HOT to D0 reset or FLR

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:0	0h RW/L	**SVID (SVID):** These RW bits have no functionality. Locked when FNCFG.BCLD = 1.

14.4.19 Subsystem ID (SID)—Offset 2Eh

This register should be implemented for any function that could be instantiated more than once in a given system, for example, a system with 2 audio subsystems, one down on the motherboard and the other plugged into a PCI expansion slot. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from the other(s). Software (BIOS) will write the value to this register. After that, the value can be read, but writes to the register will have no effect. The write to this register should be combined with the write to the SVID to create one 32-bit write. This register is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:0	0h RW/L	**SID (SID):** These RW bits have no functionality. Locked when FNCFG.BCLD = 1.

14.4.20 Capability Pointer (CAPPTR)—Offset 34h

This optional register is used to point to a linked list of new capabilities implemented by this device.

Access Method

Type: CFG Register (Size: 8 bits)
Device: 31
Function: 3

Default: 50h

Bit Range	Default and Access	Field Name (ID): Description
7:0	50h RO	**Capability Pointer (CAPPTR):** Indicates that the first capability pointer offset is offset 50h (Power Management Capability).

14.4.21 Interrupt Line (INTLN)—Offset 3Ch

This register is not affected by FLR.

Access Method

Type: CFG Register (Size: 8 bits)
Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**Interrupt Line (INTLN):** Hardware does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

14.4.22 Interrupt Pin (INTPN)—Offset 3Dh

This register is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register (Size: 8 bits)
Device: 31
Function: 3

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
7:4	0h RO	Reserved.
3:0	1h RW/L	**Interrupt Pin (INTPN):** Identifies the interrupt pin the function uses. 0h: No interrupt pin 1h: INTA 2h: INTB 3h: INTC 4h: INTD 5h - Fh: reserved Locked when FNCFG.BCLD = 1.

14.4.23 PCI Power Management Capability ID (PID)—Offset 50h

This register declares the power management capability structure.

Access Method

Type: CFG Register (Size: 16 bits)
Device: 31
Function: 3

Default: 6001h

Bit Range	Default and Access	Field Name (ID): Description
15:8	60h RW/L	**Next Capability (NEXT):** Points to the next capability structure (MSI). Locked when FNCFG.BCLD = 1.
7:0	1h RO	**Cap ID (CAP):** Indicates that this pointer is a PCI power management capability

14.4.24 Power Management Capabilities (PC)—Offset 52h

This register provides information on the capabilities of the function related to power management.

Access Method

Type: CFG Register (Size: 16 bits)
Device: 31
Function: 3

Default: C043h

Bit Range	Default and Access	Field Name (ID): Description
15:11	18h RW/L	**PME_Support (PMES):** Indicates PME# can be generated from D3 and D0 states. Programmable by BIOS for the option to declare SUS well wake is supported or not: 19h (SUS well wake supported) or 09h (SUS well wake not supported). Locked when FNCFG.BCLD = 1
10	0h RO	**D2_Support (D2S):** The D2 state is not supported.
9	0h RO	**D1_Support (D1S):** The D1 state is not supported.
8:6	1h RW/L	**Aux_Current (AC):** Reports 55 mA maximum Suspend well current required when in the D3cold state. Programmable by BIOS for the option to declare SUS well wake is supported or not: 001b (SUS well wake supported) or 000b (SUS well wake not supported). Locked when FNCFG.BCLD = 1.
5	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
4	0h RO	Reserved.
3	0h RO	**PME Clock (PMEC):** Does not apply. Hardwired to 0.
2:0	3h RW/L	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification. Programmable by BIOS to older revision if compatibility issue is found. Locked when FNCFG.BCLD = 1.

14.4.25 Power Management Control And Status (PCS)—Offset 54h

PMES and PMEE bits reside in Resume well, and reset by resume reset.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	**Data (DT):** Does not apply. Hardwired to 0's.
23	0h RO	**Bus Power/Clock Control Enable (BPCCE):** Does not apply. Hardwired to0.
22	0h RO	**B2/B3 Support (B23):** Does not apply. Hardwired to 0.
21:16	0h RO	Reserved.
15	0h RW/1C/V	**PME Status (PMES):** This bit is set when the Intel HD Audio controller would normally assert the PME# signal independent of the state of the PME bit. This bit is cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.
14:9	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
8	0h RW	**PME Enable (PMEE):** When set, and if corresponding PMES is also set, the Intel HD Audio subsystem send PME to PMC. This bit is cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.
7:4	0h RO	Reserved.
3	1h RW/L	**No Soft Reset (NSR):** When set (1), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. When clear (0), devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon transition from the D3hot to the D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled. Locked when FNCFG.BCLD = 1.
2	0h RO	Reserved.
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the Intel HD Audio subsystem and to set a new power state. The values are: 00 D0 state 11 D3HOT state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally, however, the data is discarded and no state change occurs. When in the D3HOT states, the Intel HD Audio subsystem s configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. When software changes this value from the D3HOT state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the function.

14.4.26 MSI Capability ID (MID)—Offset 60h

NEXT field is not affected by D3HOT to D0 reset or FLR

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 7005h

Bit Range	Default and Access	Field Name (ID): Description
15:8	70h RO/V	**Next Capability (NEXT):** Points to the PCI Express* capability structure. The value of this field depends on the FNCFG.HDASPCID bit. When FNCFG.HDASPCID is 0 , this field has a value of 70h where it points to the PCI Express capability structure. When FNCFG.HDASPCID bit is 1 , this field has a value of 00h to indicate that this is the last capability structure in the list.
7:0	5h RO	**Cap ID (CAP):** Indicates that this pointer is a MSI capability

14.4.27 MSI Message Control (MMC)—Offset 62h

This register provides system software control over MSI.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7	1h RO	**64b Address Capability (ADD64):** Indicates the ability to generate a 64-bitmessage address
6:4	0h RO	**Multiple Message Enable (MME):** Normally this is a R/W register. However since only 1 message is supported, these bits are hardwired to 000 = 1 message.
3:1	0h RO	**Multiple Message Capable (MMC):** Hardwired to 0 indicating request for 1message
0	0h RW	**MSI Enable (ME):** If set to 1 an MSI will be generated instead of an INTx#signal. If set to 0, an MSI may not be generated.

14.4.28 MSI Message Lower Address (MMLA)—Offset 64h

This register specifies the MSI message address (lower 32 bits).

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**MSI Message Lower Address (MMLA):** Lower Address used for MSI Message.
1:0	0h RO	Reserved.

14.4.29 MSI Message Upper Address (MMUA)—Offset 68h

This register specifies the MSI message address (upper 32 bits).

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI Message Upper Address (MMUA):** Upper 32 bits of address used for MSIMessage.

14.4.30 MSI Message Data (MMD)—Offset 6Ch

This register specifies the MSI message data.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:0	0h RW	**MSI Message Data (MMD):** Data used for MSI Message.

14.4.31 PCI Express Capability ID (PXID)—Offset 70h

This register declares the PCI Express capability structure.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 10h

Bit Range	Default and Access	Field Name (ID): Description
15:8	0h RO	**Next Capability (NEXT):** Indicates that this is the last capability structure in the list.
7:0	10h RO	**Cap ID (CAP):** Indicates that this pointer is a PCI Express capability structure.

14.4.32 PCI Express Capabilities (PXC)—Offset 72h

This register identifies PCI Express device Function type and associated capabilities.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 91h

Bit Range	Default and Access	Field Name (ID): Description
15:14	0h RO	Reserved.
13:9	0h RO	**Interrupt Message Number (IMN):** Hardwired to 0.
8	0h RO	**Slot Implemented (SI):** Hardwired to 0.
7:4	9h RO	**Device/Port Type (DPT):** Indicates that this is a Root Complex IntegratedEndpoint Device.
3:0	1h RO	**Capability Version (CV):** Indicates version #1 PCI Express capability

14.4.33 Device Capabilities (DEVCAP)—Offset 74h

This register is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 10000000h

Bit Range	Default and Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	1h RW/L	**Functional Level Reset (FLR):** A 1 indicates that the Intel HD Audio subsystem supports the Function Level Reset capability. Locked when FNCFG.BCLD = 1.
27:26	0h RO	**Captured Slot Power Limit Scale (SPLS):** Hardwired to 0.
25:18	0h RO	**Captured Slot Power Limit Value (SPLV):** Hardwired to 0.
17:15	0h RO	Reserved.
14	0h RO	**Power Indicator Present (PIP):** Hardwired to 0.
13	0h RO	**Attention Indicator Present (AIP):** Hardwired to 0.
12	0h RO	**Attention Button Present (ABP):** Hardwired to 0.
11:9	0h RW/L	**Endpoint L1 Acceptable Latency (L1CAP):** This bit field is defined in the PCI Express spec as RO. At this time it is risky to assign a hardwired value to this bit field. Making it RW would cause a WHQL failure. By making it RW/L it will appear as RO to WHQL testing while allowing BIOS to write a value at boot that is determined by post silicon system testing. Locked when FNCFG.BCLD = 1.

Bit Range	Default and Access	Field Name (ID): Description
8:6	0h RW/L	**Endpoint L0s Acceptable Latency (L0SCAP):** This bit field is defined in the PCI Express spec as RO. At this time it is risky to assign a hardwired value to this bit field. Making it RW would cause a WHQL failure. By making it RW/L it will appear as RO to WHQL testing while allowing BIOS to write a value at boot that is determined by post silicon system testing. Locked when FNCFG.BCLD = 1.
5	0h RO	**Extended Tag Field Support (ETCAP):** Indicates 5 bit tag supported.
4:3	0h RO	**Phantom Functions Supported (PFCAP):** Indicates phantom functions notsupported.
2:0	0h RO	**Max Payload Size Supported (MPCAP):** Indicates 128B maximum payloadsize capability.

14.4.34 Device Control (DEVC)—Offset 78h

NSNPEN bit is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 2800h

Bit Range	Default and Access	Field Name (ID): Description
15	0h WO	**Initiate FLR (IF):** Used to initiate FLR transition. A write of 1 initiates FLR transition. Since hardware must not respond to any cycles until FLR completion, the read value by software from this bit is 0 .
14:12	2h RW	**Max Read Request Size (MRRS):** This field sets the maximum Read Request size for the Function as a Requester. The Function must not generate Read Requests with size exceeding the set value. Defined encodings for this field are: 000: 128 B 001: 256 B 010: 512 B 011: 1024 B 100: 2048 B 101: 4096 B 110 111: Reserved
11	1h RW	**Enable No Snoop (NSNPEN):** When set to 1 (or EM2.FNSNPEN = 1) the Intel HD Audio controller is permitted to set the No Snoop bit in the Requester Attributes of a bus Initiator transaction. In this case VC0, VCp, or VC1 may be used for isochronous transfers. When set to 0 (and EM2.FNSNPEN = 0) the Intel HD Audio controller will not set the No Snoop bit. In the case isochronous transfers will not use VC1(VCi) even if it is enabled since VC1 is never snooped. Isochronous transfers will use either VCp or VC0. This bit is not affected by D3HOT to D0 reset or FLR.
10	0h RO	**Auxiliary (AUX) Power PM Enable (AUXPEN):** Hardwired to 0 indicating Intel HD Audio device does not draw AUX power.
9	0h RO	**Phantom Functions Enable (PFEN):** Hardwired to 0 disabling phantom functions.
8	0h RO	**Extended Tag Field Enable (ETEN):** Hardwired to 0 enabling 5-bit tag.

Bit Range	Default and Access	Field Name (ID): Description
7:5	0h RO	**Max Payload Size (MAXPAY):** Hardwired to 000 indicating 128 B.
4	0h RO	**Enable Relaxed Ordering (ROEN):** Hardwired to 0 disabling relaxed ordering.
3	0h RW	**Unsupported Request Reporting Enable (URREN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
2	0h RW	**Fatal Error Reporting Enable (FEREN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
1	0h RW	**Non-Fatal Error Reporting Enable (NFEREN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
0	0h RW	**Correctable Error Reporting Enable (CEREN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.

14.4.35 Device Status (DEVS)—Offset 7Ah

This register provides information about PCI Express device (Function) specific parameters.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 10h

Bit Range	Default and Access	Field Name (ID): Description
15:6	0h RO	Reserved.
5	0h RO/V	**Transactions Pending (TXP):** A 1 indicates that the Intel HD Audio controller has issued Non-Posted requests which have not been completed. A 0 indicates that Completions for all Non-Posted Requests have been received.
4	1h RW/L	**AUX Power Detected (AUXDET):** Hardwired to 1 indicating the device is connected to Suspend power. Programmable by BIOS for the option to declare SUS well wake is supported or not: 1b (SUS well wake supported) or 0b (SUS well wake not supported). Locked when FNCFG.BCLD = 1.
3	0h RO	**Unsupported Request Detected (URDET):** Not implemented. Hardwired to 0.
2	0h RO	**Fatal Error Detected (FEDET):** Not implemented. Hardwired to 0.
1	0h RO	**Non-Fatal Error Detected (NFEDET):** Not implemented. Hardwired to 0.
0	0h RO	**Correctable Error Detected (CEDET):** Not implemented. Hardwired to 0.

15 SMBus Interface (D31:F4)

15.1 SMBus Configuration Registers

Table 15-1. Summary of SMBus Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	1h	Vendor ID (VID)—Offset 0h	8086h
2h	3h	Device ID (DID)—Offset 2h	XXXXh
4h	5h	Command Register (CMD)—Offset 4h	0h
6h	7h	Device Status (DS)—Offset 6h	280h
8h	8h	Revision ID (RID)—Offset 8h	XXh
9h	9h	Programming Interface (PI)—Offset 9h	0h
Ah	Ah	Sub Class Code (SCC)—Offset Ah	5h
Bh	Bh	Base Class Code (BCC)—Offset Bh	Ch
10h	13h	SMBus Memory Base Address_31_0 (SMBMBAR_31_0)—Offset 10h	4h
14h	17h	SMBus Memory Base Address_63_32 (SMBMBAR_63_32)—Offset 14h	0h
20h	23h	SMB Base Address (SBA)—Offset 20h	1h
2Ch	2Dh	Subsystem Vendor Identifiers (SVID)—Offset 2Ch	0h
2Eh	2Fh	Subsystem Identifiers (SID)—Offset 2Eh	0h
3Ch	3Ch	Interrupt Line (INTLN)—Offset 3Ch	0h
3Dh	3Dh	Interrupt Pin (INTPN)—Offset 3Dh	1h
40h	40h	Host Configuration (HCFG)—Offset 40h	0h
50h	53h	TCO Base Address (TCOBASE)—Offset 50h	1h
54h	57h	TCO Control (TCOCTL)—Offset 54h	0h
80h	83h	SMBus Power Gating (SMBSM)—Offset 80h	0h

15.1.1 Vendor ID (VID)—Offset 0h

Vendor ID

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 4

Default: 8086h

Bit Range	Default and Access	Field Name (ID): Description
15:0	8086h RO	**Vendor ID (VID):** Value indicates Intel as the vendor

15.1.2 Device ID (DID)—Offset 2h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 4

Default: XXXXh

Bit Range	Default and Access	Field Name (ID): Description
15:0	-- RO/V	**Device ID (DID):** Indicates the value assigned to the PCH SMBus controller. Refer to the Device and Revision ID Table in Volume 1 for default setting.

15.1.3 Command Register (CMD)—Offset 4h

Command Register

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 4

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (INTD):** 1 = Disables SMBus to assert its PIRQB# signal. Defaults to 0.
9	0h RO	**Fast Back to Back Enable (FBE):** Reserved as 0. Read Only.
8	0h RW	**SERR# Enable (SERRE):** 1 = Enables SERR# generation
7	0h RO	**Wait Cycle Control (WCC):** Reserved as 0. Read Only.
6	0h RW	**Parity Error Response (PER):** 1 = Sets Detected Parity Error bit when parity error is detected
5	0h RO	**VGA Palette Snoop (VGAPS):** Reserved as 0. Read Only.
4	0h RO	**Postable Memory Write Enable (PMWE):** Reserved as 0. Read Only.
3	0h RO	**Special Cycle Enable (SCE):** Reserved as 0. Read Only.
2	0h RO	**Bus Initiator Enable (BME):** Reserved as 0. Read Only.

Bit Range	Default and Access	Field Name (ID): Description
1	0h RW	**Memory Space Enable (MSE):** 1= Enables memory mapped config space.
0	0h RW	**I/O Space Enable (IOSE):** 1= enables access to the SM Bus I/O space registers as defined by the Base Address Register.

15.1.4 Device Status (DS)—Offset 6h

Device Status

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 4

Default: 280h

Bit Range	Default and Access	Field Name (ID): Description
15	0h RW/1C	**Detected Parity Error (DPE):** 1 = Parity error detected
14	0h RW/1C	**Signaled System Error (SSE):** 1 = System error detected
13	0h RO	**Received Initiator Abort (RMA):** Reserved as 0.
12	0h RO	**Received Target Abort (RTA):** Reserved as '0'.
11	0h RW/1C	**Signaled Target-Abort Status (STA):** Reserved as 0.
10:9	1h RO	**DEVSEL# Timing Status (DEVT):** This 2-bit field defines the timing for DEVSEL# assertion. These read only bits indicate the Intel PCH's DEVSEL# timing when performing a positive decode. Note: PCH generates DEVSEL# with medium time.
8	0h RO	**Data Parity Error Detected (DPED):** Reserved as 0.
7	1h RO	**Fast Back-to-Back Capable (FBC):** Reserved as '1'.
6	0h RO	**User Definable Features (UDF):** Reserved as 0.
5	0h RO	**66 MHz Capable (C_66M):** Reserved as 0.
4	0h RO	**Capabilities List Indicator (CLI):** Hardwired to 0 because there are no capability list structures in this function.
3	0h RO	**Interrupt Status (INTS):** This bit indicates that an interrupt is pending. It is independent from the state of the Interrupt Enable bit in the command register.
2:0	0h RO	Reserved.

15.1.5 Revision ID (RID)—Offset 8h

Revision ID

Access Method

Type: CFG Register (Size: 8 bits)
Device: 31
Function: 4

Default: XXh

Bit Range	Default and Access	Field Name (ID): Description
7:0	-- RO	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

15.1.6 Programming Interface (PI)—Offset 9h

Programming Interface

Access Method

Type: CFG Register (Size: 8 bits)
Device: 31
Function: 4

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RO	**Programming Interface (PI):** No programming interface defined.

15.1.7 Sub Class Code (SCC)—Offset Ah

Sub Class Code

Access Method

Type: CFG Register (Size: 8 bits)
Device: 31
Function: 4

Default: 5h

Bit Range	Default and Access	Field Name (ID): Description
7:0	5h RO	**Sub Class Code (SCC):** A value of 05h indicates that this device is a SM Bus serial controller.

15.1.8 Base Class Code (BCC)—Offset Bh

Base Class Code

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 4

Default: Ch

Bit Range	Default and Access	Field Name (ID): Description
7:0	Ch RO	**Base Class Code (BCC):** A value of 0Ch indicates that this device is a serial controller

15.1.9 SMBus Memory Base Address_31_0 (SMBMBAR_31_0)—Offset 10h

SMBus Memory Base Address_31_0

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 4

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RW	**Base Address (BA):** Provides the 32 byte system memory base address for the PCH SMB logic.
7:4	0h RO	**Hardwired_0 (HARDWIRED_0):** Hardwired to 0.
3	0h RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that SMBMBAR is not pre-fetchable
2:1	2h RO	**Address Range (ADDRNG):** Indicates that this SMBMBAR can be located anywhere in 64 bit address space
0	0h RO	**Memory Space Indicator (MSI):** Indicates that the SMB logic is memory mapped.

15.1.10 SMBus Memory Base Address_63_32 (SMBMBAR_63_32)—Offset 14h

SMBus Memory Base Address_63_32

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 4

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Base Address (BA):** Bits 63-32 of SMbus Memory Base Address

15.1.11 SMB Base Address (SBA)—Offset 20h

SMB Base Address

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 4

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:5	0h RW	**Base Address (BA):** Provides the 32 byte t system I/O base address for the SMB logic.
4:1	0h RO	Reserved.
0	1h RO	**IO Space Indicator (IOSI):** This read-only bit always is 1, indicating that the SMB logic is I/O mapped.

15.1.12 Subsystem Vendor Identifiers (SVID)—Offset 2Ch

Subsystem Vendor ID

Access Method

Type: CFG Register (Size: 16 bits)
Device: 31
Function: 4

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:0	0h RW/O	**Subsystem Vendor ID (SVID):** BIOS sets the value in this register to identify the Subsystem Vendor ID. The SMBus SVID register, in combination with the SMBus Subsystem ID register, enables the operating system to distinguish each subsystem from the others. Note: The software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

15.1.13 Subsystem Identifiers (SID)—Offset 2Eh

Subsystem ID

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 4

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:0	0h RW/O	**Subsystem ID (SID):** BIOS can write to this register to identify the Subsystem ID. The SID register, in combination with the SVID, enable the operating system to distinguish each subsystem from other(s). Note: The software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

15.1.14 Interrupt Line (INTLN)—Offset 3Ch

Interrupt Line

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**Interrupt Line (INTLN):** This data is not used by the hardware. It is to communicate to software the interrupt line that the interrupt pin is connected to PIRQB#.

15.1.15 Interrupt Pin (INTPN)—Offset 3Dh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
7:0	1h RW/O	**Interrupt Pin (INTPN):** This defines the interrupt pin to be used by the SMBus controller. Bits : Pins 0h : No Interrupt 1h : INTA# 2h : INTB# 3h : INTC# 4h : INTD# 5h-Fh : Reserved

15.1.16 Host Configuration (HCFG)—Offset 40h

Host Configuration

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:5	0h RO	Reserved.
4	0h RW/1L	**SPD Write Disable (SPDWD):** When this bit is set to 1, writes to SMBus addresses 50h – 57h are disabled. Note: This bit is R/WO and will be reset on PLTRST# assertion. This bit should be set by BIOS to '1'. Software can only program this bit when both the START bit and Host Busy bit are '0'; otherwise, the write may result in undefined behavior.
3	0h RW	**SSRESET (SSRESET):** Soft SMBUS Reset: When this bit is 1, the SMbus state machine and logic in PCH is reset. The HW will reset this bit to 0 when reset operation is completed.
2	0h RW	**I2C_EN (I2CEN):** When this bit is 1, the PCH is enabled to communicate with I2C devices. This will change the formatting of some commands. When this bit is 0, behavior is for SMBus.
1	0h RW	**SMB_SMI_EN (SSEN):** When this bit is set, any source of an SMB interrupt will instead be routed to generate an SMI#.
0	0h RW	**HST_EN (HSTEN):** When set, the SMB Host Controller interface is enabled to execute commands. The HST_INT_EN bit needs to be enabled in order for the SMB Host Controller to interrupt or SMI#. Additionally, the SMB Host Controller will not respond to any new requests until all interrupt requests have been cleared.

15.1.17 TCO Base Address (TCOBASE)—Offset 50h

TCO Base Address

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 4

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:5	0h RW/L	**TCO Base Address (TCOBA):** Provides the 32 bytes of I/O space for TCO logic, mappable anywhere in the 64k I/O space on 32-byte boundaries.
4:1	0h RO	Reserved.
0	1h RO	**I/O Space (IOS):** Indicates an I/O Space

15.1.18 TCO Control (TCOCTL)—Offset 54h

TCO Control

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 4

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**TCO Base Enable (TCO_BASE_EN):** When set, decode of the I/O range pointed to by the TCO base register is enabled.
7:1	0h RO	Reserved.
0	0h RW/O	**TCO Base Lock (TCO_BASE_LOCK):** When set to 1, this bit locks down the TCO Base Address Register (TCOBASE) at offset 50h. The Base Address Field becomes read-only. This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a platform reset.

15.1.19 SMBus Power Gating (SMBSM)—Offset 80h

15.2 SMBus I/O and Memory Mapped I/O Registers

The SMBus registers can be accessed through I/O BAR or Memory BAR registers in PCI configuration space. The offsets are the same for both I/O and Memory Mapped I/O registers.

Table 15-2. Summary of SMBus I/O and Memory Mapped I/O Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	0h	Host Status Register Address (HSTS)—Offset 0h	0h
2h	2h	Host Control Register (HCTL)—Offset 2h	0h

Table 15-2. Summary of SMBus I/O and Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3h	3h	Host Command Register (HCMD)—Offset 3h	0h
4h	4h	Transmit Target Address Register (TSA)—Offset 4h	0h
5h	5h	Data 0 Register (HD0)—Offset 5h	0h
6h	6h	Data 1 Register (HD1)—Offset 6h	0h
7h	7h	Host Block Data (HBD)—Offset 7h	0h
8h	8h	Packet Error Check Data Register (PEC)—Offset 8h	0h
9h	9h	Receive Target Address Register (RSA)—Offset 9h	44h
Ah	Bh	Target Data Register (SD)—Offset Ah	0h
Ch	Ch	Auxiliary Status (AUXS)—Offset Ch	0h
Dh	Dh	Auxiliary Control (AUXC)—Offset Dh	0h
Eh	Eh	SMLINK_PIN_CTL Register (SMLC)—Offset Eh	4h
Fh	Fh	SMBUS_PIN_CTL Register (SMBC)—Offset Fh	4h
10h	10h	Target Status Register (SSTS)—Offset 10h	0h
11h	11h	Target Command Register (SCMD)—Offset 11h	0h
14h	14h	Notify Device Address Register (NDA)—Offset 14h	0h
16h	16h	Notify Data Low Byte Register (NDLB)—Offset 16h	0h
17h	17h	Notify Data High Byte Register (NDHB)—Offset 17h	0h

15.2.1 Host Status Register Address (HSTS)—Offset 0h

All status bits are set by hardware and cleared by the software writing a one to the particular bit position. Writing a zero to any bit position has no affect.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7	0h RW/1C	**BYTE_DONE_STS (BDS):** This bit will be set to 1 when the host controller has received a byte (for Block Read commands) or if it has completed transmission of a byte (for Block Write commands) when the 32-byte buffer is not being used. Note that this bit will be set, even on the last byte of the transfer. Software clears the bit by writing a 1 to the bit position. This bit has no meaning for block transfers when the 32- byte buffer is enabled. Note: When the last byte of a block message is received, the host controller will set this bit. However, it will not immediately set the INTR bit (bit 1 in this register). When the interrupt handler clears the BYTE_DONE_STS bit, the message is considered complete, and the host controller will then set the INTR bit (and generate another interrupt). Thus, for a block message of n bytes, the PCH will generate n+1 interrupts. The interrupt handler needs to be implemented to handle these cases.
6	0h RW/1C	**In Use Status (IUS):** After a full PCI reset, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the host controller. This bit has no other effect on the hardware, and is only used as semaphore among various independent software threads that may need to use the Intel PCHs SMBus logic.
5	0h RW/1C	**SMBALERT_STS (SMSTS):** PCH sets this bit to a 1 to indicates source of the interrupt or SMI# was the SMBAlert# signal. Software resets this bit by writing a 1 to this location. This bit should also be cleared by RSMRST# (but not PLTRST#).
4	0h RW/1C	**Failed (FAIL):** When set, this indicates that the source of the interrupt or SMI# was a failed bus transaction. This is set in response to the KILL bit being set to terminate the host transaction.
3	0h RW/1C	**Bus Error (BERR):** When set, this indicates the source of the interrupt or SMI# was a transaction collision.
2	0h RW/1C	**Device Error (DERR):** When set, this indicates that the source of the interrupt or SMI# was due one of the following: unsupported Command Field Unclaimed Cycle (host initiated) Host Device Time-out Error. CRC Error
1	0h RW/1C	**Interrupt (INTR):** When set, this indicates that the source of the interrupt or SMI# was the successful completion of its last command.
0	0h RW/1C	**Host Busy (HBSY):** A 1 indicates that the PCH is running a command from the host interface. No SMB registers should be accessed while this bit is set. Exception: The BLOCK DATA REGISTER can be accessed when this bit is set ONLY when the SMB_CMD bits (in Host control register) are programmed for Block command or I2C Read command. This is necessary in order to check the DONE_STS bit.

15.2.2 Host Control Register (HCTL)—Offset 2h

Note: A read to this register will clear the pointer in the 32-byte buffer.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7	0h RW	**PEC_EN (PEC_EN):** When set to 1, this bit causes the host controller to perform the SMBus transaction with the Packet Error Checking phase appended. For writes, the value of the PEC byte is transferred from the PEC Register. For reads, the PEC byte is loaded in to the PEC Register. When this bit is cleared to 0, the SMBus host controller does not perform the transaction with the PEC phase appended. This bit must be written prior to the write in which the START bit is set.
6	0h RW	**START (START):** This write-only bit is used to initiate the command described in the SMB_CMD field. All registers should be setup prior to writing a 1 to this bit position. This bit always reads zero. The HOST_BUSY bit in the Host Status register (offset 00h) can be used to identify when the PCH has finished the command.
5	0h RW	**LAST_BYTE (LAST_BYTE):** This bit is used for I2C Read commands. Software sets this bit to indicate that the next byte will be the last byte to be received for the block. This causes the PCH to send a NACK (instead of an ACK) after receiving the last byte. Note: This bit may be set when the TCO timer causes the SECOND_TO_STS bit to be set. SW should clear the LAST_BYTE bit (if it is set) before starting any new command. Note: In addition to I2C Read Commands, the LAST_BYTE bit will also cause Block Read/Write cycles to stop prematurely (at the end of the next byte).
4:2	0h RW	**SMB_CMD (SMB_CMD):** As shown by the bit encoding below, indicates which command the PCH is to perform. If enabled, the PCH will generate an interrupt or SMI# when the command has completed. If the value is for a non-supported or reserved command, the PCH will set the device error(DEV_ERR) status bit and generate an interrupt when the START bit is set. The PCH will perform no command, and will not operate until DEV_ERR is cleared.Val. 000 - Quick: The Target address and read/write value (bit 0) are stored in the tx Target address register. 001 - Byte: This command uses the transmit Target address and command registers. Bit 0 of the Target address register determines if this is a read or write command. 010 - Byte Data: This command uses the transmit Target address, command, and DATA0 registers. Bit 0 of the Target address register determines if this is a read or write command. If it is a read, the DATA0 register will contain the read data. 011 - Word Data: This command uses the transmit Target address, command, DATA0 and DATA1 registers. Bit 0 of the Target address register determines if this is a read or write command. If it is a read, after the command completes the DATA0 and DATA1 registers will contain the read data. 100 - Process Call: This command uses the transmit Target address, command, DATA0 and DATA1 registers. Bit 0 of the Target address register determines if this is a read or write command. After the command completes, the DATA0 and DATA1 registers will contain the read data. 101 - Block: This command uses the transmit Target address, command, and DATA0 registers, and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block reads, the count is received and stored in the DATA0 register. Bit 0 of the Target address register selects if this is a read or write command. For writes, data is retrieved from the first n (where n is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. 110 - I2C Read: This command uses the transmit Target address, command, DATA0, DATA1 registers, and the Block Data Byte register. The read data is stored in the Block Data Byte register. The PCH will continue reading data until the NAK is received. 111 - Block-Process: This command uses the transmit Target address, command, DATA0 and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block read, the count is received and stored in the DATA0 register. Bit 0 of the Target address register always indicate a write command. For writes, data is retrieved from the first m (where m is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. Note: E32B bit in the Auxiliary Control Register must be set for this command to work.
1	0h RW	**KILL (KILL):** When set, kills the current host transaction taking place, sets the FAILED status bit, and asserts the interrupt (or SMI#) selected by the SMB_INTRSEL field. This bit, once set, must be cleared to allow the SMB Host Controller to function normally.
0	0h RW	**INTREN (INTREN):** Enable the generation of an interrupt or SMI# upon the completion of the command.

15.2.3 Host Command Register (HCMD)—Offset 3h

Host Command Register

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**Host Command Register (HCMD):** This eight bit field is transmitted by the host controller in the command field of the SMB protocol during the execution of any command.

15.2.4 Transmit Target Address Register (TSA)—Offset 4h

This register is transmitted by the host controller in the Target address field of the SMB protocol. This is the address of the target.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:1	0h RW	**ADDRESS (ADDR):** 7-bit address of the targeted Target. Note: Writes to TSA values of A0h - AEh are blocked depending on the setting of the SPD write disable bit in HCFG - HostConfiguration.
0	0h RW	**RW (RW):** Direction of the host transfer. 1 = read, 0 = write

15.2.5 Data 0 Register (HD0)—Offset 5h

Data 0 Registe

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**DATA0/COUNT (DATA0_COUNT):** This field contains the eight bit data sent in the DATA0 field of the SMB protocol. For block write commands, this register reflects the number of bytes to transfer. This register should be programmed to a value between 1 and 32 for block counts. A count of 0 or a count above 32 will result in unpredictable behavior. The host controller does not check or log unsupported block counts.

15.2.6 Data 1 Register (HD1)—Offset 6h

Data 1 Register

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**DATA1 (DATA1):** This eight bit register is transmitted in the DATA1 field of the SMB protocol during the execution of any command.

15.2.7 Host Block Data (HBD)—Offset 7h

Host Block Data

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**Block Data (BDTA):** This is either a register, or a pointer into a 32- byte block array, depending upon whether the E32B bit is set in the Auxiliary Control register. When the E32B bit is cleared, this is a register containing a byte of data to be sent on a block write or read from on a block read, just as it behaved on the PCH. When the E32B bit is set, reads and writes to this register are used to access the 32-byte block data storage array. An internal index pointer is used to address the array, which is reset to 0 by reading the HCTL register (offset 02h). The index pointer then increments automatically upon each access to this register. The transfer of block data into (read) or out of (write) this storage array during an SMBus transaction always starts at index address 0. When the E2B bit is set, for writes, software will write up to 32-bytes to this register as part of the setup for the command. After the Host Controller has sent the Address, Command, and Byte Count fields, it will send the bytes in the SRAM pointed to by this register. When the E2B bit is cleared for writes, software will place a single byte in this register. After the host controller has sent the address, command, and byte count fields, it will send the byte in this register. If there is more data to send, software will write the next series of bytes to the SRAM pointed to by this register and clear the DONE_STS bit. The controller will then send the next byte. During the time between the last byte being transmitted to the next byte being transmitted, the controller will insert wait-states on the interface. When the E2B bit is set for reads, after receiving the byte count into the Data0 register, the first series of data bytes go into the SRAM pointed to by this register. If the byte count has been exhausted or the 32-byte SRAM has been filled, the controller will generate an SMI# or interrupt (depending on configuration) and set the DONE_STS bit. Software will then read the data. During the time between when the last byte is read from the SRAM to when the DONE_STS bit is cleared, the controller will insert waitstates on the interface.

15.2.8 Packet Error Check Data Register (PEC)—Offset 8h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**PEC_DATA (PEC_DATA):** This 8-bit register is written with the SMBus PEC data prior to a write transaction. For read transactions, the PEC data is loaded from the SMBus into this register and is then read by software. Software must ensure that the INUSE_STS bit is properly maintained to avoid having this field over-written by a write transaction following a read transaction.

15.2.9 Receive Target Address Register (RSA)—Offset 9h

Receive Target Address Register

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 44h

Bit Range	Default and Access	Field Name (ID): Description
7	0h RO	Reserved.
6:0	44h RW	**Target_ADDR[6:0] (SA_6_0):** This field is the Target address that the PCH decodes for read and write cycles. The default is not 0 so that it can respond even before the CPU comes up (or if the CPU is dead). This register is reset by RSMRST#, but not by PLTRST#.

15.2.10 Target Data Register (SD)—Offset Ah

Target Data Register

Access Method

Type: IO Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:0	0h RO/V	**Target_DATA[15:0] (SD_15_0):** This field is the 16-bit data value written by the external SMBus Initiator. The CPU can then read the value from this register. This register is reset by RSMRST#, but not by PLTRST#. Target_DATA[7:0] corresponds to the Data Message Byte 0 at Target Write Register 4 in the table. Target_[15:8] corresponds to the Data Message Byte 1 at Target Write Register 5 in the table.

15.2.11 Auxiliary Status (AUXS)—Offset Ch

All bits in this register are in the core well.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:1	0h RO	Reserved.
0	0h RW/1C	**CRC Error (CRCE):** This bit is set if a received message contained a CRC error. When this bit is set, the DERR bit of the host status register will also be set. This bit will be set by the controller if a software abort occurs in the middle of the CRC portion of the cycle or an abort happens after PCH has received the final data bit transmitted by external Target.

15.2.12 Auxiliary Control (AUXC)—Offset Dh

All bits in this register are in the resume well.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:2	0h RO	Reserved.
1	0h RW	**Enable 32-byte Buffer (E32B):** When set, the Host Block Data register is a pointer into a 32-byte buffer, as opposed to a single register. This enables the block commands to transfer or receive up to 32-bytes before the PCH generates an interrupt.
0	0h RW	**Automatically Append CRC (AAC):** When set, the PCH will automatically append the CRC. This bit must not be changed during SM Bus transactions, or undetermined behavior will result. It should be programmed only once during the lifetime of the function.

15.2.13 SMLINK_PIN_CTL Register (SMLC)—Offset Eh

Note: This register is in the resume well and is reset by RSMRST#

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	1h RW	**SMLINK_CLK_CTL (SMLINK_CLK_CTL):** 0 = PCH will drive the SMLINK[0] pin low, independent of what the other SMLINK logic would otherwise indicate for the SMLINK(0) pin. 1 = The SMLINK[0] pin is Not overdriven low. The other SMLINK logic controls the state of the pin.
1	0h RO/V	**SMLINK[1]_CUR_STS (SMLINK1_CUR_STS):** This bit has a default value that is dependent on an external signal level. This returns the value on the SMLINK[1] pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.
0	0h RO/V	**SMLINK[0]_CUR_STS (SMLINK0_CUR_STS):** This bit has a default value that is dependent on an external signal level. This returns the value on the SMLINK[0] pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.

15.2.14 SMBUS_PIN_CTL Register (SMBC)—Offset Fh

Note: This register is in the resume well and is reset by RSMRST#

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	1h RW	**SMBCLK_CTL (SMBCLK_CTL):** 0 = PCH will drive the SMBCLK pin low, independent of what the other SMB logic would otherwise indicate for the SMBCLK pin. 1 = The SMBCLK pin is Not overdriven low. The other SMBus logic controls the state of the pin.
1	0h RO/V	**SMBDATA_CUR_STS (SMBDATA_CUR_STS):** This bit has a default value that is dependent on an external signal level. This returns the value on the SMBDATA pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.
0	0h RO/V	**SMBCLK_CUR_STS (SMBCLK_CUR_STS):** This bit has a default value that is dependent on an external signal level. This returns the value on the SMBCLK pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.

15.2.15 Target Status Register (SSTS)—Offset 10h

All bits in this register are implemented in the 64 kHz clock domain. Therefore, software must poll the register until a write takes effect before assuming that a write has completed internally.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:1	0h RO	Reserved.
0	0h RW/1C	**HOST_NOTIFY_STS (HNS):** The PCH sets this bit to a 1 when it has completely received a successful Host Notify Command on the SMBus pins. Software reads this bit to determine that the source of the interrupt or SMI# was the reception of the Host Notify Command. Software clears this bit after reading any information needed from the Notify address and data registers by writing a 1 to this bit. Note that the PCH will allow the Notify Address and Data registers to be over-written once this bit has been cleared. When this bit is 1, the PCH will NACK the first byte (host address) of any new Host Notify commands on the SMBus. Writing a 0 to this bit has no effect.

15.2.16 Target Command Register (SCMD)—Offset 11h

All bits in this register are implemented in the 64 kHz clock domain. Therefore, software must poll the register until a write takes effect before assuming that a write has completed internally. Also, software must confirm the prior written value before writing to the register again.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h RW	**SMBALERT_DIS (SMB_D):** Software sets this bit to 1 to block the generation of the interrupt or SMI# due to the SMBALERT# source. This bit is logically inverted and ANDed with the SMBALERT_STS bit. The resulting signal is distributed to the SMI# and/or interrupt generation logic. This bit does not effect the wake logic.
1	0h RW	**HOST_NOTIFY_WKEN (HNW):** Software sets this bit to 1 to enable the reception of a Host Notify command as a wake event. When enabled this event is ORed in with the other SMBus wake events and is reflected in the SMB_WAK_STS bit of the General Purpose Event 0 Status register.
0	0h RW	**HOST_NOTIFY_INTREN (HNI):** Software sets this bit to 1 to enable the generation of interrupt or SMI# when HOST_NOTIFY_STS is 1. This enable does not affect the setting of the HOST_NOTIFY_STS bit. When the interrupt is generated, either PIRQB or SMI# is generated, depending on the value of the SMB_SMI_EN bit (D31, F3, Off40h, B1). If the HOST_NOTIFY_STS bit is set when this bit is written to a 1, then the interrupt (or SMI#) will be generated. The interrupt (or SMI#) is logically generated by ANDing the STS and INTREN bits.

15.2.17 Notify Device Address Register (NDA)—Offset 14h

Notify Device Address Register

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:1	0h RO/V	**DEVICE_ADDRESS (DEV_ADDR):** This field contains the 7-bit device address received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.
0	0h RO	Reserved.

15.2.18 Notify Data Low Byte Register (NDLB)—Offset 16h

Notify Data Low Byte Register

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RO	**DATA_LOW_BYTE (DLB):** This field contains the first (low) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.

15.2.19 Notify Data High Byte Register (NDHB)—Offset 17h

Notify Data High Byte Register

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RO	**DATA_HIGH_BYTE (DHB):** This field contains the second (high) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.

15.3 SMBus PCR Registers

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset). The offsets are DWORD aligned byte addresses.

Table 15-3. Summary of SMBus PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	TCO Configuration (TCOCFG)—Offset 0h	0h
Ch	Fh	General Control (GC)—Offset Ch	0h
10h	13h	Power Control Enable (PCE)—Offset 10h	9h

15.3.1 TCO Configuration (TCOCFG)—Offset 0h

TCO Configuration

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RW	**TCO IRQ Enable (IE):** When set, TCO IRQ is enabled, as selected by the TCO_IRQ_SEL field. When cleared, TCO IRQ is disabled.
6:0	0h RO	Reserved.

15.3.2 General Control (GC)—Offset Ch

General Control

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**Function Disable (FD):** When set to one, this disables the PCI config register space for the SMBus device.

15.3.3 Power Control Enable (PCE)—Offset 10h

Power Control Enable

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 9h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	1h RO	**Sleep Enable (SE):** When this bit is clear, the SMBus will never asset sleep to the controller. If set, then SMBus may assert sleep during power gating.
2	0h RO	**D3-Hot Enable (D3HE):** No support for D3 Hot power gating.
1	0h RO	**I3 Enable (I3E):** No support for S0i3 power gating.
0	1h RW	**PMC Request Enable (PMCRE):** When set to 1, the SMBus will engage power gating if it is idle and other conditions are met.

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16 SPI Interface (D31:F5)

16.1 SPI PCI Configuration Registers

Table 16-1. Summary of SPI PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device ID and Vendor SPI BAR1 MMIO (BIOS_SPI_BAR1)—Offset E0hID (BIOS_SPI_DID_VID)—Offset 0h	XXXX8086h
4h	7h	Status and Command (BIOS_SPI_STS_CMD)—Offset 4h	400h
8h	Bh	Revision ID and Class Code (BIOS_SPI_CC_RID)—Offset 8h	C8000XXh
Ch	Fh	BIST, Header Type, Latency Timer, Cache Line Size (BIOS_SPI_BIST_HTYPE_LT_CLS)—Offset Ch	0h
10h	13h	SPI BAR0 MMIO (BIOS_SPI_BAR0)—Offset 10h	0h
D0h	D3h	SPI Unsupported Request Status (BIOS_SPI_UR_STS_CTL)—Offset D0h	0h
D8h	DBh	BIOS Decode Enable (BIOS_SPI_BDE)—Offset D8h	FFCFh
DCh	DFh	BIOS Control (BIOS_SPI_BC)—Offset DCh	28h
E0h	E3h	SPI BAR1 MMIO (BIOS_SPI_BAR1)—Offset E0h	0h

16.1.1 Device ID and Vendor SPI BAR1 MMIO (BIOS_SPI_BAR1)—Offset E0hID (BIOS_SPI_DID_VID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function:

Default: XXXX8086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	-- RO/V	**Device Identification (DID):** Identifier for the SPI Flash Controller in Host Root Space. Refer to the Device and Version ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor Identification (VID):** This field identifies the manufacturer of the device. 0x8086 indicates Intel

16.1.2 Status and Command (BIOS_SPI_STS_CMD)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function:

Default: 400h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Detected Parity Error (DPE):** Detected Parity Error (DPE): 0 = No parity error detected by the controller. 1 = The controller detects a parity error on its interface.
30	0h RW/1C/V	**Signaled System Error (SSE):** Signaled System Error (SSE): 0 = No SERR# detected by the controller. 1 = The controller detects a SERR# on its interface.
29	0h RO	**Received Initiator Abort (RMA):** Hardwired to 0.
28	0h RO	**Received Target Abort (RTA):** Hardwired to 0.
27	0h RW/1C/V	**Signaled Target Abort (STA)**
26:25	0h RO	Reserved.
24	0h RO	**Initiator Data Parity Error (MDPE):** See the PCI spec.
23:21	0h RO	Reserved.
20	0h RO	**Capablities List (CAPL):** Hardwired to 0 indicating that a Capabilities List is not present.
19	0h RO	**Interrupt Status (INTS):** Hardwired to 0.
18:11	0h RO	Reserved.
10	1h RO	**Interrupt Disable (INTD):** Hardwired to 1 br] 0 = Interrupt is enabled 1 = interrupt is disabled
9	0h RO	Reserved.
8	0h RW	**System Error Enable (SERREN):** 0 = SERR# is disabled 1 = SERR# is Enabled
7	0h RO	Reserved.
6	0h RW	**Parity Error Response (PERRR):** Hardwired to 0. No response to parity errors from the controller.
5:3	0h RO	Reserved.
2	0h RW	**Bus Initiator Enable (BME):** 0 = Disabled 1 = Enabled
1	0h RW	**Memory Space Enable (MSE):** 0 = Disables memory mapped Configuration space. 1 = Enables memory mapped Configuration space.
0	0h RO	**IO Space Enable (IOSE):** 0 = Disabled 1 = Enabled

16.1.3 Revision ID and Class Code (BIOS_SPI_CC_RID)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function:

Default: C8000XXh

Bit Range	Default & Access	Field Name (ID): Description
31:24	Ch RO	**Base Class Code (BCC):** Base Class Code
23:16	80h RO	**Sub-Class Code (SCC):** Sub-Class Code
15:8	0h RO	**Programming Interface (PI):** Programming Interface
7:0	-- RO/V	**Revision ID (RID):** Revision ID (RID): Indicates the part revision. Refer to the Device and Version ID Table in Volume 1 for the default value.

16.1.4 BIST, Header Type, Latency Timer, Cache Line Size (BIOS_SPI_BIST_HTYPE_LT_CLS)—Offset Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:16	0h RO	**Header Type (HTYPE):** Implements Type 0 Configuration.
15:8	0h RO	**Latency Timer (LT):** Does not apply. Hardwired to 0.
7:0	0h RO	**Cacheline Size (CLSZ):** Does not apply. Hardwired to 0.

16.1.5 SPI BAR0 MMIO (BIOS_SPI_BAR0)—Offset 10h

Base Address for BAR0 - MMIO Registers

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**Memory BAR (MEMBAR):** Software programs this register with the base address of the device's memory region. The Host/BIOS MMIO registers in the flash controller are offset from this BAR.
11:4	0h RO	**Memory Size (MEMSIZE):** Hardwired to 0 to indicate 4KB of memory space
3	0h RO	**Prefetchable (PREFETCH):** A device can mark a range as prefetchable if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables.
2:1	0h RO	**Type (TYP):** Hardwired to 0 to indicate that Base register is 32 bits wide and mapping can be done anywhere in the 32-bit Memory Space.
0	0h RO	**Memory Space Indicator (MEMSPACE):** Hardwired to 0 to identify a Memory BAR.

16.1.6 SPI Unsupported Request Status (BIOS_SPI_UR_STS_CTL)—Offset D0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW/1C/V	**Unsupported Request Detected (URD):** Set to 1 by hardware upon detecting an Unspported Request that is not considered an Advisory Non-Fatal error. Cleared to 0 when software writes a 1 to this register.
0	0h RW	**Unsupported Request Reporting Enabled (URRE):** If set to 1 by software, the flash controller generates a DoSERR sideband message when the URD bit transitions from 0 to 1.

16.1.7 BIOS Decode Enable (BIOS_SPI_BDE)—Offset D8h

This register only effects BIOS decode if BIOS is resident on SPI.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function:

Default: FFCFh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	1h RO	**F8-FF Enable (EF8):** Enables decoding of 512K of the following BIOS ranges: FFF80000h - FFFFFFFFh FFB80000h - FFBFFFFFh
14	1h RW/L	**F0-F8 Enable (EF0):** Enables decoding of 512K of the following BIOS ranges: FFF00000h - FFF7FFFFh FFB00000h - FFB7FFFFh
13	1h RW/L	**E8-EF Enable (EE8):** Enables decoding of 512K of the following BIOS ranges: FFE80000h - FFEFFFFFh FFA80000h - FFAFFFFFh
12	1h RW/L	**E0-E8 Enable (EE0):** Enables decoding of 512K of the following BIOS ranges: FFE00000h - FFE7FFFFh FFA00000h - FFA7FFFFh
11	1h RW/L	**D8-DF Enable (ED8):** Enables decoding of 512K of the following BIOS ranges: FFD80000h - FFDFFFFFh FF980000h - FF9FFFFFh
10	1h RW/L	**D0-D7 Enable (ED0):** Enables decoding of 512K of the following BIOS ranges: FFD00000h - FFD7FFFFh FF900000h - FF97FFFFh
9	1h RW/L	**C8-CF Enable (EC8):** Enables decoding of 512K of the following BIOS ranges: FFC80000h - FFCFFFFFh FF880000h - FF8FFFFFh
8	1h RW/L	**C0-C7 Enable (EC0):** Enables decoding of 512K of the following BIOS ranges: FFC00000h - FFC7FFFFh FF800000h - FF87FFFFh
7	1h RW/L	**Legacy F Segment Enable (LFE):** Legacy F Segment Enable (LFE): This enables the decoding of the legacy 64KB range at F0000h - FFFFFh
6	1h RW/L	**Legacy E Segment Enable (LEE):** Legacy E Segment Enable (LFE): This enables the decoding of the legacy 64KB range at E0000h - EFFFFh
5:4	0h RO	Reserved.
3	1h RW/L	**70-7F Enable (E70):** Enables decoding of 1MB of the following BIOS ranges: FF700000h - FF7FFFFFh FF300000h - FF3FFFFFh
2	1h RW/L	**60-6F Enable (E60):** Enables decoding of 1MB of the following BIOS ranges: FF600000h - FF6FFFFFh FF200000h - FF2FFFFFh
1	1h RW/L	**50-5F Enable (E50):** Enables decoding of 1MB of the following BIOS ranges: FF500000h - FF5FFFFFh FF100000h - FF1FFFFFh
0	1h RW/L	**40-4F Enable (E40):** Enables decoding of 1MB of the following BIOS ranges: FF400000h - FF4FFFFFh FF000000h - FF0FFFFFh

16.1.8 BIOS Control (BIOS_SPI_BC)—Offset DCh

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function:

Default: 28h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RW/L	**Extended BIOS Range Lock (EXT_BIOS_LOCK):** When set, prevents BIOS_SPI_BAR1.MEMBAR, EXT_BIOS_EN and EXT_BIOS_LIMIT_OFFSET from being changed. This bit can only be written from 0 to 1 once. This field is only used when the extended BIOS direct read range decoding is supported. (SPI_EXT_BIOS_BAR1_EN=1).
27	0h RW/L	**Extended BIOS Range Enable (EXT_BIOS_EN):** When set, enables the extended BIOS range decoding on SPI BAR1.This field is only used when the extended BIOS direct read range decoding is supported. (SPI_EXT_BIOS_BAR1_EN=1). This field is locked when EXT_BIOS_LOCK =1.
26:12	0h RW/L	**Extended BIOS Range Limit Offset (EXT_BIOS_LIMIT_OFFSET):** This field defines the offset of the extended BIOS range upper limit from the upper limit of the BIOS region in the flash.This field is only used when the extended BIOS direct read range decoding is supported. (SPI_EXT_BIOS_BAR1_EN=1).
11	0h RW/L	**Async SMI Enable for BIOS Write Protection (ASE_BWP):** When set to '1' the flash controller will generate an SMI when it blocks a BIOS write or erase due to WPD = 0. The value in this field can be written by software as long as the BIOS Interface Lock-Down (BILD) is not set.
10	0h RO/V	**Asynchronous SMI Status (SPI_ASYNC_SS):** Status indication that the SPI Flash Controller has asserted an asynchronous SMI. Hardware clears the bit when it sends the De-assert SMI message. 0 : default state 1 : SPI flash controller asserted asynchronous SMI
9	0h RO	Reserved.
8	0h RW/1C/V	**Synchronous SMI Status (SPI_SYNC_SS):** Status indication that the SPI Flash Controller has asserted a synchronous SMI. Hardware clears the bit when it sends the De-assert Synchronous SMI message. 0 : default state 1 : SPI flash controller asserted Synchronous SMI
7	0h RW/L	**BIOS Interface Lock-Down (BILD):** When set, prevents TS and BBS from being changed. This bit can only be written from 0 to 1 once.
6	0h RW/V/L	**Boot BIOS Strap (BBS):** This field determines the destination of accesses to the BIOS memory range. 0 = SPI 1 = Reserved the range that is decoded is further qualified by BIOS Decode Enable. The value in this field can be overwritten by software as long as the BIOS Interface Lock-Down (BILD) is not set
5	1h RW/L	**Enable InSMM.STS (EISS):** When this bit is set, the BIOS region is not writable until the CPU sets the InSMM.STS bit. If this bit [5] is set, then WPD must be a '1' and InSMM.STS(0xFED3_0880[0]) must be '1' also in order to write to BIOS region of SPI Flash. If this bit [5] is clear, then the InSMM.STS is a don't care. This bit is locked by LE
4	0h RO/V	**Top Swap Status (TSS):** This bit provides a read-only path to view the state of the Top Swap bit. It is duplicated here to be consistent with the eSPI version of the BC register.

Bit Range	Default & Access	Field Name (ID): Description
3:2	2h RW	**SPI Read Configuration (SRC):** These bits are located in PCI Config space to allow them to be set early in the boot flow. This 2-bit field controls two policies related to BIOS reads on the SPI interface: Bit 3- Prefetch Enable Bit 2- Cache Disable Settings are summarized below: 00 = No prefetching, but caching enabled. Direct Memory reads load the read buffer cache with valid data, allowing repeated reads to the same range to complete quickly 01 = No prefetching and no caching. One-to-one correspondence of host BIOS reads to SPI cycles. This value can be used to invalidate the cache. 10 = Prefetching and Caching enabled. This mode is used for long sequences of short reads to consecutive addresses (i.e. shadowing) 11 = Unsupported. Caching must be enabled when Prefetching is enabled.
1	0h RW/L	**Lock Enable (LE):** When set, setting the WPD bit will cause SMI. When cleared, setting the WPD bit will not cause SMI. Once set, this bit can only be cleared by a PLTRST#. When this bit is set, EISS - bit [5] of this register is locked down.
0	0h RW	**Write Protect Disable (WPD):** When set, access to the BIOS space is enabled for both read and write cycles to BIOS. When cleared, only read cycles are permitted to the FWH or SPI flash. When this bit is written from a '0' to a '1' and the LE bit is also set, an SMI# is generated. This ensures that only SMM code can update BIOS.

16.1.9 SPI BAR1 MMIO (BIOS_SPI_BAR1)—Offset E0h

Base Address for BAR1 - Direct Reads to Flash Region 1 (Extended Bios Region)

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RW/L	**Memory BAR (MEMBAR):** Software programs this register with the base address of the device's memory region. The Host/BIOS MMIO registers in the flash controller are offset from this BAR. This BAR is locked when EXT_BIOS_LOCK =1, and it is used to direct read the extended BIOS region above 16MB.
24:4	0h RO	**Memory Size (MEMSIZE):** Hardwired to 0 to indicate 32MB (RTL uses parameter EXT_BIOS_SIZE) of memory space.
3	0h RO	**Prefetchable (PREFETCH):** A device can mark a range as prefetchable if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables.
2:1	0h RO	**Type (TYP):** Hardwired to 0 to indicate that Base register is 32 bits wide and mapping can be done anywhere in the 32-bit Memory Space.
0	0h RO	**Memory Space Indicator (MEMSPACE):** Hardwired to 0 to identify a Memory BAR.

16.2 SPI Memory Mapped Registers

The SPI memory mapped registers are accessed based upon offsets from SPI_BAR0 (in PCI config SPI_BAR0 register).

Table 16-2. Summary of SPI Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	BIOS Flash Primary Region (BIOS_BFPREG)—Offset 0h	0h
4h	7h	Hardware Sequencing Flash Status and Control (BIOS_HSFSTS_CTL)—Offset 4h	2000h
8h	Bh	Flash Address (BIOS_FADDR)—Offset 8h	0h
Ch	Fh	Discrete Lock Bits (BIOS_DLOCK)—Offset Ch	0h
10h	13h	Flash Data 0 (BIOS_FDATA0)—Offset 10h	0h
14h	17h	Flash Data 1 (BIOS_FDATA1)—Offset 14h	0h
18h	1Bh	Flash Data 2 (BIOS_FDATA2)—Offset 18h	0h
1Ch	1Fh	Flash Data 3 (BIOS_FDATA3)—Offset 1Ch	0h
20h	23h	Flash Data 4 (BIOS_FDATA4)—Offset 20h	0h
24h	27h	Flash Data 5 (BIOS_FDATA5)—Offset 24h	0h
28h	2Bh	Flash Data 6 (BIOS_FDATA6)—Offset 28h	0h
2Ch	2Fh	Flash Data 7 (BIOS_FDATA7)—Offset 2Ch	0h
30h	33h	Flash Data 8 (BIOS_FDATA8)—Offset 30h	0h
34h	37h	Flash Data 9 (BIOS_FDATA9)—Offset 34h	0h
38h	3Bh	Flash Data 10 (BIOS_FDATA10)—Offset 38h	0h
3Ch	3Fh	Flash Data 11 (BIOS_FDATA11)—Offset 3Ch	0h
40h	43h	Flash Data 12 (BIOS_FDATA12)—Offset 40h	0h
44h	47h	Flash Data 13 (BIOS_FDATA13)—Offset 44h	0h
48h	4Bh	Flash Data 14 (BIOS_FDATA14)—Offset 48h	0h
4Ch	4Fh	Flash Data 15 (BIOS_FDATA15)—Offset 4Ch	0h
50h	53h	Flash Region Access Permissions (BIOS_FRACC)—Offset 50h	42C2h
54h	57h	Flash Region 0 (BIOS_FREG0)—Offset 54h	0h
58h	5Bh	Flash Region 1 (BIOS_FREG1)—Offset 58h	7FFFh
5Ch	5Fh	Flash Region 2 (BIOS_FREG2)—Offset 5Ch	7FFFh
60h	63h	Flash Region 3 (BIOS_FREG3)—Offset 60h	7FFFh
64h	67h	Flash Region 4 (BIOS_FREG4)—Offset 64h	7FFFh
68h	6Bh	Flash Region 5 (BIOS_FREG5)—Offset 68h	7FFFh
84h	87h	Flash Protected Range 0 (BIOS_FPR0)—Offset 84h	0h
88h	8Bh	Flash Protected Range 1 (BIOS_FPR1)—Offset 88h	0h
8Ch	8Fh	Flash Protected Range 2 (BIOS_FPR2)—Offset 8Ch	0h
90h	93h	Flash Protected Range 3 (BIOS_FPR3)—Offset 90h	0h
94h	97h	Flash Protected Range 4 (BIOS_FPR4)—Offset 94h	0h
98h	9Bh	Global Protected Range 0 (BIOS_GPR0)—Offset 98h	0h
B0h	B3h	Secondary Flash Region Access Permissions (BIOS_SFRACC)—Offset B0h	0h
B4h	B7h	Flash Descriptor Observability Control (BIOS_FDOC)—Offset B4h	0h
B8h	BBh	Flash Descriptor Observability Data (BIOS_FDOD)—Offset B8h	0h
C0h	C3h	Additional Flash Control (BIOS_AFC)—Offset C0h	0h
C4h	C7h	Vendor Specific Component Capabilities for Component 0 (BIOS_SFDP0_VSCC0)—Offset C4h	2000h

Table 16-2. Summary of SPI Memory Mapped Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
C8h	CBh	Vendor Specific Component Capabilities for Component 1 (BIOS_SFDP1_VSCC1)—Offset C8h	2000h
CCh	CFh	Parameter Table Index (BIOS_PTINX)—Offset CCh	0h
D0h	D3h	Parameter Table Data (BIOS_PTDATA)—Offset D0h	0h
D4h	D7h	SPI Bus Requester Status (BIOS_SBRS)—Offset D4h	0h

16.2.1 BIOS Flash Primary Region (BIOS_BFPREG)—Offset 0h

BIOS Flash Primary Region

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	Reserved.
30:16	0h RO/V	**BIOS Flash Primary Region Limit (PRL):** This specifies address bits 26:12 for the Primary Region Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Limit, or the Flash Descriptor.FLREG6.Region Limit depending on the BFPREG.SBRS bit.
15	0h RO	Reserved.
14:0	0h RO/V	**BIOS Flash Primary Region Base (PRB):** This specifies address bits 26:12 for the Primary Region Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Base, or the Flash Descriptor.FLREG6.Region Base depending on the BFPREG.SBRS bit.

16.2.2 Hardware Sequencing Flash Status and Control (BIOS_HSFSTS_CTL)—Offset 4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 2000h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW	**Flash SPI SMI# Enable (FSMIE):** When set to 1, the SPI asserts an SMI# request whenever the Flash Cycle Done bit is 1.
30	0h RO	Reserved.
29:24	0h RW	**Flash Data Byte Count (FDBC):** This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The contents of this register are 0s based with 0b representing 1 byte and 3Fh representing 64 bytes. The number of bytes transferred is the value of this field plus 1. This field is ignored for the Block Erase command.
23:22	0h RO	Reserved.
21	0h RW	**Write Enable Type (WET):** 0: Use 06h as the write enable instruction 1: Use 50h as the write enable instruction. Note that this setting is not supported as no supported flash devices require the 50h opcode to enable a non-volatile status register write.
20:17	0h RW	**Flash Cycle (FCYCLE):** This field defines the Flash SPI cycle type generated to the FLASH when the FGO bit is set as defined below: 0 Read (1 up to 64 bytes by setting FDBC) 1 Reserved 2 Write (1 up to 64 bytes by setting FDBC) 3 4k Block Erase 4 64k Sector erase 5 Read SFDP 6 Read JEDEC ID 7 write status 8 read status 9 RPMC Op1 A RPMC Op2 Flash controller hardware automatically inserts a write enable opcode prior to Write and erase operations. Hardware automatically polls for device not-busy using read status after write and erase operations. If the device does not support 64k erase size (or if it does not support SFDP) then only 4k is allowed. Note: if reserved 1 is programmed to this field, flash controller will handle it as if it is 0 (Read)
16	0h RW/1S/V	**Flash Cycle Go (FGO):** A write to this register with a 1 in this bit initiates a request to the Flash SPI Arbiter to start a cycle. This register is cleared by hardware when the cycle is granted by the SPI arbiter to run the cycle on the SPI bus. When the cycle is complete, the FDONE bit is set. Software is forbidden to write to any register in the HSFLCTL register between the FGO bit getting set and the FDONE bit being cleared. Any attempt to violate this rule will be ignored by hardware. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1. This saves an additional memory write. This bit always returns 0 on reads.
15	0h RW/L	**Flash Configuration Lock-Down (FLOCKDN):** When set to 1, those Flash Program Registers that are locked down by this FLOCKDN bit cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
14	0h RO/V	**Flash Descriptor Valid (FDV):** This bit is set to a 1 if the Flash Controller read the correct Flash Descriptor Signature. If the Flash Descriptor Valid bit is not 1 , software cannot use the Hardware Sequencing registers, but must use the software sequencing registers. Any attempt to use the Hardware Sequencing registers will result in the FCERR bit being set
13	1h RO/V	**Flash Descriptor Override Pin-Strap Status (FDOPSS):** This register reflects the value the Flash Descriptor Override Pin-Strap. '1': No override '0': The Flash Descriptor Override strap is set
12	0h RW/L	**PRR3 PRR4 Lock-Down (PRR34_LOCKDN):** When set to 1, the BIOS PRR3 and PRR4 registers cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.

Bit Range	Default and Access	Field Name (ID): Description
11	0h RW/L	**Write Status Disable (WRSDIS):** 0 = Write status operation may be issued using Hardware Sequencing. 1 = Write status is not allowed as a Hardware Sequencing operation. The flash controller will block the operation and set the FCERR bit when software sets the 'go' bit. This bit is locked when FLOCKDN is set.
10:6	0h RO	Reserved.
5	0h RO/V	**SPI Cycle In Progress (H_SCIP):** Hardware sets this bit when software sets the Flash Cycle Go (FGO) bit in the Hardware Sequencing Flash Control register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0.
4:3	0h RO	Reserved.
2	0h RW/1C/V	**Access Error Log (H_AEL):** Hardware sets this bit to a 1 when an attempt was made to access the BIOS region using the direct access method or an access to the BIOS Program Registers that violated the security restrictions. This bit is simply a log of an access security violation. This bit is cleared by software writing a '1'.
1	0h RW/1C/V	**Flash Cycle Error (FCERR):** Hardware sets this bit to 1 when a program register access is blocked to the FLASH due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1 or until hardware reset occurs. Software must clear this bit before setting the FLASH Cycle GO bit in this register.
0	0h RW/1C/V	**Flash Cycle Done (FDONE):** The PCH sets this bit to 1 when the SPI Cycle completes after software previously set the FGO bit. This bit remains asserted until cleared by software writing a 1 or hardware reset. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access.

16.2.3 Flash Address (BIOS_FADDR)—Offset 8h

Flash Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26:0	0h RW	**Flash Linear Address (FLA):** The FLA is the starting byte linear address of a SPI Read or Write cycle or an address within a Block for the Block Erase command. The Flash Linear Address must fall within a region for which BIOS has access permissions. Hardware must convert the FLA into a Flash Physical Address (FPA) before running this cycle on the SPI bus.

16.2.4 Discrete Lock Bits (BIOS_DLOCK)—Offset Ch

Lockable BIOS registers may be locked by either the global FLOCKDN bit or by the individual DLOCK bit. Each lockable bit in this register is locked either by itself or by the FLOCKDN bit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:17	0h RO	Reserved.
16	0h RW/L	**SSEQ Lock-Down (SSEQLOCKDN):** BIOS Software Sequencing registers are locked when the logical OR of this bit and FLOCKDN is true. The affected registers are SSFSTS_CTL.SCF, PREOP_OPTYPE, OPMENU0, and OPMENU1. Once set to 1 this register is only cleared by host partition reset.
15	0h RW/L	**Spare1 (SPARE1):** Once set to 1 this register is only cleared by host partition reset.
14	0h RW/L	**Spare2 (SPARE2):** Once set to 1 this register is only cleared by host partition reset.
13	0h RW/L	**Spare3 (SPARE3):** Once set to 1 this register is only cleared by host partition reset.
12	0h RW/L	**PR4 Lock-Down (PR4LOCKDN):** BIOS PR4 register is locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by BIOS partition reset.
11	0h RW/L	**PR3 Lock-Down (PR3LOCKDN):** BIOS PR3 register is locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by BIOS partition reset.
10	0h RW/L	**PR2 Lock-Down (PR2LOCKDN):** BIOS PR2 register is locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by BIOS partition reset.
9	0h RW/L	**PR1 Lock-Down (PR1LOCKDN):** BIOS PR1 register is locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by BIOS partition reset.
8	0h RW/L	**PR0 Lock-Down (PR0LOCKDN):** BIOS PR0 register is locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by BIOS partition reset.
7	0h RW/L	**Spare4 (SPARE4):** Once set to 1 this register is only cleared by host partition reset.
6	0h RW/L	**Spare5 (SPARE5):** Once set to 1 this register is only cleared by host partition reset.
5	0h RW/L	**Spare6 (SPARE6):** Once set to 1 this register is only cleared by host partition reset.
4	0h RW/L	**Spare7 (SPARE7):** Once set to 1 this register is only cleared by host partition reset.
3	0h RW/L	**SBMRAG Lock-Down (SBMRAGLOCKDN):** BIOS SFRACC.BMRAG register bits are locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by host partition reset.

Bit Range	Default and Access	Field Name (ID): Description
2	0h RW/L	**SBMWAG Lock-Down (SBMWAGLOCKDN):** BIOS SFRACC.BMWAG register bits are locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by host partition reset.
1	0h RW/L	**BMRAG Lock-Down (BMRAGLOCKDN):** BIOS FRACC.BMRAG register bits are locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by host partition reset.
0	0h RW/L	**BMWAG Lock-Down (BMWAGLOCKDN):** BIOS FRACC.BMWAG register bits are locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by host partition reset.

16.2.5 Flash Data 0 (BIOS_FDATA0)—Offset 10h

Flash Data 0

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 0 (FD0):** This field is shifted out as the SPI Data on the Initiator-Out Target-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Initiator-In Target-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13-...8-23-22-...16-31...24. Bit 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

16.2.6 Flash Data 1 (BIOS_FDATA1)—Offset 14h

Flash Data 1

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 1 (FD1):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD0 has completely shifted in/out.

16.2.7 Flash Data 2 (BIOS_FDATA2)—Offset 18h

Flash Data 2

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 2 (FD2):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD1 has completely shifted in/out.

16.2.8 Flash Data 3 (BIOS_FDATA3)—Offset 1Ch

Flash Data 3

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 3 (FD3):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD2 has completely shifted in/out.

16.2.9 Flash Data 4 (BIOS_FDATA4)—Offset 20h

Flash Data 4

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 4 (FD4):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD3 has completely shifted in/out.

16.2.10 Flash Data 5 (BIOS_FDATA5)—Offset 24h

Flash Data 5

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 5 (FD5):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD4 has completely shifted in/out.

16.2.11 Flash Data 6 (BIOS_FDATA6)—Offset 28h

Flash Data 6

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 6 (FD6):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD5 has completely shifted in/out.

16.2.12 Flash Data 7 (BIOS_FDATA7)—Offset 2Ch

Flash Data 7

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 7 (FD7):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD6 has completely shifted in/out.

16.2.13 Flash Data 8 (BIOS_FDATA8)—Offset 30h

Flash Data 8

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 8 (FD8):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD7 has completely shifted in/out.

16.2.14 Flash Data 9 (BIOS_FDATA9)—Offset 34h

Flash Data 9

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 9 (FD9):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD8 has completely shifted in/out.

16.2.15 Flash Data 10 (BIOS_FDATA10)—Offset 38h

Flash Data 10

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 10 (FD10):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD9 has completely shifted in/out.

16.2.16 Flash Data 11 (BIOS_FDATA11)—Offset 3Ch

Flash Data 11

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 11 (FD11):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD10 has completely shifted in/out.

16.2.17 Flash Data 12 (BIOS_FDATA12)—Offset 40h

Flash Data 12

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 12 (FD12):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD11 has completely shifted in/out.

16.2.18 Flash Data 13 (BIOS_FDATA13)—Offset 44h

Flash Data 13

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 13 (FD13):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD12 has completely shifted in/out.

16.2.19 Flash Data 14 (BIOS_FDATA14)—Offset 48h

Flash Data 14

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 14 (FD14):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD13 has completely shifted in/out.

16.2.20 Flash Data 15 (BIOS_FDATA15)—Offset 4Ch

Flash Data 15

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 15 (FD15):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD14 has completely shifted in/out.

16.2.21 Flash Region Access Permissions (BIOS_FRACC)—Offset 50h

Flash Region Access Permissions

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 42C2h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RW/L	**BIOS Initiator Write Access Grant (BMWAG):** BIOS Initiator Write Access Grant (BMWAG): Each bit [31:24] corresponds to Initiator[7:0]. BIOS can grant one or more Initiators write access to the BIOS region 1 overriding the permissions in the Flash Descriptor. The contents of this register are locked by the FLOCKDN bit.

Bit Range	Default and Access	Field Name (ID): Description
23:16	0h RW/L	**BIOS Initiator Read Access Grant (BMRAG):** BIOS Initiator Read Access Grant (BMRAG): Each bit [23:16] corresponds to Initiator[7:0]. BIOS can grant one or more Initiators read access to the BIOS region 1 overriding the read permissions in the Flash Descriptor. The contents of this register are locked by the FLOCKDN bit
15:8	42h RO/V	**BIOS Region Write Access (BRWA):** BIOS Region Write Access (BRWA): Each bit [15:8] corresponds to Regions [7:0]. If the bit is set, this Initiator can erase and write that particular region through register accesses. The contents of this register are that of the Flash Descriptor.Flash Initiator 1.Initiator Region Write Access OR a particular Initiator has granted BIOS write permissions in their Initiator Write Access Grant register OR the Flash Descriptor Security Override strap is set. BIOS always have the write access to its own Region 1 and Region 6 by default.
7:0	C2h RO/V	**BIOS Region Read Access (BRRA):** BIOS Region Read Access (BRRA): Each bit [7:0] corresponds to Regions [7:0]. If the bit is set, this Initiator can read that particular region through register accesses. The contents of this register are that of the Flash Descriptor.Flash Initiator 1.Initiator Region Write Access OR a particular Initiator has granted BIOS read permissions in their Initiator Read Access Grant register OR the Flash Descriptor Security Override strap is set. BIOS always have the read access to its own Region 1 and Region 6 by default.

16.2.22 Flash Region 0 (BIOS_FREG0)—Offset 54h

Flash Region 0

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	Reserved.
30:16	0h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region 0 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Limit.
15	0h RO	Reserved.
14:0	0h RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region 0 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Base.

16.2.23 Flash Region 1 (BIOS_FREG1)—Offset 58h

Flash Region 1

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 7FFFh

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	Reserved.
30:16	0h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region 1 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Limit.
15	0h RO	Reserved.
14:0	7FFFh RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region 1 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Base.

16.2.24 Flash Region 2 (BIOS_FREG2)—Offset 5Ch

Flash Region 2

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 7FFFh

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	Reserved.
30:16	0h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region 2 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Limit.
15	0h RO	Reserved.
14:0	7FFFh RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region 2 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Base.

16.2.25 Flash Region 3 (BIOS_FREG3)—Offset 60h

Flash Region 3

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 7FFFh

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	Reserved.
30:16	0h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region 3 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Limit.
15	0h RO	Reserved.
14:0	7FFFh RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region 3 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Base.

16.2.26 Flash Region 4 (BIOS_FREG4)—Offset 64h

Flash Region 4

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 7FFFh

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	Reserved.
30:16	0h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region 4 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG4.Region Limit.
15	0h RO	Reserved.
14:0	7FFFh RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region 4 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG4.Region Base.

16.2.27 Flash Region 5 (BIOS_FREG5)—Offset 68h

Flash Region 5

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 7FFFh

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	Reserved.
30:16	0h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region 5 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG5.Region Limit.
15	0h RO	Reserved.
14:0	7FFFh RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region 5 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG5.Region Base.

16.2.28 Flash Protected Range 0 (BIOS_FPR0)—Offset 84h

This register cannot be written when the FLOCKDN bit is set to 1.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0h RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

16.2.29 Flash Protected Range 1 (BIOS_FPR1)—Offset 88h

This register cannot be written when the FLOCKDN bit is set to 1.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0h RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

16.2.30 Flash Protected Range 2 (BIOS_FPR2)—Offset 8Ch

This register cannot be written when the FLOCKDN bit is set to 1.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0h RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

16.2.31 Flash Protected Range 3 (BIOS_FPR3)—Offset 90h

This register cannot be written when the PRR34_LOCKDN bit is set to 1

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0h RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

16.2.32 Flash Protected Range 4 (BIOS_FPR4)—Offset 94h

This register cannot be written when the PRR34_LOCKDN bit is set to 1

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0h RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

16.2.33 Global Protected Range 0 (BIOS_GPR0)—Offset 98h

This register is initialized via softstraps. This protected range applies globally to all Initiators / flash requesters.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO/V	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0h RO/V	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range. Note: If either Write or Read protection is enabled, then Limit must be configured greater than or equal to Base.
15	0h RO/V	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0h RO/V	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range. Note: If either Write or Read protection is enabled, then Limit must be configured greater than or equal to Base.

16.2.34 Secondary Flash Region Access Permissions (BIOS_SFRACC)—Offset B0h

Secondary Flash Region Access Permissions

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RW/L	**Secondary BIOS Initiator Write Access Grant (SECONDARYBIOS_MWAG):** Each bit 31:29 corresponds to Initiator7:0. BIOS can grant one or more Initiators write access to the Secondary BIOS region 6 overriding the permissions in the Flash Descriptor. Bits for unassigned Initiators are reserved. The contents of this register are locked by the FLOCKDN bit.
23:16	0h RW/L	**Secondary BIOS Initiator Read Access Grant (SECONDARYBIOS_MRAG):** Each bit 28:16 corresponds to Initiator7:0. BIOS can grant one or more Initiators read access to the Secondary BIOS region 6 overriding the read permissions in the Flash Descriptor. Bits for unassigned Initiators are reserved. The contents of this register are locked by the FLOCKDN bit.
15:0	0h RO	Reserved.

16.2.35 Flash Descriptor Observability Control (BIOS_FDOC)—Offset B4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14:12	0h RW	**Flash Descriptor Section Select (FDSS):** Selects which section within the loaded Flash Descriptor to observe. 000: Flash Signature and Descriptor Map 001: Component 010: Region 011: Initiator Others: Reserved
11:2	0h RW	**Flash Descriptor Section Index (FDSI):** Selects the DW offset within the Flash Descriptor Section to observe.
1:0	0h RO	Reserved.

16.2.36 Flash Descriptor Observability Data (BIOS_FDOD)—Offset B8h

Flash Descriptor Observability Data

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Flash Descriptor Section Data (FDSD):** Returns the DW of data to observe as selected in the Flash Descriptor Observability Control.

16.2.37 Additional Flash Control (BIOS_AFC)—Offset C0h

Additional Flash Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW/V/P	**Stop Prefetch on Flush Pending (SPFP):** When set to 1, the in progress of a prefetch will be ended if subsequence access from the Initiator of the same interface is detected to be a cache-miss and read cache will be flushed. When set to 0, the prefetch will be allowed to complete prior to flushing.

16.2.38 Vendor Specific Component Capabilities for Component 0 (BIOS_SFDP0_VSCC0)—Offset C4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 2000h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO/V	**Component Property Parameter Table Valid (CPPTV):** This bit is set to a 1 if the Flash Controller detects a valid SFDP Component Property Parameter Table in Component 0. Note: If this bit is set software must not overwrite bits that were initialized by hardware via SFDP discovery.
30	0h RW/L	**Vendor Component Lock (VCL):** 0: The lock bit is not set 1: The Vendor Component Lock bit is set. This register locks itself when set.
29	0h RW/V/L	**64k Erase Valid (EO_64K_VALID):** 0: The EO_64k opcode is not valid. 1: The EO_64k opcode is valid.
28	0h RW/V/L	**4k Erase Valid (EO_4K_VALID):** 0: The EO_4k opcode is not valid. 1: The EO_4k opcode is valid.
27	0h RW/L	**RPMC Supported (RPMC_SUPPORTED):** 0: The device does not support RPMC. 1: The device supports RPMC.
26	0h RW/V/L	**Deep Powerdown Supported (DEEP_PWRDN_SUPPORTED):** 0: The device does not support Deep Powerdown. 1: The device supports Deep Powerdown.
25	0h RW/V/L	**Suspend/Resume Supported (SUSPEND_RESUME_SUPPORTED):** 1: The device does not support Suspend/Resume. 0: The device supports Suspend/Resume.
24	0h RW/V/L	**Soft Reset Supported (SOFT_RST_SUPPORTED):** 0: The device does not support Soft Reset. 1: The device supports Soft Reset.
23:16	0h RW/V/L	**64k Erase Opcode (EO_64K):** This register is programmed with the Flash 64k sector erase instruction opcode for component 0. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit.
15:8	20h RW/V/L	**4k Erase Opcode (EO_4K):** This register is programmed with the Flash 64k sector erase instruction opcode for component 0. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit.
7:5	0h RW/V/L	**Quad Enable Requirements (QER):** 000 = Part does not require a Quad Enable bit to be set, either because Quad is not supported or because the manufacturer somehow permanently enables Quad capability. 001 = Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to status register clears all bits in register 2, therefore status register writes MUST be two bytes. 010 = Part requires bit 6 of status register 1 to be set to enable quad IO. 011 = Part requires bit 7 of the configuration register to be set to enable Quad. 100 = Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to the status register does not clear the second byte. This register is locked by the Vendor Component Lock (VCL) bit. If the SFDP table contains this information, the flash controller loads these bits from the table. The flash controller uses this information to prevent clearing the QE bit in the flash device's status register when WSR=1.
4	0h RW/V/L	**Write Enable on Write Status (WEWS):** 0 = 50h is the opcode to enable a status register write 1 : 06h is the opcode to enable a status register write This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit. Note: Hardware ignores the state of this bit.

Bit Range	Default and Access	Field Name (ID): Description
3	0h RW/V/L	**Write Status Required (WSR):** 0 = No requirement to write to the Write Status Register prior to a write 1 = A write is required to the Write Status Register prior to write and erase to remove any protection. This is required for SST components. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit. Note: Hardware ignores the state of this bit.
2	0h RW/V/L	**Write Granularity (WG):** 0 : Reserved 1 : 64 Byte This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit. Note: Hardware ignores the state of this bit.
1:0	0h RO	Reserved.

16.2.39 Vendor Specific Component Capabilities for Component 1 (BIOS_SFDP1_VSCC1)—Offset C8h

This register pertain to cycles targeting addresses outside of Component 0. The lockable bits in this register are locked when either CPPTV is set to 1 by hardware or when VCL is 1.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 2000h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO/V	**Component Property Parameter Table Valid (CPPTV):** This bit is set to a 1 if the Flash Controller detects a valid SFDP Component Property Parameter Table in Component 1. Note: If this bit is set software must not overwrite bits that were initialized by hardware via SFDP discovery RO
30	0h RO	Reserved.
29	0h RW/V/L	**64k Erase Valid (EO_64K_VALID):** 0: The EO_64k opcode is not valid. 1: The EO_64k opcode is valid.
28	0h RW/V/L	**4k Erase Valid (EO_4K_VALID):** 0: The EO_4k opcode is not valid. 1: The EO_4k opcode is valid.
27	0h RW/L	**RPMC Supported (RPMC_SUPPORTED):** 0 The device does not support RPMC. 1 The device supports RPMC.
26	0h RW/V/L	**Deep Powerdown Supported (DEEP_PWRDN_SUPPORTED):** 0 The device does not support Deep Powerdown. 1 The device supports Deep Powerdown.
25	0h RW/V/L	**Suspend/Resume Supported (SUSPEND_RESUME_SUPPORTED):** 1 the device supports Suspend/Resume
24	0h RW/V/L	**Soft Reset Supported (SOFT_RST_SUPPORTED):** 0: The device does not support Soft Reset. 1: The device supports Soft Reset.
23:16	0h RW/V/L	**64k Erase Opcode (EO_64K):** This register is programmed with the Flash 64k sector erase instruction opcode for component 1. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit.

Bit Range	Default and Access	Field Name (ID): Description
15:8	20h RW/V/L	**4k Erase Opcode (EO_4K):** This register is programmed with the Flash 4k subsector erase instruction opcode for component 1. Software must program this register if the SFDP table for this component does not show 4 kByte erase capability. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit.
7:5	0h RW/V/L	**Quad Enable Requirements (QER):** 000 = Part does not require a Quad Enable bit to be set, either because Quad is not supported or because the manufacturer somehow permanently enables Quad capability. 001 = Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to status register clears all bits in register 2, therefore status register writes MUST be two bytes. 010 = Part requires bit 6 of status register 1 to be set to enable quad IO. 011 = Part requires bit 7 of the configuration register to be set to enable Quad. 100 = Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to the status register does not clear the second byte. This register is locked by the Vendor Component Lock (VCL) bit. If the SFDP table contains this information, the flash controller loads these bits from the table. The flash controller uses this information to prevent clearing the QE bit in the flash device's status register when WSR=1.
4	0h RW/V/L	**Write Enable on Write Status (WEWS):** 0 : 50h is the opcode to enable a status register write 1 : 06h is the opcode to enable a status register write This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit.
3	0h RW/V/L	**Write Status Required (WSR):** 0: No requirement to write to the Write Status Register prior to a write 1: A write is required to the Write Status Register prior to write and erase to remove any protection. This is required for SST components. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit.
2	0h RW/V/L	**Write Granularity (WG):** 0 : Reserved 1 : 64 Byte This register is locked by the Vendor Component Lock (VCL) bit orthe CPPTV bit. Note: Hardware ignores the state of this bit.
1:0	0h RO	Reserved.

16.2.40 Parameter Table Index (BIOS_PTINX)—Offset CCh

Observability control for Component Property Tables. Note: The PTINX and PTDATA registers do not have any meaning in Target-attach flash mode because the SPI controller does not perform SFDP discovery.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:14	0h RW	**Supported Parameter Table (SPT):** Selects which supported parameter table to observe. 00 : Component 0 Property Parameter Table 01 : Component 1 Property Parameter Table 10 - 11 : Reserved
13:12	0h RW	**Header or Data (HORD):** Select parameter table header DW vs Data DW. 00 : SFDP Header 01 : Parameter Table Header 10 : Data 11 : Reserved
11:2	0h RW	**Parameter Table DW Index (PTDWI):** Selects the DW offset within the parameter table to observe.
1:0	0h RO	Reserved.

16.2.41 Parameter Table Data (BIOS_PTDATA)—Offset D0h

Parameter Table Data

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Parameter Table DW Data (PTDWD):** Returns the DW of data to observe as selected in the Parameter Table Index register. Note: The returned value of reserved fields in the SFDP header or table must be ignored by software. The flash controller may return either 0 or 1 for these fields.

16.2.42 SPI Bus Requester Status (BIOS_SBRS)—Offset D4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO/V	**TPM Access Ongoing (TPM_ACC_ONG):** Indicates that a TPM access is in progress.
30	0h RO/V	**eSPI Access Ongoing (ESPI_ACC_ONG):** This bit is only defined if eSPI and SPI are sharing the SPI bus.
29:18	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
17:15	0h RO/V	**Initiator 5 Status (M5STATUS):** Refer description under M1STATUS.
14:12	0h RO/V	**Initiator 6 Status (M6STATUS):** Refer description under M1STATUS.
11:9	0h RO/V	**Initiator 4 Status (M4STATUS):** Refer description under M1STATUS.
8:6	0h RO/V	**Initiator 3 Status (M3STATUS):** Refer description under M1STATUS.
5:3	0h RO/V	**Initiator 2 Status (M2STATUS):** Refer description under M1STATUS.
2:0	0h RO/V	**Initiator 1 Status (M1STATUS):** Indicates whether this Initiator has an outstanding transaction enqueued or in flight and the transaction type. 0xx : no transaction 100 : flash read transaction 101 : flash write transaction 110 : flash erase transaction 111 : flash RPMC transaction

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17 UART Interface (D30:F0/F1, D25:F2 and D17:F0)

17.1 UART PCI Configuration Registers

Table 17-1. Summary of UART PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device ID and Vendor ID (DEVVENDID)—Offset 0h	XXXX8086h
4h	7h	Status and Command (STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	Revision ID and Class Code (REVCLASSCODE)—Offset 8h	C8000XXh
Ch	Fh	Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch	800000h
10h	13h	Base Address (BAR)—Offset 10h	4h
14h	17h	Base Address High (BAR_HIGH)—Offset 14h	0h
18h	1Bh	Base Address 1 (BAR1)—Offset 18h	4h
1Ch	1Fh	Base Address 1 High (BAR1_HIGH)—Offset 1Ch	0h
2Ch	2Fh	Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch	0h
30h	33h	EXPANSION ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h	0h
34h	37h	Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	Interrupt Register (INTERRUPTREG)—Offset 3Ch	0h
80h	83h	Power Management Capability ID (POWERCAPID)—Offset 80h	39001h
84h	87h	Power Management Control and Status (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
94h	97h	Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG)—Offset 94h	1400010h
98h	9Bh	SW LTR update MMIO Location (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	2101h
9Ch	9Fh	Device IDLE Pointer (DEVICE_IDLE_POINTER_REG)—Offset 9Ch	24C1h
A0h	A3h	Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	F0800h
B0h	B3h	General Purpose Read Write Register1 (GEN_REGRW1)—Offset B0h	0h
B4h	B7h	General Purpose Read Write 2 (GEN_REGRW2)—Offset B4h	0h
B8h	BBh	General Purpose PCI Read Write 3 (GEN_REGRW3)—Offset B8h	0h
BCh	BFh	General Purpose Read Write 4 (GEN_REGRW4)—Offset BCh	0h
C0h	C3h	General Purpose Input (GEN_INPUT_REG)—Offset C0h	0h

17.1.1 Device ID and Vendor ID (DEVVENDID)—Offset 0h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 16
Function: 0

Default: XXXX8086h

Bit Range	Default and Access	Field Name (ID): Description
31:16	-- RO/P	**Device ID Field (DEVICEID):** This is a 16-bit value assigned to the controller. See the Device and Revision ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor ID Field (VENDORID):** Identifies the manufacturer of the device. 8086h = Intel.

17.1.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 16
Function: 0

Default: 100000h

Bit Range	Default and Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW/1C	**RMA Field (RMA):** S/W writes a '1' to this bit to clear it.
28	0h RW/1C	**RTA Field (RTA):** S/W writes a '1' to this bit to clear it.
27:21	0h RO	Reserved.
20	1h RO	**Cap List Field (CAPLIST):** Indicates that the controller contains a capabilities pointer list.
19	0h RO	**Intrerrupt Status Field (INTR_STATUS):** This bit reflects state of interrupt in the device.
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** Setting this bit disables INTx assertion. The interrupt disabled is legacy INTx# interrupt. This bit has no connection with interrupt status bit.
9	0h RO	Reserved.
8	0h RW	**SERR Enable Field (SERR_ENABLE):** Not implemented.
7:3	0h RO	Reserved.
2	0h RW	**BME Field (BME):** If this bit is 0, the controller does not generate any new upstream transaction as a Initiator.
1	0h RW	**MSE Field (MSE):** 0 = Disables memory mapped Configuration space. 1 = Enables memory mapped configuration space.
0	0h RO	Reserved.

17.1.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: C8000XXh

Bit Range	Default and Access	Field Name (ID): Description
31:8	C8000h RO	**Class Code (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	-- RO/P	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

17.1.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 800000h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	1h RO	**MultiFunction Device Field (MULFNDEV):** 0 = Single Function Device 1 = Multi Function device
22:16	0h RO	**Header Type Field (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	0h RO	**Latency Timer Field (LATTIMER):** Hardwired to 0.
7:0	0h RW/P	**Cache Line Size Field (CACHELINE_SIZE)**

17.1.5 Base Address (BAR)—Offset 10h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:12	0h RW	**Base Address Field (BASEADDR):** Provides system memory base address for the controller.
11:4	0h RO	**Size Field (SIZEINDICATOR):** Always returns 0. The size of this register depends on the size of the memory space.
3	0h RO	**Prefetchable Field (PREFETCHABLE):** 0 indicates that this BAR is not prefetchable.
2:1	2h RO	**Type Field (TYPE):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** 0 indicates this BAR is present in the memory space.

17.1.6 Base Address High (BAR_HIGH)—Offset 14h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Base Address High Field (BASEADDR_HIGH)**

17.1.7 Base Address 1 (BAR1)—Offset 18h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:12	0h RW	**Base Address Field (BASEADDR1):** This field is present if BAR1 is enabled.
11:4	0h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** 0 indicates that this BAR is not prefetchable.
2:1	2h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** 0 indicates this BAR is present in the memory space.

17.1.8 Base Address 1 High (BAR1_HIGH)—Offset 1Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Base Address High Field (BASEADDR1_HIGH)**

17.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RW/O/P	**Subsystem ID Field (SUBSYSTEMID):** The register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one subsystem from the other. This register is a Read Write Once type register.
15:0	0h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** The register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

17.1.10 EXPANSION ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

EXPANSION ROM base address register is a RO indicates support for expansion ROMs

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO	**EXPANSION ROM base address field (EXPANSION_ROM_BASE):** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

17.1.11 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Capabilities Pointer register indicates what the next capability is

Access Method

Type: CFG Register (Size: 32 bits)
Device: 16
Function: 0

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Indicates what the next capability is.

17.1.12 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: CFG Register (Size: 32 bits)
Device: 16
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**Min Gnt Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	Reserved.
11:8	0h RO	**Interrupt Pin Field (INTPIN)**
7:0	0h RW/P	**Int Line Field (INTLINE):** It is used to communicate to software, the interrupt line to which the interrupt pin is connected.

17.1.13 Power Management Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 16
Function: 0

Default: 39001h

Bit Range	Default and Access	Field Name (ID): Description
31:27	0h RO	**PME Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for for a bit indicates that the function is not capable of asserting the PME# signal while in that power state. Bit 27 = 1: PME# can be asserted from D0. Bit 30 = 1: PME# can be asserted from D3 hot. Other bits are not used.
26:19	0h RO	Reserved.
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	90h RO	**Next Cap Field (NXTCAP):** Points to the next capability structure.
7:0	1h RO	**Power Capability ID Field (POWER_CAP):** Indicates power management capability is supported.

17.1.14 Power Management Control and Status (PMECTRLSTATUS)—Offset 84h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C/P	**PME Status Field (PMESTATUS)**
14:9	0h RO	Reserved.
8	0h RW/P	**PME Enable Field (PMEENABLE):** 0 = PME message is disabled 1 = PME message is enabled.
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	0h RO	Reserved.
1:0	0h RW	**Power State Field (POWERSTATE):** This field is used both to determine the current power state and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field,the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked.

17.1.15 PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 16
Function: 0

Default: F0140009h

Bit Range	Default and Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision ID (REVID):** Revision ID of capability structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	0h RO	**Next Capability Field (NEXT_CAP):** Points to the next capability structure. This points to NULL.
7:0	9h RO	**Capability ID Field (CAPID)**

17.1.16 Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG)—Offset 94h

Extended Vendor capability register for VSEC Length revision and ID

Access Method

Type: CFG Register (Size: 32 bits)
Device: 16
Function: 0

Default: 1400010h

Bit Range	Default and Access	Field Name (ID): Description
31:20	14h RO	**Vendor Specific ID Field (VSEC_LENGTH):** Vendor Specific Extended Capability Length
19:16	0h RO	**Vendor Specific Revision Field (VSEC_REV):** Vendor specific Extended Capability revision
15:0	10h RO	**Vendor Specific Length Field (VSECID):** Vendor Specific Extended Capability ID

17.1.17 SW LTR update MMIO Location (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

Software location pointer in MMIO space as an offset specified by BAR

Access Method

Type: CFG Register (Size: 32 bits)
Device: 16
Function: 0

Default: 2101h

Bit Range	Default and Access	Field Name (ID): Description
31:4	210h RO	**SW LTR Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR BAR Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	1h RO	**SW LTR Valid Field (SW_LAT_VALID)**

17.1.18 Device IDLE Pointer (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Device IDLE pointer register giving details on Device MMIO offset location BAR NUM and D0i3 Valid Strap

Access Method

Type: CFG Register (Size: 32 bits)
Device: 16
Function: 0

Default: 24C1h

Bit Range	Default and Access	Field Name (ID): Description
31:4	24Ch RO	**D0i3 Dword Offset Field (DWORD_OFFSET):** contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR NUM Field (BAR_NUM):** Indicates that the D0i3 MMIO location is always at BAR0.
0	1h RO	**D0i3 Valid Field (VALID):** 0 = Not valid 1 = Valid

17.1.19 Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 16
Function: 0

Default: F0800h

Bit Range	Default and Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW/P	**HAE Field (HAE)**
20	0h RO	Reserved.
19	1h RW/P	**Sleep Enable Field (SLEEP_EN)**
18	1h RW/P	**D3 Hen Field (PGE):** If clear, the controller will never request a PG. If 1, then the function will power gate when idle and the DevIdle bit is set.
17	1h RW/P	**Device Idle En Field (I3_ENABLE):** If 1, then function will power gate when idle and the PMCSR[1:0] register in the function = 11 (D3).
16	1h RW/P	**PMC Request Enable Field (PMCRE):** If this bit is set to '1', the function will power gate when idle.
15:13	0h RO	Reserved.
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** This value is written by BIOS to communicate to the Driver.
9:0	0h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** This value is written by BIOS to communicate to the Driver.

17.1.20 General Purpose Read Write Register1 (GEN_REGRW1)—Offset B0h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 16
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Field (GEN_REG_RW1):** General purpose read write PCI register.

17.1.21 General Purpose Read Write 2 (GEN_REGRW2)—Offset B4h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 16
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Field (GEN_REG_RW2):** General purpose read write PCI register.

17.1.22 General Purpose PCI Read Write 3 (GEN_REGRW3)—Offset B8h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 16
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Field (GEN_REG_RW3):** General purpose read write PCI register.

17.1.23 General Purpose Read Write 4 (GEN_REGRW4)—Offset BCh

Access Method

Type: CFG Register (Size: 32 bits)
Device: 16
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Field (GEN_REG_RW4):** General purpose read write PCI register.

17.1.24 General Purpose Input (GEN_INPUT_REG)—Offset C0h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 16
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO	**General Purpose Input Field (GEN_REG_INPUT_RW):** General Purpose Input Register.

17.2 UART Memory Mapped Registers

The registers in this section are memory-mapped registers based on the BAR defined in PCH Configuration space.

Table 17-2. Summary of UART Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Receive Buffer Register (RBR)—Offset 0h	0h
0h	3h	Transmit Holding Register (THR)—Offset 0h	0h
0h	3h	Divisor Latch Low Register (DLL)—Offset 0h	0h
4h	7h	Divisor Latch High (DLH)—Offset 4h	0h
4h	7h	Interrupt Enable Register (IER)—Offset 4h	0h
8h	Bh	Interrupt Identification (IIR)—Offset 8h	1h
8h	Bh	FIFO Control (FCR)—Offset 8h	1h
Ch	Fh	Line Control Register (LCR)—Offset Ch	0h
10h	13h	Modem Control Register (MCR)—Offset 10h	0h
14h	17h	Line Status Register (LSR)—Offset 14h	60h
18h	1Bh	Modem Status Register (MSR)—Offset 18h	0h
1Ch	1Fh	Scratchpad Register (SCR)—Offset 1Ch	0h
30h	33h	Shadow Receive Buffer and Shadow Transmit Holding 0 (SRBR_STHR0)—Offset 30h	0h
70h	73h	FIFO Access Register (FAR)—Offset 70h	0h
74h	77h	Transmit FIFO Read (TFR)—Offset 74h	0h
78h	7Bh	Receive FIFO Write (RFW)—Offset 78h	0h
7Ch	7Fh	UART Status Register (USR)—Offset 7Ch	6h
80h	83h	Transmit FIFO Level (TFL)—Offset 80h	0h
84h	87h	Receive FIFO Level (RFL)—Offset 84h	0h
88h	8Bh	Software Reset (SRR)—Offset 88h	0h
8Ch	8Fh	Shadow Request to Send (SRTS)—Offset 8Ch	0h
90h	93h	Shadow Break Control (SBCR)—Offset 90h	0h
94h	97h	Shadow DMA Mode (SDMAM)—Offset 94h	0h
98h	9Bh	Shadow FIFO Enable (SFE)—Offset 98h	0h
9Ch	9Fh	Shadow RCVR Trigger (SRT)—Offset 9Ch	0h
A0h	A3h	Shadow TX Empty Trigger (STET)—Offset A0h	0h
A4h	A7h	Halt TX (HTX)—Offset A4h	0h
A8h	ABh	DMA Software Acknowledge (DMASA)—Offset A8h	0h
F4h	F7h	Component Parameter (CPR)—Offset F4h	43F32h

17.2.1 Receive Buffer Register (RBR)—Offset 0h

RBR mode is only available when LCR register, DLAB bit = 0.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RO	**rbr (rbr):** Data byte received on the serial input port in UART mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an over-run error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an over-run error occurs.

17.2.2 Transmit Holding Register (THR)—Offset 0h

THR mode is only available when LCR register, DLAB bit = 0.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h WO	**thr (thr):** Data to be transmitted on the serial output port in UART mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFOs are disabled (FCR[0] = 0) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFOs are enabled (FCR[0] = 1) and THRE is set, 64 characters of data may be written to the THR before the FIFO is full. Any attempt to write data when the FIFO is full results in the write data being lost.

17.2.3 Divisor Latch Low Register (DLL)—Offset 0h

DLL mode is only available when LCR register, DLAB bit = 1.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**dll (dll):** Lower 8 bits of a 16-bit, read/write Divisor Latch register that contains the baud rate divisor for the UART. This register may be accessed only when the DLAB bit (LCR[7]) is set. The output baud rate is equal to the serial clock frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur.

17.2.4 Divisor Latch High (DLH)—Offset 4h

DLH mode is only available when LCR register [7] (DLAB bit) = 1

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h NA	**dlh (dlh):** Upper 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may be accessed only when the DLAB bit (LCR[7]) is set. The output baud rate is equal to the serial clock frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur.

17.2.5 Interrupt Enable Register (IER)—Offset 4h

IER mode is only available when LCR register [7] (DLAB bit) = 0.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RW	**PTIME (PTIME):** THRE Interrupt Mode Enable: This is used to enable/disable the generation of THRE Interrupt. 0 = disabled 1 = enabled
6:4	0h RO	Reserved.
3	0h RW	**EDSSI (EDSSI):** Enable Modem Status Interrupt: This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0 = disabled 1 = enabled
2	0h RW	**ELSI (ELSI):** Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0 = disabled 1 = enabled
1	0h RW	**ETBEI (ETBEI):** Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0 = disabled 1 = enabled
0	0h RW	**ERBFI (ERBFI):** Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 0 = disabled 1 = enabled

17.2.6 Interrupt Identification (IIR)—Offset 8h

Note that the register can also be used as FIFO Control Register (FCR) when it is written to.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:6	0h RO	**FIFOSE (FIFOSE):** FIFOs Enabled. This is used to indicate whether the FIFOs are enabled or disabled. 00 = disabled 11 = enabled
5:4	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
3:0	1h RO	**IID (IID):** This indicates the highest priority pending interrupt which can be one of the following types: 0000 = modem status 0001 = no interrupt pending 0010 = THR empty 0100 = received data available 0110 = receiver line status 0111 = busy detect 1100 = character timeout Note: An interrupt of type 0111 (busy detect) is never indicated because the controller is compatible with UART_16550 mode. Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

17.2.7 FIFO Control (FCR)—Offset 8h

Note that the register can also be used as Interrupt Identification register (IIR)when it is read from.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:6	0h WO	**RCVR (RCVR):** This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. The following trigger levels are supported: 00 = 1 character in the FIFO 01 = FIFO ¼ full 10 = FIFO ½ full 11 = FIFO 2 less than full
5:4	0h WO	**TET (TET):** This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported: 00 = FIFO empty 01 = 2 characters in the FIFO 10 = FIFO ¼ full 11 = FIFO ½ full
3	0h RO	Reserved.
2	0h WO	**XFIFOR (XFIFOR):** This resets the control portion of the transmit FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
1	0h WO	**RFIFOR (RFIFOR):** This resets the control portion of the receive FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
0	1h WO	**FIFOE (FIFOE):** This is used to indicate whether the FIFOs are enabled or disabled. 00 = disabled 11 = enabled

17.2.8 Line Control Register (LCR)—Offset Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h NA	**Res_31_8 (Res_31_8):** Reserved
7	0h RW	**DLAB (DLAB):** This bit is used to enable reading and writing of the Divisor Latch register(DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers
6	0h RW	**Break (Break):** This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the serial out line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	0h RO	Reserved.
4	0h RW	**EPS (EPS):** Even Parity Select. If UART_16550_COMPATIBLE == NO, then writable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked. Reset Value: 0x0
3	0h RW	**PEN (PEN):** This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0 = parity disabled 1 = parity enabled
2	0h RW	**STOP (STOP):** This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0 = 1 stop bit 1 = 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit
1:0	0h RW	**DLS (DLS):** This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits

17.2.9 Modem Control Register (MCR)—Offset 10h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:6	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
5	0h RW	**AFCE (AFCE):** Auto Flow Control Enable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set. The bit is used to help for flow control using external IO pins with the pairing device. 0 = Auto Flow Control Mode disabled 1 = Auto Flow Control Mode enabled
4	0h RW	**LoopBack (LoopBack):** LoopBack Bit. This is used to put the UART into a diagnostic mode for test purposes. Data on the serial out line is held high, while serial data output is looped back to the serial in line, internally. In this mode all the interrupts are fully functional. Also, in loop back mode, the modem control input (cts_n,) are disconnected and the modem control output (rts_n) are looped back to the inputs, internally.
3:2	0h RO	Reserved.
1	0h RW	**RTS (RTS):** Request to Send. This is used to directly control the Request to Send (rts_n) output. The Request To Send output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	0h RO	Reserved.

17.2.10 Line Status Register (LSR)—Offset 14h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 60h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RW	**RFE (RFE):** Receiver FIFO Error bit. This bit is only relevant when FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. 0 = no error in RX FIFO 1 = error in RX FIFO This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO
6	1h RW	**TEMT (TEMT):** Transmitter Empty bit. If FIFOs enabled(FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
5	1h RW	**THRE (THRE):** Transmit Holding Register Empty bit. If THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If both THRE Interrupt and FIFO modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting

Bit Range	Default and Access	Field Name (ID): Description
4	0h RW	**BI (BI):** Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. It is set whenever the serial input (sin) is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.
3	0h RW	**FE (FE):** Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit(LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit(LSR[4]). 0 = no framing error 1 = framing error Reading the LSR clears the FE bit.
2	0h RW	**PE (PE):** Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0 = no parity error 1 = parity error Reading the LSR clears the PE bit.
1	0h RW	**OE (OE):** Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and anew character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0 = no overrun error 1 = overrun error Reading the LSR clears the OE bit.
0	0h RW	**DR (DR):** Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0 = no data ready 1 = data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

17.2.11 Modem Status Register (MSR)—Offset 18h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:5	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
4	0h RO	**CTS (CTS):** Clear to Send. This is used to indicate the current state of the modem control line cts_n.This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it isan indication that the modem or data set is ready to exchange data with the UART. 0 = cts_n input is de-asserted (logic 1) 1 = cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).
3:1	0h RO	Reserved.
0	0h RO	**DCTS (DCTS):** Delta Clear to Send. This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0 = no change on cts_n since last read of MSR 1 = change on cts_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS).Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs(software or otherwise), then the DCTS bit is set when the reset is removed if the cts_nsignal remains asserted.

17.2.12 Scratchpad Register (SCR)—Offset 1Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h NA	**Reserrved (Reserrved):** Reserved
7:0	0h RW	**scr (scr):** This register is for programmers to use as a temporary storage space.

17.2.13 Shadow Receive Buffer and Shadow Transmit Holding 0 (SRBR_STHR0)—Offset 30h

There are a total of 16 Shadow Receive Buffer Registers (SRBR_STHR[15:0]. The register description is the same for all of them. The other registers are at the following offsets:
SRBR_STHR1 at offset 34h
SRBR_STHR2 at offset 38h
SRBR_STHR3 at offset 3Ch
.....
SRBR_STHR14 at offset 68h
SRBR_STHR15 at offset 6Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**srbr_sthr0 (srbr_sthr0):** Used as SRBR: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the Initiator. This register contains the data byte received on the serial input port (sin) in UART mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Used as STHR: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the Initiator. This register contains data to be transmitted on the serial output port (sout) in UART mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFOs are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFOs are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.

17.2.14 FIFO Access Register (FAR)—Offset 70h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**srbr_sthr (srbr_sthr):** Writes have no effect when FIFO_ACCESS == No, always readable. This register is use to enable a FIFO access mode for testing, so that the receive FIFO can be written by the Initiator and the transmit FIFO can be read by the Initiator when FIFOs are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the Initiator and the THR to be read by the Initiator. 0 = FIFO access mode disabled 1 = FIFO access mode enabled Note, that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFOs are treated as empty. Reset Value: 0x0

17.2.15 Transmit FIFO Read (TFR)—Offset 74h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RO	**tfr (tfr):** Transmit FIFO Read. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, reading this register gives the data at the top of the transmit FIFO. Each consecutive read pops the transmit FIFO and gives the next data value that is currently at the top of the FIFO. When FIFOs are not implemented or not enabled, reading this register gives the data in the THR. Reset Value: 0x0

17.2.16 Receive FIFO Write (RFW)—Offset 78h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9	0h WO	**RFFE (RFFE):** Receive FIFO Framing Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are enabled, this bit is used to write framing error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write framing error detection information to the RBR.
8	0h WO	**RFPE (RFPE):** Receive FIFO Parity Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are enabled, this bit is used to write parity error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write parity error detection information to the RBR.
7:0	0h WO	**RFWD (RFWD):** Receive FIFO Write Data. These bits are only valid when FIFO access mode is enabled(FAR[0] is set to one). When FIFOs are enabled, the data that is written to the RFWD is pushed into the receive FIFO. Each consecutive write pushes the new data to the next write location in the receive FIFO. When FIFOs are not implemented or not enabled, the data that is written to the RFWD is pushed into the RBR.

17.2.17 UART Status Register (USR)—Offset 7Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 6h

Bit Range	Default and Access	Field Name (ID): Description
31:5	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
4	0h RO	**RFF (RFF):** Receive FIFO Full. This is used to indicate that the receive FIFO is completely full. 0 = Receive FIFO not full 1 = Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.
3	0h RO	**RFNE (RFNE):** Receive FIFO Not Empty. This is used to indicate that the receive FIFO contains one or more entries. 0 = Receive FIFO is empty 1 = Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.
2	1h RO	**TFE (TFE):** Transmit FIFO Empty. This is used to indicate that the transmit FIFO is completely empty. 0 = Transmit FIFO is not empty 1 = Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty
1	1h RO	**TFNF (TFNF):** Transmit FIFO Not Full. This is used to indicate that the transmit FIFO in not full. 0 = Transmit FIFO is full 1 = Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	0h RO	Reserved.

17.2.18 Transmit FIFO Level (TFL)—Offset 80h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4:0	0h RO	**tfl (tfl):** Transmit FIFO Level. This is indicates the number of data entries in the transmit FIFO. Reset Value: 0x0

17.2.19 Receive FIFO Level (RFL)—Offset 84h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:5	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
4:0	0h RO	**rfl (rfl):** Receive FIFO Level. This is indicates the number of data entries in the receive FIFO. Reset Value: 0x0

17.2.20 Software Reset (SRR)—Offset 88h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW	**XFR (XFR):** XMIT FIFO Reset. This is a shadow register for the XMIT FIFO Reset bit (FCR[2]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the transmit FIFO. This resets the control portion of the transmit FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
1	0h RW	**RFR (RFR):** RCVR FIFO Reset. This is a shadow register for the RCVR FIFO Reset bit (FCR[1]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the receive FIFO This resets the control portion of the receive FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
0	0h RW	**UR (UR):** UART Reset. This asynchronously resets the UART controller and synchronously removes the reset assertion.

17.2.21 Shadow Request to Send (SRTS)—Offset 8Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
0	0h RW	**srts (srts):** Shadow Request to Send. This is a shadow register for the RTS bit (MCR[1]), this can be used to remove the burden of having to performing a read-modify-write on the MCR. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the DW_apb_uart is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] = 0), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] = 1) and FIFOs enable (FCR[0] = 1), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). Note that in Loopback mode (MCR[4] = 1), the rts_n output is held inactive-high while the value of this location is internally looped back to an input. Reset Value: 0x0

17.2.22 Shadow Break Control (SBCR)—Offset 90h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**sbcb (sbcb):** Shadow Break Control Register. This is a shadow register for the Break bit (LCR[6]), this can be used to remove the burden of having to performing a read modify write on the LCR. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. When in Loopback Mode, the break condition is internally looped back to the receiver.

17.2.23 Shadow DMA Mode (SDMAM)—Offset 94h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**sdmam (sdmam):** Shadow DMA Mode. This is a shadow register for the DMA mode bit (FCR[3]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the DMA Mode bit gets updated. 0 = mode 0 1 = mode 1

17.2.24 Shadow FIFO Enable (SFE)—Offset 98h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**sfe (sfe):** Shadow FIFO Enable. This is a shadow register for the FIFO enable bit (FCR[0]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the FIFO enable bit gets updated.This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. If this bit is set to zero (disabled) after being enabled then both the XMIT and RCVR controller portion of FIFOs are reset. Reset Value: 0x0

17.2.25 Shadow RCVR Trigger (SRT)—Offset 9Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RW	**srt (srt):** Shadow RCVR Trigger. This is a shadow register for the RCVR trigger bits(FCR[7:6]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the RCVR trigger bit gets updated. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. It also determines when the dma_rx_req_n signal is asserted when DMA Mode (FCR[3]) = 1. The following trigger levels are supported: 00 = 1 character in the FIFO 01 = FIFO ¼ full 10 = FIFO ½ full 11 = FIFO 2 less than full

17.2.26 Shadow TX Empty Trigger (STET)—Offset A0h

Shadow TX Empty Trigger. This is a shadow register for the TX empty trigger bits(FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TXempty trigger bit gets updated. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RW	**stet (stet):** Shadow TX Empty Trigger: This is a shadow register for the TX empty trigger bits(FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TX empty trigger bit gets updated. 165 This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported: 00 = FIFO empty 01 = 2 characters in the FIFO 10 = FIFO ¼ full 11 = FIFO ½ full

17.2.27 Halt TX (HTX)—Offset A4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**htx (htx):** This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the Initiator when FIFOs are implemented and enabled. 0 = Halt TX disabled 1 = Halt TX enabled Note, if FIFOs are not enabled, the setting of the halt TX register has no effect on operation.

17.2.28 DMA Software Acknowledge (DMASA)—Offset A8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
0	0h WO	**dmasa (dmasa):** This register is use to perform a DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the UART should clear its request. This causes the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.

17.2.29 Component Parameter (CPR)—Offset F4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 43F32h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:16	4h RO	**FIFO_MODE (FIFO_MODE):** 0x00 = 0 0x01 = 16 0x02 = 32 to 0x80 = 2048
15:14	0h RO	Reserved.
13	1h RO	**DMA_EXTRA (DMA_EXTRA):** 0 = FALSE, 1 = TRUE
12	1h RO	**UART_ADD_ENCODED_PARAMS (UART_ADD_ENCODED_PARAMS):** 0 = FALSE, 1 = TRUE
11	1h RO	**SHADOW (SHADOW):** 0 = FALSE, 1 = TRUE
10	1h RO	**FIFO_STAT (FIFO_STAT):** 0 = FALSE, 1 = TRUE
9	1h RO	**FIFO_ACCESS (FIFO_ACCESS):** 0 = FALSE, 1 = TRUE
8	1h RO	**ADDITIONAL_FEAT (ADDITIONAL_FEAT):** 0 = FALSE, 1 = TRUE
7	0h RO	**SIR_LP_MODE (SIR_LP_MODE):** 0 = FALSE, 1 = TRUE
6	0h RO	**SIR_MODE (SIR_MODE):** 0 = FALSE, 1 = TRUE
5	1h RO	**THRE_MODE (THRE_MODE):** 0 = FALSE, 1 = TRUE
4	1h RO	**AFCE_MODE (AFCE_MODE):** 0 = FALSE, 1 = TRUE
3:2	0h RO	Reserved.
1:0	2h RO	**APB_DATA_WIDTH (APB_DATA_WIDTH):** 00 = 8 bits

17.3 UART Additional Memory Mapped Registers

Table 17-3. Summary of UART Additional Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
200h	203h	Clock Configuration (CLOCKS)—Offset 200h	0h
204h	207h	Resets (RESETS)—Offset 204h	0h
210h	213h	Active LTR (ACTIVELTR_VALUE)—Offset 210h	800h
214h	217h	Idle LTR (IDLELTR_VALUE)—Offset 214h	800h
218h	21Bh	Tx Byte Count (TX_BYTE_COUNT)—Offset 218h	0h
21Ch	21Fh	Rx Byte Count (RX_BYTE_COUNT)—Offset 21Ch	0h
228h	22Bh	SW Scratch 0 (SW_SCRATCH_0)—Offset 228h	0h
238h	23Bh	clock Gate (CLOCK_GATE)—Offset 238h	0h
240h	243h	Address Low (REMAP_ADDR_LO)—Offset 240h	0h
244h	247h	Address High (REMAP_ADDR_HI)—Offset 244h	0h
24Ch	24Fh	Device Idle Control (DEVIDLE_CONTROL)—Offset 24Ch	8h
2FCh	2FFh	Capabilities (CAPABLITIES)—Offset 2FCh	10h

17.3.1 Clock Configuration (CLOCKS)—Offset 200h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW	**clk_update (clk_update):** Update the clock divider after setting new m and n values. 0 - No clock Update 1 - Clock gets updated.
30:16	0h RW	**n_val (n_val):** This is the denominator value (N) for the M over N divider logic that creates CLK_OUT. Used to generate the input clk to the UART.
15:1	0h RW	**m_val (m_val):** The numerator value (M) for the M over N divider logic that creates the CLK_OUT. Used to generate the input clk to the UART.
0	0h RW	**clk_en (clk_en):** UART Serial Clock (output of M/N, input to UART) Clock Enable 0 – Clock disabled 1 – Clock Enabled.

17.3.2 Resets (RESETS)—Offset 204h

software reset

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW	**reset_dma (reset_dma):** Reset the DMA controller 0 = DMA controller is in reset (Reset Asserted) 1 = DMA controller is NOT at reset (Reset Released)
1:0	0h RO	Reserved.

17.3.3 Active LTR (ACTIVELTR_VALUE)—Offset 210h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 800h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**snoop_requirment (snoop_requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10 -bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	Reserved.
12:10	2h RW	**snoop_latency_scale (snoop_latency_scale):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which do not match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**snoop_value (snoop_value):** 10-bit latency value

17.3.4 Idle LTR (IDLELTR_VALUE)—Offset 214h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 800h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
15	0h RW	**snoop_requirment (snoop_requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10 -bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	Reserved.
12:10	2h RW	**snoop_latency_scale (snoop_latency_scale):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**snoop_value (snoop_value):** 10-bit latency value

17.3.5 Tx Byte Count (TX_BYTE_COUNT)—Offset 218h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	**tx_count_overflow (tx_count_overflow):** 0 = count valid 1 = count overflow/invalid
30:24	0h RO	Reserved.
23:0	0h RO	**tx_byte_count (tx_byte_count)**

17.3.6 Rx Byte Count (RX_BYTE_COUNT)—Offset 21Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	**rx_count_overflow (rx_count_overflow):** [be] 0= count valid 1= count overflow/invalid
30:24	0h RO	Reserved.
23:0	0h RO	**rx_byte_count (rx_byte_count):** rx_byte_count

17.3.7 SW Scratch 0 (SW_SCRATCH_0)—Offset 228h

The same registers are available at the following offsets:
SW SCRATCH 1: offset 22Ch
SW SCRATCH 2: offset 230h
SW SCRATCH 3: offset 234h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SW_Scratch_0 (SW_Scratch_0):** Scratch Pad Register for SW to generated Local DATA for iDMA

17.3.8 clock Gate (CLOCK_GATE)—Offset 238h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:2	0h RW	**sw_dma_clk_ctl (sw_dma_clk_ctl):** DMA clock gate cntrol bits. 00: hw clk enable 01: Reserved 10: force off 11: force on
1:0	0h RW	**sw_ip_clk_ctl (sw_ip_clk_ctl):** Clock gate cntrol bits.{br] 00: HW clk enable 01: Reserved 10: force clock off 11: force clock on

17.3.9 Address Low (REMAP_ADDR_LO)—Offset 240h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**uart_remap_addr_low (uart_remap_addr_low):** Low 32 bits of BAR address read by SW

17.3.10 Address High (REMAP_ADDR_HI)—Offset 244h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**uart_remap_addr_high (uart_remap_addr_high):** High 32 bits of BAR address read by SW

17.3.11 Device Idle Control (DEVIDLE_CONTROL)—Offset 24Ch

This register allows a device driver to enable/disable a devices entry into DevIdle. By enabling DevIdle, SW specifies that it will not touch the device without accessing this register prior to accessing any other MMIO device register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**intr_req_capable (intr_req_capable):** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0.
3	1h RW/1C	**restore_required (restore_required):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**devidle (devidle):** SW sets this bit to 1 to move the function into the DevIdle state. Writing this bit to 0 will return the function to the fully active D0 state (D0i0)
1	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
0	0h RO	**cmd_in_progress (cmd_in_progress):** HW sets this bit on a 1->0 or 0->1 transition of DEVIDLE. While set, the other bits in this register are not valid and it is unsupported for SW to write to any bit in this register. HW clears this bit upon completing the DevIdle transition command. When clear, all the other bits in the register are valid and SW may write to any bit. If Interrupt Request (IR) was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW. SW writes to this bit have no effect.

17.3.12 Capabilities (CAPABLITIES)—Offset 2FCh

capabilities register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 10h

Bit Range	Default and Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RO	**iDMA_present (iDMA_present):** 0= DMA present 1= DMA not present
7:4	1h RO	**instance_type (instance_type):** 0000 = IC2 0001 = UART 0010 = SPI 0011 – 1111 = Reserved
3:0	0h RO	**instance_number (instance_number)**

17.4 UART DMA Controller Registers

Table 17-4. Summary of UART DMA Controller Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
800h	803h	DMA Transfer Source Address Low (SAR_LO0)—Offset 800h	0h
804h	807h	DMA Transfer Source Address High (SAR_HI0)—Offset 804h	0h
808h	80Bh	DMA Transfer Destination Address Low (DAR_LO0)—Offset 808h	0h
80Ch	80Fh	DMA Transfer Destination Address High (DAR_HI0)—Offset 80Ch	0h
810h	813h	Linked List Pointer Low (LLP_LO0)—Offset 810h	0h
814h	817h	Linked List Pointer High (LLP_HI0)—Offset 814h	0h
818h	81Bh	Control Register Low (CTL_LO0)—Offset 818h	0h
81Ch	81Fh	Control Register High (CTL_HI0)—Offset 81Ch	0h
820h	823h	Source Status (SSTAT0)—Offset 820h	0h
828h	82Bh	Destination Status (DSTAT0)—Offset 828h	0h

Table 17-4. Summary of UART DMA Controller Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
830h	833h	Source Status Address Low (SSTATAR_LO0)—Offset 830h	0h
834h	837h	Source Status Address High (SSTATAR_HI0)—Offset 834h	0h
838h	83Bh	Destination Status Address Low (DSTATAR_LO0)—Offset 838h	0h
83Ch	83Fh	Destination Status Address High (DSTATAR_HI0)—Offset 83Ch	0h
840h	843h	DMA Transfer Configuration Low (CFG_LO0)—Offset 840h	203h
844h	847h	DMA Transfer Configuration High (CFG_HI0)—Offset 844h	0h
848h	84Bh	Source Gather (SGR0)—Offset 848h	0h
850h	853h	Destination Scatter (DSR0)—Offset 850h	0h
AC0h	AC3h	Raw Interrupt Status (RawTfr)—Offset AC0h	0h
AC8h	ACBh	Raw Status for Block Interrupts (RawBlock)—Offset AC8h	0h
AD0h	AD3h	Raw Status for Source Transaction Interrupts (RawSrcTran)—Offset AD0h	0h
AD8h	ADBh	Raw Status for Destination Transaction Interrupts (RawDstTran)—Offset AD8h	0h
AE0h	AE3h	Raw Status for Error Interrupts (RawErr)—Offset AE0h	0h
AE8h	AEBh	Interrupt Status (StatusTfr)—Offset AE8h	0h
AF0h	AF3h	Status for Block Interrupts (StatusBlock)—Offset AF0h	0h
AF8h	AFBh	Status for Source Transaction Interrupts (StatusSrcTran)—Offset AF8h	0h
B00h	B03h	Status for Destination Transaction Interrupts (StatusDstTran)—Offset B00h	0h
B08h	B0Bh	Status for Error Interrupts (StatusErr)—Offset B08h	0h
B10h	B13h	Mask for Transfer Interrupts (MaskTfr)—Offset B10h	0h
B18h	B1Bh	Mask for Block Interrupts (MaskBlock)—Offset B18h	0h
B20h	B23h	Mask for Source Transaction Interrupts (MaskSrcTran)—Offset B20h	0h
B28h	B2Bh	Mask for Destination Transaction Interrupts (MaskDstTran)—Offset B28h	0h
B30h	B33h	Mask for Error Interrupts (MaskErr)—Offset B30h	0h
B38h	B3Bh	Clear for Transfer Interrupts (ClearTfr)—Offset B38h	0h
B40h	B43h	Clear for Block Interrupts (ClearBlock)—Offset B40h	0h
B48h	B4Bh	Clear for Source Transaction Interrupts (ClearSrcTran)—Offset B48h	0h
B50h	B53h	Clear for Destination Transaction Interrupts (ClearDstTran)—Offset B50h	0h
B58h	B5Bh	Clear for Error Interrupts (ClearErr)—Offset B58h	0h
B60h	B63h	Combined Status register (StatusInt)—Offset B60h	0h
B98h	B9Bh	DMA Configuration (DmaCfgReg)—Offset B98h	0h
BA0h	BA3h	DMA Channel Enable (ChEnReg)—Offset BA0h	0h

17.4.1 DMA Transfer Source Address Low (SAR_LO0)—Offset 800h

NOTE: SAR_LO0 is for DMA Channel 0. The same register definition,SAR_LO1, is available for Channel 1 at address 858h.
SAR_LO0 (CH0): offset 800h
SAR_LO1 (CH1): offset 858h
The starting source address is programmed by software before the DMA channel is

enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SAR_LO (SAR_LO):** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected). 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

17.4.2 DMA Transfer Source Address High (SAR_HI0)—Offset 804h

NOTE: SAR_HI0 is for DMA Channel 0. The same register definition, SAR_HI1, is available for Channel 1 at address 85Ch.
SAR_HI0 (CH0): offset 804h
SAR_HI1 (CH1): offset 85Ch
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SAR_HI (SAR_HI):** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

17.4.3 DMA Transfer Destination Address Low (DAR_LO0)—Offset 808h

NOTE: DAR_LO0 is for DMA Channel 0. The same register definition, DAR_LO1, is available for Channel 1 at address 860h.
DAR_LO0 (CH0): offset 808h
DAR_LO1 (CH1): offset 860h
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DAR_LO (DAR_LO):** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

17.4.4 DMA Transfer Destination Address High (DAR_HI0)—Offset 80Ch

NOTE: DAR_HI0 is for DMA Channel 0. The same register definition, DAR_HI1, is available for Channel 1 at address 864h.
DAR_HI0 (CH0): offset 80Ch
DAR_HI1 (CH1): offset 864h
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DAR_HI (DAR_HI):** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

17.4.5 Linked List Pointer Low (LLP_LO0)—Offset 810h

NOTE: LLP_LO0 is for DMA Channel 0. The same register definition, LLP_LO1, is available for Channel 1 at address 868h.
LLP_LO0 (CH0): offset 810h
LLP_LO1 (CH1): offset 868h
The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**LOC (LOC):** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	Reserved.

17.4.6 Linked List Pointer High (LLP_HI0)—Offset 814h

NOTE: LLP_HI0 is for DMA Channel 0. The same register definition, LLP_HI1, is available for Channel 1 at address 86Ch.
LLP_HI0 (CH0): offset 814h

LLP_LO1 (CH1): offset 86Ch
The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**LOC (LOC):** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.

17.4.7 Control Register Low (CTL_LO0)—Offset 818h

NOTE: CTL_LO0 is for DMA Channel 0. The same register definition, CTL_LO1, is available for Channel 1 at address 870h.
LLP_HI0 (CH0): offset 818h
LLP_LO1 (CH1): offset 870h
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled. If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RW	**LLP_SRC_EN (LLP_SRC_EN):** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN (LLP_DST_EN):** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	Reserved.
21:20	0h RW	**TT_FC (TT_FC):** The following transfer types are supported. 00 = Reserved 01 = Memory to Peripheral 10 = Peripheral to Memory 11 = Reserved Flow Control is always assigned to the DMA.

Bit Range	Default and Access	Field Name (ID): Description
19	0h RO	Reserved.
18	0h RW	**DST_SCATTER_EN (DST_SCATTER_EN):** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN (SRC_GATHER_EN):** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control
16:14	0h RW	**SRC_MSIZE (SRC_MSIZE):** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. Source BURST SIZE (in DW) = (2 ^ SRC_TR_WIDTH) Table 24 Encoding for SRC_MSIZE and DST_MSIZE
13:11	0h RW	**DEST_MSIZE (DEST_MSIZE):** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination.
10	0h RW	**SINC (SINC):** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	Reserved.
8	0h RW	**DINC (DINC):** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	Reserved.
6:4	0h RW	**SRC_TR_WIDTH (SRC_TR_WIDTH):** BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations)
3:1	0h RW	**DST_TR_WIDTH (DST_TR_WIDTH):** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations)
0	0h RW	**INT_EN (INT_EN):** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

17.4.8 Control Register High (CTL_HI0)—Offset 81Ch

NOTE: CTL_HI0 is for DMA Channel 0. The same register definition, CTL_HI1, is available for Channel 1 at address 874h.
CTL_HI0 (CH0): offset 81Ch
CTL_HI1 (CH1): offset 874h
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:29	0h RW	**CH_CLASS (CH_CLASS):** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior.
28:18	0h NA	**RESERVED (RESERVED0):** Reserved
17	0h RW	**DONE (DONE):** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS (BLOCK_TS):** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register.

17.4.9 Source Status (SSTAT0)—Offset 820h

NOTE: SSTAT0 is for DMA Channel 0. The same register definition, SSTAT1, is available for Channel 1 at address 878h.
SSTAT0 (CH0): offset 820h
SSTAT1 (CH1): offset 878h
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block.
Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA Target interface.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SSTAT (SSTAT):** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA Target interface.

17.4.10 Destination Status (DSTAT0)—Offset 828h

NOTE: DSTAT0 is for DMA Channel 0. The same register definition, DSTAT1, is available for Channel 1 at address 880h.
DSTAT0 (CH0): offset 828h
DSTAT1 (CH1): offset 880h
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI.
Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA Target interface.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DSTAT (DSTAT):** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA Target interface

17.4.11 Source Status Address Low (SSTATAR_LO0)—Offset 830h

NOTE: SSTATAR_LO0 is for DMA Channel 0. The same register definition, SSTATAR_LO1, is available for Channel 1 at address 888h.
SSTATAR_LO0(CH0): offset 830h
SSTATAR_LO1(CH1): offset 888h
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR_LO (SSTATAR_LO):** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block

17.4.12 Source Status Address High (SSTATAR_HI0)—Offset 834h

NOTE: SSTATAR_HI0 is for DMA Channel 0. The same register definition, SSTATAR_HI1, is available for Channel 1 at address 88Ch.
SSTATAR_HI0(CH0): offset 834h
SSTATAR_HI1(CH1): offset 88Ch
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR_HI (SSTATAR_HI):** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block

17.4.13 Destination Status Address Low (DSTATAR_LO0)—Offset 838h

NOTE: DSTATAR_LO0 is for DMA Channel 0. The same register definition, DSTATAR_LO1, is available for Channel 1 at address 890h.
DSTATAR_LO0(CH0): offset 838h
DSTATAR_LO1(CH1): offset 890h
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR_LO (DSTATAR_LO):** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

17.4.14 Destination Status Address High (DSTATAR_HI0)—Offset 83Ch

NOTE: DSTATAR_LO0 is for DMA Channel 0. The same register definition, DSTATAR_HI1, is available for Channel 1 at address 894h.
DSTATAR_HI0(CH0): offset 83Ch
DSTATAR_HI1(CH1): offset 894h
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR_HI (DSTATAR_HI):** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

17.4.15 DMA Transfer Configuration Low (CFG_LO0)—Offset 840h

NOTE: CFG_LO0 is for DMA Channel 0. The same register definition, CFG_LO1, is available for Channel 1 at address 898h.
CFG_LO0(CH0): offset 840h
CFG_LO1(CH1): offset 898h
This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 203h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW	**RELOAD_DST (RELOAD_DST):** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated
30	0h RW	**RELOAD_SRC (RELOAD_SRC):** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
21	0h RW	**SRC_OPT_BL (SRC_OPT_BL):** Optimize Source Burst Length: 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE))
20	0h RW	**DST_OPT_BL (DST_OPT_BL):** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE))
19	0h RW	**SRC_HS_POL (SRC_HS_POL):** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL (DST_HS_POL):** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17:11	0h RO	Reserved.
10	0h RW	**CH_DRAIN (CH_DRAIN):** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1h RO	**FIFO_EMPTY (FIFO_EMPTY):** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP (CH_SUSP):** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN (SS_UPD_EN):** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0
6	0h RW	**DS_UPD_EN (DS_UPD_EN):** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN (CTL_HI_UPD_EN):** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	Reserved.
3	0h RW	**HSHAKE_NP_WR (HSHAKE_NP_WR):** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port. 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-ofblock writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR (ALL_NP_WR):** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port. 0x0 : Non-Posted Writes will only be used at end of block transfers and in HWHandshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used
1	1h RW	**SRC_BURST_ALIGN (SRC_BURST_ALIGN):** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary. 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN (DST_BURST_ALIGN):** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary. 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

17.4.16 DMA Transfer Configuration High (CFG_HI0)—Offset 844h

NOTE: CFG_HI0 is for DMA Channel 0. The same register definition, CFG_HI1, is available for Channel 1 at address 89Ch.
CFG_HI0(CH0): offset 844h
CFG_HI1(CH1): offset 89Ch

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:18	0h RW	**WR_ISSUE_THD (WR_ISSUE_THD):** Write Issue Threshold. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD (RD_ISSUE_THD):** Read Issue Threshold. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER (DST_PER):** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface.
3:0	0h RW	**SRC_PER (SRC_PER):** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface.

17.4.17 Source Gather (SGR0)—Offset 848h

NOTE: SGR0 is for DMA Channel 0. The same register definition, SGR1, is available for Channel 1 at address 8A0h.
SGR0(CH0): offset 848h
SGR1(CH1): offset 8A0h
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:20	0h RW	**SGC (SGC):** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI (SGI):** Source gather interval.

17.4.18 Destination Scatter (DSR0)—Offset 850h

NOTE: DSR0 is for DMA Channel 0. The same register definition, DSR1, is available for Channel 1 at address 8A8h.
DSR0(CH0): offset 850h
DSR1(CH1): offset 8A8h
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:20	0h RW	**DSC (DSC):** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries
19:0	0h RW	**DSI (DSI):** Destination scatter interval.

17.4.19 Raw Interrupt Status (RawTfr)—Offset AC0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Raw interrupt status for ch1 and ch0

17.4.20 Raw Status for Block Interrupts (RawBlock)—Offset AC8h

RawBlock - Raw Status for Block Interrupts Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Raw interrupt status for ch1 and ch0

17.4.21 Raw Status for Source Transaction Interrupts (RawSrcTran)—Offset AD0h

RawSrcTran - Raw Status for Source Transaction Interrupts Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Raw interrupt status for ch 1 and ch0

17.4.22 Raw Status for Destination Transaction Interrupts (RawDstTran)—Offset AD8h

RawDstTran - Raw Status for Destination Transaction Interrupts Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Raw interrupt status for ch 1 and ch0

17.4.23 Raw Status for Error Interrupts (RawErr)—Offset AE0h

RawErr - Raw Status for Error Interrupts Register Error interrupt will be asserted by the DMA in the following cases: IOSF Fabric returns an Unsuccessful Completion with UR Completion Status for a Non-Posted transaction issued by the DMA to Memory. This error occurs when an invalid address range is programed into the DMA SRC/Dest Field outside of the Host memory region on the memory side of the DMA transaction IOSF2OCP bridge will return error (triggering error interrupt from DMA) if the IOSF2OCP Bridge is programmed incorrectly. Peripheral side trasactions where invalid addressing can result in an OCP fabric error which will be translated into an Error Interupt. The SW should view this error as a serious programming error and handle it according to the specified error handling procedures for the product and OS.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Raw interrupt status for ch1 and ch0

17.4.24 Interrupt Status (StatusTfr)—Offset AE8h

Status for Transfer Interrupts Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Status for interrtup for ch 1 and ch0

17.4.25 Status for Block Interrupts (StatusBlock)—Offset AF0h

statusBlock: Status for Block Interrupts Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Status for interrtup for ch 1 and ch0

17.4.26 Status for Source Transaction Interrupts (StatusSrcTran)—Offset AF8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Status for interrtup for ch 1 and ch0

17.4.27 Status for Destination Transaction Interrupts (StatusDstTran)—Offset B00h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Status for interrtup for ch 1 and ch0

17.4.28 Status for Error Interrupts (StatusErr)—Offset B08h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Status for interrtup for ch 1 and ch0

17.4.29 Mask for Transfer Interrupts (MaskTfr)—Offset B10h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch 1 and ch0. 0 = write disabled 1 = write enabled

Bit Range	Default and Access	Field Name (ID): Description
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** Interrupt mask per ch1 and ch0 . 0-mask 1-unmask

17.4.30 Mask for Block Interrupts (MaskBlock)—Offset B18h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** Interrupt mask ch1 and ch0. 0-mask 1-unmask

17.4.31 Mask for Source Transaction Interrupts (MaskSrcTran)—Offset B20h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** Interrupt mask ch1 and ch0. 0-mask 1-unmask

17.4.32 Mask for Destination Transaction Interrupts (MaskDstTran)—Offset B28h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** Interrupt mask ch1 and ch0. 0-mask 1-unmask

17.4.33 Mask for Error Interrupts (MaskErr)—Offset B30h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0)**
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** Interrupt mask ch1 and ch0. 0-mask 1-unmask

17.4.34 Clear for Transfer Interrupts (ClearTfr)—Offset B38h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

17.4.35 Clear for Block Interrupts (ClearBlock)—Offset B40h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

17.4.36 Clear for Source Transaction Interrupts (ClearSrcTran)—Offset B48h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

17.4.37 Clear for Destination Transaction Interrupts (ClearDstTran)—Offset B50h

Clear for Destination Transaction Interrupts Register

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

17.4.38 Clear for Error Interrupts (ClearErr)—Offset B58h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

17.4.39 Combined Status register (StatusInt)—Offset B60h

The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran,StatusErr is Ored to produce a single bit for each interrupt type in the Combined Status register (StatusInt). This register is read-only

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**ERR (ERR):** OR of the contents of StatusErr register.

Bit Range	Default and Access	Field Name (ID): Description
3	0h RO	**DSTT (DSTT):** OR of the contents of StatusDst register.
2	0h RO	**SRCT (SRCT):** OR of the contents of StatusSrcTran register
1	0h RO	**BLOCK (BLOCK):** OR of the contents of StatusBlock register.
0	0h RO	**TFR (TFR):** OR of the contents of StatusTfr register.

17.4.40 DMA Configuration (DmaCfgReg)—Offset B98h

This register is used to enable the DMA, which must be done before any channel activity can begin. If the global channel enable bit is cleared while any channel is still active, then DmaCfgReg.DMA_EN still returns 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the DmaCfgReg.DMA_EN bit returns 0.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**DMA_EN (DMA_EN):** DMA Enable bit. 0 = DMA Disabled 1 = DMA Enabled

17.4.41 DMA Channel Enable (ChEnReg)—Offset BA0h

This is the DMA Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive, it can then enable an inactive channel with the required priority. All bits of this register are cleared to 0 when the global DMA channel enable bit, DmaCfgReg(0), is 0. When the global channel enable bit is 0, then a write to the ChEnReg register is ignored and a read will always read back 0. The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel write enable bit, ChEnReg.CH_EN_WE, is asserted on the same OCP write transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Channel enable write enable.
7:2	0h RO	Reserved.
1:0	0h RW	**CH_EN (CH_EN):** Enables/Disables the channel. Setting this bit enables a channel, clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel The ChEnReg.CH_EN bit is automatically cleared by hardware to disable the channel after the last OCP transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer.

17.5 UART PCR Registers

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 17-5. Summary of UART PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
220h	223h	PCI Configuration Control for UART0 (PCICFGCTR9)—Offset 220h	0h
224h	227h	PCI Configuration Control for UART1 (PCICFGCTR10)—Offset 224h	0h
228h	22Bh	PCI Configuration Control for UART2 (PCICFGCTR11)—Offset 228h	0h
22Ch	22Fh	PCI Configuration Control for UART3 (PCICFGCTR12)—Offset 22Ch	0h

17.5.1 PCI Configuration Control for UART0 (PCICFGCTR9)—Offset 220h

Controls the PCI Configuration Space

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:20	0h RW	**PCICFGCTR1 - PCI IRQ Num Field (PCI_IRQ1):** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	0h RW	**PCICFGCTR1 - ACPI IRQ Field (ACPI_IRQ1):** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	0h RW	**Interrupt Pin (IPIN1):** This register indicates the values to be used for Global Interrupts. 0 = No interrupt Pin 1 = INTA 2 = INTB 3 = INTC 4 = INTD 5 - FF: Reserved
7	0h RW	**BAR1 Disable (BAR1_DISABLE1):** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	0h RW	**PME Support (PME_SUPPORT1):** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1	0h RW	**ACPI Interrupt Enable Field (ACPI_INTR_EN1):** When set, ACPI IRQ number field (bits 19:12) will be used for IRQ messages. When 0, PCI IRQ number field (bits 27:20) will be used for IRQ message.
0	0h RW	**PCICFGCTR1 - PCI CFG Disable Field (PCI_CFG_DIS1):** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported

17.5.2 PCI Configuration Control for UART1 (PCICFGCTR10)—Offset 224h

Same definition as PCICFGCTR9.

17.5.3 PCI Configuration Control for UART2 (PCICFGCTR11)—Offset 228h

Same definition as PCICFGCTR9.

17.5.4 PCI Configuration Control for UART3 (PCICFGCTR12)—Offset 22Ch

Same definition as PCICFGCTR9.

18 Intel® Trace Hub Interface (D31:F7)

18.1 Intel® Trace Hub Configuration Registers

Table 18-1. Summary of Intel® Trace Hub Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Vendor ID (VID)—Offset 0h	XXXX8086h
4h	7h	Command (CMD)—Offset 4h	100000h
8h	Bh	Revision ID (RID)—Offset 8h	130000XXh
Ch	Fh	Header Type (HT)—Offset Ch	0h
10h	13h	Trace Buffer Lower BAR (MTB_LBAR)—Offset 10h	4h
14h	17h	Trace Buffer Upper BAR (MTB_UBAR)—Offset 14h	0h
18h	1Bh	Software Lower BAR (SW_LBAR)—Offset 18h	4h
1Ch	1Fh	Software Upper BAR (SW_UBAR)—Offset 1Ch	0h
20h	23h	RTIT Lower BAR (RTIT_LBAR)—Offset 20h	4h
24h	27h	RTIT Upper BAR (RTIT_UBAR)—Offset 24h	0h
2Ch	2Fh	Subsystem Vendor ID (SVID)—Offset 2Ch	0h
34h	37h	Capabilities Pointer (CAP)—Offset 34h	40h
3Ch	3Fh	Interrupt Line (INTL)—Offset 3Ch	1FFh
40h	43h	MSI Capability ID (MSICID)—Offset 40h	860000h
44h	47h	MSI Lower Message Address (MSILMA)—Offset 44h	0h
48h	4Bh	MSI Upper Message Address (MSIUMA)—Offset 48h	0h
4Ch	4Fh	MSI Message Data (MSIMD)—Offset 4Ch	0h
70h	73h	Firmware Lower Bar (FW_LBAR)—Offset 70h	4h
74h	77h	Firmware Upper Bar (FW_UBAR)—Offset 74h	0h
80h	83h	Device Specific Control (NPKDSC)—Offset 80h	0h
B4h	B7h	Power Control Enable Register (DEVIDLEPCE)—Offset B4h	8h

18.1.1 Vendor ID (VID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 9638086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	963h RO	**DID:** The value that uniquely identifies the Intel Trace Hub.
15:0	8086h RO	**Vendor ID (VID):** 8086 is Intel Vendor Identification code.

18.1.2 Command (CMD)—Offset 4h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 31

Function: 7

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30	0h RW/1C	**Signaled System Error (SSE):** This bit is set when the device has detected an un-correctable error and reported it via SERR message over sideband. This requires SERR Enable bit to be set in Command register.
29	0h RW/1C	**Received Initiator Abort Status (RMA):** This bit is set when device receives a Completion transaction with Unsupported Request completion status. No error will be reported.
28	0h RW/1C	**Received Target Abort Status (RTA):** This bit is set when device receives a Completion transaction with Completer Abort completion status. No error will be reported
27	0h RW/1C	**Signaled Target Abort Status (STA):** Set by the device when aborting a request that violates the device programming model. When SERR Enable is set SERR message will be send over sideband.
26:25	0h RO	Reserved.
24	0h RW/1C	**MDPE:** Initiator Data Parity Error
23:21	0h RO	Reserved.
20	1h RO	**Capabilities List (CLIST):** Indicates the controller contains a capabilities pointer list and the capability pointer register is implemented at offset 0x40 in the configuration space
19	0h RO	**Interrupt Status (INSTAT):** Reflects the state of the interrupt pin at the input of the enable/disable circuit. When the interrupt is asserted, and cleared when the interrupt is cleared (independent of the state of Interrupt Disable bit in command register. This bit is only associated with the INTx messages and has no meaning if the device is using MSI.
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (IntDis):** Disables the function to generate INTx interrupt. A value of 0 enables the function to generate INTA messages on IOSF sideband. Note: this bit has no effect on MSI generation.
9	0h RO	Reserved.
8	0h RW	**System Error Enable (SERREn):** Setting this bit enables the generation of System Error message, when required through sideband interface.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6	0h RW	**PERE:** Parity Error Response Enable
5:3	0h RO	Reserved.
2	0h RW	**Bus Initiator Enable (BME):** When set enables the ability to issue Memory or IO requests, including MSI.
1	0h RW	**Memory Space Enable (MEM):** When set, Memory Space Decoding is enabled and memory transactions targeting the device are accepted. Note: The MSE has to be set to accept any memory transaction on the primary interface targeting any of Trace Hub's BARs.
0	0h RO	Reserved.

18.1.3 Revision ID (RID)—Offset 8h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 7

Default: 13000001h

Bit Range	Default & Access	Field Name (ID): Description
31:8	130000h RO	**Class Code (Class):** Class Code
7:0	1h RO	**Revision ID (RID):** Indicates the device specific revision identifier.

18.1.4 Header Type (HT)—Offset Ch

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 7

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:16	0h RO	**Header Type (HT):** Implements a Type 0 configuration header
15:0	0h RO	Reserved.

18.1.5 Trace Buffer Lower BAR (MTB_LBAR)—Offset 10h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Lower Base Address (ADDR):** Lower programmable Base Address.
19:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PF):** Value of 0 indicates the BAR cannot be prefetched.
2:1	2h RO	**Address Range (ADRNG):** Value of 0x2 indicates that the BAR is located anywhere system memory space (i.e. 64-bit addressing)
0	0h RO	**Space Type (SPTY):** Value of 0 indicates the BAR is located in memory space.

18.1.6 Trace Buffer Upper BAR (MTB_UBAR)—Offset 14h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Upper Base Address (ADDR):** Upper programmable Base Address.

18.1.7 Software Lower BAR (SW_LBAR)—Offset 18h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RW	**Lower Base Address (ADDR):** Lower programmable Base Address.
22:4	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**Prefetchable (PF):** Value of 0 indicates the BAR cannot be prefetched.
2:1	2h RO	**Address Range (ADRNG):** Value of 0x2 indicates that the BAR is located anywhere system memory space (i.e. 64-bit addressing)
0	0h RO	**Space Type (SPTY):** Value of 0 indicates the BAR is located in memory space

18.1.8 Software Upper BAR (SW_UBAR)—Offset 1Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Upper Base Address (ADDR):** Upper programmable Base Address.

18.1.9 RTIT Lower BAR (RTIT_LBAR)—Offset 20h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RW	**Lower Base Address (ADDR):** Lower Base Address: Lower programmable Base Address
13:4	0h RO	Reserved.
3	0h RO	**PF:** Prefetchable: Value of 0 indicates the BAR cannot be prefetched
2:1	2h RO	**TYPE:** Address Range: Value of 0x2 indicates that the BAR is located anywhere system memory space (i.e. 64-bit addressing)
0	0h RO	**MEM:** Space Type: Value of 0 indicates the BAR is located in memory space

18.1.10 RTIT Upper BAR (RTIT_UBAR)—Offset 24h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Upper Base Address (ADDR):** Upper Base Address: Upper programmable Base Address

18.1.11 Subsystem Vendor ID (SVID)—Offset 2Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Subsystem ID (SID):** Writable only once
15:0	0h RW	**Subsystem Vendor ID (SVID):** Be set once by BIOS then becomes RO.

18.1.12 Capabilities Pointer (CAP)—Offset 34h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 40h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	40h RO	**Capability Pointer: (CAPPTR):** Pointer to first capability structure at 40h.

18.1.13 Interrupt Line (INTL)—Offset 3Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 1FFh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	1h RW/O	**Interrupt Pin (INTPIN):** Trace Hub uses a single INTx interrupt bonded to INTA.
7:0	FFh RW	**Interrupt Line (INTL):** Hardware does not use this field. Rather it is programmed by system software and device drivers to communicate interrupt line routing information.

18.1.14 MSI Capability ID (MSICID)—Offset 40h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 860000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	1h RO	**Multiple Message Capable (AC64b):** Value of 0 indicates the device only support single interrupt message.
22:20	0h RW	**MSI Enable (MME):** If set, MSI is enabled and the legacy interrupts messages (over IOSF sideband) will not be generated
19:17	3h RO	**MSI Next Capability Pointer (MMC):** Value of 0 indicates there are no further capabilities (i.e. the capability linked list is ended)
16	0h RW	**MSI Capability ID (MSIE):** MSI Capability ID with a value of 05h indicating the presence of the MSI capability register set
15:8	0h RO	**64-bit Address Capable (MSINCP):** Trace Hub is capable of generating 64-bit memory addresses
7:0	0h RO	Reserved.

18.1.15 MSI Lower Message Address (MSILMA)—Offset 44h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**MSI Message Lower Address (MSILMA):** Lower 32-bits of system software assigned message address to the device with bits[1:0] always cleared indicating message address has to always be DW aligned.
1:0	0h RO	Reserved.

18.1.16 MSI Upper Message Address (MSIUMA)—Offset 48h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**MSI Message Upper Address (MSIUMA):** Upper 32 bits of system software assigned message address to the device.

18.1.17 MSI Message Data (MSIMD)—Offset 4Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**MSI Message Data (MSIMD):** 16 bit message data pattern assigned by the system software to the device. When MSI is generated the actual data is 32 bit and the upper 16 bits are always 0.

18.1.18 Firmware Lower Bar (FW_LBAR)—Offset 70h

Firmware Lower Bar

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RW	**ADDR:** Lower Base Address: Lower programmable Base Address
20:4	0h RO	Reserved.
3	0h RO	**PF:** Prefetchable: Value of 0 indicates the BAR cannot be prefetched
2:1	2h RO	**TYPE:** Address Range: Value of 0x2 indicates that the BAR is located anywhere system memory space (i.e. 64-bit addressing)
0	0h RO	**MEM:** Space Type: Value of 0 indicates the BAR is located in memory space

18.1.19 Firmware Upper Bar (FW_UBAR)—Offset 74h

Firmware Upper Bar

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**UADDR:** Upper Base Address: Upper programmable Base Address

18.1.20 Device Specific Control (NPKDSC)—Offset 80h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	Reserved.
10	0h RW/1C	**Unsupported Request Detect (URD):** This bit is set when an unsupported request is detected.
9:4	0h RO	Reserved.
3	0h RW	**Unsupported Request Reporting Enable (URRE):** When set, this bit enables the reporting unsupported requests as system errors
2	0h RW/1C	**Capture Done Interrupt Status (CDINTS):** Formerly Legacy Interrupt Asserted. Equivalent to MSUSTS.MSU_INT, for software compatibility. This this bit indicates when the capture done event has occurred. Software can clear the capture done interrupt event by writing a 1 to this bit, or writing a 1 to the MSUSTS.MSU_INT bit
1	0h RW	**Software Reset: (FLR):** Writing a 1 to this bit will assert the reset signals. Reading this bit will always return a zero.
0	0h RO	Reserved.

18.1.21 Power Control Enable Register (DEVIDLEPCE)—Offset B4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	1h RW	**Sleep Enable (SE):** If clear, Trace Hub will never assert sleep. If set, it will assert sleep during power gating
2	0h RO	Reserved.
1	0h RO	**Device Idle Enable (DEVIDLEN):** It set, Trace Hub will power gate when idle and D0I3C[2] is programmed to 1h (D0I3C[2] = 0x1)
0	0h RO	Reserved.

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19 Generic SPI Interface (D30:F2/F3 and D18:F6)

19.1 GSPI PCI Configuration Registers

Table 19-1. Summary of GSPI PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device ID and Vendor ID (DEVVENDID)—Offset 0h	XXXX8086h
4h	7h	Status and Command (STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	Revision ID and Class Code (REVCLASSCODE)—Offset 8h	78000XXh
Ch	Fh	Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch	800000h
10h	13h	Base Address (BAR)—Offset 10h	4h
14h	17h	Base Address High (BAR_HIGH)—Offset 14h	0h
18h	1Bh	Base Address High (BAR1)—Offset 18h	4h
1Ch	1Fh	Base Address 1 High (BAR1_HIGH)—Offset 1Ch	0h
2Ch	2Fh	Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch	0h
30h	33h	EXPANSION ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h	0h
34h	37h	Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	Interrupt (INTERRUPTREG)—Offset 3Ch	0h
80h	83h	Power Management Capability ID (POWERCAPID)—Offset 80h	39001h
84h	87h	Power Management Control and Status (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
94h	97h	Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG)—Offset 94h	1400010h
98h	9Bh	SW LTR Update MMIO Location (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	2101h
9Ch	9Fh	Device IDLE Pointer (DEVICE_IDLE_POINTER_REG)—Offset 9Ch	24C1h
A0h	A3h	Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	F0800h
B0h	B3h	General Purpose Read Write 1 (GEN_REGRW1)—Offset B0h	0h
B4h	B7h	General Purpose Read Write 2 (GEN_REGRW2)—Offset B4h	0h
B8h	BBh	General Purpose Read Write 3 (GEN_REGRW3)—Offset B8h	0h
BCh	BFh	General Purpose Read Write 4 (GEN_REGRW4)—Offset BCh	0h
C0h	C3h	General Purpose Input (GEN_INPUT_REG)—Offset C0h	0h

19.1.1 Device ID and Vendor ID (DEVVENDID)—Offset 0h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 30
Function: 2

Default: XXXX8086h

Bit Range	Default and Access	Field Name (ID): Description
31:16	-- RO/P	**Device ID Field (DEVICEID):** This is a 16-bit value assigned to the controller. See the Device and Revision ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor ID Field (VENDORID):** Identifies the manufacturer of the device. 8086h = Intel.

19.1.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 100000h

Bit Range	Default and Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW/1C	**RMA Field (RMA):** S/W writes a '1' to this bit to clear it.
28	0h RW/1C	**RTA Field (RTA):** S/W writes a '1' to this bit to clear it.
27:21	0h RO	Reserved.
20	1h RO	**Cap List Field (CAPLIST):** Indicates that the controller contains a capabilities pointer list.
19	0h RO	**Intrerrupt Status Field (INTR_STATUS):** This bit reflects state of interrupt in the device.
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** Setting this bit disables INTx assertion. The interrupt disabled is legacy INTx# interrupt. This bit has no connection with interrupt status bit.
9	0h RO	Reserved.
8	0h RW	**SERR Enable Field (SERR_ENABLE):** Not implemented.
7:3	0h RO	Reserved.
2	0h RW	**BME Field (BME):** If this bit is 0, the controller does not generate any new upstream transaction as a Initiator.
1	0h RW	**MSE Field (MSE):** 0 = Disables memory mapped Configuration space. 1 = Enables memory mapped Configuration space.
0	0h RO	Reserved.

19.1.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 78000XXh

Bit Range	Default and Access	Field Name (ID): Description
31:8	78000h RO	**Class Code (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	-- RO/P	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

19.1.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 800000h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	1h RO	**MultiFunction Device Field (MULFNDEV):** 0 = Single Function Device 1 = Multi Function device.
22:16	0h RO	**Header Type Field (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	0h RO	**Latency Timer Field (LATTIMER):** Hardwired to 0.
7:0	0h RW/P	**Cache Line Size Field (CACHELINE_SIZE)**

19.1.5 Base Address (BAR)—Offset 10h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:12	0h RW	**Base Address Field (BASEADDR):** Provides system memory base address for the controller.
11:4	0h RO	**Size Field (SIZEINDICATOR):** Always returns 0. The size of this register depends on the size of the memory space.
3	0h RO	**Prefetchable Field (PREFETCHABLE):** 0 indicates that this BAR is not prefetchable.
2:1	2h RO	**Type Field (TYPE):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** 0 indicates this BAR is present in the memory space.

19.1.6 Base Address High (BAR_HIGH)—Offset 14h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Base Address High Field (BASEADDR_HIGH)**

19.1.7 Base Address High (BAR1)—Offset 18h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:12	0h RW	**Base Address Field (BASEADDR1):** This field is present if BAR1 is enabled.
11:4	0h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** 0 indicates that this BAR is not prefetchable.
2:1	2h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** 0 Indicates this BAR is present in the memory space.

19.1.8 Base Address 1 High (BAR1_HIGH)—Offset 1Ch

Access Method

Type: CFG Register (Size: 32 bits)
Device: 30
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Base Address High Field (BASEADDR1_HIGH)**

19.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: CFG Register (Size: 32 bits)
Device: 30
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RW/O/P	**Subsystem ID Field (SUBSYSTEMID):** The register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one subsystem from the other. This register is a Read Write Once type register.
15:0	0h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** The register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

19.1.10 EXPANSION ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

EXPANSION ROM base address register is a RO indicates support for expansion ROMs

Access Method

Type: CFG Register (Size: 32 bits)
Device: 30
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO	**EXPANSION ROM base address field (EXPANSION_ROM_BASE):** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

19.1.11 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Capabilities Pointer register indicates what the next capability is

Access Method

Type: CFG Register (Size: 32 bits)
Device: 30
Function: 2

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Indicates what the next capability is.

19.1.12 Interrupt (INTERRUPTREG)—Offset 3Ch

Access Method

Type: CFG Register (Size: 32 bits)
Device: 30
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**Min Gnt Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers // Re-Check Desc Padma
15:12	0h RO	Reserved.
11:8	0h RO	**Interrupt Pin Field (INTPIN)**
7:0	0h RW/P	**Int Line Field (INTLINE):** It is used to communicate to software, the interrupt line to which the interrupt pin is connected.

19.1.13 Power Management Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 30
Function: 2

Default: 39001h

Bit Range	Default and Access	Field Name (ID): Description
31:27	0h RO	**PME Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for for a bit indicates that the function is not capable of asserting the PME# signal while in that power state. Bit 27 = 1: PME# can be asserted from D0. Bit 30 = 1: PME# can be asserted from D3 hot. Other bits are not used.
26:19	0h RO	Reserved.
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	90h RO	**Next Cap Field (NXTCAP):** Points to the next capability structure.
7:0	1h RO	**Power Capability ID Field (POWER_CAP):** Indicates power management capability.

19.1.14 Power Management Control and Status (PMECTRLSTATUS)—Offset 84h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C/P	**PME Status Field (PMESTATUS)**
14:9	0h RO	Reserved.
8	0h RW/P	**PME Enable Field (PMEENABLE):** 0 = PME message is disabled 1 = PME message is enabled.
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	0h RO	Reserved.
1:0	0h RW	**Power State Field (POWERSTATE):** This field is used both to determine the current power state and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field,the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked.

19.1.15 PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 30
Function: 2

Default: F0140009h

Bit Range	Default and Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision IDField (REVID):** Revision ID of capability structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	0h RO	**Next Capability Field (NEXT_CAP):** Points to the next capability structure. This points to NULL.
7:0	9h RO	**Capability ID Field (CAPID)**

19.1.16 Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG)—Offset 94h

Extended Vendor capability register for VSEC Length revision and ID

Access Method

Type: CFG Register (Size: 32 bits)
Device: 30
Function: 2

Default: 1400010h

Bit Range	Default and Access	Field Name (ID): Description
31:20	14h RO	**Vendor Specific ID Field (VSEC_LENGTH):** Vendor Specific Extended Capability Length
19:16	0h RO	**Vendor Specific Revision Field (VSEC_REV):** Vendor specific Extended Capability revision
15:0	10h RO	**Vendor Specific Length Field (VSECID):** Vendor Specific Extended Capability ID

19.1.17 SW LTR Update MMIO Location (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

Software location pointer in MMIO space as an offset specified by BAR

Access Method

Type: CFG Register (Size: 32 bits)
Device: 30
Function: 2

Default: 2101h

Bit Range	Default and Access	Field Name (ID): Description
31:4	210h RO	**SW LTR Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR BAR Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	1h RO	**SW LTR Valid Field (SW_LAT_VALID)**

19.1.18 Device IDLE Pointer (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Device IDLE pointer register giving details on Device MMIO offset location BAR NUM and D0i3 Valid Strap

Access Method

Type: CFG Register (Size: 32 bits)
Device: 30
Function: 2

Default: 24C1h

Bit Range	Default and Access	Field Name (ID): Description
31:4	24Ch RO	**D0i3 Dword Offset Field (DWORD_OFFSET):** contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR NUM Field (BAR_NUM):** Indicates that the D0i3 MMIO location is always at BAR0.
0	1h RO	**D0i3 Valid Field (VALID):** 0 = Not valid 1 = Valid

19.1.19 Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 30
Function: 2

Default: F0800h

Bit Range	Default and Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW/P	**HAE Field (HAE)**
20	0h RO	Reserved.
19	1h RW/P	**Sleep Enable Field (SLEEP_EN)**
18	1h RW/P	**D3 Hen Field (PGE):** If clear, the controller will never request a PG. If 1, then the function will power gate when idle and the DevIdle bit is set.
17	1h RW/P	**Device Idle En Field (I3_ENABLE):** If 1, then function will power gate when idle and the POWERSTATE bits in the function = 11 (D3).
16	1h RW/P	**PMC Request Enable Field (PMCRE):** If this bit is set to '1', the function will power gate when idle.
15:13	0h RO	Reserved.
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** This value is written by BIOS to communicate to the Driver.
9:0	0h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** This value is written by BIOS to communicate to the Driver.

19.1.20 General Purpose Read Write 1 (GEN_REGRW1)—Offset B0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Field (GEN_REG_RW1):** General purpose read write PCI register.

19.1.21 General Purpose Read Write 2 (GEN_REGRW2)—Offset B4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Field (GEN_REG_RW2):** General purpose read write PCI register.

19.1.22 General Purpose Read Write 3 (GEN_REGRW3)—Offset B8h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 30
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Field (GEN_REG_RW3):** General purpose read write PCI register.

19.1.23 General Purpose Read Write 4 (GEN_REGRW4)—Offset BCh

Access Method

Type: CFG Register (Size: 32 bits)
Device: 30
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Field (GEN_REG_RW4):** General purpose read write PCI register.

19.1.24 General Purpose Input (GEN_INPUT_REG)—Offset C0h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 30
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO	**General Purpose Input Field (GEN_REG_INPUT_RW):** General Purpose Input Register.

19.2 Generic SPI (GSPI) Memory Mapped Registers

Table 19-2. Summary of Generic SPI (GSPI) Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	SSP (GSPI) Control Register 0 (SSCR0)—Offset 0h	0h
4h	7h	SSP (GSPI) Control Register 1 (SSCR1)—Offset 4h	0h
8h	Bh	SSP (GSPI) Status Register (SSSR)—Offset 8h	4h
10h	13h	SSP (GSPI) Data (SSDR)—Offset 10h	0h
28h	2Bh	SSP (GSPI) Time Out (SSTO)—Offset 28h	0h
44h	47h	REG SITF (SITF)—Offset 44h	0h
48h	4Bh	REG SIRF (SIRF)—Offset 48h	0h

19.2.1 SSP (GSPI) Control Register 0 (SSCR0)—Offset 0h

All bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits must be zeroes, and Read values of these bits is undetermined.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW	**MOD (MOD):** Mode Set to 0 - Normal SSP Mode : Full Duplex Serial peripheral interface. 1 = reserved
30	0h RW	**ACS (ACS):** Set to 0 for Clock selection which is determined by the NCS and ECS bits in this register. 1 = reserved
29:24	0h RO	Reserved.
23	0h RW	**TIM (TIM):** Transmit FIFO Under Run Interrupt Mask When set, this bit will mask the Transmit FIFO Under Run (TUR) event from generating an SSP interrupt. The SSSR status register will still indicate that an TUR event has occurred. This bit can be written to at any time (before or after SSP is enabled). 0 = Transmit FIFO Under Run(TUR) events will generate an SSP interrupt 1 = TUR events will be masked
22	0h RW	**RIM (RIM):** Receive FIFO Over Run Interrupt Mask When set, this bit will mask the Receive FIFO Over Run (ROR) event from generating an SSP interrupt. The SSSR status register will still indicate that an ROR event has occurred. This bit can be written to at any time (before or after SSP is enabled) 0 = receive FIFO Over Run(ROR) events will generate an SSP interrupt 1 = ROR events will be masked

Bit Range	Default and Access	Field Name (ID): Description
21	0h RW	**NCS (NCS):** Network Clock Select The SSCR0.NCS bit in conjunction with SSCR0.ECS determines which clock is used. 0 - Clock selection is determined by ECS bit 1 – Reserved
20	0h RW	**EDSS (EDSS):** Extended Data Size Select The 1-bit extended field is used in conjunction with the data size select SSCR0.DSS bits to select the size of the data transmitted and received by the Enhanced SSP. 0 = A zero is prepended to the DSS value which sets the DSS range from 4-16 bits 1 = A one is pre-appended to the DSS value which sets the DSS range from 17-32 bits
19:8	0h RW	**SCR (SCR):** Serial Clock Rate Value used to generate transmission rate of SSP. Note: The SPI Interface Controller (SSP) baud rate (or Serial bit-rate clock SPI_CLK_OUT) can be generated either by the M/N divider or internally to the SSP (SSCR0.SCR) by dividing the on-chip SSP_CLK (output of M/N) to generate baud rates.
7	0h RW	**SSE (SSE):** Synchronous Serial Port Enable The SSP enable bit, SSCR0.SSE, enables and disables all SSP operations. When SSCR0.SSE=0, the Enhanced SSP is disabled; when SSCR0.SSE=1, it is enabled. When the Enhanced SSP is disabled, all of its clocks can be stopped by programmers to minimize power consumption. On reset, the Enhanced SSP is disabled. When the SSCR0.SSE bit is cleared during active operation, the Enhanced SSP is disabled immediately, terminating the current frame being transmitted or received. Clearing SSCR0.SSE resets the Enhanced SSP FIFOs and the Enhanced SSP status bits; however, the Enhanced SSP Control registers are not reset. Note: After reset or after clearing the SSCR0.SSE, users must ensure that the SSCR1, SSITR and SSTO control registers are properly re-configured and that the SSSR register is reset before re- enabling the Enhanced SSP with the SSCR0.SSE. Also, the SSCR0.SSE bit must be cleared before reconfiguring the SSCR0, SSCR1, registers; other control bits in SSCR0 can be written at the same time as the SSCR0.SSE. When any SSP is disabled, its five pins can be used as GPIOs. 0 = SSP operation disabled 1 = SSP operation enabled.
6	0h RW	**ECS (ECS):** External Clock Select: 0 = use On-chip clock (output of M/N Divider) to produce the SSP's serial clock (SSPSCLK). Selects the use of the the output of the M/N Divider (MBAR0 + 0x800, CLOCKS) to create the SSP's serial clock (SSPCLK) Note: Setting M=N=1 will provide a pass through of the M/N Divider of the serial clock. See SCR for Serial Clock Rate generation. 1 = Reserved
5:4	0h RW	**FRF (FRF):** Frame Format Set to 00 - Serial Peripheral Interface (SPI) 01 - 10 = reserved
3:0	0h RW	**DSS (DSS):** Data Size Select With EDSS as MSB. The CPU or DMA access data through the Enhanced SSP Ports Transmit and Receive FIFOs. A CPU access takes the form of programmed I/O, transferring one FIFO entry per access. CPU accesses would normally be triggered off of an SSSR Interrupt and must always be 32 bits wide. CPU Writes to the FIFOs are 32 bits wide, but the serializing logic will ignore all bits beyond the programmed FIFO data size (EDSS/DSS value). CPU Reads to the FIFOs are also 32 bits wide, but the Receive data written into the RX FIFO (from the RXD line) is stored with zeroes in the MSBs down to the programmed data size. The FIFOs can also be accessed by DMA Single transactions, which must be 1, 2 or 4 bytes, depending upon the EDSS value, and must also transfer one FIFO entry per access. When the SSCR0.EDSS bit is set, DMA Single transactions must be 4 bytes (the DMA must have the Enhanced SSP configured as a 32-bit peripheral).The DMAs _TR.width register must be at least the SSP data size programmed into the SSP control registers EDSS and DSS. The FIFO is seen as one 32-bit location by the processor. For Writes, the Enhanced SSP port takes the data from the Transmit FIFO, serializes it, and sends it over the serial wire (SSPTXD) to the external peripheral. Receive data from the external peripheral (on SSPRXD) is converted to parallel words and stored in the Receive FIFO. A programmable FIFO trigger threshold, when exceeded, generates an Interrupt or DMA service request that, if enabled, signals the CPU or DMA respectively to empty the Receive FIFO or to refill the Transmit FIFO. The Transmit and Receive FIFOs are differentiated by whether the access is a Read or a Write transfer. Reads automatically target the Receive FIFO, while Writes will write data to the Transmit FIFO. From a memory-map perspective, they are at the same address. FIFOs are 64 samples deep by 32 bits wide. Each read or write is to 1 SSP sample. The 4-bit Data Size Select SSCR0.DSS field is used in conjunction with the extended data size select SSCR0.EDSS bit to select the size of the data transmitted and received by the Enhanced SSP. The concatenated 5-bit value of SSCR0.EDSS and SSCR0.DSS provides a data range from 4 to 32 bits in length. Note: When data is programmed to be less than 32 bits, the FIFO should be programmed right-justified. Although it is possible to program data sizes of 1, 2, and 3 bits, these sizes are reserved and produce unpredictable results in the Enhanced SSP. 0011 4 bits 0111 8 bits 1111 16, 32 bits (Note: To differentiate between 16 bits and 32 bits check the EDSS bit, for 32 bit data EDSS = 1)

19.2.2 SSP (GSPI) Control Register 1 (SSCR1)—Offset 4h

The Enhanced SSP Control 1 registers contain bit fields that control various SSP functions. Bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits should be zeroes, and Read value of these bits are undetermined.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**RWOT (RWOT):** Receive With Out Transmit 0 = Transmit/Receive mode 1 = Receive without transmit mode
22	0h RW	**TRAIL (TRAIL):** Trailing Byte 0 = Processor based, trailing bytes are handled by processor 1 - DMA based, trailing bytes are handled by DMA
21	0h RW	**TSRE (TSRE):** Transmit Service Request Enable 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
20	0h RW	**RSRE (RSRE):** Receive Service Request Enable 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
19	0h RW	**TINTE (TINTE):** Receive FIFO Time-out Interrupt Enable The SSCR1.TINTE is a read-write bit used to mask or enable the Receiver Time-out Interrupt. When SSCR1.TINTE=0, the Interrupt is masked and the state of the SSSR.TINT bit is ignored by the Interrupt controller. When SSCR1.TINTE=1, the Interrupt is enabled, and whenever the SSSR.TINT bit is set to one an Interrupt request is made to the Interrupt controller. Note that programming SSCR1.TINTE=0 does not affect the current state of the SSSR.TINT or the ability of logic to set and clear the SSSR.TINT; it only blocks the generation of the Interrupt request. 0 = Receiver Time-out interrupts are disabled 1 = Receiver Time-out interrupts are enabled
18:17	0h RO	Reserved.
16	0h RW	**IFS (IFS):** Invert Frame Signal 0 = Frame signal (Chip Select) is active low 1 = Frame signal (Chip Select) is active high
15:5	0h RO	Reserved.
4	0h RW	**SPH (SPH):** SPI SSPSCLK phase setting 0 = SSPSCLK is inactive one sycle at the start of a frame and cycle at the end of a frame 1 = SSPSCLK is inactive for one half cycle at the start of a frame and one cycle at the end of a frame
3	0h RW	**SPO (SPO):** SPI SSPSCLK polarity setting 0 = The inactive or idle state of SSPSCLK is low 1 = The inactive or idle state of SSPSCLK is high

Bit Range	Default and Access	Field Name (ID): Description
2	0h RO	Reserved.
1	0h RW	**TIE (TIE):** Transmit FIFO Interrupt Enable 0 = Transmit FIFO level interrupt is disabled 1 = Transmit FIFO level interrupt is enabled
0	0h RW	**RIE (RIE):** Receive FIFO Interrupt Enable 0 = Receive FIFO level interrupt is disabled 1 = Receive FIFO level interrupt is enabled

19.2.3 SSP (GSPI) Status Register (SSSR)—Offset 8h

The Enhanced SSP Status registers contain bits that signal overrun errors as well as the Transmit and Receive FIFO service requests. Each of these hardware-detected events signals an Interrupt request to the Interrupt controller. The Status register also contains flags that indicate when the Enhanced SSP is actively transmitting data, when the Transmit FIFO is not full, and when the Receive FIFO is not empty. One Interrupt signal is sent to the Interrupt Controller for each SSP. These events can cause an Interrupt: End-of-Chain, Receiver Time-out, Peripheral Trailing Byte, Receive FIFO overrun, Receive FIFO request, and Transmit FIFO request

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW/1C	**TUR (TUR):** Transmit FIFO Under Run 0 = Transmit FIFO has not experienced an under run 1 = Attempted read from the transmit FIFO when the FIFO was empty, request interrupt
20	0h RO	Reserved.
19	0h RW/1C	**TINT (TINT):** Receiver Time-out Interrupt 0 = No receiver time-out pending 1 = Receiver time-out pending
18	0h RW/1C	**PINT (PINT):** Peripheral Trailing Byte Interrupt 0 - No peripheral trailing byte interrupt pending 1 - Peripheral trailing byte interrupt pending
17:8	0h RO	Reserved.
7	0h RW/1C	**ROR (ROR):** Receive FIFO Overrun 0 = Receive FIFO has not experienced an overrun 1 = Attempted data write to full receive FIFO, request interrupt
6	0h RO	**RFS (RFS):** Receive FIFO Service Request 0 = Receive FIFO level is at or below RFT threshold (RFT), or SSP disabled 1 = Receive FIFO level exceeds RFT threshold (RFT), request interrupt

Bit Range	Default and Access	Field Name (ID): Description
5	0h RO	**TFS (TFS):** Transmit FIFO Service Request 0 = Transmit FIFO level exceeds the Low Water Mark Transmit FIFO (SITF.LWMTF), or SSP disabled 1 = Transmit FIFO level is at or below the Low Water Mark Transmit FIFO (SITF.LWMTF), request interrupt
4	0h RO	**BSY (BSY):** SSP Busy 0 = SSP is idle or disabled 1 = SSP currently transmitting or receiving a frame
3	0h RO	**RNE (RNE):** Receive FIOF Not Empty 0 = Receive FIFO is empty 1 = Receive FIFO is not empty
2	1h RO	**TNF (TNF):** Transmit FIFO Not Full 0 = Transmit FIFO is full 1 = Transmit FIFO is not full
1:0	0h RO	Reserved.

19.2.4 SSP (GSPI) Data (SSDR)—Offset 10h

The Enhanced SSP Data registers are single address locations that Read-Write data transfers can access.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DATA (DATA):** Data word to be written to/read from transmit/receive FIFO

19.2.5 SSP (GSPI) Time Out (SSTO)—Offset 28h

The Enhanced SSP Time-Out registers have single bit fields that specify the time-out value used to signal a period of inactivity within the Receive FIFO. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:0	0h RW	**TIMEOUT (TIMEOUT):** Timeout Value Is the value that defines the timeout interval for the rcv FIFO. The Interval is given by TIMEOUT/Parallel (Bus) Clock Frequency. When the number of samples in the Receive FIFO is less than rcv FIFO trigger threshold level, and no additional data is received, the Timeout timer will decrement. The time-out timer is reset after a new sample is received. In DMA Mode of operation this value needs to be set when the Rcv FIFO Trigger Threshold is greater than 1 Rcv FIFO Entry (the required MSize (Single Burst) for SSP DMA peripheral transfers) When in PIO mode of operation this value needs to be set when the total transfer size is not a even divison of the Rcv FIFO trigger threshold level. Is such a case the TIMEOUT value is calculated to be greater than the time to transfer the FIFO Entry size at the desired Bit Rate.

19.2.6 REG SITF (SITF)—Offset 44h

The SPI Transmit FIFO register is for writing the water mark for the SPI transmit FIFO and also for reading the number of entries in the SPI transmit FIFO

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21:16	0h RO	**SITFL (SITFL):** SPI Transmit FIFO Level Number of entries in SPI Transmit FIFO.
15:14	0h RO	Reserved.
13:8	0h RW	**LWMTF (LWMTF):** Low Water Mark Transmit FIFO. Set the low water mark of the SPI transmit FIFO. 6'b000000 = 1 entry through 6'b111111 = 64 entries
7:6	0h RO	Reserved.
5:0	0h RW	**HWMTF (HWMTF):** High Water Mark Transmit FIFO. Set the high water mark of the SPI transmit FIFO. 6'b000000 = 1 entry through 6'b111111 = 64 entries

19.2.7 REG SIRF (SIRF)—Offset 48h

The SPI Receive FIFO register is for writing the water mark for the SPI receive FIFO and also for reading the number of entries in the SPI receive FIFO

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:8	0h RO	**SIRFL (SIRFL):** SPI Receive FIFO Level Number of entries in SPI Receive FIFO.
7:6	0h RO	Reserved.
5:0	0h RW	**WMRF (WMRF):** Water Mark Receive FIFO. Set the water mark of the SPI receive FIFO. 6'b000000 = 1 entry through 6'b111111 = 64 entries

19.3 Generic SPI (GSPI) Additional Registers

The registers in this section are memory mapped based on the BAR defined in PCI configuration space.

Table 19-3. Summary of Generic SPI (GSPI) Additional Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
200h	203h	Clocks (CLOCKS)—Offset 200h	0h
204h	207h	Resets (RESETS)—Offset 204h	0h
210h	213h	Active LTR (ACTIVELTR_VALUE)—Offset 210h	800h
214h	217h	Idle LTR Value (IDLELTR_VALUE)—Offset 214h	800h
218h	21Bh	TX Bit Count (TX_BIT_COUNT)—Offset 218h	0h
21Ch	21Fh	Rx Bit Count (RX_BIT_COUNT)—Offset 21Ch	0h
220h	223h	REG SSP_REG (SSP_REG)—Offset 220h	0h
224h	227h	GSPI CS Control (SPI_CS_CONTROL)—Offset 224h	3000h
228h	22Bh	SW Scratch 0 (SW_SCRATCH)—Offset 228h	0h
22Ch	22Fh	SW Scratch 1 (SW_SCRATCH_1)—Offset 22Ch	0h
230h	233h	SW Scratch 2 (SW_SCRATCH_2)—Offset 230h	0h
234h	237h	SW Scratch 3 (SW_SCRATCH_3)—Offset 234h	0h
238h	23Bh	Clock Gate (CLOCK_GATE)—Offset 238h	0h
240h	243h	Remap Address Low (REMAP_ADDR_LO)—Offset 240h	0h
244h	247h	Remap Address High (REMAP_ADDR_HI)—Offset 244h	0h
24Ch	24Fh	Device Idle Control (DEVIDLE_CONTROL)—Offset 24Ch	8h
250h	253h	Delay Rx Clock (DEL_RX_CLK)—Offset 250h	0h
2FCh	2FFh	Capabilities (CAPABLITIES)—Offset 2FCh	620h

19.3.1 Clocks (CLOCKS)—Offset 200h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW	**Clock Update (clk_update):** Update the clock divider after seeing new m and n values 0 = No clock Update. 1 – Clock gets updated.
30:16	0h RW	**N Value (n_val):** This is the denominator value (N) for the M over N divider logic that creates the SPI_ CLK_OUT for the SSP.Used to generate the input clk to SSP.
15:1	0h RW	**M Value (m_val):** The numerator value (M) for the M over N divider logic that creates the SPI_CLK_OUT for the SSP.Used to generate the input clk to SSP.
0	0h RW	**Clock Enable (clk_en):** Clock Enable of the m over n divider 0 = Clock disabled 1 = Clock Enabled.

19.3.2 Resets (RESETS)—Offset 204h

software reset

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW	**DMA Reset (reset_dma):** DMA Software Reset Control 0 = DMA is in reset (Reset Asserted) 1 = DMA is NOT at reset (Reset Released)
1:0	0h RW	**Controller Reset (reset_ip):** Used to reset the GSPI Host Controller by SW control. All GSPI Configuration State and Operational State will be forced to the Default state. There is no timing requirement (SW can assert and de-assert in back to back transactions. Driver should re-initialize registers related to Driver context following a controller reset. 00 = Host Controller is in reset 01 = Reserved 10 = Reserved 11 = Host Controller is NOT at reset.

19.3.3 Active LTR (ACTIVELTR_VALUE)—Offset 210h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 800h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**Snoop Requirement (snoop_requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	Reserved.
12:10	2h RW	**Snoop Latency Scale (snoop_latency_scale):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**Snoop Value (snoop_value):** 10-bit latency value

19.3.4 Idle LTR Value (IDLELTR_VALUE)—Offset 214h

IdleLTR_Register

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 800h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**Snoop Requirement (snoop_requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10 -bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	Reserved.
12:10	2h RW	**Snoop Latency Scale (snoop_latency_scale):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**Snoop Value (snoop_value):** 10-bit latency value

19.3.5 TX Bit Count (TX_BIT_COUNT)—Offset 218h

TX_BIT_COUNT_Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	**Tx Count Overflow (tx_count_overflow):** 0 = Count valid 1 = count overflow/invalid
30:24	0h RO	Reserved.
23:0	0h RO	**Tx Bit Count (tx_bit_count):** 24-bit up-counter which counts the number of TX bits on the Serial bus. The counter is forced to be cleared by software Read

19.3.6 Rx Bit Count (RX_BIT_COUNT)—Offset 21Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	**Rx Count Overflow (rx_count_overflow):** 0 = count valid 1 = count overflow/invalid
30:24	0h RO	Reserved.
23:0	0h RO	**Rx Bit Count (rx_bit_count):** 24-bit up-counter which counts the number of RX Bits on the Serial bus. The counter is forced to be cleared by software Read

19.3.7 REG SSP_REG (SSP_REG)—Offset 220h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**Disable DMA Finish (disable_ssp_dma_finish):** This bit needs to be set to 1 if GSPI is using DMA multi-Block Chaining and the SW driver does not plan to re-enable the DMA manually after every Link List completion 1 = DMA finish Disabled Note: Required for multi-block transfer 0 – DMA finish not disabled.

19.3.8 GSPI CS Control (SPI_CS_CONTROL)—Offset 224h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 3000h

Bit Range	Default and Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	1h RW	**CS1 Polarity (cs1_polarity):** This Bit selects the Inactive/Idle polarity of SPI CS1 Signal. 0 = low 1 = high ***Note:*** When program the CS polarity existing S0ix, the CS may not be toggling unless dynamic clock gating is disabled or SSE bit in SSP Control register is set
12	1h RW	**CS0 Polarity (cs0_polarity):** This Bit selects the Inactive/Idle polarity of SPI CS0 Signal. 0 = Low 1 = High ***Note:*** When program the CS polarity existing S0ix, the CS may not be toggling unless dynamic clock gating is disabled or SSE bit in SSP Control register is set
11:10	0h RO	Reserved.
9:8	0h RW	**Chip Select 1 Output Select (cs1_output_sel):** These Bits select which GSPI CS Signal is to be driven by the SSP Frame (CS). 00 = GSPI CS0 01 = GSPI CS1, if applicable 10 = GSPI CS2, if applicable 11= GSPI CS3, if applicable
7:2	0h RO	Reserved.
1	0h RW	**Chip Select State (cs_state):** Manual SW control of SPI Chip Select (CS) 0 = CS is set to low 1 = CS is set to high
0	0h RW	**Chip Select Mode (cs_mode):** GSPI Chip Select Mode. 0 = HW Mode- CS is under HW control 1 = SW Mode – CS is under SW Control using cs_state bit

19.3.9 SW Scratch 0 (SW_SCRATCH)—Offset 228h

NOTE: The same registers are available at the following offsets:
SW SCRATCH 1: offset 22Ch
SW SCRATCH 2: offset 230h
SW SCRATCH 3: offset 234h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Scratch 0 (reg_SW_Scratch_0):** Scratch Pad Register for SW to generate Local DATA for DMA.

19.3.10 SW Scratch 1 (SW_SCRATCH_1)—Offset 22Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Scratch 1 (reg_SW_Scratch_1):** Scratch Pad Register for SW to generated Local DATA for iDMA

19.3.11 SW Scratch 2 (SW_SCRATCH_2)—Offset 230h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Scratch 2 (reg_SW_Scratch_2):** Scratch Pad Register for SW to generate Local DATA for DMA.

19.3.12 SW Scratch 3 (SW_SCRATCH_3)—Offset 234h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Scratch 3 (reg_SW_Scratch_3):** Scratch Pad Register for SW to generate Local DATA for DMA.

19.3.13 Clock Gate (CLOCK_GATE)—Offset 238h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:2	0h RW	**DMA Clock Control (sw_dma_clk_ctl):** DMA Clock Control 00 = Dyanamic Clock Gate Enable 01 = Reserved 10 = Force DMA Clock off 11 = Force DMA Clock on
1:0	0h RW	**Clock Control (sw_ip_clk_ctl):** Clock Control 00 = Dynamic Clock Gate Enable 01 = Reserved 10 = Force Clocks off 11 = Force Clocks on

19.3.14 Remap Address Low (REMAP_ADDR_LO)—Offset 240h

REMAP_ADDR_LO_Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Remap Address Low (spi_remap_addr_low):** Low 32 bits of BAR address read by SW

19.3.15 Remap Address High (REMAP_ADDR_HI)—Offset 244h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Remap address High (spi_remap_addr_high):** High 32 bits of BAR address read by SW

19.3.16 Device Idle Control (DEVIDLE_CONTROL)—Offset 24Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**Interrupt Request Capable (intr_req_capable):** Set to '1' by HW if it is capable of generating an interrupt on command completion, else '0'.
3	1h RW/1C	**Restore Required (restore_required):** When set (by HW), SW must restore state to the controller. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a '1'. This bit will be set on initial power up.
2	0h RW	**Device Idle (devidle):** SW sets this bit to '1' to move the function into the DevIdle state. Writing this bit to '0' will return the function to the fully active D0 state (D0i0).
1	0h RO	Reserved.
0	0h RO	**Command In Progress (cmd_in_progress):** HW sets this bit on a 1->0 or 0->1 transition of DEVIDLE. While set, the other bits in this register are not valid and it is unsupported for SW to write to any bit in this register. HW clears this bit upon completing the DevIdle transition command. When clear, all the other bits in the register are valid and SW may write to any bit. If Interrupt Request (IR) was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW. SW writes to this bit have no effect.

19.3.17 Delay Rx Clock (DEL_RX_CLK)—Offset 250h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RW	**Rx Clock Select (RX_CLK_SEL):** 00 = The output of the internal (M/N and/or baud rate) clock divider is used as-is to clock in the receive data to the RxFIFO. 01 = An internally delayed version of the internal clock divider output is used to clock in the receive data to the RxFIFO. This allows some additional setup time on the PCH side. 10 = The receive data is clocked on the subsequent negedge of the Tx clock, allowing a full cycle propagation delay on the platform. 11: The receive data is clocked on the subsequent negedge of the delayed Rx clock, maximizing the amount of delay allowed for capturing the receive data. Note: This capability is only supported for default SSP configuration with active high clocks (SSCR1.SPO = 0 and SSCR1.SPH = 0). Other combinations of SPO and SPH setting are not supported for non-zero settings of this field.

19.3.18 Capabilities (CAPABLITIES)—Offset 2FCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 620h

Bit Range	Default and Access	Field Name (ID): Description
31:11	0h RO	Reserved.
10	1h RO	**SPI CS1 Support (spi_cs1_oe_stat):** 0 = Not Supported; 1 = Supported
9	1h RO	**SPI CS0 Support (spi_cs0_oe_stat):** 0 = Not Supported; 1 = Supported
8	0h RO	**DMA Present (iDMA_present):** 0= DMA present 1= DMA not present
7:4	2h RO	**Instance Type (instance_type):** 0000 = I2C 0001 = UART 0010 = GSPI 0011 – 1111 = Reserved
3:0	0h RO	**Instance Number (instance_number):** 0h: SPI0 1h: SPI1

19.4 GSPI DMA Controller Registers

The registers in this section are memory mapped based on the BAR defined in PCI configuration space.

Table 19-4. Summary of GSPI DMA Controller Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
800h	803h	DMA Transfer Source Address Low (SAR_LO0)—Offset 800h	0h
804h	807h	DMA Transfer Source Address High (SAR_HI0)—Offset 804h	0h
808h	80Bh	DMA Transfer Destination Address Low (DAR_LO0)—Offset 808h	0h
80Ch	80Fh	DMA Transfer Destination Address High (DAR_HI0)—Offset 80Ch	0h
810h	813h	Linked List Pointer Low (LLP_LO0)—Offset 810h	0h
814h	817h	Linked List Pointer High (LLP_HI0)—Offset 814h	0h
818h	81Bh	Control Register Low (CTL_LO0)—Offset 818h	0h
81Ch	81Fh	Control Register High (CTL_HI0)—Offset 81Ch	0h
820h	823h	Source Status (SSTAT0)—Offset 820h	0h
828h	82Bh	Destination Status (DSTAT0)—Offset 828h	0h
830h	833h	Source Status Address Low (SSTATAR_LO0)—Offset 830h	0h
834h	837h	Source Status Address High (SSTATAR_HI0)—Offset 834h	0h
838h	83Bh	Destination Status Address Low (DSTATAR_LO0)—Offset 838h	0h
83Ch	83Fh	Destination Status Address High (DSTATAR_HI0)—Offset 83Ch	0h
840h	843h	DMA Transfer Configuration Low (CFG_LO0)—Offset 840h	203h
844h	847h	DMA Transfer Configuration High (CFG_HI0)—Offset 844h	0h
848h	84Bh	Source Gather (SGR0)—Offset 848h	0h
850h	853h	Destination Scatter (DSR0)—Offset 850h	0h
858h	85Bh	DMA Transfer Source Address Low (SAR_LO1)—Offset 858h	0h
85Ch	85Fh	DMA Transfer Source Address High (SAR_HI1)—Offset 85Ch	0h
860h	863h	DMA Transfer Destination Address Low (DAR_LO1)—Offset 860h	0h
864h	867h	DMA Transfer Destination Address High (DAR_HI1)—Offset 864h	0h
868h	86Bh	Linked List Pointer Low (LLP_LO1)—Offset 868h	0h
86Ch	86Fh	Linked List Pointer High (LLP_HI1)—Offset 86Ch	0h
870h	873h	Control Register Low 1 (CTL_LO1)—Offset 870h	0h
874h	877h	Control Register High 1 (CTL_HI1)—Offset 874h	0h
878h	87Bh	Source Status 1 (SSTAT1)—Offset 878h	0h
880h	883h	Destination Status 1 (DSTAT1)—Offset 880h	0h
888h	88Bh	Source Status Address Low (SSTATAR_LO1)—Offset 888h	0h
88Ch	88Fh	Source Status Address High (SSTATAR_HI1)—Offset 88Ch	0h
890h	893h	Destination Status Address Low (DSTATAR_LO1)—Offset 890h	0h
894h	897h	Destination Status Address High (DSTATAR_HI1)—Offset 894h	0h
898h	89Bh	DMA Transfer Configuration Low (CFG_LO1)—Offset 898h	0h
89Ch	89Fh	DMA Transfer Configuration High 1 (CFG_HI1)—Offset 89Ch	0h
8A0h	8A3h	Source Gather 1 (SGR1)—Offset 8A0h	0h
8A8h	8ABh	Destination Scatter 1 (DSR1)—Offset 8A8h	0h
AC0h	AC3h	Raw Interrupt Status (RawTfr)—Offset AC0h	0h
AC8h	ACBh	Raw Status for Block Interrupts (RawBlock)—Offset AC8h	0h
AD0h	AD3h	Raw Status for Source Transaction Interrupts (RawSrcTran)—Offset AD0h	0h

Table 19-4. Summary of GSPI DMA Controller Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
AD8h	ADBh	Raw Status for Destination Transaction Interrupts (RawDstTran)—Offset AD8h	0h
AE0h	AE3h	Raw Status for Error Interrupts (RawErr)—Offset AE0h	0h
AE8h	AEBh	Interrupt Status (StatusTfr)—Offset AE8h	0h
AF0h	AF3h	Status for Block Interrupts (StatusBlock)—Offset AF0h	0h
AF8h	AFBh	Status for Source Transaction Interrupts (StatusSrcTran)—Offset AF8h	0h
B00h	B03h	Status for Destination Transaction Interrupts (StatusDstTran)—Offset B00h	0h
B08h	B0Bh	Status for Error Interrupts (StatusErr)—Offset B08h	0h
B10h	B13h	Mask for Transfer Interrupts (MaskTfr)—Offset B10h	0h
B18h	B1Bh	Mask for Block Interrupts (MaskBlock)—Offset B18h	0h
B20h	B23h	Mask for Source Transaction Interrupts (MaskSrcTran)—Offset B20h	0h
B28h	B2Bh	Mask for Destination Transaction Interrupts (MaskDstTran)—Offset B28h	0h
B30h	B33h	Mask for Error Interrupts (MaskErr)—Offset B30h	0h
B38h	B3Bh	Clear for Transfer Interrupts (ClearTfr)—Offset B38h	0h
B40h	B43h	Clear for Block Interrupts (ClearBlock)—Offset B40h	0h
B48h	B4Bh	Clear for Source Transaction Interrupts (ClearSrcTran)—Offset B48h	0h
B50h	B53h	Clear for Destination Transaction Interrupts (ClearDstTran)—Offset B50h	0h
B58h	B5Bh	Clear for Error Interrupts (ClearErr)—Offset B58h	0h
B60h	B63h	Combined Status register (StatusInt)—Offset B60h	0h
B98h	B9Bh	DMA Configuration (DmaCfgReg)—Offset B98h	0h
BA0h	BA3h	DMA Channel Enable (ChEnReg)—Offset BA0h	0h

19.4.1 DMA Transfer Source Address Low (SAR_LO0)—Offset 800h

NOTE: SAR_LO0 is for DMA Channel 0. The same register definition,SAR_LO1, is available for Channel 1 at address 858h.
SAR_LO0 (CH0): offset 800h
SAR_LO1 (CH1): offset 858h
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SAR_LO (SAR_LO):** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

19.4.2 DMA Transfer Source Address High (SAR_HI0)—Offset 804h

NOTE: SAR_HI0 is for DMA Channel 0. The same register definition, SAR_HI1, is available for Channel 1 at address 85Ch.
SAR_HI0 (CH0): offset 804h
SAR_HI1 (CH1): offset 85Ch
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SAR_HI (SAR_HI):** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

19.4.3 DMA Transfer Destination Address Low (DAR_LO0)—Offset 808h

NOTE: DAR_LO0 is for DMA Channel 0. The same register definition, DAR_LO1, is available for Channel 1 at address 860h.
DAR_LO0 (CH0): offset 808h
DAR_LO1 (CH1): offset 860h
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DAR_LO (DAR_LO):** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

19.4.4 DMA Transfer Destination Address High (DAR_HI0)—Offset 80Ch

NOTE: DAR_HI0 is for DMA Channel 0. The same register definition, DAR_HI1, is available for Channel 1 at address 864h.
DAR_HI0 (CH0): offset 80Ch
DAR_HI1 (CH1): offset 864h
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DAR_HI (DAR_HI):** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

19.4.5 Linked List Pointer Low (LLP_LO0)—Offset 810h

NOTE: LLP_LO0 is for DMA Channel 0. The same register definition, LLP_LO1, is available for Channel 1 at address 868h.
LLP_LO0 (CH0): offset 810h
LLP_LO1 (CH1): offset 868h
The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**LOC (LOC):** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	Reserved.

19.4.6 Linked List Pointer High (LLP_HI0)—Offset 814h

NOTE: LLP_HI0 is for DMA Channel 0. The same register definition, LLP_HI1, is available for Channel 1 at address 86Ch.
LLP_HI0 (CH0): offset 814h
LLP_LO1 (CH1): offset 86Ch
The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

19.4.7 Control Register Low (CTL_LO0)—Offset 818h

NOTE: CTL_LO0 is for DMA Channel 0. The same register definition, CTL_LO1, is available for Channel 1 at address 870h.
LLP_HI0 (CH0): offset 818h
LLP_LO1 (CH1): offset 870h
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled. If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RW	**LLP_SRC_EN (LLP_SRC_EN):** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN (LLP_DST_EN):** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	Reserved.
21:20	0h RW	**TT_FC (TT_FC):** The following transfer types are supported. 00: Reserved 01: Memory to Peripheral 10: Peripheral to Memory 11: Peripheral to Peripheral Flow Control is always assigned to the DMA.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	Reserved.
18	0h RW	**DST_SCATTER_EN (DST_SCATTER_EN):** 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN (SRC_GATHER_EN):** 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE (SRC_MSIZE):** Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source.
13:11	0h RW	**DEST_MSIZE (DEST_MSIZE):** Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination.
10	0h RW	**SINC (SINC):** Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	Reserved.
8	0h RW	**DINC (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. If the device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	Reserved.
6:4	0h RW	**SRC_TR_WIDTH (SRC_TR_WIDTH):** BURST_SIZE (IN DW) = (2^ MSIZE) (i.e. 2 to-the-power-of MSIZE) 1.Transferred Bytes Per Burst = BURST_SIZE * (2 ^ TR_WIDTH) Since Max Burst Length is limited to 16 DW, encodings 101 (32 DW), 110 (64 DW) and 111 (128 DW) are not supported. 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported.
3:1	0h RW	**DST_TR_WIDTH (DST_TR_WIDTH):** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations)
0	0h RW	**INT_EN (INT_EN):** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

19.4.8 Control Register High (CTL_HI0)—Offset 81Ch

NOTE: CTL_HI0 is for DMA Channel 0. The same register definition, CTL_HI1, is available for Channel 1 at address 874h.
CTL_HI0 (CH0): offset 81Ch
CTL_HI1 (CH1): offset 874h
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**CH_CLASS (CH_CLASS):** A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior.
28:18	0h NA	**RESERVED (RESERVED0):** Reserved
17	0h RW	**DONE (DONE):** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS (BLOCK_TS):** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register.

19.4.9 Source Status (SSTAT0)—Offset 820h

NOTE: SSTAT0 is for DMA Channel 0. The same register definition, SSTAT1, is available for Channel 1 at address 878h.
SSTAT0 (CH0): offset 820h
SSTAT1 (CH1): offset 878h
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block.
Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA Target interface.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTAT (SSTAT):** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA Target interface.

19.4.10 Destination Status (DSTAT0)—Offset 828h

NOTE: DSTAT0 is for DMA Channel 0. The same register definition, DSTAT1, is available for Channel 1 at address 880h.
DSTAT0 (CH0): offset 828h
DSTAT1 (CH1): offset 880h
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI.
Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA Target interface.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTAT (DSTAT):** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA Target interface

19.4.11 Source Status Address Low (SSTATAR_LO0)—Offset 830h

NOTE: SSTATAR_LO0 is for DMA Channel 0. The same register definition, SSTATAR_LO1, is available for Channel 1 at address 888h.
SSTATAR_LO0(CH0): offset 830h
SSTATAR_LO1(CH1): offset 888h
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR_LO (SSTATAR_LO):** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block

19.4.12 Source Status Address High (SSTATAR_HI0)—Offset 834h

NOTE: SSTATAR_HI0 is for DMA Channel 0. The same register definition, SSTATAR_HI1, is available for Channel 1 at address 88Ch.
SSTATAR_HI0(CH0): offset 834h
SSTATAR_HI1(CH1): offset 88Ch
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR_HI (SSTATAR_HI):** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block

19.4.13 Destination Status Address Low (DSTATAR_LO0)—Offset 838h

NOTE: DSTATAR_LO0 is for DMA Channel 0. The same register definition, DSTATAR_LO1, is available for Channel 1 at address 890h.
DSTATAR_LO0(CH0): offset 838h
DSTATAR_LO1(CH1): offset 890h
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR_LO (DSTATAR_LO):** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

19.4.14 Destination Status Address High (DSTATAR_HI0)—Offset 83Ch

NOTE: DSTATAR_HI0 is for DMA Channel 0. The same register definition, DSTATAR_HI1, is available for Channel 1 at address 894h.
DSTATAR_HI0(CH0): offset 83Ch
DSTATAR_HI1(CH1): offset 894h
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR_HI (DSTATAR_HI):** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

19.4.15 DMA Transfer Configuration Low (CFG_LO0)—Offset 840h

NOTE: CFG_LO0 is for DMA Channel 0. The same register definition, CFG_LO1, is available for Channel 1 at address 898h.
CFG_LO0(CH0): offset 840h
CFG_LO1(CH1): offset 898h
This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 203h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RELOAD_DST (RELOAD_DST):** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated
30	0h RW	**RELOAD_SRC (RELOAD_SRC):** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**SRC_OPT_BL (SRC_OPT_BL):** Optimize Source Burst Length: 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ SRC_MSIZE)) This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL (DST_OPT_BL):** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ DST_MSIZE)) This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL (SRC_HS_POL):** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL (DST_HS_POL):** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17:11	0h RO	Reserved.
10	0h RW	**CH_DRAIN (CH_DRAIN):** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1h RO	**FIFO_EMPTY (FIFO_EMPTY):** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP (CH_SUSP):** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN (SS_UPD_EN):** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0
6	0h RW	**DS_UPD_EN (DS_UPD_EN):** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN (CTL_HI_UPD_EN):** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	Reserved.
3	0h RW	**HSHAKE_NP_WR (HSHAKE_NP_WR):** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR (ALL_NP_WR):** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN (SRC_BURST_ALIGN):** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN (DST_BURST_ALIGN):** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary.

19.4.16 DMA Transfer Configuration High (CFG_HI0)—Offset 844h

NOTE: CFG_HI0 is for DMA Channel 0. The same register definition, CFG_HI1, is available for Channel 1 at address 89Ch.
CFG_HI0(CH0): offset 844h
CFG_HI1(CH1): offset 89Ch

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:18	0h RW	**WR_ISSUE_THD (WR_ISSUE_THD):** Write Issue Threshold. Used to relax the issue criterion for Writes. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD (RD_ISSUE_THD):** Read Issue Threshold. Used to relax the issue criterion for Reads. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER (DST_PER):** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.
3:0	0h RW	**SRC_PER (SRC_PER):** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.

19.4.17 Source Gather (SGR0)—Offset 848h

NOTE: SGR0 is for DMA Channel 0. The same register definition, SGR1, is available for Channel 1 at address 8A0h.
SGR0(CH0): offset 848h
SGR1(CH1): offset 8A0h
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**SGC (SGC):** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI (SGI)**

19.4.18 Destination Scatter (DSR0)—Offset 850h

NOTE: DSR0 is for DMA Channel 0. The same register definition, DSR1, is available for Channel 1 at address 8A8h.
DSR0(CH0): offset 850h
DSR1(CH1): offset 8A8h
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**DSC (DSC)**
19:0	0h RW	**DSI (DSI)**

19.4.19 DMA Transfer Source Address Low (SAR_LO1)—Offset 858h

This register is for DMA Channel 1 and has the same definition as SAR_LO0 register at offset 800h.

19.4.20 DMA Transfer Source Address High (SAR_HI1)—Offset 85Ch

This register is for DMA channel 1 and has the same definition as SAR_HI0 at offset 804h.

19.4.21 DMA Transfer Destination Address Low (DAR_LO1)—Offset 860h

This register is for DMA channel 1 and has the same definition as DAR_LO0 at offset 808h.

19.4.22 DMA Transfer Destination Address High (DAR_HI1)—Offset 864h

This register is for DMA channel 1 and has the same definition as DAR_HI0 at offset 80Ch.

19.4.23 Linked List Pointer Low (LLP_LO1)—Offset 868h

This register is for DMA channel 1 and has the same definition as LLP_LO0 at offset 810h.

19.4.24 Linked List Pointer High (LLP_HI1)—Offset 86Ch

This register is for DMA channel 1 and has the same definition as LLP_HI0 at offset 814h.

19.4.25 Control Register Low 1 (CTL_LO1)—Offset 870h

This register is for DMA channel 1 and has the same definition as CTL_LO0 at offset 818h.

19.4.26 Control Register High 1 (CTL_HI1)—Offset 874h

This register is for DMA channel 1 and has the same definition as CTL_HI0 at offset 81Ch.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:18	0h NA	**RESERVED (RESERVED0):** Reserved
17:0	0h RO	Reserved.

19.4.27 Source Status 1 (SSTAT1)—Offset 878h

This register is for DMA channel 1 and has the same definition as SSTAT0 at offset 820h.

19.4.28 Destination Status 1 (DSTAT1)—Offset 880h

This register is for DMA channel 1 and has the same definition as DSTAT0 at offset 828h.

19.4.29 Source Status Address Low (SSTATAR_LO1)—Offset 888h

This register is for DMA channel 1 and has the same definition as SSTATAR_LO0 at offset 830h.

19.4.30 Source Status Address High (SSTATAR_HI1)—Offset 88Ch

This register is for DMA channel 1 and has the same definition as SSTATAR_HI0 at offset 834h.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR_HI (SSTATAR_HI):** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block

19.4.31 Destination Status Address Low (DSTATAR_LO1)—Offset 890h

This register is for DMA channel 1 and has the same definition as DSTATAR_LO0 at offset 838h.

19.4.32 Destination Status Address High (DSTATAR_HI1)—Offset 894h

This register is for DMA channel 1 and has the same definition as DSTATAR_HI0 at offset 83Ch.

19.4.33 DMA Transfer Configuration Low (CFG_LO1)—Offset 898h

This register is for DMA channel 1 and has the same definition as CFG_LO0 at offset 840h.

19.4.34 DMA Transfer Configuration High 1 (CFG_HI1)—Offset 89Ch

This register is for DMA channel 1 and has the same definition as CFG_HI0 at offset 844h.

19.4.35 Source Gather 1 (SGR1)—Offset 8A0h

This register is for DMA channel 1 and has the same definition as SDR0 at offset 848h.

19.4.36 Destination Scatter 1 (DSR1)—Offset 8A8h

This register is for DMA channel 1 and has the same definition as DSR0 at offset 850h.

19.4.37 Raw Interrupt Status (RawTfr)—Offset AC0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Bit0 for channel 0 and bit 1 for channel 1.

19.4.38 Raw Status for Block Interrupts (RawBlock)—Offset AC8h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Bit 0 for channel 0 and bit 1 for channel 1.

19.4.39 Raw Status for Source Transaction Interrupts (RawSrcTran)—Offset AD0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Bit 0 for channel 0 and bit 1 for channel 1.

19.4.40 Raw Status for Destination Transaction Interrupts (RawDstTran)—Offset AD8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Bit 0 for channel 0 and bit 1 for channel 1.

19.4.41 Raw Status for Error Interrupts (RawErr)—Offset AE0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Bit 0 for channel 0 and bit 1 for channel 1.

19.4.42 Interrupt Status (StatusTfr)—Offset AE8h

Status for Transfer Interrupts Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Bit 0 for channel 0 and bit 1 for channel 1.

19.4.43 Status for Block Interrupts (StatusBlock)—Offset AF0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Bit 0 for channel 0 and bit 1 for channel 1.

19.4.44 Status for Source Transaction Interrupts (StatusSrcTran)—Offset AF8h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Bit 0 is for channel 0 and bit 1 is for channel 1.

19.4.45 Status for Destination Transaction Interrupts (StatusDstTran)—Offset B00h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Bit 0 is for channel 0 and bit 1 is for channel 1.

19.4.46 Status for Error Interrupts (StatusErr)—Offset B08h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Bit 0 is for channel 0 and bit 1 is for channel 1.

19.4.47 Mask for Transfer Interrupts (MaskTfr)—Offset B10h

Mask for Transfer Interrupts Register

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** 0-mask 1-unmask

19.4.48 Mask for Block Interrupts (MaskBlock)—Offset B18h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** 0-mask 1-unmask

19.4.49 Mask for Source Transaction Interrupts (MaskSrcTran)—Offset B20h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** 0-mask 1-unmask

19.4.50 Mask for Destination Transaction Interrupts (MaskDstTran)—Offset B28h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** 0-mask 1-unmask

19.4.51 Mask for Error Interrupts (MaskErr)—Offset B30h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** 0-mask 1-unmask

19.4.52 Clear for Transfer Interrupts (ClearTfr)—Offset B38h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

19.4.53 Clear for Block Interrupts (ClearBlock)—Offset B40h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

19.4.54 Clear for Source Transaction Interrupts (ClearSrcTran)—Offset B48h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

19.4.55 Clear for Destination Transaction Interrupts (ClearDstTran)—Offset B50h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

19.4.56 Clear for Error Interrupts (ClearErr)—Offset B58h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

19.4.57 Combined Status register (StatusInt)—Offset B60h

The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran,StatusErr is Ored to produce a single bit for each interrupt type in the Combined Status register (StatusInt). Th is register is read-only

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**ERR (ERR):** OR of the contents of StatusErr register.
3	0h RO	**DSTT (DSTT):** OR of the contents of StatusDst register.
2	0h RO	**SRCT (SRCT):** OR of the contents of StatusSrcTran register
1	0h RO	**BLOCK (BLOCK):** OR of the contents of StatusBlock register.
0	0h RO	**TFR (TFR):** OR of the contents of StatusTfr register.

19.4.58 DMA Configuration (DmaCfgReg)—Offset B98h

This register is used to enable the DMA, which must be done before any channel activity can begin. If the global channel enable bit is cleared while any channel is still active, then DmaCfgReg.DMA_EN still returns 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the DmaCfgReg.DMA_EN bit returns 0.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**DMA_EN (DMA_EN):** 0 = DMA Disabled 1 = DMA Enabled

19.4.59 DMA Channel Enable (ChEnReg)—Offset BA0h

This is the DMA Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive, it can then enable an inactive channel with the required priority. All bits of this register are cleared to 0 when the global DMA channel enable bit, DmaCfgReg(0), is 0. When the global channel enable bit is 0, then a write to the ChEnReg register is ignored and a read will always read back 0. The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel write enable bit, ChEnReg.CH_EN_WE, is asserted on the same OCP write transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**Channel Enable Write Enable (CH_EN_WE):** Channel enable write enable.
7:2	0h RO	Reserved.
1:0	0h RW	**CH_EN (CH_EN):** Enables/Disables the channel. Setting this bit enables a channel, clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel The ChEnReg.CH_EN bit is automatically cleared by hardware to disable the channel after the last OCP transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer.

19.5 GSPI PCR Registers

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 19-5. Summary of GSPI PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
23Ch	23Fh	PCI Configuration Control for GSPI0 — Offset 23Ch	0h
240h	243h	PCI Configuration Control for GSPI1 — Offset 240h	0h
244h	247h	PCI Configuration Control for GSPI2 — Offset 244h	0h

19.5.1 PCI Configuration Control for GSPI0 — Offset 23Ch

Controls the PCI Configuration Space

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:20	0h RW	**PCI IRQ Num Field (PCI_IRQ):** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	0h RW	**PCICFGCTR1 - ACPI IRQ Field (ACPI_IRQ):** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	0h RW	**Interrupt Pin (IPIN7):** This register indicates the values to be used for Global Interrupts. 0 = No interrupt Pin 1 = INTA 2 = INTB 3 = INTC 4 = INTD 5 - FF: Reserved
7	0h RW	**BAR1 Disable (BAR1_DISABLE):** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	0h RW	**PME Support (PME_SUPPORT):** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1	0h RW	**ACPI Interrupt Enable Field (ACPI_INTR_EN):** When set, the Bridge uses ACPI Sideband opcodes for messages. When cleared, the Bridge uses global IOSF opcodes
0	0h RW	**PCI CFG Disable Field (PCI_CFG_DIS):** When set, PCI configuration accesses return UR response. When 0, PCI configuration accesses are supported

19.5.2 PCI Configuration Control for GSPI1 — Offset 240h

Same definition as PCI Configuration Control for GSPI0.

19.5.3 PCI Configuration Control for GSPI2 — Offset 244h

Same definition as PCI Configuration Control for GSPI0.

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20 PCIe Interface (D29:F0-F3, D28:F0-F3 and D28:F6)

20.1 PCIe Interface (D29:F0-F3 and D28:F0-F3 and D28: F6) Registers

Table 20-1. Summary of PCIe Interface (D28:F0-F3, D28: F6 and D29:F0-F3) Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Identifiers (ID)—Offset 0h	XXXX8086h
4h	7h	Device Command And Primary Status (CMD_PSTS)—Offset 4h	100000h
8h	Bh	Revision ID And Class Code (RID_CC)—Offset 8h	60400FXh
Ch	Fh	Cache Line Size, Primary Latency Timer And Header Type (CLS_PLT_HTYPE)—Offset Ch	810000h
18h	1Bh	Bus Numbers And Secondary Latency Timer (BNUM_SLT)—Offset 18h	0h
1Ch	1Fh	I/O Base And Limit And Secondary Status (IOBL_SSTS)—Offset 1Ch	0h
20h	23h	Memory Base And Limit (MBL)—Offset 20h	0h
24h	27h	Prefetchable Memory Base And Limit (PMBL)—Offset 24h	10001h
28h	2Bh	Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h	0h
2Ch	2Fh	Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch	0h
34h	37h	Capabilities List Pointer (CAPP)—Offset 34h	40h
3Ch	3Fh	Interrupt Information And Bridge Control (INTR_BCTRL)—Offset 3Ch	0h
40h	43h	Capabilities List And PCI Express Capabilities (CLIST_XCAP)—Offset 40h	428010h
44h	47h	Device Capabilities (DCAP)—Offset 44h	8001h
48h	4Bh	Device Control And Device Status (DCTL_DSTS)—Offset 48h	100000h
4Ch	4Fh	Link Capabilities (LCAP)—Offset 4Ch	710C00h
50h	53h	Link Control And Link Status (LCTL_LSTS)—Offset 50h	10000h
54h	57h	Slot Capabilities (SLCAP)—Offset 54h	40060h
58h	5Bh	Slot Control And Slot Status (SLCTL_SLSTS)—Offset 58h	0h
5Ch	5Fh	Root Control (RCTL)—Offset 5Ch	0h
60h	63h	Root Status (RSTS)—Offset 60h	0h
64h	67h	Device Capabilities 2 (DCAP2)—Offset 64h	80837h
68h	6Bh	Device Control 2 And Device Status 2 (DCTL2_DSTS2)—Offset 68h	0h
6Ch	6Fh	Link Capabilities 2 (LCAP2)—Offset 6Ch	0h
70h	73h	Link Control 2 And Link Status 2 (LCTL2_LSTS2)—Offset 70h	1h
80h	83h	Message Signaled Interrupt Identifiers And Message Signaled Interrupt Message Control (MID_MC)—Offset 80h	9005h
84h	87h	Message Signaled Interrupt Message Address (MA)—Offset 84h	0h
88h	8Bh	Message Signaled Interrupt Message Data (MD)—Offset 88h	0h
90h	93h	Subsystem Vendor Capability (SVCAP)—Offset 90h	A00Dh

Table 20-1. Summary of PCIe Interface (D28:F0-F3, D28: F6 and D29:F0-F3) Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
94h	97h	Subsystem Vendor IDs (SVID)—Offset 94h	0h
A0h	A3h	Power Management Capability And PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h	C8030001h
A4h	A7h	PCI Power Management Control And Status (PMCS)—Offset A4h	8h
D0h	D3h	Additional Configuration 1 (CCFG)—Offset D0h	0h
100h	103h	Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h	0h
104h	107h	Uncorrectable Error Status (UES)—Offset 104h	0h
108h	10Bh	Uncorrectable Error Mask (UEM)—Offset 108h	0h
10Ch	10Fh	Uncorrectable Error Severity (UEV)—Offset 10Ch	60011h
110h	113h	Correctable Error Status (CES)—Offset 110h	0h
114h	117h	Correctable Error Mask (CEM)—Offset 114h	2000h
118h	11Bh	Advanced Error Capabilities And Control (AECC)—Offset 118h	0h
12Ch	12Fh	Root Error Command (REC)—Offset 12Ch	0h
130h	133h	Root Error Status (RES)—Offset 130h	0h
134h	137h	Error Source Identification (ESID)—Offset 134h	0h
200h	203h	L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h	0h
204h	207h	L1 Sub-States Capabilities (L1SCAP)—Offset 204h	28281Fh
208h	20Bh	L1 Sub-States Control 1 (L1SCTL1)—Offset 208h	0h
20Ch	20Fh	L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch	28h
220h	223h	ACS Extended Capability Header (ACSECH)—Offset 220h	0h
224h	227h	ACS Capability Register And ACS Control Register (ACSCAPR_ACSCTLR)—Offset 224h	1Fh

20.1.1 Identifiers (ID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: XXXX8086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	-- RO/V	**Device Identification (DID):** The value of this ID is product specific. Refer to the Device and Revision ID Table in Volume 1 for default value.
15:0	8086h RO	**Vendor Identification (VID):** Indicates Intel

20.1.2 Device Command And Primary Status (CMD_PSTS)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**DPE - Detected Parity Error (DPE):** Set when the root port receives a command or data from the backbone with a parity error. This is set even if PCMD.PERE is not set.
30	0h RW/1C/V	**Signaled System Error (SSE):** Set when the root port signals a system error to the internal SERR# logic.
29	0h RW/1C/V	**Received Initiator Abort (RMA):** Set when the root port receives a completion with unsupported request status from the backbone.
28	0h RW/1C/V	**Received Target Abort (RTA):** Set when the root port receives a completion with completer abort from the backbone.
27	0h RW/1C/V	**Signaled Target Abort (STA):** Set whenever the root port forwards a target abort received from the downstream device onto the backbone.
26:25	0h RO	**Primary DEVSEL# Timing Status (PDTS):** Reserved per PCI-Express spec
24	0h RW/1C/V	**Initiator Data Parity Error Detected (DPD):** Set when the root port receives a completion with a data parity error on the backbone and PCMD.PERE is set.
23	0h RO	**Primary Fast Back to Back Capable (PFBC):** Reserved per PCI-Express spec.
22	0h RO	Reserved.
21	0h RO	**Primary 66 MHz Capable (PC66):** Reserved per PCI-Express spec.
20	1h RO	**Capabilities List (CLIST):** Indicates the presence of a capabilities list.
19	0h RO/V	**Interrupt Status (IS):** Indicates status of hot plug and power management interrupts on the root port that result in INTx# message generation. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of CMD.ID.
18:11	0h RO	Reserved.
10	0h RW/V2	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts on enabled hot plug and power management events. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt for hot plug or power management and MSI is not enabled. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RO and returns a value of 0 when read, else it is RW with the functionality described above.
9	0h RO	**Fast Back to Back Enable (FBE):** Reserved per PCI-Express spec.
8	0h RW	**SERR# Enable (SEE):** When set, enables the root port to generate an SERR# message when PSTS.SSE is set.
7	0h RO	**Wait Cycle Control (WCC):** Reserved per PCI-Express spec.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Parity Error Response Enable (PERE):** Indicates that the device is capable of reporting parity errors as a Initiator on the backbone.
5	0h RO	**VGA Palette Snoop (VGA_PSE):** Reserved per PCI-Express spec.
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** Reserved per PCI-Express spec.
3	0h RO	**Special Cycle Enable (SCE):** Reserved per PCI-Express and PCI bridge spec.
2	0h RW	**Bus Initiator Enable (BME):** When set, allows the root port to forward Memory and I/O Read/Write cycles onto the backbone from a PCI-Express device. When this bit is 0b, Memory and I/O requests received at a Root Port must be handled as Unsupported Requests (UR). This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O requests is not controlled by this bit.
1	0h RW	**Memory Space Enable (MSE):** When set, memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI-Express device. When cleared, these memory cycles are Initiator aborted on the backbone.
0	0h RW	**I/O Space Enable (IOSE):** When set, I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI-Express device. When cleared, these cycles are Initiator aborted on the backbone..

20.1.3 Revision ID And Class Code (RID_CC)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 60400FXh

Bit Range	Default & Access	Field Name (ID): Description
31:24	6h RO	**Base Class Code (BCC):** Indicates the device is a bridge device.
23:16	4h RO/V	**Sub-Class Code (SCC):** The default indicates the device is a PCI-to-PCI bridge. If the MPC.Bridge Type register is set to a '1' for a Host Bridge, this register reads 00h.
15:8	0h RO/V	**Programming Interface (PI):** PCI-to-PCI bridge.
7:0	-- RO/V	**Revision ID (RID):** Indicates the revision of the bridge. Refer to Device and Revision ID table in Vol1 for specific value.

20.1.4 Cache Line Size, Primary Latency Timer And Header Type (CLS_PLT_HTYPE)—Offset Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 810000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	1h RO	**Multi-function Device (MFD):** This bit is '1' to indicate a multi-function device.
22:16	1h RO/V	**Header Type (HTYPE):** The default mode identifies the header layout of the configuration space, which is a PCI-to-PCI bridge. If the MPC.Bridge Type register is set to a '1' for a Host Bridge, this register reads 00h.
15:11	0h RO	**Latency Count (CT):** Reserved per PCI-Express spec
10:8	0h RO	Reserved.
7:0	0h RW	**Line Size (LS):** This is read/write but contains no functionality, per PCI-Express spec

20.1.5 Bus Numbers And Secondary Latency Timer (BNUM_SLT)—Offset 18h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/V2	**Secondary Latency Timer (SLT):** For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is a RW register; else this register is RO and returns 0. This register does not affect the behavior of any HW logic.
23:16	0h RW	**Subordinate Bus Number (SBBN):** Indicates the highest PCI bus number below the bridge.
15:8	0h RW	**Secondary Bus Number (SCBN):** Indicates the bus number the port.
7:0	0h RW	**Primary Bus Number (PBN):** Indicates the bus number of the backbone.

20.1.6 I/O Base And Limit And Secondary Status (IOBL_SSTS)—Offset 1Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Detected Parity Error (DPE):** Set when the port receives a poisoned TLP.
30	0h RW/1C/V	**Received System Error (RSE):** Set when the port receives an ERR_FATAL or ERR_NONFATAL message from the device.
29	0h RW/1C/V	**Received Initiator Abort (RMA):** Set when the port receives a completion with Unsupported Request status to the device.
28	0h RW/1C/V	**Received Target Abort (RTA):** Set when the port receives a completion with Completion Abort status to the device.
27	0h RW/1C/V	**Signaled Target Abort (STA):** Set when the port generates a completion with Completion Abort status to the device.
26:25	0h RO/V	**Secondary DEVSEL# Timing Status (SDTS):** Reserved per PCI-Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 01b when read, else this register returns a value of 00b.
24	0h RW/1C/V	**Data Parity Error Detected (DPD):** Set when the BCTRL.PERE, and either of the following two conditions occurs: Port receives completion marked poisoned. Port poisons a write request to the secondary side.
23	0h RO/V	**Secondary Fast Back to Back Capable (SFBC):** Reserved per PCI Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 1b when read, else this register returns a value of 0b.
22	0h RO	Reserved.
21	0h RO	**Secondary 66 MHz Capable (SC66):** Reserved per PCI Express spec
20:16	0h RO	Reserved.
15:12	0h RW	**I/O Address Limit (IOLA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to FFFh.
11:8	0h RO	**I/O Limit Address Capability (IOLC):** Indicates that the bridge does not support 32-bit I/O addressing.
7:4	0h RW	**I/O Base Address (IOBA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	0h RO	**I/O Base Address Capability (IOBC):** Indicates that the bridge does not support 32-bit I/O addressing.

20.1.7 Memory Base And Limit (MBL)—Offset 20h

Accesses that are within the ranges specified in this register will be sent to the attached device if CMD.MSE is set. Accesses from the attached device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Memory Limit (ML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	0h RO	Reserved.
15:4	0h RW	**Memory Base (MB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	0h RO	Reserved.

20.1.8 Prefetchable Memory Base And Limit (PMBL)—Offset 24h

Accesses that are within the ranges specified in this register will be sent to the device if CMD.MSE is set. Accesses from the device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 10001h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Prefetchable Memory Limit (PML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	1h RO	**64-bit Indicator (I64L):** Indicates support for 64-bit addressing.
15:4	0h RW	**Prefetchable Memory Base (PMB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	1h RO	**64-bit Indicator (I64B):** Indicates support for 64-bit addressing.

20.1.9 Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Prefetchable Memory Base Upper Portion (PMBU):** Upper 32-bits of the prefetchable address base.

20.1.10 Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch

Access Method

Type: CFG Register (Size: 32 bits)
Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Prefetchable Memory Limit Upper Portion (PMLU):** Upper 32-bits of the prefetchable address limit.

20.1.11 Capabilities List Pointer (CAPP)—Offset 34h

This is Capabilities List Pointer register. Refer to register field for more details

Access Method

Type: CFG Register (Size: 32 bits)
Device: 28
Function:

Default: 40h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	40h RW/O	**Capabilities Pointer (PTR):** Indicates that the pointer for the first entry in the capabilities list. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. Capability Linked List (Default Settings) Offset Capability Next Pointer 40h PCI Express 80h 80h Message Signaled Interrupt (MSI)90h 90h Subsystem Vendor A0h A0h PCI Power Management 00h Extended PCIe Capability Linked List Offset Capability Next Pointer 100h Advanced Error Reporting 000h

20.1.12 Interrupt Information And Bridge Control (INTR_BCTRL)—Offset 3Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27	0h RW/V2	**Discard Timer SERR# Enable (DTSE):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
26	0h RO	**Discard Timer Status (DTS):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, this register can remain RO as no secondary discard timer exists that will ever cause it to be set.
25	0h RW/V2	**Secondary Discard Timer (SDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
24	0h RW/V2	**Primary Discard Timer (PDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
23	0h RO	**Fast Back to Back Enable (FBE):** Reserved per Express spec.
22	0h RW	**Secondary Bus Reset (SBR):** Triggers a Hot Reset on the PCI-Express port.
21	0h RW/V2	**Initiator Abort Mode (MAM):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
20	0h RW	**VGA 16-Bit Decode (V16):** When set, indicates that the I/O aliases of the VGA range (see BCTRL:VE definition below), are not enabled. 0: Execute 10-bit address decode on VGA I/O accesses. 1: Execute 16-bit address decode on VGA I/O accesses.
19	0h RW	**VGA Enable (VE):** When set, the following ranges will be claimed off the backbone by the root port: Memory ranges A0000h-BFFFFh I/O ranges 3B0h 3BBh and 3C0h 3DFh, and all aliases of bits 15:10 in any combination of 1's
18	0h RW	**ISA Enable (IE):** This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64KB of PCI I/O space. If this bit is set, the root port will block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1KB block (offsets 100h to 3FFh).
17	0h RW	**SERR# Enable (SE):** When set, ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone. When cleared, they are not.
16	0h RW	**Parity Error Response Enable (PERE):** When set, poisoned write TLPs and completions indicating poisoned TLPs will set the SSTS.DPD.
15:8	0h RO/V	**Interrupt Pin (IPIN):** Indicates the interrupt pin driven by the root port. 0000 0001 = INTA# 0000 0010 = INTB# 0000 0011 = INTC# 0000 0100 = INTD# Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

20.1.13 Capabilities List And PCI Express Capabilities (CLIST_XCAP)—Offset 40h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 428010h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:25	0h RO	**Interrupt Message Number (IMN):** The Root Port does not have multiple MSI interrupt numbers.
24	0h RW/O	**Slot Implemented (SI):** Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset.
23:20	4h RO	**Device / Port Type (DT):** Indicates this is a PCI-Express root port
19:16	2h RO	**Capability Version (CV):** Version 2.0 indicates devices compliant to the PCI Express 2.0 and 3.0 specification which incorporates the Register Expansion ECN.
15:8	80h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability. The default value of this register is 80h which points to the MSI Capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	10h RO	**Capability ID (CID):** Indicates this is a PCI Express capability

20.1.14 Device Capabilities (DCAP)—Offset 44h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 8001h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
28	0h RO	**Function Level Reset Capable (FLRC):** Not supported in Root Ports
27:26	0h RO	**Captured Slot Power Limit Scale (CSPS):** Not supported
25:18	0h RO	**Captured Slot Power Limit Value (CSPV):** Not supported
17:16	0h RO	Reserved.
15	1h RO	**Role Based Error Reporting (RBER):** Indicates that this device implements the functionality defined in the Error Reporting ECN as required by the PCI Express 1.1 spec.
14:12	0h RO	Reserved.
11:9	0h RO	**Endpoint L1 Acceptable Latency (E1AL):** Reserved for root ports.
8:6	0h RO	**Endpoint L0 Acceptable Latency (E0AL):** Reserved for Root port.
5	0h RO	**Extended Tag Field Supported (ETFS):** The Root Port never needs to initiate a transaction as a Requester with the Extended Tag bits being set. This bit does not affect the root port's ability to forward requests as a bridge as the root port always supports forwarding requests with extended tags.
4:3	0h RO	**Phantom Functions Supported (PFS):** No phantom functions supported
2:0	1h RW/O	**Max Payload Size Supported (MPS):** BIOS should write to this field during system initialization. Max Payload Size of up to 256B is supported. Programming this field to any values other than 128B or 256B max payload size will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface.

20.1.15 Device Control And Device Status (DCTL_DSTS)—Offset 48h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**Transactions Pending (TDP):** This bit has no meaning for the root port since it never initiates a non-posted request with its own Requester ID.
20	1h RO	**AUX Power Detected (APD):** The root port contains AUX power for wakeup
19	0h RW/1C/V	**Unsupported Request Detected (URD):** Indicates an unsupported request was detected.
18	0h RW/1C/V	**Fatal Error Detected (FED):** Indicates a fatal error was detected. Set when a fatal error occurred on from a data link protocol error, buffer overflow, or malformed tlp
17	0h RW/1C/V	**Non-Fatal Error Detected (NFED):** Indicates a non-fatal error was detected. Set when an received a non-fatal error occurred from a poisoned tlp, unexpected completions, unsupported requests, completor abort, or completer timeout
16	0h RW/1C/V	**Correctable Error Detected (CED):** Indicates a correctable error was detected. Set when received an internal correctable error from receiver errors / framing errors, tlp crc error, dllp crc error, replay num rollover, replay timeout.
15	0h RO	Reserved.
14:12	0h RO	**Max Read Request Size (MRRS):** Hardwired to 0. This field applies only to the PCIe link interface. A separate register is defined for the IOSF interface.
11	0h RO	**Enable No Snoop (ENS):** Not supported. The root port will never issue non-snoop requests.
10	0h RW/P	**Aux Power PM Enable (APME):** The OS will set this bit to '1' if the device connected has detected aux power. It has no effect on the root port otherwise.
9	0h RO	**Phantom Functions Enable (PFE):** Not supported
8	0h RO	**Extended Tag Field Enable (ETFE):** Not supported
7:5	0h RW	**Max Payload Size (MPS):** The root port only supports up to 256B max payload. Programming this field to any values greater than DCAP.MPS will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. A separate register is defined for the IOSF interface.Note: Software should ensure that the system is quiescent and no TLP is in progress prior to changing this field. BIOS should program this field prior to enabling BME. Register Attribute: Static.
4	0h RO	**Enable Relaxed Ordering (ERO):** Not supported
3	0h RW	**Unsupported Request Reporting Enable (URE):** When set, allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-Advisory UR is received with the severity set by the Uncorrectable Error Severity register.
2	0h RW	**Fatal Error Reporting Enable (FEE):** enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Non-Fatal Error Reporting Enable (NFE):** When set, enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	0h RW	**Correctable Error Reporting Enable (CEE):** When set, enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

20.1.16 Link Capabilities (LCAP)—Offset 4Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 710C00h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**Port Number (PN):** Indicates the port number for the root port. This value is different for each implemented port: Port # Value of PN field 1 01h 2 02h 3 03h 4 04h : : x 0Xh Note: Depending on the platform, the number of Root Ports supported may vary. In this case, the encodings defined in this register will be scaled accordingly.
23	0h RO	Reserved.
22	1h RW/O	**ASPM Optionality Compliance (ASPMOC):** ASPM Optionality Compliance(ASPMOC): This bit must be set to 1b for PCIe 3.0 compliant port. Components implemented against certain earlier versions of this specification will have this bit set to 0b. Software is permitted to use the value of this bit to help determine whether to enable ASPM or whether to run ASPM compliance tests.
21	1h RO	**Link Bandwidth Notification Capability (LBNC):** This port supports Link Bandwidth Notification status and interrupt mechanisms.
20	1h RO	**Link Active Reporting Capable (LARC):** This port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine.
19	0h RO	**Surprise Down Error Reporting Capable (SDERC):** Set to '0' to indicate the Root Port does not support Surprise Down Error Reporting
18	0h RO	**Clock Power Management (CPM):** '0' Indicates that root ports do not support the CLKREQ# mechanism.

Bit Range	Default & Access	Field Name (ID): Description
17:15	2h RW/O	**L1 Exit Latency (EL1):** Indicates an exit latency of 2us to 4us. 000b Less than 1 us 001b 1 us to less than 2 us 010b 2 us to less than 4 us 011b 4 us to less than 8 us 100b 8 us to less than 16 us 101b 16 us to less than 32 us 110b 32 us to 64 us 111b More than 64 us Note: If PXP PLL shutdown is enabled, BIOS should program this latency to comprehend PLL lock latency.
14:12	0h RO/V	**L0s Exit Latency (EL0):** Indicates an exit latency based upon common-clock configuration: LCTL.CCC Value 0 MPC.UCEL 1 MPC.CCEL
11:10	3h RW/O	**Active State Link PM Support (APMS):** Indicates the level of active state power management on this link Bits Definition 00 No ASPM Supported 01 L0s Supported 10 L1 Supported 11 L0s and L1 supported
9:4	0h RO/V	Port # Value of PN field RPC 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h
3:0	0h RO/V	**Max Link Speeds (MLS):** This field indicates the maximum Link speed of the associated Port. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the maximum Link speed. Defined encodings are: 0001b: 2.5 GT/s supported. 0010b: 5.0 GT/s supported. 0011b: 8.0 GT/s supported. Others: reserved

20.1.17 Link Control And Link Status (LCTL_LSTS)—Offset 50h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 28

Function:

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Link Autonomous Bandwidth Status (LABS):** This bit is Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The default value of this bit is 0b.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RW/1C/V	**Link Bandwidth Management Status (LBMS):** This bit is Set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: - A Link retraining has completed following a write of 1b to the Retrain Link bit Note: This bit is Set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. - Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. The default value of this bit is 0b.
29	0h RO/V	**Link Active (LA):** Set to 1b when the Data Link Control and Management State Machine is in the DL_Active state, 0b otherwise.
28	0h RO/V	**Slot Clock Configuration (SCC):** In normal mode, root port uses the same reference clock as on the platform and does not generate its own clock. Note: When operating in PCI Express mode, the default of this register bit is dependent on the PCIe Non-Common Clock With SSC Mode Enable Strap. If the strap enables non-common clock with SSC support, this bit shall default to '0'. Otherwise, this bit shall default to '1'.
27	0h RO/V	**Link Training (LT):** The root port sets this bit whenever link training is occurring, or that 1b was written to the Retrain Link bit but Link training has not yet begun. It clears the bit upon completion of link training.
26	0h RO	Reserved.
25:20	0h RO/V	**Negotiated Link Width (NLW):** For the root ports, this register could take on several values: Port # Value of PN field RPC 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h The value of this register is undefined if the link has not successfully trained.
19:16	1h RO/V	**Current Link Speed (CLS):** This field indicates the negotiated Link speed of the given link. Defined encodings are: 0001b: 2.5 GT/s supported. 0010b: 5.0 GT/s supported. 0011b: 8.0 GT/s supported. Others: reserved
15:12	0h RO	Reserved.
11	0h RW	**Link Autonomous Bandwidth Interrupt Enable (LABIE):** Link Autonomous Bandwidth Interrupt Enable - When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set.
10	0h RW	**Link Bandwidth Management Interrupt Enable (LBMIE):** When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. Functions that do not implement the Link Bandwidth Notification Capability must hardwire this bit to 0b. Default value of this bit is 0b.
9	0h RW	**Hardware Autonomous Width Disable (HAWD):** When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Default value of this bit is 0b. Note: When operating as PCI Express, this bit defines the value of the Link Upconfigure Capability in TS2 Ordered Sets.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**Enable Clock Power Management (ECPM):** Reserved. Not supported on Root Ports.
7	0h RW	**Extended Synch (ES):** When set, forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0. Note: This functionality is not applicable for Mobile Express.
6	0h RW	**Common Clock Configuration (CCC):** When set, indicates that the Root Port and device are operating with a distributed common reference clock.
5	0h WO	**Retrain Link (RL):** When set, the root port will train its downstream link. This bit always returns '0' when read. Software uses LSTS.LT and LSTS.LTE to check the status of training. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress.
4	0h RW	**Link Disable (LD):** When set, the root port will disable the link by directing the LTSSM to the Disabled state.
3	0h RW/O	**Read Completion Boundary Control (RCBC):** Indicates the read completion boundary is 64 bytes.
2	0h RO	Reserved.
1:0	0h RW	**Active State Link PM Control (ASPM):** Indicates whether the root port should enter L0s or L1 or both. Bits Definition 00 Disabled 01 L0s Entry Enabled 10 L1 Entry Enabled 11 L0s and L1 Entry Enabled The value of this register is used unless the Root Port ASPM Control Override Enable register is set, in which case the Root Port ASPM Control Override value is used.

20.1.18 Slot Capabilities (SLCAP)—Offset 54h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 40060h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/O	**Physical Slot Number (PSN__31_24):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
23:19	0h RW/O	**Physical Slot Number (PSN__23_19):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
18	1h RO	**No Command Completed Support (NCCS):** Set to '1' as this port does not implement a Hot Plug controller and can handle back-2-back writes to all fields of the slot control register without delay between successive writes.
17	0h RO	**Electromechanical Interlock Present (EMIP):** Set to 0 to indicate that no electro-mechanical interlock is implemented.

Bit Range	Default & Access	Field Name (ID): Description
16:15	0h RW/O	**Slot Power Limit Scale (SLS):** specifies the scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset.
14:8	0h RW/O	**Slot Power Limit Value (SLV__14_8):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
7	0h RW/O	**Slot Power Limit Value (SLV__7_7):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
6	1h RW/O	**Hot Plug Capable (HPC):** When set, Indicates that hot plug is supported.
5	1h RW/O	**Hot Plug Surprise (HPS):** When set, indicates the device may be removed from the slot without prior notification.
4	0h RO	**Power Indicator Present (PIP):** Indicates that a power indicator LED is not present for this slot.
3	0h RO	**Attention Indicator Present (AIP):** Indicates that an attention indicator LED is not present for this slot.
2	0h RO	**MRL Sensor Present (MSP):** Indicates that an MRL sensor is not present
1	0h RO	**Power Controller Present (PCP):** Indicates that a power controller is not implemented for this slot
0	0h RO	**Attention Button Present (ABP):** Indicates that an attention button is not implemented for this slot.

20.1.19 Slot Control And Slot Status (SLCTL_SLSTS)—Offset 58h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RW/1C/V	**Data Link Layer State Changed (DLLSC):** This bit is set when the value reported in Data Link Layer Link Active field of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot plugged device.
23	0h RO	**Electromechanical Interlock Status (EMIS):** Reserved as this port does not support and electromechanical interlock.
22	0h RO/V	**Presence Detect State (PDS):** If XCAP.SI is set (indicating that this root port spawns a slot), then this bit indicates whether a device is connected ('1') or empty ('0'). If XCAP.SI is cleared, this bit is a '1'.
21	0h RO	**MRL Sensor State (MS):** Reserved as the MRL sensor is not implemented.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**Command Completed (CC):** This register is RO as this port does not implement a Hot Plug Controller..
19	0h RW/1C/V	**Presence Detect Changed (PDC):** This bit is set by the root port when the PDS bit changes state.
18	0h RO	**MRL Sensor Changed (MSC):** Reserved as the MRL sensor is not implemented.
17	0h RO	**Power Fault Detected (PFD):** Reserved as a power controller is not implemented.
16	0h RO	**Attention Button Pressed (ABP):** This register is RO as this port does not implement an attention button
15:14	0h RO	Reserved.
13	0h RW	**Auto Slot Power Limit Disable (ASPLD):** When set, this bit disables automatic sending of Set_Slot_Power_Limit message when the link transitions from non-DL_Up status to DL_Up status. Register Attribute: Dynamic.
12	0h RW	**Data Link Layer State Changed Enable (DLLSCE):** When set, this field enables generation of a hot plug interrupt when the Data Link Layer Link Active field is changed
11	0h RO	**Electromechanical Interlock Control (EMIC):** Reserved as this port does not support an Electromechanical Interlock.
10	0h RO	**Power Controller Control (PCC):** This bit has no meaning for module based hot plug.
9:8	0h RO	**Power Indicator Control (PIC):** This register is RO as this port does not implement a Hot Plug Controller..
7:6	0h RO	**Attention Indicator Control (AIC):** This register is RO as this port does not implement a Hot Plug Controller..
5	0h RW	**Hot Plug Interrupt Enable (HPE):** When set, enables generation of a hot plug interrupt on enabled hot plug events.
4	0h RO	**Command Completed Interrupt Enable (CCE):** This register is RO as this port does not implement a Hot Plug Controller..
3	0h RW	**Presence Detect Changed Enable (PDE):** When set, enables the generation of a hot plug interrupt or wake message when the presence detect logic changes state.
2	0h RO	**MRL Sensor Changed Enable (MSE):** This register is RO as this port does not implement a Hot Plug Controller..
1	0h RO	**Power Fault Detected Enable (PFE):** This register is RO as this port does not implement a Hot Plug Controller...
0	0h RO	**Attention Button Pressed Enable (ABE):** This register is RO as this port does not implement a Hot Plug Controller..

20.1.20 Root Control (RCTL)—Offset 5Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	0h RW	**PME Interrupt Enable (PIE):** When set, enables interrupt generation when RSTS.PS is in a set state (either due to a '0' to '1' transition, or due to this bit being set with RSTS.PS already set).
2	0h RW	**System Error on Fatal Error Enable (SFE):** When set, an SERR# will be generated if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port. This register is not dependent on CMD.SEE being set.
1	0h RW	**System Error on Non-Fatal Error Enable (SNE):** When set, an SERR# will be generated if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port. This register is not dependent on CMD.SEE being set.
0	0h RW	**System Error on Correctable Error Enable (SCE):** When set, an SERR# will be generated if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port. This register is not dependent on CMD.SEE being set.

20.1.21 Root Status (RSTS)—Offset 60h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RO/V	**PME Pending (PP):** Indicates another PME is pending when the PME status bit is set. When the original PME is cleared by software, it will be set again, the requestor ID will be updated, and this bit will be cleared. Root ports have a one deep PME pending queue.
16	0h RW/1C/V	**PME Status (PS):** Indicates that PME was asserted by the requestor ID in RID. Subsequent PMEs are kept pending until this bit is cleared.
15:0	0h RO/V	**PME Requestor ID (RID):** Indicates the PCI requestor ID of the last PME requestor. Valid only when PS is set. Root ports are capable of storing the requester ID for two PM_PME messages, with one active (this register) and a one deep pending queue. Subsequent PM_PME messages will be dropped.

20.1.22 Device Capabilities 2 (DCAP2)—Offset 64h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 80837h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19:18	2h RW/O	**Optimized Buffer Flush/Fill Supported (OBFFS):** 00b - OBFF is not supported. 01b - OBFF is supported using Message signaling only. 10b - OBFF is supported using WAKE# signaling only. 11b - OBFF is supported using WAKE# and Message signaling. Note: OBFF is not supported. BIOS should program this field to 00b.
17:12	0h RO	Reserved.
11	1h RW/O	**LTR Mechanism Supported (LTRMS):** A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism capability. BIOS must write to this register with either a '1' or a '0' to enable/disable the root port from declaring support for the LTR capability.
10:6	0h RO	Reserved.
5	1h RO	**ARI Forwarding Supported (AFS):** ARI Forwarding Supported (AFS): Applicable only to Switch Downstream Ports and Root Ports; must be 0b for other Function types. This bit must be set to 1b if a Switch Downstream Port or Root Port supports this optional capability. Note: This bit is not made RWO to simplify implementation, since there is a requirement that the ARI Forwarding Enable bit must be hardwired to 0b if ARI Forwarding Supported bit is 0b. It is low risk to keep this risk 1b. Register Attribute: Static.
4	1h RO	**Completion Timeout Disable Supported (CTDS):** A value of 1b indicates support for the Completion Timeout Disable mechanism.
3:0	7h RO	**Completion Timeout Ranges Supported (CTRS):** This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50us to 10ms Range B: 10ms to 250ms Range C: 250ms to 4s Range D: 4s to 64s Bits are set according to the table below to show timeout value ranges supported. 0000b Completion Timeout programming not supported. 0001b Range A 0010b Range B 0011b Ranges A and B 0110b Ranges B and C 0111b Ranges A, B, and C [lt]-- This is what PCH supports 1110b Ranges B, C, and D 1111b Ranges A, B, C, and D All other values are reserved.

20.1.23 Device Control 2 And Device Status 2 (DCTL2_DSTS2)—Offset 68h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	Reserved.
10	0h RW	**LTR Mechanism Enable (LTREN):** When Set to 1b, this bit enables the Latency Tolerance Reporting (LTR) mechanism. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. If DCAP2.LTRMS is clear, programming this field to any non-zero values will have no effect.
9:6	0h RO	Reserved.
5	0h RW	**ARI Forwarding Enable (AFE):** ARI Forwarding Enable (AFE): When set, the Downstream Port disables its traditional Device Number field being 0b enforcement when turning a Type 1 Configuration Request into a Type 0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port. Register Attribute: Dynamic.
4	0h RW	**Completion Timeout Disable (CTD):** When set to 1b, this bit disables the Completion Timeout mechanism. This field is required for all devices that support the Completion Timeout Disable Capability. Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding requests. If this is done, it is permitted to base the start time for each request on either the time this bit was cleared or the time each request was issued.
3:0	0h RW	**Completion Timeout Value (CTV):** In Devices that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. A Device that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50us to 50ms. Devices that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Values Supported field. The root port targeted configurable ranges are listed below, along with the range allowed by the PCI Express 2.0 specification. Defined encodings: 0000b Default range: 40-50ms (spec range 50us to 50ms) Values available if Range A (50us to 10 ms) programmability range is supported: 0001b 90-100us (spec range is 50 us to 100 us) 0010b 9-10ms (spec range is 1ms to 10 ms) Values available if Range B (10ms to 250ms) programmability range is supported: 0101b 40-50ms (spec range is 16ms to 55ms) 0110b 160-170ms (spec range is 65ms to 210ms) Values available if Range C (250ms to 4s) programmability range is supported: 1001b 400-500ms (spec range is 260ms to 900ms) 1010b 1.6-1.7s (spec range is 1s to 3.5s) Values not defined above are Reserved. Software is permitted to change the value in this field at any time. For requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding requests, and is permitted to base the start time for each request either on when this value was changed or on when each request was issued.

20.1.24 Link Capabilities 2 (LCAP2)—Offset 6Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:16	0h RO	**Lower SKP OS Reception Supported Speeds Vector (LSOSRSS):** Lower SKP OS Reception Supported Speeds Vector(LSOSRSS): If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports receiving SKP OS at the rate defined for SRNS while running in SRIS. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector.
15:9	0h RO	**Lower SKP OS Generation Supported Speeds Vector (LSOSGSSV):** Lower SKP OS Generation Supported Speeds Vector(LSOSGSSV): If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports software control of the SKP Ordered Set transmission scheduling rate. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector.
8	0h RO	**Crosslink Supported (CS):** Crosslink Supported (CS): No support for Crosslink. Register Attribute: Static.
7:1	0h RO/V	**Supported Link Speeds Vector (SLSV):** Supported Link Speeds Vector (SLSV): This field indicates the supported Link speed of the associated Port. For each bit, a value of 1b indicates that the corresponding Link speed is supported; otherwise, the Link speed is not supported. Bit definitions within this field for PCI Express are: Bit 0: 2.5 GT/s. Bit 1: 5.0 GT/s. Bit 2: 8.0 GT/s. Bits 6:3: Reserved.
0	0h RO	Reserved.

20.1.25 Link Control 2 And Link Status 2 (LCTL2_LSTS2)—Offset 70h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW/1C/V/P	**Link Equalization Request (LER):** Link Equalization Request (LER): This bit is set by hardware to request the Link equalization process to be performed on the Link. Register Attribute: Dynamic.
20	0h RO/V/P	**Equalization Phase 3 Successful (EQP3S):** Equalization Phase 3 Successful (EQP3S): When set to 1, this bit indicates that Phase 3 of the Transmitter Equalization procedure has successfully completed.
19	0h RO/V/P	**Equalization Phase 2 Successful (EQP2S):** Equalization Phase 2 Successful (EQP2S): When set to 1, this bit indicates that Phase 2 of the Transmitter Equalization procedure has successfully completed.
18	0h RO/V/P	**Equalization Phase 1 Successful (EQP1S):** Equalization Phase 1 Successful (EQP1S): When set to 1, this bit indicates that Phase 1 of the Transmitter Equalization procedure has successfully completed.
17	0h RO/V/P	**Equalization Complete (EQC):** Equalization Complete (EC): When set to 1, this bit indicates that the Transmitter Equalization procedure has completed
16	0h RO/V	**Current De-emphasis Level (CDL):** When the Link is operating at 5.0 GT/s speed, this bit reflects the level of de-emphasis. Encodings: 1b -3.5 dB 0b -6 dB The value in this bit is undefined when the Link is not operating at 5.0 GT/s speed.
15:12	0h RW/P	**Compliance Preset/De-emphasis (CD):** For 8.0 GT/s Data Rate: This field sets the Transmitter Preset in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Results are undefined if a reserved preset encoding is used when entering Polling.Compliance in this way. For 5.0 GT/s Data Rate: This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 0001b -3.5 dB 0000b -6 dB When the Link is not operating at 2.5 GT/s speed, the setting of this bit has no effect. The default value of this field is 0000b. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this field is set to the default value.
11	0h RW/P	**Compliance SOS (CSOS):** When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. The default value of this bit is 0b. This bit is applicable when the Link is operating at 2.5 GT/s or 5.0 GT/s data rates only. Register Attribute: Static.
10	0h RW/P	**Enter Modified Compliance (EMC):** When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Default value of this bit is 0b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.

Bit Range	Default & Access	Field Name (ID): Description
9:7	0h RW/P	**Transmit Margin (TM):** This field controls the value of the nondeemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate (see PCI Express Chapter 4 for details of how the Transmitter voltage level is determined in various states). Encodings: 000b Normal operating range 001b 800-1200 mV for full swing and 400-700 mV for half-swing 010b - (n-1) Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n : 200-400 mV for full-swing and 100-200 mV for half-swing n - 111b reserved For a Multi-Function device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. Default value of this field is 000b. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 000b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.
6	0h RW/P	**Selectable De-emphasis (SD):** When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. Encodings: 1b -3.5 dB 0b -6 dB When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect. When the Link is operating at 2.5 GT/s speed, the setting of this bit has no effect.
5	0h RO	**Hardware Autonomous Speed Disable (HASD):** Reserved. This port cannot autonomously change speeds.
4	0h RW/P	**Enter Compliance (EC):** Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value. Register Attribute: Static.
3:0	1h RW/V/P	**Target Link Speed (TLS):** Target Link Speed (TLS): This field sets an upper limit on Link operational speed by restricting the values advertised by the upstream component in its training sequences. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported 2.5 GT/s. 0010b: Supported 5 GT/s. 0011b: Supported 8 GT/s. All other encodings are reserved. If a value is written to this field that does not correspond to a supported speed, the result is undefined. The default value of this field is GEN1. Note: This register field could be used by REUT software to limit the link speed to 2.5 GT/s, 5 GT/s, or 8 GT/s data rate.

20.1.26 Message Signaled Interrupt Identifiers And Message Signaled Interrupt Message Control (MID_MC)—Offset 80h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 9005h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RO	**64-Bit Address Capable (C64):** Capable of generating a 32-bit message only.
22:20	0h RW	**Multiple Message Enable (MME):** These bits are RW for software compatibility, but only one message is ever sent by the root port.
19:17	0h RO	**Multiple Message Capable (MMC):** Only one message is required.
16	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. CMD.BME must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated.
15:8	90h RW/O	**Next Pointer (NEXT):** Indicates the location of the next capability in the list. The default value of this register is 90h which points to the Subsystem Vendor capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	5h RO	**Capability ID (CID):** Capabilities ID indicates MSI.

20.1.27 Message Signaled Interrupt Message Address (MA)—Offset 84h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Address (ADDR):** Lower 32 bits of the system specified message address, always DW aligned.
1:0	0h RO	Reserved.

20.1.28 Message Signaled Interrupt Message Data (MD)—Offset 88h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[lb]15:0[rb]) during the data phase of the MSI memory write transaction.

20.1.29 Subsystem Vendor Capability (SVCAP)—Offset 90h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: A00Dh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	A0h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability in the list. The default value of this register is A0h which points to the PCI Power Management capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	Dh RO	**Capability Identifier (CID):** Value of 0Dh indicates this is a PCI bridge subsystem vendor capability.

20.1.30 Subsystem Vendor IDs (SVID)—Offset 94h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem Identifier (SID):** Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).
15:0	0h RW/O	**Subsystem Vendor Identifier (SVID):** Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

20.1.31 Power Management Capability And PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: C8030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	19h RO	**PME Support (PMES):** Indicates PME# is supported for states D0, D3HOT and D3COLD. The root port does not generate PME#, but reporting that it does is necessary for legacy operating systems to enable PME# in devices connected behind this root port.
26	0h RO	**D2_Support (D2S):** The D2 state is not supported.
25	0h RO	**D1_Support (D1S):** The D1 state is not supported.
24:22	0h RO	**Aux_Current (AC):** Reports 375mA maximum suspend well current required when in the D3COLD state.
21	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
20	0h RO	Reserved.
19	0h RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
18:16	3h RO	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0h RO	**Next Capability (NEXT):** Indicates this is the last item in the list.
7:0	1h RO	**Capability Identifier (CID):** Value of 01h indicates this is a PCI power management capability.

20.1.32 PCI Power Management Control And Status (PMCS)—Offset A4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Data (DTA):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
23	0h RO	**Bus Power / Clock Control Enable (BPCE):** Reserved per PCI Express specification
22	0h RO	**B2/B3 Support (B23S):** Reserved per PCI Express specification.
21:16	0h RO	Reserved.
15	0h RO	**PME Status (PMES):** Indicates a PME was received on the downstream link.
14:13	0h RO	**Data Scale (DSC):** Reserved
12:9	0h RO	**Data Select (DSEL):** Reserved
8	0h RW/P	**PME Enable (PMEE):** Indicates PME is enabled. The root port takes no action on this bit, but it must be RW for legacy operating systems to enable PME# on devices connected to this root port.
7:4	0h RO	Reserved.
3	1h RW/O	**No Soft Reset (NSR):** When set to 1 this bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset. Configuration context is preserved. Upon transition from D3hot to D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the Power State bits. When clear, devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the Power State bits. Configuration Context is lost when performing the soft reset. Upon transition from D3hot to D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	Reserved.
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00 - D0 state 11 - D3HOT state When in the D3HOT state, the controller's configuration space is available, but the I/O and memory spaces are not. Type 1 configuration cycles are also not accepted. Interrupts are not required to be blocked as software will disable interrupts prior to placing the port into D3HOT. If software attempts to write a '10' or '01' to these bits, the write will be ignored.

20.1.33 Additional Configuration 1 (CCFG)—Offset D0h

BIOS may program this register.

20.1.34 Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Set to 000h as this is the last capability in the list. Point to the next capability.
19:16	0h RW/O	**Capability Version (CV):** For systems that support AER, BIOS should write a 1h to this register else it should write 0
15:0	0h RW/O	**Capability ID (CID):** For systems that support AER, BIOS should write a 0001h to this register else it should write 0

20.1.35 Uncorrectable Error Status (UES)—Offset 104h

This register must maintain its state through a platform reset. It loses its state upon loss of core power.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW/1C/V/P	**ACS Violation Status (AVS):** Indicates an ACS Violation is logged
20	0h RW/1C/V/P	**Unsupported Request Error Status (URE):** Indicates an unsupported request was received.
19	0h RO	**ECRC Error Status (EE):** ECRC is not supported.
18	0h RW/1C/V/P	**Malformed TLP Status (MT):** Indicates a malformed TLP was received.
17	0h RW/1C/V/P	**Receiver Overflow Status (RO):** Indicates a receiver overflow occurred.
16	0h RW/1C/V/P	**Unexpected Completion Status (UC):** Indicates an unexpected completion was received.
15	0h RW/1C/V/P	**Completor Abort Status (CA):** Indicates a completer abort was received
14	0h RW/1C/V/P	**Completion Timeout Status (CT):** Indicates a completion timed out. This is signaled if Completion Timeout is enabled and a completion fails to return within the amount of time specified by the Completion Timeout Value
13	0h RO	**Flow Control Protocol Error Status (FCPE):** Not supported.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C/V/P	**Poisoned TLP Status (PT):** Indicates a poisoned TLP was received.
11:6	0h RO	Reserved.
5	0h RO	**Surprise Down Error Status (SDE):** Surprise Down is not supported.
4	0h RW/1C/V/P	**Data Link Protocol Error Status (DLPE):** Indicates a data link protocol error occurred.
3:1	0h RO	Reserved.
0	0h RO	**Training Error Status (TE):** Not supported.

20.1.36 Uncorrectable Error Mask (UEM)—Offset 108h

When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW/P	**ACS Violation Mask (AVM):** Mask for ACS Violation errors
20	0h RW/P	**Unsupported Request Error Mask (URE):** Mask for uncorrectable errors.
19	0h RO	**ECRC Error Mask (EE):** ECRC is not supported.
18	0h RW/P	**Malformed TLP Mask (MT):** Mask for malformed TLPs
17	0h RW/P	**Receiver Overflow Mask (RO):** Mask for receiver overflows.
16	0h RW/P	**Unexpected Completion Mask (UC):** Mask for unexpected completions.
15	0h RW/P	**Completor Abort Mask (CM):** Mask for completer abort.
14	0h RW/P	**Completion Timeout Mask (CT):** Mask for completion timeouts.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	**Flow Control Protocol Error Mask (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Mask (PT):** Mask for poisoned TLPs.
11:6	0h RO	Reserved.
5	0h RO	**Surprise Down Error Mask (SDE):** Surprise Down is not supported.
4	0h RW/P	**Data Link Protocol Error Mask (DLPE):** Mask for data link protocol errors.
3:1	0h RO	Reserved.
0	0h RO	**Training Error Mask (TE):** Not supported.

20.1.37 Uncorrectable Error Severity (UEV)—Offset 10Ch

This register gives the option to make an uncorrectable error fatal or non-fatal. An error is fatal if the bit is set. An error is non-fatal if the bit is cleared. This register is only reset by a loss of core power.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 60011h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW/P	**ACS Violation Severity (AVS):** Severity for ACS violation.
20	0h RW/P	**Unsupported Request Error Severity (URE):** Severity for unsupported request reception.
19	0h RO	**ECRC Error Severity (EE):** ECRC is not supported.
18	1h RW/P	**Malformed TLP Severity (MT):** Severity for malformed TLP reception.
17	1h RW/P	**Receiver Overflow Severity (RO):** Severity for receiver overflow occurrences.
16	0h RW/P	**Unexpected Completion Severity (UC):** Severity for unexpected completion reception.
15	0h RW/P	**Completor Abort Severity (CA):** Severity for completer abort.
14	0h RW/P	**Completion Timeout Severity (CT):** Severity for completion timeout.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	**Flow Control Protocol Error Severity (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Severity (PT):** Severity for poisoned TLP reception.
11:6	0h RO	Reserved.
5	0h RO	**Surprise Down Error Severity (SDE):** Surprise Down is not supported.
4	1h RW/P	**Data Link Protocol Error Severity (DLPE):** Severity for data link protocol errors.
3:1	0h RO	Reserved.
0	1h RO	**Training Error Severity (TE):** TE not supported. This bit is left as RO='1' for ease of implementation..

20.1.38 Correctable Error Status (CES)—Offset 110h

This register is only reset by a loss of core power

Access Method

Type: CFG Register (Size: 32 bits)

Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	0h RW/1C/V/P	**Advisory Non-Fatal Error Status (ANFES):** When set, indicates that an Advisory Non-Fatal Error occurred.
12	0h RW/1C/V/P	**Replay Timer Timeout Status (RTT):** Indicates the replay timer timed out.
11:9	0h RO	Reserved.
8	0h RW/1C/V/P	**Replay Number Rollover Status (RNR):** Indicates the replay number rolled over.
7	0h RW/1C/V/P	**Bad DLLP Status (BD):** Indicates a bad DLLP was received.
6	0h RW/1C/V/P	**Bad TLP Status (BT):** Indicates a bad TLP was received.
5:1	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/1C/V/P	**Receiver Error Status (RE):** Indicates a receiver error occurred.

20.1.39 Correctable Error Mask (CEM)—Offset 114h

When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 28
Function:

Default: 2000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	1h RW/P	**Advisory Non-Fatal Error Mask (ANFEM):** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.
12	0h RW/P	**Replay Timer Timeout Mask (RTT):** Mask for replay timer timeout.
11:9	0h RO	Reserved.
8	0h RW/P	**Replay Number Rollover Mask (RNR):** Mask for replay number rollover.
7	0h RW/P	**Bad DLLP Mask (BD):** Mask for bad DLLP reception.
6	0h RW/P	**Bad TLP Mask (BT):** Mask for bad TLP reception.
5:1	0h RO	Reserved.
0	0h RW/P	**Receiver Error Mask (RE):** Mask for receiver errors.

20.1.40 Advanced Error Capabilities And Control (AECC)—Offset 118h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	0h RO	**Completion Timeout Prefix/Header Log Capable (CTPHLC):** If set, this bit indicates that port records the prefix/header of Request TLPs that experience a Completion Timeout error. Note: BIOS should program this bit before enable the Completion Timeout mechanism. Register Attribute: Static.
11:9	0h RO	Reserved.
8	0h RO	**ECRC Check Enable (ECE):** ECRC is not supported.
7	0h RO	**ECRC Check Capable (ECC):** ECRC is not supported.
6	0h RO	**ECRC Generation Enable (EGE):** ECRC is not supported.
5	0h RO	**ECRC Generation Capabile (EGC):** ECRC is not supported.
4:0	0h RO/V/P	**First Error Pointer (FEP):** Identifies the bit position of the first error reported in the Uncorrectable Error Status Register.

20.1.41 Root Error Command (REC)—Offset 12Ch

This register allows errors to generate interrupts.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW	**Fatal Error Reporting Enable (FERE):** When set, the root port will generate an interrupt when a fatal error is reported by the attached device.
1	0h RW	**Non-fatal Error Reporting Enable (NERE):** When set, the root port will generate an interrupt when a non-fatal error is reported by the attached device.
0	0h RW	**Correctable Error Reporting Enable (CERE):** When set, the root port will generate an interrupt when a correctable error is reported by the attached device.

20.1.42 Root Error Status (RES)—Offset 130h

This register can track more than one error and set the multiple bits if a second or subsequent error occurs and the first has not been serviced. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Advanced Error Interrupt Message Number (AEMN):** Reserved. There is only one error interrupt allocated.
26:7	0h RO	Reserved.
6	0h RW/1C/V/P	**Fatal Error Message Received (FEMR):** Set when one or more Fatal Uncorrectable Error Messages have been received.
5	0h RW/1C/V/P	**Non-Fatal Error Messages Received (NFEMR):** Set when one or more Non-Fatal Uncorrectable error messages have been received
4	0h RW/1C/V/P	**First Uncorrectable Fatal (FUF):** Set when the first Uncorrectable Error message received is for a fatal error.
3	0h RW/1C/V/P	**Multiple ERR_FATAL/NONFATAL Received (MENR):** Set when either a fatal or a non-fatal error is received and the ENR bit is already set.
2	0h RW/1C/V/P	**ERR_FATAL/NONFATAL Received (ENR):** Set when either a fatal or a non-fatal error message is received.
1	0h RW/1C/V/P	**Multiple ERR_COR Received (MCR):** Set when a correctable error message is received and the CR bit is already set.
0	0h RW/1C/V/P	**ERR_COR Received (CR):** Set when a correctable error message is received.

20.1.43 Error Source Identification (ESID)—Offset 134h

Size:32 bits
Identifies the source (Requester ID) of the first correctable and uncorrectable (Non-Fatal / Fatal) errors reported in the Root Error Status register. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO/V/P	**ERR_FATAL/NONFATAL Source Identification (EFNFSID):** Loaded with the Requester ID indicated in the received ERR_FATAL or ERR_NONFATAL Message with the ERR_FATAL/NONFATAL Received register is not already set.
15:0	0h RO/V/P	**ERR_COR Source Identification (ECSID):** Loaded with the Requester ID indicated in the received ERR_COR Message with the ERR_COR Received register is not already set.

20.1.44 L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h

Size: 32 bits
Note: When operating in Mobile Express mode, this capability should not be enabled.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.
19:16	0h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 1h
15:0	0h RW/O	**PCI Express Extended Capability ID (PCIEEC):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 001Eh.

20.1.45 L1 Sub-States Capabilities (L1SCAP)—Offset 204h

This is L1 Sub-States Capabilities register. Refer to register field for more details

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 28281Fh

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:19	5h RW/O	**Port Tpower_on Value (PTV):** Along with the Port T_POWER_ON Scale Field in the L1 Substates Capabilities register sets theTime (in us) that this Port requires the port on the opposite side of Link to wait in L1.OFF_EXIT after sampling CLKREQ# asserted before actively driving the interface. Port Tpower_on is calculated by multiplying the value in this field by the value in the Port Tpower_on scale field in the L1 Sub-States Capabilities 2 register. Required for all Ports that support L1.OFF.
18	0h RO	Reserved.
17:16	0h RW/O	**Port Tpower_on Scale (PTPOS):** Specifies the scale used for Tpower_on value field in the L1 Substates Capabilities register. 00b: 2us 01b: 10us 10b: 100us 11b: Reserved Required for all Ports that support L1.OFF.
15:8	28h RW/O	**Port Common Mode Restore Time (PCMRT):** This is the time (in us) required for this Port to re-establish common mode. Required for all ports that support L1.OFF.
7	0h RO	Reserved.
6	0h RW/1C/V	**L1-Substate Exit Interrupt Status (L1SSEIS):** CLKREQ# Acceleration Interrupt Status - For a Downstream Port that has both the CLKREQ# Acceleration Supported and CLKREQ# Acceleration Interrupt Enable bits Set, when set this bit indicates that the Port has completed the CLKREQ# Acceleration Link Activation process, and that the Link has reached L0. Software must then clear this bit by writing a 1b to this bit. Must be hardwired to 0b for Upstream Ports. Default value is 0b.
5	0h RW/O	**L1-Substate Exit Supported (L1SSES):** CLKREQ# Acceleration Supported - When set this bit indicates that this Port supports CLKREQ# Accelration (see [lt]Ref to Ch6 sect to be written!!![gt])
4	1h RW/O	**L1 PM Substates Supported (L1PSS):** When Set this bit indicates that this Port supports L1 PM Substates. For compatibility with possible future extensions, software must not enable L1 PM Substates unless this bit is set. This RWO field must be programmed prior to enabling ASPM. Required for both Upstream and Downstream Ports.
3	1h RW/O	**ASPM L1.1 Substates Supported (AL11S):** When set, this bit indicates that this port supports L1 substates for ASPM L1.SNOOZ is supported. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
2	1h RW/O	**ASPM L1.2 Supported (AL12S):** When set, this bit indicates that ASPM_L1.OFF is supported. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
1	1h RW/O	**PCI-PM L1.1 Supported (PPL11S):** When set, this bit indicates that L1.SNOOZ sub-state is supported and this bit must be set by all ports implementing L1 Sub-States. A port that supports L1.OFF must support L1.SNOOZ. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
0	1h RW/O	**PCI-PM L1.2 Supported (PPL12S):** When set, this bit indicates that PCI-PM L1.OFF power management feature is supported. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static

20.1.46 L1 Sub-States Control 1 (L1SCTL1)—Offset 208h

This is L1 Sub-States Control 1 register. Refer to register field for more details

Access Method

Type: CFG Register (Size: 32 bits)
Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**L1.2 LTR Threshold Latency ScaleValue (L12LTRTLSV):** This field contains the L1.OFF LTR Threshold Latency Scale Value for this particular PCIe Root Port. The value in this field, together with L12LTRTLV is compared against both the snoop and non-snoop LTR values of the device. 000: L12LTRSTLV times 1 ns 001: L12LTRSTLV times 32 ns 010: L12LTRSTLV times 1024 ns 011: L12LTRSTLV times 32768 ns 100: L12LTRSTLV times 1048576 ns 101: L12LTRSTLV times 33554432 ns Others: Not Permitted. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
28:26	0h RO	Reserved.
25:16	0h RW	**L1.2 LTR Threshold Latency Value (L12OFFLTRTLV):** This field contains the L1.2 LTR Threshold Latency Value for this particular PCIe Root Port. The value in this field, together with L12LTRTLSV is compared against both the snoop and non-snoop LTR values of the device. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
15:8	0h RW	**Common Mode Restore Time (CMRT):** This is the Tcommon_mode time (in us) the PCIe Root Port needs to continue sending TS1 and refrain from sending TS2 in Recovery state to allow the TX common mode to be established prior to sending TS2. The timer starts from the time when the first TS1 has been sent and the receiver has detected un-squelch. The value in this field defines the time in micro-seconds. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
7:4	0h RO	Reserved.
3	0h RW	**ASPM L1.1 Enabled (AL11E):** When set, this bit indicates that ASPM L1.SNOOZ substates are enabled for ASPM. Required for both upstream and downstream ports. Register Attribute: Dynamic
2	0h RW	**ASPM L1.2 Enable (AL12E):** When set, this bit indicates that ASPM L1.OFF substates are enabled for PCI-PM. Required for both upstream and downstream ports. Register Attribute: Dynamic.
1	0h RW	**PCI-PM L1.SNOOZ Enable (PPL11E):** When set, this bit indicates that PCI-PM L1.SNOOZ power management feature is enabled. If L1.OFF is enabled, L1.SNOOZ must also be enabled. This field must be programmed prior to enabling ASPM L1. Register Attribute: Dynamic

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**PCI-PM L1.2 Enabled (PPL12E):** When set, this bit indicates that PCI-PM L1.OFF power management feature is enabled. L1.OFF can only be enabled if the platform supports bi-directional CLKREQPLUS#. This field must be programmed prior to enabling ASPM L1. Ports that support L1.OFF shall support Latency Tolerance Reporting. Register Attribute: Dynamic

20.1.47 L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch

This is L1 Sub-States Control 2 register. Refer to register field for more details

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 28h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:3	5h RW	**Power On Wait Time (POWT):** Along with the Tpower_on Scale sets the minimum amount of time (in us) that the Port must wait in L1.OFF EXIT after sampling CLKREQPLUS# asserted before actively driving the interface. The timer starts counting when CLKREQPLUS# is sampled asserts in L1.OFF state. Tpower_on value is calculated by multiplying the value in this field by the value in the TPOS field. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
2	0h RO	Reserved.
1:0	0h RW	**Tpower_on Scale (TPOS):** Specifies the scale used for Tpower_on value. 00b: 2 us 01b: 10 us 10b: 100us 11b: Reserved. Required for all Ports that support L1.OFF. Register Attribute: Static

20.1.48 ACS Extended Capability Header (ACSECH)—Offset 220h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): For systems that support ACS Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0h RW/O	**Capability ID (CID):** Capability ID (CID): For systems that support ACS Extended Capability, BIOS should write a 000Dh to this register else it should write 0.

20.1.49 ACS Capability Register And ACS Control Register (ACSCAPR_ACSCTLR)—Offset 224h

This is ACS Capability Register and ACS Control register. Refer to register field for more details

Access Method

Type: CFG Register (Size: 32 bits)

Device: 28

Function:

Default: 1Fh

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22	0h RO	**ACS Direct Translated P2P Enable (TE):** ACS Direct Translated P2P Enable (T): ACS Direct Translated P2P is not supported.
21	0h RO	**ACS P2P Egress Control Enable (EE):** ACS P2P Egress Control Enable (E): ACS P2P Egress Control is not supported.
20	0h RW	**ACS Upstream Forwarding Enable (UE):** When set, the component forwards upstream any Request or Completion TLPs it receives that were redirected upstream by a component lower in the hierarchy. Note that the U bit only applies to upstream TLPs arriving at a Downstream Port, and whose normal routing targets the same Downstream Port. Upstream I/O, Configuration, VDM Message, Message are never affected by ACS Upstream Forwarding Enable. Register Attribute: Static
19	0h RW	**ACS P2P Completion Redirect Enable (CE):** ACS P2P Completion Redirect (C): Determines when the component redirects peer-to-peer Completions upstream; applicable only to Read Completions whose Relaxed Ordering Attribute is clear. Requests are never affected by ACS P2P Completion Redirect. Default value of this field is 0b. Register Attribute: Static.
18	0h RW	**ACS P2P Request Redirect Enable (RE):** ACS P2P Request Redirect Enable (R): Determines when the component redirects peer-to-peer memory Requests targeting another peer port upstream. I/O, Configuration, VDM Messages and Completions are never affected by ACS P2P Request Redirect. Default value of this field is 0b. Register Attribute: Static.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**ACS Translation Blocking Enable (BE):** ACS Translation Blocking Enable (B): When set, the component blocks all upstream Memory Requests whose Address Translation (AT) field is not set to the default value. I/O, Configuration, Completions and Messages are never affected by ACS Translation Blocking. Default value of this field is 0b. Register Attribute: Static.
16	0h RW	**ACS Source Validation Enable (VE):** ACS Source Validation Enable (V): When set, the component validates the Bus Number from the Requester ID of upstream Requests against the secondary / subordinate Bus Numbers. I/O, Configuration and Completions are never affected by ACS Source Validation. Default value of this field is 0b. Register Attribute: Static.
15:7	0h RO	Reserved.
6	0h RO	**ACS Direct Translated P2P (T):** ACS Direct Translated P2P (T): ACS Direct Translated P2P is not supported.
5	0h RO	**ACS P2P Egress Control (E):** ACS P2P Egress Control (E): ACS P2P Egress Control is not supported.
4	1h RW/O	**ACS Upstream Forwarding (U):** Required for Root Ports if the RC supports Redirected Request Validation: required for Switch Downstream Ports: must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Upstream Forwarding Register Attribute: Static
3	1h RW/O	**ACS P2P Completion Redirect (C):** ACS P2P Completion Redirect (C): Required for all Functions that support ACS P2P Request Redirect; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Completion Redirect. Register Attribute: Static.
2	1h RW/O	**ACS P2P Request Redirect (R):** ACS P2P Request Redirect (R): Required for Root Ports that support peer-to-peer traffic with other Root Ports; required for Switch Downstream Ports; required for multi-function device Functions that support peer-to-peer traffic with other Functions; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Request Redirect. Register Attribute: Static.
1	1h RW/O	**ACS Translation Blocking (B):** ACS Translation Blocking (B): Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Translation Blocking. Register Attribute: Static.
0	1h RW/O	**ACS Source Validation (V):** ACS Source Validation (V): Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Source Validation. Register Attribute: Static.

21 I2C Interface (D25: F0-F1, D21:F0-F3)

21.1 I2C PCI Configuration Registers

Table 21-1. Summary of I2C PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device ID and Vendor ID (DEVVENDID)—Offset 0h	XXXX8086h
4h	7h	Status and Command (STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	Revision ID and Class Code (REVCLASSCODE)—Offset 8h	C8000XXh
Ch	Fh	Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch	800000h
10h	13h	Base Address (BAR)—Offset 10h	4h
14h	17h	Base Address Register High (BAR_HIGH)—Offset 14h	0h
18h	1Bh	Base Address 1 (BAR1)—Offset 18h	4h
1Ch	1Fh	Base Address 1 High (BAR1_HIGH)—Offset 1Ch	0h
2Ch	2Fh	Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch	0h
34h	37h	Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	Interrupt Register (INTERRUPTREG)—Offset 3Ch	0h
80h	83h	Power Management Capability ID (POWERCAPID)—Offset 80h	39001h
84h	87h	Power Management Control and Status (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
98h	9Bh	SW LTR update MMIO Location (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	2101h
9Ch	9Fh	Device IDLE Pointer (DEVICE_IDLE_POINTER_REG)—Offset 9Ch	24C1h
A0h	A3h	Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	F0800h
B0h	B3h	General Purpose Read Write 1 (GEN_REGRW1)—Offset B0h	0h
B4h	B7h	General Purpose PCI Read Write 2 (GEN_REGRW2)—Offset B4h	0h
B8h	BBh	General Purpose PCI Read Write 3 (GEN_REGRW3)—Offset B8h	0h
BCh	BFh	General Purpose PCI Read Write 4 (GEN_REGRW4)—Offset BCh	0h
C0h	C3h	General Purpose Input (GEN_INPUT_REG)—Offset C0h	0h

21.1.1 Device ID and Vendor ID (DEVVENDID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: XXXX8086h

Bit Range	Default and Access	Field Name (ID): Description
31:16	-- RO/P	**Device ID Field (DEVICEID):** This is a 16-bit value assigned to the controller. Refer the Device and Revision ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor ID Field (VENDORID):** Identifies the manufacturer of the device. 8086h = Intel.

21.1.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 100000h

Bit Range	Default and Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW/1C	**RMA Field (RMA):** S/W writes a '1' to this bit to clear it.
28	0h RW/1C	**RTA Field (RTA):** S/W writes a '1' to this bit to clear it.
27:21	0h RO	Reserved.
20	1h RO	**Cap List Field (CAPLIST):** Indicates that the controller contains a capabilities pointer list.
19	0h RO	**Intrerrupt Status Field (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit is a 0 and this Interrupt Status bit is a 1, will the device's/function's interrupt message be sent. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** Setting this bit disables INTx assertion. The interrupt disabled is legacy INTx# interrupt. This bit has no connection with interrupt status bit.
9	0h RO	Reserved.
8	0h RW	**SERR Enable Field (SERR_ENABLE):** Not implemented.
7:3	0h RO	Reserved.
2	0h RW	**BME Field (BME):** If this bit is 0, the controller does not generate any new upstream transaction as a Initiator.
1	0h RW	**MSE Field (MSE):** 0 = Disables memory mapped Configuration space. 1 = Enables memory mapped Configuration space.

Bit Range	Default and Access	Field Name (ID): Description
0	0h RO	Reserved.

21.1.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: C8000XXh

Bit Range	Default and Access	Field Name (ID): Description
31:8	C8000h RO	**Class Code (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	-- RO/P	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

21.1.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 800000h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	1h RO	**MultiFunction Device Field (MULFNDEV):** 0 = Single Function Device 1 = Multi Function device
22:16	0h RO	**Header Type Field (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	0h RO	**Latency Timer Field (LATTIMER):** Hardwired to 0.
7:0	0h RW/P	**Cache Line Size Field (CACHELINE_SIZE)**

21.1.5 Base Address (BAR)—Offset 10h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:12	0h RW	**Base Address Field (BASEADDR):** Provides system memory base address for the controller.
11:4	0h RO	**Size Field (SIZEINDICATOR):** Always returns 0. The size of this register depends on the size of the memory space.
3	0h RO	**Prefetchable Field (PREFETCHABLE):** 0 indicates that this BAR is not prefetchable.
2:1	2h RO	**Type Field (TYPE):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** 0 indicates this BAR is present in the memory space.

21.1.6 Base Address Register High (BAR_HIGH)—Offset 14h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Base Address High Field (BASEADDR_HIGH)**

21.1.7 Base Address 1 (BAR1)—Offset 18h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:12	0h RW	**Base Address Field (BASEADDR1):** This field is present if BAR1 is enabled.
11:4	0h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** 0 indicates that this BAR is not prefetchable.
2:1	2h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** 0 Indicates this BAR is present in the memory space.

21.1.8 Base Address 1 High (BAR1_HIGH)—Offset 1Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Base Address High Field (BASEADDR1_HIGH)**

21.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RW/O/P	**Subsystem ID Field (SUBSYSTEMID):** The register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one subsystem from the other. This register is a Read Write Once type register.
15:0	0h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** The register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

21.1.10 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Capabilities Pointer register indicates what the next capability is

Access Method

Type: CFG Register (Size: 32 bits)
Device: 21
Function: 0

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Indicates what the next capability is.

21.1.11 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: CFG Register (Size: 32 bits)
Device: 21
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**Min Gnt Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers // Re-Check Desc Padma
15:12	0h RO	Reserved.
11:8	0h RO	**Interrupt Pin Field (INTPIN)**
7:0	0h RW/P	**Int Line Field (INTLINE):** It is used to communicate to software, the interrupt line to which the interrupt pin is connected.

21.1.12 Power Management Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 21
Function: 0

Default: 39001h

Bit Range	Default and Access	Field Name (ID): Description
31:27	0h RO	**PME Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for for a bit indicates that the function is not capable of asserting the PME# signal while in that power state. Bit 27 = 1: PME# can be asserted from D0. Bit 30 = 1: PME# can be asserted from D3 hot. Other bits are not used.
26:19	0h RO	Reserved.
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	90h RO	**Next Cap Field (NXTCAP):** Points to the next capability structure.
7:0	1h RO	**Power Capability ID Field (POWER_CAP):** Indicates power management capability.

21.1.13 Power Management Control and Status (PMECTRLSTATUS)—Offset 84h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C/P	**PME Status Field (PMESTATUS)**
14:9	0h RO	Reserved.
8	0h RW/P	**PME Enable Field (PMEENABLE):** 0 = PME message is disabled 1 = PME message is enabled.
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	0h RO	Reserved.
1:0	0h RW	**Power State Field (POWERSTATE):** This field is used both to determine the current power state and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field,the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked.

21.1.14 PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: F0140009h

Bit Range	Default and Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision IDField (REVID):** Revision ID of capability structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	0h RO	**Next Capability Field (NEXT_CAP):** Points to the next capability structure. This points to NULL.
7:0	9h RO	**Capability ID Field (CAPID)**

21.1.15 SW LTR update MMIO Location (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

Software location pointer in MMIO space as an offset specified by BAR

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 2101h

Bit Range	Default and Access	Field Name (ID): Description
31:4	210h RO	**SW LTR Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR BAR Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	1h RO	**SW LTR Valid Field (SW_LAT_VALID)**

21.1.16 Device IDLE Pointer (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Device IDLE pointer register giving details on Device MMIO offset location BAR NUM and D0i3 Valid Strap

Access Method

Type: CFG Register (Size: 32 bits)

Device: 21
Function: 0

Default: 24C1h

Bit Range	Default and Access	Field Name (ID): Description
31:4	24Ch RO	**D0i3 Dword Offset Field (DWORD_OFFSET):** contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR NUM Field (BAR_NUM):** Indicates that the D0i3 MMIO location is always at BAR0.
0	1h RO	**D0i3 Valid Field (VALID):** 0 = Not valid 1 = Valid

21.1.17 Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 21
Function: 0

Default: F0800h

Bit Range	Default and Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19	1h RW/P	**Sleep Enable Field (SLEEP_EN)**
18	1h RW/P	**D3 Hen Field (PGE):** If clear, the controller will never request a PG. If 1, then the function will power gate when idle and the DevIdle bit is set.
17	1h RW/P	**Device Idle En Field (I3_ENABLE):** If 1, then function will power gate when idle and the POWERSTATE bits in the function = 11 (D3).
16	1h RW/P	**PMC Request Enable Field (PMCRE):** If this bit is set to '1', the function will power gate when idle.
15:13	0h RO	Reserved.
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** This value is written by BIOS to communicate to the Driver.

Bit Range	Default and Access	Field Name (ID): Description
9:0	0h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** This value is written by BIOS to communicate to the Driver.

21.1.18 General Purpose Read Write 1 (GEN_REGRW1)—Offset B0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Field (GEN_REG_RW1):** General purpose read write PCI register.

21.1.19 General Purpose PCI Read Write 2 (GEN_REGRW2)—Offset B4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Field (GEN_REG_RW2):** General purpose read write PCI register.

21.1.20 General Purpose PCI Read Write 3 (GEN_REGRW3)—Offset B8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Field (GEN_REG_RW3):** General purpose read write PCI register.

21.1.21 General Purpose PCI Read Write 4 (GEN_REGRW4)—Offset BCh

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Field (GEN_REG_RW4):** General purpose read write PCI register.

21.1.22 General Purpose Input (GEN_INPUT_REG)—Offset C0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO	**General Purpose Input Field (GEN_REG_INPUT_RW):** General purpose input register.

21.2 I2C Memory Mapped Registers

The registers in this section are memory-mapped registers based on the BAR defined in PCH Configuration space.

Table 21-2. Summary of I2C Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	I2C Control (IC_CON)—Offset 0h	77h
4h	7h	I2C Target Address (IC_TAR)—Offset 4h	1055h
Ch	Fh	I2C High Speed Initiator Mode Code Address (IC_HS_MADDR)—Offset Ch	1h
10h	13h	Rx/Tx Data Buffer and Command (IC_DATA_CMD)—Offset 10h	0h

Table 21-2. Summary of I2C Memory Mapped Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
14h	17h	Standard Speed I2C Clock SCL High Count (IC_SS_SCL_HCNT)—Offset 14h	1F4h
18h	1Bh	Standard Speed I2C Clock SCL Low Count (IC_SS_SCL_LCNT)—Offset 18h	24Ch
1Ch	1Fh	Fast Speed I2C Clock SCL High Count (IC_FS_SCL_HCNT)—Offset 1Ch	4Bh
20h	23h	Fast Speed I2C Clock SCL Low Count (IC_FS_SCL_LCNT)—Offset 20h	A3h
24h	27h	High Speed I2C Clock SCL High Count (IC_HS_SCL_HCNT)—Offset 24h	8h
28h	2Bh	High Speed I2C Clock SCL Low Count (IC_HS_SCL_LCNT)—Offset 28h	14h
2Ch	2Fh	I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch	0h
30h	33h	Interrupt Mask Register (IC_INTR_MASK)—Offset 30h	8FFh
34h	37h	Raw Interrupt Status (IC_RAW_INTR_STAT)—Offset 34h	0h
38h	3Bh	Receive FIFO Threshold (IC_RX_TL)—Offset 38h	0h
3Ch	3Fh	Transmit FIFO Threshold (IC_TX_TL)—Offset 3Ch	0h
40h	43h	Clear Combined and Individual Interrupt (IC_CLR_INTR)—Offset 40h	0h
44h	47h	Clear RX_UNDER Interrupt (IC_CLR_RX_UNDER)—Offset 44h	0h
48h	4Bh	Clear RX_OVER Interrupt (IC_CLR_RX_OVER)—Offset 48h	0h
4Ch	4Fh	Clear TX_OVER Interrupt (IC_CLR_TX_OVER)—Offset 4Ch	0h
50h	53h	Clear RD_REQ Interrupt (IC_CLR_RD_REQ)—Offset 50h	0h
54h	57h	Clear TX_ABRT Interrupt (IC_CLR_TX_ABRT)—Offset 54h	0h
58h	5Bh	Clear RX_DONE Interrupt (IC_CLR_RX_DONE)—Offset 58h	0h
5Ch	5Fh	Clear ACTIVITY Interrupt (IC_CLR_ACTIVITY)—Offset 5Ch	0h
60h	63h	Clear STOP_DET Interrupt (IC_CLR_STOP_DET)—Offset 60h	0h
64h	67h	Clear START_DET Interrupt (IC_CLR_START_DET)—Offset 64h	0h
68h	6Bh	Clear GEN_CALL Interrupt (IC_CLR_GEN_CALL)—Offset 68h	0h
6Ch	6Fh	I2C Enable (IC_ENABLE)—Offset 6Ch	0h
70h	73h	I2C Status (IC_STATUS)—Offset 70h	6h
74h	77h	I2C Transmit FIFO Level (IC_TXFLR)—Offset 74h	0h
78h	7Bh	Receive FIFO Level (IC_RXFLR)—Offset 78h	0h
7Ch	7Fh	SDA Hold Time Length (IC_SDA_HOLD)—Offset 7Ch	1h
80h	83h	Transmit Abort Source (IC_TX_ABRT_SOURCE)—Offset 80h	0h
88h	8Bh	DMA Control (IC_DMA_CR)—Offset 88h	0h
8Ch	8Fh	DMA Transmit Data Level (IC_DMA_TDLR)—Offset 8Ch	0h
90h	93h	Receive Data Level (IC_DMA_RDLR)—Offset 90h	0h
98h	9Bh	ACK General Call (IC_ACK_GENERAL_CALL)—Offset 98h	1h
9Ch	9Fh	I2C Enable Status (IC_ENABLE_STATUS)—Offset 9Ch	0h
A0h	A3h	SS and FS Spike Suppression Limit (IC_FS_SPKLEN)—Offset A0h	7h

21.2.1 I2C Control (IC_CON)—Offset 0h

I2C Control Register

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 77h

Bit Range	Default and Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**TX_EMPTY_CTRL (TX_EMPTY_CTRL):** This bit controls the generation of the TX_EMPTY interrupt, as described in the IC_RAW_INTR_STAT register.
7	0h RO	Reserved.
6	1h RW	**IC_Target_DISABLE (IC_Target_DISABLE):** This bit controls whether I2C has its Target disabled. If this bit is set (Target is disabled), the function only works as a Initiator and does not perform any action that requires a Target. 0:Reserved 1: Target is disabled
5	1h RW	**IC_RESTART_EN (IC_RESTART_EN):** Determines whether RESTART conditions may be sent when I2C is acting as a Initiator. 0: Restart disable 1: Restart enable When the RESTART is disabled, the IP is incapable of performing the following functions: • Sending a START BYTE • Performing any high-speed mode operation • Performing direction changes in combined format mode • Performing a read operation with a 10-bit address By replacing RESTART condition followed by a STOP and a subsequent START condition, split operations are broken down into multiple transfers. If the above operations are performed, it will result in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register.
4	1h RO	**IC_10BITADDR_Initiator_rd_only (IC_10BITADDR_Initiator_rd_only):** Identifies if I2C operates in 7 or 10 bit addressing. 0: 7-bit addressing 1: 10-bit addressing
3	0h RO	Reserved.
2:1	3h RW	**SPEED (SPEED):** These bits control at which speed the I2C operates. 01: standard mode (0 to 100 kbit/s) 10: fast mode (<= 400 kbit/s) 11: High Speed Mode (<= 3.4 Mbit/s)
0	1h RW	**Initiator_MODE (Initiator_MODE):** This bit controls whether I2C Initiator is enabled. 0 = Reserved 1 = Initiator Enabled Note: For Initiator Device Configuration Software must ensure that this bit is set to 1, and bit 6 must also be set to 1. Else this will result in configuration error.

21.2.2 I2C Target Address (IC_TAR)—Offset 4h

The register should only be updated when the I2C is not enabled (IC_ENABLE=0) or No Initiator mode operations are active (IC_STATUS[5] = 0 and IC_CON[0] = 1 and IC_STATUS[2] = 1).

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 1055h

Bit Range	Default and Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	1h RW	**IC_10BITADDR_Initiator (IC_10BITADDR_Initiator):** This bit controls whether the I2C starts its transfers in 7-or 10-bit addressing mode when acting as a Initiator. 0: 7 bit addressing 1: 10-bit addressing
11	0h RW	**SPECIAL (SPECIAL):** This bit indicates whether software performs a General Call or START BYTE command. 0: ignore bit 10 GC_OR_START and use IC_TAR normally. 1: perform special I2C command as specified in GC_OR_START bit.
10	0h RW	**GC_OR_START (GC_OR_START):** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call or START byte command is to be performed by the I2C. 0: General Call Address – after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. The I2C remains in General Call mode until the SPECIAL bit value (bit 11) is cleared. 1: START BYTE
9:0	55h RW	**IC_TAR (IC_TAR):** This is the target address for any Initiator transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.

21.2.3 I2C High Speed Initiator Mode Code Address (IC_HS_MADDR)—Offset Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2:0	1h RW	**IC_HS_MAR (IC_HS_MAR):** This bit field holds the value of the I2C HS mode Initiator code. HS-mode Initiator codes are reserved 8-bit codes (00001xxx) that are not used for Target addressing or other purposes. Each Initiator has its unique Initiator code; up to eight highspeed mode Initiators can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0s if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2).

21.2.4 Rx/Tx Data Buffer and Command (IC_DATA_CMD)—Offset 10h

I2C Data Command Register

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:11	0h RO	Reserved.
10	0h WO	**RESTART (RESTART):** This bit controls whether a RESTART is issued before the byte is sent or received. 1: a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command. 0: a RESTART is issued only if the transfer direction is changing from the previous command.
9	0h WO	**STOP (STOP):** This bit controls whether a STOP is issued after the byte is sent or received. 1: STOP is issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the Initiator immediately tries to start a new transfer by issuing a START and arbitrating for the bus. 0: STOP is not issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the Initiator continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the Initiator holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO.
8	0h WO	**CMD (CMD):** This bit controls whether a read or a write is performed. 1 = Read. 0 = Write When a command is entered in the TX FIFO, this bit distinguishes the write and read commands. In Target-receiver mode, this bit is a do not care because writes to this register are not required. In Target-transmitter mode, a 0 indicates that the data in IC_DATA_CMD is to be transmitted. When programming this bit, note the following: attempting to perform a read operation after a General Call command has been sent results in a TX_ABRT interrupt (bit 6 of the IC_RAW_INTR_STAT register), unless bit 11 (SPECIAL) in the IC_TAR register has been cleared. If a "1" is written to this bit after receiving a RD_REQ interrupt, then a TX_ABRT interrupt occurs.
7:0	0h RW	**DAT (DAT):** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the I2C. However, when you read this register, these bits return the value of data received on the I2C interface.

21.2.5 Standard Speed I2C Clock SCL High Count (IC_SS_SCL_HCNT)—Offset 14h

This register sets the SCL clock high-period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The register is only used in Initiator mode.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 1F4h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	1F4h RW	**IC_SS_SCL_HCNT (IC_SS_SCL_HCNT):** This register sets the SCL clock high-period count for standard speed. The value of the registers should be within the range {6, 65525}.

21.2.6 Standard Speed I2C Clock SCL Low Count (IC_SS_SCL_LCNT)—Offset 18h

This register sets the SCL clock low-period countfor standard speed.. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 24Ch

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	24Ch RW	**IC_SS_SCL_LCNT (IC_SS_SCL_LCNT):** Standard Speed I2C Clock SCL Low Count Register. The register value should always be >= 8

21.2.7 Fast Speed I2C Clock SCL High Count (IC_FS_SCL_HCNT)—Offset 1Ch

Fast Speed I2C Clock SCL High Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 4Bh

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	4Bh RW	**IC_FS_SCL_HCNT (IC_FS_SCL_HCNT):** This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Initiator Code and START BYTE or General CALL.. The minimum value of this field is 6.

21.2.8 Fast Speed I2C Clock SCL Low Count (IC_FS_SCL_LCNT)—Offset 20h

Fast Speed I2C Clock SCL Low Count Register. This register must be set before any I2C bus transaction can take place to ensure proper I/O timing.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: A3h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	A3h RW	**IC_FS_SCL_LCNT (IC_FS_SCL_LCNT):** This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Initiator Code and START BYTE or General CALL. The register should be programmed with a minimum value of 8.

21.2.9 High Speed I2C Clock SCL High Count (IC_HS_SCL_HCNT)—Offset 24h

High Speed I2C Clock SCL High Count Register. This register must be set before any I2C bus transaction can take place to ensure proper I/O timing.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	8h RW	**IC_HS_SCL_HCNT (IC_HS_SCL_HCNT):** This register sets the SCL clock high period count for high speed.

21.2.10 High Speed I2C Clock SCL Low Count (IC_HS_SCL_LCNT)—Offset 28h

High Speed I2C Clock SCL Low Count Register. This register must be set before any I2C bus transaction can take place to ensure proper I/O timing.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 14h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	14h RW	**IC_HS_SCL_LCNT (IC_HS_SCL_LCNT):** This register sets the SCL clock low period count for high speed.

21.2.11 I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch

I2C Interrupt Status Register. Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	0h RO	**R_Initiator_ON_HOLD (R_Initiator_ON_HOLD):** Indicates whether a Initiator is holding the bus and the TX FIFO is empty. Enabled only when I2C_DYNAMIC_TAR_UPDATE = 1 and IC_EMPTYFIFO_HOLD_Initiator_EN = 1
12	0h RO	Reserved.
11	0h RO	**R_GEN_CALL (R_GEN_CALL):** Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling the controller or when the processor reads bit 0 of the IC_CLR_GEN_CALL register
10	0h RO	**R_START_DET (R_START_DET):** Indicates whether a START or RESTART condition has occurred on the I2C interface.
9	0h RO	**R_STOP_DET (R_STOP_DET):** Indicates whether a STOP condition has occurred on the I2C interface.

Bit Range	Default and Access	Field Name (ID): Description
8	0h RO	**R_ACTIVITY (R_ACTIVITY):** This bit captures the controller activity and stays set until it is cleared. There are four ways to clear it: 1. Disabling the controller, 2. Reading the IC_CLR_ACTIVITY register, 3. Reading the IC_CLR_INTR register, 4. System reset Note: Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the controller is idle, this bit remains set until cleared, indicating that there was activity on the bus.
7	0h RO	Reserved.
6	0h RO	**R_TX_ABRT (R_TX_ABRT):** This bit indicates if the controler, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. When this bit is set to 1, the IC_TX_ABRT_SOURCE register indicates the reason why the transmit abort takes places. NOTE: The controller flushes/resets/empties the TX FIFO whenever this bit is set. The TX FIFO remains in this flushed state until the register IC_CLR_TX_ABRT is read. Once this read is performed, the TX FIFO is then ready to accept more data bytes.
5	0h RO	Reserved.
4	0h RO	**R_TX_EMPTY (R_TX_EMPTY):** The behavior of the TX_EMPTY interrupt status differs based on the TX_EMPTY_CTRL selection in the IC_CON register. When TX_EMPTY_CTRL = 0: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register. When TX_EMPTY_CTRL = 1: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register and the transmission of the address/data from the internal shift register for the most recently popped command is completed. It is automatically cleared by hardware when the buffer level goes above the threshold. When IC_ENABLE[0] is set to 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the Initiator or Target state machines. When there is no longer any activity, then with ic_en=0, this bit is set to 0.
3	0h RO	**R_TX_OVER (R_TX_OVER):** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register. When the module is disabled, this bit keeps its level until the Initiator or Target state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.
2	0h RO	**R_RX_FULL (R_RX_FULL):** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (IC_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the IC_ENABLE bit 0 is programmed with a 0, regardless of the activity that continues.
1	0h RO	**R_RX_OVER (R_RX_OVER):** Set if the receive buffer is completely filled to IC_RX_BUFFER_DEPTH and an additional byte is received from an external I2C device. The controller acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the Initiator goes into idle, and when ic_en goes to 0, this interrupt is cleared.
0	0h RO	**R_RX_UNDER (R_RX_UNDER):** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the Initiator or Target state machines go into idle, and when ic_en goes to 0, this interrupt is cleared

21.2.12 Interrupt Mask Register (IC_INTR_MASK)—Offset 30h

These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register

Access Method

Type: MEM Register (Size: 32 bits)

Device:

Function:

Default: 8FFh

Bit Range	Default and Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	0h RW	**M_Initiator_ON_HOLD (M_Initiator_ON_HOLD):** This bit masks the R_MST_ON_HOLD interrupt bit in the IC_INTR_STAT register.
12	0h RO	Reserved.
11	1h RW	**M_GEN_CALL (M_GEN_CALL):** M_GEN_CALL_field
10	0h RW	**M_START_DET (M_START_DET):** M_START_DET_field
9	0h RW	**M_STOP_DET (M_STOP_DET):** M_STOP_DET_field
8	0h RW	**M_ACTIVITY (M_ACTIVITY):** M_ACTIVITY_field
7	1h RW	**M_RX_DONE (M_RX_DONE):** M_RX_DONE_field
6	1h RW	**M_TX_ABRT (M_TX_ABRT):** M_TX_ABRT_field
5	1h RW	**M_RD_REQ (M_RD_REQ):** M_RD_REQ_field
4	1h RW	**M_TX_EMPTY (M_TX_EMPTY):** M_TX_EMPTY_field
3	1h RW	**M_TX_OVER (M_TX_OVER):** M_TX_OVER_field
2	1h RW	**M_RX_FULL (M_RX_FULL):** M_RX_FULL_field
1	1h RW	**M_RX_OVER (M_RX_OVER):** M_RX_OVER_field
0	1h RW	**M_RX_UNDER (M_RX_UNDER):** M_RX_UNDER_field

21.2.13 Raw Interrupt Status (IC_RAW_INTR_STAT)—Offset 34h

Unlike the IC_INTR_STAT register, these bits are not masked so they always show the true status of the controller.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	0h RO	**Initiator_ON_HOLD (Initiator_ON_HOLD):** Same as in reg_IC_INTR_STAT
12	0h RO	Reserved.
11	0h RO	**GEN_CALL (GEN_CALL):** Same as in reg_IC_INTR_STAT
10	0h RO	**START_DET (START_DET):** Same as in reg_IC_INTR_STAT
9	0h RO	**STOP_DET (STOP_DET):** Same as in reg_IC_INTR_STAT
8	0h RO	**RAW_INTR_ACTIVITY (RAW_INTR_ACTIVITY):** Same as in reg_IC_INTR_STAT
7	0h RO	**RX_DONE (RX_DONE):** Same as in reg_IC_INTR_STAT
6	0h RO	**TX_ABRT (TX_ABRT):** Same as in reg_IC_INTR_STAT
5	0h RO	**RD_REQ (RD_REQ):** Same as in reg_IC_INTR_STAT
4	0h RO	**TX_EMPTY (TX_EMPTY):** Same as in reg_IC_INTR_STAT
3	0h RO	**TX_OVER (TX_OVER):** Same as in reg_IC_INTR_STAT
2	0h RO	**RX_FULL (RX_FULL):** Same as in reg_IC_INTR_STAT
1	0h RO	**RX_OVER (RX_OVER):** Same as in reg_IC_INTR_STAT
0	0h RO	**RX_UNDER (RX_UNDER):** Same as in reg_IC_INTR_STAT

21.2.14 Receive FIFO Threshold (IC_RX_TL)—Offset 38h

I2C Receive FIFO Threshold Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**RX_TL (RX_TL):** Receive FIFO Threshold Level. Controls the level of entries (or above) that triggers the RX_FULL interrupt (bit 2 in IC_RAW_INTR_STAT register). The valid range is 0-0x3F. (Values > 0x3F are set to depth of the buffer). A value of 0 sets the threshold for 1 entry, and a value of 63 sets the threshold for 64 entries.

21.2.15 Transmit FIFO Threshold (IC_TX_TL)—Offset 3Ch

I2C Transmit FIFO Threshold Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**TX_TL (TX_TL):** Transmit FIFO Threshold Level Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 0 entries, and a value of 255 sets the threshold for 255 entries.

21.2.16 Clear Combined and Individual Interrupt (IC_CLR_INTR)—Offset 40h

Clear Combined and Individual Interrupt Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_INTR (CLR_INTR):** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.

21.2.17 Clear RX_UNDER Interrupt (IC_CLR_RX_UNDER)—Offset 44h

Clear RX_UNDER Interrupt Register

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_RX_UNDER (CLR_RX_UNDER):** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

21.2.18 Clear RX_OVER Interrupt (IC_CLR_RX_OVER)—Offset 48h

Clear RX_OVER Interrupt Register

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_RX_OVER (CLR_RX_OVER):** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

21.2.19 Clear TX_OVER Interrupt (IC_CLR_TX_OVER)—Offset 4Ch

Clear TX_OVER Interrupt Register

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_TX_OVER (CLR_TX_OVER):** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

21.2.20 Clear RD_REQ Interrupt (IC_CLR_RD_REQ)—Offset 50h

Clear RD_REQ Interrupt Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_RD_REQ (CLR_RD_REQ):** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register

21.2.21 Clear TX_ABRT Interrupt (IC_CLR_TX_ABRT)—Offset 54h

Clear TX_ABRT Interrupt Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_TX_ABRT (CLR_TX_ABRT):** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.

21.2.22 Clear RX_DONE Interrupt (IC_CLR_RX_DONE)—Offset 58h

Clear RX_DONE Interrupt Register

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_RX_DONE (CLR_RX_DONE):** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

21.2.23 Clear ACTIVITY Interrupt (IC_CLR_ACTIVITY)—Offset 5Ch

Clear ACTIVITY Interrupt Register

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_ACTIVITY (CLR_ACTIVITY):** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register

21.2.24 Clear STOP_DET Interrupt (IC_CLR_STOP_DET)—Offset 60h

Clear STOP_DET Interrupt Register

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_STOP_DET (CLR_STOP_DET):** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register

21.2.25 Clear START_DET Interrupt (IC_CLR_START_DET)—Offset 64h

Clear START_DET Interrupt Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_START_DET (CLR_START_DET):** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

21.2.26 Clear GEN_CALL Interrupt (IC_CLR_GEN_CALL)—Offset 68h

Clear GEN_CALL Interrupt Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_GEN_CALL (CLR_GEN_CALL):** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register

21.2.27 I2C Enable (IC_ENABLE)—Offset 6Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW	**ABORT (ABORT):** Software can abort I2C transfer by setting this bit. Hw will clear this ABORT bit once the STOP has been detected
0	0h RW	**ENABLE (ENABLE):** Controls whether the controller is enabled. 0: Disables I2C controller(TX and RX FIFOs are held in an erased state) 1: Enables I2C controller. Software can disable the controller while it is active. However, it is important that care be taken to ensure that the controller is disabled properly. When the controller is disabled, the following occurs: -The TX FIFO and RX FIFO get flushed. -Status bits in the IC_INTR_STAT register are still active until the controller goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the controller stops the current transfer at the end of the current byte and does not acknowledge the transfer.

21.2.28 I2C Status (IC_STATUS)—Offset 70h

I2C Status Register. This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. When the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register: - Bits 1 and 2 are set to 1 - Bits 3 and 4 are set to 0 When the Initiator or Target state machines goes to idle and IC_ENABLE=0: - Bits 5 and 6 are set to 0

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 6h

Bit Range	Default and Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5	0h RO	**MST_ACTIVITY (MST_ACTIVITY):** When the Initiator state machine is not in the IDLE state, this bit is set. 0: Initiator is in IDLE state 1: Initiator is not in IDLE
4	0h RO	**RFF (RFF):** When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. 0: Receive FIFO is not full 1: Receive FIFO is full
3	0h RO	**RFNE (RFNE):** This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. 0: Receive FIFO is empty 1: Receive FIFO is not empty
2	1h RO	**TFE (TFE):** When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty
1	1h RO	**TFNF (TFNF):** Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. 0: Transmit FIFO is full 1: Transmit FIFO is not full
0	0h RO	**IC_STATUS_ACTIVITY (IC_STATUS_ACTIVITY):** I2C Activity Status

21.2.29 I2C Transmit FIFO Level (IC_TXFLR)—Offset 74h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:7	0h RO	Reserved.
6:0	0h RO	**TXFLR (TXFLR):** Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO

21.2.30 Receive FIFO Level (IC_RXFLR)—Offset 78h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:7	0h RO	Reserved.
6:0	0h RO	**RXFLR (RXFLR):** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

21.2.31 SDA Hold Time Length (IC_SDA_HOLD)—Offset 7Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	1h RW	**IC_SDA_TX_HOLD (IC_SDA_TX_HOLD):** Sets the required SDA hold time in units of ic_clk period (133Mhz), when the I2C Host Controller acts as a transmitter.

21.2.32 Transmit Abort Source (IC_TX_ABRT_SOURCE)—Offset 80h

This register has 32 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]).
Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:23	0h RO	**TX_FLUSH_CNT (TX_FLUSH_CNT):** This field preserves the TXFLR value prior to the last TX_ABRT event. It is cleared whenever I2C is disabled. Mode Applicable:Initiator-Transmitter
22:17	0h RO	Reserved.
16	0h RO	**ABRT_USER_ABRT (ABRT_USER_ABRT):** This is a Initiator-mode-only bit. Initiator has detected the user initiated transfer abort (IC_ENABLE[1]) Mode Applicable:Initiator-Transmitter
15	0h RO	**ABRT_SLVRD_INTX (ABRT_SLVRD_INTX):** 1: When the processor side responds to a Target mode request for data to be transmitted to a remote Initiator and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register. Mode Applicable: Target Transmitter 14 RO 1'h0
14:13	0h RO	Reserved.
12	0h RO	**ARB_LOST (ARB_LOST):** 1: Initiator has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the Target transmitter has lost arbitration. Mode Applicable: Initiator or Target Transmitter
11	0h RO	**ABRT_Initiator_DIS (ABRT_Initiator_DIS):** 1: User tries to initiate a Initiator operation with the Initiator mode disabled. Mode Applicable: Initiator Transmitter or Receiver
10	0h RO	**ABRT_10B_RD_NORSTRT (ABRT_10B_RD_NORSTRT):** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the Initiator sends a read command in 10-bit addressing mode. Mode Applicable: Initiator Receiver
9	0h RO	**ABRT_SBYTE_NORSTRT (ABRT_SBYTE_NORSTRT):** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; restart must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets re-asserted.
8	0h RO	**ABRT_HS_NORSTRT (ABRT_HS_NORSTRT):** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the Initiator to transfer data in High Speed mode. Mode Applicable: Initiator Transmitter or Receiver
7	0h RO	**ABRT_SBYTE_ACKDET (ABRT_SBYTE_ACKDET):** 1: Initiator has sent a START Byte and the START Byte was acknowledged (wrong behavior). Mode Applicable: Initiator
6	0h RO	**ABRT_HS_ACKDET (ABRT_HS_ACKDET):** 1: Initiator is in High Speed mode and the High Speed Initiator code was acknowledged (wrong behavior). Mode Applicable: Initiator
5	0h RO	**ABRT_GCALL_READ (ABRT_GCALL_READ):** 1: Controller in Initiator mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0h RO	**ABRT_GCALL_NOACK (ABRT_GCALL_NOACK):** 1: DW_apb_i2c in Initiator mode sent a General Call and no Target on the bus acknowledged the General Call. Mode Applicable: Initiator Transmitter
3	0h RO	**ABRT_TXDATA_NOACK (ABRT_TXDATA_NOACK):** 1: This is a Initiator-mode only bit. Initiator has received an acknowledgment for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote Target(s). Mode Applicable: Initiator Transmitter
2	0h RO	**ABRT_10ADDR2_NOACK (ABRT_10ADDR2_NOACK):** 1: Initiator is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any Target. Mode Applicable: Initiator Transmitter or Receiver
1	0h RO	**ABRT_10ADDR1_NOACK (ABRT_10ADDR1_NOACK):** 1: Initiator is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any Target. Mode Applicable: Initiator Transmitter or Receiver
0	0h RO	**ABRT_7B_ADDR_NOACK (ABRT_7B_ADDR_NOACK):** 1: Initiator is in 7-bit addressing mode and the address sent was not acknowledged by any Target. Mode Applicable: Initiator Transmitter or Receiver

21.2.33 DMA Control (IC_DMA_CR)—Offset 88h

This register is only valid when the controller is configured with a set of DMA Controller interface signals.
When the controller is not configured for DMA operation, this register does not exist and writing to the register's address has no effect and reading from this register address will return zero.
The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW	**TDMAE (TDMAE):** Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel. 0 = Transmit DMA disabled 1 = Transmit DMA enabled
0	0h RW	**RDMAE (RDMAE):** Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel. 0 = Receive DMA disabled 1 = Receive DMA enabled

21.2.34 DMA Transmit Data Level (IC_DMA_TDLR)—Offset 8Ch

DMA Transmit Data Level Register

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5:0	0h RW	**DMATDL (DMATDL):** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

21.2.35 Receive Data Level (IC_DMA_RDLR)—Offset 90h

I2C Receive Data Level Register

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5:0	0h RW	**DMARDL (DMARDL):** Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

21.2.36 ACK General Call (IC_ACK_GENERAL_CALL)—Offset 98h

I2C ACK General Call Register. The register controls whether DW_apb_i2c responds with a ACK or NACK when it receives an I2C General Call address

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	1h RW	**ACK_GEN_CALL (ACK_GEN_CALL):** When set to 1, the controller responds with a ACK when it receives a General Call. When set to 0, the controller does not generate General Call interrupts.

21.2.37 I2C Enable Status (IC_ENABLE_STATUS)—Offset 9Ch

The register is used to report the hardware status when the IC_ENABLE register is set from 1 to 0; that is, when the controller is disabled.
If IC_ENABLE has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.
If IC_ENABLE has been set to 0, bits 2:1 is only be valid as soon as bit 0 is read as '0'.
When IC_ENABLE has been written with '0,' a delay occurs for bit 0 to be read as '0' because disabling the controller depends on I2C bus activities.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**IC_EN (IC_EN):** When read as 1, the controller is deemed to be in an enabled state. When read as 0, the controller is deemed completely inactive.

21.2.38 SS and FS Spike Suppression Limit (IC_FS_SPKLEN)—Offset A0h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in SS or FS modes.
The relevant I2C requirement is tSP as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 7h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	7h RW	**IC_FS_SPKLEN (IC_FS_SPKLEN):** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set.

21.3 I2C Additional Registers

The registers in this section are memory-mapped registers based on the BAR defined in PCH Configuration space.

Table 21-3. Summary of I2C Additional Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
204h	207h	Soft Reset (RESETS)—Offset 204h	0h
210h	213h	Active LTR (ACTIVELTR_VALUE)—Offset 210h	800h
214h	217h	Idle LTR (IDLELTR_VALUE)—Offset 214h	800h
218h	21Bh	TX ACK Count (TX_ACK_COUNT)—Offset 218h	0h

Table 21-3. Summary of I2C Additional Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
21Ch	21Fh	RX ACK Count (RX_BYTE_COUNT)—Offset 21Ch	0h
220h	223h	Interrupt Status for Tx Complete (TX_COMPLETE_INTR_STAT)—Offset 220h	0h
224h	227h	Tx Complete Interrupt Clear (TX_COMPLETE_INTR_CLR)—Offset 224h	0h
228h	22Bh	SW Scratch Register 0 (SW_SCRATCH_0)—Offset 228h	0h
22Ch	22Fh	SW Scratch Register 1 (SW_SCRATCH_1)—Offset 22Ch	0h
230h	233h	SW Scratch Register 2 (SW_SCRATCH_2)—Offset 230h	0h
234h	237h	SW Scratch Register 3 (SW_SCRATCH_3)—Offset 234h	0h
238h	23Bh	Clock Gate (CLOCK_GATE)—Offset 238h	0h
240h	243h	Remap Address Low (REMAP_ADDR_LO)—Offset 240h	0h
244h	247h	Remap Address High (REMAP_ADDR_HI)—Offset 244h	0h
24Ch	24Fh	Device Idle Control (DEVIDLE_CONTROL)—Offset 24Ch	8h
2FCh	2FFh	Capabilities (CAPABLITIES)—Offset 2FCh	0h

21.3.1 Soft Reset (RESETS)—Offset 204h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW	**reset_dma (reset_dma):** DMA Software Reset Control. 0 = IP is in reset (Reset Asserted) 1 = IP is NOT at reset (Reset Released)
1:0	0h RW	**reset_ip (reset_ip):** Used to reset the I2C Host Controller by SW control. All I2C Configuration State and Operational State will be forced to the Default state. There is no timing requirement (SW can assert and de-assert in back to back transactions). This reset does NOT impact the settings by BIOS, the PCI configuration header information, DMA channel configuration and interrupt assignment/mapping/etc. Driver should re-initialize registers related to Driver context following an I2C host controller reset. 00 = I2C Host Controller is in reset (Reset Asserted) 01 = Reserved 10 = Reserved 11 = I2C Host Controller is NOT at reset (Reset Released)

21.3.2 Active LTR (ACTIVELTR_VALUE)—Offset 210h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 800h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**Snoop Requirement (snoop_requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10 -bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time
14:13	0h RO	Reserved.
12:10	2h RW	**i2c_sw_ltr_snoop_scale_reg_12_10 (i2c_sw_ltr_snoop_scale_reg_12_10):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**Snoop Value (snoop_value):** 10-bit latency value

21.3.3 Idle LTR (IDLELTR_VALUE)—Offset 214h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 800h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**snoop_requirement (snoop_requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10 -bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time
14:13	0h RO	Reserved.
12:10	2h RW	**snoop_latency_scale (snoop_latency_scale):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**snoop_value (snoop_value):** 10-bit latency value.

21.3.4 TX ACK Count (TX_ACK_COUNT)—Offset 218h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	**TX Count Overflow (tx_ack_count_overflow):** Count overflow indication. 0= Count valid 1= Count overflow/invalid
30:24	0h RO	Reserved.
23:0	0h RO	**TX Ack Count (tx_ack_count):** Count ACK seen on Write commands, 24-bit up-counter which counts the number of TX ACKs on the I2C bus. The Counter is forced to be cleared by software Read.

21.3.5 RX ACK Count (RX_BYTE_COUNT)—Offset 21Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	**RX ACK Count Overflow (rx_ack_count_overflow):** Rx ACK count overflow 0= count valid 1= count overflow/invalid
30:24	0h RO	Reserved.
23:0	0h RO	**RX ACK Count (rx_ack_count):** Counts ACK seen on Read commands, 24-bit readable (MMIO) up-counter which counts the number of RX bytes received on the I2C bus. The Counter is forced to be cleared by software Read

21.3.6 Interrupt Status for Tx Complete (TX_COMPLETE_INTR_STAT)—Offset 220h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW	**TX Completion Interrupt Mask (tx_intr_stat_mask):** 0 = Unmask 1= Mask
0	0h RO	**TX Completion Interrupt (tx_intr_stat):** 0 = Low 1 = High

21.3.7 Tx Complete Interrupt Clear (TX_COMPLETE_INTR_CLR)—Offset 224h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**TX Completion Interrupt Clear (i2c_tx_complete_intr_clr_0):** Read this register to clear the TX_COMPLETE_INTR_STAT register

21.3.8 SW Scratch Register 0 (SW_SCRATCH_0)—Offset 228h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SW Scratch 0 (SW_Scratch_0):** Scratch Pad Register for SW to generated Local CMD or DATA for DMA.

21.3.9 SW Scratch Register 1 (SW_SCRATCH_1)—Offset 22Ch

Same definition as SW_SCRATCH_0.

21.3.10 SW Scratch Register 2 (SW_SCRATCH_2)—Offset 230h

Same definition as SW_SCRATCH_0.

21.3.11 SW Scratch Register 3 (SW_SCRATCH_3)—Offset 234h

Same definition as SW_SCRATCH_0.

21.3.12 Clock Gate (CLOCK_GATE)—Offset 238h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:2	0h RW	**DMA Clock Control (sw_dma_clk_ctl):** 00 = Dyanamic Clock Gate Enable 01 = Reserved 10 = Force iDMA Clock off 11 = Force iDMA Clock on
1:0	0h RW	**Controller Clock Control (sw_ip_clk_ctl):** 00 = Dynamic Clock Gate Enable 01 = Reserved 10 = Force Clocks off 11 = Force Clocks on

21.3.13 Remap Address Low (REMAP_ADDR_LO)—Offset 240h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Remap Address Low (i2c_remap_addr_lo_reg):** Must be programmed to the same value as low 32 bits (0x 010 BAR Low) Note: Must be programed for all I2C controllers configurations (DMA or PIO only)

21.3.14 Remap Address High (REMAP_ADDR_HI)—Offset 244h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Remap Address High (i2c_remap_addr_hi):** Must be programmed to the same value as low 32 bits (0x 014 BAR High)

21.3.15 Device Idle Control (DEVIDLE_CONTROL)—Offset 24Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**Interrupt Request Capable (intr_req_capable):** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0.
3	1h RW/1C	**Restore Required (restore_required):** When set (by HW), SW must restore state to the controller. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up. Note: If SW is setting bit 3 together with any other bit of this register, only bit 3 is written; SW is required to do 2 writes in this case : bit 3 first and all other bits second.
2	0h RW	**Device Idle (devidle):** SW sets this bit to 1 to move the function into the DevIdle state. Writing this bit to 0 will return the function to the fully active D0 state.
1	0h RO	Reserved.
0	0h RO	**Command In Progress (cmd_in_progress):** HW sets this bit on a 1->0 or 0->1 transition of DEVIDLE. While set, the other bits in this register are not valid and it is unsupported for SW to write to any bit in this register. HW clears this bit upon completing the DevIdle transition command. When clear, all the other bits in the register are valid and SW may write to any bit. If Interrupt Request (IR) was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW. SW writes to this bit have no effect.

21.3.16 Capabilities (CAPABLITIES)—Offset 2FCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9	0h RO	**Serial Clock Frequency (serial_clk_freq):** 1 indicates 133 MHz clock.
8	0h RO	**DMA Present (iDMA_present):** 0= DMA present 1= DMA not present
7:4	0h RO	**Instance Type (instance_type):** 0000 = I2C 0001 = UART 0010 = SPI 0011 – 1111 = Reserved
3:0	0h RO	**instance_number (instance_number):** 0h: I2C0 1h: I2C1 2h: I2C2 ... 5h: I2C5

21.4 I2C DMA Controller Registers

The registers in this section are memory-mapped registers based on the BAR defined in PCH Configuration space.

Table 21-4. Summary of I2C DMA Controller Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
800h	803h	DMA Transfer Source Address Low (SAR_LO0)—Offset 800h	0h
804h	807h	DMA Transfer Source Address High (SAR_HI0)—Offset 804h	0h
808h	80Bh	DMA Transfer Destination Address Low (DAR_LO0)—Offset 808h	0h
80Ch	80Fh	DMA Transfer Destination Address High (DAR_HI0)—Offset 80Ch	0h
810h	813h	Linked List Pointer Low (LLP_LO0)—Offset 810h	0h
814h	817h	Linked List Pointer High (LLP_HI0)—Offset 814h	0h
818h	81Bh	Control Register Low (CTL_LO0)—Offset 818h	0h
81Ch	81Fh	Control Register High (CTL_HI0)—Offset 81Ch	0h
820h	823h	Source Status (SSTAT0)—Offset 820h	0h
828h	82Bh	Destination Status (DSTAT0)—Offset 828h	0h
830h	833h	Source Status Address Low (SSTATAR_LO0)—Offset 830h	0h
834h	837h	Source Status Address High (SSTATAR_HI0)—Offset 834h	0h
838h	83Bh	Destination Status Address Low (DSTATAR_LO0)—Offset 838h	0h
83Ch	83Fh	Destination Status Address High (DSTATAR_HI0)—Offset 83Ch	0h
840h	843h	DMA Transfer Configuration Low (CFG_LO0)—Offset 840h	203h
844h	847h	DMA Transfer Configuration High (CFG_HI0)—Offset 844h	0h
848h	84Bh	Source Gather (SGR0)—Offset 848h	0h
850h	853h	Destination Scatter (DSR0)—Offset 850h	0h
AC0h	AC3h	Raw Interrupt Status (RawTfr)—Offset AC0h	0h

Table 21-4. Summary of I2C DMA Controller Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
AC8h	ACBh	Raw Status for Block Interrupts (RawBlock)—Offset AC8h	0h
AD0h	AD3h	Raw Status for Source Transaction Interrupts (RawSrcTran)—Offset AD0h	0h
AD8h	ADBh	Raw Status for Destination Transaction Interrupts (RawDstTran)—Offset AD8h	0h
AE0h	AE3h	Raw Status for Error Interrupts (RawErr)—Offset AE0h	0h
AE8h	AEBh	Status for Transfer Interrupts (StatusTfr)—Offset AE8h	0h
AF0h	AF3h	Status for Block Interrupts (StatusBlock)—Offset AF0h	0h
AF8h	AFBh	Status for Source Transaction Interrupts (StatusSrcTran)—Offset AF8h	0h
B00h	B03h	Status for Destination Transaction Interrupts (StatusDstTran)—Offset B00h	0h
B08h	B0Bh	Status for Error Interrupts (StatusErr)—Offset B08h	0h
B10h	B13h	Mask for Transfer Interrupts (MaskTfr)—Offset B10h	0h
B18h	B1Bh	Mask for Block Interrupts (MaskBlock)—Offset B18h	0h
B20h	B23h	Mask for Source Transaction Interrupts (MaskSrcTran)—Offset B20h	0h
B28h	B2Bh	Mask for Destination Transaction Interrupts (MaskDstTran)—Offset B28h	0h
B30h	B33h	Mask for Error Interrupts (MaskErr)—Offset B30h	0h
B38h	B3Bh	Clear for Transfer Interrupts (ClearTfr)—Offset B38h	0h
B40h	B43h	Clear for Block Interrupts (ClearBlock)—Offset B40h	0h
B48h	B4Bh	Clear for Source Transaction Interrupts (ClearSrcTran)—Offset B48h	0h
B50h	B53h	Clear for Destination Transaction Interrupts (ClearDstTran)—Offset B50h	0h
B58h	B5Bh	Clear for Error Interrupts (ClearErr)—Offset B58h	0h
B60h	B63h	Combined Status (StatusInt)—Offset B60h	0h
B98h	B9Bh	DMA Configuration (DmaCfgReg)—Offset B98h	0h
BA0h	BA3h	DMA Channel Enable (ChEnReg)—Offset BA0h	0h

21.4.1 DMA Transfer Source Address Low (SAR_LO0)—Offset 800h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer. Source Address Register for lowe 32-bits for Channels 0-1

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SAR_LO (SAR_LO):** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

21.4.2 DMA Transfer Source Address High (SAR_HI0)—Offset 804h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer. Source Address Register for upper 32-bits for Channels 0-1

Access Method

Type: MEM Register (Size: 32 bits)

Device:

Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SAR_HI (SAR_HI):** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

21.4.3 DMA Transfer Destination Address Low (DAR_LO0)—Offset 808h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.Destination Address Register for Channels 0-1

Access Method

Type: MEM Register (Size: 32 bits)

Device:

Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DAR_LO (DAR_LO):** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

21.4.4 DMA Transfer Destination Address High (DAR_HI0)—Offset 80Ch

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer. Destination Address Register for Upper 32-bits for Channels 0-1

Access Method

Type: MEM Register (Size: 32 bits)

Device:

Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DAR_HI (DAR_HI):** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

21.4.5 Linked List Pointer Low (LLP_LO0)—Offset 810h

The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**LOC (LOC):** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	Reserved.

21.4.6 Linked List Pointer High (LLP_HI0)—Offset 814h

The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

21.4.7 Control Register Low (CTL_LO0)—Offset 818h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RW	**LLP_SRC_EN (LLP_SRC_EN):** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN (LLP_DST_EN):** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	Reserved.
21:20	0h RW	**TT_FC (TT_FC):** The following transfer types are supported. 00: Reserved 01: Memory to Peripheral 10: Peripheral to Memory 11: Reserved Flow Control is always assigned to the DMA.
19	0h RO	Reserved.
18	0h RW	**DST_SCATTER_EN (DST_SCATTER_EN):** 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN (SRC_GATHER_EN):** 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE (SRC_MSIZE):** Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. Source BURST SIZE (in DW) = (2 ^ SRC_TR_WIDTH)
13:11	0h RW	**DEST_MSIZE (DEST_MSIZE):** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination.
10	0h RW	**SINC (SINC):** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	Reserved.
8	0h RW	**DINC (DINC):** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)

Bit Range	Default and Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**SRC_TR_WIDTH (SRC_TR_WIDTH):** BURST_SIZE (IN DW) = (2^ MSIZE) (i.e. 2 to-the-power-of MSIZE) 1.Transferred Bytes Per Burst = BURST_SIZE * (2 ^ TR_WIDTH) Note that encodings 101 (32 DW), 110 (64 DW) and 111 (128 DW) are not supported. 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported.
3:1	0h RW	**DST_TR_WIDTH (DST_TR_WIDTH):** BURST SIZE (in DW) = (2^ MSIZE) (i.e. 2 to-the-power-of MSIZE) Transferred Bytes Per Burst = BURST_SIZE * (2 ^ TR_WIDTH) Since Max Burst Length is limited to 16 DW, encodings 101 (32 DW), 110 (64 DW) and 111 (128 DW) are not supported. For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported.
0	0h RW	**INT_EN (INT_EN):** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

21.4.8 Control Register High (CTL_HI0)—Offset 81Ch

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:29	0h RW	**CH_CLASS (CH_CLASS):** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior.
28:18	0h NA	**RESERVED (RESERVED0):** Reserved
17	0h RW	**DONE (DONE):** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS (BLOCK_TS):** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register.

21.4.9 Source Status (SSTAT0)—Offset 820h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SSTAT (SSTAT):** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA Target interface.

21.4.10 Destination Status (DSTAT0)—Offset 828h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note: This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA Target interface.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DSTAT (DSTAT):** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA Target interface

21.4.11 Source Status Address Low (SSTATAR_LO0)—Offset 830h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx registe

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR_LO (SSTATAR_LO):** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block

21.4.12 Source Status Address High (SSTATAR_HI0)—Offset 834h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR_HI (SSTATAR_HI):** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block

21.4.13 Destination Status Address Low (DSTATAR_LO0)—Offset 838h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR_LO (DSTATAR_LO):** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

21.4.14 Destination Status Address High (DSTATAR_HI0)—Offset 83Ch

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR_HI (DSTATAR_HI):** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

21.4.15 DMA Transfer Configuration Low (CFG_LO0)—Offset 840h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 203h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW	**RELOAD_DST (RELOAD_DST):** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated
30	0h RW	**RELOAD_SRC (RELOAD_SRC):** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
21	0h RW	**SRC_OPT_BL (SRC_OPT_BL):** 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE))
20	0h RW	**DST_OPT_BL (DST_OPT_BL):** 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE))
19	0h RW	**SRC_HS_POL (SRC_HS_POL):** 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL (DST_HS_POL):** 0 = Active high 1 = Active low
17:11	0h RO	Reserved.
10	0h RW	**CH_DRAIN (CH_DRAIN):** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1h RO	**FIFO_EMPTY (FIFO_EMPTY):** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP (CH_SUSP):** Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN (SS_UPD_EN):** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0
6	0h RW	**DS_UPD_EN (DS_UPD_EN):** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN (CTL_HI_UPD_EN):** If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	Reserved.
3	0h RW	**HSHAKE_NP_WR (HSHAKE_NP_WR):** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port. 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-ofblock writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR (ALL_NP_WR):** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port. 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used
1	1h RW	**SRC_BURST_ALIGN (SRC_BURST_ALIGN):** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary. 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary.
0	1h RW	**DST_BURST_ALIGN (DST_BURST_ALIGN):** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary. 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

21.4.16 DMA Transfer Configuration High (CFG_HI0)—Offset 844h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:18	0h RW	**WR_ISSUE_THD (WR_ISSUE_THD):** Write Issue Threshold. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD (RD_ISSUE_THD):** Read Issue Threshold. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER (DST_PER):** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface.
3:0	0h RW	**SRC_PER (SRC_PER):** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface.

21.4.17 Source Gather (SGR0)—Offset 848h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:20	0h RW	**SGC (SGC):** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI (SGI)**

21.4.18 Destination Scatter (DSR0)—Offset 850h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:20	0h RW	**DSC (DSC):** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries
19:0	0h RW	**DSI (DSI)**

21.4.19 Raw Interrupt Status (RawTfr)—Offset AC0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Bit0 for channel 0 and bit 1 for channel 1.

21.4.20 Raw Status for Block Interrupts (RawBlock)—Offset AC8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Bit 0 for channel 0 and bit 1 for channel 1.

21.4.21 Raw Status for Source Transaction Interrupts (RawSrcTran)—Offset AD0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Bit 0 for channel 0 and bit 1 for channel 1.

21.4.22 Raw Status for Destination Transaction Interrupts (RawDstTran)—Offset AD8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Bit 0 for channel 0 and bit 1 for channel 1.

21.4.23 Raw Status for Error Interrupts (RawErr)—Offset AE0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Bit 0 for channel 0 and bit 1 for channel 1.

21.4.24 Status for Transfer Interrupts (StatusTfr)—Offset AE8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Bit 0 for channel 0 and bit 1 for channel 1.

21.4.25 Status for Block Interrupts (StatusBlock)—Offset AF0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Bit 0 for channel 0 and bit 1 for channel 1.

21.4.26 Status for Source Transaction Interrupts (StatusSrcTran)—Offset AF8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Bit 0 for channel 0 and bit 1 for channel 1.

21.4.27 Status for Destination Transaction Interrupts (StatusDstTran)—Offset B00h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Bit 0 for channel 0 and bit 1 for channel 1.

21.4.28 Status for Error Interrupts (StatusErr)—Offset B08h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Bit 0 for channel 0 and bit 1 for channel 1.

21.4.29 Mask for Transfer Interrupts (MaskTfr)—Offset B10h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0)**
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** Interrupt mask per ch1 and ch0 . 0-mask 1-unmask

21.4.30 Mask for Block Interrupts (MaskBlock)—Offset B18h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** Interrupt mask ch1 and ch0. 0-mask 1-unmask

21.4.31 Mask for Source Transaction Interrupts (MaskSrcTran)—Offset B20h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** Interrupt mask ch1 and ch0. 0-mask 1-unmask

21.4.32 Mask for Destination Transaction Interrupts (MaskDstTran)—Offset B28h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** Interrupt mask ch1 and ch0. 0-mask 1-unmask

21.4.33 Mask for Error Interrupts (MaskErr)—Offset B30h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** Interrupt mask ch1 and ch0. 0-mask 1-unmask

21.4.34 Clear for Transfer Interrupts (ClearTfr)—Offset B38h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

21.4.35 Clear for Block Interrupts (ClearBlock)—Offset B40h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

21.4.36 Clear for Source Transaction Interrupts (ClearSrcTran)—Offset B48h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

21.4.37 Clear for Destination Transaction Interrupts (ClearDstTran)—Offset B50h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

21.4.38 Clear for Error Interrupts (ClearErr)—Offset B58h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

21.4.39 Combined Status (StatusInt)—Offset B60h

The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran,StatusErr is Ored to produce a single bit for each interrupt type in the Combined Status register (StatusInt). This register is read-only

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**ERR (ERR):** OR of the contents of StatusErr register.
3	0h RO	**DSTT (DSTT):** OR of the contents of StatusDst register.

Bit Range	Default and Access	Field Name (ID): Description
2	0h RO	**SRCT (SRCT):** OR of the contents of StatusSrcTran register
1	0h RO	**BLOCK (BLOCK):** OR of the contents of StatusBlock register.
0	0h RO	**TFR (TFR):** OR of the contents of StatusTfr register.

21.4.40 DMA Configuration (DmaCfgReg)—Offset B98h

This register is used to enable the DMA, which must be done before any channel activity can begin. If the global channel enable bit is cleared while any channel is still active, then DmaCfgReg.DMA_EN still returns 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the DmaCfgReg.DMA_EN bit returns 0.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**DMA_EN (DMA_EN):** DMA Enable bit. 0 = DMA Disabled 1 = DMA Enabled

21.4.41 DMA Channel Enable (ChEnReg)—Offset BA0h

This is the DMA Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive, it can then enable an inactive channel with the required priority. All bits of this register are cleared to 0 when the global DMA channel enable bit, DmaCfgReg(0), is 0. When the global channel enable bit is 0, then a write to the ChEnReg register is ignored and a read will always read back 0. The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel write enable bit, ChEnReg.CH_EN_WE, is asserted on the same OCP write transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Channel enable write enable.
7:2	0h RO	Reserved.
1:0	0h RW	**CH_EN (CH_EN):** Enables/Disables the channel. Setting this bit enables a channel, clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel The ChEnReg.CH_EN bit is automatically cleared by hardware to disable the channel after the last OCP transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer.

21.5 I2C PCR Registers

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 21-5. Summary of I2C PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
200h	203h	PCI Configuration Control for I2C0 (PCICFGCTR1)—Offset 200h	0h
204h	207h	PCI Configuration Control for I2C1 (PCICFGCTR2)—Offset 204h	0h
208h	20Bh	PCI Configuration Control for I2C2 (PCICFGCTR3)—Offset 208h	0h
20Ch	20Fh	PCI Configuration Control for I2C3 (PCICFGCTR4)—Offset 20Ch	0h
210h	213h	PCI Configuration Control for I2C4 (PCICFGCTR5)—Offset 210h	0h
214h	217h	PCI Configuration Control for I2C5 (PCICFGCTR6)—Offset 214h	0h
218h	21Bh	PCI Configuration Control for I2C6 (PCICFGCTR7)—Offset 218h	0h
21Ch	21Fh	PCI Configuration Control for I2C7 (PCICFGCTR8)—Offset 21Ch	0h

21.5.1 PCI Configuration Control for I2C0 (PCICFGCTR1)—Offset 200h

Controls the PCI Configuration Space

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:20	0h RW	**PCICFGCTR1 - PCI IRQ Num Field (PCI_IRQ1):** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	0h RW	**PCICFGCTR1 - ACPI IRQ Field (ACPI_IRQ1):** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	0h RW	**Interrupt Pin (IPIN1):** This register indicates the values to be used for Global Interrupts. 0 = No interrupt Pin 1 = INTA 2 = INTB 3 = INTC 4 = INTD 5 - FF: Reserved
7	0h RW	**BAR1 Disable (BAR1_DISABLE1):** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	0h RW	**PME Support (PME_SUPPORT1):** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1	0h RW	**ACPI Interrupt Enable Field (ACPI_INTR_EN1):** When set, ACPI IRQ number field (bits 19:12) will be used for IRQ messages. When 0, PCI IRQ number field (bits 27:20) will be used for IRQ message.
0	0h RW	**PCICFGCTR1 - PCI CFG Disable Field (PCI_CFG_DIS1):** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported

21.5.2 PCI Configuration Control for I2C1 (PCICFGCTR2)—Offset 204h

Same definition as PCICFGCTR1

21.5.3 PCI Configuration Control for I2C2 (PCICFGCTR3)—Offset 208h

Same definition as PCICFGCTR1.

21.5.4 PCI Configuration Control for I2C3 (PCICFGCTR4)—Offset 20Ch

Same definition as PCICFGCTR1.

21.5.5 PCI Configuration Control for I2C4 (PCICFGCTR5)—Offset 210h

Same definition as PCICFGCTR1.

21.5.6 PCI Configuration Control for I2C5 (PCICFGCTR6)—Offset 214h

Same definition as PCICFGCTR1.

21.5.7 PCI Configuration Control for I2C6 (PCICFGCTR7)—Offset 218h

Same definition as PCICFGCTR1.

21.5.8 PCI Configuration Control for I2C7 (PCICFGCTR8)—Offset 21Ch

Same definition as PCICFGCTR1.

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22 SATA Interface (D23: F0)

22.1 SATA Configuration Registers

Table 22-1. Summary of SATA Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Identifiers (ID)—Offset 0h	XXXX8086h
4h	5h	Command (CMD)—Offset 4h	0h
6h	7h	Device Status (STS)—Offset 6h	210h
8h	8h	Revision ID (RID)—Offset 8h	XXh
9h	9h	Programming Interface (PI)—Offset 9h	1h
Ah	Bh	Class Code (CC)—Offset Ah	106h
Ch	Ch	Cache Line Size (CLS)—Offset Ch	0h
Dh	Dh	Initiator Latency Timer (MLT)—Offset Dh	0h
Eh	Eh	Header Type (HTYPE)—Offset Eh	0h
10h	13h	MSI-X Table Base Address (MXTBA)—Offset 10h	0h
14h	17h	MSI-X Pending Bit Array Base Address (MXPBA)—Offset 14h	0h
20h	23h	AHCI Index Data Pair Base Address (AIDPBA)—Offset 20h	1h
24h	27h	AHCI Base Address (ABAR)—Offset 24h	0h
2Ch	2Fh	Sub System Identifiers (SS)—Offset 2Ch	0h
34h	34h	Capabilities Pointer (CAP)—Offset 34h	80h
3Ch	3Dh	Interrupt Information (INTR)—Offset 3Ch	100h
70h	71h	PCI Power Management Capability ID (PID)—Offset 70h	A801h
72h	73h	PCI Power Management Capability ID (PID)—Offset 70h	4003h
74h	75h	PCI Power Management Control And Status (PMCS)—Offset 74h	8h
80h	81h	Message Signalled Interrupt Identifier (MID)—Offset 80h	7005h
82h	83h	Message Signalled Interrupt Message Control (MC)—Offset 82h	0h
84h	87h	Message Signalled Interrupt Message Address (MA)—Offset 84h	0h
88h	89h	Message Signalled Interrupt Message Data (MD)—Offset 88h	0h
90h	93h	Port Mapping Register (MAP)—Offset 90h	0h
94h	97h	Port Control And Status (PCS)—Offset 94h	0h
9Ch	9Fh	SATA General Configuration (SATAGC)—Offset 9Ch	0h
A0h	A0h	SATA Initialization Register Index (SIRI)—Offset A0h	0h
A4h	A7h	SATA Initialization Register Data (SIRD)—Offset A4h	0h
A8h	ABh	Serial ATA Capability Register 0 (SATACR0)—Offset A8h	100012h
ACh	AFh	Serial ATA Capability Register 1 (SATACR1)—Offset ACh	48h
C0h	C3h	Scratch Pad (SP)—Offset C0h	0h
D0h	D1h	MSI-X Identifiers (MXID)—Offset D0h	11h
D2h	D3h	MSI-X Message Control (MXC)—Offset D2h	0h
D4h	D7h	MSI-X Table Offset And Table BIR (MXT)—Offset D4h	0h

Table 22-1. Summary of SATA Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
D8h	DBh	MSI-X PBA Offset And PBA BIR (MXP)—Offset D8h	1h
E0h	E3h	BIST FIS Control/Status (BFCS)—Offset E0h	0h
E4h	E7h	BIST FIS Transmit Data 1 (BFTD1)—Offset E4h	0h
E8h	EBh	BIST FIS Transmit Data 2 (BFTD2)—Offset E8h	0h

22.1.1 Identifiers (ID)—Offset 0h

When the MMIO RUN.RUNE=1, read access to this double-word is return with UR.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: XXXX8086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	-- RO	**Device ID (DID):** Indicates the Device ID of the SATA controller. Refer to the Device and Revision ID Table in Volume 1 for default value.
15:0	8086h RO	**Vendor ID (VID):** 16-bit field which indicates the company vendor as Intel.

22.1.2 Command (CMD)—Offset 4h

Command

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts. This bit has no effect on MSI operation. 0 = Internal INTx# messages are generated if there is an interrupt and MSI is not enabled. 1 = Internal INTx# messages will not be generated.
9	0h RO	Reserved.
8	0h RW	**SERR# Enable (SEE):** 0 = SERR# messages will not be generated. 1 = SERR# messages are generated if STS.DPD register is set or bit 8 of the SATAGC.URD register is set.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6	0h RW	**Parity Error Response Enable (PEE):** 0 = Disabled. SATA controller will not generate PERR# when a data parity error is detected. 1 = Enabled. SATA controller will generate PERR# when a data parity error is detected.
5:3	0h RO	Reserved.
2	0h RW	**Bus Initiator Enable (BME):** Controls the SATA Controller's ability to act as a Initiator for data transfers. This bit does not impact the generation of completions for split transaction commands.
1	0h RW	**Memory Space Enable (MSE):** Controls access to the SATA Controller's target memory space (for AHCI).
0	0h RW	**I/O Space Enable (IOSE):** Controls access to the SATA Controller's target I/O space.

22.1.3 Device Status (STS)—Offset 6h

Device Status

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 210h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C/V	**Detected Parity Error (DPE):** 0 = No parity error detected by SATA controller. 1 = SATA controller detects a parity error on its interface.
14	0h RW/1C/V	**Signalled System Error (SSE):** 0 = No SERR# detected by SATA controller. 1 = SATA controller detects a SERR# on its interface.
13	0h RW/1C/V	**Received Initiator-Abort Status (RMA):** 0 = Initiator abort not generated. 1 = SATA controller received a Initiator abort.
12	0h RW/1C/V	**Received Target-Abort Status (RTA):** 0 = Target abort not generated. 1 = SATA controller received a target abort.
11	0h RW/1C/V	**Signalled Target-Abort Status (STA):** This bit must be set by a target device whenever it terminates a transaction with Target-Abort. Devices that will never signal Target-Abort do not need to implement this bit.
10:9	1h RO	**DEVSEL# Timing Status (DEVT):** 01 = Hardwired; Controls the device select time for the SATA controller's PCI interface.
8	0h RW/1C/V	**Initiator Data Parity Error Detected (DPD):** For PCH, this bit can only be set on read completions received from the bus when there is a parity error. 0 = No data parity error received. 1 = SATA controller, as a Initiator, either detects a parity error or sees the parity error line asserted, and the parity error response bit (bit 6 of the command register) is set.
7:5	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	1h RO	**Capabilities List (CL):** Indicates the presence of a capabilities list. The minimum requirement for the capabilities list must be PCI power management for the SATA Controller.
3	0h RO/V	**Interrupt Status (IS):** Reflects the state of INTx# messages, IRQ14 or IRQ15. 0 = Interrupt is cleared (independent of the state of CMD.ID). 1 = Interrupt is to be asserted
2:0	0h RO	Reserved.

22.1.4 Revision ID (RID)—Offset 8h

Revision ID

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 23
Function: 0

Default: XXh

Bit Range	Default & Access	Field Name (ID): Description
7:0	-- RO	**Revision ID (RID):** Indicates stepping of the host controller hardware. Refer to Device ID and Revision Table in Vol1 for specific value.

22.1.5 Programming Interface (PI)—Offset 9h

Programming Interface

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 23
Function: 0

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
7:0	1h RO	**Interface (IF):** If CC.SCC=06h (AHCI mode), it indicates that this is an AHCI HBA that has a major revision of 1. If CC.SCC=04h (RAID mode), it indicates that there is no programming interface (IF=00h).

22.1.6 Class Code (CC)—Offset Ah

Class Code

Access Method

Type: CFG Register (Size: 16 bits)
Device: 23
Function: 0

Default: 106h

Bit Range	Default & Access	Field Name (ID): Description
15:8	1h RO	**Base Class Code (BCC):** Indicates that this is a mass storage device.
7:0	6h RO	**Sub Class Code (SCC):** This field specifies the sub-class code of the controller, per the table below: MAP.SMS SCC Register Value 0b 06h (AHCI Controller) 1b 04h (RAID Controller)

22.1.7 Cache Line Size (CLS)—Offset Ch

Cache Line Size

Access Method

Type: CFG Register (Size: 8 bits)
Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Cache Line Size (CLS):** This register has no meaning for the SATA controller.

22.1.8 Initiator Latency Timer (MLT)—Offset Dh

Initiator Latency Timer

Access Method

Type: CFG Register (Size: 8 bits)
Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Initiator Latency Timer (MLT):** This register has no meaning for the SATA controller.

22.1.9 Header Type (HTYPE)—Offset Eh

Header Type

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 23 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Multi-function Device (MFD):** 1: indicates this controller is part of a multi-function device. 0: indicates this controller is a single function device.
6:0	0h RO	**Header Layout (HL):** Indicates that the controller uses a target device layout.

22.1.10 MSI-X Table Base Address (MXTBA)—Offset 10h

This BAR is used to allocate 32K, 16K or 8K Memory space for the MSI-X Table. The Memory space size is determined by BIOS by making bit-14 and bit-13 Read-Only '1' or Read-Write '0' based on SATAGC.MSS[1:0].

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 23 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RW	**Base Address (BA):** Base address of memory space.
14	0h RW	**Base Address Bit 14 (BAB14):** When SATAGC.MSS[1:0]=00, this bit is Read Only '0' else it's Read Write '0'.
13	0h RW	**Base Address Bit 13 (BAB13):** When SATAGC.MSS[1:0]=00 or 01, this bit is Read Only '0' else it's Read Write '0'.
12:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PF):** Indicates that this range is not pre-fetchable.
2:1	0h RO	**Type (TP):** Indicates that this range can be mapped anywhere in 32-bit address space.
0	0h RO	**Resource Type Indicator (RTE):** Indicates a request for Memory space.

22.1.11 MSI-X Pending Bit Array Base Address (MXPBA)—Offset 14h

This BAR is used to allocate 256-byte Memory space for the MSI-X PBA.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Base Address (BA):** Base address of memory space (aligned to 256B).
7:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PF):** Indicates that this range is not pre-fetchable.
2:1	0h RO	**Type (TP):** Indicates that this range can be mapped anywhere in 32-bit address space.
0	0h RO	**Resource Type Indicator (RTE):** Indicates a request for Memory space.

22.1.12 AHCI Index Data Pair Base Address (AIDPBA)—Offset 20h

This BAR is used to allocate I/O space for the AHCI index/data pair mechanism.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 23
Function: 0

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:5	0h RW	**Base Address (BA):** Base address of the I/O space.
4:1	0h RO	Reserved.
0	1h RO	**Resource Type Indicator (RTE):** Indicates a request for IO space.

22.1.13 AHCI Base Address (ABAR)—Offset 24h

This register represents a memory BAR allocating space for the AHCI memory registers. Note that Bit[31:16] of this register must be programmed to a value greater than 0 to ensure the memory is mapped to an address of 1 MBytes and greater (i.e. ABAR must be 00010000h or greater). Otherwise, memory cycle targeting the ABAR range may not be accepted. The Memory space size is determined by BIOS by making bit 15:11 Read-Only 1 or Read-Write 0 based on SATAGC.ASSEL[1:0].

Access Method

Type: CFG Register (Size: 32 bits)
Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RW	**Base Address (BA):** Base address of register memory space.
18	0h RW	**Base Address Bit 18 (BAB18):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 256K, this bit is Read Only '0' else it's Read Write '0'.
17	0h RW	**Base Address Bit 17 (BAB17):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 128K, this bit is Read Only '0' else it's Read Write '0'.
16	0h RW	**Base Address Bit 16 (BAB16):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 64K, this bit is Read Only '0' else it's Read Write '0'.
15	0h RW	**Base Address Bit 15 (BAB15):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 32K, this bit is Read Only '0' else it's Read Write '0'.
14	0h RW	**Base Address Bit 14 (BAB14):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 16K, this bit is Read Only '0' else it's Read Write '0'.
13:11	0h RW	**Base Address Bit 13-11 (BAB1311):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 2K, this bit is Read Only '0' else it's Read Write '0'.
10:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PF):** Indicates that this range is not pre-fetchable
2:1	0h RO	**Type (TP):** Indicates that this range can be mapped anywhere in 32-bit address space
0	0h RO	**Resource Type Indicator (RTE):** Indicates a request for register memory space.

22.1.14 Sub System Identifiers (SS)—Offset 2Ch

This register is initialized to logic 0 by the assertion of PLTRST#. This register can be written only once after PLTRST# de-assertion.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SSID):** This is written by BIOS. No hardware action taken on this value.
15:0	0h RW/O	**Subsystem Vendor ID (SSVID):** This is written by BIOS. No hardware action taken on this value.

22.1.15 Capabilities Pointer (CAP)—Offset 34h

Capabilities Pointer

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 23
Function: 0

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
7:0	80h RW/L	**Capability Pointer (CP):** Indicates that the first capability pointer offset is 80h. Note: Refer to SATAGC.REGLOCK description in order to lock the register to become RO. This register is not reset by FLR.

22.1.16 Interrupt Information (INTR)—Offset 3Ch

Interrupt Information

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 100h

Bit Range	Default & Access	Field Name (ID): Description
15:8	1h RW/O	**Interrupt Pin (IPIN):** This register tells which interrupt pin the device function uses. A value of 1 corresponds to INTA#. A value of 2 corresponds to INTB#. A value of 3 corresponds to INTC#. A value of 4 corresponds to INTD#. This register is not reset by FLR.
7:0	0h RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register. Interrupt Line register is not reset by FLR.

22.1.17 PCI Power Management Capability ID (PID)—Offset 70h

PCI Power Management Capability ID

Access Method

Type: CFG Register (Size: 16 bits)
Device: 23
Function: 0

Default: A801h

Bit Range	Default & Access	Field Name (ID): Description
15:8	A8h RW/L	**Next Capability (NEXT):** A8h is the location of the Serial ATA capability structure. Note: Refer to the SGC.REGLOCK description in order to lock the register to become RO.
7:0	1h RO	**Cap ID (CID):** Indicates that this pointer is a PCI power management capability.

22.1.18 PCI Power Management Capabilities (PC)—Offset 72h

PCI Power Management Capabilities

Access Method

Type: CFG Register (Size: 16 bits)
Device: 23
Function: 0

Default: 4003h

Bit Range	Default & Access	Field Name (ID): Description
15:11	8h RO	**PME_Support (PME_SUPPORT):** The default value 01000 which indicates PME# can be generated from the D3HOT state in the SATA controller.
10	0h RO	**D2_Support (D2_SUPPORT):** The D2 state is not supported.
9	0h RO	**D1_Support (D1_SUPPORT):** The D1 state is not supported.
8:6	0h RO	**Aux_Current (AUX_CURRENT):** PME# from D3COLD state is not supported, therefore this field is 000b.
5	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
4	0h RO	Reserved.
3	0h RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
2:0	3h RO	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification.

22.1.19 PCI Power Management Control And Status (PMCS)—Offset 74h

PCI Power Management Control And Status

Access Method

Type: CFG Register (Size: 16 bits)
Device: 23
Function: 0

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C/V	**PME Status (PMES):** Bit is set when a PME event is to be requested, and if this bit and PMEE is set, a PME# will be generated from the SATA controller.
14:9	0h RO	Reserved.
8	0h RW	**PME Enable (PMEE):** When set, the SATA controller asserts PME# when exiting D3HOT on a wake event. Note: Software is advised to clear PMEE and PMES together prior to changing CC.SCC through MAP.SMS.
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset (NSFRST):** These bits are used to indicate whether devices transitioning from D3HOT state to D0 state will perform an internal reset. 0 = Device transitioning from D3HOT state to D0 state perform an internal reset. 1 = Device transitioning from D3HOT state to D0 state do not perform an internal reset. Configuration content is preserved. Upon transition from the D3HOT state to D0 state initialized state, no additional operating system intervention is required to preserve configuration context beyond writing to the PowerState bits. Regardless of this bit, the controller transition from D3HOT state to D0 state by a system or bus segment reset will return to the state D0 uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	Reserved.
1:0	0h RW	**Power State (PS):** These bits are used both to determine the current power state of the SATA controller and to set a new power state. 00 = D0 state 11 = D3HOT state When in the D3HOTstate, the controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked.

22.1.20 Message Signalled Interrupt Identifier (MID)—Offset 80h

Message Signalled Interrupt Identifier

Access Method

Type: CFG Register (Size: 16 bits)
Device: 23
Function: 0

Default: 7005h

Bit Range	Default & Access	Field Name (ID): Description
15:8	70h RW/L	**Next Pointer (NEXT):** Indicates the next item in the list is the PCI power management pointer. BIOS may program this field to A8h indicating that the next item is Serial ATA Capability Structure. Note: Refer the SGC.REGLOCK description in order to lock the register to become RO.
7:0	5h RO	**Capability ID (CID):** Capabilities ID indicates MSI.

22.1.21 Message Signalled Interrupt Message Control (MC)—Offset 82h

Message Signalled Interrupt Message Control

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7	0h RO	**64-Bit Address Capable (C64):** Capable of generating a 32-bit message only.
6:4	0h RO	**Multiple Message Enable (MME):** When this field is cleared to 000 (and MSIE is set), only a single MSI message will be generated for all SATA ports, and bits [15:0] of the message vector will be driven from MD[15:0].
3:1	0h RO	**Multiple Message Capable (MMC):** Not supported.
0	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. Note that CMD.ID bit has not effect on MSI. Software must clear this bit to 0 to disable MSI first before changing the number of messages allocated in the MMC field.

22.1.22 Message Signalled Interrupt Message Address (MA)—Offset 84h

Message Signalled Interrupt Message Address

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Address (ADDR):** Lower 32 bits of the system specified message address, always DWORD aligned.
1:0	0h RO	Reserved.

22.1.23 Message Signalled Interrupt Message Data (MD)—Offset 88h

Message Signalled Interrupt Message Data

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 23 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word of the data bus of the MSI memory write transaction.

22.1.24 Port Mapping Register (MAP)—Offset 90h

Port Mapping Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 23 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW/O	**SATA Port 1 Disable (SPD1):** Similar to SPD0 but for port 1. This bit is only applicable to project(s) that has port 1 physically.
16	0h RW/O	**SATA Port 0 Disable (SPD0):** A 1 prevents the SATA port from being enabled via config PCS.PxE. Write of 1 to PCS.PxE has no effect when the corresponding SPD[x] bit is 1. In preventing a port(s) from being enabled, BIOS shall first configure MAP.SPDx. And only then BIOS configures the PCS.PxE. This bit is only applicable to project(s) that has port 0 physically.
15:8	0h RO	Reserved.
7:0	0h RW	**Port Clock Disable (PCD):** When any of these bits is set to 1, the clock driven to the associated port logic is gated and will not toggle. When this bit is cleared to 0, all clocks to the associated port logic will operate normally. Assignment of the bits is: Bit 0: Port 0 Bit 1: Port 1 ... Bit 7: Port 7 NOTE: if a port is not available, the bit is not applicable and reserved.

22.1.25 Port Control And Status (PCS)—Offset 94h

By default, the SATA ports are set (by hardware) to the disabled state (e.g. bits[5:0] == '0') as a result of an initial power on reset. When enabled by software, the ports can transition between the on, partial, and slumber states and can detect devices. When disabled, the port is in the off state and cannot detect any devices. Note: This register is not reset by FLR. Note: AHCI specific notes: If an AHCI-aware or RAID enabled operating system is being booted then system BIOS shall insure that all

supported SATA ports are enabled prior to passing control to the OS. Once the AHCI aware OS is booted it becomes the enabling/disabling policy owner for the individual SATA ports. This is accomplished by manipulating a port's PxSCTL.DET and PxCMD.SUD fields. Because an AHCI or RAID aware OS will typically not have knowledge of the PxE bits and because the PxE bits act as Initiator on/off switches for the ports, pre-boot software must insure that these bits are set to '1' prior to booting the OS, regardless as to whether or not a device is currently on the port.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RO/V	**Port 1 Present (P1P):** This bit is set when COMINIT is received as a response to COMRESET. 0 = No device detected. 1 = The presence of a device on Port 1 has been detected. The status of this bit may change at any time. This bit is cleared when the port is disabled using P1E. This bit is not cleared upon surprise removal of a device.
16	0h RO/V	**Port 0 Present (P0P):** This bit is set when COMINIT is received as a response to COMRESET. 0 = No device detected. 1 = The presence of a device on Port 0 has been detected. The status of this bit may change at any time. This bit is cleared when the port is disabled using P0E. This bit is not cleared upon surprise removal of a device.
15:2	0h RO	Reserved.
1	0h RW/V	**Port 1 Enabled (P1E):** 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. Note: This bit takes precedence over P1CMD.SUD (offset ABAR+198h:bit 1). When MAP.SPD[1] is 1, this is reserved and is read-only 0.
0	0h RW/V	**Port 0 Enabled (P0E):** 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. Note: This bit takes precedence over P0CMD.SUD (offset ABAR+118h:bit 1). When MAP.SPD[0] is 1, this is reserved and is read-only 0.

22.1.26 SATA General Configuration (SATAGC)—Offset 9Ch

SATA General Configuration

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/O	**Register Lock (REGLOCK):** 0 = Will not lock CAP.CP, PID.NEXT, MID.NEXT, or SATACR0.NEXT 1 = Setting this bit will lock CAP.CP, PID.NEXT, MID.NEXT, and SATACR0.NEXT. Once locked, these register bits will become RO. BIOS is requested to program this field to '1' prior to OS handoff. Note: This field is not reset by FLR.
30:16	0h RO	Reserved.
15	0h RW	**Data Phase Parity Error Enable (DPPEE):** When '1', IOSF data phase parity error handling is enabled. When '0', the data phase parity error handling is disabled. Note: This field is not reset by FLR.
14:12	0h RW	**Write Request_Size Select/Max_Payload_Size (WRRSELMPS):** These two bits select the max write request size that SATA host controller will initiate for DMA write to memory. SATA host controller will internally break up larger write request based on these bits. The request is address-aligned to the selected size. Defined encodings for this field are: 000b = 128 address aligned bytes max payload size 111b = 64 address aligned bytes max payload size. All other values are reserved for SATA host controller. Note: This field is not reset by FLR (not supported).
11	0h RW	**Command Parity Error Enable (CPEE):** When '1', command parity error handing is enable. When '0' the command parity error handling is disabled. Note: This field is not reset by FLR.
10	0h RW	**SATA Controller Function Disable (SCFD):** BIOS program this bit to 1 to disable the SATA Controller function. When 0, SATA Controller function is enabled. When disable, SATA Host Controller will not claimed the register access targeting its Configuration Space. In IOSF primary Fabric Decode scheme, it's expected BIOS also program the corresponding bit used by the Fabric Decoder accordingly hence both SATA SIP and Fabric Decoder are in sync, and BIOS need to program this bit before programming the one in Fabric Decoder. Once this bit is set, BIOS isnot able to revert it back to Function Enable until next round of platform reset. This register field is not reset by FLR.
9	0h RW	**Unsupported Request Reporting Enable (URRE):** If set to 1 by software, it allows reporting of an Unsupported Request as a system error. If both URRE and PCI configuration SERR# Enable registers are set to a 1, then the agent must set the Signaled System Error bit in the PCI Status register and send a DO_SERR message in IOSF-SB interface.
8	0h RW/1C/V	**Unsupported Request Detected (URD):** Set to 1 by hardware upon detecting an Unsupported Request on IOSF Primary interface that is not considered Advisory Non-Fatal. Cleared to 0 by SW. URD bit is only set based on IOSF primary bus interface activity. Its not set based on IOSF sideband bus interface activity.
7	0h RW/O	**Alternate ID Enable (AIE):** 0 = Clearing this bit when in RAID mode, the SATA Controller located at Device 23: Function 0 will report its Device ID as 2822h for Desktop SKUs or 282Ah for Mobile SKUs of the PCH. Clearing this bit is required for the Intel® Rapid Storage Technology driver (including the Windows* Vista operating system and later in-box version of the driver) to load on the platform. Intel® Smart Response Technology also requires that the bit be cleared in order to be enabled on the platform. 1 = Setting this bit when in RAID mode, the SATA Controller located at Device 23: Function 0 will report its Device ID as A107h for Desktop SKUs or 9D07h for Mobile SKUs of the Chipset. This setting will prevent the Intel® Rapid Storage Technology driver (including the Windows* operating system in-box version of the driver) from loading on the platform. During the Windows* OS installation, the user will be required to "load" (formerly done by pressing the F6 button on the keyboard) the appropriate RAID storage driver that is enabled by this setting. Note: BIOS is recommended to program this bit prior to programming the MAP.SMS field to reflect RAID. This field is reset by PLTRST# and BIOS is required to reprogram the value (either 0 or 1) after resuming from S3, S4 or S5. This insures that the value is properly and cannot be changed during runtime. Note: This field is not reset by FLR (not supported).
6	0h RW/O/V	**AIE0 DevID Selection (DEVIDSEL):** This register allows BIOS to select Device ID when AIE=0. This bit only has effect in Desktop SKU. In Mobile SKU this bit has no effect at all. Refer to config register offset 09h PI for usage. 0 : 2822h 1 : 2826h Note: This field is not reset by FLR.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/O	**FLR Capability Selection (FLRCSSEL):** This allows the FLR Capability to be bypassed. Refer to config offset B0h. BIOS is required to program this bit to 1 and config offset A8h SATACR0.NEXT to 00h. Note: This field is not reset by FLR.
4:3	0h RW/O	**MXTBA Size Select (MSS):** These 2 bits select the size of the Memory space for the MSI-X Table defined in BAR 0 (Configuration space offset 10h). MSS[1:0] MSI-X Table Memory space size 00 32K 01 16K 10 8K 11 Reserved Note: This field is not reset by FLR (not supported).
2:0	0h RW/O	**ABAR Size Select (ASSEL):** These 3 bits select the size of the Memory space for the ABAR in BAR 5 (Configuration space offset 24h). ASSEL[2:0] ABAR Memory space size 000 2K 001 16K 010 32K 011 64K 100 128K 101 256K 110 512K 111 Reserved Note: This field is not reset by FLR (not supported).

22.1.27 SATA Initialization Register Index (SIRI)—Offset A0h

SATA Initialization Register Index

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RW	**Index (IDX):** 6-bit index pointer into the 256-byte space. Data is written into the SIRD (DFTD) register and read from the SIRD register. This point to a DWord register. The byte enables on the SIRD register affect what will be written.
1:0	0h RO	Reserved.

22.1.28 SATA Initialization Register Data (SIRD)—Offset A4h

SATA Initialization Register Data

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Data (DTA):** 32-bit data value that is written to the register pointed to by SIRI, or read from the register pointed to by SIRI.

22.1.29 Serial ATA Capability Register 0 (SATACR0)—Offset A8h

The SATACR0.NEXT is not changed from RO to become RWO because there is an existing method (SATAGC.FLRCSSEL bit) to bypass the FLR Capability structure, and since the FLR Capability ID.NEXT is already indicating end of capability structure, it does not need change to be RWO.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 23
Function: 0

Default: 100012h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	1h RO	**Major Revision (MAJREV):** Major revision number of the SATA Capability Pointer implemented.
19:16	0h RO	**Minor Revision (MINREV):** Minor revision number of the SATA Capability Pointer implemented.
15:8	0h RW/L	**Next Capability Pointer (NEXT):** 00h indicating the final item in the Capability List. The RW/L register attribute allows for flexibility in determining the capability structure available in this PCI function. Refer to SATAGC.REGLOCK description in order to lock the register to become RO. This register is not reset by FLR.
7:0	12h RO	**Capability ID (CAP):** The value of 12h has been assigned by the PCI SIG to designate the SATA Capability pointer.

22.1.30 Serial ATA Capability Register 1 (SATACR1)—Offset ACh

Serial ATA Capability Register 1

Access Method

Type: CFG Register (Size: 32 bits)
Device: 23
Function: 0

Default: 48h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:4	4h RO	**BAR Offset (BAROFST):** Indicates the offset into the BAR where the Index/Data pair are located (in DWord granularity). The Index and Data I/O registers are located at offset 10h within the I/O space defined by LBAR. A value of 004h indicates offset 10h. 000h = 0h offset 001h = 4h offset 002h = 8h offset 003h = Bh offset 004h = 10h offset ... FFFh = 3FFFh offset (maximum 16KB)
3:0	8h RO	**BAR Location (BARLOC):** Indicates the absolute PCI Configuration register address of the BAR containing the Index/Data pair (in DWord granularity). The Index and Data I/O registers reside within the space defined by LBAR in the SATA controller. A value of 8h indicates offset 20h, which is LBAR. 0000 - 0011b = reserved 0100b = 10h => BAR0 0101b = 14h => BAR1 0110b = 18h => BAR2 0111b = 1Ch => BAR3 1000b = 20h => LBAR 1001b = 24h => BAR5 1010–1110b = reserved 1111b = Index/Data pair in PCI Configuration space. This is not supported in the PCH.

22.1.31 Scratch Pad (SP)—Offset C0h

Scratch Pad

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data (DT):** This is a read/write register that is available for software to use. No hardware action is taken on this register.

22.1.32 MSI-X Identifiers (MXID)—Offset D0h

MSI-X Identifiers

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 11h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW/L	**Next Pointer (NEXT):** Indicates the next item in the list. This may be other capability pointers or it may be the last item in the list.The RW/L register attribute allows for flexibility in determining the capability structure available in this PCI function. Refer to SATAGC.REGLOCK description in order to lock the register to become RO. This register is not reset by FLR.
7:0	11h RO	**Capability ID (CID):** Capabilities ID indicates this is an MSI-X capability.

22.1.33 MSI-X Message Control (MXC)—Offset D2h

MSI-X Message Control

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**MSI-X Enable (MXE):** If set to '1' and the MSI Enable bit in the MSI Message Control register is cleared to '0', the function is permitted to use MSI-X to request service and is prohibited from using its INTx# pin (if implemented). If cleared to '0', the function is prohibited from using MSI-X to request service.
14	0h RW	**Function Mask (FM):** If set to '1', all of the vectors associated with the function are masked, regardless of their per vector Mask bit states. If cleared to '0', each vector's Mask bit determines whether the vector is masked or not. Setting or clearing the MSI-X Function Mask bit has no effect on the state of the per vector Mask bits.
13:11	0h RO	Reserved.
10:0	0h RO	**Table Size (TS):** This value indicates the size of the MSI-X Table as the value n, which is encoded as n - 1. For example, a returned value of 3h corresponds to a table size of 4..

22.1.34 MSI-X Table Offset And Table BIR (MXT)—Offset D4h

MSI-X Table Offset And Table BIR

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RW/O	**Table Offset (TO):** Used as an offset from the address contained by one of the function's Base Address registers to point to the base of the MSI-X Table. The lower three Table BIR bits are masked off (cleared to 000b) by system software to form a 32-bit Qword-aligned offset.
2:0	0h RO	**Table BIR (TBIR):** This field indicates which one of a function's Base Address registers, located beginning at 10h in Configuration Space, is used to map the function's MSI-X Table into system memory. A read-only value of '0' means 10h.

22.1.35 MSI-X PBA Offset And PBA BIR (MXP)—Offset D8h

MSI-X PBA Offset And PBA BIR

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RW/O	**PBA Offset (PBAO):** Used as an offset from the address contained by one of the function's Base Address registers to point to the base of the MSI-X PBA. The lower three PBA BIR bits are masked off (cleared to 000b) by software to form a 32-bit Qword-aligned offset.
2:0	1h RO	**PBA BIR (PBIR):** This field indicates which one of a function's Base Address registers, located beginning at 10h in Configuration Space, is used to map the function's MSI-X PBA into system memory. A read-only value of '1' means 14h.

22.1.36 BIST FIS Control/Status (BFCS)—Offset E0h

BIST FIS Control/Status

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	0h RW	**Port 2 BIST FIS Initiate (P2BFI):** When a rising edge is detected on this bit field, the PCH initiates a BIST FIS to the device on Port 2,using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 2 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PCS.P2E prior to attempting additional BIST FISes or to return the PCH to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P2BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully. Note: Bit may be Reserved depending on if port is available in the given SKU.
11	0h RW/1C/V	**BIST FIS Successful (BFS):** 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set any time a BIST FIS transmitted by PCH receives an R_OK completion status from the device. Note: This bit must be cleared by software prior to initiating a BIST FIS.
10	0h RW/1C/V	**BIST FIS Failed (BFF):** 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set any time a BIST FIS transmitted by PCH receives an R_ERR completion status from the device. Note: This bit must be cleared by software prior to initiating a BIST FIS.
9	0h RW	**Port 1 BIST FIS Initiate (P1BFI):** When a rising edge is detected on this bit field, the PCH initiates a BIST FIS to the device on Port 1,using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 1 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PCS.P1E prior to attempting additional BIST FISes or to return the PCH to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P1BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully.
8	0h RW	**Port 0 BIST FIS Initiate (P0BFI):** When a rising edge is detected on this bit field, the PCH initiates a BIST FIS to the device on Port 0,using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 0 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PCS.P0E prior to attempting additional BIST FISes or to return the PCH to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P0BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully.
7:2	0h RW	**BIST FIS Parameters (BFP):** These 6 bits form the contents of the upper 6 bits of the BIST FIS Pattern Definition in any BIST FIS transmitted by the PCH. This field is not port specific—its contents will be used for any BIST FIS initiated on port 0, port 1, port 2, or port 3. The specific bit definitions are: Bit 7: T – Far End Transmit mode Bit 6: A – Align Bypass mode Bit 5: S – Bypass Scrambling Bit 4: L – Far End Retimed Loopback Bit 3: F – Far End Analog Loopback Bit 2: P – Primitive bit for use with Transmit mode
1:0	0h RO	Reserved.

22.1.37 BIST FIS Transmit Data 1 (BFTD1)—Offset E4h

BIST FIS Transmit Data 1

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data (DATA):** The data programmed into this register will form the contents of the second DW of any BIST FIS initiated by the SATA controller. This register is not port specific - its contents will be used for BIST FIS initiated on any port. Although the 2nd and 3rd DWs of the BIST FIS are only meaningful when the T bit of the BIST FIS is set to indicate Far-End Transmit mode, this register's contents will be transmitted as the BIST FIS 2nd DW regardless of whether or not the T bit is indicated in the BFCS register.

22.1.38 BIST FIS Transmit Data 2 (BFTD2)—Offset E8h

BIST FIS Transmit Data 2

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data (DATA):** The data programmed into this register will form the contents of the third DW of any BIST FIS initiated by the SATA controller. This register is not port specific - its contents will be used for BIST FIS initiated on any port. Although the 2nd and 3rd DWs of the BIST FIS are only meaningful when the T bit of the BIST FIS is set to indicate Far-End Transmit mode, this register's contents will be transmitted as the BIST FIS 3rd DW regardless of whether or not the T bit is set in the BFCS register.

22.2 SATA ABAR Registers

Table 22-2. Summary of SATA ABAR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	HBA Capabilities (GHC_CAP)—Offset 0h	FF36FF07h
4h	7h	Global HBA Control (GHC)—Offset 4h	80000000h
8h	Bh	Interrupt Status Register (IS)—Offset 8h	0h
Ch	Fh	Ports Implemented (GHC_PI)—Offset Ch	0h
10h	13h	AHCI Version (VS)—Offset 10h	10301h
1Ch	1Fh	Enclosure Management Location (EM_LOC)—Offset 1Ch	1600002h
20h	23h	Enclosure Management Control (EM_CTL)—Offset 20h	7010000h
24h	27h	HBA Capabilities Extended (GHC_CAP2)—Offset 24h	3Ch
A0h	A3h	Vendor Specific (VSP)—Offset A0h	48h
A4h	A7h	Vendor Specific Capabilities Register (VS_CAP)—Offset A4h	1002DEh
C0h	C3h	RAID Platform ID (RPID)—Offset C0h	311C02h
C4h	C5h	Premium Feature Block (PFB)—Offset C4h	0h
C8h	C9h	SW Feature Mask (SFM)—Offset C8h	3Fh
100h	103h	Port 0 Command List Base Address (P0CLB)—Offset 100h	0h
104h	107h	Port 0 Command List Base Address Upper 32-bits (P0CLBU)—Offset 104h	0h

Table 22-2. Summary of SATA ABAR Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
108h	10Bh	Port 0 FIS Base Address (P0FB)—Offset 108h	0h
10Ch	10Fh	Port 0 FIS Base Address Upper 32-bits (P0FBU)—Offset 10Ch	0h
110h	113h	Port 0 Interrupt Status (P0IS)—Offset 110h	0h
114h	117h	Port 0 Interrupt Enable (P0IE)—Offset 114h	0h
118h	11Bh	Port 0 Command (P0CMD)—Offset 118h	4h
120h	123h	Port 0 Task File Data (P0TFD)—Offset 120h	9h
124h	127h	Port 0 Signature (P0SIG)—Offset 124h	FFFFFFFFh
128h	12Bh	Port 0 Serial ATA Status (P0SSTS)—Offset 128h	0h
12Ch	12Fh	Port 0 Serial ATA Control (P0SCTL)—Offset 12Ch	0h
130h	133h	Port 0 Serial ATA Error (P0SERR)—Offset 130h	0h
134h	137h	Port 0 Serial ATA Active (P0SACT)—Offset 134h	0h
138h	13Bh	Port 0 Command Issue (P0CI)—Offset 138h	0h
144h	147h	Port 0 Device Sleep (P0DEVSLP)—Offset 144h	1E022852h
180h	183h	Port 1 Command List Base Address (P1CLB)—Offset 180h	0h
184h	187h	Port 1 Command List Base Address Upper 32-bits (P1CLBU)—Offset 184h	0h
188h	18Bh	Port 1 FIS Base Address (P1FB)—Offset 188h	0h
18Ch	18Fh	Port 1 FIS Base Address Upper 32-bits (P1FBU)—Offset 18Ch	0h
190h	193h	Port 1 Interrupt Status (P1IS)—Offset 190h	0h
194h	197h	Port 1 Interrupt Enable (P1IE)—Offset 194h	0h
198h	19Bh	Port 1 Command (P1CMD)—Offset 198h	0h
1A0h	1A3h	Port 1 Task File Data (P1TFD)—Offset 1A0h	0h
1A4h	1A7h	Port 1 Signature (P1SIG)—Offset 1A4h	0h
1A8h	1ABh	Port 1 Serial ATA Status (P1SSTS)—Offset 1A8h	0h
1ACh	1AFh	Port 1 Serial ATA Control (P1SCTL)—Offset 1ACh	0h
1B0h	1B3h	Port 1 Serial ATA Error (P1SERR)—Offset 1B0h	0h
1B4h	1B7h	Port 1 Serial ATA Active (P1SACT)—Offset 1B4h	0h
1B8h	1BBh	Port 1 Command Issue (P1CI)—Offset 1B8h	0h
1C4h	1C7h	Port 1 Device Sleep (P1DEVSLP)—Offset 1C4h	0h

22.2.1 HBA Capabilities (GHC_CAP)—Offset 0h

HBA Capabilities. This register indicates basic capabilities of the HBA to driver software. The RWO bits in this register are only cleared upon PLTRST#. This register is not reset by FLR.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 23
Function: 0

Default: FF36FF07h

Bit Range	Default and Access	Field Name (ID): Description
31	1h RW/O	**Supports 64-bit Addressing (S64A):** Indicates that the SATA controller can access 64-bit data structures. The 32-bit upper bits of the port DMA Descriptor, the PRD Base, and each PRD entry are read/write.
30	1h RW/O	**Supports Native Command Queuing Acceleration (SCQA):** When set to 1, indicates that the SATA controller supports SATA command queuing using the DMA Setup FIS. The PCH handles DMA Setup FISes natively, and can handle auto-activate optimization through that FIS.
29	1h RW/O	**Supports SNotification Register (SSNTF):** When set to 1, indicates the SATA controller supports the PxSNTF (SNotification) register and its associated functionality. When cleared to 0, the SATA controller does not support the PxSNTF (SNotification) register and its associated functionality.
28	1h RW/O	**Supports Mechanical Presence Switch (SMPS):** When set to 1, indicates whether the SATA controller supports mechanical presence switches on its ports for use in hot-plug operations. This value is loaded by platform BIOS prior to operating system initialization. If this bit is set, BIOS must also map the SATAGP pins to the SATA controller through GPIO space.
27	1h RW/O	**Supports Staggered Spin-up (SSS):** Indicates whether the SATA controller supports staggered spin-up on its ports, for use in balancing power spikes. This value is loaded by platform BIOS prior to OS initialization. 0 = Staggered spin-up not supported. 1 = Staggered spin-up supported.
26	1h RW/O	**Supports Aggressive Link Power Management (SALP):** 0 = Software shall treat the PxCMD.ALPEand PxCMD.ASP bits as reserved. 1 = The SATA controller supports auto-generating link requests to the partial or slumber states when there are no commands to process.
25	1h RW/O	**Supports Activity LED (SAL):** Indicates the SATA controller supports a single output pin (SATALED#) which indicates activity.
24	1h RW/O	**Supports Command List Override (SCLO):** When set to 1, indicates that the HBA supports the PxCMD.CLO bit and it's associated function. When cleared to 0., The HBA is not capable of clearing the BSY and DRQ bits in the Status register in order to issue a software reset if these bits are still set from a previous operation.
23:20	3h RW/O	**Interface Speed Support (ISS):** Indicates the maximum speed the SATA controller can support on its ports. 1h = 1.5Gb/s 2h = 3Gb/s 3h = 6Gb/s The default of this field is dependent upon the PCH SKU. If at least one PCH SATA port supports 6Gb/s, the default will be 3h. If no PCH SATA ports support 6Gb/s, then the default will be 2h and writes of 3h will be ignored by the PCH. Refer to Volume 1, Chapter 1 for details on 6Gb/s port availability.
19	0h RO	Reserved.
18	1h RO	**Supports AHCI mode only (SAM):** The SATA controller may optionally support AHCI access mechanism only. 0 = SATA controller supports both IDE and AHCI Modes 1 = SATA controller supports AHCI Mode Only Note: BIOS should program this field as “1” since IDE mode is not supported.
17	1h RO	**Supports Port Multiplier (SMP):** Not supported.
16	0h RO	Reserved.
15	1h RO	**PIO Multiple DRQ Block (PMD):** Hardwired to 1. The SATA controller supports PIO Multiple DRQ Command Block.
14	1h RW/O	**Slumber State Capable (SSC):** When set to 1, the SATA controller supports the slumber state.
13	1h RW/O	**Partial State Capable (PSC):** When set to 1, the SATA controller supports the partial state.
12:8	1Fh RO	**Number of Command Slots (NCS):** Hardwired to 1Fh to indicate support for 32 slots.

Bit Range	Default and Access	Field Name (ID): Description
7	0h RO	**Command Completion Coalescing Supported (CCCS):** 0 = Command Completion Coalescing Not Supported 1 = Command Completion Coalescing Supported
6	0h RO	**Enclosure Management Supported (EMS):** 0 = Enclosure Management Not Supported 1 = Enclosure Management Supported
5	0h RW/O	**Supports External SATA (SXS):** 0 = External SATA is not supported on any ports 1 = External SATA is supported on one or more ports When set, software can examine each SATA port's Command register (PxCMD.ESP) to determine which port is routed externally.
4:0	7h RO	**Number of Ports (NP):** Indicates number of supported ports. The number of ports indicated in this field may be more than the number of ports indicated in the PI (ABAR + 0Ch) register. Field value dependent on number of ports available in a given SKU.

22.2.2 Global HBA Control (GHC)—Offset 4h

Global HBA Control. This register controls various global actions of the HBA.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 23

Function: 0

Default: 80000000h

Bit Range	Default and Access	Field Name (ID): Description
31	1h RO	**AHCI Enable (AE):** When set, indicates that an AHCI driver is loaded and communication to the HBA shall be via AHCI mechanisms. This can be used by an HBA that supports both legacy mechanisms (such as SFF-8038i) and AHCI to know when the HBA is running under an AHCI driver. 0 = Software will only communicate with the HBA using legacy mechanisms. 1 = Software shall only talk to the HBA using AHCI. The HBA will not have to allow command processing via both AHCI and legacy mechanisms. Note: Software shall set this bit to 1 before accessing other AHCI registers. Note: The implementation of this bit is dependent upon the value of the CAP.SAM bit. If CAP.SAM is '0', then GHC.AE should be RW and shall have a reset value of '0'. If CAP.SAM is '1', then GHC.AE shall be read only and shall have a reset value of '1'.
30:3	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
2	0h RO	**MSI Revert to Single Message (MRSM):** When set to 1 by hardware, indicates that the HBA requested more than one MSI vector but has reverted to using the first vector only. When this bit is cleared to 0, the HBA has not reverted to single MSI mode (i.e. hardware is already in single MSI mode, software has allocated the number of messages requested, or hardware is sharing interrupt vectors if MC.MME < MC.MMC). The HBA may revert to single MSI mode when the number of vectors allocated by the host is less than the number requested. This bit shall only be set to 1 when the following conditions hold: MC.MSIE = 1 (MSI is enabled) MC.MMC > 0 (multiple messages requested) MC.MME > 0 (more than one message allocated) MC.MME != MC.MMC (messages allocated not equal to number requested) When this bit is set to 1, single MSI mode operation is in use and software is responsible for clearing bits in the IS register to clear interrupts. This bit shall be cleared to 0 by hardware when any of the four conditions stated is false. This bit is also cleared to 0 when MC.MSIE = 1 and MC.MME = 0h. In this case, the hardware has been programmed to use single MSI mode, and is not reverting to that mode. For PCH, the HBA shall always revert to single MSI mode when the number of vectors allocated by the host is leass than the number requested. Value of MRSM is a don't care when GHC.HR=1.
1	0h RW	**Interrupt Enable (IE):** This global bit enables interrupts from the PCH. 0 = All interrupt sources from all ports are disabled. 1 = Interrupts are allowed from the AHCI controller.
0	0h RW/1S	**HBA Reset (HR):** Resets the PCH AHCI controller. 0 = No effect. 1 = When set by software, this bit causes an internal reset of the PCH AHCI controller. All state machines that relate to data transfers and native command queuing will return to an idle condition, and all ports are re-initialized using COMRESET.

22.2.3 Interrupt Status Register (IS)—Offset 8h

Interrupt Status Register. This register indicates which of the ports within the controller have an interrupt pending and require service.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 23

Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW/1C	**Interrupt Pending Status Port 2 (IPS2):** This bit is only applicable to system that has Port 2 physically. 0 = No interrupt pending. 1 = Port 2 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt
1	0h RW/1C	**Interrupt Pending Status Port 1 (IPS1):** This bit is only applicable to system that has Port 1 physically. 0 = No interrupt pending. 1 = Port 1 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.
0	0h RW/1C	**Interrupt Pending Status Port 0 (IPS0):** This bit is only applicable to system that has Port 0 physically. 0 = No interrupt pending. 1 = Port 0 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.

22.2.4 Ports Implemented (GHC_PI)—Offset Ch

Ports Implemented. This register indicates which ports are exposed to the HBA. It is loaded by platform BIOS. It indicates which ports that the device supports are available for software to use. Any available port may not be implemented. This register is not reset by FLR. There is BIOS programming requirement on the PI register.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW/O	**Port 2 Implemented (PI2):** 0 = The port is not implemented. 1 = The port is implemented. Note: This bit may be Reserved and is RO '0' depending on if port is available in the given SKU. Refer to Volume 1, Chapter 1 for details if port is available.
1	0h RW/O	**Port 1 Implemented (PI1):** 0 = The port is not implemented. 1 = The port is implemented.
0	0h RW/O	**Port 0 Implemented (PI0):** 0 = The port is not implemented. 1 = The port is implemented.

22.2.5 AHCI Version (VS)—Offset 10h

AHCI Version. This register indicates the major and minor version of the AHCI specification. It is BCD encoded. The upper two bytes represent the major version number, and the lower two bytes represent the minor version number. Example: Version 3.12 would be represented as 00030102h.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 10301h

Bit Range	Default and Access	Field Name (ID): Description
31:16	1h RO	**Major Version Number (MJR):** Indicates the major version is 1
15:0	301h RO	**Minor Version Number (MNR):** Indicates the minor version is 30

22.2.6 Enclosure Management Location (EM_LOC)—Offset 1Ch

Enclosure Management Location. The enclosure management location register identifies the location and size of the enclosure management message buffer. This register is not implemented if enclosure management is not supported (i.e. CAP.EMS = 0).

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 1600002h

Bit Range	Default and Access	Field Name (ID): Description
31:16	160h RO	**Offset (OFST):** The offset of the message buffer in Dwords from the beginning of the ABAR.
15:0	2h RO	**Buffer Size (SZ):** Specifies the size of the transmit message buffer area in Dwords. If both transmit and receive buffers are supported, then the transmit buffer begins at ABAR[EM_LOC.OFST*4] and the receive buffer directly follows it. If both transmit and receive buffers are supported, both buffers are of the size indicated in the Buffer Size field. A value of 0 is invalid. Note that SATA controller only supports transmit buffer.

22.2.7 Enclosure Management Control (EM_CTL)—Offset 20h

Enclosure Management Control. This register is used to control and obtain status for the enclosure management interface. The register incluldes information on the attributes of the implementation, enclosure management messages supported, the status of the interface, whether any messages are pending, and is used to initiate sending messages. This register is not implemented if enclosure management is not supported (i.e. CAP.EMS = 0).

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 7010000h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27	0h RO	**Port Multiplier Support (ATTR_PM):** The HBA does not support enclosure management messages for devices attached via a Port Multiplier. Software should use the Serial ATA enclosure management bridge that is built into many Port Multipliers for enclosure services with these devices. For more information on Serial ATA enclosure management bridges, refer to the Serial ATA II: Extensions to Serial ATA 1.0a revision 1.2 specification.
26	1h RW/O	**Activity LED Hardware Driven (ATTR_ALHD):** If set to 1, the HBA drives the activity LED for the LED message type in hardware and does not utilize software settings for this LED. The HBA does not begin transmitting the hardware based activity signal until after software has written CTL.TM=1 after a reset condition.
25	1h RO	**Transmit Only (ATTR_XMT):** If set to 1, the HBA only supports transmitting messages and does not support receiving messages. If cleared to 0, the HBA supports transmitting and receiving messages.

Bit Range	Default and Access	Field Name (ID): Description
24	1h RO	**Single Message Buffer (ATTR_SMB):** If set to 1, the HBA has one message buffer that is shared for messages to transmit and messages received. In this case, unsolicited receive messages are not supported and it is software's responsibility to manage access to this buffer. If cleared to 0, there are separate receive and transmit buffers such that unsolicited messages could be supported.
23:20	0h RO	Reserved.
19	0h RO	**SGPIO Enclosure Management Messages (SUPP_SGPIO):** If set to 1, the HBA supports the SGPIO register interface message type.
18	0h RO	**SES-2 Enclosure Management Messages (SUPP_SES2):** If set to 1, the HBA supports the SES-2 message type.
17	0h RO	**SAF-TE Enclosure Management Messages (SUPP_SAFTE):** If set to 1, the HBA supports the SAF-TE message type.
16	1h RO	**LED Message Types (SUPP_LED):** If set to 1, the HBA supports the LED message type defined in LED Message Type.
15:10	0h RO	Reserved.
9	0h RW/1S	**Reset (RST):** When set to 1 by software, the HBA shall reset all enclosure management message logic and take all appropriate reset actions to ensure messages can be transmitted/received after the reset. After the HBA completes the reset operation, the HBA shall set the value to 0. A write of 0 by software to this field shall have no effect.
8	0h RW/1S	**Transmit Message (CTL_TM):** When set to 1 by software, the HBA shall transmit the message contained in the message buffer. When the message is completely sent, the HBA shall clear this bit to 0. A write of 0 to this bit by software shall have no effect. Software shall not change the contents of the message buffer while CTL.TM is set to 1.
7:1	0h RO	Reserved.
0	0h RO	**Message Received (STS_MR):** Message received is not supported.

22.2.8 HBA Capabilities Extended (GHC_CAP2)—Offset 24h

HBA Capabilities Extended. This register indicates basic capabilities of the HBA to driver software. The RWO bits in this register are only cleared upon PLTRST#. This register is not reset by FLR.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 23
Function: 0

Default: 3Ch

Bit Range	Default and Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5	1h RW/O	**DEVSLP Entrance from Slumber Only (DESO):** This bit specifies that the HBA shall only assert DEVSLP if the interface is in Slumber. 0 = The host may enter DEVSLP from any link state (active, Partial, or Slumber). 1 = The host shall ignore software directed entrance to DEVSLP by means of PxCMD.ICC bit unless PxSSTS.IPM = 6h.
4	1h RW/O	**Supports Aggressive DEVSLP Management (SADM):** 0 = Aggressive DEVSLP Management is not supported and software shall treat the PxDEVSLP.ADSE field as reserved. 1 = The host supports hardware assertion of the DEVSLP signal after the idle timeout expires.
3	1h RW/O	**Supports DEVSLP (SDS):** 0 = DEVSLP is not supported. 1 = Supports the DEVSLP feature.
2	1h RW/O	**Automatic Partial to Slumber Transitions (APST):** 0 = Automatic Partial to Slumber Transition is not supported. 1 = Supports Automatic Partial to Slumber Transitions.
1	0h RO	Reserved.
0	0h RO	**BIOS/OS Handoff (BOH):** Not supported.

22.2.9 Vendor Specific (VSP)—Offset A0h

Vendor Specific

Access Method

Type: MEM Register (Size: 32 bits)

Device: 23
Function: 0

Default: 48h

Bit Range	Default and Access	Field Name (ID): Description
31:7	0h RO	Reserved.
6	1h RO	**Software Feature Mask Supported (SFMS):** Set to 1 if the platform is enabled for premium storage features mask (SFM) as described in VS MMIO space at offset ABAR[RPID.(OFST*4)+4].
5	0h RO	**Premium Features Supported (PFS):** Set to 1 if the platform is enabled for premium storage features (PFB) as described in VS MMIO space at offset ABAR[RPID.OFST*4]. Set to 0 if the platform is not enabled for premium storage features.
4	0h RO	**Platform Type (PT):** Set to 1 if mobile platform. Clear (0) if desktop.
3	1h RO	**Supports RAID Platform ID Reporting (SRPIR):** If set to 1, then indicates that the RAID Platform ID is reported via ABAR + C0h. Set to 0 if this ID is not reported via MMIO space.
2:0	0h RO	Reserved.

22.2.10 Vendor Specific Capabilities Register (VS_CAP)—Offset A4h

Vendor Specific Capabilities Register

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 1002DEh

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:16	10h RW/O	**NVM Remapped Register Offset (NRMO):** Specifies the offset (in 128B unit) within ABAR as to where the PCIe NAND memory BAR register space is remapped. For example, NRMO=1 means ABAR + 128B. This allows the remapped offset to shift between ABAR + 0B, and ABAR + 512KK - 128B, with 128B step. The remapped offset into the AHCI memory space must not overlap with the memory space used for SATA. The remapped offset into the AHCI memory space and the remapped size must not exceed the allocated AHCI memory space of the integrated AHCI controller. Only valid when NRMBE = 1. The reset default of this field is 10h, this places the start of the PCIe NAND memory BAR register space at ABAR + 2K. This field is not reset by FLR.
15:13	0h RO	Reserved.
12:1	16Fh RW/O	**Memory Space Limit. (MSL):** This field specifies the size (in 128B unit) of the remapped memory space for the PCIe NAND device. It is a 0-based field. For example, MSL=1 means 256B. This allows the remapped size to shift between 128B and 512K with the step of 128B.Memory BAR offset from 0 to MSL of the PCIe NAND device are remapped under the integrated AHCI controller memory space.The remapped offset into the AHCI memory space and the value programmed in this field must not exceed the allocated AHCI memory space of the integrated AHCI controller. Only valid when NRMBE = 1. The reset default of this field is 16Fh which specifies the size of the remapped memory space as 34k.This field is not reset by FLR.
0	0h RW/O	**PCIe NAND Memory BAR Remapped Enable (NRMBE):** Set to 1 if a PCIe NAND device is present and remapping of its memory BAR register space is enabled. Cleared to 0 if there is no PCIe NAND device present or the remapping of its memory BAR register space is disabled. This bit is not reset by FLR.

22.2.11 RAID Platform ID (RPID)—Offset C0h

RAID Platform ID. This register is used by the Intel Matrix Storage Manager OROM to match the features supported by the OROM with the platform on which the OROM is executing. This prevents the use of an OROM designed for newer chipsets from being use on older chipsets as this could reduce up-sell potential.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 311C02h

Bit Range	Default and Access	Field Name (ID): Description
31:16	31h RO	**Offset (OFST):** The offset of the Premium Feature Block (PFB) in DWords from the beginning of the ABAR. SFM follows directly after PFB.
15:0	1C02h RO	**RAID Platform ID (RPID):** Specifies the DID value that has been assigned to the platform. This is the same DID that is reported by the SATA controller when SATAGC.AIE is set to 1 except that the DID is always reported through this register, regardless if the programming of SATAGC.AIE.

22.2.12 Premium Feature Block (PFB)—Offset C4h

Access Method

Type: MEM Register (Size: 16 bits)
Device: 23
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:5	0h RO	Reserved.
4	0h RO	**Reserved (Reserved):** Read value is the same as VSP.PFS.
3	0h RO	**Reserved (Reserved):** Read value is the same as VSP.PFS.
2	0h RO	**Reserved (Reserved):** Read value is the same as VSP.PFS.
1	0h RO	**Supports Email Alert (SEA):** Read value is the same as VSP.PFS. If set to 1, then this feature is supported as part of the premium feature set.
0	0h RO	**Supports OEM IOCTL (SOI):** Read value is the same as VSP.PFS. If set to 1, then this feature is supported as part of the premium feature set.

22.2.13 SW Feature Mask (SFM)—Offset C8h

SW Feature Mask. The following will be programmed by the BIOS when VS_CAP.SFMS == 1. The feature mask is used by SW to determine which non-premium features shall be supported by SW. These register bits are not reset by FLR since they are programmed by BIOS.

Access Method

Type: MEM Register (Size: 16 bits)
Device: 23
Function: 0

Default: 3Fh

Bit Range	Default and Access	Field Name (ID): Description
15:12	0h RO	Reserved.
11:10	0h RW/O	**OROM UI Normal Delay. (OROM_UI_Normal_Delay):** Values of these bits specify the delay of the OROM UI Splash Screen in a normal status. 00 = 2 secs (default and previous value); 01 = 4 secs; 10 = 6 secs; 11 = 8 secs. If bit 5 == 0, then these values are disregarded.
9	0h RW/O	**Smart Response Technology. (Smart_Response_Technology):** If set to '1', then Smart Response Technology is enabled. If cleared to '0', the feature is disabled.
8	0h RW/O	**RRT Only on ESATA (IRRT_Only_on_ESATA):** If set to 1, then only RRT volumes can span internal and external SATA ports (e.g. eSATA). If cleared to 0, then any RAID volume can span internal and external SATA ports (e.g. eSATA).
7	0h RW/O	**LED Locate (LED_Locate):** If set to 1, then LED/SGPIO hardware is attached and the ping to locate feature is enabled in the OS.
6	0h RW/O	**HDDUNLOCK (HDDUNLOCK):** If set to 1, then HDD password unlock is enabled in the OS.
5	1h RW/O	**OROM UI and BANNER (OROM_UI_and_BANNER):** If set to 1, then the OROM UI is displayed. When cleared to 0, the OROM UI and BANNER are not displayed if all disks and volumes have a normal status.
4	1h RW/O	**RRT (IRRT):** If set to 1, then Rapid Recovery Technology is enabled.
3	1h RW/O	**R5 (R5):** If set to 1, then RAID5 is enabled
2	1h RW/O	**R10 (R10):** If set to 1, then RAID10 is enabled
1	1h RW/O	**R1 (R1):** If set to 1, then RAID1 is enabled
0	1h RW/O	**R0 (R0):** If set to 1, then RAID0 is enabled

22.2.14 Port 0 Command List Base Address (P0CLB)—Offset 100h

Port 0 Command List Base Address

Access Method

Type: MEM Register (Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RW	**Command List Base Address (CLB):** Indicates the 32-bit base for the command list for this port. This base is used when fetching commands to execute. This address must be 1K aligned as indicated by bits 31:10 being read/write. Note that these bits are not reset on a HBA reset.
9:0	0h RO	Reserved.

22.2.15 Port 0 Command List Base Address Upper 32-bits (P0CLBU)—Offset 104h

Port 0 Command List Base Address Upper 32-bits

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Command List Base Address Upper (CLBU):** Indicates the upper 32-bits for the command list base address for this port. This base is used when fetching commands to execute. Note that these bits are not reset on a HBA reset.

22.2.16 Port 0 FIS Base Address (P0FB)—Offset 108h

Port 0 FIS Base Address

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RW	**FIS Base Address (FB):** Indicates the 32-bit base for received FISes. This address must be 256-byte aligned as indicated by bits 31:08 being read/write. When FIS-based switching is in use, this structure is 4KB in length and the address shall be 4KB aligned. Note that these bits are not reset on a HBA reset.
7:0	0h RO	Reserved.

22.2.17 Port 0 FIS Base Address Upper 32-bits (P0FBU)—Offset 10Ch

Port 0 FIS Base Address Upper 32-bits

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**FIS Base Address Upper (FBU):** Indicates the upper 32-bits for the received FIS base for this port. Note that these bits are not reset on a HBA reset.

22.2.18 Port 0 Interrupt Status (P0IS)—Offset 110h

Port 0 Interrupt Status

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	**Cold Presence Detect Status (CPDS):** The SATA controller does not support cold presence detect.
30	0h RW/1C	**Task File Error Status (TFES):** This bit is set whenever the status register is updated by the device and the error bit (bit 0 of the Status field in the received FIS) is set.
29	0h RW/1C	**Host Bus Fatal Error Status (HBFS):** Indicates that the HBA encountered a host bus error that it cannot recover from, such as a bad software pointer. In PCI, such an indication would be a target or Initiator abort.
28	0h RW/1C	**Host Bus Data Error Status (HBDS):** Indicates that the HBA encountered a data error (uncorrectable ECC / parity) when reading from or writing to system memory.
27	0h RW/1C	**Interface Fatal Error Status (IFS):** Indicates that the HBA encountered an error on the SATA interface which caused the transfer to stop.
26	0h RW/1C	**Interface Non-fatal Error Status (INFS):** Indicates that the HBA encountered an error on the SATA interface but was able to continue operation.
25	0h RO	Reserved.
24	0h RW/1C	**Overflow Status (OFS):** Indicates that the HBA received more bytes from a device than was specified in the PRD table for the command.
23	0h RW/1C	**Incorrect Port Multiplier Status (IPMS):** Indicates that the HBA received a FIS from a device whose port multiplier field did not match what was expected. The IPMS bit may be set during emuneration process. It is recommended that IPMS only be used after enumeration is complete on the Port Multiplier.
22	0h RO	**PhyRdy Change Status (PRCS):** When set to one indicates the internal PhyRdy signal changed state. This bit reflects the state of PxSERR.DIAG.N. This bit is RO and is only cleared when PxSERR.DIAG.N is cleared.
21:8	0h RO	Reserved.
7	0h RW/1C	**Device Mechanical Presence Status (DMPS):** When set, indicates that a platform mechanical presence switch has been opened or closed, which may lead to a change in the connection state of the device. This bit is only valid in systems that support mechanical presence switch (CAP.SMPS and PxCMD.MPSP are set).
6	0h RO	**Port Connect Change Status (PCS):** This bit reflects the state of PxSERR.DIAG.X. This bit is only cleared when PxSERR.DIAG.X is cleared. 1 = Change in Current Connect Status. 0 = No change in Current Connect Status.
5	0h RW/1C	**Descriptor Processed (DPS):** A PRD with the I. bit set has transferred all of its data.

Bit Range	Default and Access	Field Name (ID): Description
4	0h RO	**Unknown FIS Interrupt (UFS):** When set to 1 indicates that an unknown FIS was received and has been copied into system memory. This bit is cleared to 0 by software clearing the PxSERR.DIAG.F bit to 0. Note that this bit does not directly reflect the PxSERR.DIAG.F bit. PxSERR.DIAG.F is set immediately when an unknown FIS is detected, whereas this bit is set when the FIS is posted to memory. Software should wait to act on an unknown FIS until this bit is set to 1 or the two bits may become out of sync.
3	0h RW/1C	**Set Device Bits Interrupt (SDBS):** A Set Device Bits FIS has been received with the I. bit set and has been copied into system memory.
2	0h RW/1C	**DMA Setup FIS Interrupt (DSS):** A DMA Setup FIS has been received with the I. bit set and has been copied into system memory.
1	0h RW/1C	**PIO Setup FIS Interrupt (PSS):** A PIO Setup FIS has been received with the I. bit set, it has been copied into system memory, and the data related to that FIS has been transferred. This bit shall be set even if the data transfer resulted in an error.
0	0h RW/1C	**Device to Host Register FIS Interrupt (DHRS):** A D2H register FIS has been received with the I. bit set, and has been copied into system memory.

22.2.19 Port 0 Interrupt Enable (P0IE)—Offset 114h

Port 0 Interrupt Enable

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	**Cold Presence Detect Enable (CPDS):** The SATA controller does not support cold presence detect.
30	0h RW	**Task File Error Enable (TFEE):** When set, GHC.IE is set, and P0S.TFES is set, the HBA shall generate an interrupt.
29	0h RW	**Host Bus Fatal Error Enable (HBFE):** When set, GHC.IE is set, and P0IS.HBFS is set, the HBA shall generate an interrupt.
28	0h RW	**Host Bus Data Error Enable (HBDE):** When set, GHC.IE is set, and P0IS.HBDS is set, the HBA shall generate an interrupt.
27	0h RW	**Interface Fatal Error Enable (IFE):** When set, GHC.IE is set, and P0IS.IFS is set, the HBA shall generate an interrupt.
26	0h RW	**Interface Non-fatal Error Enable (INFE):** When set, GHC.IE is set, and P0IS.INFS is set, the HBA shall generate an interrupt.
25	0h RO	Reserved.
24	0h RW	**Overflow Enable (OFE):** When set, and GHC.IE and P0IS.OFS are set, the HBA shall generate an interupt.
23	0h RW	**Incorrect Port Multiplier Enable (IPME):** When set, and GHC.IE and P0IS.IPMS are set, the HBA shall generate an interupt. BIOS is required to program this field to '0'. The same applies to AHCI driver.
22	0h RW	**PhyRdy Change Interrupt Enable (PRCE):** When set, and GHC.IE is set, and PxIS.PRCS is set, the HBA shall generate an interrupt.

Bit Range	Default and Access	Field Name (ID): Description
21:8	0h RO	Reserved.
7	0h RW	**Device Mechanical Enable (DMPE):** When set, and P0IS.DMPS is set, the HBA shall generate an interrupt.
6	0h RW	**Port Change Interrupt Enable (PCE):** When set, GHC.IE is set, and P0IS.PCS is set, the HBA shall generate an interrupt.
5	0h RW	**Descriptor Processed Interrupt Enable (DPE):** When set, GHC.IE is set, and P0IS.DPS is set, the HBA shall generate an interrupt.
4	0h RW	**Unknown FIS Interrupt Enable (UFE):** When set, GHC.IE is set, and PxIS.UFS is set to 1, the HBA shall generate an interrupt.
3	0h RW	**Set Device Bits FIS Interrupt Enable (SDBE):** When set, GHC.IE is set, and P0IS.SDBS is set, the HBA shall generate an interrupt.
2	0h RW	**DMA Setup FIS Interrupt Enable (DSE):** When set, GHC.IE is set, and P0IS.DSS is set, the HBA shall generate an interrupt.
1	0h RW	**PIO Setup FIS Interrupt Enable (PSE):** When set, GHC.IE is set, and P0IS.PSS is set, the HBA shall generate an interrupt.
0	0h RW	**Device to Host Register FIS Interrupt Enable (DHRE):** When set, GHC.IE is set, and P0IS.DHRS is set, the HBA shall generate an interrupt.

22.2.20 Port 0 Command (P0CMD)—Offset 118h

Port 0 Command

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RW	**Interface Communication Control (ICC):** This is a four bit field which can be used to control reset and power states of the interface. Writes to this field will cause actions on the interface, either as primitives or an OOB sequence, and the resulting status of the interface will be reported in the PxSSTS register. Value Definition Fh–9h Reserved 8h DEVSLP: This will cause the PCH to assert the DEVSLP signal associated with the port. The PCH will ignore the DEVSLP idle timeout value that is specified by PxDEVSLP.DITO. Software will only request DEVSLP when the interface is in an idle state (that is, PxCI is cleared to 0h and PxSACT is cleared to 0h). If the interface is not idle at the time this register is written, then the PCH will take no action and the interface will remain in its current state. If PxCAP2.DESO is set to '1' and PxSSTS.IPM is not set to '6h', then the host will take no action on the interface and will remain in its current state. Additionally, the HBA shall not assert the DEVSLP signal until PHYRDY has been achieved (after a previous de-assertion). 7h Reserved 6h Slumber: This will cause the PCH to request a transition of the interface to the slumber state. The SATA device may reject the request and the interface will remain in its current state. 5h–3h Reserved 2h Partial: This will cause the PCH to request a transition of the interface to the partial state. The SATA device may reject the request and the interface will remain in its current state. 1h Active: This will cause the PCH to request a transition of the interface into the active state. If the requested transition is from the DEVSLP state, then the host controller shall wait until PxDEVSLP.DMAT has expired before deasserting the DEVSLP Signal. 0h No-Op/Idle: When software reads this value, it indicates the PCH is not in the process of changing the interface state or sending a device reset, and a new link command may be issued. When system software writes a non-reserved value other than No-Op (0h), the HBA shall perform the action and update this field back to Idle (0h). If software writes to this field to change the state to a state the link is already in (i.e. interface is in the active state and a request is made to go to the active state), the HBA shall take no action and return this field to Idle. If the interface is in a low power state and the software wants to transition to a different low power state, software must first bring the link to active and then initiate the transition to the desired low power state (with the exception of DEVSLP). The transition to DEVSLP may occur from any other state if CAP2.DESO is cleared to '0'. If CAP2.DESO is set to '1', then DEVSLP may only be transitioned to if the link is in Slumber.
27	0h RW	**Aggressive Slumber Partial (ASP):** When set to 1, and the ALPE bit is set, the HBA shall aggressively enter the Slumber state when it clears a bit in the PxCI or PxSACT register and the register values are then PxCI = 0h and PxSACT = 0h. When cleared, and the ALPE bit is set, the HBA will aggressively enter the Partial state when it clears a bit in the PxCI or PxSACT register and the register values are then PxCI = 0h and PxSACT = 0h. If CAP.SALP is cleard to 0., software shall treat this bit as reserved.
26	0h RW	**Aggressive Link Power Management Enable (ALPE):** When set, the HBA will aggressively enter a lower link power state (Partial or Slumber) based upon the setting of the ASP bit. Software shall only set this bit to 1 if CAP.SALP is set to 1. If CAP.SALP is cleared to 0, software shall treat this bit as reserved. BIOS is recommeded to program this field to 1.
25	0h RW	**Drive LED on ATAPI Enable (DLAE):** When set, the HBA will drive the LED pin active for commands regardless of the state of PxCMD.ATAPI. When cleared, the HBA will only drive the LED pin active for commands if PxCMD.ATAPI is set to 0.. This bit is set by software
24	0h RW	**Device is ATAPI (ATAPI):** When set, the connected device is an ATAPI device. This bit is used by the HBA to control whether or not to generate the desktop LED when commands are active.
23	0h RW	**Automatic Partial to Slumber Transitions Enabled (APSTE):** 0 = This port will not perform Automatic Partial to Slumber Transitions. 1 = The HBA may perform Automatic Partial to Slumber Transitions. Note: Software shall only set this bit to '1' if CAP2.APST is set to '1'; if CAP2.APST is cleared to '0' software shall treat this bit as reserved.
22	0h RO	**FIS-based Switching Capable Port (FBSCP):** The SATA controller does not support FIS-Based Switching.
21	0h RW/O	**External SATA Port (ESP):** 0 = This port supports internal SATA devices only. 1 = This port will be used with an external SATA device and hot-plug is supported. When set, CAP.SXS must also be set. This bit is not reset by Function Level Reset.

Bit Range	Default and Access	Field Name (ID): Description
20	0h RO	**Cold Presence Detection (CPD):** The SATA controller does not support cold presence detect.
19	0h RW/O	**Mechanical Presence Switch Attached to Port (MPSP):** If set to 1, the platform supports a mechanical presence switch attached to this port. If cleared to 0, the platform does not support a mechanical presence switch attached to this port.
18	0h RW/O	**Hot Plug Capable Port (HPCP):** This indicates whether the this port is connected to a device which can be hot plugged. SATA by definition is hot-pluggable, but not all platforms are constructed to allow the device to be removed (it may be screwed into the chassis, for example). This bit can be used by system software to indicate a feature such as eject device to the end-user. 0 = Port is not capable of hot-plug. 1 = Port is hot-plug capable. The HBA takes no action on the state of this bit – it is for system software only. For example, if this bit is cleared, and a hot plug event occurs, the HBA shall still treat it as a proper hot plug event. Note: This bit is not reset on a HBA reset. This field is not reset by FLR.
17	0h RO	**Port Multiplier Attached (PMA):** When set, a Port Multiplier is attached to the HBA for this port. When cleared, a Port Multiplier is not attached to the HBA for this port. This bit is a read only 0. when CAP.PMS = 0., and read/write when CAP.PMS = 1.. Note that this bit is set by software; hardware does not auto-detect that a Port Multiplier is attached.
16	0h RO	Reserved.
15	0h RO	**Command List Running (CR):** When this bit is set it indicates that the command list DMA engine for the port is running.
14	0h RO	**FIS Receive Running (FR):** When this bit is set it indicates that the FIS Receive DMA engine for the port is running. Note to software: When FR bit stays set, please read the PxIS.PCS and PxSERR.DET.X to service the PCS interrupt accordingly if any
13	0h RO	**Mechanical Presence Switch State (MPSS):** The MPSS bit reports the state of a mechanical presence switch attached to this port. If CAP.SMPS is set to 1 and the mechanical presence switch is closed then this bit is cleared to 0. If CAP.SMPS is set to 1 and the mechanical presence switch is open then this bit is set to 1. If CAP.SMPS is set to 0 then this bit is cleared to 0. Software should only use this bit if both CAP.SMPS and PxCMD.MPSP are set to 1.
12:8	0h RO	**Current Command Slot (CCS):** Indicates the current command slot the HBA is processing. This field is valid when the PxCMD.ST bit is set, and is constantly updated by the HBA. This field can be updated as soon as the HBA recognizes an active command slot, or at some point soon after when it begins processing the command. When PxCMD.ST transitions from a 1 to a 0, the HBA will reset this field to 0. After PxCMD.ST transitions from 0 to 1, the highest priority slot to issue from next is command slot 0. After the first command has been issued, the highest priority slot to issue from next is PxCMD.CCS + 1. For example, after the HBA has issued its first command, if PxCMD.CCS = 0h and PxCI is set to 3h, the next command that will be issued is from command slot 1.
7	0h RO	Reserved.
6	0h RO	**PHYSLP Present (PSP):** If set to '1', the platform supports PHYSLP on this port. If cleared to '0', the platform does not support PHYSLP on this port. This bit may only be set to '1' if CAP2.SPS is set to '1'.
5	0h RO	Reserved.
4	0h RW	**FIS Receive Enable (FRE):** When set, the HBA may post received FISes into the FIS receive area pointed to by PxFB and PxFBU. When cleared, received FISes are not accepted by the HBA, except for the first D2H register FIS after the initialization sequence.
3	0h RW/1S	**Command List Override (CLO):** Setting this bit to 1 causes PxTFD.STS.BSY and PxTFD.STS.DRQ to be cleared to 0. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the PxTFD.STS register. The HBA sets this bit to 0 when PxTFD.STS.BSY and PxTFD.STS.DRQ have been cleared to 0. A write to this register with a value of 0 shall have no effect.

Bit Range	Default and Access	Field Name (ID): Description
2	1h RO	**Power On Device (POD):** The SATA controller does not support cold presence detect.
1	0h RW	**Spin-Up Device (SUD):** This bit is read/write and default to 0 for HBAs that support staggered spin-up via CAP.SSS. This bit is read only 1 for HBAs that do not support staggered spin-up. 0 = No Action 1 = On an edge detect from 0 to 1, the PCH shall start a COMRESET initialization sequence to the device. Clearing this bit causes no action on the interface. Clearing this bit to 0 does not cause any OOB signal to be sent on the interface. When this bit is cleared to 0 and PxSCTL.DET = 0h, the HBA will enter listen mode.
0	0h RW	**Start (ST):** When set, the HBA may process the command list. When cleared, the HBA may not process the command list. Whenever this bit is changed from a 0 to a 1, the HBA starts processing the command list at entry 0. Whenever this bit is changed from a 1 ot a 0, the PxCI and PxSACT register is cleared by the HBA upon the HBA putting the controller into an idle state. PxTFD shall be updated also.

22.2.21 Port 0 Task File Data (P0TFD)—Offset 120h

Port 0 Task File Data

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 9h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	0h RO	**Error (ERR):** Contains the latest copy of the task file error register.
7	0h RO	**Status Busy (STS_BSY):** Status - Indicates the interface is busy.
6:4	0h RO	Reserved.
3	1h RO	**Status Drq (STS_DRQ):** Status - Indicates a data transfer is requested.
2:1	0h RO	Reserved.
0	1h RO	**Status Err (STS_ERR):** Status - Indicates an error during the transfer.

22.2.22 Port 0 Signature (P0SIG)—Offset 124h

Port 0 Signature

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: FFFFFFFFh

Bit Range	Default and Access	Field Name (ID): Description
31:0	FFFFFFFFh RO	**Signature (SIG):** Contains the signature received from a device on the first D2H Register FIS. The bit order is as follows: Bit Field 31:24 LBA High Register 23:16 LBA Mid Register 15:8 LBA Low Register 7:0 Sector Count Register

22.2.23 Port 0 Serial ATA Status (P0SSTS)—Offset 128h

Port 0 Serial ATA Status

Access Method

Type: MEM Register (Size: 32 bits)

Device: 23

Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11:8	0h RO	**Interface Power Management (IPM):** Indicates the current interface state. Value Description 0h Device not present or communication not established 1h Interface in active state 2h Interface in PARTIAL power management state 6h Interface in SLUMBER power management state 8h DEVSLP asserted All other values reserved. This field reflects the interface power management state for both device and host initiated power management. Note: If an Automatic Partial to Slumber Transition occurs, PxSSTS.IPM shall reflect that the host has entered Slumber (PxSSTS.IPM = '6h').
7:4	0h RO	**Current Interface Speed (SPD):** Indicates the negotiated interface communication speed. Value Description 0h Device not present or communication not established 1h Generation 1 communication rate negotiated 2h Generation 2 communication rate negotiated 3h Generation 3 communication rate negotiated All other values reserved.
3:0	0h RO	**Device Detection (DET):** Indicates the interface device detection and Phy state. Value Description 0h No device detected and Phy communication not established 1h Device presence detected but Phy communication not established 3h Device presence detected and Phy communication established 4h Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode All other values reserved. Note: While the true reset default value of this register is 0h, the value read from this register depends on drive presence and the point in time within the initialization process when the register is read. Note: The means by which the implementation determines device presence may be vendor specific. However, device presence shall always be indicated anytime a COMINIT signal is received.

22.2.24 Port 0 Serial ATA Control (P0SCTL)—Offset 12Ch

Port 0 Serial ATA Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19:16	0h RW	**Port Multiplier Port (PMP):** This field is not used by AHCI.
15:12	0h RW	**Select Power Management (SPM):** This field is not used by AHCI.
11:8	0h RW	**Interface Power Management Transitions Allowed (IPM):** Indicates which power states the HBA is allowed to transition to. If an interface power management state is not allowed via this register field, the HBA will not initiate that state and the HBA will PMNAKp any request from the device to enter that state. Value Description 0h No interface restrictions 1h Transitions to the PARTIAL state disabled 2h Transitions to the SLUMBER state disabled 3h Transitions to both PARTIAL and SLUMBER states disabled 4h Transitions to the DEVSLP power management state are disabled 5h Transitions to the Partial and DEVSLP power management states are disabled 6h Transitions to the Slumber and DEVSLP power management states are disabled 7h Transitions to the Partial, Slumber and DEVSLP power management states are disabled All other values reserved.
7:4	0h RW	**Speed Allowed (SPD):** Indicates the highest allowable speed of the interface. Value Description 0h No speed negotiation restrictions 1h Limit speed negotiation to Generation 1 communication rate 2h Limit speed negotiation to a rate not greater than Generation 2 communication rate 3h Limit speed negotiation to a rate not greater than Generation 3 communication rate All other values reserved Note: If software changes SPD after port has been enabled, software is required to perform a port reset via DET=1h.
3:0	0h RW	**Device Detection Initialization (DET):** Controls the HBA.s device detection and interface initialization. Value Description 0h No device detection or initialization action requested. 1h Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications reinitialized. While this field is 1h, COMRESET is continuously transmitted on the interface. Software should leave the DET field set to 1h for a minimum of 1 millisecond to ensure that a COMRESET is sent on the interface. 4h Disable the Serial ATA interface and put Phy in offline mode. All other values reserved. This field may only be changed when PxCMD.ST is '0'. Changing this field while the HBA is running results in undefined behavior. When PxCMD.ST is set to '1', this field should have a value of 0h. Note: It is permissible to implement any of the Serial ATA defined behaviors for transmission of COMRESET when PxSCTL.DET = 1h.

22.2.25 Port 0 Serial ATA Error (P0SERR)—Offset 130h

Port 0 Serial ATA Error

Access Method

Type: MEM Register (Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RW/1C	**Diagnostics (DIAG):** Contains diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes. Bit Field 31:27 Reserved 26 Exchanged (X): When set to one this bit indicates that a change in device presence has been detected since the last time this bit was cleared. The means by which the implementation determines that the device presence has changed is vendor specific. This bit shall always be set to one anytime a COMINIT signal is received. This bit is reflected in the P0IS.PCS bit. 25 Unrecognized FIS Type (F): Indicates that one or more FISs were received by the Transport layer with good CRC, but had a type field that was not recognized/known. 24 Transport state transition error (T): Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared. 23 Link Sequence Error (S): Indicates that one or more Link state machine error conditions were encountered. The Link Layer state machine defines the conditions under which the link layer detects an erroneous transition. 22 Handshake Error (H): Indicates that one or more R_ERR handshake response was received in response to frame transmission. Such errors may be the result of a CRC error detected by the recipient, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame. 21 CRC Error (C): Indicates that one or more CRC errors occurred with the Link Layer. 20 Disparity Error (D): This field is not used by AHCI. 19 10B to 8B Decode Error (B): Indicates that one or more 10B to 8B decoding errors occurred. 18 Comm Wake (W): Indicates that a Comm Wake signal was detected by the Phy. 17 Phy Internal Error (I): Indicates that the Phy detected some internal error. 16 PhyRdy Change (N): When set to 1 this bit indicates that the internal PhyRdy signal changed state since the last time this bit was cleared. The state of this bit is reflected in the PxIS.PRCS interrupt status bit and an interrupt will be generated if enabled.
15:0	0h RW/1C	**Error (ERR):** The ERR field contains error information for use by host software in determining the appropriate response to the error condition. If one or more of bits 11:8 of this register are set, the controller will stop the current transfer. Bit Field 15:12 Reserved 11 Internal Error (E): The SATA controller failed due to a Initiator or target abort when attempting to access system memory. 10 Protocol Error (P): A violation of the Serial ATA protocol was detected. 9 Persistent Communication or Data Integrity Error (C): A communication error that was not recovered occurred that is expected to be persistent. Persistent communications errors may arise from faulty interconnect with the device, from a device that has been removed or has failed, or a number of other causes. 8 Transient Data Integrity Error (T): A data integrity error occurred that was not recovered by the interface. 7:2 Reserved 1 Recovered Communications Error (M): Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of Phy synchronization, or from other causes and may be derived from the PhyNRdy signal between the Phy and Link layers. 0 Recovered Data Integrity Error (I): A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action.

22.2.26 Port 0 Serial ATA Active (P0SACT)—Offset 134h

Port 0 Serial ATA Active

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/1S	**Device Status (DS):** System software sets this bit for native command queuing commands prior to setting the PxCI.CI bit in the same command slot entry. This field is cleared via the Set Device Bits FIS. This field is also cleared when PxCMD.ST is cleared by software. Note that this field is not cleared by COMRESET or SRST.

22.2.27 Port 0 Command Issue (P0CI)—Offset 138h

Port 0 Commands Issued

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Commands Issued (CI):** This field is set by software to indicate to the HBA that a command has been built in system memory for a command slot and may be sent to the device. When the HBA receives a FIS which clears the BSY, ERR, and DRQ bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field shall only be set to '1' by software when PxCMD.ST is set to '1'. This field is also cleared when PxCMD.ST is written from a '1' to a '0' by software.

22.2.28 Port 0 Device Sleep (P0DEVSLP)—Offset 144h

Port 0 Device Sleep

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 1E022852h

Bit Range	Default and Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:25	Fh RW/O	**DITO Multiplier (DM):** DITO multiplier that the HBA applies to the specified DITO value, effectively extending the range of DITO from 1ms to 16368ms. A value of 0h indicates a multiplier of 1. A maximum multiplier of 16 may be applied. The HBA computes the total idle timeout as a product of DM and DITO (i.e. DITO actual = DITO * (DM+1)). Note: These bits are not reset by controller reset.
24:15	4h RW	**DEVSLP Idle Timeout (DITO):** This field specifies the amount of the time (in approximate 1ms granularity) that the HBA shall wait before driving the DEVSLP signal. Hardware reloads its port specific DEVSLP timer with this value each time the port transitions out of DEVSLP state. For example: from DEVSLP to active or PxDEVSLP.ADSE transitions from 0 to a 1. If CAP2.SDS or CAP2.SADM or PxDEVSLP.DSP is cleared to 0 then these bits are read-only 0h and software shall treat these bits as reserved. Software shall only set this value when PxCMD.ST is cleared to 0 and PxDEVSLP.ADSE is cleared to 0. Note: These bits are not reset by controller reset.
14:10	Ah RW	**DEVSLP Minimum Assertion Time (MDAT):** This field specifies the minimum amount of time (in 1ms granulatity) that the HBA must assert the DEVSLP signal before it may be de-asserted. The norminal value is 10ms and the minimum is 1ms depending on device identification information. If CAP2.SDS is cleared to 0 or PxDEVSLP.DSP is cleared to 0 then these bits are read-only 0h and software shall treat these bits as reserved. Software shall only set this value when PxCMD.ST is cleared to 0, PxDEVSLP.ADSE is cleared to 0, and prior to setting PxCMD.ICC to 8h. Note: These bits are not reset by controller reset.
9:2	14h RW	**DEVSLP Exit Timeout (DETO):** This field specifies the maximum duration (in approximate 1ms granularity) from DEVSLP de-assertion until the device is ready to accept OOB. The norminal value is 20ms while the max value is 255ms depending on device identification information. If CAP2.SDS is cleared to 0 or PxDEVSLP.DSP is cleared to 0 then these bits are read-only 0h and software shall treat these bits as reserved. Software shall only set this value when PxCMD.ST is cleared to 0, PxDEVSLP.ADSE is cleared to 0, and prior to setting PxCMD.ICC to 8h. Note: These bits are not reset by controller reset.
1	1h RW/O	**DEVSLP Present (DSP):** If set to '1', the platform supports DEVSLP on this port. If cleared to '0', the platform does not support DEVSLP on this port. This bit may only be set to '1' if CAP2.SDS is set to '1'. DSP is mutually exclusive with the PxCMD.HPCP bit and PxCMD.ESP bit. BIOS is required to program this field to ‘1’ if the system supports the DEVSLP feature. Note: These bits are not reset by controller reset.
0	0h RW	**Aggressive DEVSLP Enable (ADSE):** This bit is read/write for HBAs that support aggressive DEVSLP management (CAP2. SADM = '1'). When this bit is set to '1', the HBA shall assert the DEVSLP signal after the port has been idle (PxCI = 0h and PxSACT = 0h) for the amount of time specified by the PxDEVSLP.DITO register and the interface is in Slumber (PxSSTS.IPM = 6h). When this bit is cleared to '0', the HBA does not enter DEVSLP unless software directed via PxCMD.ICC. This bit shall only be set to '1' if PxDEVSLP.DSP is set to '1'. If this bit is set to '1' and software clears the bit to '0', then the HBA shall de-assert the DEVSLP signal if asserted. Note that these bits are not reset on a HBA reset. BIOS is recommended to program this field to '1' if the platform support the DEVSLP feature. If CAP2.SDS is cleared to '0' or CAP2.SADM is cleared to '0', or if PxDEVSLP.DSP is cleared to '0' then these bits are read-only 0h and software shall treat these bits as reserved.

22.2.29 Port 1 Command List Base Address (P1CLB)—Offset 180h

Same bit definition as P0CLB.

22.2.30 Port 1 Command List Base Address Upper 32-bits (P1CLBU)—Offset 184h

Same bit definition as P0CLBU.

22.2.31 Port 1 FIS Base Address (P1FB)—Offset 188h

Same bit definition as P0FB.

22.2.32 Port 1 FIS Base Address Upper 32-bits (P1FBU)—Offset 18Ch

Same bit definition as P0FBU.

22.2.33 Port 1 Interrupt Status (P1IS)—Offset 190h

Same bit definition as P0IS.

22.2.34 Port 1 Interrupt Enable (P1IE)—Offset 194h

Same bit definition as P0IE.

22.2.35 Port 1 Command (P1CMD)—Offset 198h

Same bit definition as P0CMD.

22.2.36 Port 1 Task File Data (P1TFD)—Offset 1A0h

Same bit definition as P0TFD.

22.2.37 Port 1 Signature (P1SIG)—Offset 1A4h

Same bit definition as P0SIG.

22.2.38 Port 1 Serial ATA Status (P1SSTS)—Offset 1A8h

Same bit definition as P0SSTS.

22.2.39 Port 1 Serial ATA Control (P1SCTL)—Offset 1ACh

Same bit definition as P0SCTL.

22.2.40 Port 1 Serial ATA Error (P1SERR)—Offset 1B0h

Same bit definition as P0SERR.

22.2.41 Port 1 Serial ATA Active (P1SACT)—Offset 1B4h

Same bit definition as P0SACT.

22.2.42 Port 1 Command Issue (P1CI)—Offset 1B8h

Same bit definition as P0CI.

22.2.43 Port 1 Device Sleep (P1DEVSLP)—Offset 1C4h

Same bit definition as P0DEVSLP.

22.3 SATA AIDP Registers

SATA AHCI IO INDEX + DATA Registers

Table 22-3. Summary of SATA AIDP Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
10h	13h	AHCI Index Register (INDEX)—Offset 10h	0h
14h	17h	AHCI Data Register (DATA)—Offset 14h	0h

22.3.1 AHCI Index Register (INDEX)—Offset 10h

This registers are only available if CC.SCC is not 01h to index into all memory registers defined in Memory Registers and the message buffer used for enclosure management. If CC.SCC is 01h, these AHCI Index Data Pair registers are not accessible and SINDEX/SDATA register pair shall be used to index into a subset of the memory registers.(See Memory Registers for more information on which registers could be indexed).

Access Method

Type: IO Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18:2	0h RW	**Index (INDEX):** This Index register is used to select the Dword offset of the Memory Mapped AHCI register to be accessed. A Dword, Word or Byte access is specified by the active byte enables of the I/O access to the Data register.
1:0	0h RO	Reserved.

22.3.2 AHCI Data Register (DATA)—Offset 14h

This registers are index into all memory registers defined in Memory Registers and the message buffer used for enclosure management.

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Data (DATA):** This Data register is a window through which data is read or written to the memory mapped register pointed to by the Index register. Note that a physical register is not actually implemented as the data is actually stored in the memory mapped registers. Since this is not a physical register, the default value is the same as the default value of the register pointed to by Index.

22.4 SATA MXPBA Registers

SATA MSI-X Pending Bit Array Registers

Table 22-4. Summary of SATA MXPBA Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	MSI-X Pending Bit Array QW 0 (MXPQW0_DW0)—Offset 0h	0h

22.4.1 MSI-X Pending Bit Array QW 0 (MXPQW0_DW0)—Offset 0h

MSI-X Pending Bit Array QW 0

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RO/V	**MSI-X vector Pending (MXVP):** For each Pending Bit that is set, the function has a pending message for the associated MSI-X Table entry. Pending bits that have no associated MSI-X Table entry are reserved. After reset, the state of reserved Pending bits must be 0. Software should never write, and should only read Pending Bits. If software writes to Pending Bits, the result is undefined. Each Pending Bit's state after reset is 0 (no message pending).

22.5 SATA MXTBA Registers

SATA MSI-X Table Entry Registers

Table 22-5. Summary of SATA MXTBA Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	MSI-X Table Entries 0 Message Lower Address (MXTE0MLA)—Offset 0h	0h
4h	7h	MSI-X Table Entries 0 Message Upper Address (MXTE0MUA)—Offset 4h	0h
8h	Bh	MSI-X Table Entries 0 Message Data (MXTE0MD)—Offset 8h	0h
Ch	Fh	MSI-X Table Entries 0 Vector Control (MXTE0VC)—Offset Ch	1h
10h	13h	MSI-X Table Entries 1 Message Lower Address (MXTE1MLA)—Offset 10h	0h
14h	17h	MSI-X Table Entries 1 Message Upper Address (MXTE1MUA)—Offset 14h	0h
18h	1Bh	MSI-X Table Entries 1 Message Data (MXTE1MD)—Offset 18h	0h
1Ch	1Fh	MSI-X Table Entries 1 Vector Control (MXTE1VC)—Offset 1Ch	1h
20h	23h	MSI-X Table Entries 2 Message Lower Address (MXTE2MLA)—Offset 20h	0h
24h	27h	MSI-X Table Entries 2 Message Upper Address (MXTE2MUA)—Offset 24h	0h
28h	2Bh	MSI-X Table Entries 2 Message Data (MXTE2MD)—Offset 28h	0h
2Ch	2Fh	MSI-X Table Entries 2 Vector Control (MXTE2VC)—Offset 2Ch	1h
30h	33h	MSI-X Table Entries 3 Message Lower Address (MXTE3MLA)—Offset 30h	0h
34h	37h	MSI-X Table Entries 3 Message Upper Address (MXTE3MUA)—Offset 34h	0h
38h	3Bh	MSI-X Table Entries 3 Message Data (MXTE3MD)—Offset 38h	0h
3Ch	3Fh	MSI-X Table Entries 3 Vector Control (MXTE3VC)—Offset 3Ch	1h
40h	43h	MSI-X Table Entries 4 Message Lower Address (MXTE4MLA)—Offset 40h	0h
44h	47h	MSI-X Table Entries 4 Message Upper Address (MXTE4MUA)—Offset 44h	0h
48h	4Bh	MSI-X Table Entries 4 Message Data (MXTE4MD)—Offset 48h	0h
4Ch	4Fh	MSI-X Table Entries 4 Vector Control (MXTE4VC)—Offset 4Ch	1h
50h	53h	MSI-X Table Entries 5 Message Lower Address (MXTE5MLA)—Offset 50h	0h
54h	57h	MSI-X Table Entries 5 Message Upper Address (MXTE5MUA)—Offset 54h	0h
58h	5Bh	MSI-X Table Entries 5 Message Data (MXTE5MD)—Offset 58h	0h
5Ch	5Fh	MSI-X Table Entries 5 Vector Control (MXTE5VC)—Offset 5Ch	1h
60h	63h	MSI-X Table Entries 6 Message Lower Address (MXTE6MLA)—Offset 60h	0h
64h	67h	MSI-X Table Entries 6 Message Upper Address (MXTE6MUA)—Offset 64h	0h
68h	6Bh	MSI-X Table Entries 6 Message Data (MXTE6MD)—Offset 68h	0h
6Ch	6Fh	MSI-X Table Entries 6 Vector Control (MXTE6VC)—Offset 6Ch	1h
70h	73h	MSI-X Table Entries 7 Message Lower Address (MXTE7MLA)—Offset 70h	0h
74h	77h	MSI-X Table Entries 7 Message Upper Address (MXTE7MUA)—Offset 74h	0h
78h	7Bh	MSI-X Table Entries 7 Message Data (MXTE7MD)—Offset 78h	0h
7Ch	7Fh	MSI-X Table Entries 7 Vector Control (MXTE7VC)—Offset 7Ch	1h

22.5.1 MSI-X Table Entries 0 Message Lower Address (MXTE0MLA)—Offset 0h

MSI-X Table Entries 0 Message Lower Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**MSI-X message lower address (MXMLA):** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	0h RO	Reserved.

22.5.2 MSI-X Table Entries 0 Message Upper Address (MXTE0MUA)—Offset 4h

MSI-X Table Entries 0 Message Upper Address

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message upper 32-bit address (MXMUA):** Specifies the upper 32-bit of the MSI-X Message.

22.5.3 MSI-X Table Entries 0 Message Data (MXTE0MD)—Offset 8h

MSI-X Table Entries 0 Message Data

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message Data (MXMD):** Specifies the 32-bit Data of the MSI-X Message.

22.5.4 MSI-X Table Entries 0 Vector Control (MXTE0VC)—Offset Ch

MSI-X Table Entries 0 Vector Control

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	1h RW	**MSI-X vector Mask (MXVM):** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

22.5.5 MSI-X Table Entries 1 Message Lower Address (MXTE1MLA)—Offset 10h

MSI-X Table Entries 1 Message Lower Address

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**MSI-X message lower address (MXMLA):** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	0h RO	Reserved.

22.5.6 MSI-X Table Entries 1 Message Upper Address (MXTE1MUA)—Offset 14h

MSI-X Table Entries 1 Message Upper Address

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message upper 32-bit address (MXMUA):** Specifies the upper 32-bit of the MSI-X Message

22.5.7 MSI-X Table Entries 1 Message Data (MXTE1MD)—Offset 18h

MSI-X Table Entries 1 Message Data

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message Data (MXMD):** Specifies the 32-bit Data of the MSI-X Message.

22.5.8 MSI-X Table Entries 1 Vector Control (MXTE1VC)—Offset 1Ch

MSI-X Table Entries 1 Vector Control

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	1h RW	**MSI-X vector Mask (MXVM):** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

22.5.9 MSI-X Table Entries 2 Message Lower Address (MXTE2MLA)—Offset 20h

MSI-X Table Entries 2 Message Lower Address

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**MSI-X message lower address (MXMLA):** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	0h RO	Reserved.

22.5.10 MSI-X Table Entries 2 Message Upper Address (MXTE2MUA)—Offset 24h

MSI-X Table Entries 2 Message Upper Address

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message upper 32-bit address (MXMUA):** Specifies the upper 32-bit of the MSI-X Message

22.5.11 MSI-X Table Entries 2 Message Data (MXTE2MD)—Offset 28h

MSI-X Table Entries 2 Message Data

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message Data (MXMD):** Specifies the 32-bit Data of the MSI-X Message.

22.5.12 MSI-X Table Entries 2 Vector Control (MXTE2VC)—Offset 2Ch

MSI-X Table Entries 2 Vector Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	1h RW	**MSI-X vector Mask (MXVM):** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

22.5.13 MSI-X Table Entries 3 Message Lower Address (MXTE3MLA)—Offset 30h

MSI-X Table Entries 3 Message Lower Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**MSI-X message lower address (MXMLA):** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	0h RO	Reserved.

22.5.14 MSI-X Table Entries 3 Message Upper Address (MXTE3MUA)—Offset 34h

MSI-X Table Entries 3 Message Upper Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message upper 32-bit address (MXMUA):** Specifies the upper 32-bit of the MSI-X Message

22.5.15 MSI-X Table Entries 3 Message Data (MXTE3MD)—Offset 38h

MSI-X Table Entries 3 Message Data

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message Data (MXMD):** Specifies the 32-bit Data of the MSI-X Message.

22.5.16 MSI-X Table Entries 3 Vector Control (MXTE3VC)—Offset 3Ch

MSI-X Table Entries 3 Vector Control

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	1h RW	**MSI-X vector Mask (MXVM):** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

22.5.17 MSI-X Table Entries 4 Message Lower Address (MXTE4MLA)—Offset 40h

MSI-X Table Entries 4 Message Lower Address

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**MSI-X message lower address (MXMLA):** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	0h RO	Reserved.

22.5.18 MSI-X Table Entries 4 Message Upper Address (MXTE4MUA)—Offset 44h

MSI-X Table Entries 4 Message Upper Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message upper 32-bit address (MXMUA):** Specifies the upper 32-bit of the MSI-X Message

22.5.19 MSI-X Table Entries 4 Message Data (MXTE4MD)—Offset 48h

MSI-X Table Entries 4 Message Data

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message Data (MXMD):** Specifies the 32-bit Data of the MSI-X Message.

22.5.20 MSI-X Table Entries 4 Vector Control (MXTE4VC)—Offset 4Ch

MSI-X Table Entries 4 Vector Control

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	1h RW	**MSI-X vector Mask (MXVM):** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

22.5.21 MSI-X Table Entries 5 Message Lower Address (MXTE5MLA)—Offset 50h

MSI-X Table Entries 5 Message Lower Address

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**MSI-X message lower address (MXMLA):** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	0h RO	Reserved.

22.5.22 MSI-X Table Entries 5 Message Upper Address (MXTE5MUA)—Offset 54h

MSI-X Table Entries 5 Message Upper Address

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message upper 32-bit address (MXMUA):** Specifies the upper 32-bit of the MSI-X Message

22.5.23 MSI-X Table Entries 5 Message Data (MXTE5MD)—Offset 58h

MSI-X Table Entries 5 Message Data

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message Data (MXMD):** Specifies the 32-bit Data of the MSI-X Message.

22.5.24 MSI-X Table Entries 5 Vector Control (MXTE5VC)—Offset 5Ch

MSI-X Table Entries 5 Vector Control

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	1h RW	**MSI-X vector Mask (MXVM):** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

22.5.25 MSI-X Table Entries 6 Message Lower Address (MXTE6MLA)—Offset 60h

MSI-X Table Entries 6 Message Lower Address

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**MSI-X message lower address (MXMLA):** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	0h RO	Reserved.

22.5.26 MSI-X Table Entries 6 Message Upper Address (MXTE6MUA)—Offset 64h

MSI-X Table Entries 6 Message Upper Address

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message upper 32-bit address (MXMUA):** Specifies the upper 32-bit of the MSI-X Message

22.5.27 MSI-X Table Entries 6 Message Data (MXTE6MD)—Offset 68h

MSI-X Table Entries 6 Message Data

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message Data (MXMD):** Specifies the 32-bit Data of the MSI-X Message.

22.5.28 MSI-X Table Entries 6 Vector Control (MXTE6VC)—Offset 6Ch

MSI-X Table Entries 6 Vector Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	1h RW	**MSI-X vector Mask (MXVM):** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

22.5.29 MSI-X Table Entries 7 Message Lower Address (MXTE7MLA)—Offset 70h

MSI-X Table Entries 7 Message Lower Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**MSI-X message lower address (MXMLA):** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	0h RO	Reserved.

22.5.30 MSI-X Table Entries 7 Message Upper Address (MXTE7MUA)—Offset 74h

MSI-X Table Entries 7 Message Upper Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message upper 32-bit address (MXMUA):** Specifies the upper 32-bit of the MSI-X Message

22.5.31 MSI-X Table Entries 7 Message Data (MXTE7MD)—Offset 78h

MSI-X Table Entries 7 Message Data

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message Data (MXMD):** Specifies the 32-bit Data of the MSI-X Message.

22.5.32 MSI-X Table Entries 7 Vector Control (MXTE7VC)—Offset 7Ch

MSI-X Table Entries 7 Vector Control

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	1h RW	**MSI-X vector Mask (MXVM):** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

§ §

23 Intel® CSE: HECI Interface (D22:F0/F1/F4/F5)

23.1 Intel® CSE:HECI PCI Configuration Registers

Table 23-1. Summary of Intel® CSE:HECI PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	HECI ID (HECI1_ID)—Offset 0h	XXXX8086h
4h	5h	HECI Command (HECI1_CMD)—Offset 4h	0h
6h	7h	HECI Status (HECI1_STS)—Offset 6h	10h
8h	Bh	Revision ID And Class Code (HECI1_RID_CC)—Offset 8h	78000XXh
Ch	Ch	Cache Line Size (HECI1_CLS)—Offset Ch	0h
Dh	Dh	Initiator Latency Timer (HECI1_MLT)—Offset Dh	0h
Eh	Eh	Header Type (HECI1_HTYPE)—Offset Eh	80h
Fh	Fh	Built In Self-Test (HECI1_BIST)—Offset Fh	0h
10h	13h	HECI MMIO Base Address Low (HECI1_MMIO_MBAR_LO)—Offset 10h	4h
14h	17h	HECI MMIO Base Address High (HECI1_MMIO_MBAR_HI)—Offset 14h	0h
2Ch	2Fh	Sub System Identifiers (HECI1_SS)—Offset 2Ch	0h
34h	37h	Capabilities Pointer (HECI1_CAP)—Offset 34h	50h
3Fh	3Fh	Maximum Latency (HECI1_MLAT)—Offset 3Fh	0h
40h	43h	Host Firmware Status (HECI1_HFS)—Offset 40h	0h
44h	47h	Miscellaneous Shadow (HECI1_MISC_SHDW)—Offset 44h	80000000h
48h	4Bh	General Status Shadow 1 (HECI1_GS_SHDW1)—Offset 48h	0h
4Ch	4Fh	Host General Status (HECI1_H_GS1)—Offset 4Ch	0h
50h	51h	PCI Power Management Capability ID (HECI1_PID)—Offset 50h	8C01h
52h	53h	PCI Power Management Capabilities (HECI1_PC)—Offset 52h	4003h
64h	67h	General Status Shadow 3 (HECI1_GS_SHDW3)—Offset 64h	0h
68h	6Bh	General Status Shadow 4 (HECI1_GS_SHDW4)—Offset 68h	0h
6Ch	6Fh	General Status Shadow 5 (HECI1_GS_SHDW5)—Offset 6Ch	0h
70h	73h	Host General Status 2 (HECI1_H_GS2)—Offset 70h	0h
74h	77h	Host General Status 3 (HECI1_H_GS3)—Offset 74h	0h
8Ch	8Dh	Message Signaled Interrupt Identifiers (HECI1_MID)—Offset 8Ch	A405h
8Eh	8Fh	Message Signaled Interrupt Message Control (HECI1_MC)—Offset 8Eh	80h
90h	93h	Message Signaled Interrupt Message Address (HECI1_MA)—Offset 90h	0h
94h	97h	Message Signaled Interrupt Upper Address (HECI1_MUA)—Offset 94h	0h
98h	99h	Message Signaled Interrupt Message Data (HECI1_MD)—Offset 98h	0h
A0h	A0h	HECI Interrupt Delivery Mode (HECI1_HIDM)—Offset A0h	0h
ACh	AFh	SW LTR Pointer Register (HECI1_SWLTRPTR)—Offset ACh	0h
B0h	B3h	Device Idle Pointer Register (HECI1_DEVIDLEPTR)—Offset B0h	8001h

Table 23-1. Summary of Intel® CSE:HECI PCI Configuration Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
B6h	B7h	DevIdle Power Control Enabled Register (HECI1_PWRCTRLEN)—Offset B6h	Eh
CCh	CFh	Host Extend Register DW4 (HECI1_HER4)—Offset CCh	0h
D4h	D7h	Host Extend Register DW6 (HECI1_HER6)—Offset D4h	0h
D8h	DBh	Host Extend Register DW7 (HECI1_HER7)—Offset D8h	0h
DCh	DFh	Host Extend Register DW8 (HECI1_HER8)—Offset DCh	0h

23.1.1 HECI ID (HECI1_ID)—Offset 0h

Identification

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: XXXX8086h

Bit Range	Default and Access	Field Name (ID): Description
31:16	-- RO/V	**Device ID (DID):** Indicates what device number assigned by Intel. Refer to the Device and Revision ID Table in Volume 1 for default value.
15:0	8086h RO	**Vendor ID (VID):** 16-bit field which indicates Intel is the vendor.

23.1.2 HECI Command (HECI1_CMD)—Offset 4h

Command

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (ID):** Disables this device from generating PCI line based interrupts. This bit does not have any effect on MSI operation.
9	0h RO	**Fast Back-to-Back Enable (FBE):** Not implemented, hardwired to 0.

Bit Range	Default and Access	Field Name (ID): Description
8	0h RO	**SERR# Enable (SEE):** Not implemented, hardwired to 0.
7	0h RO	**Wait Cycle Enable (WCC):** Not implemented, hardwired to 0.
6	0h RO	**Parity Error Response Enable (PEE):** Not implemented, hardwired to 0.
5	0h RO	**VGA Palette Snooping Enable (VAG):** Not implemented, hardwired to 0
4	0h RO	**Memory Write And Invalidate Enable (MWIE):** Not implemented, hardwired to 0.
3	0h RO	**Special Cycle Enable (SCE):** Not implemented, hardwired to 0.
2	0h RW	**Bus Initiator Enable (BME):** Controls the HECI host controller's abiity to act as a system memory Initiator for data transfers. When this bit is cleared, HECI bus Initiator activity stops and any active DMA engines return to an idle condition. This bit is made visible to firmware through the H_PCI_CSR register, and changes to this bit may be configured by the H_PCI_CSR register to generate an MSI to mIA. When this bit is '0', HECI is blocked from generating MSI to the host CPU. Note that this bit does not block HECI accesses to CSE-UMA.
1	0h RW	**Memory Space Enable (MSE):** Controls access to the HECI host controller's memory mapped register space.
0	0h RO	**I/O Space Enable (IOSE):** Not implemented, hardwired to 0.

23.1.3 HECI Status (HECI1_STS)—Offset 6h

Status

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 22
Function: 0

Default: 10h

Bit Range	Default and Access	Field Name (ID): Description
15	0h RO	**Detected Parity Error (DPE):** Not implemented, hardwired to 0.
14	0h RO	**Signaled System Error (SSE):** Not implemented, hardwired to 0.
13	0h RO	**Received Initiator-Abort (RMA):** Not implemented, hardwired to 0.
12	0h RO	**Received Target Abort (RTA):** Not implemented, hardwired to 0.
11	0h RO	**Signaled Target-Abort (STA):** Not implemented, hardwired to 0.
10:9	0h RO	**DEVSEL# Timing (DEVT):** These bits are hardwired to 00.

Bit Range	Default and Access	Field Name (ID): Description
8	0h RO	**Initiator Data Pariy Error Detected (DPD):** Not implemented, hardwired to 0.
7	0h RO	**Fast Back-to-Back Capable (FBC):** Not implemented, hardwired to 0.
6	0h RO	Reserved.
5	0h RO	**66 MHz Capable (C66):** Not implemented, hardwired to 0.
4	1h RO	**Capabilities List (CL):** Indicates the presence of a capabilities list, hardwired to 1.
3	0h RO/V	**Interrupt Status (IS):** Reflects the state of the INTx# signal at the input of the enable/disable circuit. This bit is a 1 when the INTx# is asserted. This bit is a 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the command register). Note that this bit is not set by an MSI.
2:0	0h RO	Reserved.

23.1.4 Revision ID And Class Code (HECI1_RID_CC)—Offset 8h

Revision ID And Class Code

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 78000XXh

Bit Range	Default and Access	Field Name (ID): Description
31:24	7h RO	**Base Class Code (BCC):** Indicates the base class code of the HECI host controller device.
23:16	80h RO	**Sub Class Code (SCC):** Indicates the sub class code of the HECI host controller device.
15:8	0h RO	**Programming Interface (PI):** Indicates the programming interface of the HECI host controller device.
7:0	-- RO/V	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

23.1.5 Cache Line Size (HECI1_CLS)—Offset Ch

Cache Line Size

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RO	**Cache Line Size (CLS):** Not implemented, hardwired to 0.

23.1.6 Initiator Latency Timer (HECI1_MLT)—Offset Dh

Initiator Latency Timer

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RO	**Initiator Latency Timer (MLT):** Not implemented, hardwired to 0.

23.1.7 Header Type (HECI1_HTYPE)—Offset Eh

Header Type

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 22
Function: 0

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RO	**Multi-Function Device (MFD):** Indicates the HECI host controller is part of a multi-function device.
6:0	0h RO	**Header Layout (HL):** Indicates that the HECI host controller uses a target device layout.

23.1.8 Built In Self-Test (HECI1_BIST)—Offset Fh

Built In Self-Test

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7	0h RO	**BIST Capable (BC):** Not implemented, hardwired to 0.
6:0	0h RO	Reserved.

23.1.9 HECI MMIO Base Address Low (HECI1_MMIO_MBAR_LO)—Offset 10h

HECI MMIO Base Address Low

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:12	0h RW	**Base Address Low (BA_LO):** Lower 32 bits of base address of register memory space.
11:4	0h RO	**Memory Size (MS):** This field is hardwired to 0 to indicate that HECI device requests 4KB of memory space.
3	0h RO	**Prefetchable (PF):** Indicates that this range is not pre-fetchable.
2:1	2h RO	**Type (TP):** Indicates that this range can be mapped anywhere in 64-bit address space.
0	0h RO	**Resource Type Indicator (RTE):** Indicates a request for register memory space.

23.1.10 HECI MMIO Base Address High (HECI1_MMIO_MBAR_HI)—Offset 14h

HECI MMIO Base Address High

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Base Address High (BA_HI):** Upper 32 bits of base address of register memory space.

23.1.11 Sub System Identifiers (HECI1_SS)—Offset 2Ch

Sub System Identifiers

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SSID):** Indicates the subsystem identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only.
15:0	0h RW/O	**Subsystem Vendor ID (SSVID):** Indicates the subsystem vendor identifier. This field should be programmed by BIOS during boot- up. Once written, this register becomes Read Only.

23.1.12 Capabilities Pointer (HECI1_CAP)—Offset 34h

Capabilities Pointer

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 50h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	50h RO	**Capability Pointer (CP):** Indicates the first capability pointer offset. It points to the PCI power management capability offset.

23.1.13 Maximum Latency (HECI1_MLAT)—Offset 3Fh

Maximum Latency

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RO	**Latency (LAT):** Not implemented, hardwired to 0.

23.1.14 Host Firmware Status (HECI1_HFS)—Offset 40h

Host Firmware Status

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Firmware Status Host Access (FS_HA):** Indicates current status of the firmware for the HECI controller. This field is the host's read only access to the FS field in the CSE Firmware Status register.

23.1.15 Miscellaneous Shadow (HECI1_MISC_SHDW)—Offset 44h

Miscellaneous Shadow

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 80000000h

Bit Range	Default and Access	Field Name (ID): Description
31	1h RO	**Miscellaneous Shadow Valid (MSVLD):** This bit is hardwired to 1 to indicate that this HECI device implements the Miscellaneous Shadow register. This bit can be used by host software that is bus/dev/function number agnostic (such as HECI operating system driver) to discover whether the Miscellaneous Shadow register is implemented or not.
30:17	0h RO	Reserved.
16	0h RO/V	**CSE UMA Size Valid (CUSZV):** This bit indicates that FW has written the CUSZ field. This field reflects the value of CSE CUBA.CUSZV.
15:12	0h RO	Reserved.
11:0	0h RO/V	**CSE UMA Size (CUSZ):** These bits reflect firmware's desired size of CSEUMA memory region at 1MB granularity, 1-based. It is configured by firmware prior to bring up core power and allowing BIOS to initialize memory. Example: 000h (0MB, no CSEUMA) 003h (3MB) 040h (64MB) FFFh (4GB) This field reflects the value of CSE CUBA.CUSZ.

23.1.16 General Status Shadow 1 (HECI1_GS_SHDW1)—Offset 48h

General Status Shadow 1

Access Method

Type: CFG Register (Size: 32 bits)
Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**General Status Shadow 1 (GSS1):** This field is host side shadow of CSE General Status 1 (CSE_GS1).

23.1.17 Host General Status (HECI1_H_GS1)—Offset 4Ch

Host General Status

Access Method

Type: CFG Register (Size: 32 bits)
Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Host General Status (H_GS1):** General status of Host. This field is not used by hardware.

23.1.18 PCI Power Management Capability ID (HECI1_PID)—Offset 50h

PCI Power Management Capability ID

Access Method

Type: CFG Register (Size: 16 bits)
Device: 22
Function: 0

Default: 8C01h

Bit Range	Default and Access	Field Name (ID): Description
15:8	8Ch RO	**Next Capability (NEXT):** Indicates the location of the next capability item in the list. This is the Message Signaled Interrupts capability.
7:0	1h RO	**Cap ID (CID):** Indicates that this pointer is a PCI power management.

23.1.19 PCI Power Management Capabilities (HECI1_PC)—Offset 52h

PCI Power Management Capabilities

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 22
Function: 0

Default: 4003h

Bit Range	Default and Access	Field Name (ID): Description
15:11	8h RO	**PME Support (PSUP):** Indicates the states that can generate PME#. HECI can assert PME# from D3hot only.
10	0h RO	**D2 Support (D2S):** The D2 state is not supported for the HECI host controller.
9	0h RO	**D1 Support (D1S):** The D1 state is not supported for the HECI host controller.
8:6	0h RO	**Aux Current (AUXC):** Reports the maximum Suspend well current required when in the D3COLD state. Value of 0 is reported.
5	0h RO	**Device Specific Initialization (DSI):** Indicates whether device-specific initialization is required.
4	0h RO	Reserved.
3	0h RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
2:0	3h RO	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification.

23.1.20 General Status Shadow 3 (HECI1_GS_SHDW3)—Offset 64h

General Status Shadow 3

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**General Status Shadow 3 (GSS3):** This field is host side shadow of CSE General Status 3 (CSE_GS3).

23.1.21 General Status Shadow 4 (HECI1_GS_SHDW4)—Offset 68h

General Status Shadow 4

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**General Status Shadow 4 (GSS4):** This field is host side shadow of CSE General Status 4 (CSE_GS4).

23.1.22 General Status Shadow 5 (HECI1_GS_SHDW5)—Offset 6Ch

General Status Shadow 5

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**General Status Shadow 5 (GSS5):** This field is host side shadow of CSE General Status 5 (CSE_GS5).

23.1.23 Host General Status 2 (HECI1_H_GS2)—Offset 70h

Host General Status 2

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Host General Status 2 (H_GS2):** General status of Host. This field is not used by hardware.

23.1.24 Host General Status 3 (HECI1_H_GS3)—Offset 74h

Host General Status 3

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Host General Status 3 (H_GS3):** General status of Host. This field is not used by hardware.

23.1.25 Message Signaled Interrupt Identifiers (HECI1_MID)—Offset 8Ch

Message Signaled Interrupt Identifiers

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 22
Function: 0

Default: A405h

Bit Range	Default and Access	Field Name (ID): Description
15:8	A4h RO	**Next Pointer (NEXT):** Indicates the location of the next capability item in the list. This is the DevIdle conventional PCI vendor specific capability.
7:0	5h RO	**Capability ID (CID):** Indicates MSI.

23.1.26 Message Signaled Interrupt Message Control (HECI1_MC)—Offset 8Eh

Message Signaled Interrupt Message Control

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 22
Function: 0

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7	1h RO	**64 Bit Address Capable (C64):** Specifies whether capable of generating 64-bit messages.
6:4	0h RO	**Multiple Message Enable (MME):** Not implemented, hardwired to 0.
3:1	0h RO	**Multiple Message Capable (MMC):** Not implemented, hardwired to 0.
0	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and INTx virtual wires are not used to generate interrupts.

23.1.27 Message Signaled Interrupt Message Address (HECI1_MA)—Offset 90h

Message Signaled Interrupt Message Address

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**Address (ADDR):** Lower 32 bits of the system specified message address, always DW aligned.
1:0	0h RO	Reserved.

23.1.28 Message Signaled Interrupt Upper Address (HECI1_MUA)—Offset 94h

Message Signaled Interrupt Upper Address

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Upper Address (UADDR):** Upper 32 bits of the system specified message address. This register is optional and only implemented if MC.C64=1.

23.1.29 Message Signaled Interrupt Message Data (HECI1_MD)—Offset 98h

Message Signaled Interrupt Message Data

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:0	0h RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the FSB during the data phase of the MSI memory write transaction.

23.1.30 HECI Interrupt Delivery Mode (HECI1_HIDM)—Offset A0h

HECI Interrupt Delivery Mode

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h RW/1S/V	**HIDM Lock (HIDM_L):** Writing 1 to this bit locks the HIDM field.
1:0	0h RW/L	**HECI Interrupt Delivery Mode (HIDM):** These bits control what type of interrupt the HECI will send when CSE FW writes to set the CSE_IG bit. They are interpreted as follows: 00 - Generate Legacy or MSI interrupt; 01 - Generate SCI; 10 - Generate SMI; This field may be locked by writing 1 to HIDM_L bit.

23.1.31 SW LTR Pointer Register (HECI1_SWLTRPTR)—Offset ACh

Software Latency Tolerance Reporting (LTR) Pointer Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	**SW LTR Update MMIO Offset Location (SWLTRLOC):** This register contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR. The value of this register is not valid, if the Valid bit is not set.
3:1	0h RO	**Base Address Register Number (BARNUM):** Contains the 0's based AR Number of the BAR which contains the location of the SW LTR MMIO register. When counting BAR Numbers, all BARs, regardless of size and type, consume one BAR Number. Bar 0 is the 1st BAR. The value of this register is not valid, if the Valid bit is not set.
0	0h RO	**Valid (Valid):** Set to 1'b1 to indicate that the function has implemented a SW LTR register as specified in the DevIdle that can be located using the SWLTRLOC register and BARNUM. Set to 1'b0 to indicate that the function has not implemented a SW LTR register that is compliant to the DevIdle definition. This could be because the function has not implemented SW LTR at all, or has a device specific version of SW LTR.

23.1.32 Device Idle Pointer Register (HECI1_DEVIDLEPTR)—Offset B0h

Device Idle Pointer Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 8001h

Bit Range	Default and Access	Field Name (ID): Description
31:4	800h RO	**Device Idle MMIO Offset Location (DEVIDLELOC):** This register contains the location pointer to the DevIdle register in MMIO space, as an offset from the specified BAR. The value of this register is not valid, if the Valid bit is not set.
3:1	0h RO	**Base Address Register Number (BARNUM):** Contains the 0's based AR Number of the BAR which contains the location of the SW LTR MMIO register. When counting BAR Numbers, all BARs, regardless of size and type, consume one BAR Number. Bar 0 is the 1st BAR. The value of this register is not valid, if the Valid bit is not set.
0	1h RO	**Valid (Valid):** Set to 1'b1 to indicate that the function has implemented a SW LTR register as specified DevIdle that can be located using the DEVIDLELOC register and BARNUM. Set to 1'b0 to indicate that the function has not implemented a DevIdle register that is compliant to the DevIdle definition. This could be because the function has not implemented SW LTR at all, or has a device specific version of device idle.

23.1.33 DevIdle Power Control Enabled Register (HECI1_PWRCTRLEN)—Offset B6h

DevIdle Power Control Enabled Register

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 22
Function: 0

Default: Eh

Bit Range	Default and Access	Field Name (ID): Description
15:6	0h RO	Reserved.
5	0h RO	**Hardware Autonomous Enable (HAE):** CSE does not support autonomous power gating on idle.
4	0h RO	Reserved.
3	1h RO	**Sleep Enable (SE):** CSE always asserts the sleep signal during power gating.
2	1h RO	**D3-Hot Enable (D3HEN):** CSE could power gate when idle and the PMCSR[1:0] register in the function =2'b11 (D3).
1	1h RO	**DEVIDLE Enable (DEVIDLEN):** CSE could power gate when idle and the DevIdle register (DevIdleC[2] = 1'b1) is set.
0	0h RO	**PMC Request Enable (PMCRE):** CSE will not power gate due to pmc_ip_sw_pg_req_b = LOW.

23.1.34 Host Extend Register DW4 (HECI1_HER4)—Offset CCh

Host Extend Register DW4

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Host Extend Register DW4 (ERDW4):** Host Extend Register DW4.

23.1.35 Host Extend Register DW6 (HECI1_HER6)—Offset D4h

Host Extend Register DW6

Access Method

Type: CFG Register (Size: 32 bits)
Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Host Extend Register DW6 (ERDW6):** Host Extend Register DW6.

23.1.36 Host Extend Register DW7 (HECI1_HER7)—Offset D8h

Host Extend Register DW7

Access Method

Type: CFG Register (Size: 32 bits)
Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Host Extend Register DW7 (ERDW7):** Host Extend Register DW7.

23.1.37 Host Extend Register DW8 (HECI1_HER8)—Offset DCh

Host Extend Register DW8

Access Method

Type: CFG Register (Size: 32 bits)
Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Host Extend Register DW8 (ERDW8):** Host Extend Register DW8.

23.2 Intel® CSE:HECI MMIO Registers

Table 23-2. Summary of Intel® CSE:HECI MMIO Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
800h	803h	DEVIDLE Control (HECI1_DEVIDLEC)—Offset 800h	0h
CBCh	CBFh	Host Enhanced Extend Register Status (HECI1_ENH_HERS)—Offset CBCh	0h

23.2.1 DEVIDLE Control (HECI1_DEVIDLEC)—Offset 800h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	0h RO	**Restore Required (RR)**
2	0h RW	**DevIdle (DEVIDLE):** SW sets this bit to 1'b1 to move the function into the DevIdle state. Writing this bit to 1'b0 will return the function to the fully active D0 state (D0i0).
1	0h RW	**Interrupt Request (IR):** SW sets this bit to 1'b1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.
0	0h RO/V	**Command-in-Progress (CIP):** HW sets this bit on a 1'b1->1'b0 or 1'b0->1'b1 transition of DEVIDLE. While set, the other bits in this register are not valid and it is unsupported for SW to write to any bit in this register. HW clears this bit when CSE FW clears its own DevIdle interrupt status bit indicating completion of the DevIdle transition command. When clear, all the other bits in the register are valid and SW may write to any bit. If Interrupt Request (IR) was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW. SW writes to this bit have no effect.

23.2.2 Host Enhanced Extend Register Status (HECI1_ENH_HERS)—Offset CBCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:31	0h	**Extend Register Valid (ERV)**
30	0h RO	Reserved.
29:30	0h	**Extend Feature Present (EFP)**
29	0h RO	Reserved.
28:29	0h	**Extend Complete (ERC)**
28:0	0h RO	Reserved.
-1:0	0h	**Extend Register Algorithm (ERA)**

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24 USB 3.2 Gen 2x1 (10 Gb/s) xHCI HC (D20: F0)

24.1 xHCI Configuration Registers

Table 24-1. Summary of xHCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	1h	Vendor ID (VID)—Offset 0h	8086h
2h	3h	Device ID (DID)—Offset 2h	34EDh
4h	5h	Command Reg (CMD)—Offset 4h	0h
6h	7h	Device Status (STS)—Offset 6h	290h
8h	8h	Revision ID (RID)—Offset 8h	0h
9h	9h	Programming Interface (PI)—Offset 9h	30h
Ah	Ah	Sub Class Code (SCC)—Offset Ah	3h
Bh	Bh	Base Class Code (BCC)—Offset Bh	Ch
Dh	Dh	Initiator Latency Timer (MLT)—Offset Dh	0h
Eh	Eh	Header Type (HT)—Offset Eh	80h
10h	17h	Memory Base Address (MBAR)—Offset 10h	4h
2Ch	2Dh	USB Subsystem Vendor ID (SSVID)—Offset 2Ch	0h
2Eh	2Fh	USB Subsystem ID (SSID)—Offset 2Eh	0h
34h	34h	Capabilities Pointer (CAP_PTR)—Offset 34h	70h
3Ch	3Ch	Interrupt Line (ILINE)—Offset 3Ch	0h
3Dh	3Dh	Interrupt Pin (IPIN)—Offset 3Dh	0h
40h	43h	XHC System Bus Configuration 1 (XHCC1)—Offset 40h	3401FDh
44h	47h	XHC System Bus Configuration 2 (XHCC2)—Offset 44h	3FC688h
50h	53h	Clock Gating (XHCLKGTEN)—Offset 50h	FDF6D3Fh
58h	5Bh	Audio Time Synchronization (AUDSYNC)—Offset 58h	0h
60h	60h	Serial Bus Release Number (SBRN)—Offset 60h	31h
61h	61h	Frame Length Adjustment (FLADJ)—Offset 61h	60h
62h	62h	Best Effort Service Latency (BESL)—Offset 62h	0h
70h	70h	PCI Power Management Capability ID (PM_CID)—Offset 70h	1h
71h	71h	Next Item Pointer 1 (PM_NEXT)—Offset 71h	80h
72h	73h	Power Management Capabilities (PM_CAP)—Offset 72h	C1C2h
74h	75h	Power Management Control/Status (PM_CS)—Offset 74h	8h
80h	80h	Message Signaled Interrupt CID (MSI_CID)—Offset 80h	5h
81h	81h	Next Item Pointer (MSI_NEXT)—Offset 81h	90h
82h	83h	Message Signaled Interrupt Message Control (MSI_MCTL)—Offset 82h	86h
84h	87h	Message Signaled Interrupt Message Address (MSI_MAD)—Offset 84h	0h

Table 24-1. Summary of xHCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
88h	8Bh	Message Signaled Interrupt Upper Address (MSI_MUAD)—Offset 88h	0h
8Ch	8Dh	Message Signaled Interrupt Message Data (MSI_MD)—Offset 8Ch	0h
A4h	A7h	High Speed Configuration 2 (HSCFG2)—Offset A4h	3800h
A8h	ABh	Super Speed Configuration 1 (SSCFG1)—Offset A8h	24000h

24.1.1 Vendor ID (VID)—Offset 0h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 8086h

Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RO	**Vendor ID (VID)**

24.1.2 Device ID (DID)—Offset 2h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 34EDh

Bit Range	Default & Access	Field Name (ID): Description
15:0	34EDh RO/V	**Device ID (DID):** See the Device and Version ID Table in Volume 1 for the default value.

24.1.3 Command Reg (CMD)—Offset 4h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (INTR_DIS)**
9	0h RO	**Fast Back to Back Enable (FBE)**
8	0h RW	**SERR# Enable (SERR):** When set to 1, the XHC is capable of generating (internally) SERR#.
7	0h RO	**Wait Cycle Control (WCC)**
6	0h RW	**Parity Error Response (PER)**
5	0h RO	**VGA Palette Snoop (VPS)**
4	0h RO	**Memory Write Invalidate (MWI)**
3	0h RO	**Special Cycle Enable (SCE)**
2	0h RW	**Bus Initiator Enable (BME)**
1	0h RW	**Memory Space Enable (MSE)**
0	0h RO	**I/O Space Enable (IOSE)**

24.1.4 Device Status (STS)—Offset 6h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 290h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**Detected Parity Error (DPE)**
14	0h RW/1C	**Signaled System Error (SSE):** This bit is set by the PCH whenever it signals SERR# (internally). The SERR_EN bit (bit 8 in the Command Register) must be 1 for this bit to be set.Software clears this bit by writing a 1 to this bit location.
13	0h RW/1C	**Received Initiator-Abort Status (RMA)**
12	0h RW/1C	**Received Target Abort Status (RTA)**
11	0h RW/1C	**Signaled Target-Abort Status (STA)**

Bit Range	Default & Access	Field Name (ID): Description
10:9	1h RO	**DEVSEL# Timing Status (DEVT)**
8	0h RW/1C	**Initiator Data Parity Error Detected (MDPED)**
7	1h RO	**Fast Back-to-Back Capable (FBBC)**
6	0h RO	**User Definable Features (UDF)**
5	0h RO	**66 MHz Capable (MC)**
4	1h RO	**Capabilities List (CL)**
3	0h RO/V	**Interrupt Status (INTR_STS)**
2:0	0h RO	Reserved.

24.1.5 Revision ID (RID)—Offset 8h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO/V	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

24.1.6 Programming Interface (PI)—Offset 9h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 30h

Bit Range	Default & Access	Field Name (ID): Description
7:0	30h RO	**Programming Interface (PI)**

24.1.7 Sub Class Code (SCC)—Offset Ah

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 3h

Bit Range	Default & Access	Field Name (ID): Description
7:0	3h RO	**Sub Class Code (SCC)**

24.1.8 Base Class Code (BCC)—Offset Bh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: Ch

Bit Range	Default & Access	Field Name (ID): Description
7:0	Ch RO	**Base Class Code (BCC)**

24.1.9 Initiator Latency Timer (MLT)—Offset Dh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Initiator Latency Timer (MLT)**

24.1.10 Header Type (HT)—Offset Eh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Multi-Function Bit (MFB)**
6:0	0h RO	**Configuration layout (CL)**

24.1.11 Memory Base Address (MBAR)—Offset 10h

Access Method

Type: CFG Register
(Size: 64 bits)

Device: 20
Function: 0

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
63:16	0h RW	**Base Address (BA)**
15:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PREFETCHABLE)**
2:1	2h RO	**Type (MBAR_TYPE)**
0	0h RO	**Resource Type Indicator (RTE)**

24.1.12 USB Subsystem Vendor ID (SSVID)—Offset 2Ch

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/L	**USB Subsystem Vendor ID (SSVID):** This register, in combination with the USB Subsystem ID register, enables the operating system to distinguish each subsystem from the others.

24.1.13 USB Subsystem ID (SSID)—Offset 2Eh

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/L	**USB Subsystem ID (SSID):** BIOS sets the value in this register to identify the Subsystem ID. This register, in combination with the Subsystem Vendor ID register, enables the operating system to distinguish each subsystem from other(s).

24.1.14 Capabilities Pointer (CAP_PTR)—Offset 34h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 70h

Bit Range	Default & Access	Field Name (ID): Description
7:0	70h RO	**Capabilities Pointer (CAP_PTR)**

24.1.15 Interrupt Line (ILINE)—Offset 3Ch

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Interrupt Line (ILINE)**

24.1.16 Interrupt Pin (IPIN)—Offset 3Dh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW/L	**Interrupt pin (IPIN)**

24.1.17 XHC System Bus Configuration 1 (XHCC1)—Offset 40h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 3401FDh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1L	**Access Control (ACCTRL):** This bit is used by BIOS to lock/unlock lockable bits. When set to '1' the write access to bits locked by this bit is disabled (locked state). When set to '0', the write access to bit locked by this bit is enabled (unlocked state). Writable once after platform reset.
30:25	0h RO	Reserved.
24	0h RW	**Initiator/Target Abort SERR (RMTASERR)**
23	0h RW/1C	**Unsupported Request Detected (URD)**
22	0h RW	**Unsupported Request Report Enable (URRE)**
21:19	6h RW	**Inactivity Initiated L1 Enable (IIL1E):** If programmed to non-zero, it allows L1 power managed to be enabled after the time-out period specified. 000: Disabled 001: 32 bb_cclk 010: 64 bb_cclk 011: 128 bb_cclk 100: 256 bb_cclk 101: 512 bb_cclk 110: 1024 bb_cclk 111: 131072 bb_cclk
18	1h RW	**XHC Initiated L1 Enable (XHCIL1E)**
17	0h RW	**D3 Initiated L1 Enable (D3IL1E):** If set, allow PCI device state D3 initiated L1 power managment to be enables.[BR
16:12	0h RO	Reserved.
11	0h RW	**SW Assisted xHC Idle (SWAXHCI):** This bit being set will indicate xHC idleness (through SW means), which must be a '1' to allow L1 entry, and subsequently allow backbone clock to be gated. This bit is to be set by Intel xHCI driver after checking that the xHCI Controller will stay in idle state for a significant period of time, e.g. all ports disconnected. This bit can be cleared under the following conditions (see SWAXHCI Policy bits in xHC System Bus Configuration 2 register) SW: SW could write 0 to clear this bit.n HW: HW, under policy control, will clear this bit on an MMIO access to the Host Controller.n HW: HW, under policy control, will clear this bit when HW exits Idle state.

Bit Range	Default & Access	Field Name (ID): Description
10:8	1h RW	**L23 to Host Reset Acknowledge Wait Count (L23HRAWC):** If programmed to non zero, it allows a wait period after the L23 PHY has shutdown before returning host reset acknowledge to PMC. 000: Disabled 001: 128 bb_cclk 010: 256 bb_cclk 011: 512 bb_cclk 100: 1024 bb_cclk 101: 2048 bb_cclk 110: 4096 bb_cclk 111: 131072 bb_cclk
7:6	3h RW	**Upstream Type Arbiter Grant Count Posted (UTAGCP)**
5:4	3h RW	**Upstream Type Arbiter Grant Count Non Posted (UDAGCNP)**
3:2	3h RW	**Upstream Type Arbiter Grant Count Completion (UDAGCCP) (UDAGCCP)**
1:0	1h RW	**Upstream Device Arbiter Grant Count (UDAGC) (UDAGC)**

24.1.18 XHC System Bus Configuration 2 (XHCC2)—Offset 44h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 3FC688h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**OC Configuration Done (OCCFGDONE)**
30	0h RW	**Enable Relaxed Ordering (RO_EN)**
29:28	0h RW	**MMIO Back to Back Rd/Wr Delay Count (RW_DLY_CNT)**
27:26	0h RO	Reserved.
25	0h RW	**DMA Request Boundary Crossing Control (DREQBCC):** This bit controls the boundary crossing limit of each Read/Write Request. 0: 4KB 1: 64B
24:22	0h RW	**IDMA Write Request Size Control (WRREQSZCTRL):** This bit controls the maximum size of each Write Request. 000: 128B 001: 256B 011 - 110: Reserved 111: 64B
21	1h RW	**XHC Upstream Read Relaxed Ordering Enable (XHCUPRDROE):** This policy controls the Relaxed Ordering attribute for upstream reads. 0 - xHC will clear RO for all upstream read requests. 1 - xHC will set RO for all upstream read requests.

Bit Range	Default & Access	Field Name (ID): Description
20:14	7Fh RW	**Upstream Non-Posted Pre-Allocation (UNPPA):** This field reserves data sizes, in 64 byte chunks, of the downstream completion resource. This value is zero based. 000000 - 111111: Pre-allocate 64 bytes - 4096 bytes If set greater than the default allows over-allocation If set less than default allows under-allocation Only allowed to be programmed when BME = 0 and no outstanding downstream completion
13:12	0h RW	**SW Assisted xHC Idle Policy (SWAXHCIP):** Note: Irrespective of the setting of this field, SW write of 0 to SWAXHCI will clear the bit. 00b (default): xHC HW clears SWAXHCI bit upon MMIO access to Host Controller OR xHC HW exits Idle state 01b: xHC HW does not autonomously clear SWAXHCI bit. The bit could be cleared only by SW. 10b: xHC HW clears SWAXHCI upon MMIO acces to Host Controller. xHC HW exit from Idle state will not clear SWAXHCI. 11b: Reserved
11	0h RW	**MMIO Read After MMIO Write Delay Disable (RAWDD):** This field controls delay on MMIO Read after MMIO Write. 0b (Default): Delay MMIO Read after MMIO Write 1b: Do not delay MMIO Read after MMIO Write Note that this delay applies after the second of the two DW writes in the case where the IOSF Gasket splits a QW write into two single DW writes to the IP.
10	1h RW	**MMIO Write After MMIO Write Delay Enable (WAWDE):** This field controls delay on MMIO Write after previous MMIO Write. 0b (Default): Do not delay MMIO Write after previous MMIO Write 1b: Delay MMIO Write after previous MMIO Write Note that the delay count does not apply on the second of the two DW writes that are generated by IOSF Gasket when it splits a QW write into two. In other words, the second of the two DW writes could happen without any delay with respect to the first DW write.The delay count, in this case, will apply after the second of the two DW writes.
9:8	2h RW	**SW Assisted Cx Inhibit (SWACXIHB):** This field controls how the DMI L1 inhibit signal from USB 3.1 to PMC will behave. 00: Never inhibit Cx 01: Inhibit Cx when Isochronous Endpoint is active (PPT Behavior) 10: Inhibit Cx when Periodic Active as defined in 40.4.3.2. 111: Always inhibit Cx
7:6	2h RW	**SW Assisted DMI L1 Inhibit (SWADMIL1IHB)**
5:3	1h RW	**L1 Force P2 Clock Gating Wait Count (L1FP2CGWC)**
2:0	0h RW	**Read Request Size Control (RDREQSZCTRL)**

24.1.19 Clock Gating (XHCLKGTEN)—Offset 50h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 0

Default: FDF6D3Fh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Frame Clk Gating When Active Periodic EPs On Scheduler (PRDCEP_FRCLK_GATEEN)**
30	0h RW	**Extend EU3S To U2 (EXTD_EU3S_TO_U2)**
29	0h RO	Reserved.
28	0h RW	**Nak'ing USB2.0 EPs for Backbone Clock Gating and PLL Shutdown (NUEFBCGPS):** This field controls whether Naking USB2.0 EPs, once in Naking low priority schedule, should be considered as active for the considerations for backbone clock gating and PLL shutdown or not. 0: Naking USB2.0 EPs are not considered to be active for Backbone Clock Gating and PLL Shutdown evaluation. 1: Naking USB2.0 EPs are considered to be active for Backbone clock gating and PLL shutdown evaluation.
27	1h RW	**SRAM Power Gate Enable (SRAMPGTEN):** This register enables the SRAM Power Gating when PLL shutdown conditions for all clock domains have been met 0 - Disallow SRAM Power Gating. 1 - Allow SRAM Power Gating
26	1h RW	**SS Link PLL Shutdown Enable (SSLSE):** This register enables the SS P3 state to be exposed to PXP PLL Shutdown conditions on behalf of all USB SS Ports ontop of trunk clock gating. 0 - P3 state NOT allowed to result in PXP PLL shutdown. 1- P3 state allowed to result in PXP PLL shutdown
25	1h RW	**USB2 PLL Shutdown Enable (USB2PLLSE):** When set, this bit allows USB2 PLL to be shutdown when HS Link trunk clock is gated, and xHC can tolerate PLL spin up time for subsequent clock request.
24	1h RW	**IOSF Sideband Trunk Clock Gating Enable (IOSFSTCGE):** When set, this bit allows the IOSF sideband clock trunk to be gated when idle conditions are met.
23:20	Dh RW	**HS Backbone PXP Trunk Clock Gate Enable (HSTCGE):** This register determines the HS Ux state(s) which will be exposed to Backbone PXP trunk gating of core clock. Uy is a state allowed to result in trunk gating when ss_tcg_ux_en(x) is asserted. (0) ==) U0 or deeper (1) ==) NA (no support for U1) (2) ==) U2 (L1) or deeper (3) ==) U3 (L2) or deeper
19:16	Fh RW	**SS Backbone PXP Trunk Clock Gate Enable (SSTCGE):** This register determines the SS Ux state(s) which will be exposed to Backbone PXP trunk gating of core clock. Uy is a state allowed to result in trunk gating when ss_tcg_ux_en(x) is asserted. (0) ==> U0 or deeper (1) ==> U1 or deeper (2) ==> U2 or deeper (3) ==> U3 or deeper
15	0h RW	**XHC Ignore_EU3S (XHCIGEU3S):** This register determines if the xHC will use the EU3S as a condition to allow for Frame timer gating. 0 - xHC may allow frame timer to be gated when EU3S is set and all ports are in the required state. 1 - xHC may allow frame timer to be gated regardless of EU3S.
14	1h RW	**XHC Frame Timer Clock Shutdown Enable (XHCFTCLKSE):** This register determines if the xHC will allow the frame timer clock to be gated. 0 - xHC will not allow ICC PLL 96MHz output to be shutdown thus keeping the frame timer running. 1 - xHC will allow ICC PLL 96MHz output to be shutdown under specific conditions.
13	1h RW	**XHC Backbone PXP Trunk Clock Gate In Presence of ISOCH EP (XHCBBTCGIPISO):** This register controls the policy on allowing Backbone PXP trunk clock gate in the presence of IDLE ISOCH EP s with active DB. Allows the periodic active to be used in enabling Backbone PXP trunk clock gating of core clock. 0 - Trunk gate of core clock is not allowed when ISOCH EP DB is set and ISOCH EP s are idle. 1 - Allow trunk gate of core clock when ISOCH EP DB is set and ISOCH EP s are idle.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**XHC HS Backbone PXP Trunk Clock Gate U2 non RWE (XHCHSTCGU2NRWE):** This register controls the policy on allowing Backbone PXP trunk gating of core clock when there is atleast 1 non Remote Wake Enabled HS Port in U2. 0 - Prevent trunk gate of core clock when a non RWE HS Port is in U2. 1 - Allow trunk gate of core clock when a non RWE HS Port is in U2.
11:10	3h RW	**XHC USB2 PLL Shutdown Lx Enable (XHCUSB2PLLSDLE):** This register determines the HS Link state(s) which will be exposed to USB2 PLL Shutdown conditions on behalf of all USB2 HS Ports. Ly is a state allowed to result in USB2 PLL Shutdown when en(x) is asserted. (0) ==> L1 or deeper (1) ==> L2 or deeper
9:8	1h RW	**HS Backbone PXP PLL Shutdown Ux Enable (HSUXDMIPLLSE):** This register determines the Ux state(s) which will be exposed to PXP PLL Shutdown conditions. PLL Shutdown is allowed in: 00b Disabled (Link states shall be disabled for DMI PLL shutdown) 01b U0 or conditions for 10b setting. 10b U2 or conditions for 11b setting. 10b U3, Disconnected, Disabled or Powered-Off.
7:5	1h RW	**SS Backbone PXP PLL Shutdown Ux Enable (SSPLLSUE):** This register determines the Ux state(s) which will be exposed to DMI PLL Shutdown conditions. PLL Shutdown is allowed in: 000b Disabled (Link states shall be ignored for DMI PLL shutdown). 001b U0 or conditions for 010b setting. 010b U1 or conditions for 011b setting. 011b U2 or conditions for 100b setting. 100b U3, Disconnected, Disabled or Powered-Off
4	1h RW	**XHC Backbone Local Clock Gating Enable (XHCBLCGE):** When set, this bit allows XHCI Controller IP backbone clock to be locally gated when idle conditions are met.
3	1h RW	**HS Link Trunk Clock Gating Enable (HSLTCGE):** When set, this bit allows High Speed Link control's 480 MHz and its 48/60 MHz link clock trunk to be gated when idle conditions are met.
2	1h RW	**SS Link Trunk Clock Gating Enable (SSLTCGE):** When set, this bit allows the SuperSpeed Link control's 250 MHz and its divided 125 MHz link clock trunk to ge gated when idle conditions are met.
1	1h RW	**IOSF Backbone Trunk Clock Gating Enable (IOSFBTCGE)**
0	1h RW	**IOSF Gasket Backbone Local Clock Gating Enable (IOSFBLCGE):** When set, this bit allows the IOSF Gasket backbone clock to be locally gated when idle conditions are met.

24.1.20 Audio Time Synchronization (AUDSYNC)—Offset 58h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:16	0h RO/V	**Captured Frame List Current Index/Frame Number (CMFI)**
15:13	0h RO	Reserved.
12:0	0h RO/V	**Captured Micro-frame BLIF (CMFB)**

24.1.21 Serial Bus Release Number (SBRN)—Offset 60h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 31h

Bit Range	Default & Access	Field Name (ID): Description
7:0	31h RO	**Serial Bus Release Number (SBRN)**

24.1.22 Frame Length Adjustment (FLADJ)—Offset 61h

This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written into these six bits, the length of the frame is adjusted. Its initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system BIOS. This register should only be modified when the HChalted bit in the USBSTS register is a one. Changing value of this register while the host controller is operating yields undefined results.

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 60h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6	1h RO	**No Frame Length Timing Capability (NO_FRAME_LENGTH_TIMING_CAP)**
5:0	20h RO	**Frame Length Timing Value (FLTV):** SOF (micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (number of High Speed bit times) FLADJ Value (decimal) (decimal) 59488 0 (00h) 59504 1 (01h) 59520 2 (02h) ... 59984 31 (1Fh) 60000 32 (20h) ... 60480 62 (3Eh) 60496 63 (3Fh) Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (# High Speed bit times) FLADJ Value

24.1.23 Best Effort Service Latency (BESL)—Offset 62h

Access Method

Type: CFG Register (Size: 8 bits)
Device: 20
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RW/L	**Default Best Effort Service Latency Deep (DBESLD):** If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESLD field. This is programmed by BIOS based on platform parameters.
3:0	0h RW/L	**Default Best Effort Service Latency (DBESL):** If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESL field. This is programmed by BIOS based on platform parameters.

24.1.24 PCI Power Management Capability ID (PM_CID)—Offset 70h

Access Method

Type: CFG Register (Size: 8 bits)
Device: 20
Function: 0

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
7:0	1h RO	**PCI Power Management Capability ID (PM_CID)**

24.1.25 Next Item Pointer 1 (PM_NEXT)—Offset 71h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
7:0	80h RW/L	**Next Item Pointer 1 (PM_NEXT):** This register defaults to 80h, which indicates that the next capability registers begin at configuration offset 80h. This register is writable when the Access Control bit is set to '0'. This allows BIOS to effectively hide the next capability registers, if necessary. This register should only be written during system initialization before the plug-and-play software has enabled any Initiator-initiated traffic. Values of: 80h implies next capability is MSI 00h implies that MSI capability is hidden. Note: This value is never expected to be programmed.

24.1.26 Power Management Capabilities (PM_CAP)—Offset 72h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: C1C2h

Bit Range	Default & Access	Field Name (ID): Description
15:11	18h RW/L	**PME_Support (PME_SUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. The PCH XHC does not support the D1 or D2 states. For all other states, the PCH XHC is capable of generating PME#. Software should never need to modify this field.
10	0h RW/L	**D2_Support (D2_SUPPORT)**
9	0h RW/L	**D1_Support (D1_SUPPORT)**
8:6	7h RW/L	**Aux_Current (AUX_CURRENT)**
5	0h RW/L	**DSI (DSI)**
4	0h RO	Reserved.
3	0h RW/L	**PME Clock (PMECLOCK)**
2:0	2h RW/L	**Version (VERSION)**

24.1.27 Power Management Control/Status (PM_CS)—Offset 74h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**PME_Status (PME_STATUS)**
14:13	0h RO	**Data_Scale (DATA_SCALE)**
12:9	0h RO	**Data_Select (DATA_SELECT)**
8	0h RW	**PME_En (PME_EN)**
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset (NSR)**
2	0h RO	Reserved.
1:0	0h RW	**PowerState (POWERSTATE)**

24.1.28 Message Signaled Interrupt CID (MSI_CID)—Offset 80h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 5h

Bit Range	Default & Access	Field Name (ID): Description
7:0	5h RO	**Capability ID (CID)**

24.1.29 Next Item Pointer (MSI_NEXT)—Offset 81h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 90h

Bit Range	Default & Access	Field Name (ID): Description
7:0	90h RW/L	**Next Pointer (NEXT_POINTER)**

24.1.30 Message Signaled Interrupt Message Control (MSI_MCTL)—Offset 82h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 86h

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	Reserved.
8	0h RO	**Per-Vector Masking Capable (PVM)**
7	1h RO	**64 Bit Address Capable (C64)**
6:4	0h RW	**Multiple Message Enable (MME)**
3:1	3h RO	**Multiple Message Capable (MMC):** Indicates the number of messages the controller wishes to assert.This field must be set by HW to reflect the number of Interrupters supported. Encoding number of Vectors requested (number of Interrupters) 000 1 001 2 010 4 011 8 100 16 101 32 110-111 Reserved
0	0h RW	**MSI Enable (MSIE)**

24.1.31 Message Signaled Interrupt Message Address (MSI_MAD)—Offset 84h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Addr (ADDR)**
1:0	0h RO	Reserved.

24.1.32 Message Signaled Interrupt Upper Address (MSI_MUAD)—Offset 88h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Upper Addr (UPPERADDR)**

24.1.33 Message Signaled Interrupt Message Data (MSI_MD)—Offset 8Ch

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data (DATA)**

24.1.34 High Speed Configuration 2 (HSCFG2)—Offset A4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 3800h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18	0h RW	**PORT1_HOST_MODE_OVERRIDE (PORT1_HOST_MODE_OVERRIDE)**
17:16	0h RW	**eUSB2SEL (EUSB2SEL)**
15	0h RW	**HS ASYNC Active IN Mask (HSAAIM)**

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**HS OUT ASYNC Active Polling EP Mask (HSOAAPEPM)**
13	1h RW	**HS IN ASYNC Active Polling EP Mask (HSIAAPEPM)**
12:11	3h RW	**HS INTR IN Periodic Active Policy Control (HSIIPAPC)**
10:4	0h RW	**HS INTR IN Periodic Active Num of EP Threshold (HSIIPANEPT)**
3:0	0h RW	**HS INTR IN Periodic Active Service Interval Threshold (HSIIPASIT)**

24.1.35 Super Speed Configuration 1 (SSCFG1)—Offset A8h

This register is modified and maintained by BIOS

Access Method

Type: CFG Register (Size: 32 bits)
Device: 20
Function: 0

Default: 24000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	1h RW	**LFPS Power Management Enable (LFPSPME):** This field provides programmability of the USB LFPS Receiver power management capability when USB3.0 ports are Disabled or in Disconnected state. 0: Do not power manage LFPS receiver. LFPS receivers are enabled in all states 1: Power manage LFPS receiver. LFPS receivers will be turned off if USB3.0 port is Disabled or Disconnected
16:15	0h RO	Reserved.
14	1h RW	**MODPHY Power Gate Enable for U2 (MPHYPGEU2):** This bit controls whether xHC will allow PHY power gating or not when a port is in U2 state. Note that this single bit controls all ports of xHC. 0b xHC shall not initiate Power Gate Request when in U2 1b xHC is enabled to initiate Power Gate Request when in U2 if power gating conditions are met.
13:0	0h RO	Reserved.

24.2 xHCI Memory Mapped Registers

Table 24-2. Summary of xHCI Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	0h	Capability Registers Length (CAPLENGTH)—Offset 0h	80h
2h	3h	Host Controller Interface Version Number (HCIVERSION)—Offset 2h	110h
4h	7h	Structural Parameters 1 (HCSPARAMS1)—Offset 4h	10000840h

Table 24-2. Summary of xHCI Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
8h	Bh	Structural Parameters 2 (HCSPARAMS2)—Offset 8h	14200054h
Ch	Fh	Structural Parameters 3 (HCSPARAMS3)—Offset Ch	A0000Ah
10h	13h	Capability Parameters (HCCPARAMS)—Offset 10h	20007FC1h
14h	17h	Doorbell Offset (DBOFF)—Offset 14h	3000h
18h	1Bh	Runtime Register Space Offset (RTSOFF)—Offset 18h	2000h
80h	83h	USB Command (USBCMD)—Offset 80h	0h
84h	87h	USB Status (USBSTS)—Offset 84h	1h
88h	8Bh	Page Size (PAGESIZE)—Offset 88h	1h
94h	97h	Device Notification Control (DNCTRL)—Offset 94h	0h
98h	9Bh	Command Ring Low (CRCR_LO)—Offset 98h	0h
9Ch	9Fh	Command Ring High (CRCR_HI)—Offset 9Ch	0h
B0h	B3h	Device Context Base Address Array Pointer Low (DCBAAP_LO)—Offset B0h	0h
B4h	B7h	Device Context Base Address Array Pointer High (DCBAAP_HI)—Offset B4h	0h
480h	483h	Port N Status and Control USB2 (PORTSCN)—Offset 480h	2A0h
484h	487h	Port Power Management Status Aand Control USB2 (PORTPMSCN)—Offset 484h	0h
48Ch	48Fh	Port N Hardware LPM Control Register (PORTHLPMCN)—Offset 48Ch	0h
540h	543h	Port Status And Control USB3 (PORTSCXUSB3)—Offset 540h	2A0h
544h	547h	Port Power Management Status And Control USB3 (PORTPMSCX)—Offset 544h	0h
548h	54Bh	USB3 Port X Link Info (PORTLIX)—Offset 548h	0h
2000h	2003h	Microframe Index (RTMFINDEX)—Offset 2000h	0h
2020h	2023h	Interrupter x Management (IMANx)—Offset 2020h	0h
2024h	2027h	Interrupter x Moderation (IMODx)—Offset 2024h	FA0h
2028h	202Bh	Event Ring Segment Table Size x (ERSTSZx)—Offset 2028h	0h
2030h	2033h	Event Ring Segment Table Base Address Low x (ERSTBA_LOx)—Offset 2030h	0h
2034h	2037h	Event Ring Segment Table Base Address High x (ERSTBA_HIx)—Offset 2034h	0h
2038h	203Bh	Event Ring Dequeue Pointer Low x (ERDP_LOx)—Offset 2038h	0h
203Ch	203Fh	Event Ring Dequeue Pointer High x (ERDP_HIx)—Offset 203Ch	0h
3000h	3003h	Door Bell x (DBx)—Offset 3000h	0h
8000h	8003h	XECP SUPP USB2_0 (XECP_SUPP_USB2_0)—Offset 8000h	2000802h
8004h	8007h	XECP SUPP USB2_1 (XECP_SUPP_USB2_1)—Offset 8004h	20425355h
8008h	800Bh	XECP SUPP USB2_2 (XECP_SUPP_USB2_2)—Offset 8008h	30180C01h
800Ch	800Fh	XECP SUPP USB3_3 (XECP_SUPP_USB2_3)—Offset 800Ch	0h
8010h	8013h	XECP SUPP USB2_4 Full Speed (XECP_SUPP_USB2_4)—Offset 8010h	C0021h
8014h	8017h	XECP_SUPP USB2_5 Low Speed (XECP_SUPP_USB2_5)—Offset 8014h	5DC0012h
8018h	801Bh	XECP SUPP USB2_6 High Speed (XECP_SUPP_USB2_6)—Offset 8018h	1E00023h
8020h	8023h	XECP SUPP USB3_0 (XECP_SUPP_USB3_0)—Offset 8020h	3101402h

Table 24-2. Summary of xHCI Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
8024h	8027h	XECP SUPP USB3_1 (XECP_SUPP_USB3_1)—Offset 8024h	20425355h
8028h	802Bh	XECP SUPP USB3_2 (XECP_SUPP_USB3_2)—Offset 8028h	8000040Dh
802Ch	802Fh	XECP SUPP USB3_3 (XECP_SUPP_USB3_3)—Offset 802Ch	0h
8030h	8033h	XECP SUPP USB3_4 (XECP_SUPP_USB3_4 (USB 3.2 Gen 1x1))—Offset 8030h	50134h
8034h	8037h	XECP SUPP USB3_5 (XECP_SUPP_USB3_5 (USB 3.2 Gen 2x1))—Offset 8034h	A4135h
8038h	803Bh	XECP SUPP USB3_6 (XECP_SUPP_USB3_6)—Offset 8038h	4E00126h
803Ch	803Fh	XECP SUPP USB3_7 (XECP_SUPP_USB3_7)—Offset 803Ch	9C00127h
8040h	8043h	XECP SUPP USB3_8 (XECP_SUPP_USB3_8)—Offset 8040h	13800128h
8044h	8047h	XECP SUPP USB3_9 (XECP_SUPP_USB3_9)—Offset 8044h	5B10129h
8094h	8097h	Host Control Scheduler (HOST_CTRL_SCH_REG)—Offset 8094h	140h
80A4h	80A7h	Power Management Control (PMCTRL_REG)—Offset 80A4h	492D5094h
80B0h	80B3h	Host Controller Misc Reg (HOST_CTRL_MISC_REG)—Offset 80B0h	37Fh
80B4h	80B7h	Host Controller Misc Reg2 (HOST_CTRL_MISC_REG2)—Offset 80B4h	0h
80B8h	80BBh	Super Speed Port Enable (SSPE_REG)—Offset 80B8h	0h
80E0h	80E3h	AUX Power Management Control (AUX_CTRL_REG1)—Offset 80E0h	8080BCE0h
80ECh	80EFh	SuperSpeed Port Link Control (HOST_CTRL_PORT_LINK_REG)—Offset 80ECh	18000C00h
80F0h	80F3h	USB2 Port Link Control 1 (USB2_LINK_MGR_CTRL_REG1)—Offset 80F0h	314803A0h
80FCh	80FFh	USB2 Port Link Control 4 (USB2_LINK_MGR_CTRL_REG4)—Offset 80FCh	8003h
8140h	8143h	Power Scheduler Control-0 (PWR_SCHED_CTRL0)—Offset 8140h	FF01903C
8144h	8147h	Power Scheduler Control-1 (PWR_SCHED_CTRL2)—Offset 8144h	23Fh
8154h	8157h	AUX Power Management Control (AUX_CTRL_REG2)—Offset 8154h	1192206h
8164h	8167h	USB2 PHY Power Management Control (USB2_PHY_PMC)—Offset 8164h	FCh
816Ch	816Fh	XHCI Aux Clock Control Register (XHCI_AUX_CCR)—Offset 816Ch	F403Ch
8174h	8177h	XHC Latency Tolerance Parameters LTV Control (XLTP_LTV1)—Offset 8174h	1400C01h
817Ch	817Fh	XHC Latency Tolerance Parameters High Idle Time Control (XLTP_HITC)—Offset 817Ch	50002h
8180h	8183h	XHC Latency Tolerance Parameters Medium Idle Time Control (XLTP_MITC)—Offset 8180h	50002h
8184h	8187h	XHC Latency Tolerance Parameters Low Idle Time Control (XLTP_LITC)—Offset 8184h	50002h
81B8h	81BBh	LFPS On Count (LFPSONCOUNT_REG)—Offset 81B8h	20C8h
81C4h	81C7h	USB2 PM Control (USB2PMCTRL_REG)—Offset 81C4h	908h
846Ch	846Fh	USB Legacy Support Capability (USBLEGSUP)—Offset 846Ch	2201h
84F4h	84F7h	Port Disable Override Capability Register (PDO_CAPABILITY)—Offset 84F4h	3C6h
84F8h	84FBh	USB2 Port Disable Override (USB2PDO)—Offset 84F8h	0h
84FCh	84FFh	USB3 Port Disable Override (USB3PDO)—Offset 84FCh	0h
8700h	8703h	Debug Capability ID Register (DCID)—Offset 8700h	5100Ah
8E10h	8E13h	Global Time Sync Capability (GLOBAL_TIME_SYNC_CAP_REG)—Offset 8E10h	12C9h

Table 24-2. Summary of xHCI Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
8E14h	8E17h	Global Time Sync Control (GLOBAL_TIME_SYNC_CTRL_REG)—Offset 8E14h	0h
8E18h	8E1Bh	Microframe Time (Local Time) (MICROFRAME_TIME_REG)—Offset 8E18h	0h
8E20h	8E23h	Always Running Time (ART) Low (ALWAYS_RUNNING_TIME_LOW)—Offset 8E20h	0h
8E24h	8E27h	Always Running Time (ART) High (ALWAYS_RUNNING_TIME_HIGH)—Offset 8E24h	0h
90A4h	90A7h	XHCI USB2 Overcurrent Pin Mapping (U2OCM1)—Offset 90A4h	0h
90A8h	90ABh	XHCI USB2 Overcurrent Pin Mapping (U2OCM2)—Offset 90A8h	0h
90ACh	90AFh	XHCI USB2 Overcurrent Pin Mapping (U2OCM3)—Offset 90ACh	0h
90B0h	90B3h	XHCI USB2 Overcurrent Pin Mapping (U2OCM4)—Offset 90B0h	0h
90B4h	90B7h	XHCI USB2 Overcurrent Pin Mapping (U2OCM5)—Offset 90B4h	0h
90B8h	90BBh	XHCI USB2 Overcurrent Pin Mapping (U2OCM6)—Offset 90B8h	0h
90BCh	90BFh	XHCI USB2 Overcurrent Pin Mapping (U2OCM7)—Offset 90BCh	0h
90C0h	90C3h	XHCI USB2 Overcurrent Pin Mapping (U2OCM8)—Offset 90C0h	0h
9124h	9127h	XHCI USB3 Overcurrent Pin Mapping (U3OCM1)—Offset 9124h	0h
9128h	912Bh	XHCI USB3 Overcurrent Pin Mapping (U3OCM2)—Offset 9128h	0h
912Ch	912Fh	XHCI USB3 Overcurrent Pin Mapping (U3OCM3)—Offset 912Ch	0h
9130h	9133h	XHCI USB3 Overcurrent Pin Mapping (U3OCM4)—Offset 9130h	0h
9134h	9137h	XHCI USB3 Overcurrent Pin Mapping (U3OCM5)—Offset 9134h	0h
9138h	913Bh	XHCI USB3 Overcurrent Pin Mapping (U3OCM6)—Offset 9138h	0h
913Ch	913Fh	XHCI USB3 Overcurrent Pin Mapping (U3OCM7)—Offset 913Ch	0h
9140h	9143h	XHCI USB3 Overcurrent Pin Mapping (U3OCM8)—Offset 9140h	0h

24.2.1 Capability Registers Length (CAPLENGTH)—Offset 0h

Access Method

Type: MEM Register
(Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
7:0	80h RW/L	**Capability Registers Length (CAPLENGTH):** This register is used as an offset to add to the Memory Base Register to find the beginning of the Operational Register Space.

24.2.2 Host Controller Interface Version Number (HCIVERSION)—Offset 2h

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 110h

Bit Range	Default & Access	Field Name (ID): Description
15:0	110h RW/L	**Host Controller Interface Version Number (HCIVERSION):** This is a two-byte register containing a BCD encoding of the version number of interface that this host controller interface conforms.

24.2.3 Structural Parameters 1 (HCSPARAMS1)—Offset 4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 10000840h

Bit Range	Default & Access	Field Name (ID): Description
31:24	10h RW/L	**Number of Ports (MAXPORTS):** This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Default value = 0Eh
23:19	0h RO	Reserved.
18:8	8h RW/L	**Number of Interrupters (MAXINTRS):** This field specifies the number of interrupters implemented on this host controller. Each interrupter is allocated to a vector of MSI and controls its generation and moderation.
7:0	40h RW/L	**Number of Device Slots (MAXSLOTS):** This field specifies the number of Device Context Structures and Doorbell Array entries this host controller can support. Valid values are in the range of 1 to 255.

24.2.4 Structural Parameters 2 (HCSPARAMS2)—Offset 8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 14200054h

Bit Range	Default & Access	Field Name (ID): Description
31:27	2h RW/L	**Max Scratchpad Buffers LO (MAXSCRATCHPADBUFS):** Indicates the number of Scratchpad Buffers system software shall reserve for the xHC.
26	1h RW/L	**Scratchpad Restore (SPR):** 0 = Indicates the Scratchpad buffer space may be freed and reallocated between power events. 1 = Indicates that the xHC requires the integrity of the Scratchpad buffer space to be maintained across power events.
25:21	1h RW/L	**Max Scratchpad Buffers HI (MAXSCRATCHPADBUFS_HI)**
20:8	0h RO	Reserved.
7:4	5h RW/L	**Event Ring Segment Table Max (ERSTMAX):** This field determines the maximum value supported by the Event Ring Segment Table Base Size registers.
3:0	4h RW/L	**Isochronous Scheduling Threshold (IST):** This field indicates to system software the minimum distance (in time) that it is required to stay ahead of the xHC while adding TRBs, in order to have the xHC process them at the correct time. The value is specified in the number if frames/ microframes. If bit [3] of IST is cleared to 0b, software can add a TRB no later than IST [2:0] microframes before that TRB is scheduled to be executed. If bit [3] of IST is set to 1b, software can add a TRB no later than IST[2:0] frames before that TRB is scheduled to be executed.

24.2.5 Structural Parameters 3 (HCSPARAMS3)—Offset Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: A0000Ah

Bit Range	Default & Access	Field Name (ID): Description
31:16	A0h RW/L	**U2 Device Exit Latency (U2DEL):** Indicates the worst case latency to transition from U2 to U0. Applies to all root hub ports. The following are permissible values: Value Description 00h Zero 01h Less than 1 µs 02h Less than 2 µs ... 0Bh-FFh Reserved
15:8	0h RO	Reserved.
7:0	Ah RW/L	**U1 Device Exit Latency (U1DEL):** Worst case latency to transition a root hub Port Link State (PLS) from U1 to U0. Applies to all root hub ports. The following are permissible values: Value Description 00h Zero 01h Less than 1 µs 02h Less than 2 µs ... 0800h-FFFFh Reserved

24.2.6 Capability Parameters (HCCPARAMS)—Offset 10h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 20007FC1h

Bit Range	Default & Access	Field Name (ID): Description
31:16	2000h RW/L	**xHCI Extended Capabilities Pointer (XECP):** This field indicates the existence of a capabilities list. The value of this field indicates a relative offset, in 32-bit words, from Base to the beginning of the first extended capability.
15:12	7h RW/L	**Maximum Primary Stream Array Size (MAXPSASIZE):** RW/L. This fields identifies the maximum size Primary Stream Array that the xHC supports. The Primary Stream Array size = 2MaxPSASize+1. Valid MaxPSASize values are 1 to 15.
11	1h RW/L	**Contiguous Frame ID Capability (CFC)**
10	1h RW/L	**Stopped EDLTA Capabilty (SEC):** This flag indicates that the host controller implementation Stream Context support a Stopped EDLTA field.
9	1h RW/L	**Stopped - Short Packet Capability (SPC):** This flag indicates that the host controller implementation is capable of generating a Stopped-Short Packet Completion Code.
8	1h RW/L	**Parst All Event Data (PAE)**
7	1h RW/L	**No Secondary SID Support (NSS):** Hardwired to '0' indicating Secondary Stream ID decoding is supported.
6	1h RW/L	**Latency Tolerance Messaging Capability (LTC):** 0 = Latency Tolerance Messaging is not supported. 1 = Latency Tolerance Messaging is supported
5	0h RW/L	**Light HC Reset Capability (LHRC):** 0 = Light Host Controller Reset is not supported. 1 = Light Host Controller Reset is supported
4	0h RW/L	**Port Indicators (PIND):** This bit indicates whether the xHC root hub ports support port indicator control. When this bit is a '1', the port status and control registers include a read/writeable field for controlling the state of the port indicator.
3	0h RW/L	**Port Power Control (PPC):** This bit indicates whether the host controller implementation includes port power control. A '1' in this bit indicates the ports have port power switches. A '0' in this bit indicates the port do not have port power switches.
2	0h RW/L	**Context Size (CSZ):** If this bit is set to '1', then the xHC uses 64 byte Context data structures. If this bit is cleared to '0', then the xHC uses 32 byte Context data structures.
1	0h RW/L	**BW Negotiation Capability (BNC):** 0 = Not capable of BW Negotiation. 1 = Capable of BW Negotiation.
0	1h RW/L	**64-bit Addressing Capability (AC64):** This bit documents the addressing range capability of the xHC. The value of this flag determines whether the xHC has implemented the high order 32- bits of 64-bit register and data structure pointer fields. Values for this flag have the following interpretation: 0 = Supports 32-bit address memory pointers 1 = Supports 64-bit address memory pointers If 32-bit address memory pointers are implemented, the xHC shall ignore the high order 32- bits of 64-bit data structure pointer fields, and system software shall ignore the high order 32- bits of 64- bit xHC registers.

24.2.7 Doorbell Offset (DBOFF)—Offset 14h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 3000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	C00h RO	**Doorbell Array Offset (DBAO):** This field defines the DWord offset of the Doorbell Array base address from the Base (for example, the base address of the xHCI Capability register address space).
1:0	0h RO	Reserved.

24.2.8 Runtime Register Space Offset (RTSOFF)—Offset 18h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 2000h

Bit Range	Default & Access	Field Name (ID): Description
31:5	100h RO	**Runtime Register Space Offset (RTRSO):** This field defines the 32-byte offset of the xHCI Runtime Registers from the Base. That is, Runtime Register Base Address = Base + Runtime Register Set Offset.
4:0	0h RO	Reserved.

24.2.9 USB Command (USBCMD)—Offset 80h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW	**Enable U3 MFINDEX Stop (EU3S):** When set to 1b, the xHC may stop the MFINDEX counting action if all Root Hub ports are in the U3, Disconnected, Disabled, or Powered-off state. When cleared to 0b, the xHC may stop the MFINDEX counting action if all Root Hub ports are in the Disconnected, Disabled, or Powered-off state.
10	0h RW	**Enable Wrap Event (EWE):** When set to 1b, the xHC shall generate a MFINDEX Wrap Event every time the MFINDEX register transitions from 03FFFh to 0. When cleared to 0b, no MFINDEX Wrap Events are generated.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Controller Restore State (CRS):** When set to 1b, MEM_BASE+80h:bit 0= 0b, and MEM_BASE+80h:bit 8 = 1b, the xHC shall perform a Restore State operation and restore its internal state. When set to 1b and MEM_BASE+80h:bit 0= 1b or MEM_BASE+80h:bit 8 = 0b, or when cleared to '0', no Restore State operation shall be performed.
8	0h RW	**Controller Save State (CSS):** When written by software with 1b and MEM_BASE+80h:bit 0=0b, the xHC shall save any internal state that will be restored by a subsequent Restore State operation. When written by software with 1b and MEM_BASE+80h:bit 0= 1b, or written with '0', no Save State operation shall be performed.
7	0h RW	**Light Host Controller Reset (LHCRST):** If the Light HC Reset Capability (LHRC) bit (MEM_BASE=10h:bit 5) is 1b, then setting this bit to 1b allows the driver to reset the xHC without affecting the state of the ports. A system software read of this bit as 0b indicates the Light Host Controller Reset has completed and it is safe for software to re-initialize the xHC. A software read of this bit as a 1b indicates the Light Host Controller Reset has not yet completed.
6:4	0h RO	Reserved.
3	0h RW	**Host System Error Enable (HSEE):** When this bit is set to 1b, and the HSE bit (MEM_BASE+84h:bit 2) is set to 1b, the xHC shall assert out-of-band error signaling to the host. The signaling is acknowledged by software clearing the HSE bit.
2	0h RW	**Interrupter Enable (INTE):** This control bit is used by software to reset the host controller. When software sets this bit to 1b, the Host Controller resets its internal pipelines, timers, counters, state machines, and so forth, to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. PCI Configuration registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values.
1	0h RW	**Host Controller Reset (HCRST):** This control bit is used by software to reset the host controller. When software sets this bit to 1b, the Host Controller resets its internal pipelines, timers, counters, state machines, and so forth, to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. PCI Configuration registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values.
0	0h RW	**Run/Stop (RS):** When set to 1b, the xHC proceeds with execution of the schedule. The xHC continues execution as long as this bit is set to 1b. When this bit is cleared to 0b, the xHC completes the current and any actively pipelined transactions on the USB and then halts. The xHC shall halt within 16 microframes after software clears the Run/ Stop bit. The HCHalted (HCH) bit (MEM_BASE+84h:bit 0) indicates when the xHC has finished its pending pipelined transactions and has entered the stopped state. Software shall not write a '1' to this flag unless the xHC is in the Halted state (that is, HCH in the USBSTS register is '1'); doing so will yield undefined results.

24.2.10 USB Status (USBSTS)—Offset 84h

This register indicates pending interrupts and various states of the Host controller. The status resulting from a transaction on the serial bus is not indicated in this register. See the Interrupts description in section 4 of the xHCI specification for additional information concerning interrupt conditions.
Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 has no effect.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	0h RO	**Host Controller Error (HCE):** This flag shall be set to indicate that an internal error condition has been detected which requires software to reset and re-initialize the xHC. 0 = No internal xHC error conditions exist. 1 = Internal xHC error condition exists.
11	0h RO	**Controller Not Ready (CNR):** 0 = Ready 1 = Not Ready Software shall not write any Doorbell or Operational register of the xHC, other than the USBSTS register, until CNR = 0b. This flag is set by the xHC after a Hardware Reset and cleared when the xHC is ready to begin accepting register writes. This flag shall remain cleared (0b) until the next Chip Hardware Reset.
10	0h RW/1C	**Save/Restore Error (SRE):** If an error occurs during a Save or Restore operation this bit shall be set to 1b. This bit shall be cleared to 0b when a Save or Restore operation is initiated or when written with 1b.
9	0h RO	**Restore State Status (RSS):** When the Controller Restore State (CRS) flag in the USB_CMDregister is written with 1b this bit shall be set to 1b and remain set while the xHC restores its internalstate. Note: When the Restore State operation is complete, this bit shall be cleared to 0b.
8	0h RO	**Save State Status (SSS)**
7:5	0h RO	Reserved.
4	0h RW/1C	**Port Change Detect (PCD):** This bit is allowed to be maintained in the Auxiliary power well. Alternatively, it is also acceptable that on a D3 to D0 transition of the xHC, this bit is loaded with the OR of all of the PORTSC change bits (including: Force port resume, overcurrent change, enable/ disable change and connect status change). Regardless of the implementation, when this bit is readable (that is, in the D0 state), it must provide a valid view of the Port Status registers. 0 = No change bit transition from a 0 to 1 or No Force Port Resume bit transition from 0 to 1 as a result of a J-K transition detected on a suspended port. 1 = The Host controller sets this bit to 1 when any port for which the Port Owner bit is set to 0 has a change bit transition from a 0 to 1 or a Force Port Resume bit transition from 0 to 1 as a result of a J-K transition detected on a suspended port.
3	0h RW/1C	**Event Interrupt (EINT):** The xHC sets this bit to 1b when the Interrupt Pending (IP) bit of any Interrupter is transitions from 0b to 1b. Software that uses EINT shall clear it prior to clearing any IP flags. A race condition will occur if software clears the IP flags then clears the EINT flag, and between the operations another IP '0' to '1' transition occurs. In this case the new IP transition will be lost.
2	0h RW/1C	**Host System Error (HSE):** The xHC sets this bit to 1b when a serious error is detected, either internal to the xHC or during a host system access involving the xHC module. Conditions that set this bit to '1' include PCI Parity error, PCI Initiator Abort, and PCI Target Abort. When this error occurs, the xHC clears the Run/Stop (R/S) bit in the USB_CMD register to prevent further execution of the scheduled TDs. If the HSEE bit in the USB_CMD register is 1b, the xHC shall also assert out-ofband error signaling to the host.
1	0h RO	Reserved.
0	1h RO	**HCHalted (HCH):** This bit is a '0' whenever the Run/Stop (R/S) bit is set to 1b. The xHC sets this bit to 1b after it has stopped executing as a result of the Run/Stop (R/S) bit being cleared to 0b, either by software or by the xHC hardware (for example, internal error). If this bit is set to1b, then SOFs, microSOFs, or Isochronous Timestamp Packets (ITP) shall not be generated by the xHC.

24.2.11 Page Size (PAGESIZE)—Offset 88h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	1h RO	**Page Size (PAGESIZE):** Hardwired to 1h to indicate support for 4 Kbyte page sizes.

24.2.12 Device Notification Control (DNCTRL)—Offset 94h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**Notification Enable (N0_N15):** When a Notification Enable bit is set, a Device Notification Event will be generated when a Device Notification Transaction Packet is received with the matching value in the Notification Type field. For example, setting N1 to '1' enables Device Notification Event generation if a Device Notification TP is received with its Notification Type field set to '1' (FUNCTION_WAKE), and so on

24.2.13 Command Ring Low (CRCR_LO)—Offset 98h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h WO	**Command Ring Pointer (CRP):** This field defines low order bits of the initial value of the 64-bitCommand Ring Dequeue Pointer. Notes: 1. Writes to this field are ignored when Command Ring Running bit (CRR) = 1b. 2. If the CRCR register is written while the Command Ring is stopped (CRR = 0b), the value ofthis field shall be used to fetch the first Command TRB the next time the Host ControllerDoorbell register is written with the DB Reason field set to Host Controller Command. 3. If the CRCR register is not written while the Command Ring is stopped (CRR = 0b), then theCommand Ring shall begin fetching Command TRBs at the current value of the internal xHCCommand Ring Dequeue Pointer. 4. Reading this field always returns 0b.
5:4	0h RO	Reserved.
3	0h RO	**Command Ring Running (CRR):** This bit is set to 1b if the Run/Stop (R/S) bit is 1b and theHost Controller Doorbell register is written with the DB Reason field set to Host ControllerCommand. It is cleared to 0b when the Command Ring is stopped after writing a 1b to theCommand Stop (CS) or Command Abort (CA) bits, or if the R/S bit is cleared to 0b.
2	0h WO	**Command Abort (CA):** Writing a 1b to this bit shall immediately terminate the currentlyexecuting command, stop the Command Ring, and generate a Command Completion Event with theCompletion Code set to Command Ring Stopped. The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Commandshall restart the Command Ring operation. Notes: 1. Writes to this flag are ignored by the xHC if Command Ring Running (CRR) = 0b. 2. Reading this bit always returns 0b.
1	0h WO	**Command Stop (CS):** Writing a 1b to this bit shall stop the operation of the Command Ringafter the completion of the currently executing command, and generate a Command CompletionEvent with the Completion Code set to Command Ring Stopped and the Command TRB Pointer setto the current value of the Command Ring Dequeue Pointer. The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Commandshall restart the Command Ring operation. Notes: 1. Writes to this flag are ignored by the xHC if Command Ring Running (CRR) bit = 0b. 2. Reading this bit always returns 0b.
0	0h WO	**Ring Cycle State (RCS):** This bit identifies the value of the xHC Consumer Cycle State (CCS)flag for the TRB referenced by the Command Ring Pointer. Notes: 1. Writes to this bit are ignored when the Command Ring Running (CRR) bit = 1b. 2. If the CRCR register is written while the Command Ring is stopped (CCR = 0b), then the valueof this flag shall be used to fetch the first Command TRB the next time the Host ControllerDoorbell register is written with the DB Reason field set to Host Controller Command. 3. If the CRCR register is not written while the Command Ring is stopped (CCR = 0b), then theCommand Ring will begin fetching Command TRBs using the current value of the internalCommand Ring CCS flag. 4. Reading this flag always returns 0b.

24.2.14 Command Ring High (CRCR_HI)—Offset 9Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h WO	**Command Ring Pointer (CRP):** Command Ring Pointer—R/W. This field defines high order bits of the initial value of the 64-bitCommand Ring Dequeue Pointer. Notes: 1. Writes to this field are ignored when Command Ring Running bit (CRR) = 1b. 2. If the CRCR register is written while the Command Ring is stopped (CRR = 0b), the value ofthis field shall be used to fetch the first Command TRB the next time the Host ControllerDoorbell register is written with the DB Reason field set to Host Controller Command. 3. If the CRCR register is not written while the Command Ring is stopped (CRR = 0b), then theCommand Ring shall begin fetching Command TRBs at the current value of the internal xHCCommand Ring Dequeue Pointer. 4. Reading this field always returns 0b.

24.2.15 Device Context Base Address Array Pointer Low (DCBAAP_LO)—Offset B0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RW	**Device Context Base Address Array Pointer (DCBAAP):** This field defines low order bits of the 64-bitbase address of the Device Context Pointer Array table (a table of address pointers that referenceDevice Context structures for the devices attached to the host.
5:0	0h RO	Reserved.

24.2.16 Device Context Base Address Array Pointer High (DCBAAP_HI)—Offset B4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Device Context Base Address Array Pointer (DCBAAP):** This field defines high order bits of the 64-bitbase address of the Device Context Pointer Array table (a table of address pointers that referenceDevice Context structures for the devices attached to the host.)

24.2.17 Port N Status and Control USB2 (PORTSCN)—Offset 480h

Note that this USB2 Port Status and Control register is available at the following offsets for all applicable USB2 ports:

USB2 Port 1: 480h
USB2 Port 2: 490h
USB2 Port 3: 4A0h
.....
USB2 Port 9: 500h
USB2 Port 10: 510h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 2A0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S	**Warm Port Reset (WPR):** When software sets this bit to 1b, the Warm Reset sequence is enabled
30	0h RW/L	**Device Removable (DR):** This bit indicates if this port has a removable device. 0 = Device is removable. 1 = Device is non-removable.
29:28	0h RO	Reserved.
27	0h RW/P	**Wake on Over-current Enable (WOE):** 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to overcurrent conditions as system wake-up events.
26	0h RW/P	**Wake on Disconnect Enable (WDE):** 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to device disconnects as system wake-up events.
25	0h RW/P	**Wake on Connect Enable (WCE):** 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to device connects as system wake-up events.
24	0h RO	**Cold Attach Status (CAS):** This bit indicates that far-end terminations were detected in the Disconnected state and the Root Hub Port State Machine was unable to advance to the Enabled state. Software shall clear this bit by writing a 1b to the WPR bit or the xHC shall clear this bit if the CSS bit transitions to 1.
23	0h RW/1C	**Port Config Error Change (CEC)**
22	0h RW/1C	**Port Link State Change (PLC):** 0 = No change 1 = Link Status Change This flag is set to ‘1’ due to the following Port Link State (PLS) transitions:
21	0h RW/1C	**Port Reset Change (PRC):** This flag is set to ‘1’ due a '1' to '0' transition of Port Reset (PR), for example, when any reset processing on this port is complete. 0 = No change 1 = Reset Complete

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW/1C	**Over-current Change (OCC):** The functionality of this bit is not dependent upon the port owner. Software clears this bit by writing a 1 to it. 0 = No change. (Default) 1 = There is a change to Overcurrent Active.
19	0h RW/1C	**Warm Port Reset Change (WRC):** This bit is set when Warm Reset processing on this port completes. 0 = No change. (Default) 1 = Warm reset complete
18	0h RW/1C	**Port Enabled Disabled Change (PEC):** 0 = No change. (Default) 1 = There is a change to PED bit.
17	0h RW/1C	**Connect Status Change (CSC):** R/WC. This flag indicates a change has occurred in the port's Current Connect Status (CCS) or Cold Attach Status (CAS) bits. 0 = No change. (Default) 1 = There is a change to the CCS or CAS bit. The xHC sets this bit to 1b for all changes to the port device connect status, even if system software has not cleared an existing Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be "setting" an already-set bit (that is, the bit will remain 1b).
16	0h RW	**Port Link State Write Strobe (LWS):** 0 = When 0b, write data in PLS field is ignored. (Default) 1 = When this bit is set to 1b on a write reference to this register, this flag enables writes to the PLS field. Reads to this bit return '0'.
15:14	0h RW/P	**Port Indicator Control (PIC)**
13:10	0h RO	**Port Speed (PORTSPEED):** A device attached to this port operates at a speed defined by the following codes: Value Speed 0001b Full-speed 0010b Low speed 0011b Highspeed All other values reserved. Refer to the eXtensible Host Controller Interface for Universal Serial Bus Specification for additional details.
9	1h RW/P	**Port Power (PP):** Default value of 1. 0 = This port is in the powered-off state 1 = This port is in the powered-on state. This indicates that the port does have power.

Bit Range	Default & Access	Field Name (ID): Description
8:5	5h RW/P	**Port Link State (PLS):** This field is used to power manage the port and reflects its currentlink state.When the port is in the Enabled state, system software may set the link U-state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port. Write Value and Description 0: The link shall transition to a U0 state from any of the U-states. 2: USB 2.0 ports only. The link should transition to the U2 State. 3: The link shall transition to a U3 state from any of the U-states. This action selectively suspends the device connected to this port. While the Port LinkState = U3, the hub does not propagate downstream-directed traffic to this port, but the hub will respond to resume signaling from the port. 5: USB 3.0 ports only. If the port is in the Disabled state (PLS = Disabled, PP= 1), then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored. 15: USB 2.0 ports only. If the port is in the U3 state (PLS = U3), then the link shall remain in the U3 state and the port shall transition to the U3Exit substate, else ignored. All other values are ignored Read Value and Definition 0: Link is in the U0 State 1: Link is in the U1 State 2: Link is in the U2 State 3: Link is in the U3 State (Device Suspended) 4: Link is in the Disabled State 5:Link is in the RxDetect State 6:Link is in the Inactive State 7: Link is in the Polling State 8:Link is in the Recovery State 9: Link is in the Hot Reset State 10: Link is in the Compliance Mode State 11: Link is in the Test Mode State 12–14: Reserved 15: Link is in the Resume State
4	0h RW/1S	**Port Reset (PR):** When software writes a 1 to this bit (from a 0), the bus reset sequence as 1=port in reset 0=port not in reset
3	0h RW	**Over-current Active (OCA):** 0 = This port does not have an overcurrent condition. (Default) 1 = This port currently has an overcurrent condition. This bit will automatically transition from 1 to 0 when the overcurrent condition is removed. The PCH automatically disables the port when the overcurrent active bit is 1.
2	0h RO	Reserved.
1	0h RW/1C	**Port Enabled Disabled (PED):** Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a 1 to this bit. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. The bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. 0=disable 1=enable(default)
0	0h RW	**Current Connect Status (CCS):** This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. 0=no device is present 1=device is present on port.

24.2.18 Port Power Management Status Aand Control USB2 (PORTPMSCN)—Offset 484h

Note that this USB2 Port Power Management Status and Control register is available at the following offsets for all applicable USB2 ports:

USB2 Port 1: 484h
USB2 Port 2: 494h
USB2 Port 3: 4A4h
.....
USB2 Port 9: 504h
USB2 Port 10: 514h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW/P	**Port Test Control (PTC):** When this field is '0', the port is not operating in a test mode. (Default) A non-zero value indicates that the port is operating in test mode and the specific test mode is indicated by the specific value. A non-zero Port Test Control value is only valid to a port that is in the Disabled state. If the port is not in this state, the xHC shall respond with the Port Test Control field set to Port Test Control Error. The encoding of the Test Mode bits for a USB 2.0 port are: Value Test Mode 0h Test mode not enabled 1h Test J_STATE 2h Test K_STATE 3h Test SE0_NAK 4h Test Packet 5h Test FORCE_ENABLE 6h–14h Reserved. 15 Port Test Control Error
27:17	0h RO	Reserved.
16	0h RW	**Hardware LPM Enable (HLE):** 0=disable 1=Enable. When this bit is a 1, hardware controlled LPM shall be enabled for this port.
15:8	0h RO	Reserved.
7:4	0h RW/P	**Host Initiated Resume Duration (HIRD)**
3	0h RW/P	**Remote Wake Enable (RWE):** The host system sets this flag to enable or disable the device for remote wake from L1. 0=disable 1=enable The value of this flag will temporarily (while in L1) override the current setting of the Remote Wake feature set by the standard Set/ClearFeature() commands defined in Universal Serial Bus Specification, revision 2.0, Chapter 9.
2:0	0h RW	**L1 Status (L1S)**

24.2.19 Port N Hardware LPM Control Register (PORTHLPMCN)—Offset 48Ch

Note that this Port Hardware Control register is available at the following offsets for all applicable USB ports:

USB2 Port 1: 48Ch
USB2 Port 2: 49Ch
USB2 Port 3: 4ACh
.....
USB2 Port 9: 50Ch
USB2 Port 10: 51Ch

This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST).The definition for the fields depend on the protocol supported.
For USB3 this register is reserved and shall be treated by software as RsvdP.
For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us...Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value.
9:2	0h RW/P	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us....FFh: 65,280us
1:0	0h RW/P	**Host Initiated Resume Duration Mode (HIRDM)**

24.2.20 Port Status And Control USB3 (PORTSCXUSB3)—Offset 540h

The USB3 Port Status and Control registers are available at the following offsets forapplicable USB3 ports:
USB3 Port 1: 540h
USB3 port 2: 550h
USB3 port 3: 560h

USB3 port 4: 570h
USB3 port 5: 580h
USB3 port 6: 590h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 2A0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S	**Warm Port Reset (WPR):** When software sets this bit to 1b, the Warm Reset sequence is enabled
30	0h RW/L	**Device Removable (DR):** This bit indicates if this port has a removable device. 0 = Device is removable. 1 = Device is non-removable.
29:28	0h RO	Reserved.
27	0h RW/P	**Wake on Over-current Enable (WOE):** 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to overcurrent conditions as system wake-up events.
26	0h RW/P	**Wake on Disconnect Enable (WDE):** 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to device disconnects as system wake-up events.
25	0h RW/P	**Wake on Connect Enable (WCE):** 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to device connects as system wake-up events.
24	0h RO	**Cold Attach Status (CAS):** This bit indicates that far-end terminations were detected in the Disconnected state and the Root Hub Port State Machine was unable to advance to the Enabled state. Software shall clear this bit by writing a 1b to the WPR bit or the xHC shall clear this bit if the CSS bit transitions to 1.
23	0h RW/1C	**Port Config Error Change (CEC)**
22	0h RW/1C	**Port Link State Change (PLC):** 0 = No change 1 = Link Status Change This flag is set to '1' due to the following Port Link State (PLS) transitions:
21	0h RW/1C	**Port Reset Change (PRC):** This flag is set to '1' due a '1' to '0' transition of Port Reset (PR), for example, when any reset processing on this port is complete. 0 = No change 1 = Reset Complete
20	0h RW/1C	**Over-current Change (OCC):** The functionality of this bit is not dependent upon the port owner. Software clears this bit by writing a 1 to it. 0 = No change. (Default) 1 = There is a change to Overcurrent Active.
19	0h RW/1C	**Warm Port Reset Change (WRC):** This bit is set when Warm Reset processing on this port completes. 0 = No change. (Default) 1 = Warm reset complete
18	0h RW/1C	**Port Enabled Disabled Change (PEC):** 0 = No change. (Default) 1 = There is a change to PED bit.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW/1C	**Connect Status Change (CSC):** R/WC. This flag indicates a change has occurred in the port's Current Connect Status (CCS) or Cold Attach Status (CAS) bits. 0 = No change. (Default) 1 = There is a change to the CCS or CAS bit. The xHC sets this bit to 1b for all changes to the port device connect status, even if system software has not cleared an existing Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be "setting" an already-set bit (that is, the bit will remain 1b).
16	0h RW	**Port Link State Write Strobe (LWS):** 0 = When 0b, write data in PLS field is ignored. (Default) 1 = When this bit is set to 1b on a write reference to this register, this flag enables writes to the PLS field. Reads to this bit return '0'.
15:14	0h RW/P	**Port Indicator Control (PIC)**
13:10	0h RO	**Port Speed (PORTSPEED):** A device attached to this portoperates at a speed defined by the following codes: Value Speed 0100b SuperSpeed (5Gb/s) 0101b SuperSpeedPlus (10Gb/s) All other values reserved.
9	1h RW/P	**Port Power (PP):** Default value of 1. 0 = This port is in the powered-off state 1 = This port is in the powered-on state. This indicates that the port does have power.
8:5	5h RW/P	**Port Link State (PLS):** This field is used to power manage the port and reflects its current link state.When the port is in the Enabled state, system software may setthe link U-state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port. Write Value and Description: 0: The link shall transition to a U0 state from any of the U-states. 2: USB 2.0 ports only. The link should transition to the U2 State. 3: The link shall transition to a U3 state from any of the U-states.This action selectively suspends the device connected to this port.While the Port Link State = U3, the hub does not propagatedownstream-directed traffic to this port, but the hub will respondto resume signaling from the port. 5: USB 3.0 ports only. If the port is in the Disabled state (PLS =Disabled, PP = 1), then the link shall transition to a RxDetect stateand the port shall transition to the Disconnected state, elseignored. 15: USB 2.0 ports only. If the port is in the U3 state (PLS = U3),then the link shall remain in the U3 state and the port shalltransition to the U3Exit substate, else ignored.All other values IgnoredNote: The Port Link State Write Strobe (LWS) shall be set to 1b towrite this field. Read Value and Definition: 0: Link is in the U0 State 1: Link is in the U1 State 2: Link is in the U2 State 3: Link is in the U3 State (Device Suspended) 4: Link is in the Disabled State 5: Link is in the RxDetect State 6: Link is in the Inactive State 7: Link is in the Polling State 8: Link is in the Recovery State 9: Link is in the Hot Reset State 10: Link is in the Compliance Mode State 11: Link is in the Test Mode State 12–14: Reserved 15: Link is in the Resume State

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/1S	**Port Reset (PR):** When software writes a1 to this bit (from a 0), the bus reset sequence as defined in the USB Specification, Revision 2.0 is started. Software writes a 0 tothis bit to terminate the bus reset sequence. Software must keep this bit at a 1 long enough to ensure the reset sequence completes as specified in the USB Specification, Revision 2.0. USB 3.0 portsshall execute the Hot Reset sequence as defined in the USB 3.0 Specification. PR remains set until reset signaling is completed by the root hub. 1 = Port is in Reset. 0 = Port is not in Reset.
3	0h RW	**Over-current Active (OCA):** 0 = This port does not have an overcurrent condition. (Default) 1 = This port currently has an overcurrent condition. This bit will automatically transition from 1 to 0 when the overcurrent condition is removed. The PCH automatically disables the port when the overcurrent active bit is 1.
2	0h RO	Reserved.
1	0h RW/1C	**Port Enabled Disabled (PED):** Ports can only be enabled by the host controller as a part of thereset and enable. Software cannot enable a port by writing a 1 to this bit. Ports can be disabled byeither a fault condition (disconnect event or other fault condition)or by host software. The bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. 0 = Disable. 1 = Enable. (Default)
0	0h RW	**Current Connect Status (CCS):** This value reflects the currentstate of the port, and may not correspond directly to the eventthat caused the Connect Status Change bit (Bit 1) to be set. 0 = No device is present. (Default) 1 = Device is present on port.

24.2.21 Port Power Management Status And Control USB3 (PORTPMSCX)—Offset 544h

The USB3 Port Status and Control registers are available at the following offsets forapplicable USB3 ports:
USB3 Port 1: 544h
USB3 port 2: 554h
USB3 port 3: 564h
USB3 port 4: 574h
USB3 port 5: 584h
USB3 port 6: 594h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	Reserved.
16	0h RW	**Force Link PM Accept (FLA):** Force Link PM Accept (FLA):
15:8	0h RW/P	**U2 Timeout (U2T):** U2 Timeout (U2T):
7:0	0h RW/P	**U1 Timeout (U1T):** U1 Timeout (U1T):

24.2.22 USB3 Port X Link Info (PORTLIX)—Offset 548h

Note that this USB3 Port Link Info register is available at the following offsets for allapplicable USB3 ports:
USB3 Port 1: 548h
USB3 port 2: 558h
USB3 port 3: 568h
USB3 port 4: 578h
USB3 port 5: 588h
USB3 port 6: 598h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**Link Error Count (LEC):** Displays the Link Error Count for the USB 3 port.

24.2.23 Microframe Index (RTMFINDEX)—Offset 2000h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:0	0h RO	**Microframe Index (IMAN0)**

24.2.24 Interrupter x Management (IMANx)—Offset 2020h

Note that there are a total of 8 IMAN registers at the following offsets:
IMAN0: at offset 2020h
IMAN1: at offset 2040h
IMAN2: at offset 2060h
.....
IMAN6: at offset 20E0h
IMAN7; at offset 2100h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW	**Interrupt Enable (IE):** This flag specifies whether the Interrupter is capable of generating an interrupt.0 = The Interrupter is prohibited from generating interrupts.1 = When this bit and the IP bit are set (1b), the Interrupter shall generate an interrupt when the Interrupter Moderation Counter reaches '0'.
0	0h RW/1C	**Interrupt Pending (IP):** 0 = No interrupt is pending for the Interrupter.1 = An interrupt is pending for this Interrupter.This bit is set to 1b when IE = 1, the IMODI Interrupt Moderation Counter field = 0b, the Event Ring associated with the Interrupter is not empty (or for the Primary Interrupter when the HCE flag is set to 1b), and EHB = 0. If MSI interrupts are enabled, this flag shall be cleared automatically when the PCI DWord write generated by the Interrupt assertion is complete. If PCI Pin Interrupts are enabled, this flag shall be cleared by software.

24.2.25 Interrupter x Moderation (IMODx)—Offset 2024h

Note that there are a total of 8 IMOD registers at the following offsets:
IMOD0 : at offset 2024h
IMOD1: at offset 2044h
IMOD2: at offset 2064h
.....
IMOD6: at offset 20E4h
IMOD7; at offset 2104h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: FA0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Interrupt Moderation Counter (IMODC):** Down counter. Loaded with Interval Moderation value—value of bits 15:0, whenever the IP bit is cleared to 0b, counts down to '0', and stops. The associated interrupt shall be signaled whenever this counter is '0', the Event Ring is not empty, the IE and IP bits = 1, and EHB = 0.This counter may be directly written by software at any time to alter the interrupt rate
15:0	FA0h RW	**Interrupt Moderation Interval (IMODI):** Minimum inter-interrupt interval. The interval is specified in 250 ns increments. A value of '0' disables interrupt throttling logic and interrupts shall be generated immediately if IP = 0, EHB = 0, and the Event Ring is not empty.

24.2.26 Event Ring Segment Table Size x (ERSTSZx)—Offset 2028h

There are 8 ERSTSZ registers available at the following address offsets:
ERSTSZ0: at offset 2028h
ERSTSZ1: at offset 2048h
ERSTSZ2: at offset 2068h
ERSTSZ3: at offset 2088h
ERSTSZ4: at offset 20A8h
ERSTSZ5: at offset 20C8h
ERSTSZ6: at offset 20E8h
ERSTSZ7: at offset 2108h
Address Offset: 2028-202Bh, 2048-204Bh, ..., 2028+(MaxInts-1)*20h-202B+(MaxInts-1)*20h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**Event Ring Segment Table Size (ERSTS):** This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register.

24.2.27 Event Ring Segment Table Base Address Low x (ERSTBA_LOx)—Offset 2030h

There are 8 ERSTBA_LO registers available at the following address offsets:
ERSTBA_LO0: at offset 2030h
ERSTBA_LO1: at offset 2050h
ERSTBA_LO2: at offset 2070h

ERSTBA_LO3: at offset 2090h
ERSTBA_LO4: at offset 20B0h
ERSTBA_LO5: at offset 20D0h
ERSTBA_LO6: at offset 20F0h
ERSTBA_LO7: at offset 2110h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RW	**Event Ring Segment Table Base Address Register (ERSTBA):** This field defines the low order bits of the start address of the Event Ring Segment Table. This field shall not be modified if HCHalted (HCH) = 0.
5:0	0h RO	Reserved.

24.2.28 Event Ring Segment Table Base Address High x (ERSTBA_HIx)—Offset 2034h

There are 8 ERSTBA_HI registers available at the following address offsets:
ERSTBA_HI0: at offset 2034h
ERSTBA_HI1: at offset 2054h
ERSTBA_HI2: at offset 2074h
ERSTBA_HI3: at offset 2094h
ERSTBA_HI4: at offset 20B4h
ERSTBA_HI5: at offset 20D4h
ERSTBA_HI6: at offset 20F4h
ERSTBA_HI7: at offset 2114h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Event Ring Segment Table Base Address (ERSTBA):** This field defines the low order bits of the start address of the Event Ring Segment Table. This field shall not be modified if HCHalted (HCH) = 0.

24.2.29 Event Ring Dequeue Pointer Low x (ERDP_LOx)—Offset 2038h

There are 8 ERDP_LO registers available at the following address offsets:
ERDP_LO0: at offset 2038h
ERDP_LO1: at offset 2058h
ERDP_LO2: at offset 2078h
ERDP_LO3: at offset 2098h
ERDP_LO4: at offset 20B8h
ERDP_LO5: at offset 20D8h
ERDP_LO6: at offset 20F8h
ERDP_LO7: at offset 2118h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RW	**Event Ring Dequeue Pointer (ERDP):** This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that Event Ring Dequeue Pointer resides in.
3	0h RW/1C	**Event Handler Busy (EHB):** This flag shall be set to '1' when the IP bit is set to '1' and cleared to '0' by software when the Dequeue Pointer register is written.
2:0	0h RW	**Dequeue ERST Segment Index (DESI):** This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that Event Ring Dequeue Pointer resides in.

24.2.30 Event Ring Dequeue Pointer High x (ERDP_HIx)—Offset 203Ch

There are 8 ERDP_LO registers available at the following address offsets:
ERDP_HI0: at offset 203Ch
ERDP_HI1: at offset 205Ch
ERDP_HI2: at offset 207Ch
ERDP_HI3: at offset 209Ch
ERDP_HI4: at offset 20BCh
ERDP_HI5: at offset 20DCh
ERDP_HI6: at offset 20FCh
ERDP_HI7: at offset 211Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Event Ring Dequeue Pointer (ERDP):** This field defines the low order bits of the 64- bit address of the current Event Ring Dequeue Pointer.

24.2.31 Door Bell x (DBx)—Offset 3000h

Door Bell registers are an array of 32 registers.
The door bell registers are at the following offset:

Door Bell 0: 3000-3003h
Door Bell 1: 3004-3007h
.....
Door Bell 30: 3078-307Bh
Door Bell 31: 307C-307Fh

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	Reserved.
7:0	0h RW	**DB Target (DT):** This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Refer to the xHCI Specification for definitions of the values.

24.2.32 XECP SUPP USB2_0 (XECP_SUPP_USB2_0)—Offset 8000h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 2000802h

Bit Range	Default & Access	Field Name (ID): Description
31:24	2h RO	**USB Major Revision: 2.0 (USB2_MAJ_REV):** Major Specification Release Number in Binary-Coded Decimal (i.e., version 3.x is 03h). This field identifies the major release number component of the specification with which the xHC is compliant.
23:16	0h RO	**USB Minor Revision (USB_MIN_REV):** Minor Specification Release Number in Binary-Coded Decimal (i.e., version x.10 is 10h). This field identifies the minor release number component of the specification with which the xHC is compliant.
15:8	8h RO	**Next Capability Pointer (NCP):** This field indicates the location of the next capability with respect to the effective address of this capability.
7:0	2h RO	**Supported Protocol ID (SPID):** This field identifies the xHCI Extended capability. Refer to Table 146 for a list of the valid xHCI extended capabilities.

24.2.33 XECP SUPP USB2_1 (XECP_SUPP_USB2_1)—Offset 8004h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 20425355h

Bit Range	Default & Access	Field Name (ID): Description
31:0	20425355h RO	**XECP_SUPP_USB2_1 (XECP_SUPP_USB2_1):** This field is a mnemonic name string that references the specification with which the xHC is compliant. Four ASCII characters may be defined. Allowed characters are: alphanumeric, space, and underscore. Alpha characters are case sensitive.

24.2.34 XECP SUPP USB2_2 (XECP_SUPP_USB2_2)—Offset 8008h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 30180C01h

Bit Range	Default & Access	Field Name (ID): Description
31:28	3h RO	**Protocol Speed ID Count (PROT_SPD_ID_CNT)**
27:21	0h RO	Reserved.
20	1h RW/L	**BESL LPM Capability (BLC)**
19	1h RW/L	**Protocol Defined - Hardware LMP Capability (HLC)**
18	0h RO	**Protocol Defined - Integrated Hub Implementation (IHI)**

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**Protocol Defined - High SPeed Only (HSO):** This field indicates the number of Protocol Speed ID (PSI) Dwords that the xHCI Supported Protocol Capability data structure contains.If this field is non-zero, then all speeds supported by the protocol shall be defined using PSI Dwords, i.e. no implied Speed ID mappings apply.
16	0h RO	Reserved.
15:8	Ch RO	**Compatible Port Count (CPC):** This field identifies the number of consecutive Root Hub Ports (starting at the Compatible Port Offset) that support this protocol. Valid values are 1 to MaxPorts.
7:0	1h RO	**Compatible Port Offset (CPO):** This field specifies the starting Port Number of Root Hub Ports that support this protocol. Valid values are '1' to MaxPorts.

24.2.35 XECP SUPP USB3_3 (XECP_SUPP_USB2_3)—Offset 800Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4:0	0h RO	**XECP_SUPP_USB3_3 (PROTOCOL_SLOT_TYPE)**

24.2.36 XECP SUPP USB2_4 Full Speed (XECP_SUPP_USB2_4)—Offset 8010h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: C0021h

Bit Range	Default & Access	Field Name (ID): Description
31:16	Ch RO	**Protocol Speed ID Mantissa (PSIM):** This field defines the mantissa that shall be applied to the PSIE when calculating the maximum bit rate represented by this PSI Dword
15:14	0h RO	**Link Protocol (LP):** Link Protocol (LP): 0: SuperSpeed 1: SuperSpeedPlus 3-2: Reserved
13:9	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**PSI Full Duplex (PFD):** If this bit is '1' the link is full-duplex (dual-simplex), and if '0' the link is half-duplex (simplex).
7:6	0h RO	**PSI Type (PLT):** This field identifies whether the PSI Dword defines a symmetric or asymmetric bit rate, and if asymmetric, then this field also indicates if this Dword defines the receive or transmit bit rate. Note that the Asymmetric PSI Dwords shall be paired, i.e. an Rx immediately followed by a Tx, and both Dwords shall define the same value for the PSIV.PLT Value Bit Rate Note 0 Symmetric Single PSI Dword 1 Reserved 2 Asymmetric Rx Paired with Asymmetric Tx PSI Dword 3 Asymmetric Tx Immediately follows Rx Asymmetric PSI Dword
5:4	2h RO	**Protocol Speed ID Exponent (PSIE):** This field defines the base 10 exponent times 3, that shall be applied to the Protocol Speed ID Mantissa when calculating the maximum bit rate represented by this PSI Dword.PSIE Value Bit Rate 0 Bits per second 1 Kb/s 2 Mb/s 3 Gb/s
3:0	1h RO	**Protocol Speed ID Value (PSIV):** If a device is attached that operates at the bit rate defined by this PSI Dword, then the value of this field shall be reported in the Port Speed field of PORTSC register (5.4.8) of a compatible port. Note, the PSIV value of '0' is reserved and shall not be defined by a PSI.

24.2.37 XECP_SUPP USB2_5 Low Speed (XECP_SUPP_USB2_5)—Offset 8014h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 5DC0012h

Bit Range	Default & Access	Field Name (ID): Description
31:16	5DCh RO	**Protocol Speed ID Mantissa (PSIM)**
15:14	0h RO	**Link Protocol (LP):** Link Protocol (LP): 0: SuperSpeed 1: SuperSpeedPlus 3-2: Reserved
13:9	0h RO	Reserved.
8	0h RO	**PSI Full Duplex (PFD)**
7:6	0h RO	**PSI Type (PLT)**
5:4	1h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	2h RO	**Protocol Speed ID Value (PSIV)**

24.2.38 XECP SUPP USB2_6 High Speed (XECP_SUPP_USB2_6)—Offset 8018h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1E00023h

Bit Range	Default & Access	Field Name (ID): Description
31:16	1E0h RO	**Protocol Speed ID Mantissa (PSIM)**
15:14	0h RO	**Link Protocol (LP):** Link Protocol (LP): 0: SuperSpeed 1: SuperSpeedPlus 3-2: Reserved
13:9	0h RO	Reserved.
8	0h RO	**PSI Full Duplex (PFD)**
7:6	0h RO	**PSI Type (PLT)**
5:4	2h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	3h RO	**Protocol Speed ID Value (PSIV)**

24.2.39 XECP SUPP USB3_0 (XECP_SUPP_USB3_0)—Offset 8020h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 3101402h

Bit Range	Default & Access	Field Name (ID): Description
31:24	3h RO	**USB Major Revision: 3.0 (USB3_MAJ_REV)**
23:16	10h RO	**USB Minor Revision (USB3_MIN_REV)**
15:8	14h RO	**Next Capability Pointer (NCP)**
7:0	2h RO	**Supported Protocol ID (SPID)**

24.2.40 XECP SUPP USB3_1 (XECP_SUPP_USB3_1)—Offset 8024h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 20425355h

Bit Range	Default & Access	Field Name (ID): Description
31:0	20425355h RO	**XECP_SUPP_USB3_1 (XECP_SUPP_USB3_1)**

24.2.41 XECP SUPP USB3_2 (XECP_SUPP_USB3_2)—Offset 8028h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 8000040Dh

Bit Range	Default & Access	Field Name (ID): Description
31:28	8h RO	**Protocol Speed ID Count (PROT_SPD_ID_CNT)**
27:16	0h RO	Reserved.
15:8	4h RO	**Compatible Port Count (CPC)**
7:0	Dh RO	**Compatible Port Offset (CPO)**

24.2.42 XECP SUPP USB3_3 (XECP_SUPP_USB3_3)—Offset 802Ch

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4:0	0h RO	**XECP_SUPP_USB3_3 (PROTOCOL_SLOT_TYPE)**

24.2.43 XECP SUPP USB3_4 (XECP_SUPP_USB3_4 (USB 3.2 Gen 1x1))—Offset 8030h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 50134h

Bit Range	Default & Access	Field Name (ID): Description
31:4	5013h RO	Reserved.
3:0	4h RO	**Protocol Speed ID Value (PSIV)**

24.2.44 XECP SUPP USB3_5 (XECP_SUPP_USB3_5 (USB 3.2 Gen 2x1))—Offset 8034h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: A4135h

Bit Range	Default & Access	Field Name (ID): Description
31:16	Ah RO	**Protocol Speed ID Mantissa (PSIM)**
15:14	1h	**link Protocol (LP):** Link Protocol (LP): 0: SuperSpeed 1: SuperSpeedPlus 3-2: Reserved
13:9	0h RO	Reserved.
8	1h RO	**PSI Full Duplex (PFD)**

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**PSI Type (PLT)**
5:4	3h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	5h RO	**Protocol Speed ID Value (PSIV)**

24.2.45 XECP SUPP USB3_6 (XECP_SUPP_USB3_6)—Offset 8038h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 4E00126h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4E0h RO	**Protocol Speed ID Mantissa (PSIM)**
15:14	0h RO	**Link Protocol (LP):** Link Protocol (LP): 0: SuperSpeed 1: SuperSpeedPlus 3-2: Reserved
13:9	0h RO	Reserved.
8	1h RO	**PSI Full Duplex (PFD)**
7:6	0h RO	**PSI Type (PLT)**
5:4	2h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	6h RO	**Protocol Speed ID Value (PSIV)**

24.2.46 XECP SUPP USB3_7 (XECP_SUPP_USB3_7)—Offset 803Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 9C00127h

Bit Range	Default & Access	Field Name (ID): Description
31:16	9C0h RO	**Protocol Speed ID Mantissa (PSIM)**
15:14	0h RO	**Link Protocol (LP):** Link Protocol (LP): 0: SuperSpeed 1: SuperSpeedPlus 3-2: Reserved
13:9	0h RO	Reserved.
8	1h RO	**PSI Full Duplex (PFD)**
7:6	0h RO	**PSI Type (PLT)**
5:4	2h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	7h RO	**Protocol Speed ID Value (PSIV)**

24.2.47 XECP SUPP USB3_8 (XECP_SUPP_USB3_8)—Offset 8040h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 13800128h

Bit Range	Default & Access	Field Name (ID): Description
31:16	1380h RO	**Protocol Speed ID Mantissa (PSIM)**
15:14	0h RO	**Link Protocol (LP):** Link Protocol (LP): 0: SuperSpeed 1: SuperSpeedPlus 3-2: Reserved
13:9	0h RO	Reserved.
8	1h RO	**PSI Full Duplex (PFD)**
7:6	0h RO	**PSI Type (PLT)**
5:4	2h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	8h RO	**Protocol Speed ID Value (PSIV)**

24.2.48 XECP SUPP USB3_9 (XECP_SUPP_USB3_9)—Offset 8044h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 5B10129h

Bit Range	Default & Access	Field Name (ID): Description
31:16	5B1h RO	**Protocol Speed ID Mantissa (PSIM)**
15:9	0h RO	Reserved.
8	1h RO	**PSI Full Duplex (PFD)**
7:6	0h RO	**PSI Type (PLT)**
5:4	2h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	9h RO	**Protocol Speed ID Value (PSIV)**

24.2.49 Host Control Scheduler (HOST_CTRL_SCH_REG)—Offset 8094h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 140h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12:11	0h RW	**Cache Size Control Reg (CACHE_SZ_CTRL):** 0: 64 1: 32 2,3: 16
10:9	0h RO	Reserved.
8	1h RW	**Turn on scratch_pad_en (TO_SCRATCH_PAD_EN)**
7	0h RW	**Scheduler Host Control Reg (STOP_SCH_UNCON)**
6	1h RW	**disable 1 pack scheduling limit when ISO pending in present microframe (DIS_SCH_LIMIT)**
5:4	0h RW	**scheduler sort pattern (SCH_SORT_PATTERN)**
3	0h RW	**enable TTE overlap prevention on interrupt OUT EPs (at cost of possible service interval slip (EN_TTE_OVERLAP_PREV_OUT)**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**enable TTE overlap prevention on interrupt IN EPs (at cost of possible service interval slip (EN_TTE_OVERLAP_PREV_IN)**
1	0h RW	**Disable TRM active IN EP valid check function (DIS_TRM_ACT_IN_VALID)**
0	0h RW	**Disable poll delay function (DIS_POLL_DELAY)**

24.2.50 Power Management Control (PMCTRL_REG)—Offset 80A4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 492D5094h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Async PME Source Enable (ASYNC_PME_SRC_EN)**
30	1h RW	**Legacy PME Source Enable (LEGACY_PME_SRC_EN)**
29	0h RW	**Reset Warn Power Gate Trigger Disable (RESET_WARN_PWR_GATE_TRIGGER_DISABLE):** This field controls the actions taken for due to reset warn. 0 - Reset Warn will trigger a HW autonomous Power Gate 1 - Reset Warn will not trigger a HW autonomous Power Gate
28	0h RW	**CLR_PME_FLAG_PULSE_AUX_CCLK (CLR_PME_FLAG_PULSE_AUX_CCLK):** Internal PME flag Clear This Write-Only bit can be used to clear the internal PME flag. SW write to '1' will clear the PME flag. SW write to '0' will have no effect and be ignored by the controller.
27	1h RW	**Disable RTD3 power gating when in D3 (DIS_D3_PG)**
26	0h RW	**XLFPSCOUNTSRC (XLFPSCOUNTSRC):** XLFPSCOUNTSRC (Source for LFPS OFF Counter) 0: Central RTC Counter for LFPS detection 1: Local Counter for LFPS detection
25	0h RW	**XELFPSRTC (XELFPSRTC)**
24	1h RW	**XMPHYSPGDD0I2 (XMPHYSPGDD0I2)**
23	0h RW	**XMPHYSPGDD0I3 (XMPHYSPGDD0I3)**
22	0h RW	**XMPHYSPGDRTD3 (XMPHYSPGDRTD3)**
21:18	Bh RW	**XD3RTCPTTM (XD3RTCPTTM):** XD3RTCPTTM (D3 RTC Port Timer Tick Multiplier) This register will be the multiplication factor for determining Wake Detection Frequency and RXDET based on the XD3RTCPTTC value. If XD3RTCPTTC is 9h and this register is Bh, frequency for RXDET H8EXIT detection while MODPHY SUS Power gating is enabled would be 99ms.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**U3 LFPS Periodic Sampling ON Time Control (U3_LFPS_PRDC_SAMPLING_ON_TIME_CTRL):** This field controls the ON time for the LFPS periodic sampling for USB3 ports. 0 ON time is 2 rtc clocks 1 ON time is 3 rtc clocks Note: This field is ignored if USB3 PHY SUS Well Power Gating is enabled.
16	1h RW	**AON LFPS Detector Enable Mode (AON_LFPS_DETECTOR_EN_MODE)**
15:8	50h RW	**SS U3 LFPS Detection Threshold (SS_U3_LFPS_DETECTION_THRESHOLD)**
7:4	9h RW	**SS_U3_LFPS_PRDC_SAMPLING_OFFTIME_CTRL (SS_U3_LFPS_PRDC_SAMPLING_OFFTIME_CTRL)**
3	0h RW	**PS3 LFPS Source Select (PS3_LFPS_SRC_SEL)**
2	1h RW	**XHCI Engine Autonomous Power Gate Exit Reset Policy (XHC_AUTO_PWRGATE_EXITRST_POLICY)**
1	0h RW	**USB2 Port Wake Unit Coupling Policy (USB2_PORT_WAKE_COUPLING_POLICY)**
0	0h RW	**USB3 Port Wake Unit Coupling Policy (USB3_PORT_WAKE_COUPLING_POLICY)**

24.2.51 Host Controller Misc Reg (HOST_CTRL_MISC_REG)—Offset 80B0h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 37Fh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**USB2_LTRUPDT_DIS (USB2_LTRUPDT_DIS):** This controls the inclusion of the USB2 LTR based on link state. Setting this bit will disable USB2 LTR and will expose a NO Requirement from USB2 thus not impacting the aggregated LTR vaule for the controller.
30	0h RW	**USB2 Line State Debounce During Port Reset Policy (USB2_LINE_STATE_DEBOUNCE_DURING_PORT_RESET_POLICY)**
29	0h RW	**TTE PEXE Credit Fix Disable (TTE_PEXE_CREDIT_FIX_DISABLE)**
28	0h RW	**TTE Scheduling policy (TTE_SCHEDULING_POLICY)**
27	0h RW	**USB3 ITP Delta Timer Source Select (USB3_ITP_DELTA_TIMER_SOURCE_SELECT)**
26	0h RW	**Frame Timer Source Select (FRAME_TIMER_SOURCE_SELECT)**
25	0h RW	**uFrame Masking Enable (UFRAME_MASKING_ENABLE)**
24	0h RW	**Late FID Check Disable (LATE_FID_CHECK_DISABLE)**

Bit Range	Default & Access	Field Name (ID): Description
23:20	0h RO	Reserved.
19	0h RW	**USB2 Resume Cx Inhibit Disable (USB2_RESUME_CX_INHIBIT_DISABLE)**
18	0h RW	**LATE_FID_TTE_DIS**
17	0h RW	**Late FID uframe Check Disable (LATE_FID_UFRAME_CHK_DIS)**
16	0h RW	**Late FID Extra Interval (LATE_FID_EXTRA_INTER)**
15:0	37Fh RW	**Valid Isoch Scheduling Range (VALID_ISOCH_SCHEDULING_RANGE)**

24.2.52 Host Controller Misc Reg2 (HOST_CTRL_MISC_REG2)—Offset 80B4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	Reserved.
25	0h RW	**ltm_belt_valid_clr (LTM_BELT_VALID_CLR)**
24	0h RW	**cfg_trm_drop_sch_req_dis (CFG_TRM_DROP_SCH_REQ_DIS)**
23	0h RW	**cfg_trm_drop_tte_req_dis (CFG_TRM_DROP_TTE_REQ_DIS)**
22	0h RW	**cfg_trm_edtla_clr_dis (CFG_TRM_EDTLA_CLR_DIS)**
21	0h RW	**cfg_xfer_is_serve_chk_en (CFG_XFER_IS_SERVE_CHK_EN)**
20	0h RW	**cfg_cpl_npkt0_fc_dis (CFG_CPL_NPKT0_FC_DIS)**
19:18	0h RO	Reserved.
17	0h RW	**Disable IDT credit leak fix (CFG_DIS_ODMA_IDT_CRD_LEAK_FIX)**
16	0h RW	**cfg_idma_ttype_chk_dis (CFG_IDMA_TTYPE_CHK_DIS)**

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**HC Reset Controller Isolation Disable (HCRST_CTRL_ISOL_DISABLE)**
14	0h RW	**cfg_dis_idma_perf_fix (DISABLE_IDMA_PERF_FIX)**
13:0	0h RO	Reserved.

24.2.53 Super Speed Port Enable (SSPE_REG)—Offset 80B8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RW	**SSPE_REG (SSPE_REG)**

24.2.54 AUX Power Management Control (AUX_CTRL_REG1)—Offset 80E0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 8080BCE0h

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**D3 Hot function enable register (D3_HOT_FXN_EN)**
30	0h RW	**Allow L1 Core Clock Gating (ALL_L1_CORE_CG)**
29	0h RW	**Allow Engine PHY Status Extension (AL_EP_SEXT)**
28	0h RW	**Allow Engine PCIe Rate Change Passing (ALL_EP_RCP)**
27	0h RW	**Allow Engine PERST Fundamental Reset (AL_PERST_FRST)**

Bit Range	Default & Access	Field Name (ID): Description
26	0h RW	**Overwrite PCIe P2 to P1 (OVR_PCIE_P2_P1)**
25	0h RW	**Set Internal SSV 1 (SET_ISSV_1)**
24	0h RW	**Clear Internal SSV 0 (CLR_ISSV_0)**
23	1h RW	**Enable save_restore_enable SW Loading (EN_SRE_SW_LD)**
22	0h RO	Reserved.
21	0h RW	**Force save_restore 1 (FORCE_SR1)**
20	0h RO	Reserved.
19	0h RW	**cfg iob drivestrength[1] (CIDS1)**
18	0h RW	**cfg iob drivestrength[0] (CIDS0)**
17	0h RW	**cfg_dis_arc_RXDP3 (CFG_DIS_ARC_RXDP3)**
16	0h RW	**cfg clk gate dis (CCGD)**
15	1h RW	**Enable CFG RXDET P3 (EN_CFG_RDP3)**
14	0h RW	**Enable CFG PIPE Reset (EN_CFG_PIPE_RST)**
13	1h RW	**Enable Filter TX Idle (EN_FILT_TX_IDLE)**
12	1h RW	**Enable Host Engine Generate PME (EN_HE_GEN_PME)**
11	1h RW	**Enable Isolation (EN_ISOL)**
10	1h RW	**Enable L1 Caused P2 Overwrite (EN_L1_P2_OVR)**
9	0h RW	**Enable Core Clock Gating (EN_CORE_CG)**
8	0h RW	**Enable PHY Status Timeout (EN_PHY_STS_TO)**
7	1h RW	**Ignore aux_pm_en PCIe Core (IGN_APE_PC)**
6	1h RW	**Enable P2 Overwrite P1 (EN_P2_OVR_P1)**
5	1h RW	**Enable P2 Remote Wake (EN_P2_REM_WAKE)**
4:1	0h RW	**Forced PM State (FORCED_PM_STATE)**
0	0h RW	**Initiate Force PM State (INIT_FPMS)**

24.2.55 SuperSpeed Port Link Control (HOST_CTRL_PORT_LINK_REG)—Offset 80ECh

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 18000C00h

Bit Range	Default & Access	Field Name (ID): Description
31:27	3h RW	**Force LTSSM State (FORCE_LTSSM_ST)**
26	0h RW	**Direct Link LTSSM State (DL_LTSSM_ST)**
25	0h RW	**Direct Link To U0 (DL_U0)**
24:21	0h RW	**Forced Compliance Pattern (FORCED_CMP_PAT)**
20:17	0h RO	Reserved.
16:15	0h RW	**PHY Low Power Latency (PHY_LP_LAT)**
14:12	0h RW	**Link Recovery Minimum Time (LR_MIN_TM)**
11:9	6h RW	**Link Polling Minimum Time (LP_MIN_TM)**
8	0h RW	**Force Link Accept PM Command (FORCE_LA_PMC)**
7	0h RW	**Direct Link Recovery U0 (DL_REC_U0)**
6	0h RW	**Link Fast Training Mode (LINK_FTM)**
5	0h RW	**Disable Link Scrambler (DIS_LINK_SCRAM)**
4	0h RW	**Direct Link U3 From U0 (DL_U3_U0)**
3	0h RW	**Direct Link U3 From U0 (DL_U2_U0)**
2	0h RW	**Direct Link U3 From U0 (DL_U1_U0)**
1	0h RW	**Enable Link Loopback Initiator Mode (EN_LINK_LB_MAST)**
0	0h RW	**Disable Link Compliance Mode (DIS_LINK_CM):** 0: Enable link compliance mode 1: Disable link compliance mode

24.2.56 USB2 Port Link Control 1 (USB2_LINK_MGR_CTRL_REG1)—Offset 80F0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 314803A0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	31h RW	**FS/LS Mode SE0 Disconnect Delay[7:0] (FSLS_SE0_DIS_DEL_7_0)**
23	0h RW	**EN_SNPS_PHY_FIX (EN_SNPS_PHY_FIX)**
22	1h RW	**EN_L1_DISC_IN_L0 (EN_L1_DISC_IN_L0)**
21	0h RW	**DIS_PURGE_ON_SETUP_FIX (DIS_PURGE_ON_SETUP_FIX)**
20	0h RW	**L1_EXIT_RECOVERY_MODE (L1_EXIT_RECOVERY_MODE)**
19	1h RW	**L1_TO_INCR_MODE (L1_TO_INCR_MODE)**
18	0h RO	Reserved.
17	0h RW	**EN_DETECT_NOMINAL_PKT_EOP (EN_DETECT_NOMINAL_PKT_EOP)**
16	0h RW	**Disable Chirp Response (DIS_CHIRP_RESPONSE)**
15	0h RW	**Disable 192 Byte Limit Check (DIS_192B_LIM)**
14	0h RW	**External Provided FS/LS Disconnect (EXT_FSLS_DIS)**
13:12	0h RW	**UTMI Reset Source Select (UTMI_RST_SEL)**
11	0h RW	**Disable HS Disconnect Window (DIS_HS_DIS_WIN)**
10	0h RW	**Disable Port Error Detection (DIS_PERR_DET)**
9	1h RW	**Disable Peek Function for ISO-OUT (DIS_PF_IOUT)**
8	1h RW	**Drive Resume-K FS/LS Serial Interface (DRV_RESK_FSLS_SER)**
7	1h RW	**Enable USB2 Drop-Ping (EN_U2_DROP_PING)**
6	0h RW	**Enable USB2 Force-Ping (EN_U2_FORCE_PING)**

Bit Range	Default & Access	Field Name (ID): Description
5	1h RW	**Enable USB2 Auto-Ping (EN_U2_AUTO_PING)**
4	0h RW	**Disable PHY SuspendM (DIS_PHY_SUSM)**
3	0h RW	**UTMI Internal Clock Gate Disable (UTMI_INT_CG_DIS)**
2	0h RW	**Disable PHY SuspendM in Disconnect State (DIS_PSUSM_DS)**
1	0h RW	**Force PHY Reset (FORCE_PHY_RST)**
0	0h RW	**USB2 Accelerated Simulation Timing (U2_ACC_SIM_TIM)**

24.2.57 USB2 Port Link Control 4 (USB2_LINK_MGR_CTRL_REG4)—Offset 80FCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 8003h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21:9	40h RW	**U2 Detect Remote Wake Delay (U2D_RWAKE_DEL)**
8:0	3h RW	**U2 Entry Ignore Linestate Changes Duration[12:4] (U2_IGN_LS_DUR_12_4)**

24.2.58 Power Scheduler Control-0 (PWR_SCHED_CTRL0)—Offset 8140h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: FF01903Ch

Bit Range	Default & Access	Field Name (ID): Description
31:24	FFh RW	**Engine Idle Hysteresis (EIH)**
23:12	19h RW	**Backbone PLL Shutdown Advance Wake (BPSAW)**
11:0	03Ch RW	**Backbone PLL Shutdown Min. Idle Duration (BPSMID)**

24.2.59 Power Scheduler Control-1 (PWR_SCHED_CTRL2)—Offset 8144h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 23Fh

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9	1h RW	**HS Interrupt-OUT Alarm (HS_INT_OUT_ALRM)**
8	0h RW	**HS Interrupt-IN Alarm (HS_INT_IN_ALRM):** HS Interrupt IN Alarm (HSII):Note: This is required to be set to enable the functionality behind the PCICFG.HSCFG2.HSIIPAPC method of tracking HS Intr IN EPs for Periodic Active.
7	0h RW	**SS Interrupt-OUT FC Alarm (SS_INT_OUT_FC_ALRM)**
6	0h RW	**SS Interrupt-IN Alarm (SS_INT_IN_FC_ALRM)**
5	1h RW	**SS Interrupt-OUT & not in FC Alarm (SS_INT_OUT_ALRM)**
4	1h RW	**SS Interrupt-IN & not in FC Alarm (SS_INT_IN_ALRM)**
3	1h RW	**HS ISO-OUT Alarm (HS_ISO_OUT_ALRM)**
2	1h RW	**HS ISO-IN Alarm (HS_ISO_IN_ALRM)**
1	1h RW	**SS ISO-OUT Alarm (SS_ISO_OUT_ALRM)**
0	1h RW	**SS ISO-IN Alarm (SS_ISO_IN_ALRM)**

24.2.60 AUX Power Management Control (AUX_CTRL_REG2)—Offset 8154h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1192206h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30	0h RW	**CFG_FAST_TRAINING (CFG_FAST_TRAINING)**
29	0h RW	**snps_phystatus_done_l1_dis (SNPS_PHYSTATUS_DONE_L1_DIS)**
28	0h RO	Reserved.
27	0h RW	**batt_charge_d3_en (BATT_CHARGE_D3_EN)**
26	0h RW	**cfg_debounce_en (CFG_DEBOUNCE_EN)**
25	0h RO	Reserved.
24	1h RW	**Enable L1 exit notification to SNPS PCIe core (EN_L1_EXIT_NOTIF_PCIE)**
23	0h RW	**DISABLE PLC ON DISCONNECT (DIS_PLC_ON_DISCONNECT)**
22	0h RW	**TREAT_IDLE_AS_TS2_IN_LTSSM_WAIT_4_TS2 (TREAT_IDLE_AS_TS2_IN_LTSSM_WAIT_4_TS2)**
21	0h RW	**Disable p2 overwrite due to the D3HOT where PCIe core enters the L1 (DIS_P2_OVERWRITE_DUE2_D3HOT)**
20	1h RW	**Enable the port to enter U3 automatically when in U1/U2 (ENABLE_AUTO_U3_ENTRY_FROM_U2_U3)**
19	1h RW	**No linkdown reset is issue during low power state (DIS_LINKDOWN_RST_DURING_LOW_POWER)**
18	0h RW	**EN_EXIT_DEEP_SLEEP_IF_PCIE_IN_P0 (EN_EXIT_DEEP_SLEEP_IF_PCIE_IN_P0)**
17	0h RW	**U2_EXIT_LFPS_TIMER_VALUE (U2_EXIT_LFPS_TIMER_VALUE)**
16	1h RW	**EN_EXIT_DEEP_SLEEP_ON_USB_PORT_WAKEUP (EN_EXIT_DEEP_SLEEP_ON_USB_PORT_WAKEUP)**
15:14	0h RW	**P3_ENTRY_TIMEOUT (P3_ENTRY_TIMEOUT)**
13	1h RW	**Enable U2 P3 Mode (EN_U2_P3)**
12:11	0h RW	**Fine Debug Mode Select (FINE_DM_SEL)**
10	0h RW	**Enable Low Power State Based Core Clock Gating (EN_LP_CORE_CG)**
9	1h RW	**Disable USB3 Port Status Changed Event (DIS_U3_PORT_SCE)**

Bit Range	Default & Access	Field Name (ID): Description
8:4	0h RW	**Debug Mode Select Register (DEB_MODE_SEL)**
3	0h RW	**Enable Auto Wakeup Non-IDLE (EN_AWAK_NIDLE)**
2	1h RW	**Enable PM Control P1 Exit P2 (EN_PMC_P1_EXIT_P2)**
1	1h RW	**Enable PCIe PIPE CLK Isolation (EN_PP_CLK_ISOL)**
0	0h RW	**Enable P2 Overwrite P1 Allowed Detect (EN_P2OVRP1_ADET)**

24.2.61 USB2 PHY Power Management Control (USB2_PHY_PMC)—Offset 8164h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: FCh

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	1h RW	**EN_CMDM_TXRXB (EN_CMDM_TXRXB)**
6	1h RW	**EN_TTE_TXRXB (EN_TTE_TXRXB)**
5	1h RW	**EN_IDMA_TXRXB (EN_IDMA_TXRXB)**
4	1h RW	**EN_ODMA_TXRXB (EN_ODMA_TXRXB)**
3	1h RW	**EN_TRM_TXRXB (EN_TRM_TXRXB)**
2	1h RW	**EN_SCH_TXRXB (EN_SCH_TXRXB)**
1	0h RW	**Enable Rx Bias ckt disable (EN_RXB_CD)**
0	0h RW	**Enable Tx Bias ckt disable (EN_TXB_CD)**

24.2.62 XHCI Aux Clock Control Register (XHCI_AUX_CCR)—Offset 816Ch

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: F403Ch

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19	1h RW	**USB3 Partition Engine/Link trunk gating Enable (PARUSB3_ENG_GEN)**
18	1h RW	**USB3 Partition Frame Timer trunk gating Enable (PARUSB3_LINK_GEN)**
17	1h RW	**USB2 link partition clock gating enable (PARUSB2_CLK_GEN)**
16	1h RW	**USB2/USHIP 12.5 MHz partition clock gating enable (USHIP_PCGEN)**
15	0h RO	Reserved.
14	1h RW	**USB3 Port Aux/Core clock gating enable (USB3_AC_CGE):** When set, allows the aux_cclk clock into the USB3 port to be gated when conditions are met.
13:12	0h RW	**Rx Detect Timer when port Aux Clock is Gated (RX_DT_ACG)**
11:8	0h RO	Reserved.
7	0h RW	**Frame Timer Clock Gating Ports in U2 Enable (FTCGPU2E)**
6	0h RW	**USB2 port clock throttle enable (USB2_PC_TE)**
5	1h RW	**XHCI Engine Aux clock gating enable (XHCI_AC_GE)**
4	1h RW	**XHCI Aux PM block clock gating enable (XHCI_APMB_CGE):** When set, allows the aux clock into the Aux PM block to be gated when idle.
3	1h RW	**USB3 Aux Clock Trunk Gating Enable (USB3_AC_TGE):** When set, allows Aux Clock Trunk feeding to USB3.0 ports to be gated when port Aux clock is gated at all USB3.0 ports and all USB3.0 modPHY instances.
2	1h RO	Reserved.
1	0h RW	**ModPHY port Aux clock gating enable in U2 (MPP_AC_GEU2):** When set, allows the aux clock into the ModPhy to be gated when Link is in U2 and pipe has been in PS3 for at least the time defined by U2 Residency Before ModPHY Clock Gating field.
0	0h RW	**ModPHY port Aux clock gating enable in Disconnected, U3 or Disabled (MPP_AC_GE_DDU3):** When set, allows the aux clock into the ModPHY to be gated when Link is in Disconnected, U3 or Disabled state.

24.2.63 XHC Latency Tolerance Parameters LTV Control (XLTP_LTV1)—Offset 8174h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1400C01h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Disable scheduler direct transition from IDLE to NO requirement (DIS_SDT_IDL_NR)**
30:26	0h RO	Reserved.
25	0h	**USB2 async active policy (EN_USB2_LTV_U0_PORT_ASYNC_ACTIVE)**
24	1h RW	**XHCI LTR Enable (XLTRE)**
23:12	400h RW	**Periodic Active LTV (PA_LTV)**
11:0	C01h RW	**USB2 Port L0 LTV (USB2_PL0_LTV)**

24.2.64 XHC Latency Tolerance Parameters High Idle Time Control (XLTP_HITC)—Offset 817Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 50002h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:16	5h RW	**Minimum High Idle Time (MHIT)**
15:13	0h RO	Reserved.
12:0	2h RW	**High Idle Wake Latency (HIWL)**

24.2.65 XHC Latency Tolerance Parameters Medium Idle Time Control (XLTP_MITC)—Offset 8180h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 50002h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:16	5h RW	**Minimum Medium Idle Time (MMIT)**
15:13	0h RO	Reserved.
12:0	2h RW	**Medium Idle Wake Latency (MIWL)**

24.2.66 XHC Latency Tolerance Parameters Low Idle Time Control (XLTP_LITC)—Offset 8184h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 50002h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:16	5h RW	**Minimum Low Idle Time (MLIT)**
15:13	0h RO	Reserved.
12:0	2h RW	**Low Idle Wake Latency (LIWL)**

24.2.67 LFPS On Count (LFPSONCOUNT_REG)—Offset 81B8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 20C8h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:16	0h RW	**U2P3 LFPS Periodic Sampling Control (XU2P3LPSC):** This field controls the OFF time for the LFPS periodic sampling for SS ports in U2P3. If LFPSPM for a port is 1, it will override the OFF time and LFPS receiver will remain OFF permanently. For Fast Sim mode, 500us will be equivalent to 5us. 0x0 Polling Disable. (RXDET Polling will become 100ms.) 0x1 500us OFF Time 0x2 1ms OFF Time 0x3 1.5ms OFF Time
15:10	8h RW	**XLFPSONCNTSSIC (XLFPSONCNTSSIC):** This time would describe the number of clocks LFPS will remain ON. LFPS detection operation may be carried out on using RTC clock or Oscillator clock. The value of this register should be adjusted accordingly. For RTC recommended value is 2. For Oscillator clock, recommended value is 8.
9:0	C8h RW	**XLFPSONCNTSS (XLFPSONCNTSS)**

24.2.68 USB2 PM Control (USB2PMCTRL_REG)—Offset 81C4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 908h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	0h RW	**Bypass Suspend SM (BYPSUSSM)**
12	0h RO	Reserved.
11	1h RW	**USB2 PHY SUS Power Gate PORTSC Block Policy (U2PSPGPSCBP):** This controls the policy for blocking PORTSC Updates while the USB2 PHY SUS Well is power gated. When set, the controller will block any updates to the PORTSC caused by port status change if the USB2 PHY SUS is power gated.
10:8	1h RW	**USB2 PHY SUS Well Power Gate Entry Hysteresis Count (U2PSPGEHC)**
7:4	0h RW	**USB2 PHY SUS Power Gate PORTSC Block Policy (U2CLPGLAT)**
3:2	2h RW	**USB2 PHY SUS Well Power Gate Policy (U2PSUSPGP)**
1:0	0h RO	Reserved.

24.2.69 USB Legacy Support Capability (USBLEGSUP)—Offset 846Ch

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 2201h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RW	**HC OS Owned Semaphore (HCOSOS):** Default = '0'. System software sets this bit to request ownership of the xHC. Ownership is obtained when this bit reads as '1' and the HC BIOS Owned Semaphore bit reads as '0'.
23:17	0h RO	Reserved.
16	0h RW	**HC BIOS Owned Semaphore (HCBIOSOS):** Default = '0'. The BIOS sets this bit to establish ownership of the xHC. System BIOS will set this bit to a '0' in response to a request for ownership of the xHC by system software.
15:8	22h RW/L	**Next Capability Pointer (NEXTCP):** This field indicates the location of the next capability with respect to the effective address of this capability. Refer to Table 145 for more information on this field.
7:0	1h RW/L	**Capability ID (CID):** This field identifies the extended capability. Refer to Table 146 for the value that identifies the capability as Legacy Support.This extended capability requires one additional 32-bit register for control/status information (USBLEGCTLSTS), and this register is located at offset xECP+04h.

24.2.70 Port Disable Override Capability Register (PDO_CAPABILITY)—Offset 84F4h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 3C6h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	3h RO	**Next Capability Pointer (NCP)**
7:0	C6h RO	**Capability ID (CID)**

24.2.71 USB2 Port Disable Override (USB2PDO)—Offset 84F8h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11:0	0h RW/O	**USB2PDO (USB2PDO):** A '1' in a bit position prevents the corresponding USB2 port from reporting a Device Connection to the XHC.This applies across all USB2 protocol ports 0 = Allows corresponding USB port to report a device connection to the xHC. 1 = Prevents the corresponding USB port from reporting a device Connection to the xHC. Port to bit mapping is in one-hot encoding, that is bit 0 controls port 1 and so on. Bit 0 = USB 2.0 port 0 ... Bit N = USB 2.0 port N

24.2.72 USB3 Port Disable Override (USB3PDO)—Offset 84FCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RW/O	**USB3 Port Disable Override (USB3PDO):** 0 = Allows corresponding USB port to report a Device Connection to the xHC. 1 = Prevents the corresponding USB port from reporting a Device Connection to the xHC. Bit 0 = USB 3.1 Port 1 ... Bit N = USB 3.1 Port N

24.2.73 Debug Capability ID Register (DCID)—Offset 8700h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 5100Ah

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	Reserved.
20:16	5h RW/L	**Debug Capability Event Ring Segment Table Max (DCERSTM)**
15:8	10h RW/L	**Next Capability Pointer (NCP)**
7:0	Ah RW/L	**Capability ID (CID)**

24.2.74 Global Time Sync Capability (GLOBAL_TIME_SYNC_CAP_REG)—Offset 8E10h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 12C9h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	12h RO	**Next Capability pointer (NCP)**
7:0	C9h RO	**Capability ID (CID)**

24.2.75 Global Time Sync Control (GLOBAL_TIME_SYNC_CTRL_REG)—Offset 8E14h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW/1S	**Time Stamp Counter Capture Initiate (TIME_STAMP_CNTR_CAPTURE_INITIATE)**

24.2.76 Microframe Time (Local Time) (MICROFRAME_TIME_REG)—Offset 8E18h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:16	0h RO	**Captured Frame List Current Index/Frame Number (CMFI)**
15:13	0h RO	Reserved.
12:0	0h RO	**Captured Micro-frame BLIF (CMFB)**

24.2.77 Always Running Time (ART) Low (ALWAYS_RUNNING_TIME_LOW)—Offset 8E20h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**GLOBAL_TIME_LOW_REG (GLOBAL_TIME_LOW)**

24.2.78 Always Running Time (ART) High (ALWAYS_RUNNING_TIME_HIGH)—Offset 8E24h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**GLOBAL_TIME_HI_REG (GLOBAL_TIME_HI)**

24.2.79 XHCI USB2 Overcurrent Pin Mapping (U2OCM1)—Offset 90A4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:0	0h RW/L	**OC Mapping (OCM)**

24.2.80 XHCI USB2 Overcurrent Pin Mapping (U2OCM2)—Offset 90A8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:0	0h RW/L	**OC Mapping (OCM)**

24.2.81 XHCI USB2 Overcurrent Pin Mapping (U2OCM3)—Offset 90ACh

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:0	0h RW/L	**OC Mapping (OCM)**

24.2.82 XHCI USB2 Overcurrent Pin Mapping (U2OCM4)—Offset 90B0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:0	0h RW/L	**OC Mapping (OCM)**

24.2.83 XHCI USB2 Overcurrent Pin Mapping (U2OCM5)—Offset 90B4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:0	0h RW/L	**OC Mapping (OCM)**

24.2.84 XHCI USB2 Overcurrent Pin Mapping (U2OCM6)—Offset 90B8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:0	0h RW/L	**OC Mapping (OCM)**

24.2.85 XHCI USB2 Overcurrent Pin Mapping (U2OCM7)—Offset 90BCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:0	0h RW/L	**OC Mapping (OCM)**

24.2.86 XHCI USB2 Overcurrent Pin Mapping (U2OCM8)—Offset 90C0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:0	0h RW/L	**OC Mapping (OCM)**

24.2.87 XHCI USB3 Overcurrent Pin Mapping (U3OCM1)—Offset 9124h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RW/L	**OC Mapping (OCM)**

24.2.88 XHCI USB3 Overcurrent Pin Mapping (U3OCM2)—Offset 9128h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RW/L	**OC Mapping (OCM)**

24.2.89 XHCI USB3 Overcurrent Pin Mapping (U3OCM3)—Offset 912Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RW/L	**OC Mapping (OCM)**

24.2.90 XHCI USB3 Overcurrent Pin Mapping (U3OCM4)—Offset 9130h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RW/L	**OC Mapping (OCM)**

24.2.91 XHCI USB3 Overcurrent Pin Mapping (U3OCM5)—Offset 9134h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RW/L	**OC Mapping (OCM)**

24.2.92 XHCI USB3 Overcurrent Pin Mapping (U3OCM6)—Offset 9138h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RW/L	**OC Mapping (OCM)**

24.2.93 XHCI USB3 Overcurrent Pin Mapping (U3OCM7)—Offset 913Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RW/L	**OC Mapping (OCM)**

24.2.94 XHCI USB3 Overcurrent Pin Mapping (U3OCM8)—Offset 9140h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RW/L	**OC Mapping (OCM)**

24.3 USB Configuration Registers

The USB Configuration Registers are distributed within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface using the following Target Port (Destination Port) Identification:

Target Port (Destination Port) Identification = 0xCA

For complete details on how to use the PCH Sideband Interface to access these PCH Private Configuration Registers reference the latest Platform Controller Hub BIOS Specification.

24.3.1 USB2 PER PORT 1 Electrical Control Register (USB2PP1)

Access Method

Type: IOBP Index: Port 0: CA004100h Port 1: CA004200h Port n: CA004n00h (Size: 32 bits)	Device: Function:

Default: See Below

Bit Range	Default and Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14	0h RW	Per Port Half Bit Pre-emphasis (PERPORTTXPEHALF) Configuration bit (per port) to select between half-bit or full-bit implementation 1 = select half-bit pre-emphasis 0 = select full-bit pre-emphasis Note: This bit is do not care when **Per Port HS TX Emphasis** is configured to "11"
13:11	0h RW	Per Port HS Pre-emphasis bias (PERPORTPETXISET)
10:8	0h RW	Per Port HS TX Bias (PERPORTTXISET)
7:0	0h RO	Reserved.

24.3.2 USB2 PER PORT 2 Electrical Control Register (USB2PP2)

Access Method

Type: IOBP Index: Port 0: CA004126h Port 1: CA004226h Port n: CA004n26h (Size: 32 bits)	**Device:** **Function:**

Default: See Below

Bit Range	Default and Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24:23	0h RW	Per Port HS TX Emphasis (IUSBTXEMPHASISEN) Enables the HS TX Emphasis for the respective port
22:0	0h RW	Reserved.

24.3.3 Global ADP VBUS COMP REG (GLB ADP VBUS COMP REG)

Access Method

Type: IOBP Index: CA00402Bh (Size: 32 bits)	Device: Function:

Default: See Below

Bit Range	Default and Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22	1h RW	Differential Disconnect Enable 0: Reserved. 1: Differential Disconnect - enabled
21:0	0h RW	Reserved.

24.3.4 USB2 COMPBG (USB2_COMPBG)

Access Method

Type: IOBP Index: CA007F04h (Size: 32 bits)	Device: Function:

Default: See Below

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	1h RW	USB2 Disconnect Reference Select (UDRS) Selects the reference voltage disconnect detector. 0: Reserved. 1: Differential Disconnect circuit.
14:13	0h RW	USB2 AFE Squelch Reference Positive Voltage Programming (UASQRPVP) These bits specify the programming options for USB2 AFE Squelch reference Positive voltage. 3h: 350mV 2h: 325mV 1h: 300mV 0h: 312.5mV
12:11	0h RW	USB2 AFE Squelch Reference Negative Voltage Programming (UASQRNVP) These bits specify the programming options for USB2 AFE Squelch reference Negative voltage. 3h: 250mV 2h: 225mV 1h: 175mV 0h: 200mV
10:7	0h RW	Differential Disconnect Reference Voltage Programming Bit Value Vref (mV) 0000: Reserved 0001: Reserved 0010: Reserved 0011: Reserved 0100: 562.5 0101: 687.5 0110: 437.5 0111: 312.5 1000: 625 1001: 750 1010: 500 1011: 375 1100: 687.5 1101: 812.5 1110: 562.5 1111: 437.5
7:0	0h RO	Reserved.

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25 USB 3.2 Gen 1x1 (5 Gb/s) Device Controller- xDCI (D20:F1)

25.1 xDCI PCI Configuration Registers

Table 25-1. Summary of xDCI PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device ID and Vendor ID (DEVVENDID)—Offset 0h	AAA8086h
4h	7h	Status and Command (STATUSCOMMAND)—Offset 4h	100000h
10h	17h	Base Address Register (BAR)—Offset 10h	4h
18h	1Fh	Base Address Register1 (BAR1)—Offset 18h	4h
2Ch	2Fh	Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch	0h
34h	37h	Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	Interrupt Register (INTERRUPTREG)—Offset 3Ch	100h
80h	83h	PowerManagement Capability ID (POWERCAPID)—Offset 80h	48039001h
84h	87h	Power Management Control and Status (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
94h	97h	Device ID and Vendor Specific Register (DEVID_VEND_SPECIFIC_REG)—Offset 94h	1400010h
98h	9Bh	SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	0h
9Ch	9Fh	Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch	10F8301h
A0h	A3h	(D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	80800h

25.1.1 Device ID and Vendor ID (DEVVENDID)—Offset 0h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 20
Function: 1

Default: AAA8086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	AAAh RO	**DEVICEID:** Device ID identifies the particular PCI device. Refer to the Device and Revision ID Table in Volume 1 for default value.
15:0	8086h RO	**Vendor Identification (VENDORID):** Vendor ID is a unique ID identifying the manufacturer of the device. 8086h = Intel

25.1.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW/1C	**Received Initiator Abort (RMA):** If the completion status received from IOSF is UR, the Bridge sets this bit. Thesoftware writes a 1 to this bit to clear it.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, the Bridge sets this bit. Thesoftware writes a 1 to this bit to clear it.
27:21	0h RO	Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Indicates that the controller contains a capabilities pointer list. The firstitem is pointed to by looking at the configuration offset 34h.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device Only when theInterrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a1, is the device/function interrupt message sent. Setting the Interrupt Disable bit to a1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Interrupt Disable: Setting this bit disables INTx assertion fromBridge. The interrupt disabled is legacy INTx# interrupt, which is the Bridge does notsend Interrupt Assert message through the IOSF Sideband Channel. Reset value ofthis bit is 0. This bit has no connection with the interrupt status bit.
9	0h RO	Reserved.
8	0h RW	**SERR Enable (SERR_ENABLE):** Not implemented
7:3	0h RO	Reserved.
2	0h RW	**Bus Initiator Enable (BME):** Bus Initiator Enable: If this bit is 0,the Bridge does not generate any newupstream transaction on IOSF as a Initiator. Reset value of this bit is 0.
1	0h RW	**Memory Space Enable (MSE):** Memory Space Enable: This bit controls Bridge response to downstreammemory accesses. When set, accesses to memory space of the device is enabled.Reset value of this bit is 0.
0	0h RO	Reserved.

25.1.3 Base Address Register (BAR)—Offset 10h

Access Method

Type: CFG Register
(Size: 64 bits)

Device: 20
Function: 1

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
63:21	0h RW	**Base Address Register Low (BASEADDR)**
20:12	0h RO	Reserved.
11:4	0h RO	**Size Indicator (SIZEINDICATOR):** Always returns 0. The size of this register depends on the size of the memory space.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable
2:1	2h RO	**Type (TYPE):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range, If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0 indicates this BAR is present in the memory space.

25.1.4 Base Address Register1 (BAR1)—Offset 18h

Memory accesses to BAR1 region are aliased to the PCI configuration space. The BAR1region is always 4K. Software access through BAR1 can only access the regular PCIconfiguration space. BAR1 memory accesses, which do not access a defined PCIconfiguration register, are treated as access to reserved register. If this register isdisabled then this is RO and always returns 0.

Access Method

Type: CFG Register
(Size: 64 bits)

Device: 20
Function: 1

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
63:32	0h RW	**Base Address high (BASEADDR1_HIGH)**
31:12	0h RW	**BASEADDR1:** This field is present if BAR1 is enabled through private configuration space.
11:4	0h RO	**Size Indicator (SIZEINDICATOR1):** Always is 0 as minimum size is 4K

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not prefetchable.
2:1	2h RO	**Type (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0 Indicates this BAR is present in the memory space.

25.1.5 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

SVID register along with SID register is to distinguish subsystem from another

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SUBSYSTEMID):** This register is implemented for any function thatcan be instantiated more than once in a given system. The SID register, incombination with the Subsystem Vendor ID register make it possible for theoperating environment to distinguish one subsystem from the other. This register is aRead Write Once type register.
15:0	0h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register must be implemented for any function thatcan be instantiated more than once in a given system. The SVID register, incombination with the Subsystem ID register, enables the operating environment todistinguish one subsystem from the other. This register is a Read Write Once register

25.1.6 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	80h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is.

25.1.7 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: CFG Register (Size: 32 bits)
Device: 20
Function: 1

Default: 100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Max Latency (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**Min Latency (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Interrupt Pin Value in this register is reflected from the IPIN value in theprivate configuration space. For a single function device, this ideally is INTA.
7:0	0h RW	**Interrupt Line (INTLINE):** PCH does not use this field directly. It is used to communicate tosoftware, the interrupt line to which the interrupt pin is connected.

25.1.8 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 20
Function: 1

Default: 48039001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	9h RO	**PMESUPPORT:**
26:19	0h RO	Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	90h RO	**Next Capability (NXTCAP):** Points to the next capability structure.
7:0	1h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

25.1.9 Power Management Control and Status (PMECTRLSTATUS)—Offset 84h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 20
Function: 1

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** 0 Software clears the bit by writing a 1 to it. 1 This bit is set when the PME# signal is asserted independent of the state of the PMEEnable bit (bit 8 in this register)
14:9	0h RO	Reserved.
8	0h RW	**PME Enable (PMEENABLE):** 1 Enables the function to assert PME#. 0 PME# message on Sideband is disabled
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	0h RO	Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state and toset a new power state.The values are: 00 D0 state 11 D3HOT state Others Reserved

25.1.10 PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**VEND_CAP:** Vendor Specific Capability ID
27:24	0h RO	**REVID:** Revision ID of capability structure
23:16	14h RO	**CAP_LENGTH:** Vendor Specific Capability Length
15:8	0h RO	**NEXT_CAP:** Next Capability
7:0	9h RO	**CAPID:** Capability ID

25.1.11 Device ID and Vendor Specific Register (DEVID_VEND_SPECIFIC_REG)—Offset 94h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 20
Function: 1

Default: 1400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	14h RO	**VSEC_LENGTH:** Vendor Specific Extended Capability Length
19:16	0h RO	**VSEC_REV:** Vendor specific Extended Capability revision
15:0	10h RO	**VSECID:** Vendor Specific Extended Capability ID

25.1.12 SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 20
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**SW_LAT_DWORD_OFFSET:** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW_LAT_BAR_NUM:** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**Valid (SW_LAT_VALID)**

25.1.13 Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Access Method

Type: CFG Register (Size: 32 bits)
Device: 20
Function: 1

Default: 10F8301h

Bit Range	Default & Access	Field Name (ID): Description
31:4	10F830h RO	**DWORD_OFFSET:** Contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR
3:1	0h RO	**BAR Number (BAR_NUM):** Indicates that the D0i3 MMIO location is always at BAR0
0	1h RO	**Valid (VALID)**

25.1.14 (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 20
Function: 1

Default: 80800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW	**HAE:** Hardware Autonomous Enable
20	0h RO	Reserved.
19	1h RW	**SLEEP_EN:** Sleep Enable
18	0h RW	**D3HEN:** D3-Hot Enable (D3HEN): If 1, then the function will power gate when idle and the PMCSR[1:0] register in the function D3.
17	0h RW	**DEVIDLEN:** If 1, then the function will power gate when idle and the DevIdle register (DevIdleC[2]=1) is set.
16	0h RW	**D3_ENABLE:** D3-Hot Enable (D3HEN): If set to 1, then function will power gate when idle and the PMCSR[1:0] register in the function = 11 (D3).
15:13	0h RO	Reserved.
12:10	2h RW/O	**POW_LAT_SCALE:** Power On Latency Scale
9:0	0h RW/O	**POW_LAT_VALUE:** Power On Latency value

25.2 xDCI MMIO Device Registers

Table 25-2. Summary of xDCI MMIO Device Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
C700h	C703h	Device Configuration Register (DCFG)—Offset C700h	80004h
C704h	C707h	Device Control Register (DCTL)—Offset C704h	F00000h

Table 25-2. Summary of xDCI MMIO Device Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
C708h	C70Bh	Device Event Enable Register (DEVTEN)—Offset C708h	0h
C70Ch	C70Fh	Device Status Register (DSTS)—Offset C70Ch	520004h
C710h	C713h	Device Generic Command Parameter (DGCMDPAR)—Offset C710h	0h
C714h	C717h	Device Generic Command (DGCMD)—Offset C714h	0h
C720h	C723h	Device Active USB Endpoint Enable (DALEPENA)—Offset C720h	0h
C800h	C803h	Device Physical Endpoint-n Command Parameter 2 (DEPCMDPAR2)—Offset C800h	0h
C804h	C807h	Device Physical Endpoint-n Command Parameter 1 (DEPCMDPAR1)—Offset C804h	0h
C808h	C80Bh	Device Physical Endpoint-n Command Parameter 0 (DEPCMDPAR0)—Offset C808h	0h
C80Ch	C80Fh	Device Physical Endpoint-n Command (DEPCMD)—Offset C80Ch	0h

25.2.1 Device Configuration Register (DCFG)—Offset C700h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 80004h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22	0h RW	**LPM Capable (LPMCAP):** The application uses this bit to control the LPM capabilities: 1'b0: LPM capability is not enabled. 1'b1: LPM capability is enabled.
21:17	4h RW	**Number of Receive Buffers (NUMP):** This bit indicates the number of receive buffers to be reported in the ACK TP.
16:12	0h RW	**Interrupt Number (INTRNUM):** Indicates interrupt number on which non-endpoint-specific device-related interrupts are generated.
11:10	0h RO	Reserved.
9:3	0h RW	**Device Address (DEVADDR)**
2:0	4h RW	**Device Speed (DEVSPD):** Indicates the speed at which the application requires the core to connect, or the maximum speed the application can support: 3’b100: SuperSpeed 3’b000: High-speed 3’b001: Full-speed

25.2.2 Device Control Register (DCTL)—Offset C704h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: F00000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Run/Stop (RUN_STOP):** The software writes 1 to this bit to start the device controller operation.To stop the device controller operation, the software must remove any active transfers and write 0 to this bit. When the controller is stopped, it sets the DSTS.DevCtrlHlt bit when the core is idle and the lower layer finishes the disconnect process. The Run/Stop bit must be used in following cases as specified: 1.After power-on reset and CSR initialization, the software must write 1 to this bit to start the device controller. The controller does not signal connect to the host until this bit is set. 2.The software uses this bit to control the device controller to perform a soft disconnect. When the software writes 0 to this bit, the host does not see that the device is connected. The device controller stays in the disconnected state until the software writes 1 to this bit. The minimum duration of keeping this bit cleared: SS: 30ms HS/FS/LS: 10ms If the software attempts a connect after the soft disconnect or detects adisconnect event, it must set DCTL[8:5] to 5 before reasserting the Run/ Stopbit. 3.When the USB or Link is in a lower power state and the Two Power Rails configuration is selected, software writes 0 to this bit to indicate that it is going to turn off the Core Power Rail. After the software turns on the Core Power Rail again and re-initializes the device controller, it must set this bit to start the device controller.
30	0h RW	**Core Soft Reset (CSFTRST):** Resets the all clock domains
29	0h RO	Reserved.
28:24	0h RW	**HIRD Threshold (HIRDTHRES):** The core asserts output signals utmi_l1_suspend_n and utmi_sleep_n on the basis of this signal: The core asserts utmi_l1_suspend_n to put the PHY into Deep Low-Power mode in L1 when both of the following are true: -HIRD value is greater than or equal to the value in DCTL.HIRD_Thres[3:0] -HIRD_Thres[4] is set to 1'b1. The core asserts utmi_sleep_n on L1 when one of the following is true: -If the HIRD value is less than HIRD_Thres[3:0] or -HIRD_Thres[4] is set to 1'b0. Note: This field must be set to '0' during SuperSpeed mode of operation.
23:20	Fh RW	**LPM NYET Response Threshold (LPM_NYET_thres):** Handshake response to LPM token specified by device application
19	0h RW	**Keep Connect (KeepConnect):** When '1', this bit enables the save and restore programming model by preventing the core from disconnecting from the host when DCTL.RunStop is set to '0'. It also enables the Hibernation Request Event to be generated when the link goes to U3 or L2. The device core disconnects from the host when DCTL.RunStop is set to '0'. This bit indicates whether to preserve this behavior ('0'), or if the core should not disconnect when RunStop is set to 0 ('1').This bit also prevents the LTSSM from automatically going to U0/L0 when the host requests resume from U3/L2.
18	0h RW	**L1 Hibernation Enable (L1HibernationEn):** When this bit is set along with KeepConnect, the device core generates a Hibernation Request Event if L1 is enabled and the HIRD value in the LPM token is larger than the threshold programmed in DCTL.HIRD_Thres. The core will not exit the LPM L1 state until software writes Recovery into the DCTL.ULStChngReq field. This prevents corner cases where the device is entering hibernation at the same time the host is attempting to exit L1.
17	0h RW	**Controller Restore State (CRS):** This command initiates the restore process. When software sets this bit to '1', the controller immediately sets DSTS.RSS to '1'. When the controller has finished the restore process, it sets DSTS.RSS to '0'. Note: When read, this field always returns '0'.
16	0h RW	**Controller Save State (CSS):** This command initiates the save process.When software sets this bit to '1', the controller immediately sets DSTS.SSS to '1'. When the controller has finished the save process, it sets DSTS.SSS to '0'. Note: When read, this field always returns '0'.
15:13	0h RO	Reserved.
12	0h RW	**Initiate U2 Enable (INITU2ENA):** 1'b0: May not initiate U2 (default) 1'b1: May initiate U2 On USB reset, hardware clears this bit to "0". Software sets this bit after receiving SetFeature(U2_ENABLE), and clears this bit when ClearFeature(U2_ENABLE) is received.If DCTL[11] (AcceptU2Ena) is 0, the link immediately exits U2 state.
11	0h RW	**Accept U2 Enable (ACCEPTU2ENA):** 1'b0: Reject U2 except when Force_LinkPM_Accept bit is set (default) 1'b1: Core accepts transition to U2 state if nothing is pending on the application side.On USB reset, hardware clears this bit to "0". Software sets this bit after receiving a SetConfiguration command

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**Initiate U1 Enable (INITU1ENA):** 1'b0: May not initiate U1 1'b1: May initiate U1 On USB reset, hardware clears this bit to "0". Software sets this bit after receiving SetFeature(U1_ENABLE), and clears this bit when ClearFeature(U1_ENABLE) is received. If DCTL[9] (AcceptU1Ena) is 0, the link immediately exits U1 state.
9	0h RW	**Accept U1 Enable (ACCEPTU1ENA):** 1'b0: Core rejects U1 except when Force_LinkPM_Accept bit is set (default) 1'b1: Core accepts transition to U1 state if nothing is pending on the application side. On USB reset, hardware clears this bit to "0". Software sets this bit after receiving a SetConfiguration command.
8:5	0h WO	**USB / Link State Change Request (ULSTCHNGREQ):** Software writes this field to issue a USB/Link state change request. A change in this field indicates a new request to the core. If software wants to issue the same request back-to-back, it must write a 0 to this field between the two requests. The result of the state change request is reflected in the USB/Link State in DSTS. These bits are self-cleared on the MAC Layer exiting suspended state. If software is updating other fields of the DCTL register and not intending to force any link state change, then it must write a 0 to this field. SS Compliance mode is normally entered and controlled by the remote link partner. Alternatively, the local link can be forced directly into Compliance mode by resetting the SS link with the RUN/STOP bit set to zero. If then '10' is written to the USB/Link State Change field and '1' to RUN/STOP, the Link will go to Compliance. Once in Compliance, 'zero' and '10' may alternately be written to this field to advance the compliance pattern. In SS mode: ValueRequested Link State Transition: 0:No Action 4:SS.Disabled 5:Rx.Detect 6:SS.Inactive 8:Recovery 10:Compliance Others:Reserved In HS/FS/LS mode: ValueRequested USB state transition 8:Remote wakeup request Others:Reserved The Remote wakeup request should be issued 2µs after the device goes into suspend state. Note: After coming out of hibernation, software should write 8 (Recovery) into this field to confirm exit from the suspended state
4:0	0h RO	Reserved.

25.2.3 Device Event Enable Register (DEVTEN)—Offset C708h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	0h RW	**Vendor Device Test LMP Received Event (VENDEVTSTRCVDEN)**
11:10	0h RO	Reserved.
9	0h RW	**Erratic Error Event Enable (ERRTICERREVTEN)**
8:7	0h RO	Reserved.
6	0h RW	**U3/L2-L1 Suspend Event Enable (U3L2L1SuspEn)**
5	0h RO	Reserved.
4	0h RW	**Resume/Remote Wakeup Detected Event Enable (WKUPEVTEN)**

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**USB/Link State Change Event Enable (ULSTCNGEN)**
2	0h RW	**Connection Done Enable (CONNECTDONEEVTEN)**
1	0h RW	**USB Reset Enable (USBRSTEVTEN)**
0	0h RW	**Disconnect Detected Event Enable (DISSCONNEVTEN)**

25.2.4 Device Status Register (DSTS)—Offset C70Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 520004h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RO	**Device Controller Not Ready (DCNRD):** The bit indicates that the core is in the process of completing the state transitions after exiting from hibernation. To complete the state transitions, it takes 256 bus clock cycles from the time DCTL[31].Run/Stop is set. During hibernation, if the UTMI/ULPI PHY is in suspended state, then the 256-bus clock cycle delay starts after the PHY exited suspended state. Software must set DCTL[31].Run/Stop to '1' and wait for this bit to be de-asserted to zero before processing DSTS.USBLnkSt. This bit is valid only when DWC_USB3_EN_PWROPT is set to two and GCTL[1].GblHibernationEn =1.
28:26	0h RO	Reserved.
25	0h RO	**Restore State Status (RSS):** When the controller has finished the restore process, it will complete the command by setting DSTS.RSS to '0'.
24	0h RO	**Save State Status (SSS):** When the controller has finished the save process, it will complete the command by setting DSTS.SSS to '0'.
23	0h RO	**Core Idle (COREIDLE):** The bit indicates that the core finished transferring all RxFIFO data to system memory, writing out all completed descriptors, and all Event Counts are zero.
22	1h RO	**Device Controller Halted (DEVCTRLHLT):** This bit is set to 0 when the Run/Stop bit in the DCTL register is set to 1. The core sets this bit to 1 when, after SW sets Run/Stop to ‘0’, the core is idle and the lower layer finishes the disconnect process. When Halted =1, the core does not generate Device events.
21:18	4h RO	**USB/Link State (USBLNKST):** In SS mode: 4'h0: U0 4'h1: U1 4'h2: U2 4'h3: U3 4'h4: SS_DIS 4'h5: RX_DET 4'h6: SS_INACT 4'h7: POLL 4'h8: RECOV 4'h9: HRESET 4'ha: CMPLY 4'hb: LPBK 4'hf: Resume/Reset In HS/FS/LS mode: 4’h0: On state 4’h2: Sleep (L1) state 4’h3: Suspend (L2) state 4’h4: Disconnected state 4’h5: Early Suspend state 4'he: Reset 4'hf: Resume

Bit Range	Default & Access	Field Name (ID): Description
17	1h RO	**RxFIFO Empty (RXFIFOEMPTY)**
16:3	0h RO	**Frame/Microframe Number of the Received SOF (SOFFN):** When the core is operating at high-speed: [16:6] indicates the frame number [5:3] indicates the microframe number When the core is operating at full-speed: [16:14] is not used. Software can ignore these 3 bits [13:3] indicates the frame number
2:0	4h RO	**Connected Speed (CONNECTSPD):** Indicates the speed at which the core has come up after speed detection through a chirp sequence: 3'b100: SuperSpeed 3'b000: High-speed 3'b001: Full-speed 3'b010: Low-speed 3'b011: Full-speed

25.2.5 Device Generic Command Parameter (DGCMDPAR)—Offset C710h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Command Parameter (PARAMETER):** This register indicates the device command parameter. This must be programmed before or along with the device command (DGCMD).

25.2.6 Device Generic Command (DGCMD)—Offset C714h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:12	0h RO	**Command Status (CMDSTATUS):** 1: CmdErr – Indicates that the device controller encountered an error while processing the command. 0: Indicates command success
11	0h RO	Reserved.
10	0h NA	**Command Active (CMDACT):** The software sets this bit to 1 to enable the device controller to execute the generic command. The device controller sets this bit to 0 after executing the command.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	Reserved.
8	0h RW	**Command Interrupt on Complete (CMDIOC):** When this bit is set, the device controller issues a Generic Command Completion event after executing the command. Note that this interrupt is mapped to DCFG.IntrNum. Note: This field must not set to '1' if the DCTL.RunStop field is '0'.
7:0	0h RW	**Command Type (CMDTYP):** Specifies the type of command the software driver is requesting the core to perform: 02h: Set Periodic Parameters 04h: Set Scratchpad Buffer Array Address Lo 05h: Set Scratchpad Buffer Array Address Hi 07h:Transmit Device Notification 09h: Selected FIFO Flush 0Ah: All FIFO Flush 0Ch: Set Endpoint NRDY 10h: Run SoC Bus LoopBack Test

25.2.7 Device Active USB Endpoint Enable (DALEPENA)—Offset C720h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**USB Active Endpoints (USBACTEP):** This field indicates if a USB endpoint is active in the current configuration and interface. Bit[0]: USB EP0-OUT Bit[1]: USB EP0-IN Bit[2]: USB EP1-OUT Bit[3]: USB EP1-IN

25.2.8 Device Physical Endpoint-n Command Parameter 2 (DEPCMDPAR2)—Offset C800h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER):** This register indicates the physical endpoint command Parameter 2. It must be programmed before issuing the command.

25.2.9 Device Physical Endpoint-n Command Parameter 1 (DEPCMDPAR1)—Offset C804h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER):** This register indicates the physical endpoint command Parameter 1. It must be programmed before issuing the command

25.2.10 Device Physical Endpoint-n Command Parameter 0 (DEPCMDPAR0)—Offset C808h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER):** This register indicates the physical endpoint command parameter 0. This must be programmed before or along with the command. For commands needing only one 32-bit parameter, this register must be programmed with the command register.

25.2.11 Device Physical Endpoint-n Command (DEPCMD)—Offset C80Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Command Parameters (COMMANDPARAM):** When this register is written: For Start Transfer command: -[31:16]: StreamID. The USB StreamID assigned to this transfer For Start Transfer command applied to an isochronous endpoint: -[31:16]: StartMicroFramNum: Indicates the (micro)frame number to which the first TRB applies For Update Transfer, End Transfer, and Start New Configuration commands: -[22:16]: Transfer Resource Index (XferRscIdx). The hardware-assigned transfer resource index for the transfer, which was returned in response to the Start Transfer command. The application software-assigned transfer resource index for a Start New Configuration command
15:12	0h RW	**Command Completion Status (CMDSTATUS):** Additional information about the completion of this command is available in this field.
11	0h RW	**HighPriority/ForceRM (HIPRI_FORCERM):** HighPriority: Only valid for Start Transfer command ForceRM: Only valid for End Transfer command ClearPendIN: Only valid for Clear Stall command – Software sets this bit to clear any pending IN transaction (on that endpoint) stuck at the lower layers when a Clear Stall command is issued.
10	0h RW	**Command Active (CMDACT):** Software sets this bit to 1 to enable the device endpoint controller to execute the generic command.The device controller sets this bit to 0 when the CmdStatus field is valid and the endpoint is ready to accept another command. This does not imply that all the effects of the previously-issued command have taken place.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	Reserved.
8	0h RW	**Command Interrupt on Complete (CMDIOC):** When this bit is set, the device controller issues a generic Endpoint Command Complete event after executing the command. Note that this interrupt is mapped to DEPCFG.IntrNum. When the DEPCFG command is executed, the command interrupt on completion goes to the interrupt pointed by the DEPCFG.IntrNum in the current command. Note: This field must not set to '1' if the DCTL.RunStop field is '0'.
7:4	0h RO	Reserved.
3:0	0h RW	**Command Type (CMDTYP):** Specifies the type of command the software driver is requesting the core to perform. 00h: Reserved 01h: Set Endpoint Configuration-64 or 96-bit Parameter 02h: Set Endpoint Transfer Resource Configuration-32-bit Parameter 03h: Get Endpoint State-No Parameter Needed 04h: Set Stall-No Parameter Needed 05h: Clear Stall (see Set Stall)-No Parameter Needed 06h: Start Transfer-64-bit Parameter 07h: Update Transfer-No Parameter Needed 08h: End Transfer-No Parameter Needed 09h: Start New Configuration-No Parameter Needed

25.3 xDCI MMIO Global Registers

Table 25-3. Summary of xDCI MMIO Global Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
C100h	C103h	Global SoC Bus Configuration 0 (GSBUSCFG0)—Offset C100h	6h
C104h	C107h	Global SoC Bus Configuration 1 (GSBUSCFG1)—Offset C104h	F00h
C108h	C10Bh	Global Tx Threshold Control (GTXTHRCFG)—Offset C108h	0h
C10Ch	C10Fh	Global Rx Threshold Control (GRXTHRCFG)—Offset C10Ch	24400000h
C110h	C113h	Global Core Control (GCTL)—Offset C110h	2000h
C114h	C117h	GPMSTS (GPMSTS)—Offset C114h	0h
C118h	C11Bh	Global Status (GSTS)—Offset C118h	0h
C130h	C133h	Bus Address Low (GBUSERRADDRLO)—Offset C130h	0h
C134h	C137h	Bus Address High (GBUSERRADDRHI)—Offset C134h	0h
C140h	C143h	GHWPARAMS0 (GHWPARAMS0)—Offset C140h	40204008h
C144h	C147h	GHWPARAMS1 (GHWPARAMS1)—Offset C144h	260C93Bh
C148h	C14Bh	GHWPARAMS2 (GHWPARAMS2)—Offset C148h	8086A0h
C14Ch	C14Fh	GHWPARAMS3 (GHWPARAMS3)—Offset C14Ch	10420085h
C150h	C153h	GHWPARAMS4 (GHWPARAMS4)—Offset C150h	222004h
C154h	C157h	GHWPARAMS5 (GHWPARAMS5)—Offset C154h	4202088h
C158h	C15Bh	GHWPARAMS6 (GHWPARAMS6)—Offset C158h	2F60020h
C15Ch	C15Fh	GHWPARAMS7 (GHWPARAMS7)—Offset C15Ch	38507E6h
C160h	C163h	GDBGFIFOSPACE (GDBGFIFOSPACE)—Offset C160h	420000h
C164h	C167h	GDBGLTSSM (GDBGLTSSM)—Offset C164h	41010440h
C168h	C16Bh	GDBGLNMCC (GDBGLNMCC)—Offset C168h	0h
C16Ch	C16Fh	GDBGBMU (GDBGBMU)—Offset C16Ch	0h
C174h	C177h	GDBGLSP (GDBGLSP)—Offset C174h	0h
C178h	C17Bh	GDBGEPINFO0 (GDBGEPINFO0)—Offset C178h	0h
C17Ch	C17Fh	GDBGEPINFO1 (GDBGEPINFO1)—Offset C17Ch	800000h

Table 25-3. Summary of xDCI MMIO Global Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
C300h	C303h	Global Transmit FIFO Size Register N (GTXFIFOSIZ0_0)—Offset C300h	42h
C380h	C383h	GRXFIFOSIZ0_0 (GRXFIFOSIZ0_0)—Offset C380h	385h
C400h	C403h	GEVNTADRLO_0 (GEVNTADRLO_0)—Offset C400h	0h
C404h	C407h	GEVNTADRHI_0 (GEVNTADRHI_0)—Offset C404h	0h
C40Ch	C40Fh	GEVNTCOUNT_0 (GEVNTCOUNT_0)—Offset C40Ch	0h
C610h	C613h	GTXFIFOPRIDEV (GTXFIFOPRIDEV)—Offset C610h	0h

25.3.1 Global SoC Bus Configuration 0 (GSBUSCFG0)—Offset C100h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 6h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW	**Data Access is Big-Endian (DATBIGEND):** This bit controls the endian modefor data accesses. 0: Little-endian (default) 1: Big-endian In big-endian mode, DMAaccess (both read and write) for packet data will utilize a Byte Invariant Big-Endianmode. Note: Since AXI requires byte invariant endianness, settingDescBigend and DatBigEnd to one causes an address invariant transform to be applied, which is not appropriate. Henceforth an AXI Initiator (DWC_USB3_MBUS_TYPE=1), this bit must be set to zero.
10:8	0h RO	Reserved.
7	0h RW	**INCR256 Burst Type Enable (INCR256BRSTENA):** If software set this bit to "1", the Initiator uses INCR to do the 256-beat burst.
6	0h RW	**INCR128 Burst Type Enable (INCR128BRSTENA):** If software set this bit to "1", the Initiator uses INCR to do the 128-beat burst.
5	0h RW	**INCR64 Burst Type Enable (INCR64BRSTENA):** If software set this bit to "1", the Initiator uses INCR to do the 64-beat burst.
4	0h RW	**INCR32 Burst Type Enable (INCR32BRSTENA):** If software set this bit to "1", the Initiator uses INCR to do the 32-beat burst.
3	0h RW	**INCR16 Burst Type Enable (INCR16BRSTENA):** If software set this bit to "1", the Initiator uses INCR to do the 16-beat burst.

Bit Range	Default & Access	Field Name (ID): Description
2	1h RW	**INCR8 Burst Type Enable (INCR8BRSTENA):** if software set this bit to "1", the Initiator uses INCR to do the 8-beat burst
1	1h RW	**INCR4 Burst Type Enable (INCR4BRSTENA):** When this bit is enabled the controller is allowed to do bursts of beat length 1, 2, 3, and 4
0	0h RW	**Undefined Length INCR Burst Type Enable (INCRBrstEna) Input to BUS-GM (INCRBRSTENA):** When enabled, this has higher priority than other burst types. For the AHB configuration. if this bit is set to 1, AHB Initiator tries to do only one INCR burst for each transfer unless it has to break it at a 1Kbyte boundary. If this bit is set to 0, the AHB Initiator may still use INCR burst type at the beginning and end bursts of transfers to align the address. The middle bursts are INCR4/8/16, depending when the type is enabled.

25.3.2 Global SoC Bus Configuration 1 (GSBUSCFG1)—Offset C104h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: F00h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	0h RW	**1k Page Boundary Enable (EN1KPAGE):** By default (this bit is disabled) the AXI breaks transfers at the 4k page boundary. When this bit is enabled, the AXI Initiator (DMA data) breaks transfers at the 1k page boundary.
11:8	Fh RW	**AXI Pipelined Transfers Burst Request Limit (PipeTransLimit):** The field controls the number of outstanding pipelined transfers requests the AXI Initiator will push to the AXI Target. Once the AXI Initiator reaches this limit, it will not make more requests on the AXI ARADDR and AWADDR buses until the associated data phases complete. This field is encoded as follows: h0: 1 request h1: 2 requests h2: 3 requests h3: 4 requests ... hF: 16 requests
7:0	0h RO	Reserved.

25.3.3 Global Tx Threshold Control (GTXTHRCFG)—Offset C108h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RO	**USB Transmit Packet Count Enable (USBTxPktCntSel):** This fieldenables/ disables the USB transmission multi-packet thresholding: 0: USB transmissionmulti-packet thresholding is disabled, the core can only start transmission on the USBafter the entire packet has been fetched into the corresponding TXFIFO. 1: USBtransmission multi-packet thresholding is enabled. The core can only start transmissionon the USB after USB Transmit Packet Count amount of packets for the USB transaction(burst) are already in the corresponding TXFIFO This mode is only valid in the hostmode. It is only used for SuperSpeed.
28	0h RO	Reserved.
27:24	0h RO	**USB Transmit Packet Count (USBTxPktCnt):** This field specifies thenumber of packets that must be in the TXFIFO before the core can start transmission forthe corresponding USB transaction (burst). This field is only valid when the USBTransmit Packet Count Enable field is set to one. Valid values are from 1 to 15.
23:16	0h RW	**USB Maximum TX Burst Size (USBMaxTxBurstSize):** When USBTxPktCntSel is one,this field specifies the Maximum Bulk OUT burst the core should do. When the systembus is slower than the USB, TX FIFO can underrun during a long burst. User canprogram a smaller value to this field to limit the TX burst size that the core can do. Itonly applies to SS Bulk, Isochronous, and Interrupt OUT endpoints in the host mode.Valid values are from 1 to 16
15:0	0h RO	Reserved.

25.3.4 Global Rx Threshold Control (GRXTHRCFG)—Offset C10Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 24400000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	1h RW	**USB ReceivePacket Count Enable (USBRxPktCntSel):** This field enables/disables theUSB reception multi-packet thresholding: n 0: The core can only start reception on theUSB when the RX FIFO has space for at least one packet. n 1: The core can only startreception on the USB when the RX FIFO has space for at least USBRxPktCnt amount ofpackets. This mode is only valid in the host mode. It is only used for SuperSpeed.
28	0h RO	Reserved.
27:24	4h RW	**USB Receive Packet Count (USBRxPktCnt):** This field specifies space (in number ofpackets) that must be available in the RX FIFO before the core can start thecorresponding USB RX transaction (burst). This field is only valid when the USB ReceivePacket Count Enable field is set to one. The valid values are from 1 to 15.
23:19	8h RW	**USB Maximum Rx Burst Size (USBMaxRxBurstSize):** This field is only validwhen USBRxPktCntSel is one. This field specifies the Maximum Bulk IN burst the coreshould do. When the system bus is slower than the USB, RX FIFO can overrun during along burst. User can program a smaller value to this field to limit the RX burst size thatthe core can do. It only applies to SS Bulk, Isochronous, and Interrupt IN endpoints inthe host mode. Valid values are from 1 to 16.
18:0	0h RO	Reserved.

25.3.5 Global Core Control (GCTL)—Offset C110h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 2000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18	0h RW	**Initiator Filter Bypass (InitiatorFILTBYPASS):** When this bit is set to 1'b1, irrespective ofthe parameter DWC_USB3_EN_BUS_FILTERS chosen, all the filters in theDWC_usb3_filter module will be bypassed. The double synchronizers to mac_clkpreceding the filters will also be bypassed. For enabling the filters, this bit should be1'b0.
17	0h RO	Reserved.
16	0h RW	**U2RSTECN (U2RSTECN):** The super speed connection fails during POLL or LMP exchange, thedevice connects at non-SS mode. If this bit is set, then device attempts three moretimes to connect at SS, even if it previously failed to operate in SS mode.
15:14	0h RW	**FRMSCLDWN (FRMSCLDWN):** This field scales down device view of a SOF/USOF/ ITP duration. For SS/HS mode: 2'h3 implements interval to be 15. 625 us 2'h2 implementsinterval to be 31.25 us 2'h1 implements interval to be 62.5 us 2'h0implements interval to be125us For FS mode, the scale-down value is multiplied by 8.
13:12	2h RW	**Port Capability Direction (PRTCAPDIR):** 2’b01: Reserved 2’b10: for Device configurations 2’b11: Reserved
11	0h RW	**Core Soft Reset (CORESOFTRESET):** 1b0 - No soft reset 1b1 - Soft reset
10:4	0h RO	Reserved.
3	0h RW	**Disable Scrambling (DISSCRAMBLE):** Transmit request to Link Partner on next transition to Recovery or Polling.
2	0h RO	Reserved.
1	0h RW	**Global Hibernation Enable (GblHibernationEn):** This bit enables hibernation at the global level. If hibernation is not enabled via this bit, the PMU immediately accepts the D0->D3 and D3->D0 power state change requests, but does not save or restore any core state. In addition, the PMUs will never drive the PHY interfaces and let the core continue to drive the PHY interfaces.
0	0h RW	**Disable Clock Gating (DSBLCLKGTNG):** When this bit is set to 1 and the core is in Low Power mode, internal clock gating is disabled.You can set this bit to 1’b1 after Power On Reset.

25.3.6 GPMSTS (GPMSTS)—Offset C114h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h WO	**PortSel (PortSel)**
27:17	0h RO	Reserved.
16:12	0h RO	**U3Wakeup (U3Wakeup)**
11:10	0h RO	Reserved.
9:0	0h RO	**U2Wakeup (U2Wakeup)**

25.3.7 Global Status (GSTS)—Offset C118h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	Reserved.
6	0h RO	**Device Interrupt Pending (Device_IP):** This field indicates that there is a pendinginterrupt pertaining to peripheral (device) operation in the Device event queue
5	0h RO	**CSR Timeout (CSRTimeout):** When this bit is 1'b1, it indicates that software performeda write or read to a core register that could not be completed withinbus clock cycles (default: 65535).
4	0h RO	**Bus Error Address Valid (BUSERRADDRVLD):** Indicates that the GBUSERRADDR register is valid and reports the first bus address that encounters a bus error.
3:2	0h RO	Reserved.
1:0	0h RO	**Current Mode of Operation (CURMOD):** Indicates the current mode of operation. 2'b00: Device mode 2'b01: Reserved

25.3.8 Bus Address Low (GBUSERRADDRLO)—Offset C130h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Bus Address Low (BUSERRADDR):** This 64-bit register contains the lower 32 bits of the first bus address that encountered a SoC bus error. It is valid when the GSTS.BusErrAddrVld field is 1.It can only be cleared by resetting the core

25.3.9 Bus Address High (GBUSERRADDRHI)—Offset C134h

25.3.10 GHWPARAMS0 (GHWPARAMS0)—Offset C140h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 40204008h

Bit Range	Default & Access	Field Name (ID): Description
31:24	40h RO	**DWC_USB3_ADWIDTH_31_24 (DWC_USB3_ADWIDTH_31_24)**
23:16	20h RO	**DWC_USB3_SDWIDTH_23_16 (DWC_USB3_SDWIDTH_23_16)**
15:8	40h RO	**DWC_USB3_MDWIDTH_15_8 (DWC_USB3_MDWIDTH_15_8)**
7:6	0h RO	**DWC_USB3_SBUS_TYPE_7_6 (DWC_USB3_SBUS_TYPE_7_6)**
5:3	1h RO	**DWC_USB3_MBUS_TYPE_5_3 (DWC_USB3_MBUS_TYPE_5_3)**
2:0	0h RO	**DWC_USB3_MODE_2_0 (DWC_USB3_MODE_2_0)**

25.3.11 GHWPARAMS1 (GHWPARAMS1)—Offset C144h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 260C93Bh

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26	0h RO	**DWC_USB3_MAC_PHY_CLKS_SYNC_26 (DWC_USB3_MAC_PHY_CLKS_SYNC_26)**
25:24	2h RO	**DWC_USB3_EN_PWROPT_25_24 (DWC_USB3_EN_PWROPT_25_24)**

Bit Range	Default & Access	Field Name (ID): Description
23	0h RO	**DWC_USB3_SPRAM_TYP_23 (DWC_USB3_SPRAM_TYP_23)**
22:21	3h RO	**DWC_USB3_NUM_RAMS_22_21 (DWC_USB3_NUM_RAMS_22_21)**
20:15	1h RO	**DWC_USB3_DEVICE_NUM_INT_20_15 (DWC_USB3_DEVICE_NUM_INT_20_15)**
14:12	4h RO	**DWC_USB3_ASPACEWIDTH_14_12 (DWC_USB3_ASPACEWIDTH_14_12)**
11:9	4h RO	**DWC_USB3_REQINFOWIDTH_11_9 (DWC_USB3_REQINFOWIDTH_11_9)**
8:6	4h RO	**DWC_USB3_DATAINFOWIDTH_8_6 (DWC_USB3_DATAINFOWIDTH_8_6)**
5:3	7h RO	**DWC_USB3_BURSTWIDTH_5_3 (DWC_USB3_BURSTWIDTH_5_3)**
2:0	3h RO	**DWC_USB3_IDWIDTH_2_0 (DWC_USB3_IDWIDTH_2_0)**

25.3.12 GHWPARAMS2 (GHWPARAMS2)—Offset C148h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 8086A0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	8086A0h RO	**DWC_USB3_USERID_31_0 (DWC_USB3_USERID_31_0)**

25.3.13 GHWPARAMS3 (GHWPARAMS3)—Offset C14Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 10420085h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:23	20h RO	**DWC_USB3_CACHE_TOTAL_XFER_RESOURCES_30_23 (DWC_USB3_CACHE_TOTAL_XFER_RESOURCES_30_23)**
22:18	10h RO	**DWC_USB3_NUM_IN_EPS_22_18 (DWC_USB3_NUM_IN_EPS_22_18)**

Bit Range	Default & Access	Field Name (ID): Description
17:12	20h RO	**DWC_USB3_NUM_EPS_17_12 (DWC_USB3_NUM_EPS_17_12)**
11	0h RO	**DWC_USB3_ULPI_CARKIT_11 (DWC_USB3_ULPI_CARKIT_11)**
10	0h RO	**DWC_USB3_VENDOR_CTL_INTERFACE_10 (DWC_USB3_VENDOR_CTL_INTERFACE_10)**
9:8	0h RO	**ghwparams3_9_8 (ghwparams3_9_8)**
7:6	2h RO	**DWC_USB3_HSPHY_DWIDTH_7_6 (DWC_USB3_HSPHY_DWIDTH_7_6)**
5:4	0h RO	**DWC_USB3_FSPHY_INTERFACE_5_4 (DWC_USB3_FSPHY_INTERFACE_5_4)**
3:2	1h RO	**DWC_USB3_HSPHY_INTERFACE_3_2 (DWC_USB3_HSPHY_INTERFACE_3_2)**
1:0	1h RO	**DWC_USB3_SSPHY_INTERFACE_1_0 (DWC_USB3_SSPHY_INTERFACE_1_0)**

25.3.14 GHWPARAMS4 (GHWPARAMS4)—Offset C150h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 222004h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	1h RO	**DWC_USB3_EXT_BUFF_CONTROL_21 (DWC_USB3_EXT_BUFF_CONTROL_21)**
20:17	1h RO	**DWC_USB3_NUM_SS_USB_INSTANCES_20_17 (DWC_USB3_NUM_SS_USB_INSTANCES_20_17)**
16:13	1h RO	**DWC_USB3_HIBER_SCRATCHBUFS_16_13 (DWC_USB3_HIBER_SCRATCHBUFS_16_13):** Number of external scratchpad buffers the core requires to save its internal state in the device mode. Each buffer is assumed to be 4KB
12	0h RO	**ghwparams4_12 (ghwparams4_12)**
11	0h RO	**ghwparams4_11 (ghwparams4_11)**
10:9	0h RO	**ghwparams4_10_9 (ghwparams4_10_9)**

Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RO	**ghwparams4_8_7 (ghwparams4_8_7)**
6	0h RO	**ghwparams4_6 (ghwparams4_6)**
5:0	4h RO	**DWC_USB3_CACHE_TRBS_PER_TRANSFER_5_0 (DWC_USB3_CACHE_TRBS_PER_TRANSFER_5_0)**

25.3.15 GHWPARAMS5 (GHWPARAMS5)—Offset C154h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 4202088h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:22	10h RO	**DWC_USB3_DFQ_FIFO_DEPTH_27_22 (DWC_USB3_DFQ_FIFO_DEPTH_27_22)**
21:16	20h RO	**DWC_USB3_DWQ_FIFO_DEPTH_21_16 (DWC_USB3_DWQ_FIFO_DEPTH_21_16)**
15:10	8h RO	**DWC_USB3_TXQ_FIFO_DEPTH_15_10 (DWC_USB3_TXQ_FIFO_DEPTH_15_10)**
9:4	8h RO	**DWC_USB3_RXQ_FIFO_DEPTH_9_4 (DWC_USB3_RXQ_FIFO_DEPTH_9_4)**
3:0	8h RO	**DWC_USB3_BMU_BUSGM_DEPTH_3_0 (DWC_USB3_BMU_BUSGM_DEPTH_3_0)**

25.3.16 GHWPARAMS6 (GHWPARAMS6)—Offset C158h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 2F60020h

Bit Range	Default & Access	Field Name (ID): Description
31:16	2F6h RO	**DWC_USB3_RAM0_DEPTH_31_16 (DWC_USB3_RAM0_DEPTH_31_16)**
15	0h RO	**BusFltrsSupport (BusFltrsSupport)**
14	0h RO	**BCSupport (BCSupport)**

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	**OTG_SS_Support (OTG_SS_Support):** 1'b0: No 3.0 support 1'b1: 3.0 support
12	0h RO	**ADPSupport (ADPSupport)**
11	0h RO	**HNPSupport (HNPSupport)**
10	0h RO	**SRPSupport (SRPSupport):** The application uses this bit to determine the DWC_usb3 core's SRP support. 1'b0: SRP support is not enabled 1'b1: SRP support is enabled
9:6	0h RO	Reserved.
5:0	20h RO	**DWC_USB3_PSQ_FIFO_DEPTH_5_0 (DWC_USB3_PSQ_FIFO_DEPTH_5_0)**

25.3.17 GHWPARAMS7 (GHWPARAMS7)—Offset C15Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 38507E6h

Bit Range	Default & Access	Field Name (ID): Description
31:16	385h RO	**DWC_USB3_RAM2_DEPTH_31_16 (DWC_USB3_RAM2_DEPTH_31_16)**
15:0	7E6h RO	**DWC_USB3_RAM1_DEPTH_15_0 (DWC_USB3_RAM1_DEPTH_15_0)**

25.3.18 GDBGFIFOSPACE (GDBGFIFOSPACE)—Offset C160h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 420000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	42h RO	**SPACE_AVAILABLE (SPACE_AVAILABLE)**
15:9	0h RO	Reserved.
8:0	0h RW	**FIFO_QUEUE_SELECT (FIFO_QUEUE_SELECT):** [8:5] indicates the FIFO/Queue Type [4:0] indicates the FIFO/Queue Number

25.3.19 GDBGLTSSM (GDBGLTSSM)—Offset C164h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 41010440h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30	1h RO	**RxElecidle (RxElecidle)**
29	0h RO	**X3_XS_SWAPPING (X3_XS_SWAPPING)**
28	0h RO	**X3_DS_HOST_SHUTDOWN (X3_DS_HOST_SHUTDOWN)**
27	0h RO	**PRTDIRECTION (PRTDIRECTION):** 1'b0: Upstream 1'b1: Downstream
26	0h RO	**LTDBTIMEOUT (LTDBTIMEOUT)**
25:22	4h RO	**LTDBLINKSTATE (LTDBLINKSTATE)**
21:18	0h RO	**LTDBSUBSTATE (LTDBSUBSTATE)**
17	0h RO	**ELASTICBUFFERMODE (ELASTICBUFFERMODE)**
16	1h RO	**TXELECLDLE (TXELECLDLE)**
15	0h RO	**RXPOLARITY (RXPOLARITY)**
14	0h RO	**TxDetRxLoopback (TxDetRxLoopback)**
13:11	0h RO	**LTDBPhyCmdState (LTDBPhyCmdState):** 000: PHY_IDLE 001: PHY_DET 010: PHY_DET_3 011: PHY_PWR_DLY 100: PHY_PWR_A 101: PHY_PWR_B
10:9	2h RO	**POWERDOWN (POWERDOWN)**
8	0h RO	**RXEQTRAIN (RXEQTRAIN)**
7:6	1h RO	**TXDEEMPHASIS (TXDEEMPHASIS)**
5:3	0h RO	**LTDBClkState (LTDBClkState):** 000: CLK_NORM 001: CLK_TO_P3 010: CLK_WAIT1 011: CLK_P3 100: CLK_TO_P0 101: CLK_WAIT2

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**TXSWING (TXSWING)**
1	0h RO	**RXTERMINATION (RXTERMINATION)**
0	0h RO	**TXONESZEROS (TXONESZEROS)**

25.3.20 GDBGLNMCC (GDBGLNMCC)—Offset C168h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8:0	0h RO	**LNMCC_BERC (LNMCC_BERC)**

25.3.21 GDBGBMU (GDBGBMU)—Offset C16Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**BMU_BCU (BMU_BCU)**
7:4	0h RO	**BMU_DCU (BMU_DCU)**
3:0	0h RO	**BMU_CCU (BMU_CCU)**

25.3.22 GDBGLSP (GDBGLSP)—Offset C174h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**LSPDEBUG (LSPDEBUG)**

25.3.23 GDBGEPINFO0 (GDBGEPINFO0)—Offset C178h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**EPDEBUG (EPDEBUG)**

25.3.24 GDBGEPINFO1 (GDBGEPINFO1)—Offset C17Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 800000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	800000h RO	**EPDEBUG (EPDEBUG)**

25.3.25 Global Transmit FIFO Size Register N (GTXFIFOSIZ0_0)—Offset C300h

FIFO_number: 0<= n <= 15 Offset: C300h + FIFO_number * 04h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 42h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**TXFSTADDR_N (TXFSTADDR_N)**
15:0	42h RW	**TXFDEP_N (TXFDEP_N)**

25.3.26 GRXFIFOSIZ0_0 (GRXFIFOSIZ0_0)—Offset C380h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 385h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**RXFSTADDR_N (RXFSTADDR_N)**
15:0	385h RW	**RXFDEP_N (RXFDEP_N)**

25.3.27 GEVNTADRLO_0 (GEVNTADRLO_0)—Offset C400h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**EVNTADRLO (EVNTADRLO)**

25.3.28 GEVNTADRHI_0 (GEVNTADRHI_0)—Offset C404h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**EVNTADRHI (EVNTADRHI)**

25.3.29 GEVNTCOUNT_0 (GEVNTCOUNT_0)—Offset C40Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h NA	**EVNTCOUNT (EVNTCOUNT)**

25.3.30 GTXFIFOPRIDEV (GTXFIFOPRIDEV)—Offset C610h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**gtxfifopridev (gtxfifopridev)**

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26 Shared SRAM (D20:F2)

26.1 PMC SSRAM PCI Configuration Space Registers

Table 26-1. Summary of PMC SSRAM PCI Configuration Space Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device Vendor ID (DEVVENDID)—Offset 0h	8086h
4h	7h	STATUSCOMMAND Status and Command (STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	Revision ID and Class Code (REVCLASSCODE)—Offset 8h	0h
Ch	Fh	Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch	0h
10h	13h	32-bit Base Address Register (BAR)—Offset 10h	4h
14h	17h	BAR HIGH (BAR_HIGH)—Offset 14h	0h
18h	1Bh	32-bit Base Address Register1 (BAR1)—Offset 18h	4h
1Ch	1Fh	BAR1 HIGH (BAR1_HIGH)—Offset 1Ch	0h
2Ch	2Fh	Subsystem Identifiers (SUBSYSTEMID)—Offset 2Ch	0h
34h	37h	Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	Interrupt Register (INTERRUPTREG)—Offset 3Ch	100h
80h	83h	POWER CAP ID PowerManagement Capability ID (POWERCAPID)—Offset 80h	48030001h
84h	87h	PME Control and Status (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	PCI Device Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
98h	9Bh	D0I3 CONTROL SW LTR MMIO REG (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	0h
9Ch	9Fh	Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch	0h
A0h	A3h	Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	800h
B0h	B3h	General Purpose Read Write Register1 (GEN_REGRW1)—Offset B0h	0h
B4h	B7h	General Purpose Read Write Register2 (GEN_REGRW2)—Offset B4h	0h
B8h	BBh	General Purpose Read Write Register3 (GEN_REGRW3)—Offset B8h	0h
BCh	BFh	General Purpose Read Write Register4 (GEN_REGRW4)—Offset BCh	0h
C0h	C3h	General Purpose Input Register (GEN_INPUT_REG)—Offset C0h	0h

26.1.1 Device Vendor ID (DEVVENDID)—Offset 0h

Device Vendor ID

Access Method

Type: CFG Register (Size: 32 bits)

Device: 20
Function: 2

Default: 8086h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	**Device Identification (DEVICEID):** Indicates the value assigned to the controller. Refer to Vol1 for default value.
15:0	8086h RO	**Vendor Identification (VENDORID):** Indicates Intel

26.1.2 STATUSCOMMAND Status and Command (STATUSCOMMAND)—Offset 4h

Status and Command

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 100000h

Bit Range	Default and Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW/1C	**RMA (RMA):** Received Initiator Abort
28	0h RW/1C	**RTA (RTA):** Received Target Abort
27:21	0h RO	Reserved.
20	1h RO	**CAPLIST (CAPLIST):** Capabilities List
19	0h RO	**INTR_STATUS (INTR_STATUS):** Interrupt Status
18:11	0h RO	Reserved.
10	0h RW	**INTR_DISABLE (INTR_DISABLE):** Interrupt Disable
9	0h RO	Reserved.
8	0h RW/1C	**SERR_ENABLE (SERR_ENABLE):** System Error Enable
7:3	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
2	0h RW	**BME (BME):** Bus Initiator Enable
1	0h RW	**MSE (MSE):** Memory Space Enable
0	0h RO	Reserved.

26.1.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Revison Class Codes

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	**CLASS_CODES (CLASS_CODES):** The register is read-only and is used to identify the generic function of the device.
7:0	0h RO	**RID (RID):** Indicates stepping of the controller. Refer to Vol1 for specific value.

26.1.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Cache Line Latency Header And BIST

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RO	**MULFNDEV (MULFNDEV):** 0 = Single Function Device 1 = Multi Function device

Bit Range	Default and Access	Field Name (ID): Description
22:16	0h RO	**HEADERTYPE (HEADERTYPE):** Header Type
15:8	0h RO	**LATTIMER (LATTIMER):** Hard wired to 00h.
7:0	0h RW	**CACHELINE_SIZE (CACHELINE_SIZE):** Cacheline Size

26.1.5 32-bit Base Address Register (BAR)—Offset 10h

Base Address Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:13	0h RW	**BAR (BASEADDR):** Software programs this register with the base address of the device's memory region
12:4	0h RO	**Size Indicator (SIZEINDICATOR):** Hardwired to 0 to indicate 8KB of memory space
3	0h RO	**Prefetchable (PREFETCHABLE):** Hardwired to 0 to indicate the device's memory space as notprefetchable.
2:1	2h RO	**Type (TYPE):** Hardwired to 10 to indicate that Base register is 64 bits wide and mapping can be done anywhere in the 64-bit Memory Space.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** Hardwired to 0 to identify a Memory BAR.

26.1.6 BAR HIGH (BAR_HIGH)—Offset 14h

BAR -Base Address Register High

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Base Address HIGH (BASEADDR_HIGH):** Base Address

26.1.7 32-bit Base Address Register1 (BAR1)—Offset 18h

Base Address Register1

Access Method

Type: CFG Register (Size: 32 bits)
Device: 20
Function: 2

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:12	0h RW	**BAR1 (BASEADDR1):** Software programs this register with the base address of the device's memory region
11:4	0h RO	**Size Indicator (SIZEINDICATOR1):** Hardwired to 0 to indicate 4KB of memory space
3	0h RO	**Prefetchable (PREFETCHABLE1):** Hardwired to 0 to indicate the device's memory space as notprefetchable.
2:1	2h RO	**Type (TYPE1):** Hardwired to 10 to indicate that Base register is 64 bits wide and mapping can be done anywhere in the 64-bit Memory Space.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** Hardwired to 0 to identify a Memory BAR.

26.1.8 BAR1 HIGH (BAR1_HIGH)—Offset 1Ch

BAR1 -Base Address Register High

Access Method

Type: CFG Register (Size: 32 bits)
Device: 20
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Base Address HIGH (BASEADDR1_HIGH):** Base Address

26.1.9 Subsystem Identifiers (SUBSYSTEMID)—Offset 2Ch

Subsystem Identifiers

Access Method

Type: CFG Register (Size: 32 bits)
Device: 20
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SUBSYSTEMID):** Written by BIOS. Not used by hardware.
15:0	0h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** Written by BIOS.Not used by hardware.

26.1.10 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	80h RO	**CAPPTR_POWER (CAPPTR_POWER):** Indicates what the next capability is. This capability points to the PM Capability (0x80) structure.

26.1.11 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Interrupt Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 100h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	**MAX_LAT (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**MIN_GNT (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	Reserved.
11:8	1h RO	**INTPIN (INTPIN):** Interrupt Pin
7:0	0h RW	**INTLINE (INTLINE):** Used to communicate to software the interrupt line that the interrupt pin is connected to.

26.1.12 POWER CAP ID PowerManagement Capability ID (POWERCAPID)—Offset 80h

PowerManagement Capability

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 48030001h

Bit Range	Default and Access	Field Name (ID): Description
31:27	9h RO	**PMESUPPORT (PMESUPPORT):** PME Support
26:19	0h RO	Reserved.
18:16	3h RW/1C	**VERSION (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	0h RO	**NXTCAP (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	1h RO	**POWER_CAP (POWER_CAP):** Indicates power management capability.

26.1.13 PME Control and Status (PMECTRLSTATUS)—Offset 84h

Power Management Control and Status Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C	**PMESTATUS (PMESTATUS):** PME Status
14:9	0h RO	Reserved.
8	0h RW	**PMEENABLE (PMEENABLE):** PME Enable
7:4	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
3	1h RO	**NO_SOFT_RESET (NO_SOFT_RESET):** When set, this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	Reserved.
1:0	0h RW	**POWERSTATE (POWERSTATE):** This field is used both to determine the current power state and to set a new power state.

26.1.14 PCI Device Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h

PCI DEVICE IDLE CAPABILITY RECORD

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: F0140009h

Bit Range	Default and Access	Field Name (ID): Description
31:28	Fh RO	**VEND_CAP (VEND_CAP):** Indicates this is Vendor Specific capability.
27:24	0h RO	**REVID (REVID):** Revision ID of capability structure
23:16	14h RO	**CAP_LENGTH (CAP_LENGTH):** Indicates the number of bytes in the capability structure.
15:8	0h RO	**NEXT_CAP (NEXT_CAP):** Points to the next capability structure. This points to NULL.
7:0	9h RO	**CAPID (CAPID):** Capability ID

26.1.15 D0I3 CONTROL SW LTR MMIO REG (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

SW LTR Update MMIO Location Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	**SW_LAT_DWORD_OFFSET (SW_LAT_DWORD_OFFSET):** This register contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR. The value of this register is a do not care, if the Valid bit is not set.
3:1	0h RO	**SW_LAT_BAR_NUM (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0.
0	0h RO	**SW_LAT_VALID (SW_LAT_VALID):** 0= not valid 1= valid

26.1.16 Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Device IDLE pointer register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	**DWORD_OFFSET (DWORD_OFFSET):** This register contains the location pointer to the DevIdle register in MMIO space, as an offset from the specified BAR. The value of this register is a do not care, if the Valid bit is not set.
3:1	0h RO	**BAR_NUM (BAR_NUM):** Indicates that the DevIdle update MMIO location is always at BAR0
0	0h RO	**VALID (VALID):** 0= not valid 1= valid

26.1.17 Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

DEVICE PG CONFIG

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 800h

Bit Range	Default and Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW	**HAE (HAE):** Hardware Autonomous Enable
20	0h RO	Reserved.
19	0h RW	**SLEEP_EN (SLEEP_EN):** Sleep Enable
18	0h RW	**PGE (PGE):** If clear, then the controller will never request a PG. If set, then the controller may request PG when proper conditions are met. Note: This Bit must be set by BIOs for PG to function
17	0h RW	**I3_ENABLE (I3_ENABLE):** If '1', then the function will power gate when idle and the DevIdle register (DevIdleC[2] = '1') is set.
16	0h RW	**PMCRE (PMCRE):** If this bit is set to '1', the function will power gate when idle.
15:13	0h RO	Reserved.
12:10	2h RW/O	**POW_LAT_SCALE (POW_LAT_SCALE):** Power On Latency Scale
9:0	0h RW/O	**POW_LAT_VALUE (POW_LAT_VALUE):** This value is written by BIOS to communicate to the Driver.

26.1.18 General Purpose Read Write Register1 (GEN_REGRW1)—Offset B0h

General Purpose Read Write Register1

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW1 (GEN_REG_RW1):** General Purpose PCI Register

26.1.19 General Purpose Read Write Register2 (GEN_REGRW2)—Offset B4h

General Purpose Read Write Register2

Access Method

Type: CFG Register (Size: 32 bits)
Device: 20
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW2 (GEN_REG_RW2):** General Purpose PCI Register

26.1.20 General Purpose Read Write Register3 (GEN_REGRW3)—Offset B8h

General Purpose Read Write Register3

Access Method

Type: CFG Register (Size: 32 bits)
Device: 20
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW3 (GEN_REG_RW3):** General Purpose PCI Register

26.1.21 General Purpose Read Write Register4 (GEN_REGRW4)—Offset BCh

General Purpose Read Write Register4

Access Method

Type: CFG Register (Size: 32 bits)
Device: 20
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW4 (GEN_REG_RW4):** General Purpose PCI Register

26.1.22 General Purpose Input Register (GEN_INPUT_REG)—Offset C0h

General Purpose Input Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_INPUT_RW (GEN_REG_INPUT_RW):** General Purpose Input Register

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27 CNVi Registers (D20:F3)

This chapter documents the registers in Bus: 0, Device 20, Function 3.

Note: These registers do not apply to S/H processors.

27.1 CNVi PCI Configuration Register

Table 27-1. Summary of Bus: 0, Device: 20, Function: 3 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	VEN DEV Identification (VEN_DEV_ID)	00008086h
4h	4	PCI COM Status (PCI_COM_STAT)	00100000h
8h	4	PCI CLASS CODE (PCI_CLASS_CODE)	02800000h
10h	4	BAR #0 (BAR0)	00000004h
14h	4	BAR #1 (BAR1)	00000000h
2Ch	4	SUBSYS Identification (SUBSYS_ID)	00008086h
34h	4	CAP PTR (CAP_PTR)	000000C8h
3Ch	4	Interrupt Error UPT (INTERRUPT)	00000100h
40h	4	GIO CAP (GIO_CAP)	00928010h
44h	4	GIO DEV CAP (GIO_DEV_CAP)	10000EC0h
48h	4	GIO DEV (GIO_DEV)	00100C10h
64h	4	GIO DEV CAP #2 (GIO_DEV_CAP_2)	00080812h
68h	4	GIO DEV #2 (GIO_DEV_2)	00000005h
80h	4	MSIX CAP HEAD (MSIX_CAP_HEAD)	000F0011h
84h	4	MSIX TABLE OFFSET (MSIX_TABLE_OFFSET)	00002000h
88h	4	MSIX PBA OFFSET (MSIX_PBA_OFFSET)	00003000h
C8h	4	PMC	C823D001h
CCh	4	PMCSR	0D000008h
D0h	4	MSI Message Control (MSI_MSG_CTRL)	00804005h
D4h	4	MSI LOW ADD (MSI_LOW_ADD)	00000000h
D8h	4	MSI HIGH ADD (MSI_HIGH_ADD)	00000000h
DCh	4	MSI DATA (MSI_DATA)	00000000h
100h	4	LTR EXTND CAP HEAD (LTR_EXTND_CAP_HEAD)	16410018h
104h	4	LTR Maximum SNOOP NOSNOOP LAT (LTR_MAX_SNOOP_NOSNOOP_LAT)	00000000h
10Ch	4	UNCORRECT Error SEV (UNCORRECT_ERR_SEV)	00462031h
110h	4	CORRECT Error Status (CORRECT_ERR_STAT)	00000000h
114h	4	CORRECT Error MASK (CORRECT_ERR_MASK)	00002000h
118h	4	ADVANCED Error CAP (ADVANCED_ERR_CAP)	00000000h
11Ch	4	HEADER LOG #1 (HEADER_LOG1)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
120h	4	HEADER LOG #2 (HEADER_LOG2)	00000000h
124h	4	HEADER LOG #3 (HEADER_LOG3)	00000000h
128h	4	HEADER LOG #4 (HEADER_LOG4)	00000000h

27.1.1 VEN DEV Identification (VEN_DEV_ID) — Offset 0h

identifies the manufacturer of the device(vendor) and type.(Offset 000 h)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 0h	00008086h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**DEV_ID:** Device ID identifies the particular PCI device
15:0	8086h RO	**VEN_ID:** vendor ID

27.1.2 PCI COM Status (PCI_COM_STAT) — Offset 4h

command and status register .(Offset 004 h)

HARDWIRED --]] HARDWIRED

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 4h	00100000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**DET_PAR_ERR:** Detected Parity Error
30	0h RW/1C	**SIG_SYS_ERR:** Signaled System Error
29	0h RW/1C	**REC_MAS_ABRT:** Received Initiator Abort

Bit Range	Default & Access	Field Name (ID): Description
28	0h RW/1C	**REC_TAR_ABRT:** Received Target Abort
27	0h RW/1C	**SIG_TAR_ABRT:** Signaled Target Abort
26:25	0h RO	**DEVSEL_TIMING:** DEVSEL Timing, does not apply to PCI Express HARDWIRED
24	0h RW/1C	**MAS_DATA_PAR_ER:** Initiator Data Parity Error
23	0h RO	**FAST_BTB_TCAP:** Fast Back-to-Back Transaction Capable, does not apply to PCI Express HARDWIRED
22	0h RO	**Reserved**
21	0h RO	**OLF_FREQ_CAP:** 66 MHz Capable, does not apply to PCI Express HARDWIRED
20	1h RO	**CAP_LST:** Capability List, must be set to 1
19	0h RO	**INTRPT_STS:** Interrupt status, reflects the state of the interrupt in the device
18:11	0h RO	**Reserved**
10	0h RW	**INTRPT_DIS:** Interrupt Disable, controls the ability of the device to generate legacy interrupt messages
9	0h RO	**FAST_BTB_TNSCEN:** Fast Back-to-Back Transaction Enable, does not apply to PCI Express HARDWIRED
8	0h RW	**SERR_EN:** SERR Enable, when set 1, the device can drive the SERR# line
7	0h RO	**IDSEL_STEP_W_CY:** IDSEL Stepping/Wait Cycle Control, does not apply to PCI Express HARDWIRED
6	0h RW	**PAR_ERR:** Parity Error Enable
5	0h RO	**VGA_PALT_SNOOP:** VGA Palette Snoop, does not apply to PCI Express HARDWIRED
4	0h RO	**MEM_WR_INVALD:** Memory Write and Invalidate, does not apply to PCI Express HARDWIRED
3	0h RO	**SPEC_CYC_ENB:** Special Cycle Enable, does not apply to PCI Express HARDWIRED
2	0h RW	**BUS_MAS:** Bus Initiator Enable
1	0h RW	**MEM_SP_ACC:** Memory Space access enable
0	0h RO	**IO_SPC_AC_EN_0:** IO Space access enable

27.1.3 PCI CLASS CODE (PCI_CLASS_CODE) — Offset 8h

revision identifier and class code(Offset 008 h)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 8h	02800000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:24	02h RO	**SE_CLASS:** Base Class, classifies the type of function the device perform
23:16	80h RO	**SUB_CLASS:** Sub-Class, identifies more specifically the function of the device
15:8	00h RO	**INTERFACE:** Interface, identifies a specific register-level programming interface
7:0	00h RO	**REV_ID:** Revision ID identifies the revision of particular PCI device

27.1.4 BAR #0 (BAR0) — Offset 10h

Base Address Register BAR0 Low (Offset 010 h)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 10h	00000004h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	00000h RW	**BS_ADD_FLD_RW:** Base Address Field
13:4	000h RO	**BS_ADD_FLD_RO:** Base Address Field HARDWIRED
3	0h RO	**PREFETCHBL:** Prefetchable, defines the block of memory as Prefetchable or not
2:1	2h RO	**DECOD_WDTH_FLD:** Decoder Width Field (10b-64bit reg) HARDWIRED
0	0h RO	**MEM_SPAC_INDIC:** Memory Space Indicator HARDWIRED

27.1.5 BAR #1 (BAR1) — Offset 14h

Base Address Register BAR0 High (Offset 014 h)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 14h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000 h RW	**BS_ADD_FLD:** Base Address Field

27.1.6 SUBSYS Identification (SUBSYS_ID) — Offset 2Ch

identifies the manufacturer of the device(vendor) and type.(Offset 02C h)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 2Ch	00008086h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**SB_DEV_ID:** Subsystem (device) ID
15:0	8086h RO	**SB_VEN_ID:** Subsystem Vendor ID

27.1.7 CAP PTR (CAP_PTR) — Offset 34h

capabilities pointer register (Offset 034 h)

bit [7:0] Point to the first item in the list of capabilities, provides an \n offset in the device's PCI Configuration Space for the location of the first

item in the Capabilities List

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 34h	000000C8h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	C8h RO	**CARDB_PTR:** Capabilities Pointer

27.1.8 Interrupt Error UPT (INTERRUPT) — Offset 3Ch

revision identifier and class code(Offset 03C h)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 3Ch	00000100h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**MAX_LATNC:** Max_Lat , Does not apply to PCI Express HARDWIRED
23:16	00h RO	**MIN_GNT:** Min_Gnt , Does not apply to PCI Express HARDWIRED
15:8	01h RO	**INT_PIN:** Interrupt Pin , Tells which interrupt pin the device uses
7:0	00h RW	**INT_LINE:** Interrupt Line, id which input interrupt request pin is routed.

27.1.9 GIO CAP (GIO_CAP) — Offset 40h

PCI Express Capabilities Register. (Offset 040 h)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 40h	00928010h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:25	00h RO	**INTRPT_MSG_NUM:** Interrupt Message Number HARDWIRED
24	0h RO	**SLT_IMPLNT:** Slot Implemented HARDWIRED
23:20	9h RO	**DEV_POR_TYP:** Device/Port Type
19:16	2h RO	**CAP_VER:** Capability Version
15:8	80h RO	**GIO_CAP_NXT_OFS:** The offset to the next PCI capability structure HARDWIRED
7:0	10h RO	**INCD_PCIE_CST:** indicates PCI Express Capability Structure HARDWIRED

27.1.10 GIO DEV CAP (GIO_DEV_CAP) — Offset 44h

The Device Capabilities register identifies PCI Express device specific capabilities.(Offset 044 h)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 44h	10000EC0h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	1h RO	**FUNC_LVL_RES:** Function Level Reset Capability [too add GEN_2]
27:26	0h RO	**SLT_PW_LSCL:** Captured Slot Power Limit Scale
25:18	00h RO	**SLT_PW_LVAL:** Captured Slot Power Limit Value

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RO	**Reserved**
15	0h RO	**ROLE_BASED_ERR:** This field indicates that the device support Error reporting
14:12	0h RO	**Reserved**
11:9	7h RO	**L1_ACC_LAT:** Endpoint L1 Acceptable Latency
8:6	3h RO	**L0S_ACC_LAT:** Endpoint L0s Acceptable Latency
5	0h RO	**EX_TAG_FIELD:** Extended Tag Field Supported
4:3	0h RO	**PHAN_FUNCS:** Phantom Functions Supported
2:0	0h RO	**MAX_PL_SIZE:** Max_Payload_Size Supported

27.1.11 GIO DEV (GIO_DEV) — Offset 48h

Device Control Register. (Offset 048 h)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 48h	00100C10h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RO	**TRANS_PEND:** indicates that a device has Non-Posted Requests which have not been completed
20	1h RO	**AUX_P_DET:** device that requires AUX power reports this bit (asynch signal)
19	0h RW/1C	**UNSOP_REQ_DET:** indicates that the device received Unsupported Request
18	0h RW/1C	**FAT_ERR_DET:** indicates status of fatal errors detected
17	0h RW/1C	**NFAT_ER_DET:** indicates status of non-fatal errors detected
16	0h RW/1C	**COR_ERR_DET:** indicates status of correctable errors detected

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**INIT_FNC_LV_RS:** Initiate Function Level Reset - A write of 1b initiates Function (init FLR) this bit is RW after gf_cfg_dev_cap_flr_sup is set from OTP
14:12	0h RW	**MAX_RDRQ_SIZE:** sets the maximum Read Request size
11	1h RW	**EN_NO_SNOOP:** Enable No Snoop (if set device is permitted to set No Snoop bit)
10	1h RW	**AUX_PM_EN:** Auxiliary (AUX) Power PM Enable. sticky value.
9	0h RO	**Reserved**
8	0h RO	**IO_SPC_AC_EN_8:** IO Space access enable
7:5	0h RW	**MAX_PAY_SIZE:** sets maximum TLP payload size for the device functions
4	1h RW	**EN_REL_ORD:** when set device permitted to set the Relaxed Ordering bit
3	0h RW	**UNSOP_REQ_REP:** enables reporting of Unsupported Request when set
2	0h RW	**FAT_ERR_REP:** controls reporting of fatal errors
1	0h RW	**NFAT_ER_REP:** controls reporting of non-fatal errors
0	0h RW	**COR_ERR_REP:** controls reporting of correctable errors

27.1.12 GIO DEV CAP #2 (GIO_DEV_CAP_2) — Offset 64h

device control 2 (and status) register. (Offset 064 h)

new at Wilkins2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 64h	00080812h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:18	2h RO	**OBFF_MEC_SUP:** OBFF suported : 0x00 -unsupported , 0x01 -sup using message signaling A, 0x10 -sup using signaling B ,0x11-supported using WAKE signaling

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RO	**Reserved**
11	1h RO	**LTR_MEC_SUP:** LTR Mechanism Supported - a value of 1b indicates support for LTR.
10:5	0h RO	**Reserved**
4	1h RO	**CMP_TO_DIS_SUP:** 1- support for the Completion Timeout Disable, 0- not supported hardwired to 0x1
3:0	2h RO	**CMP_TO_RNG_SUP:** Completion Timeout Ranges Supported hardwired to 0x2

27.1.13 GIO DEV #2 (GIO_DEV_2) — Offset 68h

device control (and status) register. (Offset 068 h)

spec section:7.8.16 new at Wilkins2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 68h	00000005h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14:13	0h RW	**OBFF_MEC_ENA:** OBFF enable: 0x00 -disable , 0x01 - enabled using message signaling A, 0x10 - message signaling B ,0x11-enabled using WAKE signaling
12:11	0h RO	**Reserved**
10	0h RW	**LTR_MEC_EN:** LTR Mechanism Enable - When Set enables the LTR.
9:5	0h RO	**Reserved**
4	0h RW	**CMP_TO_DIS:** When Set, this bit disables the Completion Timeout mechanism
3:0	5h RW	**CMP_TO_VAL:** this field allows system SW to modify the Completion Timeout value

27.1.14 MSIX CAP HEAD (MSIX_CAP_HEAD) — Offset 80h

MSIX Capability .(Offset 080 h)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 80h	000F0011h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**MSIX_ENABLE:** If set to 1, the function is permitted to use MSI-X to request service. System configuration software sets this bit to enable MSI-X. A device driver is prohibited from writing this bit to mask a function's service request. If 0, the function is prohibited from using MSI-X to request service.
30	0h RW	**FUN_MASK:** If set to 1, all of the vectors associated with the function are masked, regardless of their per-vector Mask bit states. If 0, each vector's Mask bit determines whether the vector is masked or not. Setting or clearing the MSI-X Function Mask bit has no effect on the state of the per-vector Mask bits
29:27	0h RO	**Reserved**
26:16	00Fh RO	**TABLE_SIZE:** System software reads this field to determine the MSI-X Table Size N, which is encoded as (N-1). Wifi Host supports Table Size of 16 and encodes a number of 15 (Pulsar).
15:8	00h RO	**NEXT_PTR:** Pointer to the next item in the capabilities list. NULL if last
7:0	11h RO	**MSIX_CAP_ID:** The value of 11h in this field identifies the function as being MSI-X capable.

27.1.15 MSIX TABLE OFFSET (MSIX_TABLE_OFFSET) — Offset 84h

MSIX Capability Structure - Table Offset Reg.(Offset 084 h)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 84h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000400h RO	**TABLE_OFFSET:** Used as an offset from the address contained by the Base Address register to point to the base of the MSI-X Table. The lower 3 bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset. In Wifi Host the table is at 0x2000, so the value of this field in 0x400.

Bit Range	Default & Access	Field Name (ID): Description
2:0	0h RO	**TABLE_BIR:** Indicates which one of a function's Base Address registers, located beginning at 10h in configuration Space, and is used to map the function's MSI-X Table into Memory Space. Wifi Host cluster uses a single BAR to point to the MSI-X structures.

27.1.16 MSIX PBA OFFSET (MSIX_PBA_OFFSET) — Offset 88h

MSIX Capability Structure - Pending Bit Array Offset Reg.(Offset 088 h)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 88h	00003000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000600h RO	**TABLE_OFFSET:** Used as an offset from the address contained by the Base Address register to point to the base of the MSI-X PBA Table. The lower 3 bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset. In Wifi Host the table is at 0x3000, so the value of this field in 0x600.
2:0	0h RO	**TABLE_BIR:** Indicates which one of a function's Base Address registers, located beginning at 10h in configuration Space, and is used to map the function's MSI-X Table into Memory Space. Wifi Host cluster uses a single BAR to point to the MSI-X structures.

27.1.17 PMC — Offset C8h

Power Management Capabilities Register(Offset 0C8 h)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + C8h	C823D001h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:27	19h RO	**PME_SUPRT:** PME Support,indicates the power states in which the device may assert PME

Bit Range	Default & Access	Field Name (ID): Description
26	0h RO	**D2_PWR_MANG:** D2 Power Management State support
25	0h RO	**D1_PWR_MANG:** D1 Power Management State support
24:22	0h RO	**AUX_CUR:** AUX Current (Used data register instead)
21	1h RO	**DEV_SPC_INT:** Device Specific Initialization
20	0h RO	**Reserved**
19	0h RO	**PME_CLK:** PME Clock, does not apply to PCI Express HARDWIRED
18:16	3h RO	**VERSION:** value indicates that this function complies with the Revision 1.2
15:8	D0h RO	**PMC_NXT_PTR:** Next PTR, pointing to the location of next item in the functions capability list HARDWIRED
7:0	01h RO	**PMC_CAP_ID:** Capability ID, Indicates the linked list item is the PCI Power Management Registers HARDWIRED

27.1.18 PMCSR — Offset CCh

Power Management Status and Control (Offset 0CC h)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + CCh	0D000008h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0Dh RO	**PWR_DIS_CON:** used to report power consumption and heat dissipation
23	0h RO	**BUS_PWR_CLK_CEN:** Bus Power/Clock Control Enable, does not apply to PCI Express HARDWIRED
22	0h RO	**B2_B3_SUPRT:** B2/B3 Support, does not apply to PCI Express HARDWIRED
21:16	0h RO	**Reserved**
15	0h RW/1C	**PME_STAT:** This bit reflects whether the function has experienced a PME. sticky value.

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RO	**DAT_SCALE:** Data Scale
12:9	0h RW	**DAT_SEL:** Data Select, selects the data value to be viewed through the Data register
8	0h RW	**PME_ENA:** PME Enable. sticky value.
7:4	0h RO	**Reserved**
3	1h RO	**NO_SOFT_RESET:** No_Soft_Reset
2	0h RO	**Reserved**
1:0	0h RW	**PWR_STATE:** Power State

27.1.19 MSI Message Control (MSI_MSG_CTRL) — Offset D0h

Capability ID and Message Control .(Offset 0D0 h)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + D0h	00804005h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	1h RO	**BITA_CAP_64:** 64 bit address capable HARDWIRED
22:20	0h RO	**MUL_MSG_ENB:** Multiple Message Enable HARDWIRED
19:17	0h RO	**MUL_MSG_CAP:** Multiple Message Capable HARDWIRED
16	0h RW	**MSI_ENA:** function is enabled to use MSI to request service and is forbidden to use its interrupt pin
15:8	40h RO	**MSI_MC_NXT_PTR:** Next Capability ponter offset new at Wilkins2 HARDWIRED
7:0	05h RO	**MSI_MC_CAP_ID:** Capability ID HARDWIRED

27.1.20 MSI LOW ADD (MSI_LOW_ADD) — Offset D4h

Specifies the lower DWORD of the address for the MSI memory write transaction (Offset 0D4 h)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + D4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000 h RW	**MSG_ADD_LOW:** ower DWORD of the address
1:0	0h RO	**MSI_LOW_AD_1_0:** HARDWIRED

27.1.21 MSI HIGH ADD (MSI_HIGH_ADD) — Offset D8h

Specifies the upper DWORD of the address for the MSI memory write transaction (Offset 0D8 h)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + D8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000 h RW	**MSG_ADD_UP:** upper DWORD of the address

27.1.22 MSI DATA (MSI_DATA) — Offset DCh

Written by the system to indicate the lower 16 bits of the data written in the MSI memory write DWORD transaction (Offset 0DC h)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + DCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**MSG_DATA:** data written in the MSI memory write DWORD transaction

27.1.23 LTR EXTND CAP HEAD (LTR_EXTND_CAP_HEAD) — Offset 100h

header of LTR extended capability reg .(Offset 100 h, in Pulsar it was 14C h)

new at Wilkins2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 100h	16410018h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:20	164h RO	**LTR_HD_NXT_PTR:** Next Capability Offset. next is the Vendor Specific Capability Header
19:16	1h RO	**LTR_HD_CAP_VER:** Capability Version. must be 1 for this version
15:0	0018h RO	**LTR_HD_CAP_ID:** PCI Express Extended Capability ID for the LTR Extended Capability is 0018h

27.1.24 LTR Maximum SNOOP NOSNOOP LAT (LTR_MAX_SNOOP_NOSNOOP_LAT) — Offset 104h

this register specifies the maximum nosnoop latency that a device is permitted to request. (Offset 104 h)

new at Wilkins2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 104h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:26	0h RW	**NSNP_MX_LAT_SCL:** no-snoop max latency scale. set by SW
25:16	000h RW	**NSNP_MX_LAT_VAL:** no-snoop max latency value. set by SW
15:13	0h RO	**Reserved**
12:10	0h RW	**SNP_MAX_LAT_SCL:** snoop max latency scale. set by SW
9:0	000h RW	**SNP_MAX_LAT_VAL:** snoop max latency value. set by SW

27.1.25 UNCORRECT Error SEV (UNCORRECT_ERR_SEV) — Offset 10Ch

Uncorrectable Error severity Register. (Offset 10C h)

at this reg bits of type RWS - the error is reported as fatal when the field is set to 1, g if it is cleared to 0, the error is considered non-fatal

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 10Ch	00462031h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RW	**TLP_PRFIX_BLOCKED_SVR:** TLP Prefix Blocked Error Severity (Optional) - report is not implemented. sticky value
24	0h RW	**ATMC_EGRS_BLOCKED_SVR:** AtomicOps Egress Blocked Severity (Optional) - report is not implemented. sticky value

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**MC_BLOCKED_TLP_SVR:** MC Blocked TLP Severity (Optional) - report is not implemented. sticky value
22	1h RW	**UNCORCT_INT_ERR_SVR:** Uncorrectable Internal Error Severity (Optional) - report is not implemented. sticky value
21	0h RW	**ACS_VIOL_SVR:** ACS Violation Severity (Optional) - report is not implemented. sticky value
20	0h RW	**UNSPR_REQ_ERR_SVR:** Unsupported Request Error severity sticky value
19	0h RO	**ECRC_ERR_SVR_19:** ECRC Error severity, is not implemented.
18	1h RW	**MAL_TLP_SVR:** Malformed TLP severity . sticky value
17	1h RW	**REC_OVRF_SVR:** Receiver Overflow severity . sticky value
16	0h RW	**UNXPL_COM_SVR:** Unexpected Completion severity . sticky value
15	0h RW	**COM_AB_SVR:** Completer Abort severity . sticky value
14	0h RW	**COM_TO_SVR:** Completion Timeout severity. sticky value
13	1h RW	**FLWCNT_PR_SVR:** Flow Control Protocol Error severity. sticky value
12	0h RW	**POIS_TLP_SVR:** Poisoned TLP severity . sticky value
11:6	0h RO	**Reserved**
5	1h RW	**SURPRISE_DWN_SVR:** Surprise Down Error Severity (Optional) . sticky value
4	1h RW	**DLNK_PRERR_SVR:** Data Link Protocol Error severity . sticky value
3:1	0h RO	**Reserved**
0	1h RO	**TRNG_ERR_SVR_0:** Training Error severity

27.1.26 CORRECT Error Status (CORRECT_ERR_STAT) — Offset 110h

PCI Express Capabilities Register. (Offset 110 h)

at this reg bits of type RW1CS - , if is set to 1 indicates that the error occurred; g software may clear the bit by writing a 1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 110h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RW	**ADV_NON_FATAL:** Advisory Non Fatal Error
12	0h RW/1C	**REPL_TO_ST:** Replay Timer Timeout Error status . sticky value
11:9	0h RO	**Reserved**
8	0h RW/1C	**REPL_ROLVR_ST:** REPLAY_NUM Rollover status . sticky value
7	0h RW/1C	**BD_DLLP_ST:** Bad DLLP status . sticky value
6	0h RW/1C	**BD_TLP_ST:** Bad TLP status . sticky value
5:1	0h RO	**Reserved**
0	0h RW/1C	**REV_ERR_ST:** Receiver Error status . sticky value

27.1.27 CORRECT Error MASK (CORRECT_ERR_MASK) — Offset 114h

PCI Express Capabilities Register. (Offset 114 h)

at this reg bits of type RWS - if set to 1 the error is masked and not reported.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 114h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	1h RW	**ADV_NON_FATAL:** Advisory Non Fatal Error -- masked by default
12	0h RW	**REPL_TO_MSK:** Replay Timer Timeout Error mask . sticky value
11:9	0h RO	**Reserved**
8	0h RW	**REPL_ROLVR_MSK:** REPLAY_NUM Rollover mask . sticky value
7	0h RW	**BD_DLLP_MSK:** Bad DLLP mask . sticky value
6	0h RW	**BD_TLP_MSK:** Bad TLP mask . sticky value
5:1	0h RO	**Reserved**
0	0h RW	**REV_ERR_MSK:** Receiver Error mask . sticky value

27.1.28 ADVANCED Error CAP (ADVANCED_ERR_CAP) — Offset 118h

Advanced Error Capabilities and Control register. (Offset 118 h)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 118h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RO	**ECRC_CHK_EN:** ECRC Check Enable, if set enables ECRC checking

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**ECRC_CHK_CP:** ECRC Check Capable, indicates the device is capable of checking ECRC
6	0h RO	**ECRC_GEN_EN:** ECRC Generation Enable, if set enables ECRC generation
5	0h RO	**ECRC_GEN_CP:** ECRC Generation Capable, indicates that the device is capable of generation ECRC
4:0	00h RO	**FRST_ERR_PNT:** error reported in the Uncorrectable Error Status register First Error Pointer, identifies bit position of the first

27.1.29 HEADER LOG #1 (HEADER_LOG1) — Offset 11Ch

captures the header of TLP associated with error. (Offset 11C h)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 11Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**HEADER_LOG_1:** captures the header of TLP associated with error

27.1.30 HEADER LOG #2 (HEADER_LOG2) — Offset 120h

captures the header of TLP associated with error. (Offset 120 h)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 120h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**HEADER_LOG_2:** captures the header of TLP associated with error

27.1.31 HEADER LOG #3 (HEADER_LOG3) — Offset 124h

captures the header of TLP associated with error. (Offset 124 h)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 124h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**HEADER_LOG_3:** captures the header of TLP associated with error

27.1.32 HEADER LOG #4 (HEADER_LOG4) — Offset 128h

captures the header of TLP associated with error. (Offset 128 h)

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:20, F:3] + 128h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
R	R	R

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**HEADER_LOG_4:** captures the header of TLP associated with error

28 Integrated Sensor Hub (ISH) (D18:F0)

28.1 ISH PCI Configuration Registers

Table 28-1. Summary of ISH PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device ID and Vendor ID (DEVVENDID)—Offset 0h	22D88086h
4h	7h	Status and Command (STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	Revision ID and Class Code (REVCLASSCODE)—Offset 8h	6h
Ch	Fh	Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch	800000h
10h	13h	Base Address Register (BAR)—Offset 10h	4h
14h	17h	Base Address Register High (BAR_HIGH)—Offset 14h	0h
18h	1Bh	Base Address Register1 (BAR1)—Offset 18h	0h
1Ch	1Fh	Base Address Register1 High (BAR1_HIGH)—Offset 1Ch	0h
2Ch	2Fh	Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch	0h
34h	37h	Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	Interrupt Register (INTERRUPTREG)—Offset 3Ch	0h
80h	83h	PowerManagement Capability ID (POWERCAPID)—Offset 80h	48039001h
84h	87h	Power Management Control and Status (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	PCI Device Idle Vendor Capability (PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
98h	9Bh	Software LTR Update MMIO Location (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	0h
A0h	A3h	D0i3 And Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	80800h

28.1.1 Device ID and Vendor ID (DEVVENDID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 18
Function: 0

Default: 22D88086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	22D8h RO/P	**Device Identification (DEVICEID):** This is a 16-bit value assigned to the PCH ISH.
15:0	8086h RO	**Vendor Identification (VENDORID):** This is a 16-bit value assigned to Intel. Intel VID = 8086h

28.1.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 18
Function: 0

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW/1C	**Received Initiator Abort (RMA)**
28	0h RW/1C	**Received Target Abort (RTA)**
27:21	0h RO	Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Indicates that the controller contains a capabilities pointer list
19	0h RO	**Interrupt Status: (INTR_STATUS):** This bit reflects state of interrupt in the device
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE)**
9	0h RO	Reserved.
8	0h RW	**SERR Enable (SERR_ENABLE):** Not implemented
7:3	0h RO	Reserved.
2	0h RW	**Bus Initiator Enable (BME)**
1	0h RW	**Memory Space Enable (MSE):** 0 = Disables memory mapped configuration space. 1 = Enables memory mapped configuration space
0	0h RO	Reserved.

28.1.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 18
Function: 0

Default: 6h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Class Code (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	6h RO/P	**Revision ID (RID):** Revision ID identifies the revision of particular PCI device.

28.1.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Cache Line size as RW with def 0 Latency timer RW with def 0 Header type with Type 0 configuration header and Reserved BIST register

Access Method

Type: CFG Register (Size: 32 bits)

Device: 18
Function: 0

Default: 800000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	1h RO	**Multi-Function Device (MULFNDEV)**
22:16	0h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header
15:8	0h RO	**Latency Timer (LATTIMER)**
7:0	0h RW/P	**Cache Line Size (CACHELINE_SIZE)**

28.1.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 18
Function: 0

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**Base Address (BASEADDR):** Provides system memory base address.
11:4	0h RO	**Size Indicator (SIZEINDICATOR):** Always returns. 0 The size of this register depends on the size of the memory space
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable
2:1	2h RO	**Type (TYPE):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0 indicates this BAR is present in the memory space.

28.1.6 Base Address Register High (BAR_HIGH)—Offset 14h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 18
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Base Address high (BASEADDR_HIGH)**

28.1.7 Base Address Register1 (BAR1)—Offset 18h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 18
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**Base Address 1 (BASEADDR1):** Base Address1 This field is present if BAR1 is enabled through private configuration space.
11:4	0h RO	**Size Indicator (SIZEINDICATOR1):** Always is 0 as minimum size is 4K
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0 Indicates this BAR is present in the memory space.

28.1.8 Base Address Register1 High (BAR1_HIGH)—Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1 register is 10

Access Method

Type: CFG Register (Size: 32 bits)
Device: 18
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Base Address 1 High (BASEADDR1_HIGH)**

28.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

SVID register along with SID register is to distinguish subsystem from another

Access Method

Type: CFG Register (Size: 32 bits)
Device: 18
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O/P	**Subsystem ID (SUBSYSTEMID):** This register is implemented for any function that can be instantiated more than once in a given system.
15:0	0h RW/O/P	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register must be implemented for any function that can be instantiated more than once in a given system

28.1.10 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 18
Function: 0

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	80h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is.

28.1.11 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 18
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Max Latency (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**Min Latency (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers // Re-Check Desc Padma
15:12	0h RO	Reserved.
11:8	0h RO	**Interrupt Pin (INTPIN)**
7:0	0h RW/P	**Interrupt Line (INTLINE):** It is used to communicate to software, the interrupt line to which the interrupt pin is connected

28.1.12 PowerManagement Capability ID (POWERCAPID)—Offset 80h

PowerManagement Capability ID register points to next capability structure and power mgmnt capability with Power management capabilities register for PME support and version

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 18
Function: 0

Default: 48039001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	9h RO	**PME Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	90h RO	**Next Capability (NXTCAP):** Points to the next capability structure.
7:0	1h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

28.1.13 Power Management Control and Status (PMECTRLSTATUS)—Offset 84h

power management control and status register to set and read PME status PME enable No Soft reset and power state

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 18
Function: 0

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C/P	**PME Status (PMESTATUS)**
14:9	0h RO	Reserved.
8	0h RW/P	**PME Enable (PMEENABLE)**
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	0h RO	Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state and to set a new power state.

28.1.14 PCI Device Idle Vendor Capability (PCIDEVIDLE_CAP_RECORD)—Offset 90h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 18
Function: 0

Default: F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision IDField (REVID):** Revision ID of capability structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	0h RO	**Next Capability Field (NEXT_CAP):** Next Capability
7:0	9h RO	**Capability ID Field (CAPID):** Capability ID

28.1.15 Software LTR Update MMIO Location (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 18
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**SW LTR Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR BAR Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**SW LTR Valid Field (SW_LAT_VALID):** This value is reflected from the SW LTR valid strap at the top level

28.1.16 D0i3 And Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 18
Function: 0

Default: 80800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW/P	**HAE Field (HAE):** Hardware Autonomous Enable
20	0h RO	Reserved.
19	1h RW/P	**Sleep Enable Field (SLEEP_EN):** Sleep Enable
18	0h RW/P	**D3 Hen Field (D3HEN):** DEVIDLE Enable (DEVIDLEN): If 1 then the function will power gate when idle and the DevIdle register (DevIdleC[2] = 1) is set.
17	0h RW/P	**Device Idle En Field (DEVIDLEN):** PMCRE: PMC Request Enable
16	0h RW/P	**PMC Request Enable Field (PMCRE):** D3-Hot Enable (D3HEN): If 1 then function will power gate when idle and the PMCSR[1:0] register in the function = 11 (D3).
15:13	0h RO	Reserved.
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** Power On Latency Scale
9:0	0h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** Power On Latency value

28.2 ISH MMIO Registers

Table 28-2. Summary of ISH MMIO Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
34h	37h	ISH Host Firmware Status (ISH_HOST_FWSTS)—Offset 34h	0h
38h	3Bh	Host Communication (HOST_COMM)—Offset 38h	0h
48h	4Bh	Inbound Doorbell Host To ISH (HOST2ISH_DOORBELL)—Offset 48h	0h
54h	57h	Outbound Doorbell ISH to Host (ISH2HOST_DOORBELL)—Offset 54h	0h
60h	63h	Outbound ISH to Host Message (ISH2HOST_MSG1)—Offset 60h	0h
E0h	E3h	Inbound Host to ISH Message (HOST2ISH_MSG1)—Offset E0h	0h
360h	363h	Remap 0 (REMAP0)—Offset 360h	0h
364h	367h	REMAP 1 (REMAP1)—Offset 364h	0h
368h	36Bh	REMAP 2 (REMAP2)—Offset 368h	0h
36Ch	36Fh	REMAP 3 (REMAP3)—Offset 36Ch	0h
6D0h	6D3h	D0I3 Control (IPC_d0i3C_reg)—Offset 6D0h	8h

28.2.1 ISH Host Firmware Status (ISH_HOST_FWSTS)—Offset 34h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**ISH_HOST_FWSTS:** This is a 32 bit register which is set to 0x0000 on a system reset or a wakeup from D3Cold. As the firmware comes up after the reset or power cycle it sets bits of this register to indicate its status.

28.2.2 Host Communication (HOST_COMM)—Offset 38h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**HOST_COMM:** Host communication register.

28.2.3 Inbound Doorbell Host To ISH (HOST2ISH_DOORBELL)—Offset 48h

Inbound doorbell register, Host core to interrupt ISH. Data 30:0 is 31bits message payload used for backward compatibility. Software can use either this 31bit message payload or 256bit payload registers. When software writes the message in to respective message register, it should set bit 31(BUSY Bit) of doorbell register to indicate that new data is written. The ISH will assert a level sensitive interrupt to the IOAPIC as long as the BUSY bit is set. When the ISH reads the message code from this register it should write back to this register and clear the BUSY bit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**BUSY:** When this bit is cleared, the ISH CPU is Ready to accept a new message.
30:0	0h RW	**PAYLOAD_31BIT:** 31bits message payload for backward compatibility.

28.2.4 Outbound Doorbell ISH to Host (ISH2HOST_DOORBELL)—Offset 54h

Outbound doorbell register for the ISH to interrupt the Host. Setting bit 31 of this register causes the Host to receive a IRQn interrupt. Data 30:0 is 31bits message payload used for backward compatibility. Software can use either this 31bit message payload or 256bit payload registers. The ISH will set bit 31 of this reg to ring the doorbell after it has completed programming the message to Host. When the Host reads the message code from this register it should write back to this register and clear the BUSY bit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**BUSY:** When this bit is cleared, the HOST CPU is Ready to accept a new message.
30:0	0h RW	**PAYLOAD_31BIT:** 31bits message payload for backward compatibility.

28.2.5 Outbound ISH to Host Message (ISH2HOST_MSG1)—Offset 60h

Inter-process Message registers for ISH core to communicate to the HOST. These are eight 32bit registers that hold the message payload from the ISH to Host. These registers are meant to be written by the ISH and read by Host. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**MSG:** Message from ISH to HOST.

28.2.6 Inbound Host to ISH Message (HOST2ISH_MSG1)—Offset E0h

Inter-process Message registers for Host to communicate to the ISH. These are eight 32bit registers that hold the message payload from the Host to ISH. These registers are meant to be written by the Host and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**MSG:** Message from HOST to ISH.

28.2.7 Remap 0 (REMAP0)—Offset 360h

Remap register for Host to communicate addresses to ISH.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**REMAP0:** REMAP0.

28.2.8 REMAP 1 (REMAP1)—Offset 364h

Remap register for Host to communicate addresses to ISH.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**REMAP1:** REMAP1.

28.2.9 REMAP 2 (REMAP2)—Offset 368h

Remap register for Host to communicate addresses to ISH.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**REMAP2:** REMAP2.

28.2.10 REMAP 3 (REMAP3)—Offset 36Ch

Remap register for Host to communicate addresses to ISH.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**REMAP3:** REMAP3.

28.2.11 D0I3 Control (IPC_d0i3C_reg)—Offset 6D0h

This is a 32 bit register which is set to 0 on a system reset or a wakeup from D3Cold. When ME writes to any of these bits with 1, an interrupt is generated. The Interrupt is then cleared by writing 1`b1 to this register after the appropriate ISR is serviced.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved (RESERVED0):** D0i3 register for storing power related information.
4	0h RO	Reserved.
3	1h RW/1C	**Resetore Required (RR):** D0i3 register for storing power related information.
2	0h RW	**D0i3 (D0i3):** D0i3 register for storing power related information.
1	0h RW	**Interrupt Required (IR):** D0i3 register for storing power related information.
0	0h RW/1C	**Command In Progress (CIP):** D0i3 register for storing power related information.

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29 Touch Host Controller (THC) Interface (D16:F6-F7)

29.1 Touch Host Controller (D16:F6 and D16:F7) Registers

Table 29-1. Summary of Touch Host Controller (D16:F6 and D16:F7) Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device ID and Vendor ID (THC_CFG_DID_VID)—Offset 0h	XXXX8086h
4h	7h	Status and Command (THC_CFG_STS_CMD)—Offset 4h	2900000h
8h	Bh	Revision ID and Class Code (THC_CFG_CC_RID)—Offset 8h	90100XXh
Ch	Fh	BIST_Header Type_Latency Timer_Cache Line Size (THC_CFG_BIST_HTYPE_LT_CLS)—Offset Ch	800000h
10h	13h	THC BAR0 MMIO Low (THC_CFG_BAR0_LOW)—Offset 10h	4h
14h	17h	THC BAR0 MMIO High (THC_CFG_BAR0_HI)—Offset 14h	0h
2Ch	2Fh	Subsystem and Vendor ID (THC_CFG_SID_SVID)—Offset 2Ch	0h
34h	37h	Capability List Pointer (THC_CFG_CAPP)—Offset 34h	50h
3Ch	3Fh	Interrupt Configuration (THC_CFG_INT)—Offset 3Ch	0h
40h	43h	THC Unsupported Request Status (THC_CFG_UR_STS_CTL)—Offset 40h	0h
50h	53h	MSI Message Control_ Next Pointer and Capability ID (THC_CFG_MSIMC_MSINP_MSICID)—Offset 50h	807005h
54h	57h	MSI Message Address (THC_CFG_MSIMA)—Offset 54h	0h
58h	5Bh	MSI Message Upper Address (THC_CFG_MSIMUA)—Offset 58h	0h
5Ch	5Fh	MSI Message Data (THC_CFG_MSIMD)—Offset 5Ch	0h
70h	73h	PCI Power Management Capability (THC_CFG_PMCAP_PMNP_PMCID)—Offset 70h	C0030001h
74h	77h	PCI Power Management Control and Status (THC_CFG_PMD_PMCSRBSE_PMCSR)—Offset 74h	8h
90h	93h	Device Idle Capability (THC_CFG_DEVIDLE)—Offset 90h	F0140009h
94h	97h	Vendor Specific Header (THC_CFG_VSHDR)—Offset 94h	1400010h
98h	9Bh	SW LTR Pointer Register (THC_CFG_SWLTRPTR)—Offset 98h	0h
9Ch	9Fh	Device Idle Pointer Register (THC_CFG_DEVIDLEPTR)—Offset 9Ch	101h
A0h	A3h	Device Idle Power On Latency (THC_CFG_DEVIDLEPOL)—Offset A0h	800h
A4h	A7h	Power Control Enables (THC_CFG_PCE)—Offset A4h	8h

29.1.1 Device ID and Vendor ID (THC_CFG_DID_VID)—Offset 0h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 16
Function: 6

Default: XXXX8086h

Bit Range	Default and Access	Field Name (ID): Description
31:16	-- RO/V	**Device Identification (DID):** This is a 16-bit value assigned to the controller. Refer the Device and Revision ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor Identification (VID):** This field identifies the manufacturer of the device. Valid vendor identifiers are allocated by the PCI SIG to ensure uniqueness. 0x8086 indicates Intel

29.1.2 Status and Command (THC_CFG_STS_CMD)—Offset 4h

This is a standard PCI config register. Refer the PCI spec for bit descriptions.

Access Method

Type: CFG Register (Size: 32 bits)

Device: 16
Function: 6

Default: 2900000h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW/1C/V	**Detected Parity Error (DPE):** Refer the PCI spec.
30	0h RW/1C/V	**Signaled System Error (SSE):** Refer the PCI spec.
29	0h RW/1C/V	**Received Initiator Abort (RMA):** Refer the PCI spec
28	0h RW/1C/V	**Received Target Abort (RTA):** Refer the PCI spec
27	0h RW/1C/V	**Signaled Target Abort (STA):** Refer the PCI spec
26:25	1h RO	**Devsel Timing (DEVT):** Refer the PCI spec
24	0h RW/1C/V	**Initiator Data Parity Error (MDPE):** Refer the PCI spec
23	1h RO	**Fast Back to Back Capable (FBTBC):** Has no meaning on the internalbackbone
22	0h RO	Reserved.
21	0h RO	**66 Mhz Capable (MCAP):** Not 66 MHz capable device. Has no meaning on the internal backbone.
20	1h RO	**Capablities List (CAPL):** Refer the PCI spec
19	0h RO/V	**Interrupt Status (INTS):** Refer the PCI spec
18:11	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
10	0h RW	**Interrupt Disable (INTD):** Refer the PCI spec
9	0h RO	**Fast Back to Back Enable (FBTBEN):** Refer the PCI spec
8	0h RW	**System Error Enable (SERREN):** Refer the PCI spec
7	0h RO	Reserved.
6	0h RW	**Parity Error Response (PERRR):** Refer the PCI spec
5	0h RO	**VGA Palette Snoop (VGAPS):** Refer the PCI spec
4	0h RO	**Memory Write and Invalidate Enable (MWRIEN):** Refer the PCI spec
3	0h RO	**Special Cycles (SPCYC):** Refer the PCI spec
2	0h RW	**Bus Initiator Enable (BME):** Refer the PCI spec
1	0h RW	**Memory Space Enable (MSE):** Refer the PCI spec
0	0h RO	**IO Space Enable (IOSE):** Refer the PCI spec

29.1.3 Revision ID and Class Code (THC_CFG_CC_RID)—Offset 8h

Revision ID and Class Code

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 90100XXh

Bit Range	Default and Access	Field Name (ID): Description
31:24	9h RW/O	**Base Class Code (BCC):** Input Device. It is a requirement that this can be programmed by BIOS following a Host reset.
23:16	1h RW/O	**Sub-Class Code (SCC):** 01h= Digitizer. It is a requirement that this can be programmed by BIOS following a Host reset.
15:8	0h RW/O	**Programming Interface (PI):** 00h = Touch Host Controller that conforms to this specification.
7:0	-- RO/V	**Revision ID (RID):** Indicates the part revision. This will reset to 0 but will overridden by the SetID IOSF-SB message during the power-up sequence.

29.1.4 BIST_Header Type_Latency Timer_Cache Line Size (THC_CFG_BIST_HTYPE_LT_CLS)—Offset Ch

BIST_Header Type, Latency Timer, Cache Line Size

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 800000h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	1h RO/V	**Multi-function Device (MFD):** See the PCI spec. The default value is from the top level parameter THC_PCI_MFD. (Note: Onesource does not support parameter for the reset value. SO the parameter need to be added to RTL/RDL directly.)
22:16	0h RO	**Header Type (HTYPE):** See the PCI spec.
15:8	0h RO	**Latency Timer (LT):** See the PCI spec.
7:0	0h RO	**Cacheline Size (CLSZ):** See the PCI spec.

29.1.5 THC BAR0 MMIO Low (THC_CFG_BAR0_LOW)—Offset 10h

Attributes and lower address bits of base address for MMIO registers.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:15	0h RW	**Memory BAR (MEMBAR):** Software programs this register with the lower 32 bit base address of the device's memory region. The MMIO registers in the touch controller are offset from this BAR.
14:4	0h RO	**Memory Size (MEMSIZE):** Hardwired to 0 to indicate 32KB of memory space.
3	0h RO	**Prefetchable (PREFETCH):** A device can mark a range as prefetchable if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables.
2:1	2h RO	**Type (TYP):** If this field is hardwired to 00 it indicates that this range can be mapped anywhere within 32-bit address space. If this field is hardwired to 10 it indicates that this range can be mapped anywhere within 64-bit address space.

Bit Range	Default and Access	Field Name (ID): Description
0	0h RO	**Memory Space Indicator (MEMSPACE):** Hardwired to 0 to identify a Memory BAR.

29.1.6 THC BAR0 MMIO High (THC_CFG_BAR0_HI)—Offset 14h

Upper address bits of base address for MMIO registers.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Memory BAR (MEMBAR):** Software programs this register with the high 32-bit base address of the device's memory region. The MMIO registers in the touch controller are offset from this BAR.

29.1.7 Subsystem and Vendor ID (THC_CFG_SID_SVID)—Offset 2Ch

Subsystem and Vendor ID

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SSID):** This is written by BIOS. No hardware action taken on this value.
15:0	0h RW/O	**Subsystem Vendor ID (SSVID):** This is written by BIOS. No hardware action taken on this value.

29.1.8 Capability List Pointer (THC_CFG_CAPP)—Offset 34h

Capability List Pointer

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 50h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	50h RO	**Capability Pointer (CP):** This register points to the starting offset of the capabilities ranges.

29.1.9 Interrupt Configuration (THC_CFG_INT)—Offset 3Ch

Interrupt Configuration

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	0h RW/O	**Interrupt pin (IPIN):** reflect the Interrupt Pin assigned to the host controller by the platform (and are hardwired). 8'h01 = INTA 8'h02 = INTB 8'h03 = INTC 8'h04 = INTD others = INTA
7:0	0h RW	**Interrupt Line (ILINE):** This data is not used by the THC. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to.

29.1.10 THC Unsupported Request Status (THC_CFG_UR_STS_CTL)—Offset 40h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW/L	**Function Disable (FD):** If set to 1 by software, THC is disabled
1	0h RW/1C/V	**Unsupported Request Detected (URD):** Set to 1 by hardware upon detecting an Unspported Request that is not considered an Advisory Non-Fatal error. Cleared to 0 when software writes a 1 to this register.
0	0h RW	**Unsupported Request Reporting Enabled (URRE):** If set to 1 by software, the touch host controller generates a DoSERR sideband message when the URD bit transitions from 0 to 1.

29.1.11 MSI Message Control_ Next Pointer and Capability ID (THC_CFG_MSIMC_MSINP_MSICID)—Offset 50h

MSI Message Control, Next Pointer and Capability ID

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 807005h

Bit Range	Default and Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RO	**Per Vector Masking Capable (PVMC):** This function does not support MSI per vector masking
23	1h RO	**64 bit address capable (XAC):** This function is not capable of sending 64 bit message address
22:20	0h RO	**Multiple Message Enable (MMEN):** Encoded number of interrupt vectors allocated by SW. Value of zero indicates one vector.
19:17	0h RO	**Multiple Message Capable (MMC):** Encoded number of interrupt vectors supported. Value of zero indicates one vector.
16	0h RW	**MSI Enable (MSIE):** If set to '1' MSI interrupt delivery is enabled. When this bit is cleared, prior to returning the configuration write completion, the device must send any pending MSI(s).
15:8	70h RO	**Next Item Pointer (NXTP):** Indicates the pointer for the next entry in the capabilities list
7:0	5h RO	**Capability ID (CAPID):** Indicates the linked list item as being the MSI Capability registers

29.1.12 MSI Message Address (THC_CFG_MSIMA)—Offset 54h

Lower bits of the MSI Message Address

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**Message Address (MADDR):** DW aligned MSI message address.
1:0	0h RO	Reserved.

29.1.13 MSI Message Upper Address (THC_CFG_MSIMUA)—Offset 58h

Upper bits of the MSI Message Address

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Message Address (MAUDDR):** Upper DW MSI message address.

29.1.14 MSI Message Data (THC_CFG_MSIMD)—Offset 5Ch

MSI Message Data

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**Message Data (MDAT):** MSI Message Data

29.1.15 PCI Power Management Capability (THC_CFG_PMCAP_PMNP_PMCID)—Offset 70h

PCI Power Management Capability

Access Method

Type: CFG Register (Size: 32 bits)
Device: 16
Function: 6

Default: C0030001h

Bit Range	Default and Access	Field Name (ID): Description
31:27	18h RW/O	**PME Support (PMES):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(27) X XXX1b - PME# can be asserted from D0 bit(28) X XX1Xb - PME# can be asserted from D1 bit(29) X X1XXb - PME# can be asserted from D2 bit(30) X 1XXXb - PME# can be asserted from D3hot bit(31) 1 XXXXb - PME# can be asserted from D3cold
26	0h RO	**D2 Support (D2S):** This device does not support D2
25	0h RO	**D1 Support (D1S):** This device does not support D1
24:22	0h RO	**Aux Current (AUXC):** Not Applicable
21	0h RO	**Device Specific Initialization (DSI):** See PCI Power Management Interface specification.
20	0h RO	Reserved.
19	0h RO	**PME Clock (PMECLK):** Not Applicable
18:16	3h RO	**Version (VER):** Value of 011b indicates that this function complies with rev 1.2 of PCI Power Management Interface Spec
15:8	0h RW/O	**Next Item Pointer (NXTP):** Indicates the pointer for the next entry in the capabilities list
7:0	1h RO	**Capability ID (CAPP):** Indicates the linked list item as being the PCI Power Management registers

29.1.16 PCI Power Management Control and Status (THC_CFG_PMD_PMCSRBSE_PMCSR)—Offset 74h

PCI Power Management Control and Status

Access Method

Type: CFG Register (Size: 32 bits)
Device: 16
Function: 6

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C/V	**PME Status (PMESTS):** See PCI Power Management Interface specification. This bit is set when the THC would normally assert the PME# signal independent of the state of the PME_En bit. Writing a 1 to this bit will clear it and cause the internal PME to deassert (if enabled). Writing a 0 has no effect. This bit must be explicitly cleared by the operating system each time the operating system is loaded.
14:13	0h RO	**Data Scale (DS):** Not Applicable
12:9	0h RO	**Data Select (DSEL):** Not Applicable
8	0h RW	**PME Enable (PMEEN):** See PCI Power Management Interface specification.
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset (NSR):** When set to 1, this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits.
2	0h RO	Reserved.
1:0	0h RW/V	**Power State (PWRST):** This 2-bit field is used both to determine the current power state of THC function and to set a new power state. The definition of the field values are: 00b - D0 state 11b - D3hot state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally however, the data is discarded and no state change occurs. When in the D3hot state, the PCH must not accept accesses to the THC memory range but the configuration space must still be accessible.

29.1.17 Device Idle Capability (THC_CFG_DEVIDLE)—Offset 90h

Device Idle Capability

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: F0140009h

Bit Range	Default and Access	Field Name (ID): Description
31:28	Fh RO	**Vendor-Specific Capability ID (VID):** A value of Fh in this 4-bit field identifies this Vendor Specific Capability as an Extended Capability, which uses a VSEC 16-bit Extended Capability ID in the subsequent four bytes. This field allows software to differentiate this capability from other Vendor Specific capabilities.
27:24	0h RO	**Vendor-Specific Capability Revision (REV):** For a VID of Fh, this field is reserved 0h.
23:16	14h RO	**Length (LENGTH):** Indicates that this capability is 20 bytes long.

Bit Range	Default and Access	Field Name (ID): Description
15:8	0h RO	**Next Capability Pointer (NCAPPP):** This field contains the offset to the next PCI Capability structure or 000h if no other items exist in the linked list of Capabilities.
7:0	9h RO	**Capability ID (CAPPID):** The value of 09h in this field indicates a Vendor Specific capability.

29.1.18 Vendor Specific Header (THC_CFG_VSHDR)—Offset 94h

Vendor Specific Header

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 1400010h

Bit Range	Default and Access	Field Name (ID): Description
31:20	14h RO	**VSEC Length (VSECL):** This field indicates the number of bytes in the entire VSEC structure, including the PCI Extended Capability header, the Vendor-Specific header, and the Vendor-Specific register
19:16	0h RO	**VSEC Rev (VSECR):** This field is a vendor-defined version number that indicates the version of the VSEC structure. Software must qualify the Vendor ID and VSEC ID before interpreting this field.
15:0	10h RO	**VSECID:** This field is a vendor-defined ID number that indicates the nature and format of the VSEC structure. Software must qualify the Vendor ID before interpreting this field.

29.1.19 SW LTR Pointer Register (THC_CFG_SWLTRPTR)—Offset 98h

SWLTRPTR Pointer Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	**SW LTR Update MMIO Offset Location (SWLTRLOC):** This register contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR. The value of this register is a do not care, if the Valid bit is not set
3:1	0h RO	**Base Address Register Number (BARNUM):** Contains the 0s based AR Number of the BAR which contains the location of the SW LTR MMIO register. When counting BAR Numbers, all BARs, regardless of size and type, consume one BAR Number. Bar 0 is the 1st BAR. The value of this register is a do not care, if the Valid bit is not set.
0	0h RO	**Valid (VALID):** Set to 1 to indicate that the function has implemented a SW LTR register as specified in the DevIdle that can be located using the SWLTRLOC register and BARNUM. Set to 0 to indicate that the function has not implemented a SW LTR register that is compliant to the DevIdle definition. This could be because the function has not implemented SW LTR at all, or has a device specific version of SW LTR.

29.1.20 Device Idle Pointer Register (THC_CFG_DEVIDLEPTR)—Offset 9Ch

Device Idle Pointer Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 101h

Bit Range	Default and Access	Field Name (ID): Description
31:4	10h RW/O	**DevIdle MMIO Offset Location (DEVIDLELOC):** This register contains the location pointer to the DevIdle register in MMIO space, as an offset from the specified BAR. The value of this register is a do not care, if the Valid bit is not set.
3:1	0h RO	**Base Address Register Number (BARNUM):** Contains the 0s based BAR Number of the BAR which contains the location of the DevIdle MMIO register. When counting BAR Numbers, all BARs, regardless of size and type, consume one BAR Number. Bar 0 is the 1st BAR. The value of this register is a do not care, if the Valid bit is not set.
0	1h RW/O	**Valid (VALID):** Set to 1 to indicate that the function has implemented a DevIdle register as specified in the DevIdle that can be located using the DEVIDLELOC register and BARNUM. Set to 0 to indicate that the function has not implemented a DevIdle register that is compliant to the DevIdle definition. This could be because the function has not implemented DevIdle at all, or has a device specific version of DevIdle.

29.1.21 Device Idle Power On Latency (THC_CFG_DEVIDLEPOL)—Offset A0h

Device Idle Power On Latency

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 800h

Bit Range	Default and Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12:10	2h RW/O	**Power On Latency Scale (POLS):** Latency Scale multiplier: 010: 1us 011: 32us All other settings are reserved. The value of this register is multiplied with the Power On Latency Value (POLV) to provide the DevIdle power on exit latency multiplier scale from 1us to 32ms. This register is defined to be RWO (read-write-once) to allow BIOS to set the initial value. This register is undefined if the DevIdle.Valid bit is 0.
9:0	0h RW/O	**Power On Latency Value (POLV):** 10-bit value that is multiplied by the Power On Latency Scale. A value of 0 indicates a power on latency of less than 1us. This register is defined to be RWO (read-write-once) to allow BIOS to set the initial value. This register is undefined if the DevIdle.Valid bit is 0.

29.1.22 Power Control Enables (THC_CFG_PCE)—Offset A4h

Power Control Enables

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5	0h RW/V	**Hardware Autonomous Enable (HAE):** If set, then the PGCB may request a PG whenever it is idle. This bit is loaded with the value from the PowerGateEnable soft strap when the soft strap pull is complete.
4	0h RO	Reserved.
3	1h RW/V	**Sleep Enable (SE):** : if clear, then IP will never asset Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing. Note that some platforms may default this bit to 0, others to 1. The SE bit is RW only. Otherwise the bit is RO.
2	0h RW	**D3-Hot Enable (D3HE):** if set, then IP will PG when idle and the PMCSR[1:0] register in the IP = 11.
1	0h RW	**I3 Enable (I3E):** if set, then IP will PG when idle and the D0i3 register (D0i3C[2] = 1) is set.
0	0h RW	**Software PowerGate Enable (SPE):** Software PowerGate Enable: If this bit is set, the IP will PG when pmc_sw_pg_req_b =0. NOTE: PMCSR[1:0] must not be used for this condition. It may be any value and the IP must PG if this bit is set and it sees pmc_sw_pg_req_b asserted and IP has met its IDLE requirements for Power Gating. This is not a force power gate mechanism, rather a PMC assisted Hardware Autonomous.

29.2 THC MMIO Space Common Register Map Registers

Table 29-2. Summary of THC MMIO Space Common Register Map Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
10h	13h	Device Idle Control Register (THC_M_CMN_DEVIDLECTRL)—Offset 10h	8h
14h	17h	THC LTR Control Register (THC_M_CMN_LTR_CTRL)—Offset 14h	C0000000h

29.2.1 Device Idle Control Register (THC_M_CMN_DEVIDLECTRL)—Offset 10h

Device Idle Control Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**Interrupt Request Capable (IRC):** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0.
3	1h RW/1C/V	**RestoreRequired (RR):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**DevIdle (DEVIDLE):** SW sets this bit to 1 to move the function into the DevIdle state. Writing this bit to 0 will return the function to the fully active D0 state (D0i0) THC currently does not support D0i3 and writing to this register has no effect.
1	0h RO	**Interrupt Request (IR):** SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.
0	0h RO/V	**Command-In-Progress (CIP):** HW sets this bit on a 1-0 or 0-1 transition of bit [2]. While set, the other bits in this register are not valid and it is unsupported for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit. If Interrupt Request bit [1] was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW. SW writes to this bit have no effect. THC currently does not support D0i3 and this bit will not ever read 1'b1.

29.2.2 THC LTR Control Register (THC_M_CMN_LTR_CTRL)—Offset 14h

THC LTR Control Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: C0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	3h RO/V	**Last LTR Message Sent (LAST_LTR_SENT):** This field reflects the last LTR message that was sent by the THC hardware. 00: infinite 01: active 10: low power 11: none
29:20	0h RW	**Active Latency Value (ACT_LTR_VAL):** The agent's latency tolerance is this value multiplied by ACT_LTR_SCALE.
19:17	0h RW	**Active Latency Scale (ACT_LTR_SCALE):** Specifies the scale for the value reported in the ACT_LTR_VAL field. Encodings: 000 - Value times 1 ns 001 - Value times 32 ns 010 - Value times 1,024 ns 011 - Value times 32,768 ns 100 - Value times 1,048,576 ns 101 - Value times 33,554,432 ns 110-111 - Not Permitted
16:7	0h RW	**Low Power Latency Value (LP_LTR_VAL):** The agent's latency tolerance is this value multiplied by LP_LTR_SCALE.
6:4	0h RW	**Low Power Latency Scale (LP_LTR_SCALE):** Specifies the scale for the value reported in the LP_LTR_VAL field. Encodings: 000 - Value times 1 ns 001 - Value times 32 ns 010 - Value times 1,024 ns 011 - Value times 32,768 ns 100 - Value times 1,048,576 ns 101 - Value times 33,554,432 ns 110-111 - Not Permitted
3	0h RO	Reserved.
2	0h RW	**Low Power LTR Requirement (LP_LTR_REQ):** If this bit is set to 1 then the agent's low power latency tolerance is LP_LTR_VAL multiplied by LP_LTR_SCALE. If this bit is 0 then the agent has no low power latency requirement (i.e. infinite latency).
1	0h RO	Reserved.
0	0h RW	**Active LTR Requirement (ACTIVE_LTR_REQ):** If this bit is set to 1 then the agent's latency tolerance is ACT_LTR_VAL multiplied by ACT_LTR_SCALE. If this bit is 0 then the agent has no active latency requirement (i.e. infinite latency).

29.3 THC MMIO Space Port 0 Register Map Registers

Table 29-3. Summary of THC MMIO Space Port 0 Register Map Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1008h	100Bh	Touch Host Controller Control Register (THC_M_PRT_CONTROL)—Offset 1008h	10000006h
1010h	1013h	THC SPI Bus Configuration Register (THC_M_PRT_SPI_CFG)—Offset 1010h	700273h
1020h	1023h	THC Interrupt Enable Register (THC_M_PRT_INT_EN)—Offset 1020h	20003604h
1024h	1027h	THC Interrupt Status Register (THC_M_PRT_INT_STATUS)—Offset 1024h	0h
1028h	102Bh	THC Error Cause Register (THC_M_PRT_ERR_CAUSE)—Offset 1028h	0h
1040h	1043h	THC SW sequencing Control (THC_M_PRT_SW_SEQ_CNTRL)—Offset 1040h	0h

Table 29-3. Summary of THC MMIO Space Port 0 Register Map Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1044h	1047h	THC SW sequencing Status (THC_M_PRT_SW_SEQ_STS)—Offset 1044h	0h
1048h	104Bh	THC SW Sequencing Data DW0 or SPI Address Register (THC_M_PRT_SW_SEQ_DATA0_ADDR)—Offset 1048h	0h
104Ch	104Fh	THC SW sequencing Data DW1 (THC_M_PRT_SW_SEQ_DATA1)—Offset 104Ch	0h
1050h	1053h	THC SW sequencing Data DW2 (THC_M_PRT_SW_SEQ_DATA2)—Offset 1050h	0h
1054h	1057h	THC SW sequencing Data DW3 (THC_M_PRT_SW_SEQ_DATA3)—Offset 1054h	0h
1058h	105Bh	THC SW sequencing Data DW4 (THC_M_PRT_SW_SEQ_DATA4)—Offset 1058h	0h
105Ch	105Fh	THC SW sequencing Data DW5 (THC_M_PRT_SW_SEQ_DATA5)—Offset 105Ch	0h
1060h	1063h	THC SW sequencing Data DW6 (THC_M_PRT_SW_SEQ_DATA6)—Offset 1060h	0h
1064h	1067h	THC SW sequencing Data DW7 (THC_M_PRT_SW_SEQ_DATA7)—Offset 1064h	0h
1068h	106Bh	THC SW sequencing Data DW8 (THC_M_PRT_SW_SEQ_DATA8)—Offset 1068h	0h
106Ch	106Fh	THC SW sequencing Data DW9 (THC_M_PRT_SW_SEQ_DATA9)—Offset 106Ch	0h
1070h	1073h	THC SW sequencing Data DW10 (THC_M_PRT_SW_SEQ_DATA10)—Offset 1070h	0h
1074h	1077h	THC SW sequencing Data DW11 (THC_M_PRT_SW_SEQ_DATA11)—Offset 1074h	0h
1078h	107Bh	THC SW sequencing Data DW12 (THC_M_PRT_SW_SEQ_DATA12)—Offset 1078h	0h
107Ch	107Fh	THC SW sequencing Data DW13 (THC_M_PRT_SW_SEQ_DATA13)—Offset 107Ch	0h
1080h	1083h	THC SW sequencing Data DW14 (THC_M_PRT_SW_SEQ_DATA14)—Offset 1080h	0h
1084h	1087h	THC SW sequencing Data DW15 (THC_M_PRT_SW_SEQ_DATA15)—Offset 1084h	0h
1088h	108Bh	THC SW sequencing Data DW16 (THC_M_PRT_SW_SEQ_DATA16)—Offset 1088h	0h
1090h	1093h	THC Write PRD Base Address Register Low (THC_M_PRT_WPRD_BA_LOW)—Offset 1090h	0h
1094h	1097h	THC Write PRD Base Address Register High (THC_M_PRT_WPRD_BA_HI)—Offset 1094h	0h
1098h	109Bh	THC Write DMA Control (THC_M_PRT_WRITE_DMA_CNTRL)—Offset 1098h	800000h
109Ch	109Fh	THC Write Interrupt Status (THC_M_PRT_WRITE_INT_STS)—Offset 109Ch	0h
10B4h	10B7h	THC device address for the bulk write (THC_M_PRT_WR_BULK_ADDR)—Offset 10B4h	1000h
10B8h	10BBh	THC Device Interrupt Cause Register Address (THC_M_PRT_DEV_INT_CAUSE_ADDR)—Offset 10B8h	0h
10BCh	10BFh	THC Device Interrupt Cause Register Value (THC_M_PRT_DEV_INT_CAUSE_REG_VAL)—Offset 10BCh	0h
10E0h	10E3h	THC TXDMA Frame Count (THC_M_PRT_TX_FRM_CNT)—Offset 10E0h	0h

Table 29-3. Summary of THC MMIO Space Port 0 Register Map Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
10E4h	10E7h	THC TXDMA Packet Count (THC_M_PRT_TXDMA_PKT_CNT)—Offset 10E4h	0h
10E8h	10EBh	THC Device Interrupt Count on this port (THC_M_PRT_DEVINT_CNT)—Offset 10E8h	0h
1100h	1103h	THC Read PRD Base Address Low for the 1st RXDMA (THC_M_PRT_RPRD_BA_LOW_1)—Offset 1100h	0h
1104h	1107h	THC Read PRD Base Address High for the 1st RXDMA (THC_M_PRT_RPRD_BA_HI_1)—Offset 1104h	0h
1108h	110Bh	THC Read PRD Control for the 1st RXDMA (THC_M_PRT_RPRD_CNTRL_1)—Offset 1108h	0h
110Ch	110Fh	THC Read DMA Control for the 1st RXDMA (THC_M_PRT_READ_DMA_CNTRL_1)—Offset 110Ch	40000000h
1110h	1113h	THC Read Interrupt Status for the 1st RXDMA (THC_M_PRT_READ_DMA_INT_STS_1)—Offset 1110h	0h
1114h	1117h	THC Read DMA Error Register for the 1st RXDMA (THC_M_PRT_READ_DMA_ERR_1)—Offset 1114h	0h
1118h	111Bh	Touch Sequencer GuC Tail Offset Address Low for the 1st RXDMA (THC_M_PRT_GUC_OFFSET_LOW_1)—Offset 1118h	0h
111Ch	111Fh	Touch Sequencer GuC Tail Offset Address High for the 1st RXDMA (THC_M_PRT_GUC_OFFSET_HI_1)—Offset 111Ch	0h
1120h	1123h	Touch Host Controller GuC Work Queue Item Size for the 1st RXDMA (THC_M_PRT_GUC_WORKQ_ITEM_SZ_1)—Offset 1120h	0h
1124h	1127h	Touch Host Controller GuC Control register for the 1st RXDMA (THC_M_PRT_GUC_WORKQ_SZ_1)—Offset 1124h	0h
1128h	112Bh	Touch Sequencer Control for the 1st DMA (THC_M_PRT_TSEQ_CNTRL_1)—Offset 1128h	0h
1130h	1133h	Touch Sequencer GuC Doorbell Address Low for the 1st RXDMA (THC_M_PRT_GUC_DB_ADDR_LOW_1)—Offset 1130h	0h
1134h	1137h	Touch Sequencer GuC Doorbell Address High for the 1st RXDMA (THC_M_PRT_GUC_DB_ADDR_HI_1)—Offset 1134h	0h
1138h	113Bh	Touch Sequencer GuC Doorbell Data (THC_M_PRT_GUC_DB_DATA_1)—Offset 1138h	1h
1140h	1143h	Touch Sequencer GuC Tail Offset Initial Value for the 1st RXDMA (THC_M_PRT_GUC_OFFSET_INITVAL_1)—Offset 1140h	0h
1170h	1173h	THC Device Address for the bulk/touch data read for the 1st RXDMA (THC_M_PRT_RD_BULK_ADDR_1)—Offset 1170h	1000h
11A0h	11A3h	THC Gfx/SW Doorbell Count from the 1st Stream RXDMA on this port (THC_M_PRT_DB_CNT_1)—Offset 11A0h	0h
11A4h	11A7h	THC Frame Count from the 1st Stream RXDMA on this port (THC_M_PRT_FRM_CNT_1)—Offset 11A4h	0h
11A8h	11ABh	THC Micro Frame Count from the 1st Stream RXDMA on this port (THC_M_PRT_UFRM_CNT_1)—Offset 11A8h	0h
11ACh	11AFh	THC Packet Count from the 1st Stream RXDMA on this port (THC_M_PRT_RXDMA_PKT_CNT_1)—Offset 11ACh	0h
11B0h	11B3h	THC Software Interrupt Count from the 1st Stream RXDMA on this port (THC_M_PRT_SWINT_CNT_1)—Offset 11B0h	0h
11B4h	11B7h	Touch Sequencer Frame Drop Counter for the 1st RXDMA (THC_M_PRT_FRAME_DROP_CNT_1)—Offset 11B4h	0h
1200h	1203h	THC Read PRD Base Address Low for the 2nd RXDMA (THC_M_PRT_RPRD_BA_LOW_2)—Offset 1200h	0h

Table 29-3. Summary of THC MMIO Space Port 0 Register Map Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1204h	1207h	THC Read PRD Base Address High for the 2nd RXDMA (THC_M_PRT_RPRD_BA_HI_2)—Offset 1204h	0h
1208h	120Bh	THC Read PRD Control for the 2nd RXDMA (THC_M_PRT_RPRD_CNTRL_2)—Offset 1208h	0h
120Ch	120Fh	THC Read DMA Control for the 2nd RXDMA (THC_M_PRT_READ_DMA_CNTRL_2)—Offset 120Ch	40000000h
1210h	1213h	THC Read Interrupt Status for the 2nd RXDMA (THC_M_PRT_READ_DMA_INT_STS_2)—Offset 1210h	0h
1214h	1217h	THC Read DMA Error Register for the 2nd RXDMA (THC_M_PRT_READ_DMA_ERR_2)—Offset 1214h	0h
1218h	121Bh	Touch Sequencer GuC Tail Offset Address Low for the 2nd RXDMA (THC_M_PRT_GUC_OFFSET_LOW_2)—Offset 1218h	0h
121Ch	121Fh	Touch Sequencer GuC Tail Offset Address High for the 2nd RXDMA (THC_M_PRT_GUC_OFFSET_HI_2)—Offset 121Ch	0h
1220h	1223h	Touch Host Controller GuC Work Queue Item Size for the 2nd RXDMA (THC_M_PRT_GUC_WORKQ_ITEM_SZ_2)—Offset 1220h	0h
1224h	1227h	Touch Host Controller GuC Control register for the 2nd RXDMA (THC_M_PRT_GUC_WORKQ_SZ_2)—Offset 1224h	0h
1228h	122Bh	Touch Sequencer Control for the 2nd DMA (THC_M_PRT_TSEQ_CNTRL_2)—Offset 1228h	0h
1230h	1233h	Touch Sequencer GuC Doorbell Address Low for the 2nd RXDMA (THC_M_PRT_GUC_DB_ADDR_LOW_2)—Offset 1230h	0h
1234h	1237h	Touch Sequencer GuC Doorbell Address High for the 2nd RXDMA (THC_M_PRT_GUC_DB_ADDR_HI_2)—Offset 1234h	0h
1238h	123Bh	Touch Sequencer GuC Doorbell Data for PRD2 (THC_M_PRT_GUC_DB_DATA_2)—Offset 1238h	1h
1240h	1243h	Touch Sequencer GuC Tail Offset Initial Value for the 2nd RXDMA (THC_M_PRT_GUC_OFFSET_INITVAL_2)—Offset 1240h	0h
1270h	1273h	THC Device Address for the bulk/touch data read for the 2nd RXDMA (THC_M_PRT_RD_BULK_ADDR_2)—Offset 1270h	1000h
12A0h	12A3h	THC Gfx/SW Doorbell Count from the 2nd Stream RXDMA on this port (THC_M_PRT_DB_CNT_2)—Offset 12A0h	0h
12A4h	12A7h	THC Frame Count from the 2nd Stream RXDMA on this port (THC_M_PRT_FRM_CNT_2)—Offset 12A4h	0h
12A8h	12ABh	THC Micro Frame Count from the 2nd Stream RXDMA on this port (THC_M_PRT_UFRM_CNT_2)—Offset 12A8h	0h
12ACh	12AFh	THC Packet Count from the 2nd Stream RXDMA on this port (THC_M_PRT_RXDMA_PKT_CNT_2)—Offset 12ACh	0h
12B0h	12B3h	THC Software Interrupt Count from the 2nd Stream RXDMA on this port (THC_M_PRT_SWINT_CNT_2)—Offset 12B0h	0h
12B4h	12B7h	Touch Sequencer Frame Drop Counter for the 2nd RXDMA (THC_M_PRT_FRAME_DROP_CNT_2)—Offset 12B4h	0h

29.3.1 Touch Host Controller Control Register (THC_M_PRT_CONTROL)—Offset 1008h

THC Control Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 10000006h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Port type for this port instance (PORT_TYPE):** 00: SPI port 01: thc port Others: reserved
29	0h RO/V	**Indication of SPI IO (SPI_IO_RDY):** 0: This SPI port IO is not ready for operation 1: This SPI port IO is ready for operation This bit is used by driver to decide whether the SPI port is ready to use, including rcomp done completion etc. SW needs to wait this bit to be 1 once on D0 entry (boot or D3 exit) before running any PIO/DMA cycles on SPI bus.
28	1h RW/L	**Whether this port is supported or not (PORT_SUPPORTED):** 0: This port is not supported 1: This port is supported This bit is used by driver to decide whether this port is supported or not. In the per port driver model, ii. BIOS will set the PORT_SUPPORTED bit to 1 only for the first port under each controller. Driver will not operate the other ports where the PORT_SUPPORTED bit is 0. In the multi-port shared driver model, BIOS may set this bit to 1 for multiple ports under the 1st THC. It will function disable the other THC. This bit is locked by THC_BIOS_LOCK_EN. For security reason, BIOS shall lock them after it completes the programming, before host software/OS is brought up.
27	0h RW/L	**Lock bit for several BIOS registers (THC_BIOS_LOCK_EN):** 0: The registers listed below are not locked 1: The registers listed below are locked. The registers locked by this bit includes: THC_M_PRT_GUC_VDM* For security reason, BIOS shall lock them after it completes the programming, before host software/OS is brought up.
26:23	0h RO	Reserved.
22:20	0h RO/V	**Port index under this THC (PORT_INDEX):** This field indicates the 0-based port index of this port in the THC.
19	0h RO	Reserved.
18:16	0h RO/V	**THC Instance index of this THC (THC_INSTANCE_INDEX):** This field indicates the 0-based instance index of this THC.
15:14	0h RO	Reserved.
13	0h RW/L	**THC Locking bit to lock driver registers (THC_DRV_LOCK_EN):** When set to 1 , prevents INT_SW_DMA_EN, INT_SW_DMA_EN2 from being changed. This bit can only be written from 0 to 1 once. Once set to 1, this bit can only be cleared by a hardware reset.
12:4	0h RO	Reserved.
3	0h RW	**Device GPIO Reset (DEVRST):** 1: Deassert Device reset/power on through GPIO. 0: Assert Device reset/power off through GPIO.

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO/V	**Hardware Status for Quiesce Status bit (THC_DEVINT_QUIESCE_HW_STS):** HW will set this bit once RX sequencer is IDLE, after completing processing of any microframe that started before the THC_DEVINT_QUIESCE_EN. SW cannot clear THC_DEVINT_QUIESCE_EN until it sees this bit set
1	1h RW	**Quiesce bit for the device interrupt (THC_DEVINT_QUIESCE_EN):** When this bit is set, THC shall complete servicing the current touch microframe or current device interrupt, and ignore the TIC's interrupt (including touch and non-touch interrupt) until the bit is cleared by SW. When SW writes 1 to this bit, THC is expected to complete processing the current microframe and then set THC_DEVINT_QUIESCE_HW_STS. THC shall not drop any outstanding interrupt asserted when THC_DEVINT_QUIESCE_EN is set. SW shall poll THC_DEVINT_QUIESCE_HW_STS to be 1 before it can clear THC_DEVINT_QUIESCE_EN. After the bit is cleared by SW, THC shall start service device interrupt as usual. This bit does not impact the activities on TXDMA and PIO operations.
0	0h RO	Reserved.

29.3.2 THC SPI Bus Configuration Register (THC_M_PRT_SPI_CFG)—Offset 1010h

THC SPI Port Configuration Register
Note: The THC_M_PRT_SPI_CFG register can't be written/updated when TX/RX DMAs is running or PIO is running cycles on the bus.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 700273h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**Enable SPI Clock Divide by 8 to support low freq device. (SPI_LOW_FREQ_EN):** 1: All the SPI read/write clock frequency (defined in SPI_TCWF/SPI_TCRF) will be divided further by 8 0: No further divider is supported.
22:20	7h RW	**SPI Touch Cycle Write Frequency (SPI_TCWF):** The listed frequencies are approximate. 100 : 30MHz divide by 4 101 : 24MHz, divide by 5 110 : 20MHz, divide by 6 111 : 17MHz, divide by 7 Others: Reserved
19:18	0h RW	**SPI Touch IO Write mode (SPI_TWMODE):** Firmware programs this mode after discovering capabilities of Touch device.
17:16	0h RO	Reserved.
15:7	4h RO	**SPI READ Max Packet Size (SPI_RD_MPS):** SPI Read Max Packet Size in 16 bytes. Software shall program this register after it negotiates with the device. This has to be programmed before it issues any other cycles to the device including the configuration, TX DMA and RX DMA.

Bit Range	Default & Access	Field Name (ID): Description
6:4	7h RW	**SPI Touch Cycle Read Frequency (SPI_TCRF):** The listed frequencies are approximate. 100 : 30MHz divide by 4 101 : 24MHz, divide by 5 110 : 20MHz, divide by 6 111 : 17MHz, divide by 7 Others: Reserved
3:2	0h RW	**SPI Touch IO Read mode (SPI_TRMODE):** Firmware programs this mode after discovering capabilities of Touch device. 00 : Single IO Read (1-1-1 0B) enabled 01: Dual IO Read (1-2-2 BBh) enabled (DIORE) 10: Quad IO Read (1-4-4/EBh) mode (QIORE) 11: Quad Parrellel IO Read (4-4-4/FBh) mode (QPIRE) enabled.
1:0	3h RW	**SPI Touch IO Read Dummy Clocks (SPI_TRDC):** Firmware programs this mode after discovering capabilities of Touch device.

29.3.3 THC Interrupt Enable Register (THC_M_PRT_INT_EN)—Offset 1020h

THC Port Interrupt Enable Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 20003604h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	1h RW	**Enable THC Transaction Error Reporting with Interrupt (TXN_ERR_INT_EN):** b0: Disable THC Transaction Error Reporting Interrupt b1: Enable HCI Transaction Error Reporting Interrupt Note:The Interrupt enable is also qualified by the MSIE or Line Interrupt Enable. When all these enables are set and when THC_TXN_ERR_INT_STS is set, an interrupt will be sent to SW.
28:24	0h RO	Reserved.
23:16	0h RW	**Enable THC Fatal Error Reporting with Interrupt (FATAL_ERR_INT_EN):** b0: Disable THC Fatal Error Reporting Interrupt b1: Enable THC Fatal Error Reporting Interrupt Note:The Interrupt enable is also qualified by the MSIE or Line Interrupt Enable. When all these enables are set and when THC_FATAL_ERR_INT_STS is set, an interrupt will be sent to SW.
15:14	0h RO	Reserved.
13	1h RW	**Enable PRD Entry Error Reporting with Interrupt (PRD_ENTRY_ERR_INT_EN)**
12	1h RW	**Enable THC Buffer Overrun Error Reporting with Interrupt (BUF_OVRRUN_ERR_INT_EN)**
11	0h RO	Reserved.
10	1h RW	**Enable Frame Babble Error Reporting with Interrupt (FRAME_BABBLE_ERR_INT_EN)**

Bit Range	Default & Access	Field Name (ID): Description
9	1h RW	**Enable Invalid Device Register Error Reporting with Interrupt (INVLD_DEV_ENTRY_INT_EN)**
8:4	0h RO	Reserved.
3	0h RW	**Stop on Frame Babble (SOFB):** When set, HW will clear the Start bit, upon detection of a frame babble, and stop read DMA operations.
2	1h RW	**Stop on Invalid Device Register (SIDR):** When set, HW will clear the Start bit, upon detection of a invalid device register, and stop read DMA operations.
1	0h RW	**Stop on THC buffer overrun (SBO):** When set, HW will clear the Start bit, upon detection of a buffer overrun, and stop read DMA operations.
0	0h RW	**Stop on Invalid PRD entry (SIPE):** When set, HW will clear the Start bit, upon detection of an invalid PRD entry, and stop read DMA operations.

29.3.4 THC Interrupt Status Register (THC_M_PRT_INT_STATUS)—Offset 1024h

THC Port Interrupt Status Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30	0h RW/1C/V	**Interrupt Status of THC fatal error (FATAL_ERR_INT_STS):** Interrupt status when a THC fatal error occurs. If the THC_Fatal_Err_Intr_En bit is also 1, then an interrupt is generated. SW clears the bit by writing 1 to the bit. 1 - A THC Fatal error occured. The error cause is captured in the FATAL_ERR_CAUSE register. 0 - No Connection status change.
29	0h RO	Reserved.
28	0h RW/1C/V	**Interrupt Status of THC transaction error (TXN_ERR_INT_STS):** Interrupt status when a THC transaction error occurs. If the THC_TXN_Err_Intr_En bit is also 1, then an interrupt is generated. SW clears the bit by writing 1 to the bit. 1 - A THC transaction error occured. The error cause is captured in the TXN_ERR_CAUSE register. 0 - No Connection status change.
27:0	0h RO	Reserved.

29.3.5 THC Error Cause Register (THC_M_PRT_ERR_CAUSE)—Offset 1028h

THC Port Interrupt Status Register

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:16	0h RO/V	**THC Fatal Error Cause (FATAL_ERR_CAUSE):** There is no fatal error cause in SPI mode.
15:14	0h RO	Reserved.
13	0h RW/1C/V	**THC Transaction Error Cause - Invalid PRD Entry (PRD_ENTRY_ERR):** This error condition occurs when the THC detects an invalid PRD entry. A PRD entry is invalid when its length is 0.
12	0h RW/1C/V	**THC Transaction Error Cause - THC Buffer Overrun (BUF_OVRRUN_ERR):** This error condition occurs when the THC can't keep up with the incoming touch data due to IOSF or other internal bottleneck, and cause internal buffer overflow.
11	0h RO	Reserved.
10	0h RW/1C/V	**THC Transaction Error Cause - Frame Babble (FRAME_BABBLE_ERR):** This error condition occurs when the THC receives larger size of the touch data than the PRD table size for the current frame. This condition is detected when the micro-frame size is read from device register and the value exceeds the remaining buffer space for the current frame.
9	0h RW/1C/V	**THC Transaction Error Cause - Invalid Device Register Setting (INVLD_DEV_ENTRY):** This error condition occurs when the THC detects invalid settings in the touch device's register INT_CAUSE. The touch device's register settings are defined in Intel Precise Touch & Stylus Gen2. The device register setting is invalid if the microframe size field is 0.
8:0	0h RO	Reserved.

29.3.6 THC SW sequencing Control (THC_M_PRT_SW_SEQ_CNTRL)—Offset 1040h

THC SW sequencing Control

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/L	**THC SW Sequencing Bus Byte Count (THC_SS_BC):** This field specifies the SPI read/write byte count to send out during the SW sequencing cycle. For SPI, this is a 1-based byte count for read or write. i.e. value 1 is for 1 byte and 2 is for 2 bytes. Valid values are in the range of 1-64. Any other value will result in THC_SS_ERR being set.
15:8	0h RW/L	**THC SW Sequencing Bus Command (THC_SS_CMD):** In SPI port, the register read and touch data read commands are mapped to SPI read cycles. The register write and bulk write commands are mapped to SPI write cycles. The other commands are not used in SPI mode.
7:2	0h RO	Reserved.
1	0h RW/L	**THC SW Sequencing Cycle Done Interrupt Enable (THC_SS_CD_IE):** When set to 1, the THC asserts an interrupt request whenever the Touch Cycle Done bit is 1.
0	0h RW/1S/V/L	**THC SW Sequence Cycle Go (TSSGO):** A write to this register with THC Arbiter to start a cycle. This register is cleared by hardware when the cycle is granted by the THC arbiter to run the cycle on the THC bus. When the cycle is complete, the TSSDONE bit is set. Software is forbidden to write to any register in the THC_SS_SEQ_CNTRL/DATA register between the TSSGO bit getting set and the TSSDONE bit being cleared. Any attempt to violate this rule will be ignored by hardware. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1. This saves an additional memory write. This bit remains set until the transaction is granted by the THC Controller's internal arbiter.

29.3.7 THC SW sequencing Status (THC_M_PRT_SW_SEQ_STS)—Offset 1044h

THC SW sequencing Status

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	0h RO/V	**THC SW Sequencing Cycle In Progress (THC_SS_CIP):** Hardware sets this bit when software sets the THC Cycle Go (TSSGO) bit. This bit remains set until the cycle completes on the bus interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0.
2	0h RO	Reserved.
1	0h RW/1C/V	**THC SW Sequencing Error (THC_SS_ERR):** Hardware sets this bit to 1 when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1 or until a partition reset occurs. Software must clear this bit before setting the THC Cycle GO bit in this register.
0	0h RW/1C/V	**THC SW Sequence Cycle Done (TSSDONE):** The THC sets this bit to 1 when the SW Touch Cycle completes after software previously set the TSSGO bit. This bit remains asserted until cleared by software writing a 1 or host partition reset. When this bit is set and the THC_SS_CD_IE MSI Enable bit is set the THC controller sends MSI. Software must make sure this bit is cleared prior to enabling the TDONE MSI assertion for a new programmed access.

29.3.8 THC SW Sequencing Data DW0 or SPI Address Register (THC_M_PRT_SW_SEQ_DATA0_ADDR)—Offset 1048h

THC SW sequencing Data DW0/Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**THC SW sequencing Data/Address (THC_SW_SEQ_DATA0_ADDR):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc. In SPI mode, this DW are programmed with byte address field. The upper address bits [31:24] will be ignored by THC on the SPI bus.

29.3.9 THC SW sequencing Data DW1 (THC_M_PRT_SW_SEQ_DATA1)—Offset 104Ch

THC SW sequencing Data DW1

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data 1 (THC_SW_SEQ_DATA1):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

29.3.10 THC SW sequencing Data DW2 (THC_M_PRT_SW_SEQ_DATA2)—Offset 1050h

THC SW sequencing Data DW2

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data DW2 (THC_SW_SEQ_DATA2):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

29.3.11 THC SW sequencing Data DW3 (THC_M_PRT_SW_SEQ_DATA3)—Offset 1054h

THC SW sequencing Data DW3

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data DW3 (THC_SW_SEQ_DATA3):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

29.3.12 THC SW sequencing Data DW4 (THC_M_PRT_SW_SEQ_DATA4)—Offset 1058h

THC SW sequencing Data DW4

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data DW4 (THC_SW_SEQ_DATA4):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

29.3.13 THC SW sequencing Data DW5 (THC_M_PRT_SW_SEQ_DATA5)—Offset 105Ch

THC SW sequencing Data DW5

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data DW5 (THC_SW_SEQ_DATA5):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

29.3.14 THC SW sequencing Data DW6 (THC_M_PRT_SW_SEQ_DATA6)—Offset 1060h

THC SW sequencing Data DW6

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW Sequencing Data DW6 (THC_SW_SEQ_DATA6):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

29.3.15 THC SW sequencing Data DW7 (THC_M_PRT_SW_SEQ_DATA7)—Offset 1064h

THC SW sequencing Data DW7

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data 7 (THC_SW_SEQ_DATA7):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

29.3.16 THC SW sequencing Data DW8 (THC_M_PRT_SW_SEQ_DATA8)—Offset 1068h

THC SW sequencing Data DW8

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data DW8 (THC_SW_SEQ_DATA8):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

29.3.17 THC SW sequencing Data DW9 (THC_M_PRT_SW_SEQ_DATA9)—Offset 106Ch

THC SW sequencing Data DW9

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data DW9 (THC_SW_SEQ_DATA9):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

29.3.18 THC SW sequencing Data DW10 (THC_M_PRT_SW_SEQ_DATA10)—Offset 1070h

THC SW sequencing Data DW10

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data 10 (THC_SW_SEQ_DATA10):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

29.3.19 THC SW sequencing Data DW11 (THC_M_PRT_SW_SEQ_DATA11)—Offset 1074h

THC SW sequencing Data DW11

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data DW11 (THC_SW_SEQ_DATA11):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

29.3.20 THC SW sequencing Data DW12 (THC_M_PRT_SW_SEQ_DATA12)—Offset 1078h

THC SW sequencing Data DW12

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data DW12 (THC_SW_SEQ_DATA12):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

29.3.21 THC SW sequencing Data DW13 (THC_M_PRT_SW_SEQ_DATA13)—Offset 107Ch

THC SW sequencing Data DW13

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data DW13 (THC_SW_SEQ_DATA13):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

29.3.22 THC SW sequencing Data DW14 (THC_M_PRT_SW_SEQ_DATA14)—Offset 1080h

THC SW sequencing Data DW14

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data DW14 (THC_SW_SEQ_DATA14):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

29.3.23 THC SW sequencing Data DW15 (THC_M_PRT_SW_SEQ_DATA15)—Offset 1084h

THC SW sequencing Data DW15

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data DW15 (THC_SW_SEQ_DATA15):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

29.3.24 THC SW sequencing Data DW16 (THC_M_PRT_SW_SEQ_DATA16)—Offset 1088h

THC SW sequencing Data DW16

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data DW16 (THC_SW_SEQ_DATA16):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

29.3.25 THC Write PRD Base Address Register Low (THC_M_PRT_WPRD_BA_LOW)—Offset 1090h

THC Write PRD Base Address

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**THC Write PRD Base Address (THC_M_PRT_WPRD_BA_LOW):** This register initializes the lower 32 bits of the 64 bit write PRD table base address, 4K aligned, thus 20bits are allocated.
11:0	0h RO	Reserved.

29.3.26 THC Write PRD Base Address Register High (THC_M_PRT_WPRD_BA_HI)—Offset 1094h

THC Write PRD Base Address Register Hi

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**THC Write PRD Base Address Register Hi (THC_M_PRT_WPRD_BA_HI):** This register initializes the upper 32 bits of the 64 bit write PRD table base address.

29.3.27 THC Write DMA Control (THC_M_PRT_WRITE_DMA_CNTRL)—Offset 1098h

THC Write DMA Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 800000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**PRD Table Entry Count for WRDMA (THC_WRDMA_PTEC):** The number of PRD entries in the write PRD tables. 00h: 1 PRD entry for the write PRD Table 01h: 2 PRD entries for the write PRD Table :: FFh: 256 PRD entries for each PRD Table
23	1h RO	**Update HW Status for WRDMA (THC_WRDMA_UHS):** If set, the HwStatus field of each PRD entry (for each PRD table) bit is updated (successful or error).
22:4	0h RO	Reserved.
3	0h RW	**Interrupt Enable on WRDMA Completion (THC_WRDMA_IE_IOC_DMACPL):** When set, interrupt is generated upon completion of the Write DMA PRD table.
2	0h RW	**Interrupt Enable on IOC for WRDMA (THC_WRDMA_IE_IOC):** When set, interrupt is generated upon completion of the PRD block transfer, with IOC=1, or when an error is encountered with the Error=1 in the THC_WRITE_DMA_INT_STS register.
1	0h RW	**Interrupt Enable on Error for WRDMA (THC_WRDMA_IE_IOC_ERROR):** When set, interrupt is generated when an error is encountered with the Write DMA Error=1.
0	0h RW/V	**Start WRDMA (THC_WRDMA_START):** SW sets the Start bit to arm the Write DMA engine. HW clears the bit after the DMA completion as indicated by interrupt and/or Status bits. SW can also clear the Start bit to abort an on-going DMA operation. In this case, HW completes all the outstanding requests to system memory and then stops the PRD actions at a safe point. SW shall poll this bit after it writes 0 to the start bit until HW completes the stop and clears the bit.

29.3.28 THC Write Interrupt Status (THC_M_PRT_WRITE_INT_STS)—Offset 109Ch

THC Write Interrupt Status

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	0h RO/V	**Active status for Write DMA (THC_WRDMA_ACTIVE):** Write DMA is active. Set by HW when the Write DMA Start bit is set by SW and auto-cleared by HW in the following conditions: - The entire Write DMA operation has been completed successfully or - The Write DMA operation has been halted by software clearing the Write DMA Start bit (and no read completion pending).
2	0h RW/1C/V	**Interrupt Status for IOC for Write DMA (THC_WRDMA_IOC_STS):** A PRD entry with IOC bit set has been completed during WRDMA operation. If the THC_WRDMA_IE_IOC bit is also 1, then an interrupt is generated. In polling mode, when THC_WRDMA_IE_IOC=0, SW clears the bit by writing 1 to the bit.
1	0h RW/1C/V	**Write DMA Error Status (THC_WRDMA_ERROR_STS):** Error encountered during write DMA operation. If the THC_WRDMA_IE_ERROR bit is also 1, then an interrupt is generated. In polling mode, when THC_WRDMA_IE_ERROR=0, SW clears the bit by writing 1 to the bit. Note: For SPI bus, there is no known error condition for this bit.
0	0h RW/1C/V	**Write DMA Completion Status bit (THC_WRDMA_CMPL_STATUS):** This bit is set upon successful completion of the Write DMA operation or by the rising edge of the Error bit. If the THC_WRDMA_IE_IOC_DMACPL bit is also 1, then an interrupt is generated. In polling mode, when THC_WRDMA_IE_IOC_DMACPL=0, SW clears the bit by writing 1 to the bit.

29.3.29 THC device address for the bulk write (THC_M_PRT_WR_BULK_ADDR)—Offset 10B4h

THC device address for the bulk write

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	1000h RW/O	**THC device address for the bulk write (THC_M_PRT_WR_BULK_ADDR):** THC Device Address for the bulk data write. The bulk write cycles addresses start from the bulk address defined in THC_M_PRT_WR_BULK_ADDR (default 0x1000) and increment on every packet until the end of the write frame. The bulk write address resumes using the address in THC_M_PRT_WR_BULK_ADDR at the beginning of every write frame. SW is responsible to program this register correctly, and make sure all resulting touch cycles will not exceed the touch device's bulk address space or roll over. Otherwise, THC's behavior is undefined. Note: For SPI devices, only 24bit addressing space is supported. Default to 0x1000.

29.3.30 THC Device Interrupt Cause Register Address (THC_M_PRT_DEV_INT_CAUSE_ADDR)—Offset 10B8h

THC Device Interrupt Cause Register Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/O	**THC Device Interrupt Cause Register Address (THC_M_PRT_DEV_INT_CAUSE_ADDR):** THC Device Interrupt Cause Register Address. This register defines the Device Interrupt Cause Register Address for RXDMA and SW operation. SW is responsible to program this register correctly based on the device register offset, and make sure all resulting touch cycles will not cause malfunction of the touch device. Otherwise, THC's behavior is undefined. Note: For SPI devices, only 24bit addressing space is supported. Default to 0x0.

29.3.31 THC Device Interrupt Cause Register Value (THC_M_PRT_DEV_INT_CAUSE_REG_VAL)—Offset 10BCh

THC Device Interrupt Cause Register Value

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**THC Device Interrupt Cause Register Value (THC_M_PRT_DEV_INT_CAUSE_REG_VAL):** THC Device Interrupt Cause Register Value. This register reflects the latest values of the Device Interrupt Cause Register when it read by the RXDMA sequencer.

29.3.32 THC TXDMA Frame Count (THC_M_PRT_TX_FRM_CNT)—Offset 10E0h

Touch TX Frame Counter

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch TX Frame Counter Reset (THC_M_PRT_TX_FRM_CNT_RST):** Reset the THC_M_PRT_TX_FRM_CNT counter. SW writing this bit to a 0x1, resets the THC_M_PRT_TX_FRM_CNT counter to a 0x0.HW clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch TX Frame Counter (THC_M_PRT_TX_FRM_CNT):** Number of Touch Frames sent from this port. The counter shall roll over back to 0 after reaching the maximum value.

29.3.33 THC TXDMA Packet Count (THC_M_PRT_TXDMA_PKT_CNT)—Offset 10E4h

Touch TX DMA Packet Counter

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch TX DMA Packet Counter Reset (THC_M_PRT_TXDMA_PKT_CNT_RST):** Reset the THC_M_PRT_TXDMA_PKT_CNT counter. SW writing this bit to a 0x1, resets the THC_M_PRT_TXDMA_PKT_CNT clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch TX DMA Packet Counter (THC_M_PRT_TXDMA_PKT_CNT):** Number of TX DMA Packet sent on this port. The counter shall roll over back to 0 after reaching the maximum value.

29.3.34 THC Device Interrupt Count on this port (THC_M_PRT_DEVINT_CNT)—Offset 10E8h

Touch Device Interrupt Counter

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch Device Interrupt Counter (THC_M_PRT_DEVINT_CNT_RST):** Reset the THC_M_PRT_DEVINT_CNT counter. SW writing this bit to a 0x1, resets the THC_M_PRT_DEVINT_CNT counter to a 0x0.HW clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch Device Interrupt Counter (THC_M_PRT_DEVINT_CNT):** Number of Device interrupts Received on this port. The counter shall roll over back to 0 after reaching the maximum value.

29.3.35 THC Read PRD Base Address Low for the 1st RXDMA (THC_M_PRT_RPRD_BA_LOW_1)—Offset 1100h

THC Read PRD Base Address for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**THC Read PRD Base Address for the 1st RXDMA (THC_M_PRT_RPRD_BA_LOW):** This register initializes the lower 32 bits of the 64 bit PRD table base address for the 1st RXDMA, 4K aligned, thus 20bits are allocated.
11:0	0h RO	Reserved.

29.3.36 THC Read PRD Base Address High for the 1st RXDMA (THC_M_PRT_RPRD_BA_HI_1)—Offset 1104h

THC Read PRD Base Address High for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**THC Read PRD Base Address High for the 1st RXDMA (THC_M_PRT_RPRD_BA_HI):** This register initializes the upper 32 bits of the 64 bit PRD table base address for the 1st RXDMA.

29.3.37 THC Read PRD Control for the 1st RXDMA (THC_M_PRT_RPRD_CNTRL_1)—Offset 1108h

THC Read PRD Control for the 1st RX DMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	0h RW	**PRD Table Entry Count for the 1st RX DMA (PTEC):** The number of PRD entries in each of the PRD tables held in the circular buffer. The PRD Entry Count must be large enough to contain the maximum raw data buffer size for any touch device. A fragmented data buffer could require a PRD entry for every 4KB of host memory allocated. In this case, for a 1MB raw data buffer, 128 PRD entries would be required. 00h: 1 PRD entry for each PRD Table 01h: 2 PRD entries for each PRD Table :: FFh: 256 PRD entries for each PRD Table
7	0h RO	Reserved.
6:0	0h RW	**PRD CB Depth for the 1st RX DMA (PCD):** This field indicates the number of PRD tables contained in the PRD address space. The filed directly corresponds to the number of raw data buffers used in the iTouch system. The raw data buffers are allocated by the host HID driver running in the OS. 00h: 1 PRD Table 01h: 2 PRD Table :: 7Fh: 128 PRD Tables

29.3.38 THC Read DMA Control for the 1st RXDMA (THC_M_PRT_READ_DMA_CNTRL_1)—Offset 110Ch

THC Read DMA Control for the 1st RXDMA

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 40000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**THC PRD CB Pointer Reset for the 1st RXDMA (TPCPR):** Setting this bit to a 1b resets DMA circular buffers read and write pointers to 00h. After the DMA CB pointers have been reset to 00h, hardware clears this bit to 0. SW can only reset tail offset when active and start are 0, i.e. DMA is idle.
30	1h RO	**Update HwStatus for the 1st RXDMA (UHS):** If set, the HwStatus field of each PRD entry (for each PRD table) bit is updated (successful or error).
29	0h RW	**Stop on Overflow for the 1st RXDMA (SOO):** When set, HW will clear the Start bit, upon detection of a DMA Buffer overflow, and stop read DMA operations.. An overflow condition occurs when the read and write pointers contain the same value.
28	0h RW/L	**Interrupt SW Enable on DMA Device Interrupt for the 1st RXDMA (INT_SW_DMA_EN):** When set to 1, an interrupt is generated to host SW even when a "touch data ready" interrupt cause is read from the touch IC INT_CAUSE register. The read DMA in the HW sequencer is not running to read the touch data in this case. The non-DMA device inband interrupt status bit is set. SW is expected to read the device interrupt cause register and if it sees the 01 (touch data ready) is set, it could potentially read the touch device using PIO.
27:24	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
23:16	0h RW/V	**THC PRD CB Write Pointer for the 1st RXDMA (TPCWP):** The write pointer is updated by SW. The write pointer points to location in the DMA CB, where the next PRD table is going to be stored. SW needs to ensure that this pointer rolls over once the circular buffer's depth has been traversed with Bit[7] as the rollover bit. E.g. if the DMA CB depth is equal to 5 entries (0100b), then the write pointers will follow this pattern (SW is required to honor this behavior) 00h 01h 02h 03h 04h 80h 81h 82h 83h 84h 00h 01h ..
15:8	0h RO/V	**THC PRD CB Read Pointer for the 1st RXDMA (TPCRP):** DMA HW consumes the PRD tables in the CB, one PRD entry at a time until the EOP bit is found set in a PRD entry. At this point HW increments the PRD read pointer. Thus, the read pointer points to the PRD which the DMA engine is currently processing. This pointer rolls over once the circular buffer's depth has been traversed with bit[7] the Rollover bit. E.g. if the DMA CB depth is equal to 4 entries (0011b), then the read pointers will follow this pattern (HW is required to honor this behavior) 00h 01h 02h 03h 80h 81h 82h 83h 00h 01h ...
7	0h RW	**Interrupt Enable on DMA Completion for the 1st RXDMA (IE_DMACPL):** When set, interrupt is generated upon completion of DMA (DMACPL_STS=1).
6	0h RO	Reserved.
5	0h RW	**Interrupt Enable at EOF for the 1st RXDMA (IE_EOF):** When set, an interrupt will be generated when EOF is detected. For raw data mode, this occurs when all micro frames have been DMA'd. For HID mode, this occurs after each HID report is DMA'd.
4	0h RW	**Interrupt Enable on Non DMA Device Interrupt (IE_NDDI):** When set, an interrupt is generated to host SW when a non-DMA device inband interrupt is received.
3	0h RW	**Interrupt Enable on Stall for the 1st RXDMA (IE_STALL):** When set, an interrupt is generated to host SW when the CB read and write pointers are the same. This condition could be used to detect a stall of the GPU and subsequent buffer overrun internal to the Touch IC.
2	0h RW	**Interrupt Enable on Completion for the 1st RXDMA (IE_IOC):** When set, interrupt is generated upon completion of the PRD block transfer, with IOC=1, or when an error is encountered with the Error=1.
1	0h RW	**Interrupt Enable (IE) on Error for the 1st RXDMA (IE_ERROR):** When set, interrupt is generated upon an read DMA error is encountered.
0	0h RW/V	**Start for the 1st RXDMA (START):** SW sets the Start bit to arm the DMA engine. Once SW sets the Start bit it cannot modify entries in the PRD table. This gives HW the option of caching the PRD table for performance reasons. SW clears the bit after the DMA completion as indicated by interrupt and/or Status bits. SW can also clear the Start bit to abort an on-going DMA operation. DMA hardware completes all the outstanding requests to system memory and then stops the PRD actions at a safe point, e.g. at a microframe boundary so that it can resumed gracefully after SW set the start bit again. HW will clear this bit upon error conditions.

29.3.39 THC Read Interrupt Status for the 1st RXDMA (THC_M_PRT_READ_DMA_INT_STS_1)—Offset 1110h

THC Read DMA Interrupt Status Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RO/V	**Active status for the 1st RXDMA (ACTIVE):** DMA is active and not completed. Set by HW when the Start bit is set by SW and auto-cleared by HW in the following conditions: - The entire DMA operation has been completed or - The DMA operation has been halted by software clearing the Start bit (and no read completion pending).
7:6	0h RO	Reserved.
5	0h RW/1C/V	**Interrupt Status of EOF Interrupt for the 1st RXDMA (EOF_INT_STS):** Interrupt status when an EOF is encountered. If the IE_EOF bit is also 1, then an interrupt is generated. SW clears the bit by writing 1 to the bit.
4	0h RW/1C/V	**Interrupt Status of non DMA device interrupt (NONDMA_INT_STS):** Interrupt status when a non-DMA device inband interrupt is received. If the IE_NDDI bit is also 1, then an interrupt is generated. SW clears the bit by writing 1 to the bit.
3	0h RW/1C/V	**Interrupt Status of PRD table stalls for the 1st RXDMA (STALL_STS):** Interrupt status when the CB read and write pointers are the same and device sends moer touch data to THC. This condition could be used to detect a stall of the GPU and subsequent buffer overrun internal to the Touch IC. If the IE_STALL bit is also 1, then an interrupt is generated. SW clears the bit by writing 1 to the bit.
2	0h RW/1C/V	**Interrupt Status of PRD completion with IOC =1 for the 1st RXDMA (IOC_STS):** An PRD entry with IOC bit set has been completed during DMA operation. If the IE_IOC bit is also 1, then an interrupt is generated. SW clears the bit by writing 1 to the bit.
1	0h RW/1C/V	**Error status for the 1st RXDMA (ERROR_STS):** Error encountered during DMA operation. An interrupt is generated if the interrupt is enabled. SW clears the bit by writing 1 to the bit.
0	0h RW/1C/V	**DMA Complete for the 1st RXDMA (DMACPL_STS):** This bit is set upon successful completion of the DMA operation when the CB read and write pointers are the same. If the IE bit is also 1, then an interrupt is generated. SW clears the bit by writing 1 to the bit.

29.3.40 THC Read DMA Error Register for the 1st RXDMA (THC_M_PRT_READ_DMA_ERR_1)—Offset 1114h

THC Read DMA Error Register for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW/1C/V	**DMA Length Error for the 1st RXDMA (DLERR):** Indicates the raw data transfer request from the Touch IC is longer than allocated PRD entries accounted for. This error condition does not apply to SPI touch device.

29.3.41 Touch Sequencer GuC Tail Offset Address Low for the 1st RXDMA (THC_M_PRT_GUC_OFFSET_LOW_1)—Offset 1118h

Touch Sequencer GuC Tail Offset Address Low for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RW	**Touch Sequencer GuC Tail Offset Address Low for the 1st RXDMA (THC_M_PRT_GUC_OFFSET_LOW):** This register initializes the lower 32 bits of the 64 bit GuC tail offset address, OW aligned. The GuC Tail Offset is a 32 bit value, updated by the THC Controller to set the GuC circular buffer to the correct value. The 64 bit memory address containing the tail offset is allocated by the graphics driver and passed to the THC Controller Driver.
2:0	0h RO	Reserved.

29.3.42 Touch Sequencer GuC Tail Offset Address High for the 1st RXDMA (THC_M_PRT_GUC_OFFSET_HI_1)—Offset 111Ch

Touch Sequencer GuC Tail Offset Address HIGH for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Touch Sequencer GuC Tail Offset Address HIGH for the 1st RXDMA (THC_M_PRT_GUC_OFFSET_HI):** This register initializes the upper 32 bits of the 64 bit GuC tail offset address. The GuC Tail Offset is a 32 bit value, updated by the THC Controller to set the GuC circular buffer to the correct value. The 64 bit memory address containing the tail offset is allocated by the graphics driver and passed to the THC Controller Driver.

29.3.43 Touch Host Controller GuC Work Queue Item Size for the 1st RXDMA (THC_M_PRT_GUC_WORKQ_ITEM_SZ_1)—Offset 1120h

Touch Host Controller GuC Work Queue Item Size for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:0	0h RW	**Touch Host Controller GuC Work Queue Item Size for the 1st RXDMA (WORKQ_ITEM_SZ):** This register initializes the WorkQueueItemSz for the GuC processing algorithm

29.3.44 Touch Host Controller GuC Control register for the 1st RXDMA (THC_M_PRT_GUC_WORKQ_SZ_1)—Offset 1124h

Touch Host Controller GuC Control register for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:0	0h RW	**Guc Work Queue Size for the 1st RXDMA (WORKQ_SZ):** This register initializes the WorkQueueSz for the GuC processing algorithm

29.3.45 Touch Sequencer Control for the 1st DMA (THC_M_PRT_TSEQ_CNTRL_1)—Offset 1128h

Touch Sequencer Control for the 1st DMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RW/1S/V	**Reset Tail Offset for the 1st RXDMA (RTO):** SW writing this bit to a 0x1 resets the current TailOffset value (that is maintained as a result of the Tail Offset calculation) to 0x0. After HW has reset the tail offset to 0x0, HW resets RTO to 0x0.
3	0h RW	**Enable GuC Processing for the 1st RXDMA (EGP):** When this bit is set to 1b, the THC sequencer will execute the GuC processing flow when TOUCH_FRAME_CHAR.EOF=1 TOUCH_FRAME_CHAR.HDR=0.
2	0h RW/1S/V	**Reset GuC Doorbell for the 1st RXDMA (RGD):** SW Writing this bit to a 0x1, resets the GuC Doorbell to 0x1 (The doorbell can never be a value of 0x0). After HW has set the doorbell to 0x1, HW sets RGD to 0x0.
1:0	0h RO	Reserved.

29.3.46 Touch Sequencer GuC Doorbell Address Low for the 1st RXDMA (THC_M_PRT_GUC_DB_ADDR_LOW_1)—Offset 1130h

Touch Sequencer GuC Doorbell Address Low for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Touch Sequencer GuC Doorbell Address Low for the 1st RXDMA (GUC_DB_ADDR_LOW):** This register initializes the lower 32 bits of the 64 bit GuC doorbell address for the 1st RXDMA, which is required to be DW aligned.
1:0	0h RO	Reserved.

29.3.47 Touch Sequencer GuC Doorbell Address High for the 1st RXDMA (THC_M_PRT_GUC_DB_ADDR_HI_1)—Offset 1134h

Touch Sequencer GuC Doorbell Address High for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Touch Sequencer GuC Doorbell Address High for the 1st RXDMA (GUC_DB_ADDR_HI):** This register initializes the upper 32 bits of the 64 bit GuC doorbell address for the 1st RXDMA.

29.3.48 Touch Sequencer GuC Doorbell Data (THC_M_PRT_GUC_DB_DATA_1)—Offset 1138h

Touch Sequencer GuC Doorbell Data for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:0	1h RW/V	**Touch Sequencer GuC Doorbell Data for the 1st RXDMA (GUC_DB_DATA):** This register initializes the 32 bits of the GuC doorbell Data for the 1st RXDMA 1)This register is also changed when HW increments the value, AND 2)SW can only re-initialize it when RXDMA is stopped including during initialization.

29.3.49 Touch Sequencer GuC Tail Offset Initial Value for the 1st RXDMA (THC_M_PRT_GUC_OFFSET_INITVAL_1)—Offset 1140h

Touch Sequencer GuC Tail Offset Initial Value for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Touch Sequencer GuC Tail Offset Initial Value for the 1st RXDMA (THC_M_PRT_GUC_OFFSET_INITVAL):** This register initializes the initial value of the GuC tail offset. The GuC Tail Offset is a 32 bit value, updated by the THC Controller to set the GuC circular buffer to the correct value.

29.3.50 THC Device Address for the bulk/touch data read for the 1st RXDMA (THC_M_PRT_RD_BULK_ADDR_1)—Offset 1170h

THC Device Address for the bulk/touch data read for the 1st RXDMA

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 1000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	1000h RW/O	**THC Device Address for the bulk/touch data read for the 1st RXDMA (THC_M_PRT_RD_BULK_ADDR):** THC Device Address for the bulk/touch data read. In SPI mode, the touch data read cycles addresses start from the bulk address specified in this register and increment every packet until the end of the microframe. The touch read address resumes using the address in this register at the beginning of every new microframe. SW is responsible to program this register correctly, and make sure all resulting touch cycles will not exceed the touch device's bulk address space or roll over. Otherwise, THC's behavior is undefined. Note: For SPI devices, only 24bit addressing space is supported. Default to 0x1000.

29.3.51 THC Gfx/SW Doorbell Count from the 1st Stream RXDMA on this port (THC_M_PRT_DB_CNT_1)—Offset 11A0h

Touch Host Controller Doorbell Counter for the 1st RXDMA

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch Host Controller Doorbell Counter Reset for the 1st RXDMA (THC_M_PRT_DB_CNT_RST):** Reset the THC_M_PRT_DB_CNT counter. SW writing this bit to a 0x1, resets the THC_M_PRT_DB_CNT counter to a 0x0.HW clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch Host Controller Doorbell Counter for the 1st RXDMA (THC_M_PRT_DB_CNT):** Number of Touch Host Controller Doorbell sent on this port. The counter shall roll over back to 0 after reaching the maximum value.

29.3.52 THC Frame Count from the 1st Stream RXDMA on this port (THC_M_PRT_FRM_CNT_1)—Offset 11A4h

Touch Frame Counter

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch Frame Counter Reset (THC_M_PRT_FRM_CNT_RST):** Reset the THC_M_PRT_FRM_CNT counter. SW writing this bit to a 0x1, resets the THC_M_PRT_FRM_CNT counter to a 0x0.HW clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch Frame Counter (THC_M_PRT_FRM_CNT):** Number of Touch Frames received on this DMA engine, including the dropped frames. The counter shall roll over back to 0 after reaching the maximum value.

29.3.53 THC Micro Frame Count from the 1st Stream RXDMA on this port (THC_M_PRT_UFRM_CNT_1)—Offset 11A8h

Touch Microframe Counter for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch Microframe Counter Reset for the 1st RXDMA (THC_M_PRT_UFRM_CNT_RST):** Reset the THC_M_PRT_UFRM_CNT_1 counter. SW writing this bit to a 0x1, resets the THC_M_PRT_UFRM_CNT counter to a 0x0.HW clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch Microframe Counter for the 1st RXDMA (THC_M_PRT_UFRM_CNT):** Number of Touch Microframes received on this DMA stream. The counter shall roll over back to 0 after reaching the maximum value.

29.3.54 THC Packet Count from the 1st Stream RXDMA on this port (THC_M_PRT_RXDMA_PKT_CNT_1)—Offset 11ACh

Touch RX DMA Packet Counter for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch RX DMA Packet Counter Reset for the 1st RXDMA (THC_M_PRT_RXDMA_PKT_CNT_RST):** Reset the THC_M_PRT_RXDMA_PKT_CNT counter. SW writing this bit to a 0x1, resets the THC_M_PRT_RXDMA_PKT_CNT clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch RX DMA Packet Counter for the 1st RXDMA (THC_M_PRT_RXDMA_PKT_CNT):** Number of RX DMA Packet received on this DMA engine. The counter shall roll over back to 0 after reaching the maximum value.

29.3.55 THC Software Interrupt Count from the 1st Stream RXDMA on this port (THC_M_PRT_SWINT_CNT_1)—Offset 11B0h

Touch Host Controller Doorbell Counter for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch Host Controller Software Interrupt Counter Reset for the 1st RXDMA (THC_M_PRT_SWINT_CNT_RST):** Reset the THC_M_PRT_SWINT_CNT_1 counter. SW writing this bit to a 0x1, resets the THC_M_PRT_SWINT_CNT_1 counter to a 0x0.HW clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch Host Controller Interrupt Counter for the 1st RXDMA (THC_M_PRT_SWINT_CNT):** Number of Touch Host Controller Doorbell sent on this DMA engine. The counter shall roll over back to 0 after reaching the maximum value.

29.3.56 Touch Sequencer Frame Drop Counter for the 1st RXDMA (THC_M_PRT_FRAME_DROP_CNT_1)—Offset 11B4h

Touch Sequencer Frame Drop Counter for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Reset Frame Dropped Counter for the 1st RXDMA (RFDC):** SW writing this bit to a 0x1, resets the frame dropped counter, TSEQ_FRAME_DROP_CTR, to a 0x0. HW clears this bit to a 0x0 after the counter has been reset. SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Number of Frames Dropped for the 1st RXDMA (NOFD):** Number of Frames Dropped for the 1st RXDMA. When the counter reaches the maximum value, it shall be kept to the maximum value until the SW reset the counter using RFDC_1 bit.

29.3.57 THC Read PRD Base Address Low for the 2nd RXDMA (THC_M_PRT_RPRD_BA_LOW_2)—Offset 1200h

THC Read PRD Base Address for the 2nd RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**THC Read PRD Base Address for the 2nd RXDMA (THC_M_PRT_RPRD_BA_LOW):** This register initializes the lower 32 bits of the 64 bit PRD table base address for the 2nd RXDMA, 4K aligned, thus 20bits are allocated.
11:0	0h RO	Reserved.

29.3.58 THC Read PRD Base Address High for the 2nd RXDMA (THC_M_PRT_RPRD_BA_HI_2)—Offset 1204h

THC Read 2nd RXDMA PRD Base Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**2nd RXDMA PRD Base Address Hi (THC_M_PRT_RPRD_BA_HI):** This register initializes the upper 32 bits of the 64 bit PRD table base address..

29.3.59 THC Read PRD Control for the 2nd RXDMA (THC_M_PRT_RPRD_CNTRL_2)—Offset 1208h

THC Read PRD Control for the 2nd RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	0h RW	**Table Entry Count for the 2nd RXDMA (PTEC):** The number of PRD entries in each of the PRD tables held in the circular buffer. The PRD Entry Count must be large enough to contain the maximum raw data buffer size for any touch device. A fragmented data buffer could require a PRD entry for every 4KB of host memory allocated. In this case, for a 1MB raw data buffer, 128 PRD entries would be required. 00h: 1 PRD entry for each PRD Table 01h: 2 PRD entries for each PRD Table :: FFh: 256 PRD entries for each PRD Table
7	0h RO	Reserved.
6:0	0h RW	**CB Depth for the 2nd RXDMA (PCD):** This field indicates the number of PRD tables contained in the PRD address space. The filed directly corresponds to the number of raw data buffers used in the iTouch system. The raw data buffers are allocated by the host HID driver running in the OS. 00h: 1 PRD Table 01h: 2 PRD Table :: 7Fh: 128 PRD Tables For Example: iTouch allocates 16 PRD tables. Each PRD table need to address 1MB of address space, requiring 256 entries. 16 PRD Tables * 256 Entries/table * 16B per table == 64KB of PRD entries.

29.3.60 THC Read DMA Control for the 2nd RXDMA (THC_M_PRT_READ_DMA_CNTRL_2)—Offset 120Ch

THC Read DMA Control for the 2nd RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 40000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**THC PRD CB Pointer Reset for the 2nd RXDMA (TPCPR):** Setting this bit to a 1b resets DMA circular buffers read and write pointers to 00h. After the DMA CB pointers have been reset to 00h, hardware clears this bit to 0. SW can only reset tail offset when active and start are 0, i.e. DMA is idle.
30	1h RO	**Update HwStatus for the 2nd RXDMA (UHS):** If set, the HwStatus field of each PRD entry (for each PRD table) bit is updated (successful or error).
29	0h RW	**Stop on Overflow for the 2nd RXDMA (SOO):** When set, HW will clear the Start bit, upon detection of a DMA Buffer overflow, and stop read DMA operations. An overflow condition occurs when the read and write pointers contain the same value.
28	0h RW/L	**Interrupt SW Enable on DMA Device Interrupt for the 2nd RXDMA (INT_SW_DMA_EN):** When set to 1, an interrupt is generated to host SW even when a "touch data ready" interrupt cause is read from the touch IC INT_CAUSE register. The read DMA in the HW sequencer is not running to read the touch data in this case. The non-DMA device inband interrupt status bit is set. SW is expected to read the device interrupt cause register and if it sees the 01 (touch data ready) is set, it could potentially read the touch device using PIO.
27:24	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
23:16	0h RW/V	**THC PRD CB Write Pointer for the 2nd RXDMA (TPCWP):** The write pointer is updated by SW. The write pointer points to location in the DMA CB, where the next PRD table is going to be stored. SW needs to ensure that this pointer rolls over once the circular buffer's depth has been traversed with Bit[7] as the rollover bit. E.g. if the DMA CB depth is equal to 5 entries (0100b), then the write pointers will follow this pattern (SW is required to honor this behavior) 00h 01h 02h 03h 04h 80h 81h 82h 83h 84h 00h 01h ..
15:8	0h RO/V	**THC PRD CB Read Pointer for the 2nd RXDMA (TPCRP):** DMA HW consumes the PRD tables in the CB, one PRD entry at a time until the EOP bit is found set in a PRD entry. At this point HW increments the PRD read pointer. Thus, the read pointer points to the PRD which the DMA engine is currently processing. This pointer rolls over once the circular buffer's depth has been traversed with bit[7] the Rollover bit. E.g. if the DMA CB depth is equal to 4 entries (0011b), then the read pointers will follow this pattern (HW is required to honor this behavior) 00h 01h 02h 03h 80h 81h 82h 83h 00h 01h ...
7	0h RW	**Interrupt Enable on DMA Completion for the 2nd RXDMA (IE_DMACPL):** When set, interrupt is generated upon completion of DMA (DMACPL_STS=1).
6	0h RO	Reserved.
5	0h RW	**Interrupt Enable at EOF for the 2nd RXDMA (IE_EOF):** When set, an interrupt will be generated when EOF is detected. For raw data mode, this occurs when all micro frames have been DMA'd. For HID mode, this occurs after each HID report is DMA'd. When EGP is set, the interrupt occurs after GuC processing is complete.
4	0h RO	Reserved.
3	0h RW	**Interrupt Enable on Stall for the 2nd RXDMA (IE_STALL):** When set, an interrupt is generated to host SW when the CB read and write pointers are the same. This condition could be used to detect a stall of the GPU and subsequent buffer overrun internal to the Touch IC.
2	0h RW	**Interrupt Enable on Completion for the 2nd RXDMA (IE_IOC):** When set, interrupt is generated upon completion of the PRD block transfer, with IOC=1, or when an error is encountered with the Error=1.
1	0h RW	**Interrupt Enable on Error for the 2nd RXDMA (IE_ERROR):** When set, interrupt is generated upon an read DMA error is encountered.
0	0h RW/V	**Start for the 2nd RXDMA (START):** SW sets the Start bit to arm the DMA engine. Once SW sets the Start bit it cannot modify entries in the PRD table. This gives HW the option of caching the PRD table for performance reasons. SW clears the bit after the DMA completion as indicated by interrupt and/or Status bits. SW can also clear the Start bit to abort an on-going DMA operation. DMA hardware completes all the outstanding requests to system memory and then stops the PRD actions at a safe point, e.g. at a microframe boundary so that it can resumed gracefully after SW set the start bit again. HW will clear this bit upon error conditions.

29.3.61 THC Read Interrupt Status for the 2nd RXDMA (THC_M_PRT_READ_DMA_INT_STS_2)—Offset 1210h

THC Read Interrupt Status for the 2nd RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RO/V	**Active status bit for the 2nd RXDMA (ACTIVE):** DMA is active and not completed. Set by HW when the Start bit is set by SW and auto-cleared by HW in the following conditions: - The entire DMA operation has been completed or - The DMA operation has been halted by software clearing the Start bit (and no read completion pending).
7:6	0h RO	Reserved.
5	0h RW/1C/V	**Interrupt Status of EOF for the 2nd RXDMA (EOF_INT_STS):** Interrupt status when an EOF is encountered. If the IE_EOF bit is also 1, then an interrupt is generated. SW clears the bit by writing 1 to the bit.
4	0h RO	Reserved.
3	0h RW/1C/V	**Interrupt Status of PRD table stalls bit for the 2nd RXDMA (STALL_STS):** Interrupt status when the CB read and write pointers are the same. This condition could be used to detect a stall of the GPU and subsequent buffer overrun internal to the Touch IC. If the IE_STALL bit is also 1, then an interrupt is generated. SW clears the bit by writing 1 to the bit.
2	0h RW/1C/V	**Interrupt Status of PRD completion with IOC =1 for the 2nd RXDMA (IOC_STS):** An PRD entry with IOC bit set has been completed during DMA operation. If the IE_IOC bit is also 1, then an interrupt is generated. SW clears the bit by writing 1 to the bit.
1	0h RW/1C/V	**Error status bit for the 2nd RXDMA (ERROR_STS):** Error encountered during DMA operation. An interrupt is generated if the interrupt is enabled. SW clears the bit by writing 1 to the bit.
0	0h RW/1C/V	**DMA Complete bit for the 2nd RXDMA (DMACPL_STS):** This bit is set upon successful completion of the DMA operation. If the IE bit is also 1, then an interrupt is generated. SW clears the bit by writing 1 to the bit.

29.3.62 THC Read DMA Error Register for the 2nd RXDMA (THC_M_PRT_READ_DMA_ERR_2)—Offset 1214h

THC Read DMA Error Register for the 2nd RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW/1C/V	**DMA Length Error for the 2nd RXDMA (DLERR):** Indicates the raw data transfer request from the Touch IC is longer than allocated PRD entries accounted for. This error condition does not apply to SPI touch device.

29.3.63 Touch Sequencer GuC Tail Offset Address Low for the 2nd RXDMA (THC_M_PRT_GUC_OFFSET_LOW_2)—Offset 1218h

Touch Sequencer GuC Tail Offset Address Low for the 2nd RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RW	**Touch Sequencer GuC Tail Offset Address Low for the 2nd RXDMA (THC_M_PRT_GUC_OFFSET_LOW):** This register initializes the lower 32 bits of the 64 bit GuC tail offset address, OW aligned. The GuC Tail Offset is a 32 bit value, updated by the THC Controller to set the GuC circular buffer to the correct value. The 64 bit memory address containing the tail offset is allocated by the graphics driver and passed to the THC Controller Driver.
2:0	0h RO	Reserved.

29.3.64 Touch Sequencer GuC Tail Offset Address High for the 2nd RXDMA (THC_M_PRT_GUC_OFFSET_HI_2)—Offset 121Ch

Touch Sequencer GuC Tail Offset Address High for the 2nd RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Touch Sequencer GuC Tail Offset Address High for the 2nd RXDMA (THC_M_PRT_GUC_OFFSET_HI):** This register initializes the upper 32 bits of the 64 bit GuC tail offset address. The GuC Tail Offset is a 32 bit value, updated by the THC Controller to set the GuC circular buffer to the correct value. The 64 bit memory address containing the tail offset is allocated by the graphics driver and passed to the THC Controller Driver.

29.3.65 Touch Host Controller GuC Work Queue Item Size for the 2nd RXDMA (THC_M_PRT_GUC_WORKQ_ITEM_SZ_2)—Offset 1220h

Touch Host Controller GuC Work Queue Item Size for the 2nd RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:0	0h RW	**WORKQ_ITEM_SZ for the 2nd RXDMA (WORKQ_ITEM_SZ):** This register initializes the WorkQueueItemSz for the GuC processing algorithm for the 2nd RXDMA

29.3.66 Touch Host Controller GuC Control register for the 2nd RXDMA (THC_M_PRT_GUC_WORKQ_SZ_2)—Offset 1224h

Touch Host Controller GuC Control register for the 2nd RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:0	0h RW	**WORKQ_SZ for PRD2 (WORKQ_SZ):** This register initializes the WorkQueueSz for the GuC processing algorithm

29.3.67 Touch Sequencer Control for the 2nd DMA (THC_M_PRT_TSEQ_CNTRL_2)—Offset 1228h

Touch Sequencer Control for the 2nd DMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RW/1S/V	**Reset Tail Offset for the 2nd RXDMA (RTO):** SW writing this bit to a 0x1 resets the current TailOffset value (that is maintained as a result of the Tail Offset calculation) to 0x0. After HW has reset the tail offset to 0x0, HW resets RTO to 0x0.
3	0h RW	**Enable GuC Processing for the 2nd RXDMA (EGP):** When this bit is set to 1b, the THC sequencer will execute the GuC processing flow when TOUCH_FRAME_CHAR.EOF=1 TOUCH_FRAME_CHAR.HDR=0.
2	0h RW/1S/V	**Reset GuC Doorbell for the 2nd RXDMA (RGD):** SW Writing this bit to a 0x1, resets the GuC Doorbell to 0x1 (The doorbell can never be a value of 0x0). After HW has set the doorbell to 0x1, HW sets RGD to 0x0.
1:0	0h RO	Reserved.

29.3.68 Touch Sequencer GuC Doorbell Address Low for the 2nd RXDMA (THC_M_PRT_GUC_DB_ADDR_LOW_2)—Offset 1230h

Touch Sequencer GuC Doorbell Address Low for the 2nd RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Touch Sequencer GuC Doorbell Address Low for the 2nd RXDMA (GUC_DB_ADDR_LOW):** This register initializes the lower 32 bits of the 64 bit GuC doorbell address for the 2nd RXDMA, which is required to be DW aligned.
1:0	0h RO	Reserved.

29.3.69 Touch Sequencer GuC Doorbell Address High for the 2nd RXDMA (THC_M_PRT_GUC_DB_ADDR_HI_2)—Offset 1234h

Touch Sequencer GuC Doorbell Address High for the 2nd RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Touch Sequencer GuC Doorbell Address High for the 2nd RXDMA (GUC_DB_ADDR_HI):** This register initializes the upper 32 bits of the 64 bit GuC doorbell address for the 2nd RXDMA

29.3.70 Touch Sequencer GuC Doorbell Data for PRD2 (THC_M_PRT_GUC_DB_DATA_2)—Offset 1238h

Touch Sequencer GuC Doorbell Data for the 2nd RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:0	1h RW/V	**Touch Sequencer GuC Doorbell Data for the 2nd RXDMA (GUC_DB_DATA):** This register initializes the 32 bits of the GuC doorbell Data for the 2nd RXDMA. 1)This register is also changed when HW increments the value, AND 2)SW can only re-initialize it when RXDMA is stopped including during initialization.

29.3.71 Touch Sequencer GuC Tail Offset Initial Value for the 2nd RXDMA (THC_M_PRT_GUC_OFFSET_INITVAL_2)—Offset 1240h

Touch Sequencer GuC Tail Offset Initial Value for the 2nd RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Touch Sequencer GuC Tail Offset Initial Value for the 2nd RXDMA (THC_M_PRT_GUC_OFFSET_INITVAL):** This register initializes the initial value of the GuC tail offset. The GuC Tail Offset is a 32 bit value, updated by the THC Controller to set the GuC circular buffer to the correct value.

29.3.72 THC Device Address for the bulk/touch data read for the 2nd RXDMA (THC_M_PRT_RD_BULK_ADDR_2)—Offset 1270h

THC Device Address for the bulk/touch data read for the 2nd RXDMA

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 1000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	1000h RW/O	**THC Device Address for the bulk/touch data read for the 2nd RXDMA (THC_M_PRT_RD_BULK_ADDR):** THC Device Address for the bulk/touch data read. In SPI mode, the touch data read cycles addresses start from the bulk address specified in this register and increment every packet until the end of the microframe. The touch read address resumes using the address in this register at the beginning of every new microframe. SW is responsible to program this register correctly, and make sure all resulting touch cycles will not exceed the touch device's bulk address space or roll over. Otherwise, THC's behavior is undefined. Note: For SPI devices, only 24bit addressing space is supported. Default to 0x1000.

29.3.73 THC Gfx/SW Doorbell Count from the 2nd Stream RXDMA on this port (THC_M_PRT_DB_CNT_2)—Offset 12A0h

Touch Host Controller Doorbell Counter for the 2nd DMA engine

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch Host Controller Doorbell Counter Reset (THC_M_PRT_DB_CNT_RST):** Reset the THC_M_PRT_DB_CNT_2 counter. SW writing this bit to a 0x1, resets the THC_M_PRT_DB_CNT2 counter to a 0x0.HW clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch Host Controller Doorbell Counter (THC_M_PRT_DB_CNT):** Number of Touch Host Controller Doorbell sent on this port. The counter shall roll over back to 0 after reaching the maximum value.

29.3.74 THC Frame Count from the 2nd Stream RXDMA on this port (THC_M_PRT_FRM_CNT_2)—Offset 12A4h

Touch Frame Counter for the 2nd DMA engine

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch Frame Counter Reset (THC_M_PRT_FRM_CNT_RST):** Reset the THC_M_PRT_FRM_CNT_2 counter. SW writing this bit to a 0x1, resets the THC_M_PRT_FRM_CNT2 counter to a 0x0.HW clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch Frame Counter (THC_M_PRT_FRM_CNT):** Number of Touch Frames received on this DMA engine, including the dropped frames. The counter shall roll over back to 0 after reaching the maximum value.

29.3.75 THC Micro Frame Count from the 2nd Stream RXDMA on this port (THC_M_PRT_UFRM_CNT_2)—Offset 12A8h

Touch Microframe Counter for the 2nd DMA engine

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch Microframe Counter Reset for the 2nd DMA engine (THC_M_PRT_UFRM_CNT_RST):** Reset the THC_M_PRT_UFRM_CNT_2 counter. SW writing this bit to a 0x1, resets the THC_M_PRT_UFRM_CNT2 counter to a 0x0.HW clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch Microframe Counter for the 2nd DMA engine (THC_M_PRT_UFRM_CNT):** Number of Touch Microframes received on this DMA engine.The counter shall roll over back to 0 after reaching the maximum value.

29.3.76 THC Packet Count from the 2nd Stream RXDMA on this port (THC_M_PRT_RXDMA_PKT_CNT_2)—Offset 12ACh

Touch RX DMA Packet Counter for the 2nd DMA engine

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch RX DMA Packet Counter Reset (THC_M_PRT_RXDMA_PKT_CNT_RST):** Reset the THC_M_PRT_RXDMA_PKT_CNT2 counter. SW writing this bit to a 0x1, resets the THC_M_PRT_INT_CNTTHC_M_PRT_RXDMA_PKT_CNT2 clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch RX DMA Packet Counter (THC_M_PRT_RXDMA_PKT_CNT):** Number of RX DMA Packet received on this DMA engine. The counter shall roll over back to 0 after reaching the maximum value.

29.3.77 THC Software Interrupt Count from the 2nd Stream RXDMA on this port (THC_M_PRT_SWINT_CNT_2)—Offset 12B0h

Touch Host Controller Doorbell Counter for the 2nd DMA engine

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch Host Controller Software Interrupt Counter Reset (THC_M_PRT_SWINT_CNT_RST):** Reset the THC_M_PRT_SWINT_CNT2 counter. SW writing this bit to a 0x1, resets the THC_M_PRT_SWINT_CNT2 counter to a 0x0.HW clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch Host Controller Interrupt Counter (THC_M_PRT_SWINT_CNT):** Number of Touch Host Controller Doorbell sent on this DMA engine. The counter shall roll over back to 0 after reaching the maximum value.

29.3.78 Touch Sequencer Frame Drop Counter for the 2nd RXDMA (THC_M_PRT_FRAME_DROP_CNT_2)—Offset 12B4h

Touch Sequencer Frame Drop Counter for the 2nd RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Reset Frame Dropped Counter for the 2nd RXDMA (RFDC):** SW writing this bit to a 0x1, resets the frame dropped counter, TSEQ_FRAME_DROP_CTR, to a 0x0. HW clears this bit to a 0x0 after the counter has been reset. SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Number of Frames Dropped for the 2nd RXDMA (NOFD):** Number of Frames Dropped for the 2nd RXDMA. Number of Frames Dropped for the 1st RXDMA. When the counter reaches the maximum value, it shall be kept to the maximum value until the SW reset the counter using RFDC_2 bit.

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30 8254 Timer

30.1 8254 Timer Registers

Table 30-1. Summary of 8254 Timer Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
40h	40h	Counter 0 - Counter Access Ports Register (C0_CAPR)—Offset 40h	0h
40h	40h	Counter 0 - Interval Timer Status Byte Format Register (C0_ITSBFR)—Offset 40h	C4h
42h	42h	Counter 2 - Counter Access Ports Register (C2_CAPR)—Offset 42h	0h
42h	42h	Counter 2 - Interval Timer Status Byte Format Register (C2_ITSBFR)—Offset 42h	0h
43h	43h	Timer Control Word Register (TCW)—Offset 43h	0h
43h	43h	Read Back Command (RBC)—Offset 43h	C0h
43h	43h	Counter Latch Command (CLC)—Offset 43h	0h

30.1.1 Counter 0 - Counter Access Ports Register (C0_CAPR)—Offset 40h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW/V	**Counter Port (CP):** Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

30.1.2 Counter 0 - Interval Timer Status Byte Format Register (C0_ITSBFR)—Offset 40h

Each counter's status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for a given counter, the next read from the counter's Counter Access Ports Register (40h for counter 0 and 42h for counter 2) returns the status byte. The status byte returns the following:

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: C4h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RO	**Counter OUT Pin State (COPS):** When this bit is a 1, the OUT pin of the counter is also a 1. When this bit is a 0, the OUT pin of the counter is also a 0.
6	1h RO	**Count Register Status (CRSTS):** This bit indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the counter mode, but until the count is loaded into the counting element (CE), the count value will be incorrect. 0 Count has been transferred from CR to CE and is available for reading. 1 Null Count. Count has not been transferred from CR to CE and is not yet available for reading.
5:4	0h RO	**Read/Write Selection Status (RW_SLT_STS):** These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	2h RO	**Mode Selection Status (MD_SLT_STS):** These bits return the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	0h RO	**Countdown Type Status (CDT_STS):** This bit reflects the current countdown type, ether 0 for binary countdown or a 1 for binary coded decimal (BCD) countdown.

30.1.3 Counter 2 - Counter Access Ports Register (C2_CAPR)—Offset 42h

Same definition as Counter 0 - Counter Access Ports Register.

30.1.4 Counter 2 - Interval Timer Status Byte Format Register (C2_ITSBFR)—Offset 42h

Same definition as counter 0.

30.1.5 Timer Control Word Register (TCW)—Offset 43h

This register is programmed prior to any counter being accessed to specify counter modes. Following reset, the control words for each register are undefined and each counter output is 0. Each timer must be programmed to bring it into a known state. There are two special commands that can be issued to the counters through this register, the Read Back Command and the Counter Latch Command. When these commands are chosen, several bits within this register are redefined.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:6	0h WO	**Counter Select (CNT_SLT):** The Counter Selection bits select the counter the control word acts upon as shown below. The Read Back Command is selected when bits[7:6] are both 1 00 Counter 0 select 01 Reserved 10 Counter 2 select 11 Read Back Command
5:4	0h WO	**Read/Write Select: (RW_SLT):** These bits are the read/write control bits. The actual counter programming is done through the counter port (40h for counter 0 and 42h for counter 2) 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	0h WO	**Counter Mode Selection (CNT_MD_SLTN):** These bits select one of six possible modes of operation for the selected counter. 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	0h WO	**Binary/BCD Countdown Select (B_BCD_CNTDWN_SLT):** 0 Binary countdown is used. The largest possible binary count is 2^16 1 Binary coded decimal (BCD) count is used.The largest possible BCD count is 10^4

30.1.6 Read Back Command (RBC)—Offset 43h

The Read Back Command is used to determine the count value, programmed mode, and current states of the OUT pin and Null count flag of the selected counter or counters. Status and/or count may be latched in any or all of the counters by selecting the counter during the register write. The count and status remain latched until read, and further latch commands are ignored until the count is read.
Both count and status of the selected counters may be latched simultaneously by setting both bit 5 and bit 4 to 0. If both are latched, the first read operation from that counter returns the latched status. The next one or two reads, depending on whether the counter is programmed for one or two byte counts, returns the latched count. Subsequent reads return an unlatched count.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: C0h

Bit Range	Default and Access	Field Name (ID): Description
7:6	3h WO	**Read Back Command (RBC):** Must be 11 to select the Read Back Command
5	0h WO	**Latch Count of Selected Counters (LCSC):** 0 Current count value of the selected counters will be latched 1 Current count will not be latched
4	0h WO	**Latch Status of Selected Counters (LSSC):** 0 Status of the selected counters will be latched 1 Status will not be latched
3	0h WO	**Counter 2 Select (CNT_2_SLT):** When set to 1, Counter 2 count and/or status will be latched
2	0h RO	Reserved.
1	0h WO	**Counter 0 Select (CNT_0_SLT):** When set to 1, Counter 0 count and/or status will be latched.
0	0h RO	Reserved.

30.1.7 Counter Latch Command (CLC)—Offset 43h

The Counter Latch Command latches the current count value. This command is used to insure that the count read from the counter is accurate. The count value is then read from each counter's count register through the Counter Ports Access Ports Register (40h for counter 0 and 42h for counter 2). The count must be read according to the programmed format, i.e. if the counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other (read, write, or programming operations for other counters may be inserted between the reads). If a counter is latched once and then latched again before the count is read, the second Counter Latch Command is ignored.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:6	0h WO	**Counter Selection (CNT_SLT):** These bits select the counter for latching. If 11 is written, then the write is interpreted as a read back command. 00 = Counter 0 01 = Reserved 10 = Counter 2
5:4	0h WO	**Counter Latch Command (CLC):** Write 00 to select the Counter Latch Command.
3:0	0h RO	Reserved.

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31 Advanced Programmable Interrupt (APIC)

31.1 APIC Indirect Registers

APIC Indirect Registers lists the registers that can be accessed within the APIC using the Index Register. When accessing these registers, accesses must be done one DWord at a time. For example, software should never access byte 2 from the Data register before accessing bytes 0 and 1. The hardware will not attempt to recover from a bad programming model in this case.

Index	Mnemonic	Register Name
10-11h	RTE0	Redirection Table Entry 0
12-13h	RTE1	Redirection Table Entry 1
14-15h	RTE2	Redirection Table Entry 2
...	...	...
3E-3Fh	RTE23	Redirection Table Entry 23
40-41h	RTE24	Redirection Table Entry 24
...	...	...
FE-FFh	RTE119	Redirection Table Entry 119

Table 31-1. Summary of APIC Indirect Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Identification Register (ID)—Offset 0h	0h
1h	4h	Version Register (VER)—Offset 1h	770020h
10h	17h	Redirection Table Entry 0 (RTE0)—Offset 10h	10000h
12h	19h	Redirection Table Entry 1 (RTE1)—Offset 12h	0h
14h	1Bh	Redirection Table Entry 2 (RTE2)—Offset 14h	0h
16h	1Dh	Redirection Table Entry 3 (RTE3)—Offset 16h	0h
18h	1Fh	Redirection Table Entry 4 (RTE4)—Offset 18h	0h
1Ah	21h	Redirection Table Entry 5 (RTE5)—Offset 1Ah	0h
1Ch	23h	Redirection Table Entry 6 (RTE6)—Offset 1Ch	0h
1Eh	25h	Redirection Table Entry 7 (RTE7)—Offset 1Eh	0h
20h	27h	Redirection Table Entry 8 (RTE8)—Offset 20h	0h
22h	29h	Redirection Table Entry 9 (RTE9)—Offset 22h	0h
24h	2Bh	Redirection Table Entry 10 (RTE10)—Offset 24h	0h
26h	2Dh	Redirection Table Entry 11 (RTE11)—Offset 26h	0h
28h	2Fh	Redirection Table Entry 12 (RTE12)—Offset 28h	0h
2Ah	31h	Redirection Table Entry 13 (RTE13)—Offset 2Ah	0h
2Ch	33h	Redirection Table Entry 14 (RTE14)—Offset 2Ch	0h
2Eh	35h	Redirection Table Entry 15 (RTE15)—Offset 2Eh	0h
30h	37h	Redirection Table Entry 16 (RTE16)—Offset 30h	0h
32h	39h	Redirection Table Entry 17 (RTE17)—Offset 32h	0h
34h	3Bh	Redirection Table Entry 18 (RTE18)—Offset 34h	0h

Table 31-1. Summary of APIC Indirect Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
36h	3Dh	Redirection Table Entry 19 (RTE19)—Offset 36h	0h
38h	3Fh	Redirection Table Entry 20 (RTE20)—Offset 38h	0h
3Ah	41h	Redirection Table Entry 21 (RTE21)—Offset 3Ah	0h
3Ch	43h	Redirection Table Entry 22 (RTE22)—Offset 3Ch	0h
3Eh	45h	Redirection Table Entry 23 (RTE23)—Offset 3Eh	0h
40h	47h	Redirection Table Entry 24 (RTE24)—Offset 40h	0h
42h	49h	Redirection Table Entry 25 (RTE25)—Offset 42h	0h
44h	4Bh	Redirection Table Entry 26 (RTE26)—Offset 44h	0h
46h	4Dh	Redirection Table Entry 27 (RTE27)—Offset 46h	0h
48h	4Fh	Redirection Table Entry 28 (RTE28)—Offset 48h	0h
4Ah	51h	Redirection Table Entry 29 (RTE29)—Offset 4Ah	0h
4Ch	53h	Redirection Table Entry 30 (RTE30)—Offset 4Ch	0h
4Eh	55h	Redirection Table Entry 31 (RTE31)—Offset 4Eh	0h
50h	57h	Redirection Table Entry 32 (RTE32)—Offset 50h	0h
52h	59h	Redirection Table Entry 33 (RTE33)—Offset 52h	0h
54h	5Bh	Redirection Table Entry 34 (RTE34)—Offset 54h	0h
56h	5Dh	Redirection Table Entry 35 (RTE35)—Offset 56h	0h
58h	5Fh	Redirection Table Entry 36 (RTE36)—Offset 58h	0h
5Ah	61h	Redirection Table Entry 37 (RTE37)—Offset 5Ah	0h
5Ch	63h	Redirection Table Entry 38 (RTE38)—Offset 5Ch	0h
5Eh	65h	Redirection Table Entry 39 (RTE39)—Offset 5Eh	0h
60h	67h	Redirection Table Entry 40 (RTE40)—Offset 60h	0h
62h	69h	Redirection Table Entry 41 (RTE41)—Offset 62h	0h
64h	6Bh	Redirection Table Entry 42 (RTE42)—Offset 64h	0h
66h	6Dh	Redirection Table Entry 43 (RTE43)—Offset 66h	0h
68h	6Fh	Redirection Table Entry 44 (RTE44)—Offset 68h	0h
6Ah	71h	Redirection Table Entry 45 (RTE45)—Offset 6Ah	0h
6Ch	73h	Redirection Table Entry 46 (RTE46)—Offset 6Ch	0h
6Eh	75h	Redirection Table Entry 47 (RTE47)—Offset 6Eh	0h
70h	77h	Redirection Table Entry 48 (RTE48)—Offset 70h	0h
72h	79h	Redirection Table Entry 49 (RTE49)—Offset 72h	0h
74h	7Bh	Redirection Table Entry 50 (RTE50)—Offset 74h	0h
76h	7Dh	Redirection Table Entry 51 (RTE51)—Offset 76h	0h
78h	7Fh	Redirection Table Entry 52 (RTE52)—Offset 78h	0h
7Ah	81h	Redirection Table Entry 53 (RTE53)—Offset 7Ah	0h
7Ch	83h	Redirection Table Entry 54 (RTE54)—Offset 7Ch	0h
7Eh	85h	Redirection Table Entry 55 (RTE55)—Offset 7Eh	0h
80h	87h	Redirection Table Entry 56 (RTE56)—Offset 80h	0h
82h	89h	Redirection Table Entry 57 (RTE57)—Offset 82h	0h
84h	8Bh	Redirection Table Entry 58 (RTE58)—Offset 84h	0h

Table 31-1. Summary of APIC Indirect Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
86h	8Dh	Redirection Table Entry 59 (RTE59)—Offset 86h	0h
88h	8Fh	Redirection Table Entry 60 (RTE60)—Offset 88h	0h
8Ah	91h	Redirection Table Entry 61 (RTE61)—Offset 8Ah	0h
8Ch	93h	Redirection Table Entry 62 (RTE62)—Offset 8Ch	0h
8Eh	95h	Redirection Table Entry 63 (RTE63)—Offset 8Eh	0h
90h	97h	Redirection Table Entry 64 (RTE64)—Offset 90h	0h
92h	99h	Redirection Table Entry 65 (RTE65)—Offset 92h	0h
94h	9Bh	Redirection Table Entry 66 (RTE66)—Offset 94h	0h
96h	9Dh	Redirection Table Entry 67 (RTE67)—Offset 96h	0h
98h	9Fh	Redirection Table Entry 68 (RTE68)—Offset 98h	0h
9Ah	A1h	Redirection Table Entry 69 (RTE69)—Offset 9Ah	0h
9Ch	A3h	Redirection Table Entry 70 (RTE70)—Offset 9Ch	0h
9Eh	A5h	Redirection Table Entry 71 (RTE71)—Offset 9Eh	0h
A0h	A7h	Redirection Table Entry 72 (RTE72)—Offset A0h	0h
A2h	A9h	Redirection Table Entry 73 (RTE73)—Offset A2h	0h
A4h	ABh	Redirection Table Entry 74 (RTE74)—Offset A4h	0h
A6h	ADh	Redirection Table Entry 75 (RTE75)—Offset A6h	0h
A8h	AFh	Redirection Table Entry 76 (RTE76)—Offset A8h	0h
AAh	B1h	Redirection Table Entry 77 (RTE77)—Offset AAh	0h
ACh	B3h	Redirection Table Entry 78 (RTE78)—Offset ACh	0h
AEh	B5h	Redirection Table Entry 79 (RTE79)—Offset AEh	0h
B0h	B7h	Redirection Table Entry 80 (RTE80)—Offset B0h	0h
B2h	B9h	Redirection Table Entry 81 (RTE81)—Offset B2h	0h
B4h	BBh	Redirection Table Entry 82 (RTE82)—Offset B4h	0h
B6h	BDh	Redirection Table Entry 83 (RTE83)—Offset B6h	0h
B8h	BFh	Redirection Table Entry 84 (RTE84)—Offset B8h	0h
BAh	C1h	Redirection Table Entry 85 (RTE85)—Offset BAh	0h
BCh	C3h	Redirection Table Entry 86 (RTE86)—Offset BCh	0h
BEh	C5h	Redirection Table Entry 87 (RTE87)—Offset BEh	0h
C0h	C7h	Redirection Table Entry 88 (RTE88)—Offset C0h	0h
C2h	C9h	Redirection Table Entry 89 (RTE89)—Offset C2h	0h
C4h	CBh	Redirection Table Entry 90 (RTE90)—Offset C4h	0h
C6h	CDh	Redirection Table Entry 91 (RTE91)—Offset C6h	0h
C8h	CFh	Redirection Table Entry 92 (RTE92)—Offset C8h	0h
CAh	D1h	Redirection Table Entry 93 (RTE93)—Offset CAh	0h
CCh	D3h	Redirection Table Entry 94 (RTE94)—Offset CCh	0h
CEh	D5h	Redirection Table Entry 95 (RTE95)—Offset CEh	0h
D0h	D7h	Redirection Table Entry 96 (RTE96)—Offset D0h	0h
D2h	D9h	Redirection Table Entry 97 (RTE97)—Offset D2h	0h
D4h	DBh	Redirection Table Entry 98 (RTE98)—Offset D4h	0h

Table 31-1. Summary of APIC Indirect Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
D6h	DDh	Redirection Table Entry 99 (RTE99)—Offset D6h	0h
D8h	DFh	Redirection Table Entry 100 (RTE100)—Offset D8h	0h
DAh	E1h	Redirection Table Entry 101 (RTE101)—Offset DAh	0h
DCh	E3h	Redirection Table Entry 102 (RTE102)—Offset DCh	0h
DEh	E5h	Redirection Table Entry 103 (RTE103)—Offset DEh	0h
E0h	E7h	Redirection Table Entry 104 (RTE104)—Offset E0h	0h
E2h	E9h	Redirection Table Entry 105 (RTE105)—Offset E2h	0h
E4h	EBh	Redirection Table Entry 106 (RTE106)—Offset E4h	0h
E6h	EDh	Redirection Table Entry 107 (RTE107)—Offset E6h	0h
E8h	EFh	Redirection Table Entry 108 (RTE108)—Offset E8h	0h
EAh	F1h	Redirection Table Entry 109 (RTE109)—Offset EAh	0h
ECh	F3h	Redirection Table Entry 110 (RTE110)—Offset ECh	0h
EEh	F5h	Redirection Table Entry 111 (RTE111)—Offset EEh	0h
F0h	F7h	Redirection Table Entry 112 (RTE112)—Offset F0h	0h
F2h	F9h	Redirection Table Entry 113 (RTE113)—Offset F2h	0h
F4h	FBh	Redirection Table Entry 114 (RTE114)—Offset F4h	0h
F6h	FDh	Redirection Table Entry 115 (RTE115)—Offset F6h	0h
F8h	FFh	Redirection Table Entry 116 (RTE116)—Offset F8h	0h
FAh	101h	Redirection Table Entry 117 (RTE117)—Offset FAh	0h
FCh	103h	Redirection Table Entry 118 (RTE118)—Offset FCh	0h
FEh	105h	Redirection Table Entry 119 (RTE119)—Offset FEh	0h

31.1.1 Identification Register (ID)—Offset 0h

This APIC ID serves as a physical name of the APIC. The APIC bus arbitration ID for the APIC is derived from its I/O APIC ID. This register is reset to 0 on power-up reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:24	0h RW	**APIC Identification (AID):** Software must program this value before using the APIC.
23:16	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
15	0h RW	**Scratchpad (SPD):** Scratchpad Field
14:0	0h RO	Reserved.

31.1.2 Version Register (VER)—Offset 1h

Each I/O APIC contains a hardwired Version Register that identifies different implementation of APIC and their versions. The maximum redirection entry information is also in this register to let software know how many interrupt are supported by this APIC.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 770020h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:16	77h RW/O	**Maximum Redirection Entries (MRE):** This is the entry number (0 being the lowest entry) of the highest entry in the redirection table. It is equal to the number of interrupt input pins minus one and is in the range of 0 through 239. In PCH this field is defaulted to 17h to indicate 24 interrupts. This field is Read-Write-Once. BIOS must write to this field after PLTRST# to lockdown the value. This allows BIOS to utilize some of the entries for its own purpose and thus advertising fewer IOxAPIC Redirection Entries to OS. BIOS may to program this field up to 78h (maximum 120 entries).
15	0h RO	**Pin Assertion Register Supported (PRQ):** Indicate that the IOxAPIC does not implement the Pin Assertion Register.
14:8	0h RO	Reserved.
7:0	20h RO	**Version (VS):** Identifies the implementation version as IOxAPIC.

31.1.3 Redirection Table Entry 0 (RTE0)—Offset 10h

The Redirection Table has a dedicated entry for each interrupt input pin. The information in the Redirection Table is used to translate the interrupt manifestation on the corresponding interrupt pin into an APIC message.
The APIC will respond to an edge triggered interrupt as long as the interrupt is held until after the acknowledge cycle has begun. Once the interrupt is detected, a delivery status bit internally to the I/O APIC is set. The state machine will step ahead and wait for an acknowledgement from the APIC unit that the interrupt message was sent. Only then will the I/O APIC be able to recognize a new edge on that interrupt pin. That new

edge will only result in a new invocation of the handler if its acceptance by the destination APIC causes the Interrupt Request register bit to go from 0 to 1. (In other words, if the interrupt was not already pending a the destination.)

Access Method

Type: MEM Register (Size: 64 bits)

Device:
Function:

Default: 10000h

Bit Range	Default and Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** These bits are sent to a local APIC only when in Processor System Bus mode. They become bits 11:4 of the address.
47:17	0h RO	Reserved.
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts; its meaning is undefined for edge triggered interrupts. 0 = Reset when an EOI message is received that matches the VCT field. 1 = Set when IOxAPIC sends the level interrupt message to the CPU. Note, this bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported 011 Reserved 100 NMI Not supported 101 INIT Not supported 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

31.1.4 Redirection Table Entry 1 (RTE1)—Offset 12h

This register has the same bit definition as RTE0.

31.1.5 Redirection Table Entry 2 (RTE2)—Offset 14h

This register has the same bit definition as RTE0.

31.1.6 Redirection Table Entry 3 (RTE3)—Offset 16h

This register has the same bit definition as RTE0.

31.1.7 Redirection Table Entry 4 (RTE4)—Offset 18h

This register has the same bit definition as RTE0.

31.1.8 Redirection Table Entry 5 (RTE5)—Offset 1Ah

This register has the same bit definition as RTE0.

31.1.9 Redirection Table Entry 6 (RTE6)—Offset 1Ch

This register has the same bit definition as RTE0.

31.1.10 Redirection Table Entry 7 (RTE7)—Offset 1Eh

This register has the same bit definition as RTE0.

31.1.11 Redirection Table Entry 8 (RTE8)—Offset 20h

This register has the same bit definition as RTE0.

31.1.12 Redirection Table Entry 9 (RTE9)—Offset 22h

This register has the same bit definition as RTE0.

31.1.13 Redirection Table Entry 10 (RTE10)—Offset 24h

This register has the same bit definition as RTE0.

31.1.14 Redirection Table Entry 11 (RTE11)—Offset 26h

This register has the same bit definition as RTE0.

31.1.15 Redirection Table Entry 12 (RTE12)—Offset 28h

This register has the same bit definition as RTE0.

31.1.16 Redirection Table Entry 13 (RTE13)—Offset 2Ah

This register has the same bit definition as RTE0.

31.1.17 Redirection Table Entry 14 (RTE14)—Offset 2Ch

This register has the same bit definition as RTE0.

31.1.18 Redirection Table Entry 15 (RTE15)—Offset 2Eh

This register has the same bit definition as RTE0.

31.1.19 Redirection Table Entry 16 (RTE16)—Offset 30h

This register has the same bit definition as RTE0.

31.1.20 Redirection Table Entry 17 (RTE17)—Offset 32h

This register has the same bit definition as RTE0.

31.1.21 Redirection Table Entry 18 (RTE18)—Offset 34h

This register has the same bit definition as RTE0.

31.1.22 Redirection Table Entry 19 (RTE19)—Offset 36h

This register has the same bit definition as RTE0.

31.1.23 Redirection Table Entry 20 (RTE20)—Offset 38h

This register has the same bit definition as RTE0.

31.1.24 Redirection Table Entry 21 (RTE21)—Offset 3Ah

This register has the same bit definition as RTE0.

31.1.25 Redirection Table Entry 22 (RTE22)—Offset 3Ch

This register has the same bit definition as RTE0.

31.1.26 Redirection Table Entry 23 (RTE23)—Offset 3Eh

This register has the same bit definition as RTE0.

31.1.27 Redirection Table Entry 24 (RTE24)—Offset 40h

This register has the same bit definition as RTE0.

31.1.28 Redirection Table Entry 25 (RTE25)—Offset 42h

This register has the same bit definition as RTE0.

31.1.29 Redirection Table Entry 26 (RTE26)—Offset 44h

This register has the same bit definition as RTE0.

31.1.30 Redirection Table Entry 27 (RTE27)—Offset 46h

This register has the same bit definition as RTE0.

31.1.31 Redirection Table Entry 28 (RTE28)—Offset 48h

This register has the same bit definition as RTE0.

31.1.32 Redirection Table Entry 29 (RTE29)—Offset 4Ah

This register has the same bit definition as RTE0.

31.1.33 Redirection Table Entry 30 (RTE30)—Offset 4Ch

This register has the same bit definition as RTE0.

31.1.34 Redirection Table Entry 31 (RTE31)—Offset 4Eh

This register has the same bit definition as RTE0.

31.1.35 Redirection Table Entry 32 (RTE32)—Offset 50h

This register has the same bit definition as RTE0.

31.1.36 Redirection Table Entry 33 (RTE33)—Offset 52h

This register has the same bit definition as RTE0.

31.1.37 Redirection Table Entry 34 (RTE34)—Offset 54h

This register has the same bit definition as RTE0.

31.1.38 Redirection Table Entry 35 (RTE35)—Offset 56h

This register has the same bit definition as RTE0.

31.1.39 Redirection Table Entry 36 (RTE36)—Offset 58h

This register has the same bit definition as RTE0.

31.1.40 Redirection Table Entry 37 (RTE37)—Offset 5Ah

This register has the same bit definition as RTE0.

31.1.41 Redirection Table Entry 38 (RTE38)—Offset 5Ch

This register has the same bit definition as RTE0.

31.1.42 Redirection Table Entry 39 (RTE39)—Offset 5Eh

This register has the same bit definition as RTE0.

31.1.43 Redirection Table Entry 40 (RTE40)—Offset 60h

This register has the same bit definition as RTE0.

31.1.44 Redirection Table Entry 41 (RTE41)—Offset 62h

This register has the same bit definition as RTE0.

31.1.45 Redirection Table Entry 42 (RTE42)—Offset 64h

This register has the same bit definition as RTE0.

31.1.46 Redirection Table Entry 43 (RTE43)—Offset 66h

This register has the same bit definition as RTE0.

31.1.47 Redirection Table Entry 44 (RTE44)—Offset 68h

This register has the same bit definition as RTE0.

31.1.48 Redirection Table Entry 45 (RTE45)—Offset 6Ah

This register has the same bit definition as RTE0.

31.1.49 Redirection Table Entry 46 (RTE46)—Offset 6Ch

This register has the same bit definition as RTE0.

31.1.50 Redirection Table Entry 47 (RTE47)—Offset 6Eh

This register has the same bit definition as RTE0.

31.1.51 Redirection Table Entry 48 (RTE48)—Offset 70h

This register has the same bit definition as RTE0.

31.1.52 Redirection Table Entry 49 (RTE49)—Offset 72h

This register has the same bit definition as RTE0.

31.1.53 Redirection Table Entry 50 (RTE50)—Offset 74h

This register has the same bit definition as RTE0.

31.1.54 Redirection Table Entry 51 (RTE51)—Offset 76h

This register has the same bit definition as RTE0.

31.1.55 Redirection Table Entry 52 (RTE52)—Offset 78h

This register has the same bit definition as RTE0.

31.1.56 Redirection Table Entry 53 (RTE53)—Offset 7Ah

This register has the same bit definition as RTE0.

31.1.57 Redirection Table Entry 54 (RTE54)—Offset 7Ch

This register has the same bit definition as RTE0.

31.1.58 Redirection Table Entry 55 (RTE55)—Offset 7Eh

This register has the same bit definition as RTE0.

31.1.59 Redirection Table Entry 56 (RTE56)—Offset 80h

This register has the same bit definition as RTE0.

31.1.60 Redirection Table Entry 57 (RTE57)—Offset 82h

This register has the same bit definition as RTE0.

31.1.61 Redirection Table Entry 58 (RTE58)—Offset 84h

This register has the same bit definition as RTE0.

31.1.62 Redirection Table Entry 59 (RTE59)—Offset 86h

This register has the same bit definition as RTE0.

31.1.63 Redirection Table Entry 60 (RTE60)—Offset 88h

This register has the same bit definition as RTE0.

31.1.64 Redirection Table Entry 61 (RTE61)—Offset 8Ah

This register has the same bit definition as RTE0.

31.1.65 Redirection Table Entry 62 (RTE62)—Offset 8Ch

This register has the same bit definition as RTE0.

31.1.66 Redirection Table Entry 63 (RTE63)—Offset 8Eh

This register has the same bit definition as RTE0.

31.1.67 Redirection Table Entry 64 (RTE64)—Offset 90h

This register has the same bit definition as RTE0.

31.1.68 Redirection Table Entry 65 (RTE65)—Offset 92h

This register has the same bit definition as RTE0.

31.1.69 Redirection Table Entry 66 (RTE66)—Offset 94h

This register has the same bit definition as RTE0.

31.1.70 Redirection Table Entry 67 (RTE67)—Offset 96h

This register has the same bit definition as RTE0.

31.1.71 Redirection Table Entry 68 (RTE68)—Offset 98h

This register has the same bit definition as RTE0.

31.1.72 Redirection Table Entry 69 (RTE69)—Offset 9Ah

This register has the same bit definition as RTE0.

31.1.73 Redirection Table Entry 70 (RTE70)—Offset 9Ch

This register has the same bit definition as RTE0.

31.1.74 Redirection Table Entry 71 (RTE71)—Offset 9Eh

This register has the same bit definition as RTE0.

31.1.75 Redirection Table Entry 72 (RTE72)—Offset A0h

This register has the same bit definition as RTE0.

31.1.76 Redirection Table Entry 73 (RTE73)—Offset A2h

This register has the same bit definition as RTE0.

31.1.77 Redirection Table Entry 74 (RTE74)—Offset A4h

This register has the same bit definition as RTE0.

31.1.78 Redirection Table Entry 75 (RTE75)—Offset A6h

This register has the same bit definition as RTE0.

31.1.79 Redirection Table Entry 76 (RTE76)—Offset A8h

This register has the same bit definition as RTE0.

31.1.80 Redirection Table Entry 77 (RTE77)—Offset AAh

This register has the same bit definition as RTE0.

31.1.81 Redirection Table Entry 78 (RTE78)—Offset ACh

This register has the same bit definition as RTE0.

31.1.82 Redirection Table Entry 79 (RTE79)—Offset AEh

This register has the same bit definition as RTE0.

31.1.83 Redirection Table Entry 80 (RTE80)—Offset B0h

This register has the same bit definition as RTE0.

31.1.84 Redirection Table Entry 81 (RTE81)—Offset B2h

This register has the same bit definition as RTE0.

31.1.85 Redirection Table Entry 82 (RTE82)—Offset B4h

This register has the same bit definition as RTE0.

31.1.86 Redirection Table Entry 83 (RTE83)—Offset B6h

This register has the same bit definition as RTE0.

31.1.87 Redirection Table Entry 84 (RTE84)—Offset B8h

This register has the same bit definition as RTE0.

31.1.88 Redirection Table Entry 85 (RTE85)—Offset BAh

This register has the same bit definition as RTE0.

31.1.89 Redirection Table Entry 86 (RTE86)—Offset BCh

This register has the same bit definition as RTE0.

31.1.90 Redirection Table Entry 87 (RTE87)—Offset BEh

This register has the same bit definition as RTE0.

31.1.91 Redirection Table Entry 88 (RTE88)—Offset C0h

This register has the same bit definition as RTE0.

31.1.92 Redirection Table Entry 89 (RTE89)—Offset C2h

This register has the same bit definition as RTE0.

31.1.93 Redirection Table Entry 90 (RTE90)—Offset C4h

This register has the same bit definition as RTE0.

31.1.94 Redirection Table Entry 91 (RTE91)—Offset C6h

This register has the same bit definition as RTE0.

31.1.95 Redirection Table Entry 92 (RTE92)—Offset C8h

This register has the same bit definition as RTE0.

31.1.96 Redirection Table Entry 93 (RTE93)—Offset CAh

This register has the same bit definition as RTE0.

31.1.97 Redirection Table Entry 94 (RTE94)—Offset CCh

This register has the same bit definition as RTE0.

31.1.98 Redirection Table Entry 95 (RTE95)—Offset CEh

This register has the same bit definition as RTE0.

31.1.99 Redirection Table Entry 96 (RTE96)—Offset D0h

This register has the same bit definition as RTE0.

31.1.100 Redirection Table Entry 97 (RTE97)—Offset D2h

This register has the same bit definition as RTE0.

31.1.101 Redirection Table Entry 98 (RTE98)—Offset D4h

This register has the same bit definition as RTE0.

31.1.102 Redirection Table Entry 99 (RTE99)—Offset D6h

This register has the same bit definition as RTE0.

31.1.103 Redirection Table Entry 100 (RTE100)—Offset D8h

This register has the same bit definition as RTE0.

31.1.104 Redirection Table Entry 101 (RTE101)—Offset DAh

This register has the same bit definition as RTE0.

31.1.105 Redirection Table Entry 102 (RTE102)—Offset DCh

This register has the same bit definition as RTE0.

31.1.106 Redirection Table Entry 103 (RTE103)—Offset DEh

This register has the same bit definition as RTE0.

31.1.107 Redirection Table Entry 104 (RTE104)—Offset E0h

This register has the same bit definition as RTE0.

31.1.108 Redirection Table Entry 105 (RTE105)—Offset E2h

This register has the same bit definition as RTE0.

31.1.109 Redirection Table Entry 106 (RTE106)—Offset E4h

This register has the same bit definition as RTE0.

31.1.110 Redirection Table Entry 107 (RTE107)—Offset E6h

This register has the same bit definition as RTE0.

31.1.111 Redirection Table Entry 108 (RTE108)—Offset E8h

This register has the same bit definition as RTE0.

31.1.112 Redirection Table Entry 109 (RTE109)—Offset EAh

This register has the same bit definition as RTE0.

31.1.113 Redirection Table Entry 110 (RTE110)—Offset ECh

This register has the same bit definition as RTE0.

31.1.114 Redirection Table Entry 111 (RTE111)—Offset EEh

This register has the same bit definition as RTE0.

31.1.115 Redirection Table Entry 112 (RTE112)—Offset F0h

This register has the same bit definition as RTE0.

31.1.116 Redirection Table Entry 113 (RTE113)—Offset F2h

This register has the same bit definition as RTE0.

31.1.117 Redirection Table Entry 114 (RTE114)—Offset F4h

This register has the same bit definition as RTE0.

31.1.118 Redirection Table Entry 115 (RTE115)—Offset F6h

This register has the same bit definition as RTE0.

31.1.119 Redirection Table Entry 116 (RTE116)—Offset F8h

This register has the same bit definition as RTE0.

31.1.120 Redirection Table Entry 117 (RTE117)—Offset FAh

This register has the same bit definition as RTE0.

31.1.121 Redirection Table Entry 118 (RTE118)—Offset FCh

This register has the same bit definition as RTE0.

31.1.122 Redirection Table Entry 119 (RTE119)—Offset FEh

This register has the same bit definition as RTE0.

Advanced Programmable Interrupt Controller (APIC) Registers Index Register (IDX)—Offset

Table 31-2. Summary of Advanced Programmable Interrupt Controller (APIC) Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
FEC00000h	FEC00003h	Advanced Programmable Interrupt Controller (APIC) Registers Index Register (IDX)—Offset FEC00000h	0h
FEC00010h	FEC00013h	Access MethodDefault: 0hData Register (DAT)—Offset FEC00010h	0h
FEC00040h	FEC00043h	Access MethodDefault: 0hEOI Register (EOI)—Offset FEC00040h	0h

FEC00000h

The Index Register will select which APIC indirect register to be manipulated by software. Software will program this register to select the desired APIC internal register.

Access MethodDefault: 0hData Register (DAT)—Offset

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**Index Register (IDX):** This is an 8 bit pointer into the I/O APIC register table.

FEC00010h

This 32-bit register specifies the data to be read or written to the register pointed to by the Index register. This register can be accessed only in DW quantities.

Access MethodDefault: 0hEOI Register (EOI)—Offset FEC00040h

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Window Register (WDW):** This is a 32-bit register for the data to be read or written to the APIC indirect register pointed to by the Index register (Memory Address FEC0_0000h).

When a write is issued to this register, the IOxAPIC will check the lower 8 bits written to this register, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, RTE.RIRR for that entry will be cleared. If multiple entries have the same vector, each of those entries will have RTE.RIRR cleared. Only bits 7:0 are used. Bits 31:8 are ignored.

Access MethodDefault: 0h

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h WO	**EOI Register (EOI):** When a write is issued to this register, the I/O APIC will check this field and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, the Remote_IRR bit for that I/O Redirection Entry will be cleared.

31.2 Advanced Programmable Interrupt Controller (APIC) Registers

Table 31-3. Summary of Advanced Programmable Interrupt Controller (APIC) Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
FEC00000h	FEC00003h	Advanced Programmable Interrupt Controller (APIC) Registers Index Register (IDX)—Offset FEC00000h	0h
FEC00010h	FEC00013h	Data Register (DAT)—Offset FEC00010h	0h
FEC00040h	FEC00043h	EOI Register (EOI)—Offset FEC00040h	0h

Index Register (IDX)—Offset FEC00000h

The Index Register will select which APIC indirect register to be manipulated by software. Software will program this register to select the desired APIC internal register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**Index Register (IDX):** This is an 8 bit pointer into the I/O APIC register table.

31.2.1 Data Register (DAT)—Offset FEC00010h

his 32-bit register specifies the data to be read or written to the register pointed to by the Index register. This register can be accessed only in DW quantities.

Access Method

Type: MEM Register (Size: 32 bits)

Device:

Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Window Register (WDW):** This is a 32-bit register for the data to be read or written to the APIC indirect register pointed to by the Index register (Memory Address FEC0_0000h).

31.2.2 EOI Register (EOI)—Offset FEC00040h

When a write is issued to this register, the IOxAPIC will check the lower 8 bits written to this register, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, RTE.RIRR for that entry will be cleared. If multiple entries have the same vector, each of those entries will have RTE.RIRR cleared. Only bits 7:0 are used. Bits 31:8 are ignored.

Access Method

Type: MEM Register (Size: 32 bits)

Device:

Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h WO	**EOI Register (EOI):** When a write is issued to this register, the I/O APIC will check this field and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, the Remote_IRR bit for that I/O Redirection Entry will be cleared.

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32 Processor Interface

32.1 Processor Interface Memory Registers Summary

Table 32-1. Summary of Processor Interface Memory Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
61h	61h	NMI Status and Control (NMI_STS_CNT)—Offset 61h	0h
70h	70h	NMI Enable (and Real Time Clock Index) (NMI_EN)—Offset 70h	80h
92h	92h	Init Register (PORT92)—Offset 92h	0h
CF9h	CF9h	Reset Control Register (RST_CNT)—Offset CF9h	0h

32.1.1 NMI Status and Control (NMI_STS_CNT)—Offset 61h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7	0h RO	**SERR# NMI Source Status (SERR_NMI_STS):** This bit is set by any of the sources of the internal SERR on the PCH backbone, this includes SERR assertions forwarded from the secondary PCI bus,ssssssss error from a PCIe port, Do_SERR or standard PCIe error message from DMI, or internal Bus 0 functions that generate SERR#. Bit 2 must be cleared in this register in order for this bit to be set. This interrupt source is enabled by setting bit 2 to 0. To reset the interrupt, set bit 2 to 1 and then set it to 0. This bit is read-only. When writing to port 61h, this bit must be 0.
6	0h RO	**IOCHK# NMI Source Status (IOCHK_NMI_STS):** This bit is set if an ISA agent (via SERIRQ) asserts IOCHK# and bit 3 is cleared in this register. This interrupt source is enabled by setting bit 3 to 0. To reset the interrupt, set bit 3 to 1 and then set it to 0. This bit is read-only. When writing to port 61h, this bit must be a 0.
5	0h RO	**Timer Counter 2 OUT Status (TMR2_OUT_STS):** This bit reflects the current state of the 8254 counter 2 output. Counter 2 must be programmed following any PCI reset for this bit to have a determinate value. When writing to port 61h, this bit must be a 0.
4	0h RO	Reserved.
3	0h RW	**IOCHK# NMI Enable (IOCHK_NMI_EN):** When this bit is a 1, IOCHK# NMIs are disabled and cleared. When this bit is a 0, IOCHK# NMIs are enabled.
2	0h RW	**PCI SERR# Enable (PCI_SERR_EN):** When this bit is a 1, the SERR# NMIs are disabled and cleared. When this bit is a 0, SERR# NMIs are enabled.
1	0h RW	**Speaker Data Enable (SPKR_DAT_EN):** When this bit is a 0, the SPKR output is a 0. When this bit is a 1, the SPKR output is equivalent to the Counter 2 OUT signal value.
0	0h RW	**Timer Counter 2 Enable (TIM_CNT2_EN):** When this bit is a 0, Counter 2 counting is disabled. Counting is enabled when this bit is 1.

32.1.2 NMI Enable (and Real Time Clock Index) (NMI_EN)—Offset 70h

This register is write-only for normal operation. In Alt-Access mode, this register can be read to find the NMI Enable status and the RTC index value.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RW/V	**NMI_EN# (NMI_EN):** When this bit is a 1, all NMI sources are disabled. When this bit is a 0, NMI sources are enabled.
6:0	0h RW/V	**Real Time Clock Index (Address) (RTC_INDX):** This data goes to the RTC to select which register or CMOS RAM address is being accessed.

32.1.3 Init Register (PORT92)—Offset 92h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:1	0h RO	Reserved.
0	0h RW	**INIT NOW (INIT_NOW):** When this bit transitions from a 0 to a 1, the PCH will force INIT# active for 16 PCI clocks.

32.1.4 Reset Control Register (RST_CNT)—Offset CF9h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:4	0h RO	Reserved.
3	0h RW	**Full Reset (FULL_RST):** When this bit is set to 1 and bit 1 is set to 1 (indicating Hard Reset, not Soft Reset), and the RST_CPU bit (bit 2) is written from 0 to 1, the PCH will do a full reset, including driving SLP_S3#, SLP_S4# and SLP_S5# active (low) for at least 3 (and no more than 5) seconds. When this bit is set, it also causes the full power cycle (SLP_S3/4/5# assertion) in response to SYSRESET#, PWROK#, and Watchdog timer reset sources.
2	0h RW	**Reset CPU (RST_CPU):** This bit will cause either a hard or soft reset to the CPU depending on the state of the SYS_RST bit (bit 1 in this same register). The software will cause the reset by setting bit 2 from a 0 to a 1.
1	0h RW	**System Reset (SYS_RST):** The bit determines the type of reset caused via RST_CPU (bit 2 of this register). If SYS_RST is 0 when RST_CPU goes from 0 to 1, then the PCH will force INIT# active for 16 PCI clocks. If SYS_RST is 1 when RST_CPU goes from 0 to 1, then the PCH will force PCI reset active for about 1 ms, however the SLP_S3#, SLP_S4# and SLP_S5# signals assertion is dependent on the value of the FULL_RST (bit3 of this register).
0	0h RO	Reserved.

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33 General Purpose I/O (GPIO)

33.1 GPIO Community 0 Registers

This Section contains the GPIO registers of Community 0- 0x6E section.

Table 33-1. Summary of GPIO Community 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8h	4	Family Base Address (FAMBAR)	00000300h
Ch	4	Pad Base Address (PADBAR)	00000700h
10h	4	Miscellaneous Configuration (MISCCFG)	32043200h
20h	4	Pad Ownership (PAD_OWN_GPP_B_0)	00000000h
24h	4	Pad Ownership (PAD_OWN_GPP_B_1)	00000000h
28h	4	Pad Ownership (PAD_OWN_GPP_B_2)	00000000h
2Ch	4	Pad Ownership (PAD_OWN_GPP_B_3)	00000000h
38h	4	Pad Ownership (PAD_OWN_GPP_A_0)	00000000h
3Ch	4	Pad Ownership (PAD_OWN_GPP_A_1)	00000000h
40h	4	Pad Ownership (PAD_OWN_GPP_A_2)	00000000h
44h	4	Pad Ownership (PAD_OWN_GPP_A_3)	00000000h
80h	4	Pad Configuration Lock (PADCFGLOCK_GPP_B_0)	00000000h
84h	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_B_0)	00000000h
90h	4	Pad Configuration Lock (PADCFGLOCK_GPP_A_0)	00000000h
94h	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_A_0)	00000000h
B0h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_B_0)	00000000h
B8h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_A_0)	00000000h
100h	4	GPI Interrupt Status (GPI_IS_GPP_B_0)	00000000h
108h	4	GPI Interrupt Status (GPI_IS_GPP_A_0)	00000000h
120h	4	GPI Interrupt Enable (GPI_IE_GPP_B_0)	00000000h
128h	4	GPI Interrupt Enable (GPI_IE_GPP_A_0)	00000000h
140h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_B_0)	00000000h
148h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_0)	00000000h
160h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_B_0)	00000000h
168h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_0)	00000000h
180h	4	SMI Status (GPI_SMI_STS_GPP_B_0)	00000000h
188h	4	SMI Status (GPI_SMI_STS_GPP_A_0)	00000000h
1A0h	4	SMI Enable (GPI_SMI_EN_GPP_B_0)	00000000h
1A8h	4	SMI Enable (GPI_SMI_EN_GPP_A_0)	00000000h
1C0h	4	NMI Status (GPI_NMI_STS_GPP_B_0)	00000000h
1C8h	4	NMI Status (GPI_NMI_STS_GPP_A_0)	00000000h
1E0h	4	NMI Enable (GPI_NMI_EN_GPP_B_0)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1E8h	4	NMI Enable (GPI_NMI_EN_GPP_A_0)	00000000h
700h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_0)	44000700h
704h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_0)	00000018h
708h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_0)	00000000h
70Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_0)	00000000h
710h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_1)	44000700h
714h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_1)	00000019h
718h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_1)	00000000h
71Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_1)	00000000h
720h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_2)	44000300h
724h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_2)	0000001Ah
728h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_2)	00000000h
72Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_2)	00000000h
730h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_3)	44000300h
734h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_3)	0000001Bh
738h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_3)	00000000h
73Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_3)	00000000h
740h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_4)	44000300h
744h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_4)	0000001Ch
748h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_4)	00000000h
74Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_4)	00000000h
750h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_5)	44000300h
754h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_5)	0000001Dh
758h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_5)	00000000h
75Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_5)	00000000h
760h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_6)	44000300h
764h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_6)	0000001Eh
768h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_6)	00000000h
76Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_6)	00000000h
770h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_7)	44000300h
774h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_7)	0000001Fh
778h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_7)	00000000h
77Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_7)	00000000h
780h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_8)	44000300h
784h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_8)	00000020h
788h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_8)	00000000h
78Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_8)	00000000h
7B0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_11)	44000300h
7B4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_11)	00000023h
7B8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_11)	00000000h
7BCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_11)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
7C0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_12)	44000700h
7C4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_12)	00000024h
7C8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_12)	00000000h
7CCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_12)	00000000h
7D0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_13)	44000700h
7D4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_13)	00000025h
7D8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_13)	00000000h
7DCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_13)	00000000h
7E0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_14)	44000200h
7E4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_14)	00000026h
7E8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_14)	00000000h
7ECh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_14)	00000000h
7F0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_15)	44000300h
7F4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_15)	00000027h
7F8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_15)	00000000h
7FCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_15)	00000000h
800h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_16)	44000300h
804h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_16)	00000028h
808h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_16)	00000000h
80Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_16)	00000000h
810h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_17)	44000300h
814h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_17)	00000029h
818h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_17)	00000000h
81Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_17)	00000000h
820h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_18)	44000200h
824h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_18)	0000002Ah
828h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_18)	00000000h
82Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_18)	00000000h
874h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_23)	0000002Fh
878h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_23)	00000000h
87Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_23)	00000000h
9A0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_0)	44000700h
9A4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_0)	00003040h
9A8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_0)	00000100h
9ACh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_0)	00000000h
9B0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_1)	44000700h
9B4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_1)	00003041h
9B8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_1)	00000100h
9BCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_1)	00000000h
9C0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_2)	44000700h
9C4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_2)	00003042h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
9C8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_2)	00000100h
9CCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_2)	00000000h
9D0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_3)	44000700h
9D4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_3)	00003043h
9D8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_3)	00000100h
9DCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_3)	00000000h
9E0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_4)	44000700h
9E4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_4)	00003044h
9E8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_4)	00000100h
9ECh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_4)	00000000h
9F0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_5)	44000700h
9F4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_5)	00003045h
9F8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_5)	00000100h
9FCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_5)	00000000h
A00h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_6)	44000700h
A04h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_6)	00003046h
A08h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_6)	00000100h
A0Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_6)	00000000h
A10h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_7)	44000300h
A14h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_7)	00000047h
A18h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_7)	00000000h
A1Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_7)	00000000h
A20h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_8)	44000300h
A24h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_8)	00000048h
A28h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_8)	00000000h
A2Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_8)	00000000h
A30h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_9)	44000700h
A34h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_9)	00001049h
A38h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_9)	00000100h
A3Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_9)	00000000h
A40h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_10)	44000700h
A44h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_10)	0000004Ah
A48h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_10)	00000100h
A4Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_10)	00000000h
A50h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_11)	44000300h
A54h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_11)	0000004Bh
A58h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_11)	00000000h
A5Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_11)	00000000h
A60h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_12)	44000300h
A64h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_12)	0000004Ch
A68h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_12)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
A6Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_12)	00000000h
A70h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_13)	44000300h
A74h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_13)	0000004Dh
A78h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_13)	00000000h
A7Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_13)	00000000h
A80h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_14)	44000300h
A84h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_14)	0000004Eh
A88h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_14)	00000000h
A8Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_14)	00000000h
A90h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_15)	44000300h
A94h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_15)	0000004Fh
A98h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_15)	00000000h
A9Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_15)	00000000h
AA0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_16)	44000300h
AA4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_16)	00000050h
AA8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_16)	00000000h
AACh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_16)	00000000h
AB0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_17)	44000300h
AB4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_17)	00000051h
AB8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_17)	00000000h
ABCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_17)	00000000h
AC0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_18)	44000300h
AC4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_18)	00000052h
AC8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_18)	00000000h
ACCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_18)	00000000h
AD0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_19)	44000300h
AD4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_19)	00000053h
AD8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_19)	00000000h
ADCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_19)	00000000h
AE0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_20)	44000300h
AE4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_20)	00000054h
AE8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_20)	00000000h
AECh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_20)	00000000h
AF0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_21)	44000300h
AF4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_21)	00000055h
AF8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_21)	00000000h
AFCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_21)	00000000h
B00h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_22)	44000300h
B04h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_22)	00000056h
B08h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_22)	00000000h
B0Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_22)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
B10h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_23)	44000700h
B14h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_23)	00003057h
B18h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_23)	00000100h
B1Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_23)	00000000h

33.1.1 Family Base Address (FAMBAR) — Offset 8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 8h	00000300h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0300h RO	**Family Base Address (FAMBAR):** This field provides the starting byte-align address of Family0 register sets within a Community. It is meant for software to discover from where the very first Family register (i.e. Family0 register) starts to compute the next Families address offsets.

33.1.2 Pad Base Address (PADBAR) — Offset Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + Ch	00000700h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0700h RO	**Pad Base Address (PADBAR):** This field provides the starting byte-align address of Pad0 register sets within a Community. It is meant for software to discover from where the very first Pad register (i.e. Pad0 register) starts to compute the next Pad address offsets.

33.1.3 Miscellaneous Configuration (MISCCFG) — Offset 10h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 10h	32043200h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	32h RW	**GPIO Driver Mode Interrupt Select (GPDMINTSEL):** IRQ globally for all pads (GPI_IS with corresponding GPI_IE enable). 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255
23:20	0h RO	**Reserved**
19:16	4h RW	**GPIO Group to GPE_DW2 assignment encoding (GPE0_DW2):** This register assigns a specific GPIO Group to the ACPI GPE0[95:64]. The setting is SoC specific.
15:12	3h RW	**GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1):** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The setting is SoC specific.
11:8	2h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0):** This register assigns a specific GPIO Group to the ACPI GPE0[31:0]. The setting is SoC specific.
7	0h RW	**GPIO IOSF Sideband VNNREQ Enable (GPVNNREQEN):** Specify whether the GPIO Community should take part in IOSFSB VNNREQ/ACK handshake 0 = Disable participation in IOSF SB VNNREQ and VNNACK handshake 1 = Enable participation in IOSF SB VNNREQ and VNNACK handshake When this bit set to 1, GPIO controller will de-assert the VNNREQ when there is no outstanding IOSF SB upstream cycle from GPIO controller. When this bit set to 1 and MISCSECCFG.SBTRIGDIS is 0, GPIO controller will assert the VNNREQ to request for the following list of IOSF-SB Message initiation. Event list: IRQ NMI SMI SSMI VNNREQ shall de-assert when MISCSECCFG.SBTRIGDIS is set to 1. As VNNAON IP, GPIO controller will assert the VNNREQ when in reset. The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pwrgate_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this power gating, this register always default to 1.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**GPIO PGCB Clock Dynamic Partition Clock Gating Enable (GPPGCBDPCGEN):** Specify whether the GPIO Community PGCB clock should take part in partition clock gating 0 = Disable participation in PGCB clock dynamic partition clock gating 1 = Enable participation in PGCB clock dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
5	0h RW	**GPIO IOSF Sideband Dynamic Partition Clock Gating Enable (GPSIDEDPCGEN):** Specify whether the GPIO Community IOSF sideband clock should take part in partition clock gating 0 = Disable participation in IOSF sideband clock dynamic partition clock gating 1 = Enable participation in IOSF sideband clock dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
4	0h RW	**GPIO RCOMP clock Dynamic Local Clock Gating (GPRCOMPCDLCGEN):** Specify whether the GPIO Community should perform local clock gating on RCOMP clock 0 = Disable dynamic RCOMP clock local clock gating 1 = Enable dynamic RCOMP clock local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
3	0h RW	**GPIO RTC clock Dynamic Local Clock Gating (GPRTCDLCGEN):** Specify whether the GPIO Community should perform local clock gating on RTC clock 0 = Disable dynamic RTC clock local clock gating 1 = Enable dynamic RTC clock local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GSX Static Local Clock Gating (GSXSLCGEN):** Specify whether the GSX controller should be statically clock gated for power saving if it is not enabled (even though the capability is available). 0 = Disable static local clock gating 1 = Enable static local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
1	0h RW	**GPIO Dynamic Partition Clock Gating Enable (GPDPCGEN):** Specify whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
0	0h RW	**GPIO Dynamic Local Clock Gating Enable (GPDLCGEN):** Specify whether the GPIO Community should perform local clock gating 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0

33.1.4 Pad Ownership (PAD_OWN_GPP_B_0) — Offset 20h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 20h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_7):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_6):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_5):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_4):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.1.5 Pad Ownership (PAD_OWN_GPP_B_1) — Offset 24h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 24h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_15):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_14):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_13):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_12):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_11):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
11:10	0h RO	**Reserved**
9:8	0h RW	**Reserved**
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Reserved**
3:2	0h RO	**Reserved**
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_8):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.1.6 Pad Ownership (PAD_OWN_GPP_B_2) — Offset 28h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 28h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_23):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:26	0h RO	**Reserved**
25:24	0h RW	**Reserved**
23:22	0h RO	**Reserved**
21:20	0h RW	**Reserved**
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Reserved**
15:14	0h RO	**Reserved**
13:12	0h RW	**Reserved**
11:10	0h RO	**Reserved**
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_18):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_17):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_16):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.1.7 Pad Ownership (PAD_OWN_GPP_B_3) — Offset 2Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 2Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5:4	0h RO	**Reserved**
3:2	0h RO	**Reserved**
1:0	0h RO	**Reserved**

33.1.8 Pad Ownership (PAD_OWN_GPP_A_0) — Offset 38h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 38h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_7):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_6):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_5):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_4):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.1.9 Pad Ownership (PAD_OWN_GPP_A_1) — Offset 3Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 3Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_15):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_14):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_13):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_12):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_11):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_10):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_9):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_8):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.1.10 Pad Ownership (PAD_OWN_GPP_A_2) — Offset 40h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 40h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_23):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_22):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_21):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_20):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_19):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_18):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_17):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_A_16):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.1.11 Pad Ownership (PAD_OWN_GPP_A_3) — Offset 44h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 44h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**Reserved**

33.1.12 Pad Configuration Lock (PADCFGLOCK_GPP_B_0) — Offset 80h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 80h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_23):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
22	0h RW	**Reserved**
21	0h RW	**Reserved**
20	0h RW	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Reserved**
18	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_18):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
17	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_17):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_16):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
15	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_15):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_14):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
13	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_13):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_12):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_11):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
10	0h RW	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Reserved**
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_8):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_7):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_6):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_5):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_4):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

33.1.13 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_B_0) — Offset 84h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 84h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**Pad Config Lock TXState (PADCFGLOCKTX_GSPI1_CLK_LOOPBK):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
24	0h RO	**Pad Config Lock TXState (PADCFGLOCKTX_GSPI0_CLK_LOOPBK):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_23):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
22	0h RW	**Reserved**
21	0h RW	**Reserved**
20	0h RW	**Reserved**
19	0h RW	**Reserved**
18	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_18):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_17):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
16	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_16):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_15):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
14	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_14):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_13):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
12	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_12):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_11):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
10	0h RW	**Reserved**
9	0h RW	**Reserved**
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_8):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_7):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_6):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_5):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_4):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

33.1.14 Pad Configuration Lock (PADCFGLOCK_GPP_A_0) — Offset 90h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 90h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_23):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
22	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_22):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
21	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_21):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_20):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
19	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_19):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_18):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
17	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_17):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_16):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
15	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_15):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_14):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
13	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_13):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_12):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_11):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_10):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_9):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_8):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_7):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_6):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_5):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_4):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

33.1.15 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_A_0) — Offset 94h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 94h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Pad Config Lock TXState (PADCFGLOCKTX_ESPI_CLK_LOOPBK):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
23	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_23):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
22	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_22):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
21	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_21):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_20):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
19	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_19):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_18):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
17	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_17):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_16):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
15	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_15):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_14):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
13	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_13):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_12):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_11):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_10):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_9):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_8):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_7):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_6):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_5):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_4):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

33.1.16 Host Software Pad Ownership (HOSTSW_OWN_GPP_B_0) — Offset B0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**Reserved**
24	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**HOSTSW_OWN_GPPC_B_23:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
22	0h RW	**Reserved**
21	0h RW	**Reserved**
20	0h RW	**Reserved**
19	0h RW	**Reserved**
18	0h RW	**HOSTSW_OWN_GPPC_B_18:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**HOSTSW_OWN_GPPC_B_17:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
16	0h RW	**HOSTSW_OWN_GPPC_B_16:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
15	0h RW	**HOSTSW_OWN_GPPC_B_15:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**HOSTSW_OWN_GPPC_B_14:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
13	0h RW	**HOSTSW_OWN_GPPC_B_13:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
12	0h RW	**HOSTSW_OWN_GPPC_B_12:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**HOSTSW_OWN_GPPC_B_11:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
10	0h RW	Reserved
9	0h RW	Reserved
8	0h RW	**HOSTSW_OWN_GPPC_B_8:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
7	0h RW	**HOSTSW_OWN_GPPC_B_7:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**HOSTSW_OWN_GPPC_B_6:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
5	0h RW	**HOSTSW_OWN_GPPC_B_5:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
4	0h RW	**HOSTSW_OWN_GPPC_B_4:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**HOSTSW_OWN_GPPC_B_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HOSTSW_OWN_GPPC_B_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RW	**HOSTSW_OWN_GPPC_B_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RW	**HOSTSW_OWN_GPPC_B_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

33.1.17 Host Software Pad Ownership (HOSTSW_OWN_GPP_A_0) — Offset B8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**HOSTSW_OWN_GPPC_A_23:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
22	0h RW	**HOSTSW_OWN_GPPC_A_22:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**HOSTSW_OWN_GPPC_A_21:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
20	0h RW	**HOSTSW_OWN_GPPC_A_20:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
19	0h RW	**HOSTSW_OWN_GPPC_A_19:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**HOSTSW_OWN_GPPC_A_18:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
17	0h RW	**HOSTSW_OWN_GPPC_A_17:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
16	0h RW	**HOSTSW_OWN_GPPC_A_16:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**HOSTSW_OWN_GPPC_A_15:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
14	0h RW	**HOSTSW_OWN_GPPC_A_14:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
13	0h RW	**HOSTSW_OWN_GPPC_A_13:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**HOSTSW_OWN_GPPC_A_12:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
11	0h RW	**HOSTSW_OWN_GPPC_A_11:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
10	0h RW	**HOSTSW_OWN_GPPC_A_10:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**HOSTSW_OWN_GPPC_A_9:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
8	0h RW	**HOSTSW_OWN_GPPC_A_8:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
7	0h RW	**HOSTSW_OWN_GPPC_A_7:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**HOSTSW_OWN_GPPC_A_6:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
5	0h RW	**HOSTSW_OWN_GPPC_A_5:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
4	0h RW	**HOSTSW_OWN_GPPC_A_4:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**HOSTSW_OWN_GPPC_A_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HOSTSW_OWN_GPPC_A_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RW	**HOSTSW_OWN_GPPC_A_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RW	**HOSTSW_OWN_GPPC_A_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

33.1.18 GPI Interrupt Status (GPI_IS_GPP_B_0) — Offset 100h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 100h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_23):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
22	0h RW/1C	**Reserved**
21	0h RW/1C	**Reserved**
20	0h RW/1C	**Reserved**
19	0h RW/1C	**Reserved**
18	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_18):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_17):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
16	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_16):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
15	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_15):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_14):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_13):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_12):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_11):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW/1C	**Reserved**
9	0h RW/1C	**Reserved**
8	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_8):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_7):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_6):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_5):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_4):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.1.19 GPI Interrupt Status (GPI_IS_GPP_A_0) — Offset 108h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 108h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_23):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
22	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_22):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_21):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
20	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_20):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
19	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_19):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_18):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
17	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_17):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
16	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_16):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_15):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_14):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_13):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_12):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
11	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_11):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_10):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_9):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
8	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_8):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_7):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_6):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_5):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_4):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.1.20 GPI Interrupt Enable (GPI_IE_GPP_B_0) — Offset 120h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 120h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_23):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
22	0h RW	**Reserved**
21	0h RW	**Reserved**
20	0h RW	**Reserved**
19	0h RW	**Reserved**
18	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_18):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_17):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
16	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_16):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
15	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_15):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_14):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_13):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_12):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_11):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW	**Reserved**
9	0h RW	**Reserved**
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_8):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_7):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_6):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_5):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_4):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.1.21 GPI Interrupt Enable (GPI_IE_GPP_A_0) — Offset 128h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 128h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_23):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
22	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_22):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
21	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_21):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_20):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
19	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_19):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
18	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_18):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
17	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_17):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_16):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
15	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_15):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_14):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_13):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_12):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_11):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_10):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_9):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_8):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_7):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_6):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_5):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_4):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.1.22 GPI General Purpose Events Status (GPI_GPE_STS_GPP_B_0) — Offset 140h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 140h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_23):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
22	0h RW/1C	**Reserved**
21	0h RW/1C	**Reserved**
20	0h RW/1C	**Reserved**
19	0h RW/1C	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_18):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
17	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_17):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
16	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_16):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_15):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_14):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
13	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_13):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_12):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_11):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW/1C	Reserved
9	0h RW/1C	Reserved
8	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_8):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_7):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_6):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_5):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_4):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.1.23 GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_0) — Offset 148h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 148h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_23):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
22	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_22):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_21):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
20	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_20):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
19	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_19):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_18):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
17	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_17):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
16	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_16):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_15):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_14):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
13	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_13):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_12):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_11):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_10):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_9):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_8):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_7):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_6):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_5):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_4):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.1.24 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_B_0) — Offset 160h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 160h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_23):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
22	0h RW	**Reserved**
21	0h RW	**Reserved**
20	0h RW	**Reserved**
19	0h RW	**Reserved**
18	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_18):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_17):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
16	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_16):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
15	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_15):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_14):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_13):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
12	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_12):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_11):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW	**Reserved**
9	0h RW	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_8):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_7):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_6):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_5):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_4):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.1.25 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_0) — Offset 168h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 168h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_23):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
22	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_22):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
21	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_21):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_20):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
19	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_19):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
18	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_18):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
17	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_17):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_16):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
15	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_15):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_14):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
13	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_13):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_12):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_11):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_10):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_9):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_8):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_7):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_6):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_5):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_4):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.1.26 SMI Status (GPI_SMI_STS_GPP_B_0) — Offset 180h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 180h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_B_23):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
22	0h RO	**Reserved**
21	0h RO	**Reserved**
20	0h RW/1C	**Reserved**
19	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_18):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
17	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_17):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_16):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
15	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_15):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_B_14):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
13	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_13):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_12):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
11	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_11):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
10	0h RO	Reserved
9	0h RO	Reserved

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_8):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
7	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_7):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_6):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
5	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_5):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_4):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
3	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_B_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

33.1.27 SMI Status (GPI_SMI_STS_GPP_A_0) — Offset 188h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 188h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RSV	**Reserved**
23	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_23):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
22	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_22):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_21):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
20	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_20):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_19):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
18	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_18):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_17):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
16	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_16):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_15):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
14	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_14):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_13):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
12	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_12):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_11):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
10	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_10):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_9):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
8	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_8):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_7):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
6	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_6):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_5):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
4	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_4):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_A_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

33.1.28 SMI Enable (GPI_SMI_EN_GPP_B_0) — Offset 1A0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 1A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**Reserved**
24	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_23):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
22	0h RO	**Reserved**
21	0h RO	**Reserved**
20	0h RW	**Reserved**
19	0h RO	**Reserved**
18	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_18):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
17	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_17):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
16	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_16):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
15	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_15):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
14	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_14):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_13):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
12	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_12):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
11	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_11):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
10	0h RO	**Reserved**
9	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_8):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
7	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_7):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
6	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_6):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_5):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
4	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_4):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
3	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

33.1.29 SMI Enable (GPI_SMI_EN_GPP_A_0) — Offset 1A8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 1A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RSV	**Reserved**
23	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_23):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
22	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_22):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
21	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_21):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
20	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_20):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
19	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_19):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
18	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_18):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
17	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_17):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
16	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_16):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_15):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
14	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_14):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
13	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_13):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_12):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
11	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_11):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
10	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_10):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_9):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
8	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_8):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
7	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_7):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_6):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
5	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_5):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
4	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_4):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_A_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

33.1.30 NMI Status (GPI_NMI_STS_GPP_B_0) — Offset 1C0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 1C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_B_23):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
22	0h RO	**Reserved**
21	0h RO	**Reserved**
20	0h RW/1C	**Reserved**
19	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_18):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
17	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_17):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_16):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_15):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_B_14):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_13):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_12):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_11):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RO	**Reserved**
9	0h RO	**Reserved**
8	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_8):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_7):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_6):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_5):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_4):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_B_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.1.31 NMI Status (GPI_NMI_STS_GPP_A_0) — Offset 1C8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 1C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RSV	**Reserved**
23	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_23):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
22	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_22):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_21):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
20	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_20):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
19	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_19):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_18):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
17	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_17):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_16):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_15):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_14):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_13):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_12):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_11):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_10):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_9):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
8	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_8):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_7):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_6):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_5):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_4):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_A_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.1.32 NMI Enable (GPI_NMI_EN_GPP_B_0) — Offset 1E0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 1E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_23):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
22	0h RO	**Reserved**
21	0h RO	**Reserved**
20	0h RW	**Reserved**
19	0h RO	**Reserved**
18	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_18):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_17):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_16):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
15	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_15):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_14):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_13):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
12	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_12):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_11):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RO	**Reserved**
9	0h RO	**Reserved**
8	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_8):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_7):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_6):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_5):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_4):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.1.33 NMI Enable (GPI_NMI_EN_GPP_A_0) — Offset 1E8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 1E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RSV	**Reserved**
23	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_23):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
22	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_22):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_21):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
20	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_20):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
19	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_19):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_18):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
17	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_17):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_16):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_15):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_14):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_13):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_12):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_11):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_10):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_9):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
8	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_8):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_7):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_6):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_5):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_4):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_A_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.1.34 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_0) — Offset 700h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 700h	44000700h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the SoC responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)

Bit Range	Default & Access	Field Name (ID): Description
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

33.1.35 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_0) — Offset 704h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 704h	00000018h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0100: 20k PD 1100: 20k PU 1111: Native controller selected by Pad Mode controls the Termination. This field should be set to 1111b for the selected native function that supports dynamic termination override. Refer to Vol1, GPIO chapter, for more info. Others: Reserved **Notes**: 1. The 20K pull-up/pull-down can only be enabled as long as the toggle rate on the signal is no more than 300KHz. 2. If a reserved value is programmed, pad may malfunction. 3. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, PU/PD settings should be programmed first to ensure the input does not float momentarily
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	18h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

33.1.36 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_0) — Offset 708h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 708h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:25	0h RO	**SoundWire Slew Control (sndwslewctrl) (SNDWSLEWCTRL):** 00 = Slow Slew Rate 01 = Middle Slew Rate 10 = Fast Slew Rate 11 = Fastest Slew Rate For iCDG buffers, this field is used to control the slew configuration, but extends beyond SoundWire to I2C, SDMMC and other applicable buffers. The setting may vary from one platform to another.
24	0h RO	**Bus Hold Enable (BUSHLDEN):** This feature uses the same build in pull-up/down resistor. In such, BIOS/FW needs to disable all pull-up/down to 'None' before enabling this feature. 1 = enable bus hold 0 = disable bus hold
23	0h RO	**Data Dependent Weak PU Control (DDPUCTRL):** 0 = normal I/O transmission mode. 1 = weak pull up configuration is overridden to disabled, when the raw RX pad state is 0 in output mode. During DFx mode like BSCAN, SCAN, HVM and etc, the DDPUCRTL shall be constrained to 0.
22	0h RO	**Analog Glitch Filter RX Pad State Select (ANALOGGFRXSEL):** Determine if the internal RX pad state should be subjected to analog glitch filter (implemented within the buffer) or not. This field only make sense when the buffer is configured as an input and is not disabled. 0 = Select non filtered RX pad state 1= Select filtered RX pad state. The mux to select filtered or non filtered RX pad state is implemented within the HIP family. During DFx mode like BSCAN, SCAN, HVM and etc, the AnalogGFRxSel shall be constrained to 0.
21:9	0h RO	**Reserved**
8	0h RO/V	**VCCIO selection (VCCIOSEL):** This bits is used to select VCCIO If the pad supports programmable VCCIO. The definition of high and low are implementation specific. 0: high voltage 1: low voltage

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Reserved**
4:1	0h RO	**Debounce duration (DEBOUNCE):** The debounce duration of value should be not less than 3. In other words, the value should not be any of 0, 1 and 2. The debounce time should be calculated as (2^debounce) * (glitch filter clock period) For example, when RTC clock (32 KHz) is used for glitch filter and debounce duration is set to 4b1011, the debounce time is (2 ^ 11) * (31.25 us) = 64ms
0	0h RO	**Debounce Enable (DEBEN):** This bit enables or disables the debouncer with the pad. 1 = Enable the debouncer of the pad 0 = Disable the debouncer of the pad

33.1.37 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_0) — Offset 70Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 70Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

33.1.38 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_1) — Offset 710h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.39 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_1) — Offset 714h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.40 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_1) — Offset 718h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.41 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_1) — Offset 71Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.42 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_2) — Offset 720h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.43 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_2) — Offset 724h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.44 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_2) — Offset 728h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.45 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_2) — Offset 72Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.46 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_3) — Offset 730h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.47 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_3) — Offset 734h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.48 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_3) — Offset 738h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.49 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_3) — Offset 73Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.50 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_4) — Offset 740h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.51 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_4) — Offset 744h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.52 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_4) — Offset 748h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.53 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_4) — Offset 74Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.54 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_5) — Offset 750h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.55 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_5) — Offset 754h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.56 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_5) — Offset 758h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.57 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_5) — Offset 75Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.58 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_6) — Offset 760h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.59 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_6) — Offset 764h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.60 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_6) — Offset 768h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.61 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_6) — Offset 76Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.62 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_7) — Offset 770h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.63 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_7) — Offset 774h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.64 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_7) — Offset 778h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.65 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_7) — Offset 77Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.66 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_8) — Offset 780h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.67 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_8) — Offset 784h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.68 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_8) — Offset 788h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.69 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_8) — Offset 78Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.70 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_11) — Offset 7B0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.71 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_11) — Offset 7B4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.72 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_11) — Offset 7B8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.73 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_11) — Offset 7BCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.74 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_12) — Offset 7C0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.75 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_12) — Offset 7C4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.76 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_12) — Offset 7C8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.77 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_12) — Offset 7CCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.78 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_13) — Offset 7D0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.79 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_13) — Offset 7D4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.80 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_13) — Offset 7D8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.81 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_13) — Offset 7DCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.82 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_14) — Offset 7E0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.83 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_14) — Offset 7E4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.84 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_14) — Offset 7E8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6E0000h + 7E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:25	0h RO	**SoundWire Slew Control (sndwslewctrl) (SNDWSLEWCTRL):** 00 = Slow Slew Rate 01 = Middle Slew Rate 10 = Fast Slew Rate 11 = Fastest Slew Rate For iCDG buffers, this field is used to control the slew configuration, but extends beyond SoundWire to I2C, SDMMC and other applicable buffers. The setting may vary from one platform to another.
24	0h RO	**Bus Hold Enable (BUSHLDEN):** This feature uses the same build in pull-up/down resistor. In such, BIOS/FW needs to disable all pull-up/down to 'None' before enabling this feature. 1 = enable bus hold 0 = disable bus hold
23	0h RO	**Data Dependent Weak PU Control (DDPUCTRL):** 0 = normal I/O transmission mode. 1 = weak pull up configuration is overridden to disabled, when the raw RX pad state is 0 in output mode. During DFx mode like BSCAN, SCAN, HVM and etc, the DDPUCRTL shall be constrained to 0.
22	0h RO	**Analog Glitch Filter RX Pad State Select (ANALOGGFRXSEL):** Determine if the internal RX pad state should be subjected to analog glitch filter (implemented within the buffer) or not. This field only make sense when the buffer is configured as an input and is not disabled. 0 = Select non filtered RX pad state 1= Select filtered RX pad state. The mux to select filtered or non filtered RX pad state is implemented within the HIP family. During DFx mode like BSCAN, SCAN, HVM and etc, the AnalogGFRxSel shall be constrained to 0.
21:12	0h RO	**Reserved**
11	0h RO/V	**Pin-strap value (PINSTRAPVAL):** This bit reflects the pin-strap value.
10:9	0h RO	**Reserved**
8	0h RO/V	**VCCIO selection (VCCIOSEL):** This bits is used to select VCCIO If the pad supports programmable VCCIO. The definition of high and low are implementation specific. 0: high voltage 1: low voltage

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Reserved**
4:1	0h RO	**Debounce duration (DEBOUNCE):** The debounce duration of value should be not less than 3. In other words, the value should not be any of 0, 1 and 2. The debounce time should be calculated as (2^debounce) * (glitch filter clock period) For example, when RTC clock (32 KHz) is used for glitch filter and debounce duration is set to 4b1011, the debounce time is (2 ^ 11) * (31.25 us) = 64ms
0	0h RO	**Debounce Enable (DEBEN):** This bit enables or disables the debouncer with the pad. 1 = Enable the debouncer of the pad 0 = Disable the debouncer of the pad

33.1.85 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_14) — Offset 7ECh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.86 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_15) — Offset 7F0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.87 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_15) — Offset 7F4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.88 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_15) — Offset 7F8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.89 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_15) — Offset 7FCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.90 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_16) — Offset 800h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.91 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_16) — Offset 804h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.92 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_16) — Offset 808h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.93 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_16) — Offset 80Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.94 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_17) — Offset 810h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.95 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_17) — Offset 814h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.96 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_17) — Offset 818h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.97 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_17) — Offset 81Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.98 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_18) — Offset 820h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.99 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_18) — Offset 824h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.100 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_18) — Offset 828h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_14, offset 7E8h.

33.1.101 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_18) — Offset 82Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.102 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_23) — Offset 870h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.103 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_23) — Offset 874h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.104 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_B_23) — Offset 878h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_14, offset 7E8h.

33.1.105 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_B_23) — Offset 87Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.106 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_0) — Offset 9A0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.107 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_0) — Offset 9A4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.108 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_0) — Offset 9A8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.109 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_0) — Offset 9ACh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.110 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_1) — Offset 9B0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.111 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_1) — Offset 9B4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.112 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_1) — Offset 9B8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.113 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_1) — Offset 9BCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.114 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_2) — Offset 9C0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.115 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_2) — Offset 9C4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.116 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_2) — Offset 9C8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.117 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_2) — Offset 9CCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.118 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_3) — Offset 9D0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.119 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_3) — Offset 9D4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.120 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_3) — Offset 9D8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.121 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_3) — Offset 9DCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.122 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_4) — Offset 9E0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.123 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_4) — Offset 9E4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.124 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_4) — Offset 9E8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.125 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_4) — Offset 9ECh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.126 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_5) — Offset 9F0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.127 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_5) — Offset 9F4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.128 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_5) — Offset 9F8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.129 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_5) — Offset 9FCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.130 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_6) — Offset A00h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.131 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_6) — Offset A04h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.132 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_6) — Offset A08h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.133 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_6) — Offset A0Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.134 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_7) — Offset A10h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.135 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_7) — Offset A14h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.136 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_7) — Offset A18h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.137 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_7) — Offset A1Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.138 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_8) — Offset A20h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.139 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_8) — Offset A24h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.140 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_8) — Offset A28h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.141 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_8) — Offset A2Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.142 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_9) — Offset A30h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.143 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_9) — Offset A34h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.144 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_9) — Offset A38h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.145 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_9) — Offset A3Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.146 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_10) — Offset A40h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.147 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_10) — Offset A44h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.148 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_10) — Offset A48h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.149 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_10) — Offset A4Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.150 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_11) — Offset A50h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.151 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_11) — Offset A54h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.152 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_11) — Offset A58h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.153 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_11) — Offset A5Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.154 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_12) — Offset A60h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.155 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_12) — Offset A64h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.156 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_12) — Offset A68h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.157 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_12) — Offset A6Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.158 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_13) — Offset A70h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.159 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_13) — Offset A74h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.160 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_13) — Offset A78h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.161 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_13) — Offset A7Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.162 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_14) — Offset A80h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.163 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_14) — Offset A84h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.164 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_14) — Offset A88h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.165 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_14) — Offset A8Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.166 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_15) — Offset A90h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.167 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_15) — Offset A94h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.168 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_15) — Offset A98h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.169 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_15) — Offset A9Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.170 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_16) — Offset AA0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.171 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_16) — Offset AA4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.172 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_16) — Offset AA8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.173 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_16) — Offset AACh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.174 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_17) — Offset AB0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.175 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_17) — Offset AB4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.176 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_17) — Offset AB8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.177 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_17) — Offset ABCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.178 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_18) — Offset AC0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.179 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_18) — Offset AC4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.180 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_18) — Offset AC8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.181 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_18) — Offset ACCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.182 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_19) — Offset AD0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.183 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_19) — Offset AD4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.184 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_19) — Offset AD8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.185 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_19) — Offset ADCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.186 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_20) — Offset AE0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.187 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_20) — Offset AE4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.188 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_20) — Offset AE8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.189 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_20) — Offset AECh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.190 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_21) — Offset AF0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.191 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_21) — Offset AF4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.192 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_21) — Offset AF8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.193 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_21) — Offset AFCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.194 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_22) — Offset B00h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.195 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_22) — Offset B04h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.196 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_22) — Offset B08h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.197 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_22) — Offset B0Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.1.198 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_23) — Offset B10h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_B_0, offset 700h.

33.1.199 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_23) — Offset B14h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_B_0, offset 704h.

33.1.200 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_A_23) — Offset B18h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_B_0, offset 708h.

33.1.201 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_A_23) — Offset B1Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_B_0, offset 70Ch.

33.2 GPIO Community 1 Registers

This Section contains the GPIO registers of Community 1- 0x6D section.

Table 33-2. Summary of GPIO Community 1 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8h	4	Family Base Address (FAMBAR)	00000300h
Ch	4	Pad Base Address (PADBAR)	00000700h
10h	4	Miscellaneous Configuration (MISCCFG)	33043200h
20h	4	Pad Ownership (PAD_OWN_GPP_S_0)	00000000h
24h	4	Pad Ownership (PAD_OWN_GPP_I_0)	00000000h
28h	4	Pad Ownership (PAD_OWN_GPP_I_1)	00000000h
2Ch	4	Pad Ownership (PAD_OWN_GPP_I_2)	00000000h
30h	4	Pad Ownership (PAD_OWN_GPP_H_0)	00000000h
34h	4	Pad Ownership (PAD_OWN_GPP_H_1)	00000000h
38h	4	Pad Ownership (PAD_OWN_GPP_H_2)	00000000h
3Ch	4	Pad Ownership (PAD_OWN_GPP_D_0)	00000000h
40h	4	Pad Ownership (PAD_OWN_GPP_D_1)	00000000h
44h	4	Pad Ownership (PAD_OWN_GPP_D_2)	00000000h
80h	4	Pad Configuration Lock (PADCFGLOCK_GPP_S_0)	00000000h
84h	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_S_0)	00000000h
88h	4	Pad Configuration Lock (PADCFGLOCK_GPP_I_0)	00000000h
8Ch	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_I_0)	00000000h
90h	4	Pad Configuration Lock (PADCFGLOCK_GPP_H_0)	00000000h
94h	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_H_0)	00000000h
98h	4	Pad Configuration Lock (PADCFGLOCK_GPP_D_0)	00000000h
9Ch	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_D_0)	00000000h
B0h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_S_0)	00000000h
B4h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_I_0)	00000000h
B8h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_H_0)	00000000h
BCh	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_D_0)	00000000h
100h	4	GPI Interrupt Status (GPI_IS_GPP_S_0)	00000000h
104h	4	GPI Interrupt Status (GPI_IS_GPP_I_0)	00000000h
108h	4	GPI Interrupt Status (GPI_IS_GPP_H_0)	00000000h
10Ch	4	GPI Interrupt Status (GPI_IS_GPP_D_0)	00000000h
120h	4	GPI Interrupt Enable (GPI_IE_GPP_S_0)	00000000h
124h	4	GPI Interrupt Enable (GPI_IE_GPP_I_0)	00000000h
128h	4	GPI Interrupt Enable (GPI_IE_GPP_H_0)	00000000h
12Ch	4	GPI Interrupt Enable (GPI_IE_GPP_D_0)	00000000h
140h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_S_0)	00000000h
144h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_I_0)	00000000h
148h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_H_0)	00000000h
14Ch	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_D_0)	00000000h
160h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_S_0)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
164h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_I_0)	00000000h
168h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_H_0)	00000000h
16Ch	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_D_0)	00000000h
180h	4	SMI Status (GPI_SMI_STS_GPP_S_0)	00000000h
184h	4	SMI Status (GPI_SMI_STS_GPP_I_0)	00000000h
188h	4	SMI Status (GPI_SMI_STS_GPP_H_0)	00000000h
18Ch	4	SMI Status (GPI_SMI_STS_GPP_D_0)	00000000h
1A0h	4	SMI Enable (GPI_SMI_EN_GPP_S_0)	00000000h
1A4h	4	SMI Enable (GPI_SMI_EN_GPP_I_0)	00000000h
1A8h	4	SMI Enable (GPI_SMI_EN_GPP_H_0)	00000000h
1ACh	4	SMI Enable (GPI_SMI_EN_GPP_D_0)	00000000h
1C0h	4	NMI Status (GPI_NMI_STS_GPP_S_0)	00000000h
1C4h	4	NMI Status (GPI_NMI_STS_GPP_I_0)	00000000h
1C8h	4	NMI Status (GPI_NMI_STS_GPP_H_0)	00000000h
1CCh	4	NMI Status (GPI_NMI_STS_GPP_D_0)	00000000h
1E0h	4	NMI Enable (GPI_NMI_EN_GPP_S_0)	00000000h
1E4h	4	NMI Enable (GPI_NMI_EN_GPP_I_0)	00000000h
1E8h	4	NMI Enable (GPI_NMI_EN_GPP_H_0)	00000000h
1ECh	4	NMI Enable (GPI_NMI_EN_GPP_D_0)	00000000h
204h	4	PWM Control (PWMC)	00000000h
20Ch	4	GPIO Serial Blink Enable (GP_SER_BLINK)	00000000h
210h	4	GPIO Serial Blink Command/Status (GP_SER_CMDSTS)	00080000h
214h	4	GPIO Serial Blink Data (GP_SER_DATA)	00000000h
700h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_0)	44000300h
704h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_0)	0080006Ch
708h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_S_0)	00000000h
70Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_S_0)	00000000h
710h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_1)	44000300h
714h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_1)	0080006Dh
718h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_S_1)	00000000h
71Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_S_1)	00000000h
720h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_2)	44000300h
724h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_2)	0080006Eh
728h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_S_2)	00000000h
72Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_S_2)	00000000h
730h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_3)	44000300h
734h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_3)	0080006Fh
738h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_S_3)	00000000h
73Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_S_3)	00000000h
740h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_4)	44000300h
744h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_4)	00800070h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
748h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_S_4)	00000000h
74Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_S_4)	00000000h
750h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_5)	44000300h
754h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_5)	00800071h
758h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_S_5)	00000000h
75Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_S_5)	00000000h
760h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_6)	44000300h
764h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_6)	00800072h
768h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_S_6)	00000000h
76Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_S_6)	00000000h
770h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_7)	44000300h
774h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_7)	00800073h
778h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_S_7)	00000000h
77Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_S_7)	00000000h
7D0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_5)	44000300h
7D4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_5)	00000019h
7D8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_5)	00000000h
7DCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_5)	00000000h
7F0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_7)	44000300h
7F4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_7)	0000001Bh
7F8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_7)	00000000h
7FCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_7)	00000000h
800h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_8)	44000300h
804h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_8)	0000001Ch
808h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_8)	00000000h
80Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_8)	00000000h
810h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_9)	44000300h
814h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_9)	0000001Dh
818h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_9)	00000000h
81Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_9)	00000000h
820h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_10)	44000300h
824h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_10)	0000001Eh
828h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_10)	00000000h
82Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_10)	00000000h
830h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_11)	44000300h
834h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_11)	0000001Fh
838h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_11)	00000000h
83Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_11)	00000000h
840h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_12)	44000300h
844h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_12)	00000020h
848h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_12)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
84Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_12)	00000000h
850h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_13)	44000300h
854h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_13)	00000021h
858h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_13)	00000000h
85Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_13)	00000000h
860h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_14)	44000300h
864h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_14)	00000022h
868h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_14)	00000000h
86Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_14)	00000000h
870h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_15)	44000300h
874h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_15)	00000023h
878h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_15)	00000000h
87Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_15)	00000000h
880h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_16)	44000300h
884h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_16)	00000024h
888h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_16)	00000000h
88Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_16)	00000000h
890h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_17)	44000300h
894h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_17)	00000025h
898h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_17)	00000000h
89Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_17)	00000000h
8A0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_18)	44000300h
8A4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_18)	00000026h
8A8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_18)	00000000h
8ACh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_18)	00000000h
8C0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_0)	44000200h
8C4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_0)	00000028h
8C8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_0)	00000000h
8CCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_0)	00000000h
8D0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_1)	44000200h
8D4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_1)	00000029h
8D8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_1)	00000000h
8DCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_1)	00000000h
8E0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_2)	44000200h
8E4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_2)	0000002Ah
8E8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_2)	00000000h
8ECh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_2)	00000000h
8F0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_3)	44000300h
8F4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_3)	0000002Bh
8F8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_3)	00000000h
8FCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_3)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
900h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_4)	44000300h
904h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_4)	0000002Ch
908h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_4)	00000000h
90Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_4)	00000000h
910h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_5)	44000300h
914h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_5)	0000002Dh
918h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_5)	00000000h
91Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_5)	00000000h
920h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_6)	44000300h
924h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_6)	0000002Eh
928h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_6)	00000000h
92Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_6)	00000000h
930h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_7)	44000300h
934h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_7)	0000002Fh
938h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_7)	00000000h
93Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_7)	00000000h
940h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_8)	44000300h
944h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_8)	00000030h
948h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_8)	00000000h
94Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_8)	00000000h
950h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_9)	44000300h
954h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_9)	00000031h
958h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_9)	00000000h
95Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_9)	00000000h
960h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_10)	44000300h
964h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_10)	00000032h
968h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_10)	00000000h
96Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_10)	00000000h
970h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_11)	44000300h
974h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_11)	00000033h
978h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_11)	00000000h
97Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_11)	00000000h
980h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_12)	44000300h
984h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_12)	00000034h
988h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_12)	00000000h
98Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_12)	00000000h
990h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_13)	44000300h
994h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_13)	00000035h
998h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_13)	00000000h
99Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_13)	00000000h
9B0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_15)	44000300h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
9B4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_15)	00000037h
9B8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_15)	00000000h
9BCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_15)	00000000h
9D0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_17)	44000200h
9D4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_17)	00000039h
9D8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_17)	00000000h
9DCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_17)	00000000h
9E0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_18)	44000700h
9E4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_18)	0000003Ah
9E8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_18)	00000000h
9ECh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_18)	00000000h
9F0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_19)	44000300h
9F4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_19)	0000003Bh
9F8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_19)	00000000h
9FCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_19)	00000000h
A00h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_20)	44000300h
A04h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_20)	0000003Ch
A08h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_20)	00000000h
A0Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_20)	00000000h
A10h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_21)	44000300h
A14h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_21)	0000003Dh
A18h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_21)	00000000h
A1Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_21)	00000000h
A20h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_22)	44000300h
A24h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_22)	0000003Eh
A28h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_22)	00000000h
A2Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_22)	00000000h
A30h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_23)	44000300h
A34h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_23)	0000003Fh
A38h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_23)	00000000h
A3Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_23)	00000000h
A40h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_0)	44000300h
A44h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_0)	00000040h
A48h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_0)	00000000h
A4Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_0)	00000000h
A50h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_1)	44000300h
A54h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_1)	00000041h
A58h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_1)	00000000h
A5Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_1)	00000000h
A60h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_2)	44000300h
A64h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_2)	00000042h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
A68h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_2)	00000000h
A6Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_2)	00000000h
A70h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_3)	44000300h
A74h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_3)	00000043h
A78h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_3)	00000000h
A7Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_3)	00000000h
A80h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_4)	44000300h
A84h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_4)	00000044h
A88h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_4)	00000000h
A8Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_4)	00000000h
A90h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_5)	44000300h
A94h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_5)	00000045h
A98h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_5)	00000000h
A9Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_5)	00000000h
AA0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_6)	44000300h
AA4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_6)	00000046h
AA8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_6)	00000000h
AACh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_6)	00000000h
AB0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_7)	44000300h
AB4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_7)	00000047h
AB8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_7)	00000000h
ABCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_7)	00000000h
AC0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_8)	44000300h
AC4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_8)	00000048h
AC8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_8)	00000000h
ACCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_8)	00000000h
AD0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_9)	44001700h
AD4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_9)	00003C49h
AD8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_9)	00000100h
ADCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_9)	00000000h
AE0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_10)	44001600h
AE4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_10)	00003C4Ah
AE8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_10)	00000100h
AECh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_10)	00000000h
AF0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_11)	44001700h
AF4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_11)	00003C4Bh
AF8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_11)	00000100h
AFCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_11)	00000000h
B00h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_12)	44001600h
B04h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_12)	00003C4Ch
B08h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_12)	00000100h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
B0Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_12)	00000000h
B10h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_13)	44000300h
B14h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_13)	0000004Dh
B18h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_13)	00000000h
B1Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_13)	00000000h
B20h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_14)	44000300h
B24h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_14)	0000004Eh
B28h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_14)	00000000h
B2Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_14)	00000000h
B30h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_15)	44000300h
B34h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_15)	0000004Fh
B38h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_15)	00000000h
B3Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_15)	00000000h
B40h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_16)	44000300h
B44h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_16)	00000050h
B48h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_16)	00000000h
B4Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_16)	00000000h
B50h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_17)	44000300h
B54h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_17)	00000051h
B58h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_17)	00000000h
B5Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_17)	00000000h
B60h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_18)	44000300h
B64h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_18)	00000052h
B68h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_18)	00000000h
B6Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_18)	00000000h
B70h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_19)	44000300h
B74h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_19)	00000053h
B78h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_19)	00000000h
B7Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_19)	00000000h

33.2.1 Family Base Address (FAMBAR) — Offset 8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 8h	00000300h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0300h RO	**Family Base Address (FAMBAR):** This field provides the starting byte-align address of Family0 register sets within a Community. It is meant for software to discover from where the very first Family register (i.e. Family0 register) starts to compute the next Families address offsets.

33.2.2 Pad Base Address (PADBAR) — Offset Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + Ch	00000700h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0700h RO	**Pad Base Address (PADBAR):** This field provides the starting byte-align address of Pad0 register sets within a Community. It is meant for software to discover from where the very first Pad register (i.e. Pad0 register) starts to compute the next Pad address offsets.

33.2.3 Miscellaneous Configuration (MISCCFG) — Offset 10h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 10h	33043200h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	33h RW	**GPIO Driver Mode Interrupt Select (GPDMINTSEL):** IRQ globally for all pads (GPI_IS with corresponding GPI_IE enable). 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255
23:20	0h RO	**Reserved**
19:16	4h RW	**GPIO Group to GPE_DW2 assignment encoding (GPE0_DW2):** This register assigns a specific GPIO Group to the ACPI GPE0[95:64]. The setting is SoC specific.
15:12	3h RW	**GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1):** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The setting is SoC specific.
11:8	2h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0):** This register assigns a specific GPIO Group to the ACPI GPE0[31:0]. The setting is SoC specific.
7	0h RW	**GPIO IOSF Sideband VNNREQ Enable (GPVNNREQEN):** Specify whether the GPIO Community should take part in IOSFSB VNNREQ/ACK handshake 0 = Disable participation in IOSF SB VNNREQ and VNNACK handshake 1 = Enable participation in IOSF SB VNNREQ and VNNACK handshake When this bit set to 1, GPIO controller will de-assert the VNNREQ when there is no outstanding IOSF SB upstream cycle from GPIO controller. When this bit set to 1 and MISCSECCFG.SBTRIGDIS is 0, GPIO controller will assert the VNNREQ to request for the following list of IOSF-SB Message initiation. Event list: IRQ NMI SMI SSMI VNNREQ shall de-assert when MISCSECCFG.SBTRIGDIS is set to 1. As VNNAON IP, GPIO controller will assert the VNNREQ when in reset. The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pwrgate_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this power gating, this register always default to 1.
6	0h RW	**GPIO PGCB Clock Dynamic Partition Clock Gating Enable (GPPGCBDPCGEN):** Specify whether the GPIO Community PGCB clock should take part in partition clock gating 0 = Disable participation in PGCB clock dynamic partition clock gating 1 = Enable participation in PGCB clock dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**GPIO IOSF Sideband Dynamic Partition Clock Gating Enable (GPSIDEDPCGEN):** Specify whether the GPIO Community IOSF sideband clock should take part in partition clock gating 0 = Disable participation in IOSF sideband clock dynamic partition clock gating 1 = Enable participation in IOSF sideband clock dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
4	0h RW	**GPIO RCOMP clock Dynamic Local Clock Gating (GPRCOMPCDLCGEN):** Specify whether the GPIO Community should perform local clock gating on RCOMP clock 0 = Disable dynamic RCOMP clock local clock gating 1 = Enable dynamic RCOMP clock local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
3	0h RW	**GPIO RTC clock Dynamic Local Clock Gating (GPRTCDLCGEN):** Specify whether the GPIO Community should perform local clock gating on RTC clock 0 = Disable dynamic RTC clock local clock gating 1 = Enable dynamic RTC clock local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
2	0h RW	**GSX Static Local Clock Gating (GSXSLCGEN):** Specify whether the GSX controller should be statically clock gated for power saving if it is not enabled (even though the capability is available). 0 = Disable static local clock gating 1 = Enable static local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
1	0h RW	**GPIO Dynamic Partition Clock Gating Enable (GPDPCGEN):** Specify whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
0	0h RW	**GPIO Dynamic Local Clock Gating Enable (GPDLCGEN):** Specify whether the GPIO Community should perform local clock gating 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0

33.2.4 Pad Ownership (PAD_OWN_GPP_S_0) — Offset 20h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 20h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPP_S_7):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPP_S_6):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPP_S_5):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPP_S_4):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPP_S_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPP_S_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPP_S_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPP_S_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.2.5 Pad Ownership (PAD_OWN_GPP_I_0) — Offset 24h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 24h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPP_I_7):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

Bit Range	Default & Access	Field Name (ID): Description
27:22	0h RO	**Reserved**
21:20	0h RW	**Pad Ownership (PAD_OWN_GPP_I_5):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:0	0h RO	**Reserved**

33.2.6 Pad Ownership (PAD_OWN_GPP_I_1) — Offset 28h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 28h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPP_I_15):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPP_I_14):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPP_I_13):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPP_I_12):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPP_I_11):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPP_I_10):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPP_I_9):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPP_I_8):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.2.7 Pad Ownership (PAD_OWN_GPP_I_2) — Offset 2Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 2Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:12	0h RW	**Reserved**
11:10	0h RO	**Reserved**
9:8	0h RW	**Pad Ownership (PAD_OWN_GPP_I_18):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPP_I_17):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPP_I_16):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.2.8 Pad Ownership (PAD_OWN_GPP_H_0) — Offset 30h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 30h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_7):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_6):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_5):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_4):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.2.9 Pad Ownership (PAD_OWN_GPP_H_1) — Offset 34h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 34h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_15):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_13):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_12):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_11):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_10):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_9):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_8):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.2.10 Pad Ownership (PAD_OWN_GPP_H_2) — Offset 38h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 38h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_23):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_22):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_21):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_20):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_19):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_18):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_17):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:0	0h RO	**Reserved**

33.2.11 Pad Ownership (PAD_OWN_GPP_D_0) — Offset 3Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 3Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_7):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_6):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_5):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_4):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.2.12 Pad Ownership (PAD_OWN_GPP_D_1) — Offset 40h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 40h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_15):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_14):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_13):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_12):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_11):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_10):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_9):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_8):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.2.13 Pad Ownership (PAD_OWN_GPP_D_2) — Offset 44h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 44h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RO	**Reserved**
15:14	0h RO	**Reserved**
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_19):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_18):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_17):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_D_16):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.2.14 Pad Configuration Lock (PADCFGLOCK_GPP_S_0) — Offset 80h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 80h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_S_7):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_S_6):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_S_5):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_S_4):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_S_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_S_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_S_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_S_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

33.2.15 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_S_0) — Offset 84h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 84h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_S_7):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_S_6):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_S_5):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_S_4):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_S_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_S_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_S_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_S_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

33.2.16 Pad Configuration Lock (PADCFGLOCK_GPP_I_0) — Offset 88h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 88h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RW	**Reserved**
18	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_I_18):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_I_17):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
16	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_I_16):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_I_15):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
14	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_I_14):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_I_13):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
12	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_I_12):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_I_11):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_I_10):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_I_9):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_I_8):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_I_7):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Reserved**
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_I_5):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
4:0	0h RW	**Reserved**

33.2.17 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_I_0) — Offset 8Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 8Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RW	**Reserved**
18	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_I_18):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_I_17):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
16	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_I_16):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_I_15):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
14	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_I_14):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_I_13):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
12	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_I_12):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_I_11):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_I_10):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_I_9):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_I_8):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_I_7):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
6	0h RW	**Reserved**
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_I_5):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
4:0	0h RW	**Reserved**

33.2.18 Pad Configuration Lock (PADCFGLOCK_GPP_H_0) — Offset 90h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 90h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_23):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
22	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_22):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_21):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
20	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_20):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_19):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
18	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_18):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_17):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
16	0h RW	**Reserved**
15	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_15):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Reserved**
13	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_13):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
12	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_12):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_11):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_10):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_9):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_8):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_7):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_6):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_5):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_4):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

33.2.19 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_H_0) — Offset 94h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 94h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_23):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
22	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_22):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_21):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
20	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_20):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_19):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
18	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_18):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_17):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
16	0h RW	**Reserved**
15	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_15):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
14	0h RW	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_13):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
12	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_12):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_11):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_10):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_9):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_8):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_7):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_6):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_5):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_4):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

33.2.20 Pad Configuration Lock (PADCFGLOCK_GPP_D_0) — Offset 98h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 98h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_19):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_18):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
17	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_17):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_16):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
15	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_15):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_14):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
13	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_13):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_12):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_11):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_10):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_9):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_8):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_7):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_6):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_5):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_4):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

33.2.21 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_D_0) — Offset 9Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 9Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_19):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_18):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
17	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_17):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_16):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
15	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_15):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_14):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
13	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_13):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_12):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_11):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_10):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_9):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_8):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_7):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_6):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_5):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_4):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

33.2.22 Host Software Pad Ownership (HOSTSW_OWN_GPP_S_0) — Offset B0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**HOSTSW_OWN_GPP_S_7:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
6	0h RW	**HOSTSW_OWN_GPP_S_6:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**HOSTSW_OWN_GPP_S_5:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
4	0h RW	**HOSTSW_OWN_GPP_S_4:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
3	0h RW	**HOSTSW_OWN_GPP_S_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HOSTSW_OWN_GPP_S_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RW	**HOSTSW_OWN_GPP_S_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RW	**HOSTSW_OWN_GPP_S_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

33.2.23 Host Software Pad Ownership (HOSTSW_OWN_GPP_I_0) — Offset B4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RW	**Reserved**
18	0h RW	**HOSTSW_OWN_GPP_I_18:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
17	0h RW	**HOSTSW_OWN_GPP_I_17:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**HOSTSW_OWN_GPP_I_16:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
15	0h RW	**HOSTSW_OWN_GPP_I_15:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
14	0h RW	**HOSTSW_OWN_GPP_I_14:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**HOSTSW_OWN_GPP_I_13:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
12	0h RW	**HOSTSW_OWN_GPP_I_12:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
11	0h RW	**HOSTSW_OWN_GPP_I_11:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**HOSTSW_OWN_GPP_I_10:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
9	0h RW	**HOSTSW_OWN_GPP_I_9:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
8	0h RW	**HOSTSW_OWN_GPP_I_8:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**HOSTSW_OWN_GPP_I_7:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
6	0h RW	**Reserved**
5	0h RW	**HOSTSW_OWN_GPP_I_5:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
4:0	0h RW	**Reserved**

33.2.24 Host Software Pad Ownership (HOSTSW_OWN_GPP_H_0) — Offset B8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW	**HOSTSW_OWN_GPPC_H_23:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
22	0h RW	**HOSTSW_OWN_GPPC_H_22:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**HOSTSW_OWN_GPPC_H_21:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
20	0h RW	**HOSTSW_OWN_GPPC_H_20:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
19	0h RW	**HOSTSW_OWN_GPPC_H_19:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**HOSTSW_OWN_GPPC_H_18:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
17	0h RW	**HOSTSW_OWN_GPPC_H_17:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
16	0h RW	**Reserved**
15	0h RW	**HOSTSW_OWN_GPPC_H_15:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
14	0h RW	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**HOSTSW_OWN_GPPC_H_13:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
12	0h RW	**HOSTSW_OWN_GPPC_H_12:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
11	0h RW	**HOSTSW_OWN_GPPC_H_11:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**HOSTSW_OWN_GPPC_H_10:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
9	0h RW	**HOSTSW_OWN_GPPC_H_9:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
8	0h RW	**HOSTSW_OWN_GPPC_H_8:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**HOSTSW_OWN_GPPC_H_7:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
6	0h RW	**HOSTSW_OWN_GPPC_H_6:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
5	0h RW	**HOSTSW_OWN_GPPC_H_5:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**HOSTSW_OWN_GPPC_H_4:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
3	0h RW	**HOSTSW_OWN_GPPC_H_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HOSTSW_OWN_GPPC_H_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RW	**HOSTSW_OWN_GPPC_H_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RW	**HOSTSW_OWN_GPPC_H_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

33.2.25 Host Software Pad Ownership (HOSTSW_OWN_GPP_D_0) — Offset BCh

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + BCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RW	**HOSTSW_OWN_GPPC_D_19:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
18	0h RW	**HOSTSW_OWN_GPPC_D_18:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**HOSTSW_OWN_GPPC_D_17:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
16	0h RW	**HOSTSW_OWN_GPPC_D_16:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
15	0h RW	**HOSTSW_OWN_GPPC_D_15:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**HOSTSW_OWN_GPPC_D_14:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
13	0h RW	**HOSTSW_OWN_GPPC_D_13:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
12	0h RW	**HOSTSW_OWN_GPPC_D_12:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**HOSTSW_OWN_GPPC_D_11:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
10	0h RW	**HOSTSW_OWN_GPPC_D_10:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
9	0h RW	**HOSTSW_OWN_GPPC_D_9:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**HOSTSW_OWN_GPPC_D_8:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
7	0h RW	**HOSTSW_OWN_GPPC_D_7:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
6	0h RW	**HOSTSW_OWN_GPPC_D_6:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**HOSTSW_OWN_GPPC_D_5:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
4	0h RW	**HOSTSW_OWN_GPPC_D_4:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
3	0h RW	**HOSTSW_OWN_GPPC_D_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HOSTSW_OWN_GPPC_D_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RW	**HOSTSW_OWN_GPPC_D_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RW	**HOSTSW_OWN_GPPC_D_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

33.2.26 GPI Interrupt Status (GPI_IS_GPP_S_0) — Offset 100h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 100h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_S_7):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_S_6):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_S_5):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_S_4):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_S_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_S_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_S_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_S_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.2.27 GPI Interrupt Status (GPI_IS_GPP_I_0) — Offset 104h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 104h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RW/1C	**Reserved**
18	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_I_18):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
17	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_I_17):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_I_16):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
15	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_I_15):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_I_14):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_I_13):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_I_12):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
11	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_I_11):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_I_10):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_I_9):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
8	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_I_8):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_I_7):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW/1C	**Reserved**
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_I_5):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4:0	0h RW/1C	**Reserved**

33.2.28 GPI Interrupt Status (GPI_IS_GPP_H_0) — Offset 108h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 108h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_23):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
22	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_22):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_21):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
20	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_20):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
19	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_19):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_18):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
17	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_17):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
16	0h RW/1C	**Reserved**
15	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_15):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW/1C	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_13):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_12):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
11	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_11):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_10):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_9):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
8	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_8):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_7):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_6):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_5):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_4):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.2.29 GPI Interrupt Status (GPI_IS_GPP_D_0) — Offset 10Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 10Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_19):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
18	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_18):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_17):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
16	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_16):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
15	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_15):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_14):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_13):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_12):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_11):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_10):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_9):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_8):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_7):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_6):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_5):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_4):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.2.30 GPI Interrupt Enable (GPI_IE_GPP_S_0) — Offset 120h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 120h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_S_7):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_S_6):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_S_5):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_S_4):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_S_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_S_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_S_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_S_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.2.31 GPI Interrupt Enable (GPI_IE_GPP_I_0) — Offset 124h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 124h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RW	**Reserved**
18	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_I_18):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
17	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_I_17):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
16	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_I_16):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_I_15):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_I_14):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_I_13):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_I_12):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_I_11):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_I_10):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_I_9):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_I_8):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_I_7):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW	**Reserved**
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_I_5):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4:0	0h RW	**Reserved**

33.2.32 GPI Interrupt Enable (GPI_IE_GPP_H_0) — Offset 128h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 128h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_23):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
22	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_22):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
21	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_21):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_20):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
19	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_19):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
18	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_18):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
17	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_17):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
16	0h RW	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_15):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW	**Reserved**
13	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_13):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_12):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_11):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_10):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_9):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_8):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_7):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_6):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_5):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_4):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.2.33 GPI Interrupt Enable (GPI_IE_GPP_D_0) — Offset 12Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 12Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_19):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
18	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_18):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
17	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_17):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_16):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
15	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_15):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_14):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_13):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_12):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_11):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_10):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_9):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_8):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_7):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_6):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_5):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_4):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.2.34 GPI General Purpose Events Status (GPI_GPE_STS_GPP_S_0) — Offset 140h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 140h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_S_7):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_S_6):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_S_5):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_S_4):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_S_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_S_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_S_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_S_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.2.35 GPI General Purpose Events Status (GPI_GPE_STS_GPP_I_0) — Offset 144h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 144h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RW/1C	**Reserved**
18	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_I_18):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
17	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_I_17):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_I_16):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
15	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_I_15):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_I_14):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_I_13):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
12	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_I_12):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_I_11):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_I_10):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
9	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_I_9):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_I_8):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_I_7):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW/1C	**Reserved**
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_I_5):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4:0	0h RW/1C	**Reserved**

33.2.36 GPI General Purpose Events Status (GPI_GPE_STS_GPP_H_0) — Offset 148h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 148h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_23):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
22	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_22):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_21):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
20	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_20):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
19	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_19):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_18):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
17	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_17):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
16	0h RW/1C	**Reserved**
15	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_15):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW/1C	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_13):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
12	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_12):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_11):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_10):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
9	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_9):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_8):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_7):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_6):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_5):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_4):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.2.37 GPI General Purpose Events Status (GPI_GPE_STS_GPP_D_0) — Offset 14Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 14Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_19):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
18	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_18):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_17):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
16	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_16):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
15	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_15):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_14):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
13	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_13):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
12	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_12):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_11):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_10):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
9	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_9):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_8):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_7):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_6):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_5):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_4):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.2.38 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_S_0) — Offset 160h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 160h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_S_7):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_S_6):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_S_5):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_S_4):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_S_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_S_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_S_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_S_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.2.39 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_I_0) — Offset 164h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 164h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RW	**Reserved**
18	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_I_18):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
17	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_I_17):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
16	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_I_16):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_I_15):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_I_14):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
13	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_I_13):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
12	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_I_12):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_I_11):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_I_10):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_I_9):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_I_8):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_I_7):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW	**Reserved**
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_I_5):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4:0	0h RW	**Reserved**

33.2.40 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_H_0) — Offset 168h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 168h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_23):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
22	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_22):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
21	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_21):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_20):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
19	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_19):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
18	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_18):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
17	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_17):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Reserved**
15	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_15):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW	**Reserved**
13	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_13):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
12	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_12):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_11):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_10):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_9):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_8):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_7):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_6):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_5):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_4):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.2.41 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_D_0) — Offset 16Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 16Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_19):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
18	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_18):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_17):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
16	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_16):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
15	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_15):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_14):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_13):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
12	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_12):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_11):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_10):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_9):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_8):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_7):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_6):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_5):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_4):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.2.42 SMI Status (GPI_SMI_STS_GPP_S_0) — Offset 180h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 180h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_S_7):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
6	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_S_6):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_S_5):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
4	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_S_4):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_S_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_S_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_S_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_S_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

33.2.43 SMI Status (GPI_SMI_STS_GPP_I_0) — Offset 184h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 184h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RSV	**Reserved**
18	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_I_18):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
17	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_I_17):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_I_16):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
15	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_I_15):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_I_14):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
13	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_I_13):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_I_12):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
11	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_I_11):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_I_10):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
9	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_I_9):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_I_8):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
7	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_I_7):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RSV	**Reserved**
5	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_I_5):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
4:0	0h RSV	**Reserved**

33.2.44 SMI Status (GPI_SMI_STS_GPP_H_0) — Offset 188h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 188h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_23):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
22	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_22):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_21):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
20	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_20):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_19):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
18	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_18):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_17):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
16	0h RSV	**Reserved**
15	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_15):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
14	0h RSV	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_13):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
12	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_12):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_11):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
10	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_10):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_9):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
8	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_8):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_7):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
6	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_6):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_5):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
4	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_4):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPPC_H_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

33.2.45 SMI Status (GPI_SMI_STS_GPP_D_0) — Offset 18Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 18Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_19):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
18	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_18):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_17):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
16	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_16):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_15):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
14	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_14):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_13):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
12	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_12):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_11):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
10	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_10):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_9):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
8	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_8):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_7):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
6	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_6):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_D_5):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
4	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_D_4):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_D_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_D_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_D_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_D_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

33.2.46 SMI Enable (GPI_SMI_EN_GPP_S_0) — Offset 1A0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 1A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_S_7):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
6	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_S_6):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_S_5):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
4	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_S_4):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
3	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_S_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_S_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_S_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_S_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

33.2.47 SMI Enable (GPI_SMI_EN_GPP_I_0) — Offset 1A4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 1A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RSV	**Reserved**
18	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_I_18):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
17	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_I_17):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
16	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_I_16):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
15	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_I_15):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
14	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_I_14):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
13	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_I_13):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
12	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_I_12):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
11	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_I_11):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
10	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_I_10):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
9	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_I_9):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
8	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_I_8):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
7	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_I_7):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
6	0h RSV	**Reserved**
5	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_I_5):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
4:0	0h RSV	**Reserved**

33.2.48 SMI Enable (GPI_SMI_EN_GPP_H_0) — Offset 1A8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 1A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_23):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
22	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_22):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
21	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_21):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
20	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_20):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
19	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_19):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
18	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_18):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
17	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_17):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
16	0h RSV	**Reserved**
15	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_15):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
14	0h RSV	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_13):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
12	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_12):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
11	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_11):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
10	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_10):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
9	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_9):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
8	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_8):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
7	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_7):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
6	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_6):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
5	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_5):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_4):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
3	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPPC_H_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

33.2.49 SMI Enable (GPI_SMI_EN_GPP_D_0) — Offset 1ACh

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 1ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_19):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
18	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_18):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_17):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
16	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_16):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
15	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_15):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_14):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
13	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_13):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
12	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_12):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_11):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
10	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_10):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
9	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_9):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_8):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
7	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_7):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
6	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_6):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_5):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
4	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_4):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
3	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

33.2.50 NMI Status (GPI_NMI_STS_GPP_S_0) — Offset 1C0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 1C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_S_7):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_S_6):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_S_5):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_S_4):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_S_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_S_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_S_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_S_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.2.51 NMI Status (GPI_NMI_STS_GPP_I_0) — Offset 1C4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 1C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RSV	**Reserved**
18	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_I_18):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
17	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_I_17):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_I_16):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
15	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_I_15):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_I_14):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_I_13):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
12	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_I_12):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_I_11):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_I_10):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
9	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_I_9):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
8	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_I_8):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_I_7):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RSV	**Reserved**
5	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_I_5):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4:0	0h RSV	**Reserved**

33.2.52 NMI Status (GPI_NMI_STS_GPP_H_0) — Offset 1C8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 1C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_23):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
22	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_22):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_21):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
20	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_20):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
19	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_19):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_18):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
17	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_17):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RSV	**Reserved**
15	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_15):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RSV	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_13):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
12	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_12):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_11):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_10):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
9	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_9):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
8	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_8):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_7):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_6):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_5):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_4):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPPC_H_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.2.53 NMI Status (GPI_NMI_STS_GPP_D_0) — Offset 1CCh

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 1CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_19):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
18	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_18):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_17):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_16):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
15	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_15):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_14):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_13):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
12	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_12):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_11):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_10):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
9	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_9):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_8):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_7):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_6):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_D_5):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_D_4):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_D_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_D_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_D_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_D_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.2.54 NMI Enable (GPI_NMI_EN_GPP_S_0) — Offset 1E0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 1E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_S_7):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_S_6):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_S_5):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_S_4):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_S_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_S_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_S_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_S_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.2.55 NMI Enable (GPI_NMI_EN_GPP_I_0) — Offset 1E4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 1E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RSV	**Reserved**
18	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_I_18):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
17	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_I_17):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_I_16):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
15	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_I_15):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_I_14):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_I_13):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
12	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_I_12):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_I_11):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_I_10):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
9	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_I_9):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
8	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_I_8):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_I_7):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RSV	**Reserved**
5	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_I_5):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4:0	0h RSV	**Reserved**

33.2.56 NMI Enable (GPI_NMI_EN_GPP_H_0) — Offset 1E8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 1E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_23):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
22	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_22):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
21	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_21):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_20):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
19	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_19):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
18	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_18):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_17):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RSV	**Reserved**
15	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_15):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RSV	**Reserved**
13	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_13):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_12):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_11):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_10):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_9):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
8	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_8):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_7):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_6):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_5):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_4):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPPC_H_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.2.57 NMI Enable (GPI_NMI_EN_GPP_D_0) — Offset 1ECh

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 1ECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO	**Reserved**
19	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_19):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
18	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_18):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_17):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_16):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
15	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_15):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_14):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_13):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
12	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_12):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_11):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_10):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
9	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_9):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_8):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_7):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_6):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_5):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_4):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.2.58 PWM Control (PWMC) — Offset 204h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 204h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**EN:** 0 = Disable PWM Output 1 = Enable PWM Output
30	0h RW/1S/V	**Software Update (SWUP):** Indication that there is an update to PWM settings pending. SW sets this bit to 1 when updating the PWM_base_unit or PWM_on_time_divisor fields. The PWM module will apply the new settings at the end of the current cycle and reset this bit. 0 = No updates pending 1 = Update pending
29:8	000000h RW	**Base Unit (BASEUNIT):** Base unit register. Unsigned 8 integer bits, 14 fraction bits. Used to determine PWM output frequency. The PWM base frequency for SPT is 32.768 KHz. Refer to PWM section for programming details.
7:0	00h RW	**On Time Divisor (ONTIMEDIV):** PWM duty cycle = PWM_on-time_divisor/256.

33.2.59 GPIO Serial Blink Enable (GP_SER_BLINK) — Offset 20Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 20Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	00h RW	**GP SER BLINK (GP_SER_BLINK):** The setting of this bit has no effect if the corresponding GPIO is programmed as an input, if the corresponding GPIO has the PWM enabled, or if Serial Blink capability does not exist . This bit should be set to a 1 before output buffer is enabled. When set to a '0', the corresponding GPIO will function normally. This bit should be set to a 1 while the corresponding PMode bit is set to 0h (GPIO Mode). Setting the PMode bit to other value (non-GPIO Mode) after the GP_SER_BLINK bit ensures PCH will not drive a 1 on the pin as an output. When this corresponding bit is set to a 1 and the pin is configured to output mode, the serial blink capability is enabled and the programmed message is serialized out through an open-drain buffer configuration. The value of the corresponding GPIOTxState bit remains unchanged and does not impact the serial blink capability in any way. Writes to this register have no effect when the corresponding pin is configured in native mode and the read value returned is undefined. Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= Pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

33.2.60 GPIO Serial Blink Command/Status (GP_SER_CMDSTS) — Offset 210h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 210h	00080000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:22	0h RW	**Data Length Select (DLS):** This read/write field determines the number of bytes to serialize on GPIO 00: Serialize bits 7:0 of GP_GB_DATA (1 byte) 01: Serialize bits 15:0 of GP_GB_DATA (2 bytes) 10: Undefined - Software must not write this value 11: Serialize bits 31:0 of GP_GB_DATA (4 bytes) Software should not modify the value in this register unless the Busy bit is clear
21:16	08h RW	**Data Rate Select (DRS):** This read/write field selects the number of 166.64ns (4 clock periods GPIO clock - if GPIO clock is 24MHz) time intervals to count between Manchester data transitions. The default of 8h results in a 1333.33 ns minimum time between transitions. A value of 0h in this register produces undefined behavior. Software should not modify the value in this register unless the Busy bit is clear.
15:9	0h RO	**Reserved**
8	0h RO/V	**BUSY:** This read-only status bit is the hardware indication that a serialization is in progress. Hardware sets this bit to 1 based on the Go bit being set. Hardware clears this bit when the Go bit is cleared by the hardware.
7:1	0h RO	**Reserved**
0	0h RW	**GO:** This bit is set to 1 by software to start the serialization process. Hardware clears the bit after the serialized data is sent. Writes of 0 to this register have no effect. Software should not write this bit to 1 unless the Busy status bit is cleared.

33.2.61 GPIO Serial Blink Data (GP_SER_DATA) — Offset 214h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 214h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GP Serial Blink Data (GP_GB_DATA):** This read-write register contains the data serialized out. The number of bits shifted out is selected through the DLS field in the GP_GB_CMDSTS register. This register should not be modified by software when the Busy bit is set.

33.2.62 Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_0) — Offset 700h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 700h	44000300h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the SoC responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)

Bit Range	Default & Access	Field Name (ID): Description
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	0h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

33.2.63 Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_0) — Offset 704h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 704h	0080006Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	2h RW	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0100: 5k PD 1100: 5k PU 1111: Native controller selected by Pad Mode controls the Termination. This field should be set to 1111b for the selected native function that supports dynamic termination override. Refer to Vol1, GPIO chapter, for more info. Others: Reserved. NOTES: 1. The 5K pull-up/pull-down can only be enabled as long as the toggle rate on the signal is no more than 300KHz. 2. If a reserved value is programmed, pad may malfunction. 3. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, PU/PD settings should be programmed first to ensure the input does not float momentarily
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	6Ch RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

33.2.64 Pad Configuration DW2 (PAD_CFG_DW2_GPP_S_0) — Offset 708h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 708h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:25	0h RW	**SoundWire Slew Control (sndwslewctrl) (SNDWSLEWCTRL):** 00 = Slow Slew Rate 01 = Middle Slew Rate 10 = Fast Slew Rate 11 = Fastest Slew Rate For iCDG buffers, this field is used to control the slew configuration, but extends beyond SoundWire to I2C, SDMMC and other applicable buffers. The setting may vary from one platform to another.
24	0h RW	**Bus Hold Enable (BUSHLDEN):** This feature uses the same build in pull-up/down resistor. In such, BIOS/FW needs to disable all pull-up/down to 'None' before enabling this feature. 1 = enable bus hold 0 = disable bus hold
23	0h RO	**Data Dependent Weak PU Control (DDPUCTRL):** 0 = normal I/O transmission mode. 1 = weak pull up configuration is overridden to disabled, when the raw RX pad state is 0 in output mode. During DFx mode like BSCAN, SCAN, HVM and etc, the DDPUCRTL shall be constrained to 0.
22	0h RO	**Analog Glitch Filter RX Pad State Select (ANALOGGFRXSEL):** Determine if the internal RX pad state should be subjected to analog glitch filter (implemented within the buffer) or not. This field only make sense when the buffer is configured as an input and is not disabled. 0 = Select non filtered RX pad state 1= Select filtered RX pad state. The mux to select filtered or non filtered RX pad state is implemented within the HIP family. During DFx mode like BSCAN, SCAN, HVM and etc, the AnalogGFRxSel shall be constrained to 0.
21:9	0h RO	**Reserved**
8	0h RO	**VCCIO selection (VCCIOSEL):** This bits is used to select VCCIO If the pad supports programmable VCCIO. The definition of high and low are implementation specific. 0: high voltage 1: low voltage

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Reserved**
4:1	0h RO	**Debounce duration (DEBOUNCE):** The debounce duration of value should be not less than 3. In other words, the value should not be any of 0, 1 and 2. The debounce time should be calculated as (2^debounce) * (glitch filter clock period) For example, when RTC clock (32 KHz) is used for glitch filter and debounce duration is set to 4b1011, the debounce time is (2 ^ 11) * (31.25 us) = 64ms
0	0h RO	**Debounce Enable (DEBEN):** This bit enables or disables the debouncer with the pad. 1 = Enable the debouncer of the pad 0 = Disable the debouncer of the pad

33.2.65 Pad Configuration DW3 (PAD_CFG_DW3_GPP_S_0) — Offset 70Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 70Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

33.2.66 Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_1) — Offset 710h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.67 Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_1) — Offset 714h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_S_0, offset 704h.

33.2.68 Pad Configuration DW2 (PAD_CFG_DW2_GPP_S_1) — Offset 718h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.69 Pad Configuration DW3 (PAD_CFG_DW3_GPP_S_1) — Offset 71Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.70 Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_2) — Offset 720h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.71 Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_2) — Offset 724h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_S_0, offset 704h.

33.2.72 Pad Configuration DW2 (PAD_CFG_DW2_GPP_S_2) — Offset 728h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.73 Pad Configuration DW3 (PAD_CFG_DW3_GPP_S_2) — Offset 72Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.74 Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_3) — Offset 730h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.75 Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_3) — Offset 734h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_S_0, offset 704h.

33.2.76 Pad Configuration DW2 (PAD_CFG_DW2_GPP_S_3) — Offset 738h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.77 Pad Configuration DW3 (PAD_CFG_DW3_GPP_S_3) — Offset 73Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.78 Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_4) — Offset 740h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.79 Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_4) — Offset 744h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_S_0, offset 704h.

33.2.80 Pad Configuration DW2 (PAD_CFG_DW2_GPP_S_4) — Offset 748h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.81 Pad Configuration DW3 (PAD_CFG_DW3_GPP_S_4) — Offset 74Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.82 Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_5) — Offset 750h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.83 Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_5) — Offset 754h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_S_0, offset 704h.

33.2.84 Pad Configuration DW2 (PAD_CFG_DW2_GPP_S_5) — Offset 758h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.85 Pad Configuration DW3 (PAD_CFG_DW3_GPP_S_5) — Offset 75Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.86 Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_6) — Offset 760h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.87 Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_6) — Offset 764h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_S_0, offset 704h.

33.2.88 Pad Configuration DW2 (PAD_CFG_DW2_GPP_S_6) — Offset 768h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.89 Pad Configuration DW3 (PAD_CFG_DW3_GPP_S_6) — Offset 76Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.90 Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_7) — Offset 770h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.91 Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_7) — Offset 774h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_S_0, offset 704h.

33.2.92 Pad Configuration DW2 (PAD_CFG_DW2_GPP_S_7) — Offset 778h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.93 Pad Configuration DW3 (PAD_CFG_DW3_GPP_S_7) — Offset 77Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.94 Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_5) — Offset 7D0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.95 Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_5) — Offset 7D4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 7D4h	0080006Ch

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RO	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	2h RW	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0100: 20k PD 1100: 20k PU 1111: Native controller selected by Pad Mode controls the Termination. This field should be set to 1111b for the selected native function that supports dynamic termination override. Refer to Vol1, GPIO chapter, for more info. Others: Reserved **Notes**: 1. The 20K pull-up/pull-down can only be enabled as long as the toggle rate on the signal is no more than 300KHz. 2. If a reserved value is programmed, pad may malfunction. 3. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, PU/PD settings should be programmed first to ensure the input does not float momentarily
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	6Ch RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

33.2.96 Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_5) — Offset 7D8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.97 Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_5) — Offset 7DCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.98 Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_7) — Offset 7F0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.99 Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_7) — Offset 7F4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.100 Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_7) — Offset 7F8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.101 Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_7) — Offset 7FCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.102 Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_8) — Offset 800h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.103 Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_8) — Offset 804h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.104 Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_8) — Offset 808h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.105 Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_8) — Offset 80Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.106 Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_9) — Offset 810h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.107 Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_9) — Offset 814h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.108 Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_9) — Offset 818h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.109 Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_9) — Offset 81Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.110 Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_10) — Offset 820h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.111 Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_10) — Offset 824h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.112 Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_10) — Offset 828h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.113 Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_10) — Offset 82Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.114 Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_11) — Offset 830h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.115 Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_11) — Offset 834h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.116 Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_11) — Offset 838h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.117 Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_11) — Offset 83Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.118 Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_12) — Offset 840h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.119 Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_12) — Offset 844h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.120 Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_12) — Offset 848h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.121 Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_12) — Offset 84Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.122 Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_13) — Offset 850h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.123 Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_13) — Offset 854h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.124 Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_13) — Offset 858h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.125 Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_13) — Offset 85Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.126 Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_14) — Offset 860h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.127 Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_14) — Offset 864h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.128 Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_14) — Offset 868h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.129 Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_14) — Offset 86Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.130 Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_15) — Offset 870h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.131 Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_15) — Offset 874h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.132 Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_15) — Offset 878h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.133 Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_15) — Offset 87Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.134 Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_16) — Offset 880h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.135 Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_16) — Offset 884h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.136 Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_16) — Offset 888h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.137 Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_16) — Offset 88Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.138 Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_17) — Offset 890h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.139 Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_17) — Offset 894h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.140 Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_17) — Offset 898h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.141 Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_17) — Offset 89Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.142 Pad Configuration DW0 (PAD_CFG_DW0_GPP_I_18) — Offset 8A0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.143 Pad Configuration DW1 (PAD_CFG_DW1_GPP_I_18) — Offset 8A4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.144 Pad Configuration DW2 (PAD_CFG_DW2_GPP_I_18) — Offset 8A8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.145 Pad Configuration DW3 (PAD_CFG_DW3_GPP_I_18) — Offset 8ACh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.146 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_0) — Offset 8C0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.147 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_0) — Offset 8C4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4hPAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.148 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_0) — Offset 8C8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6D0000h + 8C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:25	0h RO	**SoundWire Slew Control (sndwslewctrl) (SNDWSLEWCTRL):** 00 = Slow Slew Rate 01 = Middle Slew Rate 10 = Fast Slew Rate 11 = Fastest Slew Rate For iCDG buffers, this field is used to control the slew configuration, but extends beyond SoundWire to I2C, SDMMC and other applicable buffers. The setting may vary from one platform to another.
24	0h RO	**Bus Hold Enable (BUSHLDEN):** This feature uses the same build in pull-up/down resistor. In such, BIOS/FW needs to disable all pull-up/down to 'None' before enabling this feature. 1 = enable bus hold 0 = disable bus hold
23	0h RO	**Data Dependent Weak PU Control (DDPUCTRL):** 0 = normal I/O transmission mode. 1 = weak pull up configuration is overridden to disabled, when the raw RX pad state is 0 in output mode. During DFx mode like BSCAN, SCAN, HVM and etc, the DDPUCRTL shall be constrained to 0.
22	0h RO	**Analog Glitch Filter RX Pad State Select (ANALOGGFRXSEL):** Determine if the internal RX pad state should be subjected to analog glitch filter (implemented within the buffer) or not. This field only make sense when the buffer is configured as an input and is not disabled. 0 = Select non filtered RX pad state 1= Select filtered RX pad state. The mux to select filtered or non filtered RX pad state is implemented within the HIP family. During DFx mode like BSCAN, SCAN, HVM and etc, the AnalogGFRxSel shall be constrained to 0.
21:12	0h RO	**Reserved**
11	0h RO/V	**Pin-strap value (PINSTRAPVAL):** This bit reflects the pin-strap value.
10:9	0h RO	**Reserved**
8	0h RO/V	**VCCIO selection (VCCIOSEL):** This bits is used to select VCCIO If the pad supports programmable VCCIO. The definition of high and low are implementation specific. 0: high voltage 1: low voltage

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Reserved**
4:1	0h RO	**Debounce duration (DEBOUNCE):** The debounce duration of value should be not less than 3. In other words, the value should not be any of 0, 1 and 2. The debounce time should be calculated as (2^debounce) * (glitch filter clock period) For example, when RTC clock (32 KHz) is used for glitch filter and debounce duration is set to 4b1011, the debounce time is (2 ^ 11) * (31.25 us) = 64ms
0	0h RO	**Debounce Enable (DEBEN):** This bit enables or disables the debouncer with the pad. 1 = Enable the debouncer of the pad 0 = Disable the debouncer of the pad

33.2.149 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_0) — Offset 8CCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.150 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_1) — Offset 8D0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.151 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_1) — Offset 8D4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.152 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_1) — Offset 8D8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_H_0, offset 8C8h.

33.2.153 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_1) — Offset 8DCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.154 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_2) — Offset 8E0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.155 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_2) — Offset 8E4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.156 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_2) — Offset 8E8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_H_0, offset 8C8h.

33.2.157 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_2) — Offset 8ECh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.158 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_3) — Offset 8F0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.159 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_3) — Offset 8F4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.160 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_3) — Offset 8F8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.161 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_3) — Offset 8FCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.162 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_4) — Offset 900h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.163 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_4) — Offset 904h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.164 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_4) — Offset 908h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.165 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_4) — Offset 90Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.166 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_5) — Offset 910h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.167 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_5) — Offset 914h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.168 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_5) — Offset 918h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.169 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_5) — Offset 91Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.170 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_6) — Offset 920h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.171 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_6) — Offset 924h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.172 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_6) — Offset 928h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.173 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_6) — Offset 92Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.174 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_7) — Offset 930h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.175 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_7) — Offset 934h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.176 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_7) — Offset 938h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.177 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_7) — Offset 93Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.178 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_8) — Offset 940h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.179 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_8) — Offset 944h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.180 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_8) — Offset 948h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.181 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_8) — Offset 94Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.182 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_9) — Offset 950h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.183 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_9) — Offset 954h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.184 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_9) — Offset 958h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.185 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_9) — Offset 95Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.186 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_10) — Offset 960h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.187 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_10) — Offset 964h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.188 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_10) — Offset 968h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.189 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_10) — Offset 96Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.190 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_11) — Offset 970h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.191 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_11) — Offset 974h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.192 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_11) — Offset 978h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.193 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_11) — Offset 97Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.194 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_12) — Offset 980h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.195 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_12) — Offset 984h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.196 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_12) — Offset 988h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.197 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_12) — Offset 98Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.198 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_13) — Offset 990h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.199 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_13) — Offset 994h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.200 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_13) — Offset 998h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.201 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_13) — Offset 99Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.202 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_15) — Offset 9B0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.203 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_15) — Offset 9B4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.204 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_15) — Offset 9B8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.205 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_15) — Offset 9BCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.206 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_17) — Offset 9D0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.207 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_17) — Offset 9D4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.208 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_17) — Offset 9D8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.209 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_17) — Offset 9DCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.210 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_18) — Offset 9E0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.211 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_18) — Offset 9E4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.212 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_18) — Offset 9E8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.213 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_18) — Offset 9ECh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.214 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_19) — Offset 9F0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.215 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_19) — Offset 9F4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.216 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_19) — Offset 9F8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.217 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_19) — Offset 9FCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.218 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_20) — Offset A00h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.219 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_20) — Offset A04h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.220 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_20) — Offset A08h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.221 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_20) — Offset A0Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.222 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_21) — Offset A10h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.223 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_21) — Offset A14h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.224 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_21) — Offset A18h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.225 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_21) — Offset A1Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.226 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_22) — Offset A20h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.227 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_22) — Offset A24h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.228 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_22) — Offset A28h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.229 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_22) — Offset A2Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.230 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_23) — Offset A30h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.231 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_23) — Offset A34h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.232 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_H_23) — Offset A38h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.233 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_H_23) — Offset A3Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.234 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_0) — Offset A40h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.235 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_0) — Offset A44h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.236 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_0) — Offset A48h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.237 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_0) — Offset A4Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.238 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_1) — Offset A50h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.239 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_1) — Offset A54h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.240 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_1) — Offset A58h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.241 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_1) — Offset A5Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.242 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_2) — Offset A60h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.243 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_2) — Offset A64h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.244 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_2) — Offset A68h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.245 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_2) — Offset A6Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.246 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_3) — Offset A70h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.247 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_3) — Offset A74h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.248 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_3) — Offset A78h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.249 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_3) — Offset A7Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.250 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_4) — Offset A80h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.251 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_4) — Offset A84h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.252 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_4) — Offset A88h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.253 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_4) — Offset A8Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.254 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_5) — Offset A90h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.255 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_5) — Offset A94h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.256 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_5) — Offset A98h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.257 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_5) — Offset A9Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.258 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_6) — Offset AA0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.259 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_6) — Offset AA4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.260 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_6) — Offset AA8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.261 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_6) — Offset AACh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.262 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_7) — Offset AB0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.263 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_7) — Offset AB4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.264 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_7) — Offset AB8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.265 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_7) — Offset ABCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.266 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_8) — Offset AC0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.267 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_8) — Offset AC4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.268 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_8) — Offset AC8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.269 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_8) — Offset ACCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.270 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_9) — Offset AD0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.271 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_9) — Offset AD4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.272 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_9) — Offset AD8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.273 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_9) — Offset ADCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.274 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_10) — Offset AE0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.275 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_10) — Offset AE4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.276 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_10) — Offset AE8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_H_0, offset 8C8h.

33.2.277 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_10) — Offset AECh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.278 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_11) — Offset AF0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.279 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_11) — Offset AF4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.280 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_11) — Offset AF8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.281 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_11) — Offset AFCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.282 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_12) — Offset B00h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.283 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_12) — Offset B04h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.284 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_12) — Offset B08h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_H_0, offset 8C8h.

33.2.285 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_12) — Offset B0Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.286 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_13) — Offset B10h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.287 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_13) — Offset B14h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.288 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_13) — Offset B18h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.289 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_13) — Offset B1Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.290 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_14) — Offset B20h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.291 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_14) — Offset B24h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.292 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_14) — Offset B28h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.293 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_14) — Offset B2Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.294 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_15) — Offset B30h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.295 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_15) — Offset B34h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.296 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_15) — Offset B38h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.297 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_15) — Offset B3Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.298 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_16) — Offset B40h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.299 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_16) — Offset B44h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.300 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_16) — Offset B48h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.301 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_16) — Offset B4Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.302 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_17) — Offset B50h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.303 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_17) — Offset B54h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.304 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_17) — Offset B58h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.305 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_17) — Offset B5Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.306 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_18) — Offset B60h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.307 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_18) — Offset B64h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.308 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_18) — Offset B68h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.309 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_18) — Offset B6Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.2.310 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_19) — Offset B70h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_S_0, offset 700h.

33.2.311 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_19) — Offset B74h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_I_5, offset 7D4h

33.2.312 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_D_19) — Offset B78h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_S_0, offset 708h.

33.2.313 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_D_19) — Offset B7Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_S_0, offset 70Ch.

33.3 GPIO Community 2 Registers

This Section contains the GPIO registers of Community 2- 0x6C section.

Table 33-3. Summary of GPIO Community 2 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8h	4	Family Base Address (FAMBAR)	00000300h
Ch	4	Pad Base Address (PADBAR)	00000700h
10h	4	Miscellaneous Configuration (MISCCFG)	34043200h
20h	4	Pad Ownership (PAD_OWN_DSW_0)	00000000h
24h	4	Pad Ownership (PAD_OWN_DSW_1)	00000000h
28h	4	Pad Ownership (PAD_OWN_DSW_2)	00000000h
80h	4	Pad Configuration Lock (PADCFGLOCK_DSW_0)	00000000h
84h	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_DSW_0)	00000000h
B0h	4	Host Software Pad Ownership (HOSTSW_OWN_DSW_0)	00000000h
100h	4	GPI Interrupt Status (GPI_IS_DSW_0)	00000000h
120h	4	GPI Interrupt Enable (GPI_IE_DSW_0)	00000000h
140h	4	GPI General Purpose Events Status (GPI_GPE_STS_DSW_0)	00000000h
160h	4	GPI General Purpose Events Enable (GPI_GPE_EN_DSW_0)	00000000h
180h	4	SMI Status (GPI_SMI_STS_DSW_0)	00000000h
1A0h	4	SMI Enable (GPI_SMI_EN_DSW_0)	00000000h
1C0h	4	NMI Status (GPI_NMI_STS_DSW_0)	00000000h
1E0h	4	NMI Enable (GPI_NMI_EN_DSW_0)	00000000h
250h	4	Event Trigger Output Enable (EVOUTEN_0)	00000000h
260h	8	Event Trigger Mapping (EVMAP_0)	0000000000000000h
700h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_0)	04000700h
704h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_0)	00003060h
708h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPD_0)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
70Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPD_0)	00000000h
710h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_1)	04000700h
714h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_1)	00003C61h
718h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPD_1)	00000000h
71Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPD_1)	00000000h
720h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_2)	04000700h
724h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_2)	00003C62h
728h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPD_2)	00000000h
72Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPD_2)	00000000h
730h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_3)	04000700h
734h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_3)	00003063h
738h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPD_3)	00000010h
73Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPD_3)	00000000h
740h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_4)	04000600h
744h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_4)	00000064h
748h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPD_4)	00000000h
74Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPD_4)	00000000h
750h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_5)	04000600h
754h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_5)	00000065h
758h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPD_5)	00000000h
75Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPD_5)	00000000h
760h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_6)	04000600h
764h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_6)	00000066h
768h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPD_6)	00000000h
76Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPD_6)	00000000h
770h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_7)	04000200h
774h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_7)	00000067h
778h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPD_7)	00000000h
77Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPD_7)	00000000h
780h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_8)	04000700h
784h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_8)	00000068h
788h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPD_8)	00000000h
78Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPD_8)	00000000h
790h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_9)	04000600h
794h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_9)	00000069h
798h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPD_9)	00000000h
79Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPD_9)	00000000h
7A0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_10)	04000600h
7A4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_10)	0000006Ah
7A8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPD_10)	00000000h
7ACh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPD_10)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
7B0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_11)	04000600h
7B4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_11)	0000006Bh
7B8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPD_11)	00000000h
7BCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPD_11)	00000000h
7C0h	4	Pad Configuration DW0 (PAD_CFG_DW0_INPUT3VSEL)	00000700h
7C4h	4	Pad Configuration DW1 (PAD_CFG_DW1_INPUT3VSEL)	00000000h
7C8h	4	Pad Configuration DW2 (PAD_CFG_DW2_INPUT3VSEL)	00000000h
7CCh	4	Pad Configuration DW3 (PAD_CFG_DW3_INPUT3VSEL)	00000000h
7D0h	4	Pad Configuration DW0 (PAD_CFG_DW0_SLP_LANB)	00000700h
7D4h	4	Pad Configuration DW1 (PAD_CFG_DW1_SLP_LANB)	00000000h
7D8h	4	Pad Configuration DW2 (PAD_CFG_DW2_SLP_LANB)	00000000h
7DCh	4	Pad Configuration DW3 (PAD_CFG_DW3_SLP_LANB)	00000000h
7E0h	4	Pad Configuration DW0 (PAD_CFG_DW0_SLP_SUSB)	00000700h
7E4h	4	Pad Configuration DW1 (PAD_CFG_DW1_SLP_SUSB)	00000000h
7E8h	4	Pad Configuration DW2 (PAD_CFG_DW2_SLP_SUSB)	00000000h
7ECh	4	Pad Configuration DW3 (PAD_CFG_DW3_SLP_SUSB)	00000000h
7F0h	4	Pad Configuration DW0 (PAD_CFG_DW0_WAKEB)	00000700h
7F4h	4	Pad Configuration DW1 (PAD_CFG_DW1_WAKEB)	00000000h
7F8h	4	Pad Configuration DW2 (PAD_CFG_DW2_WAKEB)	00000000h
7FCh	4	Pad Configuration DW3 (PAD_CFG_DW3_WAKEB)	00000000h
800h	4	Pad Configuration DW0 (PAD_CFG_DW0_DRAM_RESETB)	00000700h
804h	4	Pad Configuration DW1 (PAD_CFG_DW1_DRAM_RESETB)	00000000h
808h	4	Pad Configuration DW2 (PAD_CFG_DW2_DRAM_RESETB)	00000000h
80Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_DRAM_RESETB)	00000000h

33.3.1 Family Base Address (FAMBAR) — Offset 8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 8h	00000300h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0300h RO	**Family Base Address (FAMBAR):** This field provides the starting byte-align address of Family0 register sets within a Community. It is meant for software to discover from where the very first Family register (i.e. Family0 register) starts to compute the next Families address offsets.

33.3.2 Pad Base Address (PADBAR) — Offset Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + Ch	00000700h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0700h RO	**Pad Base Address (PADBAR):** This field provides the starting byte-align address of Pad0 register sets within a Community. It is meant for software to discover from where the very first Pad register (i.e. Pad0 register) starts to compute the next Pad address offsets.

33.3.3 Miscellaneous Configuration (MISCCFG) — Offset 10h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 10h	34043200h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	34h RW	**GPIO Driver Mode Interrupt Select (GPDMINTSEL):** IRQ globally for all pads (GPI_IS with corresponding GPI_IE enable). 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255
23:20	0h RO	**Reserved**
19:16	4h RW	**GPIO Group to GPE_DW2 assignment encoding (GPE0_DW2):** This register assigns a specific GPIO Group to the ACPI GPE0[95:64]. The setting is SoC specific.
15:12	3h RW	**GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1):** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The setting is SoC specific.
11:8	2h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0):** This register assigns a specific GPIO Group to the ACPI GPE0[31:0]. The setting is SoC specific.
7	0h RW	**GPIO IOSF Sideband VNNREQ Enable (GPVNNREQEN):** Specify whether the GPIO Community should take part in IOSFSB VNNREQ/ACK handshake 0 = Disable participation in IOSF SB VNNREQ and VNNACK handshake 1 = Enable participation in IOSF SB VNNREQ and VNNACK handshake When this bit set to 1, GPIO controller will de-assert the VNNREQ when there is no outstanding IOSF SB upstream cycle from GPIO controller. When this bit set to 1 and MISCSECCFG.SBTRIGDIS is 0, GPIO controller will assert the VNNREQ to request for the following list of IOSF-SB Message initiation. Event list: IRQ NMI SMI SSMI VNNREQ shall de-assert when MISCSECCFG.SBTRIGDIS is set to 1. As VNNAON IP, GPIO controller will assert the VNNREQ when in reset. The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pwrgate_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this power gating, this register always default to 1.
6	0h RW	**GPIO PGCB Clock Dynamic Partition Clock Gating Enable (GPPGCBDPCGEN):** Specify whether the GPIO Community PGCB clock should take part in partition clock gating 0 = Disable participation in PGCB clock dynamic partition clock gating 1 = Enable participation in PGCB clock dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**GPIO IOSF Sideband Dynamic Partition Clock Gating Enable (GPSIDEDPCGEN):** Specify whether the GPIO Community IOSF sideband clock should take part in partition clock gating 0 = Disable participation in IOSF sideband clock dynamic partition clock gating 1 = Enable participation in IOSF sideband clock dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
4	0h RW	**GPIO RCOMP clock Dynamic Local Clock Gating (GPRCOMPCDLCGEN):** Specify whether the GPIO Community should perform local clock gating on RCOMP clock 0 = Disable dynamic RCOMP clock local clock gating 1 = Enable dynamic RCOMP clock local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
3	0h RW	**GPIO RTC clock Dynamic Local Clock Gating (GPRTCDLCGEN):** Specify whether the GPIO Community should perform local clock gating on RTC clock 0 = Disable dynamic RTC clock local clock gating 1 = Enable dynamic RTC clock local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
2	0h RW	**GSX Static Local Clock Gating (GSXSLCGEN):** Specify whether the GSX controller should be statically clock gated for power saving if it is not enabled (even though the capability is available). 0 = Disable static local clock gating 1 = Enable static local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
1	0h RW	**GPIO Dynamic Partition Clock Gating Enable (GPDPCGEN):** Specify whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
0	0h RW	**GPIO Dynamic Local Clock Gating Enable (GPDLCGEN):** Specify whether the GPIO Community should perform local clock gating 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0

33.3.4 Pad Ownership (PAD_OWN_DSW_0) — Offset 20h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 20h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPD_7):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPD_6):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPD_5):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPD_4):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPD_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPD_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPD_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPD_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.3.5 Pad Ownership (PAD_OWN_DSW_1) — Offset 24h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 24h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RO	**Pad Ownership (PAD_OWN_WAKEB):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RO	**Pad Ownership (PAD_OWN_SLP_SUSB):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RO	**Pad Ownership (PAD_OWN_SLP_LANB):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RO	**Pad Ownership (PAD_OWN_INPUT3VSEL):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPD_11):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPD_10):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPD_9):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPD_8):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.3.6 Pad Ownership (PAD_OWN_DSW_2) — Offset 28h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 28h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**Pad Ownership (PAD_OWN_DRAM_RESETB):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.3.7 Pad Configuration Lock (PADCFGLOCK_DSW_0) — Offset 80h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 80h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RO	**Pad Config Lock (PADCFGLOCK_DRAM_RESETB):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
15	0h RO	**Pad Config Lock (PADCFGLOCK_WAKEB):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO	**Pad Config Lock (PADCFGLOCK_SLP_SUSB):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
13	0h RO	**Pad Config Lock (PADCFGLOCK_SLP_LANB):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO	**Pad Config Lock (PADCFGLOCK_INPUT3VSEL):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_11):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_10):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_9):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_8):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_7):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_6):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_5):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_4):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

33.3.8 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_DSW_0) — Offset 84h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 84h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RO	**Pad Config Lock TXState (PADCFGLOCKTX_DRAM_RESETB):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
15	0h RO	**Pad Config Lock TXState (PADCFGLOCKTX_WAKEB):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO	**Pad Config Lock TXState (PADCFGLOCKTX_SLP_SUSB):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
13	0h RO	**Pad Config Lock TXState (PADCFGLOCKTX_SLP_LANB):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO	**Pad Config Lock TXState (PADCFGLOCKTX_INPUT3VSEL):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_11):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_10):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_9):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_8):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_7):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_6):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_5):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_4):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

33.3.9 Host Software Pad Ownership (HOSTSW_OWN_DSW_0) — Offset B0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RO	**HOSTSW_OWN_DRAM_RESETB:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
15	0h RO	**HOSTSW_OWN_WAKEB:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO	**HOSTSW_OWN_SLP_SUSB:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
13	0h RO	**HOSTSW_OWN_SLP_LANB:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
12	0h RO	**HOSTSW_OWN_INPUT3VSEL:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**HOSTSW_OWN_GPD_11:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
10	0h RW	**HOSTSW_OWN_GPD_10:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
9	0h RW	**HOSTSW_OWN_GPD_9:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**HOSTSW_OWN_GPD_8:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
7	0h RW	**HOSTSW_OWN_GPD_7:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
6	0h RW	**HOSTSW_OWN_GPD_6:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**HOSTSW_OWN_GPD_5:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
4	0h RW	**HOSTSW_OWN_GPD_4:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
3	0h RW	**HOSTSW_OWN_GPD_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HOSTSW_OWN_GPD_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RW	**HOSTSW_OWN_GPD_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RW	**HOSTSW_OWN_GPD_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

33.3.10 GPI Interrupt Status (GPI_IS_DSW_0) — Offset 100h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 100h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RO	**GPI Interrupt Status (GPI_INT_STS_DRAM_RESETB):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
15	0h RO	**GPI Interrupt Status (GPI_INT_STS_WAKEB):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO	**GPI Interrupt Status (GPI_INT_STS_SLP_SUSB):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RO	**GPI Interrupt Status (GPI_INT_STS_SLP_LANB):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RO	**GPI Interrupt Status (GPI_INT_STS_INPUT3VSEL):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_11):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_10):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_9):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_8):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_7):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_6):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_5):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_4):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.3.11 GPI Interrupt Enable (GPI_IE_DSW_0) — Offset 120h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 120h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RO	**GPI Interrupt Enable (GPI_INT_EN_DRAM_RESETB):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
15	0h RO	**GPI Interrupt Enable (GPI_INT_EN_WAKEB):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RO	**GPI Interrupt Enable (GPI_INT_EN_SLP_SUSB):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	**GPI Interrupt Enable (GPI_INT_EN_SLP_LANB):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RO	**GPI Interrupt Enable (GPI_INT_EN_INPUT3VSEL):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_11):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_10):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_9):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_8):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_7):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_6):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_5):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_4):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.3.12 GPI General Purpose Events Status (GPI_GPE_STS_DSW_0) — Offset 140h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 140h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RO	**GPI General Purpose Events Status (GPI_GPE_STS_DRAM_RESETB):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
15	0h RO	**GPI General Purpose Events Status (GPI_GPE_STS_WAKEB):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO	**GPI General Purpose Events Status (GPI_GPE_STS_SLP_SUSB):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
13	0h RO	**GPI General Purpose Events Status (GPI_GPE_STS_SLP_LANB):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
12	0h RO	**GPI General Purpose Events Status (GPI_GPE_STS_INPUT3VSEL):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_11):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_10):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
9	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_9):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_8):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_7):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_6):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_5):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_4):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.3.13 GPI General Purpose Events Enable (GPI_GPE_EN_DSW_0) — Offset 160h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 160h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RO	**GPI General Purpose Events Enable (GPI_GPE_EN_DRAM_RESETB):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
15	0h RO	**GPI General Purpose Events Enable (GPI_GPE_EN_WAKEB):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RO	**GPI General Purpose Events Enable (GPI_GPE_EN_SLP_SUSB):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	**GPI General Purpose Events Enable (GPI_GPE_EN_SLP_LANB):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
12	0h RO	**GPI General Purpose Events Enable (GPI_GPE_EN_INPUT3VSEL):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_11):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_10):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_9):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_8):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_7):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_6):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_5):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_4):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.3.14 SMI Status (GPI_SMI_STS_DSW_0) — Offset 180h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 180h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RSV	**GPI SMI Status (GPI_SMI_STS_DRAM_RESETB):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
15	0h RSV	**GPI SMI Status (GPI_SMI_STS_WAKEB):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RSV	**GPI SMI Status (GPI_SMI_STS_SLP_SUSB):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
13	0h RSV	**GPI SMI Status (GPI_SMI_STS_SLP_LANB):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RSV	**GPI SMI Status (GPI_SMI_STS_INPUT3VSEL):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
11	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPD_11):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPD_10):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
9	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPD_9):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPD_8):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
7	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPD_7):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPD_6):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
5	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPD_5):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPD_4):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
3	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPD_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPD_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPD_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPD_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

33.3.15 SMI Enable (GPI_SMI_EN_DSW_0) — Offset 1A0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 1A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RSV	**GPI SMI Enable (GPI_SMI_EN_DRAM_RESETB):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
15	0h RSV	**GPI SMI Enable (GPI_SMI_EN_WAKEB):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
14	0h RSV	**GPI SMI Enable (GPI_SMI_EN_SLP_SUSB):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
13	0h RSV	**GPI SMI Enable (GPI_SMI_EN_SLP_LANB):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
12	0h RSV	**GPI SMI Enable (GPI_SMI_EN_INPUT3VSEL):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPD_11):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
10	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPD_10):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
9	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPD_9):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPD_8):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
7	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPD_7):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
6	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPD_6):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPD_5):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
4	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPD_4):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
3	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPD_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPD_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPD_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPD_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

33.3.16 NMI Status (GPI_NMI_STS_DSW_0) — Offset 1C0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 1C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RSV	**GPI NMI Status (GPI_NMI_STS_DRAM_RESETB):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
15	0h RSV	**GPI NMI Status (GPI_NMI_STS_WAKEB):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RSV	**GPI NMI Status (GPI_NMI_STS_SLP_SUSB):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RSV	**GPI NMI Status (GPI_NMI_STS_SLP_LANB):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
12	0h RSV	**GPI NMI Status (GPI_NMI_STS_INPUT3VSEL):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPD_11):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPD_10):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
9	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPD_9):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPD_8):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPD_7):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPD_6):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPD_5):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPD_4):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPD_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPD_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPD_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPD_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.3.17 NMI Enable (GPI_NMI_EN_DSW_0) — Offset 1E0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 1E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RSV	**GPI NMI Enable (GPI_NMI_EN_DRAM_RESETB):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
15	0h RSV	**GPI NMI Enable (GPI_NMI_EN_WAKEB):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RSV	**GPI NMI Enable (GPI_NMI_EN_SLP_SUSB):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RSV	**GPI NMI Enable (GPI_NMI_EN_SLP_LANB):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
12	0h RSV	**GPI NMI Enable (GPI_NMI_EN_INPUT3VSEL):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPD_11):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPD_10):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
9	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPD_9):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
8	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPD_8):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPD_7):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPD_6):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPD_5):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPD_4):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPD_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPD_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPD_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPD_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.3.18 Event Trigger Output Enable (EVOUTEN_0) — Offset 250h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 250h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**EV Trigger Output Enable (EVOUTEN):** When a bit is '0', the corresponding output is masked to '0' I.e. no valid pin assigned to. When a bit is set to '1' the corresponding output is enabled and depends on the EVMAP settings.

33.3.19 Event Trigger Mapping (EVMAP_0) — Offset 260h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	64 bit	FD6C0000h + 260h	0000000000000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
63:61	0h RO	**Reserved**
60	0h RW	**Event Trigger Mapping to PMU[15] (EVMAPPM_15):** 000b = GPIO[i] event trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
59:57	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
56	0h RW	**Event Trigger Mapping to PMU[14] (EVMAPPM_14):** 000b = GPIO[i] event trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
55:53	0h RO	**Reserved**
52	0h RW	**Event Trigger Mapping to PMU[13] (EVMAPPM_13):** 000b = GPIO[i] event trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
51:49	0h RO	**Reserved**
48	0h RW	**Event Trigger Mapping to PMU[12] (EVMAPPM_12):** 000b = GPIO[i] event trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
47:45	0h RO	**Reserved**
44	0h RW	**Event Trigger Mapping to PMU[11] (EVMAPPM_11):** 000b = GPIO[i] event trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
43:41	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
40	0h RW	**Event Trigger Mapping to PMU[10] (EVMAPPM_10):** 000b = GPIO[i] event trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
39:37	0h RO	**Reserved**
36	0h RW	**Event Trigger Mapping to PMU[9] (EVMAPPM_9):** 000b = GPIO[i] event trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
35:33	0h RO	**Reserved**
32	0h RW	**Event Trigger Mapping to PMU[8] (EVMAPPM_8):** 000b = GPIO[i] event trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
31:29	0h RO	**Reserved**
28	0h RW	**Event Trigger Mapping to PMU[7] (EVMAPPM_7):** 000b = GPIO[i] event trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
27:25	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Event Trigger Mapping to PMU[6] (EVMAPPM_6):** 000b = GPIO[i] event trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
23:21	0h RO	**Reserved**
20	0h RW	**Event Trigger Mapping to PMU[5] (EVMAPPM_5):** 000b = GPIO[i] event trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
19:17	0h RO	**Reserved**
16	0h RW	**Event Trigger Mapping to PMU[4] (EVMAPPM_4):** 000b = GPIO[i] event trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
15:13	0h RO	**Reserved**
12	0h RW	**Event Trigger Mapping to PMU[3] (EVMAPPM_3):** 000b = GPIO[i] event trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
11:9	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Event Trigger Mapping to PMU[2] (EVMAPPM_2):** 000b = GPIO[i] event trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
7:5	0h RO	**Reserved**
4	0h RW	**Event Trigger Mapping to PMU[1] (EVMAPPM_1):** 000b = GPIO[i] event trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community
3:1	0h RO	**Reserved**
0	0h RW	**Event Trigger Mapping to PMU[0] (EVMAPPM_0):** 000b = GPIO[i] event trigger 001b = GPIO[i+16*1] event trigger 010b = GPIO[i+16*2] event trigger 011b = GPIO[i+16*3] event trigger 100b = GPIO[i+16*4] event trigger 101b = GPIO[i+16*5] event trigger 110b = GPIO[i+16*6] event trigger 111b = GPIO[i+16*7] event trigger i = 0, 1, ..., 14, 15 series continues if more than 128 pins per community

33.3.20 Pad Configuration DW0 (PAD_CFG_DW0_GPD_0) — Offset 700h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 700h	04000700h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the SoC responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)

Bit Range	Default & Access	Field Name (ID): Description
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	**Reserved**
10	1h RO/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

33.3.21 Pad Configuration DW1 (PAD_CFG_DW1_GPD_0) — Offset 704h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 704h	00003060h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RO	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	Ch RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0100: 20k PD 1100: 20k PU 1111: Native controller selected by Pad Mode controls the Termination. This field should be set to 1111b for the selected native function that supports dynamic termination override. Refer to Vol1, GPIO chapter, for more info. Others: Reserved **Notes**: 1. The 20K pull-up/pull-down can only be enabled as long as the toggle rate on the signal is no more than 300KHz. 2. If a reserved value is programmed, pad may malfunction. 3. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, PU/PD settings should be programmed first to ensure the input does not float momentarily
9:8	0h RO	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	60h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

33.3.22 Pad Configuration DW2 (PAD_CFG_DW2_GPD_0) — Offset 708h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 708h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:25	0h RO	**SoundWire Slew Control (sndwslewctrl) (SNDWSLEWCTRL):** 00 = Slow Slew Rate 01 = Middle Slew Rate 10 = Fast Slew Rate 11 = Fastest Slew Rate For iCDG buffers, this field is used to control the slew configuration, but extends beyond SoundWire to I2C, SDMMC and other applicable buffers. The setting may vary from one platform to another.
24	0h RO	**Bus Hold Enable (BUSHLDEN):** This feature uses the same build in pull-up/down resistor. In such, BIOS/FW needs to disable all pull-up/down to 'None' before enabling this feature. 1 = enable bus hold 0 = disable bus hold
23	0h RO	**Data Dependent Weak PU Control (DDPUCTRL):** 0 = normal I/O transmission mode. 1 = weak pull up configuration is overridden to disabled, when the raw RX pad state is 0 in output mode. During DFx mode like BSCAN, SCAN, HVM and etc, the DDPUCRTL shall be constrained to 0.
22	0h RO	**Analog Glitch Filter RX Pad State Select (ANALOGGFRXSEL):** Determine if the internal RX pad state should be subjected to analog glitch filter (implemented within the buffer) or not. This field only make sense when the buffer is configured as an input and is not disabled. 0 = Select non filtered RX pad state 1= Select filtered RX pad state. The mux to select filtered or non filtered RX pad state is implemented within the HIP family. During DFx mode like BSCAN, SCAN, HVM and etc, the AnalogGFRxSel shall be constrained to 0.
21:9	0h RO	**Reserved**
8	0h RO	**VCCIO selection (VCCIOSEL):** This bits is used to select VCCIO If the pad supports programmable VCCIO. The definition of high and low are implementation specific. 0: high voltage 1: low voltage

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Reserved**
4:1	0h RO	**Debounce duration (DEBOUNCE):** The debounce duration of value should be not less than 3. In other words, the value should not be any of 0, 1 and 2. The debounce time should be calculated as (2^debounce) * (glitch filter clock period) For example, when RTC clock (32 KHz) is used for glitch filter and debounce duration is set to 4b1011, the debounce time is (2 ^ 11) * (31.25 us) = 64ms
0	0h RO	**Debounce Enable (DEBEN):** This bit enables or disables the debouncer with the pad. 1 = Enable the debouncer of the pad 0 = Disable the debouncer of the pad

33.3.23 Pad Configuration DW3 (PAD_CFG_DW3_GPD_0) — Offset 70Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 70Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

33.3.24 Pad Configuration DW0 (PAD_CFG_DW0_GPD_1) — Offset 710h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPD_0, offset 700h.

33.3.25 Pad Configuration DW1 (PAD_CFG_DW1_GPD_1) — Offset 714h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPD_0, offset 704h.

33.3.26 Pad Configuration DW2 (PAD_CFG_DW2_GPD_1) — Offset 718h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPD_0, offset 708h.

33.3.27 Pad Configuration DW3 (PAD_CFG_DW3_GPD_1) — Offset 71Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPD_0, offset 70Ch.

33.3.28 Pad Configuration DW0 (PAD_CFG_DW0_GPD_2) — Offset 720h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPD_0, offset 700h.

33.3.29 Pad Configuration DW1 (PAD_CFG_DW1_GPD_2) — Offset 724h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPD_0, offset 704h.

33.3.30 Pad Configuration DW2 (PAD_CFG_DW2_GPD_2) — Offset 728h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPD_0, offset 708h.

33.3.31 Pad Configuration DW3 (PAD_CFG_DW3_GPD_2) — Offset 72Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPD_0, offset 70Ch.

33.3.32 Pad Configuration DW0 (PAD_CFG_DW0_GPD_3) — Offset 730h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPD_0, offset 700h.

33.3.33 Pad Configuration DW1 (PAD_CFG_DW1_GPD_3) — Offset 734h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPD_0, offset 704h.

33.3.34 Pad Configuration DW2 (PAD_CFG_DW2_GPD_3) — Offset 738h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPD_0, offset 708h.

33.3.35 Pad Configuration DW3 (PAD_CFG_DW3_GPD_3) — Offset 73Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPD_0, offset 70Ch.

33.3.36 Pad Configuration DW0 (PAD_CFG_DW0_GPD_4) — Offset 740h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPD_0, offset 700h.

33.3.37 Pad Configuration DW1 (PAD_CFG_DW1_GPD_4) — Offset 744h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPD_0, offset 704h.

33.3.38 Pad Configuration DW2 (PAD_CFG_DW2_GPD_4) — Offset 748h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPD_0, offset 708h.

33.3.39 Pad Configuration DW3 (PAD_CFG_DW3_GPD_4) — Offset 74Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPD_0, offset 70Ch.

33.3.40 Pad Configuration DW0 (PAD_CFG_DW0_GPD_5) — Offset 750h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPD_0, offset 700h.

33.3.41 Pad Configuration DW1 (PAD_CFG_DW1_GPD_5) — Offset 754h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPD_0, offset 704h.

33.3.42 Pad Configuration DW2 (PAD_CFG_DW2_GPD_5) — Offset 758h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPD_0, offset 708h.

33.3.43 Pad Configuration DW3 (PAD_CFG_DW3_GPD_5) — Offset 75Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPD_0, offset 70Ch.

33.3.44 Pad Configuration DW0 (PAD_CFG_DW0_GPD_6) — Offset 760h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPD_0, offset 700h.

33.3.45 Pad Configuration DW1 (PAD_CFG_DW1_GPD_6) — Offset 764h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPD_0, offset 704h.

33.3.46 Pad Configuration DW2 (PAD_CFG_DW2_GPD_6) — Offset 768h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPD_0, offset 708h.

33.3.47 Pad Configuration DW3 (PAD_CFG_DW3_GPD_6) — Offset 76Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPD_0, offset 70Ch.

33.3.48 Pad Configuration DW0 (PAD_CFG_DW0_GPD_7) — Offset 770h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPD_0, offset 700h.

33.3.49 Pad Configuration DW1 (PAD_CFG_DW1_GPD_7) — Offset 774h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPD_0, offset 704h.

33.3.50 Pad Configuration DW2 (PAD_CFG_DW2_GPD_7) — Offset 778h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6C0000h + 778h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:25	0h RO	**SoundWire Slew Control (sndwslewctrl) (SNDWSLEWCTRL):** 00 = Slow Slew Rate 01 = Middle Slew Rate 10 = Fast Slew Rate 11 = Fastest Slew Rate For iCDG buffers, this field is used to control the slew configuration, but extends beyond SoundWire to I2C, SDMMC and other applicable buffers. The setting may vary from one platform to another.
24	0h RO	**Bus Hold Enable (BUSHLDEN):** This feature uses the same build in pull-up/down resistor. In such, BIOS/FW needs to disable all pull-up/down to 'None' before enabling this feature. 1 = enable bus hold 0 = disable bus hold
23	0h RO	**Data Dependent Weak PU Control (DDPUCTRL):** 0 = normal I/O transmission mode. 1 = weak pull up configuration is overridden to disabled, when the raw RX pad state is 0 in output mode. During DFx mode like BSCAN, SCAN, HVM and etc, the DDPUCRTL shall be constrained to 0.
22	0h RO	**Analog Glitch Filter RX Pad State Select (ANALOGGFRXSEL):** Determine if the internal RX pad state should be subjected to analog glitch filter (implemented within the buffer) or not. This field only make sense when the buffer is configured as an input and is not disabled. 0 = Select non filtered RX pad state 1= Select filtered RX pad state. The mux to select filtered or non filtered RX pad state is implemented within the HIP family. During DFx mode like BSCAN, SCAN, HVM and etc, the AnalogGFRxSel shall be constrained to 0.

Bit Range	Default & Access	Field Name (ID): Description
21:12	0h RO	**Reserved**
11	0h RO/V	**Pin-strap value (PINSTRAPVAL):** This bit reflects the pin-strap value.
10:9	0h RO	**Reserved**
8	0h RO	**VCCIO selection (VCCIOSEL):** This bits is used to select VCCIO If the pad supports programmable VCCIO. The definition of high and low are implementation specific. 0: high voltage 1: low voltage
7:5	0h RO	**Reserved**
4:1	0h RO	**Debounce duration (DEBOUNCE):** The debounce duration of value should be not less than 3. In other words, the value should not be any of 0, 1 and 2. The debounce time should be calculated as (2^debounce) * (glitch filter clock period) For example, when RTC clock (32 KHz) is used for glitch filter and debounce duration is set to 4b1011, the debounce time is (2 ^ 11) * (31.25 us) = 64ms
0	0h RO	**Debounce Enable (DEBEN):** This bit enables or disables the debouncer with the pad. 1 = Enable the debouncer of the pad 0 = Disable the debouncer of the pad

33.3.51 Pad Configuration DW3 (PAD_CFG_DW3_GPD_7) — Offset 77Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPD_0, offset 70Ch.

33.3.52 Pad Configuration DW0 (PAD_CFG_DW0_GPD_8) — Offset 780h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPD_0, offset 700h.

33.3.53 Pad Configuration DW1 (PAD_CFG_DW1_GPD_8) — Offset 784h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPD_0, offset 704h.

33.3.54 Pad Configuration DW2 (PAD_CFG_DW2_GPD_8) — Offset 788h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPD_0, offset 708h.

33.3.55 Pad Configuration DW3 (PAD_CFG_DW3_GPD_8) — Offset 78Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPD_0, offset 70Ch.

33.3.56 Pad Configuration DW0 (PAD_CFG_DW0_GPD_9) — Offset 790h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPD_0, offset 700h.

33.3.57 Pad Configuration DW1 (PAD_CFG_DW1_GPD_9) — Offset 794h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPD_0, offset 704h.

33.3.58 Pad Configuration DW2 (PAD_CFG_DW2_GPD_9) — Offset 798h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPD_0, offset 708h.

33.3.59 Pad Configuration DW3 (PAD_CFG_DW3_GPD_9) — Offset 79Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPD_0, offset 70Ch.

33.3.60 Pad Configuration DW0 (PAD_CFG_DW0_GPD_10) — Offset 7A0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPD_0, offset 700h.

33.3.61 Pad Configuration DW1 (PAD_CFG_DW1_GPD_10) — Offset 7A4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPD_0, offset 704h.

33.3.62 Pad Configuration DW2 (PAD_CFG_DW2_GPD_10) — Offset 7A8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPD_0, offset 708h.

33.3.63 Pad Configuration DW3 (PAD_CFG_DW3_GPD_10) — Offset 7ACh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPD_0, offset 70Ch.

33.3.64 Pad Configuration DW0 (PAD_CFG_DW0_GPD_11) — Offset 7B0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPD_0, offset 700h.

33.3.65 Pad Configuration DW1 (PAD_CFG_DW1_GPD_11) — Offset 7B4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPD_0, offset 704h.

33.3.66 Pad Configuration DW2 (PAD_CFG_DW2_GPD_11) — Offset 7B8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPD_0, offset 708h.

33.3.67 Pad Configuration DW3 (PAD_CFG_DW3_GPD_11) — Offset 7BCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPD_0, offset 70Ch.

33.3.68 Pad Configuration DW0 (PAD_CFG_DW0_INPUT3VSEL) — Offset 7C0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPD_0, offset 700h.

33.3.69 Pad Configuration DW1 (PAD_CFG_DW1_INPUT3VSEL) — Offset 7C4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPD_0, offset 704h.

33.3.70 Pad Configuration DW2 (PAD_CFG_DW2_INPUT3VSEL) — Offset 7C8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPD_0, offset 708h.

33.3.71 Pad Configuration DW3 (PAD_CFG_DW3_INPUT3VSEL) — Offset 7CCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPD_0, offset 70Ch.

33.3.72 Pad Configuration DW0 (PAD_CFG_DW0_SLP_LANB) — Offset 7D0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPD_0, offset 700h.

33.3.73 Pad Configuration DW1 (PAD_CFG_DW1_SLP_LANB) — Offset 7D4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPD_0, offset 704h.

33.3.74 Pad Configuration DW2 (PAD_CFG_DW2_SLP_LANB) — Offset 7D8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPD_0, offset 708h.

33.3.75 Pad Configuration DW3 (PAD_CFG_DW3_SLP_LANB) — Offset 7DCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPD_0, offset 70Ch.

33.3.76 Pad Configuration DW0 (PAD_CFG_DW0_SLP_SUSB) — Offset 7E0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPD_0, offset 700h.

33.3.77 Pad Configuration DW1 (PAD_CFG_DW1_SLP_SUSB) — Offset 7E4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPD_0, offset 704h.

33.3.78 Pad Configuration DW2 (PAD_CFG_DW2_SLP_SUSB) — Offset 7E8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPD_0, offset 708h.

33.3.79 Pad Configuration DW3 (PAD_CFG_DW3_SLP_SUSB) — Offset 7ECh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPD_0, offset 70Ch.

33.3.80 Pad Configuration DW0 (PAD_CFG_DW0_WAKEB) — Offset 7F0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPD_0, offset 700h.

33.3.81 Pad Configuration DW1 (PAD_CFG_DW1_WAKEB) — Offset 7F4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPD_0, offset 704h.

33.3.82 Pad Configuration DW2 (PAD_CFG_DW2_WAKEB) — Offset 7F8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPD_0, offset 708h.

33.3.83 Pad Configuration DW3 (PAD_CFG_DW3_WAKEB) — Offset 7FCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPD_0, offset 70Ch.

33.3.84 Pad Configuration DW0 (PAD_CFG_DW0_DRAM_RESETB) — Offset 800h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPD_0, offset 700h.

33.3.85 Pad Configuration DW1 (PAD_CFG_DW1_DRAM_RESETB) — Offset 804h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPD_0, offset 704h.

33.3.86 Pad Configuration DW2 (PAD_CFG_DW2_DRAM_RESETB) — Offset 808h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPD_0, offset 708h.

33.3.87 Pad Configuration DW3 (PAD_CFG_DW3_DRAM_RESETB) — Offset 80Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPD_0, offset 70Ch.

33.4 GPIO Community 4 Registers

This Section contains the GPIO registers of Community 4- 0x6A section.

Table 33-4. Summary of GPIO Community 4 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8h	4	Family Base Address (FAMBAR)	00000300h
Ch	4	Pad Base Address (PADBAR)	00000700h
10h	4	Miscellaneous Configuration (MISCCFG)	36043200h
20h	4	Pad Ownership (PAD_OWN_GPP_C_0)	00000000h
24h	4	Pad Ownership (PAD_OWN_GPP_C_1)	00000000h
28h	4	Pad Ownership (PAD_OWN_GPP_C_2)	00000000h
2Ch	4	Pad Ownership (PAD_OWN_GPP_F_0)	00000000h
30h	4	Pad Ownership (PAD_OWN_GPP_F_1)	00000000h
34h	4	Pad Ownership (PAD_OWN_GPP_F_2)	00000000h
38h	4	Pad Ownership (PAD_OWN_GPP_F_3)	00000000h
3Ch	4	Pad Ownership (PAD_OWN_HVCMOS_0)	00000000h
40h	4	Pad Ownership (PAD_OWN_GPP_E_0)	00000000h
44h	4	Pad Ownership (PAD_OWN_GPP_E_1)	00000000h
48h	4	Pad Ownership (PAD_OWN_GPP_E_2)	00000000h
4Ch	4	Pad Ownership (PAD_OWN_GPP_E_3)	00000000h
50h	4	Pad Ownership (PAD_OWN_JTAG_0)	00000000h
54h	4	Pad Ownership (PAD_OWN_JTAG_1)	00000000h
80h	4	Pad Configuration Lock (PADCFGLOCK_GPP_C_0)	00000000h
84h	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_C_0)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
88h	4	Pad Configuration Lock (PADCFGLOCK_GPP_F_0)	00000000h
8Ch	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_F_0)	00000000h
90h	4	Pad Configuration Lock (PADCFGLOCK_HVCMOS_0)	00000000h
94h	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_HVCMOS_0)	00000000h
98h	4	Pad Configuration Lock (PADCFGLOCK_GPP_E_0)	00000000h
9Ch	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_E_0)	00000000h
A0h	4	Pad Configuration Lock (PADCFGLOCK_JTAG_0)	00000000h
A4h	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_JTAG_0)	00000000h
B0h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_C_0)	00000000h
B4h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_F_0)	00000000h
B8h	4	Host Software Pad Ownership (HOSTSW_OWN_HVCMOS_0)	00000000h
BCh	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_E_0)	00000000h
C0h	4	Host Software Pad Ownership (HOSTSW_OWN_JTAG_0)	00000000h
100h	4	GPI Interrupt Status (GPI_IS_GPP_C_0)	00000000h
104h	4	GPI Interrupt Status (GPI_IS_GPP_F_0)	00000000h
108h	4	GPI Interrupt Status (GPI_IS_HVCMOS_0)	00000000h
10Ch	4	GPI Interrupt Status (GPI_IS_GPP_E_0)	00000000h
110h	4	GPI Interrupt Status (GPI_IS_JTAG_0)	00000000h
120h	4	GPI Interrupt Enable (GPI_IE_GPP_C_0)	00000000h
124h	4	GPI Interrupt Enable (GPI_IE_GPP_F_0)	00000000h
128h	4	GPI Interrupt Enable (GPI_IE_HVCMOS_0)	00000000h
12Ch	4	GPI Interrupt Enable (GPI_IE_GPP_E_0)	00000000h
130h	4	GPI Interrupt Enable (GPI_IE_JTAG_0)	00000000h
140h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_0)	00000000h
144h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_0)	00000000h
148h	4	GPI General Purpose Events Status (GPI_GPE_STS_HVCMOS_0)	00000000h
14Ch	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_E_0)	00000000h
150h	4	GPI General Purpose Events Status (GPI_GPE_STS_JTAG_0)	00000000h
160h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_0)	00000000h
164h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_0)	00000000h
168h	4	GPI General Purpose Events Enable (GPI_GPE_EN_HVCMOS_0)	00000000h
16Ch	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_E_0)	00000000h
170h	4	GPI General Purpose Events Enable (GPI_GPE_EN_JTAG_0)	00000000h
180h	4	SMI Status (GPI_SMI_STS_GPP_C_0)	00000000h
184h	4	SMI Status (GPI_SMI_STS_GPP_F_0)	00000000h
188h	4	SMI Status (GPI_SMI_STS_HVCMOS_0)	00000000h
18Ch	4	SMI Status (GPI_SMI_STS_GPP_E_0)	00000000h
190h	4	SMI Status (GPI_SMI_STS_JTAG_0)	00000000h
1A0h	4	SMI Enable (GPI_SMI_EN_GPP_C_0)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1A4h	4	SMI Enable (GPI_SMI_EN_GPP_F_0)	00000000h
1A8h	4	SMI Enable (GPI_SMI_EN_HVCMOS_0)	00000000h
1ACh	4	SMI Enable (GPI_SMI_EN_GPP_E_0)	00000000h
1B0h	4	SMI Enable (GPI_SMI_EN_JTAG_0)	00000000h
1C0h	4	NMI Status (GPI_NMI_STS_GPP_C_0)	00000000h
1C4h	4	NMI Status (GPI_NMI_STS_GPP_F_0)	00000000h
1C8h	4	NMI Status (GPI_NMI_STS_HVCMOS_0)	00000000h
1CCh	4	NMI Status (GPI_NMI_STS_GPP_E_0)	00000000h
1D0h	4	NMI Status (GPI_NMI_STS_JTAG_0)	00000000h
1E0h	4	NMI Enable (GPI_NMI_EN_GPP_C_0)	00000000h
1E4h	4	NMI Enable (GPI_NMI_EN_GPP_F_0)	00000000h
1E8h	4	NMI Enable (GPI_NMI_EN_HVCMOS_0)	00000000h
1ECh	4	NMI Enable (GPI_NMI_EN_GPP_E_0)	00000000h
1F0h	4	NMI Enable (GPI_NMI_EN_JTAG_0)	00000000h
21Ch	4	GSX Controller Capabilities (GSX_CAP)	00000000h
220h	4	GSX Channel-0 Capabilities DW0 (GSX_C0CAP_DW0)	00000000h
224h	4	GSX Channel-0 Capabilities DW1 (GSX_C0CAP_DW1)	00012000h
228h	4	GSX Channel-0 GP Input Level DW0 (GSX_C0GPILVL_DW0)	00000000h
22Ch	4	GSX Channel-0 GP Input Level DW1 (GSX_C0GPILVL_DW1)	00000000h
230h	4	GSX Channel-0 GP Output Level DW0 (GSX_C0GPOLVL_DW0)	00000000h
234h	4	GSX Channel-0 GP Output Level DW1 (GSX_C0GPOLVL_DW1)	00000000h
238h	4	GSX Channel-0 Command (GSX_C0CMD)	00000000h
23Ch	4	GSX Channel-0 Test Mode (GSX_C0TM)	00000000h
700h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_0)	44000700h
704h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_0)	0000006Eh
708h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_C_0)	00000000h
70Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_C_0)	00000000h
710h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_1)	44000700h
714h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_1)	0000006Fh
718h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_C_1)	00000000h
71Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_C_1)	00000000h
720h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_2)	44000200h
724h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_2)	00000070h
728h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_C_2)	00000000h
72Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_C_2)	00000000h
730h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_3)	44000700h
734h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_3)	00000071h
738h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_C_3)	00000000h
73Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_C_3)	00000000h
740h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_4)	44000700h
744h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_4)	00000072h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
748h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_C_4)	00000000h
74Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_C_4)	00000000h
750h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_5)	44000200h
754h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_5)	00000073h
758h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_C_5)	00000000h
75Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_C_5)	00000000h
760h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_6)	44000300h
764h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_6)	00000074h
768h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_C_6)	00000000h
76Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_C_6)	00000000h
770h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_7)	44000300h
774h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_7)	00000075h
778h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_C_7)	00000000h
77Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_C_7)	00000000h
880h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_0)	44000700h
884h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_0)	00000056h
888h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_0)	00000100h
88Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_0)	00000000h
890h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_1)	44000700h
894h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_1)	00003057h
898h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_1)	00000100h
89Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_1)	00000000h
8A0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_2)	44000700h
8A4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_2)	00000058h
8A8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_2)	00000100h
8ACh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_2)	00000000h
8B0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_3)	44000700h
8B4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_3)	00003059h
8B8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_3)	00000100h
8BCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_3)	00000000h
8C0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_4)	44000700h
8C4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_4)	0000005Ah
8C8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_4)	00000100h
8CCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_4)	00000000h
8D0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_5)	44000B00h
8D4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_5)	0000005Bh
8D8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_5)	00000100h
8DCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_5)	00000000h
8E0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_6)	44000300h
8E4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_6)	0000005Ch
8E8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_6)	00000100h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8ECh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_6)	00000000h
8F0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_7)	44000200h
8F4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_7)	0000005Dh
8F8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_7)	00000000h
8FCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_7)	00000000h
920h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_10)	44000200h
924h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_10)	00000060h
928h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_10)	00000000h
92Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_10)	00000000h
930h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_11)	44000300h
934h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_11)	00000061h
938h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_11)	00000000h
93Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_11)	00000000h
940h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_12)	44000300h
944h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_12)	00000062h
948h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_12)	00000000h
94Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_12)	00000000h
950h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_13)	44000300h
954h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_13)	00000063h
958h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_13)	00000000h
95Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_13)	00000000h
960h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_14)	44000300h
964h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_14)	00000064h
968h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_14)	00000000h
96Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_14)	00000000h
970h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_15)	44000300h
974h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_15)	00000065h
978h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_15)	00000000h
97Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_15)	00000000h
980h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_16)	44000300h
984h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_16)	00000066h
988h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_16)	00000000h
98Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_16)	00000000h
990h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_17)	44000300h
994h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_17)	00000067h
998h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_17)	00000000h
99Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_17)	00000000h
9A0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_18)	44000300h
9A4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_18)	00000068h
9A8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_18)	00000000h
9ACh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_18)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
9E0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_22)	44000300h
9E4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_22)	0000006Ch
9E8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_22)	00000000h
9ECh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_22)	00000000h
9F0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_23)	44000300h
9F4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_23)	0000006Dh
9F8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_23)	00000000h
9FCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_23)	00000000h
A10h	4	Pad Configuration DW0 (PAD_CFG_DW0_L_BKLTEN)	40000700h
A14h	4	Pad Configuration DW1 (PAD_CFG_DW1_L_BKLTEN)	00000000h
A18h	4	Pad Configuration DW2 (PAD_CFG_DW2_L_BKLTEN)	00000000h
A1Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_L_BKLTEN)	00000000h
A20h	4	Pad Configuration DW0 (PAD_CFG_DW0_L_BKLTCTL)	40000700h
A24h	4	Pad Configuration DW1 (PAD_CFG_DW1_L_BKLTCTL)	00000000h
A28h	4	Pad Configuration DW2 (PAD_CFG_DW2_L_BKLTCTL)	00000000h
A2Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_L_BKLTCTL)	00000000h
A30h	4	Pad Configuration DW0 (PAD_CFG_DW0_L_VDDEN)	40000700h
A34h	4	Pad Configuration DW1 (PAD_CFG_DW1_L_VDDEN)	00000000h
A38h	4	Pad Configuration DW2 (PAD_CFG_DW2_L_VDDEN)	00000000h
A3Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_L_VDDEN)	00000000h
A40h	4	Pad Configuration DW0 (PAD_CFG_DW0_SYS_PWROK)	40000700h
A44h	4	Pad Configuration DW1 (PAD_CFG_DW1_SYS_PWROK)	00000000h
A48h	4	Pad Configuration DW2 (PAD_CFG_DW2_SYS_PWROK)	00000000h
A4Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_SYS_PWROK)	00000000h
A50h	4	Pad Configuration DW0 (PAD_CFG_DW0_SYS_RESETB)	40000700h
A54h	4	Pad Configuration DW1 (PAD_CFG_DW1_SYS_RESETB)	00000000h
A58h	4	Pad Configuration DW2 (PAD_CFG_DW2_SYS_RESETB)	00000000h
A5Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_SYS_RESETB)	00000000h
A60h	4	Pad Configuration DW0 (PAD_CFG_DW0_MLK_RSTB)	40000700h
A64h	4	Pad Configuration DW1 (PAD_CFG_DW1_MLK_RSTB)	00000000h
A68h	4	Pad Configuration DW2 (PAD_CFG_DW2_MLK_RSTB)	00000000h
A6Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_MLK_RSTB)	00000000h
A70h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_0)	44000300h
A74h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_0)	00000026h
A78h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_0)	00000000h
A7Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_0)	00000000h
A80h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_1)	44000300h
A84h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_1)	00000027h
A88h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_1)	00000000h
A8Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_1)	00000000h
A90h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_2)	44000300h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
A94h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_2)	00000028h
A98h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_2)	00000000h
A9Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_2)	00000000h
AA0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_3)	44000300h
AA4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_3)	00000029h
AA8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_3)	00000000h
AACh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_3)	00000000h
AB0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_4)	44000300h
AB4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_4)	00000030h
AB8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_4)	00000000h
ABCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_4)	00000000h
AC0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_5)	44000300h
AC4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_5)	00000031h
AC8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_5)	00000000h
ACCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_5)	00000000h
AD0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_6)	44000200h
AD4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_6)	00000032h
AD8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_6)	00000000h
ADCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_6)	00000000h
AE0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_7)	44000300h
AE4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_7)	00000033h
AE8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_7)	00000000h
AECh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_7)	00000000h
AF0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_8)	44000300h
AF4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_8)	00000034h
AF8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_8)	00000000h
AFCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_8)	00000000h
B00h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_9)	44000300h
B04h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_9)	00000035h
B08h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_9)	00000000h
B0Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_9)	00000000h
B10h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_10)	44000300h
B14h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_10)	00000036h
B18h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_10)	00000000h
B1Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_10)	00000000h
B20h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_11)	44000300h
B24h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_11)	00000037h
B28h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_11)	00000000h
B2Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_11)	00000000h
B30h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_12)	44000300h
B34h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_12)	00000038h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
B38h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_12)	00000000h
B3Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_12)	00000000h
B40h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_13)	44000300h
B44h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_13)	00000039h
B48h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_13)	00000000h
B4Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_13)	00000000h
B50h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_14)	44000300h
B54h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_14)	0000003Ah
B58h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_14)	00000000h
B5Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_14)	00000000h
B60h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_15)	44000B00h
B64h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_15)	0000003Bh
B68h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_15)	00000000h
B6Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_15)	00000000h
B70h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_16)	44000B00h
B74h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_16)	0000003Ch
B78h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_16)	00000000h
B7Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_16)	00000000h
B80h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_17)	44000300h
B84h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_17)	0000003Dh
B88h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_17)	00000000h
B8Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_17)	00000000h
B90h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_18)	44001700h
B94h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_18)	00003C3Eh
B98h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_18)	00000100h
B9Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_18)	00000000h
BA0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_19)	44001600h
BA4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_19)	00003C3Fh
BA8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_19)	00000100h
BACh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_19)	00000000h
BB0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_20)	44001700h
BB4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_20)	00003C40h
BB8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_20)	00000100h
BBCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_20)	00000000h
BC0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_21)	44001600h
BC4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_21)	00003C41h
BC8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_21)	00000100h
BCCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_21)	00000000h
BD0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_22)	44000B00h
BD4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_22)	00001042h
BD8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_22)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
BDCh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_22)	00000000h
BE0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_23)	44000200h
BE4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_23)	00000043h
BE8h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_23)	00000000h
BECh	4	Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_23)	00000000h
C00h	4	Pad Configuration DW0 (PAD_CFG_DW0_JTAG_TDO)	40000700h
C04h	4	Pad Configuration DW1 (PAD_CFG_DW1_JTAG_TDO)	00003C00h
C08h	4	Pad Configuration DW2 (PAD_CFG_DW2_JTAG_TDO)	00000000h
C0Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_JTAG_TDO)	00000000h
C10h	4	Pad Configuration DW0 (PAD_CFG_DW0_JTAGX)	40000700h
C14h	4	Pad Configuration DW1 (PAD_CFG_DW1_JTAGX)	00003C00h
C18h	4	Pad Configuration DW2 (PAD_CFG_DW2_JTAGX)	00000000h
C1Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_JTAGX)	00000000h
C40h	4	Pad Configuration DW0 (PAD_CFG_DW0_CPU_TRSTB)	40000700h
C44h	4	Pad Configuration DW1 (PAD_CFG_DW1_CPU_TRSTB)	00003C00h
C48h	4	Pad Configuration DW2 (PAD_CFG_DW2_CPU_TRSTB)	00000000h
C4Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_CPU_TRSTB)	00000000h
C50h	4	Pad Configuration DW0 (PAD_CFG_DW0_JTAG_TDI)	40000700h
C54h	4	Pad Configuration DW1 (PAD_CFG_DW1_JTAG_TDI)	00003C00h
C58h	4	Pad Configuration DW2 (PAD_CFG_DW2_JTAG_TDI)	00000000h
C5Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_JTAG_TDI)	00000000h
C60h	4	Pad Configuration DW0 (PAD_CFG_DW0_JTAG_TMS)	40000700h
C64h	4	Pad Configuration DW1 (PAD_CFG_DW1_JTAG_TMS)	00003C00h
C68h	4	Pad Configuration DW2 (PAD_CFG_DW2_JTAG_TMS)	00000000h
C6Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_JTAG_TMS)	00000000h
C70h	4	Pad Configuration DW0 (PAD_CFG_DW0_JTAG_TCK)	40000700h
C74h	4	Pad Configuration DW1 (PAD_CFG_DW1_JTAG_TCK)	00003C00h
C78h	4	Pad Configuration DW2 (PAD_CFG_DW2_JTAG_TCK)	00000000h
C7Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_JTAG_TCK)	00000000h
C80h	4	Pad Configuration DW0 (PAD_CFG_DW0_DBG_PMODE)	40000700h
C84h	4	Pad Configuration DW1 (PAD_CFG_DW1_DBG_PMODE)	00003C00h
C88h	4	Pad Configuration DW2 (PAD_CFG_DW2_DBG_PMODE)	00000800h
C8Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_DBG_PMODE)	00000000h

33.4.1 Family Base Address (FAMBAR) — Offset 8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 8h	00000300h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0300h RO	**Family Base Address (FAMBAR):** This field provides the starting byte-align address of Family0 register sets within a Community. It is meant for software to discover from where the very first Family register (i.e. Family0 register) starts to compute the next Families address offsets.

33.4.2 Pad Base Address (PADBAR) — Offset Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + Ch	00000700h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0700h RO	**Pad Base Address (PADBAR):** This field provides the starting byte-align address of Pad0 register sets within a Community. It is meant for software to discover from where the very first Pad register (i.e. Pad0 register) starts to compute the next Pad address offsets.

33.4.3 Miscellaneous Configuration (MISCCFG) — Offset 10h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 10h	36043200h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	36h RW	**GPIO Driver Mode Interrupt Select (GPDMINTSEL):** IRQ globally for all pads (GPI_IS with corresponding GPI_IE enable). 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255
23:20	0h RO	**Reserved**
19:16	4h RW	**GPIO Group to GPE_DW2 assignment encoding (GPE0_DW2):** This register assigns a specific GPIO Group to the ACPI GPE0[95:64]. The setting is SoC specific.
15:12	3h RW	**GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1):** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The setting is SoC specific.
11:8	2h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0):** This register assigns a specific GPIO Group to the ACPI GPE0[31:0]. The setting is SoC specific.
7	0h RW	**GPIO IOSF Sideband VNNREQ Enable (GPVNNREQEN):** Specify whether the GPIO Community should take part in IOSFSB VNNREQ/ACK handshake 0 = Disable participation in IOSF SB VNNREQ and VNNACK handshake 1 = Enable participation in IOSF SB VNNREQ and VNNACK handshake When this bit set to 1, GPIO controller will de-assert the VNNREQ when there is no outstanding IOSF SB upstream cycle from GPIO controller. When this bit set to 1 and MISCSECCFG.SBTRIGDIS is 0, GPIO controller will assert the VNNREQ to request for the following list of IOSF-SB Message initiation. Event list: IRQ NMI SMI SSMI VNNREQ shall de-assert when MISCSECCFG.SBTRIGDIS is set to 1. As VNNAON IP, GPIO controller will assert the VNNREQ when in reset. The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pwrgate_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this power gating, this register always default to 1.
6	0h RW	**GPIO PGCB Clock Dynamic Partition Clock Gating Enable (GPPGCBDPCGEN):** Specify whether the GPIO Community PGCB clock should take part in partition clock gating 0 = Disable participation in PGCB clock dynamic partition clock gating 1 = Enable participation in PGCB clock dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**GPIO IOSF Sideband Dynamic Partition Clock Gating Enable (GPSIDEDPCGEN):** Specify whether the GPIO Community IOSF sideband clock should take part in partition clock gating 0 = Disable participation in IOSF sideband clock dynamic partition clock gating 1 = Enable participation in IOSF sideband clock dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
4	0h RW	**GPIO RCOMP clock Dynamic Local Clock Gating (GPRCOMPCDLCGEN):** Specify whether the GPIO Community should perform local clock gating on RCOMP clock 0 = Disable dynamic RCOMP clock local clock gating 1 = Enable dynamic RCOMP clock local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
3	0h RW	**GPIO RTC clock Dynamic Local Clock Gating (GPRTCDLCGEN):** Specify whether the GPIO Community should perform local clock gating on RTC clock 0 = Disable dynamic RTC clock local clock gating 1 = Enable dynamic RTC clock local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
2	0h RW	**GSX Static Local Clock Gating (GSXSLCGEN):** Specify whether the GSX controller should be statically clock gated for power saving if it is not enabled (even though the capability is available). 0 = Disable static local clock gating 1 = Enable static local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
1	0h RW	**GPIO Dynamic Partition Clock Gating Enable (GPDPCGEN):** Specify whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
0	0h RW	**GPIO Dynamic Local Clock Gating Enable (GPDLCGEN):** Specify whether the GPIO Community should perform local clock gating 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0

33.4.4 Pad Ownership (PAD_OWN_GPP_C_0) — Offset 20h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 20h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_7):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into successful Completion status. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_6):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_5):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_4):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_C_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.4.5 Pad Ownership (PAD_OWN_GPP_C_1) — Offset 24h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 24h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

33.4.6 Pad Ownership (PAD_OWN_GPP_C_2) — Offset 28h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 28h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

33.4.7 Pad Ownership (PAD_OWN_GPP_F_0) — Offset 2Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 2Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_7):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_6):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_5):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_4):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.4.8 Pad Ownership (PAD_OWN_GPP_F_1) — Offset 30h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 30h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_15):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_14):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_13):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_12):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_11):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

Bit Range	Default & Access	Field Name (ID): Description
11:10	0h RO	**Reserved**
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_10):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:0	0h RO	**Reserved**

33.4.9 Pad Ownership (PAD_OWN_GPP_F_2) — Offset 34h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 34h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_23):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_22):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
23:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_18):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_17):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_16):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.4.10 Pad Ownership (PAD_OWN_GPP_F_3) — Offset 38h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 38h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**Reserved**

33.4.11 Pad Ownership (PAD_OWN_HVCMOS_0) — Offset 3Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 3Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:20	0h RO	**Pad Ownership (PAD_OWN_MLK_RSTB):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RO	**Pad Ownership (PAD_OWN_SYS_RESETB):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RO	**Pad Ownership (PAD_OWN_SYS_PWROK):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RO	**Pad Ownership (PAD_OWN_L_VDDEN):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RO	**Pad Ownership (PAD_OWN_L_BKLTCTL):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RO	**Pad Ownership (PAD_OWN_L_BKLTEN):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.4.12 Pad Ownership (PAD_OWN_GPP_E_0) — Offset 40h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 40h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_7):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_6):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_5):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_4):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.4.13 Pad Ownership (PAD_OWN_GPP_E_1) — Offset 44h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 44h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_15):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_14):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_13):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_12):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_11):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_10):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_9):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_8):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.4.14 Pad Ownership (PAD_OWN_GPP_E_2) — Offset 48h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 48h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_23):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_22):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_21):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_20):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_19):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_18):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_17):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_E_16):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.4.15 Pad Ownership (PAD_OWN_GPP_E_3) — Offset 4Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 4Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**Reserved**

33.4.16 Pad Ownership (PAD_OWN_JTAG_0) — Offset 50h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 50h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RO	**Pad Ownership (PAD_OWN_JTAG_TCK):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RO	**Pad Ownership (PAD_OWN_JTAG_TMS):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RO	**Pad Ownership (PAD_OWN_JTAG_TDI):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RO	**Pad Ownership (PAD_OWN_CPU_TRSTB):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
15:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RO	**Pad Ownership (PAD_OWN_JTAGX):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RO	**Pad Ownership (PAD_OWN_JTAG_TDO):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.4.17 Pad Ownership (PAD_OWN_JTAG_1) — Offset 54h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 54h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**Pad Ownership (PAD_OWN_DBG_PMODE):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.4.18 Pad Configuration Lock (PADCFGLOCK_GPP_C_0) — Offset 80h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 80h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_7):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_6):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_5):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_4):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

33.4.19 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_C_0) — Offset 84h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 84h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_7):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_6):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_5):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_4):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

33.4.20 Pad Configuration Lock (PADCFGLOCK_GPP_F_0) — Offset 88h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 88h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_23):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
22	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_22):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
21:19	0h RW	**Reserved**
18	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_18):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_17):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
16	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_16):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_15):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
14	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_14):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_13):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
12	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_12):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_11):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_10):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
9:8	0h RW	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_7):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_6):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_5):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_4):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

33.4.21 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_F_0) — Offset 8Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 8Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_23):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
22	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_22):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
21:19	0h RW	**Reserved**
18	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_18):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_17):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
16	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_16):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_15):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
14	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_14):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_13):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
12	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_12):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_11):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_10):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
9:8	0h RW	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_7):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_6):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_5):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_4):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

33.4.22 Pad Configuration Lock (PADCFGLOCK_HVCMOS_0) — Offset 90h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 90h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RSV	**Pad Config Lock (PADCFGLOCK_MLK_RSTB):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
4	0h RSV	**Pad Config Lock (PADCFGLOCK_SYS_RESETB):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**Pad Config Lock (PADCFGLOCK_SYS_PWROK):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**Pad Config Lock (PADCFGLOCK_L_VDDEN):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
1	0h RSV	**Pad Config Lock (PADCFGLOCK_L_BKLTCTL):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RSV	**Pad Config Lock (PADCFGLOCK_L_BKLTEN):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

33.4.23 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_HVCMOS_0) — Offset 94h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 94h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_MLK_RSTB):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
4	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_SYS_RESETB):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_SYS_PWROK):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_L_VDDEN):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
1	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_L_BKLTCTL):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_L_BKLTEN):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

33.4.24 Pad Configuration Lock (PADCFGLOCK_GPP_E_0) — Offset 98h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 98h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_23):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
22	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_22):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
21	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_21):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_20):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
19	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_19):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_18):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
17	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_17):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_16):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
15	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_15):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_14):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
13	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_13):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_12):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_11):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_10):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_9):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_8):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_7):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_6):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_5):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_4):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_E_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

33.4.25 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_E_0) — Offset 9Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 9Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_23):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
22	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_22):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
21	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_21):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_20):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
19	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_19):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_18):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
17	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_17):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_16):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
15	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_15):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_14):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
13	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_13):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_12):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_11):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_10):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_9):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_8):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_7):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_6):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_5):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_4):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_E_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

33.4.26 Pad Configuration Lock (PADCFGLOCK_JTAG_0) — Offset A0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RSV	**Pad Config Lock (PADCFGLOCK_DBG_PMODE):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
7	0h RSV	**Pad Config Lock (PADCFGLOCK_JTAG_TCK):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RSV	**Pad Config Lock (PADCFGLOCK_JTAG_TMS):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
5	0h RSV	**Pad Config Lock (PADCFGLOCK_JTAG_TDI):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RSV	**Pad Config Lock (PADCFGLOCK_CPU_TRSTB):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
3	0h RSV	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**Reserved**
1	0h RSV	**Pad Config Lock (PADCFGLOCK_JTAGX):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
0	0h RSV	**Pad Config Lock (PADCFGLOCK_JTAG_TDO):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

33.4.27 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_JTAG_0) — Offset A4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_DBG_PMODE):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
7	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_JTAG_TCK):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_JTAG_TMS):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
5	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_JTAG_TDI):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_CPU_TRSTB):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
3	0h RSV	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**Reserved**
1	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_JTAGX):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
0	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_JTAG_TDO):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

33.4.28 Host Software Pad Ownership (HOSTSW_OWN_GPP_C_0) — Offset B0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**HOSTSW_OWN_GPPC_C_7:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
6	0h RW	**HOSTSW_OWN_GPPC_C_6:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**HOSTSW_OWN_GPPC_C_5:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
4	0h RW	**HOSTSW_OWN_GPPC_C_4:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
3	0h RW	**HOSTSW_OWN_GPPC_C_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HOSTSW_OWN_GPPC_C_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RW	**HOSTSW_OWN_GPPC_C_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RW	**HOSTSW_OWN_GPPC_C_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

33.4.29 Host Software Pad Ownership (HOSTSW_OWN_GPP_F_0) — Offset B4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**HOSTSW_OWN_GPPC_F_23:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
22	0h RW	**HOSTSW_OWN_GPPC_F_22:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
21:19	0h RW	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**HOSTSW_OWN_GPPC_F_18:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
17	0h RW	**HOSTSW_OWN_GPPC_F_17:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
16	0h RW	**HOSTSW_OWN_GPPC_F_16:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**HOSTSW_OWN_GPPC_F_15:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
14	0h RW	**HOSTSW_OWN_GPPC_F_14:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
13	0h RW	**HOSTSW_OWN_GPPC_F_13:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**HOSTSW_OWN_GPPC_F_12:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
11	0h RW	**HOSTSW_OWN_GPPC_F_11:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
10	0h RW	**HOSTSW_OWN_GPPC_F_10:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
9:8	0h RW	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**HOSTSW_OWN_GPPC_F_7:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
6	0h RW	**HOSTSW_OWN_GPPC_F_6:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
5	0h RW	**HOSTSW_OWN_GPPC_F_5:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**HOSTSW_OWN_GPPC_F_4:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
3	0h RW	**HOSTSW_OWN_GPPC_F_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HOSTSW_OWN_GPPC_F_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RW	**HOSTSW_OWN_GPPC_F_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RW	**HOSTSW_OWN_GPPC_F_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

33.4.30 Host Software Pad Ownership (HOSTSW_OWN_HVCMOS_0) — Offset B8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RSV	**HOSTSW_OWN_MLK_RSTB:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
4	0h RSV	**HOSTSW_OWN_SYS_RESETB:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**HOSTSW_OWN_SYS_PWROK:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**HOSTSW_OWN_L_VDDEN:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RSV	**HOSTSW_OWN_L_BKLTCTL:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RSV	**HOSTSW_OWN_L_BKLTEN:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

33.4.31 Host Software Pad Ownership (HOSTSW_OWN_GPP_E_0) — Offset BCh

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + BCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**HOSTSW_OWN_GPPC_E_23:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
22	0h RW	**HOSTSW_OWN_GPPC_E_22:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**HOSTSW_OWN_GPPC_E_21:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
20	0h RW	**HOSTSW_OWN_GPPC_E_20:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
19	0h RW	**HOSTSW_OWN_GPPC_E_19:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**HOSTSW_OWN_GPPC_E_18:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
17	0h RW	**HOSTSW_OWN_GPPC_E_17:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
16	0h RW	**HOSTSW_OWN_GPPC_E_16:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**HOSTSW_OWN_GPPC_E_15:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
14	0h RW	**HOSTSW_OWN_GPPC_E_14:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
13	0h RW	**HOSTSW_OWN_GPPC_E_13:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**HOSTSW_OWN_GPPC_E_12:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
11	0h RW	**HOSTSW_OWN_GPPC_E_11:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
10	0h RW	**HOSTSW_OWN_GPPC_E_10:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**HOSTSW_OWN_GPPC_E_9:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
8	0h RW	**HOSTSW_OWN_GPPC_E_8:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
7	0h RW	**HOSTSW_OWN_GPPC_E_7:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**HOSTSW_OWN_GPPC_E_6:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
5	0h RW	**HOSTSW_OWN_GPPC_E_5:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
4	0h RW	**HOSTSW_OWN_GPPC_E_4:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**HOSTSW_OWN_GPPC_E_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HOSTSW_OWN_GPPC_E_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RW	**HOSTSW_OWN_GPPC_E_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RW	**HOSTSW_OWN_GPPC_E_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

33.4.32 Host Software Pad Ownership (HOSTSW_OWN_JTAG_0) — Offset C0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RSV	**HOSTSW_OWN_DBG_PMODE:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
7	0h RSV	**HOSTSW_OWN_JTAG_TCK:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RSV	**HOSTSW_OWN_JTAG_TMS:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
5	0h RSV	**HOSTSW_OWN_JTAG_TDI:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
4	0h RSV	**HOSTSW_OWN_CPU_TRSTB:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
3	0h RSV	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**Reserved**
1	0h RSV	**HOSTSW_OWN_JTAGX:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RSV	**HOSTSW_OWN_JTAG_TDO:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

33.4.33 GPI Interrupt Status (GPI_IS_GPP_C_0) — Offset 100h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 100h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_7):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_6):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_5):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_4):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.4.34 GPI Interrupt Status (GPI_IS_GPP_F_0) — Offset 104h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 104h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_23):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
22	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_22):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
21:19	0h RW/1C	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_18):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
17	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_17):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
16	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_16):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_15):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_14):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_13):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_12):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
11	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_11):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_10):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9:8	0h RW/1C	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_7):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_6):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_5):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_4):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.4.35 GPI Interrupt Status (GPI_IS_HVCMOS_0) — Offset 108h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 108h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RSV	**GPI Interrupt Status (GPI_INT_STS_MLK_RSTB):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RSV	**GPI Interrupt Status (GPI_INT_STS_SYS_RESETB):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI Interrupt Status (GPI_INT_STS_SYS_PWROK):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI Interrupt Status (GPI_INT_STS_L_VDDEN):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RSV	**GPI Interrupt Status (GPI_INT_STS_L_BKLTCTL):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RSV	**GPI Interrupt Status (GPI_INT_STS_L_BKLTEN):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.4.36 GPI Interrupt Status (GPI_IS_GPP_E_0) — Offset 10Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 10Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**GPI Interrupt Status (GPI_INT_STS_GPPE_CLK_LOOPBK):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
23	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_23):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
22	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_22):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
21	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_21):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
20	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_20):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_19):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
18	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_18):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
17	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_17):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_16):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
15	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_15):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_14):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_13):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_12):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
11	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_11):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_10):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_9):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
8	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_8):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_7):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_6):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_5):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_4):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_E_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.4.37 GPI Interrupt Status (GPI_IS_JTAG_0) — Offset 110h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 110h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RSV	**GPI Interrupt Status (GPI_INT_STS_DBG_PMODE):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RSV	**GPI Interrupt Status (GPI_INT_STS_JTAG_TCK):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RSV	**GPI Interrupt Status (GPI_INT_STS_JTAG_TMS):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RSV	**GPI Interrupt Status (GPI_INT_STS_JTAG_TDI):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RSV	**GPI Interrupt Status (GPI_INT_STS_CPU_TRSTB):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RSV	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**Reserved**
1	0h RSV	**GPI Interrupt Status (GPI_INT_STS_JTAGX):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RSV	**GPI Interrupt Status (GPI_INT_STS_JTAG_TDO):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.4.38 GPI Interrupt Enable (GPI_IE_GPP_C_0) — Offset 120h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 120h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_7):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_6):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_5):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_4):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.4.39 GPI Interrupt Enable (GPI_IE_GPP_F_0) — Offset 124h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 124h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_23):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
22	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_22):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
21:19	0h RW	**Reserved**
18	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_18):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_17):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
16	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_16):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
15	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_15):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_14):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_13):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
12	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_12):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_11):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_10):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9:8	0h RW	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_7):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_6):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_5):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_4):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.4.40 GPI Interrupt Enable (GPI_IE_HVCMOS_0) — Offset 128h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 128h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_MLK_RSTB):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_SYS_RESETB):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_SYS_PWROK):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_L_VDDEN):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_L_BKLTCTL):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_L_BKLTEN):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.4.41 GPI Interrupt Enable (GPI_IE_GPP_E_0) — Offset 12Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 12Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_23):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
22	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_22):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
21	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_21):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_20):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
19	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_19):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
18	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_18):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
17	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_17):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_16):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
15	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_15):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
14	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_14):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
13	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_13):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_12):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_11):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_10):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_9):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_8):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_7):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_6):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_5):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_4):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_E_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.4.42 GPI Interrupt Enable (GPI_IE_JTAG_0) — Offset 130h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 130h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_DBG_PMODE):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
7	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_JTAG_TCK):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_JTAG_TMS):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_JTAG_TDI):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_CPU_TRSTB):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RSV	**Reserved**
2	0h RSV	**Reserved**
1	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_JTAGX):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_JTAG_TDO):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.4.43 GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_0) — Offset 140h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 140h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_7):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_6):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_5):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_4):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.4.44 GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_0) — Offset 144h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 144h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_23):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
22	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_22):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
21:19	0h RW/1C	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_18):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
17	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_17):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
16	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_16):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_15):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_14):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
13	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_13):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_12):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_11):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_10):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
9:8	0h RW/1C	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_7):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_6):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_5):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_4):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.4.45 GPI General Purpose Events Status (GPI_GPE_STS_HVCMOS_0) — Offset 148h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 148h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_MLK_RSTB):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_SYS_RESETB):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_SYS_PWROK):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_L_VDDEN):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_L_BKLTCTL):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_L_BKLTEN):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.4.46 GPI General Purpose Events Status (GPI_GPE_STS_GPP_E_0) — Offset 14Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 14Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_23):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
22	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_22):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_21):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
20	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_20):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
19	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_19):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_18):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
17	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_17):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
16	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_16):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_15):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_14):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
13	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_13):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_12):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_11):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_10):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_9):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_8):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_7):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_6):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_5):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_4):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_E_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.4.47 GPI General Purpose Events Status (GPI_GPE_STS_JTAG_0) — Offset 150h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 150h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_DBG_PMODE):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_JTAG_TCK):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_JTAG_TMS):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_JTAG_TDI):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_CPU_TRSTB):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RSV	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**Reserved**
1	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_JTAGX):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_JTAG_TDO):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.4.48 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_0) — Offset 160h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 160h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_7):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_6):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_5):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_4):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.4.49 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_0) — Offset 164h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 164h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_23):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
22	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_22):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
21:19	0h RW	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_18):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
17	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_17):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
16	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_16):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
15	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_15):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_14):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
13	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_13):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
12	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_12):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_11):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_10):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
9:8	0h RW	**Reserved**
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_7):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_6):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_5):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_4):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.4.50 GPI General Purpose Events Enable (GPI_GPE_EN_HVCMOS_0) — Offset 168h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 168h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_MLK_RSTB):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_SYS_RESETB):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_SYS_PWROK):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_L_VDDEN):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_L_BKLTCTL):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_L_BKLTEN):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.4.51 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_E_0) — Offset 16Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 16Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPE_CLK_LOOPBK):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
23	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_23):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
22	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_22):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_21):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
20	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_20):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
19	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_19):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
18	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_18):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_17):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
16	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_16):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
15	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_15):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
14	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_14):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_13):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
12	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_12):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_11):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_10):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_9):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_8):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_7):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_6):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_5):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_4):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_E_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.4.52 GPI General Purpose Events Enable (GPI_GPE_EN_JTAG_0) — Offset 170h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 170h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_DBG_PMODE):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
7	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_JTAG_TCK):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_JTAG_TMS):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_JTAG_TDI):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_CPU_TRSTB):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RSV	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**Reserved**
1	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_JTAGX):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_JTAG_TDO):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.4.53 SMI Status (GPI_SMI_STS_GPP_C_0) — Offset 180h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 180h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_7):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
6	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_6):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_5):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
4	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_4):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_C_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

33.4.54 SMI Status (GPI_SMI_STS_GPP_F_0) — Offset 184h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 184h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_F_23):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
22	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_F_22):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
21:19	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_F_18):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
17	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_F_17):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_F_16):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
15	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_F_15):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_F_14):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
13	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_F_13):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_F_12):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
11	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_F_11):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_F_10):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
9:8	0h RO	**Reserved**
7	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_F_7):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_F_6):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
5	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_F_5):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_F_4):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
3	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_F_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_F_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_F_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_F_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

33.4.55 SMI Status (GPI_SMI_STS_HVCMOS_0) — Offset 188h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 188h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RSV	**GPI SMI Status (GPI_SMI_STS_MLK_RSTB):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
4	0h RSV	**GPI SMI Status (GPI_SMI_STS_SYS_RESETB):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI SMI Status (GPI_SMI_STS_SYS_PWROK):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Status (GPI_SMI_STS_L_VDDEN):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RSV	**GPI SMI Status (GPI_SMI_STS_L_BKLTCTL):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RSV	**GPI SMI Status (GPI_SMI_STS_L_BKLTEN):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

33.4.56 SMI Status (GPI_SMI_STS_GPP_E_0) — Offset 18Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 18Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_E_23):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
22	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_E_22):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_E_21):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
20	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_E_20):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_E_19):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
18	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_E_18):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_E_17):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
16	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_16):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_15):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
14	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_14):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_13):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
12	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_E_12):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_E_11):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
10	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_E_10):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**GPI SMI Status (GPI_SMI_STS_GPPC_E_9):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
8	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_8):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_7):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
6	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_6):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_5):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
4	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_4):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

33.4.57 SMI Status (GPI_SMI_STS_JTAG_0) — Offset 190h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 190h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RSV	**GPI SMI Status (GPI_SMI_STS_DBG_PMODE):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
7	0h RSV	**GPI SMI Status (GPI_SMI_STS_JTAG_TCK):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RSV	**GPI SMI Status (GPI_SMI_STS_JTAG_TMS):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
5	0h RSV	**GPI SMI Status (GPI_SMI_STS_JTAG_TDI):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RSV	**GPI SMI Status (GPI_SMI_STS_CPU_TRSTB):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
3	0h RSV	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**Reserved**
1	0h RSV	**GPI SMI Status (GPI_SMI_STS_JTAGX):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
0	0h RSV	**GPI SMI Status (GPI_SMI_STS_JTAG_TDO):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

33.4.58 SMI Enable (GPI_SMI_EN_GPP_C_0) — Offset 1A0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 1A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_7):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
6	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_6):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_5):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
4	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_4):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
3	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

33.4.59 SMI Enable (GPI_SMI_EN_GPP_F_0) — Offset 1A4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 1A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_23):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
22	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_22):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
21:19	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_18):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
17	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_17):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
16	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_16):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_15):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
14	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_14):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
13	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_13):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_12):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
11	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_11):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
10	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_10):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
9:8	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_7):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
6	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_6):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
5	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_5):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_4):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
3	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_F_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

33.4.60 SMI Enable (GPI_SMI_EN_HVCMOS_0) — Offset 1A8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 1A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RSV	**GPI SMI Enable (GPI_SMI_EN_MLK_RSTB):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
4	0h RSV	**GPI SMI Enable (GPI_SMI_EN_SYS_RESETB):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI SMI Enable (GPI_SMI_EN_SYS_PWROK):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Enable (GPI_SMI_EN_L_VDDEN):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RSV	**GPI SMI Enable (GPI_SMI_EN_L_BKLTCTL):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RSV	**GPI SMI Enable (GPI_SMI_EN_L_BKLTEN):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

33.4.61 SMI Enable (GPI_SMI_EN_GPP_E_0) — Offset 1ACh

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 1ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPE_CLK_LOOPBK):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
23	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_23):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
22	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_22):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
21	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_21):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
20	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_20):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_19):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
18	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_18):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
17	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_17):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_16):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
15	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_15):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
14	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_14):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_13):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
12	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_12):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
11	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_11):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_10):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
9	0h RO	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_9):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
8	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_8):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_7):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
6	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_6):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
5	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_5):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_4):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
3	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

33.4.62 SMI Enable (GPI_SMI_EN_JTAG_0) — Offset 1B0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 1B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RSV	**GPI SMI Enable (GPI_SMI_EN_DBG_PMODE):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
7	0h RSV	**GPI SMI Enable (GPI_SMI_EN_JTAG_TCK):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
6	0h RSV	**GPI SMI Enable (GPI_SMI_EN_JTAG_TMS):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
5	0h RSV	**GPI SMI Enable (GPI_SMI_EN_JTAG_TDI):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
4	0h RSV	**GPI SMI Enable (GPI_SMI_EN_CPU_TRSTB):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
3	0h RSV	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**Reserved**
1	0h RSV	**GPI SMI Enable (GPI_SMI_EN_JTAGX):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RSV	**GPI SMI Enable (GPI_SMI_EN_JTAG_TDO):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

33.4.63 NMI Status (GPI_NMI_STS_GPP_C_0) — Offset 1C0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 1C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_7):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_6):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_5):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_4):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_C_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.4.64 NMI Status (GPI_NMI_STS_GPP_F_0) — Offset 1C4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 1C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_F_23):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
22	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_F_22):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
21:19	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_F_18):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
17	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_F_17):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_F_16):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_F_15):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_F_14):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_F_13):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_F_12):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_F_11):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_F_10):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
9:8	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_F_7):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_F_6):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_F_5):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_F_4):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_F_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_F_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_F_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_F_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.4.65 NMI Status (GPI_NMI_STS_HVCMOS_0) — Offset 1C8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 1C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RSV	**GPI NMI Status (GPI_NMI_STS_MLK_RSTB):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Status (GPI_NMI_STS_SYS_RESETB):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI NMI Status (GPI_NMI_STS_SYS_PWROK):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Status (GPI_NMI_STS_L_VDDEN):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Status (GPI_NMI_STS_L_BKLTCTL):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Status (GPI_NMI_STS_L_BKLTEN):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.4.66 NMI Status (GPI_NMI_STS_GPP_E_0) — Offset 1CCh

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 1CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_E_23):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
22	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_E_22):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_E_21):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
20	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_E_20):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
19	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_E_19):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_E_18):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
17	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_E_17):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_16):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_15):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_14):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_13):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_E_12):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_E_11):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_E_10):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**GPI NMI Status (GPI_NMI_STS_GPPC_E_9):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
8	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_8):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_7):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_6):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_5):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_4):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.4.67 NMI Status (GPI_NMI_STS_JTAG_0) — Offset 1D0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 1D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RSV	**GPI NMI Status (GPI_NMI_STS_DBG_PMODE):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RSV	**GPI NMI Status (GPI_NMI_STS_JTAG_TCK):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RSV	**GPI NMI Status (GPI_NMI_STS_JTAG_TMS):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RSV	**GPI NMI Status (GPI_NMI_STS_JTAG_TDI):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Status (GPI_NMI_STS_CPU_TRSTB):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**Reserved**
1	0h RSV	**GPI NMI Status (GPI_NMI_STS_JTAGX):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Status (GPI_NMI_STS_JTAG_TDO):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.4.68 NMI Enable (GPI_NMI_EN_GPP_C_0) — Offset 1E0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 1E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_7):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_6):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_5):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_4):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.4.69 NMI Enable (GPI_NMI_EN_GPP_F_0) — Offset 1E4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 1E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_23):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
22	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_22):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
19:21	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_18):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
17	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_17):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_16):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_15):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_14):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_13):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_12):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_11):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_10):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
9:8	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_7):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_6):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_5):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_4):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_F_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.4.70 NMI Enable (GPI_NMI_EN_HVCMOS_0) — Offset 1E8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 1E8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RSV	**GPI NMI Enable (GPI_NMI_EN_MLK_RSTB):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Enable (GPI_NMI_EN_SYS_RESETB):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**GPI NMI Enable (GPI_NMI_EN_SYS_PWROK):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Enable (GPI_NMI_EN_L_VDDEN):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Enable (GPI_NMI_EN_L_BKLTCTL):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Enable (GPI_NMI_EN_L_BKLTEN):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.4.71 NMI Enable (GPI_NMI_EN_GPP_E_0) — Offset 1ECh

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 1ECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_23):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
22	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_22):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_21):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
20	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_20):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
19	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_19):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_18):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
17	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_17):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
16	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_16):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_15):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
14	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_14):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
13	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_13):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_12):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
11	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_11):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
10	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_10):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_9):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
8	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_8):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_7):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_6):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_5):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_4):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.4.72 NMI Enable (GPI_NMI_EN_JTAG_0) — Offset 1F0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 1F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RSV	**GPI NMI Enable (GPI_NMI_EN_DBG_PMODE):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
7	0h RSV	**GPI NMI Enable (GPI_NMI_EN_JTAG_TCK):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RSV	**GPI NMI Enable (GPI_NMI_EN_JTAG_TMS):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI NMI Enable (GPI_NMI_EN_JTAG_TDI):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Enable (GPI_NMI_EN_CPU_TRSTB):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**Reserved**
1	0h RSV	**GPI NMI Enable (GPI_NMI_EN_JTAGX):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Enable (GPI_NMI_EN_JTAG_TDO):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.4.73 GSX Controller Capabilities (GSX_CAP) — Offset 21Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 21Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RO	**Number of Channels (NC):** This is a zero-based number. Each channel is capable of input and output GPIO.

33.4.74 GSX Channel-0 Capabilities DW0 (GSX_C0CAP_DW0) — Offset 220h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 220h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:10	0h RO	**Power Well (PW):** Indicates the power well. This field is project defined, and is as below in PCH. '00' means Core power well '01' reserved '1x' reserved
9:5	00h RW/O	**Number of Output Expanders (NOUT):** BIOS programs this field to indicate number of output expander components which corresponds to multiple of CxGPO in byte granularity. This field is 1-based ('00001' means 1 output expander which produces 8 bits of CxGPO). If this channel does not have output, this register shall be written with value of '00000'.
4:0	00h RW/O	**Number of Input Expanders (NIN):** BIOS programs this field to indicate number of input expander components which corresponds to multiple of CxGPO. This field is 1-based ('00001' means 1 input expander which produces 8 bits of CxGPI). If this channel does not have input, this register shall be written with value of '00000'. Typically, the combine total value of supported NOUT+NIN <= 8.

33.4.75 GSX Channel-0 Capabilities DW1 (GSX_C0CAP_DW1) — Offset 224h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 224h	00012000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25:12	0012h RO/V	**SCLK Rate(SCLKR) (SCLKR):** Toggle rate of GSXSCLK. SCLKR and SCLKRD are BCD encoded. The SCLKR represent MHz rate as a whole number, and SCLKR_D represent the decimal number. Example: GSXSCLK toggle rate of 16KHz would be represented as SCLKR=000h and SCLKR_D=016h. GSXSCLK typically is 15.625 12MHz or less to support long routing to multiple expanders, i.e. SCLKR=012h015h and SCLKR_D=000h625h. In the case, when ALTSCLK is '1', SCLKR and SCLKR_D shall reflect 3MHz
11:0	000h RO/V	**SCLK Rate Decimal (SCLKR_D):** Refer to SCLKR description.

33.4.76 GSX Channel-0 GP Input Level DW0 (GSX_C0GPILVL_DW0) — Offset 228h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 228h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**GPI Level DW0[31:0] (GPILVL_DW0):** BIOS or software read returns the value of the CxGPI received over the GSX channel. GPILVL_DW0[y] corresponds to CxGPI[y] where y falls within [31:0] range. CGPILVL_DW0[0] contains the first bit being serially shifted in during an atomic input serialization process. Hardware serialization process shifts in each bit of CxGPI value in ascending order from [bit 0] to [((NIN*8)-1)'s MSB bit]. This register is updated by hardware on bit by bit basis. During the input serialization process, when a bit is serially shifted in based on SCLK toggle rate, the corresponding register bit is updated by hardware.

33.4.77 GSX Channel-0 GP Input Level DW1 (GSX_C0GPILVL_DW1) — Offset 22Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 22Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**GPI Level DW1[31:0] (GPILVL_DW1):** Refer to CxGPILVL_DW0 register description. GPILVL_DW1[y] corresponds to CxGPI[y] where y is within [63:32] range.

33.4.78 GSX Channel-0 GP Output Level DW0 (GSX_C0GPOLVL_DW0) — Offset 230h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 230h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GPO Level DW0[31:0] (GPOLVL_DW0):** BIOS or software writes to this field to program the value of each output bit that will be sent in the serialization process. GPOLVL_DW0[y] corresponds to CxGPO[y] where y within CxGPO[31:0] range. GPOLVL_DW0[0] is the last bit in this register to be shifted out serially. Hardware serialization process shifts out each bit of CxGPOLVL_DW1 & CxGPOLVL_DW0 in descending order from [((NOUT*8)-1)'s MSB bit] to [bit 0]. Depending on CxCAP.NOUT, unused byte(s) of CxGPOLVL_DW1 and/or CxGPOLVL_DW0 is not serialized out.

33.4.79 GSX Channel-0 GP Output Level DW1 (GSX_C0GPOLVL_DW1) — Offset 234h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 234h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GPO Level DW1[31:0] (GPOLVL_DW1):** Refer to CxGPOLVL_DW0 register description. GPOLVL_DW1[y] corresponds to CxGPO[y] where y is within CxGPO[63:32] range.

33.4.80 GSX Channel-0 Command (GSX_C0CMD) — Offset 238h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 238h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW/1S/V	**Input and Output Expander Reset Sequence (IOERST):** Software writes '1' to this bit to cause a reset sequence that brings both input and output expander into a default state. Serialization process will be able to begin at default bit position again. Specifically: GSXSRESET# going to output expanders is asserted while GSXSLOAD shall be held in '0' logic state such that any stale pin state previously latched into input expanders is being reloaded. The serialization thereafter can start from default bit position. Hardware automatically clears the bit to zero after the process above has been completed. Software shall have both ST and RUN bit equal to '0' when setting IOERST to '1'.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO/V	**RUN:** This bit reflects the status of the serialization process. A '1' indicates that the serialization process is in progress. When software clears the ST bit, software shall poll on RUN bit to be '0' before software can write '1' to ST bit again.
1	0h RO/V	**BSY:** Software reads this field to determine if the serialization of most recently updated GPOLVL_DW1 and/or GPOLVL_DW0 content has been completely serialized out on the GSX. H/w sets this bit when either GPOLVL_DW1 or GPOLVL_DW0 is written to. Hardware will automatically clear the bit to'0' after all of the newly written value of GPOLVL_DW1 and/or GPOLVL_DW0 bits have been serialized out at least once. This allows software a method to ensure no collapsing of any particular CxGPO[y] bit during a back to back software update of GPOLVL_DW0 or GPOLVL_DW1. Software may reprogram the GPOLVL_DW1 and/or GPOLVL_DW0 at any time irrespective of state of BSY bit if intermediate software update being collapsed is not a concern. Irrespective of the state of BSY bit, hardware serialization process walks thru each bit of GPOLVL_DW1 & GPOLVL_DW0 from bit[63] to bit[0] in descending order. Example: if hardware serialization is in the midst of serializing out CxGPO[3] and software updates GPOLVL_DW0, hardware serialization will serialize out the updated value of GPOLVL_DW0[2 to 0] as CxGPO[2:0]. Then hardware will serialize out the updated value of GPOLVL_DW1[MSB to 0] and so on (assuming >4 output expanders case).
0	0h RW	**ST:** This bit is set to 1 by software to start the serialization process. Software should not write this bit to 1 unless: the Busy status bit is cleared, and the CxCAP has been programmed. Also refer to the CxGPILVL(U) description if default input value is desired. Once this bit is set to 1, the serialization processes for input and output are running continuously. If software clears the ST bit to '0', hardware shall stop the serialization process at a convenient time but at atomic boundary. Note: Clearing Start bit does not trigger GSXSRESET# to be asserted.

33.4.81 GSX Channel-0 Test Mode (GSX_C0TM) — Offset 23Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 23Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RW	**Bit-bang GSXSRESET# (BBGSXSRESETB):** This bit allows software to directly bit bang the GSXSRESET#.
11	0h RW	**Bit-bang GSXSLOAD (BBGSXSLOAD):** This bit allows software to directly bit bang the GSXSLOAD.
10	0h RW	**Bit-bang GSXSDOUT (BBGSXSDOUT):** This bit allows software to directly bit bang the GSXSDOUT.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Bit-bang GSXSCLK (BBGSCLK):** This bit allows software to directly bit bang the GSXSCLK.
8	0h RW	**Bit-bang Enable (BBE):** When this bit is '1', the bit-bang mode is enable and the CxTM.BBGSXS* register bits are directly controlling the GSX pins.
7:1	0h RO	**Reserved**
0	0h RW	**Alternate SCLK Rate (ALTSCLK):** This test mode allows slower toggle rate of the GSX channel. '0' - default value of SCLKR.SCLKR_D '1' - default value of SCLKR.SCLKR_D divide by 4

33.4.82 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_0) — Offset 700h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 700h	44000700h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the SoC responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)

Bit Range	Default & Access	Field Name (ID): Description
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

33.4.83 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_0) — Offset 704h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 704h	0000006Eh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0100: 20k PD 1100: 20k PU 1111: Native controller selected by Pad Mode controls the Termination. This field should be set to 1111b for the selected native function that supports dynamic termination override. Refer to Vol1, GPIO chapter, for more info. Others: Reserved **Notes**: 1. The 20K pull-up/pull-down can only be enabled as long as the toggle rate on the signal is no more than 300KHz. 2. If a reserved value is programmed, pad may malfunction. 3. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, PU/PD settings should be programmed first to ensure the input does not float momentarily
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	6Eh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

33.4.84 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_C_0) — Offset 708h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 708h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:25	0h RO	**SoundWire Slew Control (sndwslewctrl) (SNDWSLEWCTRL):** 00 = Slow Slew Rate 01 = Middle Slew Rate 10 = Fast Slew Rate 11 = Fastest Slew Rate For iCDG buffers, this field is used to control the slew configuration, but extends beyond SoundWire to I2C, SDMMC and other applicable buffers. The setting may vary from one platform to another.
24	0h RO	**Bus Hold Enable (BUSHLDEN):** This feature uses the same build in pull-up/down resistor. In such, BIOS/FW needs to disable all pull-up/down to 'None' before enabling this feature. 1 = enable bus hold 0 = disable bus hold
23	0h RO	**Data Dependent Weak PU Control (DDPUCTRL):** 0 = normal I/O transmission mode. 1 = weak pull up configuration is overridden to disabled, when the raw RX pad state is 0 in output mode. During DFx mode like BSCAN, SCAN, HVM and etc, the DDPUCRTL shall be constrained to 0.
22	0h RO	**Analog Glitch Filter RX Pad State Select (ANALOGGFRXSEL):** Determine if the internal RX pad state should be subjected to analog glitch filter (implemented within the buffer) or not. This field only make sense when the buffer is configured as an input and is not disabled. 0 = Select non filtered RX pad state 1= Select filtered RX pad state. The mux to select filtered or non filtered RX pad state is implemented within the HIP family. During DFx mode like BSCAN, SCAN, HVM and etc, the AnalogGFRxSel shall be constrained to 0.
21:9	0h RO	**Reserved**
8	0h RO/V	**VCCIO selection (VCCIOSEL):** This bits is used to select VCCIO If the pad supports programmable VCCIO. The definition of high and low are implementation specific. 0: high voltage 1: low voltage

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Reserved**
4:1	0h RO	**Debounce duration (DEBOUNCE):** The debounce duration of value should be not less than 3. In other words, the value should not be any of 0, 1 and 2. The debounce time should be calculated as (2^debounce) * (glitch filter clock period) For example, when RTC clock (32 KHz) is used for glitch filter and debounce duration is set to 4b1011, the debounce time is (2 ^ 11) * (31.25 us) = 64ms
0	0h RO	**Debounce Enable (DEBEN):** This bit enables or disables the debouncer with the pad. 1 = Enable the debouncer of the pad 0 = Disable the debouncer of the pad

33.4.85 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_C_0) — Offset 70Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 70Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

33.4.86 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_1) — Offset 710h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.87 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_1) — Offset 714h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.88 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_C_1) — Offset 718h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.89 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_C_1) — Offset 71Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.90 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_2) — Offset 720h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.91 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_2) — Offset 724h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.92 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_C_2) — Offset 728h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD6A0000h + 728h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:25	0h RO	**SoundWire Slew Control (sndwslewctrl) (SNDWSLEWCTRL):** 00 = Slow Slew Rate 01 = Middle Slew Rate 10 = Fast Slew Rate 11 = Fastest Slew Rate For iCDG buffers, this field is used to control the slew configuration, but extends beyond SoundWire to I2C, SDMMC and other applicable buffers. The setting may vary from one platform to another.
24	0h RO	**Bus Hold Enable (BUSHLDEN):** This feature uses the same build in pull-up/down resistor. In such, BIOS/FW needs to disable all pull-up/down to 'None' before enabling this feature. 1 = enable bus hold 0 = disable bus hold
23	0h RO	**Data Dependent Weak PU Control (DDPUCTRL):** 0 = normal I/O transmission mode. 1 = weak pull up configuration is overridden to disabled, when the raw RX pad state is 0 in output mode. During DFx mode like BSCAN, SCAN, HVM and etc, the DDPUCRTL shall be constrained to 0.
22	0h RO	**Analog Glitch Filter RX Pad State Select (ANALOGGFRXSEL):** Determine if the internal RX pad state should be subjected to analog glitch filter (implemented within the buffer) or not. This field only make sense when the buffer is configured as an input and is not disabled. 0 = Select non filtered RX pad state 1= Select filtered RX pad state. The mux to select filtered or non filtered RX pad state is implemented within the HIP family. During DFx mode like BSCAN, SCAN, HVM and etc, the AnalogGFRxSel shall be constrained to 0.
21:12	0h RO	**Reserved**
11	0h RO/V	**Pin-strap value (PINSTRAPVAL):** This bit reflects the pin-strap value.
10:9	0h RO	**Reserved**
8	0h RO/V	**VCCIO selection (VCCIOSEL):** This bits is used to select VCCIO If the pad supports programmable VCCIO. The definition of high and low are implementation specific. 0: high voltage 1: low voltage

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Reserved**
4:1	0h RO	**Debounce duration (DEBOUNCE):** The debounce duration of value should be not less than 3. In other words, the value should not be any of 0, 1 and 2. The debounce time should be calculated as (2^debounce) * (glitch filter clock period) For example, when RTC clock (32 KHz) is used for glitch filter and debounce duration is set to 4b1011, the debounce time is (2 ^ 11) * (31.25 us) = 64ms
0	0h RO	**Debounce Enable (DEBEN):** This bit enables or disables the debouncer with the pad. 1 = Enable the debouncer of the pad 0 = Disable the debouncer of the pad

33.4.93 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_C_2) — Offset 72Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.94 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_3) — Offset 730h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.95 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_3) — Offset 734h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.96 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_C_3) — Offset 738h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.97 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_C_3) — Offset 73Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.98 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_4) — Offset 740h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.99 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_4) — Offset 744h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.100 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_C_4) — Offset 748h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.101 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_C_4) — Offset 74Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.102 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_5) — Offset 750h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.103 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_5) — Offset 754h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.104 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_C_5) — Offset 758h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_2, offset 728h.

33.4.105 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_C_5) — Offset 75Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.106 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_6) — Offset 760h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.107 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_6) — Offset 764h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.108 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_C_6) — Offset 768h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.109 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_C_6) — Offset 76Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.110 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_7) — Offset 770h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.111 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_7) — Offset 774h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.112 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_C_7) — Offset 778h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.113 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_C_7) — Offset 77Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.113.1 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_0) — Offset 880h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.114 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_0) — Offset 884h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.115 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_0) — Offset 888h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_2, offset 728h.

33.4.116 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_0) — Offset 88Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.117 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_1) — Offset 890h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.118 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_1) — Offset 894h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.119 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_1) — Offset 898h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.120 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_1) — Offset 89Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.121 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_2) — Offset 8A0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.122 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_2) — Offset 8A4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.123 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_2) — Offset 8A8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_2, offset 728h.

33.4.124 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_2) — Offset 8ACh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.125 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_3) — Offset 8B0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.126 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_3) — Offset 8B4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.127 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_3) — Offset 8B8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.128 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_3) — Offset 8BCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.129 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_4) — Offset 8C0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.130 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_4) — Offset 8C4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.131 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_4) — Offset 8C8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.132 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_4) — Offset 8CCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.133 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_5) — Offset 8D0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.134 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_5) — Offset 8D4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.135 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_5) — Offset 8D8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.136 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_5) — Offset 8DCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.137 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_6) — Offset 8E0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.138 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_6) — Offset 8E4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.139 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_6) — Offset 8E8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.140 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_6) — Offset 8ECh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.141 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_7) — Offset 8F0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.142 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_7) — Offset 8F4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.143 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_7) — Offset 8F8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_2, offset 728h.

33.4.144 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_7) — Offset 8FCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.145 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_10) — Offset 920h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.146 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_10) — Offset 924h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.147 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_10) — Offset 928h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_2, offset 728h.

33.4.148 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_10) — Offset 92Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.149 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_11) — Offset 930h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.150 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_11) — Offset 934h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.151 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_11) — Offset 938h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.152 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_11) — Offset 93Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.153 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_12) — Offset 940h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.154 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_12) — Offset 944h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.155 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_12) — Offset 948h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.156 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_12) — Offset 94Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.157 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_13) — Offset 950h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.158 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_13) — Offset 954h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.159 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_13) — Offset 958h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.160 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_13) — Offset 95Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.161 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_14) — Offset 960h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.162 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_14) — Offset 964h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.163 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_14) — Offset 968h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.164 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_14) — Offset 96Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.165 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_15) — Offset 970h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.166 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_15) — Offset 974h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.167 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_15) — Offset 978h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.168 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_15) — Offset 97Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.169 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_16) — Offset 980h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.170 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_16) — Offset 984h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.171 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_16) — Offset 988h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.172 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_16) — Offset 98Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.173 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_17) — Offset 990h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.174 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_17) — Offset 994h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.175 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_17) — Offset 998h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.176 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_17) — Offset 99Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.177 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_18) — Offset 9A0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.178 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_18) — Offset 9A4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.179 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_18) — Offset 9A8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.180 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_18) — Offset 9ACh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.181 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_22) — Offset 9E0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.182 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_22) — Offset 9E4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.183 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_22) — Offset 9E8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.184 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_22) — Offset 9ECh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.185 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_23) — Offset 9F0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.186 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_23) — Offset 9F4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.187 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_F_23) — Offset 9F8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.188 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_F_23) — Offset 9FCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.189 Pad Configuration DW0 (PAD_CFG_DW0_L_BKLTEN) — Offset A10h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.190 Pad Configuration DW1 (PAD_CFG_DW1_L_BKLTEN) — Offset A14h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.191 Pad Configuration DW2 (PAD_CFG_DW2_L_BKLTEN) — Offset A18h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.192 Pad Configuration DW3 (PAD_CFG_DW3_L_BKLTEN) — Offset A1Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.193 Pad Configuration DW0 (PAD_CFG_DW0_L_BKLTCTL) — Offset A20h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.194 Pad Configuration DW1 (PAD_CFG_DW1_L_BKLTCTL) — Offset A24h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.195 Pad Configuration DW2 (PAD_CFG_DW2_L_BKLTCTL) — Offset A28h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.196 Pad Configuration DW3 (PAD_CFG_DW3_L_BKLTCTL) — Offset A2Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.197 Pad Configuration DW0 (PAD_CFG_DW0_L_VDDEN) — Offset A30h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.198 Pad Configuration DW1 (PAD_CFG_DW1_L_VDDEN) — Offset A34h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.199 Pad Configuration DW2 (PAD_CFG_DW2_L_VDDEN) — Offset A38h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.200 Pad Configuration DW3 (PAD_CFG_DW3_L_VDDEN) — Offset A3Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.201 Pad Configuration DW0 (PAD_CFG_DW0_SYS_PWROK) — Offset A40h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.202 Pad Configuration DW1 (PAD_CFG_DW1_SYS_PWROK) — Offset A44h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.203 Pad Configuration DW2 (PAD_CFG_DW2_SYS_PWROK) — Offset A48h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.204 Pad Configuration DW3 (PAD_CFG_DW3_SYS_PWROK) — Offset A4Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.205 Pad Configuration DW0 (PAD_CFG_DW0_SYS_RESETB) — Offset A50h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.206 Pad Configuration DW1 (PAD_CFG_DW1_SYS_RESETB) — Offset A54h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.207 Pad Configuration DW2 (PAD_CFG_DW2_SYS_RESETB) — Offset A58h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.208 Pad Configuration DW3 (PAD_CFG_DW3_SYS_RESETB) — Offset A5Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.209 Pad Configuration DW0 (PAD_CFG_DW0_MLK_RSTB) — Offset A60h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.210 Pad Configuration DW1 (PAD_CFG_DW1_MLK_RSTB) — Offset A64h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.211 Pad Configuration DW2 (PAD_CFG_DW2_MLK_RSTB) — Offset A68h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.212 Pad Configuration DW3 (PAD_CFG_DW3_MLK_RSTB) — Offset A6Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.213 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_0) — Offset A70h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.214 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_0) — Offset A74h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.215 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_0) — Offset A78h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.216 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_0) — Offset A7Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.217 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_1) — Offset A80h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.218 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_1) — Offset A84h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.219 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_1) — Offset A88h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.220 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_1) — Offset A8Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.221 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_2) — Offset A90h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.222 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_2) — Offset A94h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.223 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_2) — Offset A98h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.224 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_2) — Offset A9Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.225 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_3) — Offset AA0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.226 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_3) — Offset AA4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.227 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_3) — Offset AA8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.228 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_3) — Offset AACh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.229 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_4) — Offset AB0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.230 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_4) — Offset AB4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.231 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_4) — Offset AB8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.232 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_4) — Offset ABCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.233 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_5) — Offset AC0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.234 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_5) — Offset AC4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.235 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_5) — Offset AC8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.236 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_5) — Offset ACCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.237 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_6) — Offset AD0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.238 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_6) — Offset AD4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.239 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_6) — Offset AD8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_2, offset 728h.

33.4.240 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_6) — Offset ADCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.241 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_7) — Offset AE0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.242 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_7) — Offset AE4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.243 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_7) — Offset AE8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.244 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_7) — Offset AECh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.245 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_8) — Offset AF0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.246 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_8) — Offset AF4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.247 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_8) — Offset AF8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.248 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_8) — Offset AFCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.249 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_9) — Offset B00h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.250 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_9) — Offset B04h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.251 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_9) — Offset B08h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_2, offset 728h.

33.4.252 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_9) — Offset B0Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.253 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_10) — Offset B10h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.254 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_10) — Offset B14h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.255 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_10) — Offset B18h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_2, offset 728h.

33.4.256 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_10) — Offset B1Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.257 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_11) — Offset B20h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.258 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_11) — Offset B24h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.259 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_11) — Offset B28h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_2, offset 728h.

33.4.260 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_11) — Offset B2Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.261 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_12) — Offset B30h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.262 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_12) — Offset B34h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.263 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_12) — Offset B38h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.264 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_12) — Offset B3Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.265 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_13) — Offset B40h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.266 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_13) — Offset B44h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.267 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_13) — Offset B48h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.268 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_13) — Offset B4Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.269 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_14) — Offset B50h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.270 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_14) — Offset B54h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.271 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_14) — Offset B58h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.272 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_14) — Offset B5Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.273 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_15) — Offset B60h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.274 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_15) — Offset B64h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.275 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_15) — Offset B68h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.276 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_15) — Offset B6Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.277 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_16) — Offset B70h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.278 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_16) — Offset B74h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.279 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_16) — Offset B78h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.280 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_16) — Offset B7Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.281 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_17) — Offset B80h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.282 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_17) — Offset B84h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.283 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_17) — Offset B88h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.284 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_17) — Offset B8Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.285 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_18) — Offset B90h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.286 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_18) — Offset B94h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.287 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_18) — Offset B98h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.288 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_18) — Offset B9Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.289 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_19) — Offset BA0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.290 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_19) — Offset BA4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.291 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_19) — Offset BA8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_2, offset 728h.

33.4.292 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_19) — Offset BACh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.293 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_20) — Offset BB0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.294 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_20) — Offset BB4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.295 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_20) — Offset BB8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.296 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_20) — Offset BBCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.297 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_21) — Offset BC0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.298 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_21) — Offset BC4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.299 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_21) — Offset BC8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_2, offset 728h.

33.4.300 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_21) — Offset BCCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.301 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_22) — Offset BD0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.302 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_22) — Offset BD4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.303 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_22) — Offset BD8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.304 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_22) — Offset BDCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.305 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_23) — Offset BE0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.306 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_23) — Offset BE4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.307 Pad Configuration DW2 (PAD_CFG_DW2_GPPC_E_23) — Offset BE8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.308 Pad Configuration DW3 (PAD_CFG_DW3_GPPC_E_23) — Offset BECh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.309 Pad Configuration DW0 (PAD_CFG_DW0_JTAG_TDO) — Offset C00h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.310 Pad Configuration DW1 (PAD_CFG_DW1_JTAG_TDO) — Offset C04h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.311 Pad Configuration DW2 (PAD_CFG_DW2_JTAG_TDO) — Offset C08h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.312 Pad Configuration DW3 (PAD_CFG_DW3_JTAG_TDO) — Offset C0Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.313 Pad Configuration DW0 (PAD_CFG_DW0_JTAGX) — Offset C10h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.314 Pad Configuration DW1 (PAD_CFG_DW1_JTAGX) — Offset C14h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.315 Pad Configuration DW2 (PAD_CFG_DW2_JTAGX) — Offset C18h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.316 Pad Configuration DW3 (PAD_CFG_DW3_JTAGX) — Offset C1Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.317 Pad Configuration DW0 (PAD_CFG_DW0_CPU_TRSTB) — Offset C40h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.318 Pad Configuration DW1 (PAD_CFG_DW1_CPU_TRSTB) — Offset C44h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.319 Pad Configuration DW2 (PAD_CFG_DW2_CPU_TRSTB) — Offset C48h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.320 Pad Configuration DW3 (PAD_CFG_DW3_CPU_TRSTB) — Offset C4Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.321 Pad Configuration DW0 (PAD_CFG_DW0_JTAG_TDI) — Offset C50h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.322 Pad Configuration DW1 (PAD_CFG_DW1_JTAG_TDI) — Offset C54h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.323 Pad Configuration DW2 (PAD_CFG_DW2_JTAG_TDI) — Offset C58h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.324 Pad Configuration DW3 (PAD_CFG_DW3_JTAG_TDI) — Offset C5Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.325 Pad Configuration DW0 (PAD_CFG_DW0_JTAG_TMS) — Offset C60h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.326 Pad Configuration DW1 (PAD_CFG_DW1_JTAG_TMS) — Offset C64h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.327 Pad Configuration DW2 (PAD_CFG_DW2_JTAG_TMS) — Offset C68h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.328 Pad Configuration DW3 (PAD_CFG_DW3_JTAG_TMS) — Offset C6Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.329 Pad Configuration DW0 (PAD_CFG_DW0_JTAG_TCK) — Offset C70h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.330 Pad Configuration DW1 (PAD_CFG_DW1_JTAG_TCK) — Offset C74h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.331 Pad Configuration DW2 (PAD_CFG_DW2_JTAG_TCK) — Offset C78h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_0, offset 708h.

33.4.332 Pad Configuration DW3 (PAD_CFG_DW3_JTAG_TCK) — Offset C7Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.4.333 Pad Configuration DW0 (PAD_CFG_DW0_DBG_PMODE) — Offset C80h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPPC_C_0, offset 700h.

33.4.334 Pad Configuration DW1 (PAD_CFG_DW1_DBG_PMODE) — Offset C84h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPPC_C_0, offset 704h.

33.4.335 Pad Configuration DW2 (PAD_CFG_DW2_DBG_PMODE) — Offset C88h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPPC_C_2, offset 728h.

33.4.336 Pad Configuration DW3 (PAD_CFG_DW3_DBG_PMODE) — Offset C8Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPPC_C_0, offset 70Ch.

33.5 GPIO Community 5 Registers

This Section contains the GPIO Community 5 - 0x69h Registers.

Table 33-5. Summary of GPIO Community 5 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8h	4	Family Base Address (FAMBAR)	00000300h
Ch	4	Pad Base Address (PADBAR)	00000700h
10h	4	Miscellaneous Configuration (MISCCFG)	37043200h
20h	4	Pad Ownership (PAD_OWN_GPP_R_0)	00000000h
24h	4	Pad Ownership (PAD_OWN_SPI_0)	00000000h
28h	4	Pad Ownership (PAD_OWN_SPI_1)	00000000h
80h	4	Pad Configuration Lock (PADCFGLOCK_GPP_R_0)	00000000h
84h	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_R_0)	00000000h
88h	4	Pad Configuration Lock (PADCFGLOCK_SPI_0)	00000000h
8Ch	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_SPI_0)	00000000h
B0h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_R_0)	00000000h
B4h	4	Host Software Pad Ownership (HOSTSW_OWN_SPI_0)	00000000h
100h	4	GPI Interrupt Status (GPI_IS_GPP_R_0)	00000000h
104h	4	GPI Interrupt Status (GPI_IS_SPI_0)	00000000h
120h	4	GPI Interrupt Enable (GPI_IE_GPP_R_0)	00000000h
124h	4	GPI Interrupt Enable (GPI_IE_SPI_0)	00000000h
140h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_0)	00000000h
144h	4	GPI General Purpose Events Status (GPI_GPE_STS_SPI_0)	00000000h
160h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_0)	00000000h
164h	4	GPI General Purpose Events Enable (GPI_GPE_EN_SPI_0)	00000000h
180h	4	SMI Status (GPI_SMI_STS_GPP_R_0)	00000000h
184h	4	SMI Status (GPI_SMI_STS_SPI_0)	00000000h
1A0h	4	SMI Enable (GPI_SMI_EN_GPP_R_0)	00000000h
1A4h	4	SMI Enable (GPI_SMI_EN_SPI_0)	00000000h
1C0h	4	NMI Status (GPI_NMI_STS_GPP_R_0)	00000000h
1C4h	4	NMI Status (GPI_NMI_STS_SPI_0)	00000000h
1E0h	4	NMI Enable (GPI_NMI_EN_GPP_R_0)	00000000h
1E4h	4	NMI Enable (GPI_NMI_EN_SPI_0)	00000000h
700h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_0)	44000700h
704h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_0)	00000058h
708h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_R_0)	00000000h
70Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_R_0)	00000000h
710h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_1)	44000700h
714h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_1)	00003C59h
718h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_R_1)	00000000h
71Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_R_1)	00000000h

Table 33-5. Summary of GPIO Community 5 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
720h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_2)	44000600h
724h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_2)	00003C5Ah
728h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_R_2)	00000000h
72Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_R_2)	00000000h
730h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_3)	44000700h
734h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_3)	00003C5Bh
738h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_R_3)	00000000h
73Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_R_3)	00000000h
740h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_4)	44000700h
744h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_4)	0000005Ch
748h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_R_4)	00000000h
74Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_R_4)	00000000h
750h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_5)	44000300h
754h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_5)	0000005Dh
758h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_R_5)	00000000h
75Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_R_5)	00000000h
760h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_6)	44000300h
764h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_6)	0000005Eh
768h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_R_6)	00000000h
76Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_R_6)	00000000h
770h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_7)	44000300h
774h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_7)	0000005Fh
778h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPP_R_7)	00000000h
77Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_GPP_R_7)	00000000h
780h	4	Pad Configuration DW0 (PAD_CFG_DW0_SPI0_IO_2)	40000700h
784h	4	Pad Configuration DW1 (PAD_CFG_DW1_SPI0_IO_2)	00003C00h
788h	4	Pad Configuration DW2 (PAD_CFG_DW2_SPI0_IO_2)	00000000h
78Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_SPI0_IO_2)	00000000h
790h	4	Pad Configuration DW0 (PAD_CFG_DW0_SPI0_IO_3)	40000700h
794h	4	Pad Configuration DW1 (PAD_CFG_DW1_SPI0_IO_3)	00003C00h
798h	4	Pad Configuration DW2 (PAD_CFG_DW2_SPI0_IO_3)	00000000h
79Ch	4	Pad Configuration DW3 (PAD_CFG_DW3_SPI0_IO_3)	00000000h
7A0h	4	Pad Configuration DW0 (PAD_CFG_DW0_SPI0_MOSI_IO_0)	40000700h
7A4h	4	Pad Configuration DW1 (PAD_CFG_DW1_SPI0_MOSI_IO_0)	00003C00h
7A8h	4	Pad Configuration DW2 (PAD_CFG_DW2_SPI0_MOSI_IO_0)	00000000h
7ACh	4	Pad Configuration DW3 (PAD_CFG_DW3_SPI0_MOSI_IO_0)	00000000h
7B0h	4	Pad Configuration DW0 (PAD_CFG_DW0_SPI0_MISO_IO_1)	40000700h
7B4h	4	Pad Configuration DW1 (PAD_CFG_DW1_SPI0_MISO_IO_1)	00003C00h
7B8h	4	Pad Configuration DW2 (PAD_CFG_DW2_SPI0_MISO_IO_1)	00000000h
7BCh	4	Pad Configuration DW3 (PAD_CFG_DW3_SPI0_MISO_IO_1)	00000000h

Table 33-5. Summary of GPIO Community 5 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
7C0h	4	Pad Configuration DW0 (PAD_CFG_DW0_SPI0_TPM_CSB)	40000700h
7C4h	4	Pad Configuration DW1 (PAD_CFG_DW1_SPI0_TPM_CSB)	00003C00h
7C8h	4	Pad Configuration DW2 (PAD_CFG_DW2_SPI0_TPM_CSB)	00000000h
7CCh	4	Pad Configuration DW3 (PAD_CFG_DW3_SPI0_TPM_CSB)	00000000h
7D0h	4	Pad Configuration DW0 (PAD_CFG_DW0_SPI0_FLASH_0_CSB)	40000700h
7D4h	4	Pad Configuration DW1 (PAD_CFG_DW1_SPI0_FLASH_0_CSB)	00003C00h
7D8h	4	Pad Configuration DW2 (PAD_CFG_DW2_SPI0_FLASH_0_CSB)	00000000h
7DCh	4	Pad Configuration DW3 (PAD_CFG_DW3_SPI0_FLASH_0_CSB)	00000000h
7E0h	4	Pad Configuration DW0 (PAD_CFG_DW0_SPI0_FLASH_1_CSB)	40000700h
7E4h	4	Pad Configuration DW1 (PAD_CFG_DW1_SPI0_FLASH_1_CSB)	00003C00h
7E8h	4	Pad Configuration DW2 (PAD_CFG_DW2_SPI0_FLASH_1_CSB)	00000000h
7ECh	4	Pad Configuration DW3 (PAD_CFG_DW3_SPI0_FLASH_1_CSB)	00000000h
7F0h	4	Pad Configuration DW0 (PAD_CFG_DW0_SPI0_CLK)	40000700h
7F4h	4	Pad Configuration DW1 (PAD_CFG_DW1_SPI0_CLK)	00003C00h
7F8h	4	Pad Configuration DW2 (PAD_CFG_DW2_SPI0_CLK)	00000000h
7FCh	4	Pad Configuration DW3 (PAD_CFG_DW3_SPI0_CLK)	00000000h

33.5.1 Family Base Address (FAMBAR) — Offset 8h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 8h	00000300h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0300h RO	**Family Base Address (FAMBAR):** This field provides the starting byte-align address of Family0 register sets within a Community. It is meant for software to discover from where the very first Family register (i.e. Family0 register) starts to compute the next Families address offsets.

33.5.2 Pad Base Address (PADBAR) — Offset Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + Ch	00000700h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0700h RO	**Pad Base Address (PADBAR):** This field provides the starting byte-align address of Pad0 register sets within a Community. It is meant for software to discover from where the very first Pad register (i.e. Pad0 register) starts to compute the next Pad address offsets.

33.5.3 Miscellaneous Configuration (MISCCFG) — Offset 10h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 10h	37043200h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	37h RW	**GPIO Driver Mode Interrupt Select (GPDMINTSEL):** IRQ globally for all pads (GPI_IS with corresponding GPI_IE enable). 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255
23:20	0h RO	**Reserved**
19:16	4h RW	**GPIO Group to GPE_DW2 assignment encoding (GPE0_DW2):** This register assigns a specific GPIO Group to the ACPI GPE0[95:64]. The setting is SoC specific.
15:12	3h RW	**GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1):** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The setting is SoC specific.
11:8	2h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0):** This register assigns a specific GPIO Group to the ACPI GPE0[31:0]. The setting is SoC specific.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**GPIO IOSF Sideband VNNREQ Enable (GPVNNREQEN):** Specify whether the GPIO Community should take part in IOSFSB VNNREQ/ACK handshake 0 = Disable participation in IOSF SB VNNREQ and VNNACK handshake 1 = Enable participation in IOSF SB VNNREQ and VNNACK handshake When this bit set to 1, GPIO controller will de-assert the VNNREQ when there is no outstanding IOSF SB upstream cycle from GPIO controller. When this bit set to 1 and MISCSECCFG.SBTRIGDIS is 0, GPIO controller will assert the VNNREQ to request for the following list of IOSF-SB Message initiation. Event list: IRQ NMI SMI SSMI VNNREQ shall de-assert when MISCSECCFG.SBTRIGDIS is set to 1. As VNNAON IP, GPIO controller will assert the VNNREQ when in reset. The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pwrgate_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this power gating, this register always default to 1.
6	0h RW	**GPIO PGCB Clock Dynamic Partition Clock Gating Enable (GPPGCBDPCGEN):** Specify whether the GPIO Community PGCB clock should take part in partition clock gating 0 = Disable participation in PGCB clock dynamic partition clock gating 1 = Enable participation in PGCB clock dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
5	0h RW	**GPIO IOSF Sideband Dynamic Partition Clock Gating Enable (GPSIDEDPCGEN):** Specify whether the GPIO Community IOSF sideband clock should take part in partition clock gating 0 = Disable participation in IOSF sideband clock dynamic partition clock gating 1 = Enable participation in IOSF sideband clock dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
4	0h RW	**GPIO RCOMP clock Dynamic Local Clock Gating (GPRCOMPCDLCGEN):** Specify whether the GPIO Community should perform local clock gating on RCOMP clock 0 = Disable dynamic RCOMP clock local clock gating 1 = Enable dynamic RCOMP clock local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
3	0h RW	**GPIO RTC clock Dynamic Local Clock Gating (GPRTCDLCGEN):** Specify whether the GPIO Community should perform local clock gating on RTC clock 0 = Disable dynamic RTC clock local clock gating 1 = Enable dynamic RTC clock local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GSX Static Local Clock Gating (GSXSLCGEN):** Specify whether the GSX controller should be statically clock gated for power saving if it is not enabled (even though the capability is available). 0 = Disable static local clock gating 1 = Enable static local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
1	0h RW	**GPIO Dynamic Partition Clock Gating Enable (GPDPCGEN):** Specify whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0
0	0h RW	**GPIO Dynamic Local Clock Gating Enable (GPDLCGEN):** Specify whether the GPIO Community should perform local clock gating 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating The default value for this register field is controlled by internal power gating soft strap signal gpio_sstrap_pmmode_def_gpcom<community name>. The soft strap is pulled by the GPIO community soft strap puller. For SOC that does not have the soft strap defined for this clock gating, this register always default to 0

33.5.4 Pad Ownership (PAD_OWN_GPP_R_0) — Offset 20h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 20h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**Pad Ownership (PAD_OWN_GPP_R_7):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW	**Pad Ownership (PAD_OWN_GPP_R_6):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPP_R_5):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Pad Ownership (PAD_OWN_GPP_R_4):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Pad Ownership (PAD_OWN_GPP_R_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**Pad Ownership (PAD_OWN_GPP_R_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Pad Ownership (PAD_OWN_GPP_R_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Pad Ownership (PAD_OWN_GPP_R_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.5.5 Pad Ownership (PAD_OWN_SPI_0) — Offset 24h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 24h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RO	**Pad Ownership (PAD_OWN_SPI0_CLK):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
27:26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RO	**Pad Ownership (PAD_OWN_SPI0_FLASH_1_CSB):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RO	**Pad Ownership (PAD_OWN_SPI0_FLASH_0_CSB):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
19:18	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RO	**Pad Ownership (PAD_OWN_SPI0_TPM_CSB):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RO	**Pad Ownership (PAD_OWN_SPI0_MISO_IO_1):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
11:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RO	**Pad Ownership (PAD_OWN_SPI0_MOSI_IO_0):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
7:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RO	**Pad Ownership (PAD_OWN_SPI0_IO_3):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.
3:2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RO	**Pad Ownership (PAD_OWN_SPI0_IO_2):** This register can be written by CSME GPIO Function** only. Write access without CSME GPIO Function SAI shall be dropped. There is no SAI restriction on register read. Status update: GPIO input event notification (if enabled) to embedded system owner via IOSF-SB Virtual Wire message, or Host SMI (if implemented), NMI (if implemented), SCI/GPE or GPI_INT status update All subsequent read/write accesses to the corresponding pad's Pad Configuration Register are verified with the owner's GPIO Function SAI. PAD_OWN[1:0] encoding: '00' = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership. During host ownership, CSME, IE and ISH do not own this pad and are not notified of the GPIO input event. '01' = CSME GPIO Mode. CSME has ownership of the pad. All accesses to Pad Configuration register set must be verified with CSME GPIO Function SAI **. Non-posted cycle access without CSME SAI shall result into nsuccessful Completionstatus. Posted cycle access without CSME SAI shall be dropped. In CSME GPIO Mode, the host related status registers related to the pad (refer to host ownership above) are masked from being updated by GPIO input event. If IOSF-SB Virtual Wire message generation is enabled for this pad, GPIO hardware sends the Virtual Wire message to CSME GPIO Function. Only CSME GPIO Function is notified of the GPIO input event. '10' = ISH GPIO Mode. Same description as CSME GPIO Mode above except verifying ISH GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. '11' = IE GPIO Mode. Same description as CSME GPIO Mode above except verifying IE GPIO Function SAI for pad related register accesses and the Virtual Wire message is delivered to the ISH GPIO Function. All other values are reserved. Implementation shall treat reserved values the same as 0h. ** During DFx mode, Secure DFx can write to the PAD_OWN.

33.5.6 Pad Ownership (PAD_OWN_SPI_1) — Offset 28h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 28h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1:0	0h RO	**Reserved**

33.5.7 Pad Configuration Lock (PADCFGLOCK_GPP_R_0) — Offset 80h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 80h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_R_7):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_R_6):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_R_5):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_R_4):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_R_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_R_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_R_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_R_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

33.5.8 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_R_0) — Offset 84h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 84h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_R_7):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_R_6):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_R_5):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_R_4):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_R_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_R_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_R_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_R_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

33.5.9 Pad Configuration Lock (PADCFGLOCK_SPI_0) — Offset 88h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 88h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RSV	**Reserved**
7	0h RSV	**Pad Config Lock (PADCFGLOCK_SPI0_CLK):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RSV	**Pad Config Lock (PADCFGLOCK_SPI0_FLASH_1_CSB):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
5	0h RSV	**Pad Config Lock (PADCFGLOCK_SPI0_FLASH_0_CSB):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RSV	**Pad Config Lock (PADCFGLOCK_SPI0_TPM_CSB):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
3	0h RSV	**Pad Config Lock (PADCFGLOCK_SPI0_MISO_IO_1):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**Pad Config Lock (PADCFGLOCK_SPI0_MOSI_IO_0):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.
1	0h RSV	**Pad Config Lock (PADCFGLOCK_SPI0_IO_3):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RSV	**Pad Config Lock (PADCFGLOCK_SPI0_IO_2):** PadCfgLock locks specific register fields in the pad specific registers (in Community or Pad) from being configured. The registers affected become Read-Only and software writes to these registers have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Lock the following register fields as read-only (RO): Pad Configuration registers (exclude GPIOTXState) GPI_NMI_EN Register (if implemented) GPI_SMI_EN Register (if implemented) GPI_GPE_EN Register (if implemented) Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 When PadCfgLock[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted cycle that is end point specific to GPIO Community. The Opcode shall be 13h. Posted access has no effect and shall be dropped internally. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific register access message PIO_PadCfg_Unlockwith Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h and Posted='0'.

33.5.10 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_SPI_0) — Offset 8Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 8Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RSV	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
7	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_SPI0_CLK):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
6	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_SPI0_FLASH_1_CSB):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_SPI0_FLASH_0_CSB):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
4	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_SPI0_TPM_CSB):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_SPI0_MISO_IO_1):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
2	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_SPI0_MOSI_IO_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_SPI0_IO_3):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.
0	0h RSV	**Pad Config Lock TXState (PADCFGLOCKTX_SPI0_IO_2):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. This field is meaningful and takes effect only if the pad is owned by host (refer to PAD_OWN register). Pads under other ownership are not affected by the PadCfgLock. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) : Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1 = pad N-1 When PadCfgLockTx[n] is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown. In order to support this optional mechanism, this register access type has to be RW and access with non-posted write cycle that is end point specific to GPIO Community. The Opcode for the write shall be 13h. Write cycle with any other opcode has no effect on the PadCfgLockTx register value. The non-posted write cycle can be generated using the P2SB bridge's ideband Message Interface Accessmethod in order to trigger a GPIO end point specific IOSF-SB message PIO_PadCfg_Unlock with Opcode of 13h. This can be achieved by programming the P2SB configuration register SBISTAT.Opcode to 13h.

33.5.11 Host Software Pad Ownership (HOSTSW_OWN_GPP_R_0) — Offset B0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**HOSTSW_OWN_GPP_R_7:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
6	0h RW	**HOSTSW_OWN_GPP_R_6:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**HOSTSW_OWN_GPP_R_5:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
4	0h RW	**HOSTSW_OWN_GPP_R_4:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
3	0h RW	**HOSTSW_OWN_GPP_R_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HOSTSW_OWN_GPP_R_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RW	**HOSTSW_OWN_GPP_R_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RW	**HOSTSW_OWN_GPP_R_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

33.5.12 Host Software Pad Ownership (HOSTSW_OWN_SPI_0) — Offset B4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RSV	**Reserved**
7	0h RSV	**HOSTSW_OWN_SPI0_CLK:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
6	0h RSV	**HOSTSW_OWN_SPI0_FLASH_1_CSB:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**HOSTSW_OWN_SPI0_FLASH_0_CSB:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
4	0h RSV	**HOSTSW_OWN_SPI0_TPM_CSB:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
3	0h RSV	**HOSTSW_OWN_SPI0_MISO_IO_1:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**HOSTSW_OWN_SPI0_MOSI_IO_0:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
1	0h RSV	**HOSTSW_OWN_SPI0_IO_3:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.
0	0h RSV	**HOSTSW_OWN_SPI0_IO_2:** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 Note: N is the number of Pads in the Community. Optionally N may be the number of pads for a group of pads in the Community. In which case there is a register for each group.

33.5.13 GPI Interrupt Status (GPI_IS_GPP_R_0) — Offset 100h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 100h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_R_7):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_R_6):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_R_5):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_R_4):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_R_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_R_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_R_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_R_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.5.14 GPI Interrupt Status (GPI_IS_SPI_0) — Offset 104h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 104h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RSV	**Reserved**
7	0h RSV	**GPI Interrupt Status (GPI_INT_STS_SPI0_CLK):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RSV	**GPI Interrupt Status (GPI_INT_STS_SPI0_FLASH_1_CSB):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI Interrupt Status (GPI_INT_STS_SPI0_FLASH_0_CSB):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RSV	**GPI Interrupt Status (GPI_INT_STS_SPI0_TPM_CSB):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RSV	**GPI Interrupt Status (GPI_INT_STS_SPI0_MISO_IO_1):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI Interrupt Status (GPI_INT_STS_SPI0_MOSI_IO_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RSV	**GPI Interrupt Status (GPI_INT_STS_SPI0_IO_3):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RSV	**GPI Interrupt Status (GPI_INT_STS_SPI0_IO_2):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[2:0] is '001' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x]. Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.5.15 GPI Interrupt Enable (GPI_IE_GPP_R_0) — Offset 120h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 120h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_R_7):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_R_6):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_R_5):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_R_4):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_R_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_R_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_R_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_R_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.5.16 GPI Interrupt Enable (GPI_IE_SPI_0) — Offset 124h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 124h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
8	0h RSV	**Reserved**
7	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_SPI0_CLK):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
6	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_SPI0_FLASH_1_CSB):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
5	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_SPI0_FLASH_0_CSB):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
4	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_SPI0_TPM_CSB):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_SPI0_MISO_IO_1):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
2	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_SPI0_MOSI_IO_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
1	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_SPI0_IO_3):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1
0	0h RSV	**GPI Interrupt Enable (GPI_INT_EN_SPI0_IO_2):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing. Each bit position correspond to 1 pad: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1

33.5.17 GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_0) — Offset 140h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 140h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_7):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_6):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_5):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_4):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.5.18 GPI General Purpose Events Status (GPI_GPE_STS_SPI_0) — Offset 144h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 144h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RSV	**Reserved**
7	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_SPI0_CLK):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_SPI0_FLASH_1_CSB):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_SPI0_FLASH_0_CSB):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
4	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_SPI0_TPM_CSB):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_SPI0_MISO_IO_1):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_SPI0_MOSI_IO_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_SPI0_IO_3):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RSV	**GPI General Purpose Events Status (GPI_GPE_STS_SPI0_IO_2):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS[i] bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN[i] does not prevent the setting of GPI_GPE_STS[i]. Each bit position correspond to 1 pad in the Community: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.5.19 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_0) — Offset 160h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 160h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_7):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_6):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_5):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_4):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.5.20 GPI General Purpose Events Enable (GPI_GPE_EN_SPI_0) — Offset 164h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 164h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RSV	**Reserved**
7	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_SPI0_CLK):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
6	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_SPI0_FLASH_1_CSB):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
5	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_SPI0_FLASH_0_CSB):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
4	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_SPI0_TPM_CSB):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
3	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_SPI0_MISO_IO_1):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_SPI0_MOSI_IO_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
1	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_SPI0_IO_3):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1
0	0h RSV	**GPI General Purpose Events Enable (GPI_GPE_EN_SPI0_IO_2):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS[i] bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'. Bit assignment: Bit0 = Pad0 Bit1 = Pad1 Bit2 = Pad2 ... Bit N-1= Pad N-1

33.5.21 SMI Status (GPI_SMI_STS_GPP_R_0) — Offset 180h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 180h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_R_7):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
6	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_R_6):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_R_5):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
4	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_R_4):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_R_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_R_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
1	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_R_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RSV	**GPI SMI Status (GPI_SMI_STS_GPP_R_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

33.5.22 SMI Status (GPI_SMI_STS_SPI_0) — Offset 184h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 184h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RSV	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
7	0h RSV	**GPI SMI Status (GPI_SMI_STS_SPI0_CLK):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
6	0h RSV	**GPI SMI Status (GPI_SMI_STS_SPI0_FLASH_1_CSB):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI SMI Status (GPI_SMI_STS_SPI0_FLASH_0_CSB):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
4	0h RSV	**GPI SMI Status (GPI_SMI_STS_SPI0_TPM_CSB):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RSV	**GPI SMI Status (GPI_SMI_STS_SPI0_MISO_IO_1):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
2	0h RSV	**GPI SMI Status (GPI_SMI_STS_SPI0_MOSI_IO_0):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RSV	**GPI SMI Status (GPI_SMI_STS_SPI0_IO_3):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.
0	0h RSV	**GPI SMI Status (GPI_SMI_STS_SPI0_IO_2):** This bit is set to '1' by hardware when a level event (See RxEdCfg, RxInv) is detected, and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN[x] does not prevent the setting of GPI_SMI_STS[x]. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 Defaults for these bits are dependent on the state of the GPI pads.

33.5.23 SMI Enable (GPI_SMI_EN_GPP_R_0) — Offset 1A0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 1A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_R_7):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
6	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_R_6):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_R_5):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
4	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_R_4):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
3	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_R_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_R_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_R_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RSV	**GPI SMI Enable (GPI_SMI_EN_GPP_R_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

33.5.24 SMI Enable (GPI_SMI_EN_SPI_0) — Offset 1A4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 1A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RSV	**Reserved**
7	0h RSV	**GPI SMI Enable (GPI_SMI_EN_SPI0_CLK):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
6	0h RSV	**GPI SMI Enable (GPI_SMI_EN_SPI0_FLASH_1_CSB):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI SMI Enable (GPI_SMI_EN_SPI0_FLASH_0_CSB):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
4	0h RSV	**GPI SMI Enable (GPI_SMI_EN_SPI0_TPM_CSB):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
3	0h RSV	**GPI SMI Enable (GPI_SMI_EN_SPI0_MISO_IO_1):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI SMI Enable (GPI_SMI_EN_SPI0_MOSI_IO_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
1	0h RSV	**GPI SMI Enable (GPI_SMI_EN_SPI0_IO_3):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1
0	0h RSV	**GPI SMI Enable (GPI_SMI_EN_SPI0_IO_2):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to '1'. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1

33.5.25 NMI Status (GPI_NMI_STS_GPP_R_0) — Offset 1C0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 1C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_R_7):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_R_6):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_R_5):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_R_4):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_R_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_R_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_R_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Status (GPI_NMI_STS_GPP_R_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.5.26 NMI Status (GPI_NMI_STS_SPI_0) — Offset 1C4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 1C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RSV	**Reserved**
7	0h RSV	**GPI NMI Status (GPI_NMI_STS_SPI0_CLK):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RSV	**GPI NMI Status (GPI_NMI_STS_SPI0_FLASH_1_CSB):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RSV	**GPI NMI Status (GPI_NMI_STS_SPI0_FLASH_0_CSB):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
4	0h RSV	**GPI NMI Status (GPI_NMI_STS_SPI0_TPM_CSB):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**GPI NMI Status (GPI_NMI_STS_SPI0_MISO_IO_1):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RSV	**GPI NMI Status (GPI_NMI_STS_SPI0_MOSI_IO_0):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
1	0h RSV	**GPI NMI Status (GPI_NMI_STS_SPI0_IO_3):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Status (GPI_NMI_STS_SPI0_IO_2):** This bit is set to '1' by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode (PMode) The corresponding GPIONMIRout is set to '1', i.e. programmed to route as NMI The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). The corresponding GPI_NMI_EN is set Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = There is no NMI event 1 = There is an NMI event Bit assignment: Bit0 = pad 0 Bit1 = pad 1 Bit2 = pad 2 ... Bit N-1= pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.5.27 NMI Enable (GPI_NMI_EN_GPP_R_0) — Offset 1E0h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 1E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_R_7):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_R_6):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_R_5):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_R_4):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_R_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
2	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_R_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_R_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Enable (GPI_NMI_EN_GPP_R_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.5.28 NMI Enable (GPI_NMI_EN_SPI_0) — Offset 1E4h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 1E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RSV	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
7	0h RSV	**GPI NMI Enable (GPI_NMI_EN_SPI0_CLK):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
6	0h RSV	**GPI NMI Enable (GPI_NMI_EN_SPI0_FLASH_1_CSB):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
5	0h RSV	**GPI NMI Enable (GPI_NMI_EN_SPI0_FLASH_0_CSB):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RSV	**GPI NMI Enable (GPI_NMI_EN_SPI0_TPM_CSB):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
3	0h RSV	**GPI NMI Enable (GPI_NMI_EN_SPI0_MISO_IO_1):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
2	0h RSV	**GPI NMI Enable (GPI_NMI_EN_SPI0_MOSI_IO_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RSV	**GPI NMI Enable (GPI_NMI_EN_SPI0_IO_3):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.
0	0h RSV	**GPI NMI Enable (GPI_NMI_EN_SPI0_IO_2):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. Bit assignment: Bit0 = Pad 0 Bit1 = Pad 1 Bit2 = Pad 2 ... Bit N-1 = Pad N-1 For pads which do not support NMI, the corresponding bit is read-only zero.

33.5.29 Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_0) — Offset 700h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 700h	44000700h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset the specified Pad Register fields. It is the SoC responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Global Reset (i.e global_rst_b) For DSW well pads, this register default value should configured as 00b. For Primary well GPIO pads, this register's default value should be configured as 01b. Note 1: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion. Note 2: The terms 'Powergood', 'Deep GPIO Reset', 'DSW', etc. are PCH-centric and are just examples. Different terms may be used in different projects. The point here is that these terms convey the nature of these resets. For example, any reset that cannot be asserted again unless power is removed (a sticky reset) may be a 'Powergood'.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	**Native Function Virtual Wire Message Enable (NAF_VWE):** This bit enables Native Function IOSF-SB Virtual wire message generation. Upon the enabling of this bit, the virtual wire message is sent to the appropriate destination enabled by pad mode selection whenever the value is different than the predefined function default value. Prior to enabling this bit, the pad mode must be set to a function where communication is done by message. When a change is detected on the pad and this bit is set, VW message is generated and delivered to the destination. 0 = Disable pad input event sampling and VW message generation. 1 = Enable pad input event sampling and VW message generation. This bit is read only 0 for pads without Native Function Virtual Wire messages enabled (e.g. GPIO Mode only pads or physical wire muxing only pads.)

Bit Range	Default & Access	Field Name (ID): Description
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	**Reserved**
12:10	1h RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ... 15 = Function 15, if applicable, control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	**Reserved**
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

33.5.30 Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_0) — Offset 704h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 704h	00000058h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**CFIO Pad Configuration I2CEN (CFIOPADCFG_I2CEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
29	0h RW	**CFIO Pad Configuration CSEN (CFIOPADCFG_CSEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
28	0h RO	**CFIO Pad Configuration PARKMODEEN_B (CFIOPADCFG_PARKMODEEN_B):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
27:26	0h RO	**CFIO Pad Configuration HYSCTL (CFIOPADCFG_HYSCTL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
25	0h RO	**CFIO Pad Configuration PADTOL (CFIOPADCFG_PADTOL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
24:22	0h RO	**CFIO Pad Configuration STRSEL (CFIOPADCFG_STRSEL):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
21	0h RO	**CFIO Pad Configuration HSMODE (CFIOPADCFG_HSMODE):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**CFIO Pad Configuration ODTUPDN (CFIOPADCFG_ODTUPDN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
19	0h RO	**CFIO Pad Configuration ODTEN (CFIOPADCFG_ODTEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
18	0h RO	**CFIO Pad Configuration ANALOGMUXEN (CFIOPADCFG_ANALOGMUXEN):** See CFIO HIP Interface for details on these control bit descriptions. These may be duplicates in the family settings register since these can be either Family or Pad signals and this is SoC specific. The superset is described here and register bits are implemented only for those configurations that are pad specific. Bits that aren't implemented or output of the CFIO are read only.
17:14	0h RW	**IO Standby State (IOSSTATE):** The I/O Standby State defines which state the pad should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled and RX drive 0 internally 2 = Drive 0 with RX disabled and RX drive 1 internally 3 = Drive 1 with RX disabled and RX drive 0 internally 4 = Drive 1 with RX disabled and RX drive 1 internally 5 = Drive 0 with RX enabled 6 = Drive 1 with RX enabled 7 = Hi-Z with RX drive 0 internally 8 = Hi-Z with RX drive 1 internally 9 = TX Disabled and RX Enabled (i.e. wake or interrupt) 15 = IO Standby signal is masked for this pad. In this mode, a pad operates as if IOStandby has not been asserted. Others = Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**TERM:** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0100: 20k PD 1100: 20k PU 1111: Native controller selected by Pad Mode controls the Termination. This field should be set to 1111b for the selected native function that supports dynamic termination override. Refer to Vol1, GPIO chapter, for more info. Others: Reserved **Notes**: 1. The 20K pull-up/pull-down can only be enabled as long as the toggle rate on the signal is no more than 300KHz. 2. If a reserved value is programmed, pad may malfunction. 3. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, PU/PD settings should be programmed first to ensure the input does not float momentarily
9:8	0h RW	**IO Standby Termination (IOSTERM):** IOSTerm defines the behaviour of the termination logic when the IO Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pullup and Pulldown 2 = Enable Pulldown 3 = Enable Pullup
7:0	58h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

33.5.31 Pad Configuration DW2 (PAD_CFG_DW2_GPP_R_0) — Offset 708h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 708h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:25	0h RO	**SoundWire Slew Control (sndwslewctrl) (SNDWSLEWCTRL):** 00 = Slow Slew Rate 01 = Middle Slew Rate 10 = Fast Slew Rate 11 = Fastest Slew Rate For iCDG buffers, this field is used to control the slew configuration, but extends beyond SoundWire to I2C, SDMMC and other applicable buffers. The setting may vary from one platform to another.
24	0h RO	**Bus Hold Enable (BUSHLDEN):** This feature uses the same build in pull-up/down resistor. In such, BIOS/FW needs to disable all pull-up/down to 'None' before enabling this feature. 1 = enable bus hold 0 = disable bus hold
23	0h RO	**Data Dependent Weak PU Control (DDPUCTRL):** 0 = normal I/O transmission mode. 1 = weak pull up configuration is overridden to disabled, when the raw RX pad state is 0 in output mode. During DFx mode like BSCAN, SCAN, HVM and etc, the DDPUCRTL shall be constrained to 0.
22	0h RO	**Analog Glitch Filter RX Pad State Select (ANALOGGFRXSEL):** Determine if the internal RX pad state should be subjected to analog glitch filter (implemented within the buffer) or not. This field only make sense when the buffer is configured as an input and is not disabled. 0 = Select non filtered RX pad state 1= Select filtered RX pad state. The mux to select filtered or non filtered RX pad state is implemented within the HIP family. During DFx mode like BSCAN, SCAN, HVM and etc, the AnalogGFRxSel shall be constrained to 0.
21:9	0h RO	**Reserved**
8	0h RO	**VCCIO selection (VCCIOSEL):** This bits is used to select VCCIO If the pad supports programmable VCCIO. The definition of high and low are implementation specific. 0: high voltage 1: low voltage

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Reserved**
4:1	0h RO	**Debounce duration (DEBOUNCE):** The debounce duration of value should be not less than 3. In other words, the value should not be any of 0, 1 and 2. The debounce time should be calculated as (2^debounce) * (glitch filter clock period) For example, when RTC clock (32 KHz) is used for glitch filter and debounce duration is set to 4b1011, the debounce time is (2 ^ 11) * (31.25 us) = 64ms
0	0h RO	**Debounce Enable (DEBEN):** This bit enables or disables the debouncer with the pad. 1 = Enable the debouncer of the pad 0 = Disable the debouncer of the pad

33.5.32 Pad Configuration DW3 (PAD_CFG_DW3_GPP_R_0) — Offset 70Ch

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 70Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

33.5.33 Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_1) — Offset 710h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_R_0, offset 700h.

33.5.34 Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_1) — Offset 714h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_R_0, offset 704h.

33.5.35 Pad Configuration DW2 (PAD_CFG_DW2_GPP_R_1) — Offset 718h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_R_0, offset 708h.

33.5.36 Pad Configuration DW3 (PAD_CFG_DW3_GPP_R_1) — Offset 71Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_R_0, offset 70Ch.

33.5.37 Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_2) — Offset 720h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_R_0, offset 700h.

33.5.38 Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_2) — Offset 724h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_R_0, offset 704h.

33.5.39 Pad Configuration DW2 (PAD_CFG_DW2_GPP_R_2) — Offset 728h

Refer to Register Field for detail

Type	Size	Offset	Default
MMIO	32 bit	FD690000h + 728h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:25	0h RO	**SoundWire Slew Control (sndwslewctrl) (SNDWSLEWCTRL):** 00 = Slow Slew Rate 01 = Middle Slew Rate 10 = Fast Slew Rate 11 = Fastest Slew Rate For iCDG buffers, this field is used to control the slew configuration, but extends beyond SoundWire to I2C, SDMMC and other applicable buffers. The setting may vary from one platform to another.
24	0h RO	**Bus Hold Enable (BUSHLDEN):** This feature uses the same build in pull-up/down resistor. In such, BIOS/FW needs to disable all pull-up/down to 'None' before enabling this feature. 1 = enable bus hold 0 = disable bus hold
23	0h RO	**Data Dependent Weak PU Control (DDPUCTRL):** 0 = normal I/O transmission mode. 1 = weak pull up configuration is overridden to disabled, when the raw RX pad state is 0 in output mode. During DFx mode like BSCAN, SCAN, HVM and etc, the DDPUCRTL shall be constrained to 0.
22	0h RO	**Analog Glitch Filter RX Pad State Select (ANALOGGFRXSEL):** Determine if the internal RX pad state should be subjected to analog glitch filter (implemented within the buffer) or not. This field only make sense when the buffer is configured as an input and is not disabled. 0 = Select non filtered RX pad state 1= Select filtered RX pad state. The mux to select filtered or non filtered RX pad state is implemented within the HIP family. During DFx mode like BSCAN, SCAN, HVM and etc, the AnalogGFRxSel shall be constrained to 0.
21:12	0h RO	**Reserved**
11	0h RO/V	**Pin-strap value (PINSTRAPVAL):** This bit reflects the pin-strap value.
10:9	0h RO	**Reserved**
8	0h RO	**VCCIO selection (VCCIOSEL):** This bits is used to select VCCIO If the pad supports programmable VCCIO. The definition of high and low are implementation specific. 0: high voltage 1: low voltage

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Reserved**
4:1	0h RO	**Debounce duration (DEBOUNCE):** The debounce duration of value should be not less than 3. In other words, the value should not be any of 0, 1 and 2. The debounce time should be calculated as (2^debounce) * (glitch filter clock period) For example, when RTC clock (32 KHz) is used for glitch filter and debounce duration is set to 4b1011, the debounce time is (2 ^ 11) * (31.25 us) = 64ms
0	0h RO	**Debounce Enable (DEBEN):** This bit enables or disables the debouncer with the pad. 1 = Enable the debouncer of the pad 0 = Disable the debouncer of the pad

33.5.40 Pad Configuration DW3 (PAD_CFG_DW3_GPP_R_2) — Offset 72Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_R_0, offset 70Ch.

33.5.41 Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_3) — Offset 730h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_R_0, offset 700h.

33.5.42 Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_3) — Offset 734h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_R_0, offset 704h.

33.5.43 Pad Configuration DW2 (PAD_CFG_DW2_GPP_R_3) — Offset 738h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_R_0, offset 708h.

33.5.44 Pad Configuration DW3 (PAD_CFG_DW3_GPP_R_3) — Offset 73Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_R_0, offset 70Ch.

33.5.45 Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_4) — Offset 740h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_R_0, offset 700h.

33.5.46 Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_4) — Offset 744h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_R_0, offset 704h.

33.5.47 Pad Configuration DW2 (PAD_CFG_DW2_GPP_R_4) — Offset 748h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_R_0, offset 708h.

33.5.48 Pad Configuration DW3 (PAD_CFG_DW3_GPP_R_4) — Offset 74Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_R_0, offset 70Ch.

33.5.49 Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_5) — Offset 750h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_R_0, offset 700h.

33.5.50 Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_5) — Offset 754h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_R_0, offset 704h.

33.5.51 Pad Configuration DW2 (PAD_CFG_DW2_GPP_R_5) — Offset 758h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_R_0, offset 708h.

33.5.52 Pad Configuration DW3 (PAD_CFG_DW3_GPP_R_5) — Offset 75Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_R_0, offset 70Ch.

33.5.53 Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_6) — Offset 760h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_R_0, offset 700h.

33.5.54 Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_6) — Offset 764h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_R_0, offset 704h.

33.5.55 Pad Configuration DW2 (PAD_CFG_DW2_GPP_R_6) — Offset 768h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_R_0, offset 708h.

33.5.56 Pad Configuration DW3 (PAD_CFG_DW3_GPP_R_6) — Offset 76Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_R_0, offset 70Ch.

33.5.57 Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_7) — Offset 770h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_R_0, offset 700h.

33.5.58 Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_7) — Offset 774h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_R_0, offset 704h.

33.5.59 Pad Configuration DW2 (PAD_CFG_DW2_GPP_R_7) — Offset 778h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_R_0, offset 708h.

33.5.60 Pad Configuration DW3 (PAD_CFG_DW3_GPP_R_7) — Offset 77Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_R_0, offset 70Ch.

33.5.61 Pad Configuration DW0 (PAD_CFG_DW0_SPI0_IO_2) — Offset 780h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_R_0, offset 700h.

33.5.62 Pad Configuration DW1 (PAD_CFG_DW1_SPI0_IO_2) — Offset 784h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_R_0, offset 704h.

33.5.63 Pad Configuration DW2 (PAD_CFG_DW2_SPI0_IO_2) — Offset 788h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_R_2, offset 728h.

33.5.64 Pad Configuration DW3 (PAD_CFG_DW3_SPI0_IO_2) — Offset 78Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_R_0, offset 70Ch.

33.5.65 Pad Configuration DW0 (PAD_CFG_DW0_SPI0_IO_3) — Offset 790h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_R_0, offset 700h.

33.5.66 Pad Configuration DW1 (PAD_CFG_DW1_SPI0_IO_3) — Offset 794h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_R_0, offset 704h.

33.5.67 Pad Configuration DW2 (PAD_CFG_DW2_SPI0_IO_3) — Offset 798h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_R_2, offset 728h.

33.5.68 Pad Configuration DW3 (PAD_CFG_DW3_SPI0_IO_3) — Offset 79Ch

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_R_0, offset 70Ch.

33.5.69 Pad Configuration DW0 (PAD_CFG_DW0_SPI0_MOSI_IO_0) — Offset 7A0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_R_0, offset 700h.

33.5.70 Pad Configuration DW1 (PAD_CFG_DW1_SPI0_MOSI_IO_0) — Offset 7A4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_R_0, offset 704h.

33.5.71 Pad Configuration DW2 (PAD_CFG_DW2_SPI0_MOSI_IO_0) — Offset 7A8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_R_2, offset 728h.

33.5.72 Pad Configuration DW3 (PAD_CFG_DW3_SPI0_MOSI_IO_0) — Offset 7ACh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_R_0, offset 70Ch.

33.5.73 Pad Configuration DW0 (PAD_CFG_DW0_SPI0_MISO_IO_1) — Offset 7B0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_R_0, offset 700h.

33.5.74 Pad Configuration DW1 (PAD_CFG_DW1_SPI0_MISO_IO_1) — Offset 7B4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_R_0, offset 704h.

33.5.75 Pad Configuration DW2 (PAD_CFG_DW2_SPI0_MISO_IO_1) — Offset 7B8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_R_0, offset 708h.

33.5.76 Pad Configuration DW3 (PAD_CFG_DW3_SPI0_MISO_IO_1) — Offset 7BCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_R_0, offset 70Ch.

33.5.77 Pad Configuration DW0 (PAD_CFG_DW0_SPI0_TPM_CSB) — Offset 7C0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_R_0, offset 700h.

33.5.78 Pad Configuration DW1 (PAD_CFG_DW1_SPI0_TPM_CSB) — Offset 7C4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_R_0, offset 704h.

33.5.79 Pad Configuration DW2 (PAD_CFG_DW2_SPI0_TPM_CSB) — Offset 7C8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_R_0, offset 708h.

33.5.80 Pad Configuration DW3 (PAD_CFG_DW3_SPI0_TPM_CSB) — Offset 7CCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_R_0, offset 70Ch.

33.5.81 Pad Configuration DW0 (PAD_CFG_DW0_SPI0_FLASH_0_CSB) — Offset 7D0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_R_0, offset 700h.

33.5.82 Pad Configuration DW1 (PAD_CFG_DW1_SPI0_FLASH_0_CSB) — Offset 7D4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_R_0, offset 704h.

33.5.83 Pad Configuration DW2 (PAD_CFG_DW2_SPI0_FLASH_0_CSB) — Offset 7D8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_R_0, offset 708h.

33.5.84 Pad Configuration DW3 (PAD_CFG_DW3_SPI0_FLASH_0_CSB) — Offset 7DCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_R_0, offset 70Ch.

33.5.85 Pad Configuration DW0 (PAD_CFG_DW0_SPI0_FLASH_1_CSB) — Offset 7E0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_R_0, offset 700h.

33.5.86 Pad Configuration DW1 (PAD_CFG_DW1_SPI0_FLASH_1_CSB) — Offset 7E4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_R_0, offset 704h.

33.5.87 Pad Configuration DW2 (PAD_CFG_DW2_SPI0_FLASH_1_CSB) — Offset 7E8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_R_0, offset 708h.

33.5.88 Pad Configuration DW3 (PAD_CFG_DW3_SPI0_FLASH_1_CSB) — Offset 7ECh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_R_0, offset 70Ch.

33.5.89 Pad Configuration DW0 (PAD_CFG_DW0_SPI0_CLK) — Offset 7F0h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW0_GPP_R_0, offset 700h.

33.5.90 Pad Configuration DW1 (PAD_CFG_DW1_SPI0_CLK) — Offset 7F4h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW1_GPP_R_0, offset 704h.

33.5.91 Pad Configuration DW2 (PAD_CFG_DW2_SPI0_CLK) — Offset 7F8h

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW2_GPP_R_0, offset 708h.

33.5.92 Pad Configuration DW3 (PAD_CFG_DW3_SPI0_CLK) — Offset 7FCh

Refer to Register Field for detail

Bit definitions are the same as PAD_CFG_DW3_GPP_R_0, offset 70Ch.

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34 High Precision Event Timer (HPET)

34.1 HPET Memory Mapped Registers

The timer registers are memory mapped directly (rather than indexed) to allow the CPU to access each register without having to use an index register. This ensures accesses are safe for multi-threaded environments. The timer register space is 1024 bytes. The registers are generally aligned on 64-bit boundaries to simplify implementation with IA64 processors. In the PCH, there are 4 possible memory address ranges beginning at 1) FED0_0000h, 2) FED0_1000h, 3) FED0_2000h, 4) FED0_3000h. The choice of address range should be selected by assigning the High Performance Event Timer Configuration (HPTC) register fields in the configuration space of the Primary to Sideband Bridge. All registers are implemented in the Primary power well, and all bits are reset by PLTRST#. Reads to reserved registers or bits will return a value of 0.
Behavorial Rules:
1. Software can read or write the various bytes in these registers using 32-bit or 64-bit accesses. Software must not attempt to read or write across register boundaries. For example, a 32-bit access should be to offset x0h, x4h, x8h, or xCh. 32-bit accesses should not be to 01h, 02h, 03h, 05h, 06h, 07h, 09h, 0Ah, 0Bh, 0Dh, 0Eh, or 0Fh. Any accesses to these offsets will result in an unexpected behavior, and may result in a Initiator abort. However, these accesses should not result in system hangs. 64-bit accesses can only be to x0h and must not cross 64-bit boundaries.
2. Software should not write to read-only registers.
3. Software should not expect any particular or consistent value when reading reserved registers or bits.

Table 34-1. Summary of HPET Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
FED000 00h	FED000 07h	General Capabilities and ID Register (GEN_CAP_ID)—Offset FED00000h	27BC86B8086A701h
FED000 10h	FED000 17h	General Config Register (GEN_CFG)—Offset FED00010h	0h
FED000 20h	FED000 27h	General Interrupt Status Register (GEN_INT_STS)—Offset FED00020h	0h
FED000F 0h	FED000F 7h	Main Counter Value (MAIN_CNTR)—Offset FED000F0h	0h
FED001 00h	FED001 07h	Timer n Config and Capabilities (TMRn_CNF_CAP)—Offset FED00100h	0h
FED001 08h	FED001 0Fh	Timer n Comparator Value (TMRn_CMP_VAL)—Offset FED00108h	FFFFFFFFFFFFFFFFh

34.1.1 General Capabilities and ID Register (GEN_CAP_ID)—Offset FED00000h

Access Method

Type: MEM Register
(Size: 64 bits)

Device:
Function:

Default: 27BC86B8086A701h

Bit Range	Default and Access	Field Name (ID): Description
63:32	27BC86Bh RO	**Main Counter Tick Period (COUNTER_CLK_PER_CAP):** This read-only field indicates the period at which the counter increments in femtoseconds (10^-15 seconds). The PCH HPET timers use a 24 MHz clock, which has a period of 41,666,667 femtoseconds. Therefore this register will always return 027BC86Bh when read.
31:16	8086h RO	**Vendor ID (VENDOR_ID_CAP):** These bits will return 8086h when read to reflect Intel as the vendor.
15	1h RO	**Legacy Rout Capable (LEG_RT_CAP):** This bit will always be 1 when read, indicating support for the Legacy Interrupt Rout.
14	0h RO	Reserved.
13	1h RO	**Counter Size (COUNT_SIZE_CAP):** This bit will return 1 when read to indicate support for 64-bit counters allowing 64 or 32-bit mode operation.
12:8	7h RO	**Number of Timers (NUM_TIM_CAP):** This value in this field will be 07h to indicate support for 8 timers in the timer block.
7:0	1h RO	**Revision ID (REV_ID):** This field indicates which revision of the function is implemented. Default value will be 01h.

34.1.2 General Config Register (GEN_CFG)—Offset FED00010h

Access Method

Type: MEM Register
(Size: 64 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
63:2	0h RO	Reserved.
1	0h RW	**Legacy Rout (LEG_RT_CNF):** If the ENABLE_CNF bit and the LEG_RT_CNF bit are both set, the interrupts will be routed as follows: • Timer 0 is routed to IRQ0 in 8259 or IRQ2 in the I/O APIC • Timer 1 is routed to IRQ8 in 8259 or IRQ8 in the I/O APIC • Timer 2-n is routed as per the routing in the timer n Configuration registers. • If the Legacy Replacement Rout bit is set, the individual routing bits for Timers 0 and 1 (APIC) will have no impact. • If the Legacy Replacement Rout bit is not set, the individual routing bits for each of the timers are used. • This bit will default to 0. BIOS can set it to 1 to enable the legacy replacement routing, or 0 to disable the legacy replacement routing.
0	0h RW	**Overall Enable (ENABLE_CNF):** This bit must be set to enable any of the timers to generate interrupts. If this bit is 0, then the main counter will halt (will not increment) and no interrupts will be caused by any of these timers. For level-triggered interrupts, if an interrupt is pending when the ENABLE_CNF bit is changed from 1 to 0, the interrupt status indications (in the various Txx_INT_STS bits) will not be cleared. Software must write to the Txx_INT_STS bits to clear the interrupts. NOTE: This bit will default to 0. BIOS can set it to 1 or 0.

34.1.3 General Interrupt Status Register (GEN_INT_STS)—Offset FED00020h

Access Method

Type: MEM Register
(Size: 64 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
63:8	0h RO	Reserved.
7	0h RW/1C	**Timer 7 Interrupt Active (T07_INT_STS):** Same functionality as Timer 0.
6	0h RW/1C	**Timer 6 Interrupt Active (T06_INT_STS):** Same functionality as Timer 0.
5	0h RW/1C	**Timer 5 Interrupt Active (T05_INT_STS):** Same functionality as Timer 0.
4	0h RW/1C	**Timer 4 Interrupt Active (T04_INT_STS):** Same functionality as Timer 0.
3	0h RW/1C	**Timer 3 Interrupt Active (T03_INT_STS):** Same functionality as Timer 0.

Bit Range	Default and Access	Field Name (ID): Description
2	0h RW/1C	**Timer 2 Interrupt Active (T02_INT_STS):** Same functionality as Timer 0.
1	0h RW/1C	**Timer 1 Interrupt Active (T01_INT_STS):** Same functionality as Timer 0.
0	0h RW/1C	**Timer 0 Interrupt Active (T00_INT_STS):** The functionality of this bit depends on whether the edge or level-triggered mode is used for this timer. (default = 0) If set to level-triggered mode: This bit will be set by hardware if the corresponding timer interrupt is active. Once the bit is set, it can be cleared by software writing a 1 to the same bit position. Writes of 0 to this bit will have no effect. If set to edge-triggered mode: This bit should be ignored by software. Software should always write 0 to this bit. NOTE: Defaults to 0. In edge triggered mode, this bit will always read as 0 and writes will have no effect.

34.1.4 Main Counter Value (MAIN_CNTR)—Offset FED000F0h

Software can read the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 0F0h or 0F4h. 64-bit accesses may only be done to 0F0h. Writes to this register should only be done while the counter is halted. Reads to this register return the current value of the main counter. If 32-bit software attempts to read a 64-bit counter, it should first halt the counter. Since this will delay the interrupts for all of the timers, this should be done only if the consequences are understood. It is strongly recommended that 32-bit software only operate the timer in 32-bit mode. Reads to this register are monotonic. No two consecutive reads will return the same value. The second of two reads will always return a larger value (unless the timer has rolled over to 0)

Access Method

Type: MEM Register (Size: 64 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
63:0	0h RW/V	**Counter Value (COUNTER_VAL):** Reads return the current value of the counter. Writes load the new value to the counter. NOTES: 1. Writes to this register should only be done while the counter is halted. 2. Reads to this register return the current value of the main counter. 3. 32-bit counters will always return 0 for the upper 32-bits of this register. 4. If 32-bit software attempts to read a 64-bit counter, it should first halt the counter. Since this will delay the interrupts for all of the timers, this should be done only if the consequences are understood. It is strongly recommended that 32-bit software only operate the timer in 32-bit mode. 5. Reads to this register are monotonic. No two consecutive reads will return the same value. The second of two reads will always return a larger value (unless the timer has rolled over to 0)

34.1.5 Timer n Config and Capabilities (TMRn_CNF_CAP)—Offset FED00100h

Timer 0: 100–107h,
Timer 1: 120–127h,
Timer 2: 140–147h,
Timer 3: 160–167h,
Timer 4: 180–187h,
Timer 5: 1A0–1A7h,
Timer 6: 1C0–1C7h,
Timer 7: 1E0–1E7h,
The letter n can be 0, 1, 2, 3, 4, 5, 6, or 7 referring to Timer 0, 1, 2, 3, 4, 5, 6, or 7.

Access Method

Type: MEM Register (Size: 64 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
63:4	0h RO	Reserved.
3	0h RW	**Timer 0 Type (TIMER0_TYPE_CNF):** Setting this bit to 1 enables the timer to generate a periodic interrupt if it is capable of doing so. If the TIMERn_PER_INT_CAP bit is 0, then this bit will always return 0 when read and writes will have no impact. For timer 0, this bit will be read/write, with default of 0. For timers 1-7, this bit will be read-only, with a fixed value of 0.
2:0	0h RO	Reserved.

34.1.6 Timer n Comparator Value (TMRn_CMP_VAL)—Offset FED00108h

Timer 0: 108h – 10Fh
Timer 1: 128h – 12Fh
Timer 2: 148h – 14Fh
Timer 3: 168h – 16Fh
Timer 4: 188h – 18Fh
Timer 5: 1A8h – 1AFh
Timer 6: 1C8h – 1CFh
Timer 7: 1E8h – 1EFh

Access Method

Type: MEM Register (Size: 64 bits)
Device:
Function:

Default: FFFFFFFFFFFFFFFFh

Bit Range	Default and Access	Field Name (ID): Description
63:0	FFFFFFFFF FFFFFFFh RW/V	**Timer 0 Comparator Value (TMR0_CMP_VAL):** If the timer is configured to non-periodic mode, when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). The value in this register does not change based on the interrupt being generated. If the timer is configured to periodic mode (supported only for Timer 0), when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). When this time out occurs, the value in this register is increased by the value last written to the register. For example, in periodic mode if the value written to the register is 0000123h: 1. An interrupt will be generated when the main counter reaches 00000123h. 2. The value in this register will then be adjusted by the hardware to 00000246h. 3. Another interrupt will be generated when the main counter reaches 00000246h. 4. The value in this register will then be adjusted by the hardware to 00000369h. As each periodic interrupt occurs, the value in this register will increment. When the incremented value is greater than the maximum value possible for this register (FFFFFFFFh for a 32-bit timer or FFFFFFFFFFFFFFFFh for a 64-bit timer), the value will wrap around through 0. For example, if the current value in a 32-bit timer is FFFF0000h and the last value written to this register is 20000, then after the next interrupt the value will change to 00010000h The default value for each timer is all 1s for the bits that are implemented. For example, a 32-bit timer will have a default value of 00000000FFFFFFFFh. A 64-bit timer will have a default value of FFFFFFFFFFFFFFFFh. Software can read or write the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 1x8h or 1xCh. 64-bit accesses may only be done to 1x8h. Comparator value. Timer 0 is 64-bits wide. Timers 1-7 are 32-bits wide.

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35 Integrated Clock

35.1 Integrated Clock Configuration Registers

Table 35-1. Summary of Integrated Clock Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
22E4h	22E7h	SRCCLKREQ Config (src_muxsel1)—Offset 22E4h	6543210h

35.1.1 SRCCLKREQ Config (src_muxsel1)—Offset 22E4h

Access Method

Type:MSG Register
(Size: 32 bits)

Device:
Function:

Default:6543210h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:24	6h RW	**SRCCLKREQ Select For CLKOUT_PCIE6 (muxsel_src6_cg_en_3_0):** Select version of SRCCLKREQ# for dynamic control of the output CLKOUT_PCIE6 0000: SRCCLKREQ0# controls CLKOUT_PCIE6 (default) 0001: SRCCLKREQ1# controls CLKOUT_PCIE6 0010: SRCCLKREQ2# controls CLKOUT_PCIE6 0011: SRCCLKREQ3# controls CLKOUT_PCIE6 0100: SRCCLKREQ4# controls CLKOUT_PCIE6 0101: SRCCLKREQ5# controls CLKOUT_PCIE6 0110: SRCCLKREQ6# controls CLKOUT_PCIE6 0111-1111: Reserved
23:20	5h RW	**SRCCLKREQ Select For CLKOUT_PCIE5 (muxsel_src5_cg_en_3_0):** Select version of SRCCLKREQ# for dynamic control of the output CLKOUT_PCIE5 0000: SRCCLKREQ0# controls CLKOUT_PCIE5 (default) 0001: SRCCLKREQ1# controls CLKOUT_PCIE5 0010: SRCCLKREQ2# controls CLKOUT_PCIE5 0011: SRCCLKREQ3# controls CLKOUT_PCIE5 0100: SRCCLKREQ4# controls CLKOUT_PCIE5 0101: SRCCLKREQ5# controls CLKOUT_PCIE5 0110: SRCCLKREQ6# controls CLKOUT_PCIE5 0111-1111: Reserved
19:16	4h RW	**SRCCLKREQ Select For CLKOUT_PCIE4 (muxsel_src4_cg_en_3_0):** Select version of SRCCLKREQ# for dynamic control of the output CLKOUT_PCIE4 0000: SRCCLKREQ0# controls CLKOUT_PCIE4 (default) 0001: SRCCLKREQ1# controls CLKOUT_PCIE4 0010: SRCCLKREQ2# controls CLKOUT_PCIE4 0011: SRCCLKREQ3# controls CLKOUT_PCIE4 0100: SRCCLKREQ4# controls CLKOUT_PCIE4 0101: SRCCLKREQ5# controls CLKOUT_PCIE4 0110: SRCCLKREQ6# controls CLKOUT_PCIE4 0111-1111: Reserved

Bit Range	Default & Access	Field Name (ID): Description
15:12	3h RW	**SRCCLKREQ Select For CLKOUT_PCIE3 (muxsel_src3_cg_en_3_0):** Select version of SRCCLKREQ# for dynamic control of the output CLKOUT_PCIE3 0000: SRCCLKREQ0# controls CLKOUT_PCIE3 (default) 0001: SRCCLKREQ1# controls CLKOUT_PCIE3 0010: SRCCLKREQ2# controls CLKOUT_PCIE3 0011: SRCCLKREQ3# controls CLKOUT_PCIE3 0100: SRCCLKREQ4# controls CLKOUT_PCIE3 0101: SRCCLKREQ5# controls CLKOUT_PCIE3 0110: SRCCLKREQ6# controls CLKOUT_PCIE3 0111-1111: Reserved
11:8	2h RW	**SRCCLKREQ Select For CLKOUT_PCIE2 (muxsel_src2_cg_en_3_0):** Select version of SRCCLKREQ# for dynamic control of the output CLKOUT_PCIE2 0000: SRCCLKREQ0# controls CLKOUT_PCIE2 (default) 0001: SRCCLKREQ1# controls CLKOUT_PCIE2 0010: SRCCLKREQ2# controls CLKOUT_PCIE2 0011: SRCCLKREQ3# controls CLKOUT_PCIE2 0100: SRCCLKREQ4# controls CLKOUT_PCIE2 0101: SRCCLKREQ5# controls CLKOUT_PCIE2 0110: SRCCLKREQ6# controls CLKOUT_PCIE2 0111-1111: Reserved
7:4	1h RW	**SRCCLKREQ Select For CLKOUT_PCIE1 (muxsel_src1_cg_en_3_0):** Select version of SRCCLKREQ# for dynamic control of the output CLKOUT_PCIE1 0000: SRCCLKREQ0# controls CLKOUT_PCIE1 (default) 0001: SRCCLKREQ1# controls CLKOUT_PCIE1 0010: SRCCLKREQ2# controls CLKOUT_PCIE1 0011: SRCCLKREQ3# controls CLKOUT_PCIE1 0100: SRCCLKREQ4# controls CLKOUT_PCIE1 0101: SRCCLKREQ5# controls CLKOUT_PCIE1 0110: SRCCLKREQ6# controls CLKOUT_PCIE1 0111-1111: Reserved
3:0	0h RW	**SRCCLKREQ Select For CLKOUT_PCIE0 (muxsel_src0_cg_en_3_0):** Select version of SRCCLKREQ# for dynamic control of the output CLKOUT_PCIE0 0000: SRCCLKREQ0# controls CLKOUT_PCIE0 (default) 0001: SRCCLKREQ1# controls CLKOUT_PCIE0 0010: SRCCLKREQ2# controls CLKOUT_PCIE0 0011: SRCCLKREQ3# controls CLKOUT_PCIE0 0100: SRCCLKREQ4# controls CLKOUT_PCIE0 0101: SRCCLKREQ5# controls CLKOUT_PCIE0 0110: SRCCLKREQ6# controls CLKOUT_PCIE0 0111-1111: Reserved

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36 Interrupt

36.1 Interrupt Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
20h	20h	Initiator Initialization Command Word 1 (MICW1)—Offset 20h	11h
20h	20h	Initiator Operational Control Word 2 (MOCW2)—Offset 20h	0h
20h	20h	Initiator Operational Control Word 3 (MOCW3)—Offset 20h	8h
21h	21h	Initiator Initialization Command Word 2 (MICW2)—Offset 21h	0h
21h	21h	Initiator Initialization Command Word 3 (MICW3)—Offset 21h	7h
21h	21h	Initiator Initialization Command Word 4 (MICW4)—Offset 21h	0h
21h	21h	Initiator Operational Control Word 1 (MOCW1)—Offset 21h	0h
A0h	A0h	Target Initialization Command Word 1 (SICW1)—Offset A0h	11h
A0h	A0h	Target Operational Control Word 2 (SOCW2)—Offset A0h	0h
A0h	A0h	Target Operational Control Word 3 (SOCW3)—Offset A0h	8h
A1h	A1h	Target Initialization Command Word 2 (SICW2)—Offset A1h	0h
A1h	A1h	Target Initialization Command Word 3 (SICW3)—Offset A1h	7h
A1h	A1h	Target Initialization Command Word 4 (SICW4)—Offset A1h	0h
A1h	A1h	Target Operational Control Word 1 (SOCW1)—Offset A1h	0h
4D0h	4D0h	Initiator Edge/Level Control (ELCR1)—Offset 4D0h	0h
4D1h	4D1h	Target Edge/Level Control (ELCR2)—Offset 4D1h	0h

36.1.1 Initiator Initialization Command Word 1 (MICW1)—Offset 20h

A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs:
1. The Interrupt Mask register is cleared.
2. IRQ7 input is assigned priority 7.
3. The Target mode address is set to 7.
4. Special Mask Mode is cleared and Status Read is set to IRR.

Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Access Method

Type: IO Register (Size: 8 bits)

Device:
Function:

Default: 11h

Bit Range	Default and Access	Field Name (ID): Description
7:5	0h WO	**ICW/OCW select (ICW_OCW_SLT1):** These bits are MCS-85 specific, and not needed. Should be programmed to 000
4	1h WO	**ICW/OCW select (ICW_OCW_SLT2):** This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	0h WO	**Edge/Level Bank Select (LTIM):** Disabled. Replaced by the edge/level triggered control registers (ELCR).
2	0h WO	**ADI-IGNORED (ADI):** Ignored for PCH. Should be programmed to 0.
1	0h WO	**Single or Cascade (SNGL):** Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	1h WO	**ICW4 Write Required (IC4):** This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

36.1.2 Initiator Operational Control Word 2 (MOCW2)—Offset 20h

*address should be 20h
Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:5	0h WO	**Rotate and EOI Codes (REOI):** R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations is listed above under the bit definition. 000 Rotate in Auto EOI Mode (Clear) 001 Non-specific EOI command 010 No Operation 011 *Specific EOI Command 100 Rotate in Auto EOI Mode (Set) 101 Rotate on Non-Specific EOI Command 110 *Set Priority Command 111 *Rotate on Specific EOI Command *L0 - L2 Are Used
4:3	0h WO	**OCW2 Select (O2S):** When selecting OCW2, bits 4:3 = 00
2:0	0h WO	**Interrupt Level Select (L2, L1, L0) (ILSLT):** L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined above, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function, programming L2, L1 and L0 to 0 is sufficient in this case.

36.1.3 Initiator Operational Control Word 3 (MOCW3)—Offset 20h

*address should be 20h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
7	0h RO	Reserved.
6	0h WO	**Special Mask Mode (SMM):** If this bit is set, the Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/ disabling of the other channel's mask bits. Bit 6, the ESMM bit, must be set for this bit to have any meaning.
5	0h WO	**Enable Special Mask Mode (ESMM):** When set, the SMM bit is enabled to set or reset the Special Mask Mode. When cleared, the SMM bit becomes a "do not care".
4:3	1h WO	**OCW3 Select (O3S):** When selecting OCW3, bits 4:3 = 01
2	0h WO	**Poll Mode Command (PMC):** When cleared, poll command is not issued. When set, the next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.
1:0	0h WO	**Register Read Command (RRC):** These bits provide control for reading the ISR and Interrupt IRR. When bit 1=0, bit 0 will not affect the register read selection. Following ICW initialization, the default OCW3 port address read will be "read IRR". To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. Value Command 00 No Action 01 No Action 10 Read IRQ Register 11 Read IS Register

36.1.4 Initiator Initialization Command Word 2 (MICW2)—Offset 21h

ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the CPU to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the Initiator controller and 70h for the Target controller.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:3	0h WO	**Interrupt Vector Base Address (IVBA):** Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.
2:0	0h WO	**Interrupt Request Level (IRL):** When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code: Code Initiator Interrupt Target Interrupt 000 IRQ0 IRQ8 001 IRQ1 IRQ9 010 IRQ2 IRQ10 011 IRQ3 IRQ11 100 IRQ4 IRQ12 101 IRQ5 IRQ13 110 IRQ6 IRQ14 111 IRQ7 IRQ15

36.1.5 Initiator Initialization Command Word 3 (MICW3)—Offset 21h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 7h

Bit Range	Default and Access	Field Name (ID): Description
7:3	0h WO	**MICW3 [7:3] (MICW3_7_3):** These bits must be programmed to zero.
2	1h WO	**Cascaded Controller Connection (CCC):** This bit must always be programmed to a 1 to indicate the Target controller for interrupts 8 - 15 is cascaded on IRQ2.
1:0	3h WO	**MICW [1:0] (MICW3_1_0):** These bits must be programmed to zero.

36.1.6 Initiator Initialization Command Word 4 (MICW4)—Offset 21h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:5	0h RO	Reserved.
4	0h WO	**Special Fully Nested Mode (SFNM):** Should normally be disabled by writing a 0 to this bit. If SFNM=1, the special fully nested mode is programmed.
3	0h WO	**Buffered Mode (BUF):** Must be cleared for non-buffered mode. Writing 1 will result in undefined behavior.
2	0h WO	**Initiator/Target in Buffered Mode (MSBM):** Not used. Should always be programmed to 0.
1	0h WO	**Automatic End of Interrupt (AEOI):** This bit should normally be programmed to 0. This is the normal end of interrupt. If this bit is 1, the automatic end of interrupt mode is programmed.
0	0h WO	**Microprocessor Mode (MM):** This bit must be written to 1 to indicate that the controller is operating in an Intel Architecture-based system. Writing 0 will result in undefined behavior.1

36.1.7 Initiator Operational Control Word 1 (MOCW1)—Offset 21h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**Interrupt Request Mask (IRM):** When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests will again be accepted by the controller. Masking IRQ2 on the Initiator controller will also mask the interrupt requests from the Target controller.

36.1.8 Target Initialization Command Word 1 (SICW1)—Offset A0h

A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs:
1. The Interrupt Mask register is cleared.
2. IRQ7 input is assigned priority 7.
3. The Target mode address is set to 7.
4. Special Mask Mode is cleared and Status Read is set to IRR.
Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 11h

Bit Range	Default and Access	Field Name (ID): Description
7:5	0h WO	**ICW/OCW select (ICW_OCW_SLT1):** These bits are MCS-85 specific, and not needed. Should be programmed to 000
4	1h WO	**ICW/OCW select (ICW_OCW_SLT2):** This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	0h WO	**Edge/Level Bank Select (LTIM):** Disabled. Replaced by the edge/level triggered control registers (ELCR).
2	0h WO	**ADI-IGNORED (ADI):** Ignored for PCH. Should be programmed to 0.
1	0h WO	**Single or Cascade (SNGL):** Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	1h WO	**ICW4 Write Required (IC4):** This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

36.1.9 Target Operational Control Word 2 (SOCW2)—Offset A0h

*address should be A0h
Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:5	0h WO	**Rotate and EOI Codes (REOI):** R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations is listed above under the bit definition. 000 Rotate in Auto EOI Mode (Clear) 001 Non-specific EOI command 010 No Operation 011 *Specific EOI Command 100 Rotate in Auto EOI Mode (Set) 101 Rotate on Non-Specific EOI Command 110 *Set Priority Command 111 *Rotate on Specific EOI Command *L0 - L2 Are Used
4:3	0h WO	**OCW2 Select (O2S):** When selecting OCW2, bits 4:3 = 00
2:0	0h WO	**Interrupt Level Select (L2, L1, L0) (ILSLT):** L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined above, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function, programming L2, L1 and L0 to 0 is sufficient in this case.

36.1.10 Target Operational Control Word 3 (SOCW3)—Offset A0h

*address should be A0h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
7	0h RO	Reserved.
6	0h WO	**Special Mask Mode (SMM):** If this bit is set, the Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/ disabling of the other channel's mask bits. Bit 6, the ESMM bit, must be set for this bit to have any meaning.
5	0h WO	**Enable Special Mask Mode (ESMM):** When set, the SMM bit is enabled to set or reset the Special Mask Mode. When cleared, the SMM bit becomes a "do not care".
4:3	1h WO	**OCW3 Select (O3S):** When selecting OCW3, bits 4:3 = 01
2	0h WO	**Poll Mode Command (PMC):** When cleared, poll command is not issued. When set, the next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.
1:0	0h WO	**Register Read Command (RRC):** These bits provide control for reading the ISR and Interrupt IRR. When bit 1=0, bit 0 will not affect the register read selection. Following ICW initialization, the default OCW3 port address read will be "read IRR". To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. Value Command 00 No Action 01 No Action 10 Read IRQ Register 11 Read IS Register

36.1.11 Target Initialization Command Word 2 (SICW2)—Offset A1h

ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the CPU to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the Initiator controller and 70h for the Target controller.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:3	0h WO	**Interrupt Vector Base Address (IVBA):** Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.
2:0	0h WO	**Interrupt Request Level (IRL):** When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code: Code Initiator Interrupt Target Interrupt 000 IRQ0 IRQ8 001 IRQ1 IRQ9 010 IRQ2 IRQ10 011 IRQ3 IRQ11 100 IRQ4 IRQ12 101 IRQ5 IRQ13 110 IRQ6 IRQ14 111 IRQ7 IRQ15

36.1.12 Target Initialization Command Word 3 (SICW3)—Offset A1h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 7h

Bit Range	Default and Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2:0	7h WO	**Target Identification Code (SIC):** This field must be programmed to 02h to match the code broadcast by the Initiator controller during the INTA# sequence.

36.1.13 Target Initialization Command Word 4 (SICW4)—Offset A1h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:5	0h RO	Reserved.
4	0h WO	**Special Fully Nested Mode (SFNM):** Should normally be disabled by writing a 0 to this bit. If SFNM=1, the special fully nested mode is programmed.
3	0h WO	**Buffered Mode (BUF):** Must be cleared for non-buffered mode. Writing 1 will result in undefined behavior.
2	0h WO	**Initiator/Target in Buffered Mode (MSBM):** Not used. Should always be programmed to 0.
1	0h WO	**Automatic End of Interrupt (AEOI):** This bit should normally be programmed to 0. This is the normal end of interrupt. If this bit is 1, the automatic end of interrupt mode is programmed.
0	0h WO	**Microprocessor Mode (MM):** This bit must be written to 1 to indicate that the controller is operating in an Intel Architecture-based system. Writing 0 will result in undefined behavior.1

36.1.14 Target Operational Control Word 1 (SOCW1)—Offset A1h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**Interrupt Request Mask (IRM):** When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests will again be accepted by the controller. Masking IRQ2 on the Initiator controller will also mask the interrupt requests from the Target controller.

36.1.15 Initiator Edge/Level Control (ELCR1)—Offset 4D0h

Initiator Edge/Level Control Register

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:3	0h RW	**Edge Level Control (ELC_7_3):** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level.
2:0	0h RO	Reserved.

36.1.16 Target Edge/Level Control (ELCR2)—Offset 4D1h

Target Edge/Level Control Register

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:6	0h RW	**Edge Level Control (ELC_15_14):** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. Bit 7 applies to IRQ15, and bit 6 to IRQ14.
5	0h RW	**Edge Level Control (ELC_13):** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. This bit applies to IRQ13.
4:1	0h RW	**Edge Level Control (ELC_12_9):** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. Bit 4 applies to IRQ12, bit 3 to IRQ11, bit 2 to IRQ10, and bit 1 to IRQ9.
0	0h RO	Reserved.

36.2 Interrupt PCR Registers

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3100h	3100h	PIRQA Routing Control (PARC)—Offset 3100h	80h
3101h	3101h	PIRQB Routing Control (PBRC)—Offset 3101h	80h
3102h	3102h	PIRQC Routing Control (PCRC)—Offset 3102h	80h
3103h	3103h	PIRQD Routing Control (PDRC)—Offset 3103h	80h
3104h	3104h	PIRQE Routing Control (PERC)—Offset 3104h	80h
3105h	3105h	PIRQF Routing Control (PFRC)—Offset 3105h	80h
3106h	3106h	PIRQG Routing Control (PGRC)—Offset 3106h	80h
3107h	3107h	PIRQH Routing Control (PHRC)—Offset 3107h	80h
3140h	3141h	PCI Interrupt Route 0 (PIR0)—Offset 3140h	3210h
3142h	3143h	PCI Interrupt Route 1 (PIR1)—Offset 3142h	0h
3144h	3145h	PCI Interrupt Route 2 (PIR2)—Offset 3144h	0h
3146h	3147h	PCI Interrupt Route 3 (PIR3)—Offset 3146h	0h
3148h	3149h	PCI Interrupt Route 4 (PIR4)—Offset 3148h	0h
314Ah	314Bh	PCI Interrupt Route 5 (PIR5)—Offset 314Ah	0h
31FCh	31FFh	General Interrupt Control (GIC)—Offset 31FCh	0h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3200h	3203h	Interrupt Polarity Control 0 (IPC0)—Offset 3200h	FF0000h
3204h	3207h	Interrupt Polarity Control 1 (IPC1)—Offset 3204h	0h
3208h	320Bh	Interrupt Polarity Control 2 (IPC2)—Offset 3208h	0h
320Ch	320Fh	Interrupt Polarity Control 3 (IPC3)—Offset 320Ch	0h
3300h	3303h	ITSS Power Reduction Control (ITSSPRC)—Offset 3300h	0h
3334h	3335h	Initiator Message Control (MMC)—Offset 3334h	0h

36.2.1 PIRQA Routing Control (PARC)—Offset 3100h

PIRQA Routing Control Register

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RW	**Interrupt Routing Enable (REN):** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	0h RO	Reserved.
3:0	0h RW	**IRQ Routing (IR):** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

36.2.2 PIRQB Routing Control (PBRC)—Offset 3101h

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RW	**Interrupt Routing Enable (REN):** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	0h RO	Reserved.
3:0	0h RW	**IRQ Routing (IR):** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

36.2.3 PIRQC Routing Control (PCRC)—Offset 3102h

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RW	**Interrupt Routing Enable (REN):** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	0h RO	Reserved.
3:0	0h RW	**IRQ Routing (IR):** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

36.2.4 PIRQD Routing Control (PDRC)—Offset 3103h

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RW	**Interrupt Routing Enable (REN):** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	0h RO	Reserved.
3:0	0h RW	**IRQ Routing (IR):** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

36.2.5 PIRQE Routing Control (PERC)—Offset 3104h

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RW	**Interrupt Routing Enable (REN):** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	0h RO	Reserved.
3:0	0h RW	**IRQ Routing (IR):** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

36.2.6 PIRQF Routing Control (PFRC)—Offset 3105h

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RW	**Interrupt Routing Enable (REN):** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	0h RO	Reserved.
3:0	0h RW	**IRQ Routing (IR):** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

36.2.7 PIRQG Routing Control (PGRC)—Offset 3106h

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RW	**Interrupt Routing Enable (REN):** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	0h RO	Reserved.
3:0	0h RW	**IRQ Routing (IR):** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

36.2.8 PIRQH Routing Control (PHRC)—Offset 3107h

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RW	**Interrupt Routing Enable (REN):** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	0h RO	Reserved.
3:0	0h RW	**IRQ Routing (IR):** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

36.2.9 PCI Interrupt Route 0 (PIR0)—Offset 3140h

This register applies to Device 31 functions.

Access Method

Type: MSG Register
(Size: 16 bits)

Device:
Function:

Default: 3210h

Bit Range	Default and Access	Field Name (ID): Description
15	0h RO	Reserved.
14:12	3h RW	**Interrupt D Pin Route (IDR):** Indicates which PIRQ in PCH is connected to the INTD# pin reported for device 31 functions: Bits Pin Bits Pin 0h PIRQA# 4h PIRQE# 1h PIRQB# 5h PIRQF# 2h PIRQC# 6h PIRQG# 3h PIRQD# 7h PIRQH#
11	0h RO	Reserved.
10:8	2h RW	**Interrupt C Pin Route (ICR):** Refer the IDR description. This field applies to INTC#
7	0h RO	Reserved.
6:4	1h RW	**Interrupt B Pin Route (IBR):** Refer the IDR description. This field applies to INTB#.
3	0h RO	Reserved.
2:0	0h RW	**Interrupt A Pin Route (IAR):** Refer the IDR description. This field applies to INTA#.

36.2.10 PCI Interrupt Route 1 (PIR1)—Offset 3142h

Same definition as PIR0, except this register applies to Device 29 functions.

36.2.11 PCI Interrupt Route 2 (PIR2)—Offset 3144h

Same definition as PIR0, except this register applies to Device 28 functions.

36.2.12 PCI Interrupt Route 3 (PIR3)—Offset 3146h

Same definition as PIR0, except this register applies to Device 23 functions.

36.2.13 PCI Interrupt Route 4 (PIR4)—Offset 3148h

Same definition as PIR0, except this register applies to Device 22 functions.

36.2.14 PCI Interrupt Route 5 (PIR5)—Offset 314Ah

Same definition as PIR0, except this register applies to Device 20 and 18 functions.

36.2.15 General Interrupt Control (GIC)—Offset 31FCh

Note: FEC10000h - FEC3FFFFh is allocated to PCIe when Port I/OxApic Enable (PAE) bit is set.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW	**Alternate Access Mode Enable (AME):** When set, read only registers can be written, and write only registers can be read.
16	0h RW	**Shutdown Policy Select (SDPS):** When cleared (default) the PCH will update INIT# in response to the shutdown Vendor Defined Message (VDM). When set to 1, PCH will treat the shutdown VDM similar to receiving a CF9h I/O write, and will drive PLTRST# active. This register is reset any time PLTRST# asserts.
15:9	0h RW	**MAX_IRQ_ENTRY_SIZE (MAXIRQSIZE):** This field indicates the size of the IOAPIC entry. The default size is 120 entries. 0000000: 120 entry size 0000001: 24 entry size (Legacy mode) 0000010 - 1111111: Reserved
8:1	0h RO	Reserved.
0	0h RO/P	**CPU Shutdown Status (CPUSDSTS):** This bit is set to 1 if the CPU sends the Shutdown Special cycle message. The Shutdown Message is recognized as an INIT# event if the Shutdown Policy Select = 0, else PCH shall treat the Shutodwn Special cycle as a request for CF9 Hard Reset. This is a sticky Read Only bit that is only reset by a loss of core power.

36.2.16 Interrupt Polarity Control 0 (IPC0)—Offset 3200h

Interrupt Polarity Control 0 Register

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: FF0000h

Bit Range	Default and Access	Field Name (ID): Description
31:0	FF0000h RW	**IRQ 31-0 Active High Polarity Disable (IPC0_IRQxAHPOLDIS):** When set to 1, the interrupt polarity associated with IRQ31 down to IRQ0 is inverted to appear as Active Low to IOAPIC. When set to 0, the interrupt is appears as Active High to IOAPIC.

36.2.17 Interrupt Polarity Control 1 (IPC1)—Offset 3204h

Interrupt Polarity Control 1 Register

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**IRQ 63-32 Active High Polarity Disable (IPC1_IRQAHPOLDIS):** When set to 1, the interrupt polarity associated with IRQ63 down to IRQ32 is inverted to appear as Active Low to IOAPIC. When set to 0, the interrupt is appears as Active High to IOAPIC.

36.2.18 Interrupt Polarity Control 2 (IPC2)—Offset 3208h

Interrupt Polarity Control 2 Register

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**IRQ 95-64 Active High Polarity Disable (IPC2_IRQAHPOLDIS):** When set to 1, the interrupt polarity associated with IRQ95 down to IRQ64 is inverted to appear as Active Low to IOAPIC. When set to 0, the interrupt is appears as Active High to IOAPIC.

36.2.19 Interrupt Polarity Control 3 (IPC3)—Offset 320Ch

Interrupt Polarity Control 3 Register

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:0	0h RW	**IRQ 119-96 Active High Polarity Disable (IPC3_IRQAHPOLDIS):** When set to 1, the interrupt polarity associated with IRQ119 down to IRQ96 is inverted to appear as Active Low to IOAPIC. When set to 0, the interrupt is appears as Active High to IOAPIC.

36.2.20 ITSS Power Reduction Control (ITSSPRC)—Offset 3300h

Power controls for the entire interrupt and timer subsystem.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	0h RW	**HPET Dynamic Clock Gating Enable (HPETDCGE):** When set, the HPET enables dynamic clock gating.
2	0h RW	**8254 Static Clock Gating Enable (CGE8254):** When set, the 8254 timer is disabled statically. This bit shall be set by BIOS if the 8254 feature is not needed in the system or before BIOS hands off the system that supports C11. Normal operation of 8254 requires this bit to 0.
1	0h RW	**Sideband Dynamic Clock Gating Enable (SBDCGE):** Setting this bit will enable all dynamic clock gating of the Sideband Clock domain.
0	0h RW	**PCI Dynamic Clock Gating Enable (PCIDCGE):** Setting this bit will enable dynamic clock gating for the Interrupt and Timer Sub System Core Logic.

36.2.21 Initiator Message Control (MMC)—Offset 3334h

Initiator Message Control Register

Access Method

Type: MSG Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:1	0h RO	Reserved.
0	0h RW/V	**Initiator Message Enable (MSTRMSG_EN):** When set, allows Interrupt and Timer Subsystem (ITSS) to release any pending/in progress IOAPIC memory write, HPET memory write, virtual wire event or error messages to the IO frabic. When cleared, ITSS prevents these messages from being issued to the IO frabic.

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37 Real Time Clock (RTC)

37.1 FRTC IO INDEX REG Registers

RTC IO Index Registers Port 70 and 71h

Table 37-1. Summary of RTC IO INDEX REG Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
70h	70h	RTC Index Register (INDEX)—Offset 70h	0h
71h	71h	RTC Target Register (TARGET)—Offset 71h	0h

37.1.1 RTC Index Register (INDEX)—Offset 70h

This 8-bit register selects which indirect register appears in the target register to be manipulated by software. Software will program this register to select the desired RTC indexed register.

Access Method

Type: MSG Register (Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**Index Register (INDEX):** Index Register for RTC

37.1.2 RTC Target Register (TARGET)—Offset 71h

This 8-bit register specifies the data to be read or written to the register pointed to by the INDEX register.

Access Method

Type: MSG Register (Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW/V	**RTC Target Register (TARGET):** RTC Target Register for RTC

37.2 RTC Indexed Registers Summary

The RTC contains two sets of indexed registers that are accessed using the two separate Index and Target registers (70h/71h or 72h/73h), as shown in the following table:

RTC (Standard) RAM Bank
Index Name
00h Seconds
01h Seconds Alarm
02h Minutes
03h Minutes Alarm
04h Hours
05h Hours Alarm
06h Day of Week
07h Day of Month
08h Month
09h Year
0Ah Register A
0Bh Register B
0Ch Register C
0Dh Register D
0Eh – 7Fh 114 Bytes of User RAM

Table 37-2. Summary of RTC Indexed Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	0h	Seconds Value (Sec)—Offset 0h	Xh
1h	1h	Seconds Alarm (Sec_Alarm)—Offset 1h	Xh
2h	2h	Minutes Value (Minutes)—Offset 2h	Xh
3h	3h	Minutes Alarm (Minutes_Alarm)—Offset 3h	Xh
4h	4h	Hours Value (Hours)—Offset 4h	Xh
5h	5h	Hours Alarm (Hours_Alarm)—Offset 5h	Xh
6h	6h	Day Of Week (Day_of_Week)—Offset 6h	Xh
7h	7h	Day Of Month (Day_of_Month)—Offset 7h	Xh
8h	8h	Month Value (Month)—Offset 8h	Xh
9h	9h	Year Value (Year)—Offset 9h	Xh
Ah	Ah	Register A (RTC_REGA)—Offset Ah	0h
Bh	Bh	Register B General Configuration (Register_B)—Offset Bh	10000XXX
Ch	Ch	Register C Flag Register (Register_C)—Offset Ch	0h
Dh	Dh	Register D Flag Register (Register_D)—Offset Dh	10XXXXXX
Eh	Eh	114 Bytes Of Lower User RAM (Register_E)—Offset Eh	Xh
80h	80h	128 Bytes Of Upper User RAM (Register_80)—Offset 80h	Xh

37.2.1 Seconds Value (Sec)—Offset 0h

RTC Index: 00h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current time second

37.2.2 Seconds Alarm (Sec_Alarm)—Offset 1h

RTC Index: 01h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores Seconds Alarm

37.2.3 Minutes Value (Minutes)—Offset 2h

RTC Index: 02h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current time Minutes

37.2.4 Minutes Alarm (Minutes_Alarm)—Offset 3h

RTC Index: 03h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores Alarm Minutes

37.2.5 Hours Value (Hours)—Offset 4h

RTC Index: 04h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current time Hours

37.2.6 Hours Alarm (Hours_Alarm)—Offset 5h

RTC Index: 05h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores Alarm Hours

37.2.7 Day Of Week (Day_of_Week)—Offset 6h

RTC Index: 06h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current Day of Week

37.2.8 Day Of Month (Day_of_Month)—Offset 7h

RTC Index: 07h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current Day of Month

37.2.9 Month Value (Month)—Offset 8h

RTC Index: 08h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current Month

37.2.10 Year Value (Year)—Offset 9h

RTC Index: 09h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current Year

37.2.11 Register A (RTC_REGA)—Offset Ah

This register is used for general configuration of the RTC functions. None of the bits are affected by RSMRST# or any other reset signal.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7	0h RO/V	**UPDATE IN PROGRESS (UIP):** This bit may be monitored as a status flag. 0 = Update cycle will not start for at least 488 micro-seconds. The time, calendar, and alarm information in RAM is always available when the UIP bit is 0. 1 = The update is soon to occur or is in progress.
6:0	0h RO	Reserved.

37.2.12 Register B General Configuration (Register_B)—Offset Bh

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RW	**Update Cycle Inhibit (SET):** Enables/Inhibits the update cycles. 0 = Update cycle occurs normally once each second. 1 = A current update cycle will abort and subsequent update cycles will not occur until SET is returned to zero. When set is one, the BIOS may initialize time and calendar bytes safely. This bit is not affected by RSMRST# nor any other reset signal. Note: Software must ensure this bit is at least transitioned from '1' to '0' once whenever the RTC coin battery is inserted. This is to ensure that the internal RTC time updates occur properly.
6	0h RW	**Periodic Interrupt Enable (PIE):** 0 = Disabled. 1 = Enabled. Allows an interrupt to occur with a time base set with the RS bits of register A. This bit is cleared by RSMRST# assertion, but not on any other reset.
5	0h RW	**Alarm Interrupt Enable (AIE):** 0 = Disabled. 1 = Enabled. Allows an interrupt to occur when the AF is set from an alarm match from the update cycle. An alarm can occur once a second, one an hour, once a day, or once a month. This bit is cleared by RTCRST# assertion, but not on any other reset.
4	0h RW	**Update-ended Interrupt Enable: (UIE):** 0 = Disabled. 1 = Enabled. Allows an interrupt to occur when the update cycle ends. This bit is cleared by RSMRST# assertion, but not on any other reset.
3	0h RW	**Square Wave Enable (SQWE):** The Square Wave Enable bit serves no function in this device. There is not SQW pin on this device. This bit is cleared by RSMRST# assertion, but not on any other reset.

Bit Range	Default and Access	Field Name (ID): Description
2	Xh RW	**Data Mode (DM):** This bit specifies either binary or BCD data representation. 0 = BCD. 1 = Binary. This bit is not affected by RSMRST# nor any other reset signal.
1	Xh RW	**Hour Format (HOURFORM):** This bit indicates the hour byte format. 0 = Twelve-hour mode is selected.In twelve hour mode, the seventh bit represents AM as zero and PM as one. 1 = Twenty-four hour mode is selected. This bit is not affected by RSMRST# nor any other reset signal.
0	Xh RW	**Daylight Savings Enable (DSE):** The Daylight Savings Enable bit triggers two special hour updates per year when set to one. One is on the first Sunday in April, where time increments from 1:59:59 AM to 3:00:00 AM. The other is the last Sunday in October when the time first reaches 1:59:59 AM, it is changed to 1:00:00 AM. The time mustincrement normally for at least two update cycles (seconds) previous to these conditions for the time change to occur properly. These special update conditions do not occur when the DSE bit is set to zero. The days for the hour adjustment are those specified in United States federal law as of 1987, which is different than previous years. If BUC.DSO bit is set, the DSE bit continues to be a R/W bit, but Daylight Saving is disabled regardless of the DSE bit. This bit is not affected by RSMRST# nor any other reset signal.

37.2.13 Register C Flag Register (Register_C)—Offset Ch

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7	0h RO/V	**Interrupt Request Flag (IRQF):** Interrupt Request Flag = (PF * PIE) + (AF * AIE) + (UF * UFE). This also causes the RTC Interrupt to be asserted. This bit is cleared upon RSMRST# assertion or a read of Register C.
6	0h RO/V	**Periodic Interrupt Flag (PF):** Periodic interrupt Flag will be one when the tap as specified by the RS bits of register A is one. If no taps are specified, this flag bit will remain at zero. This bit is cleared upon RSMRST# assertion or a read of Register C.
5	0h RO/V	**Alarm Flag (AF):** Alarm Flag will be high after all Alarm values match the current time. This bit is cleared upon RTCRST# assertion or a read of Register C.
4	0h RO/V	**Update-ended Flag (UF):** Updated-ended flag will be high immediately following an update cycle for each second. The bit is cleared upon RSMRST# assertion or a read of Register C.
3:0	0h RO	Reserved.

37.2.14 Register D Flag Register (Register_D)—Offset Dh

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RO	**Valid RAM and Time Bit (VRT):** This bit is hard-wired to 1 in the RTC power well. This bit should always be written as a 0 for write cycle, however it will return a 1 for read cycles.
6	0h RO	Reserved.
5:0	Xh RW	**Date Alarm (Date_Alarm):** These bits store the date of month alarm value. If set to 000000, then a dont care state is assumed. The host must configure the dates alarm for these bits to do anything, yet they can be written at any time. If the date alarm is not enabled, these bits will return zeros. These bits are not affected by any reset assertion.

37.2.15 114 Bytes Of Lower User RAM (Register_E)—Offset Eh

Remaining 114 Bytes of Lower User RAM. Each byte in this bank share the same description as shown below. RAM default values are undetermined and the last written value will be retained until RTC power is removed.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	Xh RW	**Lower User RAM (LOWER_USER_RAM):** RTC RAM lower unused range

37.2.16 128 Bytes Of Upper User RAM (Register_80)—Offset 80h

128 Bytes of Upper User RAM. Each byte in this bank share the same description as shown below. RAM default values are undetermined and the last written value will be retained until RTC power is removed.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	Xh RW	**Upper User RAM (UPPER_USER_RAM):** RTC RAM upper unused range

37.3 RTC PCR Registers

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 37-3. Summary of RTC PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3400h	3403h	RTC Configuration (RC)—Offset 3400h	0h
3414h	3417h	Backed Up Control (BUC)—Offset 3414h	0h
3F04h	3F07h	RTC Update In Progress SMI Control (UIPSMI)—Offset 3F04h	0h

37.3.1 RTC Configuration (RC)—Offset 3400h

All bits in this register are in the Primary Well.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW/1L	**Bios Interface Lock-Down (BILD):** When set, prevents RTC version of TS (BUC.TS) from being changed. This bit can only be written from 0 to 1 once. This BILD bit has different function compared SPI and eSPI version but BIOS should set all the corresponding bits after reset in order to lock down the BIOS interface correctly.
30:7	0h RO	Reserved.
6	0h RW	**RTC High Power Mode HW Disable (HPM_HW_DIS):** When set to 1 the internal VRM that generates the rtc well supply voltage in SUS mode is disabled when SLP_S0# is asserted to '0'. (via irtcdswen pin to RTC EBB). When 0, HW control of the RTC internal VRM is disabled.
5	0h RW	**RTC High Power Mode SW Disable (HPM_SW_DIS):** When set to 1 the internal VRM that generates the rtc well supply voltage in SUS mode is disabled (via irtcdswen pin to RTC EBB). When 0 the internal VRM powers the rtc well when RSMRST# is '1'. (default)
4	0h RW/1L	**Partial Range Lock in Upper 128 Bytes (UL):** When set, bytes 38h-3Fh in the upper 128 byte bank of RTC RAM are locked and cannot be accessed. Writes will be dropped and reads will not return any guaranteed data. Bit reset on system reset.

Bit Range	Default and Access	Field Name (ID): Description
3	0h RW/1L	**Partial Range Lock in Lower 128 Bytes (LL):** When set, bytes 38h-3Fh in the lower 128 byte bank of RTC RAM are locked and cannot be accessed. Writes will be dropped and reads will not return any guaranteed data. Bit reset on system reset.
2	0h RW	**Upper 128 Byte Enable (UE):** When set, the upper 128 byte bank of RTC RAM can be accessed.
1:0	0h RO	Reserved.

37.3.2 Backed Up Control (BUC)—Offset 3414h

All bits in this register are in the RTC well and only cleared by RTCRST#.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RW	**Daylight Savings Override (SDO):** When this bit is a '1', the DSE bit in the RTC Register B bit(0) is a RW bit but has no effect where daylight savings is hard-disabled internally. When this bit is a '0', the DSE bit in the RTC register B bit(0) is a RW bit that is configurable by software to enable the daylight savings. System BIOS shall configure this bit accordingly during the boot process before RTC time is initialized.
3:1	0h RO	Reserved.
0	0h RW/L	**Top Swap (TS):** *If PCH is strapped for Top-Swap (GNT(3)# is low at rising edge of PWROK), then this bit cannot be cleared by software. The strap jumper should be removed and the system rebooted.

37.3.3 RTC Update In Progress SMI Control (UIPSMI)—Offset 3F04h

This register exists in the Core well.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW/1C/V	**RTC UIP Low-to-High (UIP_L2H):** This sticky status bit is set whenever the RTC Update-In-Progress signal transitions from low to high (i.e., at the start of an update).
16	0h RW/1C/V	**RTC UIP High-to-Low (UIP_H2L):** This sticky status bit is set whenever the RTC Update-In-Progress signal transitions from high to low (i.e., at the start of an update).
15:2	0h RO	Reserved.
1	0h RW	**RTC UIP Low-to-High SMI Enable (UIP_L2H_SMI_en):** When this bit is set, a '1' in bit 17 will assert the internal SMI signal to the Power Management SMI logic
0	0h RW	**RTC UIP High-to-Low SMI Enable (UIP_H2L_SMI_en):** When this BIOS is set, a '1' in bit 16 will assert the internal SMI signal to the Power Management SMI logic

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38 System Management TCO

38.1 SMBus TCO I/O Registers

The TCO I/O registers reside in a 32-byte range that starts from the IO Base Address described in the TCOBAR register in the SMBus PCI Configuration space.

Table 38-1. Summary of SMBus TCO I/O Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	1h	TCO_RLD Register (TRLD)—Offset 0h	4h
2h	2h	TCO_DAT_IN Register (TDI)—Offset 2h	0h
3h	3h	TCO_DAT_OUT Register (TDO)—Offset 3h	0h
4h	5h	TCO1_STS Register (TSTS1)—Offset 4h	0h
6h	7h	TCO2_STS Register (TSTS2)—Offset 6h	0h
8h	9h	TCO1_CNT Register (TCTL1)—Offset 8h	0h
Ah	Bh	TCO2_CNT Register (TCTL2)—Offset Ah	8h
Ch	Dh	TCO Message Registers (TMSG)—Offset Ch	0h
Eh	Eh	TCO_WDSTATUS Register (TWDS)—Offset Eh	0h
10h	10h	LEGACY_ELIM Register (LE)—Offset 10h	3h
12h	13h	TCO_TMR Register (TTMR)—Offset 12h	4h

38.1.1 TCO_RLD Register (TRLD)—Offset 0h

TCO_RLD Register

Access Method

Type: IO Register
(Size: 16 bits)

Device:
Function:

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
15:10	0h RO	Reserved.
9:0	4h RW	**TCORLD (TCORLD):** Reading this register will return the current count of the TCO timer. Writing any value to this register will reload the timer to prevent the timeout.

38.1.2 TCO_DAT_IN Register (TDI)—Offset 2h

TCO_DAT_IN Register

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**TCO_DAT_IN (TDI):** Data Register for passing commands from the OS to the SMI handler. Writes to this register will cause an SMI and set the OS_TCO_SMI bit in the TCO_STS register.

38.1.3 TCO_DAT_OUT Register (TDO)—Offset 3h

TCO_DAT_OUT Register

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**TCO_DAT_OUT (TDO):** Data Register for passing commands from the SMI handler to the OS. Writes to this register will set the TCO_INT_STS bit in the TCO_STS register. It also causes an interrupt, as selected by the TCO_IRQ_SEL bits.

38.1.4 TCO1_STS Register (TSTS1)—Offset 4h

Unless otherwise indicated, these bits are sticky and are cleared by writing a 1 to the corresponding bit position.

Access Method

Type: IO Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:14	0h RO	Reserved.
13	0h RO	**TCO Target Select (TCO_SLVSEL):** This register bit indicates the value of TCO Target Select Soft Strap.
12	0h RW/1C	**CPUSERR_STS (CPUSERR_STS):** This bit is set to 1 if the CPU complex sends a DMI special cycle message indicating that it wants to cause an SERR#. The software must read the MCH to find out why it wanted the SERR#. Software must write a 1 back to this bit to clear it.
11	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
10	0h RW/1C	**CPUSMI_STS (CPUSMI_STS):** This bit is set to 1 if the CPU complex sends a DMI special cycle message indicating that it wants to cause an SMI. The software must read the CPU to find out why it wanted the SMI. Software must write a 1 back to this bit to clear it.
9	0h RW/1C	**CPUSCI_STS (CPUSCI_STS):** This bit is set to 1 if the CPU complex sends a DMI special cycle message indicating that it wants to cause an SCI. The software must read the CPU to find out why it wanted the SCI. Software must write a 1 back to this bit to clear it.
8	0h RW/1C	**BIOSWR_STS (BIOSWR_STS):** PCH sets this bit to 1 and generates an SMI# to indicate an unsupported attempt to write to the BIOS located in the FWH. This occurs when either: a) The BIOSWP bit is changed from 0 to 1 and the LE bit is also set, or b) Any write is attempted to the BIOS and the BIOSWP bit is also set. This bit does not get set to 1 when: 1) a or b above occurs on eSPI controller. 2) a or b above occurs on SPI Flash controller. Note: On write cycles attempted to the 4MB lower alias to the BIOS space, the BIOSWR_STS bit will not be set.
7	0h RW/1C	**NEWCENTURY_STS (NEWCENTURY_STS):** This bit will be set when the year rolls over from 1999 to 2000. If the bit is already 1, it will remain 1. This bit can be cleared either by software writing a 1 back to the bit position, or by RTCRST# going active. When this bit is set, an SMI# will be generated. However, this will not be a wake event (i.e. if the system is in a sleeping state when the NEWCENTURY_STS bit is set, the system will not wake up). Note: This bit 7 is not valid when the RTC battery is first put in (or if the RTC battery does not provide sufficient power when the system is unplugged). Software can determine that the RTC well was not maintained by checking the RTC_PWR_STS bit (GEN_PMCON_3 register in the Power Management Controller, D31:F2:A4, bit 2) or by other means (such as doing a checksum on the RTC RAM array). If the RTC well is determined to not have been maintained, the BIOS should set the time to a legal value and then clear the NEWCENTURY_STS bit. Note: This bit may take up to 3 RTCCLKs for the bit to be cleared when a 1 is written to the bit to clear it. After writing a 1 to the NEWCENTURY_STS bit, software should also not exit the SMI handler until after the bit has been cleared. This is to make sure the SMI is not re-entered. BIOS Assumption: When booting, the BIOS checks the NEWCENTURY_STS bit. If set, the BIOS should increment the value in the RTC RAM register associated with the century. The BIOS should then clear the NEWCENTURY_STS bit. This scenario would occur if the system was asleep when the century rolls over. If the system is in an S0 state (not sleeping) and the SMI# occurs with the NEWCENTURY_STS bit sets, the SMI handler should increment the value in the RTC RAM register and clear the NEWCENTURY_STS bit.
6:4	0h RO	Reserved.
3	0h RW/1C	**TIMEOUT (TIMEOUT):** Bit set to 1 by PCH to indicate that the SMI was caused by TCO timer reaching 0. Note: The SMI handler should clear this bit to prevent an immediate re-entry to the SMI handler.
2	0h RW/1C	**TCO_INT_STS (TCO_INT_STS):** Bit set to 1 when SMI handler caused the interrupt by writing to the TCO_DAT_OUT register.
1	0h RW/1C	**OS_TCO_SMI (OS_TCO_SMI):** Bit set to 1 when OS code caused an SMI# by writing to the TCO_DAT_IN register.
0	0h RO/V	**NMI2SMI_STS (NMI2SMI_STS):** The PCH sets this bit when an SMI# occurs because an event occurred that would otherwise have caused an NMI.

38.1.5 TCO2_STS Register (TSTS2)—Offset 6h

TCO2_STS Register

Access Method

Type: IO Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:5	0h RO	Reserved.
4	0h RW/1C	**SMLINK_Target_SMI_STS (SMLINK_Target_SMI_STS):** The PCH will set this bit to 1 when it receives the SMI message (encoding 08h in the command type) on the SMLinks Target Interface. Software clears the bit by writing a 1 to this bit position. This bit is in the resume well. It is reset by RSMRST#, but not by the PCI Reset associated with exit from S3-S5 states. This allows the software (presumably BIOS) to get the interrupt, refer this new bit set, and decidedly go into the pre-determined (by local policy) sleep state.
3	0h RO	Reserved.
2	0h RO/V	**NO_REBOOT_PIN_STRAP_STATUS (NRSTRAP_STS):** This bit reflects the state of the No_Reboot strap that is sampled on PWROK rise.
1	0h RW/1C	**SECOND_TO_STS (SECOND_TO_STS):** PCH sets this bit to 1 to indicate that the TIMEOUT bit had been (or is currently) set and a second timeout occurred before the TCO_RLD register was written. If this bit is set and the NO_REBOOT config bit is 0, then the PCH will reboot the system after the second timeout. The reboot is done by asserting PLTRST#. This bit is only cleared by writing a 1 to this bit or by a RSMRST#.
0	0h RW/1C	**INTRD_DET (INTRD_DET):** The bit is set to 1 by the PCH to indicate that an intrusion was detected. This bit is cleared by writing a 1 to this bit or by RTCRST#. Note: This bit has a recovery time. After writing a 1 to this bit position (to clear it), the bit may be read back as a 1 for up 65 microseconds before it is read as a 0. Software must be aware of this recovery time when reading this bit after clearing it. Note: If the INTRUDER# signal is active when the software attempts to clear the INTRD_DET bit, the bit will remain as a 1, and the SMI# will be generated again immediately. The SMI handler can clear the INTRD_SEL bits to avoid further SMIs. However, if the INTRUDER# signals goes inactive and then active again, there will not be further SMIs. If the INTRUDER# signal goes inactive some point after the INTRD_DET bit is written as a 1, then the INTRD_DET signal will go to a 0 when INTRUDER# input signal goes inactive. Note that this is slightly different than a classic sticky bit, since most sticky bits would remain active indefinitely when the signal goes active and would immediately go inactive when a 1 is written to the bit.

38.1.6 TCO1_CNT Register (TCTL1)—Offset 8h

TCO1_CNT Register

Access Method

Type: IO Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12	0h RW	**TCO_LOCK (TCO_LOCK):** When set to 1, this bit prevents writes from changing the TCO_EN bit (in offset 30h of Power Management I/O space). Once this bit is set to 1, it can not be cleared by software writing a 0 to this bit location. A core-well reset is required to change this bit from 1 to 0. This bit defaults to 0.
11	0h RW	**TCO_TMR_HALT (TCO_TMR_HALT):** 1 = The TCO timer will halt. It will not count, and thus cannot reach a value that would cause an SMI# or to cause the SECOND_TO_STS bit to be set. This will also prevent rebooting. 0 = The TCO timer is enabled to count. This is the default.
10	0h RO	Reserved.
9	0h RW	**NMI2SMI_EN (NMI2SMI_EN):** Setting this bit 1 forces all NMIs to instead cause an SMI#, and will be reported in the TCO1_STS register. NMI2SMI_EN bit is set AND the NMI_EN# bit is set to 0, the NMI# will be routed to cause an SMI#. No NMI will be caused. However, if the GBL_SMI_EN bit is not set, then no SMI# will be generated, either. If NMI2SMI_EN is set but the NMI_EN# bit is set to 1, then no NMI or SMI# will be generated. The following table shows the possible combinations: NMI_EN#, GBL_SMI_EN 00: No SMI# based on NMI events (since no SMI# at all because SMI_EN = 0) 01: SMI# will be caused based on NMI events 10: No SMI# at all because SMI_EN is 0 11: No SMI# based on NMI events because NMI_EN#=1
8	0h RW	**NMI_NOW (NMI_NOW):** Writing a 1 to this bit causes an NMI. This allows the BIOS or SMI handler to force entry to the NMI handler. The NMI handler is expected to clear this bit. Another NMI will not be generated until the bit is cleared by writing a 1 back to the same bit position.
7:1	0h RO	Reserved.
0	0h RW	**NO_REBOOT_MSUS (NR_MSUS):** This bit reflects the No Reboot pin strap state. It is sampled high on PWROK. This bit may be set or cleared by software if the strap is sampled low but may not override the strap when the it indicates No Reboot. When set, the TCO timer will count down and generate the SMI# on the first timeout, but will not reboot on the second timeout.

38.1.7 TCO2_CNT Register (TCTL2)—Offset Ah

TCO2_CNT Register

Access Method

Type: IO Register
(Size: 16 bits)

Device:
Function:

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
15:6	0h RO	Reserved.
5:4	0h RW	**OS_POLICY (OS_POLICY):** OS-based software writes to these bits to select the policy that the BIOS will use after the platform resets due the WDT. The following convention is recommended for the BIOS and OS: 00 Boot normally 01 Shut down 10 Dont load OS. Hold in pre-boot state and use LAN to determine next step 11 Reserved Implementation note: These are just scratch pad bits. They should not be reset when the TCO logic resets the platform due to Watchdog Timer.
3	1h RW	**SMB_ALERT_DISABLE (SMB_ALERT_DISABLE):** Disables muxed GPIO/ SMBALERT# signal as an alert source for the heartbeats and the SMBus Target. At reset (RSMRST# pin assertion only), this bit is set and the muxed GPIO/SMBALERT# alerts are disabled.
2:1	0h RW	**INTRD_SEL (INTRD_SEL):** Selects the action to take if the INTRUDER# signal goes active. 11: Reserved 01: Interrupt (as selected by TCO_INT_SEL). 10: SMI# 00 INTRUDER# does not cause SMI# or interrupt
0	0h RO	Reserved.

38.1.8 TCO Message Registers (TMSG)—Offset Ch

TCOBASE+0Ch (MSG1) TCOBASE+0Dh (MSG2) BIOS can write into these registers to indicate its boot progress. The external microcontroller can read these registers to monitor the boot progress

Access Method

Type: IO Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:8	0h RW	**TCO Message2 (MSG2):** TCO Message2
7:0	0h RW	**TCO Message1 (MSG1):** TCO Message1

38.1.9 TCO_WDSTATUS Register (TWDS)—Offset Eh

TCO_WDSTATUS Register

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**TCO_WDSTATUS Register (TWDS):** The BIOS or system management software can write into this register to indicate more details on the boot progress. The register will rest to 00h based on a RSMRST# (but not PCI Reset). The external microcontroller can read this register to monitor boot progress.

38.1.10 LEGACY_ELIM Register (LE)—Offset 10h

LEGACY_ELIM Register

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 3h

Bit Range	Default and Access	Field Name (ID): Description
7:2	0h RO	Reserved.
1	1h RW	**IRQ12_CAUSE (IRQ12_CAUSE):** When software sets the bit to 1, IRQ12 will be high (asserted). When software sets the bit to 0, IRQ12 will be low (not asserted). Default for this bit is 1.
0	1h RW	**IRQ1_CAUSE (IRQ1_CAUSE):** When software sets the bit to 1, IRQ1 will be high (asserted). When software sets the bit to 0, IRQ1 will be low (not asserted). Default for this bit is 1.

38.1.11 TCO_TMR Register (TTMR)—Offset 12h

TCO_TMR Register

Access Method

Type: IO Register
(Size: 16 bits)

Device:
Function:

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
15:10	0h RO	Reserved.
9:0	4h RW	**TCOTMR (TCOTMR):** Value that is loaded into the timer each time the TCO_RLD register is written. Values of 0000h or 0001h will be ignored and should not be attempted. The timer is clocked at approximately 0.6 seconds, and thus allows timeouts ranging from 1.2 second to 613.8 seconds. Note: The timer has an error of +/- 1 tick (0.6s).

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39 FIA Configuration

39.1 FIA Configuration PCR Registers

Table 39-1. Summary of FIA Configuration PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
100h	103h	PCIe Device Reference Clock Request Enable 1 (PDRCRE1)—Offset 100h	0h
108h	10Bh	PCIe Device Reference Clock Request Mapping 1 (PDRCRM1)—Offset 108h	40C2040h
10Ch	10Fh	PCIe Device Reference Clock Request Mapping 2 (PDRCRM2)—Offset 10Ch	9207185h
110h	113h	PCIe Device Reference Clock Request Mapping 3 (PDRCRM3)—Offset 110h	2CAh
300h	303h	HSIO Lane Owner Status 1 (LOS1)—Offset 300h	0h
304h	307h	HSIO Lane Owner Status 2 (LOS2)—Offset 304h	0h

39.1.1 PCIe Device Reference Clock Request Enable 1 (PDRCRE1)—Offset 100h

Access Method

Type:MSG Register
(Size: 32 bits)

Device:
Function:

Default:0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW/L	**PCIe Root Port 12 CLKREQ Mapping Enable (P11CKRQME):** Same description as bit 0.
10	0h RW/L	**PCIe Root Port 11 CLKREQ Mapping Enable (P10CKRQME):** Same description as bit 0.
9	0h RW/L	**PCIe Root Port 10 CLKREQ Mapping Enable (P9CKRQME):** Same description as bit 0.
8	0h RW/L	**PCIe Root Port 9 CLKREQ Mapping Enable (P8CKRQME):** Same description as bit 0.
7	0h RW/L	Reserved

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/L	**PCIe Root Port 7 CLKREQ Mapping Enable (P6CKRQME):** Same description as bit 0.
5	0h RW/L	Reserved
4	0h RW/L	Reserved
3	0h RW/L	**PCIe Root Port 4 CLKREQ Mapping Enable (P3CKRQME):** Same description as bit 0.
2	0h RW/L	**PCIe Root Port 3 CLKREQ Mapping Enable (P2CKRQME):** Same description as bit 0.
1	0h RW/L	**PCIe Root Port 2 CLKREQ Mapping Enable (P1CKRQME):** Same description as bit 0.
0	0h RW/L	**PCIe Root Port 1 CLKREQ Mapping Enable (P0CKRQME):** The mapping of PCIe Root Port to the corresponding CLKREQ# pin is configured by this field. 1 = This PCIe Root Port has the CLKREQ pin presence and the corresponding register (PDRCRM) will indicate which CLKREQ# pin the PCIe Root Port is mapped to. 0 = no presence and will be masked to a de-asserted state.

39.1.2 PCIe Device Reference Clock Request Mapping 1 (PDRCRM1)—Offset 108h

Access Method

Type:MSG Register
(Size: 32 bits)

Device:
Function:

Default:40C2040h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:24	4h RW/L	Reserved.
23	0h RO	Reserved.
22:18	3h RW/L	**PCIe Root Port 4 CLKREQ Mapping (P3CKRQM):** Same definition as bits[4:0].

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	Reserved.
16:12	2h RW/L	**PCIe Root Port 3 CLKREQ Mapping (P2CKRQM):** Same definition as bits[4:0].
11	0h RO	Reserved.
10:6	1h RW/L	**PCIe Root Port 2 CLKREQ Mapping (P1CKRQM):** Same definition as bits[4:0].
5	0h RO	Reserved.
4:0	0h RW/L	**PCIe Root Port 1 CLKREQ Mapping (P0CKRQM):** The mapping of the PCIe* Root Port to the corresponding CLKREQ# pin is configured by this field. This register is only valid if the corresponding enable bit in PDRCRE register is set to 1. 00h: The PCIe* Root Port maps to CLKREQ0# pin 01h: The PCIe* Root Port maps to CLKREQ1# pin 02h: The PCIe* Root Port maps to CLKREQ2# pin ... Others: Reserved NOTE: If a CLKREQ# pin is not implemented in hardware, the corresponding encoding is reserved. Software must never map multiple PCIe* Root Ports to the same CLKREQ# pin. The hardware behavior is undefined if this ever happens. Configuring this field to map to any unsupported CLKREQ# pins may result in undefined hardware behavior.

39.1.3 PCIe Device Reference Clock Request Mapping 2 (PDRCRM2)—Offset 10Ch

Access Method

Type:MSG Register
(Size: 32 bits)

Device:
Function:

Default:9207185h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:24	9h RW/L	**PCIe Root Port 10 CLKREQ Mapping (P9CKRQM):** Same description as bits[4:0].
23	0h RO	Reserved.
22:18	8h RW/L	**PCIe Root Port 9 CLKREQ Mapping (P8CKRQM):** Same description as bits[4:0].

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	Reserved.
16:12	7h RW/L	Reserved.
11	0h RO	Reserved.
10:6	6h RW/L	**PCIe Root Port 7 CLKREQ Mapping (P6CKRQM):** Root Port to the corresponding CLKREQ# pin is configured by this field. This register is only valid if the corresponding enable bit in PDRCRE register is set to 1. 00h: The PCIe* Root Port maps to CLKREQ0# pin 01h: The PCIe* Root Port maps to CLKREQ1# pin 02h: The PCIe* Root Port maps to CLKREQ2# pin ... 0Eh: The PCIe* Root Port maps to CLKREQ14# pin 0Fh: The PCIe* Root Port maps to CLKREQ15# pin Others: Reserved NOTE: If a CLKREQ# pin is not implemented in hardware, the corresponding encoding is reserved. Software must never map multiple PCIe* Root Ports to the same CLKREQ# pin. The hardware behavior is undefined if this ever happens. Configuring this field to map to any unsupported CLKREQ# pins may result in undefined hardware behavior.
5	0h RO	Reserved.
4:0	5h RW/L	Reserved.

39.1.4 PCIe Device Reference Clock Request Mapping 3 (PDRCRM3)—Offset 110h

Access Method

Type:MSG Register
(Size: 32 bits)

Device:
Function:

Default:2CAh

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
10:6	Bh RW/L	**PCIe Root Port 12 CLKREQ Mapping (P11CKRQM):** Same description as bits[4:0].
5	0h RO	Reserved.
4:0	Ah RW/L	**PCIe Root Port 11 CLKREQ Mapping (P10CKRQM):** The mapping of the PCIe* Root Port to the corresponding CLKREQ# pin is configured by this field. This register is only valid if the corresponding enable bit in PDRCRE register is set to 1. 00h: The PCIe* Root Port maps to CLKREQ0# pin 01h: The PCIe* Root Port maps to CLKREQ1# pin 02h: The PCIe* Root Port maps to CLKREQ2# pin ... Others: Reserved NOTE: If a CLKREQ# pin is not implemented in hardware, the corresponding encoding is reserved. Software must never map multiple PCIe* Root Ports to the same CLKREQ# pin. The hardware behavior is undefined if this ever happens. Configuring this field to map to any unsupported CLKREQ# pins may result in undefined hardware behavior.

39.1.5 HSIO Lane Owner Status 1 (LOS1)—Offset 300h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default:0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO/V	**Lane 7 Owner (L7O):** Same description as bits [3:0].
27:24	0h RO/V	Reserved.
23:20	0h RO/V	Reserved.
19:16	0h RO/V	**Lane 4 Owner (L4O):** Same description as bits [3:0].
15:12	0h RO/V	**Lane 3 Owner (L3O):** Same description as bits [3:0].

Bit Range	Default & Access	Field Name (ID): Description
11:8	0h RO/V	**Lane 2 Owner (L2O):** Same description as bits [3:0].
7:4	0h RO/V	**Lane 1 Owner (L1O):** Same description as bits [3:0].
3:0	0h RO/V	**Lane 0 Owner (L0O):** This register indicates the lane owner for Lane 0. 0000: PCIe. 0001: USB3.2. 0010: SATA. 0111:UFS. 1111: No owner Others: Reserved.

39.1.6 HSIO Lane Owner Status 2 (LOS2)—Offset 304h

Access Method

Type:MSG Register
(Size: 32 bits)

Device:
Function:

Default:0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:12	0h RO/V	**Lane 11 Owner (L11O):** Same description as bits [3:0].
11:8	0h RO/V	**Lane 10 Owner (L10O):** Same description as bits [3:0].
7:4	0h RO/V	**Lane 9 Owner (L9O):** Same description as bits [3:0]. 0000: PCIe. 0001: USB3.2. 0010: SATA. 0111:UFS. 1111: No owner Others: Reserved.
3:0	0h RO/V	Reserved.

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40 On Package DMI (OPDMI)

40.1 OPDMI PCR Registers

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 40-1. Summary of OPDMI PCR Register

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
2014h	2017h	Virtual Channel 0 Resource Control (V0CTL)—Offset 2014h	80000000h
201Ah	201Bh	Virtual Channel 0 Resource Status (V0STS)—Offset 201Ah	0h
2020h	2023h	Virtual Channel 1 Resource Control (V1CTL)—Offset 2020h	0h
2026h	2027h	Virtual Channel 1 Resource Status (V1STS)—Offset 2026h	0h
2040h	2043h	ME Virtual Channel (VCm) Resource Control (VMCTL)—Offset 2040h	0h
2046h	2047h	ME Virtual Channel Resource Status (VMSTS)—Offset 2046h	0h
2084h	2087h	Uncorrectable Error Status (UES)—Offset 2084h	0h
2088h	208Bh	Uncorrectable Error Mask (UEM)—Offset 2088h	0h
208Ch	208Fh	Uncorrectable Error Severity (UEV)—Offset 208Ch	0h
2090h	2093h	Correctable Error Status (CES)—Offset 2090h	0h
2094h	2097h	Correctable Error Mask (CEM)—Offset 2094h	2000h
20ACh	20AFh	Root Error Command (REC)—Offset 20ACh	0h
20B0h	20B3h	Root Error Status (RES)—Offset 20B0h	0h
20B4h	20B7h	Error Source Identification (ESID)—Offset 20B4h	0h
2234h	2237h	DMI Control Register (Common) (DMIC)—Offset 2234h	0h
223Ch	223Fh	IOSF Primary Control And Status (IPCS_IOSFSBCS)—Offset 223Ch	0h
2304h	2307h	DMI Port Link Control (DMILINKC)—Offset 2304h	0h
2320h	2323h	DMI PLL Shutdown (Common) (DMIPLLDOWN)—Offset 2320h	0h
2608h	260Bh	Target Link Speed (TLS)—Offset 2608h	2h
2618h	261Bh	Link Configuration (LCFG)—Offset 2618h	0h
2730h	2733h	eSPI Generic I/O Range 1 (LPCLGIR1)—Offset 2730h	0h
2734h	2737h	eSPI Generic I/O Range 2 (LPCLGIR2)—Offset 2734h	0h
2738h	273Bh	eSPI Generic I/O Range 3 (LPCLGIR3)—Offset 2738h	0h
273Ch	273Fh	eSPI Generic I/O Range 4 (LPCLGIR4)—Offset 273Ch	0h
2740h	2743h	eSPI Generic Memory Range (LPCGMR)—Offset 2740h	0h
2744h	2747h	eSPI BIOS Decode Enable (LPCBDE)—Offset 2744h	FFCFh
274Ch	274Fh	General Control and Status (GCS)—Offset 274Ch	0h
2750h	2753h	I/O Trap Register 1 - Lower DW (IOT1_LOW)—Offset 2750h	0h
2754h	2757h	I/O Trap Register 1 - Upper DW (IOT1_HIGH)—Offset 2754h	0h
2770h	2773h	eSPI I/O Decode Range (LPCIOD)—Offset 2770h	0h
2774h	2777h	eSPI I/O Enable (LPCIOE)—Offset 2774h	0h

Table 40-1. Summary of OPDMI PCR Register

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
2778h	277Bh	TCO Base Address (TCOBASE)—Offset 2778h	0h
277Ch	277Fh	General Purpose Memory Range 1 (GPMR1)—Offset 277Ch	0h
2780h	2783h	General Purpose Memory Range 1 Destination ID (GPMR1DID)—Offset 2780h	0h
27ACh	27AFh	PM Base Address (PMBASEA)—Offset 27ACh	0h
27B0h	27B3h	PM Base Control (PMBASEC)—Offset 27B0h	0h
27B4h	27B7h	ACPI Base Address (ACPIBA)—Offset 27B4h	0h
27B8h	27BBh	ACPI Base Destination ID (ACPIBDID)—Offset 27B8h	0h

40.1.1 Virtual Channel 0 Resource Control (V0CTL)—Offset 2014h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 80000000h

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**Virtual Channel Enable (EN):** Enables the VC when set. Disables the VC when cleared.
30:27	0h RO	Reserved.
26:24	0h RO	**Virtual Channel Identifier (ID):** Indicates the ID to use for this virtual channel
23:16	0h RO	Reserved.
15:10	0h RW/L	**Extended TC/VC Map (ETVM):** Defines the upper 8-bits of the VC0 16-bit TC/VC mapping registers. These registers use the PCI Express reserved TC[3] traffic class bit.This register is Read-Only if DMIC.SRL field is set.
9:7	0h RO	Reserved.
6:1	0h RW/L	**Transaction Class / Virtual Channel Map (TVM):** Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel. This register is Read-Only if DMIC.SRL field is set.
0	0h RO	Reserved.

40.1.2 Virtual Channel 0 Resource Status (V0STS)—Offset 201Ah

Access Method

Type: MSG Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	Reserved.
1	0h RO/V	**VC Negotiation Pending (NP):** When set, indicates the virtual channel is still being negotiated with ingress ports.
0	0h RO	Reserved.

40.1.3 Virtual Channel 1 Resource Control (V1CTL)—Offset 2020h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Virtual Channel Enable (EN):** Enables the VC when set. Disables the VC when cleared.
30:28	0h RO	Reserved.
27:24	0h RW/L	**Virtual Channel Identifier (ID):** Indicates the ID to use for this virtual channel. This register is Read-Only if the DMIC.SRL field is set.
23:16	0h RO	Reserved.
15:10	0h RW/L	**Extended TC/VC Map (ETVM):** Defines the upper 8-bits of the VC1 16-bit TC/VC mapping registers. These registers use the PCI Express reserved TC[3] traffic class bit. This register is Read-Only if the DMIC.SRL field is set. If VC1 is not enabled, the register output sent to the users of this register is forced to 0.
9:8	0h RO	Reserved.
7:1	0h RW/L	**Transaction Class / Virtual Channel Map (TVM):** Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel. This register is Read-Only if the DMIC.SRL field is set. If VC1 is not enabled, the register output sent to the users of this register is forced to 0.
0	0h RO	Reserved.

40.1.4 Virtual Channel 1 Resource Status (V1STS)—Offset 2026h

Virtual Channel 1 Resource Status

Access Method

Type: MSG Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	Reserved.
1	0h RO/V	**VC Negotiation Pending (NP):** When set, indicates the virtual channel is still being negotiated with ingress ports.
0	0h RO	Reserved.

40.1.5 ME Virtual Channel (VCm) Resource Control (VMCTL)—Offset 2040h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Virtual Channel Enable (EN):** Enables the VC when set. Disables the VC when cleared. This register is Read-Only if the DMIC.SRL field is set.
30:28	0h RO	Reserved.
27:24	0h RW/L	**Virtual Channel Identifier (ID):** Indicates the ID to use for this virtual channel. This register is Read-Only if the DMIC.SRL field is set.
23:16	0h RO	Reserved.
15:10	0h RW/L	**Extended TC/VC Map (ETVM):** Defines the upper 8-bits of the VCm 16-bit TC/VC mapping registers. These registers use the PCIe reserved TC[3] traffic class bit. This register is Read-Only if the DMIC.SRL field is set. If VCm is not enabled, the register output sent to the users of this register is forced to 0. This register is Read-Only if DMIC.SRL field is set
9:8	0h RO	Reserved.
7:1	0h RW/L	**Transaction Class / Virtual Channel Map (TVM):** Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel. This register is Read-Only if the DMIC.SRL field is set. If VCm is not enabled, the register output sent to the users of this register is forced to 0. This register is Read-Only if DMIC.SRL field is set
0	0h RO	Reserved.

40.1.6 ME Virtual Channel Resource Status (VMSTS)—Offset 2046h

Access Method

Type: MSG Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	Reserved.
1	0h RO/V	**VC Negotiation Pending (NP):** When set, indicates the virtual channel is still being negotiated with ingress ports.
0	0h RO	Reserved.

40.1.7 Uncorrectable Error Status (UES)—Offset 2084h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	Reserved.
20	0h RW/1C/V/P	**Unsupported Request Error Status (URE):** Indicates an unsupported request was received.
19	0h RO	**ECRC Error Status (EE):** ECRC is not supported.
18	0h RW/1C/V/P	**Malformed TLP Status (MT):** Indicates a malformed TLP was received.
17	0h RW/1C/V/P	**Receiver Overflow Status (RO):** Indicates a receiver overflow occurred.
16	0h RO	**Unexpected Completion Status (UC):** Reserved, not supported.
15	0h RW/1C/V/P	**Completer Abort Status (CA):** Indicates a completer abort was received.
14	0h RO	**Completion Timeout Status (CT):** Reserved, not supported.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	**Flow Control Protocol Error Status (FCPE):** Reserved, not supported.
12	0h RW/1C/V/P	**Poisoned TLP Status (PT):** Indicates a poisoned TLP was received.
11:5	0h RO	Reserved.
4	0h RW/1C/V/P	**Data Link Protocol Error Status (DLPE):** Indicates a data link protocol error occurred.
3:1	0h RO	Reserved.
0	0h RO	**Training Error Status (TE):** Not supported

40.1.8 Uncorrectable Error Mask (UEM)—Offset 2088h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	Reserved.
20	0h RW/P	**Unsupported Request Error Mask (URE):** Mask for uncorrectable errors.
19	0h RO	**ECRC Error Mask (EE):** ECRC is not supported.
18	0h RW/P	**Malformed TLP Mask (MT):** Mask for malformed TLPs.
17	0h RW/P	**Receiver Overflow Mask (RO):** Mask for receiver overflows.
16	0h RO	**Unexpected Completion Mask (UC):** Reserved, Not supported.
15	0h RW/P	**Completer Abort Mask (CM):** Mask for completer abort.
14	0h RO	**Completion Timeout Mask (CT):** Reserved, not supported.
13	0h RO	**Flow Control Protocol Error Mask (FCPE)**
12	0h RW/P	**Poisoned TLP Mask (PT):** Mask for poisoned TLPs.
11:5	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/P	**Data Link Protocol Error Mask (DLPE):** Mask for data link protocol errors.
3:1	0h RO	Reserved.
0	0h RO	**Training Error Mask (TE):** Not supported.

40.1.9 Uncorrectable Error Severity (UEV)—Offset 208Ch

These registers are reset by core PWROK

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	Reserved.
20	0h RW/P	**Unsupported Request Error Severity (URE):** Severity for unsupported request reception.
19	0h RO	**ECRC Error Severity (EE):** Not Supported.
18	0h RW/P	**Malformed TLP Severity (MT):** Severity for malformed TLP reception.
17	0h RW/P	**Receiver Overflow Severity (RO):** Severity for receiver overflow occurrences.
16	0h RO	**Unexpected Completion Severity (UC):** Not supported.
15	0h RW/P	**Completer Abort Severity (CA):** Severity for completer.
14	0h RO	**Completion Timeout Severity (CT):** Not supported.
13	0h RO	**Flow Control Protocol Error Severity (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Severity (PT):** Severity for poisoned TLP reception.
11:5	0h RO	Reserved.
4	0h RW/P	**Data Link Protocol Error Severity (DLPE):** Severity for data link protocol errors.
3:1	0h RO	Reserved.
0	0h RW/P	**Training Error Severity (TE):** TE not supported. This bit is RW for ease of implementation.

40.1.10 Correctable Error Status (CES)—Offset 2090h

These registers are reset by core PWROK

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	0h RW/1C/V/P	**Advisory Non-Fatal Error Status (ANFES):** When set, indicates that a Advisory Non-Fatal Error occurred.
12	0h RW/1C/V/P	**Replay Timer Timeout Status (RTT):** Indicates the replay timer timed out.
11:9	0h RO	Reserved.
8	0h RW/1C/V/P	**Replay Number Rollover Status (RNR):** Indicates the replay number rolled over.
7	0h RW/1C/V/P	**Bad DLLP Status (BD):** Indicates a bad DLLP was received.
6	0h RW/1C/V/P	**Bad TLP Status (BT):** Indicates a bad TLP was received.
5:1	0h RO	Reserved.
0	0h RW/1C/V/P	**Receiver Error Status (RE):** Indicates a receiver error occurred.

40.1.11 Correctable Error Mask (CEM)—Offset 2094h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 2000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13	1h RW/P	**Advisory Non-Fatal Error Mask (ANFEM):** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.
12	0h RW/P	**Replay Timer Timeout Mask (RTT):** Mask for replay timer timeout.
11:9	0h RO	Reserved.
8	0h RW/P	**Replay Number Rollover Mask (RNR):** Mask for replay number rollover.
7	0h RW/P	**Bad DLLP Mask (BD):** Mask for bad DLLP reception.
6	0h RW/P	**Bad TLP Mask (BT):** Mask for bad TLP reception.
5:1	0h RO	Reserved.
0	0h RW/P	**Receiver Error Mask (RE):** Mask for receiver errors.

40.1.12 Root Error Command (REC)—Offset 20ACh

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Drop Poisoned Downstream Packets (DPDP):** When set to a '1': if downstream packet on OPI is received with the EP bit set, this packet and all subsquent packets with data received on DMI for any VC will have their Unsupported Transaction (UT) field set causing them to be forwarded to the Error Handler. When cleared to a '0', downstream packets from OPI with the EP bit set are forwarded onto the downstream backbone normally.
30	0h RW	**Unsupported Transaction Policy Bit (UTPB):** When set to 1, the Unsupported Transactions detected on OPI will not set the UES.URE bit. This subsequently ensures that SERR will never be signaled in response to Unsupported Transactions regardless of UEV.URE. When set to 0, the Unsupported Transactions detected on OPI will set the UES.URE bit.
29:3	0h RO	Reserved.
2	0h RO	**Fatal Error Reporting Enable (FERE):** When set, the root port will generate an interrupt when a fatal error is reported by the attached device. Not implemented by PCH.
1	0h RO	**Non-fatal Error Reporting Enable (NERE):** When set, the root port will generate an interrupt when a non-fatal error is reported by the attached device. Not implemented in PCH.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	Reserved.

40.1.13 Root Error Status (RES)—Offset 20B0h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Advanced Error Interrupt Message Number (AEMN):** There is only one error interrupt allocated.
26:4	0h RO	Reserved.
3	0h RO	**Multiple ERR_FATAL/NONFATAL Recvieved (MENR):** Set when either a fatal or a non-fatal error is received and the ENR bit is already set. This is not supported in PCH.
2	0h RW/1C/V	**ERR_FATAL/NONFATAL Received (ENR):** Set when either a fatal or a non-fatal error message is received or an internal fatal error is detected (all internal uncorrectable errors are fatal).
1	0h RO	**Multiple ERR_COR Received (MCR):** Set when a correctable error message is received and the CR bit is already set. This is not supported in PCH
0	0h RW/1C/V	**ERR_COR Received (CR):** Set when a correctable error message is received or an internal correctable error is detected.

40.1.14 Error Source Identification (ESID)—Offset 20B4h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO/V	**ERR_FATAL/NONFATAL Source Identification (EFNFSID):** Loaded with the requester ID indicated in the received ERR_FATAL or ERR_NONFATAL message when RES.ENR is first set, or the internal requestor ID if an internally detected error.
15:0	0h RO/V	**ERR_COR Source Identification (ECSID):** Loaded with the requester ID indicated in the received ERR_COR message when RES.CR is first set, or the internal requester ID if an internally detected error

40.1.15 DMI Control Register (Common) (DMIC)—Offset 2234h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Secured Register Lock (SRL):** When this bit is set, all the secured registers will be locked and will be Read-Only.
30:5	0h RO	Reserved.
4	0h RW	**Partition/Trunk Oscillator Clock Gate Enable (PTOCGE):** When set, this bit allows the oscillator clock to be gated at the partition/trunk level when the conditions are met. When cleared, the oscillator clock gating at the partition/trunk level is disabled.
3	0h RW	**DMI Link CLKREQ Enable (DMILCLKREQEN):** When set, this bit enables DMI to de-assert the DMI link CLKREQ. When cleared, DMI link CLKREQ is not allowed to de-assert.
2	0h RW	**DMI Backbone CLKREQ Enable (DMIBBCLKREQEN):** When set, this bit enables DMI to de-assert the Primary backbone CLKREQ. When cleared, DMI Primary backbone CLKREQ is not allowed to de-assert.
1	0h RW	**DMI Link Dynamic Clock Gate Enable (DMILCGEN):** When set, this bit enables dynamic clock gating on the DMI Link clock domain logic. When cleared, dynamic clock gating on the DMI Link clock domain is disabled.
0	0h RW	**DMI Backbone Dynamic Clock Gate Enable (DMIBCGEN):** When set, this bit enables dynamic clock gating on the DMI backbone domain logic. When cleared, dynamic clock gating on the DMI backbone clock domain is disabled.

40.1.16 IOSF Primary Control And Status (IPCS_IOSFSBCS)—Offset 223Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14:12	0h RW	**IOSF Primary ISM Idle Counter (PRIC):** BIOS may need to program this register field.
11:0	0h RO	Reserved.

40.1.17 DMI Port Link Control (DMILINKC)—Offset 2304h

BIOS may need to program this register.

40.1.18 DMI PLL Shutdown (Common) (DMIPLLDOWN)—Offset 2320h

BIOS may need to program this register.

40.1.19 Target Link Speed (TLS)—Offset 2608h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 2h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	2h RO/V	**Target Link Speed (TLS):** Specifies the Target link speed that should be used if speed change is supported. Bit | Description 0000 | SPEED0: 100 Mb/s per-lane 0001 | SPEED1: 1 Gb/s per-lane 0010 | SPEED2: 2 Gb/s per-lane 0011 | SPEED3: 4 GT/s per-lane 0100-1111 | Reserved Note: The default value of bit[1:0] is defined by soft strap. Bit[3:2] are hardwired to '00'. This field is Read-only (RO) in with TLS value defined by soft-strap. Only static speed configuration is supported.

40.1.20 Link Configuration (LCFG)—Offset 2618h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	Reserved.
25	0h RW/L	**Secure Register Lock (SRL):** When set, the secured register will be locked.
24:0	0h RO	Reserved.

40.1.21 eSPI Generic I/O Range 1 (LPCLGIR1)—Offset 2730h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW/L	**Address[7:2] Mask (ADDRMASK):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set
17:16	0h RO	Reserved.
15:2	0h RW/L	**Address[15:2] DWord-aligned address (ADDR):** Address[15:2]: DWord-aligned address. PCH does not provide decode down to the word or byte level. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set
1	0h RW/L	**ISH Decode Enable (ISHDE):** When this bit is set to '1', then the range specified in this register is enabled for decoding to ISH. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set
0	0h RW/L	**eSPI Decode Enable (LPCDEN):** When this bit is set to 1 and ISHDE=0, then the range specified in this register is enabled for decoding to eSPI. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.

40.1.22 eSPI Generic I/O Range 2 (LPCLGIR2)—Offset 2734h

Same description as LPCLGIR1 register.

40.1.23 eSPI Generic I/O Range 3 (LPCLGIR3)—Offset 2738h

Same description as LPCLGIR1 register.

40.1.24 eSPI Generic I/O Range 4 (LPCLGIR4)—Offset 273Ch

Same description as LPCLGIR1 register.

40.1.25 eSPI Generic Memory Range (LPCGMR)—Offset 2740h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/L	**Memory Address[31:16] (MEMADDR):** This field specifies a 64KB memory block anywhere in the 4GB memory space that will be decoded to eSPI as standard eSPI Memory Cycle if enabled. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
15:1	0h RO	Reserved.
0	0h RW/L	**eSPI Memory Range Decode Enable (LPCMRDEN):** When this bit is set to '1', then the range specified in this register is enabled for decoding to eSPI. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.

40.1.26 eSPI BIOS Decode Enable (LPCBDE)—Offset 2744h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: FFCFh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	1h RO	**F8-FF Enable (EF8):** Enables decoding of 512K of the following BIOS range: Data space: FFF80000h – FFFFFFFFh Feature space: FFB80000h – FFBFFFFFh Register Attribute: Static.
14	1h RW/L	**F0-F8 Enable (EF0):** Enables decoding of 512K of the following BIOS range: Data space: FFF00000h – FFF7FFFFh Feature space: FFB00000h – FFB7FFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
13	1h RW/L	**E8-EF Enable (EE8):** Enables decoding of 512K of the following BIOS range: Data space: FFE80000h – FFEFFFFFh Feature space: FFA80000h – FFAFFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
12	1h RW/L	**E0-E8 Enable (EE0):** Enables decoding of 512K of the following BIOS range: Data space: FFE00000h – FFE7FFFFh Feature Space: FFA00000h – FFA7FFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
11	1h RW/L	**D8-DF Enable (ED8):** Enables decoding of 512K of the following BIOS range: Data space: FFD80000h – FFDFFFFFh Feature space: FF980000h – FF9FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.

Bit Range	Default & Access	Field Name (ID): Description
10	1h RW/L	**D0-D7 Enable (ED0):** Enables decoding of 512K of the following BIOS range: Data space: FFD00000h – FFD7FFFFh Feature space: FF900000h – FF97FFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
9	1h RW/L	**C8-CF Enable (EC8):** Enables decoding of 512K of the following BIOS range: Data space: FFC80000h – FFCFFFFFh Feature space: FF880000h – FF8FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
8	1h RW/L	**C0-C7 Enable (EC0):** Enables decoding of 512K of the following BIOS range: Data space: FFC00000h – FFC7FFFFh Feature space: FF800000h – FF87FFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
7	1h RW/L	**Legacy F Segment Enable (LFE):** This enables the decoding of the legacy 64KB range at F0000h – FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
6	1h RW/L	**Legacy E Segment Enable (LEE):** This enables the decoding of the legacy 64KB range at E0000h – EFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
5:4	0h RO	Reserved.
3	1h RW/L	**70-7F Enable (E70):** Enables decoding of 1MB of the following BIOS range: Data space: FF700000h – FF7FFFFFh Feature space: FF300000h – FF3FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
2	1h RW/L	**60-6F Enable (E60):** Enables decoding of 1MB of the following BIOS range: Data space: FF600000h – FF6FFFFFh Feature Space: FF200000h – FF2FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
1	1h RW/L	**50-5F Enable (E50):** Enables decoding of 1MB of the following BIOS range: Data space: FF500000h – FF5FFFFFh Feature Space: FF100000h – FF1FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
0	1h RW/L	**40-4F Enable (E40):** Enables decoding of 1MB of the following BIOS range: Data space: FF400000h – FF4FFFFFh Feature space: FF000000h – FF0FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.

40.1.27 General Control and Status (GCS)—Offset 274Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/L	**RPR Destination ID (RPRDID):** This field specifies the PCIe port Destination ID that is the target of the I/O ranges specified in the RPR field. Only one PCIe root port at a time can be enabled for Port 8xh support. This field is only valid when GCS.RPR field is set. BIOS must program the bits which are not used to zeros. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set
15:12	0h RO	Reserved.
11	0h RW/L	**Reserved Page Route (RPR):** Determines where to send the reserved page registers. These addresses are sent to PCIe Root Port or eSPI for the purpose of generating POST codes. The I/O addresses modified by this field are: 80h - 8Fh.When cleared, DMI will not perform source decode on the I/O ranges specified above. The cycles hitting these ranges will end up in P2SB which will then forward the cycle to eSPI through IOSF Sideband. When set, access to the I/O ranges specified above will be forwarded to PCIe Root Port with the destination ID specified in GCS.RPRDID using DMI source decode.The aliases for these registers, at 90h, 94h, 95h, 96h, 98h, 9Ch, 9Dh, and 9Eh, are never source decoded by DMI. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
10	0h RW/V/L	**Boot BIOS Strap (BBS):** This field determines the destination of accesses to the BIOS memory range. 0 = SPI 1 = eSPI When SPI or eSPI is selected, the range that is decoded is further qualified by other configuration bits described in the respective sections.The value in this field can be overwritten by software as long as the BIOS Interface Lock-Down (bit 0) and DMIC.SRL are not set. Register Attribute: Static.
9:1	0h RO	Reserved.
0	0h RW/O	**BIOS Interface Lock-Down (BILD):** When set, prevents GCS.BBS from being changed. This bit can only be written from 0 to 1 once. Register Attribute: Static.

40.1.28 I/O Trap Register 1 - Lower DW (IOT1_LOW)—Offset 2750h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address[7:2] Mask (ADDRMASK):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RO	Reserved.
15:2	0h RW	**Address[15:2] DWord-aligned address (ADDR):** DWord-aligned address.
1	0h RO	Reserved.
0	0h RW	**Trap Enable (TNSMIEN):** When this bit is set to 1, then the trapping logic specified in this register is enabled.

40.1.29 I/O Trap Register 1 - Upper DW (IOT1_HIGH)—Offset 2754h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW	**Read/Write Mask (RWMASK):** When this bit is 1, the trapping logic will operate on both read and write cycles. When this bit is 0, the cycle must match the type specified in bit 16.
16	0h RW	**Read/Write# (RW):** 1 = Read 0 = Write The value in this field does not matter if bit 17 is set.
15:8	0h RO	Reserved.
7:4	0h RW	**Byte Enable Mask (BEMASK):** A 1 in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
3:0	0h RW	**Byte Enable (BE):** Active-high, DWord-aligned byte enables.

40.1.30 eSPI I/O Decode Range (LPCIOD)—Offset 2770h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	0h RW/L	**FDD Range (FDD):** The following table describes which range to decode for the FDD Port. Bits | Decode Range 0 | 3F0h 3F5h, 3F7h | (Primary) 1 | 370h 375h, 377h (Secondary) This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set
11:10	0h RO	Reserved.
9:8	0h RW/L	**LPT Range (LPT):** The following table describes which range to decode for the LPT Port. Bits | Decode Range 00 | 378h 37Fh and 778h 77Fh 01 | 278h 27Fh (port 279h is read only) and 678h 67Fh 10 | 3BCh 3BEh and 7BCh 7BEh 11 | Reserved. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set
7	0h RO	Reserved.
6:4	0h RW/L	**ComB Range (CB):** The following table describes which range to decode for the COMB Port. Bits | Decode Range 000 | 3F8h 3FFh (COM1) 001 | 2F8h 2FFh (COM2) 010 | 220h 227h 011 | 228h 22Fh 100 | 238h 23Fh 101 | 2E8h 2EFh | (COM 4) 110 | 338h 33Fh 111 | 3E8h 3EFh (COM 3) This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set
3	0h RO	Reserved.
2:0	0h RW/L	**ComA Range (CA):** The following table describes which range to decode for the COMA Port. Bits | Decode Range 000 | 3F8h 3FFh (COM1) 001 | 2F8h 2FFh (COM2) 010 | 220h 227h 011 | 228h 22Fh 100 | 238h 23Fh 101 | 2E8h 2EFh (COM 4) 110 | 338h 33Fh 111 | 3E8h 3EFh (COM 3) This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set

40.1.31 eSPI I/O Enable (LPCIOE)—Offset 2774h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9	0h RW/L	**High Gameport Enable (HGE):** Enables decoding of the I/O locations 208h to 20Fh to eSPI. This register is Read-Only if the DMIC.SRL field is set.
8	0h RW/L	**Low Gameport Enable (LGE):** Enables decoding of the I/O locations 200h to 207h to eSPI. This register is Read-Only if the DMIC.SRL field is set.
7:4	0h RO	Reserved.
3	0h RW/L	**Floppy Drive Enable (FDE):** Enables decoding of the FDD range to eSPI. Range is selected by LIOD.FDE. This register is Read-Only if the DMIC.SRL field is set.
2	0h RW/L	**Parallel Port Enable (PPE):** Enables decoding of the LPT range to eSPI. Range is selected by LIOD.LPT. This register is Read-Only if the DMIC.SRL field is set.
1	0h RW/L	**Com Port B Enable (CBE):** Enables decoding of the COMB range to eSPI. Range is selected by LIOD.CB. This register is Read-Only if the DMIC.SRL field is set.
0	0h RW/L	**Com Port A Enable (CAE):** Enables decoding of the COMA range to eSPI. Range is selected by LIOD.CA. This register is Read-Only if the DMIC.SRL field is set.

40.1.32 TCO Base Address (TCOBASE)—Offset 2778h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:5	0h RW/L	**TCO Base Address (TCOBA):** Provides the 32 bytes of I/O space for TCO logic, that can be map anywhere in the 64k I/O space on 32-byte boundaries. This register is Read-Only if the DMIC.SRL field is set.
4:2	0h RO	Reserved.
1	0h RW/L	**TCO Enable (TCOEN):** When set, decode of the I/O range specified by the TCO base address. This register is Read-Only if the DMIC.SRL field is set.
0	0h RO	Reserved.

40.1.33 General Purpose Memory Range 1 (GPMR1)—Offset 277Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/L	**General Purpose Memory Range Limit 1 (GPMRL1):** This field specifies limit address bits[31:16] for the General Purpose Memory Range 1. Bits [15:0] are assumed to be 'FFFFh'. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set
15:0	0h RW/L	**General Purpose Memory Range Base 1 (GPMRB1):** This field specifies base address bits[31:16] for the General Purpose Memory Range 1. Bits [15:0] are assumed to be '0000h'. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set

40.1.34 General Purpose Memory Range 1 Destination ID (GPMR1DID)—Offset 2780h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**General Purpose Memory Range 1 Decode Enable (GPMR1DE):** When enabled, memory cycles that falls within the GPMR1.GPMRL1 and GPMR1.GPMRB1 range inclusive will be forwarded using source decode to the destination ID specified in GPMR1DID.GPMR1DID field. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set
30:0	0h RW/L	**General Purpose Memory Range 1 Destination ID (GPMR1DID):** The destination ID to be used to forward the cycle decoded to hit the General Purpose Memory Range 1. BIOS must program the bits which are not used to zeros. Hardware will ignore the unused bits. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set

40.1.35 PM Base Address (PMBASEA)—Offset 27ACh

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/L	**PM Base Address Memory Range Limit (PMBAMRL):** This field specifies limit address bits[31:16] for the PM Base Address memory range. Bits [15:0] are assumed to be FFFFh. This register is Read-Only if the DMIC.SRL field is set.
15:0	0h RW/L	**PM Base Address Memory Range Base (PMBAMRB):** This field specifies base address bits[31:16] for the PM Base Address memory range. Bits [15:0] are assumed to be 0000h. This register is Read-Only if the DMIC.SRL field is set.

40.1.36 PM Base Control (PMBASEC)—Offset 27B0h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**PM Base Address Memory Range Decode Enable (PMBAMRDE):** When enabled, memory cycles that falls within the PMBASEADDR.PMBAMRB and PMBASEADDR.PMBAMRL range inclusive will be forwarded using source decode to the destination ID specified in PMBASEC.PMBDID field. This register is Read-Only if the DMIC.SRL field is set.
30:0	0h RW/L	**PM Base Destination ID (PMBDID):** The destination ID to be used to forward the cycle decoded to hit the PM Base Address range. BIOS must program the bits which are not used to zeros. Hardware will ignore the unused bits. This register is Read-Only if the DMIC.SRL field is set.

40.1.37 ACPI Base Address (ACPIBA)—Offset 27B4h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
23:18	0h RW/L	**Address[7:2] Mask (ADDR72MASK):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size. This register is Read-Only if the DMIC.SRL field is set.
17:16	0h RO	Reserved.
15:2	0h RW/L	**Address[15:2] DWord-aligned address (ADDR):** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level. This register is Read-Only if the DMIC.SRL field is set.
1	0h RO	Reserved.
0	0h RW/L	**ACPI I/O Base Address Decode Enable (ACPIBADE):** When this bit is set to 1, then the range specified in this register is enabled for decoding to the destination ID specified in ACPIBDID register. This register is Read-Only if the DMIC.SRL field is set.

40.1.38 ACPI Base Destination ID (ACPIBDID)—Offset 27B8h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**ACPI Base Destination ID (ACPIBDID):** The destination ID to be used to forward the cycle decoded to hit the ACPI Base Address range. BIOS must program the bits which are not used to zeros. Hardware will ignore the unused bits. This register is Read-Only if the DMIC.SRL field is set.

41 IO Strap

41.1 IO Trap Registers

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 41-1. Summary of IO Trap Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1D00h	1D03h	PSTH Control Register (PSTHCTL)—Offset 1D00h	0h
1E00h	1E03h	Trap Status Register (TRPSTS)—Offset 1E00h	0h
1E10h	1E13h	Trapped Cycle Register (TRPCYC1)—Offset 1E10h	0h
1E18h	1E1Bh	Trapped Write Data Register (TRPWRDATA1)—Offset 1E18h	0h
1E80h	1E83h	I/O Trap Registers 1 (IOTRP1_1)—Offset 1E80h	0h
1E84h	1E87h	I/O Trap Registers 1 (IOTRP1_2)—Offset 1E84h	0h
1E88h	1E8Bh	I/O Trap Registers 2 (IOTRP2_1)—Offset 1E88h	0h
1E8Ch	1E8Fh	I/O Trap Registers 2 (IOTRP2_2)—Offset 1E8Ch	0h
1E90h	1E93h	I/O Trap Registers 3 (IOTRP3_1)—Offset 1E90h	0h
1E94h	1E97h	I/O Trap Registers 3 (IOTRP3_2)—Offset 1E94h	0h
1E98h	1E9Bh	I/O Trap Registers 4 (IOTRP4_1)—Offset 1E98h	0h
1E9Ch	1E9Fh	I/O Trap Registers 4 (IOTRP4_2)—Offset 1E9Ch	0h

41.1.1 PSTH Control Register (PSTHCTL)—Offset 1D00h

PSTH control register

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW	**PSTH IOSF Primary Trunk Clock Gating Enable (PSTHIOSFPTCGE):** 0 = Disable 1 = Enable
1	0h RW	**PSTH IOSF Sideband Trunk Clock Gating Enable (PSTHIOSFSTCGE):** 0 = Disable 1 = Enable
0	0h RW	**PSTH Dynamic Clock Gating Enable (PSTHDCGE):** 0 = Disable 1 = Enable

41.1.2 Trap Status Register (TRPSTS)—Offset 1E00h

Trap status register

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RW/1C/V	**Cycle Trap SMI# Status (SMISTAT):** These bits are set by hardware when the corresponding Cycle Trap register is enabled and a matching cycle is received (and trapped). These bits are OR'ed together to create a single status bit in the Power Management register space.Note that the SMI# and trapping must be enabled in order to set these bits. This is because, in order to do the cycle comparison, packets must be delayed by several clocks from the DMI pins to the internal receiver. This delay is only enabled when at least one of the trap ranges is enabled. These bits are set before the completion is generated for the trapped cycle, thereby guaranteeing that the processor can enter the SMI# handler when the instruction completes. Each status bit is cleared by writing a '1' to the corresponding bit location in this register.

41.1.3 Trapped Cycle Register (TRPCYC1)—Offset 1E10h

This register saves information about the I/O Cycle that was trapped and generated the SMI# for software to read.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RO/V	**Read-Write (TRPRWR):** 1 = Read, 0 = Write
23:20	0h RO	Reserved.
19:16	0h RO/V	**Active-High Byte Enables (TRPBE):** This is the DWord-aligned byte enables associated with the trapped cycle. A 1 in any bit location indicates that the corresponding byte is enabled in the cycle.
15:2	0h RO/V	**IO Address (TRPADDR):** This is the DWord-aligned address of the trapped cycle.
1:0	0h RO	Reserved.

41.1.4 Trapped Write Data Register (TRPWRDATA1)—Offset 1E18h

This register saves the data from I/O write cycles that are trapped for software to read

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Data (TRPDATA):** DWord of I/O write data. This field is undefined after trapping a read cycle.

41.1.5 I/O Trap Registers 1 (IOTRP1_1)—Offset 1E80h

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address Mask (TRP1ADDRM):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW	**Address (TRP1ADDR):** DWord-aligned address
1	0h RO	Reserved.
0	0h RW	**Trap and SMI Enable (TRP1EN):** When this bit is set to 1, then the trapping logic specified in this register is enabled.

41.1.6 I/O Trap Registers 1 (IOTRP1_2)—Offset 1E84h

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW	**Read-Write Mask (TRP1RWM):** When this bit is '1', the trapping logic will operate on both read and write cycles. When this bit is '0', the cycle must match the type specified in bit 48.
16	0h RW	**Read/Write (TRP1RW):** 1 = Read, 0 = Write, the value in this field does not matter if bit 49 is set.
15:8	0h RO	Reserved.
7:4	0h RW	**Byte Enable Mask (TRP1BEM):** A '1' in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
3:0	0h RW	**Byte Enables (TRP1BE):** Active-high, DWord-aligned byte enables

41.1.7 I/O Trap Registers 2 (IOTRP2_1)—Offset 1E88h

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address Mask (TRP2ADDRM):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW	**Address (TRP2ADDR):** DWord-aligned address
1	0h RO	Reserved.
0	0h RW	**Trap and SMI Enable (TRP2EN):** When this bit is set to 1, then the trapping logic specified in this register is enabled.

41.1.8 I/O Trap Registers 2 (IOTRP2_2)—Offset 1E8Ch

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW	**Read-Write Mask (TRP2RWM):** When this bit is '1', the trapping logic will operate on both read and write cycles. When this bit is '0', the cycle must match the type specified in bit 48.
16	0h RW	**Read/Write (TRP2RW):** 1 = Read, 0 = Write, the value in this field does not matter if bit 49 is set.
15:8	0h RO	Reserved.
7:4	0h RW	**Byte Enable Mask (TRP2BEM):** A '1' in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
3:0	0h RW	**Byte Enables (TRP2BE):** Active-high, DWord-aligned byte enables

41.1.9 I/O Trap Registers 3 (IOTRP3_1)—Offset 1E90h

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address Mask (TRP3ADDRM):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:16	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
15:2	0h RW	**Address (TRP3ADDR):** DWord-aligned address
1	0h RO	Reserved.
0	0h RW	**Trap and SMI Enable (TRP3EN):** When this bit is set to 1, then the trapping logic specified in this register is enabled.

41.1.10 I/O Trap Registers 3 (IOTRP3_2)—Offset 1E94h

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW	**Read-Write Mask (TRP3RWM):** When this bit is '1', the trapping logic will operate on both read and write cycles. When this bit is '0', the cycle must match the type specified in bit 48.
16	0h RW	**Read/Write (TRP3RW):** 1 = Read, 0 = Write, the value in this field does not matter if bit 49 is set.
15:8	0h RO	Reserved.
7:4	0h RW	**Byte Enable Mask (TRP3BEM):** A '1' in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
3:0	0h RW	**Byte Enables (TRP3BE):** Active-high, DWord-aligned byte enables

41.1.11 I/O Trap Registers 4 (IOTRP4_1)—Offset 1E98h

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address Mask (TRP4ADDRM):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW	**Reserved (TRP4ADDR):** DWord-aligned address
1	0h RO	Reserved.
0	0h RW	**Trap and SMI Enable (TRP4EN):** When this bit is set to 1, then the trapping logic specified in this register is enabled.

41.1.12 I/O Trap Registers 4 (IOTRP4_2)—Offset 1E9Ch

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW	**Read-Write Mask (TRP4RWM):** When this bit is '1', the trapping logic will operate on both read and write cycles. When this bit is '0', the cycle must match the type specified in bit 48.
16	0h RW	**Read/Write (TRP4RW):** 1 = Read, 0 = Write, the value in this field does not matter if bit 49 is set.
15:8	0h RO	Reserved.
7:4	0h RW	**Byte Enable Mask (TRP4BEM):** A '1' in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
3:0	0h RW	**Byte Enables (TRP4BE):** Active-high, DWord-aligned byte enables

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42 eMMC Registers

42.1 eMMC Configuration Registers

This section contains the registers in Bus: 0, Device 26, Function 0.

Table 42-1. Summary of Bus: 0, Device: 26, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	DEVVENDID - Offset 0h	00008086h
4h	4	STATUSCOMMAND - Offset 4h	00100000h
8h	4	REVCLASSCODE - Offset 8h	08050100h
Ch	4	CLLATHEADERBIST - Offset Ch	00000000h
10h	4	BAR - Offset 10h	00000004h
14h	4	BAR_HIGH - Offset 14h	00000000h
18h	4	BAR1 - Offset 18h	00000004h
1Ch	4	BAR1_HIGH - Offset 1Ch	00000000h
2Ch	4	SUBSYSTEMID - Offset 2Ch	00000000h
30h	4	EXPANSION_ROM_BASEADDR - Offset 30h	00000000h
34h	4	CAPABILITYPTR - Offset 34h	00000080h
3Ch	4	INTERRUPTREG - Offset 3Ch	00000000h
80h	4	POWERCAPID - Offset 80h	00039001h
84h	4	PMECTRLSTATUS - Offset 84h	00000008h
90h	4	PCIDEVIDLE_CAP_RECORD - Offset 90h	F0140009h
94h	4	D0I3_CONTROL_SW_LTR_MMIO_REG - Offset 98h	01400010h
98h	4	D0I3_CONTROL_SW_LTR_MMIO_REG - Offset 98h	00008041h
9Ch	4	DEVICE_IDLE_POINTER_REG - Offset 9Ch	000081C1h
A0h	4	D0I3_MAX_POW_LAT_PG_CONFIG - Offset A0h	00290800h
B0h	4	GEN_REGRW1 - Offset B0h	00000000h
B4h	4	GEN_REGRW2 - Offset B4h	00000000h
B8h	4	GEN_REGRW3 - Offset B8h	00000000h
BCh	4	GEN_REGRW4 - Offset BCh	00000000h
C0h	4	GEN_INPUT_REG - Offset C0h	00000000h

42.1.1 DEVVENDID - Offset 0h

Vendor ID Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 0h	00008086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**DEVICEID:** DEVICEID
15:0	8086h RO	**VENDORID:** VENDORID

42.1.2 STATUSCOMMAND - Offset 4h

PCI Command Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 4h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW/1C	**RMA:** RMA
28	0h RW/1C	**RTA:** RTA
27:21	0h RO	**Reserved**
20	1h RO	**CAPLIST:** CAPLIST
19	0h RO	**INTR_STATUS:** INTR_STATUS
18:11	0h RO	**Reserved**
10	0h RW	**INTR_DISABLE:** INTR_DISABLE
9	0h RO	**Reserved**
8	0h RW	**SERR_ENABLE:** SERR_ENABLE
7:3	0h RO	**Reserved**
2	0h RW	**BME:** BME
1	0h RW	**MSE:** MSE
0	0h RO	**Reserved**

42.1.3 REVCLASSCODE - Offset 8h

Revision ID Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 8h	08050100h

Bit Range	Default & Access	Field Name (ID): Description
31:8	080501h RO	**CLASS_CODES:** CLASS_CODES
7:0	00h RO	**RID:** RID

42.1.4 CLLATHEADERBIST - Offset Ch

Cache Line Latency Header and BIST Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**MULFNDEV:** MULFNDEV
22:16	00h RO	**HEADERTYPE:** HEADERTYPE
15:8	00h RO	**LATTIMER:** LATTIMER
7:0	00h RW	**CACHELINE_SIZE:** CACHELINE_SIZE

42.1.5 BAR - Offset 10h

BAR -Base Address Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 10h	00000004h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**BASEADDR:** BASEADDR
11:4	00h RO	**SIZEINDICATOR:** SIZEINDICATOR
3	0h RO	**PREFETCHABLE:** PREFETCHABLE

Bit Range	Default & Access	Field Name (ID): Description
2:1	2h RO	**TYPE:** TYPE
0	0h RO	**MESSAGE_SPACE:** MESSAGE_SPACE

42.1.6 BAR_HIGH - Offset 14h

BAR -Base Address Register High

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**BASEADDR_HIGH:** BASEADDR_HIGH

42.1.7 BAR1 - Offset 18h

BAR1 -Base Address Register1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 18h	00000004h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**BASEADDR1:** BASEADDR1
11:4	00h RO	**SIZEINDICATOR1:** SIZEINDICATOR1
3	0h RO	**PREFETCHABLE1:** PREFETCHABLE1
2:1	2h RO	**TYPE1:** TYPE1
0	0h RO	**MESSAGE_SPACE1:** MESSAGE_SPACE1

42.1.8 BAR1_HIGH - Offset 1Ch

BAR1 -Base Address Register1 High

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**BASEADDR1_HIGH:** BASEADDR1_HIGH

42.1.9 SUBSYSTEMID - Offset 2Ch

SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**SUBSYSTEMID:** SUBSYSTEMID
15:0	0000h RW/O	**SUBSYSTEMVENDORID:** SUBSYSTEMVENDORID

42.1.10 EXPANSION_ROM_BASEADDR - Offset 30h

Expansion ROM Base Address Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** EXPANSION_ROM_BASE

42.1.11 CAPABILITYPTR - Offset 34h

Capabilities Pointer Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 34h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**CAPPTR_POWER:** CAPPTR_POWER

42.1.12 INTERRUPTREG - Offset 3Ch

Interrupt Line Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**MAX_LAT:** MAX_LAT
23:16	00h RO	**MIN_GNT:** MIN_GNT
15:12	0h RO	**Reserved**
11:8	0h RO	**INTPIN:** INTPIN
7:0	00h RW	**INTLINE:** INTLINE

42.1.13 POWERCAPID - Offset 80h

Power Management Capability ID Regsiter

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 80h	00039001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**PMESUPPORT:** PMESUPPORT
26:19	0h RO	**Reserved**
18:16	3h RO	**VERSION:** VERSION
15:8	90h RO	**NXTCAP:** NXTCAP
7:0	01h RO	**POWER_CAP:** POWER_CAP

42.1.14 PMECTRLSTATUS - Offset 84h

Power Management Control and Status Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 84h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C	**PMESTATUS:** PMESTATUS
14:9	0h RO	**Reserved**
8	0h RW	**PMEENABLE:** PMEENABLE
7:4	0h RO	**Reserved**
3	1h RO	**NO_SOFT_RESET:** NO_SOFT_RESET
2	0h RO	**Reserved**
1:0	0h RW	**POWERSTATE:** POWERSTATE

42.1.15 PCIDEVIDLE_CAP_RECORD - Offset 90h

PCI Device Idle Capability Record Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 90h	F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**VEND_CAP:** VEND_CAP
27:24	0h RO	**REVID:** REVID
23:16	14h RO	**CAP_LENGTH:** CAP_LENGTH
15:8	00h RO	**NEXT_CAP:** NEXT_CAP
7:0	09h RO	**CAPID:** CAPID

42.1.16 DEVID_VEND_SPECIFIC_REG - Offset 94h

Device ID Vendor Specific Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 94h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**VSEC_LENGTH:** VSEC_LENGTH
19:16	0h RO	**VSEC_REV:** VSEC_REV
15:0	0010h RO	**VSECID:** VSECID

42.1.17 D0I3_CONTROL_SW_LTR_MMIO_REG - Offset 98h

SW LTR Update MMIO Location Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 98h	00008041h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000804h RO	**SW_LAT_DWORD_OFFSET:** SW_LAT_DWORD_OFFSET
3:1	0h RO	**SW_LAT_BAR_NUM:** SW_LAT_BAR_NUM
0	1h RO	**SW_LAT_VALID:** SW_LAT_VALID

42.1.18 DEVICE_IDLE_POINTER_REG - Offset 9Ch

Device IDLE Pointer Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + 9Ch	000081C1h

Bit Range	Default & Access	Field Name (ID): Description
31:4	000081Ch RO	**DWORD_OFFSET:** DWORD_OFFSET
3:1	0h RO	**BAR_NUM:** BAR_NUM
0	1h RO	**VALID:** VALID

42.1.19 D0I3_MAX_POW_LAT_PG_CONFIG - Offset A0h

Doi3 Max Power On Latency

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + A0h	00290800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	1h RW	**HAE:** HAE
20	0h RO	**Reserved**
19	1h RW	**SLEEP_EN:** SLEEP_EN
18	0h RW	**PGE:** PGE
17	0h RW	**I3_ENABLE:** I3_ENABLE
16	1h RW	**PMCRE:** PMCRE
15:13	0h RO	**Reserved**
12:10	2h RW/O	**POW_LAT_SCALE:** POW_LAT_SCALE
9:0	000h RW/O	**POW_LAT_VALUE:** POW_LAT_VALUE

42.1.20 GEN_REGRW1 - Offset B0h

General Purpose PCI RW Register1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW1:** GEN_REG_RW1

42.1.21 GEN_REGRW2 - Offset B4h

General Purpose PCI RW Register2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + B4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW2:** GEN_REG_RW2

42.1.22 GEN_REGRW3 - Offset B8h

General Purpose PCI RW Register3

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW3:** GEN_REG_RW3

42.1.23 GEN_REGRW4 - Offset BCh

General Purpose PCI RW Register4

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW4:** GEN_REG_RW4

42.1.24 GEN_INPUT_REG - Offset C0h

General Input Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:26, F:0] + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**GEN_REG_INPUT_RW:** GEN_REG_INPUT_RW

42.2 EMMC Memory Mapped Registers

These registers are memory mapped based on BAR0 defined in PCI configuration space.

Table 42-2. Summary of EMMC Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	SDMA System Address (sdmasysaddr)—Offset 0h	0h
4h	5h	Block Size (blocksize)—Offset 4h	0h
6h	7h	Block Count Register (blockcount)—Offset 6h	0h
8h	Bh	Argument 1 (argument1)—Offset 8h	0h
Ch	Dh	Transfer Mode Register (transfermode)—Offset Ch	0h
Eh	Fh	Command (command)—Offset Eh	0h
10h	13h	Response (Response 0 And 1)—Offset 10h	0h
14h	15h	Response 2 (response2)—Offset 14h	0h
16h	17h	Response 3 (response3)—Offset 16h	0h
18h	19h	Response 4 (response4)—Offset 18h	0h
1Ah	1Bh	Response 5 (response5)—Offset 1Ah	0h
1Ch	1Dh	Response 6 (response6)—Offset 1Ch	0h
1Eh	1Fh	Response 7 (response7)—Offset 1Eh	0h
20h	23h	Buffer Data Port Register (dataport)—Offset 20h	0h
24h	27h	Present State (PRESENTSTATE)—Offset 24h	1FF00000h
28h	28h	Host Control 1 (hostcontrol1)—Offset 28h	0h
29h	29h	Power Control Register (powercontrol)—Offset 29h	0h
2Ah	2Ah	Block Gap Control Register (blockgapcontrol)—Offset 2Ah	80h
2Bh	2Bh	Wakeup Control (wakeupcontrol)—Offset 2Bh	0h
2Ch	2Dh	Clock Control (clockcontrol)—Offset 2Ch	0h
2Eh	2Eh	Timeout Control (timeoutcontrol)—Offset 2Eh	0h
2Fh	2Fh	Software Reset (softwarereset)—Offset 2Fh	0h
30h	31h	Normal Interrupt Status (normalintrsts)—Offset 30h	0h
32h	33h	Error Interrupt Status (errorintrsts)—Offset 32h	0h
34h	35h	Normal Interrupt Status Enable (normalintrstsena)—Offset 34h	0h
36h	37h	Error Interrupt Status Enable (errorintrstsena)—Offset 36h	0h
38h	39h	Normal Interrupt Signal Enable (normalintrsigena)—Offset 38h	0h
3Ah	3Bh	(errorintrsigena)—Offset 3Ah	0h
3Ch	3Dh	Auto CMD12 Error Status (autocmderrsts)—Offset 3Ch	0h
3Eh	3Fh	Host Control 2 (hostcontrol2)—Offset 3Eh	0h
40h	47h	(capabilities)—Offset 40h	74462C881h
48h	4Fh	(maxcurrentcap)—Offset 48h	0h
50h	51h	(ForceEventforAUTOCMDErrorStatus)—Offset 50h	0h
52h	53h	Force Event Register for Error Interrupt Status (forceeventforerrintsts)—Offset 52h	0h
54h	54h	ADMA Error Status (admaerrsts)—Offset 54h	0h

Table 42-2. Summary of EMMC Memory Mapped Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
58h	5Bh	ADMA System Address Register 1 (admasysaddr01)—Offset 58h	0h
5Ch	5Dh	ADMA System Address Register2 (admasysaddr2)—Offset 5Ch	0h
60h	61h	Preset Value for Initialization (presetvalue0)—Offset 60h	4h
62h	63h	Preset Preset Value for Default Speed (presetvalue1)—Offset 62h	0h
64h	65h	Preset Value for High Speed (presetvalue2)—Offset 64h	0h
66h	67h	Preset Value for SDR12 (presetvalue3)—Offset 66h	0h
68h	69h	Preset Value for SDR25 (presetvalue4)—Offset 68h	0h
6Ah	6Bh	Preset Value for SDR50 (presetvalue5)—Offset 6Ah	0h
6Ch	6Dh	Preset Value for SDR104 (presetvalue6)—Offset 6Ch	0h
6Eh	6Fh	Preset Value for DDR50 (presetvalue7)—Offset 6Eh	0h
70h	73h	Boot Timeout Control (boottimeoutcnt)—Offset 70h	0h
74h	75h	PRESETVALUE8 Reg (PRESETVALUE8) — Offset 74h	0h
78h	79h	VENDREG Reg (VENDREG) — Offset 78h	0h
FCh	FDh	Slot Interrupt Status (slotintrsts)—Offset FCh	0h
FEh	FFh	HOSTCONTROLLERVER Reg (HOSTCONTROLLERVER) — Offset FEh	1002h

42.2.1 SDMA System Address (sdmasysaddr)—Offset 0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SDMA System Address Register/Argument2 Register (sdma_sysaddress):** This register contains the physical system memory address used for DMA transfers or the second argument for the Auto CMD23. 1) SDMA System Address: This register contains the system memory address for a SDMA transfer. When the Host Controller stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. 2) Argument 2: This register is used with the Auto CMD23 to set a 32-bit block count value to the argument of the CMD23 while executing Auto CMD23.

42.2.2 Block Size (blocksize)—Offset 4h

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14:12	0h RW	**Host DMA Buffer Size (host_sdma_buf_size):** To perform long DMA transfer, System Address register shall be updated at every system boundary during DMA transfer. These bits specify the size of contiguous buffer in the system memory. The DMA transfer shall wait at the every boundary specified by these fields and the HC generates the DMA Interrupt to request the HD to update the System Address register. These bits shall support when the DMA Support in the Capabilities register is set to 1 and this function is active when the DMA Enable in the Transfer Mode register is set to 1. 000b - 4KB(Detects A11 Carry out) 001b - 8KB(Detects A12 Carry out) 010b - 16KB(Detects A13 Carry out) 011b - 32KB(Detects A14 Carry out) 100b - 64KB(Detects A15 Carry out) 101b -128KB(Detects A16 Carry out) 110b - 256KB(Detects A17 Carry out) 111b - 512KB(Detects A18 Carry out)
11:0	0h RW	**Transfer Block Size (xfer_blocksize):** This register specifies the block size for block data transfers for CMD17, CMD18, CMD24, CMD25, and CMD53. It can be accessed only if no transaction is executing. Read operations during transfer return an invalid value and write operations shall be ignored. 0000h - No Data Transfer 0001h - 1 Byte 0002h - 2 Bytes 0003h - 3 Bytes 0004h - 4 Bytes 01FFh - 511 Bytes 0200h - 512 Bytes 0800h - 2048 Bytes

42.2.3 Block Count Register (blockcount)—Offset 6h

This register is enabled when Block Count Enable in the Transfer Mode register is set to 1 and is valid only for multiple block transfers. The HC decrements the block count after each block transfer and stops when the count reaches zero.
0000h - Stop Count
0001h - 1 block
0002h - 2 blocks
FFFFh - 65535 blocks.

Access Method

Type: MEM Register (Size: 16 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Block Count (block_cnt_16bit)**

42.2.4 Argument 1 (argument1)—Offset 8h

The SD/eMMC Command Argument is specified as bit39- 8 of Command-Format.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Command Argument 1 (command_argument1):** The Command Argument is specified as bit [39:8] of Command-Format

42.2.5 Transfer Mode Register (transfermode)—Offset Ch

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	Reserved.
5	0h RW	**Multi / Single Block Select (xfermode_multiblksel):** This bit enables multiple block data transfers. 0 - Single Block 1 - Multiple Block.
4	0h RW	**Data Transfer Direction Select (xfermode_dataxferdir):** This bit defines the direction of data transfers. 0 - Write (Host to Card) 1 - Read (Card to Host)
3:2	0h RW	**Auto CMD Enable (xfermode_autocmdena):** This field determines use of auto command functions 00b - Auto Command Disabled 01b - Auto CMD12 Enable 10b - Auto CMD23 Enable.
1	0h RW	**Block Count Enable (xfermode_blkcntena):** This bit is used to enable the Block count register, which is only relevant for multiple block transfers. When this bit is 0, the Block Count register is disabled, which is useful in executing an infinite transfer. 0 - Disable 1 - Enable.
0	0h RW	**DMA Enable (xfermode_dmaenable):** If this bit is set to 1, a DMA operation shall begin when the HD writes to the upper byte of Command register (00Fh). 0 - Disable 1 - Enable.

42.2.6 Command (command)—Offset Eh

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	Reserved.
13:8	0h RW	**Command Index (command_cmdindex):** This bit shall be set to the command number (CMD0-63, ACMD0-63).
7:6	0h RW	**Command Type (command_cmdtype):** There are three types of special commands. Suspend, Resume and Abort. These bits shall be set to 00b for all other commands. 00b - Normal 01b - Suspend 10b - Resume 11b - Abort
5	0h RW	**Data Present Select (command_datapresent):** This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line. If is set to 0 for the following: 1. Commands using only CMD line(ex. CMD52) 2. Commands with no data transfer but using busy signal on DAT[0] line (R1b or R5b ex. CMD38) 3. Resume Command 0 - No Data Present 1 - Data Present
4	0h RW	**Command Index Check Enable (command_indexchkena):** If this bit is set to 1, the HC shall check the index field in the response to see if it has the same value as the command index.
3	0h RW	**Command CRC Check Enable (command_crcchkena):** If this bit is set to 1, the HC shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked. 0 - Disable 1 – Enable
2	0h RO	Reserved.
1:0	0h RW	**Response Type Select (command_responsetype):** 00 - No Response 01 - Response length 136 10 - Response length 48 11 - Response length 48 check Busy after response

42.2.7 Response (Response 0 And 1)—Offset 10h

The response registers contains the 128 bit response received from the External Device.
There are 8 response registers:
Response 0: offset 10h
Response 1: offset 12h
Response 2: offset 14h
Response 3: offset 16h
Response 4: offset 18h
Response 5: offset 1Ah
Response 6: offset 1Ch
Response 7: offset 1Eh

Register details:
Response Register 0 and 1 = Response [31:0]
Response Register 2 and 3 = Response [63:32]
Response Register 4 and 5 = Response [95:64]
Response Register 6 and 7 = Response [127:96]

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Command Response 31_0 (command_response_31_0):** Response bits [31:0]

42.2.8 Response 2 (response2)—Offset 14h

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO	**Command Response 47_32 (command_response_47_32):** Response bits [47:32]

42.2.9 Response 3 (response3)—Offset 16h

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO	**command Response 63_48 (command_response_63_48):** Response bits [63:48]

42.2.10 Response 4 (response4)—Offset 18h

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO	**Command Response 79_64 (command_response_79_64):** Response bits [79:64]

42.2.11 Response 5 (response5)—Offset 1Ah

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO	**Command Response 95_80 (command_response_95_80):** Response bits [95:80]

42.2.12 Response 6 (response6)—Offset 1Ch

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO	**Command Response 111_96 (command_response_111_96):** Response bits [111:96]

42.2.13 Response 7 (response7)—Offset 1Eh

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO	**Command Response 127_112 (command_response_127_112):** Response bits [127:112]

42.2.14 Buffer Data Port Register (dataport)—Offset 20h

The Host Controller Buffer can be accessed through this 32-bit Data Port Register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data Port (sdhcdmactrl_piobufrddata):** The Host Controller Buffer can be accessed through this 32-bit Data Port Register.

42.2.15 Present State (PRESENTSTATE)—Offset 24h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1FF00000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:25	Fh RO	**DAT4 Line Signal Level (sdif_dat4in_dsync):** sdif_dat4in_dsync
24	1h RO	**CMD Line Signal Level (sdif_cmdin_dsync):** This status is used to check CMD line level to recover from errors, and for debugging
23:20	Fh RO	**DAT0 Line Signal Level (sdif_dat0in_dsync):** This status is used to check DAT line level to recover from errors, and for debugging.
19	0h RO	**Write Protect Switch Pin Level (sdif_wp_dsync):** The Write Protect Switch is supported for memory and combo cards. This bit reflects the SDWP# pin. 0 - Write protected (SDWP# = 0) 1 - Write enabled (SDWP# = 1).
18	0h RO	**Card Level Detect (sdif_cd_n_dsync):** This bit reflects the inverse value of the SDCD# pin. 0 - No Card present (SDCD# = 1) 1 - Card present (SDCD# = 0).
17	0h RO	**Card State Stable (sdhccarddet_statestable_dsync):** This bit is used for testing. If it is 0, the Card Detect Pin Level is not stable. If this bit is set to 1, it means the Card Detect Pin Level is stable. The Software Reset For All in the Software Reset Register shall not affect this bit. 0 - Reset of Debouncing 1 - No Card or Inserted.
16	0h RO	**Card Inserted (sdhccarddet_inserted_dsync):** This bit indicates whether a card has been inserted. Changing from 0 to 1 generates a Card Insertion Interrupt in the Normal Interrupt Status register and changing from 1 to 0 generates a Card Removal Interrupt in the Normal Interrupt Status register.
15:12	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**Buffer Read Enable (sdhcdmactrl_piobufrdena):** This status is used for non-DMA read transfers. This read only flag indicates that valid data exists in the host side buffer status. If this bit is 1, readable data exists in the buffer. A change of this bit from 1 to 0 occurs when all the block data is read from the buffer. A change of this bit from 0 to 1 occurs when all the block data is ready in the buffer and generates the Buffer Read Ready Interrupt. 0 - Read Disable 1 - Read Enable
10	0h RO	**Buffer Write Enable (sdhcdmactrl_piobufwrena):** This status is used for non-DMA write transfers. This read only flag indicates if space is available for write data. If this bit is 1, data can be written to the buffer. A change of this bit from 1 to 0 occurs when all the block data is written to the buffer.
9	0h RO	**Read Transfer Active (sdhcdmactrl_rdxferactive):** This status is used for detecting completion of a read transfer. This bit is set to 1 for either of the following conditions: • After the end bit of the read command • When writing a 1 to continue Request in the Block Gap Control register to restart a read transfer. This bit is cleared to 0 for either of the following conditions: • When the last data block as specified by block length is transferred to the system. • When all valid data blocks have been transferred to the system and no current block transfers are being sent as a result of the Stop At Block Gap Request set to 1. A transfer complete interrupt is generated when this bit changes to 0. 1 - Transferring data 0 - No valid data
8	0h RO	**Write Transfer Active (sdhcdmactrl_wrxferactive):** This status indicates a write transfer is active. If this bit is 0, it means no valid write data exists in the HC. This bit is set in either of the following cases: • After the end bit of the write command. • When writing a 1 to Continue Request in the Block Gap Control register to restart a write transfer. This bit is cleared in either of the following cases: • After getting the CRC status of the last data block as specified by the transfer count (Single or Multiple) • After getting a CRC status of any block where data transmission is about to be stopped by a Stop At Block Gap Request. During a write transaction, a Block Gap Event interrupt is generated when this bit is changed to 0, as a result of the Stop At Block Gap Request being set. This status is useful for the HD in determining when to issue commands during write busy. 1 - transferring data 0 - No valid data
7:4	0h RO	Reserved.
3	0h RO	**Re-Tuning Request (Re-Tune):** Host Controller may request Host Driver to execute re-tuning sequence by setting this bit when the data window is shifted by temperature drift and any issue receiving the correct data. This bit is cleared when a command is issued with setting Execute Tuning in the Host Control 2 register. Changing of this bit from 0 to 1 generates Re-Tuning Event. This bit is cleared when a command is issued with setting Execute Tuning in the Host Control 2 register. Changing of this bit from 0 to 1 generates Re-Tuning Event. Refer to Normal Interrupt registers for more detail. This bit isn't set to 1 if Sampling Clock Select in the Host Control 2 register is set to 0 (using fixed sampling clock). 1: Sampling clock needs re-tuning 0: Fixed or well tuned sampling clock
2	0h RO	**DATA line Active (Data Activity):** This bit indicates whether one of the DAT line on SD bus is in use. 1 - DAT line active 0 - DAT line inactive
1	0h RO	**Command Inhibit (DAT) (presentstate_inhibitdat):** This status bit is generated if either the DAT Line Active or the Read transfer Active is set to 1. If this bit is 0, it indicates the HC can issue the next SD command. Commands with busy signal belong to Command Inhibit (DAT). Changing from 1 to 0 generates a Transfer Complete interrupt in the Normal interrupt status register.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**Command Inhibit (CMD) (presentstate_inhibitcmd):** If this bit is 0, it indicates the CMD line is not in use and the HC can issue a SD command using the CMD line. This bit is set immediately after the Command register (00Fh) is written. This bit is cleared when the command response is received. Even if the Command Inhibit (DAT) is set to 1, Commands using only the CMD line can be issued if this bit is 0. Changing from 1 to 0 generates a Command complete interrupt in the Normal Interrupt Status register. If the HC cannot issue the command because of a command conflict error or because of Command Not Issued By Auto CMD12 Error, this bit shall remain 1 and the Command Complete is not set. Status issuing Auto CMD12 is not read from this bit. Auto CMD12 and Auto CMD23 consist of two responses. In this case, this bit is not cleared by the response of CMD12 or CMD23 but cleared by the response of a read/ write command. Status issuing Auto CMD12 is not read from this bit. So if a command is issued during Auto CMD12 operation, Host Controller shall manage to issue two commands: CMD12 and a command set by Command register.

42.2.16 Host Control 1 (hostcontrol1)—Offset 28h

Access Method

Type: MEM Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Card Detect Signal Detection (hostctrl1_cdsigselect):** This bit selects source for card detection. 1- The card detect test level is selected 0- SDCD# is selected (for normal use).
6	0h RW	**Card Detect Test Level (hostctrl1_cdtestlevel):** This bit is enabled while the Card Detect Signal Selection is set to 1 and it indicates card inserted or not. Generates (card ins or card removal) interrupt when the normal int sts enable bit is set. 1 - Card Inserted 0 - No Card.
5	0h RW	**Extended Data Transfer Width (hostctrl1_extdatawidth):** This bit controls 8-bit bus width mode for embedded device. Support of this function is indicated in 8-bit Support for Embedded Device in the Capabilities register. If a device supports 8-bit bus mode, this bit may be set to 1. If this bit is 0, bus width is controlled by Data Transfer Width in the Host Control 1 register.
4:3	0h RW	**DMA Select (hostctrl1_dmaselect):** One of supported DMA modes can be selected. The host driver shall check support of DMA modes by referring the Capabilities register. 00 - SDMA is selected 01 - 32-bit Address ADMA1 is selected 10 - 32-bit Address ADMA2 is selected 11 - 64-bit Address ADMA2 is selected.
2	0h RW	**High Speed Enable (hostctrl1_highspeedena):** This bit is optional. Before setting this bit, the HD shall check the High Speed Support in the capabilities register. If this bit is set to 0 (default), the HC outputs CMD line and DAT lines at the falling edge of the SD clock (up to 25 MHz/ 20MHz for MMC). If this bit is set to 1, the HC outputs CMD line and DAT lines at the rising edge of the SD clock (up to 50 MHz for SD/52MHz for MMC)/ 208Mhz.
1	0h RW	**Data Transfer Width (hostctrl1_datawidth):** This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card. 1 - 4 bit mode 0 - 1 bit mode.
0	0h RW	**LED Control (hostctrl1_ledcontrol):** This bit is used to caution the user not to remove the card while the SD card is being accessed. If the software is going to issue multiple SD commands, this bit can be set during all transactions. It is not necessary to change for each transaction. 1 - LED on 0 - LED off.

42.2.17 Power Control Register (powercontrol)—Offset 29h

This register is used to program the Bus power and voltage level

Access Method

Type: MEM Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	Reserved.
4	0h RW	**eMMC HW Reset (emmc_hwreset):** Hardware reset signal is generated for eMMC card when this bit is set 1 - Drives the hardware reset pin as ZERO (Active LOW to eMMC card) 0 - Deassert the hardware reset pin.
3:1	0h RW	**SD Bus Voltage Select (pwrctrl_sdbusvoltage):** By setting these bits, the HC selects the voltage level for the SD card. Before setting this register, the HC shall check the voltage support bits in the capabilities register. If unsupported voltage is selected, the Host System shall not supply SD bus voltage 111b - 3.3 V 110b - 3.0 V 101b - 1.8 V.
0	0h RW	**Bus Power (pwrctrl_sdbuspower):** Before setting this bit, the SD host driver shall set SD Bus Voltage Select. If the HC detects the No Card State, this bit shall be cleared. 1 - Power on 0 - Power off.

42.2.18 Block Gap Control Register (blockgapcontrol)—Offset 2Ah

This register is used to program the block gap request, read wait control and interrupt at block gap.

Access Method

Type: MEM Register
(Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
7	1h RW	**Boot Acknowledge Check (boot_ack_chk):** To check for the boot acknowledge in boot operation. 1 - wait for boot ack from eMMC card 0 - Will not wait for boot ack from eMMC card.
6	0h RW	**Alternate Boot Enable (alt_boot_en):** To start boot code access in alternative mode. 1- To start alternate boot mode access 0 - To stop alternate boot mode access.
5	0h RW	**Boot Code Access (BOOT_EN):** To start boot code access 1- To start boot code access 0 - To stop boot code access
4	0h RW	**SPI mode enable (spi_mode):** SPI mode enable bit. 1- SPI mode 0 - SD mode

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	Reserved.
2	0h RW	**Read Wait Control (rd_wait_ctrl):** The read wait function is optional for SDIO cards. If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using DAT[2] line. Otherwise the HC has to stop the SD clock to hold read data, which restricts commands generation. When the HD detects a card insertion, it shall set this bit according to the CCCR of the card. If the card does not support read wait, this bit shall never be set to 1 otherwise DAT line conflict may occur. If this bit is set to 0, Suspend / Resume cannot be supported 1 - Enable Read Wait Control 0 - Disable Read Wait Control
1	0h RW	**Continue Request (continue_req):** This bit is used to restart a transaction which was stopped using the Stop At Block Gap Request. To cancel stop at the block gap, set Stop At block Gap Request to 0 and set this bit to restart the transfer. The HC automatically clears this bit in either of the following cases: 1) In the case of a read transaction, the DAT Line Active changes from 0 to 1 as a read transaction restarts. 2) In the case of a write transaction, the Write transfer active changes from 0 to 1 as the write transaction restarts.
0	0h RW	**Stop At Block Gap Request (stopatblkgap_req):** This bit is used to stop executing a transaction at the next block gap for non- DMA,SDMA and ADMA transfers. Until the transfer complete is set to 1, indicating a transfer completion the HD shall leave this bit set to 1. Clearing both the Stop At Block Gap Request and Continue Request shall not cause the transaction to restart.

42.2.19 Wakeup Control (wakeupcontrol)—Offset 2Bh

This register is used to program the wakeup functionality.

Access Method

Type: MEM Register (Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h RW	**Wakeup Event On SD Card Removal (wkupctrl_cardremoval):** This bit enables wakeup event via Card Removal assertion in the Normal Interrupt Status register. FN_WUS (Wake up Support) in CIS does not affect this bit. 1 - Enable 0 – Disable.
1	0h RW	**Wakeup On Card Insertion (wkupctrl_cardinsertion):** This bit enables wakeup event via Card Insertion assertion in the Normal Interrupt Status register. FN_WUS (Wake up Support) in CIS does not affect this bit. 1 - Enable 0 – Disable
0	0h RW	**Wakeup Event Enable On Card Interrupt (wkupctrl_cardinterrupt):** This bit enables wakeup event via Card Interrupt assertion in the Normal Interrupt Status register. This bit can be set to 1 if FN_WUS (Wake Up Support) in CIS is set to 1. 1 - Enable 0 - Disable.

42.2.20 Clock Control (clockcontrol)—Offset 2Ch

This register is used to program the Clock frequency select, generator select, Clock enable,Internal Clock state fields.

Access Method

Type: MEM Register (Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**SDCLK Frequency Select (clkctrl_sdclkfreqsel):** This register is used to select the frequency of the SDCLK pin. The frequency is not programmed directly; rather this register holds the divisor of the Base Clock Frequency For SD clock in the capabilities register. Only the following settings are allowed. 80h - base clock divided by 256 40h - base clock divided by 128 20h - base clock divided by 64 10h - base clock divided by 32 08h - base clock divided by 16 04h - base clock divided by 8 02h - base clock divided by 4 01h - base clock divided by 2 00h - base clock(10MHz-63MHz) Setting 00h specifies the highest frequency of the SD Clock.
7:6	0h RW	**Upper Bits of SDCLK Frequency Select (clkctrl_sdclkfreqsel_upperbits):** Bit 07-06 is assigned to bit 09-08 of clock divider in SDCLK Frequency Select.
5	0h RW	**Clock Generator Select (clkctrl_clkgensel):** This bit is used to select the clock generator mode in SDCLK Frequency Select. If the Programmable Clock Mode is supported (non-zero value is set to Clock Multiplier in the Capabilities register), this bit attribute is RW, and if not supported,this bit attribute is RO and zero is read. This bit depends on the setting of Preset Value Enable in the Host Control 2 register. If the Preset Value Enable = 0, this bit is set by Host Driver. If the Preset Value Enable = 1, this bit is automatically set to a value specified in one of Preset Value registers. 1: Programmable Clock Mode 0: Divided Clock Mode.
4:3	0h RO	Reserved.
2	0h RW	**SD Clock Enable (clkctrl_sdclkena):** The HC shall stop SDCLK when writing this bit to 0. SDCLK frequency Select can be changed when this bit is 0.
1	0h RO	**Internal Clock Stable (sdhcclkgen_intclkstable_dsync):** This bit is set to 1 when SD clock is stable after writing to Internal Clock Enable in this register to 1. The SD Host Driver shall wait to set SD Clock Enable until this bit is set to 1.
0	0h RW	**Internal Clock Enable (clkctrl_intclkena):** This bit is set to 0 when the HD is not using the HC or the HC awaits a wakeup event. The HC should stop its internal clock to go very low power state. 1 - Oscillate 0 - Stop.

42.2.21 Timeout Control (timeoutcontrol)—Offset 2Eh

This value determines the interval by which DAT line time-outs are detected. Refer to the Data Time-out Error in the Error Interrupt Status register for information on factors that dictate time-out generation. Time-out clock frequency will be generated by dividing the sd clock TMCLK by this value. When setting this register, prevent inadvertent time-out events by clearing the Data Time-out Error Status Enable (in the Error Interrupt Status Enable register)
1110 - TMCLK * 2^27
0001 - TMCLK * 2^14
0000 - TMCLK * 2^13.

Access Method

Type: MEM Register (Size: 8 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	Reserved.
3:0	0h RW	**Data Timeout Counter Value (timeout_ctrvalue):** This value determines the interval by which DAT line time-outs are detected. Refer to the Data Time-out Error in the Error Interrupt Status register for information on factors that dictate time-out generation. Time-out clock frequency will be generated by dividing the sd clock TMCLK by this value. When setting this register, prevent inadvertent time-out events by clearing the Data Time-out Error Status Enable (in the Error Interrupt Status Enable register) 1111 - Reserved 1110 - TMCLK * 2^27 ---------- ---------- 0001 - TMCLK * 2^14 0000 - TMCLK * 2^13

42.2.22 Software Reset (softwarereset)—Offset 2Fh

This register is used to program the software reset for data, command and for all.

Access Method

Type: MEM Register (Size: 8 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h RW	**Software Reset for DAT Line (swreset_for_dat):** Only part of data circuit is reset. The following registers and bits are cleared by this bit: Buffer Data Port Register - Buffer is cleared and initialized. Present State register - Buffer read Enable - Buffer write Enable - Read Transfer Active - Write Transfer Active - DAT Line Active - Command Inhibit (DAT) Block Gap Control register - Continue Request - Stop At Block Gap Request Normal Interrupt Status register - Buffer Read Ready - Buffer Write Ready - Block Gap Event - Transfer Complete 1 - Reset 0 - Work.
1	0h RW	**Software Reset for CMD Line (swreset_for_cmd):** Only part of command circuit is reset. The following registers and bits are cleared by this bit: Present State register - Command Inhibit (CMD) Normal Interrupt Status register - Command Complete 1 - Reset 0 - Work.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Software Reset for All (swreset_for_all):** This reset affects the entire HC except for the card detection circuit. Register bits of type ROC, RW, RW1C, RWAC are cleared to 0. During its initialization, the HD shall set this bit to 1 to reset the HC. The HC shall reset this bit to 0 when capabilities registers are valid and the HD can read them. Additional use of Software Reset For All may not affect the value of the Capabilities registers. If this bit is set to 1, the SD card shall reset itself and must be re initialized by the HD. 1 - Reset 0 - Work

42.2.23 Normal Interrupt Status (normalintrsts)—Offset 30h

This register gives the status of all the interrupts

Access Method

Type: MEM Register (Size: 16 bits)

Device:

Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Error Interrupt (reg_errorintrsts):** If any of the bits in the Error Interrupt Status Register are set, then this bit is set. Therefore the HD can test for an error by checking this bit first. 0 - No Error 1 – Error.
14	0h RW1C	**Boot terminate Interrupt (normalintrsts_bootcomplete):** This status is set if the boot operation get terminated 0 - Boot operation is not terminated 1 - Boot operation is terminated.
13	0h RW1C	**Boot Acknowledge Rcv (normalintrsts_rcvbootack):** This status is set if the boot acknowledge is received from device. 0 - Boot ack is not received 1 - Boot ack is received.
12	0h RO	**Re-Tuning Event (normalintrsts_retuningevent):** This status is set if Re-Tuning Request in the Present State register changes from 0 to 1. Host Controller requests Host Driver to perform re-tuning for next data transfer. Current data transfer (not large block count) can be completed without retuning. 1 Re-Tuning should be performed 0 Re-Tuning is not required.
11	0h RO	**INT_C_ Status (normalintrsts_intc):** This status is set if INT_C is enabled and INT_C# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_C interrupt factor.
10	0h RO	**INT_B_Status (normalintrsts_intb):** This status is set if INT_B is enabled and INT_B# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_B interrupt factor.
9	0h RO	**INT_A Status (normalintrsts_inta):** This status is set if INT_A is enabled and INT_A# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_A interrupt factor.
8	0h RO	**Card Interrupt (normalintrsts_cardintsts):** In 1-bit mode, the HC shall detect the Card Interrupt without SD Clock to support wakeup. In 4-bit mode, the card interrupt signal is sampled during the interrupt cycle, so there are some sample delays between the interrupt signal from the card and the interrupt to the Host system. 0 - No Card Interrupt 1 - Generate Card Interrupt.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW1C	**Card Removal (normalintrsts_cardremsts):** This status is set if the Card Inserted in the Present State register changes from 1 to 0. When the HD writes this bit to 1 to clear this status the status of the Card Inserted in the Present State register should be confirmed. 0 - Card State Stable or Debouncing 1 - Card Removed.
6	0h RW1C	**Card Insertion (normalintrsts_cardinssts):** This status is set if the Card Inserted in the Present State register changes from 0 to 1.
5	0h RW/1C	**Buffer Read Ready (normalintrsts_bufrdready):** This status is set if the Buffer Read Enable changes from 0 to 1.
4	0h RW1C	**Buffer Write Ready (normalintrsts_bufwrready):** This status is set if the Buffer Write Enable changes from 0 to 1.
3	0h RW1C	**DMA Interrupt (normalintrsts_dmainterrupt):** This status is set if the HC detects the Host DMA Buffer Boundary in the Block Size Register.
2	0h RW1C	**Block Gap Event (normalintrsts_blkgapevent):** If the Stop At Block Gap Request in the Block Gap Control Register is set, this bit is set.
1	0h RW1C	**Transfer Complete (normalintrsts_xfercomplete):** This bit is set when a read / write transaction is completed.
0	0h RW1C	**Command Complete (normalintrsts_cmdcomplete):** This bit is set when we get the end bit of the command response (Except Auto CMD12 and Auto CMD23). 0 - No Command Complete 1 - Command Complete

42.2.24 Error Interrupt Status (errorintrsts)—Offset 32h

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12	0h RW/1C	**Target Response Error (errorintrsts_hosterror):** Occurs when detecting ERROR in DMA transaction 0 - no error 1 – error.
11:10	0h RO	Reserved.
9	0h RW	**ADMA Error (errorintrsts_admaerror):** This bit is set when the Host Controller detects errors during ADMA based data transfer. The state of the ADMA at an error occurrence is saved in the ADMA Error Status Register. 1- Error 0- No error.
8	0h RW	**Auto CMD Error (errorintrsts_autocmderror):** This bit is set when detecting that one of the bits D00-D04 in Auto CMD Error Status register has changed from 0 to 1.
7	0h RW	**Current Limit Error (errorintrsts_currlimiterror):** By setting the SD Bus Power bit in the Power Control Register, the HC is requested to supply power for the SD Bus.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Data End Bit Error (errorintrsts_dataendbiterror):** Occurs when detecting 0 at the end bit position of read data which uses the DAT line or the end bit position of the CRC status. 0 - No Error 1 – Error.
5	0h RW	**Data CRC Error (errorintrsts_datacrcerror):** Occurs when detecting CRC error when transferring read data which uses the DAT line or when detecting the Write CRC Status having a value of other than "010". 0 - No Error 1 – Error.
4	0h RW	**Data Timeout Error (errorintrsts_datatimeouterror):** Occurs when detecting one of following timeout conditions. 1. Busy Timeout for R1b, R5b type. 2. Busy Timeout after Write CRC status 3. Write CRC status Timeout 4. Read Data Timeout 0 - No Error 1 – Timeout.
3	0h RW	**Command Index Error (errorintrsts_cmdindexerror):** Occurs if a Command Index error occurs in the Command Response. 0 - No Error 1 – Error.
2	0h RW	**Command End Bit Error (errorintrsts_cmdendbiterror):** Occurs when detecting that the end bit of a command response is 0. 0 - No Error 1 - End Bit Error Generated.
1	0h RW	**Command CRC Error (errorintrsts_cmdcrcerror):** 0 - No Error 1 - CRC Error Generated.
0	0h RW	**Command Timeout Error (errorintrsts_cmdtimeouterror):** Occurs only if the no response is returned within 64 SDCLK cycles from the end bit of the command. 0 - No Error 1 – Timeout.

42.2.25 Normal Interrupt Status Enable (normalintrstsena)—Offset 34h

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RO	Reserved.
9	0h RW	**INT_A Status Enable (int_a_stsena):** If this bit is set to 0, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_A and may set this bit again after all interrupt requests to INT_A pin are cleared to prevent inadvertent interrupts.
8	0h RW	**Card Interrupt Status Enable (sdhcregset_cardintstsena):** If this bit is set to 0, the HC shall clear Interrupt request to the System. The Card Interrupt detection is stopped when this bit is cleared and restarted when this bit is set to 1.
7	0h RW	**Card Removal Status Enable (sdhcregset_cardremstsena):** This status is set if the Card Inserted in the Present State register changes from 1 to 0.
6	0h RW	**Card Insertion Status Enable (sdhcregset_cardinsstsena):** This status is set if the Card Inserted in the Present State register changes from 0 to 1.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Buffer Read Ready Status Enable (buffrd_readtstsena):** This status is set if the Buffer Read Enable changes from 0 to 1.
4	0h RW	**Buffer Write Ready Status Enable (buffwr_readtstsena):** This status is set if the Buffer Write Enable changes from 0 to 1.
3	0h RW	**DMA Interrupt Status Enable (dmaintrstsena):** This status is set if the HC detects the Host DMA Buffer Boundary in the Block Size register.
2	0h RW	**Block Gap Event Status Enable (blockgap_eventstsena):** If the Stop At Block Gap Request in the BlockGap Control Register is set, this bit is set.
1	0h RW	**Transfer Complete Status Enable (xfrcmpltstsena):** This bit is set when a read / write transaction is completed.
0	0h RW	**Command Complete Status Enable (cmdcmpltstsena):** This bit is set when we get the end bit of the command response.

42.2.26 Error Interrupt Status Enable (errorintrstsena)—Offset 36h

This register is used to enable the Error Interrupt Status register fields.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12	0h RO	**Transfer Response Error (xfrresponce_err):** xfrresponce_err
11	0h RO	Reserved.
10	0h RW	**Tuning error status enable (tune_errstsena):** 0 - Masked 1 - Enabled
9	0h RW	**ADMA Error Status Enable (adma_errstsena):** 0 - Masked 1 - Enabled
8	0h RW	**Auto CMD12 Error Status Enable (autocmd12_errstsena):** 0 - Masked 1 - Enabled
7	0h RW	**Current Limit Error Status Enable (currentlim_errstsena):** 0 - Masked 1 - Enabled
6	0h RW	**Data End Bit Error Status Enable (dataendbit_errstsena):** 0 - Masked 1 - Enabled
5	0h RW	**Data CRC Error Status Enable (datacrc_errstsena):** 0 - Masked 1 - Enabled

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Data Timeout Error Status Enable (datatimeout_errstsena):** 0 - Masked 1 - Enabled
3	0h RW	**Command Index Error Status Enable (cmdindex_errstsena):** 0 - Masked 1 - Enabled
2	0h RW	**Command End Bit Error Status Enable (cmdendbit_errstsena):** 0 - Masked 1 - Enabled
1	0h RW	**Command CRC Error Status Enable (cmdcrc_errstsena):** 0 - Masked 1 - Enabled
0	0h RW	**Command Timeout Error Status Enable (cmdtimeout_errstsena):** 0 - Masked 1 - Enabled

42.2.27 Normal Interrupt Signal Enable (normalintrsigena)—Offset 38h

This register is used to enable the Normal Interrupt Signal register. All the bits are RW, except for Reserved bits, and defined as follows:
0 - Masked
1 - Enabled.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Boot Terminate Interrupt Signal Enable (bootintr_sigena):** bootintr_sigena
13	0h RW	**Boot ack rcv Signal Enable (bootack_rcvsigena):** bootack_rcvsigena
12	0h RW	**Re-Tuning Event Signal Enable (retune_eventsigena):** retune_eventsigena
11	0h RW	**INT_C Signal Enable (int_c_sigena):** int_c_sigena
10	0h RW	**INT_B Signal Enable (int_b_sigena):** int_b_sigena
9	0h RW	**INT_A Signal Enable (int_a_sigena):** int_a_sigena
8	0h RW	**Card Interrupt Signal Enable (sdhcregset_cardintstsena):** sdhcregset_cardintstsena
7	0h RW	**Card Removal Signal Enable (sdhcregset_cardremstsena):** sdhcregset_cardremstsena

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Card Insertion Signal Enable (sdhcregset_cardinsstsena):** sdhcregset_cardinsstsena
5	0h RW	**Buffer Read Ready Signal Enable (buffrd_readtsigena):** buffrd_readtsigena
4	0h RW	**Buffer Write Ready Signal Enable (buffwr_readtsigena):** buffwr_readtsigena
3	0h RW	**DMA Interrupt Signal Enable (dmaintrsigena)**
2	0h RW	**Block Gap Event Signal Enable (blockgap_eventsigena)**
1	0h RW	**Transfer Complete Signal Enable (xfrcmpltsigena)**
0	0h RW	**Command Complete Signal Enable (cmdcmpltsigena)**

42.2.28 (errorintrsigena)—Offset 3Ah

This register is used to enable the Normal Interrupt Signal register. All the bits are RW, except for Reserved bits, and defined as follows:
0 - Masked
1 - Enabled.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RW	**Tuning Error Signal Enable (tune_errsigena):** tune_errsigena
9	0h RW	**ADMA Error Signal Enable (adma_errsigena):** adma_errsigena
8	0h RW	**Auto CMD Error Signal Enable (autocmd12_errsigena):** autocmd12_errsigena
7	0h RW	**Current Limit Error Signal Enable (currentlim_errsigena):** currentlim_errsigena
6	0h RW	**Data End Bit Error Signal Enable (dataendbit_errsigena):** dataendbit_errsigena
5	0h RW	**Data CRC Error Signal Enable (datacrc_errsigena):** datacrc_errsigena
4	0h RW	**Data Timeout Error Signal Enable (datatimeout_errsigena):** datatimeout_errsigena
3	0h RW	**Command Index Error Signal Enable (cmdindex_errsigena):** cmdindex_errsigena

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Command End Bit Error Signal Enable (cmdendbit_errsigena):** cmdendbit_errsigena
1	0h RW	**Command CRC Error Signal Enable (cmdcrc_errsigena):** cmdcrc_errsigena
0	0h RW	**Command Timeout Error Signal Enable (cmdtimeout_errsigena):** cmdtimeout_errsigena

42.2.29 Auto CMD12 Error Status (autocmderrsts)—Offset 3Ch

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7	0h RO	**Command Not Issued By Auto CMD12 Error (autocmderrsts_nexterror):** Setting this bit to 1 means CMD_wo_DAT is not executed due to an Auto CMD12 error(D04- D01) in this register. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23 0 – No Error 1 – Not Issued.
6:5	0h RO	Reserved.
4	0h RO	**Auto CMD Index Error (autocmderrsts_indexerror):** Occurs if the Command Index error occurs in response to a command. 0 – No Error 1 – Error
3	0h RO	**Auto CMD End Bit Error (autocmderrsts_endbiterror):** Occurs when detecting that the end bit of command response is 0. 0 – No Error 1 – End Bit Error Generated.
2	0h RO	**Auto CMD CRC Error (autocmderrsts_crcerror):** Occurs when detecting a CRC error in the command response. 0 – No Error 1 – CRC Error Generated.
1	0h RO	**Auto CMD Timeout Error (autocmderrsts_timeouterror):** Occurs if the no response is returned within 64 SDCLK cycles from the end bit of the command. If this bit is set to 1, the other error status bits (D04 - D02) are meaningless. 0 - No Error 1 - Timeout.
0	0h RO	**Auto CMD12 not Executed (autocmderrsts_notexecerror):** If memory multiple block data transfer is not started due to command error, this bit is not set because it is not necessary to issue Auto CMD12. Setting this bit to 1 means the HC cannot issue Auto CMD12 to stop memory multiple block transfer due to some error. 0 - Executed 1 - Not Executed.

42.2.30 Host Control 2 (hostcontrol2)—Offset 3Eh

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Preset Value Enable (hostctrl2_presetvalueenable):** Host Controller Version 3.00 supports this bit. As the operating SDCLK frequency and I/O driver strength depend on the Host System implementation, it is difficult to determine these parameters in the Standard Host Driver. When Preset Value Enable is set to automatic. This bit enables the functions defined in the Preset Value registers. 1 Automatic Selection by Preset Value are Enabled 0 SDCLK and Driver Strength are controlled by Host Driver.
14	0h RW	**Asynchronous Interrupt Enable (hostctrl2_asynchintrenable):** This bit can be set to 1 if a card support asynchronous interrupt and Asynchronous Interrupt Support is set to 1 in the Capabilities register. 0 – Disabled 1 – Enabled.
13:10	0h RO	Reserved.
9	0h RW	**Driver Strength Select (hostctrl2_driverstrength):** Host Controller output driver in 1.8V signaling is selected by this bit. In 3.3V signaling, this field is not effective.
8	0h RO	Reserved.
7	0h RW	**Sampling Clock Select (hostctrl2_samplingclkselect):** This bit is set by tuning procedure when Execute Tuning is cleared. Writing 1 to this bit is meaningless and ignored. Setting 1 means that tuning is completed successfully and setting 0 means that tuning is failed. Controller is receiving response or a read data block. 0 - Fixed clock is used to sample data 1 - Tuned clock is used to sample data
6	0h RW	**Execute Tuning (hostctrl2_executetuning):** This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to Sampling Clock Select. Tuning procedure is aborted by writing 0 for more detail about tuning procedure. 0 - Not Tuned or Tuning Completed 1 - Execute Tuning.
5:4	0h RO	Reserved.
3	0h RW	**1.8V Signaling Enable (hostctrl2_1p8vsignallingena):** This bit controls voltage regulator for I/O cell. 3.3V is supplied to the card regardless of signaling voltage. Setting this bit from 0 to 1 starts changing signal voltage from 3.3V to 1.8V.
2:0	0h RW	**UHS Mode Select (hostctrl2_uhsmodeselect):** This field is used to select one of UHS-I modes and effective when 1.8V Signaling Enable is set to 1. Select in the Clock Control register and Driver Strength Select according to Preset Value registers. In this case, one of preset value registers is selected by this field. Host Driver needs to reset SD Clock Enable before changing this field to avoid generating clock glitch. After setting this field, Host Driver sets SD Clock Enable again. 000b - SDR12 001b - SDR25 010b - SDR50 011b - SDR104 100b - DDR50 101b - HS400

42.2.31 (capabilities)—Offset 40h

This register provides the host driver with information specific to the host controller implementation. Please note, that the default values shown here assume no bypass of the capabilities register. In case software decides to bypass the default capabilities register values the reset values will present the bypassed value.

Access Method

Type: MEM Register
(Size: 64 bits)

Device:
Function:

Default: 74462C881h

Bit Range	Default & Access	Field Name (ID): Description
63:35	0h RO	Reserved.
34	1h RO	**DDR50 Support (corecfg_ddr50support):** This bit indicates whether DDR50 is supported. 0 –Not Supported 1 –Supported.
33	1h RO	**SDR104 Support (corecfg_sdr104support):** This bit indicates whether SDR104 is supported.SDR104 requires tuning. 0 –Not Supported 1 –Supported.
32	1h RO	**SDR50 Support (corecfg_sdr50support):** This bit indicates whether SDR50 is supported. 0 –Not Supported 1 –Supported.
31:30	1h RO	**Slot Type (corecfg_slottype):** This field indicates usage of a slot by a specific Host System. (A host controller register set is defined per slot.) Embedded slot for one device (01b) means that only one on-removable device is connected to a SD bus slot. Shared Bus Slot (10b) can be set if Host Controller supports Shared Bus Control register. The Standard Host Driver controls only a removable card or one embedded device is connected to a SD bus slot.
29	0h RO	**Asynchronous Interrupt Support (corecfg_asynchintrsupport):** This bit indicates whether the HC supports Asynchronous Interrupt 0 –Not Supported 1 –Supported.
28:27	0h RO	Reserved.
26	1h RO	**Voltage Support 1.8V (corecfg_1p8voltsupport):** This bit indicates whether the HC supports 1.8V. 0 –Not Supported 1 –Supported.
25	0h RO	**Voltage Support 3.0V (corecfg_3p0voltsupport):** This bit indicates whether the HC supports 3.0V. 0 –Not Supported 1 –Supported.
24	0h RO	**Voltage Support 3.3V (corecfg_3p3voltsupport):** This bit indicates whether the HC supports 3.3V. 0 –Not Supported 1 –Supported.
23	0h RO	Reserved.
22	1h RO	**SDMA Support (corecfg_sdmasupport):** This bit indicates whether the HC is capable of using DMA to transfer data between system memory and the HC directly. (SDMA Mode) 0 –Not Supported 1 –Supported
21	1h RO	**High Speed Support (corecfg_highspeedsupport):** This bit indicates whether the HC and the Host System support High Speed mode. 0 –Not Supported 1 –Supported
20:18	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
17:16	2h RO	**Max Block Length (corecfg_maxblklength):** This value indicates the maximum block size that the HD can read and write to the buffer in the HC. The buffer shall transfer this block size without wait cycles. Sizes can be defined as indicated below. 00 - 512 byte 01 - 1024 byte 10 - 2048 byte 11 - 4096 byte.
15:8	C8h RO	**Base Clock Frequency for SD Clock (corecfg_baseclkfreq):** (1) 6-bit Base Clock Frequency This mode is supported by the Host Controller Version 1.00 and 2.00. Upper 2- bit is not effective and always 0. Unit values are1MHz. The supported clock range is 10MHz to 63MHz. 0011 1111b 63MHz 0000 0010b 2MHz 0000 0001b 1MHz (2) 8-bit Base Clock Frequency This mode is supported by the Host Controller Version 3.00. Unit values are 1MHz. The supported clock range is 10MHz to 255MHz. FFh 255MHz 02h 2MHz 01h 1MHz.
7	1h RO	**Timeout Clock Unit (corecfg_timeoutclkunit):** This bit shows the unit of base clock frequency used to detect Data Timeout Error. 0 - KHz 1 - MHz.
6	0h RO	Reserved.
5:0	1h RO	**Timeout Clock Frequency (corecfg_timeoutclkfreq):** This bit shows the base clock frequency used to detect Data Timeout Error. Not 0 - 1Khz to 63Khz or 1Mhz to 63Mhz.

42.2.32 (maxcurrentcap)—Offset 48h

Maximum Current Capabilities

Access Method

Type: MEM Register (Size: 64 bits)

Device:

Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:24	0h RO	Reserved.
23:16	0h WO	**Maximum Current for 1.8V (corecfg_maxcurrent1p8v):** 0 – Get value via another method 1 – 4mA 2 – 8mA 3 – 12mA ... 255 – 1020mA
15:8	0h WO	**Maximum Current for 3.0V (corecfg_maxcurrent3p0v):** 0 – Get value via another method 1 – 4mA 2 – 8mA 3 – 12mA ... 255 – 1020mA

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h WO	**corecfg_maxcurrent3p3v:** 0 – Get value via another method 1 – 4mA 2 – 8mA 3 – 12mA ... 255 – 1020mA

42.2.33 (ForceEventforAUTOCMDErrorStatus)—Offset 50h

Force Event REGISTER for AUTO CMD Error Status

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7	0h RO	**forcecmdnotissuedbyautocmd12err:** Force Event for Command Not Issued by AUTO CMD12 Error 1 – Interrupt is generated 0 – No Interrupt
6:5	0h RO	Reserved.
4	0h RO	**forceautocmdindexerr:** Force Event for AUTO CMD Index Error 1 – Interrupt is generated 0 – No Interrupt
3	0h RO	**forceautocmdendbiterr:** Force Event for AUTO CMD End Bit Error 1 – Interrupt is generated 0 – No Interrupt
2	0h RO	**forceautocmdcrcerr:** Force Event for AUTO CMD Timeout Error 1 – Interrupt is generated 0 – No Interrupt
1	0h RO	**forceautocmdtimeouterr:** Force Event for AUTO CMD Timeout Error 1 – Interrupt is generated 0 – No Interrupt
0	0h WO	**forceautocmdnotexec:** Force Event for AUTO CMD12 Not Executed 1 – Interrupt is generated 0 – No Interrupt

42.2.34 Force Event Register for Error Interrupt Status (forceeventforerrintsts)—Offset 52h

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RO	**Force Event for Tuning Error (forcetuningerr):** 1 – Interrupt is generated 0 – No Interrupt
9	0h RO	**forceadmaerr:** forceadmaerr
8	0h RO	**Force Event for Auto CMD Error (forceautocmderr):** 1 – Interrupt is generated 0 – No Interrupt
7	0h RO	**Force Event for Current Limit (forcecurrlimerr):** 1 – Interrupt is generated 0 – No Interrupt
6	0h WO	**Force Event for Data End Bit Error (forcedatendbiterr):** 1 – Interrupt is generated 0 – No Interrupt
5	0h RO	**Force Event for Data CRC Error (forcedatcrcerr):** 1 – Interrupt is generated 0 – No Interrupt
4	0h RO	**Force Event for Data Timeout Error (forcedattimeouterr):** 1 – Interrupt is generated 0 – No Interrupt
3	0h RO	**Force Event for Command Index Error (forcecmdindexerr):** 1 – Interrupt is generated 0 – No Interrupt
2	0h RO	**Force Event for Command CRC Error (forcecmdendbiterr):** 1 – Interrupt is generated 0 – No Interrupt
1	0h RO	**Force Event for Command CRC Error (forcecmdcrcerr):** 1 – Interrupt is generated 0 – No Interrupt
0	0h RO	**Force Event for CMD Timeout Error (forcecmdtimeouterr):** 1 – Interrupt is generated 0 – No Interrupt

42.2.35 ADMA Error Status (admaerrsts)—Offset 54h

When the ADMA Error interrupt occur, this register holds the ADMA State in ADMA Error States field and ADMA System Address holds address around the error descriptor

Access Method

Type: MEM Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**ADMA Length Mismatch Error (admaerrsts_admalenmismatcherr):** ADMA Length Mismatch Error This error occurs in the following 2 cases. While Block Count Enable being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length. Total data length can not be divided by the block length. 1 - Error 0 - No error
1:0	0h RO	**ADMA Error State (admaerrsts_admaerrorstate):** This field indicates the state of ADMA when error is occurred during ADMA data transfer. This field never indicates "10" because ADMA never stops in this state. D01 – D00 : ADMA Error State when error occurred Contents of SYS_SDR register. 00 - ST_STOP (Stop DMA) Points to next of the error descriptor. 01 - ST_FDS (Fetch Descriptor) Points to the error descriptor 10 - Never set this state (Not used). 11 - ST_TFR (Transfer Data) Points to the next of the error descriptor

42.2.36 ADMA System Address Register 1 (admasysaddr01)—Offset 58h

This register contains the physical address used for ADMA data transfer.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**ADMA 32 bit System Address (adma_32bit_sysaddress):** This register holds byte address of executing command of the Descriptor table.

42.2.37 ADMA System Address Register2 (admasysaddr2)—Offset 5Ch

Access Method

Type: MEM Register (Size: 16 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**ADMA System Address (adma_64bit_sysaddress2):** This register holds byte address of executing command of the Descriptor table. 64-bit Address Descriptor uses Upper 32-bit of this register.

42.2.38 Preset Value for Initialization (presetvalue0)—Offset 60h

Access Method

Type: MEM Register (Size: 16 bits)

Device:
Function:

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**Driver Strength Select Value (DriverStrengthSelectValue):** Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. 11b Driver Type D is Selected 10b Driver Type C is Selected 01b Driver Type A is Selected 00b Driver Type B is Selected
13:11	0h RO	Reserved.
10	0h RO	**Clock Generator Select Value (ClockGeneratorSelectValue):** This bit is effective when Host Controller supports programmable clock generator. 1: Programmable Clock Generator 0: Host Controller Ver2.00 Compatible Clock Generator
9:0	4h RO	**SDCLK Frequency Select Value (SDCLKFrequencySelectValue):** 10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system.

42.2.39 Preset Preset Value for Default Speed (presetvalue1)—Offset 62h

Same description as Preset Value 0 register.

42.2.40 Preset Value for High Speed (presetvalue2)—Offset 64h

Same description as Preset Value 0 register.

42.2.41 Preset Value for SDR12 (presetvalue3)—Offset 66h

Same description as Preset Value 0 register.

42.2.42 Preset Value for SDR25 (presetvalue4)—Offset 68h

Same description as Preset Value 0 register.

42.2.43 Preset Value for SDR50 (presetvalue5)—Offset 6Ah

Same description as Preset Value 0 register.

42.2.44 Preset Value for SDR104 (presetvalue6)—Offset 6Ch

Same description as Preset Value 0 register.

42.2.45 Preset Value for DDR50 (presetvalue7)—Offset 6Eh

Same description as Preset Value 0 register.

42.2.46 Boot Timeout Control (boottimeoutcnt)—Offset 70h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Boot Timeout Control (boot_timeoutcnt):** This value determines the interval by which DAT line time-outs are detected during boot operation for eMMC card.

42.2.47 PRESETVALUE8 Reg (PRESETVALUE8) — Offset 74h

DriverStrengthSelectValue

Note: Bit definitions are the same as PRESETVALUE0, offset 60h.

42.2.48 VENDREG Reg (VENDREG) — Offset 78h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:1	0h RO	Reserved.
0	0h RW	VENDOR_ENHANCEDSTROBE: VENDOR_ENHANCEDSTROBE

42.2.49 Slot Interrupt Status (slotintrsts)—Offset FCh

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:1	0h RO	Reserved.
0	0h RO	**Slot 0 Interrupt Status (sdhchostif_slotintrstsslot0):** sdhchostif_slotintrstsslot0

42.2.50 HOSTCONTROLLERVER Reg (HOSTCONTROLLERVER) — Offset FEh

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	10h RO	SDHC_VENVERNUM: SDHC_VENVERNUM
7:0	02h RO	SPECIFICATIONVERSIONNUMBER: SPECIFICATIONVERSIONNUMBER

42.3 EMMC Additional Registers

These registers are memory mapped based on BAR0 defined in PCI configuration space.

Table 42-3. Summary of EMMC Additional Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
804h	805h	Software LTR Value (SW_LTR_val)—Offset 804h	800h
808h	809h	Auto LTR Value (Auto_LTR_val)—Offset 808h	800h
810h	813h	Capabilities Bypass (Cap_byps)—Offset 810h	0h
814h	817h	Capabilities Bypass 1 (Cap_byps_reg1)—Offset 814h	3040EF3Ch
818h	81Bh	Capabilities Bypass Register II (Cap_byps_reg2)—Offset 818h	40040C8h
81Ch	81Fh	Device Idle D0i3 (reg_D0i3)—Offset 81Ch	8h
820h	823h	Tx CMD Delay Control (Tx_CMD_dly)—Offset 820h	400h
824h	827h	Tx Delay Control 1 (Tx_DATA_dly_1)—Offset 824h	A18h
828h	82Bh	Tx Delay Control 2 (Tx_DATA_dly_2)—Offset 828h	1C1C1C00h
82Ch	82Fh	Rx CMD Data Delay Control 1 (Rx_CMD_Data_dly_1)—Offset 82Ch	1C1C1C00h
830h	833h	Rx Strobe Delay Control (Rx_Strobe_Ctrl_Path)—Offset 830h	500h
834h	837h	Rx CMD Data Path Delay Control 2 (Rx_CMD_Data_dly_2)—Offset 834h	181Ch
838h	83Bh	Initiator DLL Software Control (Initiator_Dll)—Offset 838h	1h

Table 42-3. Summary of EMMC Additional Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
840h	843h	Auto Tuning Value (Auto_tuning)—Offset 840h	0h

42.3.1 Software LTR Value (SW_LTR_val)—Offset 804h

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 800h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Snoop_Requirment:** Snoop_Requirment
14:13	0h RO	Reserved.
12:10	2h RW	**Snoop Latency Scale (Snoop_latency_scale):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -) 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**Snoop Value (Snoop_value):** 10-bit latency value

42.3.2 Auto LTR Value (Auto_LTR_val)—Offset 808h

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 800h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Snoop Requirment (Snoop_Requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	Reserved.
12:10	2h RW	**Snoop Latency Scale (Snoop_latency_scale):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -) 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**Snoop Value (Snoop_value):** 10-bit latency value

42.3.3 Capabilities Bypass (Cap_byps)—Offset 810h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**Enable Capabilities Bypass (Enable_Cap_Bypass):** 5Ah: Enable Capabilities Bypass Others: Capabilities Bypass disabled (using default values)

42.3.4 Capabilities Bypass 1 (Cap_byps_reg1)—Offset 814h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 3040EF3Ch

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	1h RW	**hs400_support:** 1 – HS400 Mode Supported 0 – HS400 Mode NOT Supported
28	1h RW	**Timeout Clock Unit (timeout_clock_unit):** 1 - to Select MHz Clock 0 - to Select KHz Clock
27:22	1h RW	**Timeout Clock Frequency (timeout_clock_freq)**
21	0h RW	**SPI Mode Support (SPI_mode_support):** 1: SPI Mode Supported 0: SPI Mode Not Supported
20:17	0h RW	**Timer Count for Re-Tuning (timer_count):** This is the Timer Count for Re-Tuning Timer for Re-Tuning Mode 1 to 3. Setting to 0h disables Re-Tuning Timer.
16	0h RW	**Use Tuning for SDR50 (tuning_for_SDR50):** 1 = Use Tuning 0 = Don't use Tuning
15	1h RW	**DDR50 Support (ddr50_support):** 1'b1 – DDR50 Mode Supported 1'b0 – DDR50 Mode NOT Supported
14	1h RW	**SDR104 Support (sdr104_support):** 1'b1 – SDR104 Mode Supported 1'b0 – SDR104 Mode NOT Supported
13	1h RW	**SDR50 Support (sdr50_support):** 1'b1 – SDR50 Mode Supported 1'b0 – SDR50 Mode NOT Supported

Bit Range	Default & Access	Field Name (ID): Description
12:11	1h RW	**Slot Type (Slot_Type):** 00 - Removable Card Slot 01 - Embedded Slot for One Device 10 - Shared Bus Slot 11 - Reserved
10	1h RW	**Asynchronous Interrupt Support (Asynchronus_Interrupt_Support):** 1'b1 – Asynchronous Interrupt Supported 1'b0 – Asynchronous Interrupt NOT Supported
9	1h RW	**64 Bit System Address Support (Sys_Addr_64bit_Support):** 1 - Core supports 64-bit System Address Bus 0 - Core supports only 32-bit System Address Bus
8	1h RW	**Voltage Support 1.8V (Voltage_Support_1_8V):** 1'b1 – 1.8V Supported 1'b0 – 1.8V NOT Supported
7	0h RW	**Voltage Support 3.0V (Voltage_Support_3V):** 1'b1 – 3.0V Supported 1'b0 – 3.0V NOT Supported
6	0h RW	**Voltage Support 3.3V (Voltage_Support_3_3V):** 1'b1 – 3.3V Supported 1'b0 – 3.3V NOT Supported
5	1h RW	**Suspend / Resume Support (Suspend_Resume_Support):** 1'b1 – Suspend/Resume Supported 1'b0 – Suspend/Resume NOT Supported
4	1h RW	**SDMA Support (SDMA_Support):** 1'b1 – SDMA Mode Supported 1'b0 – SDMA Mode NOT Supported
3	1h RW	**High Speed Support (High_Speed_Support):** 1'b1 – High Speed Mode Supported 1'b0 – High Speed Mode NOT Supported
2	1h RW	**ADMA2 Support (ADMA2_Support):** 1'b1 – ADMA2 Mode Supported 1'b0 – ADAM2 Mode NOT Supported
1:0	0h RW	**Max Burst Length (Max_Burst_Length):** Maximum Block Length supported by the Core/Device 00: 512 (Bytes) 01: 1024 10: 2048 11: Reserved

42.3.5 Capabilities Bypass Register II (Cap_byps_reg2)—Offset 818h

Access Method

Type: MEM Register (Size: 32 bits)

Device:

Function:

Default: 40040C8h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26:21	20h RW	**Tuning Count Value (tuning_count_val):** Configures the Number of Taps (Phases) of the rxclk_in that is supported. The Tuning State machine uses this information to select one of the Taps (Phases) of the rxclk_in during the Tuning Procedure

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**Tuning Disable (tuning_dis):** Disable the 1.5x Tuning count when calculating total tuning count.
19	0h RW	**Driver Type 4 Support (driver_type_4):** 1: Supported 0: NOT Supported
18	0h RW	**Driver Type D Support (driver_type_D):** 1: Supported 0: NOT Supported
17	0h RW	**Driver Type C Support (driver_type_C):** 1: Supported 0: NOT Supported
16	0h RW	**Driver Type A Support (driver_type_A):** 1: Supported 0: NOT Supported
15	0h RO	Reserved.
14	1h RW	**8-bit Support for Embedded Device (support_8_bit_embedded):** 1: Supported 0: NOT Supported
13:8	0h RO	Reserved.
7:0	C8h RW	**Base Clock Frequency (base_sd_clock)**

42.3.6 Device Idle D0i3 (reg_D0i3)—Offset 81Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**Interrupt Request Capable (Interrupt_Request_Capable):** 0 – HW not capable to issue in interrupt on command completion 1 – HW capable to issue an interrupt on command completion
3	1h RW/1C	**Restore Required (RestoreRequired):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**D0i3 (D0i3):** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1	0h RO	Reserved.
0	0h RO	**Command In Progress (Cmd_In_Progress):** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit. If Interrupt Request bit [1] was set for the current command, HW may clear this bit before the interrupt has been made visible to SW.

42.3.7 Tx CMD Delay Control (Tx_CMD_dly)—Offset 820h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 400h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14:8	4h RW	**Tx CMD Delay (DDR Mode) (ddr_mode):** Tx CMD Delay (DDR Mode). 0 - 39: Select number of active delay elements. Each = 125pSec. 40 - 127: Reserved
7	0h RO	Reserved.
6:0	0h RW	**Tx CMD Delay (SDR Mode) (sdr_mode):** Tx CMD Delay (SDR Mode). 0 - 39: Select number of active delay elements. Each = 125pSec. 40 - 127 - Reserved

42.3.8 Tx Delay Control 1 (Tx_DATA_dly_1)—Offset 824h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: A18h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14:8	Ah RW	**Tx Data Delay (HS400 Mode) (hs400_mode):** Tx Data Delay (HS400 Mode). 0 - 78: Select number of active delay elements. Each = 125pSec. 79 - 127: Reserved
7	0h RO	Reserved.
6:0	18h RW	**Tx Data Delay (SDR104/HS200 Mode) (sdr104_hs200_mode):** 0-79 - Select the required delay, as a multiple of 125pSec. 80 – 127 – Reserved

42.3.9 Tx Delay Control 2 (Tx_DATA_dly_2)—Offset 828h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1C1C1C00h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:24	1Ch RW	**Tx Data Delay (SDR50 Mode) (sdr50_mode):** 0 - 79: Select the required delay, as a multiple of 125pSec. 80 - 127: Reserved
23	0h RO	Reserved.
22:16	1Ch RW	**Tx Data Delay (DDR50 Mode) (ddr50_mode):** 0 - 78: Select number of active delay elements. Each = 125pSec. 79 - 127: Reserved
15	0h RO	Reserved.
14:8	1Ch RW	**Tx Data Delay (SDR25/HS50 Mode) (sdr25_hs50_mode):** 0 - 79: Select the required delay, as a multiple of 125pSec. 80 - 127: Reserved
7	0h RO	Reserved.
6:0	0h RW	**Tx Data Delay (SDR12/Compatibility Mode) (sdr12_comp_mode):** 0 - 79: Select the required delay, as a multiple of 125pSec. 80 - 127: Reserved

42.3.10 Rx CMD Data Delay Control 1 (Rx_CMD_Data_dly_1)—Offset 82Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1C1C1C00h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:24	1Ch RW	**Rx CMD + Data Delay (SDR50 Mode) (sdr50_mode):** 0-119 - Select the required delay, as a multiple of 125pSec. 120 – 127 – Reserved
23	0h RO	Reserved.
22:16	1Ch RW	**Rx CMD + Data Delay (DDR50 Mode) (ddr50_mode):** 0-78: Select number of active delay elements. Each = 125 pSec. 79-127: Reserved
15	0h RO	Reserved.
14:8	1Ch RW	**Rx CMD + Data Delay (SDR25/HS50 Mode) (sdr25_hs50_mode):** 0-119 - Select the required delay, as a multiple of 125pSec. 120 – 127 – Reserved
7	0h RO	Reserved.
6:0	0h RW	**Rx CMD + Data Delay (SDR12/Compatibility Mode) (sdr12_comp_mode):** 0-119 - Select the required delay, as a multiple of 125pSec. 120 – 127 – Reserved

42.3.11 Rx Strobe Delay Control (Rx_Strobe_Ctrl_Path)—Offset 830h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 500h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	Reserved.
16	0h RW	**Auto Tuning (auto_tuning):** Enable Auto Tuning for HS400 Strobe Path. 0: Auto Tuning Disabled 1: Auto Tuning Enabled
15	0h RO	Reserved.
14:8	5h RW	**Rx Strobe Delay DLL 1(HS400 Mode) (hs400_mode1):** 0-39: Select number of active delay elements. Each = 125 pSec. 0-63: Reserved
7	0h RO	Reserved.
6:0	0h RW	**Rx Strobe Delay DLL 2(HS400 Mode) (hs400_mode2):** 0-39: Select number of active delay elements. Each = 125 pSec. 40-63: Reserved

42.3.12 Rx CMD Data Path Delay Control 2 (Rx_CMD_Data_dly_2)—Offset 834h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 181Ch

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:16	0h RW	**Clock Source (clk_source):** Clock Source for Rx Path. 00: Rx Clock after Output Buffer 01: Rx Clock before Output Buffer 10: Automatic Selection based on Working mode (HS 200 before buffer, all others after buffer) 11 - Reserved
15:14	0h RO	Reserved.
13:8	18h RW	**Rx Path PLL (path_pll):** Rx Path PLL #3 Delay value For Auto Tuning Mode. 0-39: Select the required delay, as a multiple of 125 pSec. 40-63: Reserved
7	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
6:0	1Ch RW	**Rx CMD + Data Delay (SDR104/HS200 Mode) (cmd_data_sdr104_hs200):** 0-79: Select the required delay, as a multiple of 125 pSec. 80-127: Reserved

42.3.13 Initiator DLL Software Control (Initiator_Dll)—Offset 838h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RW	**SW reset for Initiator DLL (SW_reset_dll):** 0: No SW Reset for Initiator DLL 1: Force Reset for Initiator DLL
23	0h RO/V	**Initiator DLL Lock Indication (DLL_lock)**
22:2	0h RO	Reserved.
1	0h RW	**Initiator DLL Software Control (Initiator_DLL_Software_Ctrl):** 0: Initiator DLL Automatic Control (SW Control Disabled). 1: Initiator DLL Software Control Enabled
0	1h RW	**Control of Initiator DLL Ref Clock (Ctrl_of_Mst_DLL_Ref_Clk):** 0: Clock is Disabled. 1: Clock is Enabled

42.3.14 Auto Tuning Value (Auto_tuning)—Offset 840h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4:0	0h RO/V	**Auto Tuning Value (auto_tuning_val):** Auto Tuning Value found by host controller.

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43 UFS Registers (D18:F7)

This chapter documents the registers in Bus: 0, Device 18, Function 7.

Note: These registers do not apply to S/H processors.

43.1 UFS Configuration Registers

Table 43-1. Summary of UFS Configuration Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	DEVICEID Ufs (DEVICEID)	00008086h
4h	4	STATUSCOMMAND Ufs (STATUSCOMMAND)	00100000h
8h	4	REVCLASSCODE Ufs (REVCLASSCODE)	01090100h
Ch	4	CLLATHEADERBIST Ufs (CLLATHEADERBIST)	00000000h
10h	4	BAR Ufs (BAR)	00000004h
14h	4	BAR_HIGH Ufs (BAR_HIGH)	00000000h
18h	4	BAR1 Ufs (BAR1)	00000004h
1Ch	4	BAR1_HIGH Ufs (BAR1_HIGH)	00000000h
2Ch	4	SUBSYSTEMID Ufs (SUBSYSTEMID)	00000000h
30h	4	EXPANSION_ROM_BASEADDR Ufs (EXPANSION_ROM_BASEADDR)	00000000h
34h	4	CAPABILITYPTR Ufs (CAPABILITYPTR)	00000080h
3Ch	4	INTERRUPTREG Ufs (INTERRUPTREG)	00000000h
80h	4	POWERCAPID Ufs (POWERCAPID)	00039001h
84h	4	PMECTRLSTATUS Ufs (PMECTRLSTATUS)	00000008h
90h	4	PCIDEVIDLE_CAP_RECORD Ufs (PCIDEVIDLE_CAP_RECORD)	F0140009h
94h	4	DEVID_VEND_SPECIFIC_REG Ufs (DEVID_VEND_SPECIFIC_REG)	01400010h
98h	4	D0I3_CONTROL_SW_LTR_MMIO_REG Ufs (D0I3_CONTROL_SW_LTR_MMIO_REG)	00008041h
9Ch	4	DEVICE_IDLE_POINTER_REG Ufs (DEVICE_IDLE_POINTER_REG)	000081C1h
A0h	4	D0I3_MAX_POW_LAT_PG_CONFIG Ufs (D0I3_MAX_POW_LAT_PG_CONFIG)	00290800h
B0h	4	GEN_REGRW1 Ufs (GEN_REGRW1)	00000000h
B4h	4	GEN_REGRW2 Ufs (GEN_REGRW2)	00000000h
B8h	4	GEN_REGRW3 Ufs (GEN_REGRW3)	00000000h
BCh	4	GEN_REGRW4 Ufs (GEN_REGRW4)	00000000h
C0h	4	GEN_INPUT_REG Ufs (GEN_INPUT_REG)	00000000h

43.1.1 DEVICEID Ufs (DEVICEID) — Offset 0h

Vendor ID Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:18, F:7] + 0h	00008086h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO/P	**DEVICEID:** Device ID identifies the particular PCI device
15:0	8086h RO	**VENDORID:** Vendor ID is a unique ID provided by the PCI SIG which identifies the manufacturer of the device

43.1.2 STATUSCOMMAND Ufs (STATUSCOMMAND) — Offset 4h

PCI Command Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:18, F:7] + 4h	00100000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW/1C	**RMA:** Received Initiator Abort
28	0h RW/1C	**RTA:** Received Target Abort
27:21	0h RO	**Reserved**
20	1h RO	**CAPLIST:** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device
18:11	0h RO	**Reserved**
10	0h RW	**INTR_DISABLE:** Interrupt Disable
9	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**SERR_ENABLE:** SERR Enable Not implemented
7:3	0h RO	**Reserved**
2	0h RW	**BME:** Bus Initiator Enable
1	0h RW	**MSE:** Memory Space Enable
0	0h RO	**Reserved**

43.1.3 REVCLASSCODE Ufs (REVCLASSCODE) — Offset 8h

Revision ID Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:18, F:7] + 8h	01090100h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	010901h RO	**CLASS_CODES:** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	00h RO/P	**RID:** Revision ID identifies the revision of particular PCI device.

43.1.4 CLLATHEADERBIST Ufs (CLLATHEADERBIST) — Offset Ch

Cache Line Latency Header and BIST Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:18, F:7] + Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**MULFNDEV:** Multi-Function Device
22:16	00h RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header
15:8	00h RO	**LATTIMER:** Latency Timer:. This register is implemented as RO with default as 0
7:0	00h RW/P	**CACHELINE_SIZE:** Cacheline Size

43.1.5 BAR Ufs (BAR) — Offset 10h

BAR -Base Address Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:18, F:7] + 10h	00000004h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**BASEADDR:** Base Address Register Low Base address of the OCP fabric memory space. Taken from Strap values as ones
11:4	00h RO	**SIZEINDICATOR:** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**PREFETCHCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable
2:1	2h RO	**TYPE:** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**MESSAGE_SPACE:** Memory Space Indicator: 0 indicates this BAR is present in the memory space.

43.1.6 BAR_HIGH Ufs (BAR_HIGH) — Offset 14h

BAR -Base Address Register High

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:18, F:7] + 14h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**BASEADDR_HIGH:** Base Address high - MSB

43.1.7 BAR1 Ufs (BAR1) — Offset 18h

BAR1 -Base Address Register1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:18, F:7] + 18h	00000004h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**BASEADDR1:** Base Address1 This field is present if BAR1 is enabled through private configuration space.
11:4	00h RO	**SIZEINDICATOR1:** Always is 0 as minimum size is 4K
3	0h RO	**PREFETCHCHABLE1:** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	2h RO	**TYPE1:** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

43.1.8 BAR1_HIGH Ufs (BAR1_HIGH) — Offset 1Ch

BAR1 -Base Address Register1 High

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:18, F:7] + 1Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**BAR1_HIGH:** Base Address: Base address of the OCP fabric memory space. Taken from Strap values as ones

43.1.9 SUBSYSTEMID Ufs (SUBSYSTEMID) — Offset 2Ch

SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:18, F:7] + 2Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O/P	**SUBSYSTEMID:** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system.
15:0	0000h RW/O/P	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

43.1.10 EXPANSION_ROM_BASEADDR Ufs (EXPANSION_ROM_BASEADDR) — Offset 30h

Expansion ROM Base Address Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:18, F:7] + 30h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:11	000000h RO	**EXPANSION_ROM_BASE:** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM
10:1	0h RO	**Reserved**
0	0h RO	**EXPANSION_ROM_ENABLE:** EXPANSION_ROM_ENABLE

43.1.11 CAPABILITYPTR Ufs (CAPABILITYPTR) — Offset 34h

Capabilities Pointer Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:18, F:7] + 34h	00000080h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is.

43.1.12 INTERRUPTREG Ufs (INTERRUPTREG) — Offset 3Ch

Interrupt Line Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:18, F:7] + 3Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**MAX_LAT:** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	**MIN_GNT:** MIN_GNT
15:12	0h RO	**Reserved**
11:8	0h RO	**INTPIN:** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW/P	**INTLINE:** Interrupt Line: It is used to communicate to software the interrupt line to which the interrupt pin is connected

43.1.13 POWERCAPID Ufs (POWERCAPID) — Offset 80h

Power Management Capability ID Regsiter

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:18, F:7] + 80h	00039001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**PMESUPPORT:** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved**
18:16	3h RO	**VERSION:** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	90h RO	**NXTCAP:** Next Capability: Points to the next capability structure.
7:0	01h RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability

43.1.14 PMECTRLSTATUS Ufs (PMECTRLSTATUS) — Offset 84h

Power Management Control and Status Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:18, F:7] + 84h	00000008h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/P	**PMESTATUS:** PME Status
14:9	0h RO	**Reserved**
8	0h RW/P	**PMEENABLE:** PME Enable
7:4	0h RO	**Reserved**
3	1h RO	**NO_SOFT_RESET:** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	0h RO	**Reserved**
1:0	0h RW	**POWERSTATE:** Power State: This field is used both to determine the current power state and to set a new power state

43.1.15 PCIDEVIDLE_CAP_RECORD Ufs (PCIDEVIDLE_CAP_RECORD) — Offset 90h

PCI Device Idle Capability Record Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:18, F:7] + 90h	F0140009h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**VEND_CAP:** Vendor Specific Capability ID
27:24	0h RO	**REVID:** Revision ID of capability structure
23:16	14h RO	**CAP_LENGTH:** Vendor Specific Capability Length
15:8	00h RO	**NEXT_CAP:** Next Capability
7:0	09h RO	**CAPID:** Capability ID

43.1.16 DEVID_VEND_SPECIFIC_REG Ufs (DEVID_VEND_SPECIFIC_REG) — Offset 94h

Device ID Vendor Specific Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:18, F:7] + 94h	01400010h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**VSEC_LENGTH:** Vendor Specific Extended Capability Length
19:16	0h RO	**VSEC_REV:** Vendor specific Extended Capability revision
15:0	0010h RO	**VSECID:** Vendor Specific Extended Capability ID

43.1.17 D0I3_CONTROL_SW_LTR_MMIO_REG Ufs (D0I3_CONTROL_SW_LTR_MMIO_REG) — Offset 98h

SW LTR Update MMIO Location Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:18, F:7] + 98h	00008041h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000804h RO	**SW_LAT_DWORD_OFFSET:** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW_LAT_BAR_NUM:** Indicates that the SW LTR update MMIO location is always at BAR0
0	1h RO	**SW_LAT_VALID:** This value is reflected from the SW LTR valid strap at the top level

43.1.18 DEVICE_IDLE_POINTER_REG Ufs (DEVICE_IDLE_POINTER_REG) — Offset 9Ch

Device IDLE Pointer Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:18, F:7] + 9Ch	000081C1h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	000081Ch RO	**DWORD_OFFSET:** contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR_NUM1:** Bar num: Indicates that the D0i3 MMIO location is always at BAR0
0	1h RO	**VALID:** Valid: This value is reflected from the D0i3 valid strap at the top level.

43.1.19 D0I3_MAX_POW_LAT_PG_CONFIG Ufs (D0I3_MAX_POW_LAT_PG_CONFIG) — Offset A0h

Doi3 Max Power On Latency

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:18, F:7] + A0h	00290800h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	1h RW/P	**HAE:** Hardware Autonomous Enable
20	0h RO	**Reserved**
19	1h RW/P	**SLEEP_EN:** Sleep Enable
18	0h RW	**PGE:** DEVIDLE Enable (DEVIDLEN): If ?1? then the function will power gate when idle and the DevIdle register (DevIdleC[2] = ?1?) is set.
17	0h RW	**I3_ENABLE:** I3_ENABLE
16	1h RW/P	**PMCRE:** PMCRE
15:13	0h RO	**Reserved**
12:10	2h RW/O/P	**POW_LAT_SCALE:** Power On Latency Scale
9:0	000h RW/O/P	**POW_LAT_VALUE:** Power On Latency value

43.1.20 GEN_REGRW1 Ufs (GEN_REGRW1) — Offset B0h

General Purpose PCI RW Register1

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:18, F:7] + B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW1:** General Purpose PCI Register: This register value is brought out as oob_gen_pci_reg1 Out of Band signal

43.1.21 GEN_REGRW2 Ufs (GEN_REGRW2) — Offset B4h

General Purpose PCI RW Register2

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:18, F:7] + B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW2:** General Purpose PCI Register: This register value is brought out as oob_gen_pci_reg2 Out of Band signal

43.1.22 GEN_REGRW3 Ufs (GEN_REGRW3) — Offset B8h

General Purpose PCI RW Register3

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:18, F:7] + B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW3:** General Purpose PCI Register: This register value is brought out as oob_gen_pci_reg3 Out of Band signal

43.1.23 GEN_REGRW4 Ufs (GEN_REGRW4) — Offset BCh

General Purpose PCI RW Register4

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:18, F:7] + BCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW4:** General Purpose PCI Register: This register value is brought out as oob_gen_pci_reg4 Out of Band signal

43.1.24 GEN_INPUT_REG Ufs (GEN_INPUT_REG) — Offset C0h

General Input Register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:18, F:7] + C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**GEN_INPUT_REG:** General Purpose Input Register: This register value reflects the value of oob_gen_input_pci Out of Band signal

43.2 UFS MMIO Registers

This section lists the registers of Universal Flash Storage interface for MMIO registers.

Table 43-2. Summary of UFS MMIO Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
804h	4	UFS_SW_LTR_VAL_REG Ufs (SW_LTR_VAL)	00000800h
808h	4	UFS_AUTO_LTR_VAL_REG Ufs (AUTO_LTR_VAL)	00000800h
81Ch	4	UFS_D0I3_CTRL Ufs (REG_D0I3)	00000000h
854h	4	UFS_PWM_DIV Ufs (PWM_DIV)	0000003Bh
858h	4	UFS_CRU_XFSM_CTRL Ufs (CRU_XFSM)	00000249h
85Ch	4	UFS_REF_CLOCK Ufs (REF_CLK)	00000002h
860h	4	UFS_HS_CLOCK_CTRL Ufs (HS_RX_CLK)	00000000h
864h	4	UFS_HBP_OBS0 Ufs (UFS_HBP_OBS0)	FFFFFFFFh
868h	4	UFS_HBP_OBS1 Ufs (UFS_HBP_OBS1)	FFFFFFFFh
86Ch	4	UFS_HBP_OBS2 Ufs (UFS_HBP_OBS2)	FFFFFFFFh
870h	4	UFS_HBP_OBS3 Ufs (UFS_HBP_OBS3)	FFFF0000h
874h	4	UFS_HBP_OBS4 Ufs (UFS_HBP_OBS4)	00000000h
878h	4	UFS_HBP_OBS5 Ufs (UFS_HBP_OBS5)	00000000h
87Ch	4	UFS_HBP_OBS6 Ufs (UFS_HBP_OBS6)	00000000h
880h	4	NEW_REQACK_EN Ufs (UFS_NEW_REQACK_EN)	00000001h
900h	4	UFS_ROOT_SPACE Ufs (ROOT_SPACE)	00000000h
904h	4	UFS_IDLE_INDICATION Ufs (UFS_IDLE_INDICATION)	00000001h

43.2.1 UFS_SW_LTR_VAL_REG Ufs (SW_LTR_VAL) — Offset 804h

Software LTR VAL_REG Register

Type	Size	Offset	Default
MMIO	32 bit	FDAA0000h + 804h	00000800h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**SNOOP_REQUIRMENT:** Snoop_Requirment (snoop_requirment) If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	**Reserved**
12:10	2h RW	**SNOOP_LATENCY_SCALE:** Snoop_latency_scale (snoop_latency_scale) Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -) 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	000h RW	**SNOOP_VALUE:** Snoop_value (snoop_value) 10-bit latency value

43.2.2 UFS_AUTO_LTR_VAL_REG Ufs (AUTO_LTR_VAL) — Offset 808h

Auto LTR VAL_REG Register

Note: Bit definitions are the same as SW_LTR_VAL, offset 804h.

43.2.3 UFS_D0I3_CTRL Ufs (REG_D0I3) — Offset 81Ch

Device Idle D0i3 Register

Type	Size	Offset	Default
MMIO	32 bit	FDAA0000h + 81Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**RESTORE_REQUIRED:** Restore Required When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing 1. This bit will be set on initial power up.
2	0h RW	**D0I3:** D0i3 SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1	0h RO	**INTERRUPT_REQUEST:** Interrupt Request SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register. Not supported in SCS
0	0h RO	**CMD_IN_PROGRESS:** Command-In-Progress HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit. If Interrupt Request bit [1] was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles

43.2.4 UFS_PWM_DIV Ufs (PWM_DIV) — Offset 854h

PWM Clock Divider Register

Type	Size	Offset	Default
MMIO	32 bit	FDAA0000h + 854h	0000003Bh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**PWM_CLK_SOURCE_SEL:** pwm_clk_source_sel
7:6	0h RW	**PWM_HVM_PRE_DIV:** PWM_HVM_pre_div
5:0	3Bh RW	**PWM_DIV_VAL:** pwm_div_val

43.2.5 UFS_CRU_XFSM_CTRL Ufs (CRU_XFSM) — Offset 858h

Internal Clokc Unit XFSM

Type	Size	Offset	Default
MMIO	32 bit	FDAA0000h + 858h	00000249h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved**
16	0h RW	**MMP_LFPS_PULL_EN_BYP:** MMP_LFPS_pull_en_byp
15:12	0h RO	**Reserved**
11:9	1h RW	**CCU_XFSM:** ccu_xfsm
8:6	1h RW	**PLL_XFSM:** pll_xfsm
5:3	1h RW	**RX_XFSM:** rx_xfsm
2:0	1h RW	**TX_XFSM:** tx_xfsm

43.2.6 UFS_REF_CLOCK Ufs (REF_CLK) — Offset 85Ch

Ref Clock Register

Type	Size	Offset	Default
MMIO	32 bit	FDAA0000h + 85Ch	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	1h RW	**REF_CLK_EN:** ref_clk_en
0	0h RW	**REF_CLK_CTRL:** ref_clk_ctrl

43.2.7 UFS_HS_CLOCK_CTRL Ufs (HS_RX_CLK) — Offset 860h

HS Clock Control Register

Type	Size	Offset	Default
MMIO	32 bit	FDAA0000h + 860h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**HS_RX_CLK_CTRL:** HS_Rx_clk_ctrl

43.2.8 UFS_HBP_OBS0 Ufs (UFS_HBP_OBS0) — Offset 864h

Observation for HBP0

Type	Size	Offset	Default
MMIO	32 bit	FDAA0000h + 864h	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	FFFFh RO	**UFS_HBP_MISR_DFX_1:** ufs_hbp_misr_dfx_1
15:0	FFFFh RO	**UFS_HBP_MISR_DFX_0:** ufs_hbp_misr_dfx_0

43.2.9 UFS_HBP_OBS1 Ufs (UFS_HBP_OBS1) — Offset 868h

Observation for HBP1

Type	Size	Offset	Default
MMIO	32 bit	FDAA0000h + 868h	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	FFFFh RO	**UFS_HBP_MISR_DFX_3:** ufs_hbp_misr_dfx_3
15:0	FFFFh RO	**UFS_HBP_MISR_DFX_2:** ufs_hbp_misr_dfx_2

43.2.10 UFS_HBP_OBS2 Ufs (UFS_HBP_OBS2) — Offset 86Ch

Observation for HBP2

Type	Size	Offset	Default
MMIO	32 bit	FDAA0000h + 86Ch	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	FFFFh RO	**UFS_HBP_MISR_DFX_4:** ufs_hbp_misr_dfx_4
15:0	FFFFh RO	**UFS_HBP_MISR_DFX_L2DATA:** ufs_hbp_misr_dfx_l2data

43.2.11 UFS_HBP_OBS3 Ufs (UFS_HBP_OBS3) — Offset 870h

Observation for HBP3

Type	Size	Offset	Default
MMIO	32 bit	FDAA0000h + 870h	FFFF0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	FFFFh RO	**UFS_HBP_MISR_DFX_AFCNAC:** ufs_hbp_misr_dfx_afcnac
15:0	0000h RO	**L2_DATA_MISR_CNT:** l2_data_misr_cnt

43.2.12 UFS_HBP_OBS4 Ufs (UFS_HBP_OBS4) — Offset 874h

Observation for HBP4

Type	Size	Offset	Default
MMIO	32 bit	FDAA0000h + 874h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**AFC_NAC_MISR_CNT:** afc_nac_misr_cnt
15:0	0000h RO	**PA_CP_MISR_CNT:** pa_cp_misr_cnt

43.2.13 UFS_HBP_OBS5 Ufs (UFS_HBP_OBS5) — Offset 878h

Observation for HBP5

Type	Size	Offset	Default
MMIO	32 bit	FDAA0000h + 878h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**TXCFG_MISR_CNT:** txcfg_misr_cnt
15:0	0000h RO	**RXCFG_MISR_CNT:** rxcfg_misr_cnt

43.2.14 UFS_HBP_OBS6 Ufs (UFS_HBP_OBS6) — Offset 87Ch

Observation for HBP6

Type	Size	Offset	Default
MMIO	32 bit	FDAA0000h + 87Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**L2_DATA_X2_MISR_CNT:** l2_data_x2_misr_cnt
15:0	0000h RO	**AFC_NAC_X2_MISR_CNT:** afc_nac_x2_misr_cnt

43.2.15 NEW_REQACK_EN Ufs (UFS_NEW_REQACK_EN) — Offset 880h

Enable for New clkreq-ack features

Type	Size	Offset	Default
MMIO	32 bit	FDAA0000h + 880h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	00000000h RO	**CNP_REQACK_EN_RESERVED_31_1:** CNP_REQACK_EN_RESERVED_31_1
0	1h RW	**NEW_CLKREQ_ACK_EN:** NEW_clkreq_ack_en

43.2.16 UFS_ROOT_SPACE Ufs (ROOT_SPACE) — Offset 900h

Root Space Register

Type	Size	Offset	Default
MMIO	32 bit	FDAA0000h + 900h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO	**ROOT_SPACE:** root_space

43.2.17 UFS_IDLE_INDICATION Ufs (UFS_IDLE_INDICATION) — Offset 904h

ufs idle indication

Type	Size	Offset	Default
MMIO	32 bit	FDAA0000h + 904h	00000001h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	1h RO	**UFS_IDLE_INDICATION:** ufs_idle_indication

43.3 UFS IO Fabric Registers

This Section of documents UFS IO Converge configuration registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1078h	8	rt5_rt_network_control UFS (RT5_RT_NETWORK_CONTROL)	0h
4020h	8	main2scc_i0_ia_agent_control UFS (MAIN2SCC_I0_IA_AGENT_CONTROL)	0h
4820h	8	scc2main_t0_ta_agent_control UFS (SCC2MAIN_T0_TA_AGENT_CONTROL)	0h
5820h	8	ufs_i0_ia_agent_control UFS (UFS_I0_IA_AGENT_CONTROL)	0h
5C20h	8	ufs_t0_ta_agent_control UFS (UFS_T0_TA_AGENT_CONTROL)	0h

43.3.1 t5_rt_network_control UFS (RT5_RT_NETWORK_CONTROL) — Offset 1078h

Control over interconnect-wide functions

Type	Size	Offset	Default
MMIO	64 bit	FDAA0000h + 1078h	0h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:57	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
56	0h RO	**CLOCK_GATE_DISABLE:** Overrides fine-grained hardware clock gating
55:11	0h RO	**Reserved**
10:8	0h RW	**RT_NETWORK_CONTROL_TIMEOUT_BASE_4:** 212 cycles
7:0	0h RO	**Reserved**

43.3.2 main2scc_i0_ia_agent_control UFS (MAIN2SCC_I0_IA_AGENT_CONTROL) — Offset 4020h

Control over agent functions

Type	Size	Offset	Default
MMIO	64 bit	FDAA0000h + 4020h	0h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:29	0h RO	**Reserved**
28	0h RO	**INBAND_ERROR_PRIMARY_REP:** Reporting of in-band errors with MErrSteer indicating a primary error (or if error steering is not enabled)
27	0h RO	**ALL_INBAND_ERROR_REP:** Reporting of all in-band errors as out-of-band errors
26	0h RW	**BURST_TIMEOUT_REP:** Open burst and ReadEx/Write timeout reporting
25	0h RW	**RESP_TIMEOUT_REP:** Response timeout reporting
24:19	0h RO	**Reserved**
18:16	0h RW	**IA_AGENT_CONTROL_BURST_TIMEOUT_4:** 64 base cycles
15:11	0h RO	**Reserved**
10:8	0h RW	**IA_AGENT_CONTROL_RESP_TIMEOUT_4:** 64 base cycles
7:5	0h RO	**Reserved**
4	0h RW	**REJECT:** Request rejection control

Bit Range	Default & Access	Field Name (ID): Description
3:1	0h RO	**Reserved**
0	0h RW	**CORE_RESET:** Reset control for agent and reset output on core interface

43.3.3 scc2main_t0_ta_agent_control UFS (SCC2MAIN_T0_TA_AGENT_CONTROL) — Offset 4820h

Control over agent functions

Type	Size	Offset	Default
MMIO	64 bit	FDAA0000h + 4820h	0h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:26	0h RO	**Reserved**
25	0h RW	**REQ_TIMEOUT_REP:** Request timeout reporting
24:11	0h RO	**Reserved**
10:8	0h RW	**TA_AGENT_CONTROL_REQ_TIMEOUT_4:** 64 base cycles
7:5	0h RO	**Reserved**
4	0h RW	**REJECT:** Request rejection control
3:1	0h RO	**Reserved**
0	0h RW	**CORE_RESET:** Reset control for agent and reset output on core interface

43.3.4 ufs_i0_ia_agent_control UFS (UFS_I0_IA_AGENT_CONTROL) — Offset 5820h

Control over agent functions

Type	Size	Offset	Default
MMIO	64 bit	FDAA0000h + 5820h	0h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:29	0h RO	**Reserved**
28	0h RO	**INBAND_ERROR_PRIMARY_REP:** Reporting of in-band errors with MErrSteer indicating a primary error (or if error steering is not enabled)
27	0h RO	**ALL_INBAND_ERROR_REP:** Reporting of all in-band errors as out-of-band errors
26	0h RW	**BURST_TIMEOUT_REP:** Open burst and ReadEx/Write timeout reporting
25:19	0h RO	**Reserved**
18:16	0h RW	**IA_AGENT_CONTROL_BURST_TIMEOUT_4:** 64 base cycles
15:5	0h RO	**Reserved**
4	0h RW	**REJECT:** Request rejection control
3:1	0h RO	**Reserved**
0	0h RW	**CORE_RESET:** Reset control for agent and reset output on core interface

43.3.5 ufs_t0_ta_agent_control UFS (UFS_T0_TA_AGENT_CONTROL) — Offset 5C20h

Control over agent functions

Type	Size	Offset	Default
MMIO	64 bit	FDAA0000h + 5C20h	0h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
63:27	0h RO	**Reserved**
26	0h RW	**FUNCTIONAL_RESET_TIMEOUT_REP:** Functional reset timeout reporting
25	0h RW	**REQ_TIMEOUT_REP:** Request timeout reporting
24:19	0h RO	**Reserved**
18:16	0h RW	**TA_AGENT_CONTROL_FUNCTIONAL_RESET_TIMEOUT_4:** 64 base cycles
15:11	0h RO	**Reserved**
10:8	0h RW	**TA_AGENT_CONTROL_REQ_TIMEOUT_4:** 64 base cycles
7:5	0h RO	**Reserved**
4	0h RW	**REJECT:** Request rejection control
3:1	0h RO	**Reserved**
0	0h RW	**CORE_RESET:** Reset control for agent and reset output on core interface

43.4 UFSHC MIMO Registers

This section documents the registers of UFSHC MIMO.

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	CAP Ufs (CAP)	0187011Fh
8h	4	VER Ufs (VER)	00000200h
10h	4	HCPID Ufs (HCPID)	00000000h
14h	4	HCMID Ufs (HCMID)	000005E6h
18h	4	AHIT Ufs (AHIT)	00000000h
20h	4	IS Ufs (IS)	00000000h
24h	4	IE Ufs (IE)	00000000h
30h	4	HCS Ufs (HCS)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
34h	4	HCE Ufs (HCE)	00000000h
38h	4	UECPA Ufs (UECPA)	00000000h
3Ch	4	UECDL Ufs (UECDL)	00000000h
40h	4	UECN Ufs (UECN)	00000000h
44h	4	UECT Ufs (UECT)	00000000h
48h	4	UECDME Ufs (UECDME)	00000000h
4Ch	4	UTRIACR Ufs (UTRIACR)	00000000h
50h	4	UTRLBA Ufs (UTRLBA)	00000000h
54h	4	UTRLBAU Ufs (UTRLBAU)	00000000h
58h	4	UTRLDBR Ufs (UTRLDBR)	00000000h
5Ch	4	UTRLCLR Ufs (UTRLCLR)	00000000h
60h	4	UTRLRSR Ufs (UTRLRSR)	00000000h
70h	4	UTMRLBA Ufs (UTMRLBA)	00000000h
74h	4	UTMRLBAU Ufs (UTMRLBAU)	00000000h
78h	4	UTMRLDBR Ufs (UTMRLDBR)	00000000h
7Ch	4	UTMRLCLR Ufs (UTMRLCLR)	00000000h
80h	4	UTMRLRSR Ufs (UTMRLRSR)	00000000h
90h	4	UICCMD Ufs (UICCMD)	00000000h
94h	4	UICCMDARG1 Ufs (UICCMDARG1)	00000000h
98h	4	UICCMDARG2 Ufs (UICCMDARG2)	00000000h
9Ch	4	UICCMDARG3 Ufs (UICCMDARG3)	00000000h

43.4.1 CAP Ufs (CAP) — Offset 0h

Host Capabilities

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 0h	0187011Fh

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RO	**CAP_CS:** CAP_Chip_Select
27	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
26	0h RO	**UICDMETMS:** UIC_DME_TEST_MODE_command_supported_Indicates_whether_the_host_controller_supports_the_UniProSM_DME_TEST_MODE_req_SAP_primitive_Value_After_Reset_0x0_Exists_Always
25	0h RO	**OODDS:** Out_of_order_data_delivery_supported_OODDS_Indicates_whether_the_DWC_ufshc_core_supports_out_of_order_data_delivery_for_UTP_data_transfer_1_The_DWC_ufshc_core_supports_out_of_order_data_delivery_from_the_target_device_0_The_DWC_ufshc_core_does_not_support_out_of_order_data_delivery_from_the_target_device_Value_After_Reset_0x0_Exists_Always
24	1h RO	**AS64:** 64bit_addressing_supported_64AS_Indicates_whether_the_host_controller_can_access_64bit_data_structures_1_The_DWC_ufshc_core_makes_the_32bit_upper_bits_of_the_UTP_Transfer_Request_List_Base_Address_Upper_32_bit_and_UTP_Task_Management_Request_List_Base_Address_Upper_32bit,_the_PRD_Base,_and_each_PRD_entry_read or write_0_These_bits_are_readonly_The_DWC_ufshc_core_treats_these_bits_as_0_If_DWC_UFSHC_MADDR_WIDTH is 32,_then_this_field_is_set_to_0_If_DWC_UFSHC_MADDR_WIDTH is 64,_then_this_field_is_set_to_1_Value_After_Reset_DWC_UFSHC_MADDR_WIDTH 0x40 Exists_Always
23	1h RO	**AUTOH8:** Autohibernation_support_AUTOH8_Indicates_whether_DWC_ufshc_controller_supports_autohibernation_0_Host_controller_does_not_support_autohibernation_1_Host_controller_supports_autohibernation_Value_After_Reset_0x1_Exists_Always
22:19	0h RO	**Reserved**
18:16	7h RO	**NUTMRS:** Number_of_UTP_Task_Management_Request_Slots_NUTMRS_Zerobased_value_indicating_the_number_of_slots_provided_by_the_UTP_Task_Management_Request_List_A_minimum_of_1_and_maximum_of_8_slots_may_be_supported_Value_After_Reset_0x7_Exists_Always
15:12	0h RO	**Reserved**
11:8	1h RO	**NPRTTS:** Number_of_outstanding_READY_TO_TRANSFER_RTT_requests_supported_NORTT_Indicates_the_maximum_number_of_outstanding_RTTs_which_are_supported_by_the_host_controller_Zerobased_value_indicates_the_maximum_number_of_RTTs_that_can_be_outstanding_on_the_host_at_a_particular_instance_A_minimum_of_two_RTTs_are_supported_and_maximum_is_implementation_specific_Value_After_Reset_0x1_Exists_Always
7:5	0h RO	**Reserved**
4:0	1Fh RO	**NUTRS:** Number_of_UTP_Transfer_Request_Slots_NUTRS_Zerobased_value_indicating_the_number_of_slots_provided_by_the_UTP_Transfer_Request_List_A_minimum_of_1_and_maximum_of_32_slots_may_be_supported_Value_After_Reset_0x1f_Exists_Always

43.4.2 VER Ufs (VER) — Offset 8h

Ver UFS

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 8h	00000200h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	02h RO	**MJR:** Major_Version_Number_MJR_Major_version_in_BCD_format_Value_After_Reset_0x2_Exists_Always
7:4	0h RO	**MNR:** Minor_Version_Number_MNR_Minor_version_in_BCD_format_Value_After_Reset_0x0_Exists_Always
3:0	0h RO	**VS:** Version_Suffix_VS_Version_suffix_in_BCD_format_Value_After_Reset_0x0_Exists_Always

43.4.3 HCPID Ufs (HCPID) — Offset 10h

Host Controller Identification Descriptor Product ID

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 10h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**PID:** Product_ID_PID_Product_ID_that_the_host_controller_manufacturer_assigns_for_the_host_controller_PID_is_defined_by_the_UFS_P_P_HCPID_parameter_Value_After_Reset_UFS_P_P_HCPID_Exists_Always

43.4.4 HCMID Ufs (HCMID) — Offset 14h

Host Controller Identification Descriptor Manufacturer ID

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 14h	000005E6h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	05h RO	**BI:** Bank_index_This_field_contains_an_index_value_of_the_bank_that_contains_the_Manufacturer_Identification_Code_The_BI_value_is_equal_to_the_number_of_the_continuation_fields_that_precede_the_MIC_BI_is_defined_by_the_UFS_P_P_HCMID_BI_parameter_Value_After_Reset_UFS_P_P_HCMID_BI_Exists_Always
7:0	E6h RO	**MIC:** Manufacturer_ID_Code_Manufacturer_Identification_code_of_the_host_controller_MIC_is_defined_by_the_UFS_P_P_HCMID_MIC_parameter_Value_After_Reset_UFS_P_P_HCMID_MIC_Exists_Always

43.4.5 AHIT Ufs (AHIT) — Offset 18h

Auto Hibernate Idle Timer

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 18h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12:10	0h RW	**TS:** Timer_scale_TS_000_Value_times_1_us_001_Value_times_10_us_010_Value_times_100_us_011_Value_times_1_ms_100_Value_times_10_ms_101_Value_times_100_ms_110_111_reserved_Value_After_Reset_0x0_Exists_Always
9:0	000h RW	**AH8ITV:** AutoHibern8_Idle_Timer_Value_AH8ITV_This_is_the_timer_for_which_the_UFS_subsystem_must_be_idle_before_the_UFS_host_controller_may_put_the_UniPro_link_into_hibernate_state_autonomously_The_idle_timer_value_is_multiplied_by_the_indicated_timer_scale_to_yield_an_absolute_timer_value_The_idle_timer_starts_decrementing_when_all_of_the_following_conditions_are_satisfied_UTRLDBR is 0_UTMRLDBR is 0_No_UIC_command_is_outstanding_The_idle_timer_continues_to_decrement_until_it_reaches_zero_or_it_is_reloaded_as_a_result_of_software_access_to_one_of_host_controller_interface_registers_When_idle_timer_changes_a_nonzero_to_zero,_the_host_controller_puts_the_UniPro_link_into_the_hibernate_state_The_host_controller_reloads_this_value_each_time_the_UniPro_link_transitions_out_of_the_hibernate_state_The_software_writes_0_to_disable_the_autohibernate_idle_timer_Any_nonzero_value_enables_the_autohibernate_idle_timer_The_software_access_to_any_one_of_host_controller_interface_registers_automatically_puts_the_UniPro_link_out_of_hibernate_state_Value_After_Reset_0x0_Exists_Always

43.4.6 IS Ufs (IS) — Offset 20h

Interrupt Status

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 20h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RW/C	**SBFES:** System_Bus_Fatal_Error_Status_SBFES_Indicates_that_the_DWC_ufshc_core_encountered_a_system_bus_error_that_it_cannot_recover_from_such_as_a_bad_software_pointer_When_the_error_occurs,_the_DWC_ufshc_core_is_stopped_and_both_UTRRSR_and_UTMRRSR_registers_are_cleared_to_0_by_the_DWC_ufshc_core_Value_After_Reset_0x0_Exists_Always
16	0h RW/C	**HCFES:** Host_Controller_Fatal_Error_Status_HCFES_Indicates_that_the_DWC_ufshc_core_encountered_a_fatal_error_that_it_cannot_recover_from_When_the_error_occurs,_the_DWC_ufshc_core_is_stopped_and_both_UTRRSR_and_UTMRRSR_are_cleared_to_0_by_the_DWC_ufshc_If_the_error_occurs,_the_host_application_must_reset_the_DWC_ufshc_core_Value_After_Reset_0x0_Exists_Always
15:13	0h RO	**Reserved**
12	0h RW/C	**UTPES:** UTP_Error_Status_UTPES_Indicates_that_the_DWC_ufshc_core_encountered_an_error_at_UTP_layer_that_it_cannot_recover_from_When_the_error_occurs,_the_DWC_ufshc_core_updates_the_UTP_error_code_field_within_the_Host_Controller_Status_register_The_host_application_must_then_handle_the_error_condition_Value_After_Reset_0x0_Exists_Always
11	0h RW/C	**DFES:** Device_Fatal_Error_Status_DFES_Indicates_that_the_DWC_ufshc_core_encountered_a_fatal_error_from_the_device_that_it_cannot_recover_from_When_the_error_occurs,_the_DWC_ufshc_core_is_stopped_and_both_UTRLRSR_and_UTMRLRSR_bits_are_cleared_to_0_by_the_DWC_ufshc_core_If_the_error_occurs,_the_host_application_must_reset_the_DWC_ufshc_Value_After_Reset_0x0_Exists_Always
10	0h RW/C	**UCCS:** UIC_Command_Completion_Status_UCCS_The_DWC_ufshc_core_sets_this_bit_to_1_after_completing_a_UIC_command_Value_After_Reset_0x0_Exists_Always
9	0h RW/C	**UTMRCS:** UTP_Task_Management_Request_Completion_Status_UTMRCS_The_DWC_ufshc_core_sets_this_bit_to_1_after_completing_a_task_management_function_Value_After_Reset_0x0_Exists_Always
8	0h RW/C	**ULSS:** UIC_Link_Startup_Status_ULSS_Indicates_that_Link_startup_process_has_been_initiated_by_the_remote_end_of_the_Link_This_bit_corresponds_to_the_UniPro_DME_LINKSTARTUP_ind_SAP_primitive_Value_After_Reset_0x0_Exists_Always
7	0h RW/C	**ULLS:** UIC_Link_Lost_Status_ULLS_This_indicates_a_condition_where_remote_end_is_trying_to_reestablish_a_link_and_the_link_is_lost_This_bit_corresponds_to_the_UniPro_DME_LINKLOST_ind_SAP_primitive_Value_After_Reset_0x0_Exists_Always

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/C	**UHES:** UIC_Hibernate_Enter_Status_UHES_Indicates_that_UniPro_hibernate_entering_process_is_complete_and_the_Link_state_is_changed_to_the_Hibernate_state_if_the_process_is_successful_The_HCS_UPMCRS_register_bit_indicates_if_the_entry_process_is_not_successful_This_bit_corresponds_to_the_UniPro_DME_HIBERNATE_ENTER_ind_SAP_primitive_Value_After_Reset_0x0_Exists_Always
5	0h RW/C	**UHXS:** UIC_Hibernate_Exit_Status_UHXS_Indicates_that_the_Link_has_exited_UniPro_Hibernate_state_The_HCS_UPMCRS_register_bit_indicates_if_the_exit_process_is_not_successful_This_bit_corresponds_to_the_UniPro_DME_HIBERNATE_EXIT_ind_SAP_primitive_Value_After_Reset_0x0_Exists_Always
4	0h RW/C	**UPMS:** UIC_Power_Mode_Status_UPMS_Indicates_that_the_UniPro PADL_part_of_the_power_mode_change_is_complete_The_HCS_UPMCRS_register_bit_indicates_the_power_mode_change_status_This_bit_corresponds_to_the_UniPro_DME_POWERMODE_ind_SAP_primitive_Value_After_Reset_0x0_Exists_Always
3	0h RW/C	**UTMS:** UIC_Test_Mode_Status_UTMS_Indicates_that_the_peer_UniPro_stack_has_been_set_to_a_given_UniPro_test_mode_This_bit_corresponds_to_the_UniPro_DME_TEST_MODE_ind_SAP_primitive_Value_After_Reset_0x0_Exists_Always
2	0h RW/C	**UE:** UIC_Error_UE_Indicates_that_a_layer_in_the_UniPro_stack_has_encountered_an_error_condition_Register_bit_HCS_UEC_indicates_the_error_code_for_the_condition_This_bit_corresponds_to_the_UniPro_DME_ERROR_ind_SAP_primitive_Value_After_Reset_0x0_Exists_Always
1	0h RW/C	**UDEPRI:** UIC_DME_ENDPOINTRESET_Indication_UDEPRI_Indicates_that_the_attached_device_has_issued_an_DME_ENDPOINTRESET_indication_which_is_not_allowed_Value_After_Reset_0x0_Exists_Always
0	0h RW/C	**UTRCS:** UTP_Transfer_Request_Completion_Status_UTRCS_The_DWC_ufshc_core_sets_this_bit_to_when_one_of_the_following_events_occur_Completion_of_a_UTP_transfer_request_with_its_UTRD_Interrupt_bit_set_to_1_Interrupt_caused_by_the_UTR_interrupt_aggregation_logic_Value_After_Reset_0x0_Exists_Always

43.4.7 IE Ufs (IE) — Offset 24h

Interrupt Enable

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 24h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RW	**SBFEE:** System_Bus_Fatal_Error_Enable_SBFEE_When_set_and_IS_SBFES_is_set,_the_DWC_ufshc_core_generates_an_interrupt_Value_After_Reset_0x0_Exists_Always
16	0h RW	**HCFEE:** Host_Controller_Fatal_Error_Enable_HCFEE_When_set_and_IS_HCFES_is_set,_the_DWC_ufshc_core_generates_an_interrupt_Value_After_Reset_0x0_Exists_Always
15:13	0h RO	**Reserved**
12	0h RW	**UTPEE:** UTP_Error_Enable_UTPEE_When_set_and_IS_UTPES_is_set,_the_DWC_ufshc_core_generates_an_interrupt_Value_After_Reset_0x0_Exists_Always
11	0h RW	**DFEE:** Device_Fatal_Error_Enable_DFEE_When_set_and_IS_DFES_is_set,_the_DWC_ufshc_core_generates_an_interrupt_Value_After_Reset_0x0_Exists_Always
10	0h RW	**UCCE:** UIC_COMMAND_Completion_Enable_UCCE_When_set_and_IS_UCCS_is_set,_the_DWC_ufshc_core_generates_an_interrupt_Value_After_Reset_0x0_Exists_Always
9	0h RW	**UTMRCE:** UTP_Task_Management_Request_Completion_Enable_UTMRCE_When_set_and_IS_UTMRCS_is_set,_the_DWC_ufshc_core_generates_an_interrupt_Value_After_Reset_0x0_Exists_Always
8	0h RW	**ULSSE:** UIC_Link_Startup_Status_Enable_ULSSE_When_set_and_IS_ULSS_is_set,_the_DWC_ufshc_core_generates_an_interrupt_Value_After_Reset_0x0_Exists_Always
7	0h RW	**ULLSSE:** UIC_Link_Lost_Status_Enable_ULLSE_When_set_and_IS_ULLS_is_set,_the_DWC_ufshc_core_generates_an_interrupt_Value_After_Reset_0x0_Exists_Always
6	0h RW	**UHESE:** UIC_Hibernate_Enter_Status_Enable_UHESE_When_set_and_IS_UHES_is_set,_the_DWC_ufshc_core_generates_an_interrupt_Value_After_Reset_0x0_Exists_Always
5	0h RW	**UHXSE:** UIC_Hibernate_Exit_Status_Enable_UHXSE_When_set_and_IS_UHXS_is_set,_the_DWC_ufshc_core_generates_an_interrupt_Value_After_Reset_0x0_Exists_Always
4	0h RW	**UPMSE:** UIC_Power_Mode_Status_Enable_UPMSE_When_set_and_IS_UPMS_is_set,_the_DWC_ufshc_core_generates_an_interrupt_Value_After_Reset_0x0_Exists_Always
3	0h RW	**UTMSE:** UIC_Test_Mode_Status_Enable_UTMSE_When_set_and_IS_UTMS_is_set,_the_DWC_ufshc_core_generates_an_interrupt_Value_After_Reset_0x0_Exists_Always

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**UEE:** UIC_Error_Enable_UEE_When_set_and_IS_UEE_is_set,_the_DWC_ufshc_core_generates_an_interrupt_Value_After_Reset_0x0_Exists_Always
1	0h RW	**UDEPRIE:** UIC_DME_ENDPOINTRESET_UDEPRIE_When_set_and_IS_UDEPRI_is_set,_the_DWC_ufshc_core_generates_an_interrupt_Value_After_Reset_0x0_Exists_Always
0	0h RW	**UTRCE:** UTP_Transfer_Request_Completion_Enable_UTRCE_When_set_and_IS_UTRCS_is_set,_the_DWC_ufshc_core_generates_an_interrupt_Value_After_Reset_0x0_Exists_Always

43.4.8 HCS Ufs (HCS) — Offset 30h

Host Controller Status

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 30h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**TLUNUTPE:** Target_LUN_of_UTP_error_TLUNUTPE_The_LUN_of_the_command_that_a_UTP_error_occurs_during_execution_of_the_command_This_field_is_valid_only_when_UTPES_is_set_The_DWC_ufshc_core_automatically_resets_this_bit_when_UTPES_is_cleared_Value_After_Reset_0x0_Exists_Always
23:16	00h RO	**TTAGUTPE:** Task_Tag_of_UTP_error_TTAGUTPE_The_Task_Tag_of_the_command_that_a_UTP_error_occurs_during_execution_of_the_command_This_field_is_valid_only_when_UTPES_is_set_The_DWC_ufshc_core_automatically_resets_this_bit_when_UTPES_is_cleared_Value_After_Reset_0x0_Exists_Always
15:12	0h RO	**UTPEC:** UTP_Error_Code_UTPEC_Indicates_the_error_code_of_a_UTP_layer_error_This_field_is_valid_only_when_UTPES_is_set_The_DWC_ufshc_core_automatically_resets_this_bit_when_UTPES_is_cleared_Value_Description__0h_Reserved__1h_Invalid_transaction_type__2hFh_Reserved_Value_After_Reset_0x0_Exists_Always
11	0h RO	**Reserved**
10:8	0h RO	**UPMCRS:** UIC_Power_Mode_Change_Request_Status_UPMCRS_Indicates_the_status_of_a_UIC_layer_request_for_power_mode_change_Value_Description_0h_PWR_OK_The_request_is_accepted_1h_PWR_LOCAL_The_local_request_is_successfully_applied_2h_PWR_REMOTE_The_remote_request_is_successfully_applied_Not_used_because_this_is_associated_with_a_UIC_power_mode_change_request_from_the_UFS_Device,_which_is_not_permitted_3h_PWR_BUSY_The_request_is_aborted_because_of_concurrent_requests_Not_used_because_this_is_associated_with_a_UIC_power_mode_change_request_from_the_UFS_Device,_which_is_not_permitted_4h_PWR_ERROR_CAP_The_request_is_rejected_because_the_requested_configuration_exceeded_the_Links_capabilities_5h_PWR_FATAL_ERROR_The_request_is_aborted_because_of_a_communication_problem_The_Link_may_not_be_operable_6h_7h_Reserved_Value_After_Reset_0x0_Exists_Always

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	**Reserved**
3	0h RO	**UCRDY:** UIC_COMMAND_Ready_UCRDY_Indicates_whether_the_DWC_ufshc_core_is_ready_to_process_the_UIC_COMMAND_The_host_application_must_only_set_UICCMD_if_HCS_UCRDY_is_set_to_1_This_field_is_set_to_1_if_all_the_following_conditions_are_true_IS_DFES_0_IS_HCFES_0_No_UIC_command_is_issued_or_the_outstanding_UIC_command_is_complete_IS_UCCS_1_The_DWC_ufshc_core_clears_this_field_to_0_when_one_of_the_following_conditions_occur_IS_DFES_1_IS_HCFES_1_A_write_access_to_the_UICCMD_register_Value_After_Reset_0x0_Exists_Always
2	0h RO	**UTMRLRDY:** UTP_Task_Management_Request_List_Ready_UTMRLRDY_This_field_is_set_to_1_if_all_of_the_following_conditions_are_true_HCS_DP_1_UTMRLDBR_FFh_IS_DFES_0_IS_HCFES_0_The_DWC_ufshc_core_clears_this_field_to_0_when_one_of_the_following_conditions_occur_HCS_DP_0_UTMRLDBR_FFh_IS_DFES_1_IS_HCFES_1_The_host_application_must_only_set_the_UTMRLRSR_bit_if_HCS_UTMRLRDY_is_set_to_1_Value_After_Reset_0x0_Exists_Always
1	0h RO	**UTRLRDY:** UTP_Transfer_Request_List_Ready_UTRLRDY_This_field_is_set_to_1_if_all_of_the_following_conditions_are_true_HCS_DP_1_UTRLDBR_FFFF_FFFFh_IS_DFES_0_IS_HCFES_0_This_field_is_cleared_to_0_by_the_host_controller_when_one_of_the_following_conditions_occur_HCS_DP_0_UTRLDBR_FFFF_FFFFh_IS_DFES_1_IS_HCFES_1_The_host_application_must_only_set_the_UTRLRSR_bit_to_1_if_HCS_UTRLRDY_is_set_to_1_Value_After_Reset_0x0_Exists_Always
0	0h RO	**DP:** Device_Present_DP_1_A_UFS_device_is_attached_to_the_DWC_ufshc_core_0_Nonvolatile_memory_is_not_attached_to_the_DWC_ufshc_core_DP_is_set_to_1_if_the_UIC_layer_is_in_the_LinkUp_power_state_Value_After_Reset_0x0_Exists_Always

43.4.9 HCE Ufs (HCE) — Offset 34h

Host Controller Enable

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 34h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**HCE:** Host_Controller_Enable_HCE_When_set_to_1,_the_DWC_ufshc_core_autonomously_goes_through_the_following_initialization_sequence_Warm_hardware_reset_of_the_DWC_ufshc_core_DME_RESET_DME_ENABLE_The_HCE_bit_stays_0_during_the_initialization_sequence_If_DME_ENABLE_is_not_successful,_HCE_stays_0_If_the_initialization_sequence_is_successful,_HCE_becomes_1_When_HCE_is_cleared_to_0,_the_DWC_ufshc_core_is_disabled_and_register_values_except_for_the_DWC_ufshc_map_DWC_ufshc_block_CAP_are_volatile_and_may_lose_their_content_If_HCE_is_1_and_a_0_is_written_to_the_HCE_register,_the_HCE_bit_stays_1_until_all_outstanding_OCP_read_requests_are_completed_Note_When_DWC_UFSHC_STANDALONE_is_1,_BUSTHRTL_DME_CTRL_LOGIC_EN_must_be_programmed_to_1_for_automatic_issue_of_DME_RESET_and_DME_ENABLE_Value_After_Reset_0x0_Exists_Always

43.4.10 UECPA Ufs (UECPA) — Offset 38h

Host UIC Error Code PHY Adapter Layer

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 38h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/C	**UIC_PHY_ERR:** UIC_PHY_Adapter_Layer_Error_ERR_Indicates_whether_an_error_was_generated_by_the_PHY_Adapter_Layer_Value_After_Reset_0x0_Exists_Always
30:5	0h RO	**Reserved**
4:0	00h RO/C	**UIC_PHY_EC:** UIC_Adapter_Layer_Error_EC_Error_code_generated_when_IS_UE_and_UECPA_ERR_are_set_to_1_Bit_Description_00_PHY_error_on_Lane_0_01_PHY_error_on_Lane_1_02_PHY_error_on_Lane_2_03_PHY_error_on_Lane_3_04_Generic_PHY_Adapter_error_is_flagged_if_there_is_a_line_reset_that_is_initiated_by_either_the_local_or_the_peer_device_Value_After_Reset_0x0_Exists_Always

43.4.11 UECDL Ufs (UECDL) — Offset 3Ch

Host UIC Error Code Data Link Layer

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 3Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/C	**UIC_DLL_ERR:** UIC_Data_Link_Layer_Error_ERR_Indicates_whether_an_error_is_generated_by_the_Data_Link_Layer_Value_After_Reset_0x0_Exists_Always
30:15	0h RO	**Reserved**
14:0	0000h RO/C	**UIC_DLL_EC:** UIC_Data_Link_Layer_Error_EC_Error_code_generated_when_IS_UE_and_UECDL_ERR_are_set_to_1_For_more_information_on_the_definitions_of_the_error_codes,_see_the_UniPro_Specification_UNIPRO_Bit_Description_00_NAC_RECEIVED_01_TCx_REPLAY_TIMER_EXPIRED_02_AFCx_REQUEST_TIMER_EXPIRED_03_FCx_PROTECTION_TIMER_EXPIRED_04_CRC_ERROR_05_RX_BUFFER_OVERFLOW_06_MAX_FRAME_LENGTH_EXCEEDED_07_WRONG_SEQUENCE_NUMBER_08_AFC_FRAME_SYNTAX_ERROR_09_NAC_FRAME_SYNTAX_ERROR_10_EOF_SYNTAX_ERROR_11_FRAME_SYNTAX_ERROR_12_BAD_CTRL_SYMBOL_TYPE_13_PA_INIT_ERROR_14_PA_ERROR_IND_RECEIVED_Value_After_Reset_0x0_Exists_Always

43.4.12 UECN Ufs (UECN) — Offset 40h

Host UIC Error Code Network Layer

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 40h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/C	**UIC_NL_ERR:** UIC_Network_Layer_Error_ERR_Indicates_whether_an_error_was_generated_by_the_Network_Layer_Value_After_Reset_0x0_Exists_Always
30:3	0h RO	**Reserved**
2:0	0h RO/C	**UIC_NL_EC:** UIC_Network_Layer_Error_Code_EC_Error_code_generated_when_IS_UE_and_UECN_ERR_are_set_to_1_For_more_information_on_the_definitions_of_the_error_codes,_see_the_UniPro_Specification_UNIPRO_Bit_Description_00_UNSUPPORTED_HEADER_TYPE_01_BAD_DEVICEID_ENC_02_LHDR_TRAP_PACKET_DROPPING_Value_After_Reset_0x0_Exists_Always

43.4.13 UECT Ufs (UECT) — Offset 44h

Host UIC Error Code Transport Layer

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 44h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/C	**UIC_TL_ERR:** UIC_Transport_Layer_Error_ERR_Indicates_whether_an_error_was_generated_by_the_Transport_Layer_Value_After_Reset_0x0_Exists_Always
30:7	0h RO	**Reserved**
6:0	00h RO/C	**UIC_TL_EC:** UIC_Transport_Layer_Error_Code_EC_Error_code_generated_when_IS_UE_and_UECT_ERR_are_set_to_1_For_more_information_on_the_definitions_of_the_error_codes,_see_the_UniPro_Specification_UNIPRO_Bit_Description_00_UNSUPPORTED_HEADER_TYPE_01_UNKNOWN_CPORTID_02_NO_CONNECTION_RX_03_CONTROLLED_SEGMENT_DROPPING_04_BAD_TC_05_E2E_CREDIT_OVERFLOW_06_SAFETY_VALVE_DROPPING_Value_After_Reset_0x0_Exists_Always

43.4.14 UECDME Ufs (UECDME) — Offset 48h

Host UIC Error Code

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 48h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/C	**UIC_DME_ERR:** UIC_DME_Error_ERR_Indicates_whether_an_error_was_generated_by_the_DME_Value_After_Reset_0x0_Exists_Always
30:1	0h RO	**Reserved**
0	0h RO/C	**UIC_DME_EC:** UIC_DME_Error_Code_EC_Error_code_generated_when_IS_UE_and_UECDME_ERR_are_set_to_1_Bit_Description_00_Generic_DME_error_Value_After_Reset_0x0_Exists_Always

43.4.15 UTRIACR Ufs (UTRIACR) — Offset 4Ch

UTP Transfer Request Interrupt Aggregation Control Register

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 4Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**IAEN:** Interrupt_Aggregation_Enable_Disable_When_set_to_0_by_the_host_application,_command_responses_are_not_counted_nor_timed_Interrupts_are_still_triggered_by_responses_where_the_interrupt_bit_is_set_in_the_UTRD_When_set_to_1,_the_interrupt_aggregation_mechanism_is_enabled_and_aggregationbased_interrupts_are_generated_Bit_Description_00_Disabled_01_Enabled_Value_After_Reset_0x0_Exists_Always
30:25	0h RO	**Reserved**
24	0h WO	**IAPWEN:** Interrupt_aggregation_parameter_write_enable_IAPWEN_When_the_host_application_writes_1,_the_values_in_IACTH_and_IATOVAL_are_updated_with_the_contents_written_at_the_same_cycle_When_the_host_application_writes_0,_the_values_in_IACTH_and_IATOVAL_are_not_updated_Note_Write_operations_to_IACTH_and_IATOVAL_are_only_allowed_when_no_commands_are_outstanding_Value_After_Reset_0x0_Exists_Always
23:21	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**IASB:** Interrupt_aggregation_status_bit_IASB_This_bit_indicates_to_the_host_application_whether_any_responses_have_been_received_and_counted_towards_interrupt_aggregation_that_is,_IASB_is_set_if_IA_counter_is_greater_than_0_Bit_Value_Description_0_No_commands_are_received_since_the_last_counter_reset_IA_counter0_1_At_least_one_command_has_been_received_and_counted_IA_counter_0_Value_After_Reset_0x0_Exists_Always
19:17	0h RO	**Reserved**
16	0h WO	**CTR:** Counter_and_Timer_Reset_CTR_When_the_host_application_writes_1,_the_interrupt_aggregation_timer_and_counter_are_reset_It_is_recommended_that_the_host_application_use_this_field_to_reset_the_timer_and_counter_every_time_it_services_newly_received_UTP_responses_Value_After_Reset_0x0_Exists_Always
15:13	0h RO	**Reserved**
12:8	00h RW	**IACTH:** Interrupt_aggregation_counter_threshold_IACTH_The_host_application_uses_this_field_to_configure_the_number_of_responses_that_are_required_to_generate_an_interrupt_As_UTP_responses_are_received_by_the_DWC_ufshc_core,_they_are_counted_When_the_count_reaches_the_value_configured_in_this_field,_an_interrupt_is_generated_IS_UTRCS_bit_is_set_The_maximum_allowed_value_is_31_When_IACTH_is_0,_responses_are_not_counted,_and_countingbased_interrupts_are_not_generated_In_order_to_write_to_this_field,_the_IAPWEN_bit_must_be_set_at_the_same_write_operation_QUERY_RESPONSE_UPIUs_and_NOP_IN_UPIUs_are_not_counted_by_the_Interrupt_Aggregation_logic_Value_After_Reset_0x0_Exists_Always
7:0	00h RW	**IATOVAL:** Interrupt_aggregation_timeout_value_IATOVAL_The_host_application_uses_this_field_to_configure_the_maximum_time_allowed_between_a_response_arrival_to_the_DWC_ufshc_core_and_the_generation_of_an_interrupt_Timer_Operation_The_timer_is_reset_by_the_application_during_the_interrupt_service_routine_It_starts_running_when_the_DWC_ufshc_core_receives_the_first_response_to_a_Regular_Command,_after_the_timer_is_reset_The_timer_stops_when_it_reaches_the_value_configured_in_IATOVAL_field,_and_IS_UTRCS_bit_is_set_When_IATOVAL_is_0,_the_timer_does_not_run,_and_timerbased_interrupts_are_not_generated_The_Time_units_in_this_field_are_40_us_Therefore,_writing_0x01_represents_a_timeout_value_of_40_us,_and_writing_0xFF_represents_a_timeout_value_of_10_2_ms_QUERY_RESPONSE_UPIUs_and_NOP_IN_UPIUs_are_not_counted_by_the_Interrupt_Aggregation_logic_Value_After_Reset_0x0_Exists_Always

43.4.16 UTRLBA Ufs (UTRLBA) — Offset 50h

UTP Transfer Request List Base Address

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 50h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:10	000000h RW	**UTP_UTRLBA:** UTP_Transfer_Request_List_Base_Address_UTRLBA_Indicates_the_32bit_base_physical_address_for_the_UTP_Transfer_Request_list_This_base_is_used_when_fetching_commands_for_execution_The_structure_pointed_to_by_this_address_range_is_1KB_in_length_This_address_is_1KB_aligned_as_indicated_by_bits_90_being_read_only_Value_After_Reset_0x0_Exists_Always
9:0	0h RO	**Reserved**

43.4.17 UTRLBAU Ufs (UTRLBAU) — Offset 54h

UTP Transfer Request List Base Address Upper 32-bits

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 54h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**UTP_UTRLBAU:** UTP_Transfer_Request_List_Base_Address_Upper_UTRLBAU_Indicates_the_upper_32bits_for_the_UTP_Transfer_Request_list_base_physical_address_This_base_is_used_when_fetching_commands_for_execution_Value_After_Reset_0x0_Exists_Always_Memory_Access_utrlbau_access

43.4.18 UTRLDBR Ufs (UTRLDBR) — Offset 58h

UTP Transfer Request List Door Bell Register

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 58h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**UTP_UTRLDBR:** UTP_Transfer_Request_List_Door_bell_Register_UTRLDBR_This_field_is_bit_significant_Each_bit_corresponds_to_a_slot_in_the_UTP_Transfer_Request_List,_where_bit_0_corresponds_to_request_slot_0_A_bit_in_this_field_is_set_to_1_by_the_host_application_to_indicate_to_the_DWC_ufshc_core_that_a_transfer_request_has_been_built_in_system_memory_for_the_associated_transfer_request_slot_and_may_be_ready_for_execution_The_host_application_indicates_no_change_to_request_slots_by_setting_the_associated_bits_in_this_filed_to_0_Bits_in_this_field_must_be_set_to_1_or_0_by_the_host_application_when_UTRLRSR_is_set_to_1_When_a_transfer_request_is_completed_with_success_or_error,_the_corresponding_bit_is_cleared_to_0_by_the_DWC_ufshc_core_The_DWC_ufshc_core_always_processes_transfer_requests_inorder_according_to_the_order_submitted_to_the_list_If_there_are_multiple_commands_with_single_door_bell_register_ringing_batch_mode,_The_dispatch_order_for_these_transfer_requests_by_host_controller_will_base_on_their_index_in_the_List_A_transfer_request_with_lower_index_value_will_be_executed_before_a_transfer_request_with_higher_index_value_This_field_is_also_cleared_when_UTRLRSR_is_written_from_a_1_to_a_0_by_the_host_application_Value_After_Reset_0x0_Exists_Always

43.4.19 UTRLCLR Ufs (UTRLCLR) — Offset 5Ch

UTP Transfer Request List CLear Register

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 5Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WO	**UTP_UTRLCLR:** UTP_Transfer_Request_List_CLear_Register_UTRLCLR_This_field_is_bit_significant_Each_bit_corresponds_to_a_slot_in_the_UTP_Transfer_Request_List,_where_bit_0_corresponds_to_request_slot_0_A_bit_in_this_field_is_set_to_0_by_the_host_application_to_indicate_to_the_DWC_ufshc_core_that_a_transfer_request_slot_is_cleared_The_DWC_ufshc_core_frees_up_any_resources_associated_to_the_request_slot_immediately,_and_sets_the_associated_bit_in_UTRLDBR_to_0_The_host_application_indicates_no_change_to_request_slots_by_setting_the_associated_bits_in_this_field_to_1_Bits_in_this_field_must_be_set_to_1_or_0_by_the_host_application_when_UTRLRSR_is_set_to_1_The_host_application_must_use_this_field_only_when_a_UTP_Transfer_Request_is_not_expected_to_complete,_for_example,_when_a_Transfer_Request_is_aborted,_or_in_case_of_a_system_bus_error,_such_as_an_invalid_UTRD_Value_After_Reset_0x0_Exists_Always

43.4.20 UTRLRSR Ufs (UTRLRSR) — Offset 60h

UTP Transfer Request List Run Stop Register

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 60h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**UTP_UTRLRSR:** UTP_Transfer_Request_List_RunStop_Register_UTRLRSR_When_set_to_1,_the_DWC_ufshc_core_may_process_the_list_The_DWC_ufshc_core_starts_processing_the_list_at_entry_0_The_DWC_ufshc_core_continues_to_process_the_list_as_long_as_this_bit_is_set_to_1_When_cleared_to_0,_the_DWC_ufshc_core_continues_to_complete_all_the_outstanding_transfer_requests_in_the_list_and_then_stops_When_cleared_to_0,_the_DWC_ufshc_core_clears_UTRLRDY_to_0_This_bit_must_be_set_to_1_when_HCS_UCRDY_and_HCS_UTRLRDY_and_HCS_UTMRLRDY_is_set_to_1_Value_After_Reset_0x0_Exists_Always

43.4.21 UTMRLBA Ufs (UTMRLBA) — Offset 70h

UTP Task Management Request List Base Address

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 70h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:10	000000h RW	**UTP_UTMRLBA:** UTP_Task_Management_Request_List_Base_Address_UTMRLBA_Indicates_the_32bit_base_physical_address_for_the_list_This_base_is_used_when_fetching_Task_Management_Functions_for_execution_The_structure_pointed_to_by_this_address_range_is_1KB_in_length_This_address_shall_be_1KB_aligned_as_indicated_by_bits_90_being_read_only_Value_After_Reset_0x0_Exists_Always
9:0	0h RO	**Reserved**

43.4.22 UTMRLBAU Ufs (UTMRLBAU) — Offset 74h

UTP Task Management Request List Base Address Upper 32-bits

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 74h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**UTP_UTMRLBAU:** UTP_Task_Management_Request_List_Base_Address_UTMRLBAU_Indicates_the_upper_32bits_for_the_list_base_physical_address_This_base_is_used_when_fetching_task_management_functions_for_execution_Value_After_Reset_0x0_Exists_Always_Memory_Access_utmrlbau_access

43.4.23 UTMRLDBR Ufs (UTMRLDBR) — Offset 78h

UTP Task Management Request List Door Bell Register

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 78h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**UTP_UTMRLDBR:** UTP_Task_Management_Request_List_Door_bell_Register_UTMRLDBR_This_field_is_bit_significant_Each_bit_corresponds_to_a_task_management_request_slot_in_the_List,_where_bit_0_corresponds_to_slot_0_The_host_application_sets_this_field_to_indicate_to_the_DWC_ufshc_core_that_a_task_management_request_is_built_in_system_memory_and_may_be_ready_for_execution_When_a_task_management_request_is_completed_with_success_or_error,_the_DWC_ufshc_core_clears_the_corresponding_bit_to_0_Bits_in_this_field_are_only_set_to_1_by_the_host_application_when_UTMRLRSR_is_set_to_1_The_DWC_ufshc_core_always_processes_task_management_request_in_order_according_to_the_order_submitted_to_the_list_If_there_are_multiple_requests_with_single_door_bell_register_ringing_batch_mode,_the_dispatch_order_for_these_requests_by_DWC_ufshc_core_are_based_on_their_index_in_the_List_A_task_management_with_lower_index_value_is_executed_before_a_task_management_request_with_a_higher_index_value_This_bit_is_cleared_when_UTMRLRSR_is_written_from_1_to_0_by_the_host_application_Value_After_Reset_0x0_Exists_Always

43.4.24 UTMRLCLR Ufs (UTMRLCLR) — Offset 7Ch

UTP Task Management Request List CLear Register

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 7Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h WO	**UTP_UTMRLCLR:** UTP_Task_Management_List_CLear_Register_UTRLCLR_This_field_is_bit_significant_Each_bit_corresponds_to_a_slot_in_the_task_management_request_List,_where_bit_0_corresponds_to_slot_0_A_bit_in_this_field_is_set_to_0_by_the_host_application_to_indicate_to_the_DWC_ufshc_core_that_a_task_management_request_slot_is_cleared_The_DWC_ufshc_core_immediately_frees_up_any_resources_associated_to_the_task_management_request_slot_and_sets_the_associated_bit_in_UTMRLDBR_to_0_The_host_application_indicates_no_change_to_task_management_request_slots_by_setting_the_associated_bits_in_this_field_to_1_Bits_in_this_field_are_only_set_to_1_or_0_by_the_host_application_when_UTRLRSR_is_set_to_1_The_host_application_uses_this_field_only_when_a_UTP_Task_Management_Request_is_not_expected_to_complete_for_example,_if_there_is_a_system_bus_error,_such_as_an_invalid_UTMRD_Value_After_Reset_0x0_Exists_Always

43.4.25 UTMRLRSR Ufs (UTMRLRSR) — Offset 80h

UTP Task Management Request List Run Stop Register

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 80h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**UTP_UTMRLRSR:** UTP_Task_Management_Request_List_RunStop_Register_UTMRLRSR_When_set_to_1,_the_DWC_ufshc_core_may_process_the_list_The_DWC_ufshc_core_starts_processing_the_list_at_entry_0_The_DWC_ufshc_core_continues_to_process_the_list_as_long_as_this_bit_is_set_to_1_When_cleared_to_0,_the_DWC_ufshc_core_continues_to_complete_all_outstanding_task_management_requests_in_the_list_and_then_stops_When_cleared_to_0,_the_DWC_ufshc_core_clears_UTMRLRDY_to_0_This_bit_is_only_set_to_1_when_HCS_UTMRLRDY_is_set_to_1_Value_After_Reset_0x0_Exists_Always

43.4.26 UICCMD Ufs (UICCMD) — Offset 90h

UIC Command

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 90h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**UICCMD_CMDOP:** Command_Opcode_CMDOP_Indicates_the_Opcode_of_a_UIC_command_to_be_dispatched_to_the_local_UIC_layer_When_this_register_is_set,_the_DWC_ufshc_core_takes_the_values_of_UICCMDARGx_as_the_corresponding_parameters_input_and_output_that_are_a_part_of_the_UIC_Command_Opcode_UIC_Commands_Configuration_01h_DME_GET_02h_DME_SET_03h_DME_PEER_GET_04h_DME_PEER_SET_05h_0Fh_Reserved_Control_10h_11h_Reserved_12h_DME_ENABLE_not_permitted_13h_Reserved_14h_DME_RESET_15h_DME_ENDPOINTRESET_16h_DME_LINKSTARTUP_17h_DME_HIBERNATE_ENTER_18h_DME_HIBERNATE_EXIT_19h_FFh_Reserved_Value_After_Reset_0x0_Exists_Always

43.4.27 UICCMDARG1 Ufs (UICCMDARG1) — Offset 94h

UIC Command Argument 1

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 94h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**UIC_ARG1:** Argument_1ARG1_This_contains_the_value_for_the_first_argument_of_the_UIC_command_if_applicable_The_contents_of_this_field_vary_depending_on_the_UIC_Command_UICCMD_

43.4.28 UICCMDARG2 Ufs (UICCMDARG2) — Offset 98h

UIC Command Argument 2

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 98h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**UIC_ARG2:** Argument_2_ARG2_This_register_contains_the_value_for_the_second_argument_of_the_UIC_command_if_applicable_The_contents_of_this_field_vary_depending_on_the_UIC_Command_

43.4.29 UICCMDARG3 Ufs (UICCMDARG3) — Offset 9Ch

UIC Command Argument 3

Type	Size	Offset	Default
MMIO	32 bit	FD320000h + 9Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
RW	RW	RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**UIC_ARG3:** Argument_3_ARG3_This_register_contains_the_value_for_the_third_argument_of_the_UIC_command_if_applicable_The_contents_of_this_field_vary_depending_on_the_UIC_Command_

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