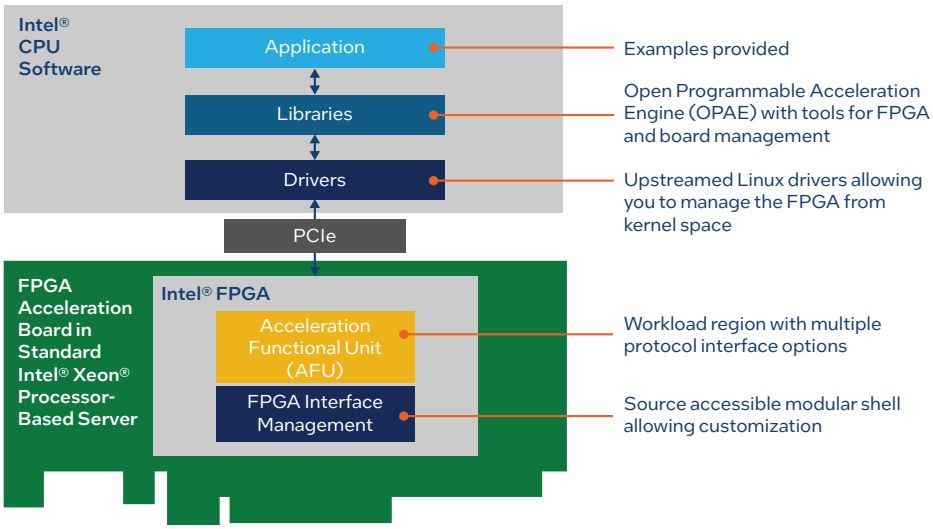
Product Brief

Acceleration
FPGA

Open FPGA Stack

Leverage an Open Source Framework to Ease Custom FPGA-based Workload and Platform Development

OFS Block Diagram



Open FPGA Stack (OFS) is a scalable, open source hardware and software infrastructure that addresses the challenges associated with designing FPGA-based acceleration platform solutions in Intel® Xeon® processor-based servers. OFS eases custom board and workload development by providing a reference infrastructure and UVM verification environment with all the necessary components that you may choose to modify or leverage as-is.

OFS enables software, hardware, and application developers to:

- **Leverage Open Source and Upstreamed Code** delivered in the OFS GitHub Repository, enabling native support from leading software vendors
- **Use Standard Interfaces and Application Programming Interfaces (APIs)** to accelerate workload development and enable code reuse
- **Port existing workloads to the Acceleration Functional Unit (AFU) Region** and proliferate across OFS-based platforms for FPGA-based acceleration or CPU offload
- **Utilize a growing ecosystem** of OFS-enabled boards and workloads provided by Intel and third parties
- **Deploy Bare Metal, Virtualized, or Containerized** applications with data center class management for NFV, SmartNIC, VRAN, FSI, and more
- **Build Application Specific FPGA Interface Managers (FIMs)** from the provided reference FIMs using a modular, 'take and tailor' approach

Board Developers

Use the open source, modular infrastructure to quickly create application specific FPGA Interface Mangers (FIMs) tailored to the differentiated needs of various boards and target workloads.

Software Developers

Leverage the OPAE software development kit, libraries, and APIs along with upstreamed, open-source kernel drivers that target the FIM and accelerate integration into common application frameworks.

Application Developers

Tap into a proven infrastructure and growing ecosystem to achieve greater return on investment and proliferation of workloads across a growing number of OFS-based platforms.

What's Inside

Hardware

Acceleration Functional Unit (AFU) Region

What it is: The AFU is the algorithm or processing unit that provides FPGA-based acceleration and/or CPU offload.

Why it's important: Workload performance is improved by offloading a computational operation for an application from the CPU to the FPGA's AFU region. The AFU region includes an optional Partial Reconfiguration (PR) region for dynamic configuration. Providing a designated area with specific insertion points for customization allows for cleaner, easier to manage RTL.

FPGA Interface Manager (FIM)

What it is: Reference FIMs provide platform management, functionality, clocks, resets, and standard interfaces to the host and AFU.

Why it's important: These easy-to-use reference FIMs are provided as working examples to help users develop their own custom platforms. They are designed to be modular and scalable, so customers can 'take and tailor' the design blocks relevant to their application.

Board Management Controller (BMC)

What it is: The BMC is responsible for controlling, monitoring, and granting access to board features.

Why it's important: The BMC provides root of trust and authentication to verify that bitstreams come from a trusted source. It interfaces to the server management controller using inudstry standard AXI protocols.

oneAPI Accelerator Support Package (ASP)

What it is: A collection of hardware and software components enabling HLD-based workload support.

Why it's important: HLD abstracts the FPGA hardware and design flow, enabling users to design FPGA custom hardware with familiar programming languages and development environments. HLD also provides extensible code that can be reused across architectures and vendors.

Software

Upstreamed, Open-Source Kernel Drivers

What it is: The OFS kernel drivers are the first layer in the FPGA software stack.

Why it's important: This layer decomposes implemented functionality into sets of individual device features, providing a clean and extensible framework for the creation and integration of additional functionalities and their features. Kernel drivers are being upstreamed to the Linux kernel (kernel.org) to enable native support for OFS by third-party open-source software vendors.

OPAE libraries and APIs

What it is: The OPAE C libraries are lightweight, user-space libraries that provide abstraction for FPGA resources in a compute environment.

Why it's important: This library abstracts hardware and OS specific details, exposing the underlying FPGA resources as a set of features accessible from within software running on the host. The unified C API supports different FPGA integration and deployment models to enable portability across OS's and bare metal, hypervisor, or containerized use models.

OPAE Tools

What it is: OPAE installs tools to expedite development.

Why it's important: These tools provide useful functions such as: displaying FPGA information, implementing a secure firmware update, enabling virtualization, downloading new images to the board, and more.

UVM Test Framework

What it is: The Universal Verification Method (UVM) test framework provides a verification environment for the FIM and AFU.

Why it's important: UVM delivers a modular, reusable, and scalable testbench structure by providing an API framework and unit test cases that can be deployed across multiple projects.

OFS Customer Development Flow

		Two Routes of Development		
		Using a custom or 3rd party board	OR	Using an OFS reference platform
Evaluation	**Step 1:** Choose a route	• Out-of-the-box, ready-to-deploy solution • Recommended for custom application development		• Full end-to-end solution that is completely open source and customizable • Recommended for custom board development
Evaluation	**Step 2**: Choose a board	Browse the OFS Board Catalog at www.intel.com/OFS		**Intel Agilex FPGA** Intel Agilex 7 FPGA I-Series Dev Kit Intel Agilex 7 FPGA F-Series Dev Kit Intel IPU F2000X-PL Platform Intel FPGA SmartNIC N6001PL-Platform **Intel Stratix 10 FPGA** D5005 Programmable Acceleration Card
Evaluation	**Step 3**: Evaluate OFS open-source resources	Board vendor will provide corresponding version of OFS technical documentation		Technical documentation can be referenced on GitHub pages at www.ofs.github.io
Development	**Step 4**: Access open-source hardware and software code	Board vendor will provide corresponding OFS software or hardware code. Contact ofs.marketing@intel.com for help facilitating communication, or post in the OFS GitHub Discussions tab		Modify or use the provided OFS software or hardware code available at www.github.com/OFS
Development	**Step 5**: Develop workloads using RTL or C/C++	Follow the OFS RTL flow OR Utilize the oneAPI development flow and build FPGA workloads in C/C++		
Technical Support	**Step 6**: Request technical support	Request support by working through the board vendor and their Intel Sales Representative		Request support through IPS or by posting a question in the Discussions tab on the OFS GitHub

Open-Source Methodology

All OFS hardware and software code is open source and delivered through the OFS GitHub Repository. Technical documentation is also open source and co-located with the code.

Intel will soon allow contributions back from users who wish to share with the OFS community. This will enable the OFS infrastructure to grow and be enriched more quickly.

Intel FPGA-Based Acceleration Platforms

Intel FPGA-based Infrastructure Processing Units (IPUs) and Programmable Acceleration Cards (PACs) are production-qualified, acceleration hardware solutions designed for telecommunications, cloud services, and other data center environments. Similarly, Intel Acceleration Development Platforms (ADPs) are reference platforms that include all major solution ingredients needed for initial evaluation before porting to a production platform.

The Stratix 10 FPGA code line of OFS is developed and validated using the Intel FPGA PAC D5005. The Intel Agilex 7 FPGA code line is developed and validated using the Intel Agilex 7 FPGA I-Series Development Kit, the Intel Agilex 7 FPGA F-Series Development Kit, the Intel FPGA IPU F2000X-PL Platform, and the Intel N6000 Development Platform. Reference platforms can be leveraged for design of an Intel-FPGA based, third party or custom platform.

Intel partners also provide OFS-enabled platforms for development and deployment. These Intel Stratix 10 and Intel Agilex FPGA-based platforms enable users to build OFS-based software and applications faster without significant hardware development or expertise. To browse all available ecosystem platforms, visit our OFS Board Catalog.

Get Started

- Visit the Open Source OFS GitHub Repository for all source code and documentation
- Browse the OFS Board Catalog
- Learn more about the Intel Agilex 7 FPGA I-Series Development Kit
- Learn more about the Intel Agilex 7 FPGA F-Series Development Kit
- Learn more about the Intel IPU F2000X-PL Platform
- Learn more about the N6000 Acceleration Development Platform
- Learn more about the Silicom FPGA SmartNIC N5010 Series

ss-1125-1.4