











Bank Number	WREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F996	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2/3	HMC Pin Assignment for LPDDR2	HPS Pin Max Select 3	HPS Pin Max Select 2	HPS Pin Max Select 1	HPS Pin Max Select 0
BA	WREFBAND0	IO			DIFF0_RX_T21a	DIFFOUT_T21a	H13	DQS3T	DQ3T						
BA	WREFBAND0	IO			DIFF0_TX_T22a	DIFFOUT_T22a	D5								
BA	WREFBAND0	IO			DIFF0_RX_T21n	DIFFOUT_T21n	H12	DQS3T	DQ3T						
BA	WREFBAND0	IO			DIFF0_TX_T22n	DIFFOUT_T22n	C4	DQ3T							
BA	WREFBAND0	IO			DIFF0_RX_T23a	DIFFOUT_T23a	F11	DQ3T							
BA	WREFBAND0	IO			DIFF0_TX_T24a	DIFFOUT_T24a	E8	DQ3T							
BA	WREFBAND0	IO			DIFF0_RX_T23n	DIFFOUT_T23n	E11	DQ3T							
BA	WREFBAND0	IO			DIFF0_TX_T24n	DIFFOUT_T24n	D7								
BA	WREFBAND0	IO			DIFF0_RX_T25a	DIFFOUT_T25a	J7								
BA	WREFBAND0	IO			DIFF0_TX_T26a	DIFFOUT_T26a	B2	DQ4T							
BA	WREFBAND0	IO			DIFF0_RX_T25n	DIFFOUT_T25n	H2								
BA	WREFBAND0	IO			DIFF0_TX_T26n	DIFFOUT_T26n	B1	DQ4T							
BA	WREFBAND0	IO			DIFF0_RX_T27a	DIFFOUT_T27a	B6	DQ4T							
BA	WREFBAND0	IO			DIFF0_TX_T27n	DIFFOUT_T27n	C3	DQ4T							
BA	WREFBAND0	IO			DIFF0_RX_T28a	DIFFOUT_T28a	B5	DQ4T							
BA	WREFBAND0	IO			DIFF0_TX_T28n	DIFFOUT_T28n	B3	DQ4T							
BA	WREFBAND0	IO			DIFF0_RX_T29a	DIFFOUT_T29a	K12	DQS4T	DQS4T						
BA	WREFBAND0	IO			DIFF0_TX_T30a	DIFFOUT_T30a	D9								
BA	WREFBAND0	IO			DIFF0_RX_T29n	DIFFOUT_T29n	J12	DQS4T	DQS4T						
BA	WREFBAND0	IO			DIFF0_TX_T30n	DIFFOUT_T30n	C2	DQ4T							
BA	WREFBAND0	IO			DIFF0_RX_T31a	DIFFOUT_T31a	G12	DQ4T							
BA	WREFBAND0	IO			DIFF0_TX_T32a	DIFFOUT_T32a	E4	DQ4T							
BA	WREFBAND0	IO			DIFF0_RX_T31n	DIFFOUT_T31n	G11	DQ4T							
BA	WREFBAND0	IO			DIFF0_TX_T32n	DIFFOUT_T32n	D4								
BA	WREFBAND0	IO			DIFF0_RX_T33a	DIFFOUT_T33a	K7	DQS7							
BA	WREFBAND0	IO			DIFF0_TX_T34a	DIFFOUT_T34a	E3	DQ5T							
BA	WREFBAND0	IO			DIFF0_RX_T33n	DIFFOUT_T33n	K8								
BA	WREFBAND0	IO			DIFF0_TX_T34n	DIFFOUT_T34n	E2	DQ5T							
BA	WREFBAND0	IO			DIFF0_RX_T35a	DIFFOUT_T35a	G19	DQS7							
BA	WREFBAND0	IO			DIFF0_TX_T36a	DIFFOUT_T36a	E1	DQ5T							
BA	WREFBAND0	IO			DIFF0_RX_T35n	DIFFOUT_T35n	F10	DQ5T							
BA	WREFBAND0	IO			DIFF0_TX_T36n	DIFFOUT_T36n	D1	DQ5T							
BA	WREFBAND0	IO			DIFF0_RX_T37a	DIFFOUT_T37a	H19	DQS5T							
BA	WREFBAND0	IO			DIFF0_TX_T38a	DIFFOUT_T38a	E7	DQS5T							
BA	WREFBAND0	IO			DIFF0_RX_T37n	DIFFOUT_T37n	J9	DQS5T							
BA	WREFBAND0	IO			DIFF0_TX_T38n	DIFFOUT_T38n	E6	DQ5T							
BA	WREFBAND0	IO			DIFF0_RX_T39a	DIFFOUT_T39a	F9	DQ5T							
BA	WREFBAND0	IO			DIFF0_TX_T40a	DIFFOUT_T40a	G7	DQ5T							
BA	WREFBAND0	IO			DIFF0_RX_T39n	DIFFOUT_T39n	F8	DQ5T							
BA	WREFBAND0	IO			DIFF0_TX_T40n	DIFFOUT_T40n	F6								
BA		MSEL0		MSEL0			L8								
BA		ICONE_DONE		ICONE_DONE			F3								
BA		MSEL1		MSEL1			K6								
BA		!STATUS		!STATUS			F4								
BA		HCE		HCE			OC								
BA		MSEL2		MSEL2			G6								
BA		MSEL3		MSEL3			L7								
BA		HCONFIG		HCONFIG			L5								
BA		MSEL4		MSEL4			L3								
		GND					J8								
		GND					A13								
		GND					A17								
		GND					A2								
		GND					A23								
		GND					A27								
		GND					AA11								
		GND					AA2								
		GND					AA3								
		GND					AA4								
		GND					AA6								
		GND					AA8								
		GND					AB1								
		GND					AB19								
		GND					AB2								
		GND					AB29								
		GND					AB5								
		GND					AB7								
		GND					AC16								
		GND					AC26								
		GND					AC3								
		GND					AC4								
		GND					AC6								
		GND					AC8								
		GND					AD1								
		GND					AD2								
		GND					AD23								
		GND					AD5								
		GND					AE10								
		GND					AE20								
		GND					AE3								
		GND					AE4								
		GND					AF1								
		GND					AF12								
		GND					AF17								
		GND					AF2								
		GND					AF27								
		GND					AF3								
		GND					AG14								
		GND					AG24								
		GND					AG9								
		GND					AH1								
		GND					AH11								
		GND					AH21								
		GND					AH6								
		GND					AI18								
		GND					AJ28								
		GND					AJ3								
		GND					AJ30								
		GND					AK15								
		GND					AK25								
		GND					AK6								
		GND					B14								
		GND					B19								
		GND					B24								
		GND					B29								
		GND					B9								
		GND					CT								
		GND					C16								
		GND					C21								
		GND					C26								
		GND					C6								
		GND					D13								
		GND					D23								
		GND					D9								
		GND					E10								
		GND					E25								
		GND					E30								
		GND					F17								
		GND					F2								
		GND					F27								
		GND					F5								



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		GND					F7								
		GND					G24								
		GND					G3								
		GND					G4								
		GND					H1								
		GND					H11								
		GND					H2								
		GND					H5								
		GND					J18								
		GND					J28								
		GND					J8								
		GND					J4								
		GND					J8								
		GND					K1								
		GND					K10								
		GND					K15								
		GND					K2								
		GND					K20								
		GND					K25								
		GND					K5								
		GND					L11								
		GND					L13								
		GND					L15								
		GND					L17								
		GND					L19								
		GND					L22								
		GND					L3								
		GND					L4								
		GND					L6								
		GND					M1								
		GND					M10								
		GND					M12								
		GND					M14								
		GND					M16								
		GND					M18								
		GND					M5								
		GND					M20								
		GND					M29								
		GND					M5								
		GND					M7								
		GND					M8								
		GND					M11								
		GND					M13								
		GND					M15								
		GND					M17								
		GND					M19								
		GND					M25								
		GND					M3								
		GND					M4								
		GND					M6								
		GND					M8								
		GND					M9								
		GND					P1								
		GND					P10								
		GND					P12								
		GND					P14								
		GND					P16								
		GND					P18								
		GND					P2								
		GND					P20								
		GND					P5								
		GND					P7								
		GND					R11								
		GND					R13								
		GND					R15								
		GND					R17								
		GND					R3								
		GND					R30								
		GND					R4								
		GND					R6								
		GND					R8								
		GND					R9								
		GND					T1								
		GND					T10								
		GND					T12								
		GND					T14								
		GND					T15								
		GND					T16								
		GND					T2								
		GND					T20								
		GND					T27								
		GND					T5								
		GND					T7								
		GND					U11								
		GND					U13								
		GND					U15								
		GND					U17								
		GND					U24								
		GND					U29								
		GND					U3								
		GND					U4								
		GND					U5								
		GND					U9								
		GND					V1								
		GND					V10								
		GND					V12								
		GND					V14								
		GND					V19								
		GND					V2								
		GND					V21								
		GND					V5								
		GND					V7								
		GND					W11								
		GND					W13								
		GND					W18								
		GND					W28								
		GND					W3								
		GND					W4								
		GND					W6								
		GND					W9								
		GND					Y1								
		GND					Y10								
		GND					Y12								
		GND					Y14								
		GND					Y15								
		GND					Y2								
		GND					Y20								
		GND					Y25								
		GND					Y30								
		GND					Y5								
		GND					Y7								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F996	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 /3/	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0	
		GND					Y8									
		GND					U22									
		GND					T18									
		VCC					M11									
		VCC					M13									
		VCC					M9									
		VCC					N10									
		VCC					N12									
		VCC					N14									
		VCC					P11									
		VCC					P13									
		VCC					R10									
		VCC					R12									
		VCC					R14									
		VCC					T11									
		VCC					T13									
		VCC					U10									
		VCC					U12									
		VCC					U14									
		VCC					V11									
		VCC					V13									
		VCC					V15									
		VCC					W10									
		VCC					W12									
		VCC					W14									
		VCC					Y11									
		VCC					Y13									
		VCC					Y9									
		VCC					U21									
		DNU					F1									
		DNU					G2									
		DNU					AA7									
		DNU					AD15									
		DNU					E26									
		DNU					J18									
		VCCP3M					AB10									
		VCCP3M					AA23									
		VCCP3M					J11									
		VCC3A					H8									
		VCC3A					AC11									
		VCC3A					AD8									
		VCC3A					AF7									
		VCC3A					AG4									
		VCC3B					AB14									
		VCC3B					AD13									
		VCC3B					AE15									
		VCC3B					AJ13									
		VCC3B					AJ8									
		VCC3B					AK10									
		VCC3A					AA17									
		VCC3A					AC21									
		VCC3A					AD18									
		VCC3A					AE25									
		VCC3A					AF22									
		VCC3A					AG19									
		VCC3A					AH16									
		VCC3A					AI26									
		VCC3A					AJ23									
		VCC3A					AK20									
		VCC3A					AB24									
		VCC3A					AD28									
		VCC3A					AG29									
		VCC3A					W23									
		VCC3B					AA27									
		VCC3B					AE30									
		VCC3B HPS					Q28									
		VCC3B HPS					Q29									
		VCC3B HPS					H06									
		VCC3B HPS					K24									
		VCC3B HPS					K30									
		VCC3B HPS					L27									
		VCC3B HPS					M24									
		VCC3B HPS					NC1									
		VCC3B HPS					P23									
		VCC3B HPS					P28									
		VCC3B HPS					R26									
		VCC3B HPS					T22									
		VCC3B HPS					U19									
		VCC3B HPS					V26									
		VCC3A HPS					F22									
		VCC3A HPS					H21									
		VCC3A HPS					E20									
		VCC3A HPS					G19									
		VCC3A HPS					D18									
		VCC3A HPS					E16									
		VCC3A HPS					H16									
		VCC3A					A7									
		VCC3A					B4									
		VCC3A					G11									
		VCC3A					D8									
		VCC3A					E5									
		VCC3A					F12									
		VCC3A					G14									
		VCC3A					G9									
		VCC3A					H6									
		VCC3A					J13									
		VCCP3A					AA10									
		VCCP3A					AC10									
		VCCP3B4A					AB18									
		VCCP3B4A					AB20									
		VCCP3B4A					AC13									
		VCCP3B4A					AC15									
		VCCP3B4A					AC17									
		VCCP3B4A					AC19									
		VCCP3B4A					AD16									
		VCCP3B4A					AE21									
		VCCP3A					V22									
		VCCP3A					V24									
		VCCP3B					U23									
		VCCP3B6B HPS					M21									
		VCCP3B6B HPS					N22									
		VCCP3B6B HPS					P21									
		VCCP3B6B HPS					R20									
		VCCP3B6B HPS					R23									
		VCCP3A HPS					K19									
		VCCP3B HPS					K18									
		VCCP3C HPS					J17									
		VCCP3D HPS					K16									
		VCCP3E					K11									
		VCCP3E					K13									
		VCCP3E					L10									



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F996	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 /3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCCPDBA					L12								
		VCCPDBA					L14								
3A	VREFB3AN0	VREFB3AN0					AD6								
3B	VREFB3AN0	VREFB3AN0					AJ15								
4A	VREFB4AN0	VREFB4AN0					AK17								
5A	VREFB5AN0	VREFB5AN0					AC24								
5B	VREFB5AN0	VREFB5AN0					AK29								
		VREFB7A7B1	VREFB7A7B1C7DNO	HPS			E22								
8A	VREFB8AN0	VREFB8AN0					B10								
		VCOH GXBL					AB6								
		VCOH GXBL					P6								
		VCOH GXBL					V6								
		VCCL GXBL					L5								
		VCCL GXBL					R5								
		VCCL GXBL					W5								
		VCCRSCLK	HPS				J20								
		RREF_TL					C1								
		VCCA PLL					N7								
		VCCA PLL					R7								
		VCCA PLL					V8								
		VCCA PLL					AA8								
		VCCA PLL					K9								
		VCCA PLL					Y22								
		VCC AUX					AB11								
		VCC AUX					AB16								
		VCC AUX					AD22								
		VCC AUX					H10								
		VCC AUX					J16								
		VCC AUX SHARED					J21								
		VCC GXBL					AA5								
		VCC GXBL					M6								
		VCC GXBL					N6								
		VCC GXBL					T6								
		VCC GXBL					U5								
		VCC GXBL					V6								
		VCC HPS					L21								
		VCC HPS					U18								
		VCC HPS					L16								
		VCC HPS					L18								
		VCC HPS					L20								
		VCC HPS					M15								
		VCC HPS					N20								
		VCC HPS					P15								
		VCC HPS					P17								
		VCC HPS					P19								
		VCC HPS					R16								
		VCC HPS					T17								
		VCC HPS					T19								
		VCC HPS					U16								

Notes:  
 (1) For more information about pin definitions and pin connection guidelines, refer to the [Cyclone V Device Family Pin Connection Guidelines](#).  
 (2) HPS\_DDR pins are for memory interface only. For the dedicated pin function corresponding with the respective memory interfaces, refer to the HMC columns.  
 (3) RESET pin is only applicable for DDR3 device.





Pin Information for the Cyclone® V 5CSTFD6 Device  
Version 1.4

Version Number	Date	Changes Made
1.0	10/18/2012	Initial release.
1.1	1/17/2013	A pin that was marked as VCC_HPS has been corrected to VCCRSTCLK_HPS
1.2	3/25/2013	Updated the following pin names: - Changed SDMMC_CLK_IN to SDMMC_FB_CLK_IN - Changed SDMMC_CLK to SDMMC_CCLK_OUT
1.3	9/30/2014	- Remove corresponding bank number from VCCRSTCLK_HPS pin. - Changed HMC Pin Assignment for DDR3 to HMC Pin Assignment for DDR3/DDR2. - Added note 3.
1.4	12/23/2016	-Renamed SDMMC_FB_CLK_IN to HPS_GPIO44.