









Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U02	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0	
		GND					AC1									
		GND					AC2									
		GND					AC3									
		GND					AD14									
		GND					AD22									
		GND					AD25									
		GND					AD3									
		GND					AD6									
		GND					AD8									
		GND					AE1									
		GND					AE16									
		GND					AE18									
		GND					AE2									
		GND					AE3									
		GND					AF24									
		GND					AF3									
		GND					AG1									
		GND					AG17									
		GND					AG2									
		GND					AG27									
		GND					AG3									
		GND					AG7									
		GND					AH10									
		GND					AH20									
		GND					B15									
		GND					B17									
		GND					B20									
		GND					B22									
		GND					B25									
		GND					B27									
		GND					B3									
		GND					B5									
		GND					BF									
		GND					C1									
		GND					C11									
		GND					C2									
		GND					C3									
		GND					D10									
		GND					D13									
		GND					D16									
		GND					D3									
		GND					E1									
		GND					E19									
		GND					E2									
		GND					E22									
		GND					E24									
		GND					E27									
		GND					E3									
		GND					E9									
		GND					F3									
		GND					G1									
		GND					G2									
		GND					G3									
		GND					H11									
		GND					H15									
		GND					H18									
		GND					H20									
		GND					H24									
		GND					H27									
		GND					H5									
		GND					H6									
		GND					H8									
		GND					H6									
		GND					J1									
		GND					J2									
		GND					J3									
		GND					J5									
		GND					J9									
		GND					K11									
		GND					K12									
		GND					K14									
		GND					K16									
		GND					K20									
		GND					K3									
		GND					K5									
		GND					K8									
		GND					L1									
		GND					L10									
		GND					L13									
		GND					L15									
		GND					L17									
		GND					L19									
		GND					L2									
		GND					L24									
		GND					L27									
		GND					L3									
		GND					L5									
		GND					L8									
		GND					L9									
		GND					M10									
		GND					M11									
		GND					M14									
		GND					M16									
		GND					M20									
		GND					M3									
		GND					M8									
		GND					M1									
		GND					M13									
		GND					M15									
		GND					M17									
		GND					M19									
		GND					N2									
		GND					N3									
		GND					N4									
		GND					P10									
		GND					P12									
		GND					P16									
		GND					P18									
		GND					P20									
		GND					P25									
		GND					P3									
		GND					P6									
		GND					P9									
		GND					R1									
		GND					R11									
		GND					R13									
		GND					R15									
		GND					R5									
		GND					R8									
		GND					T10									
		GND					T14									
		GND					T3									
		GND					U1									
		GND					U12									



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					I17								
		GND					I2								
		GND					U20								
		GND					U24								
		GND					U27								
		GND					U8								
		GND					U8								
		GND					V14								
		GND					V3								
		GND					V8								
		GND					V9								
		GND					W1								
		GND					W16								
		GND					W18								
		GND					W2								
		GND					W3								
		GND					W4								
		GND					Y12								
		GND					Y14								
		GND					Y20								
		GND					Y26								
		GND					Y3								
		GND					Z26								
		GND					Z27								
		VCC					J11								
		VCC					K13								
		VCC					K16								
		VCC					L11								
		VCC					L12								
		VCC					L14								
		VCC					M12								
		VCC					M13								
		VCC					M16								
		VCC					M8								
		VCC					N10								
		VCC					N11								
		VCC					N12								
		VCC					N14								
		VCC					N8								
		VCC					P11								
		VCC					P13								
		VCC					P14								
		VCC					P16								
		VCC					R10								
		VCC					R12								
		VCC					R14								
		VCC					R9								
		VCC					T13								
		VCC					T9								
		VCC					L4								
		VCC					T4								
		VCC					M5								
		VCC					M5								
		VCC					R5								
		VCC					T5								
		VCC					U26								
		DNU					A2								
		DNU					B2								
		DNU					D1								
		DNU					D2								
		DNU					H1								
		DNU					H2								
		DNU					M1								
		DNU					M2								
		DNU					T1								
		DNU					T2								
		DNU					Y1								
		DNU					Y2								
		DNU					AD1								
		DNU					AD2								
		DNU					U8								
		DNU					AE14								
		DNU					D23								
		DNU					E12								
		DNU					V10								
		VCCP6M					AD24								
		VCCP6M					H18								
		VCCP6M					D7								
		VCCBAT					AA5								
		VCCIO3A					H5								
		VCCIO3A					AA12								
		VCCIO3B					AE10								
		VCCIO3B					AE13								
		VCCIO3B					AG4								
		VCCIO4A					AA16								
		VCCIO4A					AE21								
		VCCIO4A					AF14								
		VCCIO4A					AF19								
		VCCIO4A					AG13								
		VCCIO4A					AG22								
		VCCIO4A					AH15								
		VCCIO4A					AK25								
		VCCIO4A					W13								
		VCCIO5A					AC25								
		VCCIO5A					W17								
		VCCIO5B					W25								
		VCCIO5B					C25								
		VCCIO5A HPS					C27								
		VCCIO5A HPS					F27								
		VCCIO5A HPS					G24								
		VCCIO5A HPS					H21								
		VCCIO5A HPS					H26								
		VCCIO5A HPS					L26								
		VCCIO5A HPS					M21								
		VCCIO5B HPS					AD27								
		VCCIO5B HPS					P27								
		VCCIO5B HPS					T23								
		VCCIO5B HPS					T25								
		VCCIO5B HPS					U16								
		VCCIO5B HPS					W27								
		VCCIO7A HPS					C20								
		VCCIO7A HPS					D18								
		VCCIO7B HPS					B13								
		VCCIO7B HPS					H14								
		VCCIO7D HPS					B10								
		VCCIO7D HPS					D8								
		VCCIO7D HPS					S5								
		VCCIO8A					AA10								
		VCCPD3A					AA14								
		VCCPD3A					AD13								
		VCCPD3A					AD16								
		VCCPD3A					AD18								
		VCCPD3A					AD21								
		VCCPD3A					AD2								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		WCCPD5A					Y21								
		WCCPD5B					W19								
		WCCPD6MB_HPS					K21								
		WCCPD6B_HPS					K24								
		WCCPD6MB_HPS					M24								
		WCCPD6B_HPS					P21								
		WCCPD6B_HPS					P24								
		WCCPD7A_HPS					E21								
		WCCPD7B_HPS					E17								
		WCCPD7C_HPS					E14								
		WCCPD7D_HPS					E13								
		WCCPD8A					E16								
		WCCPD8B					A25								
3A	VREFB3AND	VREFB3AND					AF12								
3B	VREFB3BND	VREFB3BND					AF16								
4A	VREFB4AND	VREFB4AND					AC06								
4B	VREFB4BND	VREFB4BND					AA25								
5A	VREFB5AND	VREFB5AND					D19								
5B	VREFB5BND	VREFB5BND					D9								
8A	VREFB8AND	VREFB8AND					F29								
		WCCRSTCLK_HPS					B1								
		RREF_TL					P4								
		WCCA_FPLL					Q4								
		WCCA_FPLL					U5								
		WCCA_FPLL					JA								
		WCCA_FPLL					AA21								
		WCCA_FPLL					M4								
		WCCA_FPLL					R4								
		WCC_AUX					AC21								
		WCC_AUX					AC8								
		WCC_AUX					AD15								
		WCC_AUX					E15								
		WCC_AUX					F8								
		WCC_AUX_SHARED					F21								
		WCCRLL_HPS					H23								
		WCC_HPS					U21								
		WCC_HPS					K17								
		WCC_HPS					L16								
		WCC_HPS					L18								
		WCC_HPS					M17								
		WCC_HPS					M19								
		WCC_HPS					N16								
		WCC_HPS					N18								
		WCC_HPS					P17								
		WCC_HPS					P19								

Notes:  
 (1) For more information about pin definitions and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.  
 (2) HPS DDR pins are for memory interface only. For the dedicated pin function corresponding with the respective memory interfaces, refer to the HMC columns.  
 (3) RESET pin is only applicable for DDR3 device.









Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR0/DDR2 (3)	HMC Pin Assignment for DDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
6E	VREFB0N0	HPS_DDR					R29			HPS_DQ_23	HPS_DQ_23				
6E	VREFB0N0	HPS_DDR					P27			HPS_DQ_21	HPS_DQ_21				
6E	VREFB0N0	HPS_DDR					N27			HPS_DQ_22	HPS_DQ_22				
6E	VREFB0N0	HPS_DDR					P26			HPS_DQ_20	HPS_DQ_20				
6E	VREFB0N0	HPS_GPI6					P29								
6E	VREFB0N0	HPS_DDR					R19			HPS_DQS_2	HPS_DQS_2				
6E	VREFB0N0	HPS_DDR					P30			HPS_RESET#	HPS_RESET#				
6E	VREFB0N0	HPS_DDR					R18			HPS_DQS#_2	HPS_DQS#_2				
6E	VREFB0N0	HPS_DDR					N28			HPS_DQ_19	HPS_DQ_19				
6E	VREFB0N0	HPS_D06					T26			HPS_DQ_17	HPS_DQ_17				
6E	VREFB0N0	HPS_DDR					N29			HPS_DQ_18	HPS_DQ_18				
6E	VREFB0N0	HPS_DDR					L26			HPS_DQ_16	HPS_DQ_16				
6E	VREFB0N0	HPS_GPI4					N30								
6A	VREFB0N0	HPS_GPI3					M22								
6A	VREFB0N0	HPS_DDR					M28			HPS_DM_1	HPS_DM_1				
6A	VREFB0N0	HPS_DDR					N23								
6A	VREFB0N0	HPS_DDR					M30			HPS_DQ_15	HPS_DQ_15				
6A	VREFB0N0	HPS_DDR					M27			HPS_DQ_13	HPS_DQ_13				
6A	VREFB0N0	HPS_D06					L28			HPS_DQ_14	HPS_DQ_14				
6A	VREFB0N0	HPS_DDR					M26			HPS_DQ_12	HPS_DQ_12				
6A	VREFB0N0	HPS_DDR					L25			HPS_CKE_0	HPS_CKE_0				
6A	VREFB0N0	HPS_DDR					N25			HPS_DQS_1	HPS_DQS_1				
6A	VREFB0N0	HPS_DDR					L30			HPS_CKE_1	HPS_CKE_1				
6A	VREFB0N0	HPS_DDR					N24			HPS_DQS#_1	HPS_DQS#_1				
6A	VREFB0N0	HPS_DDR					K27			HPS_DQ_11	HPS_DQ_11				
6A	VREFB0N0	HPS_DDR					L26			HPS_DQ_9	HPS_DQ_9				
6A	VREFB0N0	HPS_D06					K28			HPS_DQ_10	HPS_DQ_10				
6A	VREFB0N0	HPS_DDR					K26			HPS_DQ_8	HPS_DQ_8				
6A	VREFB0N0	HPS_GPI1					J26								
6A	VREFB0N0	HPS_GPI0					M25								
6A	VREFB0N0	HPS_DDR					K29			HPS_DM_0	HPS_DM_0				
6A	VREFB0N0	HPS_DDR					J29			HPS_DQ_7	HPS_DQ_7				
6A	VREFB0N0	HPS_DDR					L28			HPS_DQ_5	HPS_DQ_5				
6A	VREFB0N0	HPS_D06					J30			HPS_DQ_6	HPS_DQ_6				
6A	VREFB0N0	HPS_DDR					L25			HPS_DQ_4	HPS_DQ_4				
6A	VREFB0N0	HPS_DDR					K28			HPS_ODT_1	HPS_ODT_1				
6A	VREFB0N0	HPS_D06					N18			HPS_DQS_0	HPS_DQS_0				
6A	VREFB0N0	HPS_DDR					H28			HPS_ODT_0	HPS_ODT_0				
6A	VREFB0N0	HPS_D06					M19			HPS_DQS#_0	HPS_DQS#_0				
6A	VREFB0N0	HPS_D06					G28			HPS_DQ_3	HPS_DQ_3				
6A	VREFB0N0	HPS_DDR					K22			HPS_DQ_1	HPS_DQ_1				
6A	VREFB0N0	HPS_D06					H28			HPS_DQ_2	HPS_DQ_2				
6A	VREFB0N0	HPS_DDR					K23			HPS_DQ_0	HPS_DQ_0				
6A	VREFB0N0	VREFB0N0					G27								
6A	VREFB0N0	HPS_DDR					F26			HPS_A_0	HPS_CA_0				
6A	VREFB0N0	HPS_DDR					G30			HPS_A_1	HPS_CA_1				
6A	VREFB0N0	HPS_DDR					J25			HPS_A_4	HPS_CA_4				
6A	VREFB0N0	HPS_DDR					F28			HPS_A_2	HPS_CA_2				
6A	VREFB0N0	HPS_DDR					J27			HPS_A_5	HPS_CA_5				
6A	VREFB0N0	HPS_DDR					F30			HPS_A_3	HPS_CA_3				
6A	VREFB0N0	HPS_D06					H29			HPS_CK	HPS_CK				
6A	VREFB0N0	HPS_DDR					F29			HPS_A_6	HPS_CA_6				
6A	VREFB0N0	HPS_D06					L23			HPS_CK#	HPS_CK#				
6A	VREFB0N0	HPS_D06					E28			HPS_A_7	HPS_CA_7				
6A	VREFB0N0	HPS_D06					J24			HPS_BA_1					
6A	VREFB0N0	HPS_D06					E29			HPS_BA_0					
6A	VREFB0N0	HPS_D06					J23			HPS_BA_2					
6A	VREFB0N0	HPS_DDR					E27			HPS_CAS#					
6A	VREFB0N0	HPS_D06					D30			HPS_MASK					
6A	VREFB0N0	HPS_D06					K27			HPS_A_8	HPS_CA_8				
6A	VREFB0N0	HPS_D06					D29			HPS_A_10					
6A	VREFB0N0	HPS_D06					G26			HPS_A_9	HPS_CA_9				
6A	VREFB0N0	HPS_D06					K29			HPS_A_11					
6A	VREFB0N0	HPS_D06					H24			HPS_CSE_0	HPS_CSE_0				
6A	VREFB0N0	HPS_D06					B30			HPS_A_12					
6A	VREFB0N0	HPS_D06					K21			HPS_CSE_1	HPS_CSE_1				
6A	VREFB0N0	HPS_D06					C29			HPS_A_13					
6A	VREFB0N0	HPS_D06					H25			HPS_A_14					
6A	VREFB0N0	HPS_D06					C28			HPS_VREF					
6A	VREFB0N0	HPS_D06					G25			HPS_A_15					
6A	VREFB0N0	HPS_R2Q_0					D27								
7		GND					J22								
7A		GND					D26								
7A		HPS_HRT					C27								
7A		HPS_HPOR					F23								
7A		HPS_T0D					B28								
7A		KC0ST0CLK_LHS					G28								
7A		HPS_TMS					A29								
7A		HPS_TCK					H22								
7A		HPS_TRST					A28								
7A		HPS_TDI					B27								
7A		GND					A26								
7A		HPS_PORSEL					F24								
7A		HPS_CLK1					G25								
7A		HPS_CLK2					F25								
7A	VREFB7A7B7C7D0	HPS_TRACE_CLK					B26					TRACE_CLK			HPS_GPI08
7A	VREFB7A7B7C7D0	HPS_TRACE_D0					B25					TRACE_D0	SPIS0_CLK	UART0_RX	HPS_GPI09
7A	VREFB7A7B7C7D0	HPS_TRACE_D1					C25					TRACE_D1	SPIS0_MOSI	UART0_TX	HPS_GPI10
7A	VREFB7A7B7C7D0	HPS_TRACE_D2					A25					TRACE_D2	SPIS0_MISO	I2C1_SDA	HPS_GPI11
7A	VREFB7A7B7C7D0	HPS_TRACE_D3					H23					TRACE_D3	SPIS0_SS0	I2C1_SCL	HPS_GPI12
7A	VREFB7A7B7C7D0	HPS_TRACE_D4					A24					TRACE_D4	SPIS1_CLK	CAN1_RX	HPS_GPI13
7A	VREFB7A7B7C7D0	HPS_TRACE_D5					G21					TRACE_D5	SPIS1_MOSI	CAN1_TX	HPS_GPI14
7A	VREFB7A7B7C7D0	HPS_TRACE_D6					C24					TRACE_D6	SPIS1_SS0	I2C0_SDA	HPS_GPI15
7A	VREFB7A7B7C7D0	HPS_TRACE_D7					E23					TRACE_D7	SPIS1_MISO	I2C0_SCL	HPS_GPI16
7A	VREFB7A7B7C7D0	HPS_SPIW0_CLK					M21					SPISW0_CLK	I2C1_SDA	UART1_CTS	HPS_GPI17
7A	VREFB7A7B7C7D0	HPS_SPIW0_MOSI					C22					SPISW0_MOSI	I2C1_SCL	UART1_RTS	HPS_GPI18
7A	VREFB7A7B7C7D0	HPS_SPIW0_MISO					B23					SPISW0_MISO	CAN1_RX	UART1_CTS	HPS_GPI19
7A	VREFB7A7B7C7D0	HPS_SPIW0_SS0/BOOTSEL0					H20					SPISW0_SS0	CAN1_TX	UART1_RTS	HPS_GPI20
7A	VREFB7A7B7C7D0	HPS_UART0_RX					B22					UART0_RX	CAN0_RX	SPIM0_SS1	HPS_GPI01
7A	VREFB7A7B7C7D0	HPS_UART0_TX_CLKSEL1					G22					UART0_TX	CAN0_TX	SPIM1_SS1	HPS_GPI02
7A	VREFB7A7B7C7D0	HPS_I2C0_SDA					E23					I2C0_SDA	UART1_RX	SPIM1_CLK	HPS_GPI03
7A	VREFB7A7B7C7D0	HPS_I2C0_SCL					D22					I2C0_SCL	UART1_TX	SPIM1_MOSI	HPS_GPI04
7A	VREFB7A7B7C7D0	HPS_CAND_RX					E24					CAND_RX	UART1_RX	SPIM1_MISO	HPS_GPI05
7A	VREFB7A7B7C7D0	HPS_CAND_TX_CLKSEL0					D24					CAND_TX	UART0_TX	SPIM1_SS0	HPS_GPI06
7A	VREFB7A7B7C7D0	HPS_NAND_ALE					H19					NAND_ALE	RGMI1_TX_CLK		HPS_GPI14
7A	VREFB7A7B7C7D0	HPS_NAND_CE					F20					NAND_CE	RGMI1_TXD0	USB1_D0	HPS_GPI15
7A	VREFB7A7B7C7D0	HPS_NAND_CLE					J19					NAND_CLE	RGMI1_TXD1	USB1_D1	HPS_GPI16
7A	VREFB7A7B7C7D0	HPS_NAND_RE					F21					NAND_RE	RGMI1_TXD2	USB1_D2	HPS_GPI17
7A	VREFB7A7B7C7D0	HPS_NAND_RB					F19					NAND_RB	RGMI1_TXD3	USB1_D3	HPS_GPI18
7A	VREFB7A7B7C7D0	HPS_NAND_DQ0					K21					NAND_DQ0	RGMI1_R0D0		HPS_GPI19
7A	VREFB7A7B7C7D0	HPS_NAND_DQ1					E21					NAND_DQ1	RGMI1_M0D0	I2C1_SDA	HPS_GPI20
7A	VREFB7A7B7C7D0	HPS_NAND_DQ2					B21					NAND_DQ2	RGMI1_M0C	I2C1_SCL	HPS_GPI21
7A	VREFB7A7B7C7D0	HPS_NAND_DQ3					K21					NAND_DQ3	RGMI1_RX_CTL	USB1_D4	HPS_GPI22
7A	VREFB7A7B7C7D0	HPS_NAND_DQ4					A20					NAND_DQ4	RGMI1_TX_CTL	USB1_D5	HPS_GPI23
7A	VREFB7A7B7C7D0	HPS_NAND_DQ5					G20					NAND_DQ5	RGMI1_RX_CLK	USB1_D6	HPS_GPI24
7A	VREFB7A7B7C7D0	HPS_NAND_DQ6					N20					NAND_DQ6	RGMI1_R0D1		HPS_GPI25
7A	VREFB7A7B7C7D0	HPS_NAND_DQ7					B19					NAND_DQ7	RGMI1_R0D2		HPS_GPI26
7A	VREFB7A7B7C7D0	HPS_NAND_WP					D21					NAND_WP	RGMI1_R0D3	OSPI_SS2	HPS_GPI27
7A	VREFB7A7B7C7D0	HPS_NAND_WE/BOOTSEL2					D21					NAND_WE	OSPI_SS1		HPS_GPI28
7A	VREFB7A7B7C7D0	HPS_GSPI_I2C0					C20					OSPI_I2C0	USB1_CLK		HPS_GPI29
7A	VREFB7A7B7C7D0	HPS_GSPI_I01					H18					OSPI_I01	USB1_STP		HPS_GPI30
7A	VREFB7A7B7C7D0	HPS_GSPI_I02					A19					OSPI_I02	USB1_DIR		HPS_G



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated TriX Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DQS/ADDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
							C19								
							F18								
							B17								
							G18								
							C17								
							H17								
							C18								
							G17								
							E18								
							E17								
							A16								
							D17								
							B16								
							F16								
							E16								
							G16								
							D16								
							D14								
							A15								
							C14								
							RGM0_RXD0								
							RGM0_TXD0								
							RGM0_RXD1								
							RGM0_TXD1								
							RGM0_TXD2								
							RGM0_RXD2								
							RGM0_TXD2								
							RGM0_RXD3								
							RGM0_TXD3								
							RGM0_RXD0								
							RGM0_RXD1								
							RGM0_RXD2								
							RGM0_RXD3								
							RGM0_RXD4								
							RGM0_RXD5								
							RGM0_RXD6								
							RGM0_RXD7								
							RGM0_RXD8								
							RGM0_RXD9								
							RGM0_RXD10								
							RGM0_RXD11								
							RGM0_RXD12								
							RGM0_RXD13								
							RGM0_RXD14								
							RGM0_RXD15								
							RGM0_RXD16								
							RGM0_RXD17								
							RGM0_RXD18								
							RGM0_RXD19								
							RGM0_RXD20								
							RGM0_RXD21								
							RGM0_RXD22								
							RGM0_RXD23								
							RGM0_RXD24								
							RGM0_RXD25								
							RGM0_RXD26								
							RGM0_RXD27								
							RGM0_RXD28								
							RGM0_RXD29								
							RGM0_RXD30								
							RGM0_RXD31								
							RGM0_RXD32								
							RGM0_RXD33								
							RGM0_RXD34								
							RGM0_RXD35								
							RGM0_RXD36								
							RGM0_RXD37								
							RGM0_RXD38								
							RGM0_RXD39								
							RGM0_RXD40								
							RGM0_RXD41								
							RGM0_RXD42								
							RGM0_RXD43								
							RGM0_RXD44								
							RGM0_RXD45								
							RGM0_RXD46								
							RGM0_RXD47								
							RGM0_RXD48								
							RGM0_RXD49								
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							RGM0_RXD51								
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							RGM0_RXD66								
							RGM0_RXD67								
							RGM0_RXD68								
							RGM0_RXD69								
							RGM0_RXD70								
							RGM0_RXD71								
							RGM0_RXD72								
							RGM0_RXD73								
							RGM0_RXD74								
							RGM0_RXD75								
							RGM0_RXD76								
							RGM0_RXD77								
							RGM0_RXD78								
							RGM0_RXD79								
							RGM0_RXD80								
							RGM0_RXD81								
							RGM0_RXD82								
							RGM0_RXD83								
							RGM0_RXD84								
							RGM0_RXD85								
							RGM0_RXD86								
							RGM0_RXD87								
							RGM0_RXD88								
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							RGM0_RXD102								
							RGM0_RXD103								
							RGM0_RXD104								
							RGM0_RXD105								
							RGM0_RXD106								
							RGM0_RXD107								
							RGM0_RXD108								
							RGM0_RXD109								
							RGM0_RXD110								
							RGM0_RXD111								
							RGM0_RXD112								
							RGM0_RXD113								
							RGM0_RXD114								
							RGM0_RXD115								
							RGM0_RXD116								
							RGM0_RXD117								
							RGM0_RXD118								
							RGM0_RXD119								
							RGM0_RXD120								
							RGM0_RXD121								
							RGM0_RXD122								
							RGM0_RXD123								
							RGM0_RXD124								
							RGM0_RXD125								
							RGM0_RXD126								
							RGM0_RXD127								
							RGM0_RXD128								
							RGM0_RXD129								
							RGM0_RXD1								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					T8								
		GND					T9								
		GND					R2								
		GND					R1								
		GND					U2								
		GND					U1								
		GND					W2								
		GND					W1								
		GND					AA2								
		GND					AA1								
		GND					AC2								
		GND					AC1								
		GND					AE2								
		GND					AE1								
		GND					WB								
		GND					W1								
		GND					A12								
		GND					A17								
		GND					AS								
		GND					AS2								
		GND					AG2								
		GND					AA11								
		GND					AA22								
		GND					AA3								
		GND					AA4								
		GND					AA5								
		GND					AA6								
		GND					AA8								
		GND					AB1								
		GND					AB19								
		GND					AB2								
		GND					AB29								
		GND					AB5								
		GND					AB7								
		GND					AC16								
		GND					AC26								
		GND					AC3								
		GND					AC4								
		GND					AC5								
		GND					AC8								
		GND					AD1								
		GND					AD2								
		GND					AD23								
		GND					AD5								
		GND					AE10								
		GND					AE20								
		GND					AE3								
		GND					AE4								
		GND					AF1								
		GND					AF12								
		GND					AF17								
		GND					AF2								
		GND					AF27								
		GND					AF3								
		GND					AG14								
		GND					AG24								
		GND					AG29								
		GND					AH1								
		GND					AH11								
		GND					AH21								
		GND					AH6								
		GND					AJ19								
		GND					AJ28								
		GND					AJ5								
		GND					AJ20								
		GND					AK15								
		GND					AK25								
		GND					AK5								
		GND					B14								
		GND					B19								
		GND					B24								
		GND					BC9								
		GND					BB								
		GND					C1								
		GND					C18								
		GND					C21								
		GND					C26								
		GND					C5								
		GND					D13								
		GND					D23								
		GND					D5								
		GND					E10								
		GND					E25								
		GND					E20								
		GND					F17								
		GND					F2								
		GND					F27								
		GND					F5								
		GND					F7								
		GND					G24								
		GND					G3								
		GND					G4								
		GND					H1								
		GND					H11								
		GND					H2								
		GND					H5								
		GND					J18								
		GND					J28								
		GND					L3								
		GND					J4								
		GND					J8								
		GND					K1								
		GND					K10								
		GND					K15								
		GND					K2								
		GND					K20								
		GND					K25								
		GND					K5								
		GND					L11								
		GND					L13								
		GND					L15								
		GND					L17								
		GND					L19								
		GND					L22								
		GND					L3								
		GND					L4								
		GND					L6								
		GND					M1								
		GND					M12								
		GND					M14								
		GND					M16								
		GND					M18								
		GND					M2								
		GND					M20								
		GND					M29								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					M6								
		GND					M7								
		GND					M8								
		GND					N11								
		GND					N13								
		GND					N15								
		GND					N17								
		GND					N19								
		GND					N26								
		GND					N5								
		GND					N4								
		GND					N6								
		GND					N8								
		GND					N9								
		GND					P1								
		GND					P10								
		GND					P12								
		GND					P16								
		GND					P16								
		GND					P18								
		GND					P2								
		GND					P20								
		GND					P5								
		GND					P7								
		GND					R11								
		GND					R13								
		GND					R16								
		GND					R17								
		GND					R3								
		GND					R20								
		GND					R4								
		GND					R6								
		GND					R8								
		GND					R9								
		GND					T1								
		GND					T10								
		GND					T12								
		GND					T14								
		GND					T15								
		GND					T16								
		GND					T2								
		GND					T20								
		GND					T27								
		GND					T9								
		GND					T7								
		GND					U11								
		GND					U13								
		GND					U15								
		GND					U17								
		GND					U24								
		GND					U29								
		GND					U3								
		GND					U4								
		GND					U6								
		GND					U8								
		GND					V1								
		GND					V10								
		GND					V12								
		GND					V14								
		GND					V19								
		GND					V2								
		GND					V21								
		GND					V5								
		GND					V7								
		GND					W11								
		GND					W13								
		GND					W18								
		GND					W28								
		GND					W3								
		GND					W4								
		GND					W6								
		GND					W9								
		GND					Y1								
		GND					Y10								
		GND					Y12								
		GND					Y14								
		GND					Y15								
		GND					Y2								
		GND					Y20								
		GND					Y25								
		GND					Y30								
		GND					Y5								
		GND					Y7								
		GND					Y8								
		GND					U22								
		GND					T18								
		VCC					M11								
		VCC					M13								
		VCC					M9								
		VCC					N10								
		VCC					N12								
		VCC					N14								
		VCC					P11								
		VCC					P13								
		VCC					R10								
		VCC					R12								
		VCC					R14								
		VCC					T11								
		VCC					T13								
		VCC					U10								
		VCC					U12								
		VCC					U14								
		VCC					V11								
		VCC					V13								
		VCC					V15								
		VCC					W10								
		VCC					W12								
		VCC					W14								
		VCC					Y11								
		VCC					Y13								
		VCC					Y3								
		VCC					L5								
		VCC					R5								
		VCC					W5								
		VCC					AAS								
		VCC					M6								
		VCC					N5								
		VCC					T6								
		VCC					U5								
		VCC					Y6								
		VCC					U21								
		BNU					F1								
		BNU					G2								
		BNU					H3								
		BNU					H4								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		DNU					K3								
		DNU					K4								
		DNU					M3								
		DNU					M4								
		DNU					P3								
		DNU					P4								
		DNU					T3								
		DNU					T4								
		DNU					V3								
		DNU					V4								
		DNU					V3								
		DNU					V4								
		DNU					AB3								
		DNU					AB4								
		DNU					AD3								
		DNU					AD4								
		DNU					AA7								
		DNU					AD15								
		DNU					EB6								
		DNU					J15								
		VCCPDM					AB10								
		VCCPGM					AA23								
		VCCPEM					J11								
		VCCSAT					HS								
		VCCIO3A					AC11								
		VCCIO3A					AB8								
		VCCIO3A					AF7								
		VCCIO3A					AG4								
		VCCIO3B					AB14								
		VCCIO3B					AD13								
		VCCIO3B					AE15								
		VCCIO3B					AJ13								
		VCCIO3B					AK8								
		VCCIO3B					AK10								
		VCCIO4A					AA17								
		VCCIO4A					AC21								
		VCCIO4A					AD18								
		VCCIO4A					AE25								
		VCCIO4A					AE32								
		VCCIO4A					AG19								
		VCCIO4A					AH16								
		VCCIO4A					AH28								
		VCCIO4A					AJ23								
		VCCIO4A					AK20								
		VCCIO5A					AB24								
		VCCIO5A					AD28								
		VCCIO5A					AG29								
		VCCIO5B					W23								
		VCCIO5B					AA27								
		VCCIO5B					AE30								
		VCCIO6A HPS					D28								
		VCCIO6A HPS					G29								
		VCCIO6A HPS					H26								
		VCCIO6A HPS					K24								
		VCCIO6A HPS					K30								
		VCCIO6A HPS					L27								
		VCCIO6A HPS					M24								
		VCCIO6A HPS					N21								
		VCCIO6B HPS					P23								
		VCCIO6B HPS					P26								
		VCCIO6B HPS					R25								
		VCCIO6B HPS					U22								
		VCCIO6B HPS					U19								
		VCCIO6B HPS					V26								
		VCCIO7A HPS					V22								
		VCCIO7A HPS					W21								
		VCCIO7B HPS					E20								
		VCCIO7B HPS					G19								
		VCCIO75 HPS					D18								
		VCCIO7D HPS					E15								
		VCCIO7D HPS					H16								
		VCCIO8A					A7								
		VCCIO8A					B4								
		VCCIO8A					C11								
		VCCIO8A					D8								
		VCCIO8A					E5								
		VCCIO8A					F13								
		VCCIO8A					G14								
		VCCIO8A					G9								
		VCCIO8A					H6								
		VCCIO8A					J13								
		VCCPD3A					AA10								
		VCCPD3A					AC10								
		VCCPD3B4A					AB18								
		VCCPD3B4A					AB20								
		VCCPD3B4A					AC13								
		VCCPD3B4A					AC15								
		VCCPD3B4A					AC17								
		VCCPD3B4A					AC19								
		VCCPD3B4A					AD16								
		VCCPD3B4A					AE21								
		VCCPD5A					V22								
		VCCPD5A					V24								
		VCCPD6B					U23								
		VCCPD6B HPS					M21								
		VCCPD6B HPS					N22								
		VCCPD6B HPS					P21								
		VCCPD6B HPS					R20								
		VCCPD6B HPS					R23								
		VCCPD7A HPS					K19								
		VCCPD7B HPS					K18								
		VCCPD7G HPS					J17								
		VCCPD7D HPS					K16								
		VCCPD8A					K11								
		VCCPD8A					K13								
		VCCPD8A					L10								
		VCCPD8A					L12								
		VCCPD8A					L14								
	3A	VREFB3A0	VREFB3A0				AN6								
	3B	VREFB3B0	VREFB3B0				AJ15								
	4A	VREFB4A0	VREFB4A0				AK17								
	5A	VREFB5A0	VREFB5A0				AK24								
	5B	VREFB5B0	VREFB5B0				AK29								
	8A	VREFB7A7B7C7D0	VREFB7A7B7C7D0	HPS			E22								
		VREFB8A0	VREFB8A0				B10								
		VREFB8B0	VREFB8B0				J20								
		RREF TL					G1								
		WCCA FPLL					N7								
		WCCA FPLL					R7								
		WCCA FPLL					V8								
		WCCA FPLL					W8								
		WCCA FPLL					X8								
		WCCA FPLL					Y8								
		WCCA FPLL					Y22								
		WCCA FPLL					AB6								
		WCCA FPLL					P5								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0	
		VCCA_FPLL					V8									
		VCC_AUX					AB11									
		VCC_AUX					AB16									
		VCC_AUX					AB22									
		VCC_AUX					H10									
		VCC_AUX					J16									
		VCC_AUX_SHARED					K21									
		VCCPLL_HPS					L21									
		VCC_HPS					U18									
		VCC_HPS					L16									
		VCC_HPS					L18									
		VCC_HPS					L20									
		VCC_HPS					M15									
		VCC_HPS					N20									
		VCC_HPS					P19									
		VCC_HPS					P17									
		VCC_HPS					P19									
		VCC_HPS					R16									
		VCC_HPS					T17									
		VCC_HPS					T19									
		VCC_HPS					U16									

Notes:

- (1) For more information about pin definitions and pin connection guidelines, refer to the [Cyclone V Device Family Pin Connection Guidelines](#).
- (2) HPS DDR pins are for memory interface only. For the dedicated pin function corresponding with the respective memory interfaces, refer to the HMC columns.
- (3) RESET pin is only applicable for DDR3 device.



Pin Information for the Cyclone® V 5CSEMA6 Device  
Version 1.4

Version Number	Date	Changes Made
1.0	10/18/2012	Initial release.
1.1	1/17/2013	A pin that was marked as VCC_HPS has been corrected to VCCRSTCLK_HPS
1.2	3/25/2013	Updated the following pin names: - Changed SDMMC_CLK_IN to SDMMC_FB_CLK_IN - Changed SDMMC_CLK to SDMMC_CCLK_OUT
1.3	9/30/2014	- Remove corresponding bank number from VCCRSTCLK_HPS pin. - Changed HMC Pin Assignment for DDR3 to HMC Pin Assignment for DDR3/DDR2. - Added note 3.
1.4	12/23/2016	-Renamed SDMMC_FB_CLK_IN to HPS_GPIO44.