



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated TriX Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DQB/ADDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
GB	L2	GXB TX L8n					H3								
GB	L2	GXB TX L8p					H4								
GB	L2	GXB RX L8p.GXB REFCLK L8p					J2								
GB	L2	GXB RX L8n.GXB REFCLK L8p					J1								
GB	L2	GXB TX L7n					K3								
GB	L2	GXB TX L7p					K4								
GB	L2	GXB RX L7p.GXB REFCLK L7p					L2								
GB	L2	GXB RX L7n.GXB REFCLK L7n					L1								
GB	L2	GXB TX L6n					M3								
GB	L2	GXB TX L6p					M4								
GB	L2	GXB RX L6p.GXB REFCLK L6p					N2								
GB	L2	GXB RX L6n.GXB REFCLK L6n					N1								
GB	L2	REFCLKL2p					P9								
GB	L2	REFCLKL2n					P8								
GB	L1	REFCLKL1p					T8								
GB	L1	REFCLKL1n					T9								
GB	L1	GXB TX L5n					P3								
GB	L1	GXB TX L5p					P4								
GB	L1	GXB RX L5p.GXB REFCLK L5p					R2								
GB	L1	GXB RX L5n.GXB REFCLK L5n					R1								
GB	L1	GXB TX L4n					T3								
GB	L1	GXB TX L4p					T4								
GB	L1	GXB RX L4p.GXB REFCLK L4p					U2								
GB	L1	GXB RX L4n.GXB REFCLK L4n					U1								
GB	L1	GXB TX L3n					V3								
GB	L1	GXB TX L3p					V4								
GB	L1	GXB RX L3p.GXB REFCLK L3p					W2								
GB	L1	GXB RX L3n.GXB REFCLK L3n					W1								
GB	L0	GXB TX L2n					Y3								
GB	L0	GXB TX L2p					Y4								
GB	L0	GXB RX L2p.GXB REFCLK L2p					AA2								
GB	L0	GXB RX L2n.GXB REFCLK L2n					AA1								
GB	L0	GXB TX L1n					AB3								
GB	L0	GXB TX L1p					AB4								
GB	L0	GXB RX L1p.GXB REFCLK L1p					AC2								
GB	L0	GXB RX L1n.GXB REFCLK L1n					AC1								
GB	L0	GXB TX L0n					AD3								
GB	L0	GXB TX L0p					AD4								
GB	L0	GXB RX L0p.GXB REFCLK L0p					AE2								
GB	L0	GXB RX L0n.GXB REFCLK L0n					AE1								
GB	L0	REFCLKL0p					WB								
GB	L0	REFCLKL0n					WB								
3A		TDO		TDO			AB9								
3A		nCS0		DATA4			AB8								
3A		TMS		TMS			AB7								
3A		AS_DATA3		DATA3			AC7								
3A		TCK		TCK			AC5								
3A		AS_DATA2		DATA2			AE8								
3A		TDI		TDI			UB								
3A		AS_DATA1		DATA1			AE5								
3A		CLK		CLK			U7								
3A		AS_DATA0/SSDO		DATA0			AE6								
3A	VREFBIAS0	ID		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	AE12	DD1B							
3A	VREFBIAS0	ID		DATA6	DIFFIO_TX_B0n	DIFFOUT_B0n	AE9	DD1B							
3A	VREFBIAS0	ID		DATA6	DIFFIO_RX_B1p	DIFFOUT_B1p	AD11	DD1B							
3A	VREFBIAS0	ID		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	AD9	DD1B							
3A	VREFBIAS0	ID		DATA9	DIFFIO_RX_B3n	DIFFOUT_B3n	AD10	DD2n1B							
3A	VREFBIAS0	ID		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	AF10	DD1B							
3A	VREFBIAS0	ID		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	AC9	DD2n1B							
3A	VREFBIAS0	ID		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	AE11	DD1B							
3A	VREFBIAS0	ID		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	AE7	DD1B							
3A	VREFBIAS0	ID		DATA13	DIFFIO_TX_B6p	DIFFOUT_B6p	AH4	DD1B							
3A	VREFBIAS0	ID		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	AD7	DD1B							
3A	VREFBIAS0	ID		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	AG3	DD1B							
3A	VREFBIAS0	ID		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	AF5	DD1B							
3A	VREFBIAS0	ID		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	AG8	DD1B							
3A	VREFBIAS0	ID		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	AF4	DD1B							
3A	VREFBIAS0	ID			DIFFIO_TX_B8p	DIFFOUT_B8p	AF9	DD1B							
3A	VREFBIAS0	ID			DIFFIO_TX_B9n	DIFFOUT_B9n	AG7	DD1B							
3A	VREFBIAS0	ID			DIFFIO_RX_B10n	DIFFOUT_B10n	AH2	DD2n							
3A	VREFBIAS0	ID			DIFFIO_TX_B9p	DIFFOUT_B9p	AF8	DD2n							
3A	VREFBIAS0	ID			DIFFIO_RX_B10p	DIFFOUT_B10p	AG1	DD2n							
3A	VREFBIAS0	ID			DIFFIO_RX_B11n	DIFFOUT_B11n	AH12	DD2n2B							
3A	VREFBIAS0	ID			DIFFIO_TX_B10p	DIFFOUT_B10p	AG6	DD2n							
3A	VREFBIAS0	ID			DIFFIO_RX_B11p	DIFFOUT_B11p	AA12	DD2n2B							
3A	VREFBIAS0	ID			DIFFIO_TX_B12p	DIFFOUT_B12p	AF6	DD2n							
3A	VREFBIAS0	ID			DIFFIO_TX_B12n	DIFFOUT_B12n	AH6	DD2n							
3A	VREFBIAS0	ID			DIFFIO_RX_B14n	DIFFOUT_B14n	AJ2	DD2n							
3A	VREFBIAS0	ID			DIFFIO_TX_B13p	DIFFOUT_B13p	AG5	DD2n							
3A	VREFBIAS0	ID			DIFFIO_RX_B14p	DIFFOUT_B14p	AJ1	DD2n							
3A	VREFBIAS0	ID			DIFFIO_RX_B15n	DIFFOUT_B15n	AD12	DD2n							
3A	VREFBIAS0	ID			DIFFIO_TX_B16p	DIFFOUT_B16p	AH3	DD2n							
3A	VREFBIAS0	ID			DIFFIO_RX_B15p	DIFFOUT_B15p	AG2	DD2n							
3B	VREFBIAS0	ID			DIFFIO_TX_B17n	DIFFOUT_B17n	AH9	DD2n							
3B	VREFBIAS0	ID			DIFFIO_RX_B18n	DIFFOUT_B18n	AG11	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_TX_B17p	DIFFOUT_B17p	AG10	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_RX_B18p	DIFFOUT_B18p	AF11	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_TX_B19n	DIFFOUT_B19n	AH3	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_RX_B19n	DIFFOUT_B19n	AG3	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_TX_B20n	DIFFOUT_B20n	AK3	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_RX_B19p	DIFFOUT_B19p	AA13	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_TX_B20p	DIFFOUT_B20p	AK2	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_TX_B21n	DIFFOUT_B21n	AK4	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_RX_B22n	DIFFOUT_B22n	AF13	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_TX_B21p	DIFFOUT_B21p	AJ4	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_RX_B22p	DIFFOUT_B22p	AE13	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_RX_B23n	DIFFOUT_B23n	AE14	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_TX_B24n	DIFFOUT_B24n	AK5	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_RX_B23p	DIFFOUT_B23p	AD14	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_TX_B24p	DIFFOUT_B24p	AJ5	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_RX_B25n	DIFFOUT_B25n	AJ7	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_RX_B25p	DIFFOUT_B25p	AG13	DD4n	DD1B	B_A_15					
3B	VREFBIAS0	ID			DIFFIO_TX_B25p	DIFFOUT_B25p	AJ6	DD4n	DD1B	B_WEP					
3B	VREFBIAS0	ID			DIFFIO_RX_B26p	DIFFOUT_B26p	AG12	DD4n	DD1B	B_A_14					
3B	VREFBIAS0	ID			DIFFIO_RX_B27n	DIFFOUT_B27n	AC14	DD5n4B	DD5n1B	B_CSz_1					
3B	VREFBIAS0	ID			DIFFIO_TX_B28n	DIFFOUT_B28n	AK8	DD4n	DD1B	B_A_13					
3B	VREFBIAS0	ID			DIFFIO_TX_B27p	DIFFOUT_B27p	AH15	DD5n4B	DD5n1B	B_CSz_0					
3B	VREFBIAS0	ID			DIFFIO_TX_B28p	DIFFOUT_B28p	AK7	DD5n4B	DD5n1B	B_A_12					
3B	VREFBIAS0	ID			DIFFIO_TX_B29n	DIFFOUT_B29n	AK9	DD4n	DD1B	B_A_11					
3B	VREFBIAS0	ID			DIFFIO_RX_B30n	DIFFOUT_B30n	AH4	DD4n	DD1B	B_A_9					
3B	VREFBIAS0	ID			DIFFIO_TX_B29p	DIFFOUT_B29p	AJ9	DD4n	DD1B	B_A_10					
3B	VREFBIAS0	ID			DIFFIO_RX_B30p	DIFFOUT_B30p	AH13	DD4n	DD1B	B_A_8					
3B	VREFBIAS0	ID		CLKIn.FPLL_BL_F8n	DIFFIO_RX_B31n	DIFFOUT_B31n	AF15	DD4n	DD1B	B_RAS#					
3B	VREFBIAS0	ID		CLKIn.FPLL_BL_F8p	DIFFIO_RX_B31p	DIFFOUT_B31p	AF14	DD4n	DD1B	B_RAS#					
3B	VREFBIAS0	ID			DIFFIO_TX_B32n	DIFFOUT_B32n	AH7	DD4n	DD1B	B_CSz#					
3B	VREFBIAS0	ID			DIFFIO_TX_B33n	DIFFOUT_B33n	AJ10	DD4n	DD1B	GND					
3B	VREFBIAS0	ID			DIFFIO_RX_B34n	DIFFOUT_B34n	AK11	DD5n	DD1B	B_BA_2					
3B	VREFBIAS0	ID			DIFFIO_TX_B33p	DIFFOUT_B33p	AH10	DD5n	DD1B	B_BA_0					
3B	VREFBIAS0	ID			DIFFIO_RX_B34p	DIFFOUT_B34p	AJ11	DD5n	DD1B	B_BA_1					
3B	VREFBIAS0	ID			DIFFIO_RX_B35n	DIFFOUT_B35n	AH8	DD5n4B	DD5n1B	B_CK#					
3B	VREFBIAS0	ID			DIFFIO_TX_B36n	DIFFOUT_B36n	AK13	DD5n	DD1B	B_CA_7					
3B	VREFBIAS0	ID			DIFFIO_RX_B35p	DIFFOUT_B35p	AA14	DD5n4B	DD5n1B	B_CK					
3B	VREFBIAS0	ID			DIFFIO_TX_B36p	DIFFOUT_B36p	AK12	DD5n	DD1B	B_CA_6					
3B	VREFBIAS0	ID			DIFFIO_TX_B37n	DIFFOUT_B37n	AJ12	DD5n	DD1B	B_CA_3					



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated TX/RX Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
3B	VREFB3BN0	ID			DIFFIO_RX B3bn	DIFFOUT_B3bn	AH15	DQ08							
3B	VREFB3BN0	ID	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUT1,FPLL_BL_FB		DIFFIO_TX B3bn	DIFFOUT_B3bn	AH12	DQ08							
3B	VREFB3BN0	ID			DIFFIO_RX B3bn	DIFFOUT_B3bn	AG15	DQ08		B.A.4					B.CA.4
3B	VREFB3BN0	ID	CLK1n		DIFFIO_TX B3bn	DIFFOUT_B3bn	V18	DQ08							B.CA.1
3B	VREFB3BN0	ID	CLK1p		DIFFIO_RX B3bn	DIFFOUT_B3bn	W15	DQ08							B.CA.1
3B	VREFB3BN0	ID	RZ0_0		DIFFIO_TX B4bn	DIFFOUT_B4bn	A14	DQ08		B.A.0					B.CA.0
4A	VREFB4AN0	ID			DIFFIO_RX B4bn	DIFFOUT_B4bn	AF18	DQ08			B.DQ.0				B.DQ.0
4A	VREFB4AN0	ID			DIFFIO_TX B4bn	DIFFOUT_B4bn	AG16	DQ08			B.DQ.2				B.DQ.2
4A	VREFB4AN0	ID			DIFFIO_RX B4bn	DIFFOUT_B4bn	AE17	DQ08			B.DQ.1				B.DQ.1
4A	VREFB4AN0	ID			DIFFIO_RX B4bn	DIFFOUT_B4bn	W16	DQ08			B.DQS0.0				B.DQS0.0
4A	VREFB4AN0	ID			DIFFIO_TX B4bn	DIFFOUT_B4bn	AF16	DQ08			B.DQ.3				B.DQ.3
4A	VREFB4AN0	ID			DIFFIO_RX B4bn	DIFFOUT_B4bn	V16	DQ08			B.DQS.0				B.DQS.0
4A	VREFB4AN0	ID			DIFFIO_TX B4bn	DIFFOUT_B4bn	AE16	DQ08			B.DQ0.0				B.DQ0.0
4A	VREFB4AN0	ID			DIFFIO_TX B4bn	DIFFOUT_B4bn	AK16	DQ08			B.DQ0.1				B.DQ0.1
4A	VREFB4AN0	ID			DIFFIO_RX B4bn	DIFFOUT_B4bn	AH20	DQ08			B.DQ.4				B.DQ.4
4A	VREFB4AN0	ID			DIFFIO_TX B4bn	DIFFOUT_B4bn	A176	DQ08			B.DQ.6				B.DQ.6
4A	VREFB4AN0	ID			DIFFIO_RX B4bn	DIFFOUT_B4bn	AG21	DQ08			B.DQ.5				B.DQ.5
4A	VREFB4AN0	ID	CLK2n		DIFFIO_RX B4bn	DIFFOUT_B4bn	AH18	DQ08							
4A	VREFB4AN0	ID	CLK2n		DIFFIO_TX B4bn	DIFFOUT_B4bn	AB17	DQ08		B.DQ.7					B.DQ.7
4A	VREFB4AN0	ID	CLK2p		DIFFIO_RX B4bn	DIFFOUT_B4bn	AW16	DQ08							
4A	VREFB4AN0	ID			DIFFIO_TX B4bn	DIFFOUT_B4bn	AH17	DQ08			B.DM.0				B.DM.0
4A	VREFB4AN0	ID			DIFFIO_TX B4bn	DIFFOUT_B4bn	AH16	DQ08			GND				GND
4A	VREFB4AN0	ID			DIFFIO_RX B5bn	DIFFOUT_B5bn	AK18	DQ08	DQ2B		B.DQ.8				B.DQ.8
4A	VREFB4AN0	ID			DIFFIO_TX B4bn	DIFFOUT_B4bn	AG18	DQ08			B.DQ.10				B.DQ.10
4A	VREFB4AN0	ID			DIFFIO_RX B5bn	DIFFOUT_B5bn	AJ17	DQ08			B.DQ.9				B.DQ.9
4A	VREFB4AN0	ID			DIFFIO_RX B5bn	DIFFOUT_B5bn	W17	DQS0B	DQ2B		B.DQS0.1				B.DQS0.1
4A	VREFB4AN0	ID			DIFFIO_TX B5bn	DIFFOUT_B5bn	AK19	DQ08			B.DQ.11				B.DQ.11
4A	VREFB4AN0	ID			DIFFIO_RX B5bn	DIFFOUT_B5bn	V17	DQS0B			B.DQS.1				B.DQS.1
4A	VREFB4AN0	ID			DIFFIO_TX B5bn	DIFFOUT_B5bn	AJ19	DQ08			B.CKE.1				B.CKE.1
4A	VREFB4AN0	ID			DIFFIO_TX B5bn	DIFFOUT_B5bn	A21	DQ08			B.CKE.0				B.CKE.0
4A	VREFB4AN0	ID			DIFFIO_RX B5bn	DIFFOUT_B5bn	AG20	DQ08			B.DQ.12				B.DQ.12
4A	VREFB4AN0	ID			DIFFIO_TX B5bn	DIFFOUT_B5bn	A20	DQ08			B.DQ.14				B.DQ.14
4A	VREFB4AN0	ID			DIFFIO_RX B5bn	DIFFOUT_B5bn	AF19	DQ08			B.DQ.13				B.DQ.13
4A	VREFB4AN0	ID	CLK3n		DIFFIO_RX B5bn	DIFFOUT_B5bn	AH17	DQ08							
4A	VREFB4AN0	ID	CLK3p		DIFFIO_TX B5bn	DIFFOUT_B5bn	AG24	DQ08			B.DQ.15				B.DQ.15
4A	VREFB4AN0	ID			DIFFIO_RX B5bn	DIFFOUT_B5bn	AC18	DQ08							
4A	VREFB4AN0	ID			DIFFIO_TX B5bn	DIFFOUT_B5bn	AG23	DQ08			B.DM.1				B.DM.1
4A	VREFB4AN0	ID			DIFFIO_TX B5bn	DIFFOUT_B5bn	AG22	DQ08			GND				GND
4A	VREFB4AN0	ID			DIFFIO_RX B5bn	DIFFOUT_B5bn	AE19	DQ08			B.DQ.16				B.DQ.16
4A	VREFB4AN0	ID			DIFFIO_TX B5bn	DIFFOUT_B5bn	AG23	DQ08			B.DQ.18				B.DQ.18
4A	VREFB4AN0	ID			DIFFIO_RX B5bn	DIFFOUT_B5bn	AE16	DQ08			B.DQ.17				B.DQ.17
4A	VREFB4AN0	ID			DIFFIO_RX B5bn	DIFFOUT_B5bn	AA18	DQS0B	DQS2B		B.DQS0.2				B.DQS0.2
4A	VREFB4AN0	ID			DIFFIO_TX B5bn	DIFFOUT_B5bn	AK22	DQ08			B.DQ.19				B.DQ.19
4A	VREFB4AN0	ID			DIFFIO_RX B5bn	DIFFOUT_B5bn	V17	DQS0B	DQS2B		B.DQS.2				B.DQS.2
4A	VREFB4AN0	ID			DIFFIO_TX B5bn	DIFFOUT_B5bn	AF21	DQ08			B.DQ.20				B.DQ.20
4A	VREFB4AN0	ID			DIFFIO_TX B5bn	DIFFOUT_B5bn	AG21	DQ08			B.RESET0				B.RESET0
4A	VREFB4AN0	ID			DIFFIO_RX B5bn	DIFFOUT_B5bn	AJ22	DQ08			B.DQ.22				B.DQ.22
4A	VREFB4AN0	ID			DIFFIO_TX B5bn	DIFFOUT_B5bn	AF20	DQ08			B.DQ.21				B.DQ.21
4A	VREFB4AN0	ID			DIFFIO_RX B5bn	DIFFOUT_B5bn	AA19	DQ08			GND				GND
4A	VREFB4AN0	ID			DIFFIO_TX B5bn	DIFFOUT_B5bn	AK24	DQ08			B.DQ.23				B.DQ.23
4A	VREFB4AN0	ID			DIFFIO_RX B5bn	DIFFOUT_B5bn	V18	DQ08			GND				GND
4A	VREFB4AN0	ID			DIFFIO_TX B5bn	DIFFOUT_B5bn	AG23	DQ08			B.DM.2				B.DM.2
4A	VREFB4AN0	ID			DIFFIO_TX B5bn	DIFFOUT_B5bn	AJ25	DQ08			GND				GND
4A	VREFB4AN0	ID			DIFFIO_RX B5bn	DIFFOUT_B5bn	AF24	DQ08	DQ3B		B.DQ.24				B.DQ.24
4A	VREFB4AN0	ID			DIFFIO_TX B5bn	DIFFOUT_B5bn	AJ24	DQ08			B.DQ.26				B.DQ.26
4A	VREFB4AN0	ID			DIFFIO_RX B5bn	DIFFOUT_B5bn	AF23	DQ08			B.DQ.25				B.DQ.25
4A	VREFB4AN0	ID			DIFFIO_TX B5bn	DIFFOUT_B5bn	AH19	DQS0B	DQS3B		B.DQS0.3				B.DQS0.3
4A	VREFB4AN0	ID			DIFFIO_RX B5bn	DIFFOUT_B5bn	AK26	DQ08			B.DQ.27				B.DQ.27
4A	VREFB4AN0	ID			DIFFIO_TX B5bn	DIFFOUT_B5bn	AG20	DQS0B	DQS3B		B.DQS.3				B.DQS.3
4A	VREFB4AN0	ID			DIFFIO_TX B5bn	DIFFOUT_B5bn	AJ26	DQ08			GND				GND
4A	VREFB4AN0	ID			DIFFIO_RX B5bn	DIFFOUT_B5bn	AH25	DQ08			GND				GND
4A	VREFB4AN0	ID			DIFFIO_RX B7bn	DIFFOUT_B7bn	AE23	DQ08			B.DQ.28				B.DQ.28
4A	VREFB4AN0	ID			DIFFIO_TX B5bn	DIFFOUT_B5bn	AG25	DQ08			B.DQ.30				B.DQ.30
4A	VREFB4AN0	ID			DIFFIO_RX B7bn	DIFFOUT_B7bn	AE22	DQ08			B.DQ.29				B.DQ.29
4A	VREFB4AN0	ID			DIFFIO_RX B7bn	DIFFOUT_B7bn	W19	DQ08			GND				GND
4A	VREFB4AN0	ID			DIFFIO_TX B7bn	DIFFOUT_B7bn	AK27	DQ08			B.DQ.31				B.DQ.31
4A	VREFB4AN0	ID			DIFFIO_RX B7bn	DIFFOUT_B7bn	V18	DQ08			GND				GND
4A	VREFB4AN0	ID			DIFFIO_TX B7bn	DIFFOUT_B7bn	AJ27	DQ08	DQ3B		B.DM.3				B.DM.3
4A	VREFB4AN0	ID			DIFFIO_TX B7bn	DIFFOUT_B7bn	AK29	DQ08			GND				GND
4A	VREFB4AN0	ID			DIFFIO_RX B7bn	DIFFOUT_B7bn	AD21	DQ10B			B.DQ.32				B.DQ.32
4A	VREFB4AN0	ID			DIFFIO_TX B7bn	DIFFOUT_B7bn	AK28	DQ10B			B.DQ.34				B.DQ.34
4A	VREFB4AN0	ID			DIFFIO_RX B7bn	DIFFOUT_B7bn	AD20	DQ10B			B.DQ.33				B.DQ.33
4A	VREFB4AN0	ID			DIFFIO_RX B7bn	DIFFOUT_B7bn	AA20	DQS0.10B	DQS3B		B.DQS0.4				B.DQS0.4
4A	VREFB4AN0	ID			DIFFIO_TX B7bn	DIFFOUT_B7bn	AH27	DQ10B			B.DQ.35				B.DQ.35
4A	VREFB4AN0	ID			DIFFIO_RX B7bn	DIFFOUT_B7bn	V19	DQS0.10B	DQS3B		B.DQS.4				B.DQS.4
4A	VREFB4AN0	ID			DIFFIO_TX B7bn	DIFFOUT_B7bn	AG28	DQ08			GND				GND
4A	VREFB4AN0	ID			DIFFIO_RX B7bn	DIFFOUT_B7bn	AK28	DQ10B	DQ3B		B.DQ.36				B.DQ.36
4A	VREFB4AN0	ID			DIFFIO_TX B7bn	DIFFOUT_B7bn	AC23	DQ10B			B.DQ.38				B.DQ.38
4A	VREFB4AN0	ID			DIFFIO_RX B7bn	DIFFOUT_B7bn	AF25	DQ10B			B.DQ.37				B.DQ.37
4A	VREFB4AN0	ID			DIFFIO_TX B7bn	DIFFOUT_B7bn	AK29	DQ10B			GND				GND
4A	VREFB4AN0	ID			DIFFIO_RX B7bn	DIFFOUT_B7bn	AE21	DQ08			GND				GND
4A	VREFB4AN0	ID			DIFFIO_TX B8bn	DIFFOUT_B8bn	AE24	DQ10B			B.DQ.39				B.DQ.39
4A	VREFB4AN0	ID			DIFFIO_RX B7bn	DIFFOUT_B7bn	AA21	DQ08			GND				GND
4A	VREFB4AN0	ID	RZ0_1		DIFFIO_TX B8bn	DIFFOUT_B8bn	AD24	DQ10B	DQ3B		B.DM.4				B.DM.4
5A	VREFB5AN0	ID			DIFFIO_RX R1p	DIFFOUT_R1p	AG27	DQ1R							
5A	VREFB5AN0	ID		INT_DONE	DIFFIO_RX R2p	DIFFOUT_R2p	AD25	DQ1R							
5A	VREFB5AN0	ID		PR_REQUEST	DIFFIO_TX R1n	DIFFOUT_R1n	AG28	DQ1R							
5A	VREFB5AN0	ID		CRC_ERROR	DIFFIO_RX R2n	DIFFOUT_R2n	AC25	DQ1R							
5A	VREFB5AN0	ID		HCIO	DIFFIO_TX R3n	DIFFOUT_R3n	AJ29	DQ1R							
5A	VREFB5AN0	ID			DIFFIO_RX R4p	DIFFOUT_R4p	W20	DQ1R							
5A	VREFB5AN0	ID		CvP_CONFDONE	DIFFIO_TX R3n	DIFFOUT_R3n	AH29	DQ1R							
5A	VREFB5AN0	ID			DIFFIO_RX R4n	DIFFOUT_R4n	V21	DQ1R							
5A	VREFB5AN0	ID		DEV_0E	DIFFIO_TX R5p	DIFFOUT_R5p	AE26	DQ08							
5A	VREFB5AN0	ID		IPERSTL0	DIFFIO_RX R6p	DIFFOUT_R6p	W21	DQS1R							
5A	VREFB5AN0	ID		DEV_1L0n	DIFFIO_TX R5n	DIFFOUT_R5n	AD27	DQ1R							
5A	VREFB5AN0	ID		IPERSTL1	DIFFIO_RX R6n	DIFFOUT_R6n	W22	DQS1R							
5A	VREFB5AN0	ID			DIFFIO_TX R7p	DIFFOUT_R7p	AA25	DQ1R							
5A	VREFB5AN0	ID			DIFFIO_RX R6n	DIFFOUT_R6n	AE22	DQ1R							
5A	VREFB5AN0	ID			DIFFIO_TX R7n	DIFFOUT_R7n	AB26	DQ08							
5A	VREFB5AN0	ID			DIFFIO_RX R8n	DIFFOUT_R8n	AB23	DQ1R							
5A	VREFB5AN0	ID			DIFFIO_TX R8p	DIFFOUT_R8p	AK24	DQ08							
5A	VREFB5AN0	ID			DIFFIO_TX R10p	DIFFOUT_R10p	AE27	DQ2R							
5A	VREFB5AN0	ID			DIFFIO_RX R8n	DIFFOUT_R8n	AB25	DQ2R							
5A	VREFB5AN0	ID			DIFFIO_TX R10n	DIFFOUT_R10n	AE28	DQ2R							
5A	VREFB5AN0	ID			DIFFIO_RX R11p	DIFFOUT_R11p	Y23	DQ2R							
5A	VREFB5AN0	ID			DIFFIO_TX R12p	DIFFOUT_R12p	AG28	DQ2R							
5A	VREFB5AN0	ID			DIFFIO_RX R11n	DIFFOUT_R11n	Y24	DQ2R							
5A	VREFB5AN0	ID			DIFFIO_TX R12n	DIFFOUT_R12n	AF28	DQ2R							
5A	VREFB5AN0	ID			DIFFIO_RX R13p	DIFFOUT_R13p	V23	DQS2R							
5A	VREFB5AN0	ID			DIFFIO_TX R14n	DIFFOUT_R14n	AF29	DQ08							
5A	VREFB5AN0	ID			DIFFIO_RX R13n	DIFFOUT_R13n	W24	DQS0.2R							

Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
5B	VREFB5BND	ID			DIFFIO_RX_R19a	DIFFOUT_R19a	A430	DQ3R							
5B	VREFB5BND	ID			DIFFIO_TX_R20a	DIFFOUT_R20a	A438	DQ3R							
5B	VREFB5BND	ID	CLK9p		DIFFIO_RX_R21a	DIFFOUT_R21a	A426	DQ3SR							
5B	VREFB5BND	ID	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUT0,FPLL_BR_FB		DIFFIO_TX_R22a	DIFFOUT_R22a	A52								
5B	VREFB5BND	ID	CLK6n		DIFFIO_RX_R21a	DIFFOUT_R21a	A827	DQ3SR							
5B	VREFB5BND	ID	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUT1		DIFFIO_TX_R22a	DIFFOUT_R22a	A029	DQ3R							
5B	VREFB5BND	ID	CLK6a,FPLL_BR_FB		DIFFIO_RX_R22a	DIFFOUT_R22a	V28	DQ3SR							
5B	VREFB5BND	ID			DIFFIO_TX_R24a	DIFFOUT_R24a	A030	DQ3R							
5B	VREFB5BND	ID	CLK6a,FPLL_BR_FB		DIFFIO_RX_R22a	DIFFOUT_R22a	V27	DQ3R							
5B	VREFB5BND	ID	R20a_2		DIFFIO_TX_R24a	DIFFOUT_R24a	A030	DQ3R							
5B	VREFB5BND_HPS	HPS_DDR								HPS_DM_4	HPS_DM_4				
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQ_39	HPS_DQ_39				
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQ_37	HPS_DQ_37				
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQ_38	HPS_DQ_38				
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQ_36	HPS_DQ_36				
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQS_4	HPS_DQS_4				
5B	VREFB5BND_HPS	HPS_GPI3													
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQS_4	HPS_DQS_4				
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQ_35	HPS_DQ_35				
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQ_33	HPS_DQ_33				
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQ_34	HPS_DQ_34				
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQ_32	HPS_DQ_32				
5B	VREFB5BND_HPS	HPS_GPI12													
5B	VREFB5BND_HPS	HPS_GPI1													
5B	VREFB5BND_HPS	HPS_DDR								HPS_DM_3	HPS_DM_3				
5B	VREFB5BND_HPS	HPS_GPI10													
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQ_31	HPS_DQ_31				
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQ_29	HPS_DQ_29				
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQ_30	HPS_DQ_30				
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQ_28	HPS_DQ_28				
5B	VREFB5BND_HPS	VREFB5BND_HPS													
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQS_3	HPS_DQS_3				
5B	VREFB5BND_HPS	HPS_GPI8													
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQS_3	HPS_DQS_3				
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQ_27	HPS_DQ_27				
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQ_25	HPS_DQ_25				
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQ_26	HPS_DQ_26				
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQ_24	HPS_DQ_24				
5B	VREFB5BND_HPS	HPS_GPI6													
5B	VREFB5BND_HPS	HPS_GPI7													
5B	VREFB5BND_HPS	HPS_DDR								HPS_DM_2	HPS_DM_2				
5B	VREFB5BND_HPS	HPS_GPI6													
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQ_21	HPS_DQ_21				
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQ_22	HPS_DQ_22				
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQ_20	HPS_DQ_20				
5B	VREFB5BND_HPS	HPS_GPI5													
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQS_2	HPS_DQS_2				
5B	VREFB5BND_HPS	HPS_DDR								HPS_RESET#	HPS_RESET#				
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQS_2	HPS_DQS_2				
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQ_18	HPS_DQ_18				
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQ_17	HPS_DQ_17				
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQ_18	HPS_DQ_18				
5B	VREFB5BND_HPS	HPS_DDR								HPS_DQ_16	HPS_DQ_16				
5A	VREFB5AND	HPS_GPI3													
5A	VREFB5AND	HPS_DDR								HPS_DM_1	HPS_DM_1				
5A	VREFB5AND	HPS_DDR													
5A	VREFB5AND	HPS_DDR								HPS_DQ_15	HPS_DQ_15				
5A	VREFB5AND	HPS_DDR								HPS_DQ_13	HPS_DQ_13				
5A	VREFB5AND	HPS_DDR								HPS_DQ_14	HPS_DQ_14				
5A	VREFB5AND	HPS_DDR								HPS_DQ_12	HPS_DQ_12				
5A	VREFB5AND	HPS_DDR								HPS_DQS_0	HPS_DQS_0				
5A	VREFB5AND	HPS_DDR								HPS_DQS_1	HPS_DQS_1				
5A	VREFB5AND	HPS_DDR								HPS_DQS_1	HPS_DQS_1				
5A	VREFB5AND	HPS_DDR								HPS_DQ_11	HPS_DQ_11				
5A	VREFB5AND	HPS_DDR								HPS_DQ_9	HPS_DQ_9				
5A	VREFB5AND	HPS_DDR								HPS_DQ_10	HPS_DQ_10				
5A	VREFB5AND	HPS_DDR								HPS_DQ_8	HPS_DQ_8				
5A	VREFB5AND	HPS_GPI1													
5A	VREFB5AND	HPS_GPI5													
5A	VREFB5AND	HPS_DDR								HPS_DM_0	HPS_DM_0				
5A	VREFB5AND	HPS_DDR								HPS_DQ_7	HPS_DQ_7				
5A	VREFB5AND	HPS_DDR								HPS_DQ_5	HPS_DQ_5				
5A	VREFB5AND	HPS_DDR								HPS_DQ_6	HPS_DQ_6				
5A	VREFB5AND	HPS_DDR								HPS_DQ_4	HPS_DQ_4				
5A	VREFB5AND	HPS_DDR								HPS_ODT_1	HPS_ODT_1				
5A	VREFB5AND	HPS_DDR								HPS_DQS_0	HPS_DQS_0				
5A	VREFB5AND	HPS_DDR								HPS_DQS_0	HPS_DQS_0				
5A	VREFB5AND	HPS_DDR								HPS_DQ_3	HPS_DQ_3				
5A	VREFB5AND	HPS_DDR								HPS_DQ_1	HPS_DQ_1				
5A	VREFB5AND	HPS_DDR								HPS_DQ_2	HPS_DQ_2				
5A	VREFB5AND	HPS_DDR								HPS_DQ_0	HPS_DQ_0				
5A	VREFB5AND	VREFB5AND_HPS													
5A	VREFB5AND	HPS_DDR								HPS_A_0	HPS_CA_0				
5A	VREFB5AND	HPS_DDR								HPS_A_1	HPS_CA_1				
5A	VREFB5AND	HPS_DDR								HPS_A_4	HPS_CA_4				
5A	VREFB5AND	HPS_DDR								HPS_A_2	HPS_CA_2				
5A	VREFB5AND	HPS_DDR								HPS_A_5	HPS_CA_5				
5A	VREFB5AND	HPS_DDR								HPS_A_3	HPS_CA_3				
5A	VREFB5AND	HPS_DDR								HPS_OK	HPS_OK				
5A	VREFB5AND	HPS_DDR								HPS_A_6	HPS_CA_6				
5A	VREFB5AND	HPS_DDR								HPS_C6#	HPS_C6#				
5A	VREFB5AND	HPS_DDR								HPS_A_7	HPS_CA_7				
5A	VREFB5AND	HPS_DDR								HPS_BA_1	HPS_BA_1				
5A	VREFB5AND	HPS_DDR								HPS_BA_2	HPS_BA_2				
5A	VREFB5AND	HPS_DDR								HPS_BA_2	HPS_BA_2				
5A	VREFB5AND	HPS_DDR								HPS_CAS#	HPS_CAS#				
5A	VREFB5AND	HPS_DDR								HPS_BA#	HPS_BA#				
5A	VREFB5AND	HPS_DDR								HPS_A_8	HPS_CA_8				
5A	VREFB5AND	HPS_DDR								HPS_A_10	HPS_CA_9				
5A	VREFB5AND	HPS_DDR								HPS_A_9	HPS_CA_9				
5A	VREFB5AND	HPS_DDR								HPS_A_11	HPS_CA_9				
5A	VREFB5AND	HPS_DDR								HPS_C5#_0	HPS_C5#_0				
5A	VREFB5AND	HPS_DDR								HPS_A_12	HPS_CA_12				
5A	VREFB5AND	HPS_DDR								HPS_C5#_1	HPS_C5#_1				
5A	VREFB5AND	HPS_DDR								HPS_A_13	HPS_CA_13				
5A	VREFB5AND	HPS_DDR								HPS_A_14	HPS_CA_14				
5A	VREFB5AND	HPS_DDR								HPS_WE#	HPS_WE#				
5A	VREFB5AND	HPS_DDR								HPS_A_15	HPS_CA_15				
5A	VREFB5AND	HPS_DQS_0													
5A	VREFB5AND	GND													
5A	VREFB5AND	GND													
5A	VREFB5AND	HPS_nPDR													
5A	VREFB5AND	HPS_nPDR													
5A	VREFB5AND	HPS_nPDR													
5A	VREFB5AND	HPS_TMS													
5A	VREFB5AND	HPS_TCK													
5A	VREFB5AND	HPS_TDI													
5A	VREFB5AND	HPS_TDO													
5A	VREFB5AND	HPS_PORSEL													
5A	VREFB5AND	HPS_PORSEL													
5A	VREFB5AND	HPS_PORSEL													



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated TriX Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0	
7A		HPS_CLK1					D05									
7A		HPS_CLK2					D06									
7A	VREF/F896/ICFG/HPS	TRACE_CLK					B06					TRACE_CLK				HPS_GPD048
7A	VREF/F896/ICFG/HPS	TRACE_D0					B07					TRACE_D0	SPIS0_CLK	UART0_RX		HPS_GPD049
7A	VREF/F896/ICFG/HPS	TRACE_D1					C26					TRACE_D1	SPIS0_MOSI	UART0_TX		HPS_GPD050
7A	VREF/F896/ICFG/HPS	TRACE_D2					A25					TRACE_D2	SPIS0_MISO	IC21_SDA		HPS_GPD051
7A	VREF/F896/ICFG/HPS	TRACE_D3					H03					TRACE_D3	SPIS0_SSD	IC21_SCL		HPS_GPD052
7A	VREF/F896/ICFG/HPS	TRACE_D4					A24					TRACE_D4	CAN0_RX	CAN0_RX		HPS_GPD053
7A	VREF/F896/ICFG/HPS	TRACE_D6					G21					TRACE_D6	SPIS0_MOSI	CAN0_TX		HPS_GPD054
7A	VREF/F896/ICFG/HPS	TRACE_D6					G24					TRACE_D6	SPIS0_SSD	IC21_SDA		HPS_GPD055
7A	VREF/F896/ICFG/HPS	TRACE_D7					E23					TRACE_D7	SPIS0_MISO	IC21_SCL		HPS_GPD056
7A	VREF/F896/ICFG/HPS	SPIM0_CLK					A23					SPIM0_CLK	IC21_SDA	UART0_CTS		HPS_GPD057
7A	VREF/F896/ICFG/HPS	SPIM0_MOSI					C22					SPIM0_MOSI	IC21_SCL	UART0_RTS		HPS_GPD058
7A	VREF/F896/ICFG/HPS	SPIM0_MISO					B23					SPIM0_MISO	CAN0_RX	UART1_CTS		HPS_GPD059
7A	VREF/F896/ICFG/HPS	SPIM0_SS0/BOOTSEL0					H00					SPIM0_SS0	CAN0_TX	UART1_RTS		HPS_GPD060
7A	VREF/F896/ICFG/HPS	UART0_RX					R02					UART0_RX	CAN0_RX	SPIM0_SSI		HPS_GPD061
7A	VREF/F896/ICFG/HPS	UART0_TX_CLKSEL1					G22					UART0_TX	CAN0_TX	SPIM0_SSI		HPS_GPD062
7A	VREF/F896/ICFG/HPS	IC20_SDA					C23					IC20_SDA	UART1_RX	SPIM0_CLK		HPS_GPD063
7A	VREF/F896/ICFG/HPS	IC20_SCL					D02					IC20_SCL	UART1_TX	SPIM0_MOSI		HPS_GPD064
7A	VREF/F896/ICFG/HPS	CAN0_RX					E24					CAN0_RX	UART0_RX	SPIM0_MISO		HPS_GPD065
7A	VREF/F896/ICFG/HPS	CAN0_TX					D04					CAN0_TX	UART0_TX	SPIM0_SSD		HPS_GPD066
7B	VREF/F896/ICFG/HPS	NAND_ALE					H15					NAND_ALE	SGMII_TX_CLK	QSPI_SS3		HPS_GPD14
7B	VREF/F896/ICFG/HPS	NAND_CE					F20					NAND_CE	RGMI0_TXD0	USB1_D0		HPS_GPD15
7B	VREF/F896/ICFG/HPS	NAND_CLE					H19					NAND_CLE	RGMI0_TXD0	USB1_D1		HPS_GPD16
7B	VREF/F896/ICFG/HPS	NAND_RE					F21					NAND_RE	RGMI0_TXD2	USB1_D2		HPS_GPD17
7B	VREF/F896/ICFG/HPS	NAND_RB					H18					NAND_RB	RGMI0_TXD3	USB1_D3		HPS_GPD18
7B	VREF/F896/ICFG/HPS	NAND_DQ0					A21					NAND_DQ0	RGMI0_RXD0			HPS_GPD19
7B	VREF/F896/ICFG/HPS	NAND_DQ1					B21					NAND_DQ1	RGMI0_MDO	IC21_SDA		HPS_GPD20
7B	VREF/F896/ICFG/HPS	NAND_DQ2					E21					NAND_DQ2	RGMI0_MDC	IC21_SCL		HPS_GPD21
7B	VREF/F896/ICFG/HPS	NAND_DQ3					H17					NAND_DQ3	RGMI0_RX_CTL	USB1_D4		HPS_GPD22
7B	VREF/F896/ICFG/HPS	NAND_DQ4					A20					NAND_DQ4	RGMI0_TX_CTL	USB1_D5		HPS_GPD23
7B	VREF/F896/ICFG/HPS	NAND_DQ6					G20					NAND_DQ6	RGMI0_RX_CLK	USB1_D6		HPS_GPD24
7B	VREF/F896/ICFG/HPS	NAND_DQ6					B20					NAND_DQ6	RGMI0_RXD1	USB1_D7		HPS_GPD25
7B	VREF/F896/ICFG/HPS	NAND_DQ7					H18					NAND_DQ7	RGMI0_R0D2			HPS_GPD26
7B	VREF/F896/ICFG/HPS	NAND_WP					D21					NAND_WP	RGMI0_RXD3	QSPI_SS2		HPS_GPD27
7B	VREF/F896/ICFG/HPS	NAND_WE/BOOTSEL2					D20					NAND_WE	QSPI_SS1			HPS_GPD28
7B	VREF/F896/ICFG/HPS	QSPI_K0					C20					QSPI_K0		USB1_CLK		HPS_GPD29
7B	VREF/F896/ICFG/HPS	QSPI_K01					H18					QSPI_K01		USB1_STP		HPS_GPD30
7B	VREF/F896/ICFG/HPS	QSPI_K03					A19					QSPI_K03		USB1_D8		HPS_GPD31
7B	VREF/F896/ICFG/HPS	QSPI_K03					E19					QSPI_K03		USB1_NXT		HPS_GPD32
7B	VREF/F896/ICFG/HPS	QSPI_SS0/BOOTSEL1					A18					QSPI_SS0				HPS_GPD33
7B	VREF/F896/ICFG/HPS	QSPI_CLK					H19					QSPI_CLK				HPS_GPD34
7B	VREF/F896/ICFG/HPS	QSPI_SS1					C19					QSPI_SS1				HPS_GPD35
7C	VREF/F896/ICFG/HPS	SDMMC_CMD					F19					SDMMC_CMD	USB0_D0			HPS_GPD36
7C	VREF/F896/ICFG/HPS	SDMMC_PAREN					B17					SDMMC_PAREN	USB0_D1			HPS_GPD37
7C	VREF/F896/ICFG/HPS	SDMMC_D0					G18					SDMMC_D0	USB0_D2			HPS_GPD38
7C	VREF/F896/ICFG/HPS	SDMMC_D1					C17					SDMMC_D1	USB0_D3			HPS_GPD39
7C	VREF/F896/ICFG/HPS	SDMMC_D4					H17					SDMMC_D4	USB0_D4			HPS_GPD40
7C	VREF/F896/ICFG/HPS	SDMMC_D5					C18					SDMMC_D5	USB0_D5			HPS_GPD41
7C	VREF/F896/ICFG/HPS	SDMMC_D6					G17					SDMMC_D6	USB0_D6			HPS_GPD42
7C	VREF/F896/ICFG/HPS	SDMMC_D7					E18					SDMMC_D7	USB0_D7			HPS_GPD43
7C	VREF/F896/ICFG/HPS	HPS_GPD044					E17					SDMMC_CLK	USB0_CLK			HPS_GPD44
7C	VREF/F896/ICFG/HPS	SDMMC_CCLK_OUT					A16					SDMMC_CCLK_OUT	USB0_STP			HPS_GPD45
7C	VREF/F896/ICFG/HPS	SDMMC_RZ					D17					SDMMC_D2	USB0_D8			HPS_GPD46
7C	VREF/F896/ICFG/HPS	SDMMC_D3					B16					SDMMC_D3	USB0_NXT			HPS_GPD47
7D	VREF/F896/ICFG/HPS	RGMI0_TX_CLK					F16					RGMI0_TX_CLK				HPS_GPD50
7D	VREF/F896/ICFG/HPS	RGMI0_TXD0					E16					RGMI0_TXD0	USB1_D0			HPS_GPD51
7D	VREF/F896/ICFG/HPS	RGMI0_TXD1					G16					RGMI0_TXD1	USB1_D1			HPS_GPD52
7D	VREF/F896/ICFG/HPS	RGMI0_TXD2					D16					RGMI0_TXD2	USB1_D2			HPS_GPD53
7D	VREF/F896/ICFG/HPS	RGMI0_TXD3					H16					RGMI0_TXD3	USB1_D3			HPS_GPD54
7D	VREF/F896/ICFG/HPS	RGMI0_RXD0					A15					RGMI0_RXD0	USB1_D4			HPS_GPD55
7D	VREF/F896/ICFG/HPS	RGMI0_MDO					C15					RGMI0_MDO	USB1_D5			HPS_GPD56
7D	VREF/F896/ICFG/HPS	RGMI0_MDC					D15					RGMI0_MDC	IC21_SDA			HPS_GPD57
7D	VREF/F896/ICFG/HPS	RGMI0_RX_CTL					B15					RGMI0_RX_CTL	USB1_D6			HPS_GPD58
7D	VREF/F896/ICFG/HPS	RGMI0_TX_CTL					H15					RGMI0_TX_CTL	USB1_D7			HPS_GPD59
7D	VREF/F896/ICFG/HPS	RGMI0_RX_CLK					C14					RGMI0_RX_CLK	USB1_D8			HPS_GPD60
7D	VREF/F896/ICFG/HPS	RGMI0_RXD1					E14					RGMI0_RXD1	USB1_STP			HPS_GPD61
7D	VREF/F896/ICFG/HPS	RGMI0_RXD2					H14					RGMI0_RXD2	USB1_D9			HPS_GPD62
7D	VREF/F896/ICFG/HPS	RGMI0_RXD3					A14					RGMI0_RXD3	USB1_NXT			HPS_GPD63
8A	VREF/BAND	ID	CLK7p				H15					DIFF0_T1p	DIFFOUT_T1p			
8A	VREF/BAND	ID	CLK7n				B13					DIFF0_T2p	DIFFOUT_T2p			DDI1T
8A	VREF/BAND	ID					G15					DIFF0_RX_T1p	DIFFOUT_T1p			
8A	VREF/BAND	ID					A13					DIFF0_T2p	DIFFOUT_T2p			DDI1T
8A	VREF/BAND	ID					C13					DIFF0_RX_T2p	DIFFOUT_T2p			DDI1T
8A	VREF/BAND	ID	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUT5,FPLL_TL_FB				A11					DIFF0_TX_T4p	DIFFOUT_T4p			DDI1T
8A	VREF/BAND	ID					B12					DIFF0_T3p	DIFFOUT_T3p			DDI1T
8A	VREF/BAND	ID	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUT4n				H13					DIFF0_T4p	DIFFOUT_T4p			DDI1T
8A	VREF/BAND	ID					F15					DIFF0_RX_T5p	DIFFOUT_T5p			DQS1T
8A	VREF/BAND	ID					C12					DIFF0_T5p	DIFFOUT_T5p			DDI1T
8A	VREF/BAND	ID					F14					DIFF0_RX_T6p	DIFFOUT_T6p			DQS1nT
8A	VREF/BAND	ID					B11					DIFF0_TX_T6p	DIFFOUT_T6p			DDI1T
8A	VREF/BAND	ID					D11					DIFF0_RX_T7p	DIFFOUT_T7p			DDI1T
8A	VREF/BAND	ID					A8					DIFF0_T8p	DIFFOUT_T8p			DDI1T
8A	VREF/BAND	ID					D10					DIFF0_RX_T7p	DIFFOUT_T7p			DDI1T
8A	VREF/BAND	ID					A8					DIFF0_TX_T8p	DIFFOUT_T8p			DDI1T
8A	VREF/BAND	ID	CLK6p,FPLL_TL_FBp				K14					DIFF0_RX_T9p	DIFFOUT_T9p			DDI1T
8A	VREF/BAND	ID	CLK6n,FPLL_TL_FBn				J14					DIFF0_TX_T10p	DIFFOUT_T10p			DDI1T
8A	VREF/BAND	ID					H7					DIFF0_TX_T10p	DIFFOUT_T10p			DDI1T
8A	VREF/BAND	ID					E9					DIFF0_RX_T11p	DIFFOUT_T11p			DDI1T
8A	VREF/BAND	ID					C9					DIFF0_TX_T12p	DIFFOUT_T12p			DDI1T
8A	VREF/BAND	ID					D9					DIFF0_RX_T11p	DIFFOUT_T11p			DDI1T
8A	VREF/BAND	ID					B8					DIFF0_TX_T12p	DIFFOUT_T12p			DDI1T
8A	VREF/BAND	ID					H14					DIFF0_RX_T13p	DIFFOUT_T13p			DQS2T
8A	VREF/BAND	ID					C10					DIFF0_TX_T14p	DIFFOUT_T14p			DQS2T
8A	VREF/BAND	ID					G13					DIFF0_RX_T13p	DIFFOUT_T13p			DQS2nT
8A	VREF/BAND	ID					C9					DIFF0_TX_T14p	DIFFOUT_T14p			DDI1T
8A	VREF/BAND	ID					F13					DIFF0_RX_T15p	DIFFOUT_T15p			DDI1T
8A	VREF/BAND	ID					A6					DIFF0_TX_T16p	DIFFOUT_T16p			DDI1T
8A	VREF/BAND	ID					E13					DIFF0_RX_T15p	DIFFOUT_T15p			DDI1T
8A	VREF/BAND	ID					H6					DIFF0_TX_T16p	DIFFOUT_T16p			DDI1T
8A	VREF/BAND	ID					H8					DIFF0_RX_T17p	DIFFOUT_T17p			DDI1T
8A	VREF/BAND	ID					A4					DIFF0_TX_T18p	DIFFOUT_T18p			DQS3T
8A	VREF/BAND	ID					C8					DIFF0_RX_T17p	DIFFOUT_T17p			DDI1T
8A	VREF/BAND	ID					A3					DIFF0_TX_T18p	DIFFOUT_T18p			DQS3T
8A	VREF/BAND	ID					E12					DIFF0_RX_T19p	DIFFOUT_T19p			DDI1T
8A	VREF/BAND	ID					D8					DIFF0_TX_T20p	DIFFOUT_T20p			DDI1T
8A	VREF/BAND	ID					D12					DIFF0_RX_T19p	DIFFOUT_T19p			DDI1T
8A	VREF/BAND	ID					C5					DIFF0_TX_T20p	DIFFOUT_T20p			DDI1T
8A	VREF/BAND	ID					H13					DIFF0_RX_T21p	DIFFOUT_T21p			DQS3nT
8A	VREF/BAND	ID					H12					DIFF0_TX_T22p	DIFFOUT_T22p			DDI1T
8A																



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
BA	VREFBAND	ID			DIFFIO_RX_T29p	DIFFOUT_T29m	K12	DQS4T	DQS2T						
BA	VREFBAND	ID			DIFFIO_TX_T30p	DIFFOUT_T30m	D2								
BA	VREFBAND	ID			DIFFIO_RX_T29m	DIFFOUT_T29p	J12	DQS4T	DQS2T						
BA	VREFBAND	ID			DIFFIO_TX_T30m	DIFFOUT_T30p	I2	DQ4T	DQ2T						
BA	VREFBAND	ID			DIFFIO_RX_T31p	DIFFOUT_T31m	G12	DQ4T	DQ2T						
BA	VREFBAND	ID			DIFFIO_TX_T32p	DIFFOUT_T32m	E4	DQ4T	DQ2T						
BA	VREFBAND	ID			DIFFIO_RX_T31m	DIFFOUT_T31p	G11	DQ4T	DQ2T						
BA	VREFBAND	ID			DIFFIO_TX_T32m	DIFFOUT_T32p	D4								
BA	VREFBAND	ID			DIFFIO_RX_T33p	DIFFOUT_T33m	K7								
BA	VREFBAND	ID			DIFFIO_TX_T34p	DIFFOUT_T34m	E3	DQ2T	DQ2T						
BA	VREFBAND	ID			DIFFIO_RX_T33m	DIFFOUT_T33p	K8								
BA	VREFBAND	ID			DIFFIO_TX_T34m	DIFFOUT_T34p	E2	DQ2T	DQ2T						
BA	VREFBAND	ID			DIFFIO_RX_T35p	DIFFOUT_T35m	G10	DQ2T	DQ2T						
BA	VREFBAND	ID			DIFFIO_TX_T36p	DIFFOUT_T36m	E1	DQ2T	DQ2T						
BA	VREFBAND	ID			DIFFIO_RX_T35m	DIFFOUT_T35p	F10	DQ2T	DQ2T						
BA	VREFBAND	ID			DIFFIO_TX_T36m	DIFFOUT_T36p	D1	DQ2T	DQ2T						
BA	VREFBAND	ID			DIFFIO_RX_T37p	DIFFOUT_T37m	J10	DQS6T	DQ2T						
BA	VREFBAND	ID			DIFFIO_TX_T38p	DIFFOUT_T38m	E7								
BA	VREFBAND	ID			DIFFIO_RX_T37m	DIFFOUT_T37p	J9	DQS4T	DQ2T						
BA	VREFBAND	ID			DIFFIO_TX_T38m	DIFFOUT_T38p	E6	DQ2T	DQ2T						
BA	VREFBAND	ID			DIFFIO_RX_T39p	DIFFOUT_T39m	F9	DQ2T	DQ2T						
BA	VREFBAND	ID			DIFFIO_TX_T40p	DIFFOUT_T40m	G7	DQ2T	DQ2T						
BA	VREFBAND	ID			DIFFIO_RX_T39m	DIFFOUT_T39p	F8	DQ2T	DQ2T						
BA	VREFBAND	ID			DIFFIO_TX_T40m	DIFFOUT_T40p	F6								
BA		MSEL0		MSEL0			L5								
BA		CONF_DONE		CONF_DONE			F3								
BA		MSEL1		MSEL1			K6								
BA		HSTATUS		HSTATUS			F4								
BA		RCE		RCE			G5								
BA		MSEL2		MSEL2			G6								
BA		MSEL3		MSEL3			L7								
BA		hCONFIG		hCONFIG			J5								
BA		MSEL4		MSEL4			I9								
	GND						JF								
	GND						A12								
	GND						A17								
	GND						A2								
	GND						A22								
	GND						A27								
	GND						AA11								
	GND						AA22								
	GND						AA3								
	GND						AA4								
	GND						AA6								
	GND						AA9								
	GND						AB1								
	GND						AB19								
	GND						AB2								
	GND						AB29								
	GND						AB5								
	GND						AB7								
	GND						AC16								
	GND						AC26								
	GND						AC3								
	GND						AC4								
	GND						AC5								
	GND						AC8								
	GND						AD1								
	GND						AD2								
	GND						AD23								
	GND						AD5								
	GND						AE10								
	GND						AE20								
	GND						AE3								
	GND						AE4								
	GND						AF1								
	GND						AF12								
	GND						AF17								
	GND						AF2								
	GND						AF27								
	GND						AF3								
	GND						AG14								
	GND						AG24								
	GND						AG8								
	GND						AH1								
	GND						AH11								
	GND						AH21								
	GND						AH6								
	GND						AJ18								
	GND						AJ28								
	GND						AJ3								
	GND						AJ20								
	GND						AK15								
	GND						AK25								
	GND						AK5								
	GND						BL4								
	GND						B19								
	GND						B24								
	GND						B26								
	GND						B9								
	GND						C1								
	GND						C16								
	GND						C21								
	GND						C26								
	GND						C6								
	GND						D13								
	GND						D23								
	GND						D3								
	GND						E10								
	GND						E25								
	GND						E30								
	GND						F17								
	GND						F2								
	GND						F27								
	GND						F5								
	GND						F7								
	GND						G24								
	GND						G3								
	GND						G4								
	GND						H1								
	GND						H11								
	GND						H6								
	GND						H6								
	GND						J18								
	GND						J28								
	GND						J3								
	GND						J4								
	GND						J6								
	GND						K1								
	GND						K10								
	GND						K16								
	GND						K3								
	GND						K20								
	GND						K28								
	GND						K5								

Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					L11								
		GND					L13								
		GND					L15								
		GND					L17								
		GND					L19								
		GND					L22								
		GND					L3								
		GND					L4								
		GND					L6								
		GND					M1								
		GND					M10								
		GND					M12								
		GND					M14								
		GND					M16								
		GND					M18								
		GND					M2								
		GND					M20								
		GND					M29								
		GND					M5								
		GND					M7								
		GND					M8								
		GND					N11								
		GND					N13								
		GND					N16								
		GND					N17								
		GND					N19								
		GND					N26								
		GND					N3								
		GND					N4								
		GND					N6								
		GND					N8								
		GND					N9								
		GND					P1								
		GND					P10								
		GND					P12								
		GND					P14								
		GND					P16								
		GND					P18								
		GND					P2								
		GND					P20								
		GND					P5								
		GND					P7								
		GND					R11								
		GND					R13								
		GND					R15								
		GND					R17								
		GND					R3								
		GND					R30								
		GND					R4								
		GND					R6								
		GND					R8								
		GND					R9								
		GND					T1								
		GND					T10								
		GND					T12								
		GND					T14								
		GND					T15								
		GND					T16								
		GND					T2								
		GND					T20								
		GND					T27								
		GND					T5								
		GND					T7								
		GND					U11								
		GND					U13								
		GND					U15								
		GND					U17								
		GND					U24								
		GND					U29								
		GND					U3								
		GND					U4								
		GND					U6								
		GND					U9								
		GND					V1								
		GND					V10								
		GND					V12								
		GND					V14								
		GND					V19								
		GND					V2								
		GND					V21								
		GND					V5								
		GND					W1								
		GND					W11								
		GND					W13								
		GND					W18								
		GND					W28								
		GND					W3								
		GND					W4								
		GND					W6								
		GND					W9								
		GND					Y1								
		GND					Y10								
		GND					Y12								
		GND					Y14								
		GND					Y15								
		GND					Y2								
		GND					Y20								
		GND					Y25								
		GND					Y30								
		GND					Y5								
		GND					Y7								
		GND					Y8								
		GND					U22								
		GND					T18								
		VCC					M11								
		VCC					M13								
		VCC					M9								
		VCC					N10								
		VCC					N12								
		VCC					N14								
		VCC					P11								
		VCC					P10								
		VCC					R10								
		VCC					R12								
		VCC					R14								
		VCC					T11								
		VCC					T13								
		VCC					U10								
		VCC					U12								
		VCC					U14								
		VCC					V1								
		VCC					V13								
		VCC					V15								
		VCC					W10								
		VCC					W12								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCC					W14								
		VCC					Y11								
		VCC					Y13								
		VCC					Y5								
		VCC					U21								
		DNU					F1								
		DNU					G2								
		DNU					AA7								
		DNU					AD15								
		DNU					E26								
		DNU					J15								
		VCCP0M					AR10								
		VCCP0M					AA23								
		VCCP0M					J1								
		VCC0A7					HE								
		VCC03A					AC11								
		VCC03A					AD8								
		VCC03A					AF7								
		VCC03A					AG4								
		VCC03B					AB14								
		VCC03B					AD13								
		VCC03B					AE15								
		VCC03B					AJ13								
		VCC03B					AJ8								
		VCC03B					AK10								
		VCC04A					AA17								
		VCC04A					AC21								
		VCC04A					AD18								
		VCC04A					AE25								
		VCC04A					AF22								
		VCC04A					AG19								
		VCC04A					AH16								
		VCC04A					AH26								
		VCC04A					AJ23								
		VCC04A					AK20								
		VCC05A					AB24								
		VCC05A					AD28								
		VCC05A					AG29								
		VCC05B					W23								
		VCC05B					AA27								
		VCC05B					AE30								
		VCC06A HPS					D26								
		VCC06A HPS					G29								
		VCC06A HPS					H26								
		VCC06A HPS					K24								
		VCC06A HPS					K30								
		VCC06A HPS					L27								
		VCC06A HPS					M24								
		VCC06A HPS					N21								
		VCC06B HPS					P23								
		VCC06B HPS					P26								
		VCC06B HPS					R25								
		VCC06B HPS					T22								
		VCC06B HPS					U19								
		VCC06B HPS					V26								
		VCC07A HPS					F22								
		VCC07A HPS					H21								
		VCC07B HPS					E20								
		VCC07B HPS					G19								
		VCC07B HPS					G18								
		VCC07B HPS					E15								
		VCC07B HPS					H16								
		VCC08A					A7								
		VCC08A					B4								
		VCC08A					C11								
		VCC08A					D8								
		VCC08A					E5								
		VCC08A					F12								
		VCC08A					G14								
		VCC08A					G9								
		VCC08A					H6								
		VCC08A					J13								
		VCCP38A					AA10								
		VCCP38A					AC10								
		VCCP38A					AB18								
		VCCP38A					AB20								
		VCCP38A					AC13								
		VCCP38A					AC15								
		VCCP38A					AC17								
		VCCP38A					AC19								
		VCCP38A					AD16								
		VCCP38A					AE21								
		VCCP5A					V22								
		VCCP5A					V24								
		VCCP5B					U23								
		VCCP6A6B HPS					M21								
		VCCP6A6B HPS					N22								
		VCCP6A6B HPS					P21								
		VCCP6A6B HPS					R20								
		VCCP6A6B HPS					R23								
		VCCP7A HPS					K19								
		VCCP7B HPS					K18								
		VCCP7C HPS					J17								
		VCCP7D HPS					K16								
		VCCP8A					K11								
		VCCP8A					K13								
		VCCP8A					L10								
		VCCP8A					L12								
		VCCP8A					L14								
3A	VREFB3A0	VREFB3A0					AD6								
3B	VREFB3B0	VREFB3B0					AJ15								
4A	VREFB4A0	VREFB4A0					AK17								
5A	VREFB5A0	VREFB5A0					AC24								
5B	VREFB5B0	VREFB5B0					AK23								
6A	VREFB7A7C7D0 HPS	VREFB7A7C7D0 HPS					E22								
	VREFB8A0	VREFB8A0					B10								
		VCC1 GXBL					AB6								
		VCC1 GXBL					PE								
		VCC1 GXBL					VE								
		VCC1 GXBL					LE								
		VCC1 GXBL					RE								
		VCC1 GXBL					WE								
		VCC1 CLK HPS					LD0								
		RREF TL					G1								
		VCCA FPLL					N7								
		VCCA FPLL					RF								
		VCCA FPLL					VB								
		VCCA FPLL					AA6								
		VCCA FPLL					WS								
		VCC AUX					Y22								
		VCC AUX					AB11								
		VCC AUX					AB16								
		VCC AUX					AD22								
		VCC AUX					HY0								
		VCC AUX					J16								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCC_AUX_SHARED					L21								
		VCC_GXBL					AA5								
		VCC_GXBL					ME								
		VCC_GXBL					NE								
		VCC_GXBL					TE								
		VCC_GXBL					US								
		VCC_GXBL					YE								
		VCCPLL_HPS					L21								
		VCC_HPS					U18								
		VCC_HPS					L18								
		VCC_HPS					L18								
		VCC_HPS					L20								
		VCC_HPS					M15								
		VCC_HPS					N20								
		VCC_HPS					P19								
		VCC_HPS					P17								
		VCC_HPS					P19								
		VCC_HPS					R18								
		VCC_HPS					T17								
		VCC_HPS					T19								
		VCC_HPS					U16								

Note:
 (1) For more information about pin definitions and pin connection guidelines, refer to the [Cyclone V Device Family Pin Connection Guidelines](#).
 (2) HPS_DDR pins are for memory interface only. For the dedicated pin function corresponding with the respective memory interfaces, refer to the HMC columns.
 (3) RESET pin is only applicable for DDR3 device.



Pin Information for the Cyclone® V 5CSTFD5 Device
Version 1.4

Version Number	Date	Changes Made
1.0	10/18/2012	Initial release.
1.1	1/17/2013	A pin that was marked as VCC_HPS has been corrected to VCCRSTCLK_HPS
1.2	3/25/2013	Updated the following pin names: - Changed SDMMC_CLK_IN to SDMMC_FB_CLK_IN - Changed SDMMC_CLK to SDMMC_CCLK_OUT
1.3	9/30/2014	- Remove corresponding bank number from VCCRSTCLK_HPS pin. - Changed HMC Pin Assignment for DDR3 to HMC Pin Assignment for DDR3/DDR2. - Added note 3.
1.4	12/23/2016	-Renamed SDMMC_FB_CLK_IN to HPS_GPIO44.