

Stratix 10 SoC FPGA Development Kit Board

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REV	DATE	PAGES	DESCRIPTION
0.1		All	INITIAL REVISION A RELEASE
A.0 release		All	Power/Sil/Mechanical Test Board Release
A.1 release		25	Add FGPA dedicated I2C port to Optical Module
		21,22	Move signal FALAP17 to FPGA clock input pin
		7	Add Header to select USB blaster code
		25	Move signal FBLAP17 to FPGA clock input pin
		28	SWAP byte assignment of FPGA DDR ports.
		15	C185 to 1uf
		35	R851 value is changed to 17.4K Wrong connection of C1614
		27	Change C249 decoupling to VDD
			Add more Power test pins
		28	Change Memory IO connection for I J K L
		10,11	Sepearte case gnd and signa gnd
		10,11	Change R63, R87 to 4.7K
		12	Update U13 Symbol
		15	ADD U18 I2C Address
		21	Fix Signal PN connections
		22	Fix Signal PN connections, add dedicated I2C ports for clock cleaner and QSFP+ ports
		25	Add dedicated I2C ports for Video and SFP ports
		30	Change JTAG RESET to DC Power good
		31	Add pull down resistor
		36	Change AC coupling cap from 4.7uf to 0.1uf
		42	Fix Signal PN connections. Change J56 from 2-pin to 3-pin
		46	Short A-GND to Signal GND



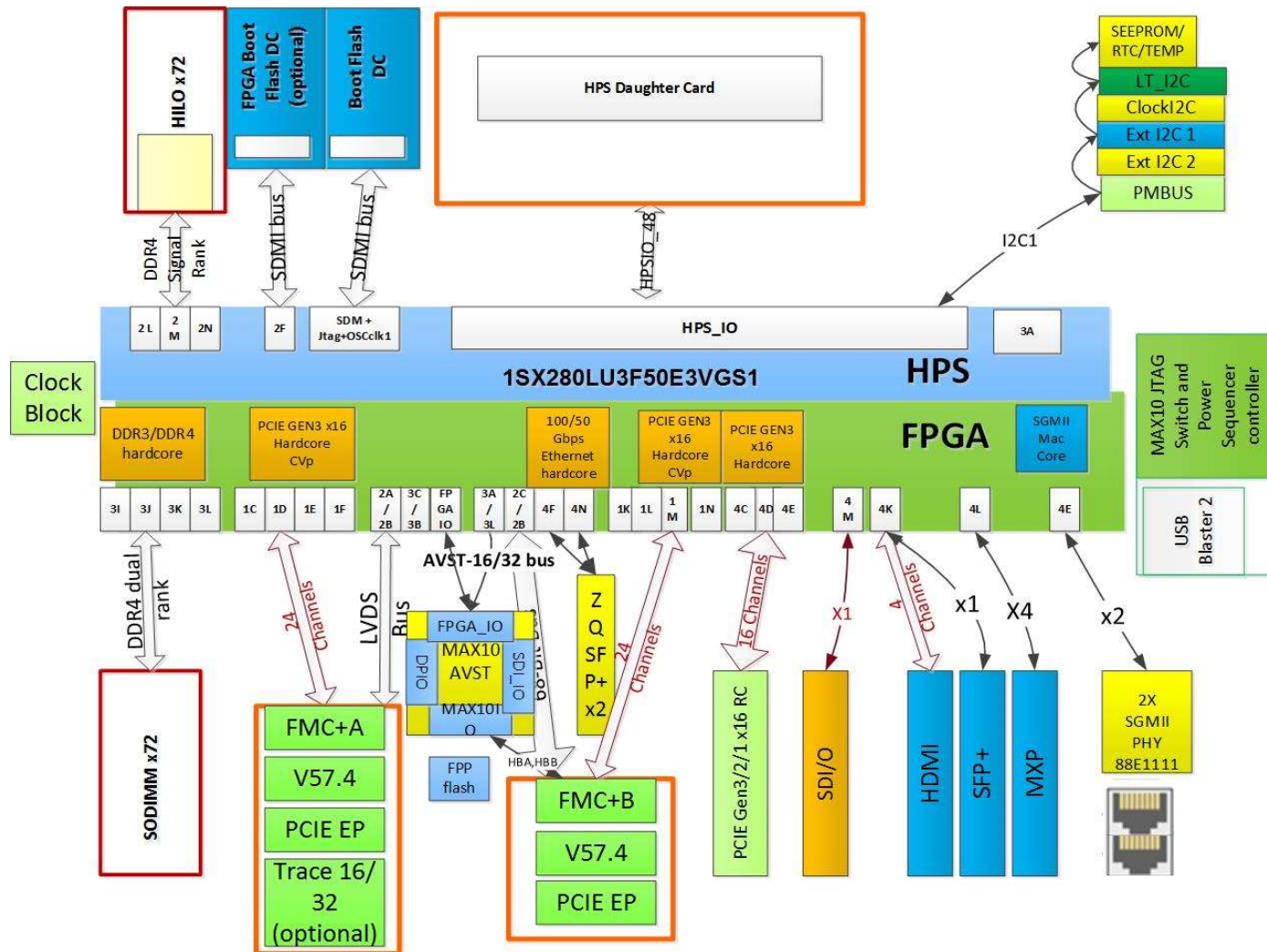
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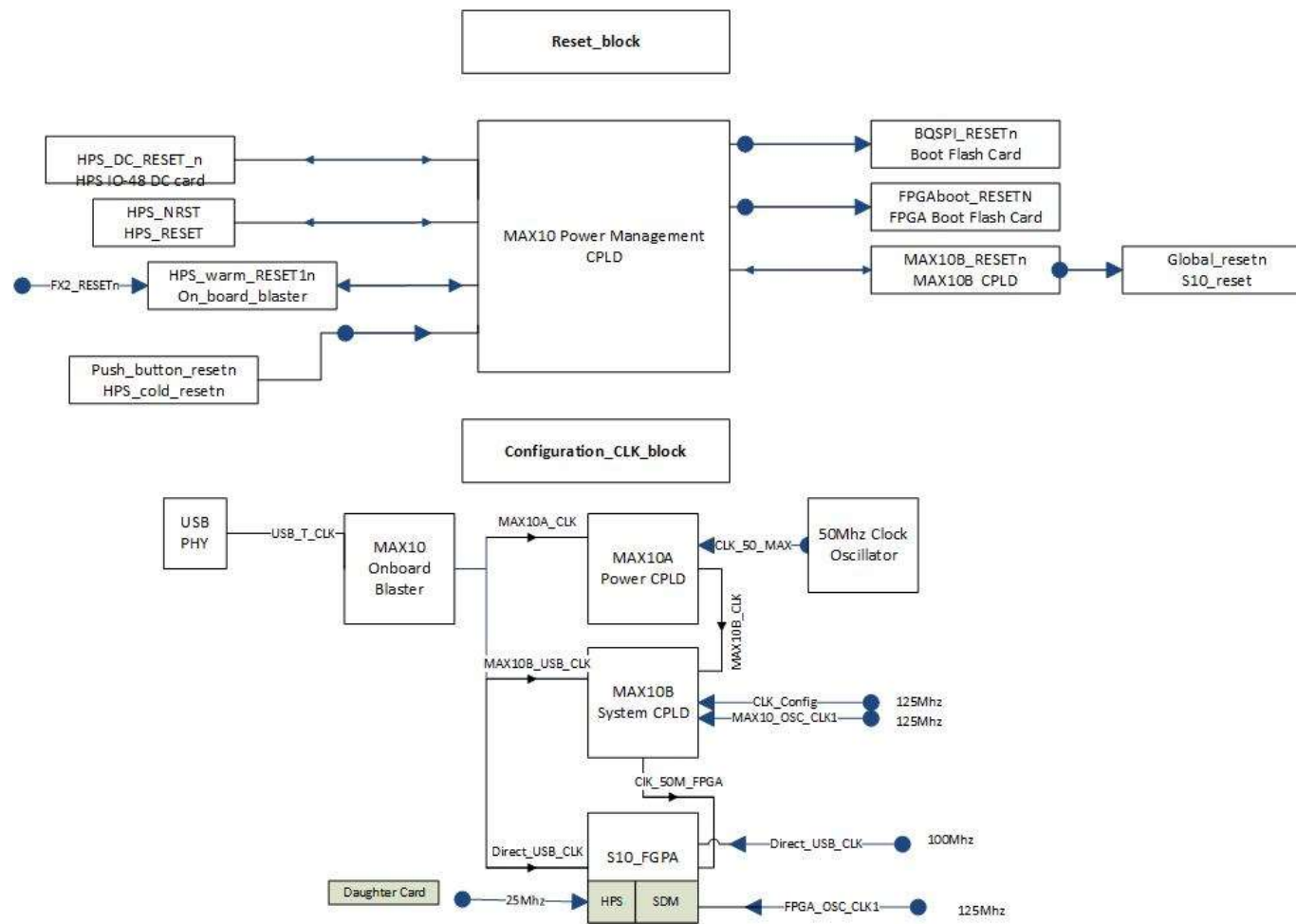
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Stratix 10 Dev Kit Block Diagram



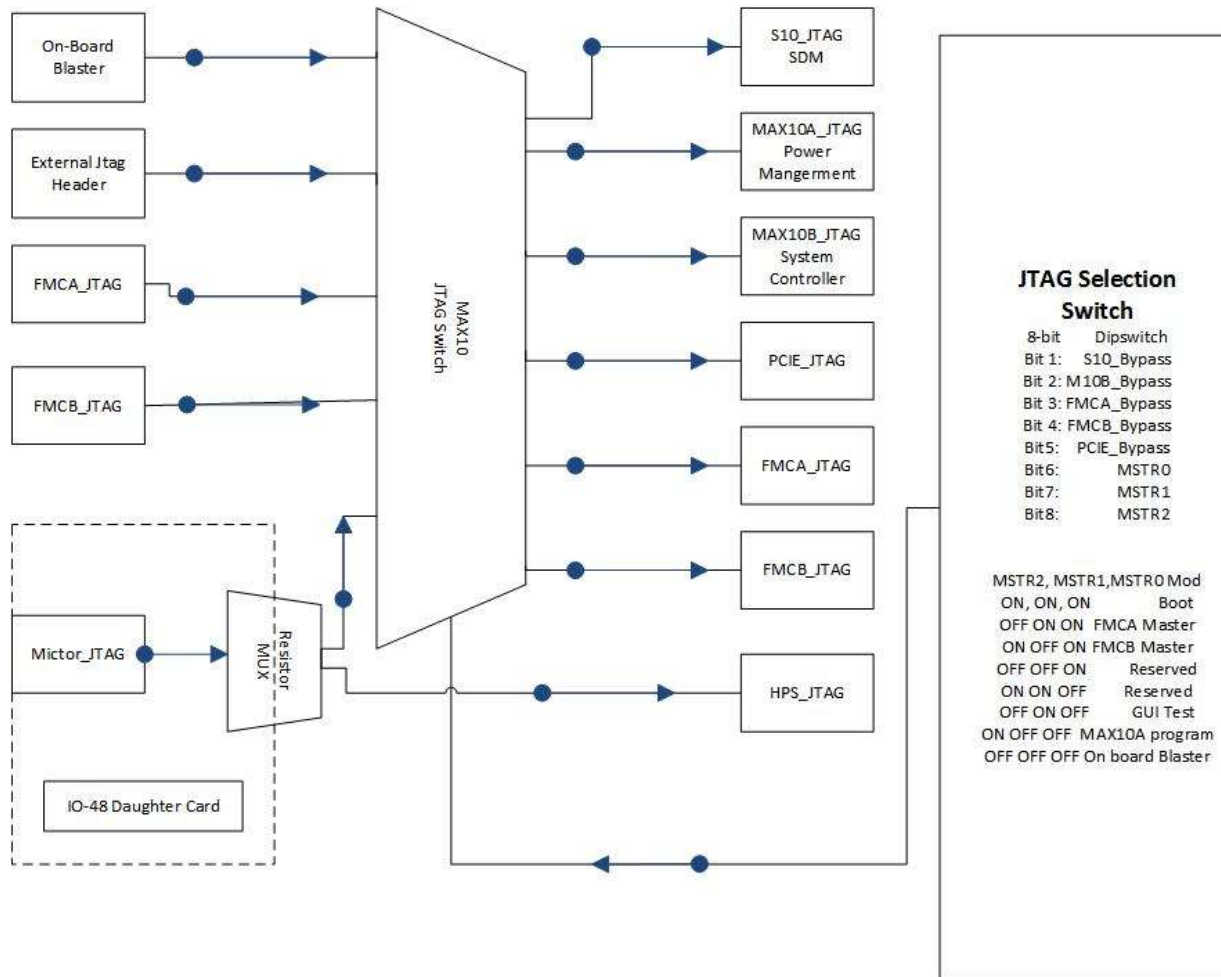
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S10soc Dev Kit Reset Block



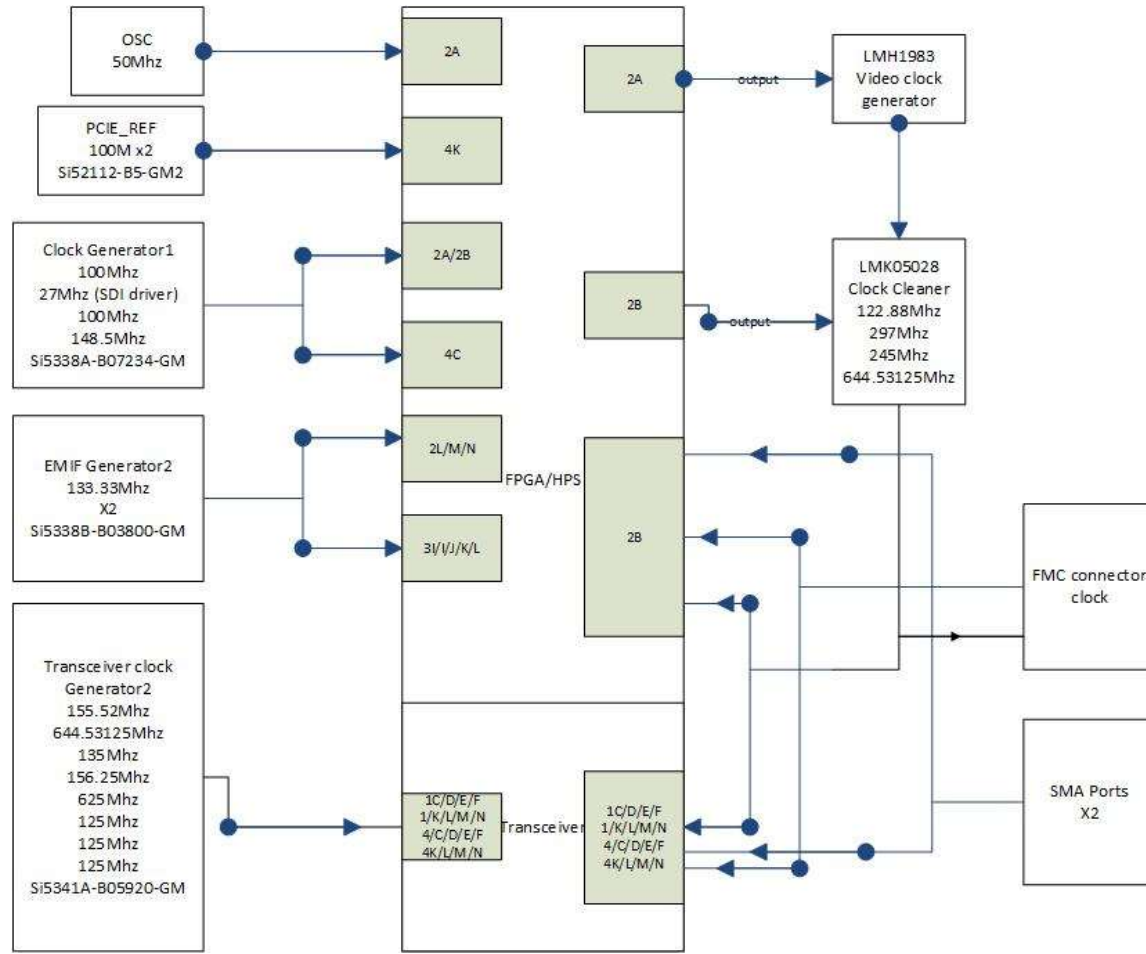
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JTAG Connection Diagram



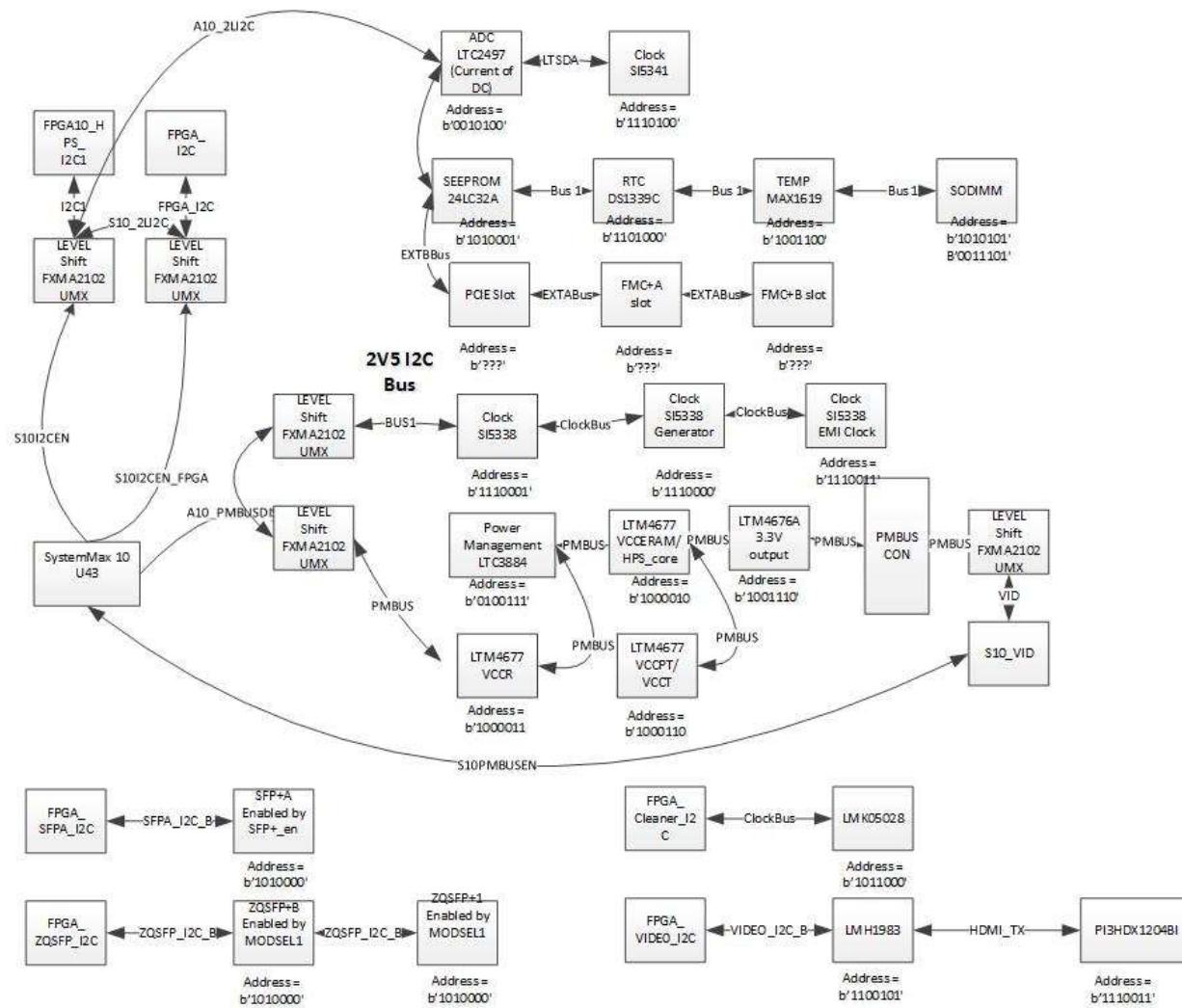
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Stratix 10 Dev Kit Clock Connection



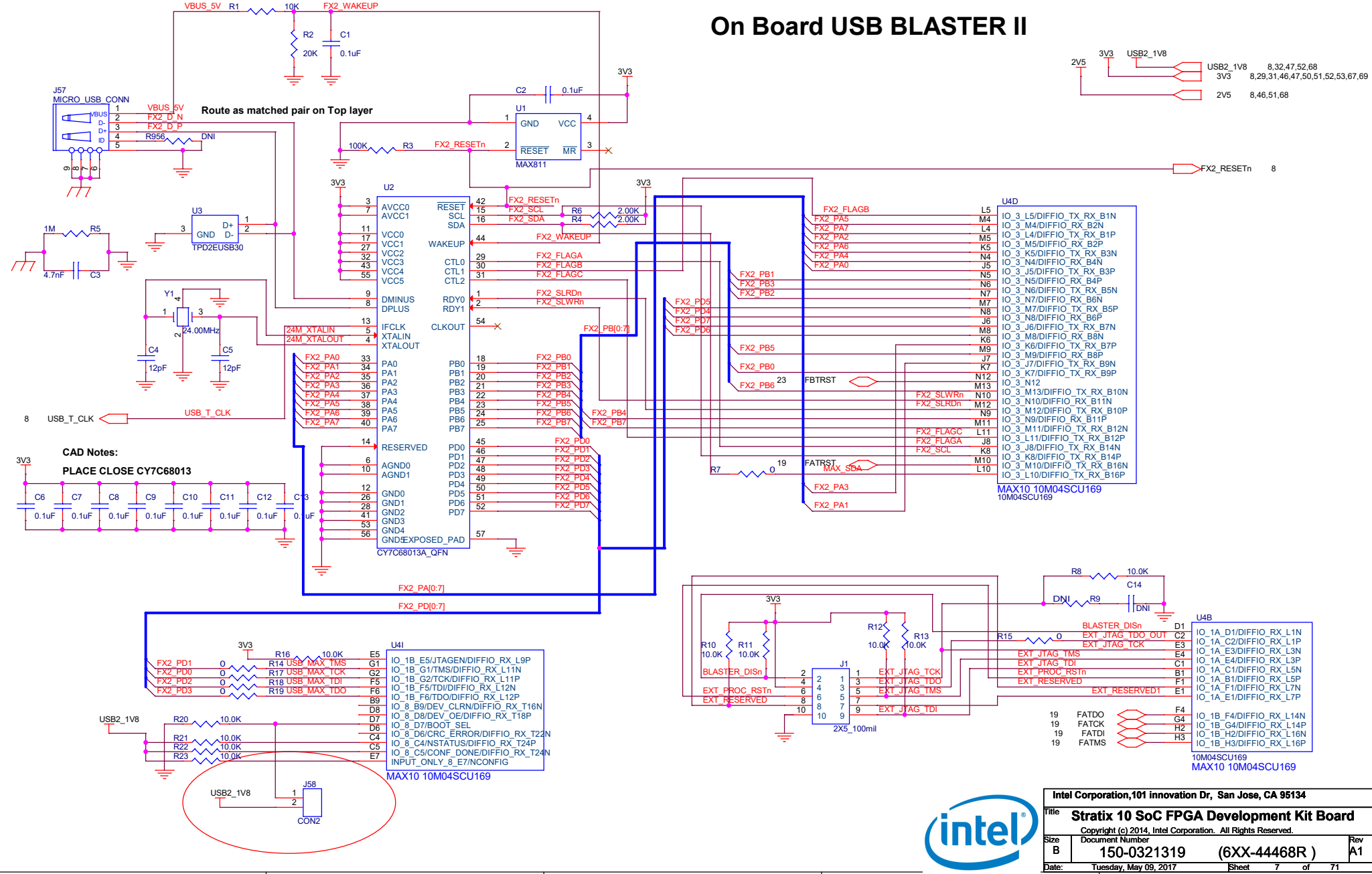
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Stratix 10 Dev Kit I2C bus Connection



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On Board USB BLASTER II



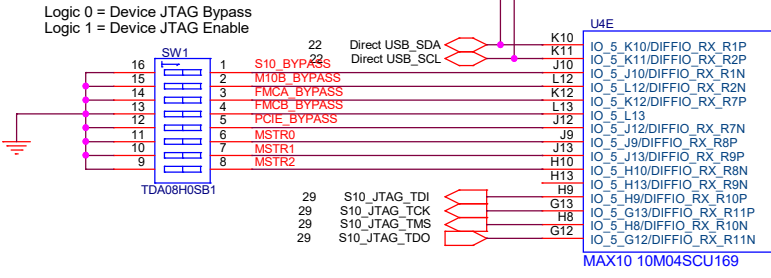
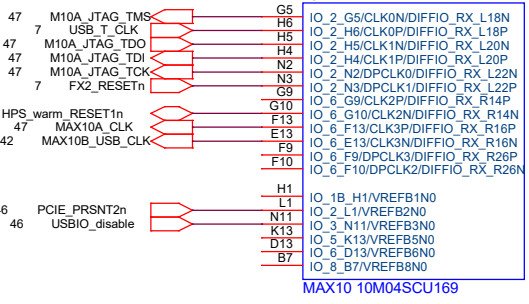
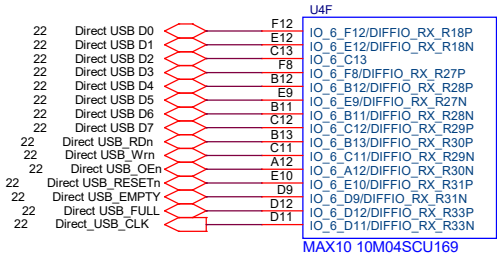
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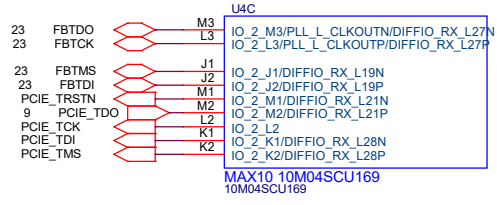
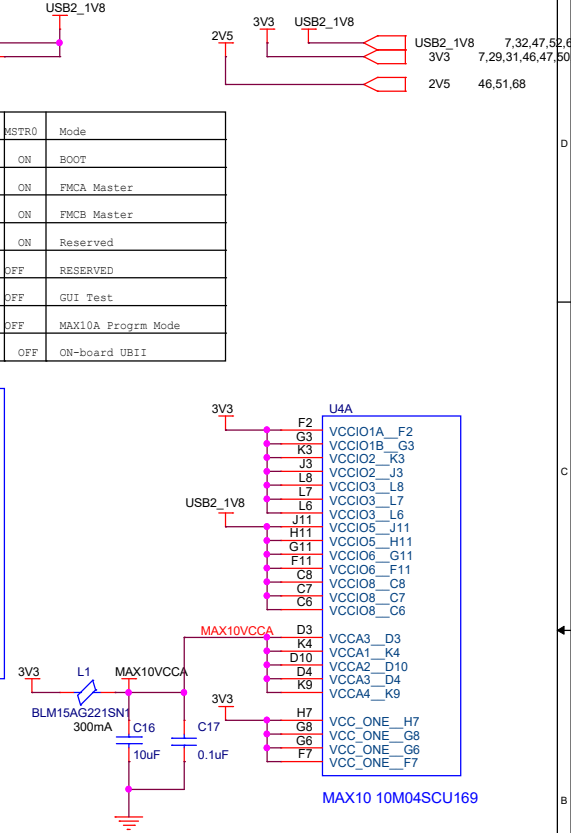
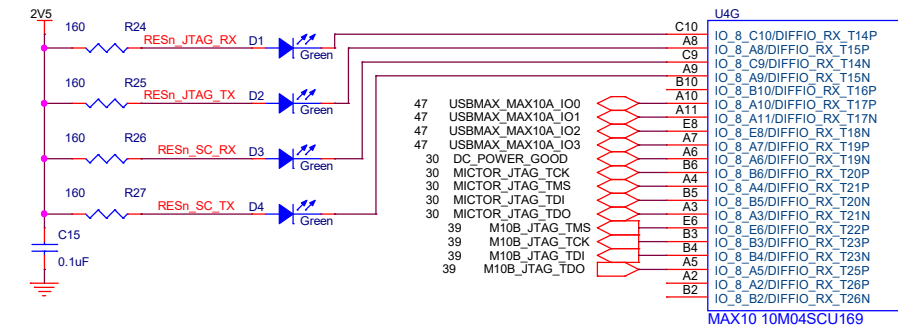
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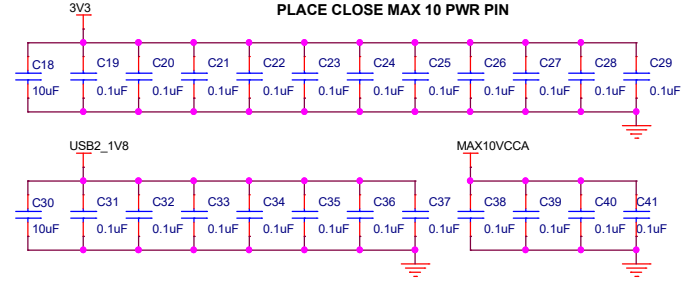
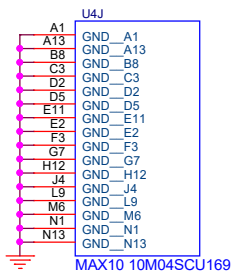
On Board USB BLASTER II 2, JTAGSwitch



MSTR2	MSTR1	MSTR0	Mode
ON	ON	ON	BOOT
OFF	ON	ON	FMCA Master
ON	OFF	ON	FMCB Master
OFF	ON	ON	Reserved
ON	ON	OFF	RESERVED
OFF	ON	OFF	GUI Test
ON	OFF	OFF	MAX10A_Program_Mode
OFF	OFF	OFF	ON-board_UBII

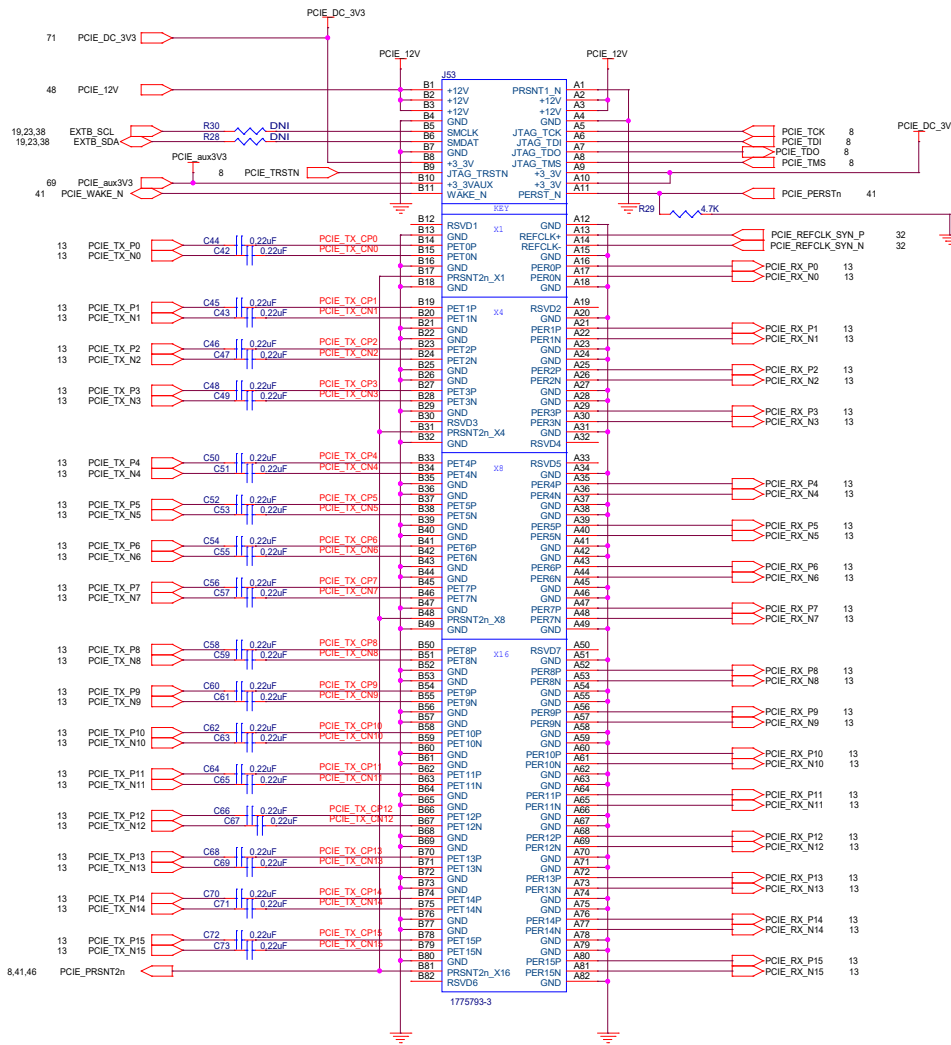


CAD Notes:
PLACE CLOSE MAX 10 PWR PIN

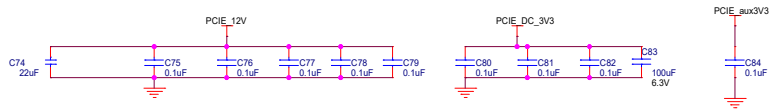


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PCI Express GEN3 X 16 Connector

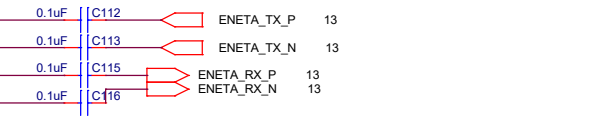
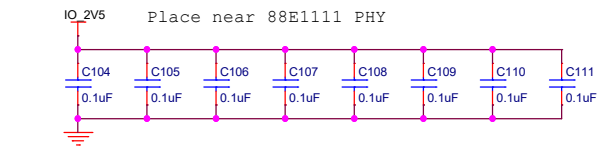
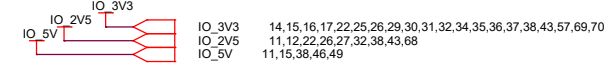


75-ohm to 100-ohm XCVR traces.

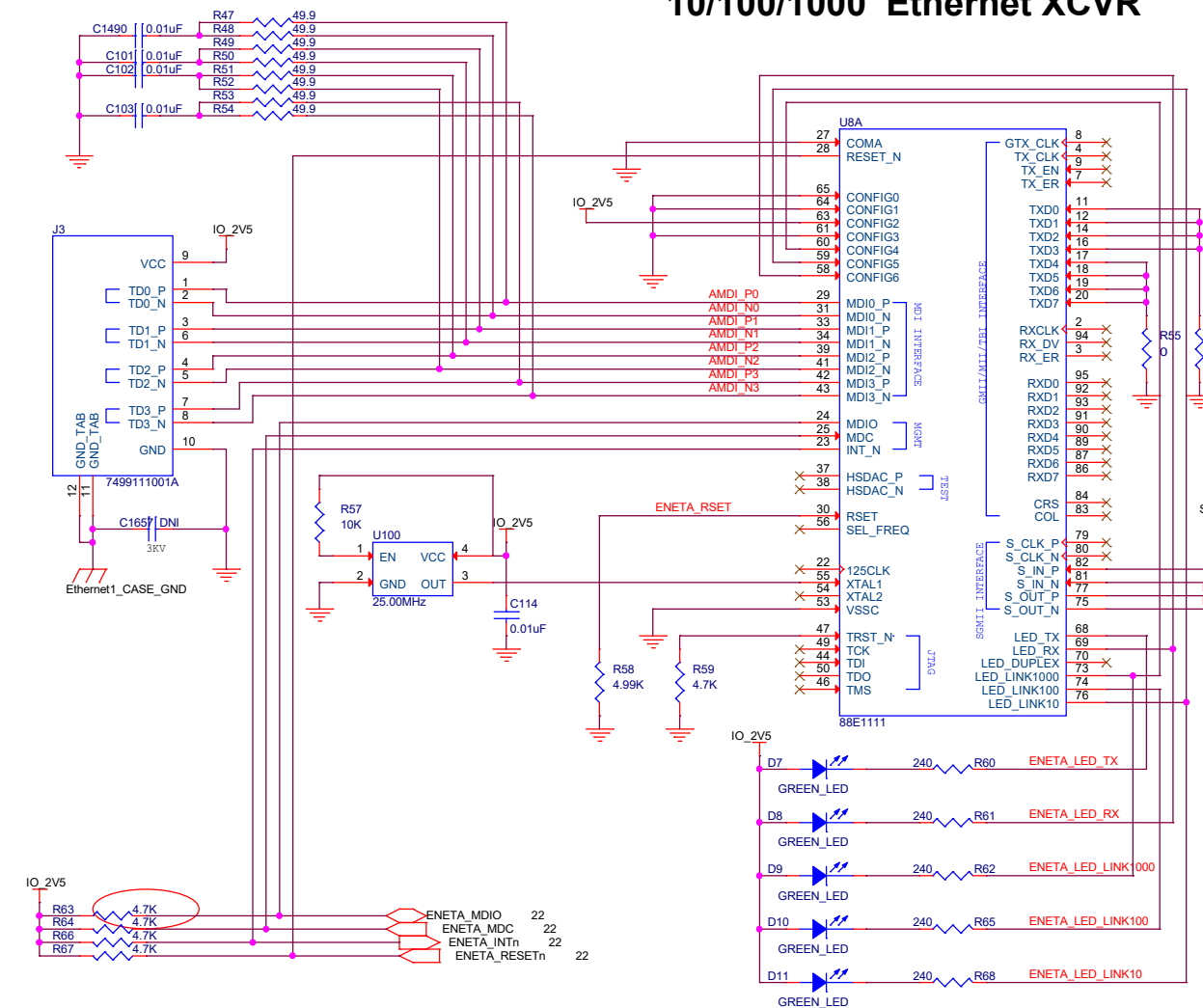
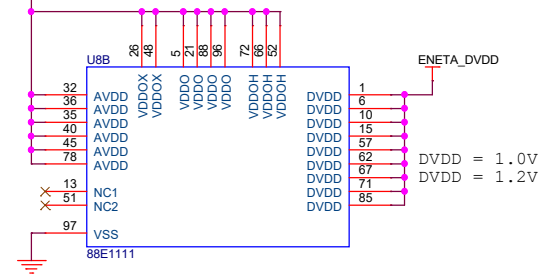


10/100/1000 Ethernet XCVR

Pin	Pin Connection	Setting Bit[2:0]	Definition
CONFIG0	GND	000	MDIO PHY Address bit (2:0) = 000
CONFIG1	GND	000	Enable Pause, PHY Address bits (4:3) = 00
CONFIG2	VDDO (2.5V or 3.3V)	111	1110 = Auto-negotiate, advertise all capabilities, prefer Master 100BASE-x FULL-DUPLEX/Auto-Negotiation enabled, 100BASE-X half-duplex
CONFIG3	GND	000	Disable crossover, Enable 125CLK
CONFIG4	LED_LINK1000	100	Hardware Config Mode Reg (2:0) = 100 SGMII without Clock with SGMII Auto-Neg to copper
CONFIG5	LED_LIN10	110	Disable fiber/copper autoselect, disable sleep mode (enable energy detect), Hardware Config Mode Reg (3) = 0
CONFIG6	LED_RX	010	Select MDIO (over 2-wire serial), interrupt polarity = active low, 50-ohm termination for fiber



88E1111-B2-CAA1C000 EOL
88E1111-B2-NDC2C000 Replacement



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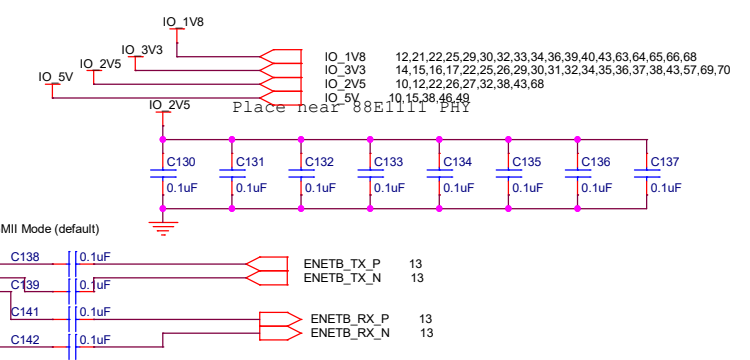
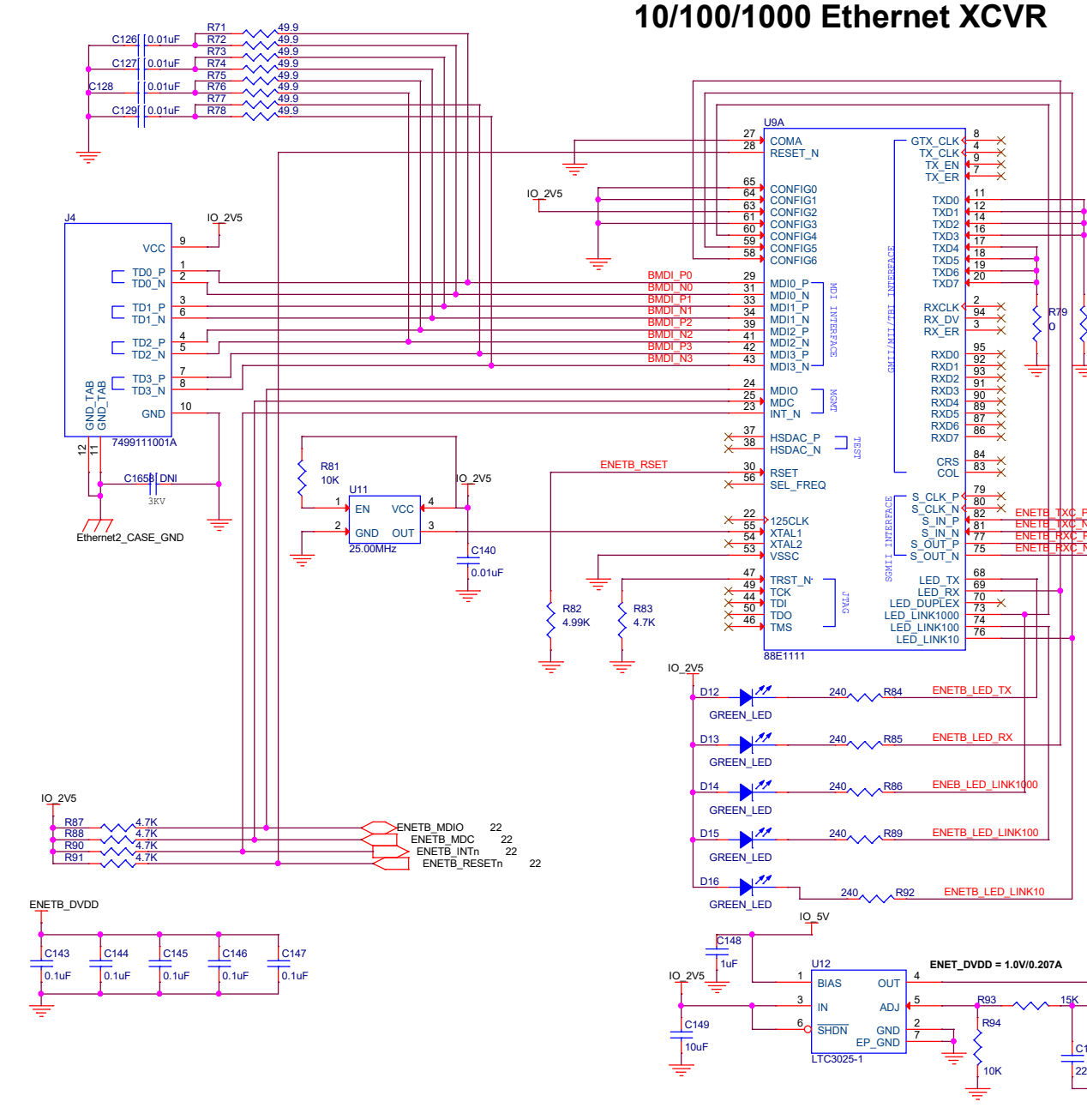
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88E1111-B2-CAA1C000 EOL
88E1111-B2-NDC2C000 Replacement



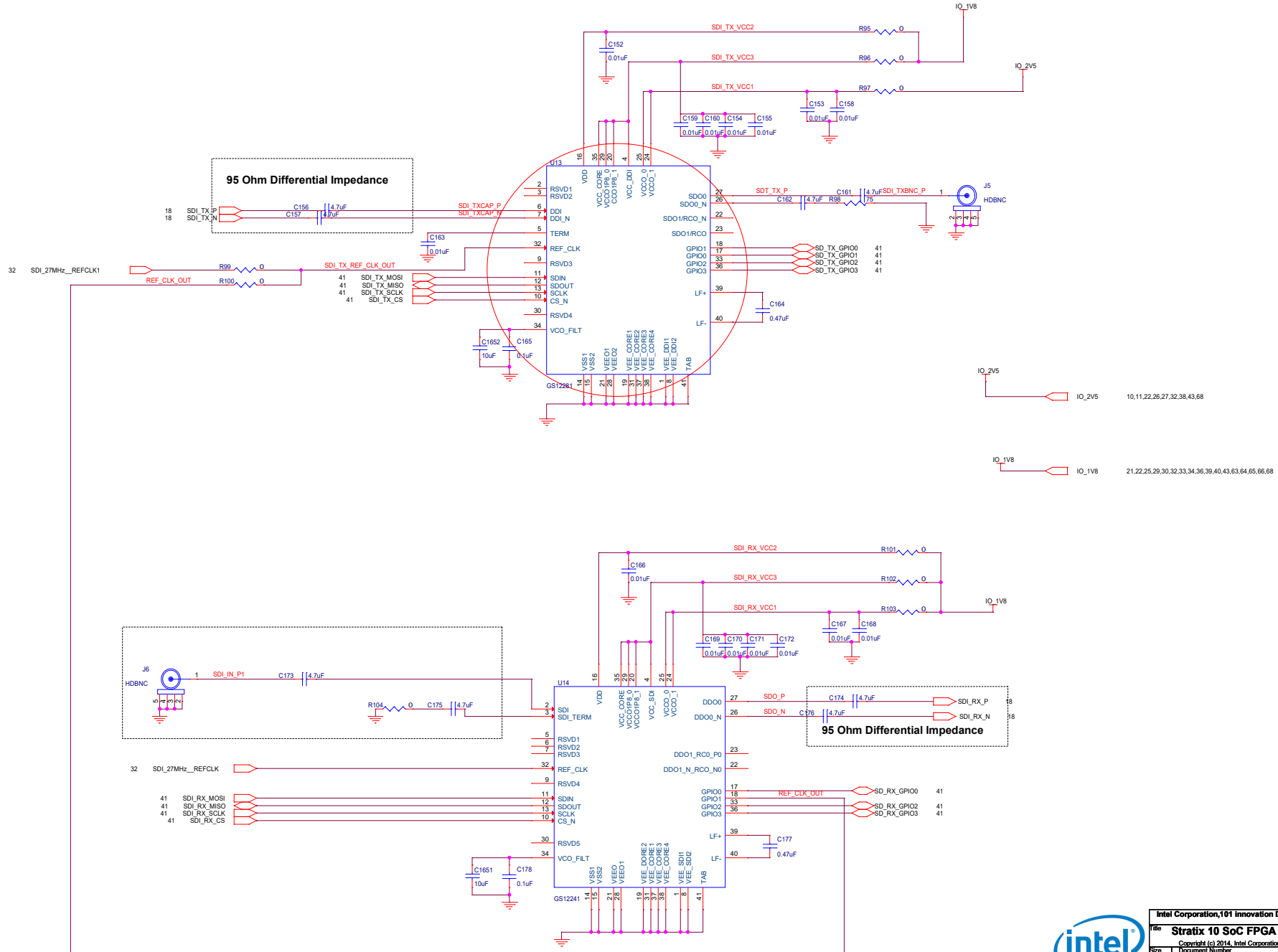
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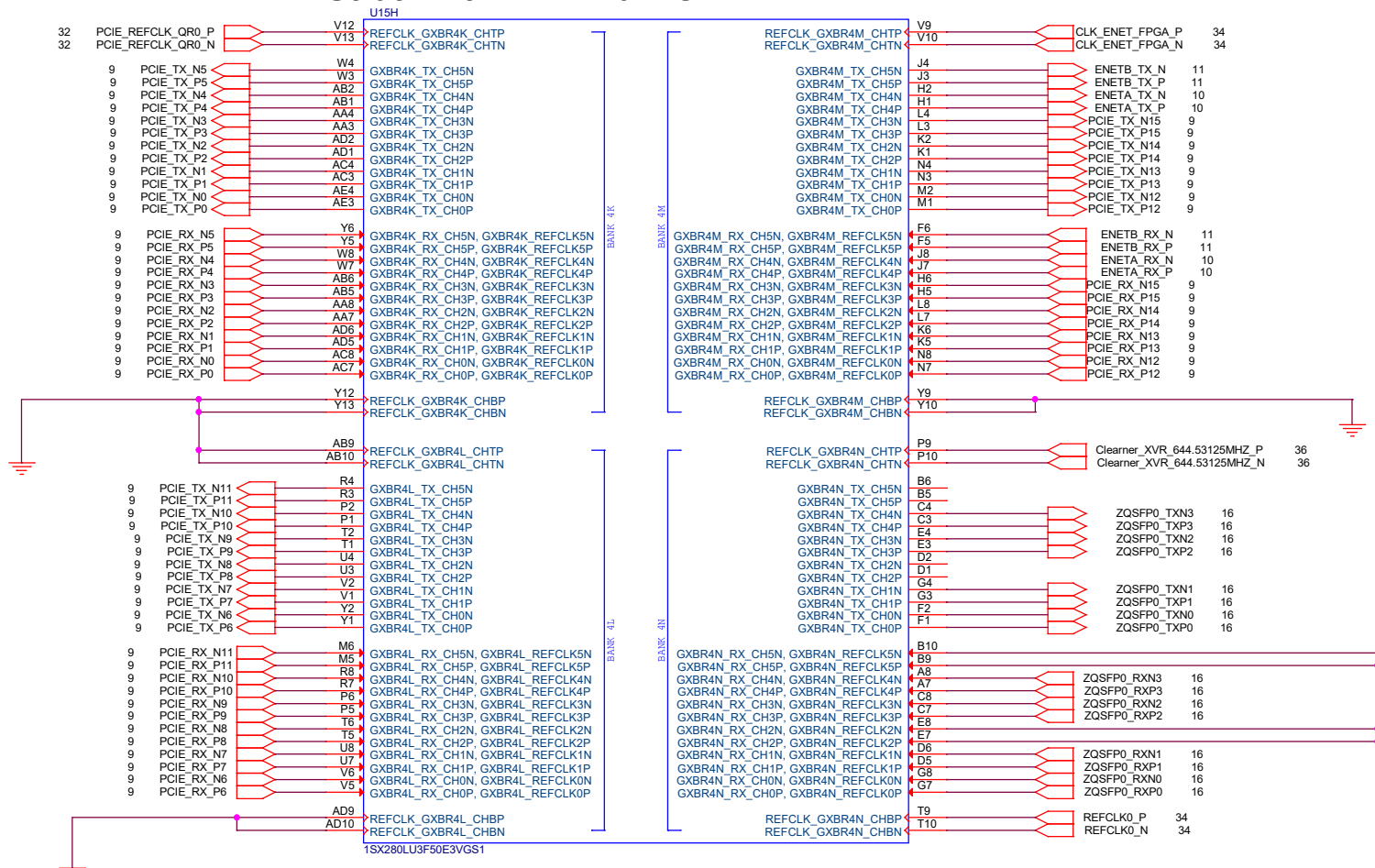
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SDI Cable Driver, Equalizer, and SMB

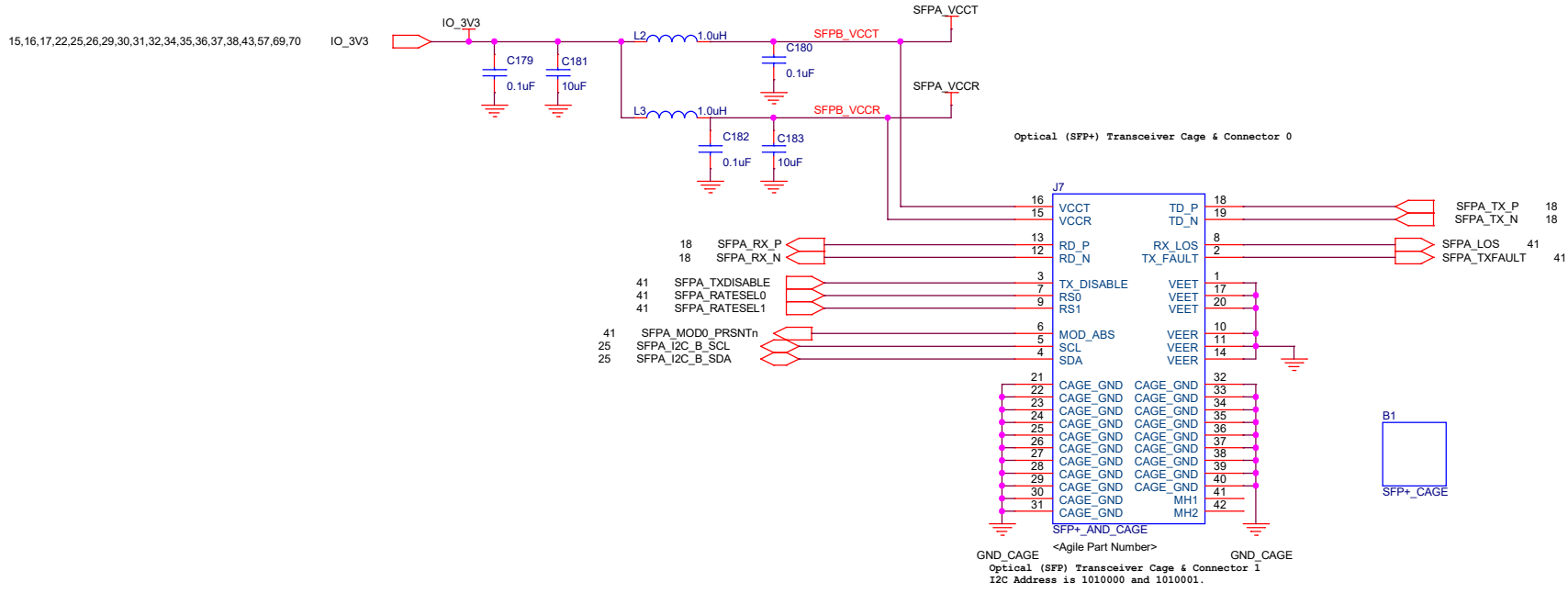


Stratix 10 XCVR Banks - 4K/L/M/N



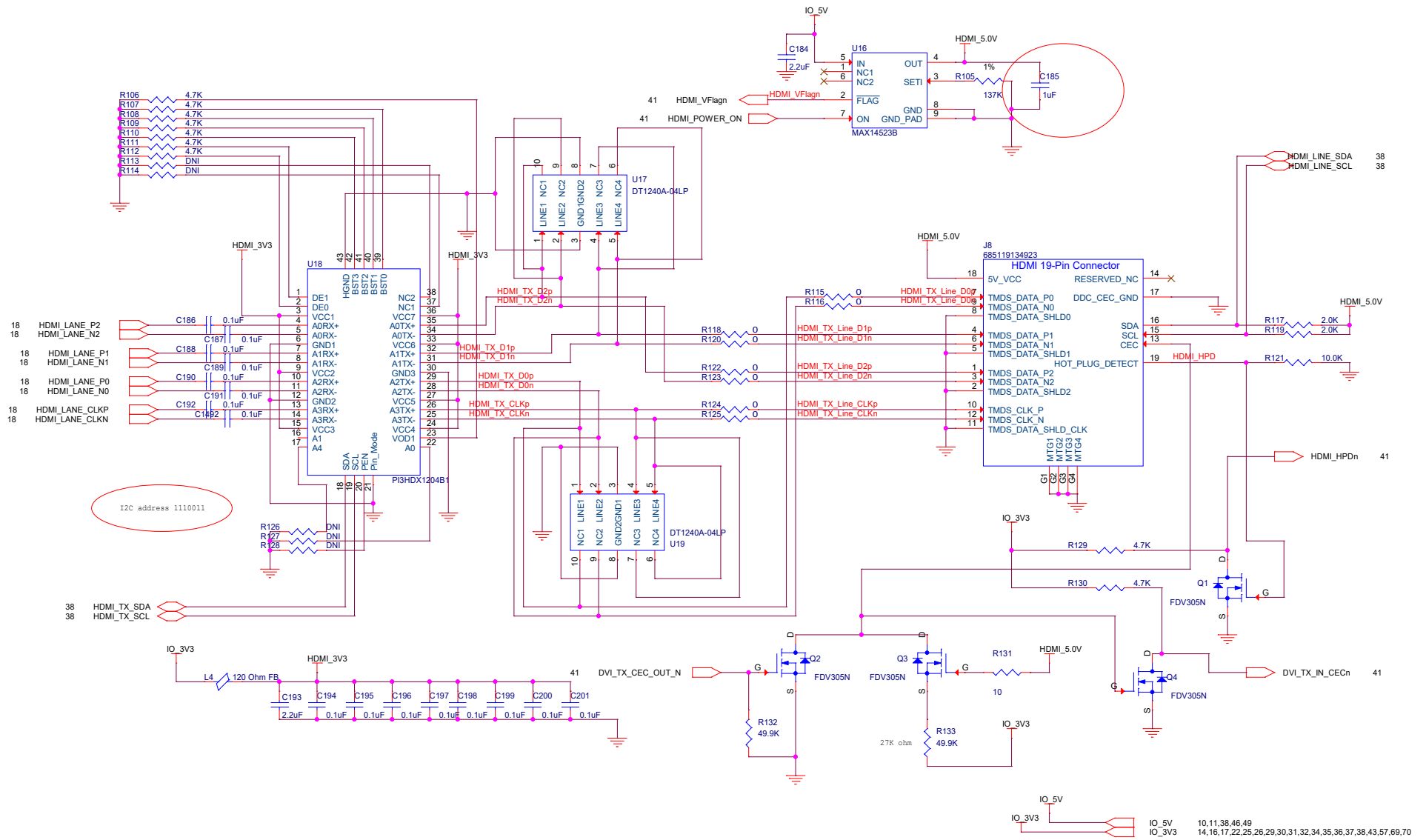
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Small Form Factor Pluggable Plus (SFP+) Port A



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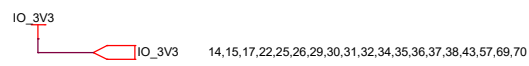
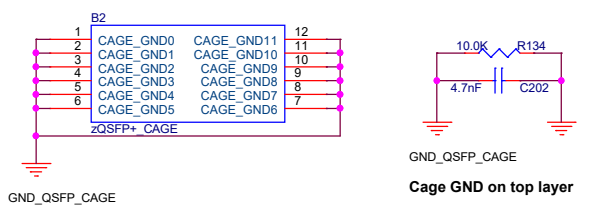
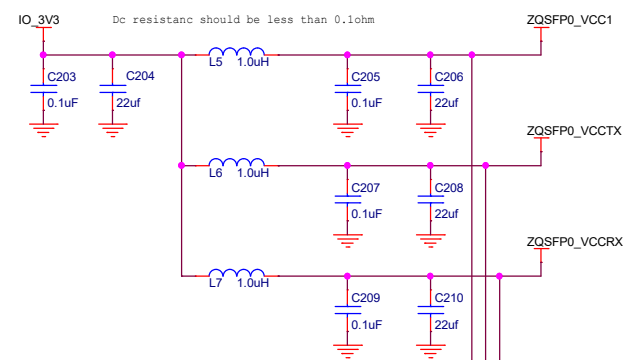
HDMI (VIDEO ONLY)



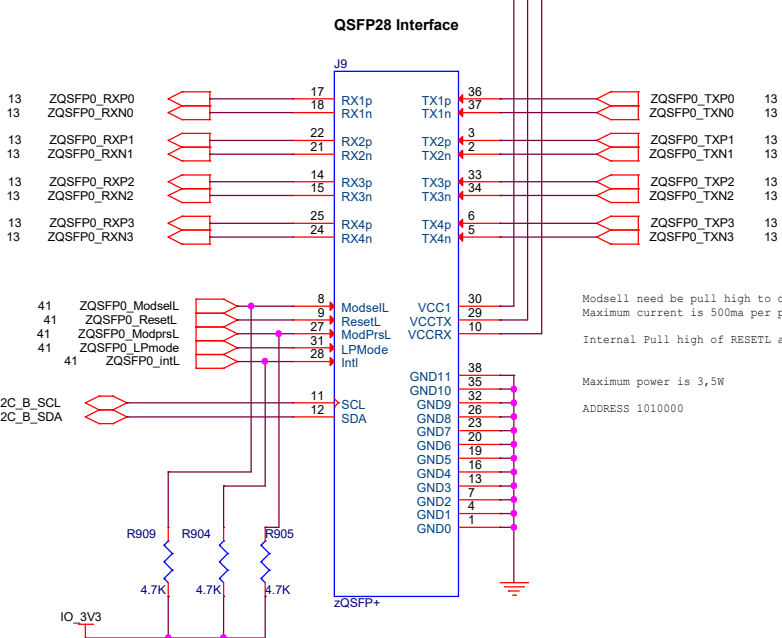
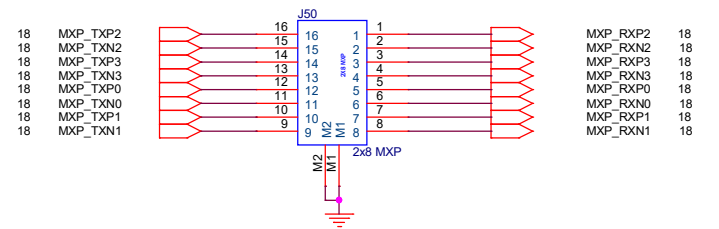
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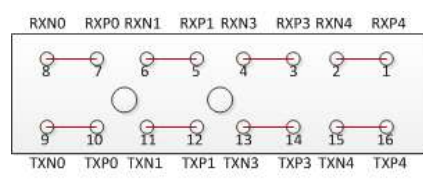
QSFP28 Interface 0 & MXP Cable connection



P and N can be swapped for better SI performance

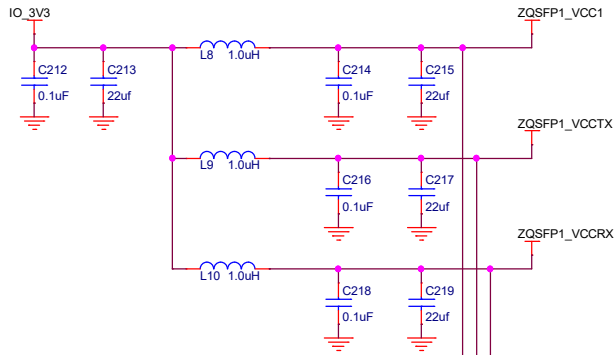


Modsell need be pull high to disabel I2C bus
 Maximum current is 500ma per pin
 Internal Pull high of RESETL and LPMode
 Maximum power is 3,5W
 ADDRESS 1010000

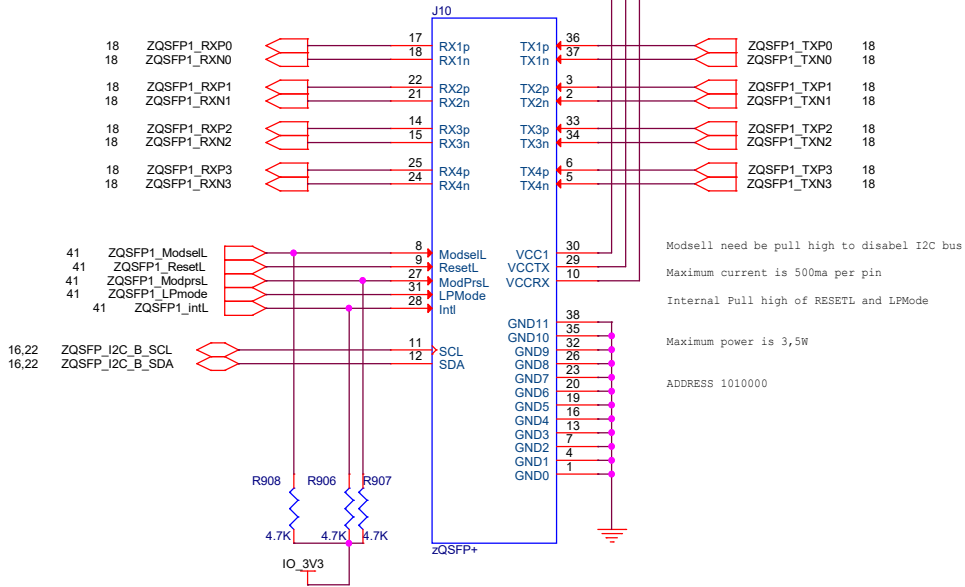


QSFP28 Interface 1

Dc resistanc should be less than 0.1ohm

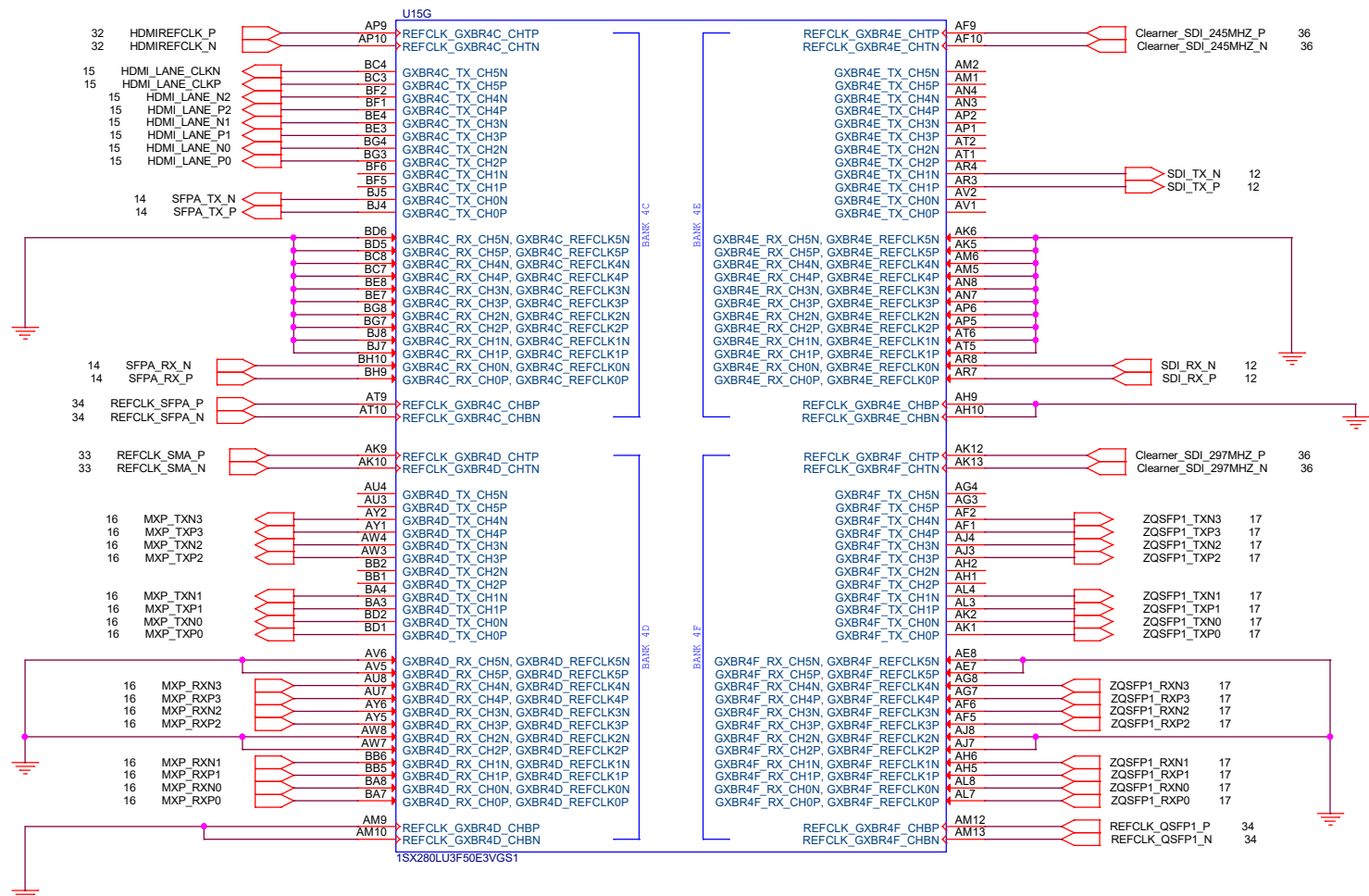


QSFP28 Interface



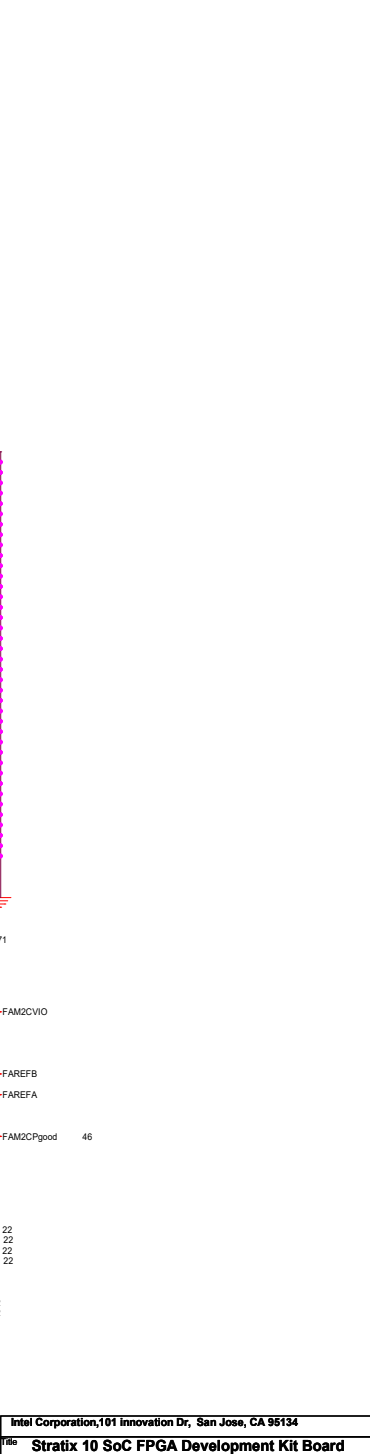
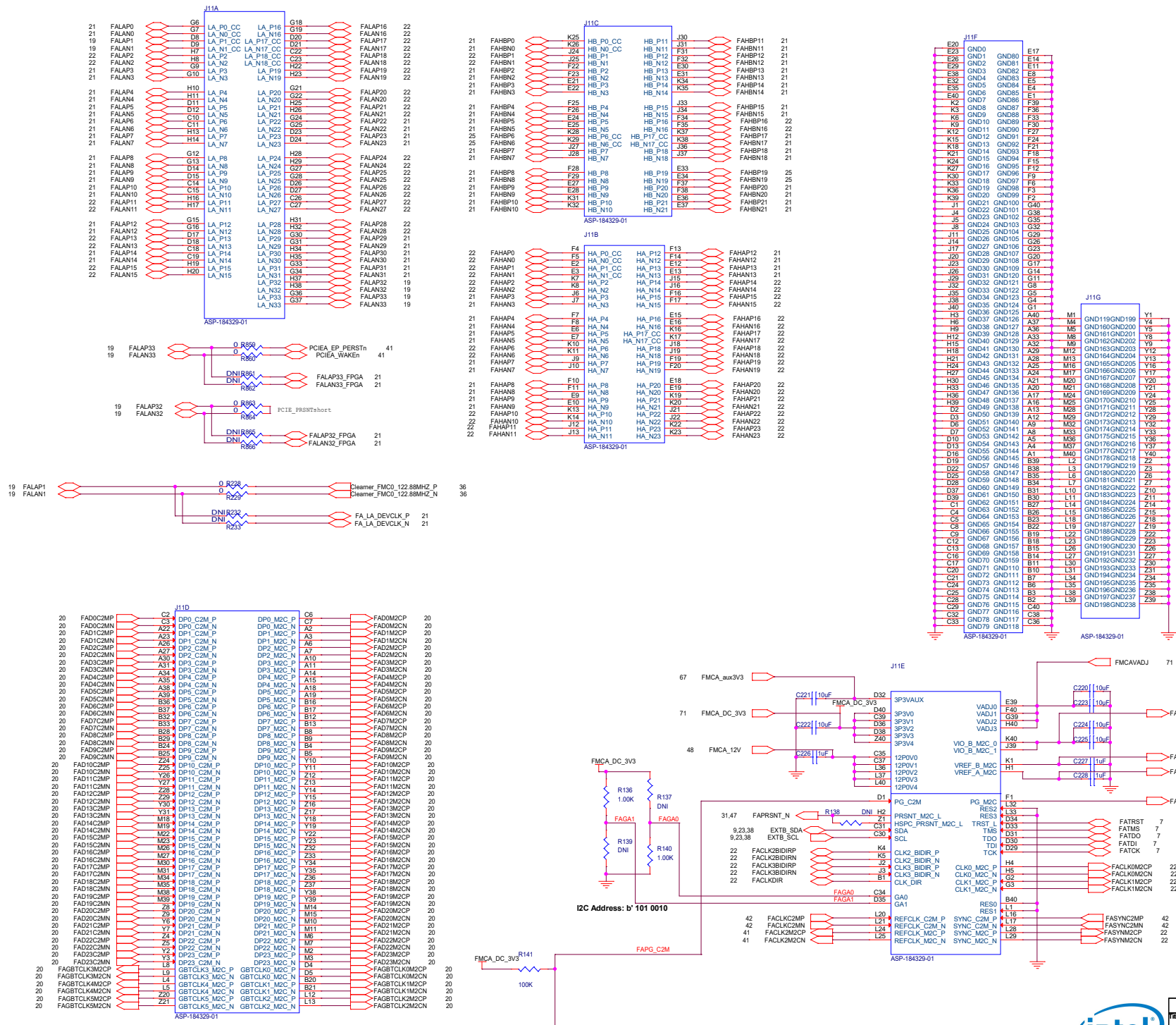
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S10 XCVR Banks - 4C/D/E/F

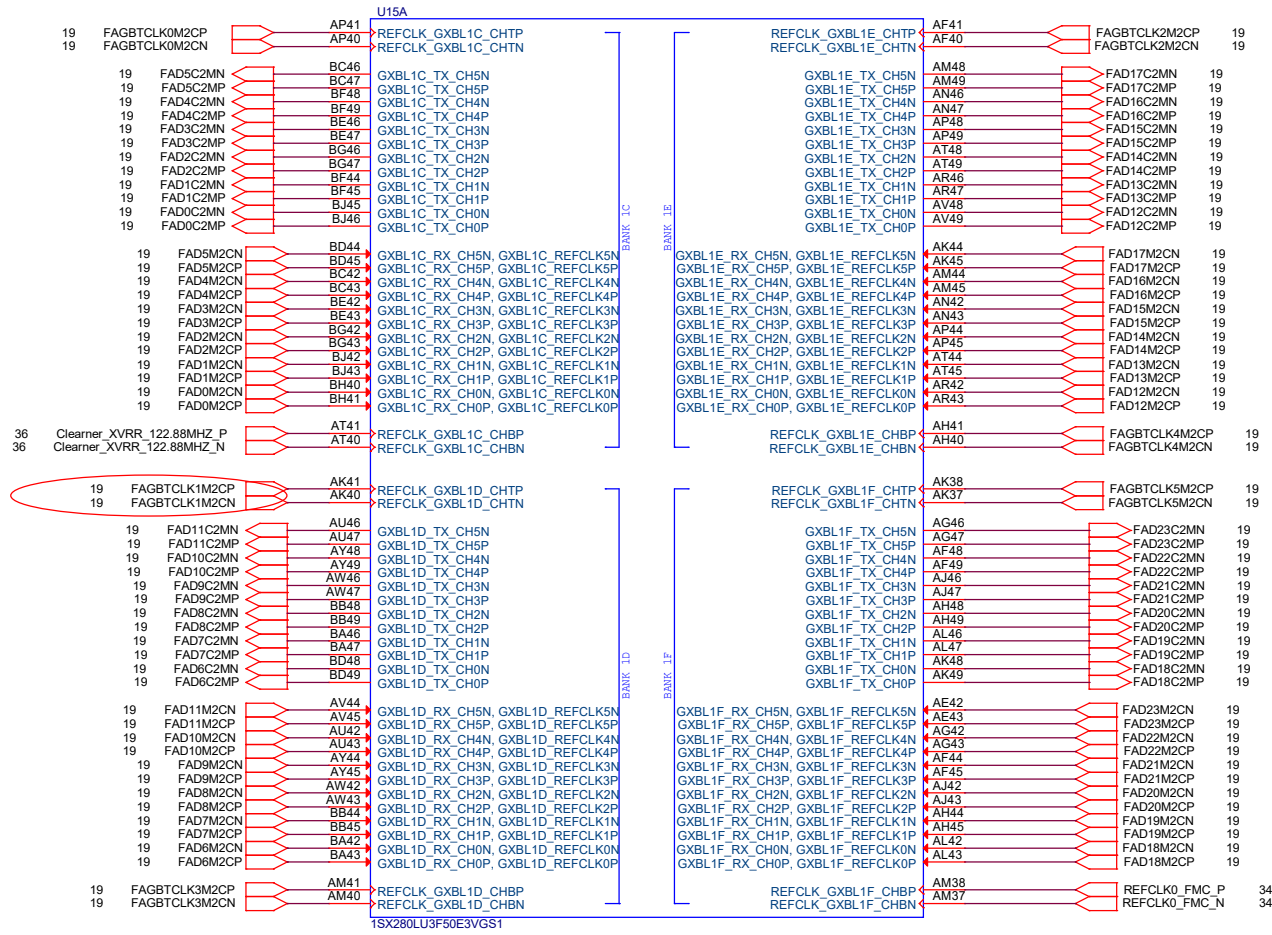


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FMC Port A

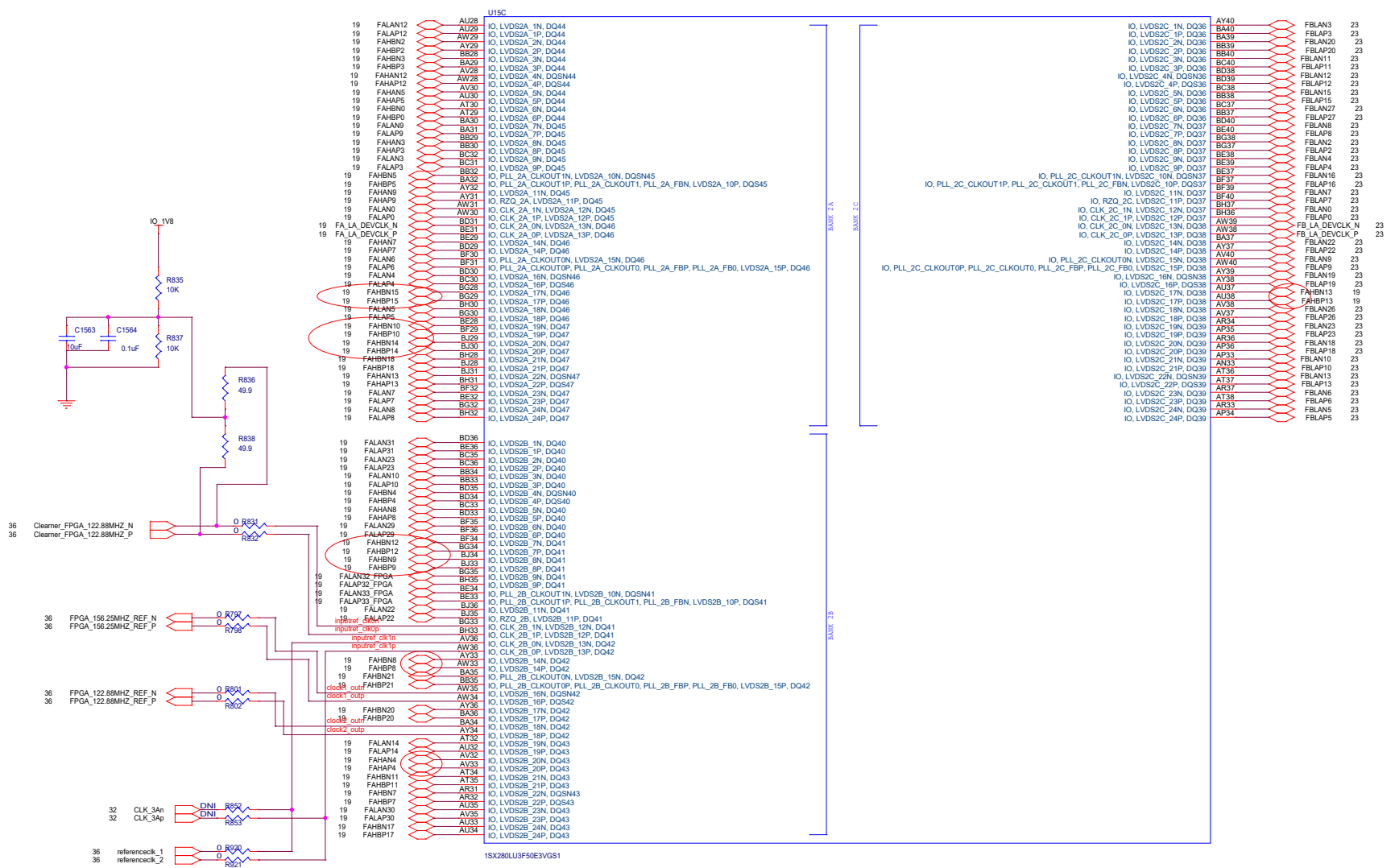


Stratix 10 XCVR Banks - 1C/D/E/F

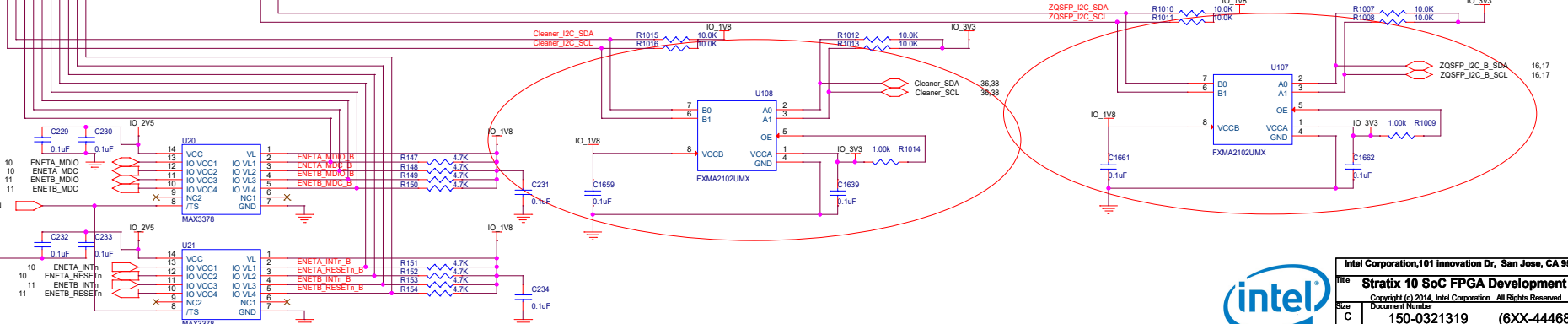
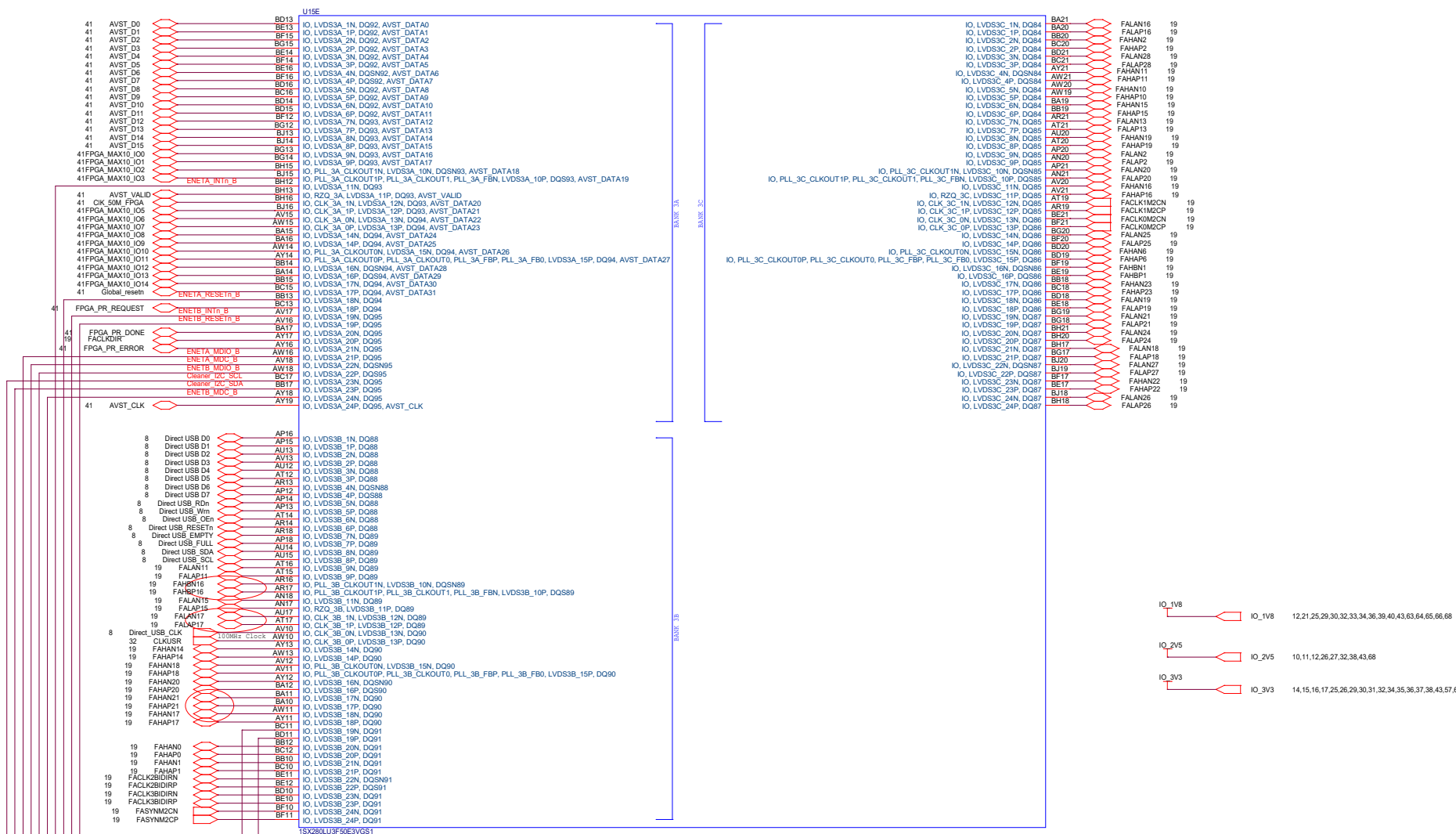


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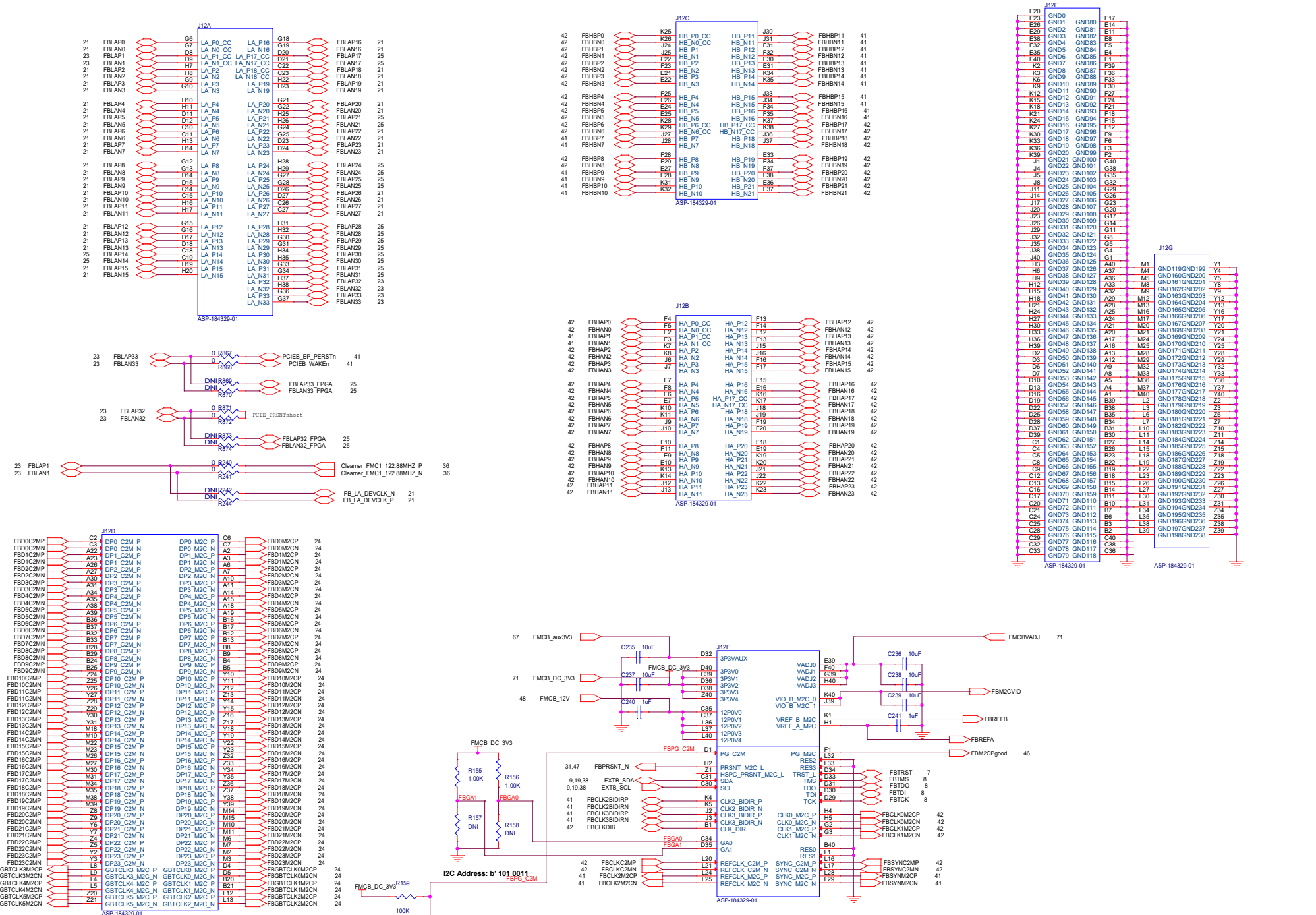
Stratix 10 Banks 2 A/B/C



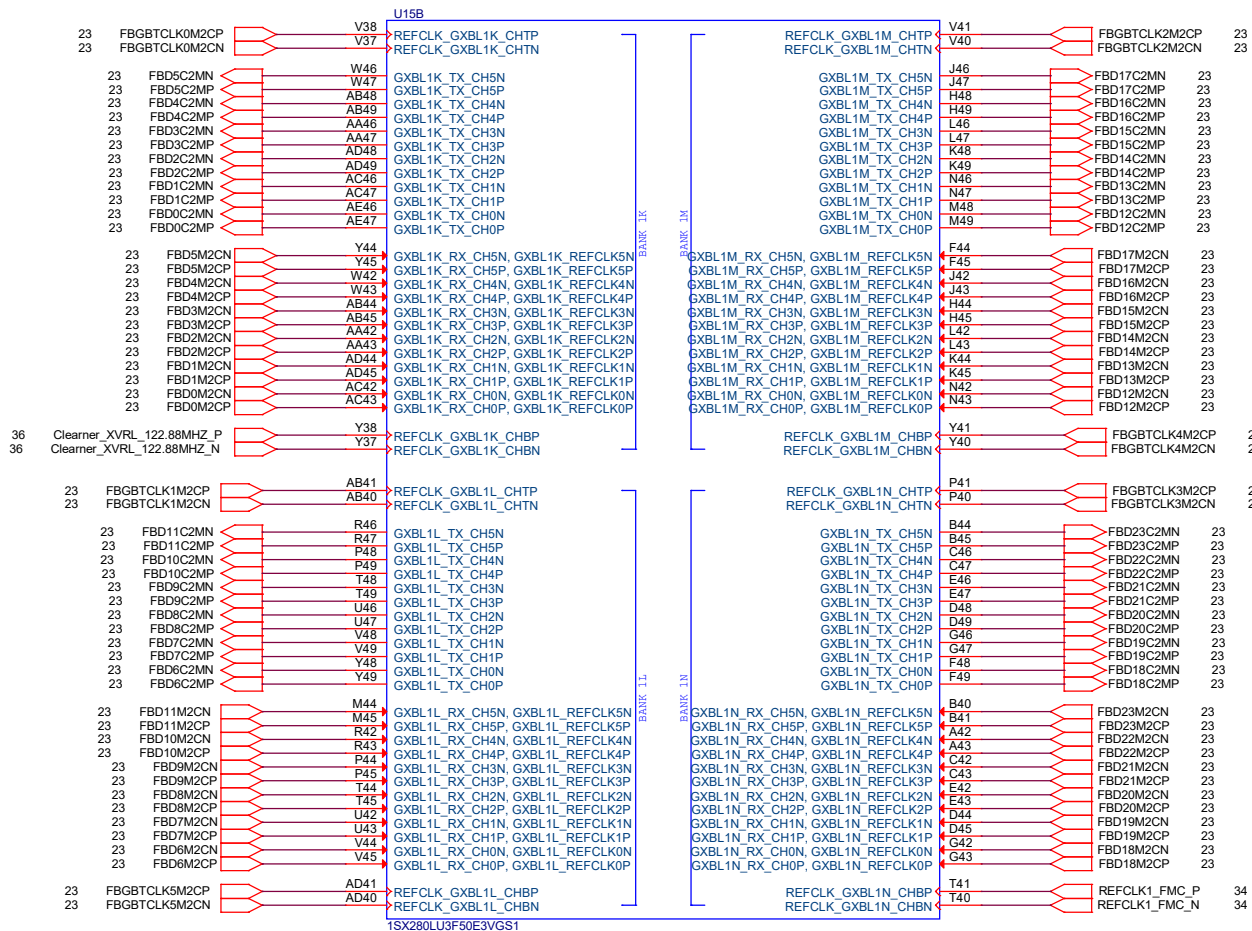
Stratix 10 Banks - 3 A/B/C



FMC Port B

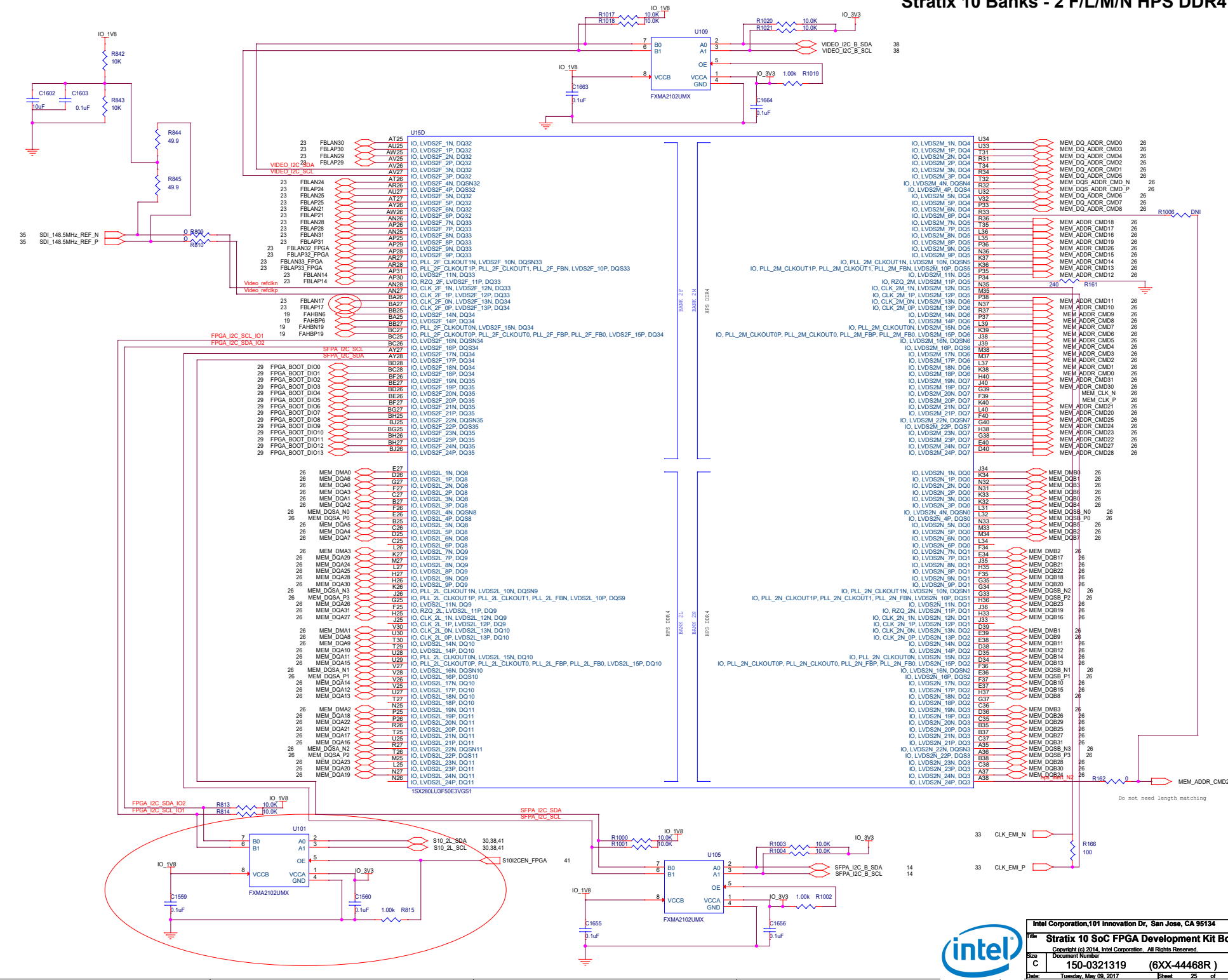


Stratix 10 XCVR Banks - 1K/L/M/N



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Stratix 10 Banks - 2 F/L/M/N HPS DDR4



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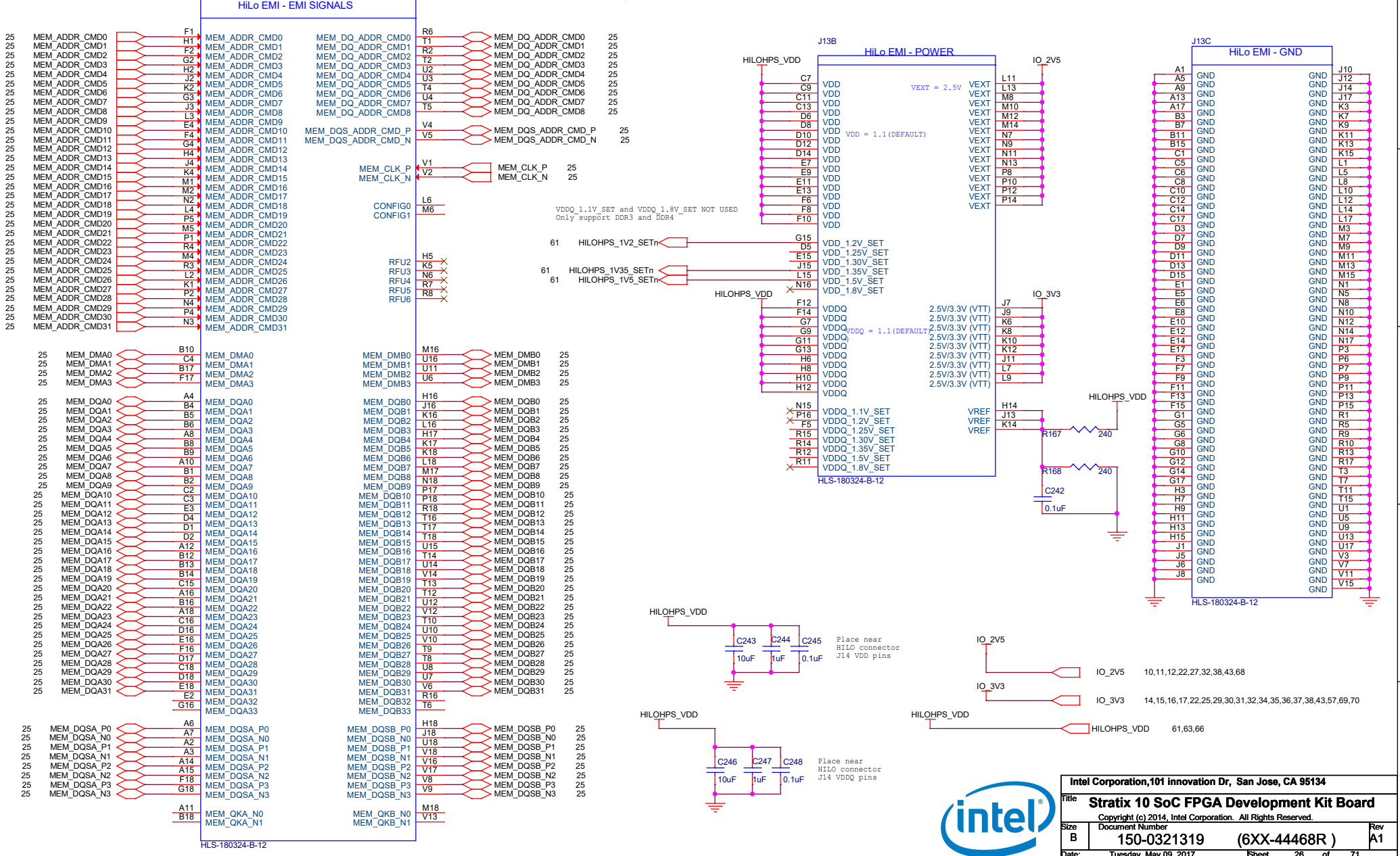
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Do not need length matching

MEM_ADDR_CMD29

External Memory Interface - HiLo connector



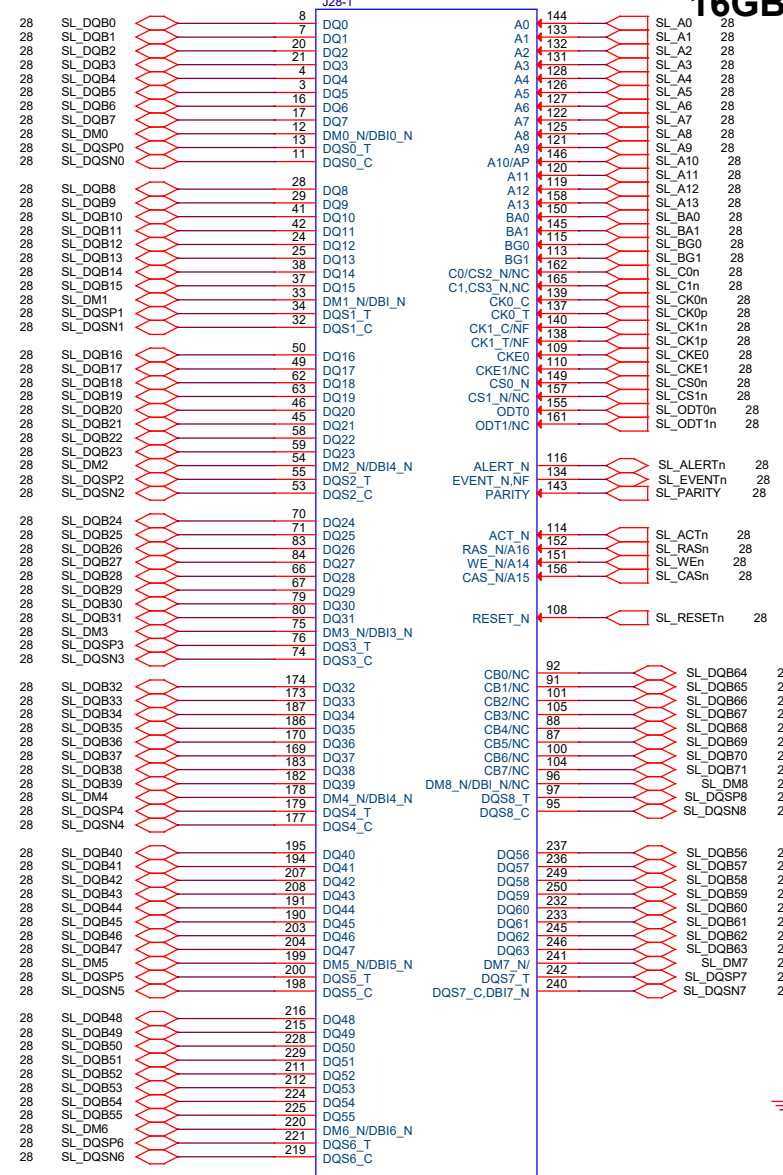
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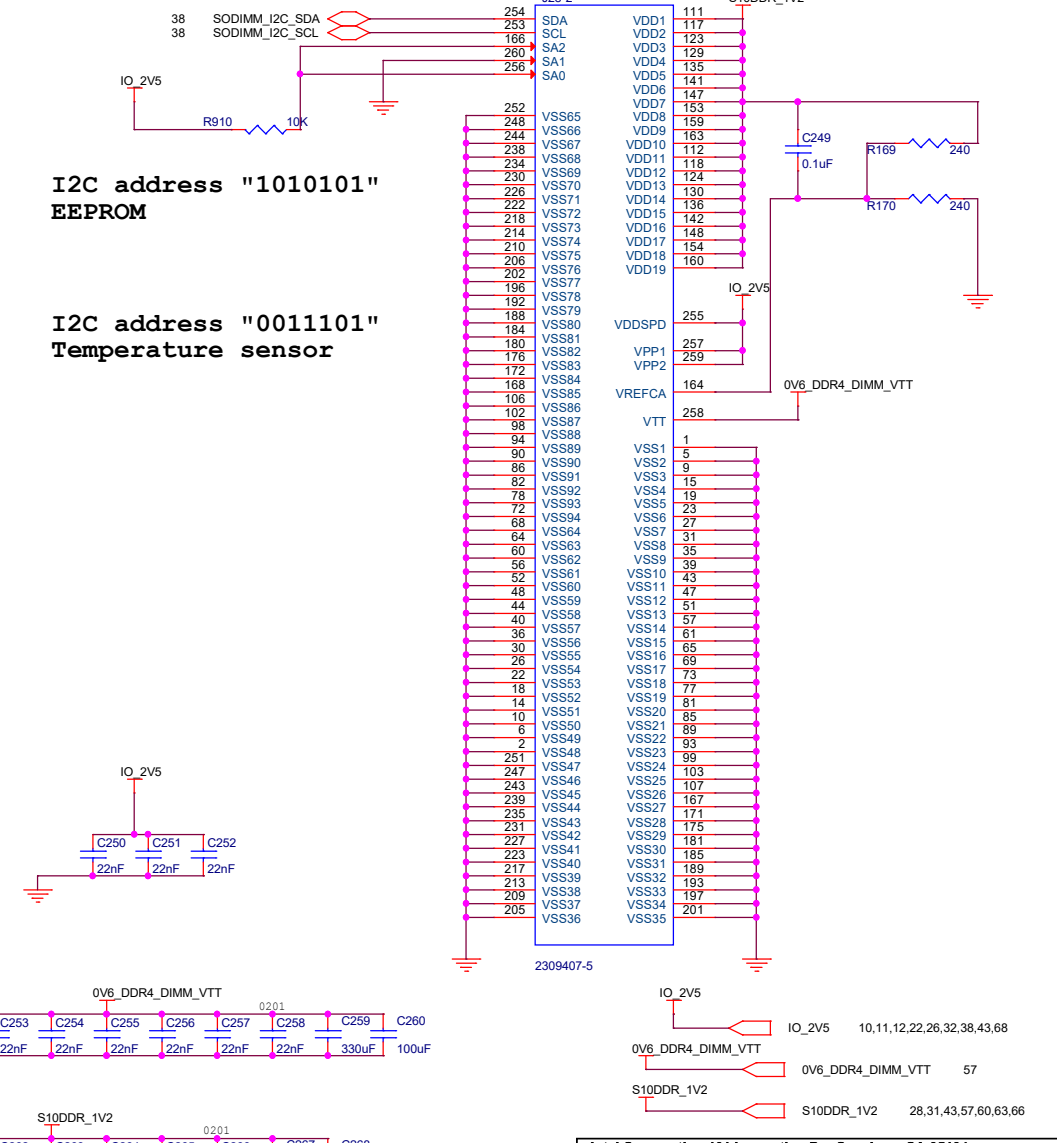
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16GB DDR4 SODIMM



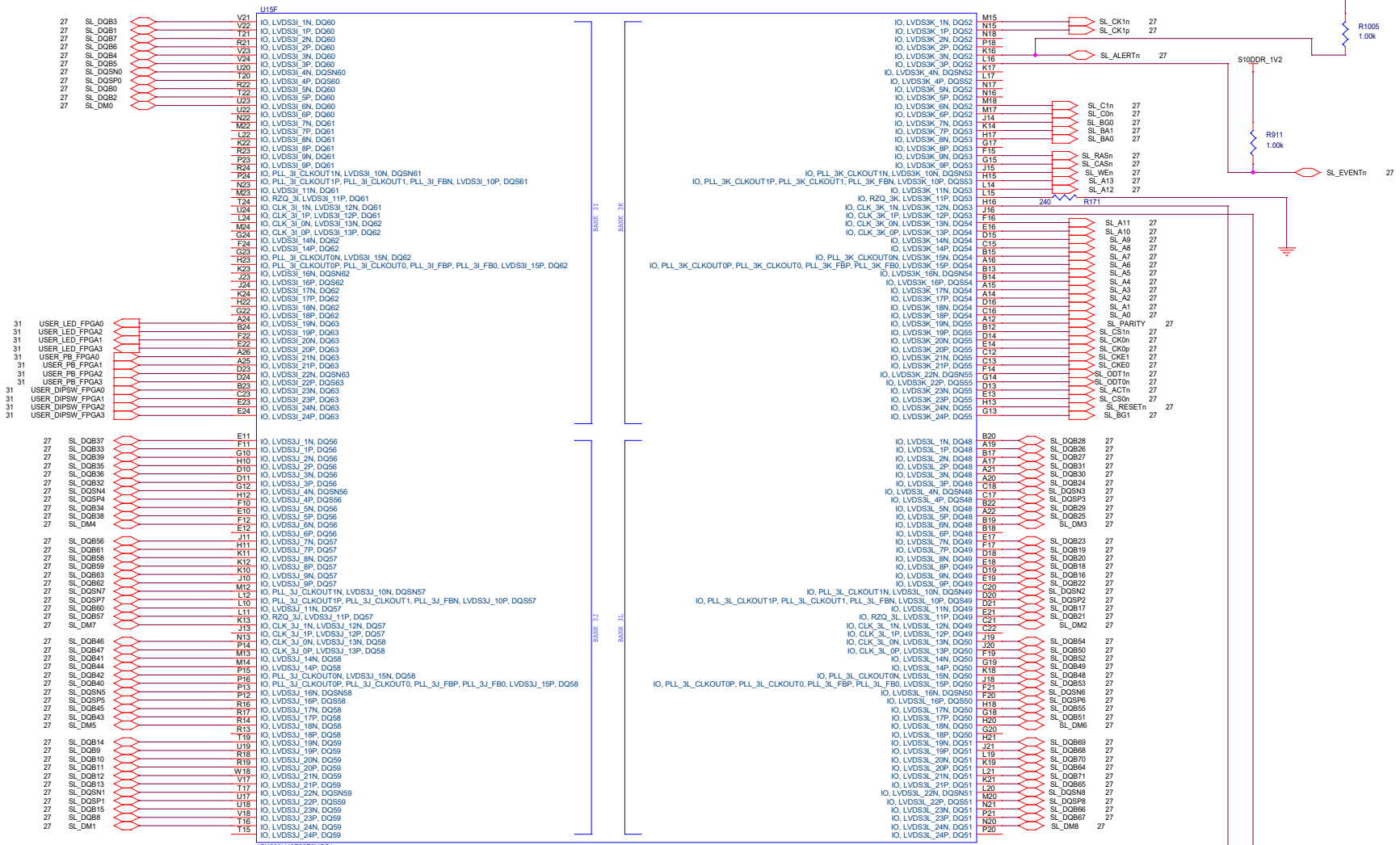
I2C address "1010101"
EEPROM

I2C address "0011101"
Temperature sensor

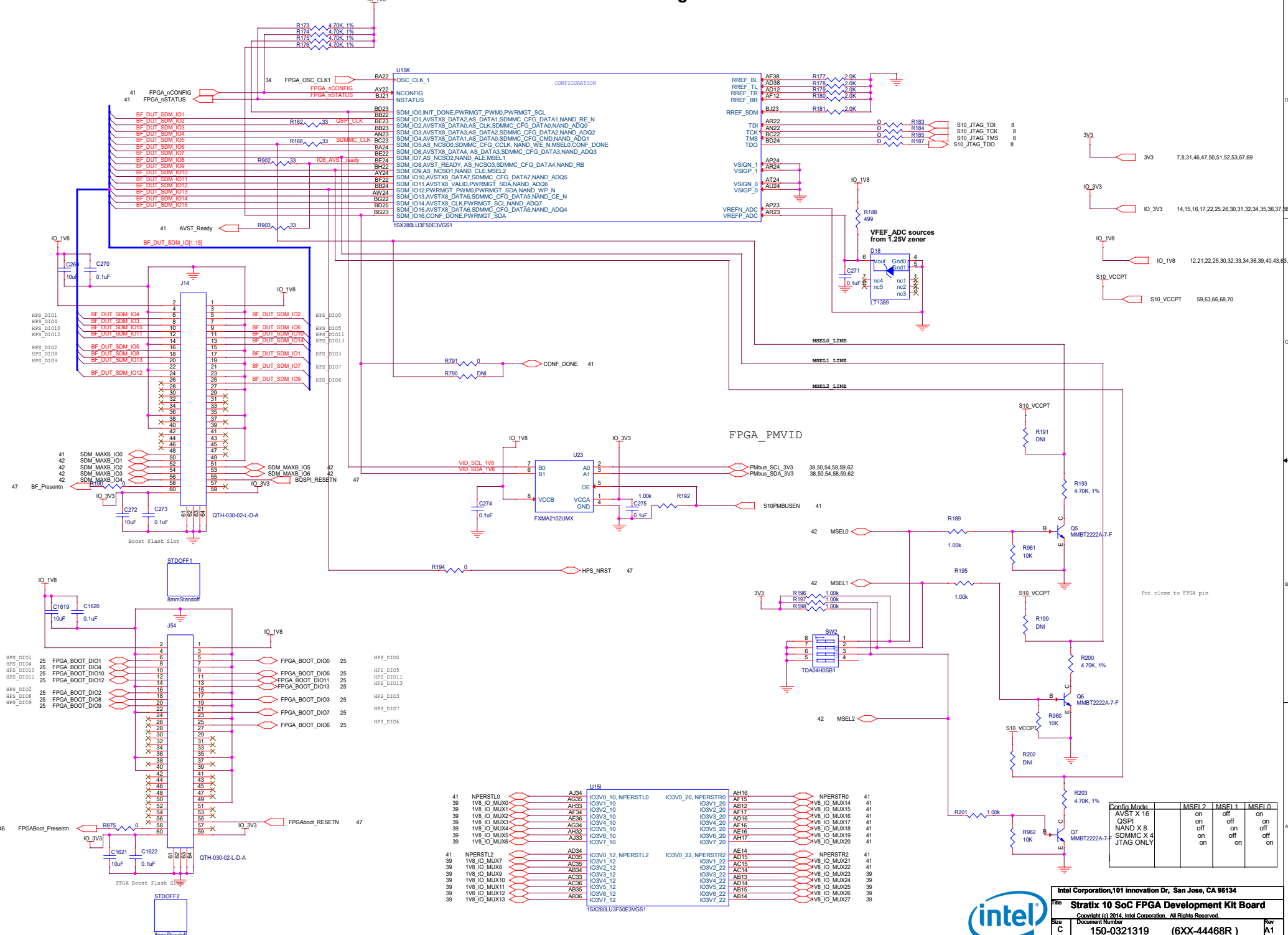


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Stratix 10 Banks - 3 I/J/L/K



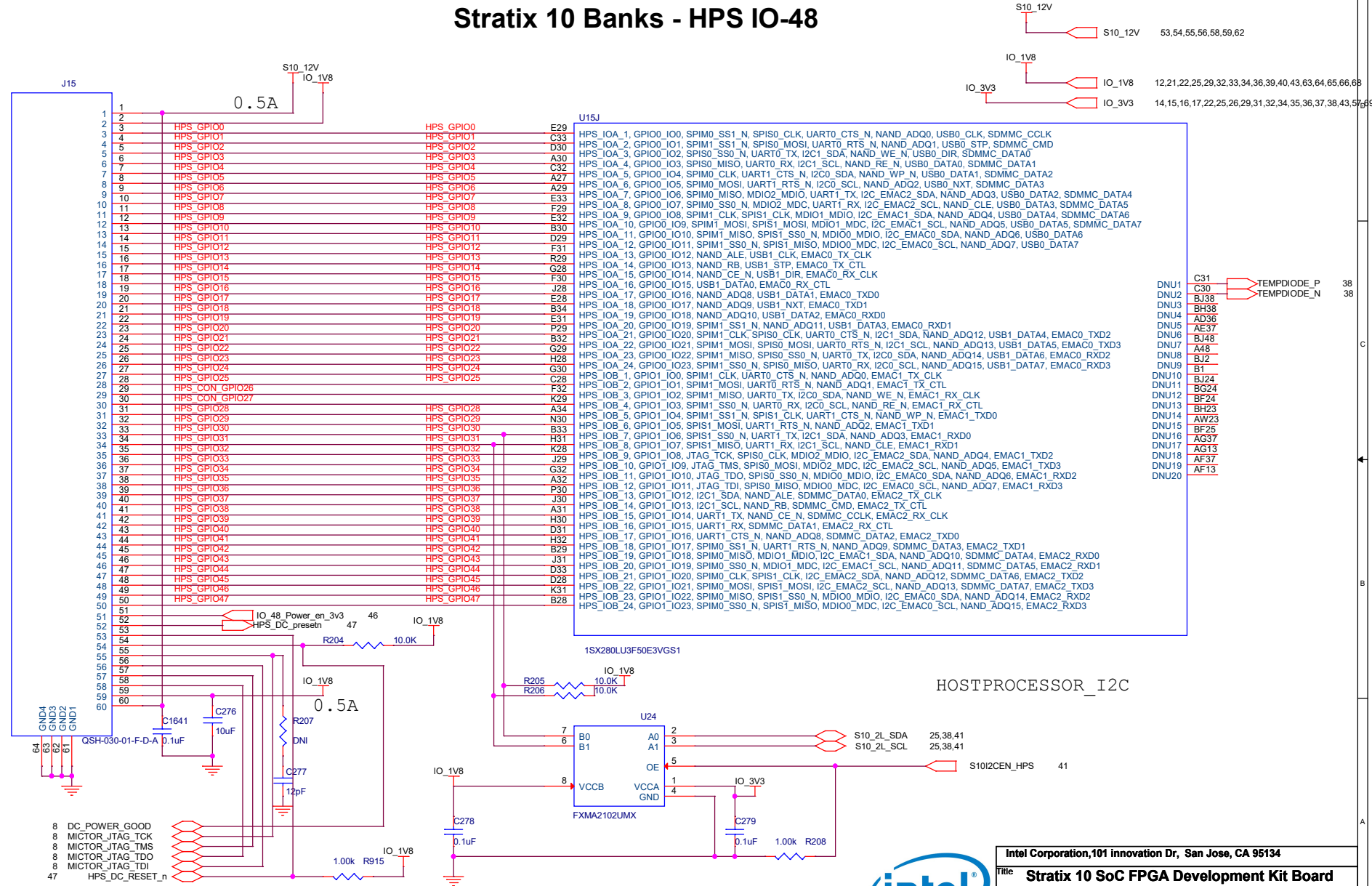
Stratix 10 Banks - Configuration



Config Mode	MSEL2	MSEL1	MSEL0
AVST X 16	on	off	on
QSPI	on	off	on
NAND X 8	off	on	off
SDMMC X 4	on	on	off
JTAG ONLY	on	on	off



Stratix 10 Banks - HPS IO-48



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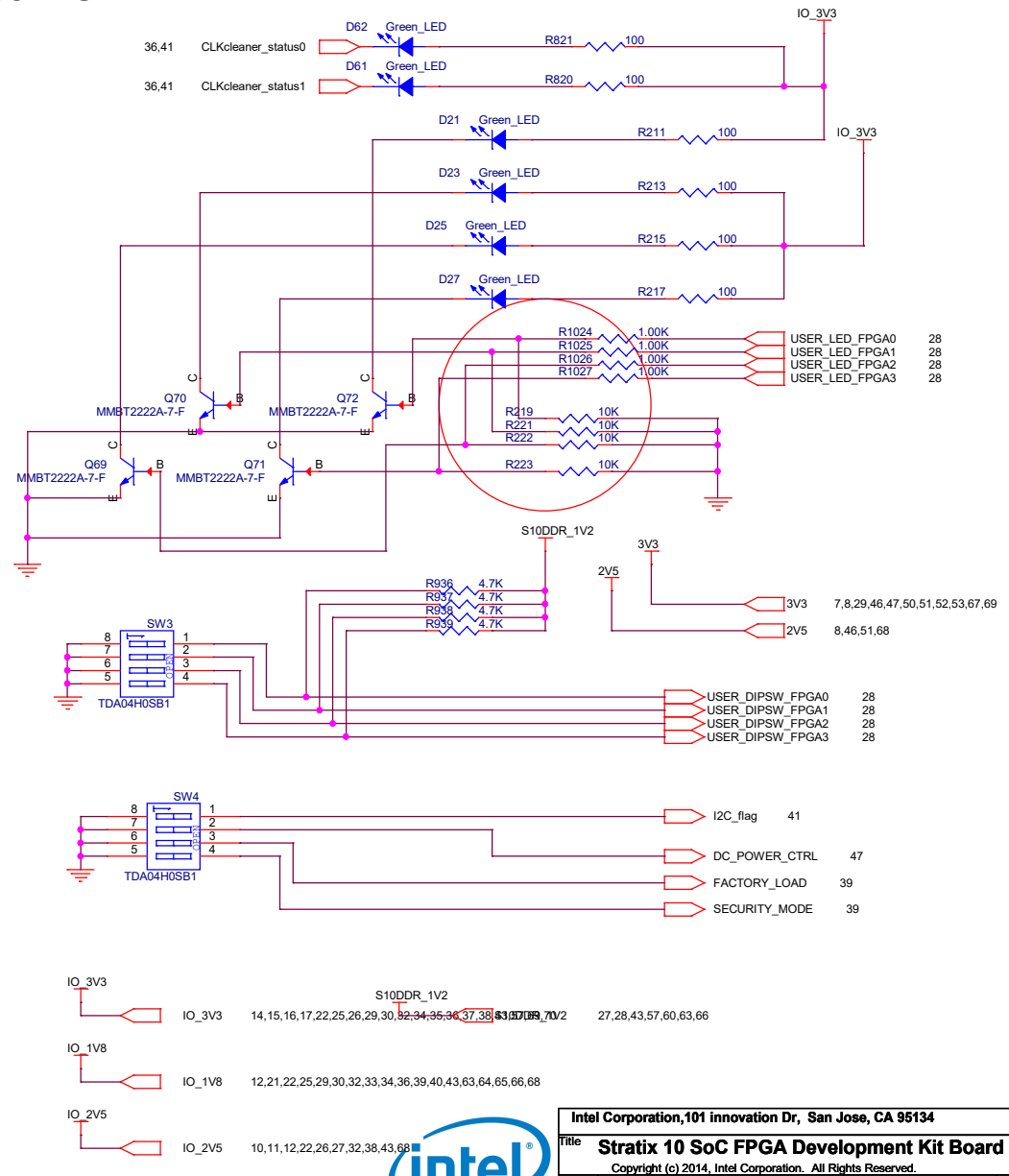
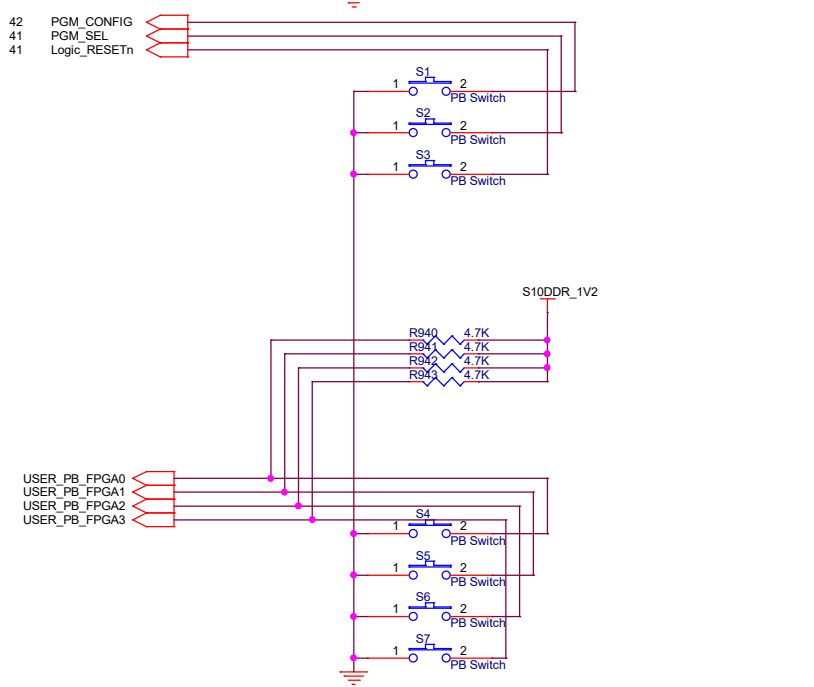
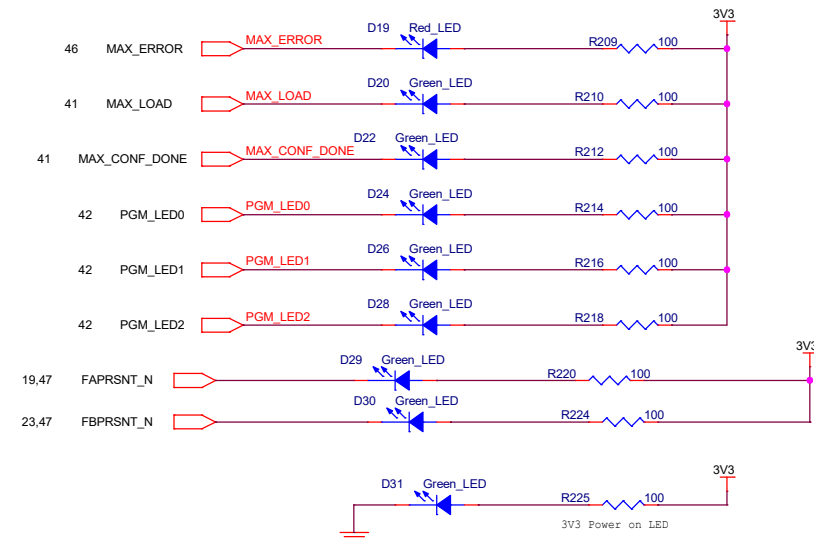
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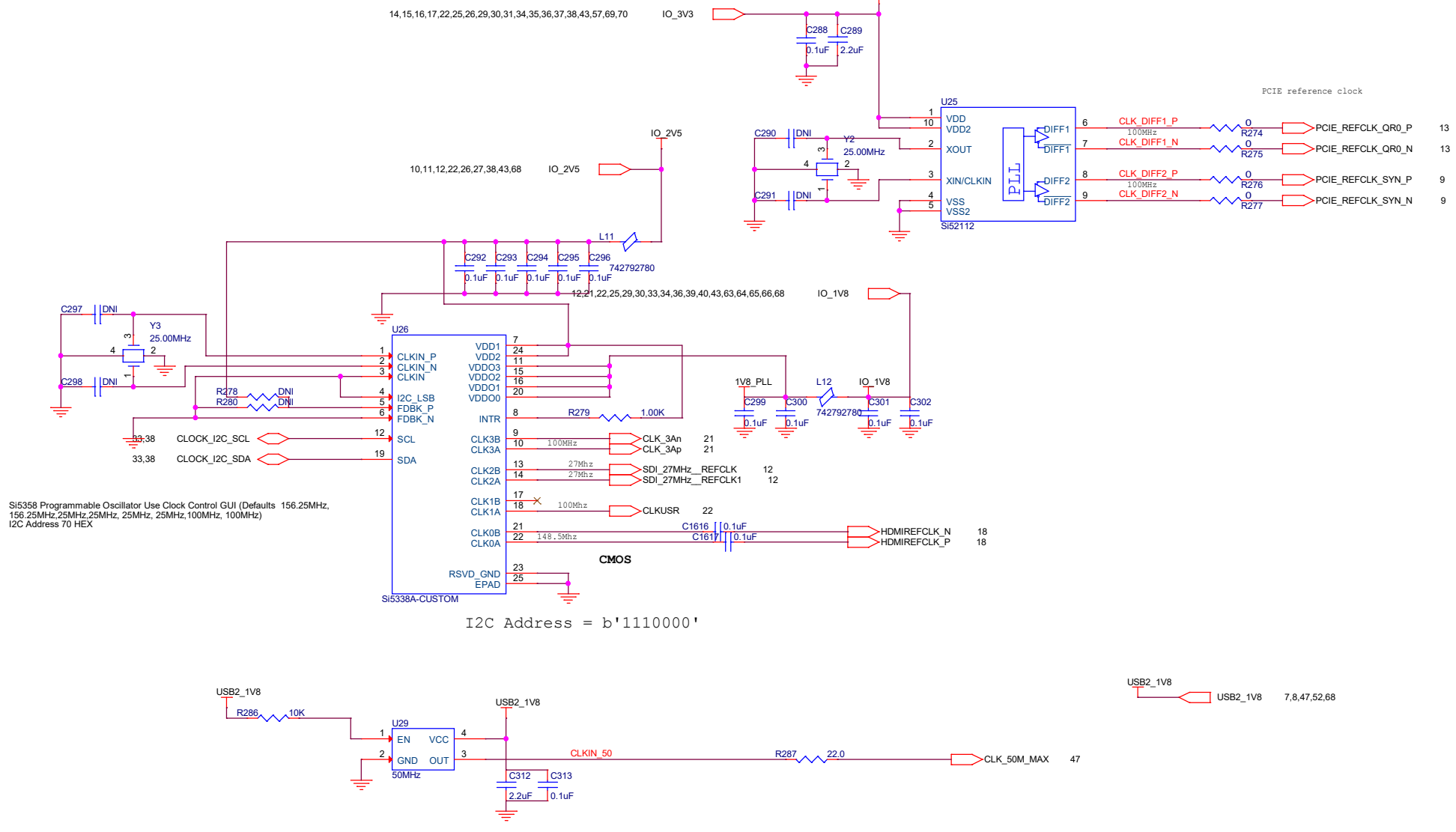
STDOFF3
8mmStandoff

User I/O



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PCIe& FPGA Reference Clock1



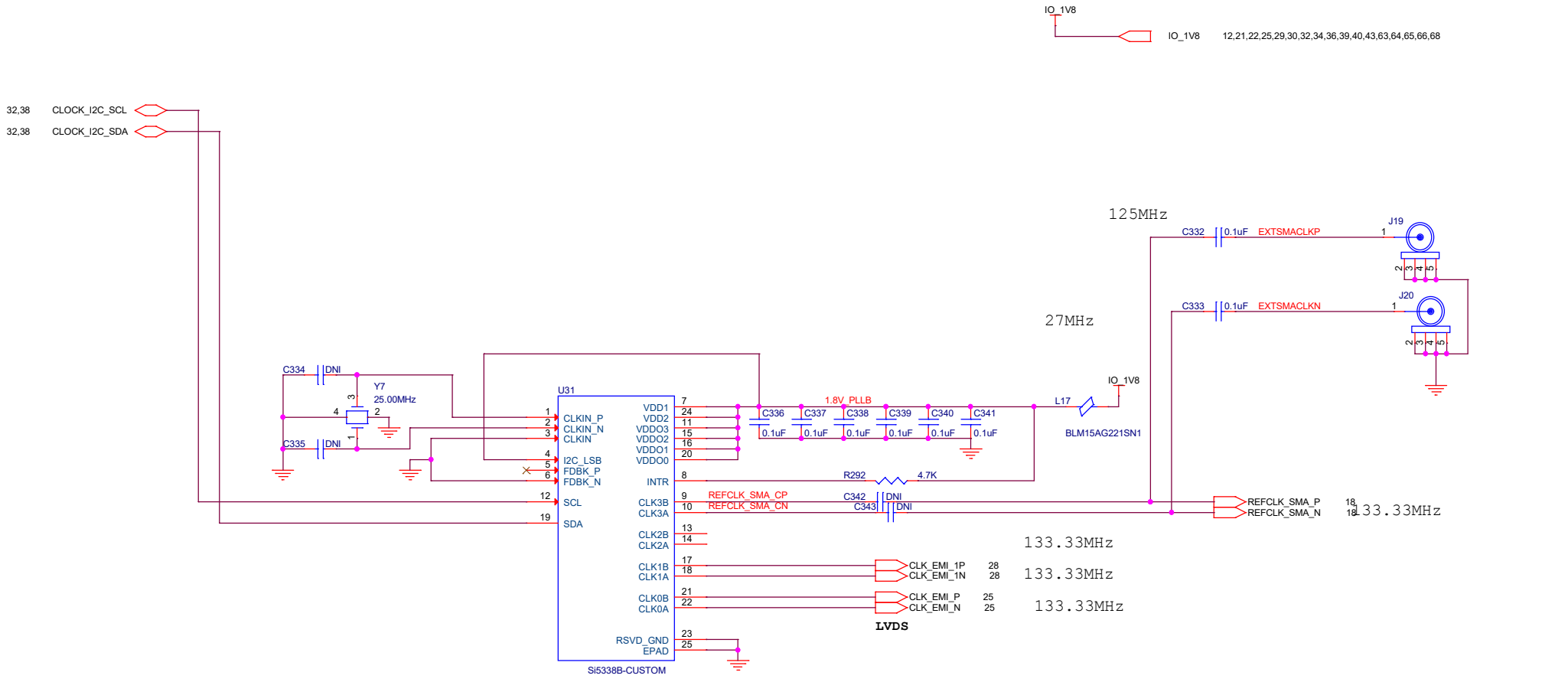
Si5358 Programmable Oscillator Use Clock Control GUI (Defaults 156.25MHz, 156.25MHz, 25MHz, 25MHz, 25MHz, 25MHz, 100MHz, 100MHz) I2C Address 70 HEX

I2C Address = b'11110000'



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FPGA Memory Reference clock

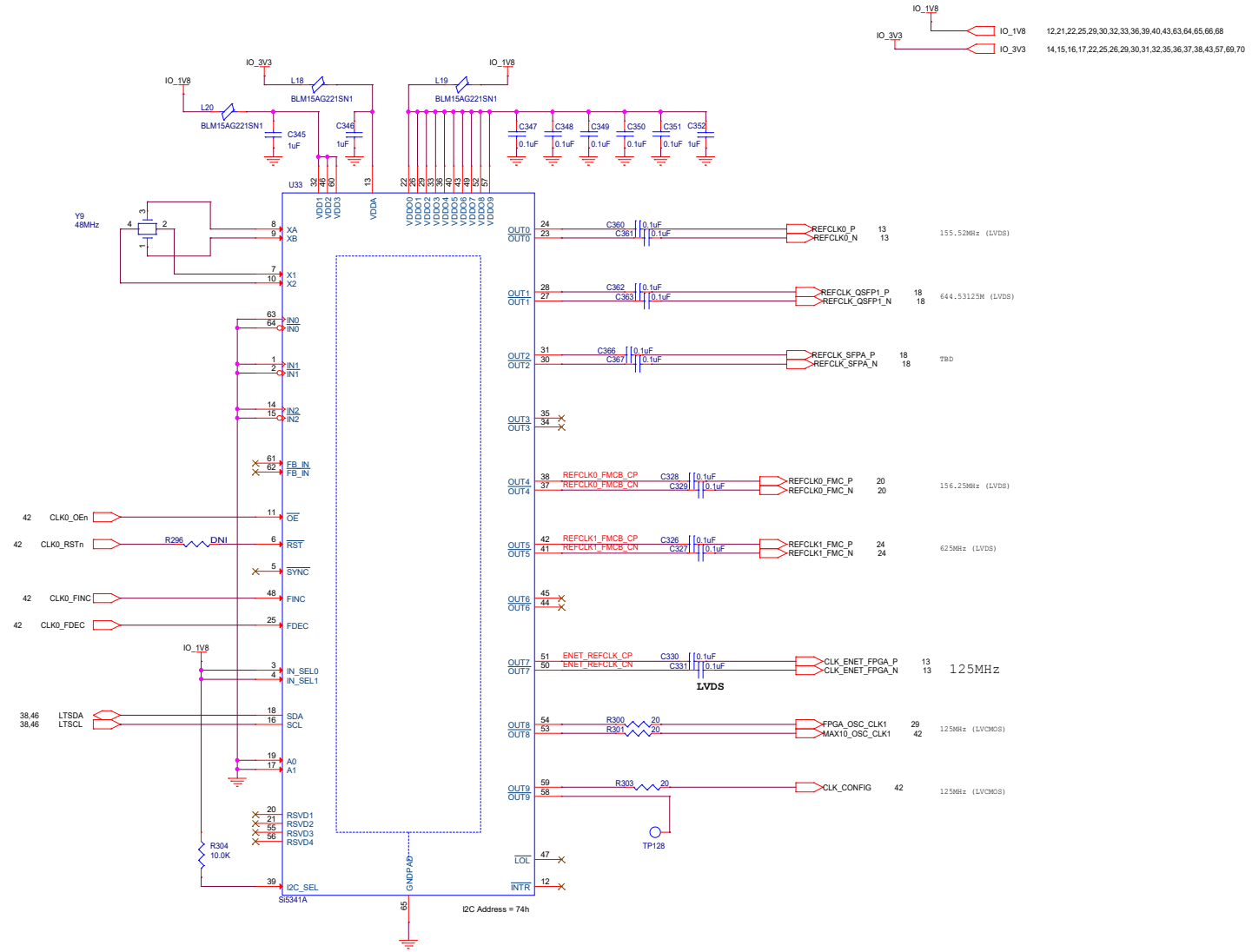


I2C Address = b'1110011'



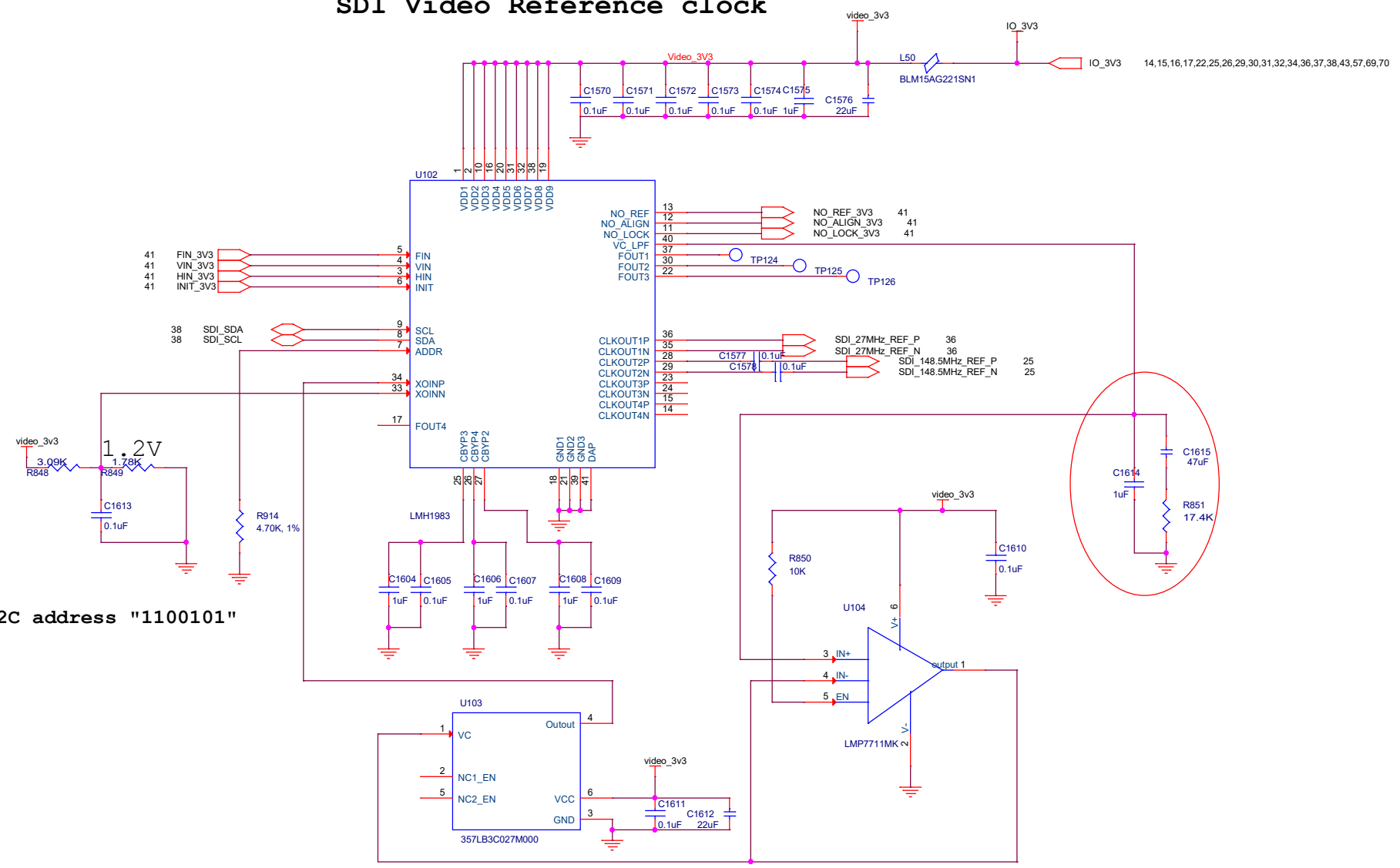
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FPGA Transceiver reference Clocks



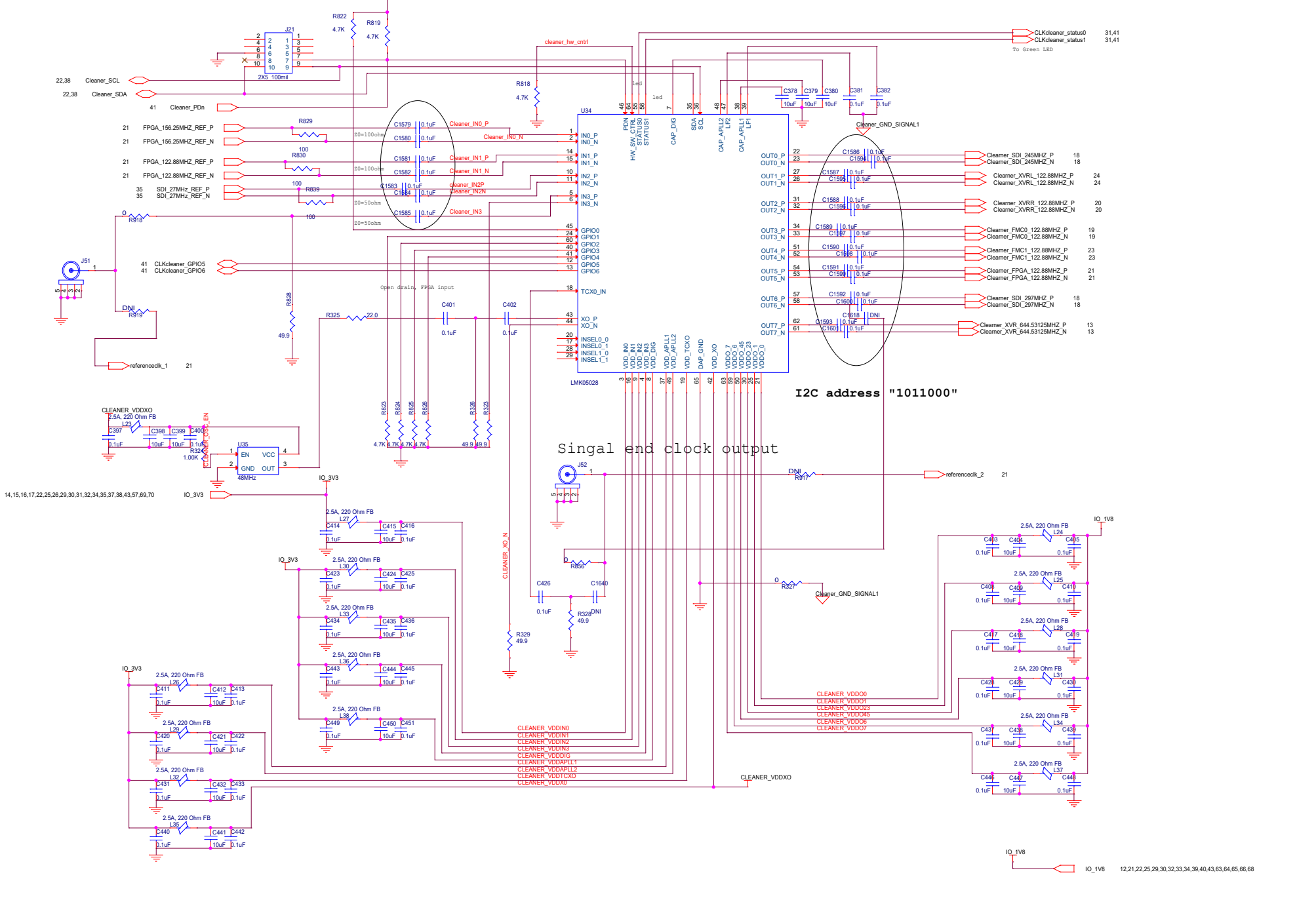
SDI Video Reference clock

I2C address "1100101"

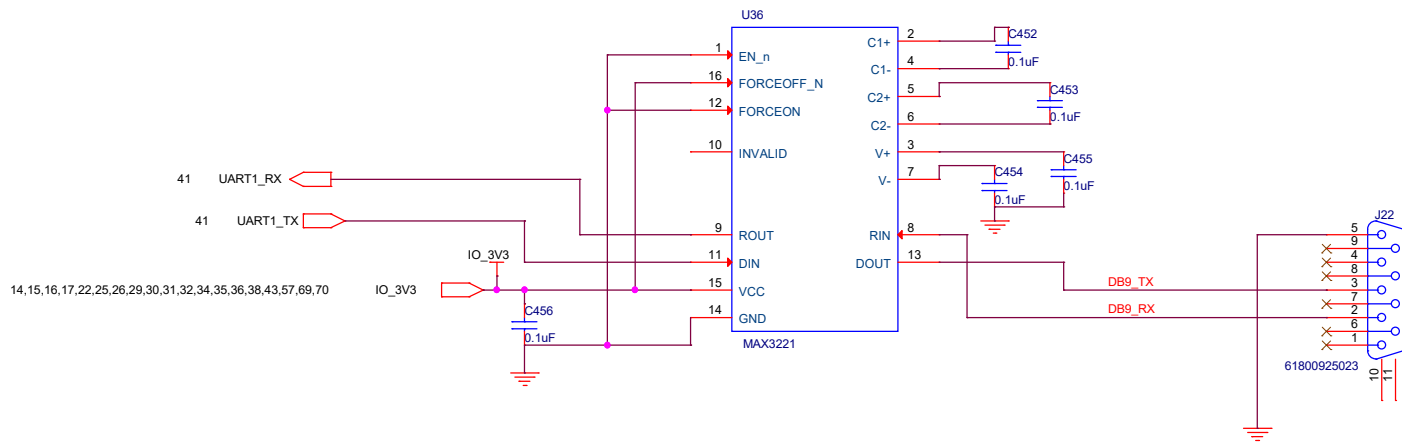


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Imk05028 CLOCK CLEANER

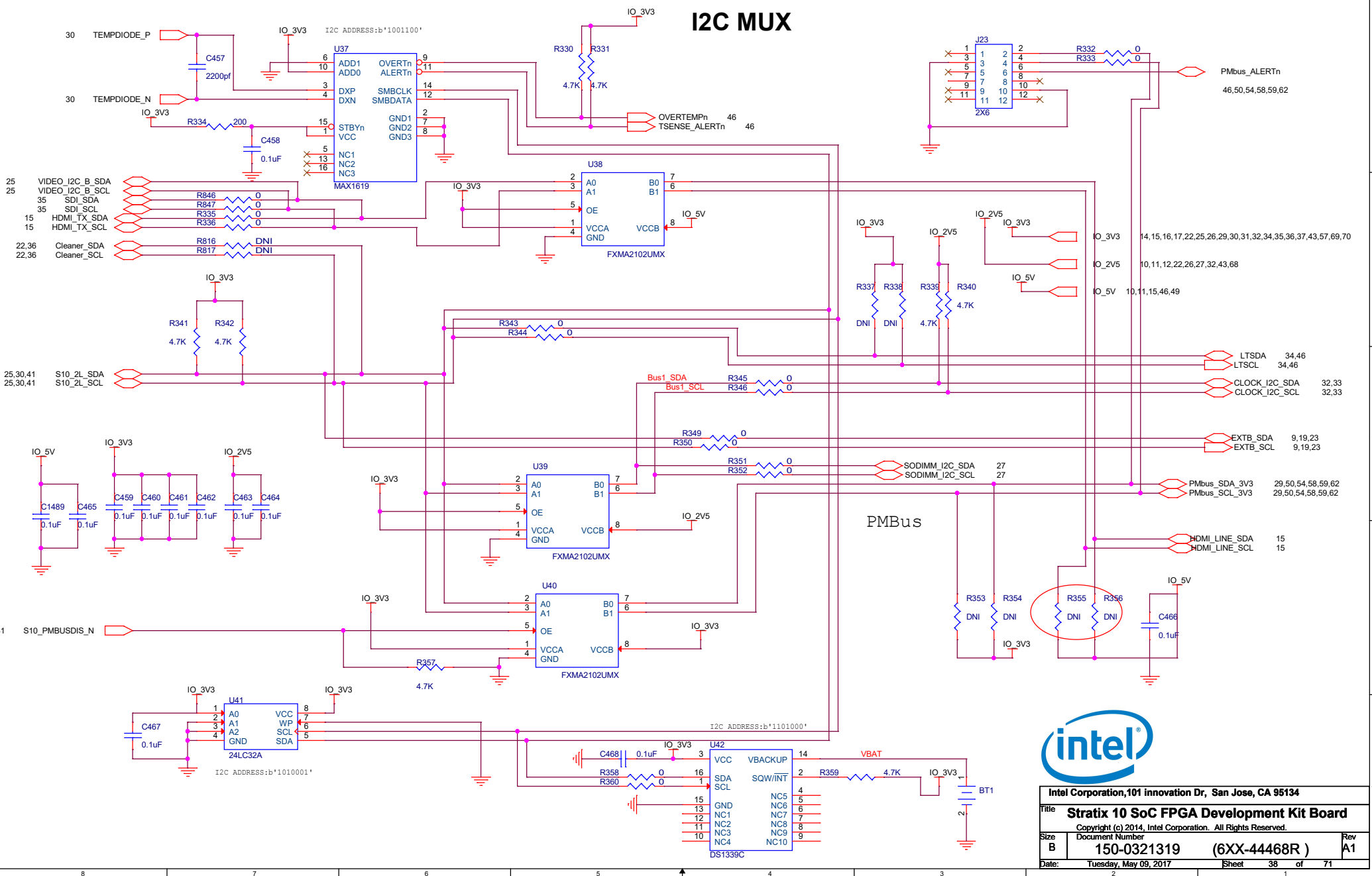


UART Port B



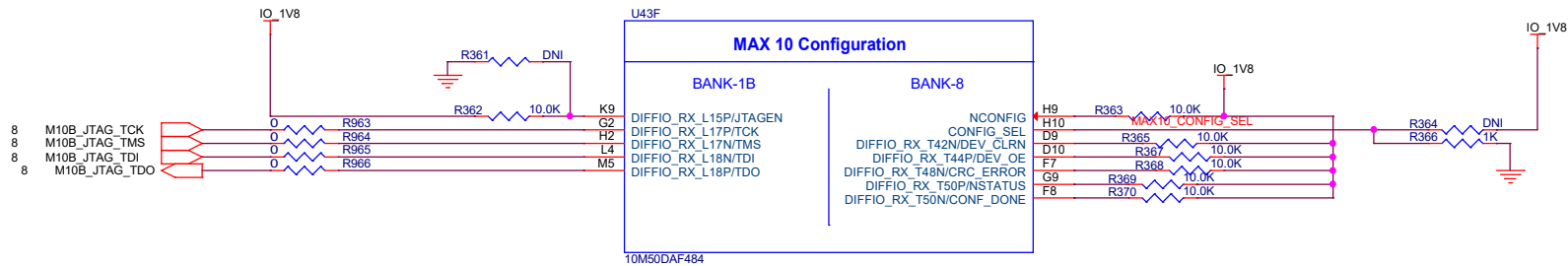
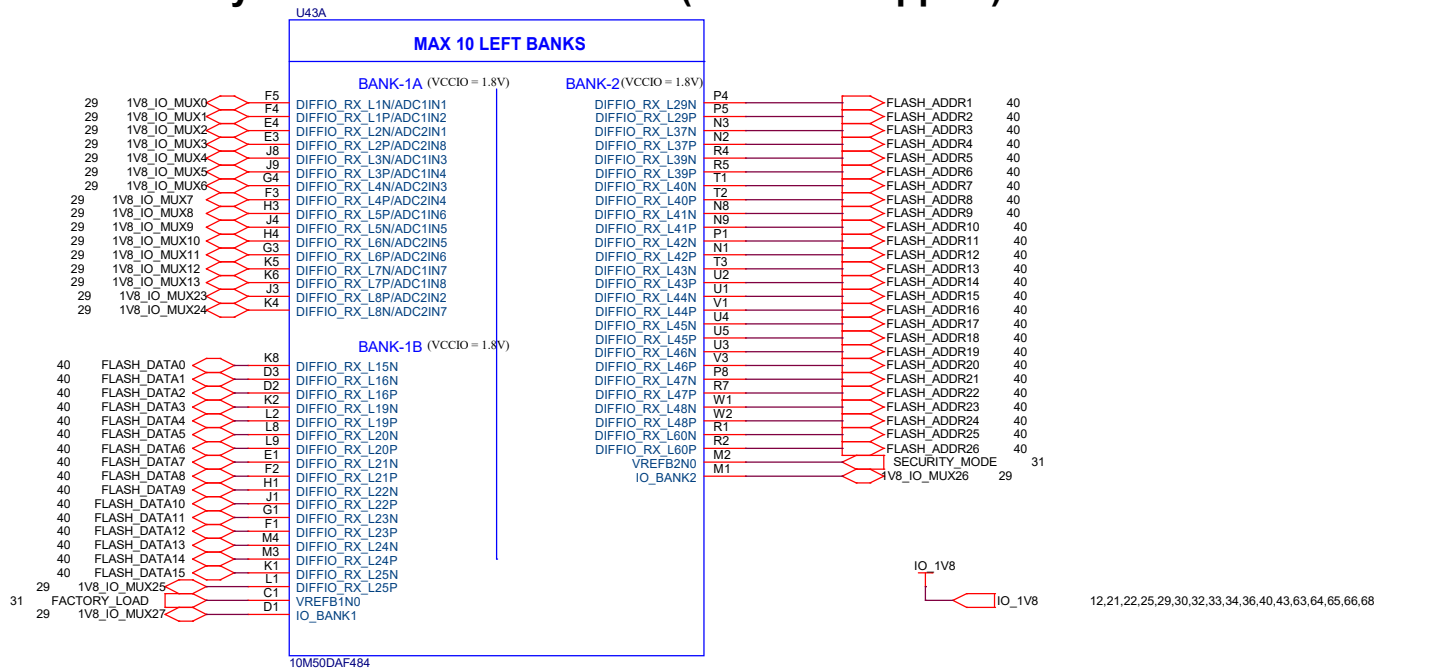
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I2C MUX



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System MAX10 Controller (NO ADC Support)

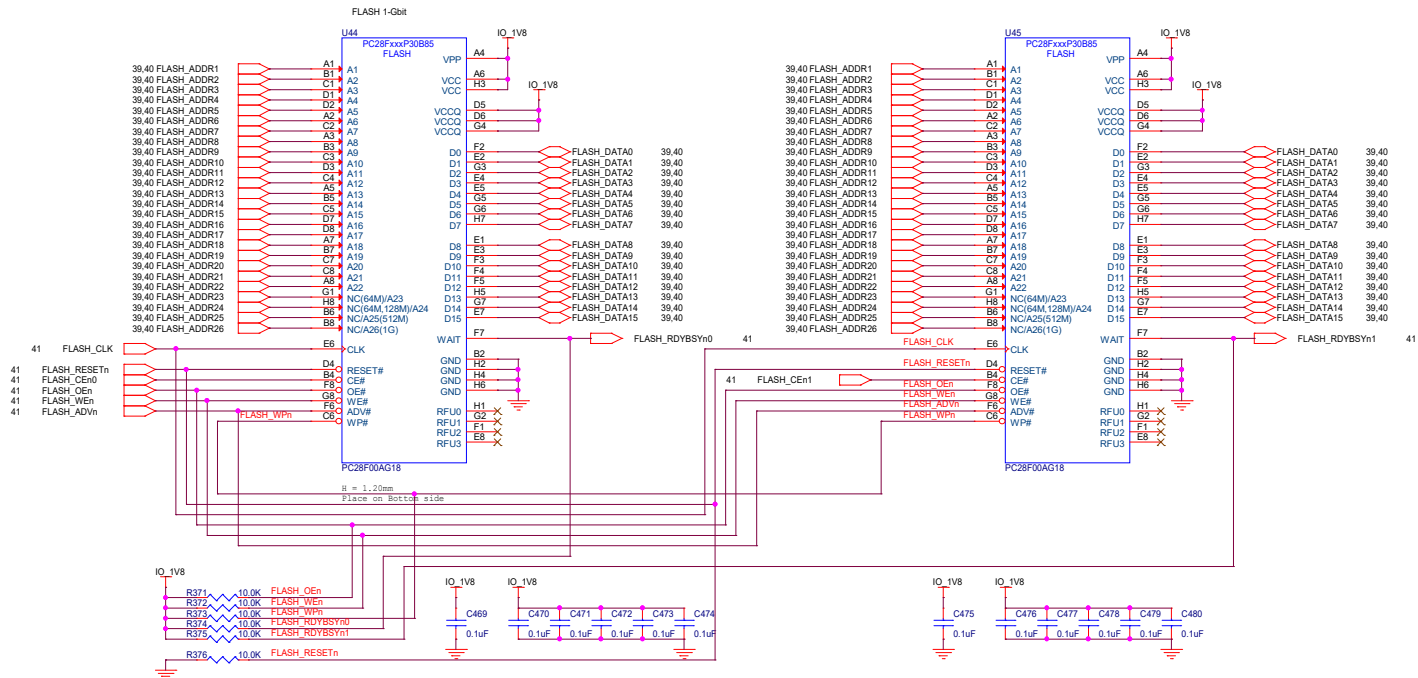


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Flash Memory

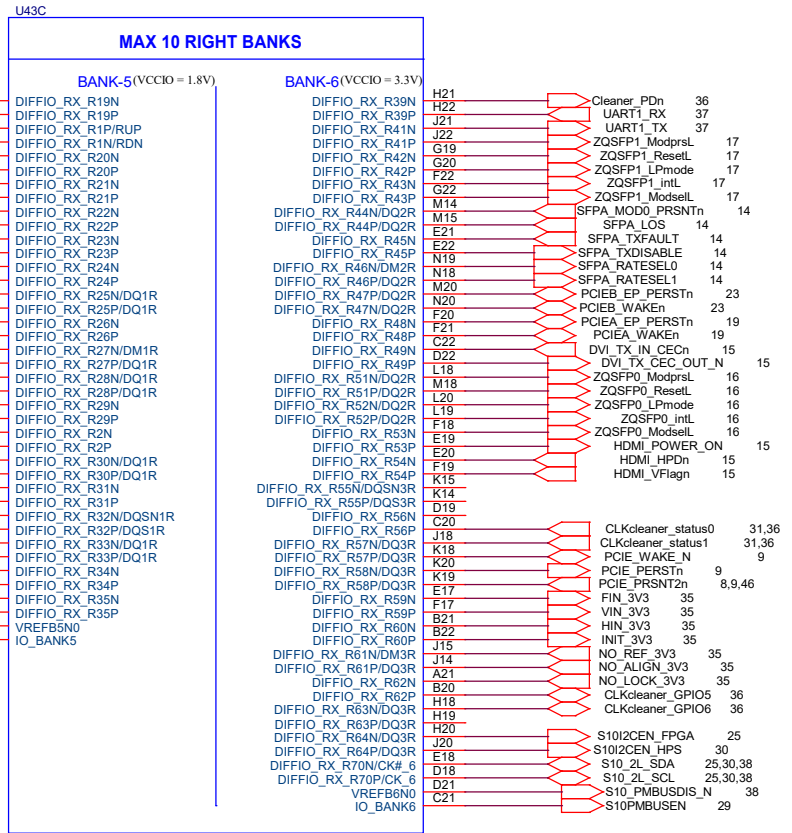
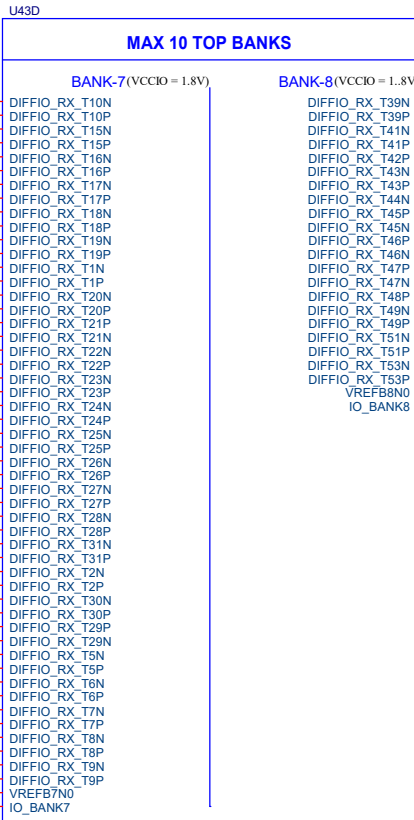
For Avalon Stream x16 Configuration

IO_1V8
IO_1V8 12.21,22,25,29,30,32,33,34,36,39,43,63,64,65,66,68



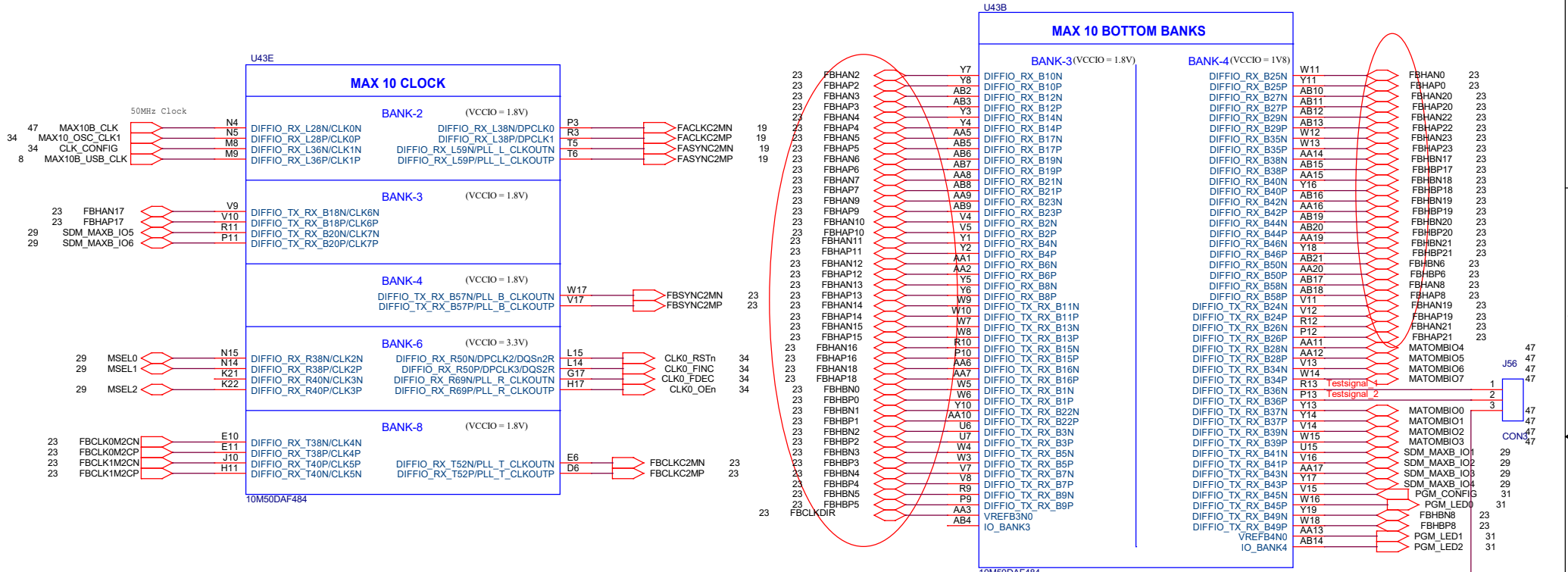
- When using a single x16 flash device a word consists of 16 data bits so addressing starts with FM_A1 mapped to address bit 1 in software.

System MAX10 Controller 2

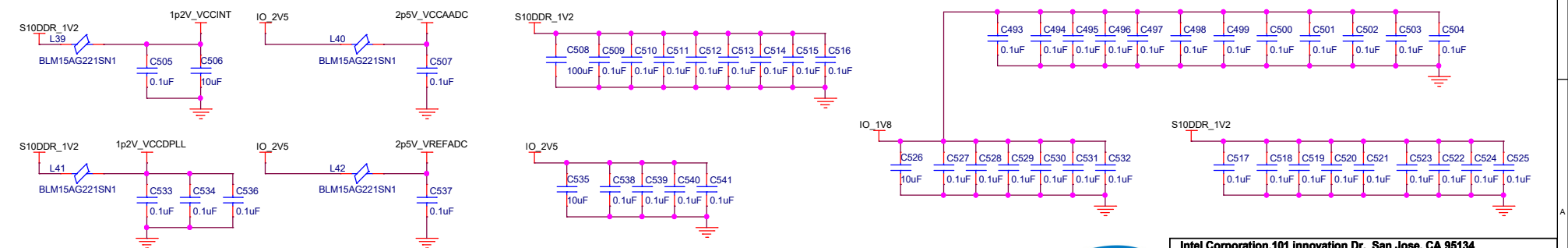
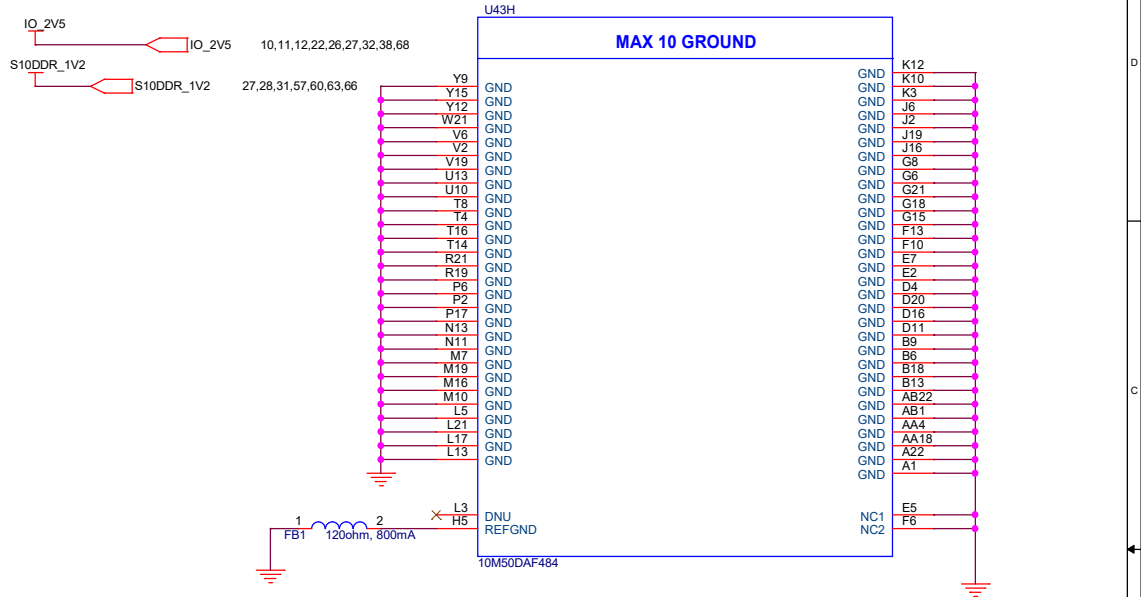
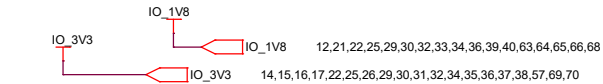
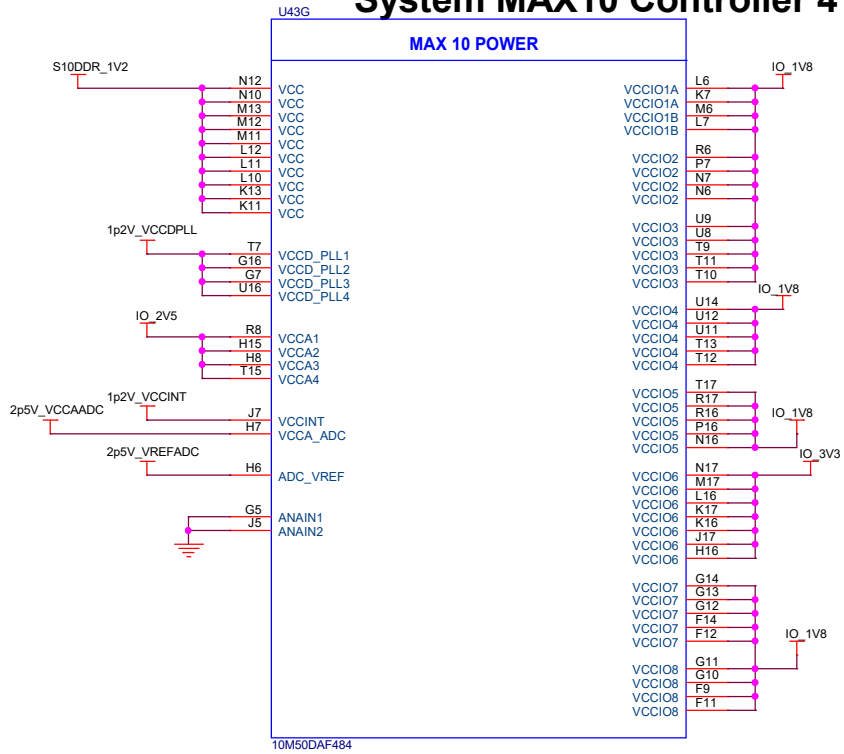


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System MAX10 Controller 3

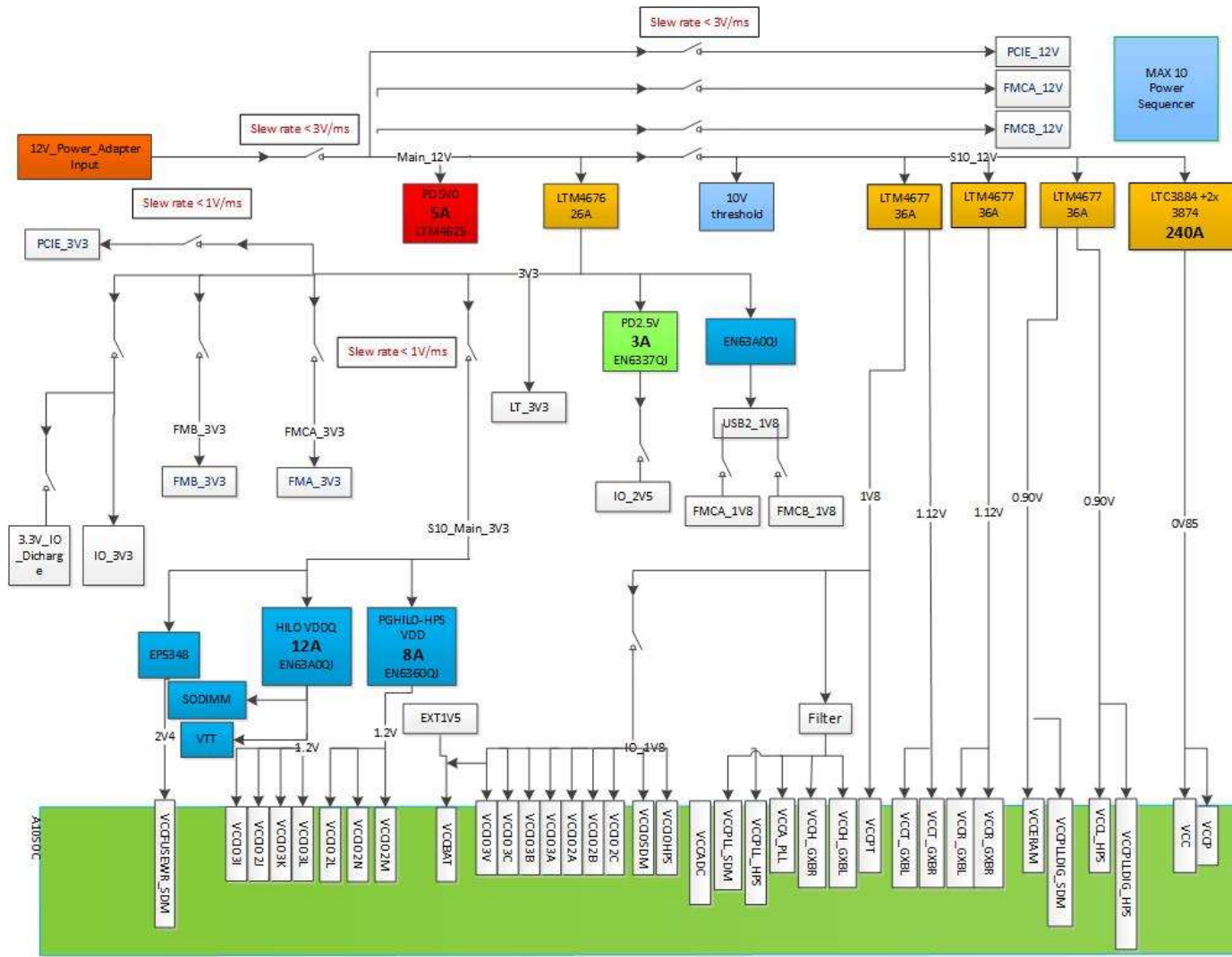


System MAX10 Controller 4



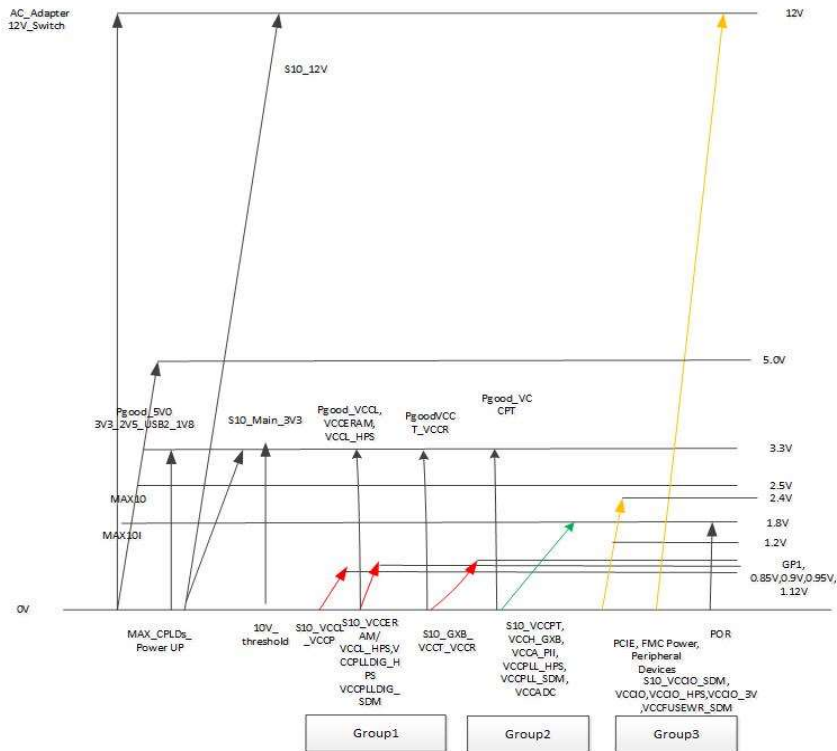
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Stratix 10 SOC DEV KIT PDN Diagram

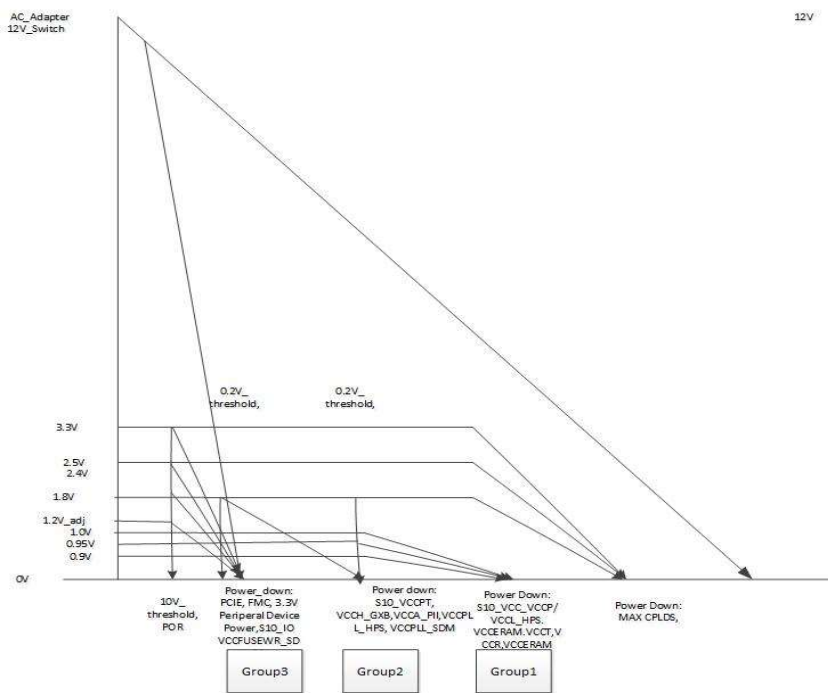


Stratix 10 SOC Power Sequence

S10 Dev KIT Power UP sequence

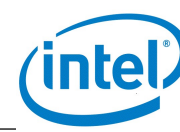
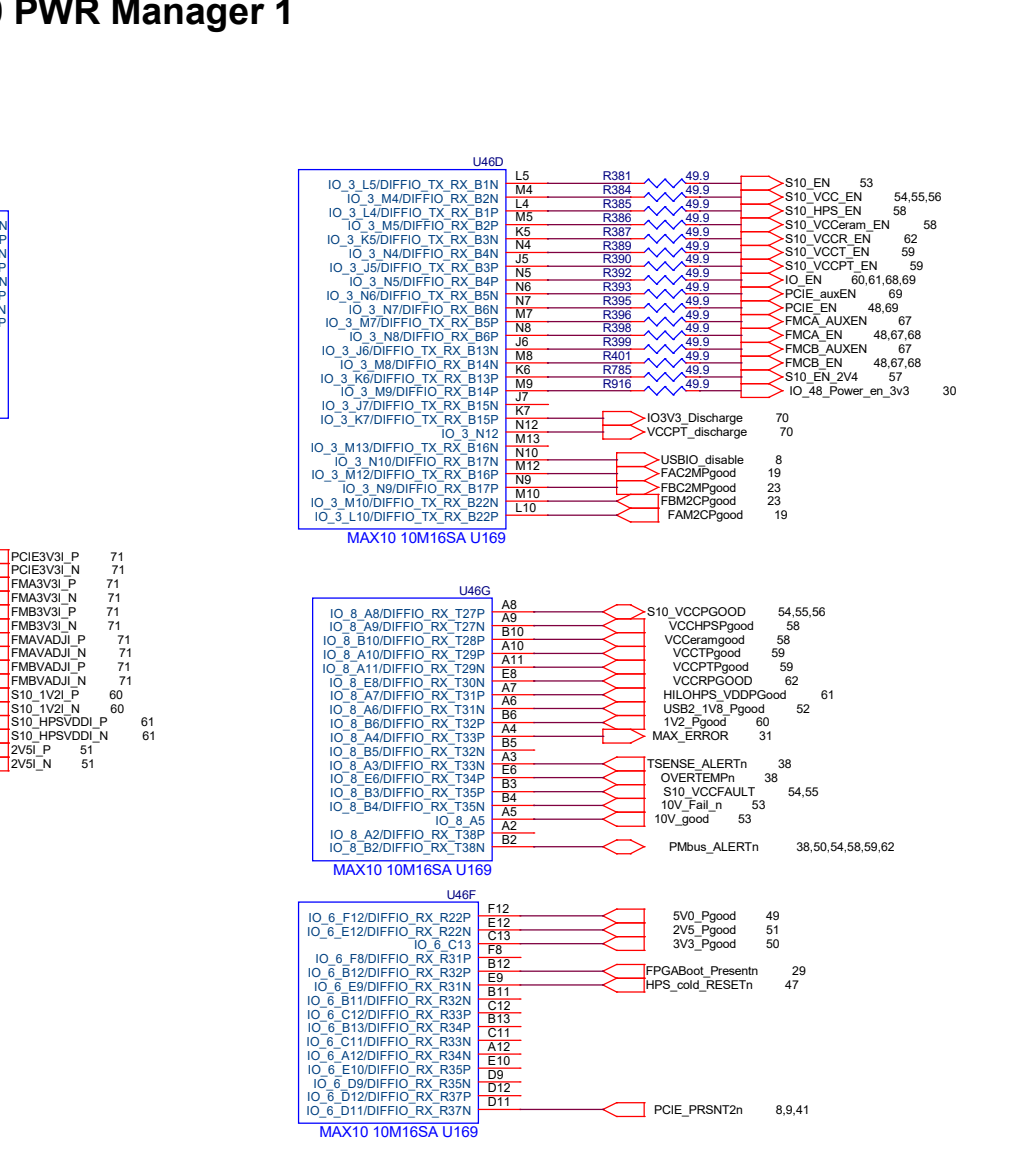
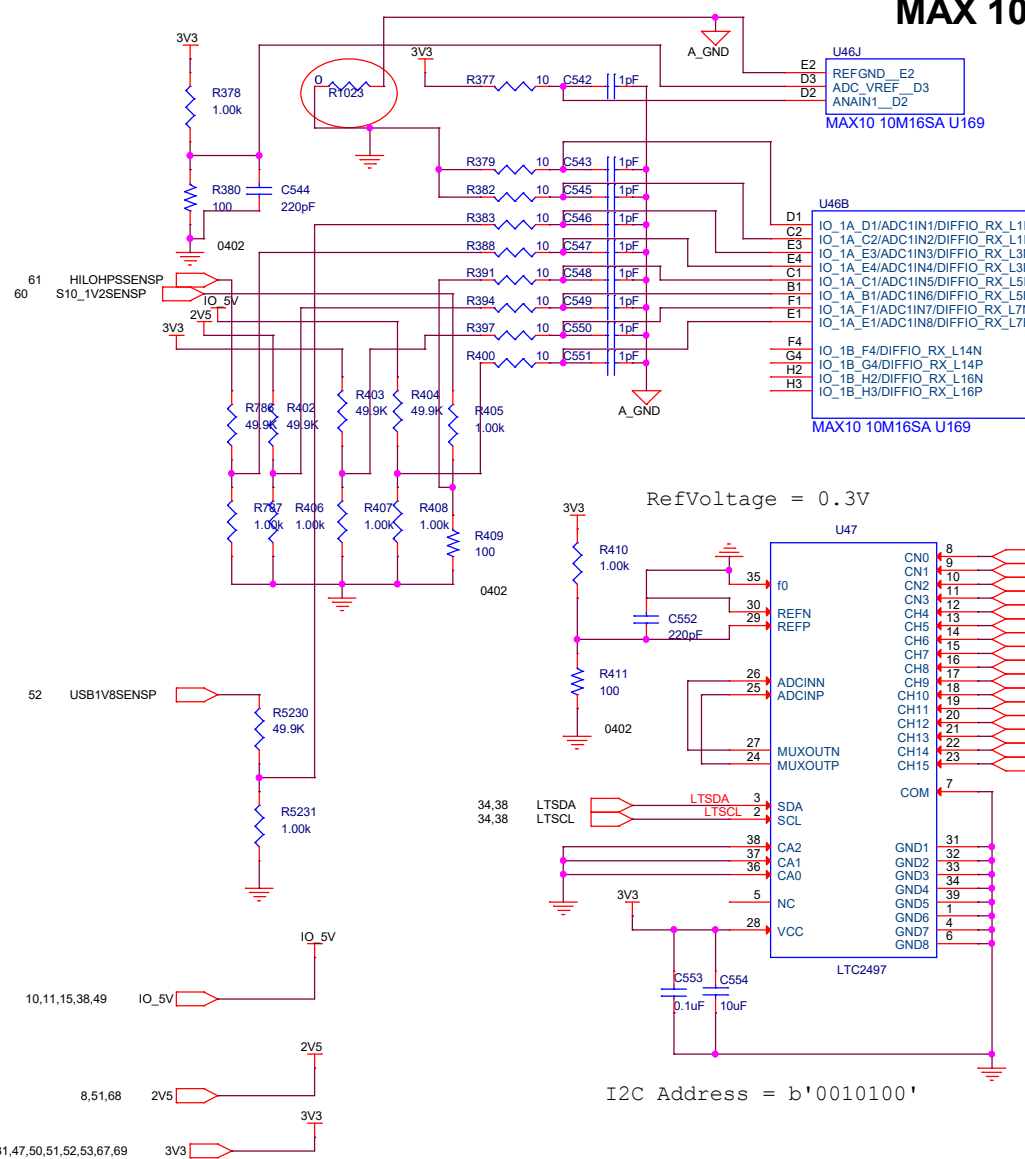


S10 Dev KIT Power Down sequence



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MAX 10 PWR Manager 1



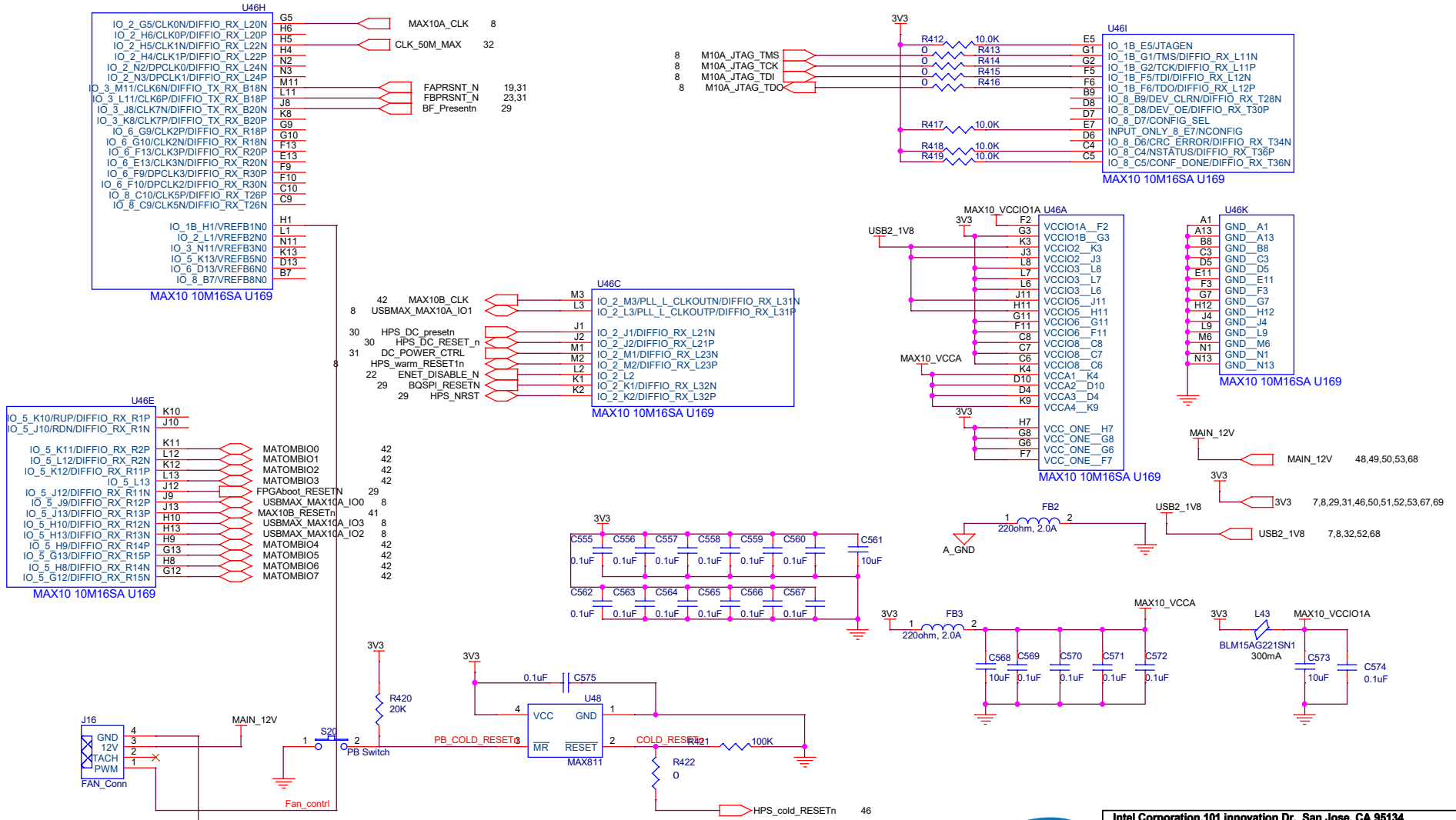
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Altera Corporation, 301, Bibo Rd #888, Shanghai, China, 201203

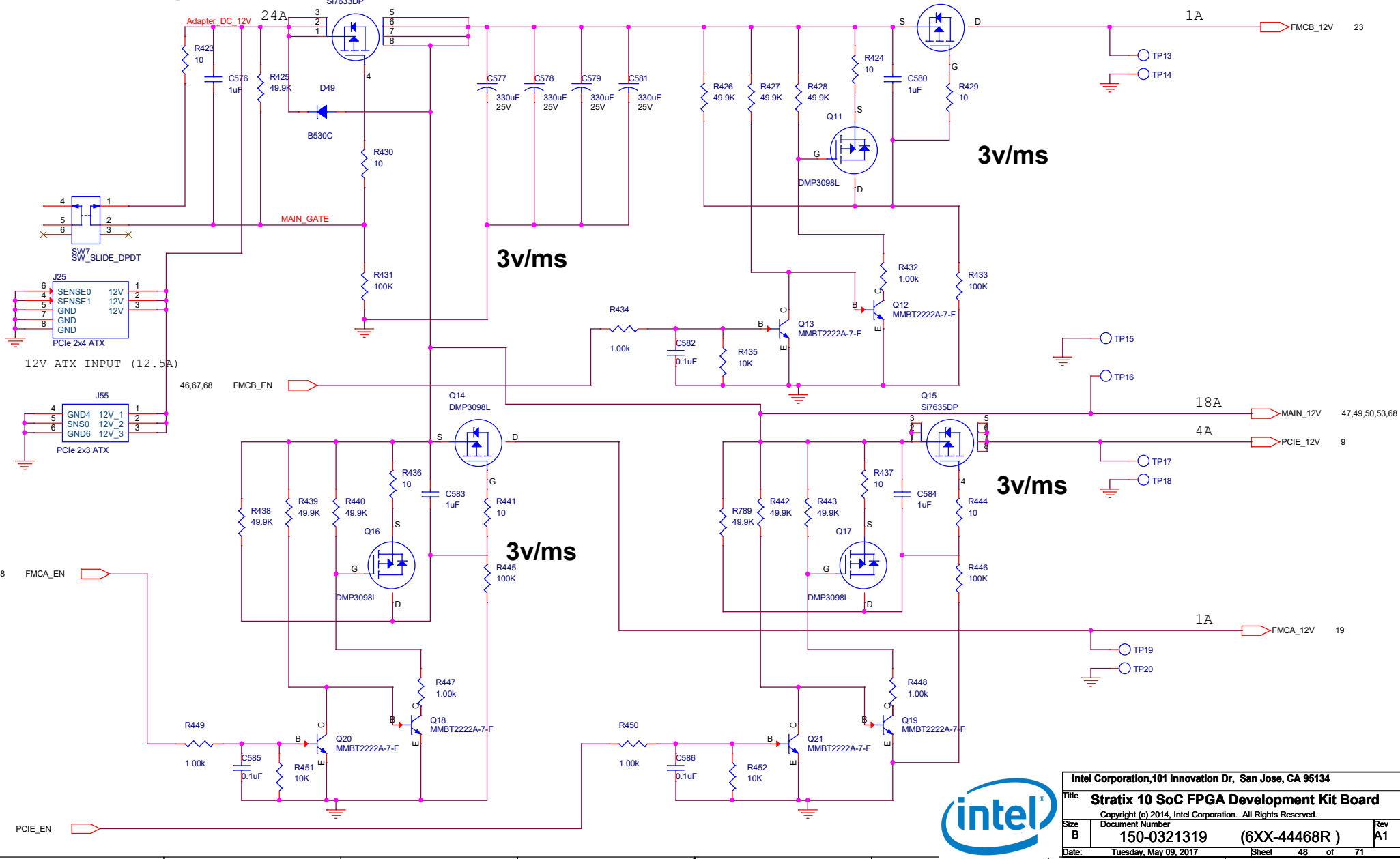


MAX10 PWR Manager 2



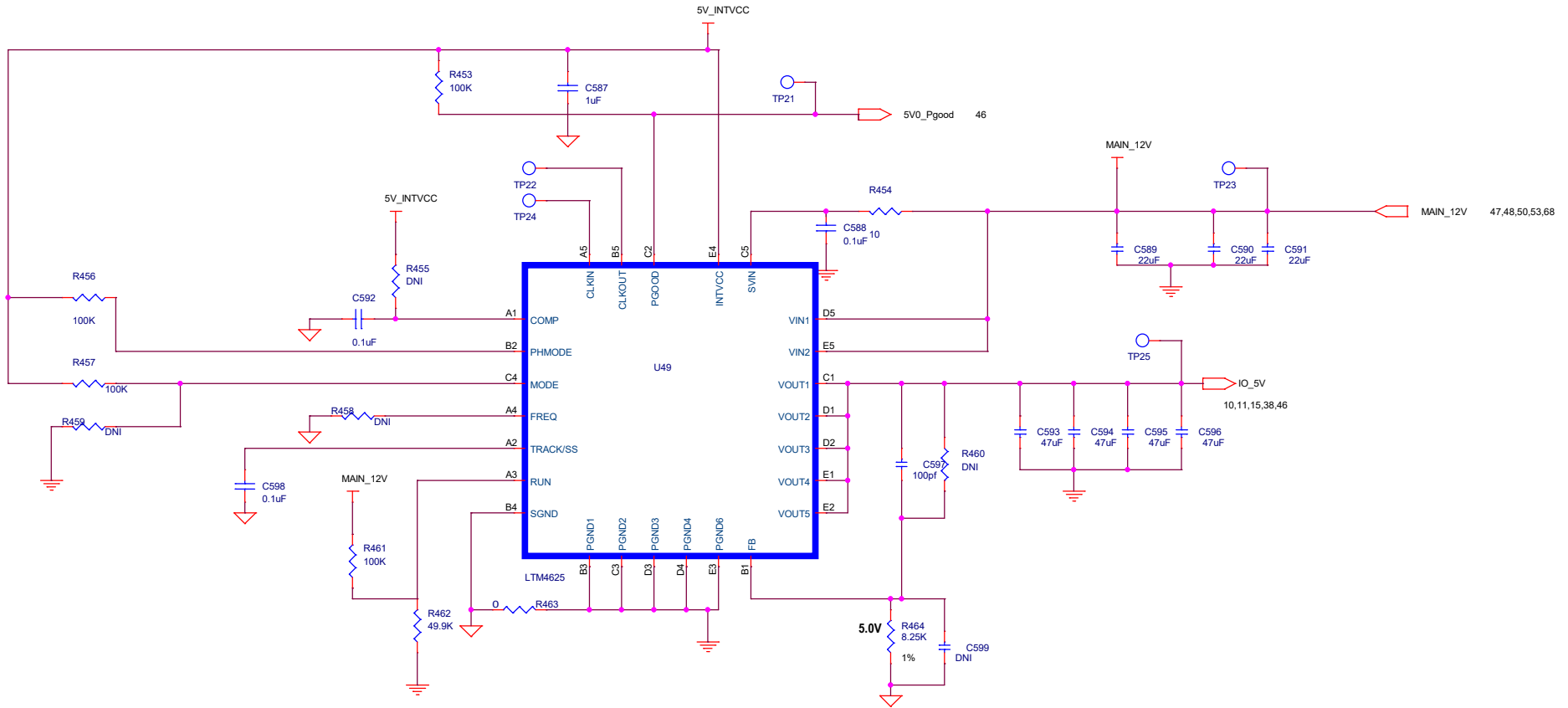
Input connector for
280 Watt AC/DC Adapter

12V Power PMOS Switches

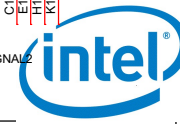
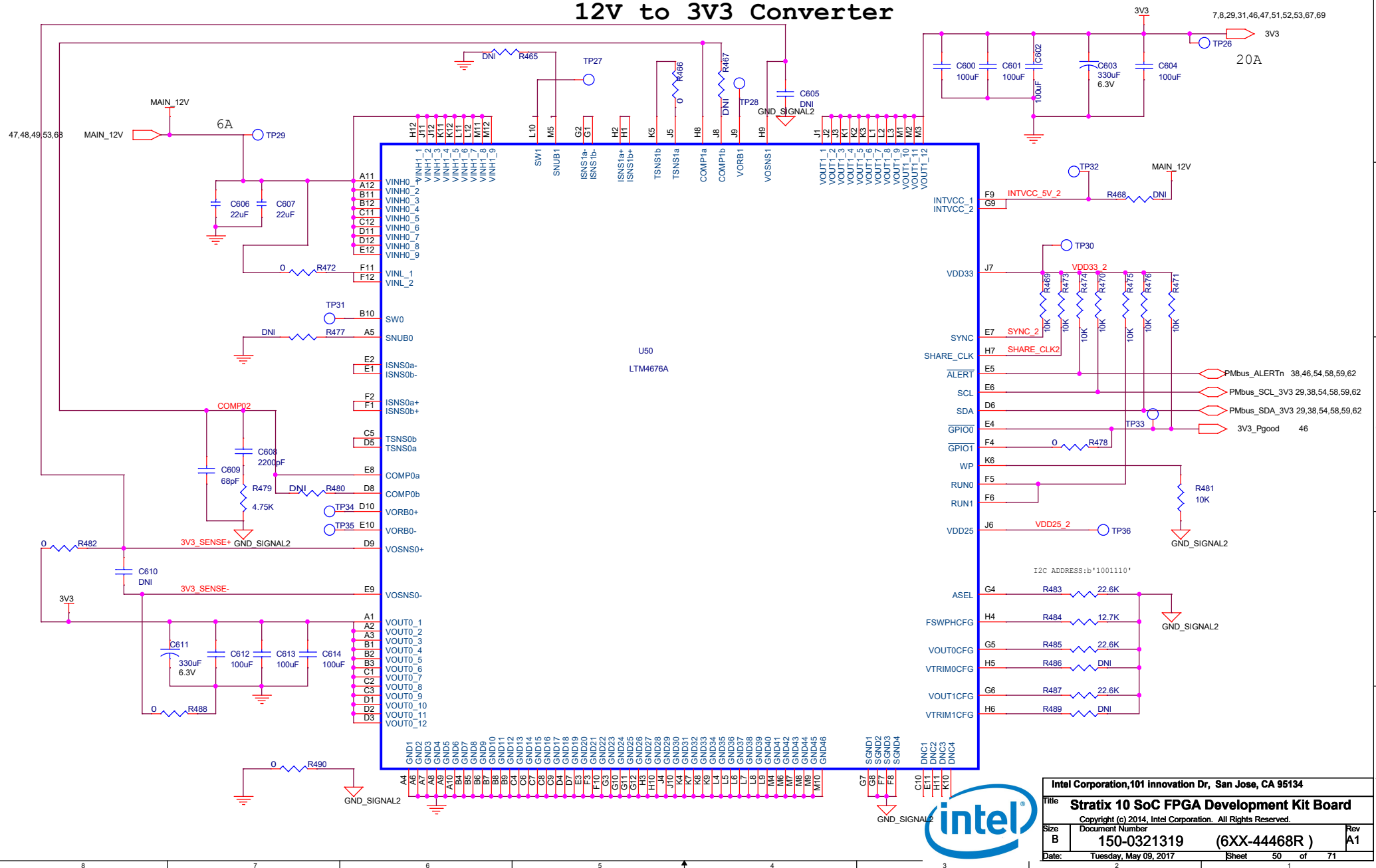


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12V to 5V Power Supply



12V to 3V3 Converter



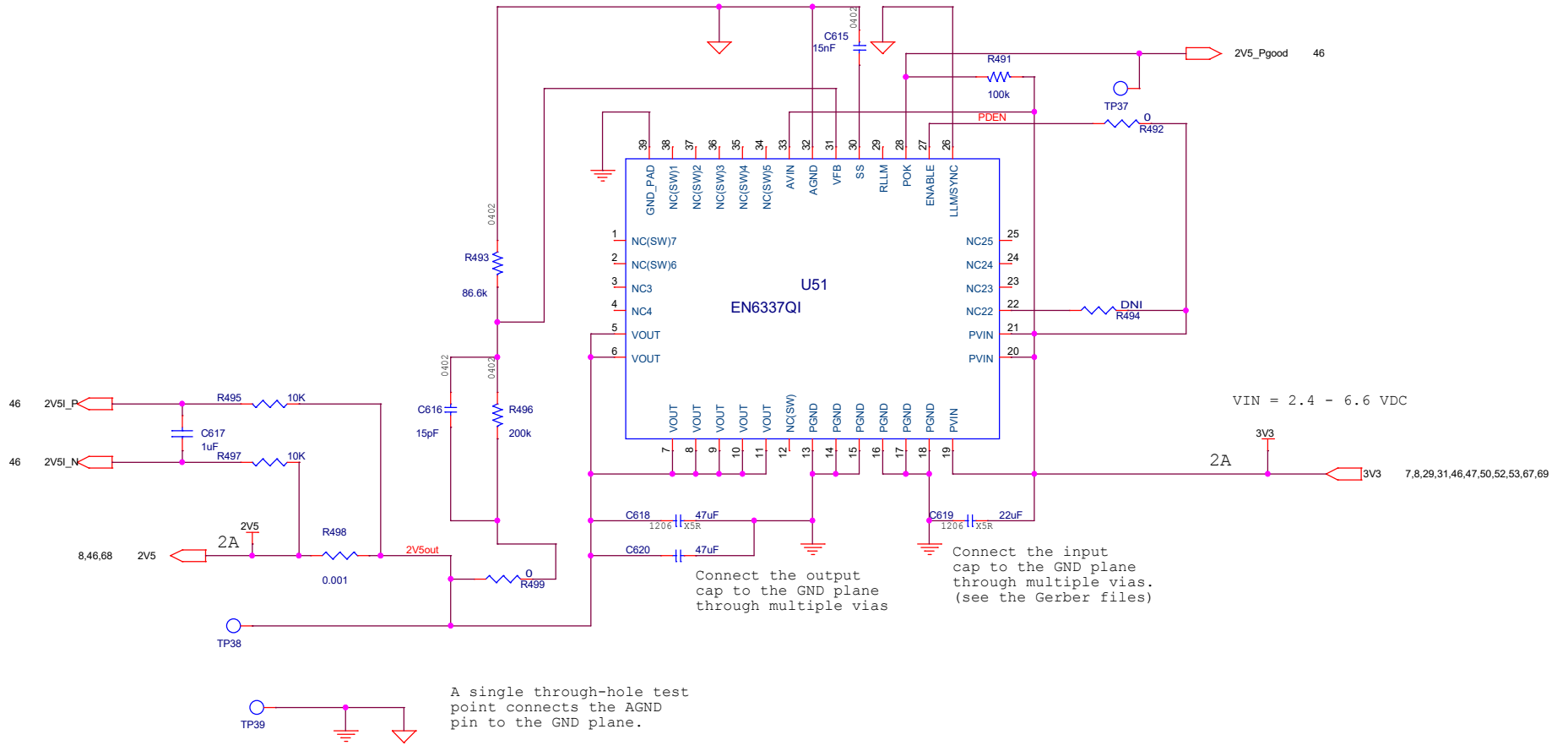
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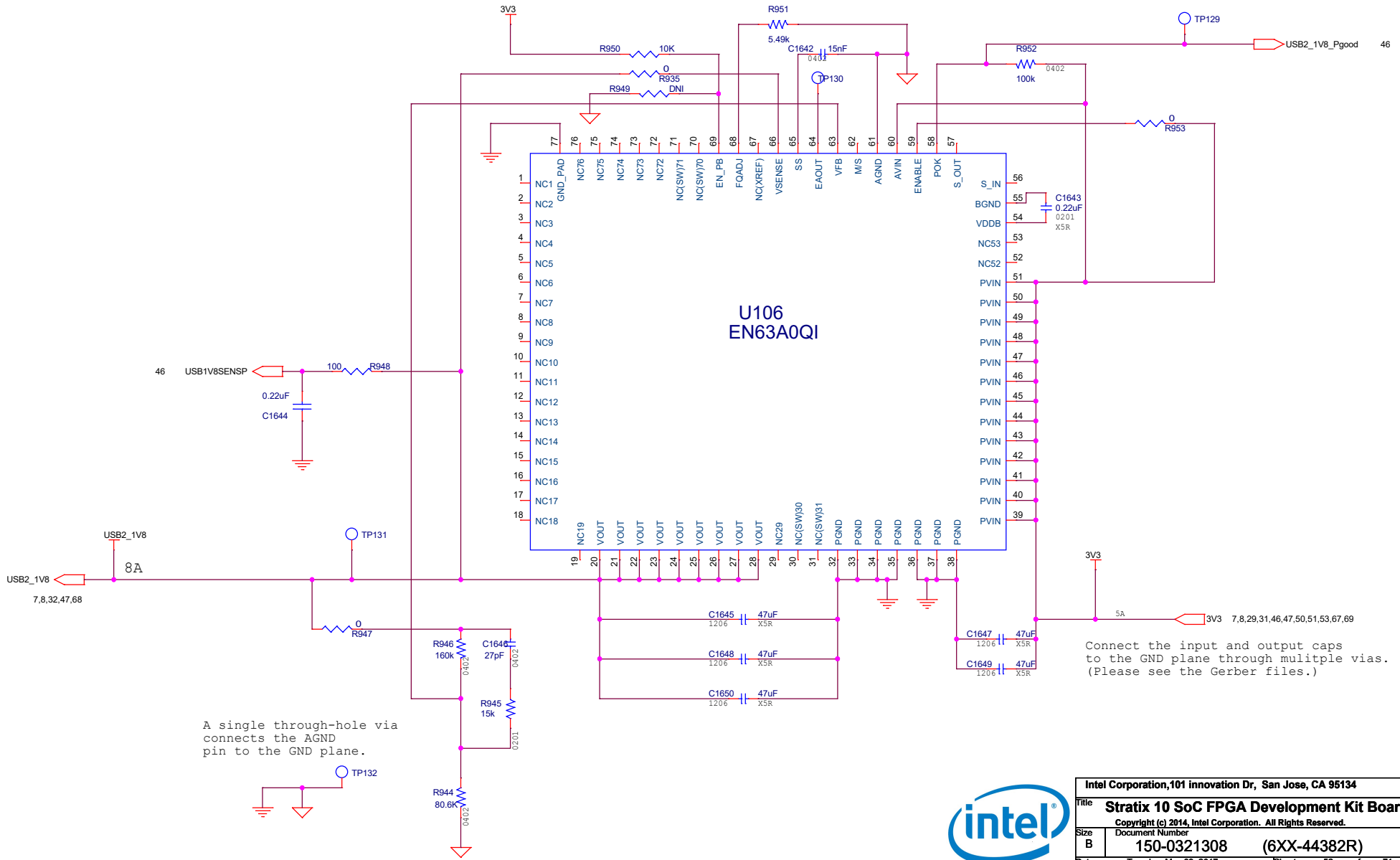
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3V3 to 2V5 Converter



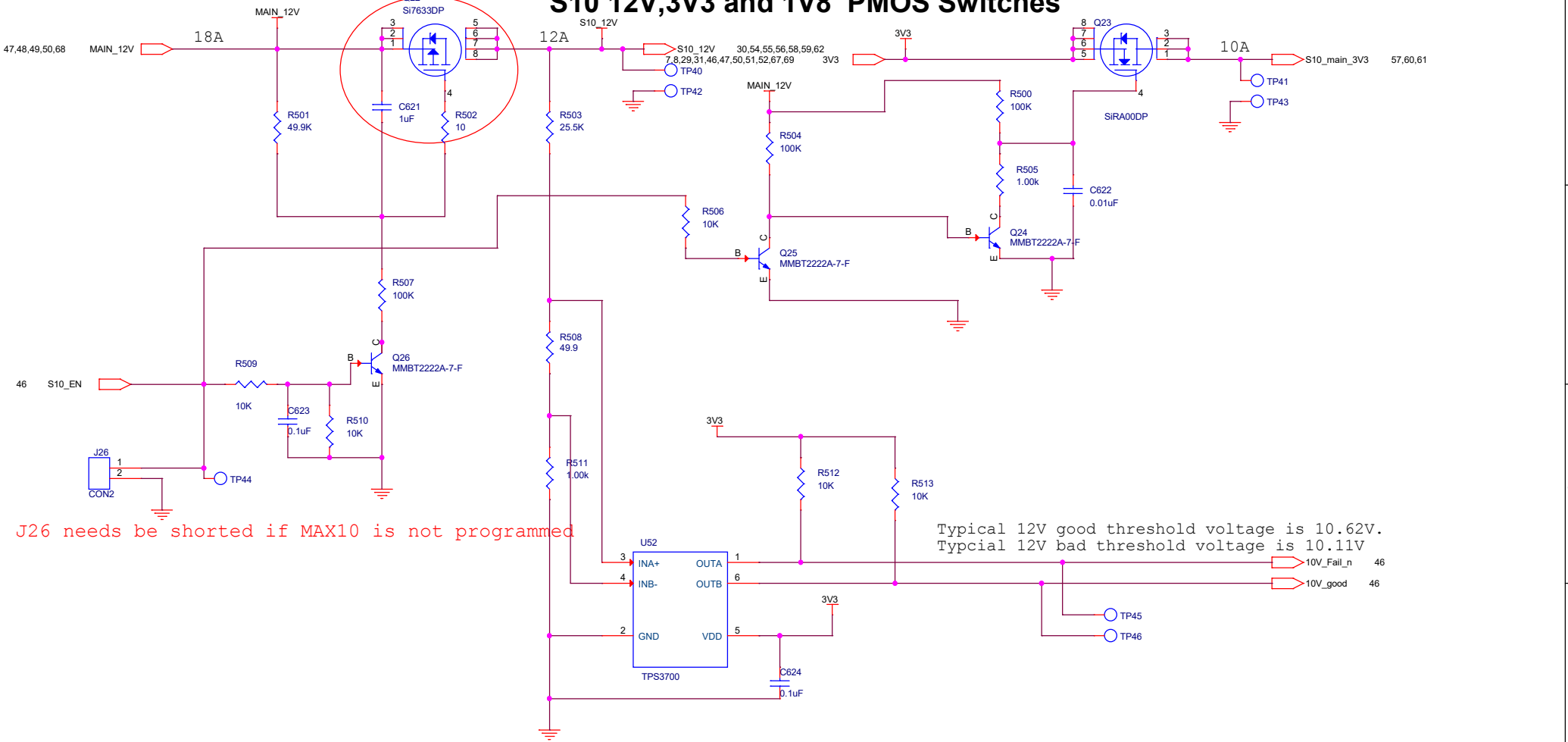
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3.3V to 1.8V Converter



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S10 12V,3V3 and 1V8 PMOS Switches



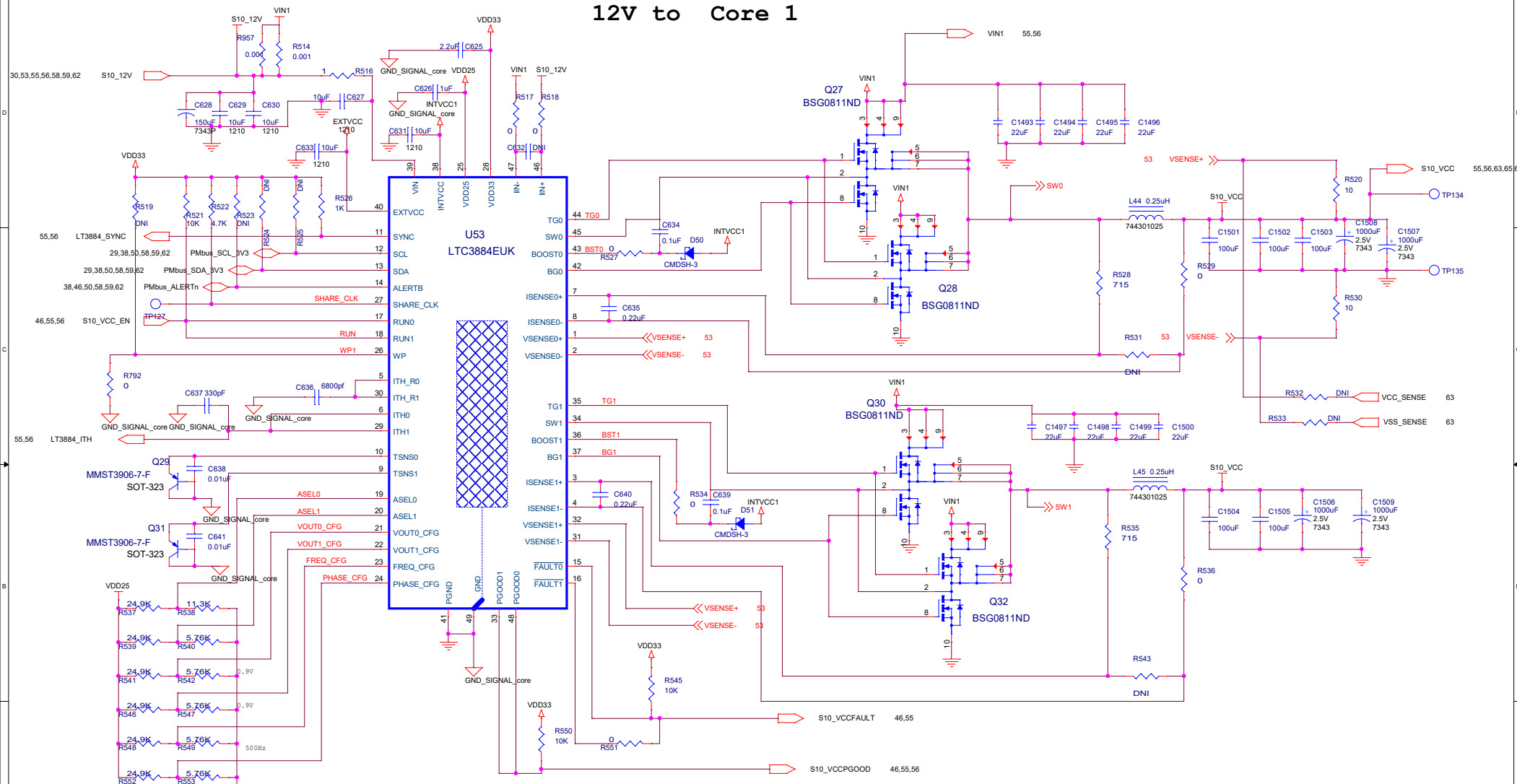
J26 needs be shorted if MAX10 is not programmed

Typical 12V good threshold voltage is 10.62V.
Typical 12V bad threshold voltage is 10.11V



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12V to Core 1



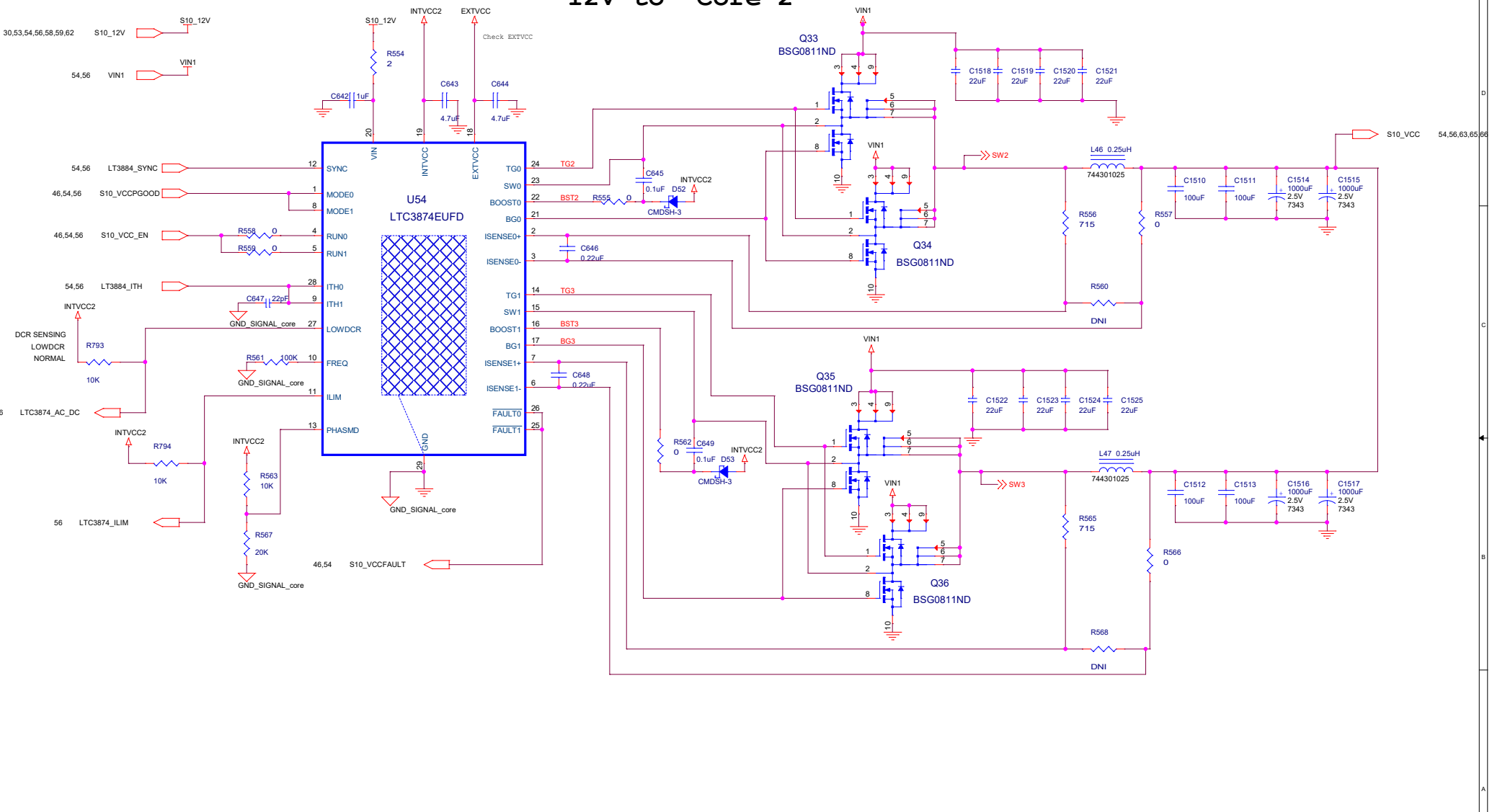
Check Phase define
Need 0.85V core voltage

I2C Address: 0X5A, 0X5B and 0X47



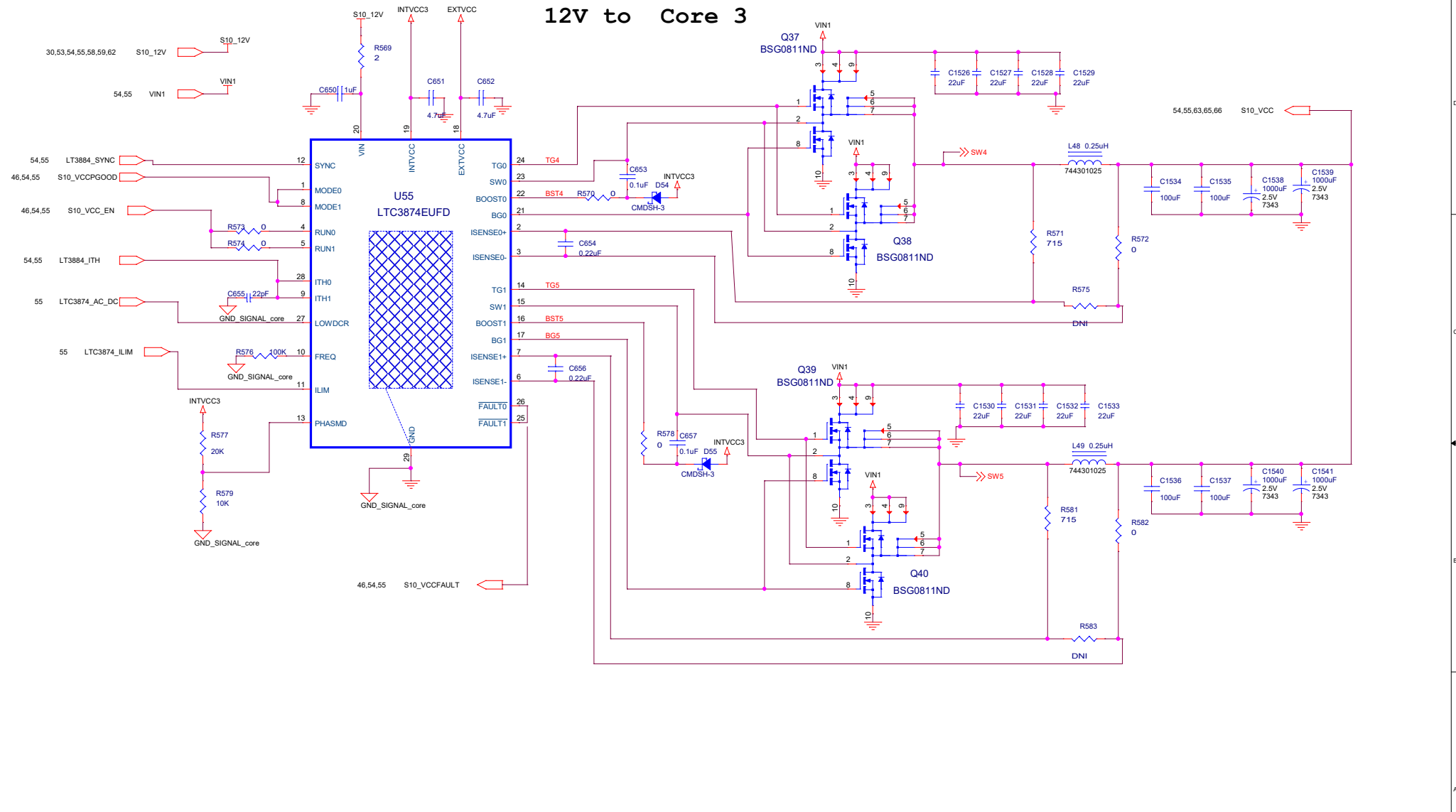
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12V to Core 2



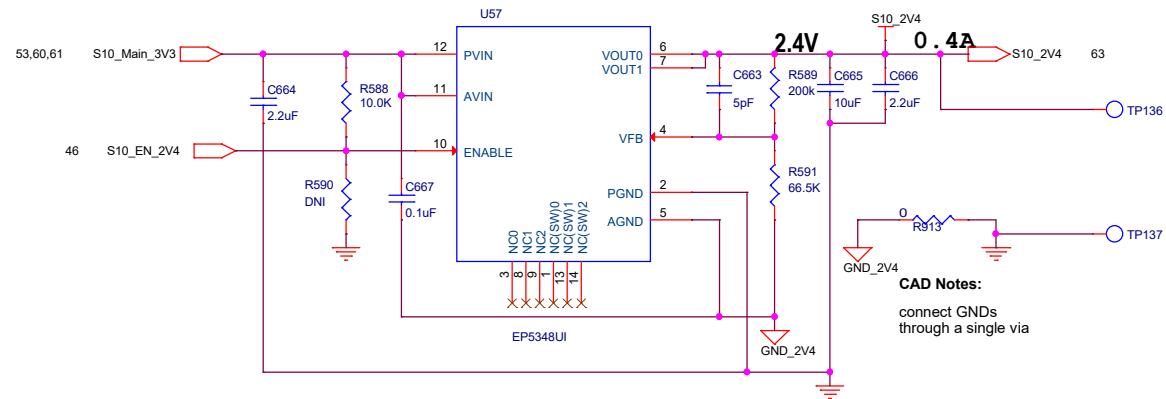
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12V to Core 3

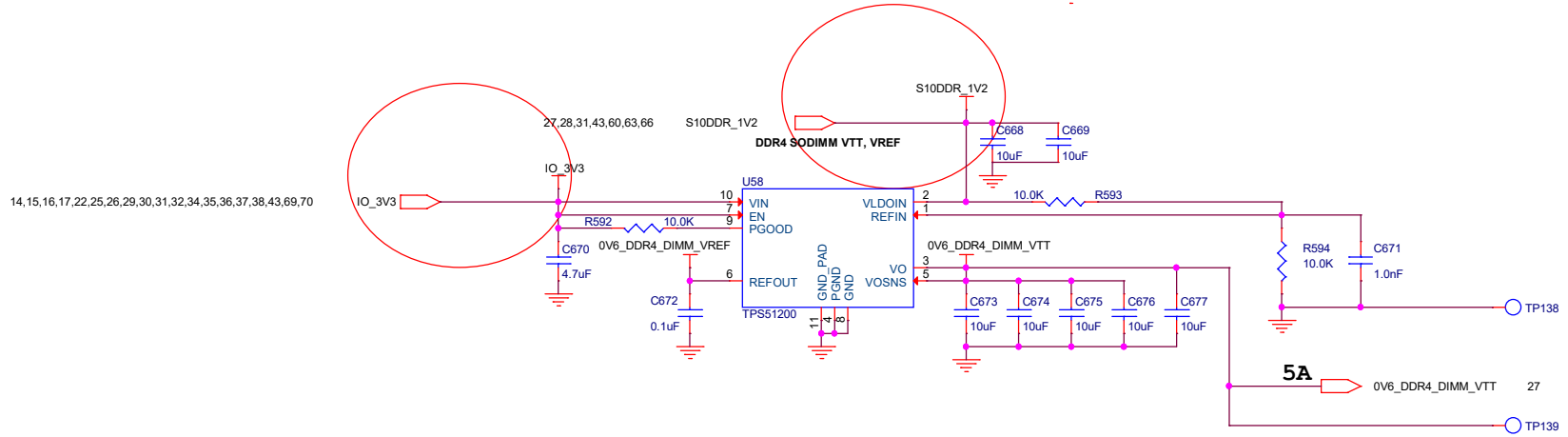


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VTT & 2V4 Power

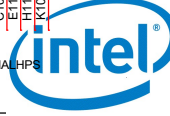
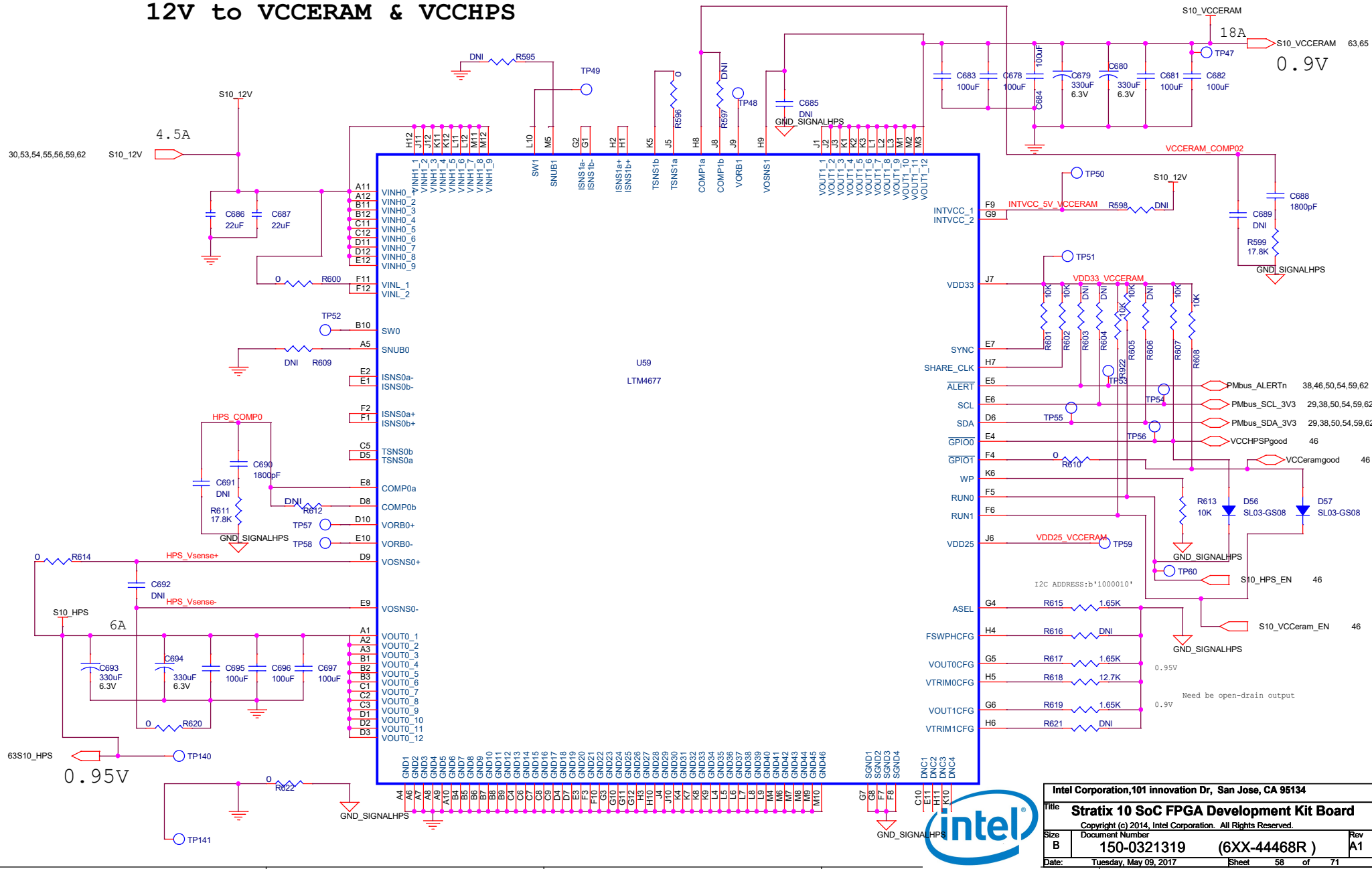


CAD Notes:
connect GNDs through a single via



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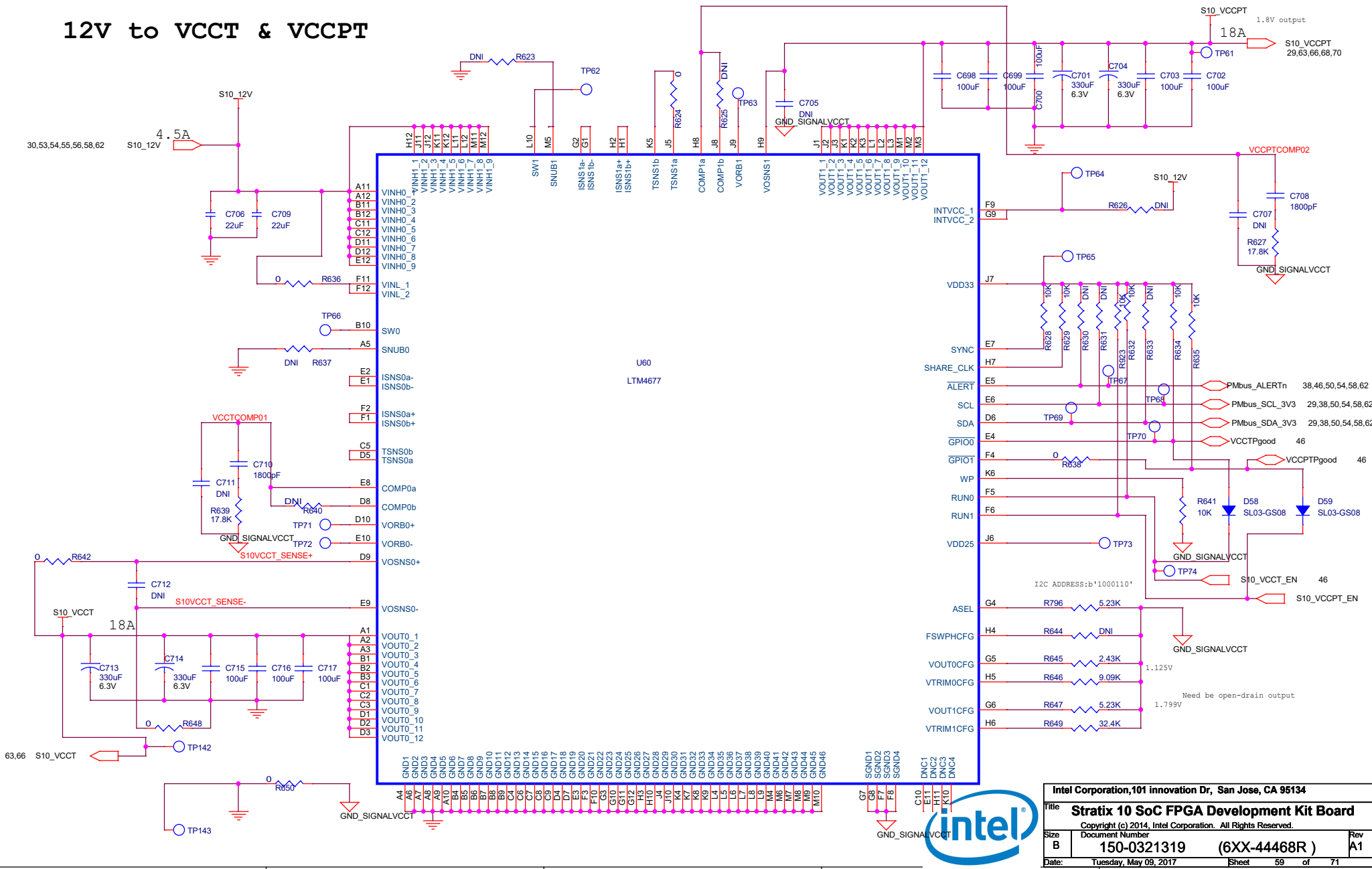
12V to VCCERAM & VVCHPS



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12V to VCCT & VCCPT

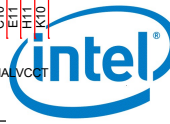
30,53,54,55,56,58,62



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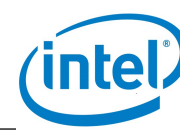
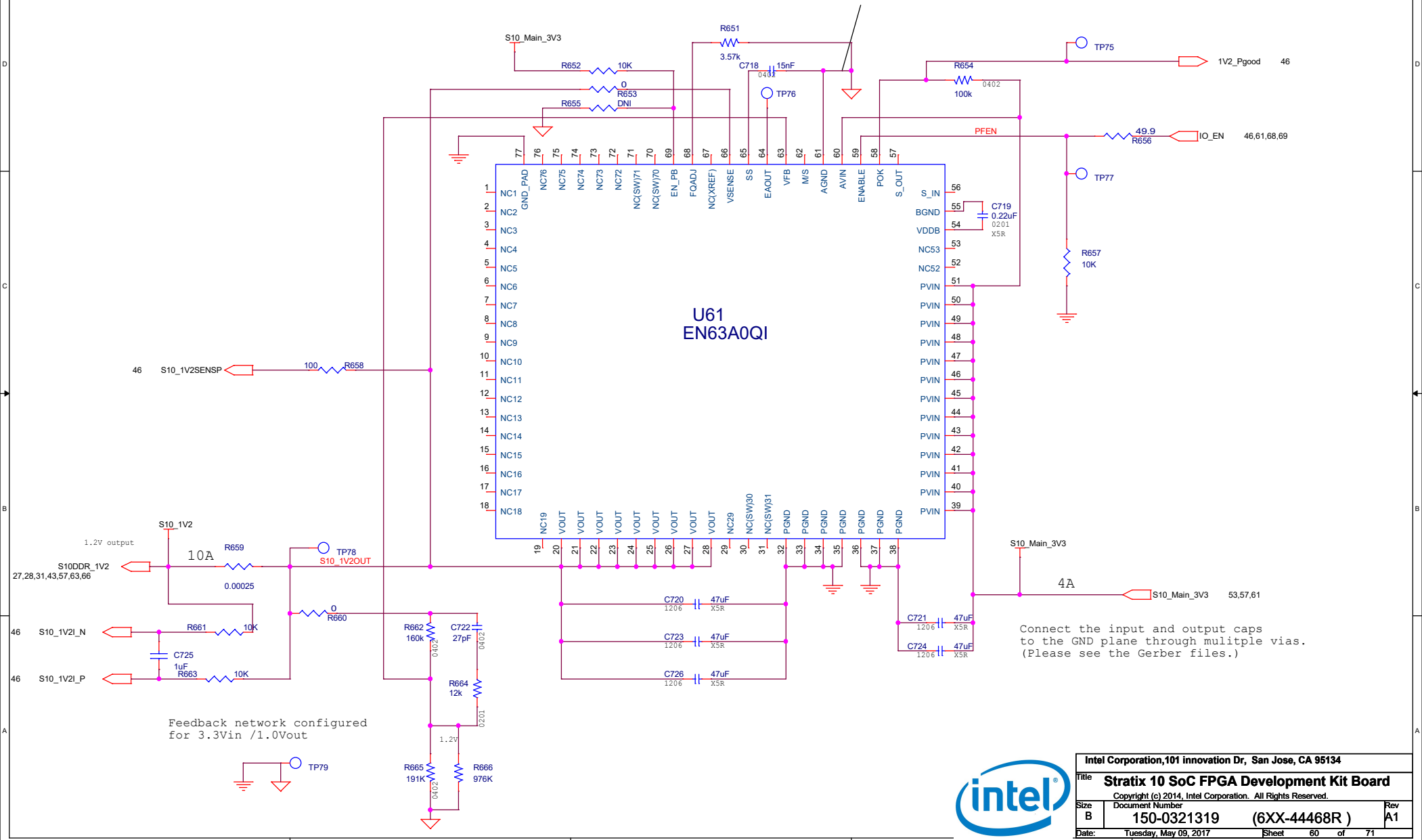
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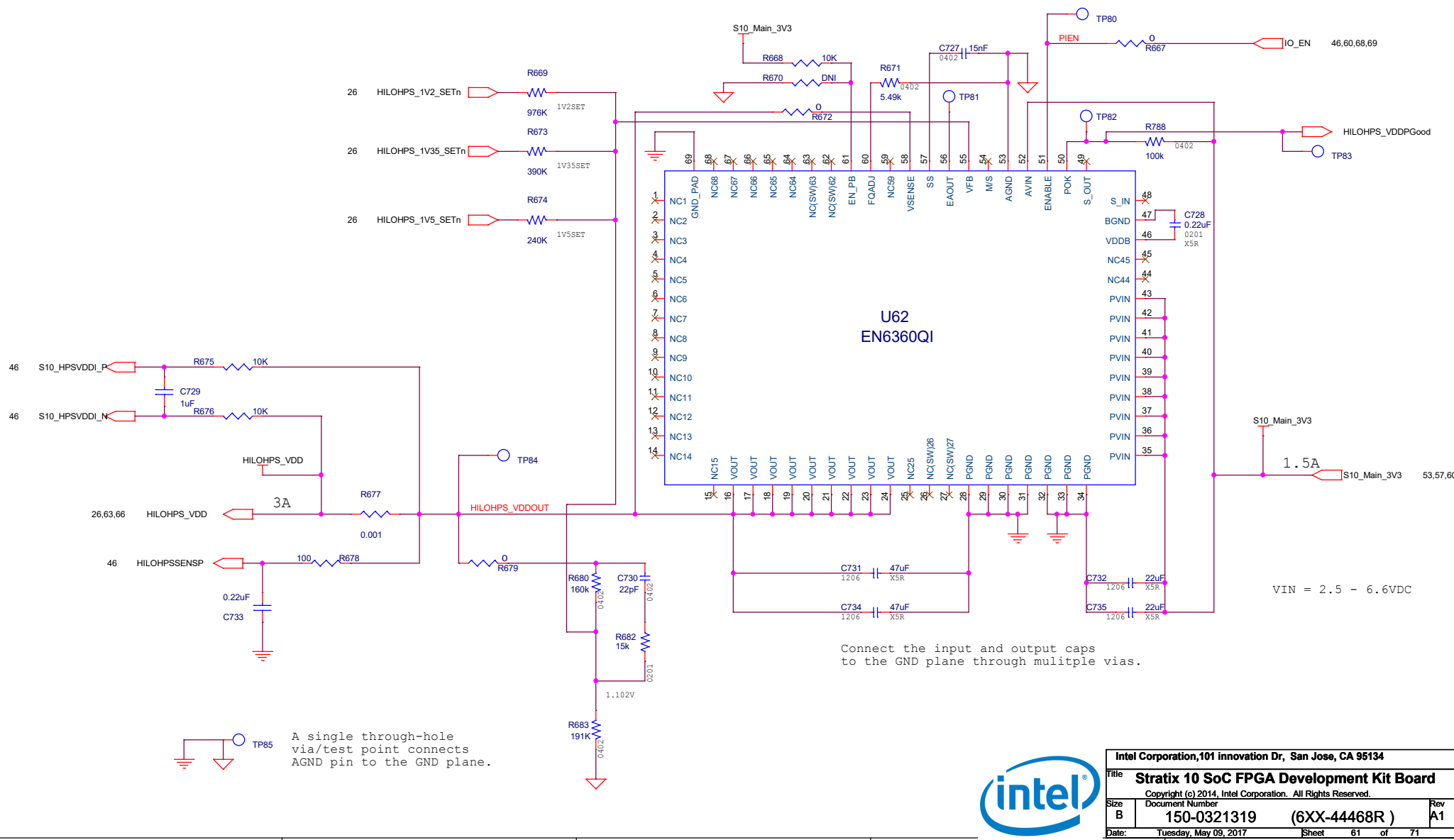
3.3V to 1.2V Converter

A single through-hole via connects the AGND pin to the GND plane.



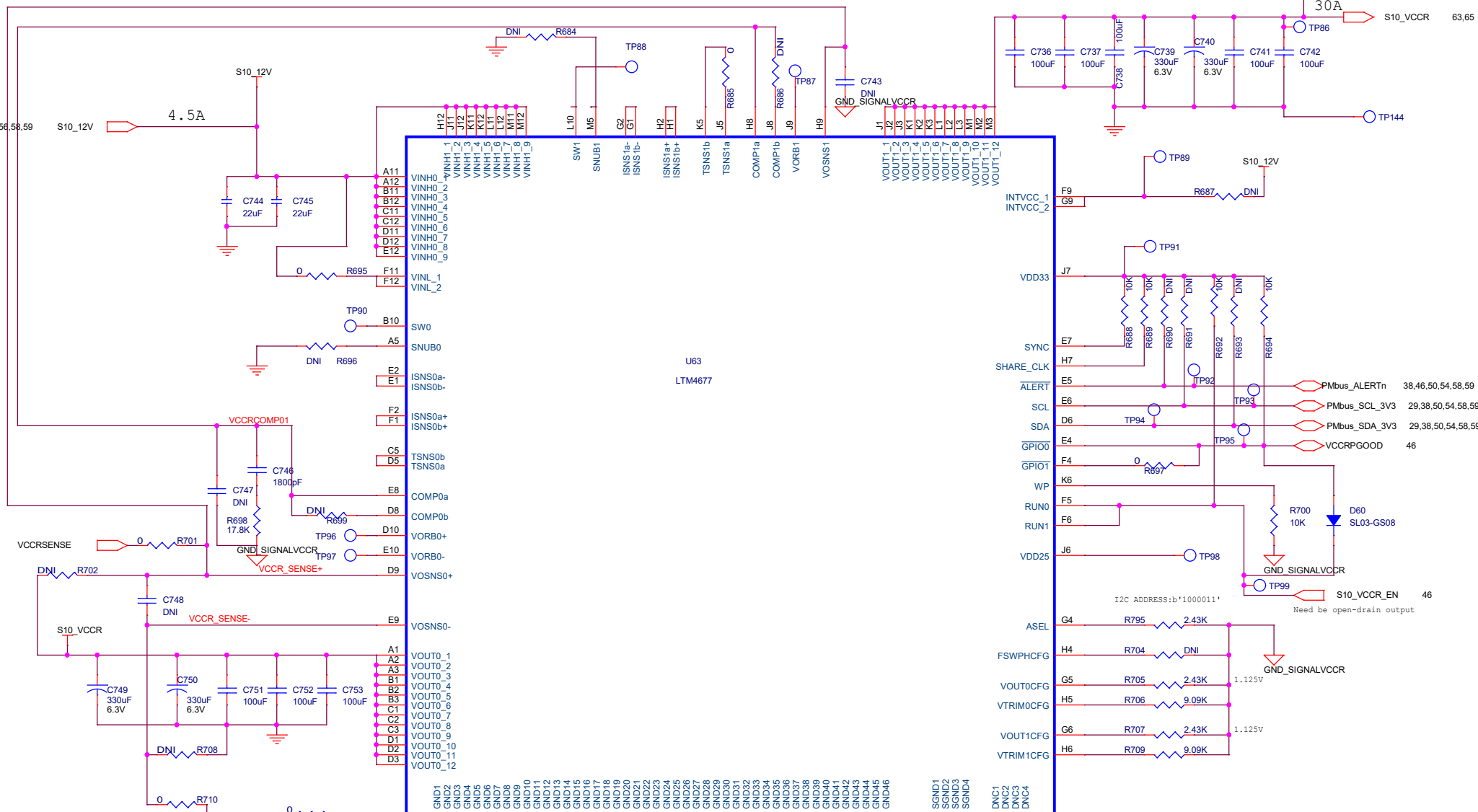
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3.3V to HPS HILO VDD converter



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12V to VCCR Converter



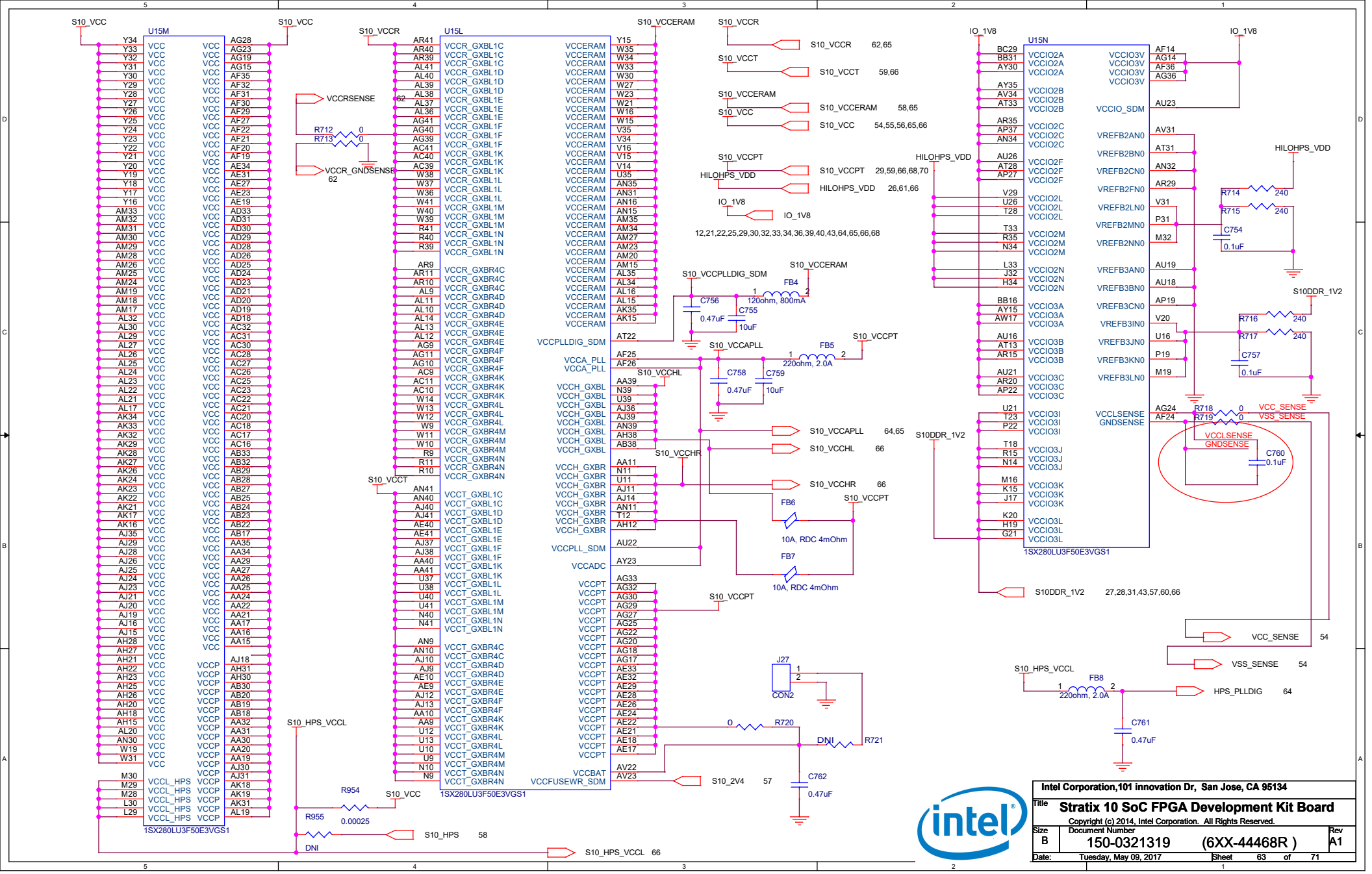
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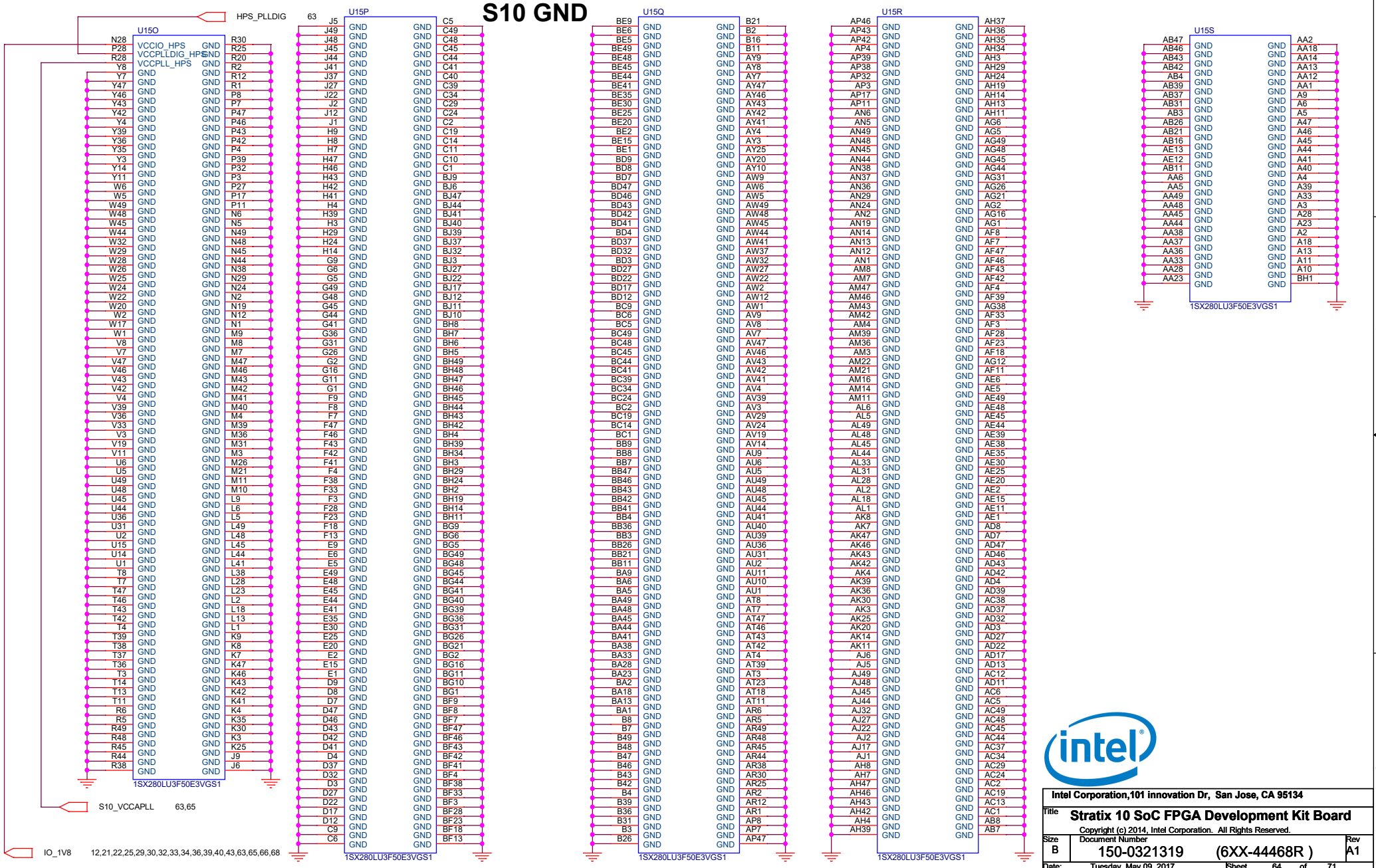
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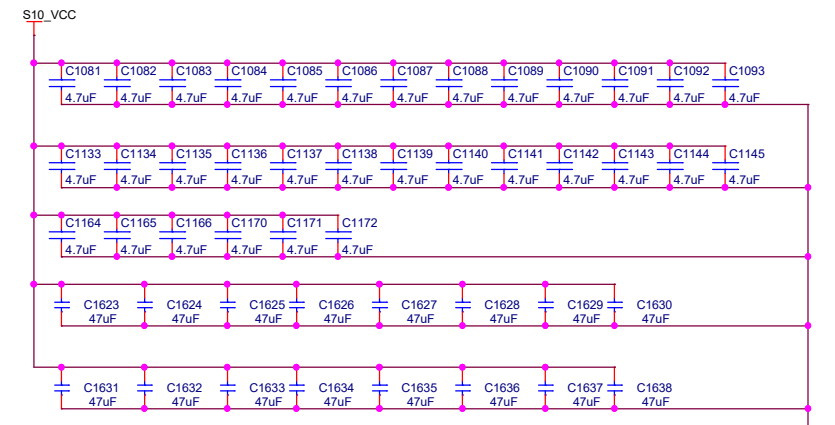
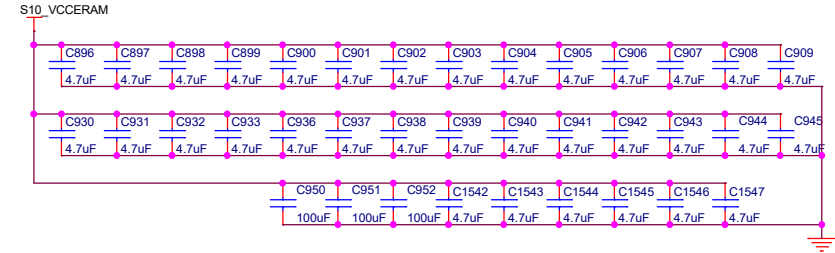
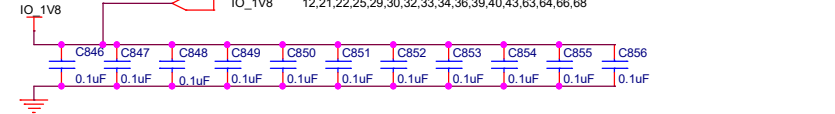
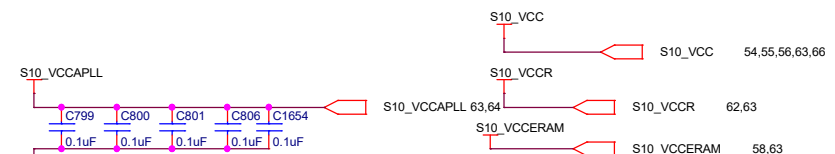
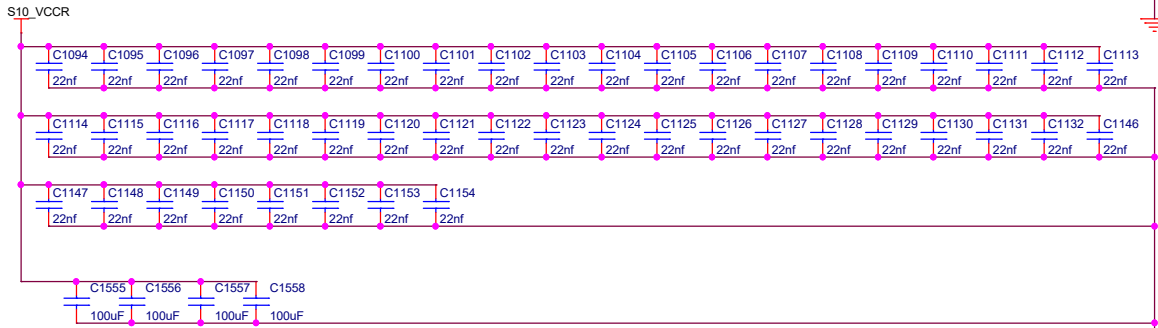
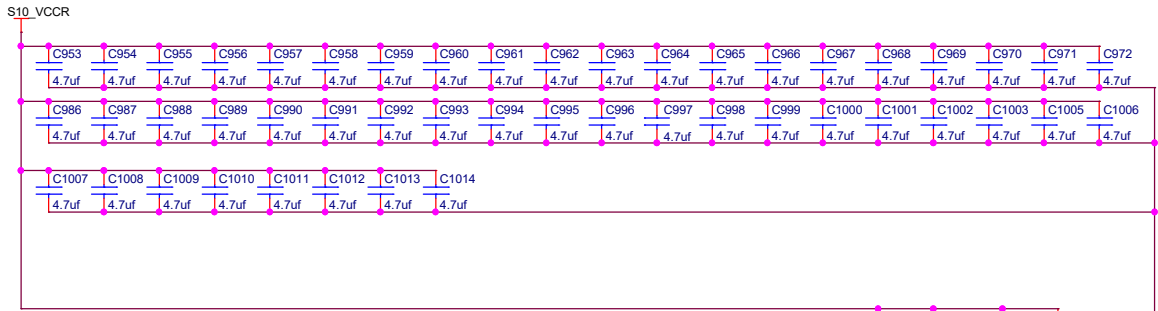
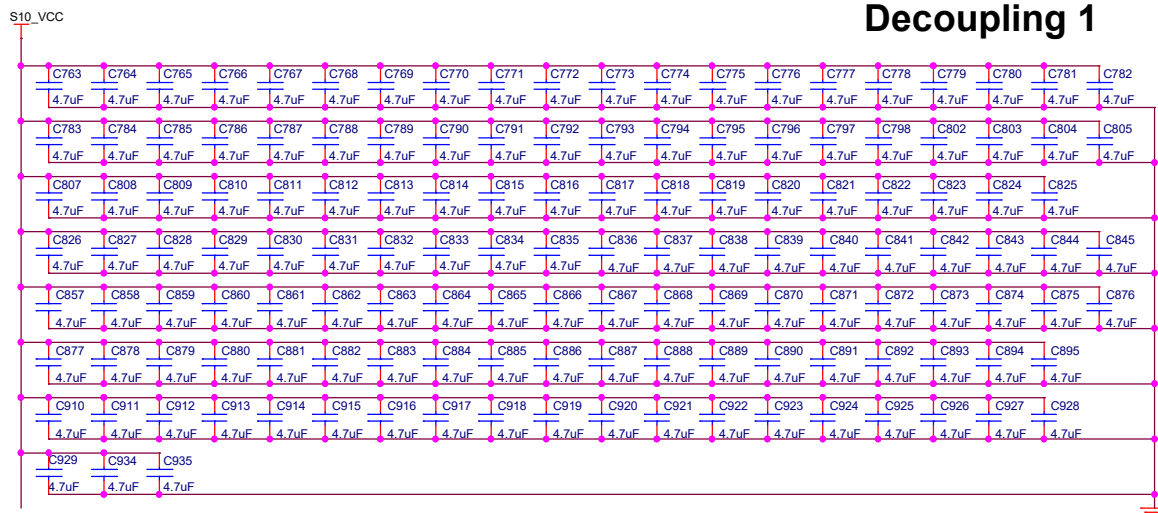
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S10 GND



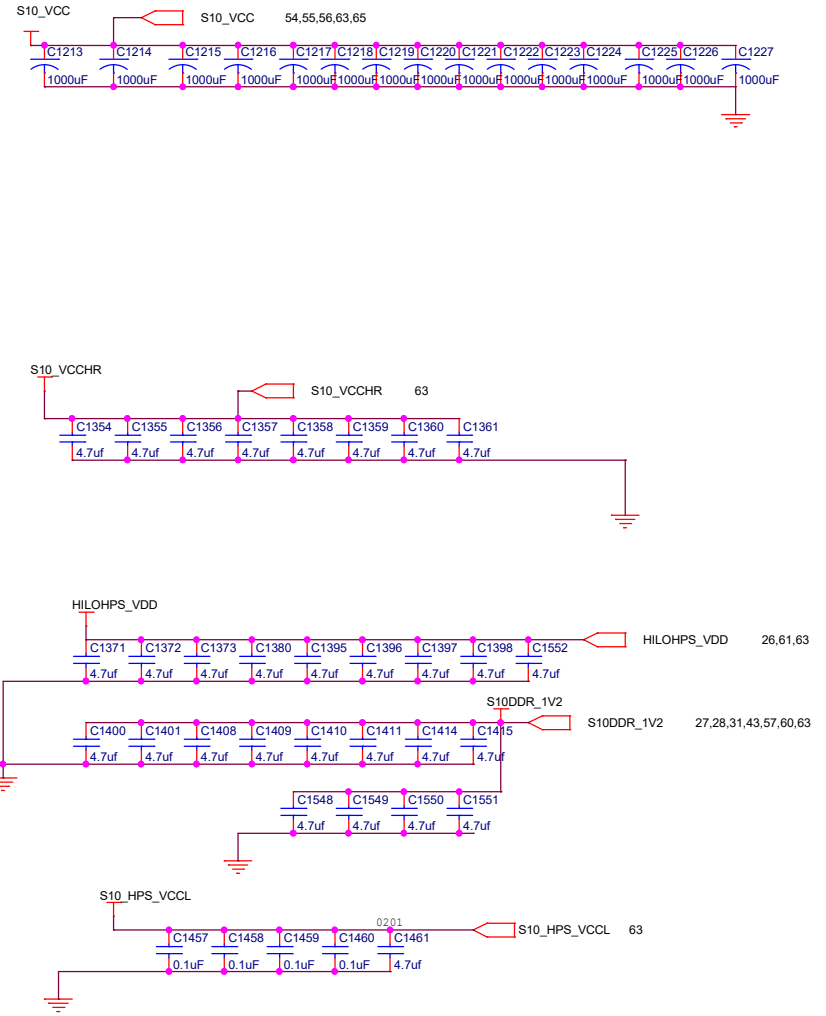
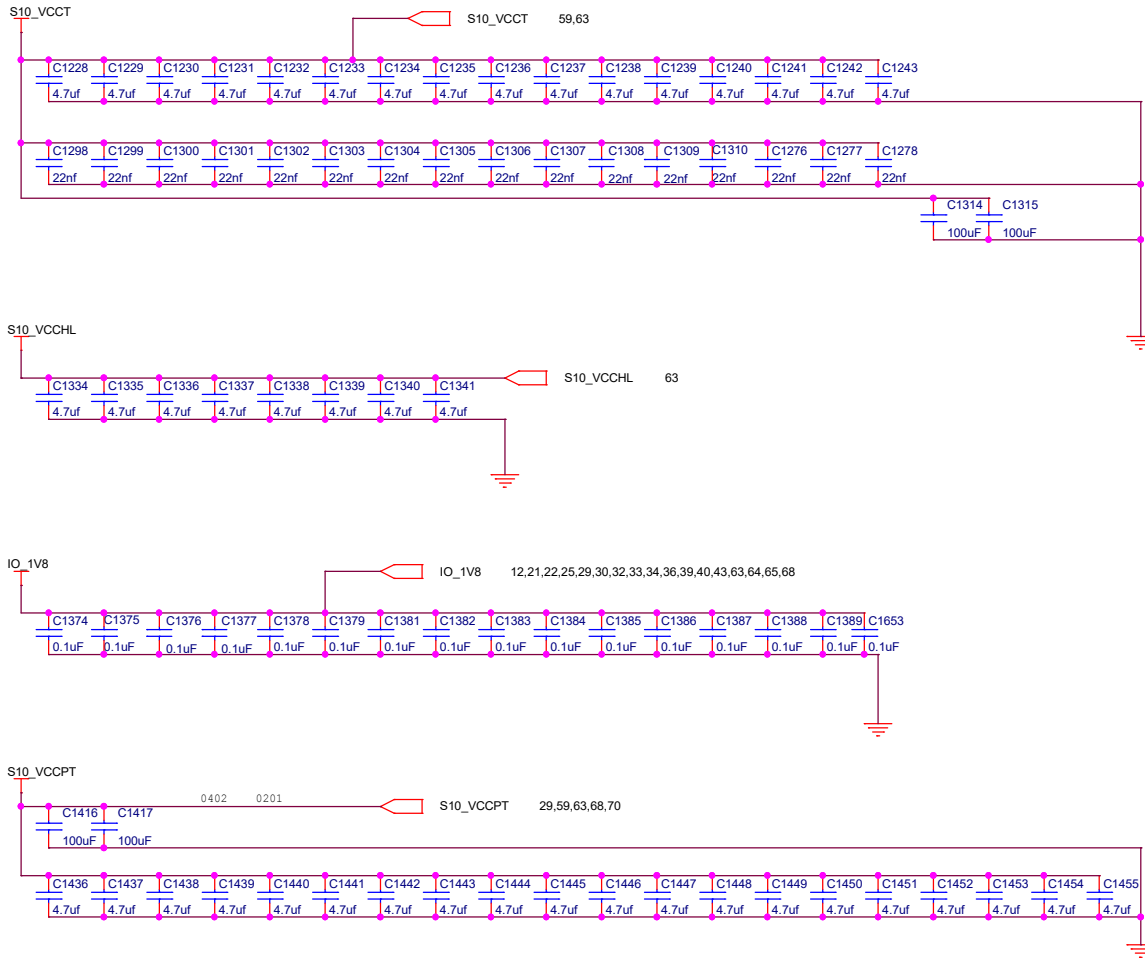
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Decoupling 1



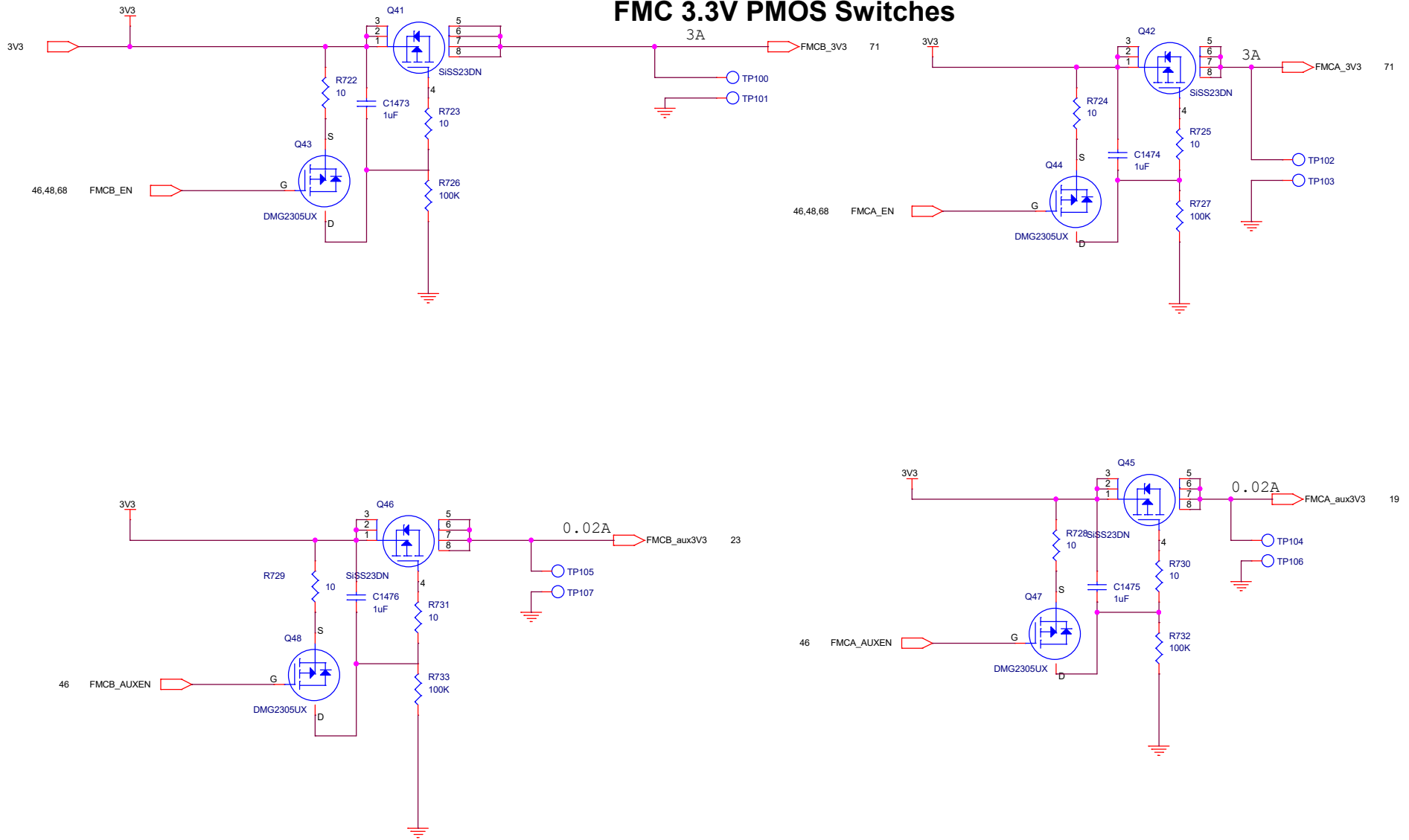
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Decoupling 2



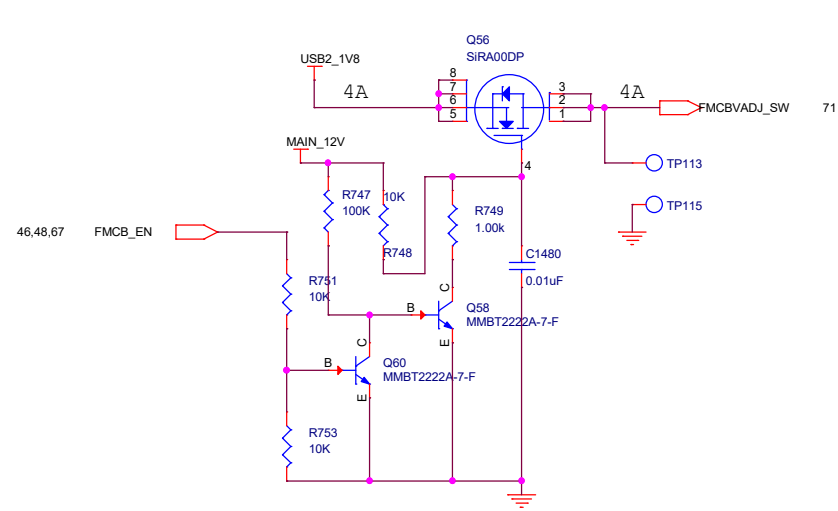
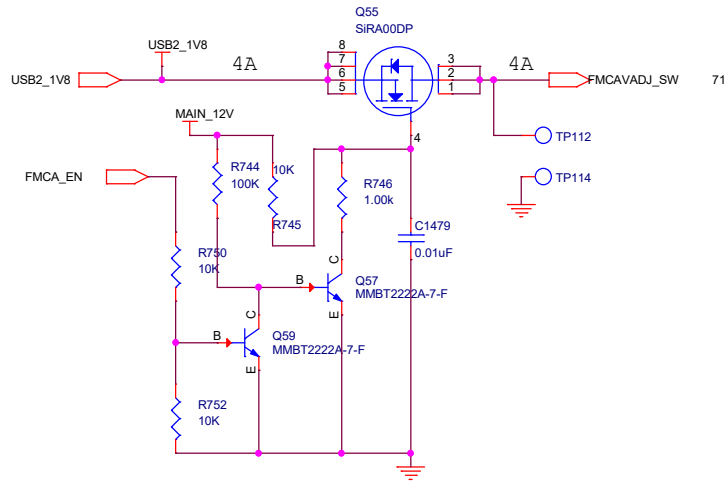
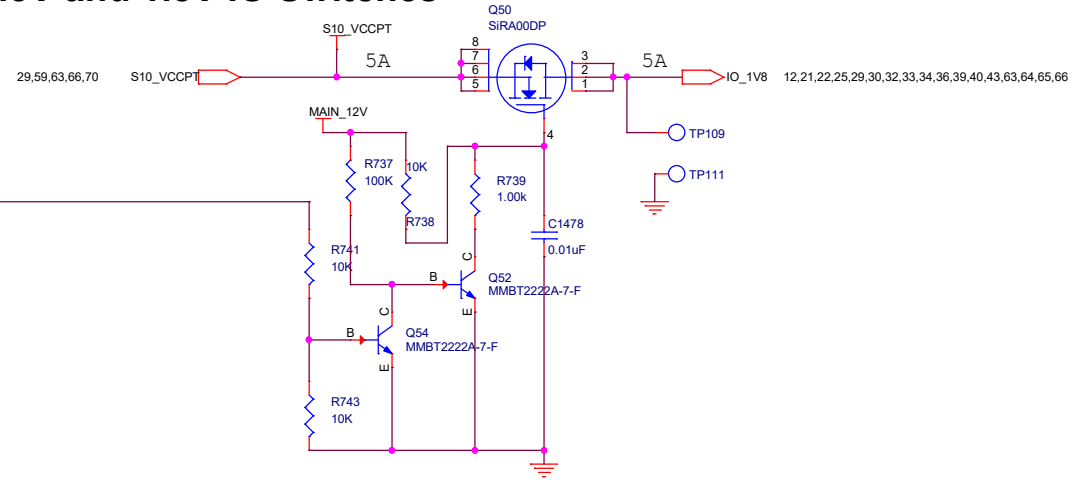
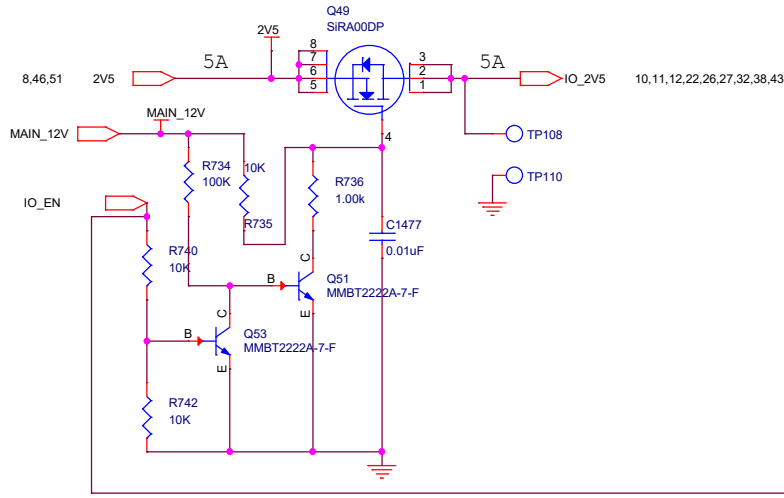
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FMC 3.3V PMOS Switches



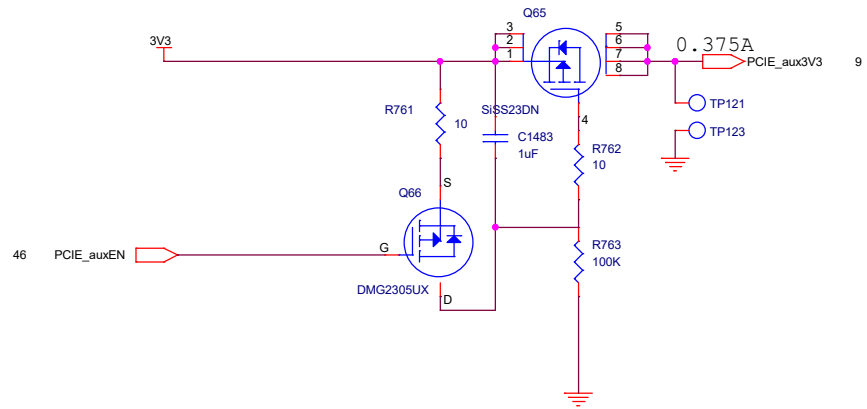
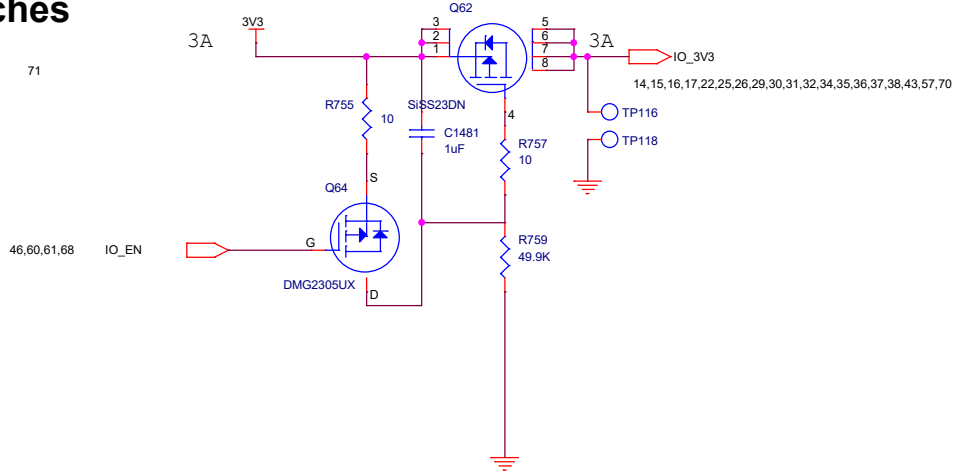
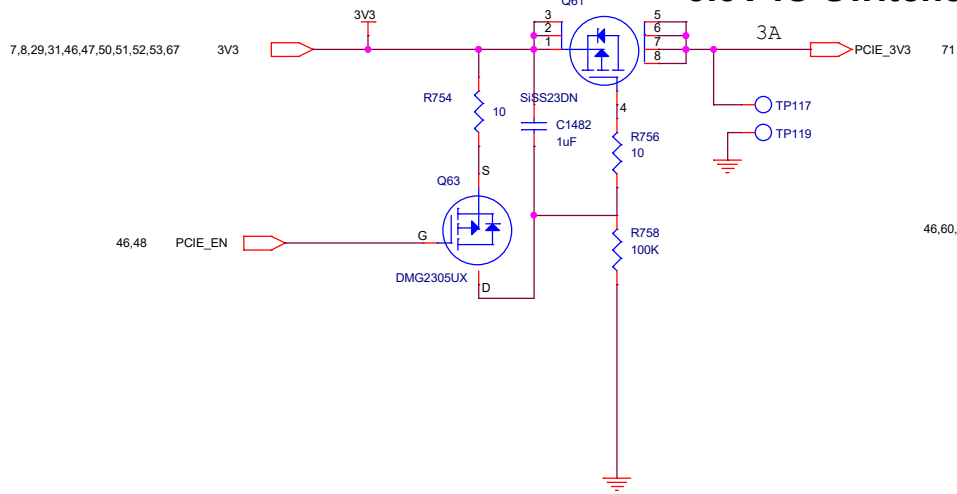
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2.5V and 1.8V IO Switches



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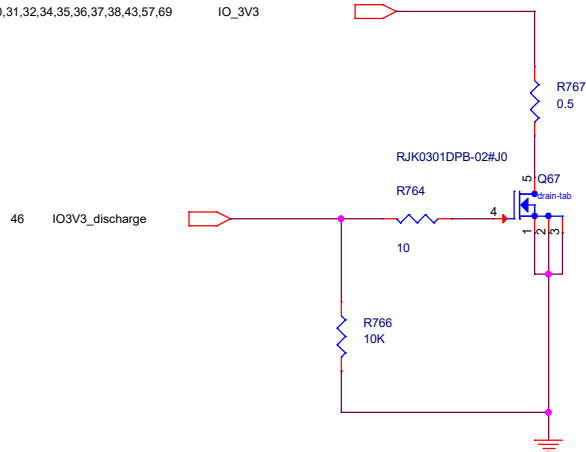
3.3V IO Switches



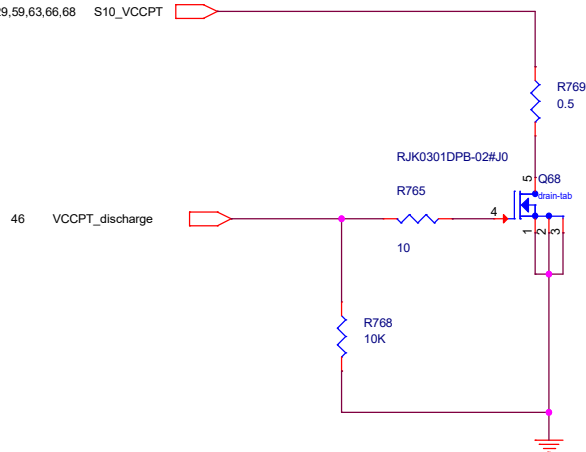
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3.3V and 1.8V Discharge Load

14,15,16,17,22,25,26,29,30,31,32,34,35,36,37,38,43,57,69 IO_3V3



29,59,63,66,68 S10_VCCPT

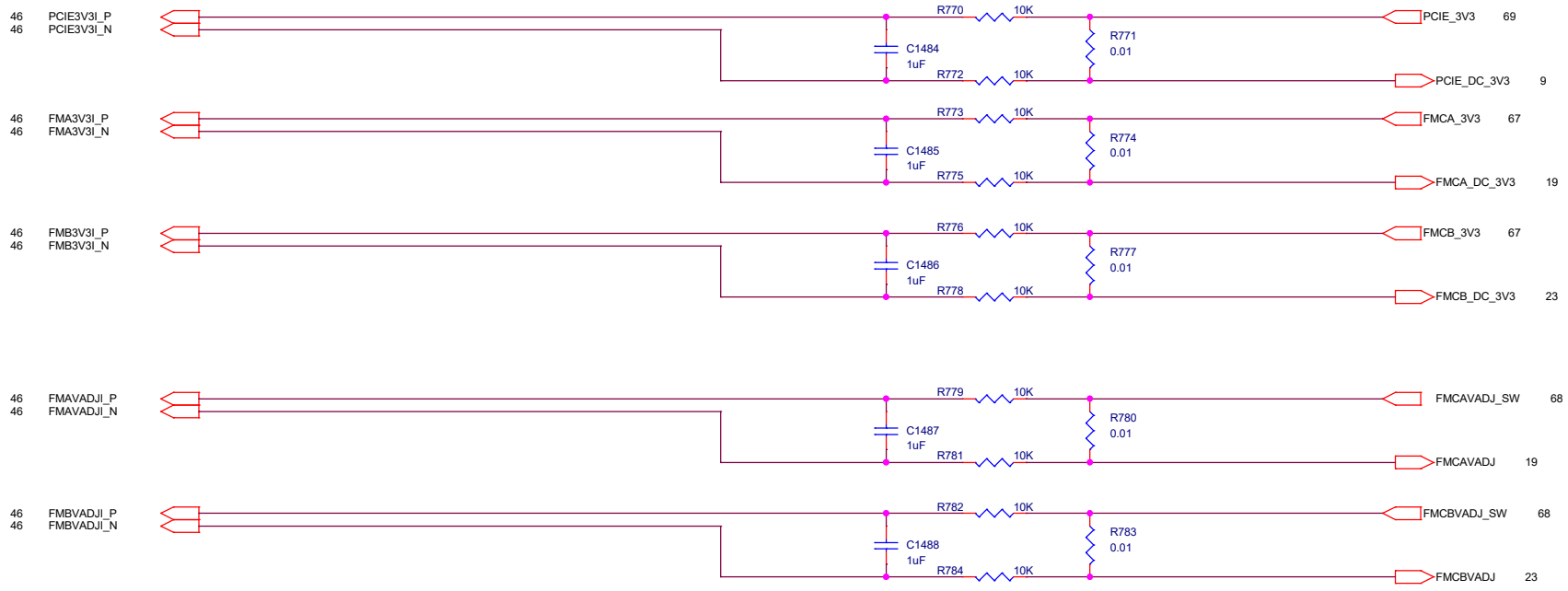


50us Discharge time



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User DC card 3.3V Current Sensors



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