

INTEL[®] STRATIX[®] 10 DEVICE L-TILE/H-TILE TRANSCEIVER DEBUG TOOL

Agenda

- Challenges with the current transceiver debug process
- Why do we need a transceiver debug tool?
- Components and features of the Transceiver Debug Tool
- Steps to run the Transceiver Debug Tool







Challenges with the Current Transceiver Debug Process Measure Transceiver Voltage Check Transceiver Channel Status

Need an external

measurement

equipment

¹ For example, a Signal Tap logic analyzer

Need an extra FPGA logic

analyzer¹

Long test time



Why Do We Need a Transceiver Debug Tool?





Components and Features of the Transceiver Debug Tool





Components and Features of the Transceiver Debug Tool

Transceiver Voltage Debug Tool

Measure VCCER at the data sampling node
Measure VCCET at the transmitter node

Transceiver Status Debug Tool

- Show the following channel status:
- Locked to data and locked to ref
- Calibration, Avalon[®] Memory Mapped (Avalon-MM) busy, and serial loopback
- Check the cable polarity swap

Transceiver Eye Debug Tool

 Measure the height or width of the eye at clock data recovery (CDR) sampling point

(intel)

Four Steps to Run the Transceiver Debug Tool

Step 1: Enable the Altera[®] Debug Master Endpoint (ADME) and compile the design

Native PHY Intellectual Property (IP)

Stratix 10 L-Tile/H-Tile Tra altera_xcvr_native_s10_htile	Insceiver Native	PHY	
PMA configuration rules:		basic 💌	
Transceiver mode:		TX/RX Duplex 👻	
Number of data channels:		4	
Data rate:		25781.25	Mbps
Enable datapath and interface reco	nfiguration		
🗹 Enable simplified data interface			
Provide separate interface for each	channel		
Enable double rate transfer mode			
TX PMA RX PMA Enhanced PCS	PCS-Core Interface	Analog PMA Settings	Dynamic Reconfiguration
Finale dynamic reconfiguration			
E and off and off and the second gold atom			
Ena le Altera Debug Master Endpol	nt		
Enalle Altera Debug Master Endpoi	nt the status of AVMM ar	bitration with PreSICE	

PCIe* IP

Avaion-MM Stratix 10 Hard IP for PCI Express altera_pcie_s10_hip_avmm_bridge IP Settings Example Designs System Settings Avaion-MM Settings Base Address Registers Device Identificat Imable HIP dynamic reconfiguration of PCIe read-only registers Enable HIP dynamic reconfiguration Enable Transceiver dynamic reconfiguration Enable Native PHY, ATXPLL and IPLL ADME for Transceiver Toolkit Imable PCIe Link Inspector

Ethernet IP

P Example Design Main General Options Device family: Target transceiver tile: PCS/PMA Options PCS/PMA Options H Traference frequency: 644.53125 ▼ MH2 MH2 MAC Options Enable link fault generation Enable Ink fault generation Enable TX CRC insertion
Main General Options Device family. Target transceiver tile: PCS/PMA Options Chable RS-FEC PHY reference frequency. MHz MHz MAC Options Chable link fault generation Chable Ink fault generation Chable IX CRC insertion
Device family: Stratu 10 Target transceiver tile: PCS/PMA Options PCS/PMA Options MHz MHz MHz MHz Chable link fault generation Enable Inx fault generation Enable TX CRC insertion
Enable RS-FEC PHY reference frequency. 644.53125 MHz MHz MHz Enable link fault generation Enable TX CRC insertion
HAC Options Enable link fault generation Enable TX CRC insertion
Enable link fault generation
Enable TX CRC insertion
Enable preamble passthrough
Enable RX/TX statistics counters
Enable strict SFD check
Coofiguration, Debug and Extension Options
☑ E able Altera Debug Master Endpoint (ADME)



Four Steps to Run the Transceiver Debug Tool

Step 2: Program the device.

Step 3: Load the design in the system console.

Step 4: Use "cd" to change the directory where you have saved the tools script file and source "S10_Ltile_Htile_Transceiver_Debug_Tool_V4p0.tcl"

System Console - Toolkits		cd {c:\users\kbalakri\system_console\scripts}
File Tools Help		
System Explorer c	C Tooliks	
connections devices designs design_instances design_instances	TACC Tracking (Beina) The AcC Tracket Also for the evolution of ACC spail path performance. The associated hardware detected.	<pre>% source S10 Ltile Htile Transceiver Debug Tool V4p0.tcl] *** ** ** ** ** ** ** ** ** ** ** ** **</pre>
	But Analyzer (Teta) The But Analyzer product relations analysis of but traffic in the system. Termical The Transcriptor Toublit The Transcriptor Toublit The Transcriptor Toublit	S1D_Ltile_Htile_Transceiver_Voltage_Debug_Tool_v4p0 Load Start - Current time- 14hr_44min_11sec alcera_xcvr_native_s10_htile.slave alcera_xcvr_native_s10_htile.slave alcera_xcvr_native_s10_htile.slave alcera_xcvr_native_s10_htile.slave S1D_Ltile_Htile_Transceiver_Voltage_Debug_Tool_v4p0 Load Stop - Current time- 14hr_44min_12sec *** *** *** *** *** *** *** *** *** **
Messages c	Inst Creage Partneh Correctors Tol Connote d	Tools Loaded Click "Tools" dropmenu on the top left corner of System Console, Select the debug tool ** ** ** ** ** ** ** ** ** ** ** ** **
Add for register Service pac. A service anned Spack It also: A service anned Spack It also: Friehed discovering URA come. Friehed discovering URA come. Freiched discovering URA come. Auto Service 1000 Come. A	This Fil consils provides secress to the hardware moduler instanciated in your FFG. You can use System Simonic free all of the following purposes: * To start, stop, or stop & start & Start Di processor * To read are write writein Reacty-Reped Arxies Will system Simon Simonic Arabit * To read the SOFC System Levis and the System Simonic Arabit * To read the SOFC System Levis and the System Simonic Arabit * To read the SOFC System Levis and the System Simonic Arabit * To read the SoFC System Levis Levis and the System Levis the Instantiated system level show (GAD) modes In addition, the discretury description Discr/septem_consols/scripts remethins Toi files that provide miscellamous willities and examples of how to screen the formulating provide miscellamous will the same supposed screen the formulating provide miscellamous will the same screen the your screen	User will observe these tabs in the system console
	od (c:\ueers\Waldit\byptem_comsoletuccipts) sewco SiQittle Mtile Transceiver Schug Teol [Vig0.tc] .	Note: Refer to the backup slides for steps on how to program the device and load the sof file



An Example of a Test Setup



TRANSCEIVER VOLTAGE TOOL

PCB Trace Properties

PCB trace resistance can be calculated as



Intel[®] Stratix[®] 10 Signal Integrity (SI) Development Kit



Sense Trace

Sense trace measures the voltage nearest to the device





Solution

Intel[®] Stratix[®] 10 L-Tile/H-Tile Transceiver Voltage Debug Tool

Measure the voltage internally

Measured voltage value accessed via the JTAG or System Console



Intel[®] Corporation

(intel)

Intel[®] Stratix[®] 10 L-Tile/H-Tile Transceiver Voltage Debug Tool Algorithm



(intel)

Intel[®] Stratix[®] 10 Device L-Tile/H-Tile Transceiver Voltage Tool

nments						
* ** ** ** ** **	** ** ** ** ** ** ** ** **	**	** ** ** ** ** ** ** ** **	** **		
ool v4p0 based o	n 017.1.2					
o use this tool ADI	ME should be Enabled					
atarate < 17.4Gb	ps - VCCET/VCCER - Min 1.	DV Typ 1.03V Max 1.06	v			
atarate > 17.4Gb	ps - VCCET/VCCER - Min 1.	1V Typ 1.12V Max 1.14	v			
ccuracy : +-18mV						
* ** ** ** ** **	** ** ** ** ** ** ** ** **	* ** ** ** ** ** ** ** **	** ** ** ** ** ** ** ** **	** ** **		
asurement Type	2000					
Measure Voltage	es once - All PHY 📄 🔲 👩	ntinuous update Disabled/ch	neck to Enable 🛛 📄 Stop th	e current measurement	LogFile	
/ + Channel						
/ + Channel devices_15G280H	H(151 251 351) @2#USB	-1#Stratix_10H_SI_Dev_Kit	e100_1 ex_100g_inst ex_	100g_inst xcvr caui4_xcvr,	_644 alt_xcvr_native_optional_rcfg_logi	ic
/ + Channel devices_15G280H	H(151 251 351) @2#USB	-1#Stratix_10H_SI_Dev_Kit	e100_1 ex_100g_inst ex_ date Disabled/check to Enab	100g_inst xcvr caui4_xcvr	_644 alt_xcvr_native_optional_rcfg_logi	ic
v + Channel devices_15G280+ Measure Vol	H(151 251 351) @2#U5B age Once	-1#Stratix_10H_SI_Dev_Kit	e100_1 ex_100g_inst ex_ date Disabled/check to Enab	100g_inst xcvr caui4_xcvr le	_644]alt_xcvr_native_optional_rcfg_logi	ic
 + Channel devices_1SG280F Measure Vol e100_1 ex_100g 	H(151 251 351) @2#U5B age Once inst ex_100g_inst xcvr cau	-1#Stratix_10H_SI_Dev_Kit continuous up i4_xcvr_644 alt_xcvr_nativ	e100_1 ex_100g_inst ex_ date Disabled/check to Enab e_optional_rcfg_logic	100g_inst xcvr caui4_xcvr, le	.644 alt_xcvr_native_optional_rcfg_log	ic
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/ + Channel devices_15G280k Measure Vol e100_1 ex_100g VCCER VCCER VCCET devices_15G280k Measure Vol e100_2 ex_100g	H(151 251 351) @2#USB age Once inst ex_100g_inst xcvr cau Ch0 1.11578V 1.13380V H(151 251 351) @2#USB age Once inst ex_100g_inst xcvr cau Ch0	-1#Stratix_10H_SI_Dev_Kit continuous up i4_xcvr_644 alt_xcvr_nativ Ch1 1.11578V 1.13380V -1#Stratix_10H_SI_Dev_Kit continuous up i4_xcvr_644 alt_xcvr_nativ Ch1	e100_1 ex_100g_inst ex_ date Disabled/check to Enab e_optional_rcfg_logic Ch2 1.11578V 1.13380V e100_2 ex_100g_inst ex_ date Disabled/check to Enab e_optional_rcfg_logic Ch2	100g_inst xcvr caui4_xcvr le Ch3 1.11578V 1.13380V 100g_inst xcvr caui4_xcvr, le Ch3	644 alt_xcvr_native_optional_rcfg_log Stop the current measurement Status Done Done 644 alt_xcvr_native_optional_rcfg_log Stop the current measurement Status	ic
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Intel[®] Stratix[®] 10 Device L-Tile/H-Tile Transceiver Voltage Tool

S10_Ltile_Htile_Transc	eiver_Voltage_Debug_Tool_v	/4p0_Beta				
Comments						
** ** ** ** ** **	** ** ** ** ** ** ** **	** ** ** ** ** ** ** ** **	** ** ** ** ** ** ** **	** ** **		
Tool_v4p0 based o	on Q17.1.2					
To use this tool AD	ME should be Enabled					
Datarate < 17.4G	bps - VCCET/VCCER - Min 1.	0V Typ 1.03V Max 1.06	W			Tool automatically finds
Datarate > 17.4G	bps - VCCET/VCCER - Min 1.	1V Typ 1.12V Max 1.14	W			
Accuracy : +-18m	V					all the PHY instance
** ** ** ** ** **	** ** ** ** ** ** ** **	** ** ** ** ** ** ** ** **	** ** ** ** ** ** ** ** **	** ** **		
Maaguwamagh Tuma						
Measurement Type	200					
Measure Voltag	ges onc <mark>e - All PHY 📄 🔲 co</mark>	ntinuous update Disabled/d	neck to Enable 👘 📄 Stop t	he current measurement	LogFile	To all as the section all sufficients
						I ool automatically finds
Phy + Channel						all the channels in the
devices_15G280	HH(151 251 351) @2#USB	-1#Stratix <mark>_</mark> 10H_SI_Dev_Ki	: e100_1 ex_100g_inst ex	_100g_inst xcvr caui4_xcvi	644 alt_xcvr_native_optional_rcfg_logic 🔴 🗕	instantiated DHV instance
Meacure Vo			data Dicabled/check to Ena	bla	Stop the current measurement	
ineasure vo	itage of ite		idate bisabled/thetk to tha	DIC	Dtop the current measurement	
e100_1 ex_100g	g_inst ex_100g_inst xcvr cau	ii4_xcvr_6 <mark>4</mark> alt_xcvr_nativ	e_optional_rcfg_logic			
	Ch0	Ch1	Ch2	Ch3	Status	Tool automatically finda
VCCER	1.11578V	1.11578V	1.11578V	1.11578V	Done	Tool automatically linus
VCCET	1.13380V	1.13380V	1.13380V	1.13380V	Done	all connected cables
devices_15G280	HH(151 251 351) @2#USB	-1#Stratix_10H_SI_Dev_Ki	: e100_2 ex_100g_inst ex;	_100g_inst xcvr caui4_xcvr		(USB1 or USB2)
Measure Vo	ltage Once	📄 continuous up	date Disabled/check to Ena	ble	Stop the current measurement	
e100_2 ex_100g	g_inst ex_100g_inst xcvr cau	ii4_xcvr_644 alt_xcvr_nativ	e_optional_rcfg_logic			
	Ch0	Ch1	Ch2	Ch3	Status	
VCCER	1.11578V	1.11578V	1.11578V	1.11578V	Done	
VCCET	1.13380V	1.13380V	1.13380V	1.13380V	Done	



Intel[®] Stratix[®] 10 Device L-Tile/H-Tile Transceiver Voltage Tool

	iver_Voltage_Debug_Tool_v•	4p0_Beta				
Comments						
** ** ** ** ** ** **	* ** ** ** ** ** ** ** ** **	* ** ** ** ** ** ** ** **	** ** ** ** ** ** ** ** **	** ** **		
Tool_v4p0 based on	Q17.1.2					
To use this tool ADM	IE should be Enabled					
Datarate < 17.4Gbp	os - VCCET/VCCER - Min 1.0	W Typ 1.03V Max 1.06	1			
Datarate > 17.4Gbp	os - VCCET/VCCER - Min 1.1	V Typ 1.12V Max 1.14	6			Measure the voltage ence
Accuracy : +-18mV						measure the voltage once
** ** ** ** ** **	* ** <mark>*</mark> ** ** ** ** ** ** ** **	* ** ** ** ** ** ** ** **	** ** ** ** ** ** ** ** **	** ** **		
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Phy + Channel						vollage
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Measure Volt	age Opce	e continuous un	date Disabled/check to Enab	le	Stop the current measurement	Step the ourrept
	ago onco	Contendodo ap		10	Stop the carrent measurement	
						otop the outrent
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e100_1 ex_100g_	inst ex_100g_inst xcvr caui	4_xcvr_644 alt_xcvr_nativ Ch1	e_optional_rcfg_logic	Ch3	Status	measurement
e100_1 ex_100g_	inst ex_100g_inst xcvr caui Ch0 1.11578V	4_xcvr_644 alt_xcvr_nativ Ch1 1.11578V	e_optional_rcfg_logic Ch2 1.11578V	Ch3 1.11578V	Status Done	measurement
e100_1 ex_100g_ VCCER VCCET	inst ex_100g_inst xcvr caui Ch0 1.11578V 1.13380V	4_xcvr_644 alt_xcvr_nativ Ch1 1.11578V 1.13380V	e_optional_rcfg_logic Ch2 1.11578V 1.13380V	Ch3 1.11578V 1.13380V	Status Done Done	measurement
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e100_1 ex_100g_ VCCER VCCET devices_15G280Hi Measure Volta e100_2 ex_100g_i VCCER	inst ex_100g_inst xcvr caui Ch0 1.11578V 1.13380V H(151 251 351) @2#USB- age Once inst ex_100g_inst xcvr caui Ch0 1.11578V	4_xcvr_644 alt_xcvr_nativ Ch1 1.11578V 1.13380V 1#Stratix_10H_51_Dev_Kit Continuous up 4_xcvr_644 alt_xcvr_nativ Ch1 1.11578V	e_optional_rcfg_logic Ch2 1.11578V 1.13380V e100_2 ex_100g_inst ex_ date Disabled/check to Enat s_optional_rcfg_logic Ch2 1.11578V	Ch3 1.11578V 1.13380V 100g_inst xcvr caui4_xc ile Ch3 1.11578V	Status Done Done wr_644 alt_xcvr_native_optional_rcfg_logic Stop the current measurement Status Done	measurement



TRANSCEIVER STATUS TOOL

Intel[®] Stratix[®] 10 Device Status Signal





Intel[®] Stratix[®] 10 Device L-Tile/H-Tile Transceiver Status Tool

_Ltile_Htile_Transceiver_St	atus_Tool_v4p0_Beta					
Comments						
	* ** ** ** ** ** ** ** ** ** ** ** ** *					
Tool_v4p0 based on Q1	7.1.2					
1. To use this tool ADME 2. Uncheck checkbox to	should be Enabled					
** ** ** ** ** ** **						
Measurement Type						
Measure Transceive	r Status Once 🔲 continuous update Disabled/check to Enable 🛛 logfile					
PHY + Channel						
devices_15G280HH(1	51 251 351) @2#USB-1#Stratix_10H_SI_Dev_Kit e100_1 ex_100g_inst ex_100g_inst xcvr caui4_	xcvr_644	alt_xcvr	_nativ	e_opt	ional_rcfg_logic
	Description	Disable	Ch0 Ch	1 Ch2	Ch3	click_for_help
rx_is_lockedtodata	{Red:NoLock, Green:LockHigh,}		• •	•	•	rx_is_lockedtodata_help
rx_is_lockedtoref	{Red:NoLock, Green:LockHigh, Dark_green: Don't Care, Since Lock_to_data is high}		• •	•	•	rx_is_lockedtoref_help
tx_cal_busy	{Red:Cal_on, Dark_Green:Cal_done}		• •	•	•	tx_cal_busy_help
rx_cal_busy	{Red:Cal_on, Dark_Green:Cal_done}		• •	•	•	rx_cal_busy_help
avmm_busy	{Red:Avmm_Busy, Dark_Green:Avmm_not_Busy}		• •	•	•	avmm_busy_help
rx_seriallpbken	{Green:Loopback_on, Dark_green:Loopback_off}		• •	•	•	rx_seriallpbken_help
prbs_counter_en	{Green:PRB5_enabled, Dark_red:PRB5_Disabled}		• •	•	•	prbs_counter_en_help
prbs_done	{Green:PRB5_patt_found, Red:PRB5_patt_not_found}			•	•	prbs_done_help
cable_P_N_swap	$\{ Green: No_need_to_swap_polarity, Red: Need_to_swap_polarity, Dark_green: Disable/No Data Lock \}$		• •	•	•	cable_P_N_swap_help
devices_15G280HH(1	51 251 351) @2#U5B-1#5tratix_10H_5I_Dev_Kit e100_2 ex_100g_inst ex_100g_inst xcvr caui4_	xcvr_644	alt_xcvr	_nativ	e_opt	ional_rcfg_logic
	Description	Disable	Ch0 Ch	1 Ch2	Ch3	click_for_help
rx_is_lockedtodata	{Red:NoLock, Green:LockHigh,}		• •	•	•	rx_is_lockedtodata_help
rx_is_lockedtoref	{Red:NoLock, Green:LockHigh, Dark_green: Don't Care, Since Lock_to_data is high}		• •	•	•	rx_is_lockedtoref_help
tx_cal_busy	{Red:Cal_on, Dark_Green:Cal_done}		• •	•	•	tx_cal_busy_help
rx_cal_busy	{Red:Cal_on, Dark_Green:Cal_done}		• •	•	•	rx_cal_busy_help
avmm_busy	{Red:Avmm_Busy, Dark_Green:Avmm_not_Busy}		• •	•	•	avmm_busy_help
rx_seriallpbken	{Green:Loopback_on, Dark_green:Loopback_off}		• •	•	•	rx_seriallpbken_help
prbs_counter_en	{Green:PRB5_enabled, Dark_red:PRB5_Disabled}		• •	•	•	prbs_counter_en_help
prbs_done	{Green:PRB5_patt_found, Red:PRB5_patt_not_found}		• •	•	•	prbs_done_help
cable P N swap	{Green:No_need_to_swap_polarity,Red:Need_to_swap_polarity, Dark_green:Disable/No Data Lock}	V			•	cable_P_N_swap_help



Intel[®] Stratix[®] 10 Device L-Tile/H-Tile Transceiver Status Tool

Ltile_Htile_Transceiver_Status_Tool_v4p0_Beta	
Comments	Tool automatically finds the
	Tool automatically linds the
Tool_v4p0 based on Q17.1.2	Native PHY instantiated
1.10 Use this tool ADMIC should be Enabled 2.1 Uncheck chardway to enable C-MBA DNI Swart text	Trailve FITT instantiated
Measurement Type	Tool automatically finds the
Measure Transceiver Status Once Continuous update Disabled/check to Enable logfile	number of channels instantiated
PHY + Channel	
devices_15G280HH(151 251 351) @2#U5B-1#5tratix_10H_5I_Dev_Kit e100_1 ex_100g_inst ex_100g_inst xcvr caui4_xcvr_644 _2t_xcvr_native_opt	inal_refg_logic
Description Disable Ch0 Ch1 Ch2 Ch3	click on the button to view
rx_is_lockedtodata {Red:NoLock, Green:LockHigh,}	rx_is_lockedtodata_help
rx_is_lockedtoref {Red:NoLock, Green:LockHigh, Dark_green: Don't Care, Since Lock_to_data is high}	rx_is_lockedtoref_help
tx_cal_busy {Red:Cal_on, Dark_Green:Cal_done}	tx_cal_busy_help
rx_cal_busy {Red:Cal_on, Dark_Green:Cal_done}	rx_cal_busy_help
avmm_busy {Red:Avmm_Busy, Dark_Green:Avmm_not_Busy}	avmm_busy_help step::02 778 deviation list violation
rx_serialpbken {Green:Loopback_on, Dark_green:Loopback_off} • • •	rx_serialpbken_help Rxurue the auxiaua PM difference limits between TK and FK in the limit is within device specification check CRP FM setting in TK FMA tab under Network HMT IP check CRP FMM setting in TK FMA tab under Network HMT IP
prbs_counter_en {Green:PRBS_enabled, Dark_red:PRB5_Disabled}	prbs_counter_en_help
prbs_done {Green:PRB5_patt_found, Red:PRB5_patt_not_found}	prbs_done_help the same could be from the internal of the same same same same same same same sam
cable_P_N_swap = {Green:No_need_to_swap_polarity,Red:Need_to_swap_polarity, Dark_green:Disable/No Data Lock} 🛛 🔹 🔹 🔹	cable_P_N_swap_help stops in the stop of t
devices_15G280HH(151 251 351)].@2#U5B-1#Stratix_10H_5I_Dev_Kit e100_2 ex_100g_inst ex_100g_inst xcvr caui4_xcvr_caui4_xcvr_native_opt	A reset to KK channel is required under following conditions: mal_rcfg_logic
Description D sable Ch0 Ch1 Ch2 Ch3	long period of dile on the link incoming data path switched from external loopback, and vice versa
rx_is_lockedtodata {Red:NoLock, Green:LockHigh,}	rx_is_lockedtodata_help
rx_is_lockedtoref {Red:NoLock, Green:LockHigh, Dark_green: Don't Care, Since Lock_to_data is high}	rx_is_lockedtoref_help
tx_cal_busy {Red:Cal_on, Dark_Green:Cal_done}	tx_cal_busy_help
rx_cal_busy {Red:Cal_on, Dark_Green:Cal_done}	rx_cal_busy_help
avmm_busy {Red:Avmm_Busy, Dark_Green:Avmm_not_Busy}	
rx_seriallpbken {Green:Loopback_on, Dark_green:Loopback_off}	number cable swap
prbs_counter_en {Green:PRBS_enabled, Dark_red:PRBS_Disabled}	prbs_counter_en_help
prbs_done {Green:PRBS_patt_found, Red:PRBS_patt_not_found}	prbs_done_help
cable_P_N_swap {Green:No_need_to_swap_polarity, Red:Need_to_swap_polarity, Dark_green:Disable/No Data Lock} 🗹 🔹 🔹 👁	cable_P_N_swap_help



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TRANSCEIVER EYE DEBUG TOOL

Intel[®] Stratix[®] 10 Device Eye Viewer (On-Die Instrumentation (ODI))

- Provides on-chip eye monitoring capabilities
- Helps to optimize link equalization parameters during board bring-up
- Supports in-system link diagnostics and equalization margin testing



Existing Intel[®] Stratix[®] 10 Transceiver Toolkit Eye Viewer Algorithm



- Loop 1: Increment the vertical threshold voltage
- Loop 2: Sweep the ODI clock across for different clock phase
- Measure the error count
- Loop end
- Plot the 2-D eye diagram



Intel[®] Stratix[®] 10 Device L-Tile/H-Tile Transceiver Eye Debug Tool Algorithm





nments																				
	** ** ** ** *				** ** ** ** ** *															
ol_v4p0 b	ased on Q17.	1.2																		
) use this t his hool mea	ool ADME sho asure the Eve	Height a	abled od Width at I	the CDR San	nling Point															
ange the	Vertical and H	iorozonta	sweep step	size to decr	ease the measur	ement time														
creasing th	he Step size w	all decrea	se the accur	acy																
** ** **	** ** ** ** *	*****	****	** ** ** **	** ** ** ** ** *	* ** ** ** ** ** ** *	********													
9-1e in the	** ** ** ** *	cation>		easurement_	057)ulian_13hr_4	**************************************	testu2-24.csv													
surement	Туре																			
Measure	Eye Once	E con	tinuous Mea	sure Eye Dis	abled/check to E	nable 📄 Stop t	he current measu	rement												
	, Channel																			
instance -	+ Channel																			
Jevices_19	SG280HH(151	251 351) @2#USB	-1#Stratix_1	IOH_SI_Dev_Kit	510_4chan_25g_i	nst1 S10_native_	_phy_ip xcvr_nal	ive_s10_htile_0	alt_xcvr_native_c	optional_rcfg_logic	:								
C		_				data Dicabled/cha	ck to Enable		Stor	the current measure	airement									
Meas	ure Eye Once			1	continuous up	date bisabled/the	cit co Endbio				al officine									
Meas	ure Eye Once			l	continuous up	date bisabled/the														
Measi	ure Eye Once	510_nativ	e_phy_ip xc	vr_native_s:	continuous up	vr_native_optiona	l_rcfg_logic													
Measi 10_4char	ure Eye Once n_25g_inst1 5 enable v	510_nativ	e_phy_ip xc	vr_native_s1	0_htile_0 alt_xc	vr_native_optiona	I_rcfg_logic	V 1e8	✓ 1e9	1e10	iel1	1e12	apply							
Measi 10_4char channel	ure Eye Once n_25g_inst1 S enable + chan_en	510_nativ srlpbk	e_phy_ip xc 2 Horiz_step	vr_native_s: 2 v	Continuous up IO_htile_O alt_xc PRB531	vr_native_optiona Vr_native_optiona Vr_native_optiona Vr_native_optiona	I_rcfg_logic V 1e7 Eye_W/H_1e7	✓ 1e8 Eye_W/H_1e8	✓ 1e9 Eye_W/H_1e9	1e10 Eye_W/H_1e10	Eve_W/H_1e11	1e12 Eye_W/H_1e12	apply Status	VOD	Post	Pre ac	jain do	:gain VG	5A DFE	Test
Measi 10_4char channel Chan0	ure Eye Once n_25g_inst1 S enable chan_en enable	510_native srlpbk 0	e_phy_ip xc 2 v Horiz_step 2 v	vr_native_s 2 v Vert_step 2 v	Continuous up IO_htile_O[alt_xc PRBS31 PRBS PRBS31	vr_native_optiona vr_native vr_na	I_rcfg_logic 1e7 Eye_W/H_1e7 32/40	✓ 1e8 Eye_W/H_1e8 32/40	✓ 1e9 Eye_W/H_1e9 28/40	1e10 Eye_W/H_1e10 	Eve_W/H_1e11	1e12 Eye_W/H_1e12 	apply Status Done	VOD 31	Post 0	Pre aci	jain do 28	:gain VG 3 22	5A DFE : 54,3,3,5,6,2,3,3,3,1,1,1,1,1,1	Test 19 si
Mease i10_4char channel Chan0 Chan1	ure Eye Once n_25g_inst1 5 enable chan_en enable enable	510_native srlpbk 0 0	e_phy_ip xc 2 • Horiz_step 2 • 2 •	vr_native_s: 2 • Vert_step 2 • 2 •	Continuous up IO_htile_O[alt_xc PRB531 PRB5 PRB531 PRB531	vr_native_optiona vr_native vr_nativ	I_rcfg_logic V 1e7 Eye_W/H_1e7 32/40 38/44	 ✓ 1e8 Eye_W/H_1e8 32/40 34/36 	♥ 1e9 Eye_W/H_1e9 28/40 34/32	1e10 Eye_W/H_1e10 	<pre>lell Eye_W/H_1ell</pre>	1e12 Eye_W/H_1e12 	apply Status Done Done	VOD 31 31	Post 0	Pre aci O 8 O 8	jain do 28 29	:gain VG 3 22 9 23	A DFE 54,3,3,5,6,2,3,3,3,1,1,1,1,1,1 53,3,3,3,5,4,3,2,3,2,2,1,1,0,2	Test 19 s 18 s
Mease 10_4char channel Chan0 Chan1 Chan2	ure Eye Once -25g_inst1 5 enable • chan_en enable • enable • enable •	510_native srlpbk 0 0	e_phy_ip xc 2 v Horiz_step 2 v 2 v 2 v	vr_native_s: 2 • Vert_step 2 • 2 • 2 •	Continuous up IO_htile_O[alt_xcc PRB531 PRB531 PRB531 PRB531 PRB531	vr_native_optiona vr_native vr_	I_rcfg_logic V 1e7 Eye_W/H_1e7 32/40 38/44 34/48	 ✓ 1e8 Eye_W/H_1e8 32/40 34/36 34/44 	▼ 1e9 Eye_W/H_1e9 28/40 34/32 32/40	1e10 Eye_W/H_1e10 	<pre>leli Eye_W/H_1e11</pre>	1612 Eye_W/H_1612 	apply Status Done Done Done	VOD 31 31 31	Post O O	Pre ac 0 8 0 8 0 8	jain do 28 29 29	igain VG 3 22 9 23 9 22	 A DFE 54,3,3,5,6,2,3,3,3,1,1,1,1,1,1 53,3,3,3,5,4,3,2,3,2,2,1,1,0,2 52,1,2,3,4,4,2,3,2,1,2,2,1,1,1 	Test 19 s 18 s 18 s
Measu i10_4char channel Chan0 Chan1 Chan2 Chan3	ure Eye Once n_25g_inst1 5 enable • enable • enable • enable • enable •	sripbk 0 0 0 0	e_phy_ip xc 2 • Horiz_step 2 • 2 • 2 • 2 •	vr_native_s: 2 • Vert_step 2 • 2 • 2 • 2 •	Continuous up IO_htile_O[alt_xcc PRB531 PRB531 PRB531 PRB531 PRB531 PRB531	vr_native_optiona vr_native_optiona v_ 1e6 Eye_W/H_1e6 36/40 42/44 40/48 40/56	I_rcfg_logic U_ 1e7 Eye_W/H_1e7 32/40 38/44 34/48 36/52	Ie8 Eye_W/H_1e8 32/40 34/36 34/44 34/44	✓ 1e9 Eye_W/H_1e9 28/40 34/32 32/40 34/44	1e10 Eye_W/H_1e10 	ieii Eye_W/H_1eii 	1e12 Eye_W/H_1e12 	apply Status Done Done Done Done	VOD 31 31 31 31	Post O O O	Pre ac 0 8 0 8 0 8 0 8	jain do 28 29 29 29	ngain VG 3 22 9 23 9 22 9 21	 A DFE 54,3,3,5,6,2,3,3,3,1,1,1,1,1,1 53,3,3,3,5,4,3,2,3,2,2,1,1,0,2 52,1,2,3,4,4,2,3,2,1,2,2,1,1,1 51,1,2,4,4,2,4,2,1,1,1,2,1,0,0 	Test. 19 se 18 se 18 se 16 se
Measu 10_4char channel Chan0 Chan1 Chan2 Chan3 levices_15	ure Eye Once -25g_inst1 S enable • chan_en enable • enable • enable • social enable •	sripbk 0 0 0 0 251 351	e_phy_ip xc 2 • Horiz_step 2 • 2 • 2 • 2 • 2 • 2 •	vr_native_s: 2 • Vert_step 2 • 2 • 2 • 2 • 2 •	Continuous up IO_htile_0 alt_xcc PRBS31 PRBS31 PR	vr_native_optiona vr_native_optiona Eve_W/H_1e6 So/40 42/44 40/48 40/56 [S10_4chan_25g_]	I_rcfg_logic [J cfg_logic [J te7 Eye_W/H_1e7 32/40 38/44 34/48 36/52 nst2 510_native_	✓ 1e8 Eye_W/H_1e8 32/40 34/36 34/44 34/44 34/44 phy_ip xcvr_nal	✓ 1e9 Eye_W/H_1e9 28/40 34/32 32/40 34/44 ive_s10_htlle_0	<pre>iel0 Eye_W/H_1e10 alt_xcvr_native_</pre>	ieii Eye_W/H_1eii sptional_rcfg_logic	□ 1e12 Eye_W/H_1e12 	apply Status Done Done Done Done	VOD 31 31 31 31	Post 0 0 0	Pre ac 0 8 0 8 0 8 0 8	yain dd 28 29 29 29	ngain VG 3 22 9 23 9 22 9 21	 A DFE 54,3,3,5,6,2,3,3,3,1,1,1,1,1,1 53,3,3,3,5,4,3,2,3,2,2,1,1,0,2 52,1,2,3,4,4,2,3,2,1,2,2,1,1,1 51,1,2,4,4,2,4,2,1,1,1,2,1,0,0 	Test, 19 se 18 se 18 se
Measi (10_4char (hannel Chan0 (han1 (han2 (han3 levices_1) Measi	ure Eye Once =_25g_inst1 S enable • chan_en enable • enable • enable • enable • ssc280HH(151 ure Eye Once	sripbk 0 0 0 1251 351	e_phy_ip xc 2 • Horiz_step 2 • 2 • 2 • 2 • 2 •	l vr_native_s: 2 v Vert_step 2 v 2 v 2 v -1#Stratix_1	PRB531 PR	vr_native_optiona vr_native_optiona vr_native_optiona Eve_w/H_1e6 36/40 42/44 40/48 40/56 [S10_4chan_25g_] date Disabled/che	I_rcfg_logic V 1e7 Eye_W/H_1e7 32/40 38/44 34/48 36/52 nst2[510_native_ ck to Enable	✓ 1e8 Eye_W/H_1e8 32/40 34/36 34/44 34/44 34/44 phy_p xcvr_nall	✓ 1e9 Eye_W/H_1e9 28/40 34/32 32/40 34/44 iive_s10_htile_0 Stop	iel0 Eye_W/H_1e10 lalt_xcvr_native_c b the current meas	i ieii Eye_W/H_1eii optional_rcfg_logic surement	□ 1e12 Eye_W/H_1e12 	apply Status Done Done Done Done	VOD 31 31 31 31	Post 0 0 0	Pre ac 0 8 0 8 0 8 0 8	jain do 28 29 29 29	:gain VG 3 22 9 23 9 22 9 21	 A DFE 54,3,3,5,6,2,3,3,3,1,1,1,1,1,1 53,3,3,3,5,4,3,2,3,2,2,1,1,0,2 52,1,2,3,4,4,2,3,2,1,2,2,1,1,1 51,1,2,4,4,2,4,2,1,1,1,2,1,0,0 	Test, 19 se 18 se 16 se
Measi 510_4char Chan0 Chan1 Chan2 Chan3 devices_15 Measi 510_4char	ure Eye Once n_25g_inst1[s enable v chan_en enable v enable v enable v enable v SG200HH(151 ure Eye Once n_25g_inst2[S	sripbk 0 0 0 1251 351	e_phy_ip xc 2 v Horiz_step 2 v 2 v 2 v 2 v 2 v 2 v	l vr_native_s1 2 v Vert_step 2 v 2 v 2 v 2 v 2 v (vr_native_s1	Continuous up IO_htile_0[alt_xc PRB531 PRB53 PRB531 PRB531 PRB531 PRB531 PRB531 PRB531 IOH_SI_Dev_Kit] Continuous up	vr_native_optiona	I_rcfg_logic V 1e7 Eye_W/H_1e7 32/40 38/44 34/48 36/52 nst2[510_native] ck to Enable I_rcfg_logic	✓ 1e6 Eye_W/H_1e8 32/40 34/36 34/44 34/44 34/44 phy_jp xcvr_nal	✓ 1e9 Eye_W/H_1e9 28/40 34/32 32/40 34/44 ive_s10_htlle_0 Stop	I tel0 Eye_W/H_1e10 lat_xcvr_native_c the current meas	ieii Eye_W/H_1eii aptional_rcfg_logic aurement	te12 Eye_W/H_1e12	apply Status Done Done Done	VOD 31 31 31 31	Post O O O	Pre ac 0 8 0 8 0 8	jain de 28 29 29	ngain VG 3 22 9 23 9 22 9 21	 DFE 54,3,3,5,6,2,3,3,3,1,1,1,1,1,1 53,3,3,3,5,4,3,2,3,2,2,1,1,0,2 52,1,2,3,4,4,2,3,2,1,2,2,1,1,1 51,1,2,4,4,2,4,2,1,1,1,2,1,0,0 	Test, 19 se 18 se 16 se
Measi ilo_4char channel Chan0 Chan1 Chan2 Chan3 levices_11 Measi ilo_4char	ure Eye Once n_25g_inst1[s enable v enable v enable v enable v enable v enable v soccation of the social states of the social s	sripbk 0 0 0 1251 351	e_phy_jp xc 2	l vr_native_s: 2 v 2 v 2 v 2 v 2 v 1#Stratx_1 [vr_native_s: 2 v	Continuous up PRB531 PRB53 PRB531 PRB531 PRB5477 PRB54777777777777777777777777777777777777	vr_native_optiona	I_rcfg_logic	✓ 1e8 Eye_W/H_1e8 32/40 34/36 34/44	✓ 1e9 Eye_W/H_1e9 28/40 34/32 32/40 34/44 twe_s10_httle_0 Stop ✓ 1e9	terminal for the current mease	i tett Eye_W/H_1e11	<pre>le12 Eye_W/H_1e12</pre>	apply Status Done Done Done Done	VOD 31 31 31 31	Post 0 0	Pre ac 0 8 0 8 0 8	pain do 28 29 29 29	ngain VG 3 22 9 23 9 22 9 21	 iA DFE 54,3,3,5,6,2,3,3,3,1,1,1,1,1,1 53,3,3,3,5,4,3,2,3,2,2,1,1,0,2 52,1,2,3,4,4,2,3,2,1,2,2,1,1,1 51,1,2,4,4,2,4,2,1,1,1,2,1,0,0 	Test 19 si 18 si 18 si 16 si
Measi i10_4char channel Chan0 Chan1 Chan2 Chan3 levices_11 Measi i10_4char channel	ure Eye Once 	sripbk 0 0 0 1251 351 310_native sripbk	e_phy_jp xc 2	l vr_native_s: 2 v 2 v 2 v 2 v 2 v 2 v 2 v 2 v 2 v 2 v	continuous up continuous up 0_htile_0[ak]_xc PRBS31 Continuous up tohtie_0[akxc PRBS31 PRBS31	vr_native_optiona vr_native_optiona vr_native_optiona vr_native_optiona vr_native_optiona vr_native_optiona vr_native_optiona vr_native_optiona vr_native_optiona	[_rdg_logic ☑ 1e7 Eve_W/H_1e7 32/40 38/44 34/48 36/52 nst2[510_native_ ck to Enable I_rdg_logic ☑ 1e7 Eve_W/H_1e7	✓ 1e8 Eye_W/H_1e8 32/40 34/36 34/44 34/44 ghy_jejxcvr_ne4 ✓ 1e8 Eye_W/H_1e8	✓ 169 Eve.W/H_169 28/40 34/32 32/40 34/44 ive_s10_htde_0 Stop ✓ 169 Eve.W/H_169 Eve.W/H_169	<pre>1e10 Eye_W/H_1e10 lait_xcvr_native_c pthe current meas 1e10 Eye_W/H_1e10</pre>	I ei1 Eye_W/H_1e11	Eye_W/H_1e12 	apply Status Done Done Done Done Done Status	VOD 31 31 31 31 31	Post 0 0 0	Pre ac 0 8 0 8 0 8 0 8	yain do 28 29 29 29 29	ngain VG 3 22 9 23 9 22 9 21	 iA DFE 54,3,3,5,6,2,3,3,3,1,1,1,1,1,1 53,3,3,5,4,3,2,3,2,2,1,1,0,2 52,1,2,3,4,4,2,3,2,1,2,2,1,1,1 51,1,2,4,4,2,4,2,1,1,1,2,1,0,0 iA DFE 	Test, 19 se 18 se 16 se Test,
Measi i10_4char channel Chan0 Chan1 Chan2 Chan3 levices_15 Measi i10_4char channel Chan0	ure Eye Once 	sripbk 0 0 1251 351 510_native sripbk 0	e_phy_ip xc 2 ↓ 4 ↓ 2 ↓ 2 ↓ 2 ↓ 2 ↓ 2 ↓ 2 ↓ 2 ↓ 2	vr_native_s1 2 • 2 • 2 • 2 • 2 • 2 • 2 • 2 • 2 • 2 •	continuous up PRES31 PRES31 PRES31 PRES31 PRES31 PRES31 PRES31 OI_SI_Dev_JKI OI_SI_Dev_JKI OI_HEL_OIAL_xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx	w_native_optiona y_native_optiona y_native_optiona y_1e6 Eve_w/N_1e6 y_2(A4 40/48 40/48 40/56 (SI0_4chan_25g_) (SI0_4chan_25g_) y_1e6 Eve_w/N_1e6 Eve_w/N_1e6 SVe_w/N_1e6 S	rdg_logic v] 167 Eye_W/H_167 32/40 33/44 34/48 36/52 nst2[510_native_ ck to Enable [rdg_logic Eye_W/H_167 	✓ 168 Eve_W/H_168 32/40 34/36 34/34 34/34 34/34 34/44 9hy_lp xcvr_nal Eve_W/H_168 32/40	▼ 169 Eye_W/H_1e9 Eye_W/H_1e9 34/32 32/40 34/44 ive_s10_htde_0 Stop V 169 Eye_W/H_1e9 30/40	1e10 Eye_W/H_1e10 at_xcvr_native_ce the current meas 1e10 Eye_W/H_1e10	ieii ieii Eye_W/H_1eii potonal_rcfg_logic aurement ieii Eye_W/H_1eii	iel2 Eye_W/H_1612 Eye_W/H_1612 Eye_W/H_1612 Eye_W/H_1612 	apply Status Done Done Done Done Apply Status Done	VOD 31 31 31 31 31 31 31	Post 0 0 0 0 Post 0	Pre aci 0 8 0 8 0 8 0 8 Pre aci 0 8	jain do 28 29 29 29 29 29 29 29 29 29 29 29 29 29	ngain VG 3 22 9 23 9 22 9 21 9 21 0 9 19	 A DFE 54,3,3,5,6,2,3,3,3,1,1,1,1,1 53,3,3,5,5,4,2,3,2,2,1,1,0,2 52,1,2,3,4,4,2,3,2,1,2,2,1,1,1 51,1,2,4,4,2,4,2,1,1,1,2,1,0,0 A DFE 46,0,2,5,3,2,2,3,3,1,1,1,1,1,0 	Test, 19 se 18 se 16 se Test, 17 se
Measi ilo_4char channel Chan0 Chan1 Chan2 Chan3 levices_15 Measi ilo_4char channel Chan0 Chan1	ure Eye Once 	sripbk 0 0 1251 351 310_native sripbk 0	e_phy_ip xc 2 ↓ 2 ↓ 2 ↓ 2 ↓ 2 ↓ 2 ↓ 2 ↓ 2 ↓	vr_native_s1 2 • 2 • 2 • 2 • 2 • 2 • 2 • 2 •	continuous up prebility	wr_native_optiona wr_native_optiona wr_native_optiona wr_native_optiona addet Disabled/che stative_optiona wr_native_optiona wr_native_optiona wr_native_optiona wr_native_optiona addet Disabled/che style addet 0 yr_native_optiona wr_native_optiona addet 0	_rdg_logic _rd	✓ 1e8 Eye_W/H_1e8 32/40 34/36 34/34 34/44 34/44 9/hy_jp xcvr_nal Eye_W/H_1e8 Eye_W/H_1e8 32/40	V 169 Eye_W/H_169 28/40 34/42 32/40 34/44 tive_s10_htile_00 V 169 Eye_W/H_169 30/40 30/40	1e10 Eye_W/H_1e10 ak_xxvr_native_c 1e10 Eye_W/H_1e10	ioli Eye_W/H_leli ioli Eye_W/H_leli Eye_W/H_leli	iei2 Eye.W/H_1ei2 Eye.W/H_1ei2 Eye.W/H_1ei2 Eye.W/H_1ei2 	apply Status Done Done Done Done Status Done Done Done	VOD 31 31 31 31 31 31 31 VOD 31 31	Post 0 0 0 0 Post 0 0	Pre ac 0 8 0 8 0 8 0 8 Pre ac 0 8 0 8	iain do 29 29 29 29 29 29 20 20 20 20	:gain VG 3 22 9 23 9 22 9 21 9 21 :gain VG 9 19 3 22	 DFE 54,3,3,5,6,2,3,3,3,1,1,1,1,1 53,3,3,5,4,4,2,3,2,2,1,1,0,2 52,1,2,3,4,4,2,3,2,1,2,2,1,1,1 51,1,2,4,4,2,4,2,1,1,1,2,1,0,0 iA DFE 46,0,2,5,3,2,2,3,3,1,1,1,1,1,0 57,3,3,4,6,3,3,3,2,1,1,2,1,1 	Test, 19 se 18 se 16 se Test, 17 se 16 se
Measi 510_4char Chan0 Chan1 Chan2 Chan3 Jevices_15 Measi 510_4char channel Chan0 Chan1 Chan1 Chan1 Chan2	ure Eye Once 	sripbk 0 0 0 1251 351 510_native sripbk 0 0	e_phy_ip xc 2 • Horiz_step 2 • 2 • 2 • 2 • 2 • 2 • 2 • 2 •	vr_native_si 2 • Vert_step 2 • 2 • 2 • 2 • 2 • 2 • 2 • 2 •	continuous up continuous up 0_htile_0 alt_xcc pR8531 pR8531 pR8531 pR8531 pR8531 pR8531 pR8531 pR8531 pR8531 continuous up pR8531 continuous up pR8531 pR8531 pR8531 pR8531 pR8531	wr_native_optiona wr_native_optiona wr_native_optiona sold additional	_rdg_logic ▼167 Eye_W/H_167 32/40 38/44 34/48 36/52 nst2[510_netive] ck to Enable _rdg_logic _167 Eye_W/H_167 	✓ 166 Eye_W/H_168 32/40 34/44 34/44 34/44 34/44 phy_jp/xcvr_nal 2/40 22/40 32/40 32/40 32/40 32/40 32/40	▼ 169 Eye_W H_1e9 28/40 34/32 32/40 34/41 stop Eye_W H_1e9 Stop ▼ 169 Eye_W H_1e9 30/40 30/40 30/40	 1e10 Eye W/H_1e10 1e10 Eye_W/H_1e10 	ieii Eye_W/H_1eii urement ieii ieii Eye_W/H_1eii	1e12 Eye.W/H_1e12 Eye.W/H_1e12 Eye.W/H_1e12	epply Status Done Done Done Done Done Status Done Done Done Done	VOD 31 31 31 31 31 31 31 31 31	Post 0 0 0 0 0 0 0 0	Pre ac. 0 8 0 8 0 8 0 8 0 8 0 8 0 8 0 8 0 8	jain do 28 29 29 29 29 29 20 20 20 20 20 20 20 20 20 20 20 20 20	ngain VG 3 22 9 23 9 22 9 21 9 21 9 21 9 21 9 21 9 19 3 22 3 20	 DFE 54,33,5,6,2,3,3,3,1,1,1,1,1,1 53,3,3,5,4,2,3,2,2,1,1,0,2 52,1,2,3,4,4,2,3,2,1,2,2,1,1,1 51,1,2,4,4,2,4,2,1,1,1,2,1,0,0 iii DFE 46,0,2,5,3,2,2,3,3,1,1,1,1,1,1,1,1 55,3,3,6,4,3,3,2,2,1,2,1,1,1 	Test_ 19 se 18 se 16 se 16 se Test_ 17 se 16 se



_Ltile_Htile_Transceive	ver_EYE_Debug_	Tool_v4p0_Br	ita																1	
Comments																				
Tool_v4p0 based o To use this tool Af	on Q17.1.2 DME should be Er	nabled																		
This tool measure	the Eye Height a	and Width at I	the CDR Sa	mpling Point																
Change the Vertice	al and Horozonti	al sweep step	size to dec	rease the measurement tim	ne															
Increasing the Ste	ep size will decrei	ase the accur	асу																	
LogEle in the follo	wing Location		acurement	057julian 13br 45min 59	sec_si-catest02-24_cs	,														
** ** ** ** ** **	* ** ** ** ** ** **	** ** ** **	*****	** ** ** ** ** ** ** ** **	* ** ** ** ** ** ** **	* **														
Measurement Type																				
Measure Eye O	Once 📃 🖂 to	ntinuous Mea	sure Eye Di	sabled/check to Enable	Stop the current me	easurement														
Phy instance + Cha	annel																			
devices_15G280	DHH(151 251 35	1) @2#USB	-1#Stratix_	10H_SI_Dev_Kit S10_4ch	an_25g_inst1 S10_nat	:ive_phy_ip xcvr_r	native_s10_htile	_0 alt_xcvr_nativ	e_optional_rcfg_lo	ogic										
Measure Ey	ye Once			continuous update Disa	bled/check to Enable		S	Stop the current m	easurement											
510_4chan_25g	j_inst1 510_nativ	/e_phy_ip xc	/r_native_s	10_htile_0 alt_xcvr_native	_optional_rcfg_logic															
ena	able 🖌	2 🗸	2 🗸	PRB531 👻 🗹 1	e6 🔽 1e7	💟 1e8	V 1e9	📄 1e10	E 1e11	E 1e12	apply						· · · · · /			
channel chan	n_en sripbk	Horiz_step	Vert_step	PRBS Eye_V	W/H_1e6 Eye_W/H_1	e7 Eye_W/H_1e	8 Eye_W/H_1e	e9 Eye_W/H_1e	IO Eye_W/H_1e	11 Eye_W/H_1e	12 Status	VOD F	Post Pre	e acgair	n dogain	N VGA	DFE T	Test_Time		
Chan0 ena	able 👻 0	2 👻	2 🗸	PRB531 - 36/40	32/40	32/40	28/40	1.2			Done	31 (0 0	8	28	22	54,3,3,5,6,2,3,3,3,1,1,1,1,1	19 sec		
Chan1 ena	able 🚽 🛛	2 👻	2 👻	PRB531 - 42/44	38/44	34/36	34/32	-			Done	31 (0 0	8	29	23	53,3,3,3,5,4,3,2,3,2,2,1,1,0,2 1	18 sec		Short Measurement Time
Chan2 ena	able 👻 0	2 -	2 🗸	PRB531 + 40/48	34/48	34/44	32/40	12	24	1	Done	31 (0 0	8	29	22	52,1,2,3,4,4,2,3,2,1,2,2,1,1,1 1	18 sec		
Chan3 ena	able 👻 0	2 🗸	2 🔻	PRB531 - 40/56	36/52	34/44	34/44	-			Done	31 (0 0	8	29	21	51,1,2,4,4,2,4,2,1,1,1,2,1,1,0 1	16 sec		
devices_15G280	OHH(151 251 35	1) @2#U5B	-1#Stratix_	10H_SI_Dev_Kit S10_4ch	an_25g_inst2 510_nat	tive_phy_ip xcvr_r	native_s10_htile	_0 alt_xcvr_nativ	e_optional_rcfg_k	ogic										
Measure Ey	ye Once			Continuous update Disa	ibled/check to Enable		S	Stop the current m	easurement											
510_4chan_25g	j_inst2 S10_nativ	/e_phy_ip xc	/r_native_s	10_htile_0 alt_xcvr_native	_optional_rcfg_logic															
ena	able 🖌	2 -	2 -	PRB531 - 1	e6 📃 1e7	🔽 1e8	🔽 1e9	📄 1e10	E 1e11	E 1e12	apply									
channel chan	n_en sripbk	Horiz_step	Vert_step	PRBS Eye_V	W/H_1e6 Eye_W/H_1	e7 Eye_W/H_1e	8 Eye_W/H_1e	e9 Eye_W/H_1e	IO Eye_W/H_1e	11 Eye_W/H_1e	12 Status	VOD F	Post Pr	e acgair	n dogain	N VGA	DFE T	Test_Time		
Chan0 ena	able 👻 0	2 🗸	2 -	PR8531 - 38/40	-	32/40	30/40				Done	31 (0 0	8	29	19	46,0,2,5,3,2,2,3,3,1,1,1,1,1,0 1	17 sec		
Chan1 ena	able 👻 0	2 -	2 -	PRB531 - 38/40	-	32/40	30/40				Done	31 (0 0	8	28	22	57,3,3,4,6,3,3,3,2,1,1,2,1,1,1 1	16 sec		
Chan2 ma	able 🚽 0	2 -	2 -	PR8531 + 42/40		36/40	34/40				Done	31 (0 0	8	28	20	55.3.3.6.4.3.3.3.2.1.2.1.1.1.1	17 sec		
				10,10																
Chan3 ena	ble - 0	2 -	2 -	PR8531 - 38/52		34/52	32/52	-			Done	31 0	n n	8	28	20	53.2.3.3.5.3.3.2.2.3.2.1.1.1.1	17 sec		

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tile_Htile_Tra	insceiver_EYE_Debug	_Tool_v4p0_E	leta																		Click to measure and
Comments Tool_v4p0 b	base 1 on Q17.1.2		** ** ** **	** ** ** ** ** ** ** ** ** **		•															log the eye once
To use this	tool ADME should be	Enabled		20010000																	Continuously measure
This tool me Change the	easure the Eye Height	tal sweet ste	blo CDD Sar	rease the measurement time																	and log the eve
Increasing t	the tep size will decr	ease the accu	racy																	'	
** ** ** **	e for owing Location -	* ** ** ** ** > log/Exe	** ** ** **	** ** ** ** ** ** ** ** ** ** ** **	** ** ** ** ** ** *	*															
** ** ** **	* ** ** ** ** ** ** **	* ** ** * <mark>*</mark> **	** ** ** **	ex	** ** ** ** ** ** **	*															Stop the current
Measurement	TVLR																				measurement
Maarura	Eve Once	ontinuous Me	arura Eva Dic	rabled/check to Enable	the current mea	rement															
measure	cye once	ununudus me	asure dye Dis	sable grine is to chable	o the current measure	drement.															
Phy instance	+ Channel																				
devices_1	SG280HH(151 251 3	51) @2#USI	8-1#Stratix_	10H_SI_Dev_Kit S10_4chan_25g	_inst1 S10_nativ	_phy_jp xcvr_na	itive_s10_htile_0	alt_xcvr_native_o	ptional_rcfg_logi	c											
Meas	sure Eye Once		I	continuous update Disabled/ch	eck to Enable		Sto	o the current meas	urement												
510.4cba	n 25a inst11510 na	tive obv inly	vr native s	10 blie Olalt xcvr pative option	al refa logic																
	enable -	2	2	PRB531 V 1e6	✓ 1e7	V 1e8	V 1e9	1e10	1e11	1e12	apply	1									
channel	chan_en sripbi	Horiz_step	Vert_step	PRBS Eye_W/H_1e	6 Eye_W/H_1e7	Eye_W/H_1e8	Eye_W/H_1e9	Eye_W/H_1e10	Eye_W/H_1e11	Eye_W/H_1e12	Status	VOD I	Post Pro	e acgain	dcgain	VGA	DFE	Test	_Time		
Chan0	enable 👻 0	2 🗸	2 🗸	PRB531 - 36/40	32/40	32/40	28/40	-			Done	31	0 0	8	28	22	54,3,3,5,6,2,3,3,3,1,1,1,	1,1,1 19 s	ec		
Chan1	enable 👻 0	2 🔻	2 🗸	PRB531 + 42/44	38/44	34/36	34/32	-			Done	31	0 0	8	29	23	53,3,3,3,5,4,3,2,3,2,2,1,	1,0,2 18 s	ec		
Chan2	enable 👻 0	2 🔻	2 🗸	PRB531 + 40/48	34/48	34/44	32/40				Done	31	0 0	8	29	22	52, 1, 2, 3, 4, 4, 2, 3, 2, 1, 2, 2,	1,1,1 18 s	ec		
Chan3	enable 👻 0	2 👻	2 👻	PRB531 + 40/56	36/52	34/44	34/44	-			Done	31	0 0	8	29	21	51,1,2,4,4,2,4,2,1,1,1,2,	1,0,0 16 s	ec		
devices 1	SG280HH(151 251 3	51) @2#US	B-1#Stratix	10H_SI_Dev_Kit 510_4chan_25c	inst2 510 nativ	phy_ip xcvr_na	tive s10 htile 0	alt_xcvr_native_o	ptional_rcfg_logi	c											
0011000 1				Continuous undate Disabled (ch	eck to Enable		T Sto	the current meas	urement												
Meas	sure Eve Once																				
Meas	sure Eye Once																				
S10_4cha	sure Eye Once in_25g_inst2 510_nal	tive_phy_ip ×	cvr_native_s	10_htile_0 alt_xcvr_native_option	nal_rcfg_logic																
Meas 510_4cha	sure Eye Once In_25g_inst2 510_nal enable 👻	tive_phy_ip xi	cvr_native_s	10_htile_0 alt_xcvr_native_option PRB531 V1e6	nal_rcfg_logic	🔽 1e8	V 1e9	🔲 1e10	🔲 1e11	1e12	apply]									
Meas 510_4cha	sure Eye Once in_25g_inst2 510_nal enable v chan_en sripbł	tive_phy_ip xi	cvr_native_s	10_htile_0 alt_xcvr_native_option PRBS31 PRBS Eye_W/H_1e	nal_rcfg_logic 1e7 6 Eye_W/H_1e7	V 1e8 Eye_W/H_1e8	V 1e9 Eye_W/H_1e9	1e10 Eye_W/H_1e10	1e11 Eye_W/H_1e11	1e12 Eye_W/H_1e12	apply Status) VOD I	Post Pr	e acgain	dcgain	VGA	DFE	Test	_Time		
S10_4cha channel Chan0	sure Eye Once in_25g_inst2 510_nal enable v chan_en sripbl enable v 0	tive_phy_jp xr 2 - K Horiz_step 2 -	vr_native_s	10_htile_0 alt_xcvr_native_option PRB531 PRB5 Eye_W/H_1e PRB531 38/40	nal_rcfg_logic 1e7 6 Eye_W/H_1e7 	V 1e8 Eye_W/H_1e8 32/40	V 1e9 Eye_W/H_1e9 30/40	1e10 Eye_W/H_1e10 	1e11 Eye_W/H_1e11 	1e12 Eye_W/H_1e12 	apply Status Done	VOD 31	Post Pri O O	e acgain 8	dogain 29	VGA 19	DFE 46,0,2,5,3,2,2,3,3,1,1,1,	Test 1,1,0 17 s	_Time ec		
S10_4cha channel Chan0 Chan1	n_25g_inst2 510_nal enable • chan_en sripbl enable • 0 enable • 0	tive_phy_ip xr 2	Vert_step	10_htile_0 alt_xcvr_native_option PRBS1 PRBS Eye_W/H_1e PRBS31 38/40 PRBS31 38/40	nal_rcfg_logic 1e7 6 Eye_W/H_1e7 	✓ 1e8 Eye_W/H_1e8 32/40 32/40	V 1e9 Eye_W/H_1e9 30/40 30/40	1e10 Eye_W/H_1e10 	1e11 Eye_W/H_1e11 	1e12 Eye_W/H_1e12 	apply Status Done Done	VOD 31 31	Post Pri O O O O	e acgain 8 8	dogain 29 28	VGA 19 22	DFE 46,0,2,5,3,2,2,3,3,1,1,1, 57,3,3,4,6,3,3,3,2,1,1,2,	Test 1,1,0 17 s 1,1,1 16 s	_Time ec ec		
S10_4cha channel Chan0 Chan1 Chan2	sure Eye Once n_25g_inst2 510_nal enable chan_en sripbl enable 0 enable 0 enable 0 on ble 0	tive_phy_ip xr 2 • K Horiz_step 2 • 2 •	vr_native_s 2 • Vert_step 2 • 2 • 2 •	10_htle_0[alt_xcvr_native_option PRBS31 → ☑ 1e6 PRBS31 → 38/40 PRBS31 → 38/40 PRBS31 → 38/40 PRBS31 → 42/40	nal_rcfg_logic 1e7 6 Eye_W/H_1e7 	Ie8 Eye_W/H_1e8 32/40 32/40 36/40	V 1e9 Eye_W/H_1e9 30/40 30/40 34/40	1e10 Eye_W/H_1e10 	1e11 Eye_W/H_1e11 	<pre>1e12 Eye_W/H_1e12</pre>	apply Status Done Done Done	VOD 31 31 31	Post Pri O O O O	e acgain 8 8 8	dogain 29 28 28	VGA 19 22 20	DFE 46,0,2,5,3,2,2,3,3,1,1,1,; 57,3,3,4,6,3,3,3,2,1,1,2,; 55,3,3,6,4,3,3,3,3,2,1,2,1;	Test 1,1,0 17s 1,1,1 16s 1,1,1 17s	_Time ec ec		

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Ltile_Htile_Transceiver_EYE_Debug_Tool_v1p0_Beta	
Connext	
Connexis	
Tool_v4p0 based on Q17.1.2	
To Use this tool Hume should be chaded	
Inis too inissue of early ring is and whom is the Curk Singing Park.	
Increasing the Step size will decrease the accuracy	
LogFile in the following Location> log[Eye_measurement_057]ulian_13hr_45min_59sec_sj-catest02-z4.csv	
	Enable or disable the
Measurement Type	
Measure Eye Ore 📄 <u>Eonthnuous Measure Eye Disabled(check to Enablet</u> 🔄 Stop the current measurement	measurement
Phy instance + Chan el	
devices_156280 *(151[251]351)@2#US8-1#Stratix_10H_51_Dev_Uki][510_4chan_25g_inst1[510_native_phy_ip xxvr_native_opbional_rcfg_logic	Choose the horizontal
Messure Eyr OnceConceConceConceConceConceConce Current messurement	step size
510_4chan_25g_st1[510_native_pf_y_p]zvvr_native_s10_Nile_0]alk_xvvr_native_optional_refg_logic	
enable v 2 · 2 v FR6531 v 1/166 V 167 V 168 V 169 1610 1611 1612 apply	Chasses the vertical
channel channen stipbk Hor step Vertisten BRRS Eva Wilh 1a6 Eva Wilh 1a6 Eva Wilh 1a9 Eva Wilh 1a9 Eva Wilh 1a10 Eva Wilh 1a11 Eva Wilh 1a12 Status VOD Dect Dea actain drawin VGB DEE Test Tese	Choose the ventical
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Download the Transceiver Debug Tool



S10_Ltile_Htile_Transceiver_Debug_Tool_V4p0.tcl



Summary

- Needs the least user intervention
- The only way to measure internal high-speed serial interface (HSSI) voltages
- Eye debug tools are 5X faster than Transceiver Toolkit eye plots[†]
- The only tool that can measure eye height and width while running a protocol



BACKUP

Step 1: Program the Device and Open System Console

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Step 2: Load the SOF File in the System Console

Quartus Prime Pro Edition											ð X	System Console - Toolk	ots.	
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Step 3: Load the SOF File in the System Console

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Welcome to Insel's FFGA System Console							
This Tcl console provides access to the hardware modules instantiated in your FPGA. You can use System Console for all of the following purposes:							
* To start, stop, or step a Nice II processor							
* To read or wire Availan Menory-Mapped (Availan-Mel) slaves using special							
masters							
* To sample the SOPC system clock as well as system reset signal * To sample the SOPC system clock as well as system reset signal							
* To run JTAG loopback texts to analyze board noise problems * To run JTAG loopback texts to analyze board noise problems							
instantiated system level debug (ID) nodes							
In addition, the directory «QuartualI Dirs/spoc_builder/system_console/scripts							
contains Tcl files that provide miscellaneous utilities and examples of how to							
access the functionality provided. You can include those macros in your							
actives by issuing ici source commands.							
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[†]Tests measure performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. Consult other sources of information to evaluate performance as you consider your purchase. For more complete information about performance and benchmark results, visit www.intel.com/benchmarks.

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