



Pin Information for the Cyclone® V 5CGXBC7 Device
Version 1.2
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M484	DQS for X8	DQS for X16
GXB_L1		REFCLK1Ln					M5		
GXB_L1		REFCLK1Lp					N4		
GXB_L0		GXB_TX_L2n					J1		
GXB_L0		GXB_TX_L2p					H1		
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					L1		
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					M1		
GXB_L0		GXB_TX_L1n					U1		
GXB_L0		GXB_TX_L1p					V1		
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					Y1		
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					AA1		
GXB_L0		GXB_TX_L0n					AC1		
GXB_L0		GXB_TX_L0p					AD1		
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AF1		
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AG1		
GXB_L0		REFCLK0Lp					AB4		
GXB_L0		REFCLK0Ln					AA3		
3A		TDO		TDO			AE4		
3A		nCSO		DATA4			AE3		
3A		TMS		TMS			AB6		
3A		AS_DATA3		DATA3			AH3		
3A		TCK		TCK			AH2		
3A		AS_DATA2		DATA2			AH4		
3A		TDI		TDI			AA6		
3A		AS_DATA1		DATA1			AF4		
3A		DCLK		DCLK			W5		
3A		AS_DATA0,ASDO		DATA0			AD5		
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	AA7	DQ1B	
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	AE7		
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	Y7	DQ1B	
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	AD7	DQ1B	
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	AC8	DQSn1B	
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	W7	DQ1B	
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	AB8	DQS1B	
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	W6		
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	U6	DQ1B	
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	AF8	DQ1B	
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	T6	DQ1B	
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	AE8	DQ1B	
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	U7		
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	AH9	DQ1B	
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	T7		
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AH8	DQ1B	
3B	VREFB3BN0	IO			DIFFIO_TX_B25n	DIFFOUT_B25n	AE10		
3B	VREFB3BN0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	Y9	DQ4B	
3B	VREFB3BN0	IO			DIFFIO_TX_B25p	DIFFOUT_B25p	AE9	DQ4B	
3B	VREFB3BN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	Y8	DQ4B	
3B	VREFB3BN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	W9	DQSn4B	
3B	VREFB3BN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AB9	DQ4B	
3B	VREFB3BN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	U9	DQS4B	
3B	VREFB3BN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AA8		
3B	VREFB3BN0	IO			DIFFIO_TX_B29n	DIFFOUT_B29n	AH10	DQ4B	
3B	VREFB3BN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	U8	DQ4B	
3B	VREFB3BN0	IO			DIFFIO_TX_B29p	DIFFOUT_B29p	AF10	DQ4B	
3B	VREFB3BN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	T8	DQ4B	
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B31n	DIFFOUT_B31n	W12		
3B	VREFB3BN0	IO			DIFFIO_TX_B32n	DIFFOUT_B32n	AD10	DQ4B	
3B	VREFB3BN0	IO	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B31p	DIFFOUT_B31p	W10		
3B	VREFB3BN0	IO			DIFFIO_TX_B32p	DIFFOUT_B32p	AD9	DQ4B	
3B	VREFB3BN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AC9		
3B	VREFB3BN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AA10	DQ5B	
3B	VREFB3BN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AB10	DQ5B	
3B	VREFB3BN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	Y10	DQ5B	



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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M484	DQS for X8	DQS for X16
3B	VREFB3BN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	AB12	DQS5B	
3B	VREFB3BN0	IO			DIFFIO_TX_B36n	DIFFOUT_B36n	AH12	DQ5B	
3B	VREFB3BN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	AA12	DQS5B	
3B	VREFB3BN0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	AF12	DQ5B	
3B	VREFB3BN0	IO	FPLL_CLKOUT1,FPLL_CLKOUTn		DIFFIO_TX_B37n	DIFFOUT_B37n	AD13	DQ5B	
3B	VREFB3BN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AF13	DQ5B	
3B	VREFB3BN0	IO	FPLL_CLKOUT0,FPLL_CLKOUTp,FPLL_FB		DIFFIO_TX_B37p	DIFFOUT_B37p	AC12	DQ5B	
3B	VREFB3BN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AE13	DQ5B	
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B39n	DIFFOUT_B39n	AA16		
3B	VREFB3BN0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	AA13	DQ5B	
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B39p	DIFFOUT_B39p	Y16		
3B	VREFB3BN0	IO			DIFFIO_TX_B40p	DIFFOUT_B40p	Y13	DQ5B	
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B41n	DIFFOUT_B41n	AB17		
4A	VREFB4AN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AC17	DQ6B	
4A	VREFB4AN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AB16	DQ6B	
4A	VREFB4AN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	AC16	DQ6B	
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	Y17	DQS6B	
4A	VREFB4AN0	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	AH16	DQ6B	
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	W17	DQS6B	
4A	VREFB4AN0	IO			DIFFIO_TX_B44p	DIFFOUT_B44p	AH17		
4A	VREFB4AN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	AE16	DQ6B	
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AA20	DQ6B	
4A	VREFB4AN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	AE17	DQ6B	
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	Y19	DQ6B	
4A	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B47n	DIFFOUT_B47n	U20		
4A	VREFB4AN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	AB19	DQ6B	
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B47p	DIFFOUT_B47p	U19		
4A	VREFB4AN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	AA19	DQ6B	
4A	VREFB4AN0	IO			DIFFIO_TX_B49n	DIFFOUT_B49n	AH20		
4A	VREFB4AN0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	AH19	DQ7B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AF21	DQ7B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	AF20	DQ7B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B51n	DIFFOUT_B51n	W20	DQS7B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B52n	DIFFOUT_B52n	AE21	DQ7B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B51p	DIFFOUT_B51p	W19	DQS7B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B52p	DIFFOUT_B52p	AD21		
4A	VREFB4AN0	IO			DIFFIO_TX_B53n	DIFFOUT_B53n	AH22	DQ7B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B54n	DIFFOUT_B54n	AF19	DQ7B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B53p	DIFFOUT_B53p	AF22	DQ7B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B54p	DIFFOUT_B54p	AE19	DQ7B	DQ1B
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B55n	DIFFOUT_B55n	AA21		
4A	VREFB4AN0	IO			DIFFIO_TX_B56n	DIFFOUT_B56n	AH25	DQ7B	DQ1B
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B55p	DIFFOUT_B55p	Y21		
4A	VREFB4AN0	IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AH24	DQ7B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B57n	DIFFOUT_B57n	AH28		
4A	VREFB4AN0	IO			DIFFIO_RX_B58n	DIFFOUT_B58n	AC22	DQ8B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B57p	DIFFOUT_B57p	AG28	DQ8B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B58p	DIFFOUT_B58p	AC21	DQ8B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	AC20	DQS8B	DQS1B
4A	VREFB4AN0	IO			DIFFIO_TX_B60n	DIFFOUT_B60n	AF28	DQ8B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	AB20	DQS8B	DQS1B
4A	VREFB4AN0	IO			DIFFIO_TX_B60p	DIFFOUT_B60p	AE28		
4A	VREFB4AN0	IO			DIFFIO_TX_B61n	DIFFOUT_B61n	AH26	DQ8B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B62n	DIFFOUT_B62n	AE24	DQ8B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	AF25	DQ8B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B62p	AD24	DQ8B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B63n	DIFFOUT_B63n	AB22		
4A	VREFB4AN0	IO			DIFFIO_TX_B64n	DIFFOUT_B64n	AF26	DQ8B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B63p	DIFFOUT_B63p	AA22		
4A	VREFB4AN0	IO			DIFFIO_TX_B64p	DIFFOUT_B64p	AE25	DQ8B	DQ1B
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	AC28	DQ1R	
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	AB24		



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Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M484	DQS for X8	DQS for X16
5A	VREFB5A0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	AB28	DQ1R	
5A	VREFB5A0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	AB25		
5A	VREFB5A0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	AA26	DQ1R	
5A	VREFB5A0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	AB23	DQ1R	
5A	VREFB5A0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	Y26	DQ1R	
5A	VREFB5A0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	AA24	DQ1R	
5A	VREFB5A0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	AA28		
5A	VREFB5A0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	Y23	DQS1R	
5A	VREFB5A0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	Y28	DQ1R	
5A	VREFB5A0	IO			DIFFIO_RX_R6n	DIFFOUT_R6n	Y24	DQSn1R	
5A	VREFB5A0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	W25	DQ1R	
5A	VREFB5A0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	W23	DQ1R	
5A	VREFB5A0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	W26		
5A	VREFB5A0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	W24	DQ1R	
5B	VREFB5B0	IO	CLK6p		DIFFIO_RX_R33p	DIFFOUT_R33p	T20		
5B	VREFB5B0	IO			DIFFIO_TX_R34p	DIFFOUT_R34p	U22	DQ5R	
5B	VREFB5B0	IO	CLK6n		DIFFIO_RX_R33n	DIFFOUT_R33n	U21		
5B	VREFB5B0	IO			DIFFIO_TX_R34n	DIFFOUT_R34n	T22	DQ5R	
5B	VREFB5B0	IO			DIFFIO_RX_R35p	DIFFOUT_R35p	T25	DQ5R	
5B	VREFB5B0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R36p	DIFFOUT_R36p	U26	DQ5R	
5B	VREFB5B0	IO			DIFFIO_RX_R35n	DIFFOUT_R35n	U25	DQ5R	
5B	VREFB5B0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R36n	DIFFOUT_R36n	V28	DQ5R	
5B	VREFB5B0	IO			DIFFIO_RX_R37p	DIFFOUT_R37p	N21	DQS5R	
5B	VREFB5B0	IO			DIFFIO_TX_R38p	DIFFOUT_R38p	U28		
5B	VREFB5B0	IO			DIFFIO_RX_R37n	DIFFOUT_R37n	M21	DQSn5R	
5B	VREFB5B0	IO			DIFFIO_TX_R38n	DIFFOUT_R38n	T28	DQ5R	
5B	VREFB5B0	IO			DIFFIO_RX_R39p	DIFFOUT_R39p	N22	DQ5R	
5B	VREFB5B0	IO			DIFFIO_TX_R40p	DIFFOUT_R40p	T23	DQ5R	
5B	VREFB5B0	IO			DIFFIO_RX_R39n	DIFFOUT_R39n	M22	DQ5R	
5B	VREFB5B0	IO			DIFFIO_TX_R40n	DIFFOUT_R40n	T24		
6A	VREFB6A0	IO	CLK5p		DIFFIO_RX_R41p	DIFFOUT_R41p	J19		
6A	VREFB6A0	IO			DIFFIO_TX_R42p	DIFFOUT_R42p	N26	DQ6R	
6A	VREFB6A0	IO	CLK5n		DIFFIO_RX_R41n	DIFFOUT_R41n	K20		
6A	VREFB6A0	IO			DIFFIO_TX_R42n	DIFFOUT_R42n	M26	DQ6R	
6A	VREFB6A0	IO			DIFFIO_RX_R43p	DIFFOUT_R43p	M24	DQ6R	
6A	VREFB6A0	IO	FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTp,FPLL_TR_FB		DIFFIO_TX_R44p	DIFFOUT_R44p	K25	DQ6R	
6A	VREFB6A0	IO			DIFFIO_RX_R43n	DIFFOUT_R43n	N25	DQ6R	
6A	VREFB6A0	IO	FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTn		DIFFIO_TX_R44n	DIFFOUT_R44n	K26	DQ6R	
6A	VREFB6A0	IO			DIFFIO_RX_R45p	DIFFOUT_R45p	J20	DQS6R	
6A	VREFB6A0	IO			DIFFIO_TX_R46p	DIFFOUT_R46p	M28		
6A	VREFB6A0	IO			DIFFIO_RX_R45n	DIFFOUT_R45n	K21	DQSn6R	
6A	VREFB6A0	IO			DIFFIO_TX_R46n	DIFFOUT_R46n	L28	DQ6R	
6A	VREFB6A0	IO			DIFFIO_RX_R47p	DIFFOUT_R47p	K23	DQ6R	
6A	VREFB6A0	IO			DIFFIO_TX_R48p	DIFFOUT_R48p	K28	DQ6R	
6A	VREFB6A0	IO			DIFFIO_RX_R47n	DIFFOUT_R47n	J23	DQ6R	
6A	VREFB6A0	IO			DIFFIO_TX_R48n	DIFFOUT_R48n	J28		
6A	VREFB6A0	IO			DIFFIO_RX_R57p	DIFFOUT_R57p	H19		
6A	VREFB6A0	IO			DIFFIO_TX_R58p	DIFFOUT_R58p	E26	DQ8R	
6A	VREFB6A0	IO			DIFFIO_RX_R57n	DIFFOUT_R57n	H20		
6A	VREFB6A0	IO			DIFFIO_TX_R58n	DIFFOUT_R58n	D26	DQ8R	
6A	VREFB6A0	IO			DIFFIO_RX_R59p	DIFFOUT_R59p	J24	DQ8R	
6A	VREFB6A0	IO			DIFFIO_TX_R60p	DIFFOUT_R60p	C28	DQ8R	
6A	VREFB6A0	IO			DIFFIO_RX_R59n	DIFFOUT_R59n	J25	DQ8R	
6A	VREFB6A0	IO			DIFFIO_TX_R60n	DIFFOUT_R60n	B28	DQ8R	
6A	VREFB6A0	IO			DIFFIO_RX_R61p	DIFFOUT_R61p	H21	DQS8R	
6A	VREFB6A0	IO			DIFFIO_TX_R62p	DIFFOUT_R62p	G26		
6A	VREFB6A0	IO			DIFFIO_RX_R61n	DIFFOUT_R61n	H22	DQSn8R	
6A	VREFB6A0	IO			DIFFIO_TX_R62n	DIFFOUT_R62n	G28	DQ8R	
6A	VREFB6A0	IO			DIFFIO_RX_R63p	DIFFOUT_R63p	H24	DQ8R	
6A	VREFB6A0	IO			DIFFIO_TX_R64p	DIFFOUT_R64p	F28	DQ8R	
6A	VREFB6A0	IO			DIFFIO_RX_R63n	DIFFOUT_R63n	H25	DQ8R	
6A	VREFB6A0	IO			DIFFIO_TX_R64n	DIFFOUT_R64n	E28		



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		GND					D25		
7A	VREFB7A0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	F20		
7A	VREFB7A0	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	G23	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	E20		
7A	VREFB7A0	IO			DIFFIO_TX_T18n	DIFFOUT_T18n	G22	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	G21	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	E22	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	F21	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	D22	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	G19	DQS3T	DQS2T
7A	VREFB7A0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	A28		
7A	VREFB7A0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	F19	DQSn3T	DQSn2T
7A	VREFB7A0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	A27	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	A22	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	A26	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	A21	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T24n	DIFFOUT_T24n	A25		
7A	VREFB7A0	IO	CLK11p		DIFFIO_RX_T25p	DIFFOUT_T25p	K17		
7A	VREFB7A0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	E24	DQ4T	DQ2T
7A	VREFB7A0	IO	CLK11n		DIFFIO_RX_T25n	DIFFOUT_T25n	J17		
7A	VREFB7A0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	D24	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	D20	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	A20	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	C19	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	A19	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	K16	DQS4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	C22		
7A	VREFB7A0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	J16	DQSn4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	C21	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	E17	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	G17	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	E16	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	F17		
7A	VREFB7A0	IO	CLK10p		DIFFIO_RX_T33p	DIFFOUT_T33p	H16		
7A	VREFB7A0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	K13	DQ5T	
7A	VREFB7A0	IO	CLK10n		DIFFIO_RX_T33n	DIFFOUT_T33n	G16		
7A	VREFB7A0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	K12	DQ5T	
7A	VREFB7A0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	D16	DQ5T	
7A	VREFB7A0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	J12	DQ5T	
7A	VREFB7A0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	C17	DQ5T	
7A	VREFB7A0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	H13	DQ5T	
7A	VREFB7A0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	J10	DQS5T	
7A	VREFB7A0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	F13		
7A	VREFB7A0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	H10	DQSn5T	
7A	VREFB7A0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	F12	DQ5T	
7A	VREFB7A0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	G10	DQ5T	
7A	VREFB7A0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	E12	DQ5T	
7A	VREFB7A0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	G9	DQ5T	
7A	VREFB7A0	IO	RZQ_2		DIFFIO_TX_T40n	DIFFOUT_T40n	D13		
8A	VREFB8A0	IO	CLK9p		DIFFIO_RX_T41p	DIFFOUT_T41p	N9		
8A	VREFB8A0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	C9	DQ6T	
8A	VREFB8A0	IO	CLK9n		DIFFIO_RX_T41n	DIFFOUT_T41n	M10		
8A	VREFB8A0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	C8	DQ6T	
8A	VREFB8A0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	D12	DQ6T	
8A	VREFB8A0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T44p	DIFFOUT_T44p	A13	DQ6T	
8A	VREFB8A0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	C13	DQ6T	
8A	VREFB8A0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T44n	DIFFOUT_T44n	A12	DQ6T	
8A	VREFB8A0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	K9	DQS6T	
8A	VREFB8A0	IO			DIFFIO_TX_T46p	DIFFOUT_T46p	D8		
8A	VREFB8A0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	J9	DQSn6T	
8A	VREFB8A0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	C7	DQ6T	
8A	VREFB8A0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	E10	DQ6T	



Pin Information for the Cyclone® V 5CGXBC7 Device
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Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M484	DQS for X8	DQS for X16
8A	VREFB8A0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	A10	DQ6T	
8A	VREFB8A0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	E9	DQ6T	
8A	VREFB8A0	IO			DIFFIO_TX_T48n	DIFFOUT_T48n	A9		
8A	VREFB8A0	IO	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T49p	DIFFOUT_T49p	N8		
8A	VREFB8A0	IO			DIFFIO_TX_T50p	DIFFOUT_T50p	A5	DQ7T	
8A	VREFB8A0	IO	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T49n	DIFFOUT_T49n	M9		
8A	VREFB8A0	IO			DIFFIO_TX_T50n	DIFFOUT_T50n	A4	DQ7T	
8A	VREFB8A0	IO			DIFFIO_RX_T51p	DIFFOUT_T51p	D10	DQ7T	
8A	VREFB8A0	IO			DIFFIO_TX_T52p	DIFFOUT_T52p	K7	DQ7T	
8A	VREFB8A0	IO			DIFFIO_RX_T51n	DIFFOUT_T51n	C10	DQ7T	
8A	VREFB8A0	IO			DIFFIO_TX_T52n	DIFFOUT_T52n	K6	DQ7T	
8A	VREFB8A0	IO			DIFFIO_RX_T53p	DIFFOUT_T53p	K8	DQS7T	
8A	VREFB8A0	IO			DIFFIO_TX_T54p	DIFFOUT_T54p	J6		
8A	VREFB8A0	IO			DIFFIO_RX_T53n	DIFFOUT_T53n	J8	DQSn7T	
8A	VREFB8A0	IO			DIFFIO_TX_T54n	DIFFOUT_T54n	H6	DQ7T	
8A	VREFB8A0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	H8	DQ7T	
8A	VREFB8A0	IO			DIFFIO_TX_T56p	DIFFOUT_T56p	F8	DQ7T	
8A	VREFB8A0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	H7	DQ7T	
8A	VREFB8A0	IO			DIFFIO_TX_T56n	DIFFOUT_T56n	E8		
9A		MSEL0		MSEL0			F7		
9A		CONF_DONE		CONF_DONE			D4		
9A		MSEL1		MSEL1			G7		
9A		nSTATUS		nSTATUS			A3		
9A		nCE		nCE			C3		
9A		MSEL2		MSEL2			A2		
9A		MSEL3		MSEL3			E4		
9A		nCONFIG		nCONFIG			G3		
9A		MSEL4		MSEL4			E5		
		GND					G4		
		GND					C26		
		GND					M11		
		GND					Y3		
		GND					G12		
		GND					J7		
		GND					K24		
		GND					AB7		
		GND					K5		
		GND					E25		
		GND					N1		
		GND					V13		
		GND					H28		
		GND					N12		
		GND					K22		
		GND					AB21		
		GND					N18		
		GND					AD8		
		GND					AD3		
		GND					AC19		
		GND					M4		
		GND					G24		
		GND					E1		
		GND					D3		
		GND					M13		
		GND					K1		
		GND					F10		
		GND					AB1		
		GND					L16		
		GND					N16		
		GND					C5		
		GND					AB5		
		GND					AF3		
		GND					A8		



Pin Information for the Cyclone® V 5CGXBC7 Device
Version 1.2
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M484	DQS for X8	DQS for X16
		GND					J21		
		GND					T19		
		GND					V17		
		GND					D28		
		GND					U5		
		GND					H23		
		GND					H5		
		GND					A1		
		GND					G1		
		GND					AA23		
		GND					W8		
		GND					W22		
		GND					T11		
		GND					T17		
		GND					J3		
		GND					AD16		
		GND					AE1		
		GND					G20		
		GND					L12		
		GND					N7		
		GND					AH7		
		GND					U18		
		GND					M3		
		GND					Y25		
		GND					AH1		
		GND					N28		
		GND					U10		
		GND					T13		
		GND					M17		
		GND					K10		
		GND					Y5		
		GND					L18		
		GND					N10		
		GND					U16		
		GND					A16		
		GND					A24		
		GND					AB13		
		GND					AF24		
		GND					H17		
		GND					AE20		
		GND					AA17		
		GND					W4		
		GND					T1		
		GND					D21		
		GND					AA4		
		GND					H3		
		GND					H9		
		GND					Y6		
		GND					U24		
		GND					K19		
		GND					AB3		
		GND					U12		
		GND					AD28		
		GND					M8		
		GND					M19		
		GND					T4		
		GND					W1		
		GND					U3		
		GND					C1		
		GND					E13		
		GND					N20		
		GND					V11		



Pin Information for the Cyclone® V 5CGXBC7 Device
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Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M484	DQS for X8	DQS for X16
		GND					AA9		
		GND					T9		
		VCC					N17		
		VCC					V18		
		VCC					L13		
		VCC					N11		
		VCC					M12		
		VCC					N13		
		VCC					M16		
		VCC					T18		
		VCC					T10		
		VCC					V12		
		VCC					U17		
		VCC					M18		
		VCC					U11		
		VCC					U13		
		VCC					L17		
		VCC					V16		
		VCC					T16		
		VCC					N19		
		VCC					L11		
		VCC					T12		
		DNU					F1		
		DNU					D1		
		DNU					AA5		
		DNU					W16		
		DNU					C25		
		DNU					H12		
		VCCPGM					AH5		
		VCCPGM					AD26		
		VCCPGM					D7		
		VCCBAT					C4		
		VCCIO3A					AF9		
		VCCIO3A					AE5		
		VCCIO3B					AE12		
		VCCIO3B					AC10		
		VCCIO3B					AH13		
		VCCIO3B					Y12		
		VCCIO4A					AH27		
		VCCIO4A					AE26		
		VCCIO4A					Y20		
		VCCIO4A					AF17		
		VCCIO4A					AH21		
		VCCIO4A					AD22		
		VCCIO5A					AB26		
		VCCIO5A					W28		
		VCCIO5B					M20		
		VCCIO5B					T21		
		VCCIO5B					N23		
		VCCIO5B					T26		
		VCCIO6A					J26		
		VCCIO6A					M25		
		VCCIO7A					D17		
		VCCIO7A					E19		
		VCCIO7A					C20		
		VCCIO7A					F22		
		VCCIO7A					J13		
		VCCIO7A					F16		
		VCCIO8A					C12		
		VCCIO8A					D9		
		VCCIO8A					G8		
		VCCIO8A					E7		



Pin Information for the Cyclone® V 5CGXBC7 Device
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Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M484	DQS for X8	DQS for X16
		VCCPD3A					AC7		
		VCCPD3B4A					AD20		
		VCCPD3B4A					AD17		
		VCCPD3B4A					AD12		
		VCCPD3B4A					AC13		
		VCCPD5A					Y22		
		VCCPD5B					N24		
		VCCPD5B					U23		
		VCCPD6A					J22		
		VCCPD7A8A					G13		
		VCCPD7A8A					E21		
		VCCPD7A8A					D19		
		VCCPD7A8A					F9		
3A	VREFB3AN0	VREFB3AN0					AF7		
3B	VREFB3BN0	VREFB3BN0					W13		
4A	VREFB4AN0	VREFB4AN0					AD19		
5A	VREFB5AN0	VREFB5AN0					AA25		
5B	VREFB5BN0	VREFB5BN0					M23		
6A	VREFB6AN0	VREFB6AN0					H26		
7A	VREFB7AN0	VREFB7AN0					A17		
8A	VREFB8AN0	VREFB8AN0					A7		
		NC					J5		
		NC					K4		
		NC					M6		
		NC					T5		
		NC					G6		
		NC					J4		
		NC					N5		
		NC					M7		
		NC					H4		
		NC					W21		
		NC					N3		
		NC					G5		
		NC					N6		
		NC					K3		
		VCCH_GXBL					W3		
		VCCL_GXBL					T3		
		RREF_TL					B1		
		VCCA_FPLL					AD4		
		VCCA_FPLL					E3		
		VCCA_FPLL					AD25		
		VCCA_FPLL					G25		
		VCC_AUX					C24		
		VCC_AUX					AE22		
		VCC_AUX					D5		
		VCC_AUX					AF16		
		VCC_AUX					AF5		
		VCC_AUX					C16		
		VCCE_GXBL					U4		
		VCCE_GXBL					Y4		

Note:
(1) For more information about pin definition and pin connection guidelines, refer to the [Cyclone V Device Family Pin Connection Guidelines](#).



Pin Information for the Cyclone® V 5CGXBC7 Device
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Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16
GXB_L1		REFCLK1Ln					G4		
GXB_L1		REFCLK1Lp					F5		
GXB_L1		GXB_TX_L5n					D3		
GXB_L1		GXB_TX_L5p					D4		
GXB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					C2		
GXB_L1		GXB_RX_L5n,GXB_REFCLK_L5n					C1		
GXB_L1		GXB_TX_L4n					E1		
GXB_L1		GXB_TX_L4p					E2		
GXB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					G2		
GXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					G1		
GXB_L1		GXB_TX_L3n					J1		
GXB_L1		GXB_TX_L3p					J2		
GXB_L1		GXB_RX_L3p,GXB_REFCLK_L3p					L2		
GXB_L1		GXB_RX_L3n,GXB_REFCLK_L3n					L1		
GXB_L0		GXB_TX_L2n					N1		
GXB_L0		GXB_TX_L2p					N2		
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					R2		
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					R1		
GXB_L0		GXB_TX_L1n					U1		
GXB_L0		GXB_TX_L1p					U2		
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					W2		
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					W1		
GXB_L0		GXB_TX_L0n					Y3		
GXB_L0		GXB_TX_L0p					Y4		
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AA2		
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AA1		
GXB_L0		REFCLK0Lp					V4		
GXB_L0		REFCLK0Ln					U4		
3A		TDO		TDO			V3		
3A		nCSO		DATA4			AB6		
3A		TMS		TMS			R4		
3A		AS_DATA3		DATA3			AA5		
3A		TCK		TCK			V5		
3A		AS_DATA2		DATA2			T5		
3A		TDI		TDI			P5		
3A		AS_DATA1		DATA1			W5		
3A		DCLK		DCLK			M5		
3A		AS_DATA0,ASDO		DATA0			AB4		
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	P6	DQ1B	
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	U7		
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	N6	DQ1B	
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	U6	DQ1B	
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	M6	DQSn1B	
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	R5	DQ1B	
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	M7	DQS1B	
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	R6		
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	R7	DQ1B	
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	L7	DQ1B	
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	T7	DQ1B	
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	L8	DQ1B	
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	T8		
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	P7	DQ1B	
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	T9		
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	P8	DQ1B	
3B	VREFB3BN0	IO			DIFFIO_TX_B25n	DIFFOUT_B25n	V8		
3B	VREFB3BN0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	N8	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B25p	DIFFOUT_B25p	W8	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	M8	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	N9	DQSn2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AA7	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	N10	DQS2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AB7		



Pin Information for the Cyclone® V 5CGXBC7 Device
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Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16
3B	VREFB3BN0	IO			DIFFIO_TX_B29n	DIFFOUT_B29n	Y7	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	U8	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B29p	DIFFOUT_B29p	W7	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	V9	DQ2B	
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B31n	DIFFOUT_B31n	R9		
3B	VREFB3BN0	IO			DIFFIO_TX_B32n	DIFFOUT_B32n	AB8	DQ2B	
3B	VREFB3BN0	IO	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B31p	DIFFOUT_B31p	P9		
3B	VREFB3BN0	IO			DIFFIO_TX_B32p	DIFFOUT_B32p	AA8	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	Y10		
3B	VREFB3BN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AA9	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AA10	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	Y9	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	L9	DQSn3B	
3B	VREFB3BN0	IO			DIFFIO_TX_B36n	DIFFOUT_B36n	W11	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	M10	DQSn3B	
3B	VREFB3BN0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	Y11		
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B37n	DIFFOUT_B37n	AB10	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	U10	DQ3B	
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B37p	DIFFOUT_B37p	AB11	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	U11	DQ3B	
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B39n	DIFFOUT_B39n	T10		
3B	VREFB3BN0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	R11	DQ3B	
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B39p	DIFFOUT_B39p	R10		
3B	VREFB3BN0	IO			DIFFIO_TX_B40p	DIFFOUT_B40p	P12	DQ3B	
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B41n	DIFFOUT_B41n	AA13		
4A	VREFB4AN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	W12	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AB13	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	Y12	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	U12	DQSn4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	R12	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	T12	DQSn4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B44p	DIFFOUT_B44p	T13		
4A	VREFB4AN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	AB15	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	W13	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	AB16	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	V13	DQ4B	
4A	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B47n	DIFFOUT_B47n	T14		
4A	VREFB4AN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	AB18	DQ4B	
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B47p	DIFFOUT_B47p	U13		
4A	VREFB4AN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	AA18	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B49n	DIFFOUT_B49n	AA19		
4A	VREFB4AN0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	Y14	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	Y19	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	W14	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B51n	DIFFOUT_B51n	P14	DQSn5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B52n	DIFFOUT_B52n	AA20	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B51p	DIFFOUT_B51p	R14	DQSn5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B52p	DIFFOUT_B52p	Y20		
4A	VREFB4AN0	IO			DIFFIO_TX_B53n	DIFFOUT_B53n	AA15	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B54n	DIFFOUT_B54n	U15	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B53p	DIFFOUT_B53p	Y15	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B54p	DIFFOUT_B54p	V15	DQ5B	DQ1B
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B55n	DIFFOUT_B55n	R15		
4A	VREFB4AN0	IO			DIFFIO_TX_B56n	DIFFOUT_B56n	AB20	DQ5B	DQ1B
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B55p	DIFFOUT_B55p	T15		
4A	VREFB4AN0	IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AB21	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B57n	DIFFOUT_B57n	AB22		
4A	VREFB4AN0	IO			DIFFIO_RX_B58n	DIFFOUT_B58n	Y16	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B57p	DIFFOUT_B57p	AA22	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B58p	DIFFOUT_B58p	Y17	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	U16	DQSn6B	DQSn1B
4A	VREFB4AN0	IO			DIFFIO_TX_B60n	DIFFOUT_B60n	AA17	DQ6B	DQ1B



Pin Information for the Cyclone® V 5CGXBC7 Device
Version 1.2
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	U17	DQS6B	DQS1B
4A	VREFB4AN0	IO			DIFFIO_TX_B60p	DIFFOUT_B60p	AB17		
4A	VREFB4AN0	IO			DIFFIO_TX_B61n	DIFFOUT_B61n	Y22	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B62n	DIFFOUT_B62n	V18	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	Y21	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B62p	W18	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B63n	DIFFOUT_B63n	W16		
4A	VREFB4AN0	IO			DIFFIO_TX_B64n	DIFFOUT_B64n	W21	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B63p	DIFFOUT_B63p	W17		
4A	VREFB4AN0	IO			DIFFIO_TX_B64p	DIFFOUT_B64p	W22	DQ6B	DQ1B
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	U22	DQ1R	
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	V20		
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	U21	DQ1R	
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	V19		
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	T19	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	T17	DQ1R	
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	T20	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	T18	DQ1R	
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	T22		
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	R16	DQS1R	
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	R22	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R6n	R17	DQSn1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	R20	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	R19	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	R21		
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	P19	DQ1R	
5B	VREFB5BN0	IO			DIFFIO_RX_R17p	DIFFOUT_R17p	P16		
5B	VREFB5BN0	IO			DIFFIO_TX_R18p	DIFFOUT_R18p	P21	DQ2R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_RX_R17n	DIFFOUT_R17n	N16		
5B	VREFB5BN0	IO			DIFFIO_TX_R18n	DIFFOUT_R18n	P22	DQ2R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_RX_R19p	DIFFOUT_R19p	N20	DQ2R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_TX_R20p	DIFFOUT_R20p	M22	DQ2R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_RX_R19n	DIFFOUT_R19n	N21	DQ2R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_TX_R20n	DIFFOUT_R20n	L22	DQ2R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_RX_R21p	DIFFOUT_R21p	P18	DQS2R	DQS1R
5B	VREFB5BN0	IO			DIFFIO_TX_R22p	DIFFOUT_R22p	K22		
5B	VREFB5BN0	IO			DIFFIO_RX_R21n	DIFFOUT_R21n	N18	DQSn2R	DQSn1R
5B	VREFB5BN0	IO			DIFFIO_TX_R22n	DIFFOUT_R22n	J22	DQ2R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_RX_R23p	DIFFOUT_R23p	M21	DQ2R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_TX_R24p	DIFFOUT_R24p	F22	DQ2R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	M20	DQ2R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_TX_R24n	DIFFOUT_R24n	E22		
5B	VREFB5BN0	IO	CLK7p.FPLL_BR_FBp		DIFFIO_RX_R25p	DIFFOUT_R25p	M16		
5B	VREFB5BN0	IO			DIFFIO_TX_R26p	DIFFOUT_R26p	E21	DQ3R	DQ1R
5B	VREFB5BN0	IO	CLK7n.FPLL_BR_FBn		DIFFIO_RX_R25n	DIFFOUT_R25n	M17		
5B	VREFB5BN0	IO			DIFFIO_TX_R26n	DIFFOUT_R26n	D22	DQ3R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_RX_R27p	DIFFOUT_R27p	L19	DQ3R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_TX_R28p	DIFFOUT_R28p	K21	DQ3R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_RX_R27n	DIFFOUT_R27n	L20	DQ3R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_TX_R28n	DIFFOUT_R28n	J21	DQ3R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_RX_R29p	DIFFOUT_R29p	L15	DQS3R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_TX_R30p	DIFFOUT_R30p	G22		
5B	VREFB5BN0	IO			DIFFIO_RX_R29n	DIFFOUT_R29n	K15	DQSn3R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_TX_R30n	DIFFOUT_R30n	G21	DQ3R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_RX_R31p	DIFFOUT_R31p	L18	DQ3R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_TX_R32p	DIFFOUT_R32p	G20	DQ3R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_RX_R31n	DIFFOUT_R31n	K19	DQ3R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_TX_R32n	DIFFOUT_R32n	H21		
5B	VREFB5BN0	IO	CLK6p		DIFFIO_RX_R33p	DIFFOUT_R33p	L17		
5B	VREFB5BN0	IO			DIFFIO_TX_R34p	DIFFOUT_R34p	E20	DQ4R	
5B	VREFB5BN0	IO	CLK6n		DIFFIO_RX_R33n	DIFFOUT_R33n	K17		
5B	VREFB5BN0	IO			DIFFIO_TX_R34n	DIFFOUT_R34n	F20	DQ4R	



Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16
5B	VREFB5B0	IO			DIFFIO_RX_R35p	DIFFOUT_R35p	H20	DQ4R	
5B	VREFB5B0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R36p	DIFFOUT_R36p	G18	DQ4R	
5B	VREFB5B0	IO			DIFFIO_RX_R35n	DIFFOUT_R35n	H19	DQ4R	
5B	VREFB5B0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R36n	DIFFOUT_R36n	G17	DQ4R	
5B	VREFB5B0	IO			DIFFIO_RX_R37p	DIFFOUT_R37p	K16	DQS4R	
5B	VREFB5B0	IO			DIFFIO_TX_R38p	DIFFOUT_R38p	F19		
5B	VREFB5B0	IO			DIFFIO_RX_R37n	DIFFOUT_R37n	J16	DQSn4R	
5B	VREFB5B0	IO			DIFFIO_TX_R38n	DIFFOUT_R38n	F18	DQ4R	
5B	VREFB5B0	IO			DIFFIO_RX_R39p	DIFFOUT_R39p	J17	DQ4R	
5B	VREFB5B0	IO			DIFFIO_TX_R40p	DIFFOUT_R40p	J19	DQ4R	
5B	VREFB5B0	IO			DIFFIO_RX_R39n	DIFFOUT_R39n	J18	DQ4R	
5B	VREFB5B0	IO			DIFFIO_TX_R40n	DIFFOUT_R40n	H18		
7A		GND					F17		
7A	VREFB7A0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	H16		
7A	VREFB7A0	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	C21	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	G16		
7A	VREFB7A0	IO			DIFFIO_TX_T18n	DIFFOUT_T18n	C20	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	D18	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	B20	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	E17	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	B21	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	G15	DQS1T	DQS1T
7A	VREFB7A0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	B22		
7A	VREFB7A0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	G14	DQSn1T	DQSn1T
7A	VREFB7A0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	A22	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	E16	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	A20	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	D17	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T24n	DIFFOUT_T24n	A19		
7A	VREFB7A0	IO	CLK11p		DIFFIO_RX_T25p	DIFFOUT_T25p	G13		
7A	VREFB7A0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	C19	DQ2T	DQ1T
7A	VREFB7A0	IO	CLK11n		DIFFIO_RX_T25n	DIFFOUT_T25n	F14		
7A	VREFB7A0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	C18	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	C16	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	B16	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	C15	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	B15	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	G12	DQS2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	A18		
7A	VREFB7A0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	H12	DQSn2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	A17	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	F15	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	B18	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	E14	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	B17		
7A	VREFB7A0	IO	CLK10p		DIFFIO_RX_T33p	DIFFOUT_T33p	H10		
7A	VREFB7A0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	A15	DQ3T	
7A	VREFB7A0	IO	CLK10n		DIFFIO_RX_T33n	DIFFOUT_T33n	G11		
7A	VREFB7A0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	A14	DQ3T	
7A	VREFB7A0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	D13	DQ3T	
7A	VREFB7A0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	C14	DQ3T	
7A	VREFB7A0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	C13	DQ3T	
7A	VREFB7A0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	D14	DQ3T	
7A	VREFB7A0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	H9	DQS3T	
7A	VREFB7A0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	A13		
7A	VREFB7A0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	G8	DQSn3T	
7A	VREFB7A0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	B13	DQ3T	
7A	VREFB7A0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	E12	DQ3T	
7A	VREFB7A0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	B12	DQ3T	
7A	VREFB7A0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	F12	DQ3T	
7A	VREFB7A0	IO	RZQ_2		DIFFIO_TX_T40n	DIFFOUT_T40n	A12		
8A	VREFB8A0	IO	CLK9p		DIFFIO_RX_T41p	DIFFOUT_T41p	G10		



Pin Information for the Cyclone® V 5CGXBC7 Device
Version 1.2
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16
8A	VREFB8A0	IO			DIFFFIO_TX_T42p	DIFFFOUT_T42p	C11	DQ4T	
8A	VREFB8A0	IO	CLK9n		DIFFFIO_RX_T41n	DIFFFOUT_T41n	F10		
8A	VREFB8A0	IO			DIFFFIO_TX_T42n	DIFFFOUT_T42n	B11	DQ4T	
8A	VREFB8A0	IO			DIFFFIO_RX_T43p	DIFFFOUT_T43p	D11	DQ4T	
8A	VREFB8A0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFFIO_TX_T44p	DIFFFOUT_T44p	A8	DQ4T	
8A	VREFB8A0	IO			DIFFFIO_RX_T43n	DIFFFOUT_T43n	E11	DQ4T	
8A	VREFB8A0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFFIO_TX_T44n	DIFFFOUT_T44n	A7	DQ4T	
8A	VREFB8A0	IO			DIFFFIO_RX_T45p	DIFFFOUT_T45p	J9	DQS4T	
8A	VREFB8A0	IO			DIFFFIO_TX_T46p	DIFFFOUT_T46p	F8		
8A	VREFB8A0	IO			DIFFFIO_RX_T45n	DIFFFOUT_T45n	J8	DQSn4T	
8A	VREFB8A0	IO			DIFFFIO_TX_T46n	DIFFFOUT_T46n	E7	DQ4T	
8A	VREFB8A0	IO			DIFFFIO_RX_T47p	DIFFFOUT_T47p	C10	DQ4T	
8A	VREFB8A0	IO			DIFFFIO_TX_T48p	DIFFFOUT_T48p	C6	DQ4T	
8A	VREFB8A0	IO			DIFFFIO_RX_T47n	DIFFFOUT_T47n	C9	DQ4T	
8A	VREFB8A0	IO			DIFFFIO_TX_T48n	DIFFFOUT_T48n	D7		
8A	VREFB8A0	IO	CLK8p,FPLL_TL_FBp		DIFFFIO_RX_T49p	DIFFFOUT_T49p	K7		
8A	VREFB8A0	IO			DIFFFIO_TX_T50p	DIFFFOUT_T50p	A10	DQ5T	
8A	VREFB8A0	IO	CLK8n,FPLL_TL_Fbn		DIFFFIO_RX_T49n	DIFFFOUT_T49n	J7		
8A	VREFB8A0	IO			DIFFFIO_TX_T50n	DIFFFOUT_T50n	A9	DQ5T	
8A	VREFB8A0	IO			DIFFFIO_RX_T51p	DIFFFOUT_T51p	D9	DQ5T	
8A	VREFB8A0	IO			DIFFFIO_TX_T52p	DIFFFOUT_T52p	B6	DQ5T	
8A	VREFB8A0	IO			DIFFFIO_RX_T51n	DIFFFOUT_T51n	D8	DQ5T	
8A	VREFB8A0	IO			DIFFFIO_TX_T52n	DIFFFOUT_T52n	B5	DQ5T	
8A	VREFB8A0	IO			DIFFFIO_RX_T53p	DIFFFOUT_T53p	H8	DQS5T	
8A	VREFB8A0	IO			DIFFFIO_TX_T54p	DIFFFOUT_T54p	C8		
8A	VREFB8A0	IO			DIFFFIO_RX_T53n	DIFFFOUT_T53n	G7	DQSn5T	
8A	VREFB8A0	IO			DIFFFIO_TX_T54n	DIFFFOUT_T54n	B8	DQ5T	
8A	VREFB8A0	IO			DIFFFIO_RX_T55p	DIFFFOUT_T55p	H6	DQ5T	
8A	VREFB8A0	IO			DIFFFIO_TX_T56p	DIFFFOUT_T56p	E6	DQ5T	
8A	VREFB8A0	IO			DIFFFIO_RX_T55n	DIFFFOUT_T55n	G6	DQ5T	
8A	VREFB8A0	IO			DIFFFIO_TX_T56n	DIFFFOUT_T56n	F7		
9A		MSEL0		MSEL0			L6		
9A		CONF_DONE		CONF_DONE			J6		
9A		MSEL1		MSEL1			K6		
9A		nSTATUS		nSTATUS			G5		
9A		nCE		nCE			H5		
9A		MSEL2		MSEL2			A2		
9A		MSEL3		MSEL3			E5		
9A		nCONFIG		nCONFIG			A4		
9A		MSEL4		MSEL4			C5		
9A		GND					F3		
		GND					R3		
		GND					AB19		
		GND					AB1		
		GND					AA16		
		GND					AA11		
		GND					AA4		
		GND					Y13		
		GND					Y2		
		GND					W20		
		GND					W4		
		GND					V17		
		GND					V2		
		GND					V1		
		GND					U19		
		GND					U9		
		GND					U5		
		GND					U3		
		GND					T1		
		GND					R13		
		GND					P10		
		GND					P2		



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Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16
		GND					N22		
		GND					N15		
		GND					N13		
		GND					N7		
		GND					M14		
		GND					M9		
		GND					M4		
		GND					M2		
		GND					M1		
		GND					L16		
		GND					L13		
		GND					L11		
		GND					L5		
		GND					L3		
		GND					K14		
		GND					K10		
		GND					K4		
		GND					K1		
		GND					J20		
		GND					J11		
		GND					J5		
		GND					J3		
		GND					H14		
		GND					H3		
		GND					H2		
		GND					F11		
		GND					F6		
		GND					F2		
		GND					F1		
		GND					E3		
		GND					D20		
		GND					D10		
		GND					D5		
		GND					D1		
		GND					C17		
		GND					C3		
		GND					B14		
		GND					B2		
		GND					A11		
		GND					A5		
		GND					AB2		
		GND					AA3		
		GND					Y8		
		GND					Y5		
		GND					Y1		
		GND					W3		
		GND					V22		
		GND					U14		
		GND					T11		
		GND					T2		
		GND					P4		
		GND					P1		
		GND					N11		
		GND					N5		
		GND					N3		
		GND					M19		
		GND					M12		
		GND					K12		
		GND					K8		
		GND					K2		
		GND					J15		
		GND					J13		



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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16
		GND					H4		
		GND					H1		
		GND					G9		
		GND					G3		
		GND					F21		
		GND					F16		
		GND					E13		
		GND					E4		
		GND					D2		
		GND					C22		
		GND					C7		
		GND					C4		
		GND					B1		
		GND					A21		
		VCC					P15		
		VCC					P13		
		VCC					N14		
		VCC					N12		
		VCC					M11		
		VCC					L12		
		VCC					K13		
		VCC					K11		
		VCC					J14		
		VCC					J12		
		VCC					H15		
		VCC					H11		
		VCC					P11		
		VCC					M15		
		VCC					M13		
		VCC					L14		
		VCC					L10		
		VCC					K9		
		VCC					J10		
		VCC					H13		
		DNU					B3		
		DNU					B4		
		DNU					AB3		
		DNU					V11		
		DNU					D21		
		DNU					E10		
		VCCPGM					Y6		
		VCCPGM					U20		
		VCCPGM					B7		
		VCCBAT					A3		
		VCCIO3A					T6		
		VCCIO3A					AA6		
		VCCIO3B					AB9		
		VCCIO3B					W10		
		VCCIO3B					V7		
		VCCIO3B					R8		
		VCCIO4A					AB14		
		VCCIO4A					Y18		
		VCCIO4A					W15		
		VCCIO4A					T16		
		VCCIO4A					AA21		
		VCCIO4A					V12		
		VCCIO5A					T21		
		VCCIO5A					R18		
		VCCIO5B					K18		
		VCCIO5B					N17		
		VCCIO5B					L21		
		VCCIO5B					H22		



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Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16
		VCCIO5B					G19		
		VCCIO5B					P20		
		VCCIO7A					B19		
		VCCIO7A					E18		
		VCCIO7A					C12		
		VCCIO7A					A16		
		VCCIO7A					H17		
		VCCIO7A					D15		
		VCCIO8A					H7		
		VCCIO8A					E8		
		VCCIO8A					B9		
		VCCIO8A					A6		
		VCCPD3A					V6		
		VCCPD3B4A					W9		
		VCCPD3B4A					V16		
		VCCPD3B4A					V14		
		VCCPD3B4A					V10		
		VCCPD5A					P17		
		VCCPD5B					N19		
		VCCPD5B					M18		
		VCCPD7A8A					F13		
		VCCPD7A8A					F9		
		VCCPD7A8A					E15		
		VCCPD7A8A					E9		
3A	VREFB3AN0	VREFB3AN0					W6		
3B	VREFB3BN0	VREFB3BN0					AB12		
4A	VREFB4AN0	VREFB4AN0					AA14		
5A	VREFB5AN0	VREFB5AN0					V21		
5B	VREFB5BN0	VREFB5BN0					K20		
7A	VREFB7AN0	VREFB7AN0					D16		
8A	VREFB8AN0	VREFB8AN0					B10		
		VCCH_GXBL					T3		
		VCCH_GXBL					M3		
		VCCL_GXBL					P3		
		VCCL_GXBL					K3		
		RREF_TL					A1		
		VCCA_FPLL					T4		
		VCCA_FPLL					F4		
		VCCA_FPLL					U18		
		VCCA_FPLL					E19		
		VCC_AUX					D6		
		VCC_AUX					D12		
		VCC_AUX					D19		
		VCC_AUX					W19		
		VCC_AUX					AA12		
		VCC_AUX					AB5		
		VCCE_GXBL					N4		
		VCCE_GXBL					J4		
		VCCE_GXBL					L4		
		VCCE_GXBL					K5		

Note:
(1) For more information about pin definition and pin connection guidelines, refer to the [Cyclone V Device Family Pin Connection Guidelines](#).



Pin Information for the Cyclone® V 5CGXBC7 Device
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Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16
GXB_L1		REFCLK1Ln					F5		
GXB_L1		REFCLK1Lp					G4		
GXB_L1		GXB_TX_L5n					D3		
GXB_L1		GXB_TX_L5p					D4		
GXB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					C2		
GXB_L1		GXB_RX_L5n,GXB_REFCLK_L5n					C1		
GXB_L1		GXB_TX_L4n					E1		
GXB_L1		GXB_TX_L4p					E2		
GXB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					G2		
GXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					G1		
GXB_L1		GXB_TX_L3n					J1		
GXB_L1		GXB_TX_L3p					J2		
GXB_L1		GXB_RX_L3p,GXB_REFCLK_L3p					L2		
GXB_L1		GXB_RX_L3n,GXB_REFCLK_L3n					L1		
GXB_L0		GXB_TX_L2n					N1		
GXB_L0		GXB_TX_L2p					N2		
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					R2		
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					R1		
GXB_L0		GXB_TX_L1n					U1		
GXB_L0		GXB_TX_L1p					U2		
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					W2		
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					W1		
GXB_L0		GXB_TX_L0n					Y3		
GXB_L0		GXB_TX_L0p					Y4		
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AA2		
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AA1		
GXB_L0		REFCLK0Lp					V4		
GXB_L0		REFCLK0Ln					U4		
3A		TDO		TDO			M5		
3A		nCSO		DATA4			R4		
3A		TMS		TMS			P5		
3A		AS_DATA3		DATA3			T4		
3A		TCK		TCK			V5		
3A		AS_DATA2		DATA2			AA5		
3A		TDI		TDI			W5		
3A		AS_DATA1		DATA1			AB3		
3A		DCLK		DCLK			V3		
3A		AS_DATA0,ASDO		DATA0			AB4		
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	R6	DQ1B	
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	U7		
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	R5	DQ1B	
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	U8	DQ1B	
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	P6	DQSn1B	
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	W8	DQ1B	
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	N6	DQS1B	
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	W9		
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	T7	DQ1B	
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	U6	DQ1B	
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	T8	DQ1B	
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	V6	DQ1B	
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	M6		
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	R7	DQ1B	
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	M7		
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	P7	DQ1B	
3B	VREFB3BN0	IO			DIFFIO_TX_B25n	DIFFOUT_B25n	AB6		
3B	VREFB3BN0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	V9	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B25p	DIFFOUT_B25p	AB5	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	V10	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	P8	DQSn2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AA7	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	N8	DQS2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AB7		



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Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16
3B	VREFB3BN0	IO			DIFFIO_TX_B29n	DIFFOUT_B29n	AA8	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	T9	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B29p	DIFFOUT_B29p	AB8	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	U10	DQ2B	
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B31n	DIFFOUT_B31n	M8		
3B	VREFB3BN0	IO			DIFFIO_TX_B32n	DIFFOUT_B32n	AA10	DQ2B	
3B	VREFB3BN0	IO	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B31p	DIFFOUT_B31p	M9		
3B	VREFB3BN0	IO			DIFFIO_TX_B32p	DIFFOUT_B32p	AA9	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	Y10		
3B	VREFB3BN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	T10	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	Y9	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	R9	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	U11	DQS3B	
3B	VREFB3BN0	IO			DIFFIO_TX_B36n	DIFFOUT_B36n	R12	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	U12	DQS3B	
3B	VREFB3BN0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	P12		
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B37n	DIFFOUT_B37n	AB10	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	R10	DQ3B	
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B37p	DIFFOUT_B37p	AB11	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	R11	DQ3B	
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B39n	DIFFOUT_B39n	P9		
3B	VREFB3BN0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	Y11	DQ3B	
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B39p	DIFFOUT_B39p	N9		
3B	VREFB3BN0	IO			DIFFIO_TX_B40p	DIFFOUT_B40p	AA12	DQ3B	
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B41n	DIFFOUT_B41n	AB13		
4A	VREFB4AN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	V13	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AB12	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	U13	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	T12	DQS4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	AA14	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	T13	DQS4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B44p	DIFFOUT_B44p	AA13		
4A	VREFB4AN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	AB15	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	Y14	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	AA15	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	Y15	DQ4B	
4A	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B47n	DIFFOUT_B47n	V14		
4A	VREFB4AN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	AB17	DQ4B	
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B47p	DIFFOUT_B47p	V15		
4A	VREFB4AN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	AB18	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B49n	DIFFOUT_B49n	AB20		
4A	VREFB4AN0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	Y16	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AB21	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	Y17	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B51n	DIFFOUT_B51n	T14	DQS5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B52n	DIFFOUT_B52n	AA17	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B51p	DIFFOUT_B51p	U15	DQS5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B52p	DIFFOUT_B52p	AA18		
4A	VREFB4AN0	IO			DIFFIO_TX_B53n	DIFFOUT_B53n	AA19	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B54n	DIFFOUT_B54n	V20	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B53p	DIFFOUT_B53p	AA20	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B54p	DIFFOUT_B54p	W19	DQ5B	DQ1B
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B55n	DIFFOUT_B55n	V16		
4A	VREFB4AN0	IO			DIFFIO_TX_B56n	DIFFOUT_B56n	AB22	DQ5B	DQ1B
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B55p	DIFFOUT_B55p	W16		
4A	VREFB4AN0	IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AA22	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B57n	DIFFOUT_B57n	Y22		
4A	VREFB4AN0	IO			DIFFIO_RX_B58n	DIFFOUT_B58n	Y20	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B57p	DIFFOUT_B57p	W22	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B58p	DIFFOUT_B58p	Y19	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	P14	DQS6B	DQS1B
4A	VREFB4AN0	IO			DIFFIO_TX_B60n	DIFFOUT_B60n	Y21	DQ6B	DQ1B



Pin Information for the Cyclone® V 5CGXBC7 Device
Version 1.2
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	R14	DQS6B	DQS1B
4A	VREFB4AN0	IO			DIFFIO_TX_B60p	DIFFOUT_B60p	W21		
4A	VREFB4AN0	IO			DIFFIO_TX_B61n	DIFFOUT_B61n	U22	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B62n	DIFFOUT_B62n	V19	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	V21	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B62p	V18	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B63n	DIFFOUT_B63n	U16		
4A	VREFB4AN0	IO			DIFFIO_TX_B64n	DIFFOUT_B64n	U21	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B63p	DIFFOUT_B63p	U17		
4A	VREFB4AN0	IO			DIFFIO_TX_B64p	DIFFOUT_B64p	U20	DQ6B	DQ1B
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	T19	DQ1R	
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	T18		
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	T20	DQ1R	
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	T17		
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	T22	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	T15	DQ1R	
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	R22	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	R15	DQ1R	
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	R21		
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	R16	DQS1R	
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	P22	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R6n	R17	DQSn1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	P19	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	P16	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	P18		
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	P17	DQ1R	
5B	VREFB5BN0	IO	CLK6p		DIFFIO_RX_R33p	DIFFOUT_R33p	N16		
5B	VREFB5BN0	IO			DIFFIO_TX_R34p	DIFFOUT_R34p	N20	DQ2R	
5B	VREFB5BN0	IO	CLK6n		DIFFIO_RX_R33n	DIFFOUT_R33n	M16		
5B	VREFB5BN0	IO			DIFFIO_TX_R34n	DIFFOUT_R34n	N21	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R35p	DIFFOUT_R35p	N19	DQ2R	
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R36p	DIFFOUT_R36p	M22	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R35n	DIFFOUT_R35n	M18	DQ2R	
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R36n	DIFFOUT_R36n	L22	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R37p	DIFFOUT_R37p	K17	DQS2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R38p	DIFFOUT_R38p	M20		
5B	VREFB5BN0	IO			DIFFIO_RX_R37n	DIFFOUT_R37n	L17	DQSn2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R38n	DIFFOUT_R38n	M21	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R39p	DIFFOUT_R39p	L19	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R40p	DIFFOUT_R40p	K21	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R39n	DIFFOUT_R39n	L18	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R40n	DIFFOUT_R40n	K22		
7A		GND					F17		
7A	VREFB7AN0	IO			DIFFIO_RX_T1p	DIFFOUT_T1p	H21		
7A	VREFB7AN0	IO			DIFFIO_TX_T2p	DIFFOUT_T2p	E21	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	G21		
7A	VREFB7AN0	IO			DIFFIO_TX_T2n	DIFFOUT_T2n	D21	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T3p	E19	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T4p	DIFFOUT_T4p	C20	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T3n	D19	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T4n	DIFFOUT_T4n	B20	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T5p	J21	DQS1T	DQS1T
7A	VREFB7AN0	IO			DIFFIO_TX_T6p	DIFFOUT_T6p	B18		
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T5n	J22	DQSn1T	DQSn1T
7A	VREFB7AN0	IO			DIFFIO_TX_T6n	DIFFOUT_T6n	B17	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T7p	C21	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T8p	DIFFOUT_T8p	G22	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T7n	B21	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T8n	DIFFOUT_T8n	F22		
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T9p	G20		
7A	VREFB7AN0	IO			DIFFIO_TX_T10p	DIFFOUT_T10p	E22	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T9n	H20		



Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16
7A	VREFB7A0	IO			DIFFIO_TX_T10n	DIFFOUT_T10n	D22	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T11p	DIFFOUT_T11p	C19	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T12p	DIFFOUT_T12p	B22	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T11n	DIFFOUT_T11n	C18	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T12n	DIFFOUT_T12n	A22	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T13p	DIFFOUT_T13p	F19	DQS2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T14p	DIFFOUT_T14p	E20		
7A	VREFB7A0	IO			DIFFIO_RX_T13n	DIFFOUT_T13n	F18	DQSn2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T14n	DIFFOUT_T14n	F20	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T15p	DIFFOUT_T15p	A18	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T16p	DIFFOUT_T16p	A20	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	A17	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T16n	DIFFOUT_T16n	A19		
7A	VREFB7A0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	K20		
7A	VREFB7A0	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	B16	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	K19		
7A	VREFB7A0	IO			DIFFIO_TX_T18n	DIFFOUT_T18n	C16	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	D17	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	G17	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	E16	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	G16	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	G18	DQS3T	DQS2T
7A	VREFB7A0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	J19		
7A	VREFB7A0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	H18	DQSn3T	DQSn2T
7A	VREFB7A0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	J18	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	E15	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	A15	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	F15	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T24n	DIFFOUT_T24n	A14		
7A	VREFB7A0	IO	CLK11p		DIFFIO_RX_T25p	DIFFOUT_T25p	H16		
7A	VREFB7A0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	J17	DQ4T	DQ2T
7A	VREFB7A0	IO	CLK11n		DIFFIO_RX_T25n	DIFFOUT_T25n	H15		
7A	VREFB7A0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	K16	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	C15	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	G15	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	B15	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	F14	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	H14	DQS4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	B13		
7A	VREFB7A0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	J13	DQSn4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	A13	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	E14	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	J11	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	F13	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	H10		
7A	VREFB7A0	IO	CLK10p		DIFFIO_RX_T33p	DIFFOUT_T33p	H13		
7A	VREFB7A0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	G11	DQ5T	
7A	VREFB7A0	IO	CLK10n		DIFFIO_RX_T33n	DIFFOUT_T33n	G13		
7A	VREFB7A0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	F12	DQ5T	
7A	VREFB7A0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	D13	DQ5T	
7A	VREFB7A0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	B12	DQ5T	
7A	VREFB7A0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	C13	DQ5T	
7A	VREFB7A0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	A12	DQ5T	
7A	VREFB7A0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	H11	DQS5T	
7A	VREFB7A0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	L8		
7A	VREFB7A0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	G12	DQSn5T	
7A	VREFB7A0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	K9	DQ5T	
7A	VREFB7A0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	D12	DQ5T	
7A	VREFB7A0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	C11	DQ5T	
7A	VREFB7A0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	E12	DQ5T	
7A	VREFB7A0	IO	RZQ_2		DIFFIO_TX_T40n	DIFFOUT_T40n	B11		
8A	VREFB8A0	IO	CLK9p		DIFFIO_RX_T41p	DIFFOUT_T41p	G10		



Pin Information for the Cyclone® V 5CGXBC7 Device
Version 1.2
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16
8A	VREFB8A0	IO			DIFFFIO_TX_T42p	DIFFFOUT_T42p	L7	DQ6T	
8A	VREFB8A0	IO	CLK9n		DIFFFIO_RX_T41n	DIFFFOUT_T41n	F10		
8A	VREFB8A0	IO			DIFFFIO_TX_T42n	DIFFFOUT_T42n	K7	DQ6T	
8A	VREFB8A0	IO			DIFFFIO_RX_T43p	DIFFFOUT_T43p	J7	DQ6T	
8A	VREFB8A0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFFIO_TX_T44p	DIFFFOUT_T44p	H8	DQ6T	
8A	VREFB8A0	IO			DIFFFIO_RX_T43n	DIFFFOUT_T43n	J8	DQ6T	
8A	VREFB8A0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFFIO_TX_T44n	DIFFFOUT_T44n	G8	DQ6T	
8A	VREFB8A0	IO			DIFFFIO_RX_T45p	DIFFFOUT_T45p	J9	DQS6T	
8A	VREFB8A0	IO			DIFFFIO_TX_T46p	DIFFFOUT_T46p	A10		
8A	VREFB8A0	IO			DIFFFIO_RX_T45n	DIFFFOUT_T45n	H9	DQS6T	
8A	VREFB8A0	IO			DIFFFIO_TX_T46n	DIFFFOUT_T46n	A9	DQ6T	
8A	VREFB8A0	IO			DIFFFIO_RX_T47p	DIFFFOUT_T47p	B10	DQ6T	
8A	VREFB8A0	IO			DIFFFIO_TX_T48p	DIFFFOUT_T48p	A5	DQ6T	
8A	VREFB8A0	IO			DIFFFIO_RX_T47n	DIFFFOUT_T47n	C9	DQ6T	
8A	VREFB8A0	IO			DIFFFIO_TX_T48n	DIFFFOUT_T48n	B5		
8A	VREFB8A0	IO	CLK8p,FPLL_TL_FBp		DIFFFIO_RX_T49p	DIFFFOUT_T49p	E10		
8A	VREFB8A0	IO			DIFFFIO_TX_T50p	DIFFFOUT_T50p	B6	DQ7T	
8A	VREFB8A0	IO	CLK8n,FPLL_TL_Fbn		DIFFFIO_RX_T49n	DIFFFOUT_T49n	F9		
8A	VREFB8A0	IO			DIFFFIO_TX_T50n	DIFFFOUT_T50n	B7	DQ7T	
8A	VREFB8A0	IO			DIFFFIO_RX_T51p	DIFFFOUT_T51p	A8	DQ7T	
8A	VREFB8A0	IO			DIFFFIO_TX_T52p	DIFFFOUT_T52p	C6	DQ7T	
8A	VREFB8A0	IO			DIFFFIO_RX_T51n	DIFFFOUT_T51n	A7	DQ7T	
8A	VREFB8A0	IO			DIFFFIO_TX_T52n	DIFFFOUT_T52n	D6	DQ7T	
8A	VREFB8A0	IO			DIFFFIO_RX_T53p	DIFFFOUT_T53p	E9	DQS7T	
8A	VREFB8A0	IO			DIFFFIO_TX_T54p	DIFFFOUT_T54p	D7		
8A	VREFB8A0	IO			DIFFFIO_RX_T53n	DIFFFOUT_T53n	D9	DQS7T	
8A	VREFB8A0	IO			DIFFFIO_TX_T54n	DIFFFOUT_T54n	C8	DQ7T	
8A	VREFB8A0	IO			DIFFFIO_RX_T55p	DIFFFOUT_T55p	G6	DQ7T	
8A	VREFB8A0	IO			DIFFFIO_TX_T56p	DIFFFOUT_T56p	F7	DQ7T	
8A	VREFB8A0	IO			DIFFFIO_RX_T55n	DIFFFOUT_T55n	H6	DQ7T	
8A	VREFB8A0	IO			DIFFFIO_TX_T56n	DIFFFOUT_T56n	E7		
9A		MSEL0		MSEL0			L6		
9A		CONF_DONE		CONF_DONE			K6		
9A		MSEL1		MSEL1			J6		
9A		nSTATUS		nSTATUS			H5		
9A		nCE		nCE			G5		
9A		MSEL2		MSEL2			A2		
9A		MSEL3		MSEL3			E5		
9A		nCONFIG		nCONFIG			A4		
9A		MSEL4		MSEL4			F3		
9A		GND					C5		
		GND					G9		
		GND					AB19		
		GND					AB14		
		GND					AB9		
		GND					AB2		
		GND					AB1		
		GND					AA4		
		GND					AA3		
		GND					Y18		
		GND					AA11		
		GND					AA6		
		GND					Y5		
		GND					Y2		
		GND					Y1		
		GND					W4		
		GND					W3		
		GND					V22		
		GND					V17		
		GND					V12		
		GND					V7		
		GND					V2		



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Version 1.2
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16
		GND					V1		
		GND					U5		
		GND					U3		
		GND					T21		
		GND					T16		
		GND					U9		
		GND					T2		
		GND					T1		
		GND					R13		
		GND					R3		
		GND					P10		
		GND					P4		
		GND					P2		
		GND					P1		
		GND					N22		
		GND					N17		
		GND					N15		
		GND					N13		
		GND					N11		
		GND					N7		
		GND					N5		
		GND					N3		
		GND					M14		
		GND					M12		
		GND					M10		
		GND					M4		
		GND					M2		
		GND					M1		
		GND					L21		
		GND					L15		
		GND					L13		
		GND					L11		
		GND					L5		
		GND					L3		
		GND					K14		
		GND					K12		
		GND					K10		
		GND					K8		
		GND					K4		
		GND					K2		
		GND					K1		
		GND					J20		
		GND					J15		
		GND					J5		
		GND					J3		
		GND					H22		
		GND					H12		
		GND					H7		
		GND					H4		
		GND					H3		
		GND					H2		
		GND					H1		
		GND					G19		
		GND					G3		
		GND					F16		
		GND					F6		
		GND					F2		
		GND					F1		
		GND					E13		
		GND					E4		
		GND					E3		
		GND					D20		



Pin Information for the Cyclone® V 5CGXBC7 Device
Version 1.2
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16
		GND					D10		
		GND					D5		
		GND					D2		
		GND					D1		
		GND					C17		
		GND					C4		
		GND					C3		
		GND					B14		
		GND					B9		
		GND					B2		
		GND					B1		
		GND					A21		
		GND					A11		
		VCC					J10		
		VCC					P15		
		VCC					P13		
		VCC					P11		
		VCC					N14		
		VCC					N12		
		VCC					N10		
		VCC					M15		
		VCC					M13		
		VCC					M11		
		VCC					L16		
		VCC					L14		
		VCC					L12		
		VCC					L10		
		VCC					K15		
		VCC					K13		
		VCC					K11		
		VCC					J16		
		VCC					J14		
		VCC					J12		
		DNU					B3		
		DNU					B4		
		DNU					Y6		
		DNU					V11		
		DNU					E17		
		DNU					L9		
		VCCPGM					V8		
		VCCPGM					R19		
		VCCPGM					F8		
		VCCBAT					A3		
		VCCIO3A					T6		
		VCCIO3A					Y8		
		VCCIO3B					R8		
		VCCIO3B					Y13		
		VCCIO3B					W10		
		VCCIO3B					T11		
		VCCIO4A					U14		
		VCCIO4A					AA21		
		VCCIO4A					AA16		
		VCCIO4A					W20		
		VCCIO4A					W15		
		VCCIO4A					U19		
		VCCIO5A					R18		
		VCCIO5A					P20		
		VCCIO5B					K18		
		VCCIO5B					M19		
		VCCIO7A					A16		
		VCCIO7A					H17		
		VCCIO7A					G14		



Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16
		VCCIO7A					F21		
		VCCIO7A					F11		
		VCCIO7A					E18		
		VCCIO7A					D15		
		VCCIO7A					C22		
		VCCIO7A					C12		
		VCCIO7A					B19		
		VCCIO8A					A6		
		VCCIO8A					G7		
		VCCIO8A					E8		
		VCCIO8A					C7		
		VCCPD3A					W6		
		VCCPD3B4A					W11		
		VCCPD3B4A					W17		
		VCCPD3B4A					W14		
		VCCPD3B4A					W12		
		VCCPD5A					P21		
		VCCPD5B					N18		
		VCCPD5B					M17		
		VCCPD7A8A					D8		
		VCCPD7A8A					E11		
		VCCPD7A8A					D16		
		VCCPD7A8A					D14		
		VCCPD7A8A					C10		
3A	VREFB3AN0	VREFB3AN0					Y7		
3B	VREFB3BN0	VREFB3BN0					Y12		
4A	VREFB4AN0	VREFB4AN0					AB16		
5A	VREFB5AN0	VREFB5AN0					R20		
5B	VREFB5BN0	VREFB5BN0					L20		
7A	VREFB7AN0	VREFB7AN0					C14		
8A	VREFB8AN0	VREFB8AN0					B8		
		VCCH_GXBL					T3		
		VCCH_GXBL					M3		
		VCCL_GXBL					K3		
		VCCL_GXBL					P3		
		RREF_TL					A1		
		VCCA_FPLL					T5		
		VCCA_FPLL					F4		
		VCCA_FPLL					U18		
		VCCA_FPLL					H19		
		VCC_AUX					E6		
		VCC_AUX					D11		
		VCC_AUX					D18		
		VCC_AUX					W18		
		VCC_AUX					W13		
		VCC_AUX					W7		
		VCCE_GXBL					J4		
		VCCE_GXBL					N4		
		VCCE_GXBL					L4		
		VCCE_GXBL					K5		

Note:
(1) For more information about pin definition and pin connection guidelines, refer to the [Cyclone V Device Family Pin Connection Guidelines](#).



Pin Information for the Cyclone® V 5CGXBC7 Device
Version 1.2
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16
GXB_L2		GXB_TX_L8n					C3		
GXB_L2		GXB_TX_L8p					C4		
GXB_L2		GXB_RX_L8p,GXB_REFCLK_L8p					D2		
GXB_L2		GXB_RX_L8n,GXB_REFCLK_L8n					D1		
GXB_L2		GXB_TX_L7n					E3		
GXB_L2		GXB_TX_L7p					E4		
GXB_L2		GXB_RX_L7p,GXB_REFCLK_L7p					F2		
GXB_L2		GXB_RX_L7n,GXB_REFCLK_L7n					F1		
GXB_L2		GXB_TX_L6n					G3		
GXB_L2		GXB_TX_L6p					G4		
GXB_L2		GXB_RX_L6p,GXB_REFCLK_L6p					H2		
GXB_L2		GXB_RX_L6n,GXB_REFCLK_L6n					H1		
GXB_L2		REFCLK2Lp					M6		
GXB_L2		REFCLK2Ln					L5		
GXB_L1		REFCLK1Ln					P6		
GXB_L1		REFCLK1Lp					N7		
GXB_L1		GXB_TX_L5n					K1		
GXB_L1		GXB_TX_L5p					K2		
GXB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					M2		
GXB_L1		GXB_RX_L5n,GXB_REFCLK_L5n					M1		
GXB_L1		GXB_TX_L4n					P1		
GXB_L1		GXB_TX_L4p					P2		
GXB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					T2		
GXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					T1		
GXB_L1		GXB_TX_L3n					W3		
GXB_L1		GXB_TX_L3p					W4		
GXB_L1		GXB_RX_L3p,GXB_REFCLK_L3p					V2		
GXB_L1		GXB_RX_L3n,GXB_REFCLK_L3n					V1		
GXB_L0		GXB_TX_L2n					AA3		
GXB_L0		GXB_TX_L2p					AA4		
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					Y2		
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					Y1		
GXB_L0		GXB_TX_L1n					AC3		
GXB_L0		GXB_TX_L1p					AC4		
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					AB2		
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					AB1		
GXB_L0		GXB_TX_L0n					AE3		
GXB_L0		GXB_TX_L0p					AE4		
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AD2		
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AD1		
GXB_L0		REFCLK0Lp					V6		
GXB_L0		REFCLK0Ln					W6		
3A		TDO		TDO			V7		
3A		nCSO		DATA4			Y6		
3A		TMS		TMS			R6		
3A		AS_DATA3		DATA3			U6		
3A		TCK		TCK			Y5		
3A		AS_DATA2		DATA2			AB5		
3A		TDI		TDI			T6		
3A		AS_DATA1		DATA1			AD5		
3A		DCLK		DCLK			N8		
3A		AS_DATA0,ASDO		DATA0			AF5		
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	T7	DQ1B	
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	U7		
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	T8	DQ1B	
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	V8	DQ1B	
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	W8	DQSn1B	
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	AB6	DQ1B	
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	Y9	DQS1B	
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	AA6		
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	R10	DQ1B	
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	AA7	DQ1B	



Pin Information for the Cyclone® V 5CGXBC7 Device
Version 1.2
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	R9	DQ1B	
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	Y8	DQ1B	
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	R8		
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	AD6	DQ1B	
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	P8		
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AD7	DQ1B	
3B	VREFB3BN0	IO			DIFFIO_TX_B25n	DIFFOUT_B25n	U9		
3B	VREFB3BN0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	Y11	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B25p	DIFFOUT_B25p	T9	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	W11	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	T11	DQSn2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AC10	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	R11	DQS2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AB10		
3B	VREFB3BN0	IO			DIFFIO_TX_B29n	DIFFOUT_B29n	AC8	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	AB11	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B29p	DIFFOUT_B29p	AC9	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	AB12	DQ2B	
3B	VREFB3BN0	IO	CLK0n,FPLL_BLn		DIFFIO_RX_B31n	DIFFOUT_B31n	T12		
3B	VREFB3BN0	IO			DIFFIO_TX_B32n	DIFFOUT_B32n	Y10	DQ2B	
3B	VREFB3BN0	IO	CLK0p,FPLL_BLn		DIFFIO_RX_B31p	DIFFOUT_B31p	T13		
3B	VREFB3BN0	IO			DIFFIO_TX_B32p	DIFFOUT_B32p	W10	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	V9		
3B	VREFB3BN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AE8	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	V10	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AD8	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	P10	DQSn3B	
3B	VREFB3BN0	IO			DIFFIO_TX_B36n	DIFFOUT_B36n	AF9	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	N10	DQS3B	
3B	VREFB3BN0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	AE9		
3B	VREFB3BN0	IO	FPLL_BLn,CLKOUT1,FPLL_BLn,CLKOUTn		DIFFIO_TX_B37n	DIFFOUT_B37n	AF8	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	U11	DQ3B	
3B	VREFB3BN0	IO	FPLL_BLn,CLKOUT0,FPLL_BLn,CLKOUTp,FPLL_BLn,FB		DIFFIO_TX_B37p	DIFFOUT_B37p	AF7	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	U10	DQ3B	
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B39n	DIFFOUT_B39n	P12		
3B	VREFB3BN0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	AF6	DQ3B	
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B39p	DIFFOUT_B39p	P11		
3B	VREFB3BN0	IO			DIFFIO_TX_B40p	DIFFOUT_B40p	AE6	DQ3B	
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B41n	DIFFOUT_B41n	AE11		
4A	VREFB4AN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AA14	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AD11	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	Y14	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	W13	DQSn4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	AD12	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	V13	DQS4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B44p	DIFFOUT_B44p	AD13		
4A	VREFB4AN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	AE10	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	Y13	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	AD10	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	W12	DQ4B	
4A	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B47n	DIFFOUT_B47n	V12		
4A	VREFB4AN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	AF12	DQ4B	
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B47p	DIFFOUT_B47p	U12		
4A	VREFB4AN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	AF11	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B49n	DIFFOUT_B49n	AC13		
4A	VREFB4AN0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	AC15	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AC14	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	AB15	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B51n	DIFFOUT_B51n	V14	DQSn5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B52n	DIFFOUT_B52n	AF13	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B51p	DIFFOUT_B51p	U14	DQS5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B52p	DIFFOUT_B52p	AE13		



Pin Information for the Cyclone® V 5CGXBC7 Device
Version 1.2
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16
4A	VREFB4AN0	IO			DIFFIO_TX_B53n	DIFFOUT_B53n	AF14	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B54n	DIFFOUT_B54n	AB16	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B53p	DIFFOUT_B53p	AE14	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B54p	DIFFOUT_B54p	AA16	DQ5B	DQ1B
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B55n	DIFFOUT_B55n	Y16		
4A	VREFB4AN0	IO			DIFFIO_TX_B56n	DIFFOUT_B56n	AF18	DQ5B	DQ1B
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B55p	DIFFOUT_B55p	Y15		
4A	VREFB4AN0	IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AE18	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B57n	DIFFOUT_B57n	AD18		
4A	VREFB4AN0	IO			DIFFIO_RX_B58n	DIFFOUT_B58n	AD16	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B57p	DIFFOUT_B57p	AC18	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B58p	DIFFOUT_B58p	AD17	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	W15	DQSn6B	DQSn1B
4A	VREFB4AN0	IO			DIFFIO_TX_B60n	DIFFOUT_B60n	AF19	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	V15	DQS6B	DQS1B
4A	VREFB4AN0	IO			DIFFIO_TX_B60p	DIFFOUT_B60p	AE19		
4A	VREFB4AN0	IO			DIFFIO_TX_B61n	DIFFOUT_B61n	AF22	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B62n	DIFFOUT_B62n	AC17	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	AF21	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B62p	AB17	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B63n	DIFFOUT_B63n	U17		
4A	VREFB4AN0	IO			DIFFIO_TX_B64n	DIFFOUT_B64n	AE21	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B63p	DIFFOUT_B63p	T17		
4A	VREFB4AN0	IO			DIFFIO_TX_B64p	DIFFOUT_B64p	AE20	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B65n	DIFFOUT_B65n	AD20		
4A	VREFB4AN0	IO			DIFFIO_RX_B66n	DIFFOUT_B66n	AE15	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_TX_B65p	DIFFOUT_B65p	AC20	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B66p	DIFFOUT_B66p	AE16	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B67n	DIFFOUT_B67n	W17	DQSn7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_TX_B68n	DIFFOUT_B68n	AD21	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B67p	DIFFOUT_B67p	W16	DQS7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_TX_B68p	DIFFOUT_B68p	AD22		
4A	VREFB4AN0	IO			DIFFIO_TX_B69n	DIFFOUT_B69n	AE23	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B70n	DIFFOUT_B70n	AF16	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_TX_B69p	DIFFOUT_B69p	AD23	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B70p	DIFFOUT_B70p	AF17	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B71n	DIFFOUT_B71n	U16		
4A	VREFB4AN0	IO			DIFFIO_TX_B72n	DIFFOUT_B72n	AF23	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B71p	DIFFOUT_B71p	U15		
4A	VREFB4AN0	IO			DIFFIO_TX_B72p	DIFFOUT_B72p	AE24	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_TX_B73n	DIFFOUT_B73n	AF24		
4A	VREFB4AN0	IO			DIFFIO_RX_B74n	DIFFOUT_B74n	AA18	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_TX_B73p	DIFFOUT_B73p	AE25	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B74p	DIFFOUT_B74p	Y18	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B75n	DIFFOUT_B75n	V17	DQSn8B	DQSn2B
4A	VREFB4AN0	IO			DIFFIO_TX_B76n	DIFFOUT_B76n	AE26	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B75p	DIFFOUT_B75p	V18	DQS8B	DQS2B
4A	VREFB4AN0	IO			DIFFIO_TX_B76p	DIFFOUT_B76p	AD26		
4A	VREFB4AN0	IO			DIFFIO_TX_B77n	DIFFOUT_B77n	AC19	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B78n	DIFFOUT_B78n	Y19	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_TX_B77p	DIFFOUT_B77p	AB19	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B78p	DIFFOUT_B78p	Y20	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B79n	DIFFOUT_B79n	W18		
4A	VREFB4AN0	IO			DIFFIO_TX_B80n	DIFFOUT_B80n	AA21	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B79p	DIFFOUT_B79p	V19		
4A	VREFB4AN0	IO			DIFFIO_TX_B80p	DIFFOUT_B80p	AB22	DQ8B	DQ2B
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	AC22	DQ1R	
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	U19		
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	AC23	DQ1R	
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	V20		
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	AA22	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	W20	DQ1R	



Pin Information for the Cyclone® V 5CGXBC7 Device
Version 1.2
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	AA23	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	W21	DQ1R	
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	AC24		
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	V22	DQS1R	
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	AB24	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R6n	U22	DQSn1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	Y23	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	T19	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	Y24		
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	U20	DQ1R	
5B	VREFB5BN0	IO	CLK7p,FPLL_BR_FBp		DIFFIO_RX_R25p	DIFFOUT_R25p	T21		
5B	VREFB5BN0	IO			DIFFIO_TX_R26p	DIFFOUT_R26p	V23	DQ2R	
5B	VREFB5BN0	IO	CLK7n,FPLL_BR_FBn		DIFFIO_RX_R25n	DIFFOUT_R25n	T22		
5B	VREFB5BN0	IO			DIFFIO_TX_R26n	DIFFOUT_R26n	V24	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R27p	DIFFOUT_R27p	T23	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R28p	DIFFOUT_R28p	AA24	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R27n	DIFFOUT_R27n	T24	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R28n	DIFFOUT_R28n	AB25	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R29p	DIFFOUT_R29p	R23	DQS2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R30p	DIFFOUT_R30p	AD25		
5B	VREFB5BN0	IO			DIFFIO_RX_R29n	DIFFOUT_R29n	P23	DQSn2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R30n	DIFFOUT_R30n	AC25	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R31p	DIFFOUT_R31p	R24	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R32p	DIFFOUT_R32p	U24	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R31n	DIFFOUT_R31n	R25	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R32n	DIFFOUT_R32n	V25		
5B	VREFB5BN0	IO	CLK6p		DIFFIO_RX_R33p	DIFFOUT_R33p	R20		
5B	VREFB5BN0	IO			DIFFIO_TX_R34p	DIFFOUT_R34p	AB26	DQ3R	
5B	VREFB5BN0	IO	CLK6n		DIFFIO_RX_R33n	DIFFOUT_R33n	P20		
5B	VREFB5BN0	IO			DIFFIO_TX_R34n	DIFFOUT_R34n	AA26	DQ3R	
5B	VREFB5BN0	IO			DIFFIO_RX_R35p	DIFFOUT_R35p	T26	DQ3R	
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R36p	DIFFOUT_R36p	Y25	DQ3R	
5B	VREFB5BN0	IO			DIFFIO_RX_R35n	DIFFOUT_R35n	R26	DQ3R	
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R36n	DIFFOUT_R36n	Y26	DQ3R	
5B	VREFB5BN0	IO			DIFFIO_RX_R37p	DIFFOUT_R37p	P21	DQS3R	
5B	VREFB5BN0	IO			DIFFIO_TX_R38p	DIFFOUT_R38p	W25		
5B	VREFB5BN0	IO			DIFFIO_RX_R37n	DIFFOUT_R37n	P22	DQSn3R	
5B	VREFB5BN0	IO			DIFFIO_TX_R38n	DIFFOUT_R38n	W26	DQ3R	
5B	VREFB5BN0	IO			DIFFIO_RX_R39p	DIFFOUT_R39p	N25	DQ3R	
5B	VREFB5BN0	IO			DIFFIO_TX_R40p	DIFFOUT_R40p	U25	DQ3R	
5B	VREFB5BN0	IO			DIFFIO_RX_R39n	DIFFOUT_R39n	P26	DQ3R	
5B	VREFB5BN0	IO			DIFFIO_TX_R40n	DIFFOUT_R40n	U26		
6A	VREFB6AN0	IO	CLK5p		DIFFIO_RX_R41p	DIFFOUT_R41p	N20		
6A	VREFB6AN0	IO			DIFFIO_TX_R42p	DIFFOUT_R42p	J25	DQ4R	
6A	VREFB6AN0	IO	CLK5n		DIFFIO_RX_R41n	DIFFOUT_R41n	M21		
6A	VREFB6AN0	IO			DIFFIO_TX_R42n	DIFFOUT_R42n	J26	DQ4R	
6A	VREFB6AN0	IO			DIFFIO_RX_R43p	DIFFOUT_R43p	N24	DQ4R	
6A	VREFB6AN0	IO	FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTp,FPLL_TR_FB		DIFFIO_TX_R44p	DIFFOUT_R44p	F26	DQ4R	
6A	VREFB6AN0	IO			DIFFIO_RX_R43n	DIFFOUT_R43n	M24	DQ4R	
6A	VREFB6AN0	IO	FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTn		DIFFIO_TX_R44n	DIFFOUT_R44n	G26	DQ4R	
6A	VREFB6AN0	IO			DIFFIO_RX_R45p	DIFFOUT_R45p	N23	DQS4R	
6A	VREFB6AN0	IO			DIFFIO_TX_R46p	DIFFOUT_R46p	G25		
6A	VREFB6AN0	IO			DIFFIO_RX_R45n	DIFFOUT_R45n	M22	DQSn4R	
6A	VREFB6AN0	IO			DIFFIO_TX_R46n	DIFFOUT_R46n	H25	DQ4R	
6A	VREFB6AN0	IO			DIFFIO_RX_R47p	DIFFOUT_R47p	M25	DQ4R	
6A	VREFB6AN0	IO			DIFFIO_TX_R48p	DIFFOUT_R48p	D26	DQ4R	
6A	VREFB6AN0	IO			DIFFIO_RX_R47n	DIFFOUT_R47n	M26	DQ4R	
6A	VREFB6AN0	IO			DIFFIO_TX_R48n	DIFFOUT_R48n	E26		
6A	VREFB6AN0	IO	CLK4p,FPLL_TR_FBp		DIFFIO_RX_R49p	DIFFOUT_R49p	K25		
6A	VREFB6AN0	IO			DIFFIO_TX_R50p	DIFFOUT_R50p	E24	DQ5R	
6A	VREFB6AN0	IO	CLK4n,FPLL_TR_FBn		DIFFIO_RX_R49n	DIFFOUT_R49n	K26		
6A	VREFB6AN0	IO			DIFFIO_TX_R50n	DIFFOUT_R50n	E25	DQ5R	



Pin Information for the Cyclone® V 5CGXBC7 Device
Version 1.2
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16
6A	VREFB6A0	IO			DIFFIO_RX_R51p	DIFFOUT_R51p	K24	DQ5R	
6A	VREFB6A0	IO			DIFFIO_TX_R52p	DIFFOUT_R52p	F24	DQ5R	
6A	VREFB6A0	IO			DIFFIO_RX_R51n	DIFFOUT_R51n	K23	DQ5R	
6A	VREFB6A0	IO			DIFFIO_TX_R52n	DIFFOUT_R52n	G24	DQ5R	
6A	VREFB6A0	IO			DIFFIO_RX_R53p	DIFFOUT_R53p	L23	DQS5R	
6A	VREFB6A0	IO			DIFFIO_TX_R54p	DIFFOUT_R54p	H23		
6A	VREFB6A0	IO			DIFFIO_RX_R53n	DIFFOUT_R53n	L24	DQSn5R	
6A	VREFB6A0	IO			DIFFIO_TX_R54n	DIFFOUT_R54n	H24	DQ5R	
6A	VREFB6A0	IO			DIFFIO_RX_R55p	DIFFOUT_R55p	H22	DQ5R	
6A	VREFB6A0	IO			DIFFIO_TX_R56p	DIFFOUT_R56p	F23	DQ5R	
6A	VREFB6A0	IO			DIFFIO_RX_R55n	DIFFOUT_R55n	J23	DQ5R	
6A	VREFB6A0	IO			DIFFIO_TX_R56n	DIFFOUT_R56n	G22		
6A	VREFB6A0	IO			DIFFIO_RX_R65p	DIFFOUT_R65p	L22		
6A	VREFB6A0	IO			DIFFIO_TX_R66p	DIFFOUT_R66p	B25	DQ6R	
6A	VREFB6A0	IO			DIFFIO_RX_R65n	DIFFOUT_R65n	K21		
6A	VREFB6A0	IO			DIFFIO_TX_R66n	DIFFOUT_R66n	B26	DQ6R	
6A	VREFB6A0	IO			DIFFIO_RX_R67p	DIFFOUT_R67p	H19	DQ6R	
6A	VREFB6A0	IO			DIFFIO_TX_R68p	DIFFOUT_R68p	D25	DQ6R	
6A	VREFB6A0	IO			DIFFIO_RX_R67n	DIFFOUT_R67n	H20	DQ6R	
6A	VREFB6A0	IO			DIFFIO_TX_R68n	DIFFOUT_R68n	C25	DQ6R	
6A	VREFB6A0	IO			DIFFIO_RX_R69p	DIFFOUT_R69p	J20	DQS6R	
6A	VREFB6A0	IO			DIFFIO_TX_R70p	DIFFOUT_R70p	D22		
6A	VREFB6A0	IO			DIFFIO_RX_R69n	DIFFOUT_R69n	J21	DQSn6R	
6A	VREFB6A0	IO			DIFFIO_TX_R70n	DIFFOUT_R70n	E23	DQ6R	
6A	VREFB6A0	IO			DIFFIO_RX_R71p	DIFFOUT_R71p	G20	DQ6R	
6A	VREFB6A0	IO			DIFFIO_TX_R72p	DIFFOUT_R72p	E21	DQ6R	
6A	VREFB6A0	IO			DIFFIO_RX_R71n	DIFFOUT_R71n	F21	DQ6R	
6A	VREFB6A0	IO			DIFFIO_TX_R72n	DIFFOUT_R72n	F22		
7A		GND					D23		
7A	VREFB7A0	IO			DIFFIO_RX_T1p	DIFFOUT_T1p	H15		
7A	VREFB7A0	IO			DIFFIO_TX_T2p	DIFFOUT_T2p	C23	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	J16		
7A	VREFB7A0	IO			DIFFIO_TX_T2n	DIFFOUT_T2n	C22	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T3p	DIFFOUT_T3p	B24	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T4p	DIFFOUT_T4p	A23	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T3n	DIFFOUT_T3n	A24	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T4n	DIFFOUT_T4n	A22	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T5p	DIFFOUT_T5p	H18	DQS1T	DQS1T
7A	VREFB7A0	IO			DIFFIO_TX_T6p	DIFFOUT_T6p	B22		
7A	VREFB7A0	IO			DIFFIO_RX_T5n	DIFFOUT_T5n	H17	DQSn1T	DQSn1T
7A	VREFB7A0	IO			DIFFIO_TX_T6n	DIFFOUT_T6n	A21	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T7p	DIFFOUT_T7p	D21	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T8p	DIFFOUT_T8p	B21	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T7n	DIFFOUT_T7n	D20	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T8n	DIFFOUT_T8n	B20		
7A	VREFB7A0	IO			DIFFIO_RX_T9p	DIFFOUT_T9p	G16		
7A	VREFB7A0	IO			DIFFIO_TX_T10p	DIFFOUT_T10p	C20	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T9n	DIFFOUT_T9n	G17		
7A	VREFB7A0	IO			DIFFIO_TX_T10n	DIFFOUT_T10n	B19	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T11p	DIFFOUT_T11p	E20	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T12p	DIFFOUT_T12p	C19	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T11n	DIFFOUT_T11n	E19	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T12n	DIFFOUT_T12n	C18	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T13p	DIFFOUT_T13p	J12	DQS2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T14p	DIFFOUT_T14p	A19		
7A	VREFB7A0	IO			DIFFIO_RX_T13n	DIFFOUT_T13n	J11	DQSn2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T14n	DIFFOUT_T14n	A18	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T15p	DIFFOUT_T15p	D18	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T16p	DIFFOUT_T16p	A17	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	D17	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T16n	DIFFOUT_T16n	A16		
7A	VREFB7A0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	H14		



Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16
7A	VREFB7A0	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	C17	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	H13		
7A	VREFB7A0	IO			DIFFIO_TX_T18n	DIFFOUT_T18n	B17	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	E18	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	A14	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	F18	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	B14	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	L12	DQS3T	DQS2T
7A	VREFB7A0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	B15		
7A	VREFB7A0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	K11	DQSn3T	DQSn2T
7A	VREFB7A0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	C15	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	C14	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	A8	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	D15	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T24n	DIFFOUT_T24n	A9		
7A	VREFB7A0	IO	CLK11p		DIFFIO_RX_T25p	DIFFOUT_T25p	G15		
7A	VREFB7A0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	C9	DQ4T	DQ2T
7A	VREFB7A0	IO	CLK11n		DIFFIO_RX_T25n	DIFFOUT_T25n	G14		
7A	VREFB7A0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	B9	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	E16	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	D10	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	D16	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	C10	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	N12	DQS4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	B10		
7A	VREFB7A0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	M12	DQSn4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	A11	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	F16	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	E10	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	E15	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	E11		
7A	VREFB7A0	IO	CLK10p		DIFFIO_RX_T33p	DIFFOUT_T33p	H12		
7A	VREFB7A0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	B12	DQ5T	
7A	VREFB7A0	IO	CLK10n		DIFFIO_RX_T33n	DIFFOUT_T33n	G11		
7A	VREFB7A0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	A13	DQ5T	
7A	VREFB7A0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	G12	DQ5T	
7A	VREFB7A0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	A12	DQ5T	
7A	VREFB7A0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	F12	DQ5T	
7A	VREFB7A0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	B11	DQ5T	
7A	VREFB7A0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	M11	DQS5T	
7A	VREFB7A0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	C13		
7A	VREFB7A0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	L11	DQSn5T	
7A	VREFB7A0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	C12	DQ5T	
7A	VREFB7A0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	E13	DQ5T	
7A	VREFB7A0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	D11	DQ5T	
7A	VREFB7A0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	D13	DQ5T	
7A	VREFB7A0	IO	RZQ_2		DIFFIO_TX_T40n	DIFFOUT_T40n	D12		
8A	VREFB8A0	IO	CLK9p		DIFFIO_RX_T41p	DIFFOUT_T41p	N9		
8A	VREFB8A0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	A5	DQ6T	
8A	VREFB8A0	IO	CLK9n		DIFFIO_RX_T41n	DIFFOUT_T41n	M10		
8A	VREFB8A0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	B6	DQ6T	
8A	VREFB8A0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	H8	DQ6T	
8A	VREFB8A0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T44p	DIFFOUT_T44p	A7	DQ6T	
8A	VREFB8A0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	H9	DQ6T	
8A	VREFB8A0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T44n	DIFFOUT_T44n	B7	DQ6T	
8A	VREFB8A0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	M9	DQS6T	
8A	VREFB8A0	IO			DIFFIO_TX_T46p	DIFFOUT_T46p	D6		
8A	VREFB8A0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	L9	DQSn6T	
8A	VREFB8A0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	E6	DQ6T	
8A	VREFB8A0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	H10	DQ6T	
8A	VREFB8A0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	D7	DQ6T	
8A	VREFB8A0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	G10	DQ6T	



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Version 1.2
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16
8A	VREFB8AN0	IO			DIFFFIO_TX_T48n	DIFFFOUT_T48n	C7		
8A	VREFB8AN0	IO	CLK8p,FPLL_TL_FBp		DIFFFIO_RX_T49p	DIFFFOUT_T49p	L8		
8A	VREFB8AN0	IO			DIFFFIO_TX_T50p	DIFFFOUT_T50p	F6	DQ7T	
8A	VREFB8AN0	IO	CLK8n,FPLL_TL_FBn		DIFFFIO_RX_T49n	DIFFFOUT_T49n	K9		
8A	VREFB8AN0	IO			DIFFFIO_TX_T50n	DIFFFOUT_T50n	G6	DQ7T	
8A	VREFB8AN0	IO			DIFFFIO_RX_T51p	DIFFFOUT_T51p	K8	DQ7T	
8A	VREFB8AN0	IO			DIFFFIO_TX_T52p	DIFFFOUT_T52p	G7	DQ7T	
8A	VREFB8AN0	IO			DIFFFIO_RX_T51n	DIFFFOUT_T51n	J8	DQ7T	
8A	VREFB8AN0	IO			DIFFFIO_TX_T52n	DIFFFOUT_T52n	F7	DQ7T	
8A	VREFB8AN0	IO			DIFFFIO_RX_T53p	DIFFFOUT_T53p	K10	DQS7T	
8A	VREFB8AN0	IO			DIFFFIO_TX_T54p	DIFFFOUT_T54p	H7		
8A	VREFB8AN0	IO			DIFFFIO_RX_T53n	DIFFFOUT_T53n	J10	DQS7T	
8A	VREFB8AN0	IO			DIFFFIO_TX_T54n	DIFFFOUT_T54n	J7	DQ7T	
8A	VREFB8AN0	IO			DIFFFIO_RX_T55p	DIFFFOUT_T55p	L7	DQ7T	
8A	VREFB8AN0	IO			DIFFFIO_TX_T56p	DIFFFOUT_T56p	D8	DQ7T	
8A	VREFB8AN0	IO			DIFFFIO_RX_T55n	DIFFFOUT_T55n	K6	DQ7T	
8A	VREFB8AN0	IO			DIFFFIO_TX_T56n	DIFFFOUT_T56n	E9		
9A		MSEL0		MSEL0			M7		
9A		CONF_DONE		CONF_DONE			A6		
9A		MSEL1		MSEL1			L6		
9A		nSTATUS		nSTATUS			B5		
9A		nCE		nCE			D5		
9A		MSEL2		MSEL2			A2		
9A		MSEL3		MSEL3			K5		
9A		nCONFIG		nCONFIG			F5		
9A		MSEL4		MSEL4			J5		
9A		GND					H5		
		GND					B4		
		GND					A25		
		GND					D24		
		GND					H26		
		GND					L25		
		GND					P24		
		GND					V26		
		GND					AA25		
		GND					AC26		
		GND					AF25		
		GND					G23		
		GND					K22		
		GND					U23		
		GND					Y22		
		GND					AD24		
		GND					C21		
		GND					F20		
		GND					L20		
		GND					K19		
		GND					N21		
		GND					M19		
		GND					T20		
		GND					P19		
		GND					W19		
		GND					AC21		
		GND					AF20		
		GND					B18		
		GND					E17		
		GND					L18		
		GND					K17		
		GND					J18		
		GND					N18		
		GND					M17		
		GND					R18		
		GND					P17		



Pin Information for the Cyclone® V 5CGXBC7 Device
Version 1.2
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16
		GND					AB18		
		GND					AE17		
		GND					A15		
		GND					D14		
		GND					H16		
		GND					L16		
		GND					L14		
		GND					K15		
		GND					J14		
		GND					N16		
		GND					N14		
		GND					M15		
		GND					T15		
		GND					R16		
		GND					R14		
		GND					P15		
		GND					V16		
		GND					AA15		
		GND					AD14		
		GND					G13		
		GND					K13		
		GND					K12		
		GND					M13		
		GND					R12		
		GND					P13		
		GND					U13		
		GND					Y12		
		GND					C11		
		GND					F10		
		GND					L10		
		GND					J9		
		GND					N11		
		GND					T10		
		GND					P9		
		GND					W9		
		GND					AC11		
		GND					AF10		
		GND					B8		
		GND					E7		
		GND					H6		
		GND					N6		
		GND					M8		
		GND					R7		
		GND					P7		
		GND					AB8		
		GND					AE7		
		GND					C5		
		GND					F4		
		GND					E5		
		GND					D4		
		GND					H4		
		GND					G5		
		GND					L4		
		GND					J4		
		GND					N4		
		GND					M5		
		GND					T5		
		GND					R4		
		GND					P5		
		GND					V5		
		GND					V4		
		GND					U4		



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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16
		GND					AA5		
		GND					Y4		
		GND					W5		
		GND					AC5		
		GND					AB4		
		GND					AF4		
		GND					AE5		
		GND					AD4		
		GND					C2		
		GND					C1		
		GND					B3		
		GND					B2		
		GND					F3		
		GND					E2		
		GND					E1		
		GND					D3		
		GND					H3		
		GND					G2		
		GND					G1		
		GND					L2		
		GND					L1		
		GND					K3		
		GND					J2		
		GND					J1		
		GND					N2		
		GND					N1		
		GND					M3		
		GND					T3		
		GND					R2		
		GND					R1		
		GND					P3		
		GND					V3		
		GND					U2		
		GND					U1		
		GND					AA2		
		GND					AA1		
		GND					Y3		
		GND					W2		
		GND					W1		
		GND					AC2		
		GND					AC1		
		GND					AB3		
		GND					AF3		
		GND					AF2		
		GND					AE2		
		GND					AE1		
		GND					AD3		
		VCC					J19		
		VCC					L19		
		VCC					K20		
		VCC					N19		
		VCC					M20		
		VCC					R19		
		VCC					L17		
		VCC					K18		
		VCC					J17		
		VCC					N17		
		VCC					M18		
		VCC					T18		
		VCC					R17		
		VCC					P18		
		VCC					L15		



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Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16
		VCC					K16		
		VCC					K14		
		VCC					J15		
		VCC					N15		
		VCC					M16		
		VCC					M14		
		VCC					T16		
		VCC					T14		
		VCC					R15		
		VCC					P16		
		VCC					P14		
		VCC					L13		
		VCC					J13		
		VCC					N13		
		VCC					R13		
		DNU					A4		
		DNU					A3		
		DNU					AB7		
		DNU					AA12		
		DNU					C24		
		DNU					F14		
		VCCPGM					AA9		
		VCCPGM					W22		
		VCCPGM					F8		
		VCCBAT					E8		
		VCCIO3A					Y7		
		VCCIO3A					AC6		
		VCCIO3B					V11		
		VCCIO3B					AA10		
		VCCIO3B					AD9		
		VCCIO3B					U8		
		VCCIO4A					U18		
		VCCIO4A					AE22		
		VCCIO4A					AA20		
		VCCIO4A					AD19		
		VCCIO4A					Y17		
		VCCIO4A					W14		
		VCCIO4A					AC16		
		VCCIO4A					AF15		
		VCCIO4A					AB13		
		VCCIO4A					AE12		
		VCCIO5A					V21		
		VCCIO5A					AB23		
		VCCIO5B					N26		
		VCCIO5B					T25		
		VCCIO5B					W24		
		VCCIO5B					R22		
		VCCIO6A					C26		
		VCCIO6A					F25		
		VCCIO6A					J24		
		VCCIO6A					E22		
		VCCIO6A					M23		
		VCCIO6A					H21		
		VCCIO7A					G18		
		VCCIO7A					B23		
		VCCIO7A					A20		
		VCCIO7A					D19		
		VCCIO7A					C16		
		VCCIO7A					F15		
		VCCIO7A					B13		
		VCCIO7A					E12		
		VCCIO7A					A10		



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Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16
		VCCIO7A					H11		
		VCCIO8A					C6		
		VCCIO8A					D9		
		VCCIO8A					G8		
		VCCIO8A					K7		
		VCCPD3A					AB9		
		VCCPD3B4A					AB21		
		VCCPD3B4A					AA19		
		VCCPD3B4A					AA17		
		VCCPD3B4A					AA13		
		VCCPD3B4A					AA11		
		VCCPD5A					U21		
		VCCPD5B					R21		
		VCCPD5B					N22		
		VCCPD6A					J22		
		VCCPD6A					L21		
		VCCPD7A8A					F11		
		VCCPD7A8A					F19		
		VCCPD7A8A					F17		
		VCCPD7A8A					F13		
		VCCPD7A8A					F9		
3A	VREFB3AN0	VREFB3AN0					AC7		
3B	VREFB3BN0	VREFB3BN0					AC12		
4A	VREFB4AN0	VREFB4AN0					AD15		
5A	VREFB5AN0	VREFB5AN0					W23		
5B	VREFB5BN0	VREFB5BN0					P25		
6A	VREFB6AN0	VREFB6AN0					L26		
7A	VREFB7AN0	VREFB7AN0					B16		
8A	VREFB8AN0	VREFB8AN0					C8		
		VCCH_GXBL					T4		
		VCCH_GXBL					L3		
		VCCH_GXBL					R3		
		VCCL_GXBL					N3		
		VCCL_GXBL					J3		
		VCCL_GXBL					U3		
		RREF_TL					B1		
		VCCA_FPLL					W7		
		VCCA_FPLL					J6		
		VCCA_FPLL					Y21		
		VCCA_FPLL					G21		
		VCC_AUX					G9		
		VCC_AUX					E14		
		VCC_AUX					G19		
		VCC_AUX					AB20		
		VCC_AUX					AB14		
		VCC_AUX					AA8		
		VCCE_GXBL					M4		
		VCCE_GXBL					K4		
		VCCE_GXBL					N5		
		VCCE_GXBL					R5		
		VCCE_GXBL					P4		
		VCCE_GXBL					U5		

Note:
(1) For more information about pin definition and pin connection guidelines, refer to the [Cyclone V Device Family Pin Connection Guidelines](#).



Pin Information for the Cyclone® V 5CGXBC7 Device
Version 1.2
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16
GXB_L2		GXB_TX_L8n					K3		
GXB_L2		GXB_TX_L8p					K4		
GXB_L2		GXB_RX_L8p,GXB_REFCLK_L8p					L2		
GXB_L2		GXB_RX_L8n,GXB_REFCLK_L8n					L1		
GXB_L2		GXB_TX_L7n					M3		
GXB_L2		GXB_TX_L7p					M4		
GXB_L2		GXB_RX_L7p,GXB_REFCLK_L7p					N2		
GXB_L2		GXB_RX_L7n,GXB_REFCLK_L7n					N1		
GXB_L2		GXB_TX_L6n					P3		
GXB_L2		GXB_TX_L6p					P4		
GXB_L2		GXB_RX_L6p,GXB_REFCLK_L6p					R2		
GXB_L2		GXB_RX_L6n,GXB_REFCLK_L6n					R1		
GXB_L2		REFCLK2Lp					P8		
GXB_L2		REFCLK2Ln					N7		
GXB_L1		REFCLK1Ln					R7		
GXB_L1		REFCLK1Lp					R8		
GXB_L1		GXB_TX_L5n					T3		
GXB_L1		GXB_TX_L5p					T4		
GXB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					U2		
GXB_L1		GXB_RX_L5n,GXB_REFCLK_L5n					U1		
GXB_L1		GXB_TX_L4n					V3		
GXB_L1		GXB_TX_L4p					V4		
GXB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					W2		
GXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					W1		
GXB_L1		GXB_TX_L3n					Y3		
GXB_L1		GXB_TX_L3p					Y4		
GXB_L1		GXB_RX_L3p,GXB_REFCLK_L3p					AA2		
GXB_L1		GXB_RX_L3n,GXB_REFCLK_L3n					AA1		
GXB_L0		GXB_TX_L2n					AB3		
GXB_L0		GXB_TX_L2p					AB4		
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					AC2		
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					AC1		
GXB_L0		GXB_TX_L1n					AD3		
GXB_L0		GXB_TX_L1p					AD4		
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					AE2		
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					AE1		
GXB_L0		GXB_TX_L0n					AF3		
GXB_L0		GXB_TX_L0p					AF4		
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AG2		
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AG1		
GXB_L0		REFCLK0Lp					W8		
GXB_L0		REFCLK0Ln					W7		
3A		TDO		TDO			W9		
3A		nCSO		DATA4			AA7		
3A		TMS		TMS			V7		
3A		AS_DATA3		DATA3			AB7		
3A		TCK		TCK			AC7		
3A		AS_DATA2		DATA2			AE7		
3A		TDI		TDI			U7		
3A		AS_DATA1		DATA1			AE5		
3A		DCLK		DCLK			T7		
3A		AS_DATA0,ASDO		DATA0			AG5		
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	U12	DQ1B	
3A	VREFB3AN0	IO		DATA5	DIFFIO_RX_B2n	DIFFOUT_B2n	AA10		
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	U11	DQ1B	
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	Y10	DQ1B	
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	Y11	DQSn1B	
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	AD9	DQ1B	
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	AA11	DQS1B	
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	AC9		
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	R10	DQ1B	
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	W10	DQ1B	
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	T11	DQ1B	
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	V9	DQ1B	
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	V10		



Pin Information for the Cyclone® V 5CGXBC7 Device
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Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16
3A	VREFB3A0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	AF6	DQ1B	
3A	VREFB3A0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	V11		
3A	VREFB3A0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AF7	DQ1B	
3A	VREFB3A0	IO			DIFFIO_TX_B9n	DIFFOUT_B9n	AB9		
3A	VREFB3A0	IO			DIFFIO_RX_B10n	DIFFOUT_B10n	AH6	DQ2B	
3A	VREFB3A0	IO			DIFFIO_TX_B9p	DIFFOUT_B9p	AA9	DQ2B	
3A	VREFB3A0	IO			DIFFIO_RX_B10p	DIFFOUT_B10p	AG6	DQ2B	
3A	VREFB3A0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	U8	DQSn2B	
3A	VREFB3A0	IO			DIFFIO_TX_B12n	DIFFOUT_B12n	AG8	DQ2B	
3A	VREFB3A0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	T9	DQS2B	
3A	VREFB3A0	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AF8		
3A	VREFB3A0	IO			DIFFIO_TX_B13n	DIFFOUT_B13n	AB8	DQ2B	
3A	VREFB3A0	IO			DIFFIO_RX_B14n	DIFFOUT_B14n	AH5	DQ2B	
3A	VREFB3A0	IO			DIFFIO_TX_B13p	DIFFOUT_B13p	AA8	DQ2B	
3A	VREFB3A0	IO			DIFFIO_RX_B14p	DIFFOUT_B14p	AH4	DQ2B	
3A	VREFB3A0	IO			DIFFIO_RX_B15n	DIFFOUT_B15n	U9		
3A	VREFB3A0	IO			DIFFIO_TX_B16n	DIFFOUT_B16n	AH7	DQ2B	
3A	VREFB3A0	IO			DIFFIO_RX_B15p	DIFFOUT_B15p	T10		
3A	VREFB3A0	IO			DIFFIO_TX_B16p	DIFFOUT_B16p	AG7	DQ2B	
3B	VREFB3B0	IO			DIFFIO_TX_B17n	DIFFOUT_B17n	AF10		
3B	VREFB3B0	IO			DIFFIO_RX_B18n	DIFFOUT_B18n	AD13	DQ3B	DQ1B
3B	VREFB3B0	IO			DIFFIO_TX_B17p	DIFFOUT_B17p	AE10	DQ3B	DQ1B
3B	VREFB3B0	IO			DIFFIO_RX_B18p	DIFFOUT_B18p	AD12	DQ3B	DQ1B
3B	VREFB3B0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	W12	DQSn3B	DQ1B
3B	VREFB3B0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	AJ2	DQ3B	DQ1B
3B	VREFB3B0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	V12	DQS3B	DQ1B
3B	VREFB3B0	IO			DIFFIO_TX_B20p	DIFFOUT_B20p	AJ1		
3B	VREFB3B0	IO			DIFFIO_TX_B21n	DIFFOUT_B21n	AK3	DQ3B	DQ1B
3B	VREFB3B0	IO			DIFFIO_RX_B22n	DIFFOUT_B22n	AE13	DQ3B	DQ1B
3B	VREFB3B0	IO			DIFFIO_TX_B21p	DIFFOUT_B21p	AJ3	DQ3B	DQ1B
3B	VREFB3B0	IO			DIFFIO_RX_B22p	DIFFOUT_B22p	AE12	DQ3B	DQ1B
3B	VREFB3B0	IO			DIFFIO_RX_B23n	DIFFOUT_B23n	AB13		
3B	VREFB3B0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	AJ5	DQ3B	DQ1B
3B	VREFB3B0	IO			DIFFIO_RX_B23p	DIFFOUT_B23p	AB12		
3B	VREFB3B0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	AJ4	DQ3B	DQ1B
3B	VREFB3B0	IO			DIFFIO_TX_B25n	DIFFOUT_B25n	AK6		
3B	VREFB3B0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	AG12	DQ4B	DQ1B
3B	VREFB3B0	IO			DIFFIO_TX_B25p	DIFFOUT_B25p	AK5	DQ4B	DQ1B
3B	VREFB3B0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	AF13	DQ4B	DQ1B
3B	VREFB3B0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	AA13	DQSn4B	DQSn1B
3B	VREFB3B0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AK7	DQ4B	DQ1B
3B	VREFB3B0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	Y12	DQS4B	DQS1B
3B	VREFB3B0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AJ7		
3B	VREFB3B0	IO			DIFFIO_TX_B29n	DIFFOUT_B29n	AK8	DQ4B	DQ1B
3B	VREFB3B0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	AG11	DQ4B	DQ1B
3B	VREFB3B0	IO			DIFFIO_TX_B29p	DIFFOUT_B29p	AJ8	DQ4B	DQ1B
3B	VREFB3B0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	AF11	DQ4B	DQ1B
3B	VREFB3B0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B31n	DIFFOUT_B31n	AC14		
3B	VREFB3B0	IO			DIFFIO_TX_B32n	DIFFOUT_B32n	AG9	DQ4B	DQ1B
3B	VREFB3B0	IO	CLK0p,FPLL_BL_FBP		DIFFIO_RX_B31p	DIFFOUT_B31p	AB14		
3B	VREFB3B0	IO			DIFFIO_TX_B32p	DIFFOUT_B32p	AF9	DQ4B	DQ1B
3B	VREFB3B0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AJ9		
3B	VREFB3B0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AJ10	DQ5B	
3B	VREFB3B0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AH9	DQ5B	
3B	VREFB3B0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AH10	DQ5B	
3B	VREFB3B0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	AA14	DQSn5B	
3B	VREFB3B0	IO			DIFFIO_TX_B36n	DIFFOUT_B36n	AK11	DQ5B	
3B	VREFB3B0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	Y13	DQS5B	
3B	VREFB3B0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	AK10		
3B	VREFB3B0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B37n	DIFFOUT_B37n	AH12	DQ5B	
3B	VREFB3B0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AG14	DQ5B	
3B	VREFB3B0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B37p	DIFFOUT_B37p	AH11	DQ5B	
3B	VREFB3B0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AG13	DQ5B	
3B	VREFB3B0	IO	CLK1n		DIFFIO_RX_B39n	DIFFOUT_B39n	AA15		
3B	VREFB3B0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	AK12	DQ5B	



Pin Information for the Cyclone® V 5CGXBC7 Device
Version 1.2
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B39p	DIFFOUT_B39p	Y15		
3B	VREFB3BN0	IO			DIFFIO_TX_B40p	DIFFOUT_B40p	AJ12	DQ5B	
4A	VREFB4AN0	IO	RZO_0		DIFFIO_TX_B41n	DIFFOUT_B41n	AK13		
4A	VREFB4AN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AF15	DQ6B	
4A	VREFB4AN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AJ14	DQ6B	
4A	VREFB4AN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	AE16	DQ6B	
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	AA16	DQSn6B	
4A	VREFB4AN0	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	AH15	DQ6B	
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	Y16	DQS6B	
4A	VREFB4AN0	IO			DIFFIO_TX_B44p	DIFFOUT_B44p	AH14		
4A	VREFB4AN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	AK15	DQ6B	
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AE17	DQ6B	
4A	VREFB4AN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	AJ15	DQ6B	
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	AD17	DQ6B	
4A	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B47n	DIFFOUT_B47n	AC15		
4A	VREFB4AN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	AF14	DQ6B	
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B47p	DIFFOUT_B47p	AB16		
4A	VREFB4AN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	AE15	DQ6B	
4A	VREFB4AN0	IO			DIFFIO_TX_B49n	DIFFOUT_B49n	AH17		
4A	VREFB4AN0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	AK17	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AG17	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	AK16	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B51n	DIFFOUT_B51n	Y18	DQSn7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_TX_B52n	DIFFOUT_B52n	AJ18	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B51p	DIFFOUT_B51p	Y17	DQS7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_TX_B52p	DIFFOUT_B52p	AJ17		
4A	VREFB4AN0	IO			DIFFIO_TX_B53n	DIFFOUT_B53n	AK18	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B54n	DIFFOUT_B54n	AG16	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_TX_B53p	DIFFOUT_B53p	AJ19	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B54p	DIFFOUT_B54p	AF16	DQ7B	DQ2B
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B55n	DIFFOUT_B55n	AB18		
4A	VREFB4AN0	IO			DIFFIO_TX_B56n	DIFFOUT_B56n	AH20	DQ7B	DQ2B
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B55p	DIFFOUT_B55p	AB17		
4A	VREFB4AN0	IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AH19	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_TX_B57n	DIFFOUT_B57n	AK20		
4A	VREFB4AN0	IO			DIFFIO_RX_B58n	DIFFOUT_B58n	AE18	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_TX_B57p	DIFFOUT_B57p	AJ20	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B58p	DIFFOUT_B58p	AD18	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	AA20	DQSn8B	DQSn2B
4A	VREFB4AN0	IO			DIFFIO_TX_B60n	DIFFOUT_B60n	AK22	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	Y20	DQS8B	DQS2B
4A	VREFB4AN0	IO			DIFFIO_TX_B60p	DIFFOUT_B60p	AK21		
4A	VREFB4AN0	IO			DIFFIO_TX_B61n	DIFFOUT_B61n	AJ22	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B62n	DIFFOUT_B62n	AF19	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	AH21	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B62p	AF18	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B63n	DIFFOUT_B63n	AA19		
4A	VREFB4AN0	IO			DIFFIO_TX_B64n	DIFFOUT_B64n	AK23	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B63p	DIFFOUT_B63p	AA18		
4A	VREFB4AN0	IO			DIFFIO_TX_B64p	DIFFOUT_B64p	AJ23	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_TX_B65n	DIFFOUT_B65n	AJ24		
4A	VREFB4AN0	IO			DIFFIO_RX_B66n	DIFFOUT_B66n	AG19	DQ9B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B65p	DIFFOUT_B65p	AH24	DQ9B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B66p	DIFFOUT_B66p	AG18	DQ9B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B67n	DIFFOUT_B67n	AC19	DQSn9B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B68n	DIFFOUT_B68n	AK25	DQ9B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B67p	DIFFOUT_B67p	AB19	DQS9B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B68p	DIFFOUT_B68p	AJ25		
4A	VREFB4AN0	IO			DIFFIO_TX_B69n	DIFFOUT_B69n	AH25	DQ9B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B70n	DIFFOUT_B70n	AE20	DQ9B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B69p	DIFFOUT_B69p	AG24	DQ9B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B70p	DIFFOUT_B70p	AD19	DQ9B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B71n	DIFFOUT_B71n	AB21		
4A	VREFB4AN0	IO			DIFFIO_TX_B72n	DIFFOUT_B72n	AK26	DQ9B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B71p	DIFFOUT_B71p	AA21		



Pin Information for the Cyclone® V 5CGXBC7 Device
Version 1.2
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16
4A	VREFB4AN0	IO			DIFFIO_TX_B72p	DIFFOUT_B72p	AJ27	DQ9B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B73n	DIFFOUT_B73n	AK28		
4A	VREFB4AN0	IO			DIFFIO_RX_B74n	DIFFOUT_B74n	AG21	DQ10B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B73p	DIFFOUT_B73p	AK27	DQ10B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B74p	DIFFOUT_B74p	AF20	DQ10B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B75n	DIFFOUT_B75n	AD20	DQSn10B	DQSn3B
4A	VREFB4AN0	IO			DIFFIO_TX_B76n	DIFFOUT_B76n	AH26	DQ10B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B75p	DIFFOUT_B75p	AC21	DQS10B	DQS3B
4A	VREFB4AN0	IO			DIFFIO_TX_B76p	DIFFOUT_B76p	AG26		
4A	VREFB4AN0	IO			DIFFIO_TX_B77n	DIFFOUT_B77n	AF23	DQ10B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B78n	DIFFOUT_B78n	AG22	DQ10B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B77p	DIFFOUT_B77p	AE22	DQ10B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B78p	DIFFOUT_B78p	AF21	DQ10B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B79n	DIFFOUT_B79n	AC22		
4A	VREFB4AN0	IO			DIFFIO_TX_B80n	DIFFOUT_B80n	AH22	DQ10B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B79p	DIFFOUT_B79p	AB22		
4A	VREFB4AN0	IO			DIFFIO_TX_B80p	DIFFOUT_B80p	AG23	DQ10B	DQ3B
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	AD23	DQ1R	
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	W22		
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	AC24	DQ1R	
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	Y21		
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	AD24	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	Y25	DQ1R	
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	AD25	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	Y26	DQ1R	
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	AB26		
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	Y23	DQS1R	
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	AA26	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R6n	W24	DQSn1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	AC26	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	Y22	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	AC27		
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	AA23	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R9p	DIFFOUT_R9p	AA24		
5A	VREFB5AN0	IO			DIFFIO_TX_R10p	DIFFOUT_R10p	AE23	DQ2R	
5A	VREFB5AN0	IO			DIFFIO_RX_R9n	DIFFOUT_R9n	AA25		
5A	VREFB5AN0	IO			DIFFIO_TX_R10n	DIFFOUT_R10n	AF24	DQ2R	
5A	VREFB5AN0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	AE27	DQ2R	
5A	VREFB5AN0	IO			DIFFIO_TX_R12p	DIFFOUT_R12p	AE25	DQ2R	
5A	VREFB5AN0	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	AD27	DQ2R	
5A	VREFB5AN0	IO			DIFFIO_TX_R12n	DIFFOUT_R12n	AE26	DQ2R	
5A	VREFB5AN0	IO			DIFFIO_RX_R13p	DIFFOUT_R13p	V21	DQS2R	
5A	VREFB5AN0	IO			DIFFIO_TX_R14p	DIFFOUT_R14p	AF25		
5A	VREFB5AN0	IO			DIFFIO_RX_R13n	DIFFOUT_R13n	V22	DQSn2R	
5A	VREFB5AN0	IO			DIFFIO_TX_R14n	DIFFOUT_R14n	AF26	DQ2R	
5A	VREFB5AN0	IO			DIFFIO_RX_R15p	DIFFOUT_R15p	Y27	DQ2R	
5A	VREFB5AN0	IO			DIFFIO_TX_R16p	DIFFOUT_R16p	AH27	DQ2R	
5A	VREFB5AN0	IO			DIFFIO_RX_R15n	DIFFOUT_R15n	W27	DQ2R	
5A	VREFB5AN0	IO			DIFFIO_TX_R16n	DIFFOUT_R16n	AG27		
5B	VREFB5BN0	IO			DIFFIO_RX_R17p	DIFFOUT_R17p	V24		
5B	VREFB5BN0	IO			DIFFIO_TX_R18p	DIFFOUT_R18p	AJ28	DQ3R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_RX_R17n	DIFFOUT_R17n	V25		
5B	VREFB5BN0	IO			DIFFIO_TX_R18n	DIFFOUT_R18n	AJ29	DQ3R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_RX_R19p	DIFFOUT_R19p	AA28	DQ3R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_TX_R20p	DIFFOUT_R20p	AH29	DQ3R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_RX_R19n	DIFFOUT_R19n	Y28	DQ3R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_TX_R20n	DIFFOUT_R20n	AG29	DQ3R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_RX_R21p	DIFFOUT_R21p	V26	DQS3R	DQS1R
5B	VREFB5BN0	IO			DIFFIO_TX_R22p	DIFFOUT_R22p	AJ30		
5B	VREFB5BN0	IO			DIFFIO_RX_R21n	DIFFOUT_R21n	U26	DQSn3R	DQSn1R
5B	VREFB5BN0	IO			DIFFIO_TX_R22n	DIFFOUT_R22n	AH30	DQ3R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_RX_R23p	DIFFOUT_R23p	AE30	DQ3R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_TX_R24p	DIFFOUT_R24p	AG28	DQ3R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	AD30	DQ3R	DQ1R
5B	VREFB5BN0	IO			DIFFIO_TX_R24n	DIFFOUT_R24n	AF28		



Pin Information for the Cyclone® V 5CGXBC7 Device
Version 1.2
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16
5B	VREFB5B0	IO	CLK7p,FPLL_BR_FBp		DIFFIO_RX_R25p	DIFFOUT_R25p	U21		
5B	VREFB5B0	IO			DIFFIO_TX_R26p	DIFFOUT_R26p	AF29	DQ4R	DQ1R
5B	VREFB5B0	IO	CLK7n,FPLL_BR_FBn		DIFFIO_RX_R25n	DIFFOUT_R25n	U22		
5B	VREFB5B0	IO			DIFFIO_TX_R26n	DIFFOUT_R26n	AF30	DQ4R	DQ1R
5B	VREFB5B0	IO			DIFFIO_RX_R27p	DIFFOUT_R27p	V27	DQ4R	DQ1R
5B	VREFB5B0	IO			DIFFIO_TX_R28p	DIFFOUT_R28p	AE28	DQ4R	DQ1R
5B	VREFB5B0	IO			DIFFIO_RX_R27n	DIFFOUT_R27n	W28	DQ4R	DQ1R
5B	VREFB5B0	IO			DIFFIO_TX_R28n	DIFFOUT_R28n	AD28	DQ4R	DQ1R
5B	VREFB5B0	IO			DIFFIO_RX_R29p	DIFFOUT_R29p	U27	DQS4R	DQ1R
5B	VREFB5B0	IO			DIFFIO_TX_R30p	DIFFOUT_R30p	AD29		
5B	VREFB5B0	IO			DIFFIO_RX_R29n	DIFFOUT_R29n	U28	DQSn4R	DQ1R
5B	VREFB5B0	IO			DIFFIO_TX_R30n	DIFFOUT_R30n	AC29	DQ4R	DQ1R
5B	VREFB5B0	IO			DIFFIO_RX_R31p	DIFFOUT_R31p	AA29	DQ4R	DQ1R
5B	VREFB5B0	IO			DIFFIO_TX_R32p	DIFFOUT_R32p	AB27	DQ4R	DQ1R
5B	VREFB5B0	IO			DIFFIO_RX_R31n	DIFFOUT_R31n	AA30	DQ4R	DQ1R
5B	VREFB5B0	IO			DIFFIO_TX_R32n	DIFFOUT_R32n	AB28		
5B	VREFB5B0	IO	CLK6p		DIFFIO_RX_R33p	DIFFOUT_R33p	U23		
5B	VREFB5B0	IO			DIFFIO_TX_R34p	DIFFOUT_R34p	AB29	DQ5R	
5B	VREFB5B0	IO	CLK6n		DIFFIO_RX_R33n	DIFFOUT_R33n	T24		
5B	VREFB5B0	IO			DIFFIO_TX_R34n	DIFFOUT_R34n	AC30	DQ5R	
5B	VREFB5B0	IO			DIFFIO_RX_R35p	DIFFOUT_R35p	T28	DQ5R	
5B	VREFB5B0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R36p	DIFFOUT_R36p	Y30	DQ5R	
5B	VREFB5B0	IO			DIFFIO_RX_R35n	DIFFOUT_R35n	T29	DQ5R	
5B	VREFB5B0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R36n	DIFFOUT_R36n	W30	DQ5R	
5B	VREFB5B0	IO			DIFFIO_RX_R37p	DIFFOUT_R37p	T25	DQS5R	
5B	VREFB5B0	IO			DIFFIO_TX_R38p	DIFFOUT_R38p	V29		
5B	VREFB5B0	IO			DIFFIO_RX_R37n	DIFFOUT_R37n	R26	DQSn5R	
5B	VREFB5B0	IO			DIFFIO_TX_R38n	DIFFOUT_R38n	W29	DQ5R	
5B	VREFB5B0	IO			DIFFIO_RX_R39p	DIFFOUT_R39p	T30	DQ5R	
5B	VREFB5B0	IO			DIFFIO_TX_R40p	DIFFOUT_R40p	U29	DQ5R	
5B	VREFB5B0	IO			DIFFIO_RX_R39n	DIFFOUT_R39n	R30	DQ5R	
5B	VREFB5B0	IO			DIFFIO_TX_R40n	DIFFOUT_R40n	V30		
6A	VREFB6A0	IO	CLK5p		DIFFIO_RX_R41p	DIFFOUT_R41p	T23		
6A	VREFB6A0	IO			DIFFIO_TX_R42p	DIFFOUT_R42p	P28	DQ6R	
6A	VREFB6A0	IO	CLK5n		DIFFIO_RX_R41n	DIFFOUT_R41n	R23		
6A	VREFB6A0	IO			DIFFIO_TX_R42n	DIFFOUT_R42n	N29	DQ6R	
6A	VREFB6A0	IO			DIFFIO_RX_R43p	DIFFOUT_R43p	P29	DQ6R	
6A	VREFB6A0	IO	FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTp,FPLL_TR_FB		DIFFIO_TX_R44p	DIFFOUT_R44p	M29	DQ6R	
6A	VREFB6A0	IO			DIFFIO_RX_R43n	DIFFOUT_R43n	P30	DQ6R	
6A	VREFB6A0	IO	FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTn		DIFFIO_TX_R44n	DIFFOUT_R44n	N30	DQ6R	
6A	VREFB6A0	IO			DIFFIO_RX_R45p	DIFFOUT_R45p	P25	DQS6R	
6A	VREFB6A0	IO			DIFFIO_TX_R46p	DIFFOUT_R46p	L28		
6A	VREFB6A0	IO			DIFFIO_RX_R45n	DIFFOUT_R45n	R25	DQSn6R	
6A	VREFB6A0	IO			DIFFIO_TX_R46n	DIFFOUT_R46n	K28	DQ6R	
6A	VREFB6A0	IO			DIFFIO_RX_R47p	DIFFOUT_R47p	R27	DQ6R	
6A	VREFB6A0	IO			DIFFIO_TX_R48p	DIFFOUT_R48p	M27	DQ6R	
6A	VREFB6A0	IO			DIFFIO_RX_R47n	DIFFOUT_R47n	R28	DQ6R	
6A	VREFB6A0	IO			DIFFIO_TX_R48n	DIFFOUT_R48n	M28		
6A	VREFB6A0	IO	CLK4p,FPLL_TR_FBp		DIFFIO_RX_R49p	DIFFOUT_R49p	P22		
6A	VREFB6A0	IO			DIFFIO_TX_R50p	DIFFOUT_R50p	K25	DQ7R	DQ2R
6A	VREFB6A0	IO	CLK4n,FPLL_TR_FBn		DIFFIO_RX_R49n	DIFFOUT_R49n	P23		
6A	VREFB6A0	IO			DIFFIO_TX_R50n	DIFFOUT_R50n	K26	DQ7R	DQ2R
6A	VREFB6A0	IO			DIFFIO_RX_R51p	DIFFOUT_R51p	N26	DQ7R	DQ2R
6A	VREFB6A0	IO			DIFFIO_TX_R52p	DIFFOUT_R52p	L29	DQ7R	DQ2R
6A	VREFB6A0	IO			DIFFIO_RX_R51n	DIFFOUT_R51n	N27	DQ7R	DQ2R
6A	VREFB6A0	IO			DIFFIO_TX_R52n	DIFFOUT_R52n	L30	DQ7R	DQ2R
6A	VREFB6A0	IO			DIFFIO_RX_R53p	DIFFOUT_R53p	N24	DQS7R	DQS2R
6A	VREFB6A0	IO			DIFFIO_TX_R54p	DIFFOUT_R54p	K30		
6A	VREFB6A0	IO			DIFFIO_RX_R53n	DIFFOUT_R53n	N25	DQSn7R	DQSn2R
6A	VREFB6A0	IO			DIFFIO_TX_R54n	DIFFOUT_R54n	J30	DQ7R	DQ2R
6A	VREFB6A0	IO			DIFFIO_RX_R55p	DIFFOUT_R55p	L25	DQ7R	DQ2R
6A	VREFB6A0	IO			DIFFIO_TX_R56p	DIFFOUT_R56p	G27	DQ7R	DQ2R
6A	VREFB6A0	IO			DIFFIO_RX_R55n	DIFFOUT_R55n	L26	DQ7R	DQ2R
6A	VREFB6A0	IO			DIFFIO_TX_R56n	DIFFOUT_R56n	G28		
6A	VREFB6A0	IO			DIFFIO_RX_R57p	DIFFOUT_R57p	R21		



Pin Information for the Cyclone® V 5CGXBC7 Device
Version 1.2
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16
6A	VREFB6A0	IO			DIFFIO_TX_R58p	DIFFOUT_R58p	J28	DQ8R	DQ2R
6A	VREFB6A0	IO			DIFFIO_RX_R57n	DIFFOUT_R57n	R22		
6A	VREFB6A0	IO			DIFFIO_TX_R58n	DIFFOUT_R58n	J29	DQ8R	DQ2R
6A	VREFB6A0	IO			DIFFIO_RX_R59p	DIFFOUT_R59p	K27	DQ8R	DQ2R
6A	VREFB6A0	IO			DIFFIO_TX_R60p	DIFFOUT_R60p	H29	DQ8R	DQ2R
6A	VREFB6A0	IO			DIFFIO_RX_R59n	DIFFOUT_R59n	J27	DQ8R	DQ2R
6A	VREFB6A0	IO			DIFFIO_TX_R60n	DIFFOUT_R60n	H30	DQ8R	DQ2R
6A	VREFB6A0	IO			DIFFIO_RX_R61p	DIFFOUT_R61p	N22	DQS8R	DQ2R
6A	VREFB6A0	IO			DIFFIO_TX_R62p	DIFFOUT_R62p	H27		
6A	VREFB6A0	IO			DIFFIO_RX_R61n	DIFFOUT_R61n	M23	DQSn8R	DQ2R
6A	VREFB6A0	IO			DIFFIO_TX_R62n	DIFFOUT_R62n	G26	DQ8R	DQ2R
6A	VREFB6A0	IO			DIFFIO_RX_R63p	DIFFOUT_R63p	F25	DQ8R	DQ2R
6A	VREFB6A0	IO			DIFFIO_TX_R64p	DIFFOUT_R64p	F30	DQ8R	DQ2R
6A	VREFB6A0	IO			DIFFIO_RX_R63n	DIFFOUT_R63n	F26	DQ8R	DQ2R
6A	VREFB6A0	IO			DIFFIO_TX_R64n	DIFFOUT_R64n	E30		
6A	VREFB6A0	IO			DIFFIO_RX_R65p	DIFFOUT_R65p	R20		
6A	VREFB6A0	IO			DIFFIO_TX_R66p	DIFFOUT_R66p	G29	DQ9R	DQ3R
6A	VREFB6A0	IO			DIFFIO_RX_R65n	DIFFOUT_R65n	T21		
6A	VREFB6A0	IO			DIFFIO_TX_R66n	DIFFOUT_R66n	F29	DQ9R	DQ3R
6A	VREFB6A0	IO			DIFFIO_RX_R67p	DIFFOUT_R67p	L23	DQ9R	DQ3R
6A	VREFB6A0	IO			DIFFIO_TX_R68p	DIFFOUT_R68p	D30	DQ9R	DQ3R
6A	VREFB6A0	IO			DIFFIO_RX_R67n	DIFFOUT_R67n	L24	DQ9R	DQ3R
6A	VREFB6A0	IO			DIFFIO_TX_R68n	DIFFOUT_R68n	C30	DQ9R	DQ3R
6A	VREFB6A0	IO			DIFFIO_RX_R69p	DIFFOUT_R69p	N21	DQS9R	DQS3R
6A	VREFB6A0	IO			DIFFIO_TX_R70p	DIFFOUT_R70p	F28		
6A	VREFB6A0	IO			DIFFIO_RX_R69n	DIFFOUT_R69n	M22	DQSn9R	DQSn3R
6A	VREFB6A0	IO			DIFFIO_TX_R70n	DIFFOUT_R70n	E28	DQ9R	DQ3R
6A	VREFB6A0	IO			DIFFIO_RX_R71p	DIFFOUT_R71p	K21	DQ9R	DQ3R
6A	VREFB6A0	IO			DIFFIO_TX_R72p	DIFFOUT_R72p	C29	DQ9R	DQ3R
6A	VREFB6A0	IO			DIFFIO_RX_R71n	DIFFOUT_R71n	K22	DQ9R	DQ3R
6A	VREFB6A0	IO			DIFFIO_TX_R72n	DIFFOUT_R72n	B29		
6A	VREFB6A0	IO			DIFFIO_RX_R73p	DIFFOUT_R73p	M21		
6A	VREFB6A0	IO			DIFFIO_TX_R74p	DIFFOUT_R74p	B28	DQ10R	DQ3R
6A	VREFB6A0	IO			DIFFIO_RX_R73n	DIFFOUT_R73n	L21		
6A	VREFB6A0	IO			DIFFIO_TX_R74n	DIFFOUT_R74n	A29	DQ10R	DQ3R
6A	VREFB6A0	IO			DIFFIO_RX_R75p	DIFFOUT_R75p	H25	DQ10R	DQ3R
6A	VREFB6A0	IO			DIFFIO_TX_R76p	DIFFOUT_R76p	D28	DQ10R	DQ3R
6A	VREFB6A0	IO			DIFFIO_RX_R75n	DIFFOUT_R75n	H26	DQ10R	DQ3R
6A	VREFB6A0	IO			DIFFIO_TX_R76n	DIFFOUT_R76n	D29	DQ10R	DQ3R
6A	VREFB6A0	IO			DIFFIO_RX_R77p	DIFFOUT_R77p	P20	DQS10R	DQ3R
6A	VREFB6A0	IO			DIFFIO_TX_R78p	DIFFOUT_R78p	E27		
6A	VREFB6A0	IO			DIFFIO_RX_R77n	DIFFOUT_R77n	N20	DQSn10R	DQ3R
6A	VREFB6A0	IO			DIFFIO_TX_R78n	DIFFOUT_R78n	D27	DQ10R	DQ3R
6A	VREFB6A0	IO			DIFFIO_RX_R79p	DIFFOUT_R79p	J22	DQ10R	DQ3R
6A	VREFB6A0	IO			DIFFIO_TX_R80p	DIFFOUT_R80p	H24	DQ10R	DQ3R
6A	VREFB6A0	IO			DIFFIO_RX_R79n	DIFFOUT_R79n	J23	DQ10R	DQ3R
6A	VREFB6A0	IO			DIFFIO_TX_R80n	DIFFOUT_R80n	J25		
7A		GND					G24		
7A	VREFB7A0	IO			DIFFIO_RX_T1p	DIFFOUT_T1p	H21		
7A	VREFB7A0	IO			DIFFIO_TX_T2p	DIFFOUT_T2p	E26	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	G21		
7A	VREFB7A0	IO			DIFFIO_TX_T2n	DIFFOUT_T2n	E25	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T3p	DIFFOUT_T3p	G22	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T4p	DIFFOUT_T4p	C27	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T3n	DIFFOUT_T3n	G23	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T4n	DIFFOUT_T4n	C26	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T5p	DIFFOUT_T5p	L20	DQS1T	DQS1T
7A	VREFB7A0	IO			DIFFIO_TX_T6p	DIFFOUT_T6p	B27		
7A	VREFB7A0	IO			DIFFIO_RX_T5n	DIFFOUT_T5n	L19	DQSn1T	DQSn1T
7A	VREFB7A0	IO			DIFFIO_TX_T6n	DIFFOUT_T6n	A28	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T7p	DIFFOUT_T7p	E22	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T8p	DIFFOUT_T8p	B26	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T7n	DIFFOUT_T7n	E21	DQ1T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T8n	DIFFOUT_T8n	A26		
7A	VREFB7A0	IO			DIFFIO_RX_T9p	DIFFOUT_T9p	J20		



Pin Information for the Cyclone® V 5CGXBC7 Device
Version 1.2
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16
7A	VREFB7A0	IO			DIFFIO_TX_T10p	DIFFOUT_T10p	D25	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T9n	DIFFOUT_T9n	H20		
7A	VREFB7A0	IO			DIFFIO_TX_T10n	DIFFOUT_T10n	C25	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T11p	DIFFOUT_T11p	C21	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T12p	DIFFOUT_T12p	D23	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T11n	DIFFOUT_T11n	C20	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T12n	DIFFOUT_T12n	C22	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T13p	DIFFOUT_T13p	K20	DQS2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T14p	DIFFOUT_T14p	E23		
7A	VREFB7A0	IO			DIFFIO_RX_T13n	DIFFOUT_T13n	J19	DQSn2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T14n	DIFFOUT_T14n	D22	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T15p	DIFFOUT_T15p	D20	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T16p	DIFFOUT_T16p	A25	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	C19	DQ2T	DQ1T
7A	VREFB7A0	IO			DIFFIO_TX_T16n	DIFFOUT_T16n	A24		
7A	VREFB7A0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	F20		
7A	VREFB7A0	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	C24	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	E20		
7A	VREFB7A0	IO			DIFFIO_TX_T18n	DIFFOUT_T18n	B24	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	F19	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	B23	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	E18	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	A23	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	L18	DQS3T	DQS2T
7A	VREFB7A0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	B22		
7A	VREFB7A0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	K18	DQSn3T	DQSn2T
7A	VREFB7A0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	B21	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	D19	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	A21	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	D18	DQ3T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T24n	DIFFOUT_T24n	A20		
7A	VREFB7A0	IO	CLK11p		DIFFIO_RX_T25p	DIFFOUT_T25p	H19		
7A	VREFB7A0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	B19	DQ4T	DQ2T
7A	VREFB7A0	IO	CLK11n		DIFFIO_RX_T25n	DIFFOUT_T25n	J18		
7A	VREFB7A0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	A19	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	G18	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	B18	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	F18	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	A18	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	K16	DQS4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	D14		
7A	VREFB7A0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	L16	DQSn4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	C14	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	C17	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	A16	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	B17	DQ4T	DQ2T
7A	VREFB7A0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	A15		
7A	VREFB7A0	IO	CLK10p		DIFFIO_RX_T33p	DIFFOUT_T33p	H17		
7A	VREFB7A0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	B14	DQ5T	
7A	VREFB7A0	IO	CLK10n		DIFFIO_RX_T33n	DIFFOUT_T33n	G17		
7A	VREFB7A0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	A14	DQ5T	
7A	VREFB7A0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	E17	DQ5T	
7A	VREFB7A0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	D12	DQ5T	
7A	VREFB7A0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	D17	DQ5T	
7A	VREFB7A0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	C12	DQ5T	
7A	VREFB7A0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	K17	DQS5T	
7A	VREFB7A0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	B13		
7A	VREFB7A0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	J17	DQSn5T	
7A	VREFB7A0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	A13	DQ5T	
7A	VREFB7A0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	C16	DQ5T	
7A	VREFB7A0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	C11	DQ5T	
7A	VREFB7A0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	C15	DQ5T	
7A	VREFB7A0	IO	RZQ_2		DIFFIO_TX_T40n	DIFFOUT_T40n	B12		
8A	VREFB8A0	IO	CLK9p		DIFFIO_RX_T41p	DIFFOUT_T41p	L15		
8A	VREFB8A0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	B11	DQ6T	



Pin Information for the Cyclone® V 5CGXBC7 Device
Version 1.2
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16
8A	VREFB8A0	IO	CLK9n		DIFFIO_RX_T41n	DIFFOUT_T41n	K15		
8A	VREFB8A0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	A11	DQ6T	
8A	VREFB8A0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	F16	DQ6T	
8A	VREFB8A0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T44p	DIFFOUT_T44p	F9	DQ6T	
8A	VREFB8A0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	E16	DQ6T	
8A	VREFB8A0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T44n	DIFFOUT_T44n	E10	DQ6T	
8A	VREFB8A0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	M9	DQS6T	
8A	VREFB8A0	IO			DIFFIO_TX_T46p	DIFFOUT_T46p	D9		
8A	VREFB8A0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	M8	DQS6T	
8A	VREFB8A0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	C10	DQ6T	
8A	VREFB8A0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	F15	DQ6T	
8A	VREFB8A0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	A10	DQ6T	
8A	VREFB8A0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	E15	DQ6T	
8A	VREFB8A0	IO			DIFFIO_TX_T48n	DIFFOUT_T48n	A9		
8A	VREFB8A0	IO	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T49p	DIFFOUT_T49p	L14		
8A	VREFB8A0	IO			DIFFIO_TX_T50p	DIFFOUT_T50p	C9	DQ7T	
8A	VREFB8A0	IO	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T49n	DIFFOUT_T49n	L13		
8A	VREFB8A0	IO			DIFFIO_TX_T50n	DIFFOUT_T50n	B8	DQ7T	
8A	VREFB8A0	IO			DIFFIO_RX_T51p	DIFFOUT_T51p	E12	DQ7T	
8A	VREFB8A0	IO			DIFFIO_TX_T52p	DIFFOUT_T52p	B7	DQ7T	
8A	VREFB8A0	IO			DIFFIO_RX_T51n	DIFFOUT_T51n	D13	DQ7T	
8A	VREFB8A0	IO			DIFFIO_TX_T52n	DIFFOUT_T52n	A8	DQ7T	
8A	VREFB8A0	IO			DIFFIO_RX_T53p	DIFFOUT_T53p	J15	DQS7T	
8A	VREFB8A0	IO			DIFFIO_TX_T54p	DIFFOUT_T54p	B6		
8A	VREFB8A0	IO			DIFFIO_RX_T53n	DIFFOUT_T53n	H15	DQS7T	
8A	VREFB8A0	IO			DIFFIO_TX_T54n	DIFFOUT_T54n	A6	DQ7T	
8A	VREFB8A0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	E11	DQ7T	
8A	VREFB8A0	IO			DIFFIO_TX_T56p	DIFFOUT_T56p	C7	DQ7T	
8A	VREFB8A0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	D10	DQ7T	
8A	VREFB8A0	IO			DIFFIO_TX_T56n	DIFFOUT_T56n	C6		
8A	VREFB8A0	IO			DIFFIO_RX_T57p	DIFFOUT_T57p	L10		
8A	VREFB8A0	IO			DIFFIO_TX_T58p	DIFFOUT_T58p	F13	DQ8T	
8A	VREFB8A0	IO			DIFFIO_RX_T57n	DIFFOUT_T57n	L9		
8A	VREFB8A0	IO			DIFFIO_TX_T58n	DIFFOUT_T58n	E13	DQ8T	
8A	VREFB8A0	IO			DIFFIO_RX_T59p	DIFFOUT_T59p	G14	DQ8T	
8A	VREFB8A0	IO			DIFFIO_TX_T60p	DIFFOUT_T60p	A5	DQ8T	
8A	VREFB8A0	IO			DIFFIO_RX_T59n	DIFFOUT_T59n	F14	DQ8T	
8A	VREFB8A0	IO			DIFFIO_TX_T60n	DIFFOUT_T60n	A4	DQ8T	
8A	VREFB8A0	IO			DIFFIO_RX_T61p	DIFFOUT_T61p	J14	DQS8T	
8A	VREFB8A0	IO			DIFFIO_TX_T62p	DIFFOUT_T62p	J7		
8A	VREFB8A0	IO			DIFFIO_RX_T61n	DIFFOUT_T61n	H14	DQS8T	
8A	VREFB8A0	IO			DIFFIO_TX_T62n	DIFFOUT_T62n	H7	DQ8T	
8A	VREFB8A0	IO			DIFFIO_RX_T63p	DIFFOUT_T63p	L11	DQ8T	
8A	VREFB8A0	IO			DIFFIO_TX_T64p	DIFFOUT_T64p	J9	DQ8T	
8A	VREFB8A0	IO			DIFFIO_RX_T63n	DIFFOUT_T63n	K11	DQ8T	
8A	VREFB8A0	IO			DIFFIO_TX_T64n	DIFFOUT_T64n	H9		
8A	VREFB8A0	IO			DIFFIO_RX_T65p	DIFFOUT_T65p	P12		
8A	VREFB8A0	IO			DIFFIO_TX_T66p	DIFFOUT_T66p	G9	DQ9T	DQ3T
8A	VREFB8A0	IO			DIFFIO_RX_T65n	DIFFOUT_T65n	N12		
8A	VREFB8A0	IO			DIFFIO_TX_T66n	DIFFOUT_T66n	F8	DQ9T	DQ3T
8A	VREFB8A0	IO			DIFFIO_RX_T67p	DIFFOUT_T67p	H12	DQ9T	DQ3T
8A	VREFB8A0	IO			DIFFIO_TX_T68p	DIFFOUT_T68p	E8	DQ9T	DQ3T
8A	VREFB8A0	IO			DIFFIO_RX_T67n	DIFFOUT_T67n	G12	DQ9T	DQ3T
8A	VREFB8A0	IO			DIFFIO_TX_T68n	DIFFOUT_T68n	D8	DQ9T	DQ3T
8A	VREFB8A0	IO			DIFFIO_RX_T69p	DIFFOUT_T69p	K13	DQS9T	DQS3T
8A	VREFB8A0	IO			DIFFIO_TX_T70p	DIFFOUT_T70p	A3		
8A	VREFB8A0	IO			DIFFIO_RX_T69n	DIFFOUT_T69n	J13	DQS9T	DQS3T
8A	VREFB8A0	IO			DIFFIO_TX_T70n	DIFFOUT_T70n	A2	DQ9T	DQ3T
8A	VREFB8A0	IO			DIFFIO_RX_T71p	DIFFOUT_T71p	P10	DQ9T	DQ3T
8A	VREFB8A0	IO			DIFFIO_TX_T72p	DIFFOUT_T72p	D7	DQ9T	DQ3T
8A	VREFB8A0	IO			DIFFIO_RX_T71n	DIFFOUT_T71n	N11	DQ9T	DQ3T
8A	VREFB8A0	IO			DIFFIO_TX_T72n	DIFFOUT_T72n	D6		
8A	VREFB8A0	IO			DIFFIO_RX_T73p	DIFFOUT_T73p	R12		
8A	VREFB8A0	IO			DIFFIO_TX_T74p	DIFFOUT_T74p	E7	DQ10T	DQ3T
8A	VREFB8A0	IO			DIFFIO_RX_T73n	DIFFOUT_T73n	R11		



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Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16
8A	VREFB8AN0	IO			DIFFIO_TX_T74n	DIFFOUT_T74n	E6	DQ10T	DQ3T
8A	VREFB8AN0	IO			DIFFIO_RX_T75p	DIFFOUT_T75p	K12	DQ10T	DQ3T
8A	VREFB8AN0	IO			DIFFIO_TX_T76p	DIFFOUT_T76p	K10	DQ10T	DQ3T
8A	VREFB8AN0	IO			DIFFIO_RX_T75n	DIFFOUT_T75n	J12	DQ10T	DQ3T
8A	VREFB8AN0	IO			DIFFIO_TX_T76n	DIFFOUT_T76n	J10	DQ10T	DQ3T
8A	VREFB8AN0	IO			DIFFIO_RX_T77p	DIFFOUT_T77p	N10	DQS10T	DQ3T
8A	VREFB8AN0	IO			DIFFIO_TX_T78p	DIFFOUT_T78p	G6		
8A	VREFB8AN0	IO			DIFFIO_RX_T77n	DIFFOUT_T77n	N9	DQSn10T	DQ3T
8A	VREFB8AN0	IO			DIFFIO_TX_T78n	DIFFOUT_T78n	F6	DQ10T	DQ3T
8A	VREFB8AN0	IO			DIFFIO_RX_T79p	DIFFOUT_T79p	M12	DQ10T	DQ3T
8A	VREFB8AN0	IO			DIFFIO_TX_T80p	DIFFOUT_T80p	G8	DQ10T	DQ3T
8A	VREFB8AN0	IO			DIFFIO_RX_T79n	DIFFOUT_T79n	M11	DQ10T	DQ3T
8A	VREFB8AN0	IO			DIFFIO_TX_T80n	DIFFOUT_T80n	G7		
9A		MSEL0		MSEL0			T8		
9A		CONF_DONE		CONF_DONE			L8		
9A		MSEL1		MSEL1			P9		
9A		nSTATUS		nSTATUS			K7		
9A		nCE		nCE			H6		
9A		MSEL2		MSEL2			G5		
9A		MSEL3		MSEL3			P7		
9A		nCONFIG		nCONFIG			C5		
9A		MSEL4		MSEL4			M7		
9A		GND					E5		
		GND					J11		
		GND					E9		
		GND					AD7		
		GND					K14		
		GND					G15		
		GND					H18		
		GND					D16		
		GND					F22		
		GND					J21		
		GND					L27		
		GND					E29		
		GND					D26		
		GND					N23		
		GND					P26		
		GND					T22		
		GND					U25		
		GND					AE29		
		GND					AH28		
		GND					V23		
		GND					Y24		
		GND					AD26		
		GND					AC23		
		GND					AB20		
		GND					AJ6		
		GND					AC13		
		GND					M10		
		GND					AK24		
		GND					AJ21		
		GND					AH2		
		GND					AH8		
		GND					AG3		
		GND					AG4		
		GND					AG15		
		GND					AG25		
		GND					AF1		
		GND					AF12		
		GND					AF22		
		GND					AE19		
		GND					AD1		
		GND					AD2		
		GND					AD5		
		GND					AD16		



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Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16
		GND					AC3		
		GND					AC4		
		GND					AC6		
		GND					AB2		
		GND					AB5		
		GND					AB10		
		GND					AA3		
		GND					AA4		
		GND					AA6		
		GND					AA27		
		GND					Y1		
		GND					Y7		
		GND					W11		
		GND					W13		
		GND					W17		
		GND					W19		
		GND					V1		
		GND					V2		
		GND					V5		
		GND					V8		
		GND					V16		
		GND					V18		
		GND					V20		
		GND					V28		
		GND					U3		
		GND					U4		
		GND					U6		
		GND					U13		
		GND					U15		
		GND					T2		
		GND					T5		
		GND					T14		
		GND					T16		
		GND					T20		
		GND					R3		
		GND					R4		
		GND					R6		
		GND					R9		
		GND					R13		
		GND					R17		
		GND					R19		
		GND					R29		
		GND					P1		
		GND					P16		
		GND					P18		
		GND					N8		
		GND					N13		
		GND					N17		
		GND					N19		
		GND					M1		
		GND					M2		
		GND					M5		
		GND					M14		
		GND					M16		
		GND					M20		
		GND					M30		
		GND					L3		
		GND					L4		
		GND					L6		
		GND					K2		
		GND					K5		
		GND					J3		
		GND					J4		
		GND					J6		
		GND					H1		



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Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16
		GND					G25		
		GND					F1		
		GND					F2		
		GND					F5		
		GND					E3		
		GND					E4		
		GND					E19		
		GND					D2		
		GND					D5		
		GND					C2		
		GND					C4		
		GND					C13		
		GND					C23		
		GND					B1		
		GND					B10		
		GND					B30		
		GND					A12		
		GND					A17		
		GND					AK2		
		GND					AK14		
		GND					AK29		
		GND					AJ11		
		GND					AH1		
		GND					AH3		
		GND					AH18		
		GND					AF2		
		GND					AF5		
		GND					AE3		
		GND					AE4		
		GND					AE6		
		GND					AE9		
		GND					AB1		
		GND					AB30		
		GND					AA17		
		GND					Y2		
		GND					Y5		
		GND					Y14		
		GND					W3		
		GND					W4		
		GND					W6		
		GND					W15		
		GND					W21		
		GND					V14		
		GND					U17		
		GND					U19		
		GND					T1		
		GND					T12		
		GND					T18		
		GND					R15		
		GND					P2		
		GND					P5		
		GND					P11		
		GND					P14		
		GND					N3		
		GND					N4		
		GND					N6		
		GND					N15		
		GND					M18		
		GND					L17		
		GND					K1		
		GND					K9		
		GND					K24		
		GND					H2		
		GND					H5		
		GND					H8		



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Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16
		GND					H11		
		GND					H28		
		GND					G3		
		GND					G4		
		GND					F12		
		GND					D1		
		GND					C3		
		GND					B2		
		GND					B20		
		GND					A27		
		VCC					N18		
		VCC					W14		
		VCC					W16		
		VCC					W20		
		VCC					V13		
		VCC					V15		
		VCC					V19		
		VCC					U16		
		VCC					U18		
		VCC					T17		
		VCC					T19		
		VCC					R14		
		VCC					R16		
		VCC					R18		
		VCC					P13		
		VCC					P15		
		VCC					N14		
		VCC					N16		
		VCC					M13		
		VCC					M17		
		VCC					M19		
		VCC					W18		
		VCC					V17		
		VCC					U14		
		VCC					U20		
		VCC					T13		
		VCC					T15		
		VCC					P17		
		VCC					P19		
		VCC					M15		
		DNU					B4		
		DNU					B3		
		DNU					AD8		
		DNU					AD14		
		DNU					F24		
		DNU					D15		
		VCCPGM					AC11		
		VCCPGM					AB24		
		VCCPGM					F10		
		VCCBAT					H10		
		VCCIO3A					AD11		
		VCCIO3A					Y9		
		VCCIO3A					U10		
		VCCIO3A					AC8		
		VCCIO3B					AE14		
		VCCIO3B					AK9		
		VCCIO3B					AK4		
		VCCIO3B					AH13		
		VCCIO3B					AG10		
		VCCIO3B					AA12		
		VCCIO4A					AC18		
		VCCIO4A					AK19		
		VCCIO4A					AJ16		
		VCCIO4A					AH23		
		VCCIO4A					AD21		



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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16
		VCCIO4A					Y19		
		VCCIO4A					AJ26		
		VCCIO4A					AG20		
		VCCIO4A					AF17		
		VCCIO4A					AB15		
		VCCIO5A					AA22		
		VCCIO5A					AF27		
		VCCIO5A					AB25		
		VCCIO5A					AE24		
		VCCIO5B					T27		
		VCCIO5B					AG30		
		VCCIO5B					W26		
		VCCIO5B					U30		
		VCCIO5B					AC28		
		VCCIO5B					Y29		
		VCCIO6A					C28		
		VCCIO6A					R24		
		VCCIO6A					P21		
		VCCIO6A					N28		
		VCCIO6A					M25		
		VCCIO6A					K29		
		VCCIO6A					J26		
		VCCIO6A					F27		
		VCCIO6A					L22		
		VCCIO6A					G30		
		VCCIO7A					A22		
		VCCIO7A					K19		
		VCCIO7A					G20		
		VCCIO7A					F17		
		VCCIO7A					E24		
		VCCIO7A					B15		
		VCCIO7A					B25		
		VCCIO7A					H23		
		VCCIO7A					D21		
		VCCIO7A					C18		
		VCCIO8A					A7		
		VCCIO8A					L12		
		VCCIO8A					J16		
		VCCIO8A					H13		
		VCCIO8A					G10		
		VCCIO8A					F7		
		VCCIO8A					D11		
		VCCIO8A					C8		
		VCCIO8A					E14		
		VCCIO8A					B5		
		VCCPD3A					AB11		
		VCCPD3A					AD10		
		VCCPD3B4A					AC17		
		VCCPD3B4A					AE11		
		VCCPD3B4A					AD15		
		VCCPD3B4A					AC12		
		VCCPD3B4A					AE21		
		VCCPD3B4A					AC20		
		VCCPD5A					W23		
		VCCPD5A					W25		
		VCCPD5B					T26		
		VCCPD5B					U24		
		VCCPD6A					M24		
		VCCPD6A					P24		
		VCCPD6A					K23		
		VCCPD7A8A					F21		
		VCCPD7A8A					G13		
		VCCPD7A8A					G16		
		VCCPD7A8A					G19		
		VCCPD7A8A					F11		



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Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16
		VCCPD7A8A					F23		
		VCCPD7A8A					D24		
3A	VREFB3AN0	VREFB3AN0					AE8		
3B	VREFB3BN0	VREFB3BN0					AJ13		
4A	VREFB4AN0	VREFB4AN0					AH16		
5A	VREFB5AN0	VREFB5AN0					AC25		
5B	VREFB5BN0	VREFB5BN0					P27		
6A	VREFB6AN0	VREFB6AN0					M26		
7A	VREFB7AN0	VREFB7AN0					B16		
8A	VREFB8AN0	VREFB8AN0					B9		
		NC					L7		
		NC					K8		
		NC					J1		
		NC					J2		
		NC					H3		
		NC					H4		
		NC					G2		
		NC					F3		
		NC					F4		
		NC					E1		
		NC					D4		
		NC					G1		
		NC					E2		
		NC					D3		
		VCCH_GXBL					AB6		
		VCCH_GXBL					V6		
		VCCH_GXBL					P6		
		VCCH_GXBL					K6		
		VCCL_GXBL					AC5		
		VCCL_GXBL					W5		
		VCCL_GXBL					R5		
		VCCL_GXBL					L5		
		RREF_TL					C1		
		VCCA_FPLL					Y8		
		VCCA_FPLL					J8		
		VCCA_FPLL					AB23		
		VCCA_FPLL					J24		
		VCC_AUX					G11		
		VCC_AUX					H16		
		VCC_AUX					H22		
		VCC_AUX					AD22		
		VCC_AUX					AC16		
		VCC_AUX					AC10		
		VCCE_GXBL					J5		
		VCCE_GXBL					AD6		
		VCCE_GXBL					AA5		
		VCCE_GXBL					Y6		
		VCCE_GXBL					N5		
		VCCE_GXBL					M6		
		VCCE_GXBL					U5		
		VCCE_GXBL					T6		

Note:
(1) For more information about pin definition and pin connection guidelines, refer to the [Cyclone V Device Family Pin Connection Guidelines](#).



Pin Information for the Cyclone® V 5CGXBC7 Device
Version 1.2

Version Number	Date	Changes Made
1.0	1/20/2012	Initial release.
1.1	3/15/2013	Added M484 package.
1.2	10/11/2013	Removed nPERST* pins because this device does not support PCIe interface.