Bank Number	VREF	PinName/Function *(2), (3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		DNU					R29									
		DNU					T29									
		RREF_TL					T30									
GXB_L1		REFCLK3Ln					W23									
GXB_L1		REFCLK3Lp					W22									
GXB_L1		GXB_TX_L11n					U27*									
GXB_L1		GXB_TX_L11p					U28*									
GXB_L1		GXB_RX_L11p,GXB_REFCLK_L11p					V30*									
GXB_L1		GXB_RX_L11n,GXB_REFCLK_L11n					V29*									
GXB_L1		GXB_TX_L10n					W27									
GXB_L1		GXB_TX_L10p					W28									
GXB_L1		GXB_RX_L10p,GXB_REFCLK_L10p					Y30									
GXB_L1		GXB_RX_L10n,GXB_REFCLK_L10n					Y29									
GXB_L1		GXB_TX_L9n					AA27*									
GXB_L1		GXB_TX_L9p					AA28*									
GXB_L1		GXB_RX_L9p,GXB_REFCLK_L9p					AB30*									
GXB_L1		GXB_RX_L9n,GXB_REFCLK_L9n					AB29*									
GXB_L1		GXB_TX_L8n					AC27*									
GXB_L1		GXB_TX_L8p					AC28*									
GXB_L1		GXB_RX_L8p,GXB_REFCLK_L8p					AD30*									
GXB_L1		GXB_RX_L8n,GXB_REFCLK_L8n					AD29*									
GXB_L1		GXB_TX_L7n					AE27									
GXB_L1		GXB_TX_L7p					AE28									
GXB_L1		GXB_RX_L7p,GXB_REFCLK_L7p					AF30									
GXB_L1		GXB_RX_L7n,GXB_REFCLK_L7n					AF29									
GXB_L1		GXB_TX_L6n					AG27*									
GXB_L1		GXB_TX_L6p					AG28*									
GXB_L1		GXB_RX_L6p,GXB_REFCLK_L6p					AH30*									
GXB_L1		GXB_RX_L6n,GXB_REFCLK_L6n					AH29*									
GXB_L1		REFCLK2Ln					AA23									
GXB_L1		REFCLK2Lp					AA22									
		DNU					AJ28									
3A		TDO		TDO			AF25									
3A		TMS		TMS			AK29									
3A		TCK		TCK			AH25									
3A		TDI		TDI			AG25									
3A		DCLK		DCLK			AK27									
3A		nCSO		DATA4			AJ27									
3A		AS_DATA3		DATA3			AK28									
3A		AS_DATA2		DATA2			AE25									
3A		AS_DATA1		DATA1			AC25									
3A		AS_DATA0,ASDO		DATA0			AK26									
3A	VREFB3AN0	IO	RZQ_0		DIFFIO_TX_B1n	DIFFOUT_B1n	AD25									
3A	VREFB3AN0	IO	CLK0n		DIFFIO_RX_B2n	DIFFOUT_B2n	AE24									
3A	VREFB3AN0	IO	CLK0p		DIFFIO_RX_B2p	DIFFOUT_B2p	AF24									
3A	VREFB3AN0	IO	CLK1n		DIFFIO_RX_B4n	DIFFOUT_B4n	AJ25									
3A	VREFB3AN0	IO	CLK1p		DIFFIO_RX_B4p	DIFFOUT_B4p	AK25									
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B5n	DIFFOUT_B5n	AD23									
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB0		DIFFIO_TX_B5p	DIFFOUT_B5p	AE23									
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT3,FPLL_BL_FBn		DIFFIO_RX_B6n	DIFFOUT_B6n	AG24									
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT2,FPLL_BL_FBp,FPLL_BL_FB1		DIFFIO_RX_B6p	DIFFOUT_B6p	AH24									
3A	VREFB3AN0	IO	VREFB3AN0				AD24									
3A	VREFB3AN0	IO	CLK2n		DIFFIO_RX_B7n	DIFFOUT_B7n	AJ24									
3A	VREFB3AN0	IO	CLK2p		DIFFIO_RX_B7p	DIFFOUT_B7p	AK24									
3A	VREFB3AN0	IO			DIFFIO_TX_B8n	DIFFOUT_B8n	AC22				CS#_3A_1	CS#_3A_1				
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AC21	DQ1B	DQ1B		CS#_3A_0	CS#_3A_0				
3A	VREFB3AN0	IO	CLK3n		DIFFIO_RX_B9n	DIFFOUT_B9n	AG23	DQ1B	DQ1B							
3A	VREFB3AN0	IO	CLK3p		DIFFIO_RX_B9p	DIFFOUT_B9p	AH23	DQ1B	DQ1B							
3A	VREFB3AN0	IO			DIFFIO_TX_B10n	DIFFOUT_B10n	AE21				ODT_3A_1	ODT_3A_1				
3A	VREFB3AN0	IO			DIFFIO_TX_B10p	DIFFOUT_B10p	AD22	DQ1B	DQ1B		ODT_3A_0	ODT_3A_0				
3A	VREFB3AN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	AK23	DQSn1B/QK1B	DQ1B		WE#_3A					
3A	VREFB3AN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	AK22	DQS1B/CQ1B/CQn1B/QKn1B	DQ1B		CAS#_3A					
3A	VREFB3AN0	IO			DIFFIO_TX_B12n	DIFFOUT_B12n	AJ22				RAS#_3A					
3A	VREFB3AN0	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AJ21	DQ1B	DQ1B		BA_3A_2					
3A	VREFB3AN0	IO			DIFFIO_RX_B13n	DIFFOUT_B13n	AF22	DQ1B	DQ1B		BA_3A_1					
3A	VREFB3AN0	IO			DIFFIO_RX_B13p	DIFFOUT_B13p	AG22	DQ1B	DQ1B		BA_3A_0					
3A	VREFB3AN0	IO			DIFFIO_TX_B14n	DIFFOUT_B14n	AE18				A_3A_15					
3A	VREFB3AN0	IO			DIFFIO_TX_B14p	DIFFOUT_B14p	AF18	DQ1B	DQ1B		A_3A_14					
3A	VREFB3AN0	IO			DIFFIO_RX_B15n	DIFFOUT_B15n	AK21	DQ1B	DQ1B		A_3A_13					
3A	VREFB3AN0	IO			DIFFIO_RX_B15p	DIFFOUT_B15p	AK20	DQ1B	DQ1B		A_3A_12					
3A	VREFB3AN0	IO			DIFFIO_TX_B16n	DIFFOUT_B16n	AH21				A_3A_11					
3A	VREFB3AN0	IO			DIFFIO_TX_B16p	DIFFOUT_B16p	AH20	DQ2B	DQ1B		A_3A_10					
3A	VREFB3AN0	IO			DIFFIO_RX_B17n	DIFFOUT_B17n	AF21	DQ2B	DQ1B		A_3A_9	CA_3A_9				
3A	VREFB3AN0	IO			DIFFIO_RX_B17p	DIFFOUT_B17p	AG21	DQ2B	DQ1B		A_3A_8	CA_3A_8				
3A	VREFB3AN0	IO			DIFFIO_TX_B18n	DIFFOUT_B18n	AD21				A_3A_7	CA_3A_7				
3A	VREFB3AN0	IO			DIFFIO_TX_B18p	DIFFOUT_B18p	AD20	DQ2B	DQ1B		A_3A_6	CA_3A_6				
3A	VREFB3AN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	AJ19	DQSn2B/QK2B	DQSn1B/QK1B		A_3A_5	CA_3A_5				
3A	VREFB3AN0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	AK19	DQS2B/CQ2B/CQn2B/QKn2B	DQS1B/CQ1B/CQn1B/QKn1B		A_3A_4	CA_3A_4				
3A	VREFB3AN0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	AG20				A_3A_3	CA_3A_3				
3A	VREFB3AN0	IO			DIFFIO_TX_B20p	DIFFOUT_B20p	AG19	DQ2B	DQ1B		A_3A_2	CA_3A_2				
3A	VREFB3AN0	IO			DIFFIO_RX_B21n	DIFFOUT_B21n	AG18	DQ2B	DQ1B		A_3A_1	CA_3A_1				
3A	VREFB3AN0	IO			DIFFIO_RX_B21p	DIFFOUT_B21p	AH18	DQ2B	DQ1B		A_3A_0	CA_3A_0				
3A	VREFB3AN0	IO			DIFFIO_TX_B22n	DIFFOUT_B22n	AD19				CKE_3A_1	CKE_3A_1				
3A	VREFB3AN0	IO			DIFFIO_TX_B22p	DIFFOUT_B22p	AD18	DQ2B	DQ1B		CKE_3A_0	CKE_3A_0				
3A	VREFB3AN0	IO			DIFFIO_RX_B23n	DIFFOUT_B23n	AF19	DQ2B	DQ1B		CK#_3A	CK#_3A				
3A	VREFB3AN0	IO			DIFFIO_RX_B23p	DIFFOUT_B23p	AE20	DQ2B	DQ1B		CK_3A	CK_3A				
3B	VREFB3BN0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	AE15				RESET#_3A					
3B	VREFB3BN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	AE14	DQ3B	DQ2B		DQ1_3B_8	DQ1_3B_8				
3B	VREFB3BN0	IO			DIFFIO_RX_B25n	DIFFOUT_B25n	AJ18	DQ3B	DQ2B		DQ1_3B_7	DQ1_3B_7				
3B	VREFB3BN0	IO			DIFFIO_RX_B25p	DIFFOUT_B25p	AK18	DQ3B	DQ2B		DQ1_3B_6	DQ1_3B_6				
3B	VREFB3BN0	IO			DIFFIO_TX_B26n	DIFFOUT_B26n	AK15									
3B	VREFB3BN0	IO			DIFFIO_TX_B26p	DIFFOUT_B26p	AK14	DQ3B	DQ2B		DM1_3B	DM1_3B				
3B	VREFB3BN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	AK17	DQSn3B/QK3B	DQ2B		DQS#1_3B	DQS#1_3B				
3B	VREFB3BN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	AK16	DQS3B/CQ3B/CQn3B/QKn3B	DQ2B		DQS1_3B	DQS1_3B				
3B	VREFB3BN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AC15									
3B	VREFB3BN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AD15	DQ3B	DQ2B		DQ1_3B_5	DQ1_3B_5				
3B	VREFB3BN0	IO			DIFFIO_RX_B29n	DIFFOUT_B29n	AJ16	DQ3B	DQ2B		DQ1_3B_4	DQ1_3B_4				
3B	VREFB3BN0	IO			DIFFIO_RX_B29p	DIFFOUT_B29p	AJ15	DQ3B	DQ2B		DQ1_3B_3	DQ1_3B_3				
3B	VREFB3BN0	IO	VREFB3BN0				AD16									
3B	VREFB3BN0	IO					AD17	DQ3B	DQ2B		DQ1_3B_2	DQ1_3B_2				
3B	VREFB3BN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	AH17	DQ3B	DQ2B		DQ1_3B_1	DQ1_3B_1				
3B	VREFB3BN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	AH16	DQ3B	DQ2B		DQ1_3B_0	DQ1_3B_0				
3B	VREFB3BN0	IO			DIFFIO_TX_B31p	DIFFOUT_B31p	AG17	DQ4B	DQ2B		DQ2_3B_8	DQ2_3B_8				
3B	VREFB3BN0	IO			DIFFIO_RX_B32n	DIFFOUT_B32n	AG14	DQ4B	DQ2B		DQ2_3B_7	DQ2_3B_7				
3B	VREFB3BN0	IO			DIFFIO_RX_B32p	DIFFOUT_B32p	AH14	DQ4B	DQ2B		DQ2_3B_6	DQ2_3B_6				
3B	VREFB3BN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AE17	DQ4B	DQ2B		DM2_3B	DM2_3B				
3B	VREFB3BN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AF16	DQSn4B/QK4B	DQSn2B/QK2B		DQS#2_3B	DQS#2_3B				
3B	VREFB3BN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AG16	DQS4B/CQ4B/CQn4B/QKn4B	DQS2B/CQ2B/CQn2B/QKn2B		DQS2_3B	DQS2_3B				
3B	VREFB3BN0	IO			DIFFIO_TX_B35p	DIFFOUT_B35p	AD14	DQ4B	DQ2B		DQ2_3B_5	DQ2_3B_5				
3B	VREFB3BN0	IO			DIFFIO_RX_B36n	DIFFOUT_B36n	AF15	DQ4B	DQ2B		DQ2_3B_4	DQ2_3B_4				
3B	VREFB3BN0	IO			DIFFIO_RX_B36p	DIFFOUT_B36p	AG15	DQ4B	DQ2B		DQ2_3B_3	DQ2_3B_3				
3B	VREFB3BN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	AD13	DQ4B	DQ2B		DQ2_3B_2	DQ2_3B_2				
3B	VREFB3BN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AB13	DQ4B	DQ2B		DQ2_3B_1	DQ2_3B_1				
3B	VREFB3BN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AC13	DQ4B	DQ2B		DQ2_3B_0	DQ2_3B_0				
3D	VREFB3DN0	IO	VREFB3DN0				AE12									
3D	VREFB3DN0	IO	CLK4n		DIFFIO_RX_B76n	DIFFOUT_B76n	AJ13									
3D	VREFB3DN0	IO	CLK4p		DIFFIO_RX_B76p	DIFFOUT_B76p	AK13									

Copyright © 2016 Altera Corp.

Bank Number	VREF	PinName/Function *(2), (3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
3D	VREFB3DN0	IO	CLK5n		DIFFIO_RX_B78n	DIFFOUT_B78n	AH12									
3D	VREFB3DN0	IO	CLK5p		DIFFIO_RX_B78p	DIFFOUT_B78p	AJ12									
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT1,FPLL_BC_CLKOUTn		DIFFIO_TX_B79n	DIFFOUT_B79n	AB12									
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT0,FPLL_BC_CLKOUTp,FPLL_BC_FB0		DIFFIO_TX_B79p	DIFFOUT_B79p	AC12									
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT3,FPLL_BC_FBn		DIFFIO_RX_B80n	DIFFOUT_B80n	AH13									
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT2,FPLL_BC_FBp,FPLL_BC_FB1		DIFFIO_RX_B80p	DIFFOUT_B80p	AG12									
3D	VREFB3DN0	IO	CLK6n		DIFFIO_RX_B82n	DIFFOUT_B82n	AF13									
3D	VREFB3DN0	IO	CLK6p		DIFFIO_RX_B82p	DIFFOUT_B82p	AF12									
3D	VREFB3DN0	IO	CLK7n		DIFFIO_RX_B84n	DIFFOUT_B84n	AD12									
3D	VREFB3DN0	IO	CLK7p		DIFFIO_RX_B84p	DIFFOUT_B84p	AD11									
		VCCD_FPLL					AB15									
		VCCA_FPLL					AB16									
		DNU					AC16									
4A	VREFB4AN0	IO		DATA10	DIFFIO_TX_B146p	DIFFOUT_B146p	AC10	DQ5B								
4A	VREFB4AN0	IO		DATA11	DIFFIO_RX_B147n	DIFFOUT_B147n	AE10	DQ5B								
4A	VREFB4AN0	IO		DATA5	DIFFIO_RX_B147p	DIFFOUT_B147p	AF10	DQ5B								
4A	VREFB4AN0	IO		DATA6	DIFFIO_TX_B148p	DIFFOUT_B148p	AD10	DQ5B								
4A	VREFB4AN0	IO		DATA12	DIFFIO_RX_B149n	DIFFOUT_B149n	AG11	DQSn5B/QK5B								
4A	VREFB4AN0	IO		DATA13	DIFFIO_RX_B149p	DIFFOUT_B149p	AH11	DQS5B/CQ5B/CQn5B/QKn5B								
4A	VREFB4AN0	IO		DATA7	DIFFIO_TX_B150n	DIFFOUT_B150n	AK12									
4A	VREFB4AN0	IO		DATA8	DIFFIO_TX_B150p	DIFFOUT_B150p	AK11	DQ5B								
4A	VREFB4AN0	IO		DATA14	DIFFIO_RX_B151n	DIFFOUT_B151n	AG10	DQ5B								
4A	VREFB4AN0	IO		DATA15	DIFFIO_RX_B151p	DIFFOUT_B151p	AH10	DQ5B								
4A	VREFB4AN0	IO		DATA9	DIFFIO_TX_B152n	DIFFOUT_B152n	AE9									
4A	VREFB4AN0	IO		CLKUSR	DIFFIO_TX_B152p	DIFFOUT_B152p	AF9	DQ5B								
4A	VREFB4AN0	IO			DIFFIO_RX_B153n	DIFFOUT_B153n	AK10	DQ5B								
4A	VREFB4AN0	IO			DIFFIO_RX_B153p	DIFFOUT_B153p	AK9	DQ5B								
4A	VREFB4AN0	IO		PR_ERROR	DIFFIO_TX_B154n	DIFFOUT_B154n	AJ10									
4A	VREFB4AN0	IO		PR_READY	DIFFIO_TX_B154p	DIFFOUT_B154p	AJ9	DQ6B								
4A	VREFB4AN0	IO		PR_DONE	DIFFIO_RX_B155n	DIFFOUT_B155n	AG9	DQ6B								
4A	VREFB4AN0	IO		PR_REQUEST	DIFFIO_RX_B155p	DIFFOUT_B155p	AH9	DQ6B								
4A	VREFB4AN0	IO		nPERSTR0	DIFFIO_TX_B156n	DIFFOUT_B156n	AD9									
4A	VREFB4AN0	IO			DIFFIO_TX_B156p	DIFFOUT_B156p	AC8	DQ6B								
4A	VREFB4AN0	IO		CvP_CONFDONE	DIFFIO_RX_B157n	DIFFOUT_B157n	AK8	DQSn6B/QK6B								
4A	VREFB4AN0	IO		CRC_ERROR	DIFFIO_RX_B157p	DIFFOUT_B157p	AK7	DQS6B/CQ6B/CQn6B/QKn6B								
4A	VREFB4AN0	IO		DEV_OE	DIFFIO_TX_B158n	DIFFOUT_B158n	AK6									
4A	VREFB4AN0	IO		DEV_CLRn	DIFFIO_TX_B158p	DIFFOUT_B158p	AK5	DQ6B								
4A	VREFB4AN0	IO		INIT_DONE	DIFFIO_RX_B159n	DIFFOUT_B159n	AG8	DQ6B								
4A	VREFB4AN0	IO		nCEO	DIFFIO_RX_B159p	DIFFOUT_B159p	AH8	DQ6B								
4A	VREFB4AN0	IO	VREFB4AN0				AC9									
4A	VREFB4AN0	IO					AE8	DQ6B								
4A	VREFB4AN0	IO	CLK11n		DIFFIO_RX_B160n	DIFFOUT_B160n	AJ4	DQ6B								
4A	VREFB4AN0	IO	CLK11p		DIFFIO_RX_B160p	DIFFOUT_B160p	AK4	DQ6B								
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_B161n	DIFFOUT_B161n	AJ7									
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB0		DIFFIO_TX_B161p	DIFFOUT_B161p	AJ6									
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT3,FPLL_BR_FBn		DIFFIO_RX_B162n	DIFFOUT_B162n	AG6									
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT2,FPLL_BR_FBp,FPLL_BR_FB1		DIFFIO_RX_B162p	DIFFOUT_B162p	AH6									
4A	VREFB4AN0	IO	CLK10n		DIFFIO_RX_B164n	DIFFOUT_B164n	AF7									
4A	VREFB4AN0	IO	CLK10p		DIFFIO_RX_B164p	DIFFOUT_B164p	AG7									
4A	VREFB4AN0	IO	CLK9n		DIFFIO_RX_B166n	DIFFOUT_B166n	AE6									
4A	VREFB4AN0	IO	CLK9p		DIFFIO_RX_B166p	DIFFOUT_B166p	AF6									
4A	VREFB4AN0	IO			DIFFIO_TX_B167n	DIFFOUT_B167n	AC7									
4A	VREFB4AN0	IO	RZQ_1		DIFFIO_TX_B167p	DIFFOUT_B167p	AD7									
4A	VREFB4AN0	IO	CLK8n		DIFFIO_RX_B168n	DIFFOUT_B168n	AC6									
4A	VREFB4AN0	IO	CLK8p		DIFFIO_RX_B168p	DIFFOUT_B168p	AD6									
		RREF_BR					AK2									
		DNU					AJ3									
		DNU					AK3									
GXB_R0		REFCLK0Rp					AA9									
GXB_R0		REFCLK0Rn					AA8									
GXB_R0		GXB_RX_R0n,GXB_REFCLK_R0n					AH2									
GXB_R0		GXB_RX_R0p,GXB_REFCLK_R0p					AH1									
GXB_R0		GXB_TX_R0p					AG3									
GXB_R0		GXB_TX_R0n					AG4									
GXB_R0		GXB_RX_R1n,GXB_REFCLK_R1n					AF2									
GXB_R0		GXB_RX_R1p,GXB_REFCLK_R1p					AF1									
GXB_R0		GXB_TX_R1p					AE3									
GXB_R0		GXB_TX_R1n					AE4									
GXB_R0		GXB_RX_R2n,GXB_REFCLK_R2n					AD2									
GXB_R0		GXB_RX_R2p,GXB_REFCLK_R2p					AD1									
GXB_R0		GXB_TX_R2p					AC3									
GXB_R0		GXB_TX_R2n					AC4									
GXB_R0		GXB_RX_R3n,GXB_REFCLK_R3n					AB2*									
GXB_R0		GXB_RX_R3p,GXB_REFCLK_R3p					AB1*									
GXB_R0		GXB_TX_R3p					AA3*									
GXB_R0		GXB_TX_R3n					AA4*									
GXB_R0		GXB_RX_R4n,GXB_REFCLK_R4n					Y2									
GXB_R0		GXB_RX_R4p,GXB_REFCLK_R4p					Y1									
GXB_R0		GXB_TX_R4p					W3									
GXB_R0		GXB_TX_R4n					W4									
GXB_R0		GXB_RX_R5n,GXB_REFCLK_R5n					V2*									
GXB_R0		GXB_RX_R5p,GXB_REFCLK_R5p					V1*									
GXB_R0		GXB_TX_R5p					U3*									
GXB_R0		GXB_TX_R5n					U4*									
GXB_R0		REFCLK1Rp					W9									
GXB_R0		REFCLK1Rn					W8									
6B	VREFB6BN0_HPS	HPS_DDR					R4				HPS_DM_4	HPS_DM_4				
6B	VREFB6BN0_HPS	HPS_DDR					R5				HPS_DQ_39	HPS_DQ_39				
6B	VREFB6BN0_HPS	HPS_DDR					P7				HPS_DQ_37	HPS_DQ_37				
6B	VREFB6BN0_HPS	HPS_DDR					N7				HPS_DQ_38	HPS_DQ_38				
6B	VREFB6BN0_HPS	HPS_DDR					R7				HPS_DQ_36	HPS_DQ_36				
6B	VREFB6BN0_HPS	HPS_DDR					R3				HPS_DQS_4	HPS_DQS_4				
6B	VREFB6BN0_HPS	HPS_GPI13					T7									
6B	VREFB6BN0_HPS	HPS_DDR					R2				HPS_DQS#_4	HPS_DQS#_4				
6B	VREFB6BN0_HPS	HPS_DDR					T8				HPS_DQ_35	HPS_DQ_35				
6B	VREFB6BN0_HPS	HPS_DDR					R1				HPS_DQ_33	HPS_DQ_33				
6B	VREFB6BN0_HPS	HPS_DDR					M6				HPS_DQ_34	HPS_DQ_34				
6B	VREFB6BN0_HPS	HPS_DDR					T1				HPS_DQ_32	HPS_DQ_32				
6B	VREFB6BN0_HPS	HPS_GPI12					N6									
6B	VREFB6BN0_HPS	HPS_GPI11					N3									
6B	VREFB6BN0_HPS	HPS_DDR					P4				HPS_DM_3	HPS_DM_3				
6B	VREFB6BN0_HPS	HPS_GPI10					P3									
6B	VREFB6BN0_HPS	HPS_DDR					N5				HPS_DQ_31	HPS_DQ_31				
6B	VREFB6BN0_HPS	HPS_DDR					N2				HPS_DQ_29	HPS_DQ_29				
6B	VREFB6BN0_HPS	HPS_DDR					R6				HPS_DQ_30	HPS_DQ_30				
6B	VREFB6BN0_HPS	HPS_DDR					P1				HPS_DQ_28	HPS_DQ_28				
6B	VREFB6BN0_HPS	VREFB6BN0_HPS					T6									
6B	VREFB6BN0_HPS	HPS_DDR					M2				HPS_DQS_3	HPS_DQS_3				
6B	VREFB6BN0_HPS	HPS_GPI9					L1									
6B	VREFB6BN0_HPS	HPS_DDR					M3				HPS_DQS#_3	HPS_DQS#_3				
6B	VREFB6BN0_HPS	HPS_DDR					M1				HPS_DQ_27	HPS_DQ_27				
6B	VREFB6BN0_HPS	HPS_DDR					L4				HPS_DQ_25	HPS_DQ_25				
6B	VREFB6BN0_HPS	HPS_DDR					U9				HPS_DQ_26	HPS_DQ_26				
6B	VREFB6BN0_HPS	HPS_DDR					K4				HPS_DQ_24	HPS_DQ_24				
6B	VREFB6BN0_HPS	HPS_GPI8					T9									
6B	VREFB6BN0_HPS	HPS_GPI7					K1									
6B	VREFB6BN0_HPS	HPS_DDR					L3				HPS_DM_2	HPS_DM_2				

Copyright © 2016 Altera Corp.

Bank Number	VREF	PinName/Function *(2), (3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
6B	VREFB6BN0_HPS	HPS_GPI6					J1									
6B	VREFB6BN0_HPS	HPS_DDR					K3				HPS_DQ_23	HPS_DQ_23				
6B	VREFB6BN0_HPS	HPS_DDR					N4				HPS_DQ_21	HPS_DQ_21				
6B	VREFB6BN0_HPS	HPS_DDR					J8				HPS_DQ_22	HPS_DQ_22				
6B	VREFB6BN0_HPS	HPS_DDR					M5				HPS_DQ_20	HPS_DQ_20				
6B	VREFB6BN0_HPS	HPS_GPI5					K8									
6B	VREFB6BN0_HPS	HPS_DDR					G8				HPS_DQS_2	HPS_DQS_2				
6B	VREFB6BN0_HPS	HPS_DDR					J2				HPS_RESET#	HPS_RESET#				
6B	VREFB6BN0_HPS	HPS_DDR					F8				HPS_DQS#_2	HPS_DQS#_2				
6B	VREFB6BN0_HPS	HPS_DDR					K2				HPS_DQ_19	HPS_DQ_19				
6B	VREFB6BN0_HPS	HPS_DDR					J4				HPS_DQ_17	HPS_DQ_17				
6B	VREFB6BN0_HPS	HPS_DDR					R9				HPS_DQ_18	HPS_DQ_18				
6B	VREFB6BN0_HPS	HPS_DDR					J3				HPS_DQ_16	HPS_DQ_16				
6B	VREFB6BN0_HPS	HPS_GPI4					P9									
6A	VREFB6AN0_HPS	HPS_GPI3					D1									
6A	VREFB6AN0_HPS	HPS_DDR					E3				HPS_DM_1	HPS_DM_1				
6A	VREFB6AN0_HPS	HPS_GPI2					C1									
6A	VREFB6AN0_HPS	HPS_DDR					F3				HPS_DQ_15	HPS_DQ_15				
6A	VREFB6AN0_HPS	HPS_DDR					F1				HPS_DQ_13	HPS_DQ_13				
6A	VREFB6AN0_HPS	HPS_DDR					M7				HPS_DQ_14	HPS_DQ_14				
6A	VREFB6AN0_HPS	HPS_DDR					G1				HPS_DQ_12	HPS_DQ_12				
6A	VREFB6AN0_HPS	HPS_DDR					L7				HPS_CKE_0	HPS_CKE_0				
6A	VREFB6AN0_HPS	HPS_DDR					D2				HPS_DQS_1	HPS_DQS_1				
6A	VREFB6AN0_HPS	HPS_DDR					A2				HPS_CKE_1	HPS_CKE_1				
6A	VREFB6AN0_HPS	HPS_DDR					E1				HPS_DQS#_1	HPS_DQS#_1				
6A	VREFB6AN0_HPS	HPS_DDR					B1				HPS_DQ_11	HPS_DQ_11				
6A	VREFB6AN0_HPS	HPS_DDR					A3				HPS_DQ_9	HPS_DQ_9				
6A	VREFB6AN0_HPS	HPS_DDR					G2				HPS_DQ_10	HPS_DQ_10				
6A	VREFB6AN0_HPS	HPS_DDR					B3				HPS_DQ_8	HPS_DQ_8				
6A	VREFB6AN0_HPS	HPS_GPI1					H3									
6A	VREFB6AN0_HPS	HPS_GPI0					H4									
6A	VREFB6AN0_HPS	HPS_DDR					K5				HPS_DM_0	HPS_DM_0				
6A	VREFB6AN0_HPS	HPS_DDR					K6				HPS_DQ_7	HPS_DQ_7				
6A	VREFB6AN0_HPS	HPS_DDR					D3				HPS_DQ_5	HPS_DQ_5				
6A	VREFB6AN0_HPS	HPS_DDR					A4				HPS_DQ_6	HPS_DQ_6				
6A	VREFB6AN0_HPS	HPS_DDR					C3				HPS_DQ_4	HPS_DQ_4				
6A	VREFB6AN0_HPS	HPS_DDR					B4				HPS_ODT_1	HPS_ODT_1				
6A	VREFB6AN0_HPS	HPS_DDR					A5				HPS_DQS_0	HPS_DQS_0				
6A	VREFB6AN0_HPS	HPS_DDR					G3				HPS_ODT_0	HPS_ODT_0				
6A	VREFB6AN0_HPS	HPS_DDR					B6				HPS_DQS#_0	HPS_DQS#_0				
6A	VREFB6AN0_HPS	HPS_DDR					G4				HPS_DQ_3	HPS_DQ_3				
6A	VREFB6AN0_HPS	HPS_DDR					C4				HPS_DQ_1	HPS_DQ_1				
6A	VREFB6AN0_HPS	HPS_DDR					E7				HPS_DQ_2	HPS_DQ_2				
6A	VREFB6AN0_HPS	HPS_DDR					D4				HPS_DQ_0	HPS_DQ_0				
6A	VREFB6AN0_HPS	VREFB6AN0_HPS					K7									
6A	VREFB6AN0_HPS	HPS_DDR					F5				HPS_A_0	HPS_CA_0				
6A	VREFB6AN0_HPS	HPS_DDR					E4				HPS_A_1	HPS_CA_1				
6A	VREFB6AN0_HPS	HPS_DDR					B7				HPS_A_4	HPS_CA_4				
6A	VREFB6AN0_HPS	HPS_DDR					G5				HPS_A_2	HPS_CA_2				
6A	VREFB6AN0_HPS	HPS_DDR					A6				HPS_A_5	HPS_CA_5				
6A	VREFB6AN0_HPS	HPS_DDR					H6				HPS_A_3	HPS_CA_3				
6A	VREFB6AN0_HPS	HPS_DDR					G6				HPS_CK	HPS_CK				
6A	VREFB6AN0_HPS	HPS_DDR					A8				HPS_A_6	HPS_CA_6				
6A	VREFB6AN0_HPS	HPS_DDR					G7				HPS_CK#	HPS_CK#				
6A	VREFB6AN0_HPS	HPS_DDR					A7				HPS_A_7	HPS_CA_7				
6A	VREFB6AN0_HPS	HPS_DDR					A10				HPS_BA_1					
6A	VREFB6AN0_HPS	HPS_DDR					H7				HPS_BA_0					
6A	VREFB6AN0_HPS	HPS_DDR					A9				HPS_BA_2					
6A	VREFB6AN0_HPS	HPS_DDR					E6				HPS_CAS#					
6A	VREFB6AN0_HPS	HPS_DDR					D5				HPS_RAS#					
6A	VREFB6AN0_HPS	HPS_DDR					D6				HPS_A_8	HPS_CA_8				
6A	VREFB6AN0_HPS	HPS_DDR					J6				HPS_A_10					
6A	VREFB6AN0_HPS	HPS_DDR					C6				HPS_A_9	HPS_CA_9				
6A	VREFB6AN0_HPS	HPS_DDR					J7				HPS_A_11					
6A	VREFB6AN0_HPS	HPS_DDR					C9				HPS_CS#_0	HPS_CS#_0				
6A	VREFB6AN0_HPS	HPS_DDR					D7				HPS_A_12					
6A	VREFB6AN0_HPS	HPS_DDR					C10				HPS_CS#_1	HPS_CS#_1				
6A	VREFB6AN0_HPS	HPS_DDR					C7				HPS_A_13					
6A	VREFB6AN0_HPS	HPS_DDR					D9				HPS_A_14					
6A	VREFB6AN0_HPS	HPS_DDR					B9				HPS_WE#					
6A	VREFB6AN0_HPS	HPS_DDR					D8				HPS_A_15					
6A	VREFB6AN0_HPS	HPS_RZQ_0					B10									
		DNU					F7									
		GND					P9									
		GND					F10									
7A		HPS_nRST					M9									
7A		HPS_nPOR					H10									
7A		HPS_TDO					N9									
		VCCRSTCLK_HPS					H9									
7A		HPS_TMS					L9									
7A		HPS_TCK					J11									
7A		HPS_TRST					K9									
7A		HPS_TDI					H11									
		GND					A12									
7A		HPS_PORSEL					A13									
7A		HPS_CLK1					A11									
7A		HPS_CLK2					A14									
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_CLK					A15						TRACE_CLK			HPS_GPIO48
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_D0					K10						TRACE_D0	SPIS0_CLK	UART0_RX	HPS_GPIO49
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_D1					A16						TRACE_D1	SPIS0_MOSI	UART0_TX	HPS_GPIO50
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_D2					L10						TRACE_D2	SPIS0_MISO	I2C1_SDA	HPS_GPIO51
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_D3					A18						TRACE_D3	SPIS0_SS0	I2C1_SCL	HPS_GPIO52
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_D4					L11						TRACE_D4	SPIS1_CLK		HPS_GPIO53
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_D5					A17						TRACE_D5	SPIS1_MOSI		HPS_GPIO54
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_D6					M11						TRACE_D6	SPIS1_SS0	I2C0_SDA	HPS_GPIO55
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_D7					B15						TRACE_D7	SPIS1_MISO	I2C0_SCL	HPS_GPIO56
7A	VREFB7A7B7C7D7EN0_HPS	SPIM0_CLK					A20						SPIM0_CLK	I2C1_SDA	UART0_CTS	HPS_GPIO57
7A	VREFB7A7B7C7D7EN0_HPS	SPIM0_MOSI					B16						SPIM0_MOSI	I2C1_SCL	UART0_RTS	HPS_GPIO58
7A	VREFB7A7B7C7D7EN0_HPS	SPIM0_MISO					A19						SPIM0_MISO		UART1_CTS	HPS_GPIO59
7A	VREFB7A7B7C7D7EN0_HPS	SPIM0_SS0,BOOTSEL0					B13						SPIM0_SS0		UART1_RTS	HPS_GPIO60
7A	VREFB7A7B7C7D7EN0_HPS	UART0_RX					M12						UART0_RX		SPIM0_SS1	HPS_GPIO61
7A	VREFB7A7B7C7D7EN0_HPS	UART0_TX,CLKSEL1					B12						UART0_TX		SPIM1_SS1	HPS_GPIO62
7A	VREFB7A7B7C7D7EN0_HPS	I2C0_SDA					N12						I2C0_SDA	UART1_RX	SPIM1_CLK	HPS_GPIO63
7A	VREFB7A7B7C7D7EN0_HPS	I2C0_SCL					B18						I2C0_SCL	UART1_TX	SPIM1_MOSI	HPS_GPIO64
7A	VREFB7A7B7C7D7EN0_HPS	UART0_RX*					C11							UART0_RX	SPIM1_MISO	HPS_GPIO65
7A	VREFB7A7B7C7D7EN0_HPS	UART0_TX*,CLKSEL0					B19							UART0_TX	SPIM1_SS0	HPS_GPIO66
7A	VREFB7A7B7C7D7EN0_HPS	SPIS1_CLK					D10						SPIS1_CLK	SPIM1_CLK		HPS_GPIO67
7A	VREFB7A7B7C7D7EN0_HPS	SPIS1_MOSI					F11						SPIS1_MOSI	SPIM1_MOSI		HPS_GPIO68
7A	VREFB7A7B7C7D7EN0_HPS	SPIS1_MISO					J10						SPIS1_MISO	SPIM1_MISO		HPS_GPIO69
7A	VREFB7A7B7C7D7EN0_HPS	SPIS1_SS0					G11						SPIS1_SS0	SPIM1_SS0		HPS_GPIO70
7A	VREFB7A7B7C7D7EN0_HPS	UART1_RX					J9						UART1_RX	SPIM1_SS1		HPS_GPIO62
7A	VREFB7A7B7C7D7EN0_HPS	UART1_TX					A21						UART1_TX	SPIM0_CLK		HPS_GPIO63
7A	VREFB7A7B7C7D7EN0_HPS	I2C1_SDA					E10						I2C1_SDA	SPIM0_MOSI		HPS_GPIO64
7A	VREFB7A7B7C7D7EN0_HPS	I2C1_SCL					A22						I2C1_SCL	SPIM0_MISO		HPS_GPIO65
7A	VREFB7A7B7C7D7EN0_HPS	SPIM0_SS0					E9							SPIM0_SS0		HPS_GPIO66
7A	VREFB7A7B7C7D7EN0_HPS	SPIS0_CLK					D11						SPIS0_CLK	SPIM0_SS1		HPS_GPIO67
7A	VREFB7A7B7C7D7EN0_HPS	SPIS0_MOSI					P12						SPIS0_MOSI			HPS_GPIO68

Copyright © 2016 Altera Corp.

Bank Number	VREF	PinName/Function *(2), (3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
7A	VREFB7A7B7C7D7EN0_HPS	SPIS0_MISO					E11						SPIS0_MISO			HPS_GPIO69
7A	VREFB7A7B7C7D7EN0_HPS	SPIS0_SS0					P13						SPIS0_SS0			HPS_GPIO70
7B	VREFB7A7B7C7D7EN0_HPS	NAND_ALE					A23						NAND_ALE	RGMII1_TX_CLK	QSPI_SS3	HPS_GPIO14
7B	VREFB7A7B7C7D7EN0_HPS	NAND_CE					C22						NAND_CE	RGMII1_TXD0	USB1_D0	HPS_GPIO15
7B	VREFB7A7B7C7D7EN0_HPS	NAND_CLE					B22						NAND_CLE	RGMII1_TXD1	USB1_D1	HPS_GPIO16
7B	VREFB7A7B7C7D7EN0_HPS	NAND_RE					D21						NAND_RE	RGMII1_TXD2	USB1_D2	HPS_GPIO17
7B	VREFB7A7B7C7D7EN0_HPS	NAND_RB					A24						NAND_RB	RGMII1_TXD3	USB1_D3	HPS_GPIO18
7B	VREFB7A7B7C7D7EN0_HPS	NAND_DQ0					C12						NAND_DQ0	RGMII1_RXD0		HPS_GPIO19
7B	VREFB7A7B7C7D7EN0_HPS	NAND_DQ1					B24						NAND_DQ1	RGMII1_MDIO	I2C3_SDA	HPS_GPIO20
7B	VREFB7A7B7C7D7EN0_HPS	NAND_DQ2					D12						NAND_DQ2	RGMII1_MDC	I2C3_SCL	HPS_GPIO21
7B	VREFB7A7B7C7D7EN0_HPS	NAND_DQ3					C15						NAND_DQ3	RGMII1_RX_CTL	USB1_D4	HPS_GPIO22
7B	VREFB7A7B7C7D7EN0_HPS	NAND_DQ4					C14						NAND_DQ4	RGMII1_TX_CTL	USB1_D5	HPS_GPIO23
7B	VREFB7A7B7C7D7EN0_HPS	NAND_DQ5					C16						NAND_DQ5	RGMII1_RX_CLK	USB1_D6	HPS_GPIO24
7B	VREFB7A7B7C7D7EN0_HPS	NAND_DQ6					C13						NAND_DQ6	RGMII1_RXD1	USB1_D7	HPS_GPIO25
7B	VREFB7A7B7C7D7EN0_HPS	NAND_DQ7					C18						NAND_DQ7	RGMII1_RXD2		HPS_GPIO26
7B	VREFB7A7B7C7D7EN0_HPS	NAND_WP					K12						NAND_WP	RGMII1_RXD3	QSPI_SS2	HPS_GPIO27
7B	VREFB7A7B7C7D7EN0_HPS	NAND_WE,BOOTSEL2					C17						NAND_WE	QSPI_SS1		HPS_GPIO28
7B	VREFB7A7B7C7D7EN0_HPS	QSPI_IO0					J12						QSPI_IO0		USB1_CLK	HPS_GPIO29
7B	VREFB7A7B7C7D7EN0_HPS	QSPI_IO1					B21						QSPI_IO1		USB1_STP	HPS_GPIO30
7B	VREFB7A7B7C7D7EN0_HPS	QSPI_IO2					C20						QSPI_IO2		USB1_DIR	HPS_GPIO31
7B	VREFB7A7B7C7D7EN0_HPS	QSPI_IO3					C21						QSPI_IO3		USB1_NXT	HPS_GPIO32
7B	VREFB7A7B7C7D7EN0_HPS	QSPI_SS0,BOOTSEL1					C19						QSPI_SS0			HPS_GPIO33
7B	VREFB7A7B7C7D7EN0_HPS	QSPI_CLK					A25						QSPI_CLK			HPS_GPIO34
7B	VREFB7A7B7C7D7EN0_HPS	QSPI_SS1					B25						QSPI_SS1			HPS_GPIO35
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_CMD					D13						SDMMC_CMD	USB0_D0		HPS_GPIO36
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_PWREN					K13						SDMMC_PWREN	USB0_D1		HPS_GPIO37
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_D0					D14						SDMMC_D0	USB0_D2		HPS_GPIO38
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_D1					L13						SDMMC_D1	USB0_D3		HPS_GPIO39
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_D4					E13						SDMMC_D4	USB0_D4		HPS_GPIO40
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_D5					N13						SDMMC_D5	USB0_D5		HPS_GPIO41
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_D6					F13						SDMMC_D6	USB0_D6		HPS_GPIO42
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_D7					P14						SDMMC_D7	USB0_D7		HPS_GPIO43
7C	VREFB7A7B7C7D7EN0_HPS	HPS_GPIO44					G13							USB0_CLK		HPS_GPIO44
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_CCLK_OUT					J13						SDMMC_CCLK_OUT	USB0_STP		HPS_GPIO45
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_D2					H13						SDMMC_D2	USB0_DIR		HPS_GPIO46
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_D3					H12						SDMMC_D3	USB0_NXT		HPS_GPIO47
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_TX_CLK					L15						RGMII0_TX_CLK			HPS_GPIO0
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_TXD0					N15						RGMII0_TXD0	USB1_D0		HPS_GPIO1
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_TXD1					K15						RGMII0_TXD1	USB1_D1		HPS_GPIO2
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_TXD2					P15						RGMII0_TXD2	USB1_D2		HPS_GPIO3
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_TXD3					D15						RGMII0_TXD3	USB1_D3		HPS_GPIO4
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_RXD0					M15						RGMII0_RXD0	USB1_D4		HPS_GPIO5
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_MDIO					E15						RGMII0_MDIO	USB1_D5	I2C2_SDA	HPS_GPIO6
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_MDC					N16						RGMII0_MDC	USB1_D6	I2C2_SCL	HPS_GPIO7
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_RX_CTL					D17						RGMII0_RX_CTL	USB1_D7		HPS_GPIO8
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_TX_CTL					M14						RGMII0_TX_CTL			HPS_GPIO9
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_RX_CLK					D16						RGMII0_RX_CLK	USB1_CLK		HPS_GPIO10
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_RXD1					L14						RGMII0_RXD1	USB1_STP		HPS_GPIO11
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_RXD2					E15						RGMII0_RXD2	USB1_DIR		HPS_GPIO12
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_RXD3					D19						RGMII0_RXD3	USB1_NXT		HPS_GPIO13
7D	VREFB7A7B7C7D7EN0_HPS	RGMII1_TX_CLK					E16						RGMII1_TX_CLK			HPS_GPIO48
7D	VREFB7A7B7C7D7EN0_HPS	RGMII1_TXD0					D18						RGMII1_TXD0			HPS_GPIO49
7D	VREFB7A7B7C7D7EN0_HPS	RGMII1_TXD1					E19						RGMII1_TXD1			HPS_GPIO50
7D	VREFB7A7B7C7D7EN0_HPS	RGMII1_TX_CTL					H15						RGMII1_TX_CTL			HPS_GPIO51
7D	VREFB7A7B7C7D7EN0_HPS	RGMII1_RXD0					D20						RGMII1_RXD0			HPS_GPIO52
7D	VREFB7A7B7C7D7EN0_HPS	RGMII1_RXD1					H14						RGMII1_RXD1			HPS_GPIO53
7E	VREFB7A7B7C7D7EN0_HPS	RGMII1_MDIO					F16						RGMII1_MDIO	SPIM0_CLK	SPIS0_CLK	HPS_GPIO54
7E	VREFB7A7B7C7D7EN0_HPS	RGMII1_MDC					J16						RGMII1_MDC	SPIM0_MOSI	SPIS0_MOSI	HPS_GPIO55
7E	VREFB7A7B7C7D7EN0_HPS	RGMII1_TXD2					F17						RGMII1_TXD2	SPIM0_MISO	SPIS0_MISO	HPS_GPIO56
7E	VREFB7A7B7C7D7EN0_HPS	RGMII1_TXD3					H16						RGMII1_TXD3	SPIM0_SS0	SPIS0_SS0	HPS_GPIO57
7E	VREFB7A7B7C7D7EN0_HPS	RGMII1_RX_CLK					L16						RGMII1_RX_CLK	SPIS1_CLK	SPIM1_CLK	HPS_GPIO58
7E	VREFB7A7B7C7D7EN0_HPS	RGMII1_RX_CTL					R16						RGMII1_RX_CTL	SPIS1_MOSI	SPIM1_MOSI	HPS_GPIO59
7E	VREFB7A7B7C7D7EN0_HPS	RGMII1_RXD2					K16						RGMII1_RXD2	SPIS1_MISO	SPIM1_MISO	HPS_GPIO60
7E	VREFB7A7B7C7D7EN0_HPS	RGMII1_RXD3					P16						RGMII1_RXD3	SPIS1_SS0	SPIM1_SS0	HPS_GPIO61
		VCCA_FPLL					T16									
		VCCD_FPLL					T15									
		DNU					G16									
8D	VREFB8DN0	IO	CLK19p		DIFFIO_RX_T31p	DIFFOUT_T31p	M17									
8D	VREFB8DN0	IO	CLK19n		DIFFIO_RX_T31n	DIFFOUT_T31n	N17									
8D	VREFB8DN0	IO	CLK18p		DIFFIO_RX_T33p	DIFFOUT_T33p	F18									
8D	VREFB8DN0	IO	CLK18n		DIFFIO_RX_T33n	DIFFOUT_T33n	G18									
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT2,FPLL_TC_FBp,FPLL_TC_FB1		DIFFIO_RX_T35p	DIFFOUT_T35p	F19									
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT3,FPLL_TC_FBn		DIFFIO_RX_T35n	DIFFOUT_T35n	G19									
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT0,FPLL_TC_CLKOUTp,FPLL_TC_FB0		DIFFIO_TX_T36p	DIFFOUT_T36p	J17									
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT1,FPLL_TC_CLKOUTn		DIFFIO_TX_T36n	DIFFOUT_T36n	J18									
8D	VREFB8DN0	IO	CLK17p		DIFFIO_RX_T37p	DIFFOUT_T37p	H18									
8D	VREFB8DN0	IO	CLK17n		DIFFIO_RX_T37n	DIFFOUT_T37n	H19									
8D	VREFB8DN0	IO	CLK16p		DIFFIO_RX_T39p	DIFFOUT_T39p	F20									
8D	VREFB8DN0	IO	CLK16n		DIFFIO_RX_T39n	DIFFOUT_T39n	G20									
8D	VREFB8DN0	IO	VREFB8DN0				G17									
8C	VREFB8CN0	IO			DIFFIO_RX_T54p	DIFFOUT_T54p	J19	DQ1T			DQ5_8C_0	DQ5_8C_0				
8C	VREFB8CN0	IO			DIFFIO_RX_T54n	DIFFOUT_T54n	K20	DQ1T			DQ5_8C_1	DQ5_8C_1				
8C	VREFB8CN0	IO			DIFFIO_TX_T55p	DIFFOUT_T55p	P19	DQ1T			DQ5_8C_2	DQ5_8C_2				
8C	VREFB8CN0	IO			DIFFIO_RX_T56p	DIFFOUT_T56p	J20	DQ1T			DQ5_8C_3	DQ5_8C_3				
8C	VREFB8CN0	IO			DIFFIO_RX_T56n	DIFFOUT_T56n	H21	DQ1T			DQ5_8C_4	DQ5_8C_4				
8C	VREFB8CN0	IO			DIFFIO_TX_T57p	DIFFOUT_T57p	N18	DQ1T			DQ5_8C_5	DQ5_8C_5				
8C	VREFB8CN0	IO			DIFFIO_RX_T58p	DIFFOUT_T58p	D22	DQS1T/CQ1T/CQn1T/QKn1T			DQS5_8C	DQS5_8C				
8C	VREFB8CN0	IO			DIFFIO_RX_T58n	DIFFOUT_T58n	E22	DQSn1T/QK1T			DQS#5_8C	DQS#5_8C				
8C	VREFB8CN0	IO			DIFFIO_TX_T59p	DIFFOUT_T59p	M18	DQ1T			DM5_8C	DM5_8C				
8C	VREFB8CN0	IO			DIFFIO_RX_T60p	DIFFOUT_T60p	A29	DQ1T			DQ5_8C_6	DQ5_8C_6				
8C	VREFB8CN0	IO			DIFFIO_RX_T60n	DIFFOUT_T60n	B30	DQ1T			DQ5_8C_7	DQ5_8C_7				
8C	VREFB8CN0	IO			DIFFIO_TX_T61p	DIFFOUT_T61p	L18	DQ1T			DQ5_8C_8	DQ5_8C_8				
8C	VREFB8CN0	IO			DIFFIO_RX_T62p	DIFFOUT_T62p	C23	DQ2T	DQ1T	DQ1T	DQ4_8C_0	DQ4_8C_0				
8C	VREFB8CN0	IO			DIFFIO_RX_T62n	DIFFOUT_T62n	D23	DQ2T	DQ1T	DQ1T	DQ4_8C_1	DQ4_8C_1				
8C	VREFB8CN0	IO					K19	DQ2T	DQ1T	DQ1T	DQ4_8C_2	DQ4_8C_2				
8C	VREFB8CN0	IO	VREFB8CN0				K18									
8C	VREFB8CN0	IO			DIFFIO_RX_T63p	DIFFOUT_T63p	A28	DQ2T	DQ1T	DQ1T	DQ4_8C_3	DQ4_8C_3				
8C	VREFB8CN0	IO			DIFFIO_RX_T63n	DIFFOUT_T63n	B28	DQ2T	DQ1T	DQ1T	DQ4_8C_4	DQ4_8C_4				
8C	VREFB8CN0	IO			DIFFIO_TX_T64p	DIFFOUT_T64p	M19	DQ2T	DQ1T	DQ1T	DQ4_8C_5	DQ4_8C_5				
8C	VREFB8CN0	IO			DIFFIO_RX_T65p	DIFFOUT_T65p	D24	DQS2T/CQ2T/CQn2T/QKn2T	DQS1T/CQ1T/CQn1T/QKn1T	DQ1T	DQS4_8C	DQS4_8C				
8C	VREFB8CN0	IO			DIFFIO_RX_T65n	DIFFOUT_T65n	E24	DQSn2T/QK2T	DQSn1T/QK1T	DQ1T	DQS#4_8C	DQS#4_8C				
8C	VREFB8CN0	IO			DIFFIO_TX_T66p	DIFFOUT_T66p	N19	DQ2T	DQ1T	DQ1T	DM4_8C	DM4_8C				
8C	VREFB8CN0	IO			DIFFIO_RX_T67p	DIFFOUT_T67p	B27	DQ2T	DQ1T	DQ1T	DQ4_8C_6	DQ4_8C_6				
8C	VREFB8CN0	IO			DIFFIO_RX_T67n	DIFFOUT_T67n	C27	DQ2T	DQ1T	DQ1T	DQ4_8C_7	DQ4_8C_7				
8C	VREFB8CN0	IO			DIFFIO_TX_T68p	DIFFOUT_T68p	A26	DQ2T	DQ1T	DQ1T	DQ4_8C_8	DQ4_8C_8				
8C	VREFB8CN0	IO			DIFFIO_TX_T68n	DIFFOUT_T68n	A27									
8C	VREFB8CN0	IO			DIFFIO_RX_T69p	DIFFOUT_T69p	F21	DQ3T	DQ1T	DQ1T	DQ3_8C_0	DQ3_8C_0				
8C	VREFB8CN0	IO			DIFFIO_RX_T69n	DIFFOUT_T69n	G21	DQ3T	DQ1T	DQ1T	DQ3_8C_1	DQ3_8C_1				
8C	VREFB8CN0	IO			DIFFIO_TX_T70p	DIFFOUT_T70p	M20	DQ3T	DQ1T	DQ1T	DQ3_8C_2	DQ3_8C_2				
8C	VREFB8CN0	IO			DIFFIO_RX_T71p	DIFFOUT_T71p	C26	DQ3T	DQ1T	DQ1T	DQ3_8C_3	DQ3_8C_3				
8C	VREFB8CN0	IO			DIFFIO_RX_T71n	DIFFOUT_T71n	D26	DQ3T	DQ1T	DQ1T	DQ3_8C_4	DQ3_8C_4				
8C	VREFB8CN0	IO			DIFFIO_TX_T72p	DIFFOUT_T72p	N20	DQ3T	DQ1T	DQ1T	DQ3_8C_5	DQ3_8C_5				
8C	VREFB8CN0	IO			DIFFIO_RX_T73p	DIFFOUT_T73p	F22	DQS3T/CQ3T/CQn3T/QKn3T	DQ1T	DQS1T/CQ1T/CQn1T/QKn1T	DQS3_8C	DQS3_8C				
8C	VREFB8CN0	IO			DIFFIO_RX_T73n	DIFFOUT_T73n	G22	DQSn3T/QK3T	DQ1T	DQSn1T/QK1T	DQS#3_8C	DQS#3_8C				
8C	VREFB8CN0	IO			DIFFIO_TX_T74p	DIFFOUT_T74p	L21	DQ3T	DQ1T	DQ1T	DM3_8C	DM3_8C				
8C	VREFB8CN0	IO			DIFFIO_RX_T75p	DIFFOUT_T75p	C24	DQ3T	DQ1T	DQ1T	DQ3_8C_6	DQ3_8C_6				
8C	VREFB8CN0	IO			DIFFIO_RX_T75n	DIFFOUT_T75n	C25	DQ3T	DQ1T	DQ1T	DQ3_8C_7	DQ3_8C_7				

Copyright © 2016 Altera Corp.

Bank Number	VREF	PinName/Function *(2), (3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
8C	VREF8CN0	IO			DIFFIO_TX_T76p	DIFFOUT_T76p	K21	DQ3T	DQ1T	DQ1T	DQ3_8C_8	DQ3_8C_8				
8B	VREF8BN0	IO			DIFFIO_RX_T77p	DIFFOUT_T77p	K22	DQ4T	DQ2T	DQ1T	DQ2_8B_0	DQ2_8B_0				
8B	VREF8BN0	IO			DIFFIO_RX_T77n	DIFFOUT_T77n	J22	DQ4T	DQ2T	DQ1T	DQ2_8B_1	DQ2_8B_1				
8B	VREF8BN0	IO			DIFFIO_TX_T78p	DIFFOUT_T78p	G23	DQ4T	DQ2T	DQ1T	DQ2_8B_2	DQ2_8B_2				
8B	VREF8BN0	IO			DIFFIO_RX_T79p	DIFFOUT_T79p	M22	DQ4T	DQ2T	DQ1T	DQ2_8B_3	DQ2_8B_3				
8B	VREF8BN0	IO			DIFFIO_RX_T79n	DIFFOUT_T79n	L22	DQ4T	DQ2T	DQ1T	DQ2_8B_4	DQ2_8B_4				
8B	VREF8BN0	IO			DIFFIO_TX_T80p	DIFFOUT_T80p	J23	DQ4T	DQ2T	DQ1T	DQ2_8B_5	DQ2_8B_5				
8B	VREF8BN0	IO			DIFFIO_RX_T81p	DIFFOUT_T81p	E25	DQS4T/CQ4T/CQn4T/QKn4T	DQS2T/CQ2T/CQn2T/QKn2T	DQ1T	DQS2_8B	DQS2_8B				
8B	VREF8BN0	IO			DIFFIO_RX_T81n	DIFFOUT_T81n	F24	DQSn4T/QK4T	DQSn2T/QK2T	DQ1T	DQS#2_8B	DQS#2_8B				
8B	VREF8BN0	IO			DIFFIO_TX_T82p	DIFFOUT_T82p	H24	DQ4T	DQ2T	DQ1T	DM2_8B	DM2_8B				
8B	VREF8BN0	IO			DIFFIO_RX_T83p	DIFFOUT_T83p	N21	DQ4T	DQ2T	DQ1T	DQ2_8B_6	DQ2_8B_6				
8B	VREF8BN0	IO			DIFFIO_RX_T83n	DIFFOUT_T83n	M21	DQ4T	DQ2T	DQ1T	DQ2_8B_7	DQ2_8B_7				
8B	VREF8BN0	IO			DIFFIO_TX_T84p	DIFFOUT_T84p	K24	DQ4T	DQ2T	DQ1T	DQ2_8B_8	DQ2_8B_8				
8B	VREF8BN0	IO			DIFFIO_RX_T85p	DIFFOUT_T85p	F26	DQ5T	DQ2T	DQ1T	DQ1_8B_0	DQ1_8B_0				
8B	VREF8BN0	IO			DIFFIO_RX_T85n	DIFFOUT_T85n	F27	DQ5T	DQ2T	DQ1T	DQ1_8B_1	DQ1_8B_1				
8B	VREF8BN0	IO					J24	DQ5T	DQ2T	DQ1T	DQ1_8B_2	DQ1_8B_2				
8B	VREF8BN0	IO	VREF8BN0				H22									
8B	VREF8BN0	IO			DIFFIO_RX_T86p	DIFFOUT_T86p	D27	DQ5T	DQ2T	DQ1T	DQ1_8B_3	DQ1_8B_3				
8B	VREF8BN0	IO			DIFFIO_RX_T86n	DIFFOUT_T86n	D28	DQ5T	DQ2T	DQ1T	DQ1_8B_4	DQ1_8B_4				
8B	VREF8BN0	IO			DIFFIO_TX_T87p	DIFFOUT_T87p	K25	DQ5T	DQ2T	DQ1T	DQ1_8B_5	DQ1_8B_5				
8B	VREF8BN0	IO			DIFFIO_TX_T87n	DIFFOUT_T87n	L24									
8B	VREF8BN0	IO			DIFFIO_RX_T88p	DIFFOUT_T88p	C28	DQS5T/CQ5T/CQn5T/QKn5T	DQ2T	DQ1T	DQS1_8B	DQS1_8B				
8B	VREF8BN0	IO			DIFFIO_RX_T88n	DIFFOUT_T88n	C29	DQSn5T/QK5T	DQ2T	DQ1T	DQS#1_8B	DQS#1_8B				
8B	VREF8BN0	IO			DIFFIO_TX_T89p	DIFFOUT_T89p	G24	DQ5T	DQ2T	DQ1T	DM1_8B	DM1_8B				
8B	VREF8BN0	IO			DIFFIO_TX_T89n	DIFFOUT_T89n	G25									
8B	VREF8BN0	IO			DIFFIO_RX_T90p	DIFFOUT_T90p	P21	DQ5T	DQ2T	DQ1T	DQ1_8B_6	DQ1_8B_6				
8B	VREF8BN0	IO			DIFFIO_RX_T90n	DIFFOUT_T90n	N22	DQ5T	DQ2T	DQ1T	DQ1_8B_7	DQ1_8B_7				
8B	VREF8BN0	IO			DIFFIO_TX_T91p	DIFFOUT_T91p	D30	DQ5T	DQ2T	DQ1T	DQ1_8B_8	DQ1_8B_8				
8B	VREF8BN0	IO			DIFFIO_TX_T91n	DIFFOUT_T91n	C30				RESET#_8A					
8A	VREF8AN0	IO			DIFFIO_RX_T92p	DIFFOUT_T92p	E28	DQ6T	DQ3T		CK_8A	CK_8A				
8A	VREF8AN0	IO			DIFFIO_RX_T92n	DIFFOUT_T92n	D29	DQ6T	DQ3T		CK#_8A	CK#_8A				
8A	VREF8AN0	IO			DIFFIO_TX_T93p	DIFFOUT_T93p	G26	DQ6T	DQ3T		CKE_8A_0	CKE_8A_0				
8A	VREF8AN0	IO			DIFFIO_TX_T93n	DIFFOUT_T93n	G27				CKE_8A_1	CKE_8A_1				
8A	VREF8AN0	IO			DIFFIO_RX_T94p	DIFFOUT_T94p	F30	DQ6T	DQ3T		A_8A_0	CA_8A_0				
8A	VREF8AN0	IO			DIFFIO_RX_T94n	DIFFOUT_T94n	E30	DQ6T	DQ3T		A_8A_1	CA_8A_1				
8A	VREF8AN0	IO			DIFFIO_TX_T95p	DIFFOUT_T95p	G29	DQ6T	DQ3T		A_8A_2	CA_8A_2				
8A	VREF8AN0	IO			DIFFIO_TX_T95n	DIFFOUT_T95n	G30				A_8A_3	CA_8A_3				
8A	VREF8AN0	IO			DIFFIO_RX_T96p	DIFFOUT_T96p	G28	DQS6T/CQ6T/CQn6T/QKn6T	DQS3T/CQ3T/CQn3T/QKn3T		A_8A_4	CA_8A_4				
8A	VREF8AN0	IO			DIFFIO_RX_T96n	DIFFOUT_T96n	F28	DQSn6T/QK6T	DQSn3T/QK3T		A_8A_5	CA_8A_5				
8A	VREF8AN0	IO			DIFFIO_TX_T97p	DIFFOUT_T97p	H27	DQ6T	DQ3T		A_8A_6	CA_8A_6				
8A	VREF8AN0	IO			DIFFIO_TX_T97n	DIFFOUT_T97n	H28				A_8A_7	CA_8A_7				
8A	VREF8AN0	IO			DIFFIO_RX_T98p	DIFFOUT_T98p	J30	DQ6T	DQ3T		A_8A_8	CA_8A_8				
8A	VREF8AN0	IO			DIFFIO_RX_T98n	DIFFOUT_T98n	H30	DQ6T	DQ3T		A_8A_9	CA_8A_9				
8A	VREF8AN0	IO			DIFFIO_TX_T99p	DIFFOUT_T99p	K28	DQ6T	DQ3T		A_8A_10					
8A	VREF8AN0	IO			DIFFIO_TX_T99n	DIFFOUT_T99n	J28				A_8A_11					
8A	VREF8AN0	IO			DIFFIO_RX_T100p	DIFFOUT_T100p	L30	DQ7T	DQ3T		A_8A_12					
8A	VREF8AN0	IO			DIFFIO_RX_T100n	DIFFOUT_T100n	K30	DQ7T	DQ3T		A_8A_13					
8A	VREF8AN0	IO			DIFFIO_TX_T101p	DIFFOUT_T101p	M27	DQ7T	DQ3T		A_8A_14					
8A	VREF8AN0	IO			DIFFIO_TX_T101n	DIFFOUT_T101n	L27				A_8A_15					
8A	VREF8AN0	IO			DIFFIO_RX_T102p	DIFFOUT_T102p	L28	DQ7T	DQ3T		BA_8A_0					
8A	VREF8AN0	IO			DIFFIO_RX_T102n	DIFFOUT_T102n	K29	DQ7T	DQ3T		BA_8A_1					
8A	VREF8AN0	IO			DIFFIO_TX_T103p	DIFFOUT_T103p	N30	DQ7T	DQ3T		BA_8A_2					
8A	VREF8AN0	IO			DIFFIO_TX_T103n	DIFFOUT_T103n	M30				RAS#_8A					
8A	VREF8AN0	IO			DIFFIO_RX_T104p	DIFFOUT_T104p	T24	DQS7T/CQ7T/CQn7T/QKn7T	DQ3T		CAS#_8A					
8A	VREF8AN0	IO			DIFFIO_RX_T104n	DIFFOUT_T104n	T23	DQSn7T/QK7T	DQ3T		WE#_8A					
8A	VREF8AN0	IO			DIFFIO_TX_T105p	DIFFOUT_T105p	K26	DQ7T	DQ3T		ODT_8A_0	ODT_8A_0				
8A	VREF8AN0	IO			DIFFIO_TX_T105n	DIFFOUT_T105n	K27				ODT_8A_1	ODT_8A_1				
8A	VREF8AN0	IO	CLK23p		DIFFIO_RX_T106p	DIFFOUT_T106p	P30	DQ7T	DQ3T							
8A	VREF8AN0	IO	CLK23n		DIFFIO_RX_T106n	DIFFOUT_T106n	N29	DQ7T	DQ3T							
8A	VREF8AN0	IO			DIFFIO_TX_T107p	DIFFOUT_T107p	R22	DQ7T	DQ3T		CS#_8A_0	CS#_8A_0				
8A	VREF8AN0	IO			DIFFIO_TX_T107n	DIFFOUT_T107n	R23				CS#_8A_1	CS#_8A_1				
8A	VREF8AN0	IO	CLK22p		DIFFIO_RX_T108p	DIFFOUT_T108p	R28									
8A	VREF8AN0	IO	CLK22n		DIFFIO_RX_T108n	DIFFOUT_T108n	P28									
8A	VREF8AN0	IO	VREF8AN0				J26									
8A	VREF8AN0	IO	FPLL_TL_CLKOUT2,FPLL_TL_FBp,FPLL_TL_FB1		DIFFIO_RX_T109p	DIFFOUT_T109p	N28									
8A	VREF8AN0	IO	FPLL_TL_CLKOUT3,FPLL_TL_FBn		DIFFIO_RX_T109n	DIFFOUT_T109n	M28									
8A	VREF8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB0		DIFFIO_TX_T110p	DIFFOUT_T110p	T25									
8A	VREF8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T110n	DIFFOUT_T110n	R26									
8A	VREF8AN0	IO	CLK21p		DIFFIO_RX_T111p	DIFFOUT_T111p	R27									
8A	VREF8AN0	IO	CLK21n		DIFFIO_RX_T111n	DIFFOUT_T111n	P27									
8A	VREF8AN0	IO	CLK20p		DIFFIO_RX_T113p	DIFFOUT_T113p	P25									
8A	VREF8AN0	IO	CLK20n		DIFFIO_RX_T113n	DIFFOUT_T113n	R25									
8A	VREF8AN0	IO	RZQ_6		DIFFIO_TX_T114n	DIFFOUT_T114n	J25									
8A		MSEL0		MSEL0			P24									
8A		MSEL1		MSEL1			N26									
8A		MSEL2		MSEL2			M25									
8A		MSEL3		MSEL3			L25									
8A		MSEL4		MSEL4			N23									
8A		CONF_DONE		CONF_DONE			N25									
8A		nSTATUS		nSTATUS			M26									
8A		nCE		nCE			M24									
8A		nCONFIG		nCONFIG			M23									
		GND					T26									
		VCC_HPS					W11									
		GND					W10									
		GND					AA24									
		GND					AA29									
		GND					AA30									
		GND					AB22									
		GND					AB23									
		GND					AB24									
		GND					AB25									
		GND					AB26									
		GND					AB27									
		GND					AB28									
		GND					AC26									
		GND					AC29									
		GND					AC30									
		GND					AD27									
		GND					AD28									
		GND					AE26									
		GND					AE29									
		GND					AE30									
		GND					AF27									
		GND					AF28									
		GND					AG26									
		GND					AG29									
		GND					AG30									
		GND					AH27									
		GND					AH28									
		GND					AJ29									
		GND					AJ30									
		GND					R30									
		GND					T27									
		GND					T28									
		GND					U22									
		GND					U23									

Copyright © 2016 Altera Corp.

Bank Number	VREF	PinName/Function *(2), (3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					U24									
		GND					U25									
		GND					U26									
		GND					U29									
		GND					U30									
		GND					V23									
		GND					V27									
		GND					V28									
		GND					W24									
		GND					W29									
		GND					W30									
		GND					Y23									
		GND					Y25									
		GND					Y26									
		GND					Y27									
		GND					Y28									
		GND					AA1									
		GND					AA2									
		GND					AA7									
		GND					AB3									
		GND					AB4									
		GND					AB5									
		GND					AB6									
		GND					AC1									
		GND					AC2									
		GND					AC5									
		GND					AD3									
		GND					AD4									
		GND					AE1									
		GND					AE2									
		GND					AE5									
		GND					AF3									
		GND					AF4									
		GND					AG1									
		GND					AG2									
		GND					AG5									
		GND					AH3									
		GND					AH4									
		GND					AJ1									
		GND					AJ2									
		GND					T3									
		GND					T4									
		GND					U1									
		GND					U2									
		GND					U5									
		GND					U6									
		GND					V3									
		GND					V4									
		GND					V8									
		GND					W1									
		GND					W2									
		GND					W5									
		GND					W7									
		GND					Y3									
		GND					Y4									
		GND					Y6									
		GND					Y8									
		VCCP					AB10									
		VCCP					AB14									
		VCCP					AB17									
		VCCP					AB20									
		VCCP					AC19									
		VCCP					P10									
		VCCP					R17									
		VCCP					R21									
		VCCP					T10									
		VCCA_FPLL					V9									
		VCCA_FPLL					V22									
		VCCPLL_HPS					U10									
		VCCBAT					H25									
		VCC_AUX					AB11									
		VCC_AUX					AB18									
		VCC_AUX					R20									
		VCC_AUX_SHARED					R13									
		VCCD_FPLL					Y9									
		VCCD_FPLL					Y22									
		VCCA_GXBR0					W6									
		VCCA_GXBL1					W26									
		VCCH_GXBR0					V7									
		VCCH_GXBL1					V24									
		VCCL_GXBR0					V5									
		VCCL_GXBR0					V6									
		VCCL_GXBL1					V25									
		VCCL_GXBL1					V26									
		VCCR_GXBL					AA25									
		VCCR_GXBL					AA26									
		VCCR_GXBR					AA5									
		VCCR_GXBR					AA6									
		VCCT_GXBR0					Y5									
		VCCT_GXBR0					Y7									
		VCCT_GXBL1					W25									
		VCCT_GXBL1					Y24									
		VCC					AA10									
		VCC					AA12									
		VCC					AA14									
		VCC					AA16									
		VCC					AA18									
		VCC					AA19									
		VCC					AA20									
		VCC					T17									
		VCC					T19									
		VCC					T21									
		VCC					T22									
		VCC					U16									
		VCC					U18									
		VCC					U20									
		VCC					V15									
		VCC					V17									
		VCC					V19									
		VCC					V21									
		VCC					W12									
		VCC					W14									
		VCC					W18									
		VCC					W20									
		VCC					Y11									
		VCC					Y13									
		VCC					Y15									

Copyright © 2016 Altera Corp.

Bank Number	VREF	PinName/Function *(2), (3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCC					Y16									
		VCC					Y17									
		VCC					Y19									
		VCC					Y21									
		VCC					W16									
		VCC_HPS					R12									
		VCC_HPS					T11									
		VCC_HPS					T13									
		VCC_HPS					U12									
		VCC_HPS					U13									
		VCC_HPS					U14									
		VCC_HPS					V11									
		VCC_HPS					V13									
		VCCIO3A					AE19									
		VCCIO3A					AE22									
		VCCIO3A					AF26									
		VCCIO3A					AH19									
		VCCIO3A					AH22									
		VCCIO3A					AH26									
		VCCIO3B					AE13									
		VCCIO3B					AE16									
		VCCIO3B					AH15									
		VCCIO3D					AE11									
		VCCIO3D					AG13									
		VCCIO4A					AD5									
		VCCIO4A					AE7									
		VCCIO4A					AF5									
		VCCIO4A					AH5									
		VCCIO4A					AH7									
		VCCIO6A_HPS					C2									
		VCCIO6A_HPS					C5									
		VCCIO6A_HPS					C8									
		VCCIO6A_HPS					F2									
		VCCIO6A_HPS					F4									
		VCCIO6A_HPS					F6									
		VCCIO6A_HPS					H1									
		VCCIO6A_HPS					J5									
		VCCIO6B_HPS					L6									
		VCCIO6B_HPS					M4									
		VCCIO6B_HPS					N1									
		VCCIO6B_HPS					P6									
		VCCIO6B_HPS					T2									
		VCCIO6B_HPS					T5									
		VCCIO7A_HPS					B14									
		VCCIO7A_HPS					B17									
		VCCIO7A_HPS					G10									
		VCCIO7A_HPS					M10									
		VCCIO7B_HPS					B20									
		VCCIO7B_HPS					E12									
		VCCIO7C_HPS					E14									
		VCCIO7D_HPS					E18									
		VCCIO7D_HPS					J14									
		VCCIO7E_HPS					G15									
		VCCIO8A					F29									
		VCCIO8A					J27									
		VCCIO8A					J29									
		VCCIO8A					M29									
		VCCIO8A					N24									
		VCCIO8A					N27									
		VCCIO8B					E27									
		VCCIO8B					F25									
		VCCIO8B					K23									
		VCCIO8C					D25									
		VCCIO8C					F23									
		VCCIO8C					J21									
		VCCIO8C					L19									
		VCCIO8D					E21									
		VCCIO8D					K17									
		VCCPD3					AB21									
		VCCPD3					AC18									
		VCCPD3					AC24									
		VCCPD4A					AB7									
		VCCPD6A6B_HPS					M8									
		VCCPD6A6B_HPS					N8									
		VCCPD6A6B_HPS					R8									
		VCCPD6A6B_HPS					U8									
		VCCPD7A_HPS					N11									
		VCCPD7B_HPS					L12									
		VCCPD7C_HPS					M13									
		VCCPD7D_HPS					M16									
		VCCPD7E_HPS					J15									
		VCCPD8					P18									
		VCCPD8					P22									
		VCCPD8					R19									
		VCCPD8					R24									
		VCCPGM					F12									
		VCCPGM					AD26									
		VCCRSTCLK_HPS					G9									
		VCC_HPS					R10									
		VCC_HPS					R11									
		VCC_HPS					R14									
		VCC_HPS					R15									
	VREFB7A7B7C7D7EN0_HPS	VREFB7A7B7C7D7EN0_HPS					F14									
		GND					AA11									
		GND					AA13									
		GND					AA15									
		GND					AA17									
		GND					AA21									
		GND					AB19									
		GND					AB8									
		GND					AB9									
		GND					AC11									
		GND					AC14									
		GND					AC17									
		GND					AC20									
		GND					AC23									
		GND					AD8									
		GND					AF11									
		GND					AF14									
		GND					AF17									
		GND					AF20									
		GND					AF23									
		GND					AF8									
		GND					AJ11									
		GND					AJ14									
		GND					AJ17									
		GND					AJ20									

Copyright © 2016 Altera Corp.

Bank Number	VREF	PinName/Function *(2), (3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					AJ23									
		GND					AJ26									
		GND					AJ5									
		GND					AJ8									
		GND					B11									
		GND					B2									
		GND					B23									
		GND					B26									
		GND					B29									
		GND					B5									
		GND					B8									
		GND					E17									
		GND					E2									
		GND					E20									
		GND					E23									
		GND					E26									
		GND					E29									
		GND					E5									
		GND					E8									
		GND					G12									
		GND					G14									
		GND					H17									
		GND					H2									
		GND					H20									
		GND					H23									
		GND					H26									
		GND					H29									
		GND					H5									
		GND					H8									
		GND					K11									
		GND					K14									
		GND					L17									
		GND					L2									
		GND					L20									
		GND					L23									
		GND					L26									
		GND					L29									
		GND					L5									
		GND					L8									
		GND					N10									
		GND					N14									
		GND					P11									
		GND					P17									
		GND					V16									
		GND					P2									
		GND					P20									
		GND					P23									
		GND					P26									
		GND					P29									
		GND					P5									
		GND					P8									
		GND					R18									
		GND					T12									
		GND					T14									
		GND					T18									
		GND					T20									
		GND					U11									
		GND					U15									
		GND					U17									
		GND					U19									
		GND					U21									
		GND					U7									
		GND					V10									
		GND					V12									
		GND					V14									
		GND					V18									
		GND					V20									
		GND					Y14									
		GND					W13									
		GND					W15									
		GND					W17									
		GND					W19									
		GND					W21									
		GND					Y10									
		GND					Y12									
		GND					Y18									
		GND					Y20									

Notes:
(1) For more information about pin definitions and pin connection guidelines, refer to the
Arria V Device Family Pin Connection Guidelines.
(2) GXB_REFCLK pin is not supported in current Quartus II version, but will be supported in future Quartus II release version.
(3) Pins with * contains similar name with other pins in the same column. For the selection of the HPS pins, refer to the "HPS Pin Mux Select x" columns.
(4) Pins with * are the 10 Gbps transceiver channels. For more information about the 10 Gbps transceiver channels clocking recommendation, refer to the
Transceiver Clocking in Arria V Devices chapter.
(5) RESET pin is only applicable for DDR3 device.

Copyright © 2016 Altera Corp.

Version Number	Date	Changes Made
1.0	4/19/2013	Initial release.
1.1	9/30/2014	Remove corresponding bank number from VCCRSTCLK_HPS pin.
1.2	7/31/2015	Renamed the following columns: - Renamed "DDR3/DDR2 hard memory PHY" to "HMC pin assignment for DDR3". - Renamed "LPDDR2 hard memory PHY" to "HMC pin assignment for LPDDR2".
1.3	12/23/2016	-Renamed SDMMC_FB_CLK_IN to HPS_GPIO44.

Copyright © 2016 Altera Corp.