

Checklist of Design Considerations for SoC FPGAs

Here are several key items to consider when selecting an SoC FPGA:

System Performance

- CPU clock rate
- Non-blocking L3 interconnect
- Processor-to-FPGA interconnect bandwidth
- Low latency processor-to-FPGA interconnect bandwidth
- FPGA-to-processor interconnect bandwidth
- FPGA-to-DDR interconnect bandwidth
- Smart memory controller for maximum throughput with lower power memory
- All hosts (FPGA and HPS) can share memory coherently with the processor
- Multiple hardened DDR controllers in FPGA

Reliability

- Error correction code (ECC) protection throughout processor system
 - L2 cache
 - On-chip RAM
 - Flash I/F
 - Hard processor system (HPS) peripherals
- ECC protection on 8, 16, and 32 bit external memory interface
- Shared memory protection for multiple hosts
 - Address range protection per port and per host
- "Fail-safe" recovery mechanism for both physical and logical boot defects
- No power-off sequencing requirement

Flexibility

- Multiple boot/configuration options
 - Processor first
 - FPGA first
 - Processor and FPGA independently
- FPGA density range
- Transceivers available in all devices
- Integrated PCIe interface available in all devices
- Maximum addressable main memory address space
- Multiple hardened DDR controllers in FPGA
- Finer control over DDR port priorities
- Multiple on-chip FPGA interfaces (AXI, Avalon® memory-mapped, Avalon streaming)
- Can use multiple flash devices (e.g. quad SPI + NAND)
- Larger quad serial peripheral interface (SPI) device support (multiple images)
- Hardware ECC for NAND flash
- Direct memory access (DMA) request interfaces for FPGA and HPS peripherals
- Coherent memory access for FPGA and HPS peripherals
- CPU reset does not force FPGA reconfiguration
- More processor and system trace options
- No need to add power-off sequencing circuitry
- Horizontal and vertical package migration within SoC FPGAs

System Cost

- Component cost savings from processor/digital signal processor (DSP)/FPGA integration into single chip
- Single- or dual-core processor option
- Number/type of peripherals integrated in HPS
- Shared memory between processor and FPGA for lower memory component cost
- Integrated phase-locked loops (PLLs) for fewer external oscillators
- Transceivers available in all devices
- Integrated PCIe interface available in all devices
- Number of power rails
- No need to add power-off sequencing circuitry
- Board space, routing, and trace savings from integrated device
- Horizontal and vertical package migration within SoC FPGAs for common platform

Power Consumption

- Component power savings from processor/DSP/FPGA integration into a single chip
- System memory power savings from using smart memory controller
- FPGA power down option
- Number of power rails
- Power supply efficiency and power consumption
- Shared memory between processor and FPGA for lower system memory power

Future Roadmap

- Vendor investment in SoC FPGA product line
- Vendor engineering team background and SoC experience
- Processor technology innovations
- FPGA technology innovations
- Development tools roadmap
- Typical product longevity

Development Tools

- Arm compatibility
- Software development environment (e.g. Eclipse)
- Compiler support
 - Hardware vector floating point (VFP) and Arm Neon support
- Operating system board support packages
- Optimized multi core debugging
- FPGA-adaptive debugging
- Arm CoreSight Compliant processor-FPGA cross-triggering
 - System Trace Macrocell (STM)
 - Global timestamping
- Single cable for in-system debug
- Trace buffer size
- Non-intrusive code profiling
- FPGA logic analyzer