



Bank Number	VREF	PinName/Function (3) (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DORS (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
3D	VREFB3D0	IO		CLK5n	DIFFIO_RX_B78n	DIFFOUT_B78n	AH12									
3D	VREFB3D0	IO		CLK5p	DIFFIO_RX_B79p	DIFFOUT_B79p	AJ12									
3D	VREFB3D0	IO			FPLL_BC_CLKOUT1_FPLL_BC_CLKOUT1	DIFFIO_TX_B79n	DIFFOUT_B79n	AB12								
3D	VREFB3D0	IO			FPLL_BC_CLKOUT0_FPLL_BC_CLKOUT0	DIFFIO_TX_B79p	DIFFOUT_B79p	AC12								
3D	VREFB3D0	IO			FPLL_BC_CLKOUT3_FPLL_BC_F80	DIFFIO_RX_B80n	DIFFOUT_B80n	AH13								
3D	VREFB3D0	IO			FPLL_BC_CLKOUT2_FPLL_BC_F80	DIFFIO_RX_B80p	DIFFOUT_B80p	AG12								
3D	VREFB3D0	IO		CLK6n	DIFFIO_RX_B82n	DIFFOUT_B82n	AP13									
3D	VREFB3D0	IO		CLK6p	DIFFIO_RX_B82p	DIFFOUT_B82p	AP12									
3D	VREFB3D0	IO		CLK7n	DIFFIO_RX_B84n	DIFFOUT_B84n	AD12									
3D	VREFB3D0	IO		CLK7p	DIFFIO_RX_B84p	DIFFOUT_B84p	AD11									
				VCC2_FPLL			AB15									
				VCCA_FPLL			AB16									
				DNJ			AC16									
4A	VREFB4A0	IO		DATA10	DIFFIO_TX_B140p	DIFFOUT_B140p	AC10	DQ58								
4A	VREFB4A0	IO		DATA11	DIFFIO_RX_B147n	DIFFOUT_B147n	AE10	DQ58								
4A	VREFB4A0	IO		DATA5	DIFFIO_RX_B147p	DIFFOUT_B147p	AF10	DQ58								
4A	VREFB4A0	IO		DATA6	DIFFIO_TX_B149p	DIFFOUT_B149p	AD10	DQ58								
4A	VREFB4A0	IO		DATA12	DIFFIO_TX_B149n	DIFFOUT_B149n	AG11	DQS58B/QK58								
4A	VREFB4A0	IO		DATA13	DIFFIO_RX_B149p	DIFFOUT_B149p	AH11	DQS58C/QK58C/QK58B								
4A	VREFB4A0	IO		DATA7	DIFFIO_TX_B150n	DIFFOUT_B150n	AK12	DQ58								
4A	VREFB4A0	IO		DATA8	DIFFIO_TX_B150p	DIFFOUT_B150p	AK11	DQ58								
4A	VREFB4A0	IO		DATA14	DIFFIO_RX_B151n	DIFFOUT_B151n	AG10	DQ58								
4A	VREFB4A0	IO		DATA15	DIFFIO_RX_B151p	DIFFOUT_B151p	AH10	DQ58								
4A	VREFB4A0	IO		DATA9	DIFFIO_TX_B152n	DIFFOUT_B152n	AE9	DQ58								
4A	VREFB4A0	IO		CLKUSR	DIFFIO_TX_B152p	DIFFOUT_B152p	AF9	DQ58								
4A	VREFB4A0	IO			DIFFIO_RX_B153n	DIFFOUT_B153n	AK10	DQ58								
4A	VREFB4A0	IO			DIFFIO_RX_B153p	DIFFOUT_B153p	AK9	DQ58								
4A	VREFB4A0	IO		PR_ERROR	DIFFIO_TX_B154n	DIFFOUT_B154n	AJ10	DQ58								
4A	VREFB4A0	IO		PR_READY	DIFFIO_TX_B154p	DIFFOUT_B154p	AJ9	DQ58								
4A	VREFB4A0	IO		PR_DONE	DIFFIO_RX_B155n	DIFFOUT_B155n	AG9	DQ58								
4A	VREFB4A0	IO		PR_REQUEST	DIFFIO_RX_B155p	DIFFOUT_B155p	AH9	DQ58								
4A	VREFB4A0	IO		PERSTR0	DIFFIO_TX_B156n	DIFFOUT_B156n	AD9	DQ58								
4A	VREFB4A0	IO			DIFFIO_TX_B156p	DIFFOUT_B156p	AC8	DQ58								
4A	VREFB4A0	IO		CLP_CONF_DONE	DIFFIO_RX_B157n	DIFFOUT_B157n	AK8	DQS58B/QK58B								
4A	VREFB4A0	IO		CRC_ERROR	DIFFIO_TX_B157p	DIFFOUT_B157p	AK7	DQS58C/QK58C/QK58A								
4A	VREFB4A0	IO		DEV_DE	DIFFIO_TX_B158n	DIFFOUT_B158n	AK6	DQ58								
4A	VREFB4A0	IO		DEV_CLRn	DIFFIO_TX_B158p	DIFFOUT_B158p	AK5	DQ58								
4A	VREFB4A0	IO		INT_DONE	DIFFIO_RX_B159n	DIFFOUT_B159n	AG8	DQ58								
4A	VREFB4A0	IO		ICE0	DIFFIO_RX_B159p	DIFFOUT_B159p	AH8	DQ58								
4A	VREFB4A0	IO		VREFB4A0			AC9	DQ58								
4A	VREFB4A0	IO					AE8	DQ58								
4A	VREFB4A0	IO		CLK11n	DIFFIO_RX_B160n	DIFFOUT_B160n	AJ4	DQ58								
4A	VREFB4A0	IO		CLK11p	DIFFIO_RX_B160p	DIFFOUT_B160p	AK4	DQ58								
4A	VREFB4A0	IO			FPLL_BR_CLKOUT1_FPLL_BR_CLKOUT1	DIFFIO_TX_B161n	DIFFOUT_B161n	AJ7								
4A	VREFB4A0	IO			FPLL_BR_CLKOUT0_FPLL_BR_CLKOUT0	DIFFIO_TX_B161p	DIFFOUT_B161p	AJ6								
4A	VREFB4A0	IO			FPLL_BR_CLKOUT3_FPLL_BR_F80	DIFFIO_RX_B162n	DIFFOUT_B162n	AG6								
4A	VREFB4A0	IO			FPLL_BR_CLKOUT2_FPLL_BR_F80	DIFFIO_RX_B162p	DIFFOUT_B162p	AG5								
4A	VREFB4A0	IO			FPLL_BR_CLKOUT2_FPLL_BR_F80_FPLL_BR_FB1	DIFFIO_RX_B162p	DIFFOUT_B162p	AH6								
4A	VREFB4A0	IO		CLK10n	DIFFIO_TX_B164n	DIFFOUT_B164n	AZ7									
4A	VREFB4A0	IO		CLK10p	DIFFIO_RX_B164p	DIFFOUT_B164p	AG7									
4A	VREFB4A0	IO		CLK9n	DIFFIO_RX_B166n	DIFFOUT_B166n	AE6									
4A	VREFB4A0	IO		CLK9p	DIFFIO_RX_B166p	DIFFOUT_B166p	AF6									
4A	VREFB4A0	IO			DIFFIO_TX_B167n	DIFFOUT_B167n	AC7									
4A	VREFB4A0	IO		RZD_1	DIFFIO_TX_B167p	DIFFOUT_B167p	AD7									
4A	VREFB4A0	IO		CLK8n	DIFFIO_RX_B168n	DIFFOUT_B168n	AC6									
4A	VREFB4A0	IO		CLK8p	DIFFIO_RX_B168p	DIFFOUT_B168p	AD6									
				RREF_BR			AK2									
				DNJ			AJ3									
				DNJ			AK3									
GXB_R0		REFCLK0Rn					AA8									
GXB_R0		REFCLK0Rp					AA8									
GXB_R0		GXB_RX_R0nGXB_REFCLK_R0n					AH2									
GXB_R0		GXB_RX_R0pGXB_REFCLK_R0p					AH1									
GXB_R0		GXB_TX_R0n					AG3									
GXB_R0		GXB_TX_R0p					AG4									
GXB_R0		GXB_RX_R1nGXB_REFCLK_R1n					AF2									
GXB_R0		GXB_RX_R1pGXB_REFCLK_R1p					AF1									
GXB_R0		GXB_TX_R1n					AE3									
GXB_R0		GXB_TX_R1p					AE4									
GXB_R0		GXB_RX_R2nGXB_REFCLK_R2n					AD2									
GXB_R0		GXB_RX_R2pGXB_REFCLK_R2p					AD1									
GXB_R0		GXB_TX_R2n					AC3									
GXB_R0		GXB_TX_R2p					AC4									
GXB_R0		GXB_RX_R3nGXB_REFCLK_R3n					AB2									
GXB_R0		GXB_RX_R3pGXB_REFCLK_R3p					AB1									
GXB_R0		GXB_TX_R3n					AA3									
GXB_R0		GXB_TX_R3p					AA4									
GXB_R0		GXB_RX_R4nGXB_REFCLK_R4n					W2									
GXB_R0		GXB_RX_R4pGXB_REFCLK_R4p					V1									
GXB_R0		GXB_TX_R4n					W3									
GXB_R0		GXB_TX_R4p					W4									
GXB_R0		GXB_RX_R5nGXB_REFCLK_R5n					V2									
GXB_R0		GXB_RX_R5pGXB_REFCLK_R5p					V1									
GXB_R0		GXB_TX_R5n					U3									
GXB_R0		GXB_TX_R5p					U4									
GXB_R0		REFCLK1Rn					W9									
GXB_R0		REFCLK1Rp					W8									
BB	VREFB8B0	HPS_DDR					R4				HPS_DM_4		HPS_DM_4			
BB	VREFB8B0	HPS_DDR					R5				HPS_DQ_39		HPS_DQ_39			
BB	VREFB8B0	HPS_DDR					P7				HPS_DQ_37		HPS_DQ_37			
BB	VREFB8B0	HPS_DDR					N7				HPS_DQ_38		HPS_DQ_38			
BB	VREFB8B0	HPS_DDR					R7				HPS_DQ_38		HPS_DQ_38			
BB	VREFB8B0	HPS_DDR					R3				HPS_DQS_4		HPS_DQS_4			
BB	VREFB8B0	HPS_GPI13					T7									
BB	VREFB8B0	HPS_DDR					R2				HPS_DQS#_4		HPS_DQS#_4			
BB	VREFB8B0	HPS_DDR					T8				HPS_DQ_35		HPS_DQ_35			
BB	VREFB8B0	HPS_DDR					R1				HPS_DQ_33		HPS_DQ_33			
BB	VREFB8B0	HPS_DDR					M6				HPS_DQ_34		HPS_DQ_34			
BB	VREFB8B0	HPS_DDR					T1				HPS_DQ_32		HPS_DQ_32			
BB	VREFB8B0	HPS_GPI12					N6									
BB	VREFB8B0	HPS_GPI11					N3									
BB	VREFB8B0	HPS_DDR					R4				HPS_DM_3		HPS_DM_3			
BB	VREFB8B0	HPS_GPI10					P3									
BB	VREFB8B0	HPS_DDR					N5				HPS_DQ_31		HPS_DQ_31			
BB	VREFB8B0	HPS_DDR					A2				HPS_DQ_29		HPS_DQ_29			
BB	VREFB8B0	HPS_DDR					R6				HPS_DQ_30		HPS_DQ_30			
BB	VREFB8B0	HPS_DDR					P1				HPS_DQ_28		HPS_DQ_28			
BB	VREFB8B0	VREFB8B0					T6									
BB	VREFB8B0	HPS_DDR					M2				HPS_DQS_3		HPS_DQS_3			
BB	VREFB8B0	HPS_GPI9					L1									
BB	VREFB8B0	HPS_DDR					M3				HPS_DQS#_3		HPS_DQS#_3			
BB	VREFB8B0	HPS_DDR					M1				HPS_DQ_27		HPS_DQ_27			
BB	VREFB8B0	HPS_DDR					L4				HPS_DQ_25		HPS_DQ_25			
BB	VREFB8B0	HPS_DDR					U9				HPS_DQ_26		HPS_DQ_26			
BB	VREFB8B0	HPS_DDR					M4				HPS_DQ_24		HPS_DQ_24			
BB	VREFB8B0	HPS_GPI8					T9									
BB	VREFB8B0	HPS_GPI7					K1									
BB	VREFB8B0	HPS_DDR					L3				HPS_DM_2		HPS_DM_2			



Bank Number	VREF	PinName/Function (3, 2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DORS (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
GB	VREFBAND0_HPS	HPS_GPI6					J1									
GB	VREFBAND0_HPS	HPS_DDR					K3									
GB	VREFBAND0_HPS	HPS_DDR					M4				HPS_DQ_23	HPS_DQ_23				
GB	VREFBAND0_HPS	HPS_DDR					J8				HPS_DQ_21	HPS_DQ_21				
GB	VREFBAND0_HPS	HPS_DDR					M5				HPS_DQ_22	HPS_DQ_22				
GB	VREFBAND0_HPS	HPS_GPI6					K8				HPS_DQ_20	HPS_DQ_20				
GB	VREFBAND0_HPS	HPS_DDR					G8				HPS_DQS_2	HPS_DQS_2				
GB	VREFBAND0_HPS	HPS_DDR					J2				HPS_RESET#	HPS_RESET#				
GB	VREFBAND0_HPS	HPS_DDR					F8				HPS_DQS#_2	HPS_DQS#_2				
GB	VREFBAND0_HPS	HPS_DDR					K2				HPS_DQ_19	HPS_DQ_19				
GB	VREFBAND0_HPS	HPS_DDR					J4				HPS_DQ_17	HPS_DQ_17				
GB	VREFBAND0_HPS	HPS_DDR					R9				HPS_DQ_18	HPS_DQ_18				
GB	VREFBAND0_HPS	HPS_DDR					J3				HPS_DQ_16	HPS_DQ_16				
GB	VREFBAND0_HPS	HPS_GPI4					P9									
GA	VREFBAND0_HPS	HPS_GPI3					D1									
GA	VREFBAND0_HPS	HPS_DDR					E3				HPS_DM_1	HPS_DM_1				
GA	VREFBAND0_HPS	HPS_GPI2					C1									
GA	VREFBAND0_HPS	HPS_DDR					F3				HPS_DQ_15	HPS_DQ_15				
GA	VREFBAND0_HPS	HPS_DDR					F1				HPS_DQ_13	HPS_DQ_13				
GA	VREFBAND0_HPS	HPS_DDR					M7				HPS_DQ_14	HPS_DQ_14				
GA	VREFBAND0_HPS	HPS_DDR					G1				HPS_DQ_12	HPS_DQ_12				
GA	VREFBAND0_HPS	HPS_DDR					L7				HPS_CKE_0	HPS_CKE_0				
GA	VREFBAND0_HPS	HPS_DDR					D2				HPS_DQS_1	HPS_DQS_1				
GA	VREFBAND0_HPS	HPS_DDR					A2				HPS_CAE_1	HPS_CAE_1				
GA	VREFBAND0_HPS	HPS_DDR					E1				HPS_DQS#_1	HPS_DQS#_1				
GA	VREFBAND0_HPS	HPS_DDR					B1				HPS_DQ_11	HPS_DQ_11				
GA	VREFBAND0_HPS	HPS_DDR					A3				HPS_DQ_9	HPS_DQ_9				
GA	VREFBAND0_HPS	HPS_DDR					G2				HPS_DQ_10	HPS_DQ_10				
GA	VREFBAND0_HPS	HPS_DDR					B3				HPS_DQ_8	HPS_DQ_8				
GA	VREFBAND0_HPS	HPS_GPI1					H3									
GA	VREFBAND0_HPS	HPS_GPI0					A4									
GA	VREFBAND0_HPS	HPS_DDR					K5				HPS_DM_0	HPS_DM_0				
GA	VREFBAND0_HPS	HPS_DDR					K6				HPS_DQ_7	HPS_DQ_7				
GA	VREFBAND0_HPS	HPS_DDR					J3				HPS_DQ_5	HPS_DQ_5				
GA	VREFBAND0_HPS	HPS_DDR					A4				HPS_DQ_6	HPS_DQ_6				
GA	VREFBAND0_HPS	HPS_DDR					C3				HPS_DQ_4	HPS_DQ_4				
GA	VREFBAND0_HPS	HPS_DDR					B4				HPS_ODT_1	HPS_ODT_1				
GA	VREFBAND0_HPS	HPS_DDR					A5				HPS_DQS_0	HPS_DQS_0				
GA	VREFBAND0_HPS	HPS_DDR					G3				HPS_ODT_0	HPS_ODT_0				
GA	VREFBAND0_HPS	HPS_DDR					B6				HPS_DQS#_0	HPS_DQS#_0				
GA	VREFBAND0_HPS	HPS_DDR					G4				HPS_DQ_3	HPS_DQ_3				
GA	VREFBAND0_HPS	HPS_DDR					C4				HPS_DQ_1	HPS_DQ_1				
GA	VREFBAND0_HPS	HPS_DDR					E7				HPS_DQ_2	HPS_DQ_2				
GA	VREFBAND0_HPS	HPS_DDR					D4				HPS_DQ_0	HPS_DQ_0				
GA	VREFBAND0_HPS	VREFBAND0_HPS					K7									
GA	VREFBAND0_HPS	HPS_DDR					F5				HPS_A_0	HPS_CA_0				
GA	VREFBAND0_HPS	HPS_DDR					E4				HPS_A_1	HPS_CA_1				
GA	VREFBAND0_HPS	HPS_DDR					B7				HPS_A_4	HPS_CA_4				
GA	VREFBAND0_HPS	HPS_DDR					G5				HPS_A_2	HPS_CA_2				
GA	VREFBAND0_HPS	HPS_DDR					A6				HPS_A_5	HPS_CA_5				
GA	VREFBAND0_HPS	HPS_DDR					H6				HPS_A_3	HPS_CA_3				
GA	VREFBAND0_HPS	HPS_DDR					G6				HPS_CK	HPS_CK				
GA	VREFBAND0_HPS	HPS_DDR					A8				HPS_A_6	HPS_CA_6				
GA	VREFBAND0_HPS	HPS_DDR					G7				HPS_CK#	HPS_CK#				
GA	VREFBAND0_HPS	HPS_DDR					A7				HPS_CA_7	HPS_CA_7				
GA	VREFBAND0_HPS	HPS_DDR					A10				HPS_BA_1					
GA	VREFBAND0_HPS	HPS_DDR					H7				HPS_BA_0					
GA	VREFBAND0_HPS	HPS_DDR					A8				HPS_BA_2					
GA	VREFBAND0_HPS	HPS_DDR					E6				HPS_CAS#					
GA	VREFBAND0_HPS	HPS_DDR					D5				HPS_RAS#					
GA	VREFBAND0_HPS	HPS_DDR					D6				HPS_A_8	HPS_CA_8				
GA	VREFBAND0_HPS	HPS_DDR					J6				HPS_A_10					
GA	VREFBAND0_HPS	HPS_DDR					C6				HPS_A_9	HPS_CA_9				
GA	VREFBAND0_HPS	HPS_DDR					J7				HPS_A_11					
GA	VREFBAND0_HPS	HPS_DDR					C9				HPS_CSN_0	HPS_CSN_0				
GA	VREFBAND0_HPS	HPS_DDR					D7				HPS_A_12					
GA	VREFBAND0_HPS	HPS_DDR					C10				HPS_CSN_1	HPS_CSN_1				
GA	VREFBAND0_HPS	HPS_DDR					C7				HPS_A_13					
GA	VREFBAND0_HPS	HPS_DDR					D9				HPS_A_14					
GA	VREFBAND0_HPS	HPS_DDR					B9				HPS_WE#					
GA	VREFBAND0_HPS	HPS_DDR					D8				HPS_A_15					
GA	VREFBAND0_HPS	HPS_RZQ_0					B10									
		DNU					F7									
		GND					P9									
		GND					F10									
ZA		HPS_nRST					M8									
ZA		HPS_nPDK					H10									
ZA		HPS_TDO					H9									
ZA		VCDRSTCLK_HPS					L9									
ZA		HPS_TMS					L9									
ZA		HPS_TXC					J11									
ZA		HPS_TRST					K9									
ZA		HPS_TDI					J11									
		GND					A19									
ZA		HPS_PORSEL					A13									
ZA		HPS_CLK1					A11									
ZA		HPS_CLK2					A14									
ZA	VREFB7A7B7C7D7E0_HPS	TRACE_CLK					A15						TRACE_CLK			HPS_GPI048
ZA	VREFB7A7B7C7D7E0_HPS	TRACE_D0					K10						TRACE_D0	SPIS0_CLK	UART0_RX	HPS_GPI049
ZA	VREFB7A7B7C7D7E0_HPS	TRACE_D1					A16						TRACE_D1	SPIS0_MOSI	UART0_TX	HPS_GPI050
ZA	VREFB7A7B7C7D7E0_HPS	TRACE_D2					L10						TRACE_D2	SPIS0_MISO	IC21_SDA	HPS_GPI051
ZA	VREFB7A7B7C7D7E0_HPS	TRACE_D3					A18						TRACE_D3	SPIS0_SS0	IC21_SCL	HPS_GPI052
ZA	VREFB7A7B7C7D7E0_HPS	TRACE_D4					L11						TRACE_D4	SPIS1_CLK		HPS_GPI053
ZA	VREFB7A7B7C7D7E0_HPS	TRACE_D6					A17						TRACE_D6	SPIS1_MOSI		HPS_GPI054
ZA	VREFB7A7B7C7D7E0_HPS	TRACE_D6					M11						TRACE_D6	SPIS1_SS0	IC20_SDA	HPS_GPI055
ZA	VREFB7A7B7C7D7E0_HPS	TRACE_D7					B15						TRACE_D7	SPIS1_MISO	IC20_SCL	HPS_GPI056
ZA	VREFB7A7B7C7D7E0_HPS	SPIM0_CLK					A20						SPIM0_CLK	IC21_SDA	UART0_CTS	HPS_GPI057
ZA	VREFB7A7B7C7D7E0_HPS	SPIM0_MOSI					B16						SPIM0_MOSI	IC21_SCL	UART0_RTS	HPS_GPI058
ZA	VREFB7A7B7C7D7E0_HPS	SPIM0_MISO					A19						SPIM0_MISO	UART1_CTS		HPS_GPI059
ZA	VREFB7A7B7C7D7E0_HPS	SPIM0_SS0					B13						SPIM0_SS0	UART1_RTS		HPS_GPI060
ZA	VREFB7A7B7C7D7E0_HPS	UART0_RX					A12						UART0_RX	SPIM0_SS1		HPS_GPI061
ZA	VREFB7A7B7C7D7E0_HPS	UART0_TX					B12						UART0_TX	SPIM1_SS1		HPS_GPI062
ZA	VREFB7A7B7C7D7E0_HPS	IC20_SDA					N12						IC20_SDA	UART1_RX	SPIM1_CLK	HPS_GPI063
ZA	VREFB7A7B7C7D7E0_HPS	IC20_SCL					B18						IC20_SCL	UART1_TX	SPIM1_MISO	HPS_GPI064
ZA	VREFB7A7B7C7D7E0_HPS	UART0_RX*					C11						UART0_RX	SPIM1_MISO		HPS_GPI065
ZA	VREFB7A7B7C7D7E0_HPS	UART0_TX					B19						UART0_TX	SPIM1_SS0		HPS_GPI066
ZA	VREFB7A7B7C7D7E0_HPS	SPIS1_CLK					D10						SPIS1_CLK	SPIM1_CLK		HPS_GPI067
ZA	VREFB7A7B7C7D7E0_HPS	SPIS1_MOSI					F11						SPIS1_MOSI	SPIM1_MOSI		HPS_GPI068
ZA	VREFB7A7B7C7D7E0_HPS	SPIS1_MISO					J10						SPIS1_MISO	SPIM1_MISO		HPS_GPI069
ZA	VREFB7A7B7C7D7E0_HPS	SPIS1_SS0					G11						SPIS1_SS0	SPIM1_SS0		HPS_GPI070
ZA	VREFB7A7B7C7D7E0_HPS	UART1_RX					J8						UART1_RX	SPIM1_SS1		HPS_GPI071
ZA	VREFB7A7B7C7D7E0_HPS	UART1_TX					A21						UART1_TX	SPIM0_CLK		HPS_GPI072
ZA	VREFB7A7B7C7D7E0_HPS	IC21_SDA					F10						IC21_SDA	SPIM0_MOSI		HPS_GPI073
ZA	VREFB7A7B7C7D7E0_HPS	IC21_SCL					A22						IC21_SCL	SPIM0_MISO		HPS_GPI074
ZA	VREFB7A7B7C7D7E0_HPS	SPIM0_SS0					E9						SPIM0_SS0			HPS_GPI075
ZA	VREFB7A7B7C7D7E0_HPS	SPIS0_CLK					D11						SPIS0_CLK	SPIM0_SS1		HPS_GPI076
ZA	VREFB7A7B7C7D7E0_HPS	SPIS0_MOSI					P12						SPIS0_MOSI			HPS_GPI077



Pin Information for the Arria® V 5ASXMB3 Device
Version 1.3
Note (1)

Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DOR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
7A	VREFB7A7B7C7D7E0_HPS	SPIS0_MISO					E11						SPIS0_MISO			HPS_GPI069
7A	VREFB7A7B7C7D7E0_HPS	SPIS0_SSD					P13						SPIS0_SSD			HPS_GPI070
7B	VREFB7A7B7C7D7E0_HPS	NAND_ALE					A23						NAND_ALE	RGMI1_TX_CLK	GSPI_SS3	HPS_GPI014
7B	VREFB7A7B7C7D7E0_HPS	NAND_CE					B22						NAND_CE	RGMI1_TXD0	USBI_D9	HPS_GPI016
7B	VREFB7A7B7C7D7E0_HPS	NAND_GLE					B22						NAND_GLE	RGMI1_TXD1	USBI_D1	HPS_GPI016
7B	VREFB7A7B7C7D7E0_HPS	NAND_RE					D21						NAND_RE	RGMI1_TXD2	USBI_D2	HPS_GPI017
7B	VREFB7A7B7C7D7E0_HPS	NAND_RB					A24						NAND_RB	RGMI1_TXD3	USBI_D3	HPS_GPI018
7B	VREFB7A7B7C7D7E0_HPS	NAND_DQ0					C12						NAND_DQ0	RGMI1_RXD0		HPS_GPI018
7B	VREFB7A7B7C7D7E0_HPS	NAND_DQ1					B24						NAND_DQ1	RGMI1_MDIO	ZC2_SDA	HPS_GPI020
7B	VREFB7A7B7C7D7E0_HPS	NAND_DQ2					D12						NAND_DQ2	RGMI1_MDC	ZC2_SCL	HPS_GPI021
7B	VREFB7A7B7C7D7E0_HPS	NAND_DQ3					C16						NAND_DQ3	RGMI1_RX_CTL	USBI_D4	HPS_GPI022
7B	VREFB7A7B7C7D7E0_HPS	NAND_DQ4					C14						NAND_DQ4	RGMI1_TX_CTL	USBI_D5	HPS_GPI023
7B	VREFB7A7B7C7D7E0_HPS	NAND_DQ5					C16						NAND_DQ5	RGMI1_RX_CLK	USBI_D6	HPS_GPI024
7B	VREFB7A7B7C7D7E0_HPS	NAND_DQ6					C13						NAND_DQ6	RGMI1_RXD1	USBI_D7	HPS_GPI026
7B	VREFB7A7B7C7D7E0_HPS	NAND_DQ7					C18						NAND_DQ7	RGMI1_RXD2		HPS_GPI026
7B	VREFB7A7B7C7D7E0_HPS	NAND_WP					K12						NAND_WP	RGMI1_RXD3	GSPI_SS2	HPS_GPI027
7B	VREFB7A7B7C7D7E0_HPS	NAND_WE/BOOTSEL2					C17						NAND_WE	GSPI_SS1		HPS_GPI028
7B	VREFB7A7B7C7D7E0_HPS	QSPI_D0					I12						QSPI_D0		USBI_CLK	HPS_GPI029
7B	VREFB7A7B7C7D7E0_HPS	QSPI_I01					B21						QSPI_I01		USBI_STP	HPS_GPI030
7B	VREFB7A7B7C7D7E0_HPS	QSPI_I02					C20						QSPI_I02		USBI_DR	HPS_GPI031
7B	VREFB7A7B7C7D7E0_HPS	QSPI_I03					C21						QSPI_I03		USBI_NXT	HPS_GPI032
7B	VREFB7A7B7C7D7E0_HPS	QSPI_SS0/BOOTSEL1					C19						QSPI_SS0			HPS_GPI033
7B	VREFB7A7B7C7D7E0_HPS	QSPI_CLK					A26						QSPI_CLK			HPS_GPI034
7B	VREFB7A7B7C7D7E0_HPS	QSPI_SS1					B26						QSPI_SS1			HPS_GPI036
7C	VREFB7A7B7C7D7E0_HPS	SDMMC_CMD					D13						SDMMC_CMD	USB0_D0		HPS_GPI036
7C	VREFB7A7B7C7D7E0_HPS	SDMMC_PWRREN					K13						SDMMC_PWRREN	USB0_D1		HPS_GPI037
7C	VREFB7A7B7C7D7E0_HPS	SDMMC_D0					D14						SDMMC_D0	USB0_D2		HPS_GPI038
7C	VREFB7A7B7C7D7E0_HPS	SDMMC_D1					L13						SDMMC_D1	USB0_D3		HPS_GPI038
7C	VREFB7A7B7C7D7E0_HPS	SDMMC_D4					E13						SDMMC_D4	USB0_D4		HPS_GPI040
7C	VREFB7A7B7C7D7E0_HPS	SDMMC_D6					N13						SDMMC_D6	USB0_D6		HPS_GPI041
7C	VREFB7A7B7C7D7E0_HPS	SDMMC_D8					F13						SDMMC_D8	USB0_D8		HPS_GPI042
7C	VREFB7A7B7C7D7E0_HPS	SDMMC_D7					P14						SDMMC_D7	USB0_D7		HPS_GPI043
7C	VREFB7A7B7C7D7E0_HPS	HPS_GPI044					G13							USB0_CLK		HPS_GPI044
7C	VREFB7A7B7C7D7E0_HPS	SDMMC_CLK_OUT					J13						SDMMC_CLK_OUT	USB0_STP		HPS_GPI046
7C	VREFB7A7B7C7D7E0_HPS	SDMMC_D2					H13						SDMMC_D2	USB0_DIR		HPS_GPI046
7C	VREFB7A7B7C7D7E0_HPS	SDMMC_D3					H12						SDMMC_D3	USB0_NXT		HPS_GPI047
7D	VREFB7A7B7C7D7E0_HPS	RGMI0_TX_CLK					L15						RGMI0_TX_CLK			HPS_GPI01
7D	VREFB7A7B7C7D7E0_HPS	RGMI0_TXD0					N15						RGMI0_TXD0	USBI_D0		HPS_GPI01
7D	VREFB7A7B7C7D7E0_HPS	RGMI0_TXD1					K15						RGMI0_TXD1	USBI_D1		HPS_GPI02
7D	VREFB7A7B7C7D7E0_HPS	RGMI0_TXD2					P16						RGMI0_TXD2	USBI_D2		HPS_GPI03
7D	VREFB7A7B7C7D7E0_HPS	RGMI0_TXD3					D16						RGMI0_TXD3	USBI_D3		HPS_GPI04
7D	VREFB7A7B7C7D7E0_HPS	RGMI0_RXD0					M15						RGMI0_RXD0	USBI_D4		HPS_GPI05
7D	VREFB7A7B7C7D7E0_HPS	RGMI0_MDIO					E15						RGMI0_MDIO	USBI_D6	ZC2_SDA	HPS_GPI06
7D	VREFB7A7B7C7D7E0_HPS	RGMI0_MDC					N16						RGMI0_MDC	USBI_D8	ZC2_SCL	HPS_GPI07
7D	VREFB7A7B7C7D7E0_HPS	RGMI0_RX_CTL					D17						RGMI0_RX_CTL	USBI_D7		HPS_GPI08
7D	VREFB7A7B7C7D7E0_HPS	RGMI0_TX_CTL					M14						RGMI0_TX_CTL			HPS_GPI09
7D	VREFB7A7B7C7D7E0_HPS	RGMI0_RX_CLK					D16						RGMI0_RX_CLK	USBI_CLK		HPS_GPI10
7D	VREFB7A7B7C7D7E0_HPS	RGMI0_RXD1					L14						RGMI0_RXD1	USBI_STP		HPS_GPI11
7D	VREFB7A7B7C7D7E0_HPS	RGMI0_RXD2					F15						RGMI0_RXD2	USBI_DIR		HPS_GPI12
7D	VREFB7A7B7C7D7E0_HPS	RGMI0_RXD3					D19						RGMI0_RXD3	USBI_NXT		HPS_GPI13
7D	VREFB7A7B7C7D7E0_HPS	RGMI1_TX_CLK					F16						RGMI1_TX_CLK			HPS_GPI048
7D	VREFB7A7B7C7D7E0_HPS	RGMI1_TXD0					D18						RGMI1_TXD0			HPS_GPI049
7D	VREFB7A7B7C7D7E0_HPS	RGMI1_TXD1					E19						RGMI1_TXD1			HPS_GPI050
7D	VREFB7A7B7C7D7E0_HPS	RGMI1_TX_CTL					H15						RGMI1_TX_CTL			HPS_GPI051
7D	VREFB7A7B7C7D7E0_HPS	RGMI1_RXD0					D20						RGMI1_RXD0			HPS_GPI052
7D	VREFB7A7B7C7D7E0_HPS	RGMI1_RXD1					H14						RGMI1_RXD1			HPS_GPI053
7E	VREFB7A7B7C7D7E0_HPS	RGMI1_MDIO					F16						RGMI1_MDIO	SPIM0_CLK	SPIS0_CLK	HPS_GPI054
7E	VREFB7A7B7C7D7E0_HPS	RGMI1_MDC					H16						RGMI1_MDC	SPIM0_MOSI	SPIS0_MOSI	HPS_GPI054
7E	VREFB7A7B7C7D7E0_HPS	RGMI1_TXD0					H16						RGMI1_TXD0	SPIM0_MISO	SPIS0_MISO	HPS_GPI056
7E	VREFB7A7B7C7D7E0_HPS	RGMI1_TXD2					F17						RGMI1_TXD2	SPIM0_SS0	SPIS0_SS0	HPS_GPI057
7E	VREFB7A7B7C7D7E0_HPS	RGMI1_RX_CLK					L16						RGMI1_RX_CLK	SPIS1_CLK	SPIM1_CLK	HPS_GPI058
7E	VREFB7A7B7C7D7E0_HPS	RGMI1_RX_CTL					R16						RGMI1_RX_CTL	SPIS1_MOSI	SPIM1_MOSI	HPS_GPI059
7E	VREFB7A7B7C7D7E0_HPS	RGMI1_RXD2					K16						RGMI1_RXD2	SPIS1_MISO	SPIM1_MISO	HPS_GPI060
7E	VREFB7A7B7C7D7E0_HPS	RGMI1_RXD3					F16						RGMI1_RXD3	SPIS1_SS0	SPIM1_SS0	HPS_GPI061
		VCCA_FPLL					F16									
		VCCD_FPLL					T15									
		INU					G16									
8D	VREFB8D0	IO	CLK19b		DIFFIO_RX_T31a	DIFFOUT_T31a	M17									
8D	VREFB8D0	IO	CLK19b		DIFFIO_RX_T31a	DIFFOUT_T31a	N17									
8D	VREFB8D0	IO	CLK19b		DIFFIO_RX_T33a	DIFFOUT_T33a	F18									
8D	VREFB8D0	IO	CLK19b		DIFFIO_RX_T33a	DIFFOUT_T33a	G18									
8D	VREFB8D0	IO	FPLL_TC_CLKOUT2_FPLL_TC_Fb0/FPLL_TC_FB1		DIFFIO_RX_T35a	DIFFOUT_T35a	F19									
8D	VREFB8D0	IO	FPLL_TC_CLKOUT3_FPLL_TC_FBn		DIFFIO_RX_T35a	DIFFOUT_T35a	G19									
8D	VREFB8D0	IO	FPLL_TC_CLKOUT0_FPLL_TC_CLKOUT1_FPLL_TC_FB0		DIFFIO_TX_T36a	DIFFOUT_T36a	J17									
8D	VREFB8D0	IO	FPLL_TC_CLKOUT0_FPLL_TC_CLKOUT1		DIFFIO_TX_T36a	DIFFOUT_T36a	H18									
8D	VREFB8D0	IO	CLK17a		DIFFIO_RX_T37a	DIFFOUT_T37a	H18									
8D	VREFB8D0	IO	CLK17a		DIFFIO_RX_T37a	DIFFOUT_T37a	H19									
8D	VREFB8D0	IO	CLK19a		DIFFIO_RX_T39a	DIFFOUT_T39a	F20									
8D	VREFB8D0	IO	CLK18a		DIFFIO_RX_T39a	DIFFOUT_T39a	G20									
8C	VREFB8C0	IO	VREFB8D0		DIFFIO_RX_T54a	DIFFOUT_T54a	I19	DOIT			D05_BC 0	D06_BC 0				
8C	VREFB8C0	IO			DIFFIO_RX_T54a	DIFFOUT_T54a	K20	DOIT			D05_BC 1	D06_BC 1				
8C	VREFB8C0	IO			DIFFIO_TX_T55a	DIFFOUT_T55a	P19	DOIT			D05_BC 2	D06_BC 2				
8C	VREFB8C0	IO			DIFFIO_TX_T55a	DIFFOUT_T55a	J20	DOIT			D05_BC 3	D06_BC 3				
8C	VREFB8C0	IO			DIFFIO_RX_T56a	DIFFOUT_T56a	H21	DOIT			D05_BC 4	D06_BC 4				
8C	VREFB8C0	IO			DIFFIO_TX_T57a	DIFFOUT_T57a	N18	DOIT			D05_BC 5	D06_BC 5				
8C	VREFB8C0	IO			DIFFIO_RX_T58a	DIFFOUT_T58a	D22	DOStTQ0T1TQ0n1TQ0n1T			D05a_BC	D06a_BC				
8C	VREFB8C0	IO			DIFFIO_TX_T59a	DIFFOUT_T59a	E22	DOStTQ0T1TQ0n1TQ0n1T			D05a_BC	D06a_BC				
8C	VREFB8C0	IO			DIFFIO_TX_T59a	DIFFOUT_T59a	M18	DOIT			DM5_BC	DM6_BC				
8C	VREFB8C0	IO			DIFFIO_RX_T60a	DIFFOUT_T60a	A29	DOIT			D05a_BC 6	D06a_BC 6				
8C	VREFB8C0	IO			DIFFIO_RX_T60a	DIFFOUT_T60a	B30	DOIT			D05a_BC 7	D06a_BC 7				
8C	VREFB8C0	IO			DIFFIO_TX_T61a	DIFFOUT_T61a	L18	DOIT			D05a_BC 8	D06a_BC 8				
8C	VREFB8C0	IO			DIFFIO_RX_T62a	DIFFOUT_T62a	C23	DOIT	DOIT		D04a_BC 0	D04a_BC 0				
8C	VREFB8C0	IO			DIFFIO_RX_T62a	DIFFOUT_T62a	B23	DOIT	DOIT		D04a_BC 1	D04a_BC 1				
8C	VREFB8C0	IO					K18	DOIT	DOIT		D04a_BC 2	D04a_BC 2				
8C	VREFB8C0	IO			DIFFIO_RX_T63a	DIFFOUT_T63a	A28	DOIT	DOIT		D04a_BC 3	D04a_BC 3				
8C	VREFB8C0	IO			DIFFIO_RX_T63a	DIFFOUT_T63a	B28	DOIT	DOIT		D04a_BC 4	D04a_BC 4				
8C	VREFB8C0	IO			DIFFIO_TX_T64a	DIFFOUT_T64a	M19	DOIT	DOIT		D04a_BC 5	D04a_BC 5				
8C	VREFB8C0	IO			DIFFIO_RX_T65a	DIFFOUT_T65a	D24	DOStTQ0T1TQ0n1TQ0n1T	DOStTQ0T1TQ0n1T		D05a4_BC	D06a4_BC				
8C	VREFB8C0	IO			DIFFIO_RX_T65a	DIFFOUT_T65a	E24	DOStTQ0T1TQ0n1TQ0n1T	DOStTQ0T1TQ0n1T		D05a4_BC	D06a4_BC				
8C	VREFB8C0	IO			DIFFIO_TX_T66a	DIFFOUT_T66a	N19	DOIT	DOIT		DM4a_BC	DM5a_BC				
8C	VREFB8C0	IO			DIFFIO_RX_T67a	DIFFOUT_T67a	B27	DOIT	DOIT		D04a_BC 6	D04a_BC 6				
8C	VREFB8C0	IO			DIFFIO_RX_T67a	DIFFOUT_T67a	C27	DOIT	DOIT		D04a_BC 7	D04a_BC 7				
8C	VREFB8C0															



Bank Number	VREF	PinName/Function (3), (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	R996 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					U24									
		GND					U25									
		GND					U26									
		GND					U29									
		GND					U30									
		GND					V23									
		GND					V27									
		GND					V28									
		GND					W24									
		GND					W29									
		GND					W35									
		GND					Y23									
		GND					Y25									
		GND					Y26									
		GND					Y27									
		GND					Y28									
		GND					AA1									
		GND					AA2									
		GND					AA7									
		GND					AB3									
		GND					AB4									
		GND					AB5									
		GND					AB6									
		GND					AC1									
		GND					AC2									
		GND					AC5									
		GND					AD3									
		GND					AD4									
		GND					AE1									
		GND					AE2									
		GND					AE5									
		GND					AF3									
		GND					AF4									
		GND					AG1									
		GND					AG2									
		GND					AG5									
		GND					AH3									
		GND					AH4									
		GND					AJ1									
		GND					AJ2									
		GND					T3									
		GND					T4									
		GND					L1									
		GND					L2									
		GND					L5									
		GND					L6									
		GND					V3									
		GND					V4									
		GND					V8									
		GND					W1									
		GND					W2									
		GND					W5									
		GND					W7									
		GND					Y3									
		GND					Y4									
		GND					Y6									
		GND					Y8									
		VCCP					AB10									
		VCCP					AB14									
		VCCP					AB17									
		VCCP					AB20									
		VCCP					AC19									
		VCCP					P10									
		VCCP					RT7									
		VCCP					R21									
		VCCP					T10									
		VCCA_FPLL					V9									
		VCCA_FPLL					V22									
		VCCPLL_HPS					L10									
		VCCBAT					H25									
		VCC_AUX					AB11									
		VCC_AUX					AB18									
		VCC_AUX					R20									
		VCC_AUX_SHARED					R13									
		VCCD_FPLL					V9									
		VCCD_FPLL					Y22									
		VCCA_GXBR0					W6									
		VCCA_GXBL1					W20									
		VCCD_GXBR0					V7									
		VCCD_GXBL1					V24									
		VCCD_GXBR0					V5									
		VCCD_GXBL1					V6									
		VCCD_GXBL1					V25									
		VCCD_GXBL1					V26									
		VCCR_GXBL					AA25									
		VCCR_GXBL					AA26									
		VCCR_GXBR					AA5									
		VCCR_GXBR					AA6									
		VCCD_GXBR0					V5									
		VCCD_GXBL1					V7									
		VCCD_GXBL1					W25									
		VCCD_GXBL1					V24									
		VCC					AA10									
		VCC					AA13									
		VCC					AA14									
		VCC					AA16									
		VCC					AA18									
		VCC					AA19									
		VCC					AA20									
		VCC					T17									
		VCC					T19									
		VCC					T21									
		VCC					T22									
		VCC					U16									
		VCC					U18									
		VCC					U20									
		VCC					V15									
		VCC					V17									
		VCC					V19									
		VCC					V21									
		VCC					W12									
		VCC					W14									
		VCC					W18									
		VCC					W20									
		VCC					Y11									
		VCC					Y13									
		VCC					Y15									



Bank Number	VREF	PinName/Function (3), (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	R966 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCC					Y16									
		VCC					Y17									
		VCC					Y19									
		VCC					Y21									
		VCC					W16									
		VCC_HPS					R12									
		VCC_HPS					T11									
		VCC_HPS					T13									
		VCC_HPS					U12									
		VCC_HPS					U13									
		VCC_HPS					U14									
		VCC_HPS					V11									
		VCC_HPS					V13									
		VCCD0A					AE19									
		VCCD0A					AE22									
		VCCD0A					AF26									
		VCCD0A					AH19									
		VCCD0A					AH22									
		VCCD0A					AH26									
		VCCD0B					AE13									
		VCCD0B					AE16									
		VCCD0B					AH15									
		VCCD0B					AE11									
		VCCD0B					AD19									
		VCCD0A					AD5									
		VCCD0A					AE7									
		VCCD0A					AP5									
		VCCD0A					AM5									
		VCCD0A					AH7									
		VCCD0A_HPS					C2									
		VCCD0A_HPS					C5									
		VCCD0A_HPS					C8									
		VCCD0A_HPS					F2									
		VCCD0A_HPS					F4									
		VCCD0A_HPS					F6									
		VCCD0A_HPS					H1									
		VCCD0A_HPS					J5									
		VCCD0B_HPS					L4									
		VCCD0B_HPS					M4									
		VCCD0B_HPS					N1									
		VCCD0B_HPS					N6									
		VCCD0B_HPS					T2									
		VCCD0B_HPS					T5									
		VCCD0A_HPS					B14									
		VCCD0A_HPS					B17									
		VCCD0A_HPS					G10									
		VCCD0A_HPS					M10									
		VCCD0B_HPS					R20									
		VCCD0B_HPS					E12									
		VCCD0C_HPS					E14									
		VCCD0D_HPS					E18									
		VCCD0D_HPS					J14									
		VCCD0E_HPS					G15									
		VCCD0A					F29									
		VCCD0A					J27									
		VCCD0A					J29									
		VCCD0A					M29									
		VCCD0A					N24									
		VCCD0A					N27									
		VCCD0B					E27									
		VCCD0B					F25									
		VCCD0B					K23									
		VCCD0C					D25									
		VCCD0C					F29									
		VCCD0C					J1									
		VCCD0C					L19									
		VCCD0D					E21									
		VCCD0D					K17									
		VCCP03					AB21									
		VCCP03					AC18									
		VCCP03					AC24									
		VCCP04					AB7									
		VCCP06A6B_HPS					MB									
		VCCP06A6B_HPS					MB									
		VCCP06A6B_HPS					MB									
		VCCP06A6B_HPS					UB									
		VCCP07A_HPS					N11									
		VCCP07B_HPS					L12									
		VCCP07C_HPS					M13									
		VCCP07D_HPS					M16									
		VCCP07E_HPS					J15									
		VCCP08					P18									
		VCCP08					P22									
		VCCD0B					R19									
		VCCP09					R24									
		VCCP0M					F12									
		VCCP0M					AD26									
		VCCP0TCLK_HPS					C9									
		VCC_HPS					R10									
		VCC_HPS					R11									
		VCC_HPS					R14									
		VCC_HPS					R15									
		VREFB7A/B7C7D7E0_HPS					F14									
		GND					AA11									
		GND					AA13									
		GND					AA15									
		GND					AA17									
		GND					AA21									
		GND					AB19									
		GND					AB8									
		GND					AB9									
		GND					AC11									
		GND					AC14									
		GND					AC17									
		GND					AC20									
		GND					AC23									
		GND					AD8									
		GND					AF11									
		GND					AF14									
		GND					AF17									
		GND					AF20									
		GND					AF23									
		GND					AF8									
		GND					AJ14									
		GND					AJ14									
		GND					AJ17									
		GND					AJ20									



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	FB96 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					A123									
		GND					A126									
		GND					A15									
		GND					A16									
		GND					B11									
		GND					B2									
		GND					B23									
		GND					B26									
		GND					B29									
		GND					B5									
		GND					B8									
		GND					E17									
		GND					E2									
		GND					E20									
		GND					E23									
		GND					E26									
		GND					E29									
		GND					E5									
		GND					E8									
		GND					G12									
		GND					G14									
		GND					H17									
		GND					H2									
		GND					H20									
		GND					H23									
		GND					H26									
		GND					H29									
		GND					H5									
		GND					H8									
		GND					K11									
		GND					K14									
		GND					L17									
		GND					L2									
		GND					L20									
		GND					L23									
		GND					L26									
		GND					L29									
		GND					L5									
		GND					L8									
		GND					N10									
		GND					N14									
		GND					P11									
		GND					P17									
		GND					P16									
		GND					P2									
		GND					P20									
		GND					P23									
		GND					P26									
		GND					P29									
		GND					P5									
		GND					P8									
		GND					R18									
		GND					T12									
		GND					T14									
		GND					T18									
		GND					T20									
		GND					U11									
		GND					U15									
		GND					U17									
		GND					U19									
		GND					U21									
		GND					U7									
		GND					V10									
		GND					V12									
		GND					V14									
		GND					V18									
		GND					V20									
		GND					V14									
		GND					W13									
		GND					W15									
		GND					W17									
		GND					W19									
		GND					W21									
		GND					Y10									
		GND					Y12									
		GND					Y18									
		GND					Y20									

Notes:
 (1) For more information about pin definitions and pin connection guidelines, refer to the [Arria V Device Family Pin Connection Guidelines](#).
 (2) GAB, REFCLK pin is not supported in current Quartus II version, but will be supported in future Quartus II release version.
 (3) Pins with * contains similar name with other pins in the same column. For the selection of the HPS pins, refer to the "HPS Pin Mux Select x" columns.
 (4) Pins with ~ are the 10 Gbps transceiver channels. For more information about the 10 Gbps transceiver channels clocking recommendation, refer to the [Transceiver Clocking in Arria V Devices chapter](#).
 (5) RESET pin is only applicable for DDR3 device.



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X0/X3	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DQS3 (6)	HMC pin assignment for FCODE2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		DNU					A38									
		REFCLK0p					B38									
		REFCLK0n					B39									
		REFCLK0p					U32									
		REFCLK0n					U31									
		GXB_TX_L17n					C36									
		GXB_TX_L17p					C37									
		GXB_RX_L17nGXB_REFCLK_L17n					D39									
		GXB_RX_L17pGXB_REFCLK_L17p					D38									
		GXB_TX_L16p					E36									
		GXB_TX_L16n					E37									
		GXB_RX_L16pGXB_REFCLK_L16p					F39									
		GXB_RX_L16nGXB_REFCLK_L16n					F38									
		GXB_TX_L15p					G36									
		GXB_TX_L15n					G37									
		GXB_RX_L15pGXB_REFCLK_L15p					H39									
		GXB_RX_L15nGXB_REFCLK_L15n					H38									
		GXB_TX_L14p					J36									
		GXB_TX_L14n					J37									
		GXB_RX_L14pGXB_REFCLK_L14p					K39									
		GXB_RX_L14nGXB_REFCLK_L14n					K38									
		GXB_TX_L13p					L36									
		GXB_TX_L13n					L37									
		GXB_RX_L13pGXB_REFCLK_L13p					M39									
		GXB_RX_L13nGXB_REFCLK_L13n					M38									
		GXB_TX_L12p					N36									
		GXB_TX_L12n					N37									
		GXB_RX_L12pGXB_REFCLK_L12p					P39									
		GXB_RX_L12nGXB_REFCLK_L12n					P38									
		REFCLK0p					W32									
		REFCLK0n					W31									
		REFCLK0p					A32									
		REFCLK0n					A31									
		GXB_TX_L11n					R36									
		GXB_TX_L11p					R37									
		GXB_RX_L11pGXB_REFCLK_L11p					T39									
		GXB_RX_L11nGXB_REFCLK_L11n					T38									
		GXB_TX_L10p					U36									
		GXB_TX_L10n					U37									
		GXB_RX_L10pGXB_REFCLK_L10p					V39									
		GXB_RX_L10nGXB_REFCLK_L10n					V38									
		GXB_TX_L9p					W36									
		GXB_TX_L9n					W37									
		GXB_RX_L9pGXB_REFCLK_L9p					Y39									
		GXB_RX_L9nGXB_REFCLK_L9n					Y38									
		GXB_TX_L8p					A36									
		GXB_TX_L8n					A37									
		GXB_RX_L8pGXB_REFCLK_L8p					B39									
		GXB_RX_L8nGXB_REFCLK_L8n					B38									
		GXB_TX_L7p					AC36									
		GXB_TX_L7n					AC37									
		GXB_RX_L7pGXB_REFCLK_L7p					AD39									
		GXB_RX_L7nGXB_REFCLK_L7n					AD38									
		GXB_TX_L6p					AE36									
		GXB_TX_L6n					AE37									
		GXB_RX_L6pGXB_REFCLK_L6p					AF39									
		GXB_RX_L6nGXB_REFCLK_L6n					AF38									
		REFCLK0p					AG32									
		REFCLK0n					AG31									
		REFCLK1n					AE32									
		REFCLK0p					AG31									
		GXB_TX_L5p					AG37									
		GXB_TX_L5n					AH36									
		GXB_RX_L5pGXB_REFCLK_L5p					AI39									
		GXB_RX_L5nGXB_REFCLK_L5n					AI38									
		GXB_TX_L4p					AJ37									
		GXB_TX_L4n					AK39									
		GXB_RX_L4pGXB_REFCLK_L4p					AL39									
		GXB_RX_L4nGXB_REFCLK_L4n					AL38									
		GXB_TX_L3p					AL36									
		GXB_TX_L3n					AL37									
		GXB_RX_L3pGXB_REFCLK_L3p					AM39									
		GXB_RX_L3nGXB_REFCLK_L3n					AM38									
		GXB_TX_L2p					AN36									
		GXB_TX_L2n					AN37									
		GXB_RX_L2pGXB_REFCLK_L2p					AP39									
		GXB_RX_L2nGXB_REFCLK_L2n					AP38									
		GXB_TX_L1p					AP36									
		GXB_TX_L1n					AP37									
		GXB_RX_L1pGXB_REFCLK_L1p					AT39									
		GXB_RX_L1nGXB_REFCLK_L1n					AT38									
		GXB_TX_L0p					AU36									
		GXB_TX_L0n					AV37									
		GXB_RX_L0pGXB_REFCLK_L0p					AW39									
		GXB_RX_L0nGXB_REFCLK_L0n					AW38									
		REFCLK0p					AG32									
		REFCLK0n					AG31									
		DNU					AK31									
		TDO		TDO			AT34									
		TMS		TMS			AM35									
		TCX		TCX			AT34									
		TDI		TDI			AT33									
		DCLK		DCLK			AV34									
		HPS0		DATA4			AM34									
		AS_DATA3		DATA3			AM34									
		AS_DATA2		DATA2			AP33									
		AS_DATA1		DATA1			AT33									
		AS_DATA0ASD0		DATA0			AV33									
		RZQ_0					AM33									
		DIFF0_TX_B1n		DIFF0_TX_B1n		DIFF0_TX_B1n	AP33									
		DIFF0_RX_B0n		DIFF0_RX_B0n		DIFF0_RX_B0n	AN34									
		DIFF0_TX_B0p		DIFF0_TX_B0p		DIFF0_TX_B0p	AP34									
		DIFF0_RX_B0n		DIFF0_RX_B0n		DIFF0_RX_B0n	AN33									
		DIFF0_TX_B0p		DIFF0_TX_B0p		DIFF0_TX_B0p	AP32									
		DIFF0_RX_B0p		DIFF0_RX_B0p		DIFF0_RX_B0p	AN34									
		DIFF0_TX_B0n		DIFF0_TX_B0n		DIFF0_TX_B0n	AP34									
		DIFF0_RX_B0p		DIFF0_RX_B0p		DIFF0_RX_B0p	AN33									
		DIFF0_TX_B0n		DIFF0_TX_B0n		DIFF0_TX_B0n	AP34									
		DIFF0_RX_B0n		DIFF0_RX_B0n		DIFF0_RX_B0n	AN33									
		DIFF0_TX_B0p		DIFF0_TX_B0p		DIFF0_TX_B0p	AP32									
		DIFF0_RX_B0p		DIFF0_RX_B0p		DIFF0_RX_B0p	AN34									
		DIFF0_TX_B0n		DIFF0_TX_B0n		DIFF0_TX_B0n	AP34									
		DIFF0_RX_B0n		DIFF0_RX_B0n		DIFF0_RX_B0n	AN33									
		DIFF0_TX_B0p		DIFF0_TX_B0p		DIFF0_TX_B0p	AP32									
		DIFF0_RX_B0p		DIFF0_RX_B0p		DIFF0_RX_B0p	AN34									
		DIFF0_TX_B0n		DIFF0_TX_B0n		DIFF0_TX_B0n	AP34									
		DIFF0_RX_B0n		DIFF0_RX_B0n		DIFF0_RX_B0n	AN33									
		DIFF0_TX_B0p		DIFF0_TX_B0p		DIFF0_TX_B0p	AP32									
		DIFF0_RX_B0p		DIFF0_RX_B0p		DIFF0_RX_B0p	AN34									
		DIFF0_TX_B0n		DIFF0_TX_B0n		DIFF0_TX_B0n	AP34									
		DIFF0_RX_B0n		DIFF0_RX_B0n		DIFF0_RX_B0n	AN33									
		DIFF0_TX_B0p		DIFF0_TX_B0p		DIFF0_TX_B0p	AP32									
		DIFF0_RX_B0p		DIFF0_RX_B0p		DIFF0_RX_B0p	AN34									
		DIFF0_TX_B0n		DIFF0_TX_B0n		DIFF0_TX_B0n	AP34									
		DIFF0_RX_B0n		DIFF0_RX_B0n		DIFF0_RX_B0n	AN33									
		DIFF0_TX_B0p		DIFF0_TX_B0p		DIFF0_TX_B0p	AP32									
		DIFF0_RX_B0p		DIFF0_RX_B0p		DIFF0_RX_B0p	AN34									
		DIFF0_TX_B0n		DIFF0_TX_B0n		DIFF0_TX_B0n	AP34									
		DIFF0_RX_B0n		DIFF0_RX_B0n		DIFF0_RX_B0n	AN33									
		DIFF0_TX_B0p		DIFF0_TX_B0p		DIFF0_TX_B0p	AP32									
		DIFF0_RX_B0p		DIFF0_RX_B0p		DIFF0_RX_B0p	AN34									
		DIFF0_TX_B0n		DIFF0_TX_B0n		DIFF0_TX_B0n	AP34									
		DIFF0_RX_B0n		DIFF0_RX_B0n		DIFF0_RX_B0n	AN33									
		DIFF0_TX_B0p		DIFF0_TX_B0p		DIFF0_TX_B0p	AP32									
		DIFF0_RX_B0p		DIFF0_RX_B0p		DIFF0_RX_B0p	AN34									



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8/X0	DQS for X16/X8	DQS for X32/X16	HMC pin assignment for DQES (6)	HMC pin assignment for FPODES	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
3A	VREF3AAND	IO			DIFFIO_TX_B16n	DIFFIOUT_B16n	AU31	DO3B			A_3A_11					
3A	VREF3AAND	IO			DIFFIO_TX_B18n	DIFFIOUT_B18n	AV31	DO3B			A_3A_10					
3A	VREF3AAND	IO			DIFFIO_TX_B17n	DIFFIOUT_B17n	AV31	DO3B			A_3A_7					
3A	VREF3AAND	IO			DIFFIO_TX_B16n	DIFFIOUT_B16n	AV31	DO3B			A_3A_8	CA_3A_9				
3A	VREF3AAND	IO			DIFFIO_TX_B17n	DIFFIOUT_B17n	AV31	DO3B			A_3A_8	CA_3A_8				
3A	VREF3AAND	IO			DIFFIO_TX_B18n	DIFFIOUT_B18n	AV31	DO3B			A_3A_7	CA_3A_7				
3A	VREF3AAND	IO			DIFFIO_TX_B19n	DIFFIOUT_B19n	AV31	DO3B			A_3A_6	CA_3A_6				
3A	VREF3AAND	IO			DIFFIO_TX_B18n	DIFFIOUT_B18n	AV30	DO3B/QK3B			A_3A_5	CA_3A_5				
3A	VREF3AAND	IO			DIFFIO_TX_B17n	DIFFIOUT_B17n	AV30	DO3B/QK3B			A_3A_4	CA_3A_4				
3A	VREF3AAND	IO			DIFFIO_TX_B20n	DIFFIOUT_B20n	AU30	DO3B			A_3A_3	CA_3A_3				
3A	VREF3AAND	IO			DIFFIO_TX_B20n	DIFFIOUT_B20n	AV30	DO3B			A_3A_2	CA_3A_2				
3A	VREF3AAND	IO			DIFFIO_TX_B21n	DIFFIOUT_B21n	AV29	DO3B			A_3A_1	CA_3A_1				
3A	VREF3AAND	IO			DIFFIO_RX_B21n	DIFFIOUT_B21n	AU29	DO3B			A_3A_0	CA_3A_0				
3A	VREF3AAND	IO			DIFFIO_TX_B22n	DIFFIOUT_B22n	AV29	DO3B			CO3_3A_1	CO3_3A_1				
3A	VREF3AAND	IO			DIFFIO_TX_B20n	DIFFIOUT_B20n	AV29	DO3B			CO3_3A_0	CO3_3A_0				
3A	VREF3AAND	IO			DIFFIO_RX_B23n	DIFFIOUT_B23n	AV29	DO3B			CO3_3A	CO3_3A				
3A	VREF3AAND	IO			DIFFIO_RX_B23n	DIFFIOUT_B23n	AV29	DO3B			CO3_3A	CO3_3A				
3B	VREF3BAND	IO			DIFFIO_TX_B24n	DIFFIOUT_B24n	AV29	DO4B			DO3B					
3B	VREF3BAND	IO			DIFFIO_TX_B24n	DIFFIOUT_B24n	AV29	DO4B			DO3B					
3B	VREF3BAND	IO			DIFFIO_RX_B25n	DIFFIOUT_B25n	AV28	DO4B			DO3B					
3B	VREF3BAND	IO			DIFFIO_RX_B25n	DIFFIOUT_B25n	AV28	DO4B			DO3B					
3B	VREF3BAND	IO			DIFFIO_TX_B26n	DIFFIOUT_B26n	AV28	DO4B			DO3B					
3B	VREF3BAND	IO			DIFFIO_TX_B26n	DIFFIOUT_B26n	AV28	DO4B			DO3B					
3B	VREF3BAND	IO			DIFFIO_RX_B27n	DIFFIOUT_B27n	AV28	DO4B			DO3B					
3B	VREF3BAND	IO			DIFFIO_RX_B27n	DIFFIOUT_B27n	AV28	DO4B			DO3B					
3B	VREF3BAND	IO			DIFFIO_TX_B28n	DIFFIOUT_B28n	AV28	DO4B			DO3B					
3B	VREF3BAND	IO			DIFFIO_TX_B28n	DIFFIOUT_B28n	AV28	DO4B			DO3B					
3B	VREF3BAND	IO			DIFFIO_RX_B29n	DIFFIOUT_B29n	AV28	DO4B			DO3B					
3B	VREF3BAND	IO			DIFFIO_RX_B29n	DIFFIOUT_B29n	AV28	DO4B			DO3B					
3B	VREF3BAND	IO			DIFFIO_TX_B30n	DIFFIOUT_B30n	AV27	DO4B			DO3B					
3B	VREF3BAND	IO			DIFFIO_TX_B30n	DIFFIOUT_B30n	AV27	DO4B			DO3B					
3B	VREF3BAND	IO			DIFFIO_RX_B31n	DIFFIOUT_B31n	AV27	DO4B			DO3B					
3B	VREF3BAND	IO			DIFFIO_RX_B31n	DIFFIOUT_B31n	AV27	DO4B			DO3B					
3B	VREF3BAND	IO			DIFFIO_TX_B31n	DIFFIOUT_B31n	AV28	DO3B			DO2B					
3B	VREF3BAND	IO			DIFFIO_TX_B32n	DIFFIOUT_B32n	AV28	DO3B			DO2B					
3B	VREF3BAND	IO			DIFFIO_RX_B32n	DIFFIOUT_B32n	AV28	DO3B			DO2B					
3B	VREF3BAND	IO			DIFFIO_RX_B32n	DIFFIOUT_B32n	AV28	DO3B			DO2B					
3B	VREF3BAND	IO			DIFFIO_TX_B33n	DIFFIOUT_B33n	AJ27	DO3B			DO2B					
3B	VREF3BAND	IO			DIFFIO_TX_B33n	DIFFIOUT_B33n	AJ27	DO3B			DO2B					
3B	VREF3BAND	IO			DIFFIO_RX_B34n	DIFFIOUT_B34n	AV28	DO3B/QK3B			DO3B					
3B	VREF3BAND	IO			DIFFIO_RX_B34n	DIFFIOUT_B34n	AV28	DO3B/QK3B			DO3B					
3B	VREF3BAND	IO			DIFFIO_TX_B35n	DIFFIOUT_B35n	AV27	DO3B			DO3B					
3B	VREF3BAND	IO			DIFFIO_TX_B35n	DIFFIOUT_B35n	AV27	DO3B			DO3B					
3B	VREF3BAND	IO			DIFFIO_RX_B36n	DIFFIOUT_B36n	AV27	DO3B			DO3B					
3B	VREF3BAND	IO			DIFFIO_RX_B36n	DIFFIOUT_B36n	AV27	DO3B			DO3B					
3B	VREF3BAND	IO			DIFFIO_TX_B37n	DIFFIOUT_B37n	AV27	DO3B			DO3B					
3B	VREF3BAND	IO			DIFFIO_TX_B37n	DIFFIOUT_B37n	AV27	DO3B			DO3B					
3B	VREF3BAND	IO			DIFFIO_RX_B38n	DIFFIOUT_B38n	AV27	DO3B			DO3B					
3B	VREF3BAND	IO			DIFFIO_RX_B38n	DIFFIOUT_B38n	AV27	DO3B			DO3B					
3B	VREF3BAND	IO			DIFFIO_TX_B39n	DIFFIOUT_B39n	AV27	DO3B			DO3B					
3B	VREF3BAND	IO			DIFFIO_TX_B39n	DIFFIOUT_B39n	AV27	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B39n	DIFFIOUT_B39n	AV27	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B40n	DIFFIOUT_B40n	AV25	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B40n	DIFFIOUT_B40n	AV25	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B41n	DIFFIOUT_B41n	AV27	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B41n	DIFFIOUT_B41n	AV27	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B42n	DIFFIOUT_B42n	AV25	DO3B/QK3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B42n	DIFFIOUT_B42n	AV25	DO3B/QK3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B43n	DIFFIOUT_B43n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B43n	DIFFIOUT_B43n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B44n	DIFFIOUT_B44n	AV25	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B44n	DIFFIOUT_B44n	AV25	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B45n	DIFFIOUT_B45n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B45n	DIFFIOUT_B45n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B46n	DIFFIOUT_B46n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B46n	DIFFIOUT_B46n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B47n	DIFFIOUT_B47n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B47n	DIFFIOUT_B47n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B48n	DIFFIOUT_B48n	AV25	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B48n	DIFFIOUT_B48n	AV25	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B49n	DIFFIOUT_B49n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B49n	DIFFIOUT_B49n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B50n	DIFFIOUT_B50n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B50n	DIFFIOUT_B50n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B51n	DIFFIOUT_B51n	AV25	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B51n	DIFFIOUT_B51n	AV25	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B52n	DIFFIOUT_B52n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B52n	DIFFIOUT_B52n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B53n	DIFFIOUT_B53n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B53n	DIFFIOUT_B53n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B54n	DIFFIOUT_B54n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B54n	DIFFIOUT_B54n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B55n	DIFFIOUT_B55n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B55n	DIFFIOUT_B55n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B56n	DIFFIOUT_B56n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B56n	DIFFIOUT_B56n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B57n	DIFFIOUT_B57n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B57n	DIFFIOUT_B57n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B58n	DIFFIOUT_B58n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B58n	DIFFIOUT_B58n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B59n	DIFFIOUT_B59n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B59n	DIFFIOUT_B59n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B60n	DIFFIOUT_B60n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B60n	DIFFIOUT_B60n	AV24	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B61n	DIFFIOUT_B61n	AV23	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B61n	DIFFIOUT_B61n	AV23	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B62n	DIFFIOUT_B62n	AV23	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B62n	DIFFIOUT_B62n	AV23	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B63n	DIFFIOUT_B63n	AV23	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B63n	DIFFIOUT_B63n	AV23	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B64n	DIFFIOUT_B64n	AV23	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B64n	DIFFIOUT_B64n	AV23	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B65n	DIFFIOUT_B65n	AV22	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B65n	DIFFIOUT_B65n	AV22	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B66n	DIFFIOUT_B66n	AV22	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_RX_B66n	DIFFIOUT_B66n	AV22	DO3B			DO3B					
3C	VREF3CAND	IO			DIFFIO_TX_B67n	DIFFIOUT_B67n</										



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X0/X3	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DQES1 (6)	HMC pin assignment for LPDDR2 (6)	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
EB	VREFBAND_HPS	HPS_DDR					L1				HPS_DQ_35	HPS_DQ_35				
EB	VREFBAND_HPS	HPS_DDR					L2				HPS_DQ_31	HPS_DQ_31				
EB	VREFBAND_HPS	HPS_DDR					F1				HPS_DQ_32	HPS_DQ_32				
EB	VREFBAND_HPS	HPS_GPIV2					K1				HPS_DQ_34	HPS_DQ_34				
EB	VREFBAND_HPS	HPS_GPH11					J2				HPS_DQ_33	HPS_DQ_33				
EB	VREFBAND_HPS	HPS_DDR					D1				HPS_DM_3	HPS_DM_3				
EB	VREFBAND_HPS	HPS_GPIV0					K2									
EB	VREFBAND_HPS	HPS_DDR					E1				HPS_DQ_31	HPS_DQ_31				
EB	VREFBAND_HPS	HPS_DDR					F2				HPS_DQ_29	HPS_DQ_29				
EB	VREFBAND_HPS	HPS_DDR					M3				HPS_DQ_30	HPS_DQ_30				
EB	VREFBAND_HPS	HPS_DDR					G2				HPS_DQ_28	HPS_DQ_28				
EB	VREFBAND_HPS	VREFBAND_HPS					M2									
EB	VREFBAND_HPS	HPS_DDR					C2				HPS_DQS_3	HPS_DQS_3				
EB	VREFBAND_HPS	HPS_GPIV3					B1				HPS_DQS_3	HPS_DQS_3				
EB	VREFBAND_HPS	HPS_DDR					D3				HPS_DQS_3	HPS_DQS_3				
EB	VREFBAND_HPS	HPS_DDR					C1				HPS_DQS_27	HPS_DQS_27				
EB	VREFBAND_HPS	HPS_DDR					A3				HPS_DQ_25	HPS_DQ_25				
EB	VREFBAND_HPS	HPS_DDR					F7				HPS_DQ_26	HPS_DQ_26				
EB	VREFBAND_HPS	HPS_DDR					A2				HPS_DQ_24	HPS_DQ_24				
EB	VREFBAND_HPS	HPS_GPIV3					N5									
EB	VREFBAND_HPS	HPS_DDR					K3									
EB	VREFBAND_HPS	HPS_DDR					D3				HPS_DM_2	HPS_DM_2				
EB	VREFBAND_HPS	HPS_GPIV3					K4									
EB	VREFBAND_HPS	HPS_DDR					C3				HPS_DQ_23	HPS_DQ_23				
EB	VREFBAND_HPS	HPS_DDR					J4				HPS_DQ_21	HPS_DQ_21				
EB	VREFBAND_HPS	HPS_DDR					M5				HPS_DQ_22	HPS_DQ_22				
EB	VREFBAND_HPS	HPS_DDR					L6				HPS_DQ_20	HPS_DQ_20				
EB	VREFBAND_HPS	HPS_GPIV3					L4									
EB	VREFBAND_HPS	HPS_DDR					G4				HPS_DQS_2	HPS_DQS_2				
EB	VREFBAND_HPS	HPS_DDR					E3				HPS_RESETr	HPS_RESETr				
EB	VREFBAND_HPS	HPS_DDR					H4				HPS_DQS_2	HPS_DQS_2				
EB	VREFBAND_HPS	HPS_DDR					F3				HPS_DQ_19	HPS_DQ_19				
EB	VREFBAND_HPS	HPS_DDR					K7				HPS_DQ_17	HPS_DQ_17				
EB	VREFBAND_HPS	HPS_DDR					N6				HPS_DQ_18	HPS_DQ_18				
EB	VREFBAND_HPS	HPS_GPIV3					J5				HPS_DQ_16	HPS_DQ_16				
EB	VREFBAND_HPS	HPS_GPIV4					M6									
EA	VREFBAND_HPS	HPS_GPIV3					C4									
EA	VREFBAND_HPS	HPS_DDR					E4				HPS_DM_1	HPS_DM_1				
EA	VREFBAND_HPS	HPS_GPIV2					B4									
EA	VREFBAND_HPS	HPS_DDR					F4				HPS_DQ_15	HPS_DQ_15				
EA	VREFBAND_HPS	HPS_DDR					A5				HPS_DQ_13	HPS_DQ_13				
EA	VREFBAND_HPS	HPS_DDR					R9				HPS_DQ_14	HPS_DQ_14				
EA	VREFBAND_HPS	HPS_DDR					A4				HPS_DQ_12	HPS_DQ_12				
EA	VREFBAND_HPS	HPS_DDR					R8				HPS_CK6_0	HPS_CK6_0				
EA	VREFBAND_HPS	HPS_DDR					D5				HPS_DQS_1	HPS_DQS_1				
EA	VREFBAND_HPS	HPS_DDR					F5				HPS_CK6_1	HPS_CK6_1				
EA	VREFBAND_HPS	HPS_DDR					E6				HPS_DQS_1	HPS_DQS_1				
EA	VREFBAND_HPS	HPS_DDR					G6				HPS_DQ_11	HPS_DQ_11				
EA	VREFBAND_HPS	HPS_DDR					G5				HPS_DQ_9	HPS_DQ_9				
EA	VREFBAND_HPS	HPS_DDR					N8				HPS_DQ_10	HPS_DQ_10				
EA	VREFBAND_HPS	HPS_DDR					M7				HPS_DQ_8	HPS_DQ_8				
EA	VREFBAND_HPS	HPS_GPIV3					B6									
EA	VREFBAND_HPS	HPS_DDR					C5				HPS_DM_0	HPS_DM_0				
EA	VREFBAND_HPS	HPS_DDR					D6				HPS_DQ_7	HPS_DQ_7				
EA	VREFBAND_HPS	HPS_DDR					A7				HPS_DQ_5	HPS_DQ_5				
EA	VREFBAND_HPS	HPS_DDR					L6				HPS_DQ_6	HPS_DQ_6				
EA	VREFBAND_HPS	HPS_DDR					A6				HPS_DQ_4	HPS_DQ_4				
EA	VREFBAND_HPS	HPS_DDR					K6				HPS_ODT_1	HPS_ODT_1				
EA	VREFBAND_HPS	HPS_DDR					F7				HPS_DQS_0	HPS_DQS_0				
EA	VREFBAND_HPS	HPS_DDR					H7				HPS_ODT_0	HPS_ODT_0				
EA	VREFBAND_HPS	HPS_DDR					E7				HPS_DQS_0	HPS_DQS_0				
EA	VREFBAND_HPS	HPS_DDR					G7				HPS_DQ_3	HPS_DQ_3				
EA	VREFBAND_HPS	HPS_DDR					C7				HPS_DQ_1	HPS_DQ_1				
EA	VREFBAND_HPS	HPS_DDR					F8				HPS_DQ_2	HPS_DQ_2				
EA	VREFBAND_HPS	HPS_DDR					D7				HPS_DQ_0	HPS_DQ_0				
EA	VREFBAND_HPS	VREFBAND_HPS					P10									
EA	VREFBAND_HPS	HPS_DDR					N9				HPS_A_0	HPS_CA_0				
EA	VREFBAND_HPS	HPS_DDR					M9				HPS_A_1	HPS_CA_1				
EA	VREFBAND_HPS	HPS_DDR					A8				HPS_A_4	HPS_CA_4				
EA	VREFBAND_HPS	HPS_DDR					N10				HPS_A_2	HPS_CA_2				
EA	VREFBAND_HPS	HPS_DDR					B7				HPS_A_5	HPS_CA_5				
EA	VREFBAND_HPS	HPS_DDR					M10				HPS_A_3	HPS_CA_3				
EA	VREFBAND_HPS	HPS_DDR					A11				HPS_CK	HPS_CK				
EA	VREFBAND_HPS	HPS_DDR					B9				HPS_A_6	HPS_CA_6				
EA	VREFBAND_HPS	HPS_DDR					C10				HPS_CK6	HPS_CK6				
EA	VREFBAND_HPS	HPS_DDR					A9				HPS_A_7	HPS_CA_7				
EA	VREFBAND_HPS	HPS_DDR					B10				HPS_BA_1	HPS_BA_1				
EA	VREFBAND_HPS	HPS_DDR					L7				HPS_BA_0	HPS_BA_0				
EA	VREFBAND_HPS	HPS_DDR					D8				HPS_BA_2	HPS_BA_2				
EA	VREFBAND_HPS	HPS_DDR					G9				HPS_CAS6	HPS_CAS6				
EA	VREFBAND_HPS	HPS_DDR					G8				HPS_RAS6	HPS_RAS6				
EA	VREFBAND_HPS	HPS_DDR					D9				HPS_A_8	HPS_CA_8				
EA	VREFBAND_HPS	HPS_DDR					K7				HPS_A_10	HPS_CA_10				
EA	VREFBAND_HPS	HPS_DDR					C10				HPS_A_9	HPS_CA_9				
EA	VREFBAND_HPS	HPS_DDR					J7				HPS_A_11	HPS_CA_11				
EA	VREFBAND_HPS	HPS_DDR					H7				HPS_CBE_0	HPS_CBE_0				
EA	VREFBAND_HPS	HPS_DDR					F9				HPS_A_17	HPS_CA_17				
EA	VREFBAND_HPS	HPS_DDR					J9				HPS_CBE_1	HPS_CBE_1				
EA	VREFBAND_HPS	HPS_DDR					E9				HPS_A_13	HPS_CA_13				
EA	VREFBAND_HPS	HPS_DDR					D11				HPS_A_14	HPS_CA_14				
EA	VREFBAND_HPS	HPS_DDR					J8				HPS_W#	HPS_W#				
EA	VREFBAND_HPS	HPS_DDR					D10				HPS_A_15	HPS_CA_15				
EA	VREFBAND_HPS	HPS_DQZ_0					K9									
EA	VREFBAND_HPS	HPS_DDR					B12									
EA	VREFBAND_HPS	HPS_DDR					C11									
EA	VREFBAND_HPS	HPS_DDR					A12									
EA	VREFBAND_HPS	HPS_DDR					R11									
EA	VREFBAND_HPS	HPS_DDR					K10									
EA	VREFBAND_HPS	HPS_DDR					T11									
EA	VREFBAND_HPS	HPS_DDR					F10									
EA	VREFBAND_HPS	VREFBAND_HPS					J10									
EA	VREFBAND_HPS	HPS_DDR					F11									
EA	VREFBAND_HPS	HPS_DDR					G10									
EA	VREFBAND_HPS	HPS_DDR					F11									
EA	VREFBAND_HPS	HPS_DDR					H10									
EA	VREFBAND_HPS	HPS_DDR					M11									
EA	VREFBAND_HPS	HPS_DDR					C12									
EA	VREFBAND_HPS	HPS_CLK1					N11									
EA	VREFBAND_HPS	HPS_CLK2					D12									
EA	VREFBAND_HPS	TRACE_CLK					L11						TRACE_CLK			HPS_GPI048
EA	VREFBAND_HPS	TRACE_D0					K12						TRACE_D0	SPIS0_CLK	UART0_RX	HPS_GPI049
EA	VREFBAND_HPS	TRACE_D1					K11						TRACE_D1	SPIS0_MOSI	UART0_TX	HPS_GPI050
EA	VREFBAND_HPS	TRACE_D2					L12						TRACE_D2	SPIS0_MISO	I2C1_SDA	HPS_GPI051
EA	VREFBAND_HPS	TRACE_D3					H12						TRACE_D3	SPIS0_SS0	I2C1_SCL	HPS_GPI052
EA	VREFBAND_HPS	TRACE_D4					F12						TRACE_D4	SPIS1_CLK		HPS_GPI053
EA	VREFBAND_HPS	TRACE_D5					G11						TRACE_D5	SPIS1_MOSI		HPS_GPI054
EA	VREFBAND_HPS	TRACE_D6					F12						TRACE_D6	SPIS1_SS0	I2C0_SDA	HPS_GPI055
EA	VREFBAND_HPS	TRACE_D7					A13						TRACE_D7	SPIS1_MISO	I2C0_SCL	HPS_GPI056
EA	VREFBAND_HPS	SPIM0_CLK					P12						SPIM0_CLK	I2C1_SDA	UART0_CTS	HPS_GPI057
EA	VREFBAND_HPS	SPIM0_MOSI					A14						SPIM0_MOSI	I2C1_SCL	UART0_RTS	HPS_GPI058
EA	VREFBAND_HPS	SPIM0_MISO					N12						SPIM0_MISO			HPS_GPI059
EA	VREFBAND_HPS	SPIM0_SS0/IOSEL0					B15						SPIM0_SS0	UART1_RTS		HPS_GPI060
EA	VREFBAND_HPS	UART0_RX														



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DQS0 (5)	HMC pin assignment for LPDDR2 (6)	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
BD	VREFBAND0	IO			DIFF0_RX_T00n	DIFFOUT_T00n	E04	DQSnTQK0T	DQSnTQK0T							
BD	VREFBAND0	IO			DIFF0_TX_T01n	DIFFOUT_T01n	J03	DQ0T	DQ0T							
BD	VREFBAND0	IO			DIFF0_RX_T02n	DIFFOUT_T02n	F04	DQ0T	DQ0T							
BD	VREFBAND0	IO			DIFF0_RX_T03n	DIFFOUT_T03n	G04	DQ0T	DQ0T							
BD	VREFBAND0	IO			DIFF0_TX_T03n	DIFFOUT_T03n	H04	DQ0T	DQ0T							
BD	VREFBAND0	IO			DIFF0_TX_T03n	DIFFOUT_T03n	J04									
BC	VREFBAND0	IO			DIFF0_RX_T04n	DIFFOUT_T04n	I06	DQ0T	DQ0T	DQ05_EC_0	DQ05_EC_0					
BC	VREFBAND0	IO			DIFF0_RX_T04n	DIFFOUT_T04n	I05	DQ0T	DQ0T	DQ05_EC_1	DQ05_EC_1					
BC	VREFBAND0	IO			DIFF0_TX_T05n	DIFFOUT_T05n	G05	DQ0T	DQ0T	DQ05_EC_2	DQ05_EC_2					
BC	VREFBAND0	IO			DIFF0_TX_T05n	DIFFOUT_T05n	H05	DQ0T	DQ0T	DQ05_EC_2	DQ05_EC_2					
BC	VREFBAND0	IO			DIFF0_RX_T06n	DIFFOUT_T06n	N04	DQ0T	DQ0T	DQ05_EC_3	DQ05_EC_3					
BC	VREFBAND0	IO			DIFF0_RX_T06n	DIFFOUT_T06n	P04	DQ0T	DQ0T	DQ05_EC_4	DQ05_EC_4					
BC	VREFBAND0	IO			DIFF0_TX_T07n	DIFFOUT_T07n	K04	DQ0T	DQ0T	DQ05_EC_5	DQ05_EC_5					
BC	VREFBAND0	IO			DIFF0_TX_T07n	DIFFOUT_T07n	I04									
BC	VREFBAND0	IO			DIFF0_RX_T08n	DIFFOUT_T08n	A05	DQSnTQK0T	DQSnTQK0T	DQ05_EC_6	DQ05_EC_6					
BC	VREFBAND0	IO			DIFF0_RX_T08n	DIFFOUT_T08n	B05	DQSnTQK0T	DQSnTQK0T	DQ05_EC_6	DQ05_EC_6					
BC	VREFBAND0	IO			DIFF0_TX_T09n	DIFFOUT_T09n	K04	DQ0T	DQ0T	DQ05_EC_7	DQ05_EC_7					
BC	VREFBAND0	IO			DIFF0_TX_T09n	DIFFOUT_T09n	L04									
BC	VREFBAND0	IO			DIFF0_RX_T10n	DIFFOUT_T10n	D05	DQ0T	DQ0T	DQ05_EC_8	DQ05_EC_8					
BC	VREFBAND0	IO			DIFF0_RX_T10n	DIFFOUT_T10n	E05	DQ0T	DQ0T	DQ05_EC_8	DQ05_EC_8					
BC	VREFBAND0	IO			DIFF0_TX_T11n	DIFFOUT_T11n	R05	DQ0T	DQ0T	DQ05_EC_9	DQ05_EC_9					
BC	VREFBAND0	IO			DIFF0_TX_T11n	DIFFOUT_T11n	S05	DQ0T	DQ0T	DQ05_EC_9	DQ05_EC_9					
BC	VREFBAND0	IO			DIFF0_RX_T12n	DIFFOUT_T12n	C06	DQ0T	DQ0T	DQ05_EC_0	DQ05_EC_0					
BC	VREFBAND0	IO			DIFF0_RX_T12n	DIFFOUT_T12n	D06	DQ0T	DQ0T	DQ05_EC_1	DQ05_EC_1					
BC	VREFBAND0	IO			DIFF0_RX_T12n	DIFFOUT_T12n	K05	DQ0T	DQ0T	DQ05_EC_2	DQ05_EC_2					
BC	VREFBAND0	IO			DIFF0_RX_T12n	DIFFOUT_T12n	L05									
BC	VREFBAND0	IO	VREFBAND0		DIFF0_RX_T13n	DIFFOUT_T13n	D06	DQ0T	DQ0T	DQ04_EC_3	DQ04_EC_3					
BC	VREFBAND0	IO			DIFF0_RX_T13n	DIFFOUT_T13n	I07	DQ0T	DQ0T	DQ04_EC_4	DQ04_EC_4					
BC	VREFBAND0	IO			DIFF0_TX_T14n	DIFFOUT_T14n	A06	DQ0T	DQ0T	DQ04_EC_5	DQ04_EC_5					
BC	VREFBAND0	IO			DIFF0_TX_T14n	DIFFOUT_T14n	A07									
BC	VREFBAND0	IO			DIFF0_RX_T15n	DIFFOUT_T15n	M06	DQSnTQK0T	DQSnTQK0T	DQ04_EC_6	DQ04_EC_6					
BC	VREFBAND0	IO			DIFF0_RX_T15n	DIFFOUT_T15n	N06	DQSnTQK0T	DQSnTQK0T	DQ04_EC_6	DQ04_EC_6					
BC	VREFBAND0	IO			DIFF0_TX_T16n	DIFFOUT_T16n	J06	DQ0T	DQ0T	DQ04_EC_7	DQ04_EC_7					
BC	VREFBAND0	IO			DIFF0_TX_T16n	DIFFOUT_T16n	K06									
BC	VREFBAND0	IO			DIFF0_RX_T17n	DIFFOUT_T17n	F06	DQ0T	DQ0T	DQ04_EC_8	DQ04_EC_8					
BC	VREFBAND0	IO			DIFF0_RX_T17n	DIFFOUT_T17n	G06	DQ0T	DQ0T	DQ04_EC_8	DQ04_EC_8					
BC	VREFBAND0	IO			DIFF0_TX_T18n	DIFFOUT_T18n	M05	DQ0T	DQ0T	DQ04_EC_9	DQ04_EC_9					
BC	VREFBAND0	IO			DIFF0_TX_T18n	DIFFOUT_T18n	N05									
BC	VREFBAND0	IO			DIFF0_RX_T19n	DIFFOUT_T19n	P07	DQ0T	DQ0T	DQ03_EC_0	DQ03_EC_0					
BC	VREFBAND0	IO			DIFF0_RX_T19n	DIFFOUT_T19n	Q07	DQ0T	DQ0T	DQ03_EC_1	DQ03_EC_1					
BC	VREFBAND0	IO			DIFF0_TX_T20n	DIFFOUT_T20n	H07	DQ0T	DQ0T	DQ03_EC_2	DQ03_EC_2					
BC	VREFBAND0	IO			DIFF0_TX_T20n	DIFFOUT_T20n	I07									
BC	VREFBAND0	IO			DIFF0_RX_T21n	DIFFOUT_T21n	J07	DQ0T	DQ0T	DQ03_EC_3	DQ03_EC_3					
BC	VREFBAND0	IO			DIFF0_RX_T21n	DIFFOUT_T21n	K07	DQ0T	DQ0T	DQ03_EC_4	DQ03_EC_4					
BC	VREFBAND0	IO			DIFF0_TX_T22n	DIFFOUT_T22n	E07	DQ0T	DQ0T	DQ03_EC_5	DQ03_EC_5					
BC	VREFBAND0	IO			DIFF0_TX_T22n	DIFFOUT_T22n	F07									
BC	VREFBAND0	IO			DIFF0_RX_T23n	DIFFOUT_T23n	R08	DQSnTQK0T	DQSnTQK0T	DQ03_EC_6	DQ03_EC_6					
BC	VREFBAND0	IO			DIFF0_RX_T23n	DIFFOUT_T23n	S08	DQSnTQK0T	DQSnTQK0T	DQ03_EC_6	DQ03_EC_6					
BC	VREFBAND0	IO			DIFF0_TX_T24n	DIFFOUT_T24n	L07	DQ0T	DQ0T	DQ03_EC_7	DQ03_EC_7					
BC	VREFBAND0	IO			DIFF0_TX_T24n	DIFFOUT_T24n	M07	DQ0T	DQ0T	DQ03_EC_8	DQ03_EC_8					
BC	VREFBAND0	IO			DIFF0_RX_T25n	DIFFOUT_T25n	N07	DQ0T	DQ0T	DQ03_EC_9	DQ03_EC_9					
BC	VREFBAND0	IO			DIFF0_RX_T25n	DIFFOUT_T25n	O07	DQ0T	DQ0T	DQ03_EC_9	DQ03_EC_9					
BC	VREFBAND0	IO			DIFF0_TX_T26n	DIFFOUT_T26n	M08	DQ0T	DQ0T	DQ02_EC_0	DQ02_EC_0					
BC	VREFBAND0	IO			DIFF0_TX_T26n	DIFFOUT_T26n	N08	DQ0T	DQ0T	DQ02_EC_1	DQ02_EC_1					
BC	VREFBAND0	IO			DIFF0_RX_T27n	DIFFOUT_T27n	F08	DQ0T	DQ0T	DQ02_EC_2	DQ02_EC_2					
BC	VREFBAND0	IO			DIFF0_RX_T27n	DIFFOUT_T27n	G08	DQ0T	DQ0T	DQ02_EC_3	DQ02_EC_3					
BC	VREFBAND0	IO			DIFF0_TX_T28n	DIFFOUT_T28n	R09	DQSnTQK0T	DQSnTQK0T	DQ02_EC_4	DQ02_EC_4					
BC	VREFBAND0	IO			DIFF0_TX_T28n	DIFFOUT_T28n	S09	DQSnTQK0T	DQSnTQK0T	DQ02_EC_4	DQ02_EC_4					
BC	VREFBAND0	IO			DIFF0_RX_T29n	DIFFOUT_T29n	I09	DQSnTQK0T	DQSnTQK0T	DQ02_EC_5	DQ02_EC_5					
BC	VREFBAND0	IO			DIFF0_RX_T29n	DIFFOUT_T29n	J09	DQ0T	DQ0T	DQ02_EC_6	DQ02_EC_6					
BC	VREFBAND0	IO			DIFF0_TX_T30n	DIFFOUT_T30n	N09	DQ0T	DQ0T	DQ02_EC_7	DQ02_EC_7					
BC	VREFBAND0	IO			DIFF0_TX_T30n	DIFFOUT_T30n	O09	DQ0T	DQ0T	DQ02_EC_8	DQ02_EC_8					
BC	VREFBAND0	IO			DIFF0_RX_T31n	DIFFOUT_T31n	G09	DQ0T	DQ0T	DQ02_EC_9	DQ02_EC_9					
BC	VREFBAND0	IO			DIFF0_RX_T31n	DIFFOUT_T31n	H09	DQ0T	DQ0T	DQ02_EC_9	DQ02_EC_9					
BC	VREFBAND0	IO			DIFF0_TX_T32n	DIFFOUT_T32n	A09	DQ0T	DQ0T	DQ01_EC_0	DQ01_EC_0					
BC	VREFBAND0	IO			DIFF0_TX_T32n	DIFFOUT_T32n	B09	DQ0T	DQ0T	DQ01_EC_1	DQ01_EC_1					
BC	VREFBAND0	IO			DIFF0_RX_T33n	DIFFOUT_T33n	C10	DQ0T	DQ0T	DQ01_EC_2	DQ01_EC_2					
BC	VREFBAND0	IO			DIFF0_RX_T33n	DIFFOUT_T33n	D10	DQ0T	DQ0T	DQ01_EC_3	DQ01_EC_3					
BC	VREFBAND0	IO			DIFF0_TX_T34n	DIFFOUT_T34n	A10	DQ0T	DQ0T	DQ01_EC_4	DQ01_EC_4					
BC	VREFBAND0	IO			DIFF0_TX_T34n	DIFFOUT_T34n	B10	DQ0T	DQ0T	DQ01_EC_5	DQ01_EC_5					
BC	VREFBAND0	IO			DIFF0_RX_T35n	DIFFOUT_T35n	A11	DQ0T	DQ0T	DQ01_EC_6	DQ01_EC_6					
BC	VREFBAND0	IO			DIFF0_RX_T35n	DIFFOUT_T35n	B11	DQ0T	DQ0T	DQ01_EC_7	DQ01_EC_7					
BC	VREFBAND0	IO			DIFF0_TX_T36n	DIFFOUT_T36n	A12	DQ0T	DQ0T	DQ01_EC_8	DQ01_EC_8					
BC	VREFBAND0	IO			DIFF0_TX_T36n	DIFFOUT_T36n	B12	DQ0T	DQ0T	DQ01_EC_9	DQ01_EC_9					
BC	VREFBAND0	IO			DIFF0_RX_T37n	DIFFOUT_T37n	A13	DQSnTQK0T	DQSnTQK0T	DQ01_EC_0	DQ01_EC_0					
BC	VREFBAND0	IO			DIFF0_RX_T37n	DIFFOUT_T37n	B13	DQSnTQK0T	DQSnTQK0T	DQ01_EC_1	DQ01_EC_1					
BC	VREFBAND0	IO			DIFF0_TX_T38n	DIFFOUT_T38n	H11	DQ0T	DQ0T	DQ01_EC_2	DQ01_EC_2					
BC	VREFBAND0	IO			DIFF0_TX_T38n	DIFFOUT_T38n	I11	DQ0T	DQ0T	DQ01_EC_3	DQ01_EC_3					
BC	VREFBAND0	IO			DIFF0_RX_T39n	DIFFOUT_T39n	J11	DQ0T	DQ0T	DQ01_EC_4	DQ01_EC_4					
BC	VREFBAND0	IO			DIFF0_RX_T39n	DIFFOUT_T39n	K11	DQ0T	DQ0T	DQ01_EC_5	DQ01_EC_5					
BC	VREFBAND0	IO			DIFF0_TX_T40n	DIFFOUT_T40n	D11	DQ0T	DQ0T	DQ01_EC_6	DQ01_EC_6					
BC	VREFBAND0	IO			DIFF0_TX_T40n	DIFFOUT_T40n	E11	DQ0T	DQ0T	DQ01_EC_7	DQ01_EC_7					
BC	VREFBAND0	IO			DIFF0_RX_T41n	DIFFOUT_T41n	G11	DQ0T	DQ0T	DQ01_EC_8	DQ01_EC_8					
BC	VREFBAND0	IO			DIFF0_RX_T41n	DIFFOUT_T41n	H11	DQ0T	DQ0T	DQ01_EC_9	DQ01_EC_9					
BC	VREFBAND0	IO			DIFF0_TX_T42n	DIFFOUT_T42n	C12	DQ0T	DQ0T	CA_BA_0	CA_BA_0					
BC	VREFBAND0	IO			DIFF0_TX_T42n	DIFFOUT_T42n	D12	DQ0T	DQ0T	CA_BA_1	CA_BA_1					
BC	VREFBAND0	IO														



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X0/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DQS3 (5)	HMC pin assignment for PDS2 (6)	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
BA	VREFBAND	I0			DIFFIO_TX_T112n	DIFFFOLUT_T112n	G32									
BA	VREFBAND	I0	CL20B0		DIFFIO_RX_T113p	DIFFFOLUT_T113p	G34	DQ11T								
BA	VREFBAND	I0	CL20B0		DIFFIO_RX_T113p	DIFFFOLUT_T113p	G34	DQ11T								
BA	VREFBAND	I0			DIFFIO_TX_T114p	DIFFFOLUT_T114p	E33	DQ11T								
BA	VREFBAND	I0			DIFFIO_TX_T114n	DIFFFOLUT_T114n	F33									
BA		MSEL0	RZQ_6	MSEL0			H35									
BA		MSEL1		MSEL1			A34									
BA		MSEL2		MSEL2			D35									
BA		MSEL3		MSEL3			A37									
BA		MSEL4		MSEL4			IP34									
BA		CONF_DONE		CONF_DONE			K35									
BA		hSTATUS		hSTATUS			F35									
BA		hCE		hCE			M35									
BA		KCONFG0		KCONFG0			A36									
		GND					P35									
		VCC_IOPS					V16									
		GND					W16									
		GND					AA33									
		GND					AA35									
		GND					AA38									
		GND					AA39									
		GND					AB31									
		GND					AB32									
		GND					AB34									
		GND					AB36									
		GND					AB37									
		GND					AC33									
		GND					AC38									
		GND					AC39									
		GND					AD32									
		GND					AD36									
		GND					AD37									
		GND					AE33									
		GND					AE35									
		GND					AE38									
		GND					AE39									
		GND					AF31									
		GND					AF32									
		GND					AF34									
		GND					AF36									
		GND					AG37									
		GND					AG38									
		GND					AG39									
		GND					AH33									
		GND					AH33									
		GND					AH34									
		GND					AH35									
		GND					AH36									
		GND					AM37									
		GND					AL35									
		GND					AJ38									
		GND					AJ39									
		GND					AK36									
		GND					AK37									
		GND					AK38									
		GND					AL38									
		GND					AL39									
		GND					AM38									
		GND					AM37									
		GND					AN35									
		GND					AN38									
		GND					AN39									
		GND					AP38									
		GND					AP39									
		GND					AP35									
		GND					AP38									
		GND					AP39									
		GND					AT36									
		GND					AT37									
		GND					AU35									
		GND					AU38									
		GND					AV39									
		GND					AV35									
		GND					AV38									
		GND					AV37									
		GND					AV38									
		GND					AV39									
		GND					AV35									
		GND					AV38									
		GND					BA36									
		GND					B37									
		GND					C35									
		GND					C38									
		GND					C39									
		GND					D36									
		GND					D37									
		GND					E35									
		GND					E38									
		GND					E39									
		GND					F36									
		GND					F37									
		GND					G35									
		GND					G38									
		GND					G39									
		GND					H35									
		GND					H37									
		GND					J35									
		GND					J38									
		GND					J39									
		GND					K36									
		GND					K37									
		GND					L36									
		GND					L39									
		GND					M35									
		GND					M37									
		GND					N35									
		GND					N38									
		GND					N39									
		GND					P36									
		GND					P37									
		GND					R34									
		GND					R38									
		GND					R39									
		GND					T32									
		GND					T38									
		GND					T37									
		GND					U33									
		GND					U35									
		GND					U36									
		GND					U39									
		GND					V32									
		GND					V34									
		GND					V36									
		GND					V37									
		GND					W33									
		GND					W38									
		GND					W39									
		GND					Y31									
		GND					Y32									



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DQS3 (5)	HMC pin assignment for PDS2 (6)	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					Y36									
		GND					Y35									
		GND					AA3									
		GND					AA4									
		GND					AA5									
		GND					AA6									
		GND					AB1									
		GND					AB2									
		GND					AB7									
		GND					AC3									
		GND					AC4									
		GND					AC8									
		GND					AD1									
		GND					AD2									
		GND					AD5									
		GND					AD7									
		GND					AE3									
		GND					AE4									
		GND					AE5									
		GND					AE8									
		GND					AF1									
		GND					AF2									
		GND					AP9									
		GND					AG3									
		GND					AG4									
		GND					AG5									
		GND					AG6									
		GND					AG7									
		GND					AG8									
		GND					AH1									
		GND					AH2									
		GND					AH5									
		GND					AL3									
		GND					AL4									
		GND					AK1									
		GND					AK2									
		GND					AK5									
		GND					AL3									
		GND					AL4									
		GND					AM1									
		GND					AM2									
		GND					AM5									
		GND					AN3									
		GND					AN4									
		GND					AP1									
		GND					AP2									
		GND					AP5									
		GND					AR3									
		GND					AR4									
		GND					AT1									
		GND					AT2									
		GND					AT5									
		GND					AT3									
		GND					AU4									
		GND					AV1									
		GND					AV2									
		GND					N3									
		GND					N4									
		GND					P1									
		GND					P2									
		GND					PS									
		GND					R3									
		GND					R4									
		GND					RS									
		GND					T1									
		GND					T2									
		GND					TS									
		GND					U3									
		GND					U4									
		GND					U5									
		GND					U6									
		GND					V1									
		GND					V2									
		GND					V7									
		GND					W3									
		GND					W4									
		GND					W8									
		GND					Y1									
		GND					Y2									
		GND					Y8									
		GND					Y7									
		VCCP					AB21									
		VCCP					AB25									
		VCCP					AB15									
		VCCP					U10									
		VCCP					U16									
		VCCP					V25									
		VCCP					V27									
		VCCP					W10									
		VCCP					V27									
		VCCA_FPLL					AC30									
		VCCA_FPLL					AD9									
		VCCA_FPLL					Y30									
		VCCA_FPLL					AA8									
		VCCA_FPLL					V31									
		VCCP_HPS					U8									
		VCCP_HPS					R33									
		VCC_AUX					AB14									
		VCC_AUX					AB8									
		VCC_AUX					U28									
		VCC_AUX_SHARED					U15									
		VCCD_FPLL					AB1									
		VCCD_FPLL					AB9									
		VCCD_FPLL					W30									
		VCCD_FPLL					W9									
		VCCD_FPLL					T31									
		VCCA_GXBLO					AF33									
		VCCA_GXBRO					AE7									
		VCCA_GXB1					AB33									
		VCCA_GXB1					AB7									
		VCCA_GXB2					V33									
		VCCD_GXBLO					AD33									
		VCCD_GXBRO					AE7									
		VCCD_GXB1					Y33									
		VCCD_GXB1					W7									
		VCCD_GXB2					T33									
		VCCD_GXBLO					AD34									
		VCCD_GXBLO					AD35									
		VCCD_GXBRO					AE5									
		VCCD_GXBRO					AE6									
		VCCD_GXB1					Y34									
		VCCD_GXB1					Y35									
		VCCD_GXB1					W5									
		VCCD_GXB1					W6									
		VCCD_GXB2					T34									
		VCCD_GXB2					T35									
		VCCD_GXB1					U34									
		VCCD_GXB1					W34									
		VCCD_GXB1					AA34									
		VCCD_GXB1					AB35									



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F157 (4)	DQ5 for X8/X9	DQ5 for X16/X18	DQ5 for X32/X36	HMC pin assignment for DQ53 (5)	HMC pin assignment for LPOD52	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCCIOBA					G33									
		VCCIOBA					K31									
		VCCIOBA					K31									
		VCCIOBA					P33									
		VCCIOBB					E38									
		VCCIOBB					E30									
		VCCIOBB					H30									
		VCCIOBB					K28									
		VCCIOBC					C25									
		VCCIOBC					D27									
		VCCIOBC					F25									
		VCCIOBC					G27									
		VCCIOBC					J26									
		VCCIOBC					M24									
		VCCIOBD					G21									
		VCCIOBD					D32									
		VCCIOBD					F21									
		VCCIOBD					G22									
		VCCIOBD					H22									
		VCCIOBD					M21									
		VCCPD3					AA27									
		VCCPD3					AA28									
		VCCPD3					AA29									
		VCCPD3					AB22									
		VCCPD3					AB23									
		VCCPD3					AB24									
		VCCPD3					AB25									
		VCCPD4A					AE10									
		VCCPD4A					AE10									
		VCCPD4B					AB12									
		VCCPD4B					AB13									
		VCCPD4B					AB16									
		VCCPD4B					AB18									
		VCCPD4B					AB19									
		VCCPD6AB_HPS					L9									
		VCCPD6AB_HPS					T10									
		VCCPD6AB_HPS					T6									
		VCCPD6AB_HPS					T8									
		VCCPD7A_HPS					R12									
		VCCPD7B_HPS					T14									
		VCCPD7C_HPS					P16									
		VCCPD7D_HPS					T17									
		VCCPD7E_HPS					R18									
		VCCPD7E_C					U21									
		VCCPD8					R32									
		VCCPD8					T30									
		VCCPD8					U22									
		VCCPD8					U24									
		VCCPD8					U26									
		VCCPD8					U29									
		VCCPD8M					J19									
		VCCPD8M					AE29									
		VCCPD8M_CLK_HPS					L10									
		VCC_HPS					T13									
		VCC_LPS					U14									
		VCC_LPS					U9									
		VCC_LPS					V10									
	VREFB7A7B7C7D7E0_HPS	VREFB7A7B7C7D7E0_HPS					P14									
		GND					AA11									
		GND					AA13									
		GND					AA15									
		GND					AA17									
		GND					AA19									
		GND					AA23									
		GND					AA30									
		GND					AB10									
		GND					AE11									
		GND					AF14									
		GND					AE17									
		GND					AE20									
		GND					AF23									
		GND					AE26									
		GND					AE28									
		GND					AB20									
		GND					AE30									
		GND					AE11									
		GND					AE14									
		GND					AF17									
		GND					AE20									
		GND					AE23									
		GND					AF26									
		GND					AE28									
		GND					AF30									
		GND					AG31									
		GND					AG3									
		GND					AJ11									
		GND					AJ14									
		GND					AJ17									
		GND					AJ20									
		GND					AK23									
		GND					AJ26									
		GND					AJ29									
		GND					AK32									
		GND					AJ38									
		GND					AM11									
		GND					AM14									
		GND					AM17									
		GND					AM20									
		GND					AM23									
		GND					AM26									
		GND					AM29									
		GND					AM38									
		GND					AM11									
		GND					AR14									
		GND					AR17									
		GND					AR20									
		GND					AR23									
		GND					AR26									
		GND					AR29									
		GND					AR32									
		GND					AR8									
		GND					AV11									
		GND					AV14									
		GND					AV17									
		GND					AV20									
		GND					AV23									
		GND					AV26									
		GND					AV29									
		GND					AV32									
		GND					AV38									
		GND					B11									
		GND					B16									
		GND					B2									
		GND					B20									
		GND					B23									
		GND					B26									
		GND					B29									



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DQS3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					B02									
		GND					B5									
		GND					B6									
		GND					E11									
		GND					E17									
		GND					E2									
		GND					E20									
		GND					E23									
		GND					E26									
		GND					E29									
		GND					E32									
		GND					E5									
		GND					E8									
		GND					F14									
		GND					H11									
		GND					H17									
		GND					H2									
		GND					H20									
		GND					H23									
		GND					H26									
		GND					H29									
		GND					H32									
		GND					H5									
		GND					H8									
		GND					H21									
		GND					H24									
		GND					K20									
		GND					L1									
		GND					L17									
		GND					L2									
		GND					L23									
		GND					L26									
		GND					L29									
		GND					L32									
		GND					L6									
		GND					L8									
		GND					N14									
		GND					N17									
		GND					N20									
		GND					P11									
		GND					P23									
		GND					P26									
		GND					P29									
		GND					P32									
		GND					P6									
		GND					W21									
		GND					T12									
		GND					T15									
		GND					T16									
		GND					T18									
		GND					T20									
		GND					T9									
		GND					U11									
		GND					U13									
		GND					U17									
		GND					U23									
		GND					U26									
		GND					U27									
		GND					U30									
		GND					U7									
		GND					V14									
		GND					V8									
		GND					V18									
		GND					V21									
		GND					V24									
		GND					V26									
		GND					V28									
		GND					V30									
		GND					V8									
		GND					W27									
		GND					W11									
		GND					W13									
		GND					W15									
		GND					W17									
		GND					W19									
		GND					W23									
		GND					W25									
		GND					W29									
		GND					V10									
		GND					V12									
		GND					V14									
		GND					V16									
		GND					V18									
		GND					V20									
		GND					V22									
		GND					V24									
		GND					V26									
		GND					V28									

Notes:
(1) For more information about pin definitions and pin connection guidelines, refer to the [Arria V Device Family Pin Connection Guidelines](#).
(2) GND_AREFCLK pin is not supported in current Quartus II version, but will be supported in future Quartus II release version.
(3) Pins with * contains similar name with other pins in the same column. For the selection of the "HPS Pin Mux Select x" columns.
(4) Pins with # are the 10 Gbps transceiver channels. For more information about the 10 Gbps transceiver channels clocking recommendation, refer to the [Transceiver Clocking in Arria V Devices](#) chapter.
(5) RESET pin is only applicable for DDR3 device.



**Pin Information for the Arria® V 5ASXMB3 Device
Version 1.3**

Version Number	Date	Changes Made
1.0	4/19/2013	Initial release.
1.1	9/30/2014	Remove corresponding bank number from VCCRSTCLK_HPS pin.
1.2	7/31/2015	Renamed the following columns: - Renamed "DDR3/DDR2 hard memory PHY" to "HMC pin assignment for DDR3". - Renamed "LPDDR2 hard memory PHY" to "HMC pin assignment for LPDDR2".
1.3	12/23/2016	-Renamed SDMMC_FB_CLK_IN to HPS_GPIO44.