Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16
GXB_L1		REFCLK1Ln					F5		
GXB_L1		REFCLK1Lp					G4		
GXB_L1		GXB_TX_L5n					D3		
GXB_L1		GXB_TX_L5p					D4		
GXB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					C2		
GXB_L1		GXB_RX_L5n,GXB_REFCLK_L5n					C1		
GXB_L1		GXB_TX_L4n					E1		
GXB_L1		GXB_TX_L4p					E2		
GXB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					G2		
GXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					G1		
GXB_L1		GXB_TX_L3n					J1		
GXB_L1		GXB_TX_L3p					J2		
GXB_L1		GXB_RX_L3p,GXB_REFCLK_L3p					L2		
GXB_L1		GXB_RX_L3n,GXB_REFCLK_L3n					L1		
GXB_L0		GXB_TX_L2n					N1		
GXB_L0		GXB_TX_L2p					N2		
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					R2		
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					R1		
GXB_L0		GXB_TX_L1n					U1		
GXB_L0		GXB_TX_L1p					U2		
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					W2		
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					W1		
GXB_L0		GXB_TX_L0n					Y3		
GXB_L0		GXB_TX_L0p					Y4		
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AA2		
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AA1		
GXB_L0		REFCLK0Lp					V4		
GXB_L0		REFCLK0Ln					U4		
3A		TDO		TDO			M5		
3A		nCSO		DATA4			R4		
3A		TMS		TMS			P5		
3A		AS_DATA3		DATA3			T4		
3A		TCK		TCK			V5		
3A		AS_DATA2		DATA2			AA5		
3A		TDI		TDI			W5		
3A		AS_DATA1		DATA1			AB3		
3A		DCLK		DCLK			V3		
3A		AS_DATA0,ASDO		DATA0			AB4		
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	R6	DQ1B	
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	U7		
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	R5	DQ1B	
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	U8	DQ1B	
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	P6	DQSn1B	
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	W8	DQ1B	
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	N6	DQS1B	
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	W9		
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	T7	DQ1B	
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	U6	DQ1B	
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	T8	DQ1B	
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	V6	DQ1B	
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	M6		
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	R7	DQ1B	
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	M7		
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	P7	DQ1B	
3B	VREFB3BN0	IO			DIFFIO_RX_B9n	DIFFOUT_B9n	AB6		
3B	VREFB3BN0	IO			DIFFIO_RX_B10n	DIFFOUT_B10n	V9	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B9p	DIFFOUT_B9p	AB5	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B10p	DIFFOUT_B10p	V10	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	P8	DQSn2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B12n	DIFFOUT_B12n	AA7	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	N8	DQS2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AB7		
3B	VREFB3BN0	IO			DIFFIO_TX_B13n	DIFFOUT_B13n	AA8	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B14n	DIFFOUT_B14n	T9	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B13p	DIFFOUT_B13p	AB8	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B14p	DIFFOUT_B14p	U10	DQ2B	
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B15n	DIFFOUT_B15n	M8		
3B	VREFB3BN0	IO			DIFFIO_TX_B16n	DIFFOUT_B16n	AA10	DQ2B	
3B	VREFB3BN0	IO	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B15p	DIFFOUT_B15p	M9		
3B	VREFB3BN0	IO			DIFFIO_TX_B16p	DIFFOUT_B16p	AA9	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B17n	DIFFOUT_B17n	Y10		

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16
3B	VREFB3BN0	IO			DIFFIO_RX_B18n	DIFFOUT_B18n	T10	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_TX_B17p	DIFFOUT_B17p	Y9	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B18p	DIFFOUT_B18p	R9	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	U11	DQSn3B	
3B	VREFB3BN0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	R12	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	U12	DQS3B	
3B	VREFB3BN0	IO			DIFFIO_TX_B20p	DIFFOUT_B20p	P12		
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B21n	DIFFOUT_B21n	AB10	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B22n	DIFFOUT_B22n	R10	DQ3B	
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B21p	DIFFOUT_B21p	AB11	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B22p	DIFFOUT_B22p	R11	DQ3B	
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B23n	DIFFOUT_B23n	P9		
3B	VREFB3BN0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	Y11	DQ3B	
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B23p	DIFFOUT_B23p	N9		
3B	VREFB3BN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	AA12	DQ3B	
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B25n	DIFFOUT_B25n	AB13		
4A	VREFB4AN0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	V13	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B25p	DIFFOUT_B25p	AB12	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	U13	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	T12	DQSn4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AA14	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	T13	DQS4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AA13		
4A	VREFB4AN0	IO			DIFFIO_TX_B29n	DIFFOUT_B29n	AB15	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	Y14	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B29p	DIFFOUT_B29p	AA15	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	Y15	DQ4B	
4A	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B31n	DIFFOUT_B31n	V14		
4A	VREFB4AN0	IO			DIFFIO_TX_B32n	DIFFOUT_B32n	AB17	DQ4B	
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B31p	DIFFOUT_B31p	V15		
4A	VREFB4AN0	IO			DIFFIO_TX_B32p	DIFFOUT_B32p	AB18	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AB20		
4A	VREFB4AN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	Y16	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AB21	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	Y17	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	T14	DQSn5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B36n	DIFFOUT_B36n	AA17	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	U15	DQS5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	AA18		
4A	VREFB4AN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AA19	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	V20	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	AA20	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	W19	DQ5B	DQ1B
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B39n	DIFFOUT_B39n	V16		
4A	VREFB4AN0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	AB22	DQ5B	DQ1B
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B39p	DIFFOUT_B39p	W16		
4A	VREFB4AN0	IO			DIFFIO_TX_B40p	DIFFOUT_B40p	AA22	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B41n	DIFFOUT_B41n	Y22		
4A	VREFB4AN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	Y20	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	W22	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	Y19	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	P14	DQSn6B	DQSn1B
4A	VREFB4AN0	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	Y21	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	R14	DQS6B	DQS1B
4A	VREFB4AN0	IO			DIFFIO_TX_B44p	DIFFOUT_B44p	W21		
4A	VREFB4AN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	U22	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	V19	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	V21	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	V18	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B47n	DIFFOUT_B47n	U16		
4A	VREFB4AN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	U21	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B47p	DIFFOUT_B47p	U17		
4A	VREFB4AN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	U20	DQ6B	DQ1B
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	T19	DQ1R	
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	T18		
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	T20	DQ1R	
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	T17		
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	T22	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	T15	DQ1R	
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	R22	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	R15	DQ1R	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	R21		
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	R16	DQS1R	
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	P22	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R6n	R17	DQSn1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	P19	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	P16	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	P18		
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	P17	DQ1R	
5B	VREFB5BN0	IO	CLK6p		DIFFIO_RX_R17p	DIFFOUT_R17p	N16		
5B	VREFB5BN0	IO			DIFFIO_TX_R18p	DIFFOUT_R18p	N20	DQ2R	
5B	VREFB5BN0	IO	CLK6n		DIFFIO_RX_R17n	DIFFOUT_R17n	M16		
5B	VREFB5BN0	IO			DIFFIO_TX_R18n	DIFFOUT_R18n	N21	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R19p	DIFFOUT_R19p	N19	DQ2R	
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R20p	DIFFOUT_R20p	M22	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R19n	DIFFOUT_R19n	M18	DQ2R	
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R20n	DIFFOUT_R20n	L22	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R21p	DIFFOUT_R21p	K17	DQS2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R22p	DIFFOUT_R22p	M20		
5B	VREFB5BN0	IO			DIFFIO_RX_R21n	DIFFOUT_R21n	L17	DQSn2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R22n	DIFFOUT_R22n	M21	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R23p	DIFFOUT_R23p	L19	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R24p	DIFFOUT_R24p	K21	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	L18	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R24n	DIFFOUT_R24n	K22		
7A		GND					F17		
7A	VREFB7AN0	IO			DIFFIO_RX_T1p	DIFFOUT_T1p	H21		
7A	VREFB7AN0	IO			DIFFIO_TX_T2p	DIFFOUT_T2p	E21	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	G21		
7A	VREFB7AN0	IO			DIFFIO_TX_T2n	DIFFOUT_T2n	D21	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T3p	E19	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T4p	DIFFOUT_T4p	C20	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T3n	D19	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T4n	DIFFOUT_T4n	B20	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T5p	J21	DQS1T	DQS1T
7A	VREFB7AN0	IO			DIFFIO_TX_T6p	DIFFOUT_T6p	B18		
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T5n	J22	DQSn1T	DQSn1T
7A	VREFB7AN0	IO			DIFFIO_TX_T6n	DIFFOUT_T6n	B17	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T7p	C21	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T8p	DIFFOUT_T8p	G22	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T7n	B21	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T8n	DIFFOUT_T8n	F22		
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T9p	G20		
7A	VREFB7AN0	IO			DIFFIO_TX_T10p	DIFFOUT_T10p	E22	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T9n	H20		
7A	VREFB7AN0	IO			DIFFIO_TX_T10n	DIFFOUT_T10n	D22	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T11p	DIFFOUT_T11p	C19	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T12p	DIFFOUT_T12p	B22	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T11n	DIFFOUT_T11n	C18	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T12n	DIFFOUT_T12n	A22	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T13p	DIFFOUT_T13p	F19	DQS2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T14p	DIFFOUT_T14p	E20		
7A	VREFB7AN0	IO			DIFFIO_RX_T13n	DIFFOUT_T13n	F18	DQSn2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T14n	DIFFOUT_T14n	F20	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T15p	DIFFOUT_T15p	A18	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T16p	DIFFOUT_T16p	A20	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	A17	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T16n	DIFFOUT_T16n	A19		
7A	VREFB7AN0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	K20		
7A	VREFB7AN0	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	B16	DQ3T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	K19		
7A	VREFB7AN0	IO			DIFFIO_TX_T18n	DIFFOUT_T18n	C16	DQ3T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	D17	DQ3T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	G17	DQ3T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	E16	DQ3T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	G16	DQ3T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	G18	DQS3T	DQS2T
7A	VREFB7AN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	J19		
7A	VREFB7AN0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	H18	DQSn3T	DQSn2T
7A	VREFB7AN0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	J18	DQ3T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	E15	DQ3T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	A15	DQ3T	DQ2T

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16
7A	VREFB7AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	F15	DQ3T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_TX_T24n	DIFFOUT_T24n	A14		
7A	VREFB7AN0	IO	CLK11p		DIFFIO_RX_T25p	DIFFOUT_T25p	H16		
7A	VREFB7AN0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	J17	DQ4T	DQ2T
7A	VREFB7AN0	IO	CLK11n		DIFFIO_RX_T25n	DIFFOUT_T25n	H15		
7A	VREFB7AN0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	K16	DQ4T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	C15	DQ4T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	G15	DQ4T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	B15	DQ4T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	F14	DQ4T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	H14	DQS4T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	B13		
7A	VREFB7AN0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	J13	DQSn4T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	A13	DQ4T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	E14	DQ4T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	J11	DQ4T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	F13	DQ4T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	H10		
7A	VREFB7AN0	IO	CLK10p		DIFFIO_RX_T33p	DIFFOUT_T33p	H13		
7A	VREFB7AN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	G11	DQ5T	
7A	VREFB7AN0	IO	CLK10n		DIFFIO_RX_T33n	DIFFOUT_T33n	G13		
7A	VREFB7AN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	F12	DQ5T	
7A	VREFB7AN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	D13	DQ5T	
7A	VREFB7AN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	B12	DQ5T	
7A	VREFB7AN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	C13	DQ5T	
7A	VREFB7AN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	A12	DQ5T	
7A	VREFB7AN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	H11	DQS5T	
7A	VREFB7AN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	L8		
7A	VREFB7AN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	G12	DQSn5T	
7A	VREFB7AN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	K9	DQ5T	
7A	VREFB7AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	D12	DQ5T	
7A	VREFB7AN0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	C11	DQ5T	
7A	VREFB7AN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	E12	DQ5T	
7A	VREFB7AN0	IO	RZQ_2		DIFFIO_TX_T40n	DIFFOUT_T40n	B11		
8A	VREFB8AN0	IO	CLK9p		DIFFIO_RX_T41p	DIFFOUT_T41p	G10		
8A	VREFB8AN0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	L7	DQ6T	
8A	VREFB8AN0	IO	CLK9n		DIFFIO_RX_T41n	DIFFOUT_T41n	F10		
8A	VREFB8AN0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	K7	DQ6T	
8A	VREFB8AN0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	J7	DQ6T	
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T44p	DIFFOUT_T44p	H8	DQ6T	
8A	VREFB8AN0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	J8	DQ6T	
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T44n	DIFFOUT_T44n	G8	DQ6T	
8A	VREFB8AN0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	J9	DQS6T	
8A	VREFB8AN0	IO			DIFFIO_TX_T46p	DIFFOUT_T46p	A10		
8A	VREFB8AN0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	H9	DQSn6T	
8A	VREFB8AN0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	A9	DQ6T	
8A	VREFB8AN0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	B10	DQ6T	
8A	VREFB8AN0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	A5	DQ6T	
8A	VREFB8AN0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	C9	DQ6T	
8A	VREFB8AN0	IO			DIFFIO_TX_T48n	DIFFOUT_T48n	B5		
8A	VREFB8AN0	IO	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T49p	DIFFOUT_T49p	E10		
8A	VREFB8AN0	IO			DIFFIO_TX_T50p	DIFFOUT_T50p	B6	DQ7T	
8A	VREFB8AN0	IO	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T49n	DIFFOUT_T49n	F9		
8A	VREFB8AN0	IO			DIFFIO_TX_T50n	DIFFOUT_T50n	B7	DQ7T	
8A	VREFB8AN0	IO			DIFFIO_RX_T51p	DIFFOUT_T51p	A8	DQ7T	
8A	VREFB8AN0	IO			DIFFIO_TX_T52p	DIFFOUT_T52p	C6	DQ7T	
8A	VREFB8AN0	IO			DIFFIO_RX_T51n	DIFFOUT_T51n	A7	DQ7T	
8A	VREFB8AN0	IO			DIFFIO_TX_T52n	DIFFOUT_T52n	D6	DQ7T	
8A	VREFB8AN0	IO			DIFFIO_RX_T53p	DIFFOUT_T53p	E9	DQS7T	
8A	VREFB8AN0	IO			DIFFIO_TX_T54p	DIFFOUT_T54p	D7		
8A	VREFB8AN0	IO			DIFFIO_RX_T53n	DIFFOUT_T53n	D9	DQSn7T	
8A	VREFB8AN0	IO			DIFFIO_TX_T54n	DIFFOUT_T54n	C8	DQ7T	
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	G6	DQ7T	
8A	VREFB8AN0	IO			DIFFIO_TX_T56p	DIFFOUT_T56p	F7	DQ7T	
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	H6	DQ7T	
8A	VREFB8AN0	IO			DIFFIO_TX_T56n	DIFFOUT_T56n	E7		
9A		MSEL0		MSEL0			L6		
9A		CONF_DONE		CONF_DONE			K6		
9A		MSEL1		MSEL1			J6		
9A		nSTATUS		nSTATUS			H5		
9A		nCE		nCE			G5		

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16
9A		MSEL2		MSEL2			A2		
9A		MSEL3		MSEL3			E5		
9A		nCONFIG		nCONFIG			A4		
9A		MSEL4		MSEL4			F3		
9A		GND					C5		
		GND					AB19		
		GND					AB14		
		GND					AB9		
		GND					AB2		
		GND					AB1		
		GND					AA11		
		GND					AA6		
		GND					AA4		
		GND					AA3		
		GND					Y18		
		GND					Y5		
		GND					Y2		
		GND					Y1		
		GND					W4		
		GND					W3		
		GND					V22		
		GND					V17		
		GND					V12		
		GND					V7		
		GND					V2		
		GND					V1		
		GND					U9		
		GND					U5		
		GND					U3		
		GND					T21		
		GND					T16		
		GND					T2		
		GND					T1		
		GND					R13		
		GND					R3		
		GND					P10		
		GND					P4		
		GND					P2		
		GND					P1		
		GND					N22		
		GND					N17		
		GND					N15		
		GND					N13		
		GND					N11		
		GND					N7		
		GND					N5		
		GND					N3		
		GND					M14		
		GND					M12		
		GND					M10		
		GND					M4		
		GND					M2		
		GND					M1		
		GND					L21		
		GND					L15		
		GND					L13		
		GND					L11		
		GND					L5		
		GND					L3		
		GND					K14		
		GND					K12		
		GND					K10		
		GND					K8		
		GND					K4		
		GND					K2		
		GND					K1		
		GND					J20		
		GND					J15		
		GND					J5		
		GND					J3		
		GND					H22		

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16
		GND					H12		
		GND					H7		
		GND					H4		
		GND					H3		
		GND					H2		
		GND					H1		
		GND					G19		
		GND					G9		
		GND					G3		
		GND					F16		
		GND					F6		
		GND					F2		
		GND					F1		
		GND					E13		
		GND					E4		
		GND					E3		
		GND					D20		
		GND					D10		
		GND					D5		
		GND					D2		
		GND					D1		
		GND					C17		
		GND					C4		
		GND					C3		
		GND					B14		
		GND					B9		
		GND					B2		
		GND					B1		
		GND					A21		
		GND					A11		
		VCC					P15		
		VCC					P13		
		VCC					P11		
		VCC					N14		
		VCC					N12		
		VCC					N10		
		VCC					M15		
		VCC					M13		
		VCC					M11		
		VCC					L16		
		VCC					L14		
		VCC					L12		
		VCC					L10		
		VCC					K15		
		VCC					K13		
		VCC					K11		
		VCC					J16		
		VCC					J14		
		VCC					J12		
		VCC					J10		
		DNU					B3		
		DNU					B4		
		DNU					E17		
		DNU					L9		
		VCCPGM					V8		
		VCCPGM					R19		
		VCCPGM					F8		
		VCCBAT					A3		
		VCCIO3A					T6		
		VCCIO3A					Y8		
		VCCIO3B					Y13		
		VCCIO3B					W10		
		VCCIO3B					T11		
		VCCIO3B					R8		
		VCCIO4A					U19		
		VCCIO4A					AA21		
		VCCIO4A					AA16		
		VCCIO4A					W20		
		VCCIO4A					W15		
		VCCIO4A					U14		
		VCCIO5A					R18		

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16
		VCCIO5A					P20		
		VCCIO5B					M19		
		VCCIO5B					K18		
		VCCIO7A					B19		
		VCCIO7A					H17		
		VCCIO7A					G14		
		VCCIO7A					F21		
		VCCIO7A					F11		
		VCCIO7A					E18		
		VCCIO7A					D15		
		VCCIO7A					C22		
		VCCIO7A					C12		
		VCCIO7A					A16		
		VCCIO8A					A6		
		VCCIO8A					G7		
		VCCIO8A					E8		
		VCCIO8A					C7		
		VCCPD3A					W6		
		VCCPD3B4A					W17		
		VCCPD3B4A					W14		
		VCCPD3B4A					W12		
		VCCPD3B4A					W11		
		VCCPD5A					P21		
		VCCPD5B					N18		
		VCCPD5B					M17		
		VCCPD7A8A					E11		
		VCCPD7A8A					D16		
		VCCPD7A8A					D14		
		VCCPD7A8A					D8		
		VCCPD7A8A					C10		
3A	VREFB3AN0	VREFB3AN0					Y7		
3B	VREFB3BN0	VREFB3BN0					Y12		
4A	VREFB4AN0	VREFB4AN0					AB16		
5A	VREFB5AN0	VREFB5AN0					R20		
5B	VREFB5BN0	VREFB5BN0					L20		
7A	VREFB7AN0	VREFB7AN0					C14		
8A	VREFB8AN0	VREFB8AN0					B8		
		NC					Y6		
		NC					V11		
		VCCH_GXBL					M3		
		VCCH_GXBL					T3		
		VCCL_GXBL					P3		
		VCCL_GXBL					K3		
		RREF_TL					A1		
		VCCA_FPLL					T5		
		VCCA_FPLL					F4		
		VCCA_FPLL					U18		
		VCCA_FPLL					H19		
		VCC_AUX					E6		
		VCC_AUX					D18		
		VCC_AUX					W18		
		VCC_AUX					W13		
		VCC_AUX					W7		
		VCC_AUX					D11		
		VCCE_GXBL					L4		
		VCCE_GXBL					N4		
		VCCE_GXBL					K5		
		VCCE_GXBL					J4		

Note:
(1) For more information about pin definition and pin connection guidelines, refer to the
Cyclone V Device Family Pin Connection Guidelines.

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16
GXB_L1		REFCLK1Ln					G4		
GXB_L1		REFCLK1Lp					F5		
GXB_L1		GXB_TX_L5n					D3		
GXB_L1		GXB_TX_L5p					D4		
GXB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					C2		
GXB_L1		GXB_RX_L5n,GXB_REFCLK_L5n					C1		
GXB_L1		GXB_TX_L4n					E1		
GXB_L1		GXB_TX_L4p					E2		
GXB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					G2		
GXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					G1		
GXB_L1		GXB_TX_L3n					J1		
GXB_L1		GXB_TX_L3p					J2		
GXB_L1		GXB_RX_L3p,GXB_REFCLK_L3p					L2		
GXB_L1		GXB_RX_L3n,GXB_REFCLK_L3n					L1		
GXB_L0		GXB_TX_L2n					N1		
GXB_L0		GXB_TX_L2p					N2		
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					R2		
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					R1		
GXB_L0		GXB_TX_L1n					U1		
GXB_L0		GXB_TX_L1p					U2		
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					W2		
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					W1		
GXB_L0		GXB_TX_L0n					Y3		
GXB_L0		GXB_TX_L0p					Y4		
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AA2		
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AA1		
GXB_L0		REFCLK0Lp					V4		
GXB_L0		REFCLK0Ln					U4		
3A		TDO		TDO			V3		
3A		nCSO		DATA4			AB6		
3A		TMS		TMS			R4		
3A		AS_DATA3		DATA3			AA5		
3A		TCK		TCK			V5		
3A		AS_DATA2		DATA2			T5		
3A		TDI		TDI			P5		
3A		AS_DATA1		DATA1			W5		
3A		DCLK		DCLK			M5		
3A		AS_DATA0,ASDO		DATA0			AB4		
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	P6	DQ1B	
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	U7		
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	N6	DQ1B	
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	U6	DQ1B	
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	M6	DQSn1B	
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	R5	DQ1B	
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	M7	DQS1B	
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	R6		
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	R7	DQ1B	
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	L7	DQ1B	
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	T7	DQ1B	
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	L8	DQ1B	
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	T8		
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	P7	DQ1B	
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	T9		
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	P8	DQ1B	
3B	VREFB3BN0	IO			DIFFIO_TX_B9n	DIFFOUT_B9n	V8		
3B	VREFB3BN0	IO			DIFFIO_RX_B10n	DIFFOUT_B10n	N8	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B9p	DIFFOUT_B9p	W8	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B10p	DIFFOUT_B10p	M8	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	N9	DQSn2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B12n	DIFFOUT_B12n	AA7	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	N10	DQS2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AB7		
3B	VREFB3BN0	IO			DIFFIO_TX_B13n	DIFFOUT_B13n	Y7	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B14n	DIFFOUT_B14n	U8	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B13p	DIFFOUT_B13p	W7	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B14p	DIFFOUT_B14p	V9	DQ2B	
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B15n	DIFFOUT_B15n	R9		
3B	VREFB3BN0	IO			DIFFIO_TX_B16n	DIFFOUT_B16n	AB8	DQ2B	
3B	VREFB3BN0	IO	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B15p	DIFFOUT_B15p	P9		
3B	VREFB3BN0	IO			DIFFIO_TX_B16p	DIFFOUT_B16p	AA8	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B17n	DIFFOUT_B17n	Y10		

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16
3B	VREFB3BN0	IO			DIFFIO_RX_B18n	DIFFOUT_B18n	AA9	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_TX_B17p	DIFFOUT_B17p	AA10	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B18p	DIFFOUT_B18p	Y9	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	L9	DQSn3B	
3B	VREFB3BN0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	W11	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	M10	DQS3B	
3B	VREFB3BN0	IO			DIFFIO_TX_B20p	DIFFOUT_B20p	Y11		
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B21n	DIFFOUT_B21n	AB10	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B22n	DIFFOUT_B22n	U10	DQ3B	
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B21p	DIFFOUT_B21p	AB11	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B22p	DIFFOUT_B22p	U11	DQ3B	
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B23n	DIFFOUT_B23n	T10		
3B	VREFB3BN0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	R11	DQ3B	
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B23p	DIFFOUT_B23p	R10		
3B	VREFB3BN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	P12	DQ3B	
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B25n	DIFFOUT_B25n	AA13		
4A	VREFB4AN0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	W12	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B25p	DIFFOUT_B25p	AB13	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	Y12	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	U12	DQSn4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	R12	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	T12	DQS4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	T13		
4A	VREFB4AN0	IO			DIFFIO_TX_B29n	DIFFOUT_B29n	AB15	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	W13	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B29p	DIFFOUT_B29p	AB16	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	V13	DQ4B	
4A	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B31n	DIFFOUT_B31n	T14		
4A	VREFB4AN0	IO			DIFFIO_TX_B32n	DIFFOUT_B32n	AB18	DQ4B	
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B31p	DIFFOUT_B31p	U13		
4A	VREFB4AN0	IO			DIFFIO_TX_B32p	DIFFOUT_B32p	AA18	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AA19		
4A	VREFB4AN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	Y14	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	Y19	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	W14	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	P14	DQSn5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B36n	DIFFOUT_B36n	AA20	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	R14	DQS5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	Y20		
4A	VREFB4AN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AA15	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	U15	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	Y15	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	V15	DQ5B	DQ1B
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B39n	DIFFOUT_B39n	R15		
4A	VREFB4AN0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	AB20	DQ5B	DQ1B
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B39p	DIFFOUT_B39p	T15		
4A	VREFB4AN0	IO			DIFFIO_TX_B40p	DIFFOUT_B40p	AB21	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B41n	DIFFOUT_B41n	AB22		
4A	VREFB4AN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	Y16	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AA22	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	Y17	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	U16	DQSn6B	DQSn1B
4A	VREFB4AN0	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	AA17	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	U17	DQS6B	DQS1B
4A	VREFB4AN0	IO			DIFFIO_TX_B44p	DIFFOUT_B44p	AB17		
4A	VREFB4AN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	Y22	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	V18	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	Y21	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	W18	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B47n	DIFFOUT_B47n	W16		
4A	VREFB4AN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	W21	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B47p	DIFFOUT_B47p	W17		
4A	VREFB4AN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	W22	DQ6B	DQ1B
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	U22	DQ1R	
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	V20		
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	U21	DQ1R	
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	V19		
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	T19	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	T17	DQ1R	
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	T20	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	T18	DQ1R	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	T22		
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	R16	DQS1R	
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	R22	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R6n	R17	DQSn1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	R20	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	R19	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	R21		
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	P19	DQ1R	
5B	VREFB5BN0	IO	CLK7p,FPLL_BR_FBp		DIFFIO_RX_R9p	DIFFOUT_R9p	M16		
5B	VREFB5BN0	IO			DIFFIO_TX_R10p	DIFFOUT_R10p	E21	DQ2R	
5B	VREFB5BN0	IO	CLK7n,FPLL_BR_FBn		DIFFIO_RX_R9n	DIFFOUT_R9n	M17		
5B	VREFB5BN0	IO			DIFFIO_TX_R10n	DIFFOUT_R10n	D22	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	L19	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R12p	DIFFOUT_R12p	K21	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	L20	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R12n	DIFFOUT_R12n	J21	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R13p	DIFFOUT_R13p	L15	DQS2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R14p	DIFFOUT_R14p	G22		
5B	VREFB5BN0	IO			DIFFIO_RX_R13n	DIFFOUT_R13n	K15	DQSn2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R14n	DIFFOUT_R14n	G21	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R15p	DIFFOUT_R15p	L18	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R16p	DIFFOUT_R16p	G20	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R15n	DIFFOUT_R15n	K19	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R16n	DIFFOUT_R16n	H21		
5B	VREFB5BN0	IO	CLK6p		DIFFIO_RX_R17p	DIFFOUT_R17p	L17		
5B	VREFB5BN0	IO			DIFFIO_TX_R18p	DIFFOUT_R18p	E20	DQ3R	
5B	VREFB5BN0	IO	CLK6n		DIFFIO_RX_R17n	DIFFOUT_R17n	K17		
5B	VREFB5BN0	IO			DIFFIO_TX_R18n	DIFFOUT_R18n	F20	DQ3R	
5B	VREFB5BN0	IO			DIFFIO_RX_R19p	DIFFOUT_R19p	H20	DQ3R	
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R20p	DIFFOUT_R20p	G18	DQ3R	
5B	VREFB5BN0	IO			DIFFIO_RX_R19n	DIFFOUT_R19n	H19	DQ3R	
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R20n	DIFFOUT_R20n	G17	DQ3R	
5B	VREFB5BN0	IO			DIFFIO_RX_R21p	DIFFOUT_R21p	K16	DQS3R	
5B	VREFB5BN0	IO			DIFFIO_TX_R22p	DIFFOUT_R22p	F19		
5B	VREFB5BN0	IO			DIFFIO_RX_R21n	DIFFOUT_R21n	J16	DQSn3R	
5B	VREFB5BN0	IO			DIFFIO_TX_R22n	DIFFOUT_R22n	F18	DQ3R	
5B	VREFB5BN0	IO			DIFFIO_RX_R23p	DIFFOUT_R23p	J17	DQ3R	
5B	VREFB5BN0	IO			DIFFIO_TX_R24p	DIFFOUT_R24p	J19	DQ3R	
5B	VREFB5BN0	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	J18	DQ3R	
5B	VREFB5BN0	IO			DIFFIO_TX_R24n	DIFFOUT_R24n	H18		
7A		GND					F17		
7A	VREFB7AN0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	H16		
7A	VREFB7AN0	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	C21	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	G16		
7A	VREFB7AN0	IO			DIFFIO_TX_T18n	DIFFOUT_T18n	C20	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	D18	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	B20	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	E17	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	B21	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	G15	DQS1T	DQS1T
7A	VREFB7AN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	B22		
7A	VREFB7AN0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	G14	DQSn1T	DQSn1T
7A	VREFB7AN0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	A22	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	E16	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	A20	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	D17	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T24n	DIFFOUT_T24n	A19		
7A	VREFB7AN0	IO	CLK11p		DIFFIO_RX_T25p	DIFFOUT_T25p	G13		
7A	VREFB7AN0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	C19	DQ2T	DQ1T
7A	VREFB7AN0	IO	CLK11n		DIFFIO_RX_T25n	DIFFOUT_T25n	F14		
7A	VREFB7AN0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	C18	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	C16	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	B16	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	C15	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	B15	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	G12	DQS2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	A18		
7A	VREFB7AN0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	H12	DQSn2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	A17	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	F15	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	B18	DQ2T	DQ1T

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16
7A	VREFB7AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	E14	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	B17		
7A	VREFB7AN0	IO	CLK10p		DIFFIO_RX_T33p	DIFFOUT_T33p	H10		
7A	VREFB7AN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	A15	DQ3T	
7A	VREFB7AN0	IO	CLK10n		DIFFIO_RX_T33n	DIFFOUT_T33n	G11		
7A	VREFB7AN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	A14	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	D13	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	C14	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	C13	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	D14	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	H9	DQS3T	
7A	VREFB7AN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	A13		
7A	VREFB7AN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	G8	DQSn3T	
7A	VREFB7AN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	B13	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	E12	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	B12	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	F12	DQ3T	
7A	VREFB7AN0	IO	RZQ_2		DIFFIO_TX_T40n	DIFFOUT_T40n	A12		
8A	VREFB8AN0	IO	CLK9p		DIFFIO_RX_T41p	DIFFOUT_T41p	G10		
8A	VREFB8AN0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	C11	DQ4T	
8A	VREFB8AN0	IO	CLK9n		DIFFIO_RX_T41n	DIFFOUT_T41n	F10		
8A	VREFB8AN0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	B11	DQ4T	
8A	VREFB8AN0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	D11	DQ4T	
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T44p	DIFFOUT_T44p	A8	DQ4T	
8A	VREFB8AN0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	E11	DQ4T	
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T44n	DIFFOUT_T44n	A7	DQ4T	
8A	VREFB8AN0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	J9	DQS4T	
8A	VREFB8AN0	IO			DIFFIO_TX_T46p	DIFFOUT_T46p	F8		
8A	VREFB8AN0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	J8	DQSn4T	
8A	VREFB8AN0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	E7	DQ4T	
8A	VREFB8AN0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	C10	DQ4T	
8A	VREFB8AN0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	C6	DQ4T	
8A	VREFB8AN0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	C9	DQ4T	
8A	VREFB8AN0	IO			DIFFIO_TX_T48n	DIFFOUT_T48n	D7		
8A	VREFB8AN0	IO	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T49p	DIFFOUT_T49p	K7		
8A	VREFB8AN0	IO			DIFFIO_TX_T50p	DIFFOUT_T50p	A10	DQ5T	
8A	VREFB8AN0	IO	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T49n	DIFFOUT_T49n	J7		
8A	VREFB8AN0	IO			DIFFIO_TX_T50n	DIFFOUT_T50n	A9	DQ5T	
8A	VREFB8AN0	IO			DIFFIO_RX_T51p	DIFFOUT_T51p	D9	DQ5T	
8A	VREFB8AN0	IO			DIFFIO_TX_T52p	DIFFOUT_T52p	B6	DQ5T	
8A	VREFB8AN0	IO			DIFFIO_RX_T51n	DIFFOUT_T51n	D8	DQ5T	
8A	VREFB8AN0	IO			DIFFIO_TX_T52n	DIFFOUT_T52n	B5	DQ5T	
8A	VREFB8AN0	IO			DIFFIO_RX_T53p	DIFFOUT_T53p	H8	DQS5T	
8A	VREFB8AN0	IO			DIFFIO_TX_T54p	DIFFOUT_T54p	C8		
8A	VREFB8AN0	IO			DIFFIO_RX_T53n	DIFFOUT_T53n	G7	DQSn5T	
8A	VREFB8AN0	IO			DIFFIO_TX_T54n	DIFFOUT_T54n	B8	DQ5T	
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	H6	DQ5T	
8A	VREFB8AN0	IO			DIFFIO_TX_T56p	DIFFOUT_T56p	E6	DQ5T	
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	G6	DQ5T	
8A	VREFB8AN0	IO			DIFFIO_TX_T56n	DIFFOUT_T56n	F7		
9A		MSEL0		MSEL0			L6		
9A		CONF_DONE		CONF_DONE			J6		
9A		MSEL1		MSEL1			K6		
9A		nSTATUS		nSTATUS			G5		
9A		nCE		nCE			H5		
9A		MSEL2		MSEL2			A2		
9A		MSEL3		MSEL3			E5		
9A		nCONFIG		nCONFIG			A4		
9A		MSEL4		MSEL4			C5		
9A		GND					F3		
		GND					F21		
		GND					AB19		
		GND					AB2		
		GND					AB1		
		GND					AA16		
		GND					AA11		
		GND					AA4		
		GND					AA3		
		GND					Y13		
		GND					Y8		
		GND					Y5		

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16
		GND					Y2		
		GND					Y1		
		GND					W20		
		GND					W4		
		GND					W3		
		GND					V22		
		GND					V17		
		GND					V2		
		GND					V1		
		GND					U19		
		GND					U14		
		GND					U9		
		GND					U5		
		GND					U3		
		GND					T11		
		GND					T2		
		GND					T1		
		GND					R13		
		GND					R3		
		GND					P10		
		GND					P4		
		GND					P2		
		GND					P1		
		GND					N22		
		GND					N15		
		GND					N13		
		GND					N11		
		GND					N7		
		GND					N5		
		GND					N3		
		GND					M19		
		GND					M14		
		GND					M12		
		GND					M9		
		GND					M4		
		GND					M2		
		GND					M1		
		GND					L16		
		GND					L13		
		GND					L11		
		GND					L5		
		GND					L3		
		GND					K14		
		GND					K12		
		GND					K10		
		GND					K8		
		GND					K4		
		GND					K2		
		GND					K1		
		GND					J20		
		GND					J15		
		GND					J13		
		GND					J11		
		GND					J5		
		GND					J3		
		GND					H14		
		GND					H4		
		GND					H3		
		GND					H2		
		GND					H1		
		GND					G9		
		GND					G3		
		GND					F16		
		GND					F11		
		GND					F6		
		GND					F2		
		GND					F1		
		GND					E13		
		GND					E4		
		GND					E3		
		GND					D20		

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16
		GND					D10		
		GND					D5		
		GND					D2		
		GND					D1		
		GND					C22		
		GND					C17		
		GND					C7		
		GND					C4		
		GND					C3		
		GND					B14		
		GND					B2		
		GND					B1		
		GND					A21		
		GND					A11		
		GND					A5		
		VCC					J14		
		VCC					P15		
		VCC					P13		
		VCC					P11		
		VCC					N14		
		VCC					N12		
		VCC					M15		
		VCC					M13		
		VCC					M11		
		VCC					L14		
		VCC					L12		
		VCC					L10		
		VCC					K13		
		VCC					K11		
		VCC					K9		
		VCC					J12		
		VCC					J10		
		VCC					H15		
		VCC					H13		
		VCC					H11		
		DNU					B3		
		DNU					B4		
		DNU					D21		
		DNU					E10		
		VCCPGM					Y6		
		VCCPGM					U20		
		VCCPGM					B7		
		VCCBAT					A3		
		VCCIO3A					T6		
		VCCIO3A					AA6		
		VCCIO3B					V7		
		VCCIO3B					AB9		
		VCCIO3B					W10		
		VCCIO3B					R8		
		VCCIO4A					T16		
		VCCIO4A					AB14		
		VCCIO4A					AA21		
		VCCIO4A					Y18		
		VCCIO4A					W15		
		VCCIO4A					V12		
		VCCIO5A					T21		
		VCCIO5A					R18		
		VCCIO5B					H22		
		VCCIO5B					P20		
		VCCIO5B					N17		
		VCCIO5B					L21		
		VCCIO5B					K18		
		VCCIO5B					G19		
		VCCIO7A					B19		
		VCCIO7A					H17		
		VCCIO7A					E18		
		VCCIO7A					D15		
		VCCIO7A					C12		
		VCCIO7A					A16		
		VCCIO8A					E8		
		VCCIO8A					H7		

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16
		VCCIO8A					B9		
		VCCIO8A					A6		
		VCCPD3A					V6		
		VCCPD3B4A					V16		
		VCCPD3B4A					W9		
		VCCPD3B4A					V14		
		VCCPD3B4A					V10		
		VCCPD5A					P17		
		VCCPD5B					N19		
		VCCPD5B					M18		
		VCCPD7A8A					F13		
		VCCPD7A8A					F9		
		VCCPD7A8A					E15		
		VCCPD7A8A					E9		
3A	VREFB3AN0	VREFB3AN0					W6		
3B	VREFB3BN0	VREFB3BN0					AB12		
4A	VREFB4AN0	VREFB4AN0					AA14		
5A	VREFB5AN0	VREFB5AN0					V21		
5B	VREFB5BN0	VREFB5BN0					K20		
7A	VREFB7AN0	VREFB7AN0					D16		
8A	VREFB8AN0	VREFB8AN0					B10		
		NC					AB3		
		NC					V11		
		NC					P22		
		NC					P21		
		NC					P18		
		NC					P16		
		NC					N21		
		NC					N20		
		NC					N18		
		NC					N16		
		NC					M22		
		NC					M21		
		NC					M20		
		NC					L22		
		NC					K22		
		NC					J22		
		NC					F22		
		NC					E22		
		VCCH_GXBL					T3		
		VCCH_GXBL					M3		
		VCCL_GXBL					P3		
		VCCL_GXBL					K3		
		RREF_TL					A1		
		VCCA_FPLL					T4		
		VCCA_FPLL					F4		
		VCCA_FPLL					U18		
		VCCA_FPLL					E19		
		VCC_AUX					D6		
		VCC_AUX					D12		
		VCC_AUX					D19		
		VCC_AUX					W19		
		VCC_AUX					AA12		
		VCC_AUX					AB5		
		VCCE_GXBL					L4		
		VCCE_GXBL					N4		
		VCCE_GXBL					K5		
		VCCE_GXBL					J4		

Note:
(1) For more information about pin definition and pin connection guidelines, refer to the
Cyclone V Device Family Pin Connection Guidelines.

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16
GXB_L1		REFCLK1Ln					P6		
GXB_L1		REFCLK1Lp					N7		
GXB_L1		GXB_TX_L5n					K1		
GXB_L1		GXB_TX_L5p					K2		
GXB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					M2		
GXB_L1		GXB_RX_L5n,GXB_REFCLK_L5n					M1		
GXB_L1		GXB_TX_L4n					P1		
GXB_L1		GXB_TX_L4p					P2		
GXB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					T2		
GXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					T1		
GXB_L1		GXB_TX_L3n					W3		
GXB_L1		GXB_TX_L3p					W4		
GXB_L1		GXB_RX_L3p,GXB_REFCLK_L3p					V2		
GXB_L1		GXB_RX_L3n,GXB_REFCLK_L3n					V1		
GXB_L0		GXB_TX_L2n					AA3		
GXB_L0		GXB_TX_L2p					AA4		
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					Y2		
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					Y1		
GXB_L0		GXB_TX_L1n					AC3		
GXB_L0		GXB_TX_L1p					AC4		
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					AB2		
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					AB1		
GXB_L0		GXB_TX_L0n					AE3		
GXB_L0		GXB_TX_L0p					AE4		
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AD2		
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AD1		
GXB_L0		REFCLK0Lp					V6		
GXB_L0		REFCLK0Ln					W6		
3A		TDO		TDO			V7		
3A		nCSO		DATA4			Y6		
3A		TMS		TMS			R6		
3A		AS_DATA3		DATA3			U6		
3A		TCK		TCK			Y5		
3A		AS_DATA2		DATA2			AB5		
3A		TDI		TDI			T6		
3A		AS_DATA1		DATA1			AD5		
3A		DCLK		DCLK			N8		
3A		AS_DATA0,ASDO		DATA0			AF5		
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	T7	DQ1B	
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	U7		
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	T8	DQ1B	
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	V8	DQ1B	
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	W8	DQSn1B	
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	AB6	DQ1B	
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	Y9	DQS1B	
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	AA6		
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	R10	DQ1B	
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	AA7	DQ1B	
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	R9	DQ1B	
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	Y8	DQ1B	
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	R8		
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	AD6	DQ1B	
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	P8		
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AD7	DQ1B	
3B	VREFB3BN0	IO			DIFFIO_TX_B9n	DIFFOUT_B9n	U9		
3B	VREFB3BN0	IO			DIFFIO_RX_B10n	DIFFOUT_B10n	Y11	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B9p	DIFFOUT_B9p	T9	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B10p	DIFFOUT_B10p	W11	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	T11	DQSn2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B12n	DIFFOUT_B12n	AC10	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	R11	DQS2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AB10		

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16
3B	VREFB3BN0	IO			DIFFIO_TX_B13n	DIFFOUT_B13n	AC8	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B14n	DIFFOUT_B14n	AB11	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B13p	DIFFOUT_B13p	AC9	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B14p	DIFFOUT_B14p	AB12	DQ2B	
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B15n	DIFFOUT_B15n	T12		
3B	VREFB3BN0	IO			DIFFIO_TX_B16n	DIFFOUT_B16n	Y10	DQ2B	
3B	VREFB3BN0	IO	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B15p	DIFFOUT_B15p	T13		
3B	VREFB3BN0	IO			DIFFIO_TX_B16p	DIFFOUT_B16p	W10	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B17n	DIFFOUT_B17n	V9		
3B	VREFB3BN0	IO			DIFFIO_RX_B18n	DIFFOUT_B18n	AE8	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_TX_B17p	DIFFOUT_B17p	V10	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B18p	DIFFOUT_B18p	AD8	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	P10	DQSn3B	
3B	VREFB3BN0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	AF9	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	N10	DQS3B	
3B	VREFB3BN0	IO			DIFFIO_TX_B20p	DIFFOUT_B20p	AE9		
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B21n	DIFFOUT_B21n	AF8	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B22n	DIFFOUT_B22n	U11	DQ3B	
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B21p	DIFFOUT_B21p	AF7	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B22p	DIFFOUT_B22p	U10	DQ3B	
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B23n	DIFFOUT_B23n	P12		
3B	VREFB3BN0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	AF6	DQ3B	
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B23p	DIFFOUT_B23p	P11		
3B	VREFB3BN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	AE6	DQ3B	
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B25n	DIFFOUT_B25n	AE11		
4A	VREFB4AN0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	AA14	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B25p	DIFFOUT_B25p	AD11	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	Y14	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	W13	DQSn4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AD12	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	V13	DQS4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AD13		
4A	VREFB4AN0	IO			DIFFIO_TX_B29n	DIFFOUT_B29n	AE10	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	Y13	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B29p	DIFFOUT_B29p	AD10	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	W12	DQ4B	
4A	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B31n	DIFFOUT_B31n	V12		
4A	VREFB4AN0	IO			DIFFIO_TX_B32n	DIFFOUT_B32n	AF12	DQ4B	
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B31p	DIFFOUT_B31p	U12		
4A	VREFB4AN0	IO			DIFFIO_TX_B32p	DIFFOUT_B32p	AF11	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AC13		
4A	VREFB4AN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AC15	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AC14	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AB15	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	V14	DQSn5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B36n	DIFFOUT_B36n	AF13	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	U14	DQS5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	AE13		
4A	VREFB4AN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AF14	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AB16	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	AE14	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AA16	DQ5B	DQ1B
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B39n	DIFFOUT_B39n	Y16		
4A	VREFB4AN0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	AF18	DQ5B	DQ1B
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B39p	DIFFOUT_B39p	Y15		
4A	VREFB4AN0	IO			DIFFIO_TX_B40p	DIFFOUT_B40p	AE18	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B41n	DIFFOUT_B41n	AD18		
4A	VREFB4AN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AD16	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AC18	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	AD17	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	W15	DQSn6B	DQSn1B
4A	VREFB4AN0	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	AF19	DQ6B	DQ1B

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	V15	DQS6B	DQS1B
4A	VREFB4AN0	IO			DIFFIO_TX_B44p	DIFFOUT_B44p	AE19		
4A	VREFB4AN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	AF22	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AC17	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	AF21	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	AB17	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B47n	DIFFOUT_B47n	U17		
4A	VREFB4AN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	AE21	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B47p	DIFFOUT_B47p	T17		
4A	VREFB4AN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	AE20	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B49n	DIFFOUT_B49n	AD20		
4A	VREFB4AN0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	AE15	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AC20	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	AE16	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B51n	DIFFOUT_B51n	W17	DQSn7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_TX_B52n	DIFFOUT_B52n	AD21	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B51p	DIFFOUT_B51p	W16	DQS7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_TX_B52p	DIFFOUT_B52p	AD22		
4A	VREFB4AN0	IO			DIFFIO_TX_B53n	DIFFOUT_B53n	AE23	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B54n	DIFFOUT_B54n	AF16	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_TX_B53p	DIFFOUT_B53p	AD23	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B54p	DIFFOUT_B54p	AF17	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B55n	DIFFOUT_B55n	U16		
4A	VREFB4AN0	IO			DIFFIO_TX_B56n	DIFFOUT_B56n	AF23	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B55p	DIFFOUT_B55p	U15		
4A	VREFB4AN0	IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AE24	DQ7B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_TX_B57n	DIFFOUT_B57n	AF24		
4A	VREFB4AN0	IO			DIFFIO_RX_B58n	DIFFOUT_B58n	AA18	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_TX_B57p	DIFFOUT_B57p	AE25	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B58p	DIFFOUT_B58p	Y18	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	V17	DQSn8B	DQSn2B
4A	VREFB4AN0	IO			DIFFIO_TX_B60n	DIFFOUT_B60n	AE26	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	V18	DQS8B	DQS2B
4A	VREFB4AN0	IO			DIFFIO_TX_B60p	DIFFOUT_B60p	AD26		
4A	VREFB4AN0	IO			DIFFIO_TX_B61n	DIFFOUT_B61n	AC19	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B62n	DIFFOUT_B62n	Y19	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	AB19	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B62p	Y20	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B63n	DIFFOUT_B63n	W18		
4A	VREFB4AN0	IO			DIFFIO_TX_B64n	DIFFOUT_B64n	AA21	DQ8B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B63p	DIFFOUT_B63p	V19		
4A	VREFB4AN0	IO			DIFFIO_TX_B64p	DIFFOUT_B64p	AB22	DQ8B	DQ2B
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	AC22	DQ1R	
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	U19		
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	AC23	DQ1R	
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	V20		
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	AA22	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	W20	DQ1R	
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	AA23	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	W21	DQ1R	
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	AC24		
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	V22	DQS1R	
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	AB24	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R6n	U22	DQSn1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	Y23	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	T19	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	Y24		
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	U20	DQ1R	
5B	VREFB5BN0	IO	CLK7p,FPLL_BR_FBp		DIFFIO_RX_R9p	DIFFOUT_R9p	T21		
5B	VREFB5BN0	IO			DIFFIO_TX_R10p	DIFFOUT_R10p	V23	DQ2R	
5B	VREFB5BN0	IO	CLK7n,FPLL_BR_FBn		DIFFIO_RX_R9n	DIFFOUT_R9n	T22		
5B	VREFB5BN0	IO			DIFFIO_TX_R10n	DIFFOUT_R10n	V24	DQ2R	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16
5B	VREFB5BN0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	T23	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R12p	DIFFOUT_R12p	AA24	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	T24	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R12n	DIFFOUT_R12n	AB25	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R13p	DIFFOUT_R13p	R23	DQS2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R14p	DIFFOUT_R14p	AD25		
5B	VREFB5BN0	IO			DIFFIO_RX_R13n	DIFFOUT_R13n	P23	DQSn2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R14n	DIFFOUT_R14n	AC25	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R15p	DIFFOUT_R15p	R24	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R16p	DIFFOUT_R16p	U24	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R15n	DIFFOUT_R15n	R25	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_TX_R16n	DIFFOUT_R16n	V25		
5B	VREFB5BN0	IO	CLK6p		DIFFIO_RX_R17p	DIFFOUT_R17p	R20		
5B	VREFB5BN0	IO			DIFFIO_TX_R18p	DIFFOUT_R18p	AB26	DQ3R	
5B	VREFB5BN0	IO	CLK6n		DIFFIO_RX_R17n	DIFFOUT_R17n	P20		
5B	VREFB5BN0	IO			DIFFIO_TX_R18n	DIFFOUT_R18n	AA26	DQ3R	
5B	VREFB5BN0	IO			DIFFIO_RX_R19p	DIFFOUT_R19p	T26	DQ3R	
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R20p	DIFFOUT_R20p	Y25	DQ3R	
5B	VREFB5BN0	IO			DIFFIO_RX_R19n	DIFFOUT_R19n	R26	DQ3R	
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R20n	DIFFOUT_R20n	Y26	DQ3R	
5B	VREFB5BN0	IO			DIFFIO_RX_R21p	DIFFOUT_R21p	P21	DQS3R	
5B	VREFB5BN0	IO			DIFFIO_TX_R22p	DIFFOUT_R22p	W25		
5B	VREFB5BN0	IO			DIFFIO_RX_R21n	DIFFOUT_R21n	P22	DQSn3R	
5B	VREFB5BN0	IO			DIFFIO_TX_R22n	DIFFOUT_R22n	W26	DQ3R	
5B	VREFB5BN0	IO			DIFFIO_RX_R23p	DIFFOUT_R23p	N25	DQ3R	
5B	VREFB5BN0	IO			DIFFIO_TX_R24p	DIFFOUT_R24p	U25	DQ3R	
5B	VREFB5BN0	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	P26	DQ3R	
5B	VREFB5BN0	IO			DIFFIO_TX_R24n	DIFFOUT_R24n	U26		
6A	VREFB6AN0	IO	CLK5p		DIFFIO_RX_R25p	DIFFOUT_R25p	N20		
6A	VREFB6AN0	IO			DIFFIO_TX_R26p	DIFFOUT_R26p	J25	DQ4R	
6A	VREFB6AN0	IO	CLK5n		DIFFIO_RX_R25n	DIFFOUT_R25n	M21		
6A	VREFB6AN0	IO			DIFFIO_TX_R26n	DIFFOUT_R26n	J26	DQ4R	
6A	VREFB6AN0	IO			DIFFIO_RX_R27p	DIFFOUT_R27p	N24	DQ4R	
6A	VREFB6AN0	IO	FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTp,FPLL_TR_FB		DIFFIO_TX_R28p	DIFFOUT_R28p	F26	DQ4R	
6A	VREFB6AN0	IO			DIFFIO_RX_R27n	DIFFOUT_R27n	M24	DQ4R	
6A	VREFB6AN0	IO	FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTn		DIFFIO_TX_R28n	DIFFOUT_R28n	G26	DQ4R	
6A	VREFB6AN0	IO			DIFFIO_RX_R29p	DIFFOUT_R29p	N23	DQS4R	
6A	VREFB6AN0	IO			DIFFIO_TX_R30p	DIFFOUT_R30p	G25		
6A	VREFB6AN0	IO			DIFFIO_RX_R29n	DIFFOUT_R29n	M22	DQSn4R	
6A	VREFB6AN0	IO			DIFFIO_TX_R30n	DIFFOUT_R30n	H25	DQ4R	
6A	VREFB6AN0	IO			DIFFIO_RX_R31p	DIFFOUT_R31p	M25	DQ4R	
6A	VREFB6AN0	IO			DIFFIO_TX_R32p	DIFFOUT_R32p	D26	DQ4R	
6A	VREFB6AN0	IO			DIFFIO_RX_R31n	DIFFOUT_R31n	M26	DQ4R	
6A	VREFB6AN0	IO			DIFFIO_TX_R32n	DIFFOUT_R32n	E26		
6A	VREFB6AN0	IO	CLK4p,FPLL_TR_FBp		DIFFIO_RX_R33p	DIFFOUT_R33p	K25		
6A	VREFB6AN0	IO			DIFFIO_TX_R34p	DIFFOUT_R34p	E24	DQ5R	
6A	VREFB6AN0	IO	CLK4n,FPLL_TR_FBn		DIFFIO_RX_R33n	DIFFOUT_R33n	K26		
6A	VREFB6AN0	IO			DIFFIO_TX_R34n	DIFFOUT_R34n	E25	DQ5R	
6A	VREFB6AN0	IO			DIFFIO_RX_R35p	DIFFOUT_R35p	K24	DQ5R	
6A	VREFB6AN0	IO			DIFFIO_TX_R36p	DIFFOUT_R36p	F24	DQ5R	
6A	VREFB6AN0	IO			DIFFIO_RX_R35n	DIFFOUT_R35n	K23	DQ5R	
6A	VREFB6AN0	IO			DIFFIO_TX_R36n	DIFFOUT_R36n	G24	DQ5R	
6A	VREFB6AN0	IO			DIFFIO_RX_R37p	DIFFOUT_R37p	L23	DQS5R	
6A	VREFB6AN0	IO			DIFFIO_TX_R38p	DIFFOUT_R38p	H23		
6A	VREFB6AN0	IO			DIFFIO_RX_R37n	DIFFOUT_R37n	L24	DQSn5R	
6A	VREFB6AN0	IO			DIFFIO_TX_R38n	DIFFOUT_R38n	H24	DQ5R	
6A	VREFB6AN0	IO			DIFFIO_RX_R39p	DIFFOUT_R39p	H22	DQ5R	
6A	VREFB6AN0	IO			DIFFIO_TX_R40p	DIFFOUT_R40p	F23	DQ5R	
6A	VREFB6AN0	IO			DIFFIO_RX_R39n	DIFFOUT_R39n	J23	DQ5R	
6A	VREFB6AN0	IO			DIFFIO_TX_R40n	DIFFOUT_R40n	G22		
6A	VREFB6AN0	IO			DIFFIO_RX_R41p	DIFFOUT_R41p	L22		
6A	VREFB6AN0	IO			DIFFIO_TX_R42p	DIFFOUT_R42p	B25	DQ6R	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16
6A	VREFB6AN0	IO			DIFFIO_RX_R41n	DIFFOUT_R41n	K21		
6A	VREFB6AN0	IO			DIFFIO_TX_R42n	DIFFOUT_R42n	B26	DQ6R	
6A	VREFB6AN0	IO			DIFFIO_RX_R43p	DIFFOUT_R43p	H19	DQ6R	
6A	VREFB6AN0	IO			DIFFIO_TX_R44p	DIFFOUT_R44p	D25	DQ6R	
6A	VREFB6AN0	IO			DIFFIO_RX_R43n	DIFFOUT_R43n	H20	DQ6R	
6A	VREFB6AN0	IO			DIFFIO_TX_R44n	DIFFOUT_R44n	C25	DQ6R	
6A	VREFB6AN0	IO			DIFFIO_RX_R45p	DIFFOUT_R45p	J20	DQS6R	
6A	VREFB6AN0	IO			DIFFIO_TX_R46p	DIFFOUT_R46p	D22		
6A	VREFB6AN0	IO			DIFFIO_RX_R45n	DIFFOUT_R45n	J21	DQSn6R	
6A	VREFB6AN0	IO			DIFFIO_TX_R46n	DIFFOUT_R46n	E23	DQ6R	
6A	VREFB6AN0	IO			DIFFIO_RX_R47p	DIFFOUT_R47p	G20	DQ6R	
6A	VREFB6AN0	IO			DIFFIO_TX_R48p	DIFFOUT_R48p	E21	DQ6R	
6A	VREFB6AN0	IO			DIFFIO_RX_R47n	DIFFOUT_R47n	F21	DQ6R	
6A	VREFB6AN0	IO			DIFFIO_TX_R48n	DIFFOUT_R48n	F22		
7A		GND					D23		
7A	VREFB7AN0	IO			DIFFIO_RX_T1p	DIFFOUT_T1p	H15		
7A	VREFB7AN0	IO			DIFFIO_TX_T2p	DIFFOUT_T2p	C23	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	J16		
7A	VREFB7AN0	IO			DIFFIO_TX_T2n	DIFFOUT_T2n	C22	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T3p	B24	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T4p	DIFFOUT_T4p	A23	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T3n	A24	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T4n	DIFFOUT_T4n	A22	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T5p	H18	DQS1T	DQS1T
7A	VREFB7AN0	IO			DIFFIO_TX_T6p	DIFFOUT_T6p	B22		
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T5n	H17	DQSn1T	DQSn1T
7A	VREFB7AN0	IO			DIFFIO_TX_T6n	DIFFOUT_T6n	A21	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T7p	D21	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T8p	DIFFOUT_T8p	B21	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T7n	D20	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T8n	DIFFOUT_T8n	B20		
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T9p	G16		
7A	VREFB7AN0	IO			DIFFIO_TX_T10p	DIFFOUT_T10p	C20	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T9n	G17		
7A	VREFB7AN0	IO			DIFFIO_TX_T10n	DIFFOUT_T10n	B19	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T11p	DIFFOUT_T11p	E20	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T12p	DIFFOUT_T12p	C19	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T11n	DIFFOUT_T11n	E19	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T12n	DIFFOUT_T12n	C18	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T13p	DIFFOUT_T13p	J12	DQS2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T14p	DIFFOUT_T14p	A19		
7A	VREFB7AN0	IO			DIFFIO_RX_T13n	DIFFOUT_T13n	J11	DQSn2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T14n	DIFFOUT_T14n	A18	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T15p	DIFFOUT_T15p	D18	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T16p	DIFFOUT_T16p	A17	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	D17	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T16n	DIFFOUT_T16n	A16		
7A	VREFB7AN0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	H14		
7A	VREFB7AN0	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	C17	DQ3T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	H13		
7A	VREFB7AN0	IO			DIFFIO_TX_T18n	DIFFOUT_T18n	B17	DQ3T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	E18	DQ3T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	A14	DQ3T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	F18	DQ3T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	B14	DQ3T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	L12	DQS3T	DQS2T
7A	VREFB7AN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	B15		
7A	VREFB7AN0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	K11	DQSn3T	DQSn2T
7A	VREFB7AN0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	C15	DQ3T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	C14	DQ3T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	A8	DQ3T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	D15	DQ3T	DQ2T

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16
7A	VREFB7AN0	IO			DIFFIO_TX_T24n	DIFFOUT_T24n	A9		
7A	VREFB7AN0	IO	CLK11p		DIFFIO_RX_T25p	DIFFOUT_T25p	G15		
7A	VREFB7AN0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	C9	DQ4T	DQ2T
7A	VREFB7AN0	IO	CLK11n		DIFFIO_RX_T25n	DIFFOUT_T25n	G14		
7A	VREFB7AN0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	B9	DQ4T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	E16	DQ4T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	D10	DQ4T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	D16	DQ4T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	C10	DQ4T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	N12	DQS4T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	B10		
7A	VREFB7AN0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	M12	DQSn4T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	A11	DQ4T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	F16	DQ4T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	E10	DQ4T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	E15	DQ4T	DQ2T
7A	VREFB7AN0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	E11		
7A	VREFB7AN0	IO	CLK10p		DIFFIO_RX_T33p	DIFFOUT_T33p	H12		
7A	VREFB7AN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	B12	DQ5T	
7A	VREFB7AN0	IO	CLK10n		DIFFIO_RX_T33n	DIFFOUT_T33n	G11		
7A	VREFB7AN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	A13	DQ5T	
7A	VREFB7AN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	G12	DQ5T	
7A	VREFB7AN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	A12	DQ5T	
7A	VREFB7AN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	F12	DQ5T	
7A	VREFB7AN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	B11	DQ5T	
7A	VREFB7AN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	M11	DQS5T	
7A	VREFB7AN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	C13		
7A	VREFB7AN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	L11	DQSn5T	
7A	VREFB7AN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	C12	DQ5T	
7A	VREFB7AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	E13	DQ5T	
7A	VREFB7AN0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	D11	DQ5T	
7A	VREFB7AN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	D13	DQ5T	
7A	VREFB7AN0	IO	RZQ_2		DIFFIO_TX_T40n	DIFFOUT_T40n	D12		
8A	VREFB8AN0	IO	CLK9p		DIFFIO_RX_T41p	DIFFOUT_T41p	N9		
8A	VREFB8AN0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	A5	DQ6T	
8A	VREFB8AN0	IO	CLK9n		DIFFIO_RX_T41n	DIFFOUT_T41n	M10		
8A	VREFB8AN0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	B6	DQ6T	
8A	VREFB8AN0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	H8	DQ6T	
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T44p	DIFFOUT_T44p	A7	DQ6T	
8A	VREFB8AN0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	H9	DQ6T	
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T44n	DIFFOUT_T44n	B7	DQ6T	
8A	VREFB8AN0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	M9	DQS6T	
8A	VREFB8AN0	IO			DIFFIO_TX_T46p	DIFFOUT_T46p	D6		
8A	VREFB8AN0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	L9	DQSn6T	
8A	VREFB8AN0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	E6	DQ6T	
8A	VREFB8AN0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	H10	DQ6T	
8A	VREFB8AN0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	D7	DQ6T	
8A	VREFB8AN0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	G10	DQ6T	
8A	VREFB8AN0	IO			DIFFIO_TX_T48n	DIFFOUT_T48n	C7		
8A	VREFB8AN0	IO	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T49p	DIFFOUT_T49p	L8		
8A	VREFB8AN0	IO			DIFFIO_TX_T50p	DIFFOUT_T50p	F6	DQ7T	
8A	VREFB8AN0	IO	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T49n	DIFFOUT_T49n	K9		
8A	VREFB8AN0	IO			DIFFIO_TX_T50n	DIFFOUT_T50n	G6	DQ7T	
8A	VREFB8AN0	IO			DIFFIO_RX_T51p	DIFFOUT_T51p	K8	DQ7T	
8A	VREFB8AN0	IO			DIFFIO_TX_T52p	DIFFOUT_T52p	G7	DQ7T	
8A	VREFB8AN0	IO			DIFFIO_RX_T51n	DIFFOUT_T51n	J8	DQ7T	
8A	VREFB8AN0	IO			DIFFIO_TX_T52n	DIFFOUT_T52n	F7	DQ7T	
8A	VREFB8AN0	IO			DIFFIO_RX_T53p	DIFFOUT_T53p	K10	DQS7T	
8A	VREFB8AN0	IO			DIFFIO_TX_T54p	DIFFOUT_T54p	H7		
8A	VREFB8AN0	IO			DIFFIO_RX_T53n	DIFFOUT_T53n	J10	DQSn7T	
8A	VREFB8AN0	IO			DIFFIO_TX_T54n	DIFFOUT_T54n	J7	DQ7T	
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	L7	DQ7T	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16
8A	VREFB8AN0	IO			DIFFIO_TX_T56p	DIFFOUT_T56p	D8	DQ7T	
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	K6	DQ7T	
8A	VREFB8AN0	IO			DIFFIO_TX_T56n	DIFFOUT_T56n	E9		
9A		MSEL0		MSEL0			M7		
9A		CONF_DONE		CONF_DONE			A6		
9A		MSEL1		MSEL1			L6		
9A		nSTATUS		nSTATUS			B5		
9A		nCE		nCE			D5		
9A		MSEL2		MSEL2			A2		
9A		MSEL3		MSEL3			K5		
9A		nCONFIG		nCONFIG			F5		
9A		MSEL4		MSEL4			J5		
9A		GND					H5		
		GND					V26		
		GND					A25		
		GND					D24		
		GND					H26		
		GND					L25		
		GND					P24		
		GND					AA25		
		GND					AC26		
		GND					AF25		
		GND					G23		
		GND					K22		
		GND					U23		
		GND					Y22		
		GND					AD24		
		GND					C21		
		GND					F20		
		GND					L20		
		GND					K19		
		GND					N21		
		GND					M19		
		GND					T20		
		GND					P19		
		GND					W19		
		GND					AC21		
		GND					AF20		
		GND					B18		
		GND					E17		
		GND					L18		
		GND					K17		
		GND					J18		
		GND					N18		
		GND					M17		
		GND					R18		
		GND					P17		
		GND					AB18		
		GND					AE17		
		GND					A15		
		GND					D14		
		GND					H16		
		GND					L16		
		GND					L14		
		GND					K15		
		GND					J14		
		GND					N16		
		GND					N14		
		GND					M15		
		GND					T15		
		GND					R16		
		GND					R14		

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16
		GND					P15		
		GND					V16		
		GND					AA15		
		GND					AD14		
		GND					G13		
		GND					K13		
		GND					K12		
		GND					M13		
		GND					R12		
		GND					P13		
		GND					U13		
		GND					Y12		
		GND					C11		
		GND					F10		
		GND					L10		
		GND					J9		
		GND					N11		
		GND					T10		
		GND					P9		
		GND					W9		
		GND					AC11		
		GND					AF10		
		GND					B8		
		GND					E7		
		GND					H6		
		GND					N6		
		GND					M8		
		GND					R7		
		GND					P7		
		GND					AB8		
		GND					AE7		
		GND					C5		
		GND					B4		
		GND					F4		
		GND					E5		
		GND					D4		
		GND					H4		
		GND					G5		
		GND					L4		
		GND					J4		
		GND					N4		
		GND					M5		
		GND					T5		
		GND					R4		
		GND					P5		
		GND					V5		
		GND					V4		
		GND					U4		
		GND					AA5		
		GND					Y4		
		GND					W5		
		GND					AC5		
		GND					AB4		
		GND					AF4		
		GND					AE5		
		GND					AD4		
		GND					C2		
		GND					C1		
		GND					B3		
		GND					B2		
		GND					F3		
		GND					E2		

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16
		GND					E1		
		GND					D3		
		GND					H3		
		GND					G2		
		GND					G1		
		GND					L2		
		GND					L1		
		GND					K3		
		GND					J2		
		GND					J1		
		GND					N2		
		GND					N1		
		GND					M3		
		GND					T3		
		GND					R2		
		GND					R1		
		GND					P3		
		GND					V3		
		GND					U2		
		GND					U1		
		GND					AA2		
		GND					AA1		
		GND					Y3		
		GND					W2		
		GND					W1		
		GND					AC2		
		GND					AC1		
		GND					AB3		
		GND					AF3		
		GND					AF2		
		GND					AE2		
		GND					AE1		
		GND					AD3		
		VCC					K20		
		VCC					L19		
		VCC					J19		
		VCC					N19		
		VCC					M20		
		VCC					R19		
		VCC					L17		
		VCC					K18		
		VCC					J17		
		VCC					N17		
		VCC					M18		
		VCC					T18		
		VCC					R17		
		VCC					P18		
		VCC					L15		
		VCC					K16		
		VCC					K14		
		VCC					J15		
		VCC					N15		
		VCC					M16		
		VCC					M14		
		VCC					T16		
		VCC					T14		
		VCC					R15		
		VCC					P16		
		VCC					P14		
		VCC					L13		
		VCC					J13		
		VCC					N13		

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16
		VCC					R13		
		DNU					A4		
		DNU					A3		
		DNU					C24		
		DNU					F14		
		VCCPGM					AA9		
		VCCPGM					W22		
		VCCPGM					F8		
		VCCBAT					E8		
		VCCIO3A					Y7		
		VCCIO3A					AC6		
		VCCIO3B					U8		
		VCCIO3B					V11		
		VCCIO3B					AA10		
		VCCIO3B					AD9		
		VCCIO4A					U18		
		VCCIO4A					AE22		
		VCCIO4A					AA20		
		VCCIO4A					AD19		
		VCCIO4A					Y17		
		VCCIO4A					W14		
		VCCIO4A					AC16		
		VCCIO4A					AF15		
		VCCIO4A					AB13		
		VCCIO4A					AE12		
		VCCIO5A					V21		
		VCCIO5A					AB23		
		VCCIO5B					N26		
		VCCIO5B					T25		
		VCCIO5B					W24		
		VCCIO5B					R22		
		VCCIO6A					C26		
		VCCIO6A					F25		
		VCCIO6A					J24		
		VCCIO6A					E22		
		VCCIO6A					M23		
		VCCIO6A					H21		
		VCCIO7A					A10		
		VCCIO7A					B23		
		VCCIO7A					A20		
		VCCIO7A					D19		
		VCCIO7A					G18		
		VCCIO7A					C16		
		VCCIO7A					F15		
		VCCIO7A					B13		
		VCCIO7A					E12		
		VCCIO7A					H11		
		VCCIO8A					C6		
		VCCIO8A					D9		
		VCCIO8A					G8		
		VCCIO8A					K7		
		VCCPD3A					AB9		
		VCCPD3B4A					AB21		
		VCCPD3B4A					AA19		
		VCCPD3B4A					AA17		
		VCCPD3B4A					AA13		
		VCCPD3B4A					AA11		
		VCCPD5A					U21		
		VCCPD5B					N22		
		VCCPD5B					R21		
		VCCPD6A					J22		
		VCCPD6A					L21		

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16
		VCCPD7A8A					F19		
		VCCPD7A8A					F17		
		VCCPD7A8A					F13		
		VCCPD7A8A					F11		
		VCCPD7A8A					F9		
3A	VREFB3AN0	VREFB3AN0					AC7		
3B	VREFB3BN0	VREFB3BN0					AC12		
4A	VREFB4AN0	VREFB4AN0					AD15		
5A	VREFB5AN0	VREFB5AN0					W23		
5B	VREFB5BN0	VREFB5BN0					P25		
6A	VREFB6AN0	VREFB6AN0					L26		
7A	VREFB7AN0	VREFB7AN0					B16		
8A	VREFB8AN0	VREFB8AN0					C8		
		NC					AA12		
		NC					M6		
		NC					AB7		
		NC					C4		
		NC					E4		
		NC					G4		
		NC					L5		
		NC					C3		
		NC					F2		
		NC					F1		
		NC					E3		
		NC					D2		
		NC					D1		
		NC					H2		
		NC					H1		
		NC					G3		
		VCCH_GXBL					R3		
		VCCH_GXBL					T4		
		VCCH_GXBL					L3		
		VCCL_GXBL					J3		
		VCCL_GXBL					N3		
		VCCL_GXBL					U3		
		RREF_TL					B1		
		VCCA_FPLL					W7		
		VCCA_FPLL					J6		
		VCCA_FPLL					Y21		
		VCCA_FPLL					G21		
		VCC_AUX					G9		
		VCC_AUX					E14		
		VCC_AUX					G19		
		VCC_AUX					AB20		
		VCC_AUX					AB14		
		VCC_AUX					AA8		
		VCCE_GXBL					K4		
		VCCE_GXBL					N5		
		VCCE_GXBL					M4		
		VCCE_GXBL					R5		
		VCCE_GXBL					P4		
		VCCE_GXBL					U5		

Note:
(1) For more information about pin definition and pin connection guidelines, refer to the
Cyclone V Device Family Pin Connection Guidelines.

Version Number	Date	Changes Made
1.0	11/29/2012	Initial release.