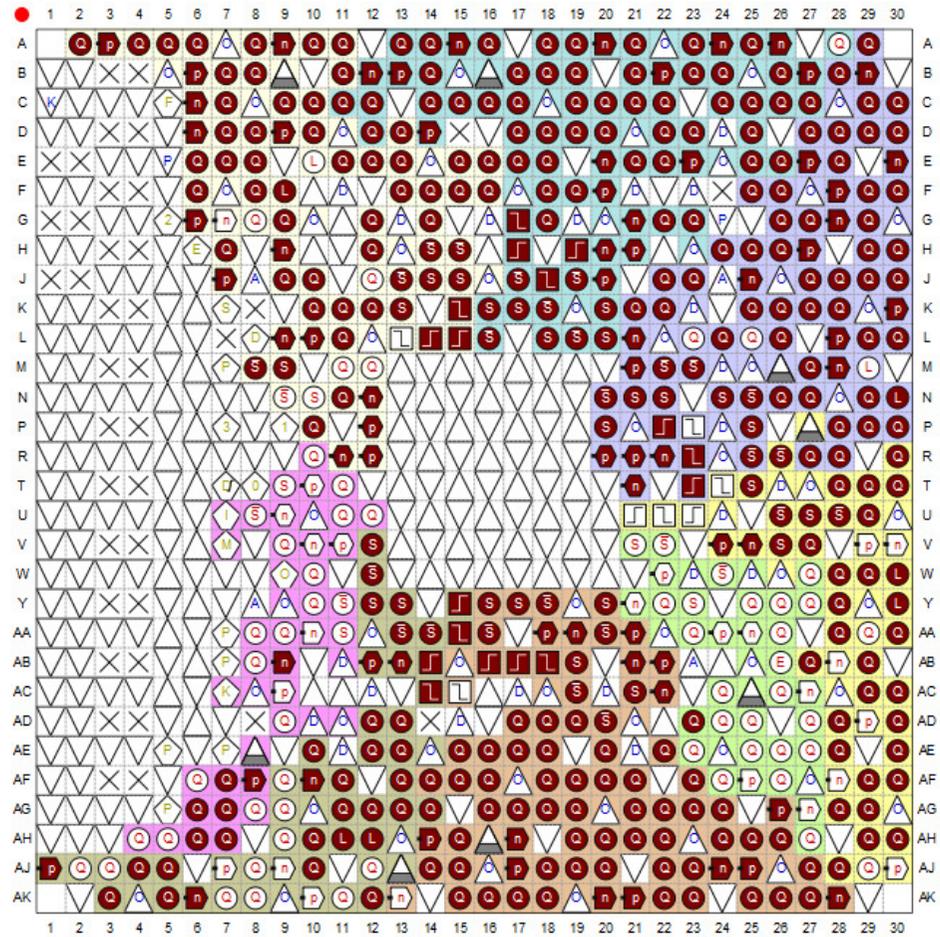
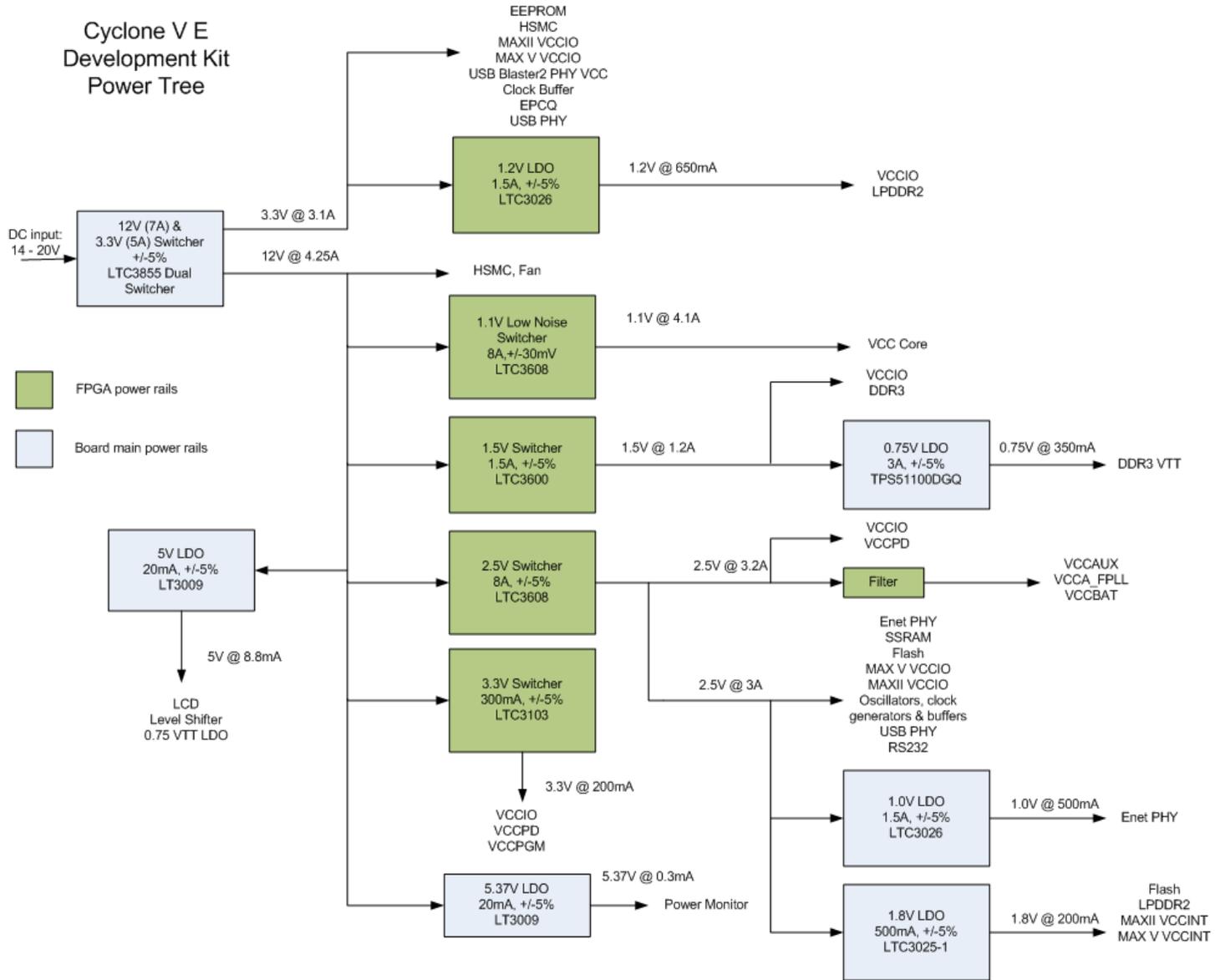


FPGA Package Top View



Altera Worldwide Service, Plot 6, Bayan Lepas Technoplex, Penang, Malaysia		
Title		Cyclone V E Development Kit Board
Size	Document Number	Rev
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Cyclone V E Development Kit Power Tree



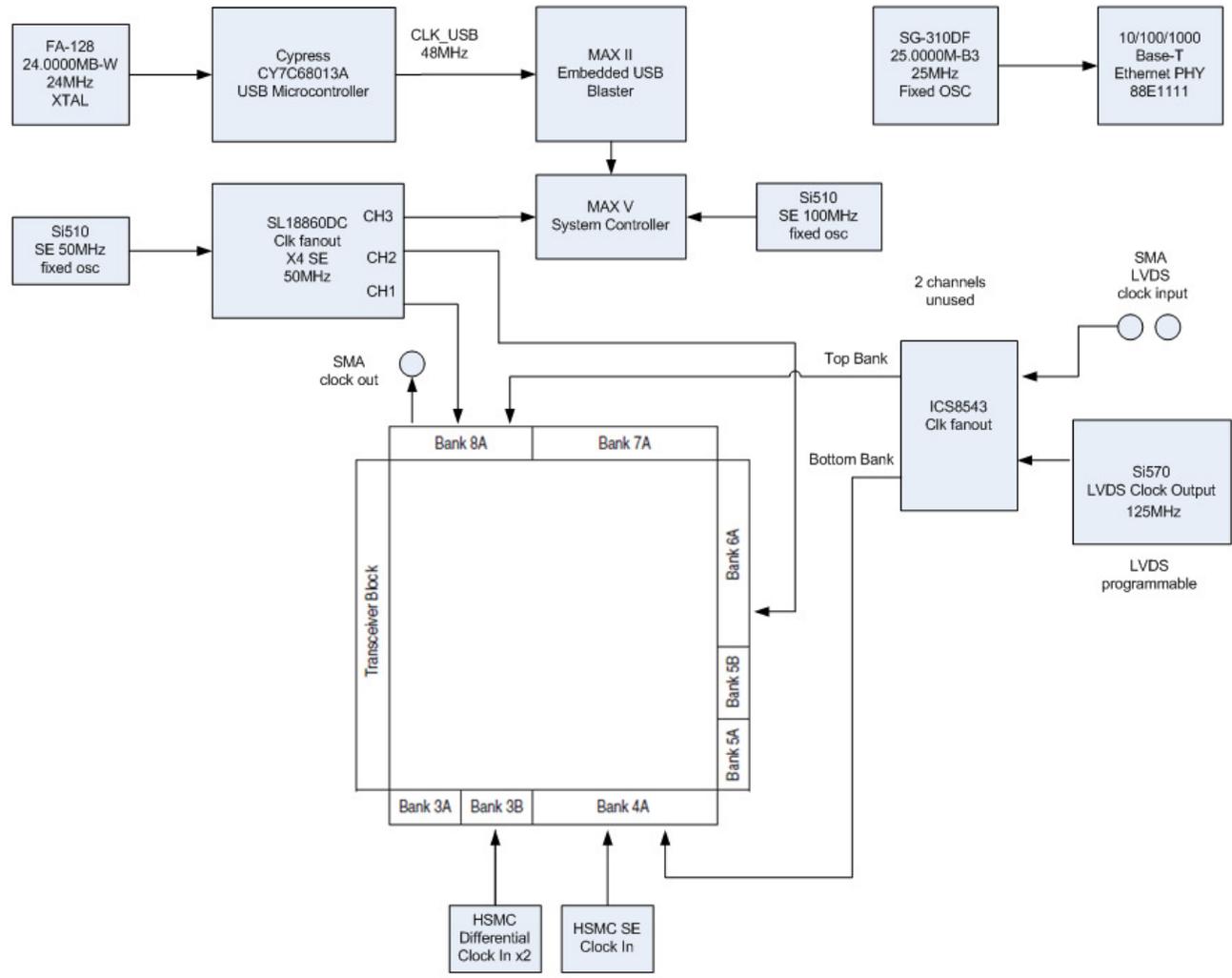
Altera Worldwide Service, Plot 6, Bayan Lepas Technoplex, Penang, Malaysia

Title **Cyclone V E Development Kit Board**

Size B Document Number 150-0321002- B1 (6XX-44161R) Rev B1

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Cyclone V E Development Kit Clock Tree

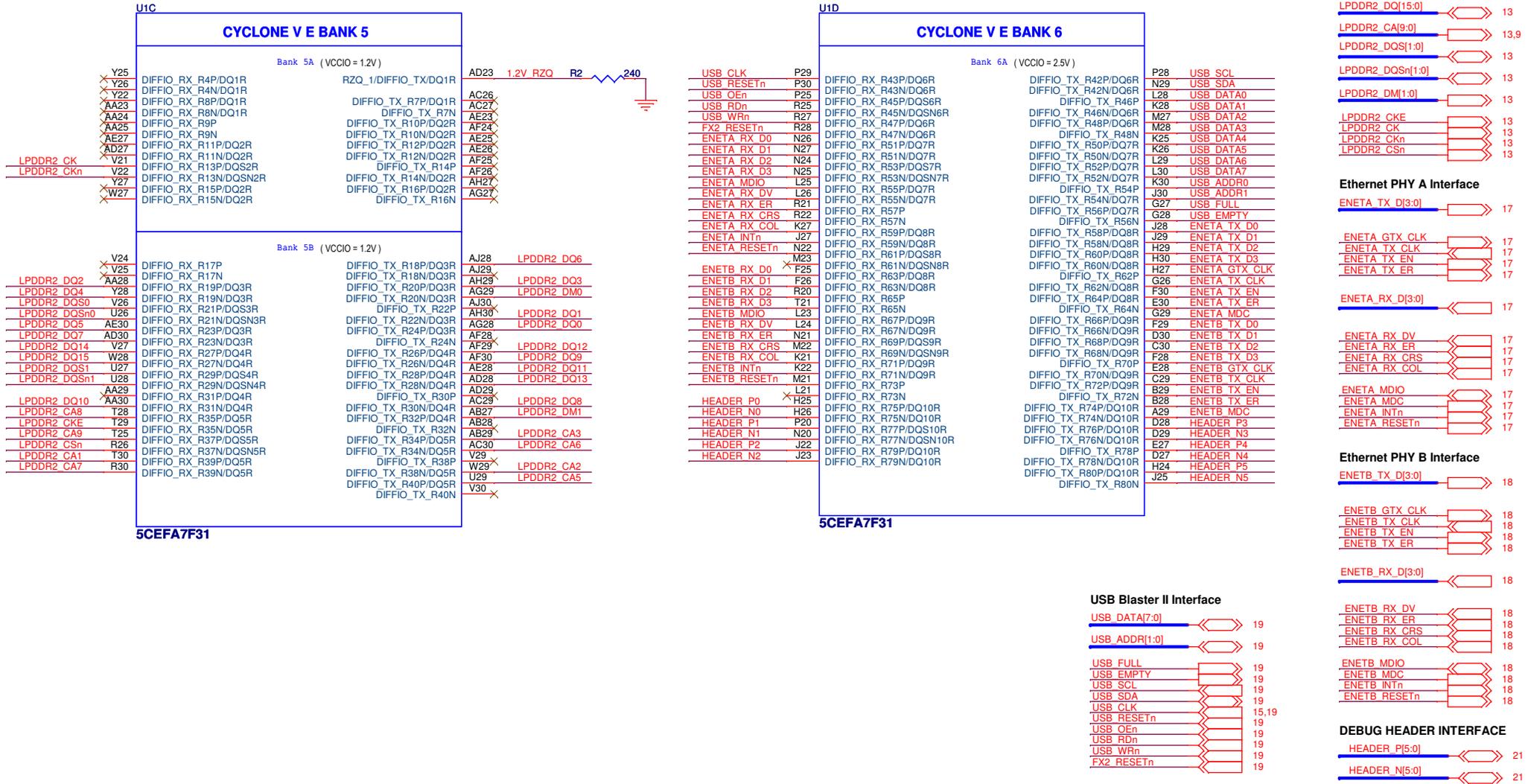


Altera Worldwide Service, Plot 6, Bayan Lepas Technoplex, Penang, Malaysia			
Title		Cyclone V E Development Kit Board	
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Cyclone V E Bank 3 and Bank 4



Cyclone V E Bank 5 and Bank 6



Altera Worldwide Service, Plot 6, Bayan Lepas Technoplex, Penang, Malaysia		
Title Cyclone V E Development Kit Board		
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Cyclone V E Bank 7 and Bank 8

U1E

CYCLONE V E BANK 7

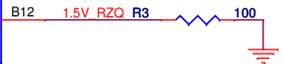
Bank 7A (VCCIO = 1.5V)

HEADER_D0	H21	DIFFIO_RX_T1P
HEADER_D1	G21	DIFFIO_RX_T1N
HEADER_D2	G22	DIFFIO_RX_T3P/DQ1T
DDR3_A1	G23	DIFFIO_RX_T3N/DQ1T
DDR3_CASn	L20	DIFFIO_RX_T5P/DQS1T
DDR3_RESEtN	L19	DIFFIO_RX_T5N/DQSN1T
DDR3_A3	E22	DIFFIO_RX_T7P/DQ1T
DDR3_A2	E21	DIFFIO_RX_T7N/DQ1T
DDR3_CLK_P	J20	DIFFIO_RX_T9P
DDR3_CLK_N	H20	DIFFIO_RX_T9N
DDR3_DQ2	C21	DIFFIO_RX_T11P/DQ2T
DDR3_DQ4	C20	DIFFIO_RX_T11N/DQ2T
DDR3_DQS_P0	K20	DIFFIO_RX_T13P/DQS2T
DDR3_DQS_N0	J19	DIFFIO_RX_T13N/DQS2T
DDR3_DQ7	D20	DIFFIO_RX_T15P/DQ2T
DDR3_DQ3	C19	DIFFIO_RX_T15N/DQ2T
DDR3_BA1	F20	DIFFIO_RX_T17P
DDR3_A11	E20	DIFFIO_RX_T17N
DDR3_DQ11	F19	DIFFIO_RX_T19P/DQ3T
DDR3_DQ14	E18	DIFFIO_RX_T19N/DQ3T
DDR3_DQS_P1	L18	DIFFIO_RX_T21P/DQS3T
DDR3_DQS_N1	K18	DIFFIO_RX_T21N/DQS3T
DDR3_BA2	D19	DIFFIO_RX_T23P/DQ3T
DDR3_DM1	D18	DIFFIO_RX_T23N/DQ3T
DDR3_DQ16	G18	DIFFIO_RX_T27P/DQ4T
DDR3_DQ19	F18	DIFFIO_RX_T27N/DQ4T
DDR3_DQS_P2	K16	DIFFIO_RX_T29P/DQS4T
DDR3_DQS_N2	L16	DIFFIO_RX_T29N/DQS4T
DDR3_DQ21	C17	DIFFIO_RX_T31P/DQ4T
DDR3_DQ22	B17	DIFFIO_RX_T31N/DQ4T
DDR3_DQ27	E17	DIFFIO_RX_T35P/DQ5T
DDR3_DQ25	D17	DIFFIO_RX_T35N/DQ5T
DDR3_DQS_P3	K17	DIFFIO_RX_T37P/DQS5T
DDR3_DQS_N3	J17	DIFFIO_RX_T37N/DQS5T
DDR3_DQ28	C16	DIFFIO_RX_T39P/DQ5T
DDR3_DQ24	C15	DIFFIO_RX_T39N/DQ5T

RZQ_2/DIFFIO_TX_T40N

5CEFA7F31

E26	HEADER_D3	DIFFIO_TX_T2P/DQ1T
E25	HEADER_D4	DIFFIO_TX_T2N/DQ1T
C27	HEADER_D5	DIFFIO_TX_T4P/DQ1T
C26	HEADER_D6	DIFFIO_TX_T4N/DQ1T
B27	HEADER_D7	DIFFIO_TX_T6P
A28	DDR3_A7	DIFFIO_TX_T6N/DQ1T
B26	DDR3_A5	DIFFIO_TX_T8P/DQ1T
A26	DDR3_A5	DIFFIO_TX_T8N
D25	DDR3_DQ6	DIFFIO_TX_T10P/DQ2T
C25	DDR3_A12	DIFFIO_TX_T10N/DQ2T
D23	DDR3_DM0	DIFFIO_TX_T12P/DQ2T
C22	DDR3_DQ5	DIFFIO_TX_T12N/DQ2T
E23	DDR3_A10	DIFFIO_TX_T14P
D22	DDR3_DQ1	DIFFIO_TX_T14N/DQ2T
A25	DDR3_DQ0	DIFFIO_TX_T16P/DQ2T
A24	DDR3_RASn	DIFFIO_TX_T16N
C24	DDR3_DQ12	DIFFIO_TX_T18P/DQ3T
B24	DDR3_DQ8	DIFFIO_TX_T18N/DQ3T
B23	DDR3_DQ13	DIFFIO_TX_T20P/DQ3T
A23	DDR3_DQ15	DIFFIO_TX_T20N/DQ3T
B22	DDR3_WEn	DIFFIO_TX_T22P
B21	DDR3_DQ10	DIFFIO_TX_T22N/DQ3T
A21	DDR3_DQ9	DIFFIO_TX_T24P/DQ3T
A20	DDR3_A4	DIFFIO_TX_T24N
B19	DDR3_DQ23	DIFFIO_TX_T26P/DQ4T
A19	DDR3_DM2	DIFFIO_TX_T26N/DQ4T
B18	DDR3_DQ17	DIFFIO_TX_T28P/DQ4T
A18	DDR3_DQ18	DIFFIO_TX_T28N/DQ4T
C14	DDR3_A9	DIFFIO_TX_T30P/DQ4T
D12	DDR3_DQ20	DIFFIO_TX_T30N/DQ4T
A16	DDR3_A0	DIFFIO_TX_T32P/DQ4T
A15	DDR3_A6	DIFFIO_TX_T32N
B14	DDR3_DM3	DIFFIO_TX_T34P/DQ5T
A14	DDR3_DQ29	DIFFIO_TX_T34N/DQ5T
D12	DDR3_DQ30	DIFFIO_TX_T36P/DQ5T
C12	DDR3_DQ26	DIFFIO_TX_T36N/DQ5T
B13	DDR3_A13	DIFFIO_TX_T38P/DQ5T
A13	DDR3_DQ31	DIFFIO_TX_T38N/DQ5T
C11	DDR3_CKE	DIFFIO_TX_T40P/DQ5T



U1F

CYCLONE V E BANK 8

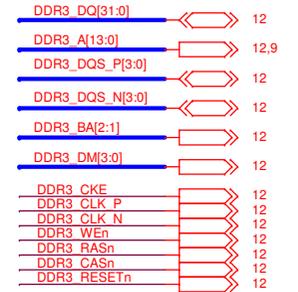
Bank 8A (VCCIO = 2.5V)

F5M_D0	F16	DIFFIO_RX_T43P/DQ6T
F5M_D1	E16	DIFFIO_RX_T43N/DQ6T
F5M_D2	M9	DIFFIO_RX_T45P/DQS6T
F5M_D3	M8	DIFFIO_RX_T45N/DQS6T
F5M_D4	F15	DIFFIO_RX_T47P/DQ6T
F5M_D5	E15	DIFFIO_RX_T47N/DQ6T
F5M_D6	E12	DIFFIO_RX_T51P/DQ7T
F5M_D7	D13	DIFFIO_RX_T51N/DQ7T
F5M_D8	J15	DIFFIO_RX_T53P/DQ7T
F5M_D9	H15	DIFFIO_RX_T53N/DQ7T
F5M_D10	E11	DIFFIO_RX_T55P/DQ7T
F5M_D11	D10	DIFFIO_RX_T55N/DQ7T
F5M_D12	L10	DIFFIO_RX_T57P
F5M_D13	L9	DIFFIO_RX_T57N
F5M_D14	G14	DIFFIO_RX_T59P/DQ8T
F5M_D15	F14	DIFFIO_RX_T59N/DQ8T
FLASH_RDYBSyn	J14	DIFFIO_RX_T61P/DQS8T
FLASH_CEn	H14	DIFFIO_RX_T61N/DQS8T
FLASH_OEn	L11	DIFFIO_RX_T63P/DQ8T
FLASH_RESEtN	K11	DIFFIO_RX_T63N/DQ8T
FLASH_WEn	P12	DIFFIO_RX_T65P
FLASH_CLK	N12	DIFFIO_RX_T65N
FLASH_ADVn	H12	DIFFIO_RX_T67P/DQ9T
MAX5_BE0	G12	DIFFIO_RX_T67N/DQ9T
MAX5_BE1	K13	DIFFIO_RX_T69P/DQ9T
MAX5_BE2	J13	DIFFIO_RX_T69N/DQ9T
MAX5_BE3	P10	DIFFIO_RX_T71P/DQ9T
MAX5_CSn	N11	DIFFIO_RX_T71N/DQ9T
MAX5_CLK	R12	DIFFIO_RX_T73P
MAX5_OEn	R11	DIFFIO_RX_T73N
MAX5_WEn	K12	DIFFIO_RX_T75P/DQ10T
RESERVED2	J12	DIFFIO_RX_T75N/DQ10T
RESERVED3	N9	DIFFIO_RX_T77P/DQS10T
RESERVED3	N9	DIFFIO_RX_T77N/DQS10T
RESERVED3	M12	DIFFIO_RX_T79P/DQ10T
RESERVED3	M11	DIFFIO_RX_T79N/DQ10T

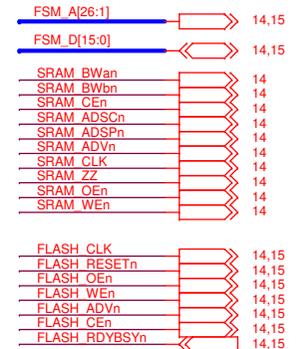
5CEFA7F31

B11	F5M_A1	DIFFIO_TX_T42P/DQ6T
A11	F5M_A2	DIFFIO_TX_T42N/DQ6T
C10	F5M_A3	DIFFIO_TX_T46P
D9	F5M_A4	DIFFIO_TX_T46N/DQ6T
A10	F5M_A5	DIFFIO_TX_T48P/DQ6T
A9	F5M_A6	DIFFIO_TX_T48N
C9	F5M_A7	DIFFIO_TX_T50P/DQ7T
B8	F5M_A8	DIFFIO_TX_T50N/DQ7T
B7	F5M_A9	DIFFIO_TX_T52P/DQ7T
A8	F5M_A10	DIFFIO_TX_T52N/DQ7T
B6	F5M_A11	DIFFIO_TX_T54P
A6	F5M_A12	DIFFIO_TX_T54N/DQ7T
C7	F5M_A13	DIFFIO_TX_T56P/DQ7T
C6	F5M_A14	DIFFIO_TX_T56N
F13	F5M_A15	DIFFIO_TX_T58P/DQ8T
E13	F5M_A16	DIFFIO_TX_T58N/DQ8T
A5	F5M_A17	DIFFIO_TX_T60P/DQ8T
A4	F5M_A18	DIFFIO_TX_T60N/DQ8T
J7	F5M_A19	DIFFIO_TX_T62P
H7	F5M_A20	DIFFIO_TX_T62N/DQ8T
J9	F5M_A21	DIFFIO_TX_T64P/DQ8T
H9	F5M_A22	DIFFIO_TX_T64N
G9	F5M_A23	DIFFIO_TX_T66P/DQ9T
F8	F5M_A24	DIFFIO_TX_T66N/DQ9T
E8	F5M_A25	DIFFIO_TX_T68P/DQ9T
D8	F5M_A26	DIFFIO_TX_T68N/DQ9T
A3	SRAM_BWan	DIFFIO_TX_T70P/DQ9T
A2	SRAM_BWbn	DIFFIO_TX_T70N/DQ9T
D7	SRAM_CEn	DIFFIO_TX_T72P/DQ9T
D6	SRAM_WEn	DIFFIO_TX_T72N
E7	SRAM_OEn	DIFFIO_TX_T74P/DQ10T
E6	SRAM_ADSCn	DIFFIO_TX_T74N/DQ10T
K10	SRAM_CLK	DIFFIO_TX_T76P/DQ10T
J10	SRAM_ADSPn	DIFFIO_TX_T76N/DQ10T
C6	SRAM_ADVn	DIFFIO_TX_T78P
F6	SRAM_ZZ	DIFFIO_TX_T78N/DQ10T
G8	RESERVED0	DIFFIO_TX_T80P/DQ10T
G7	RESERVED1	DIFFIO_TX_T80N

DDR3 Interface



Flash and SSRAM Interface



DEBUG HEADER INTERFACE



MAX V System Controller Interface



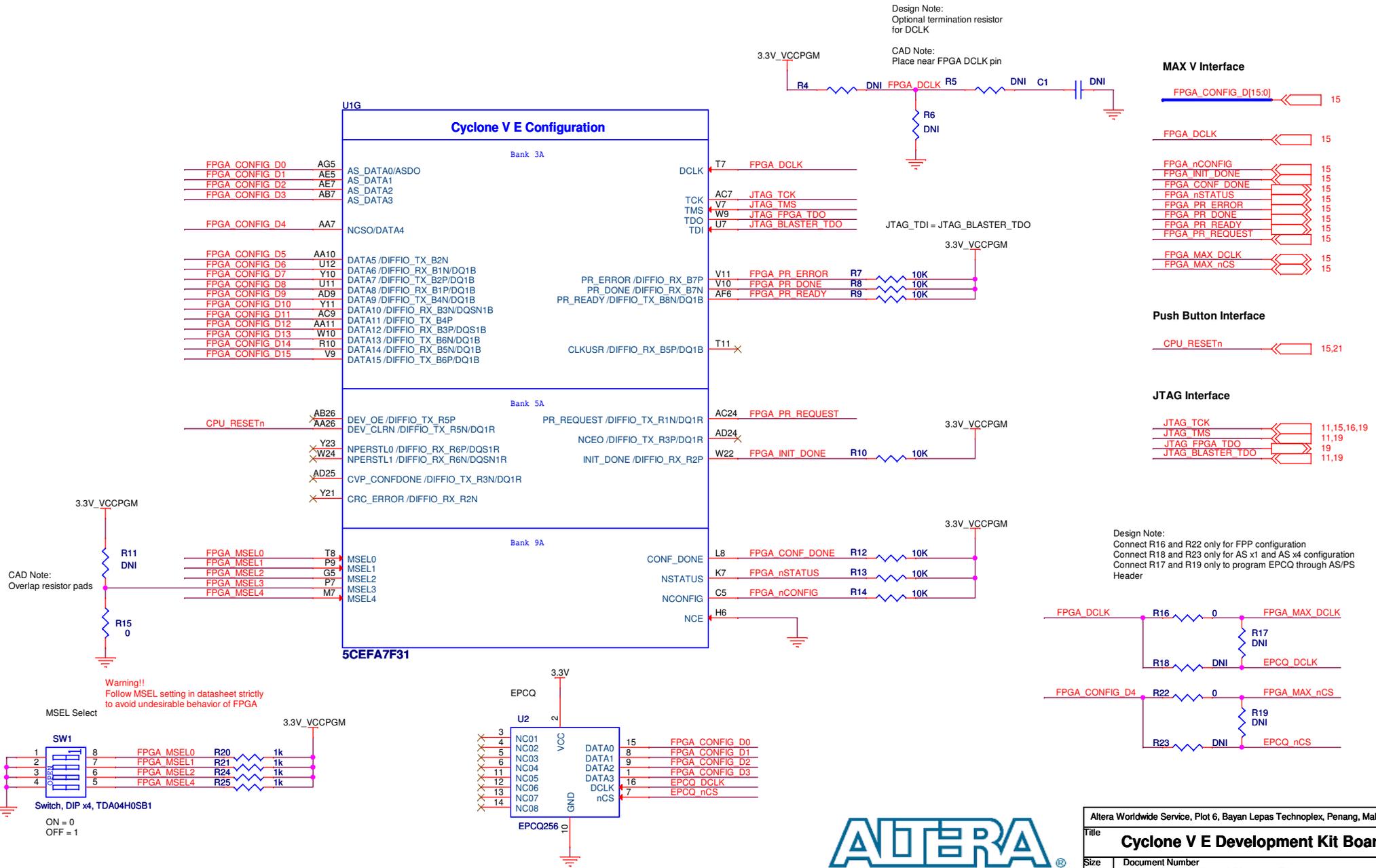
Altera Worldwide Service, Plot 6, Bayan Lepas Technoplex, Penang, Malaysia

Title **Cyclone V E Development Kit Board**

Size B Document Number 150-0321002- B1 (6XX-44161R) Rev B1

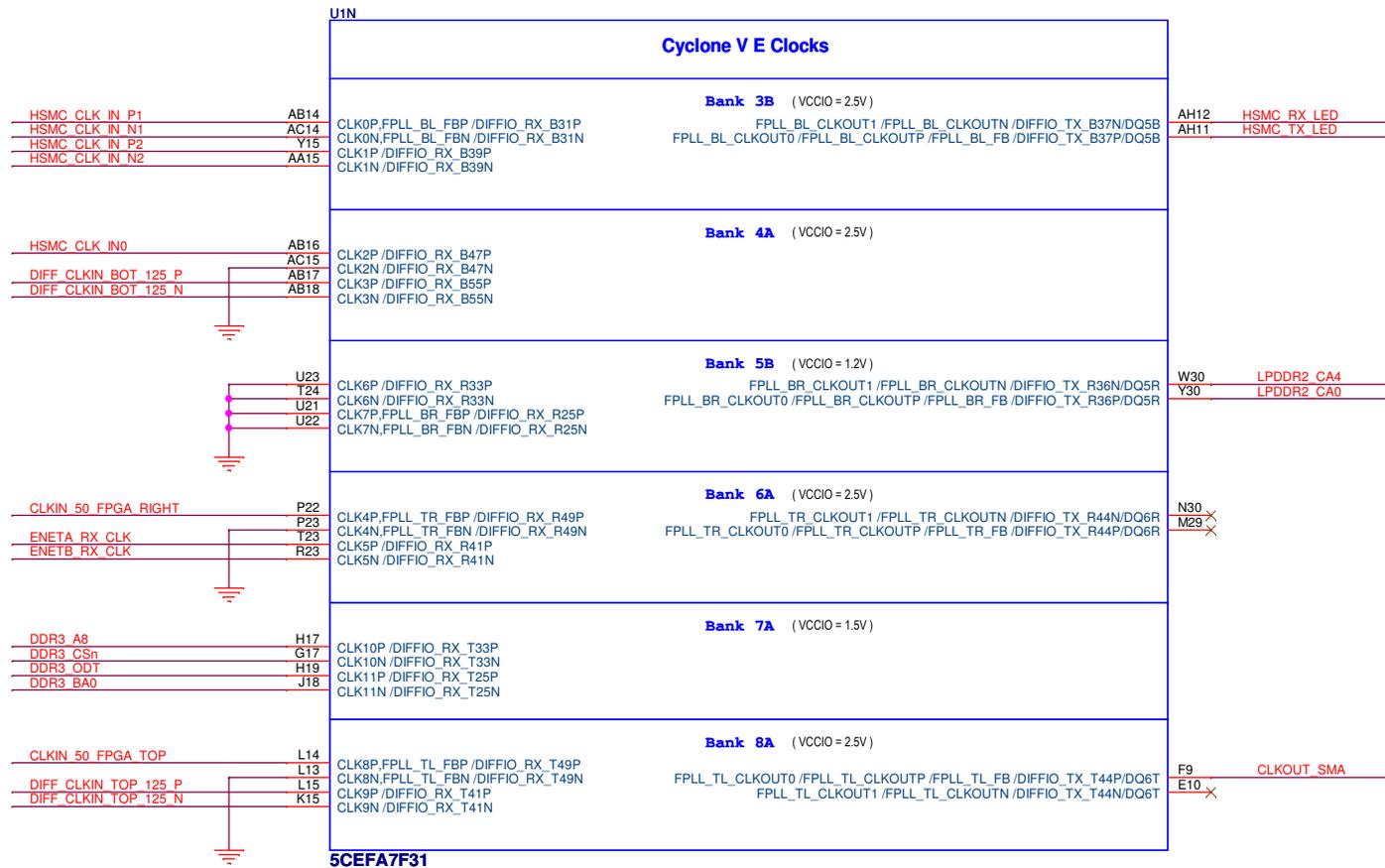
Date: Thursday, November 15, 2012 Sheet 7 of 29

Cyclone V E Configuration

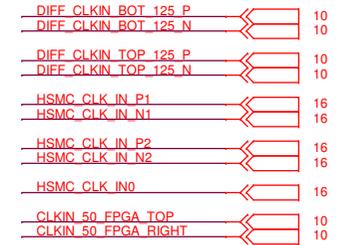


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Title Cyclone V E Development Kit Board		
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Cyclone V E Clocks



PLL INTERFACE



HSMC LED INTERFACE



DDR3 INTERFACE



LPDDR2 INTERFACE

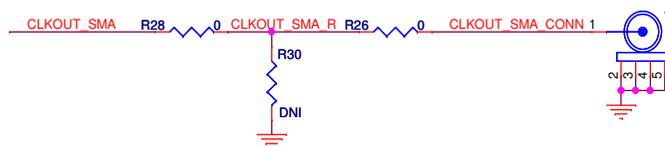
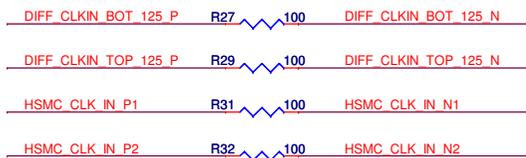


ETHERNET INTERFACE



CAD Note:
Place resistors near FPGA pins

CAD Note:
Place resistors near FPGA pins
and near to each other



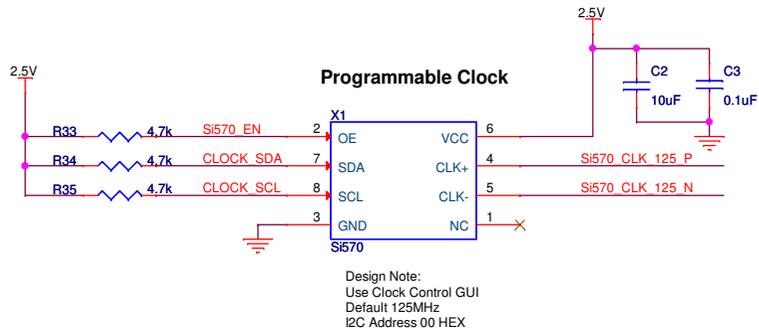
Altera Worldwide Service, Plot 6, Bayan Lepas Technoplex, Penang, Malaysia

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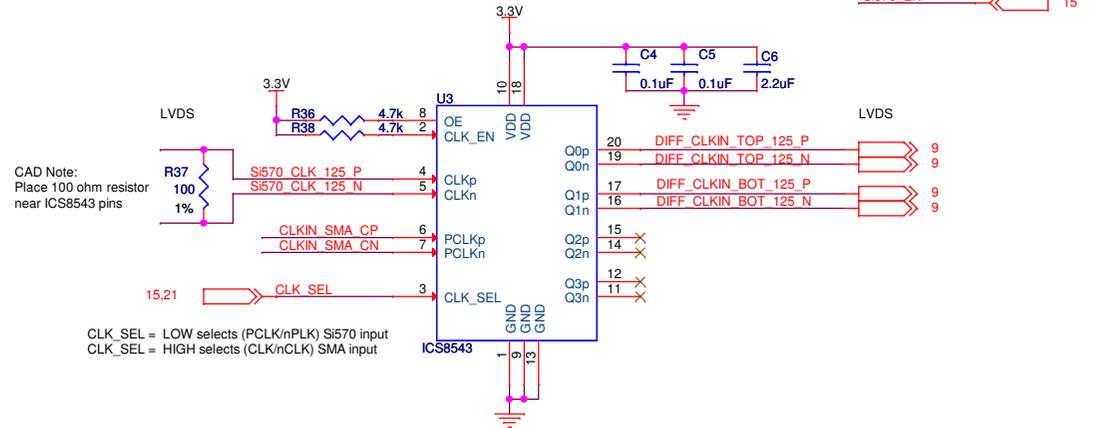
Size B Document Number 150-0321002- B1 (6XX-44161R) Rev B1

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PLL



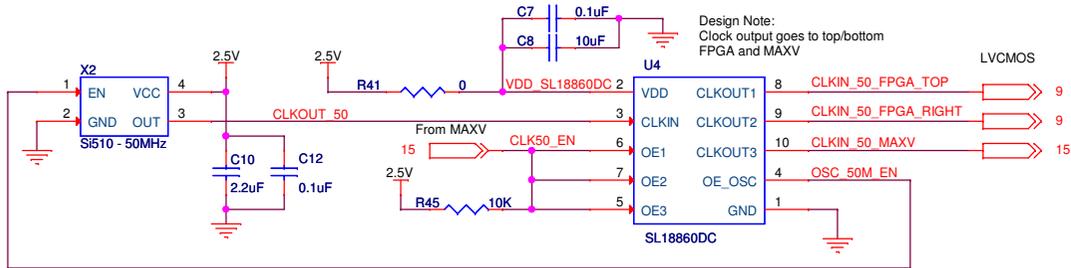
Differential Clock Distribution to Top, Bottom & Right Banks



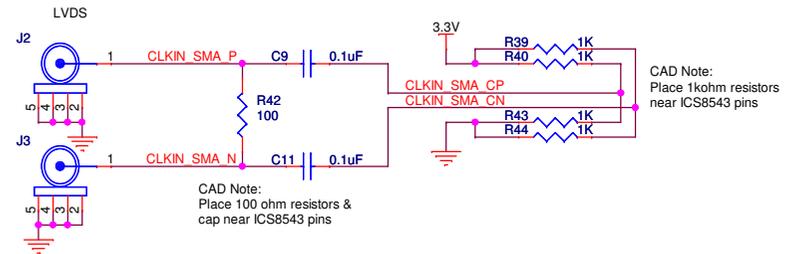
FPGA Interface



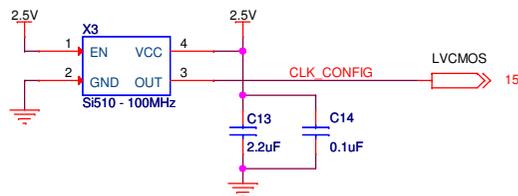
50MHz LVCMOS Clocks for FPGA and MAXV



User Clock Input



100MHz Configuration Clock



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Title **Cyclone V E Development Kit Board**

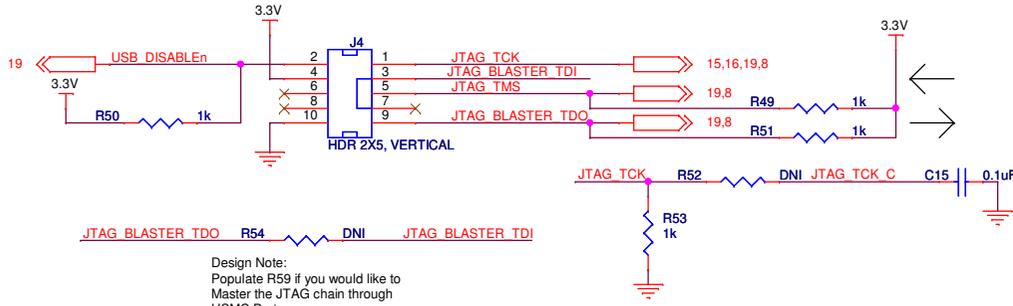
Size B Document Number 150-0321002- B1 (6XX-44161R)

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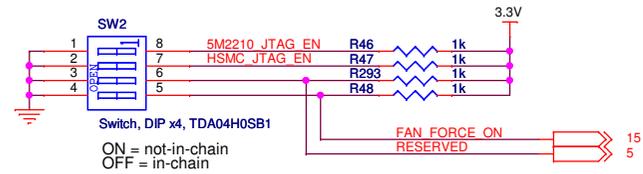
JTAG

USB Blaster Programming Header (uses JTAG mode only)



Design Note:
Populate R59 if you would like to
Master the JTAG chain through
HSMC Port.

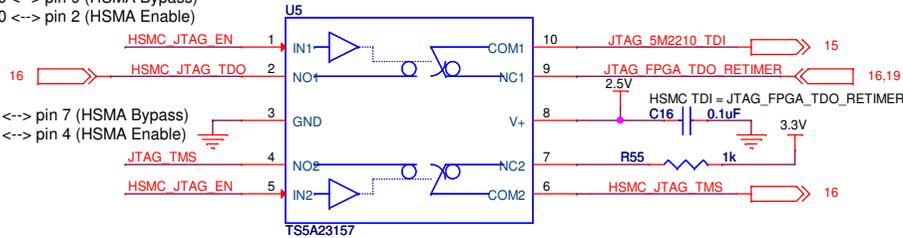
JTAG Chain Control



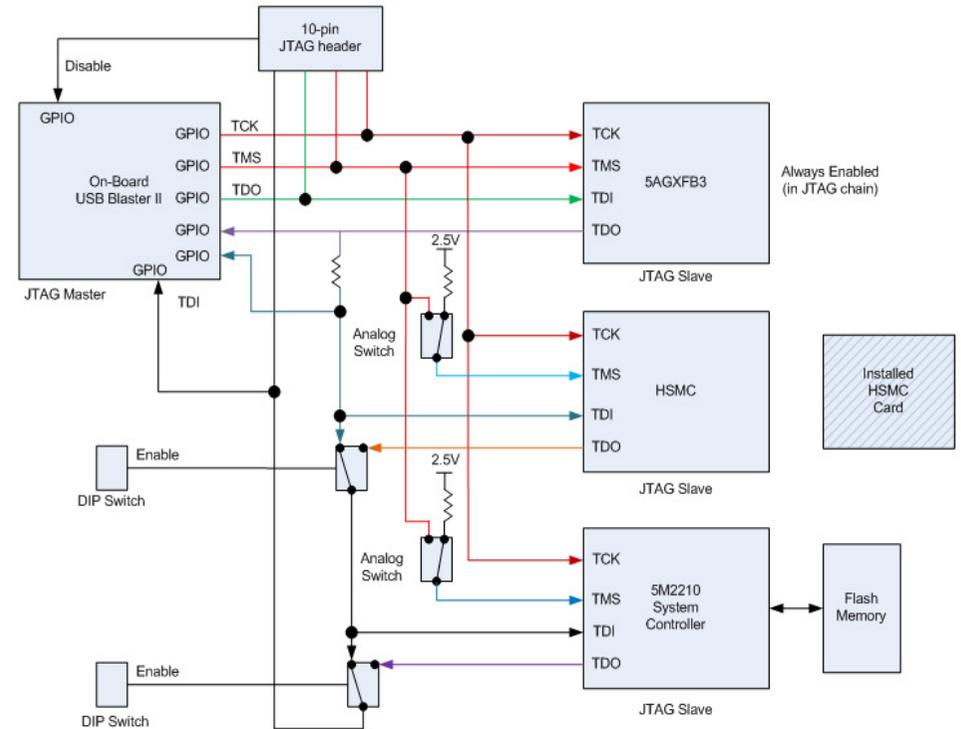
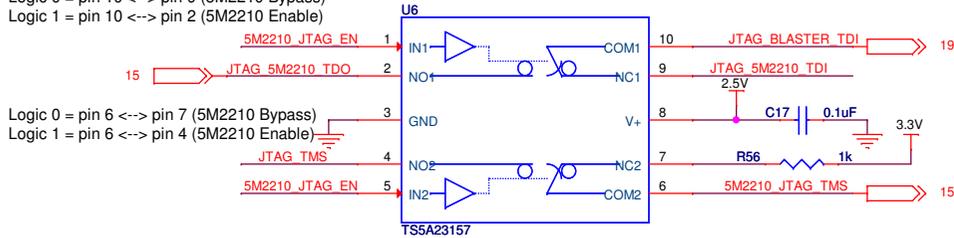
TS5A23157 Switch Functions

When Pins 1 & 5 are:
LOW --> NC to/from COM = ON and NO to/from COM = OFF
HIGH --> NC to/from COM = OFF and NO to/from COM = ON

Logic 0 = pin 10 <-> pin 9 (HSMA Bypass)
Logic 1 = pin 10 <-> pin 2 (HSMA Enable)



Logic 0 = pin 10 <-> pin 9 (5M2210 Bypass)
Logic 1 = pin 10 <-> pin 2 (5M2210 Enable)



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Title **Cyclone V E Development Kit Board**

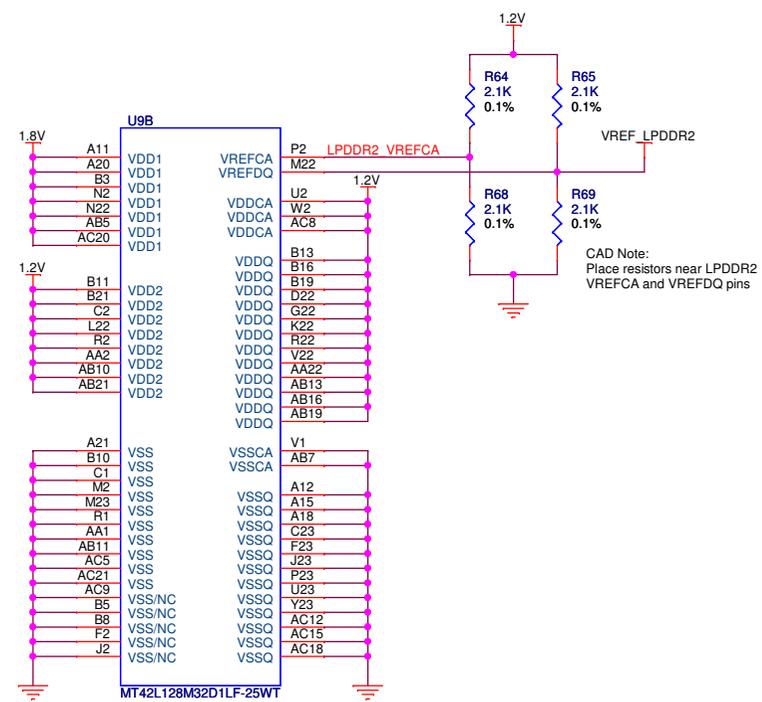
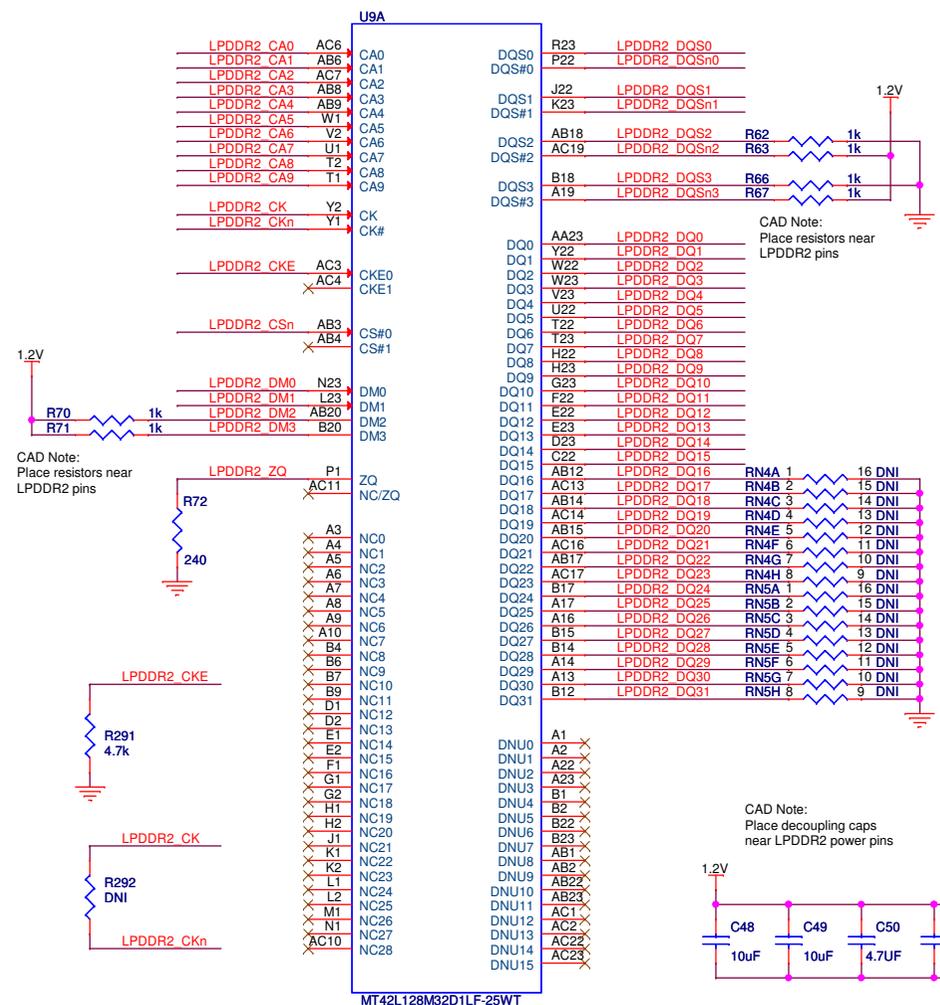
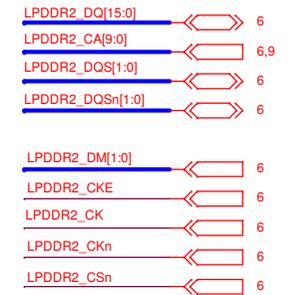
Size B Document Number 150-0321002- B1 (6XX-44161R) Rev B1

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LPDDR2 SDRAM x16

LPDDR2 SDRAM (16M X 32 X 8 banks x 1 die)

FPGA Interface

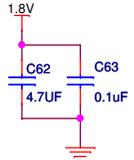
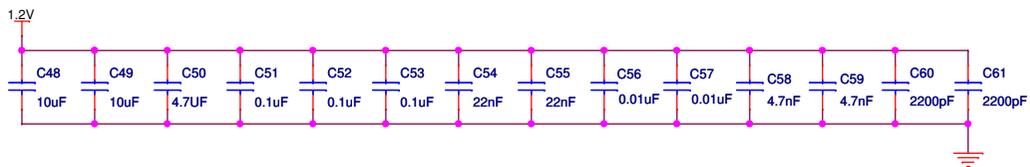


CAD Note:
Place resistors near LPDDR2 pins

CAD Note:
Place resistors near LPDDR2 VREFCA and VREFDQ pins

Design Note:
Pin compatible between MT42L128M32D1LF-25 and MT42L64M32D1KQ
Pins AC9, B5, B8, F2 and J2 can be VSS/NC

CAD Note:
Place decoupling caps near LPDDR2 power pins

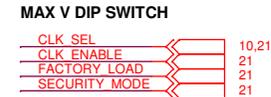
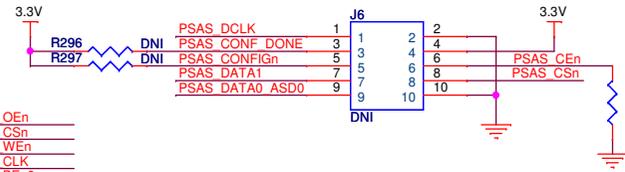
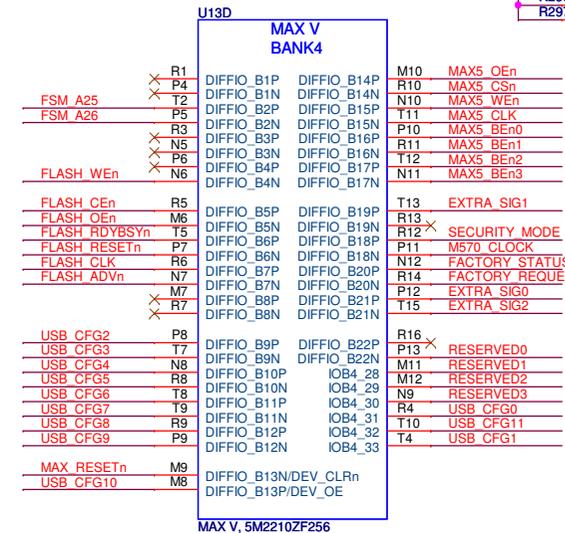
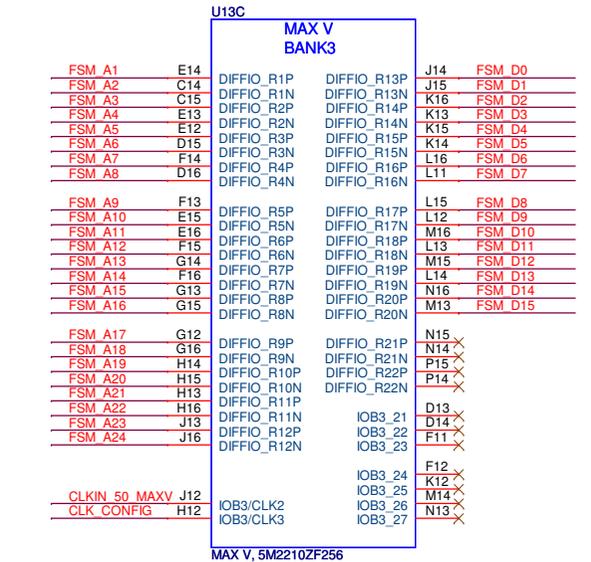
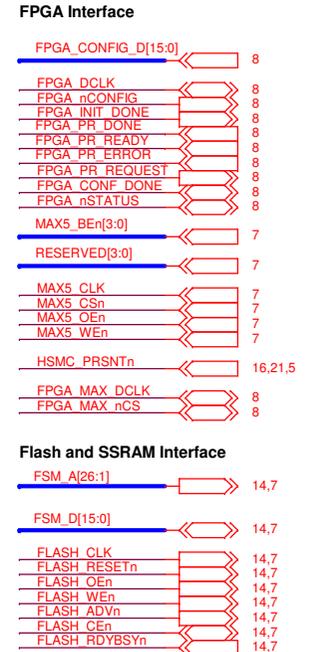
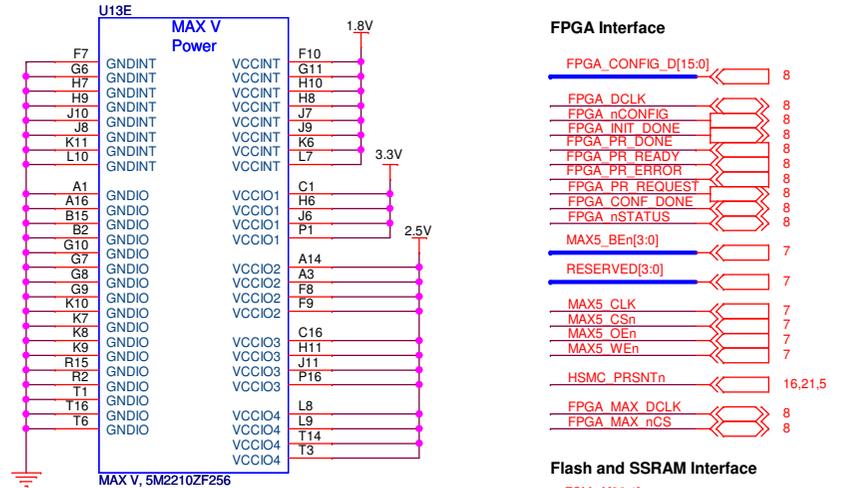
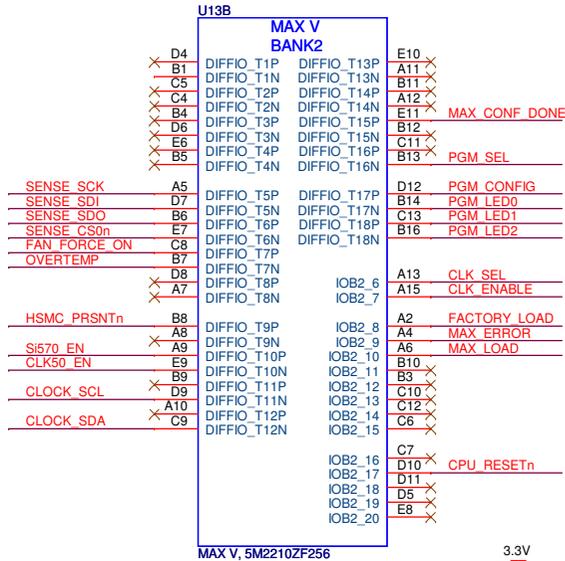
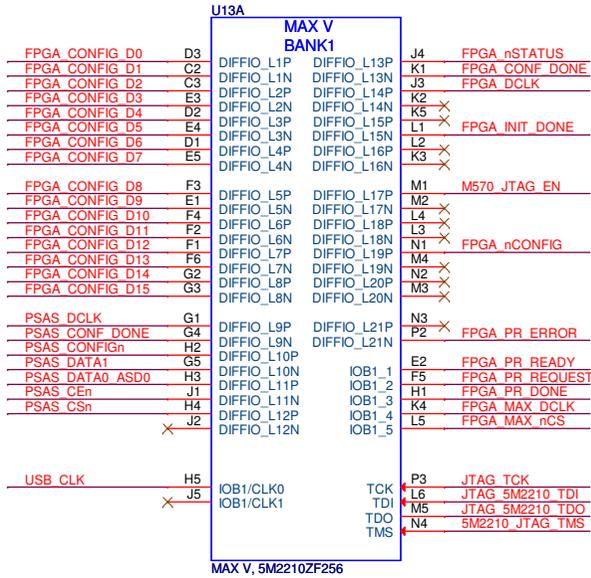


Design Note:
Only x16 configuration is used on the x32 device



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Title Cyclone V E Development Kit Board		
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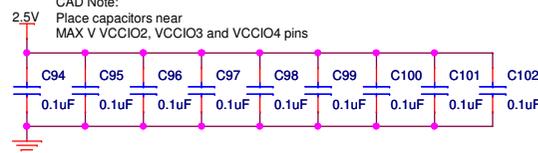
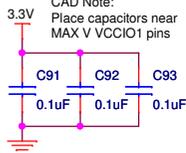
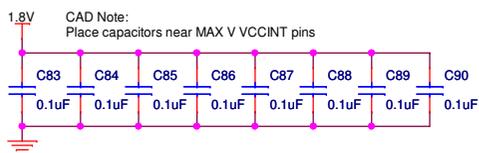
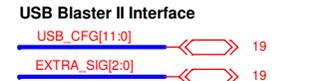
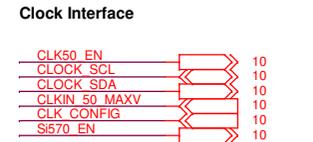
5M2210 System Controller



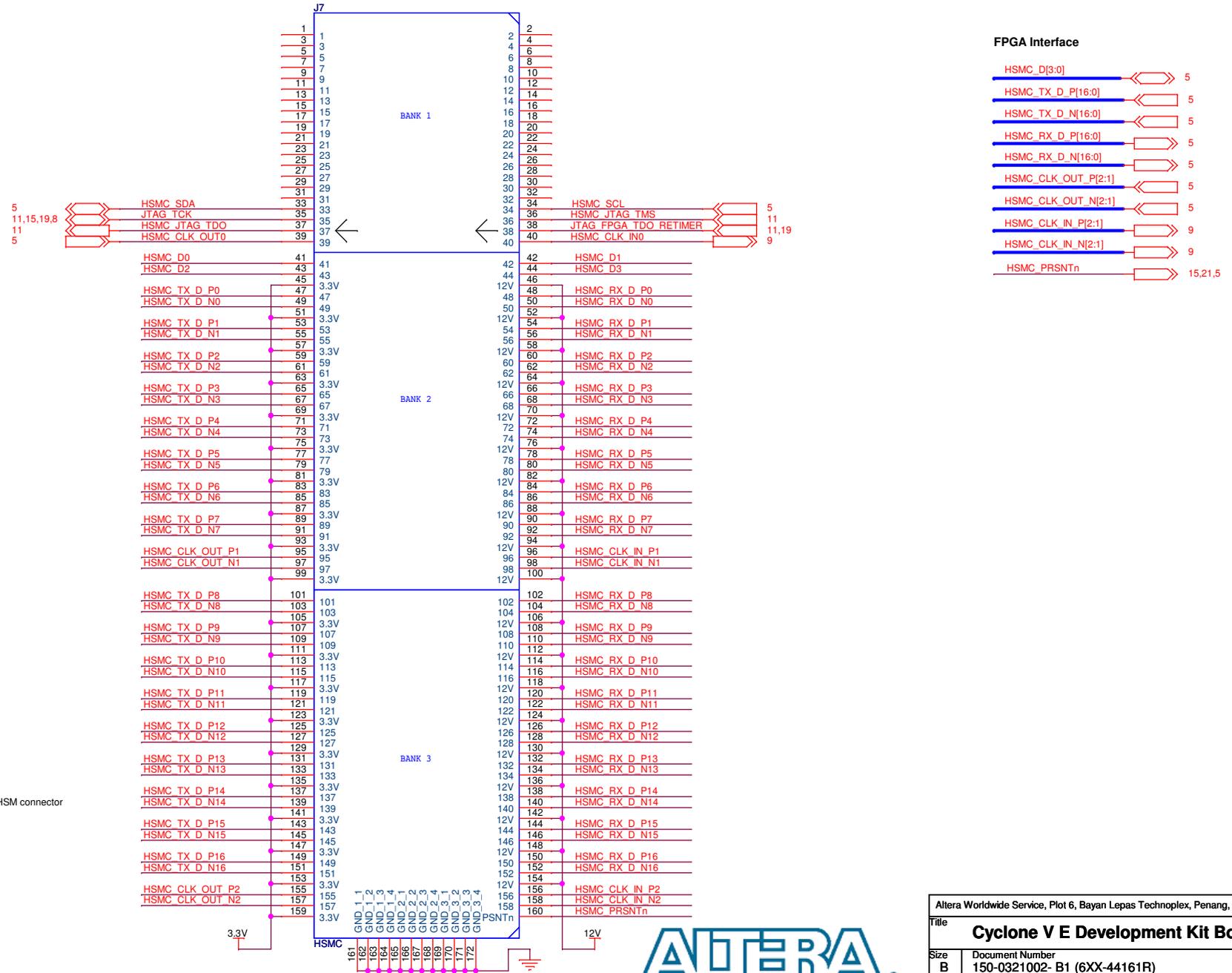
Power Monitor interface



MAX V LED

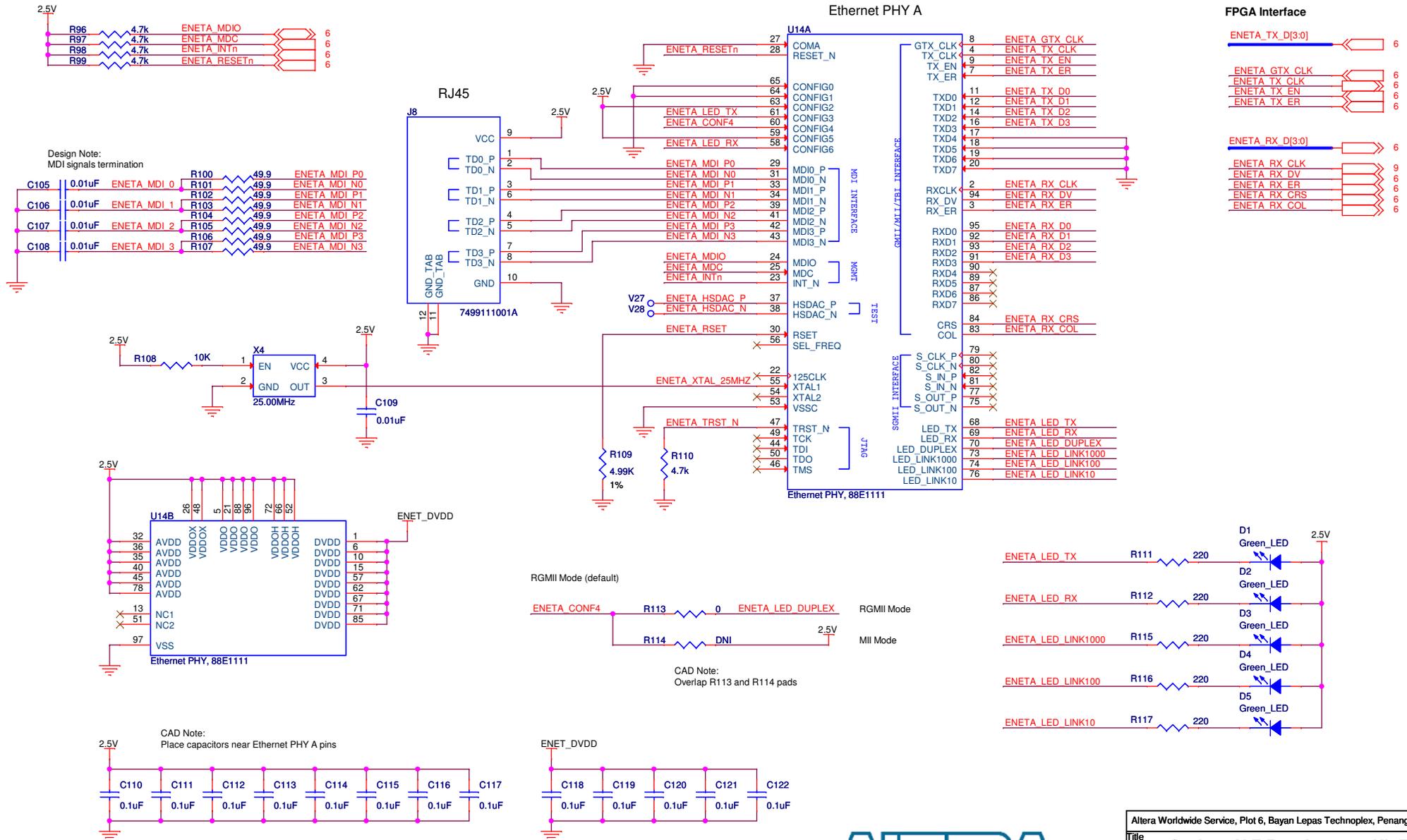


HSMC Port

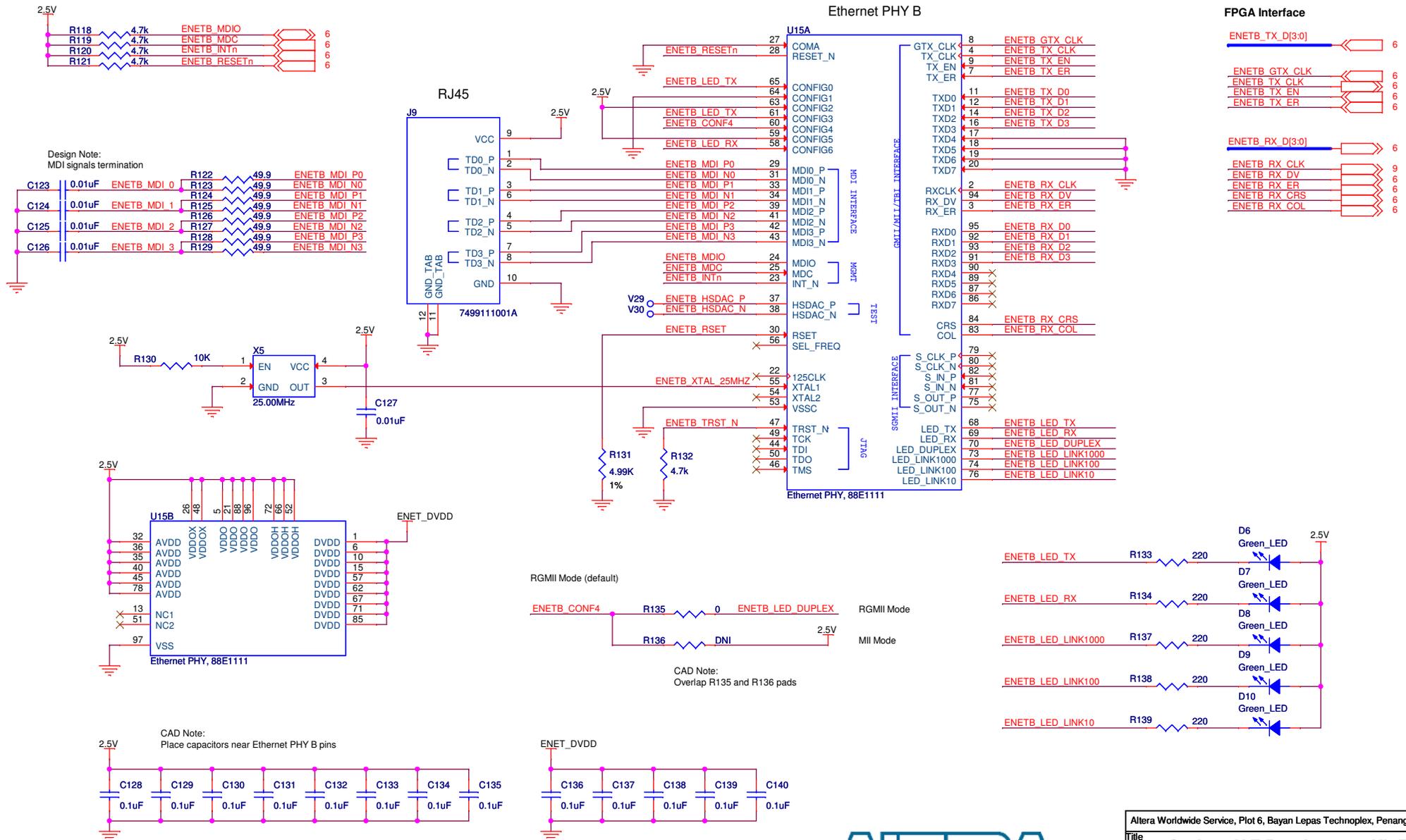


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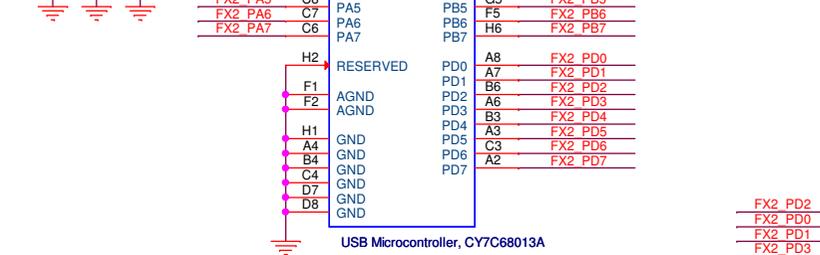
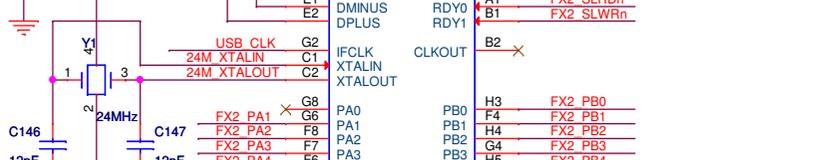
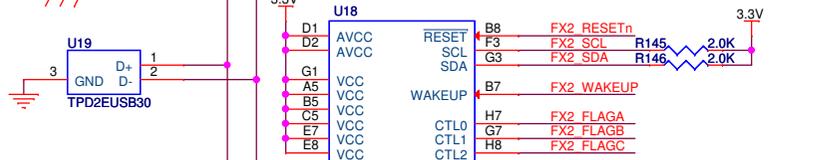
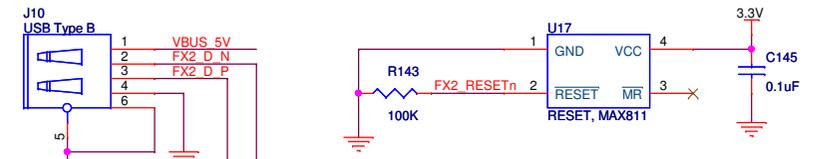
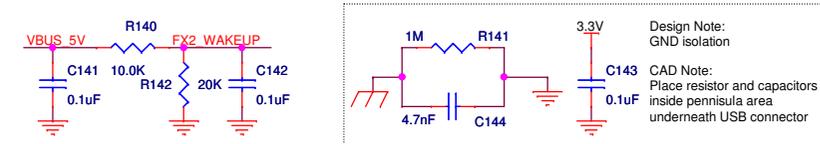
10/100/1000 Ethernet A



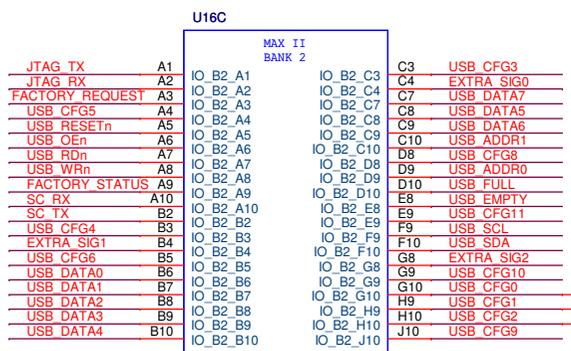
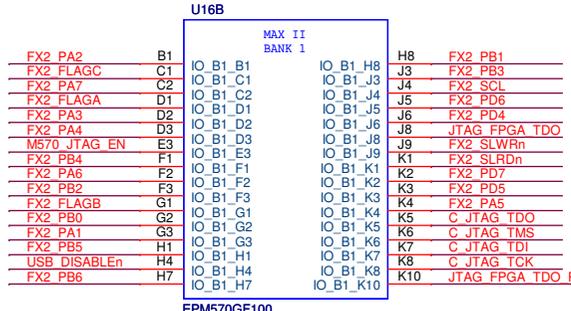
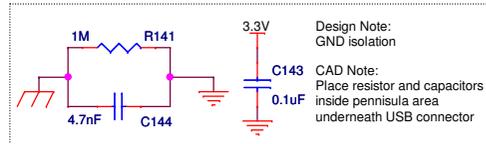
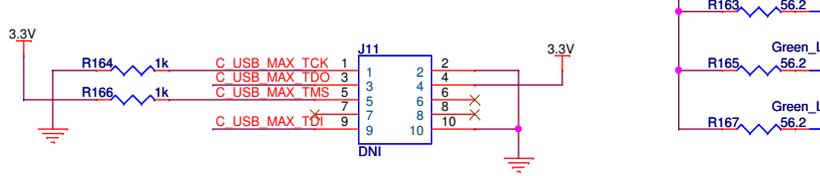
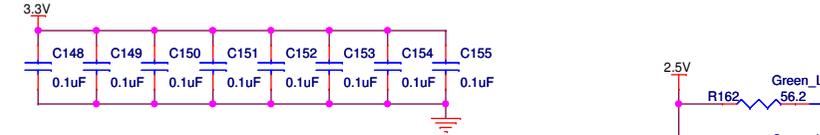
10/100/1000 Ethernet B



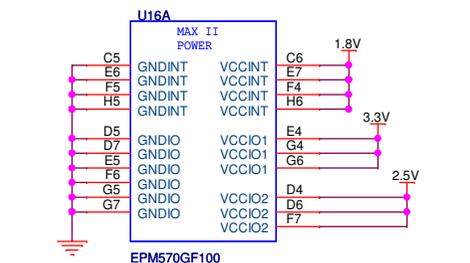
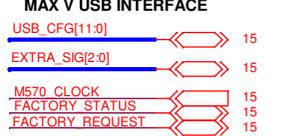
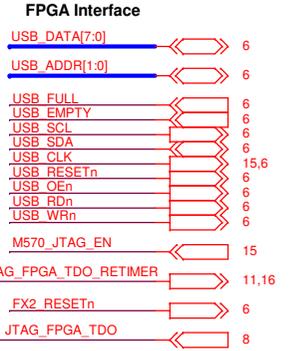
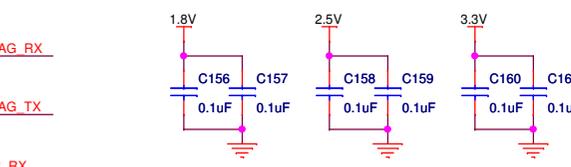
USB Blaster II



CAD Note:
Place capacitors near CY7C68013A power pins

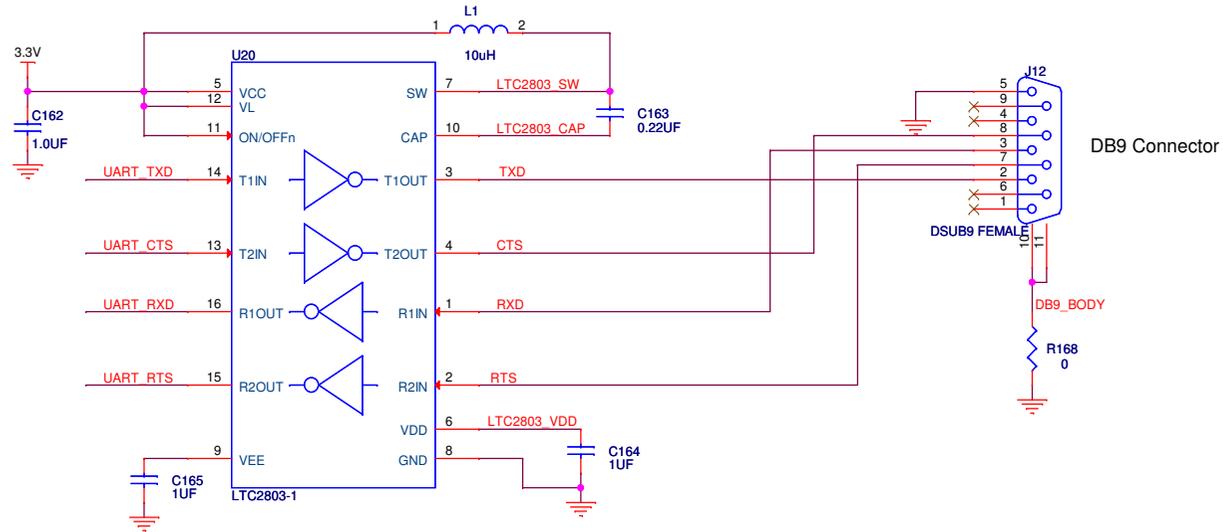


CAD Note:
Place capacitors near MAXII EPM570 power pins



UART

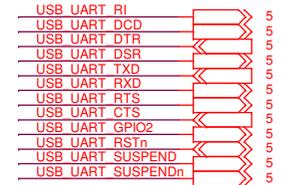
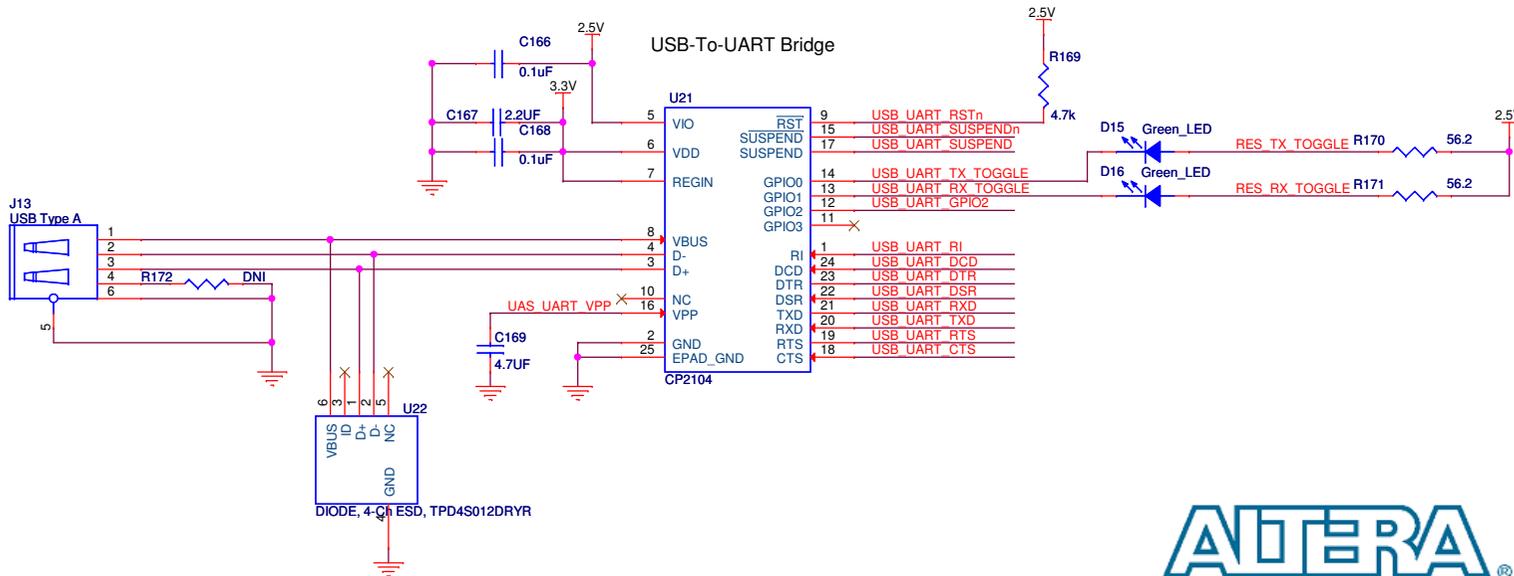
RS-232 Transceiver



FPGA Interface



USB-To-UART Bridge



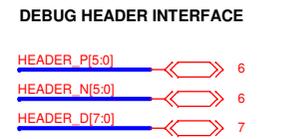
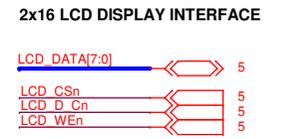
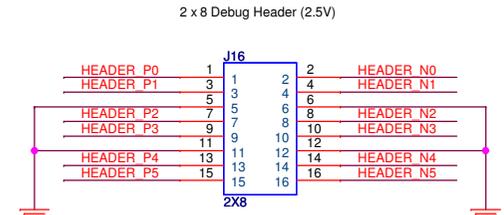
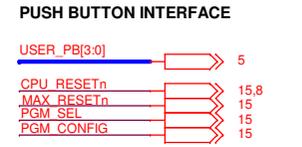
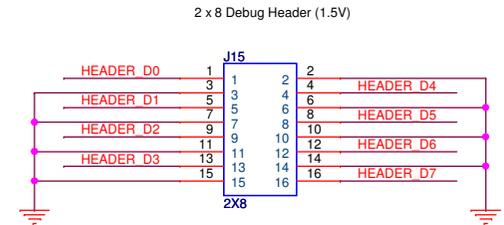
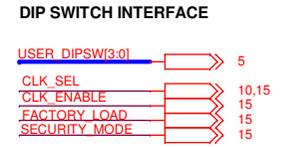
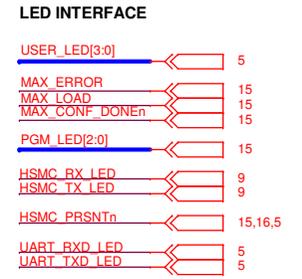
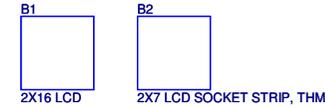
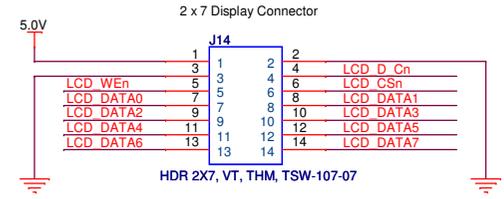
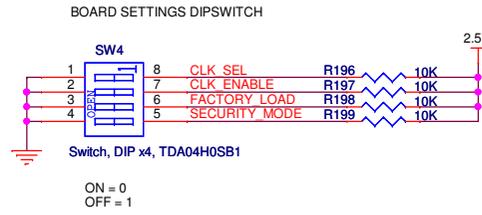
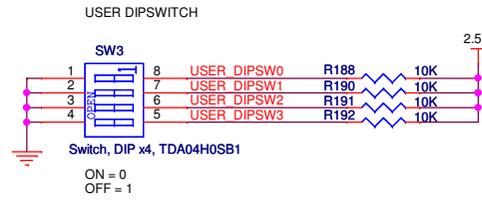
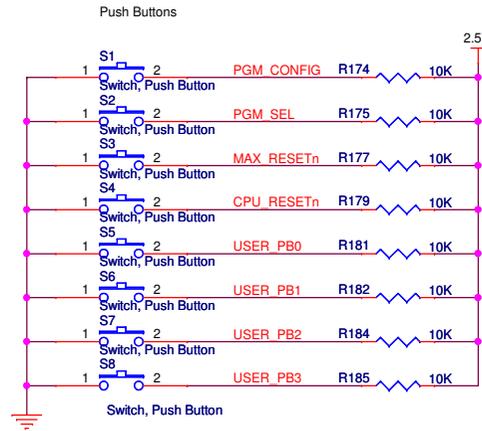
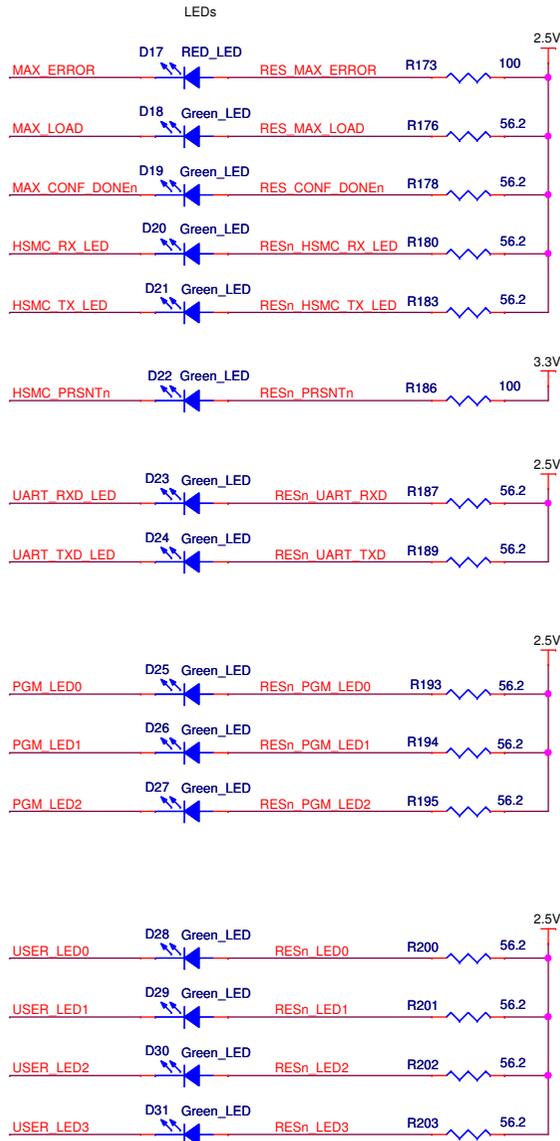
Altera Worldwide Service, Plot 6, Bayan Lepas Technoplex, Penang, Malaysia

Title **Cyclone V E Development Kit Board**

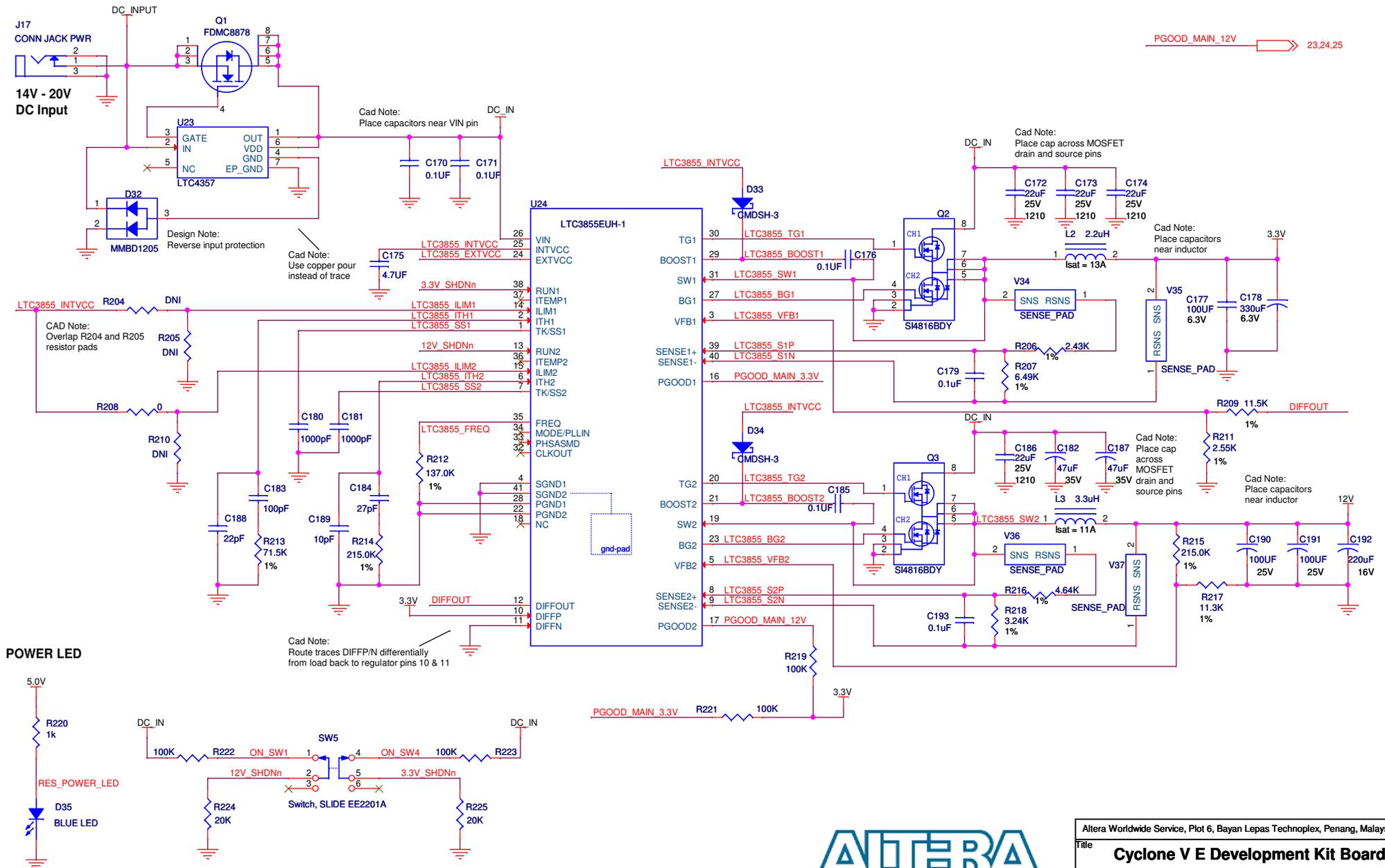
Size B Document Number 150-0321002- B1 (6XX-44161R) Rev B1

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User I/O and Connector

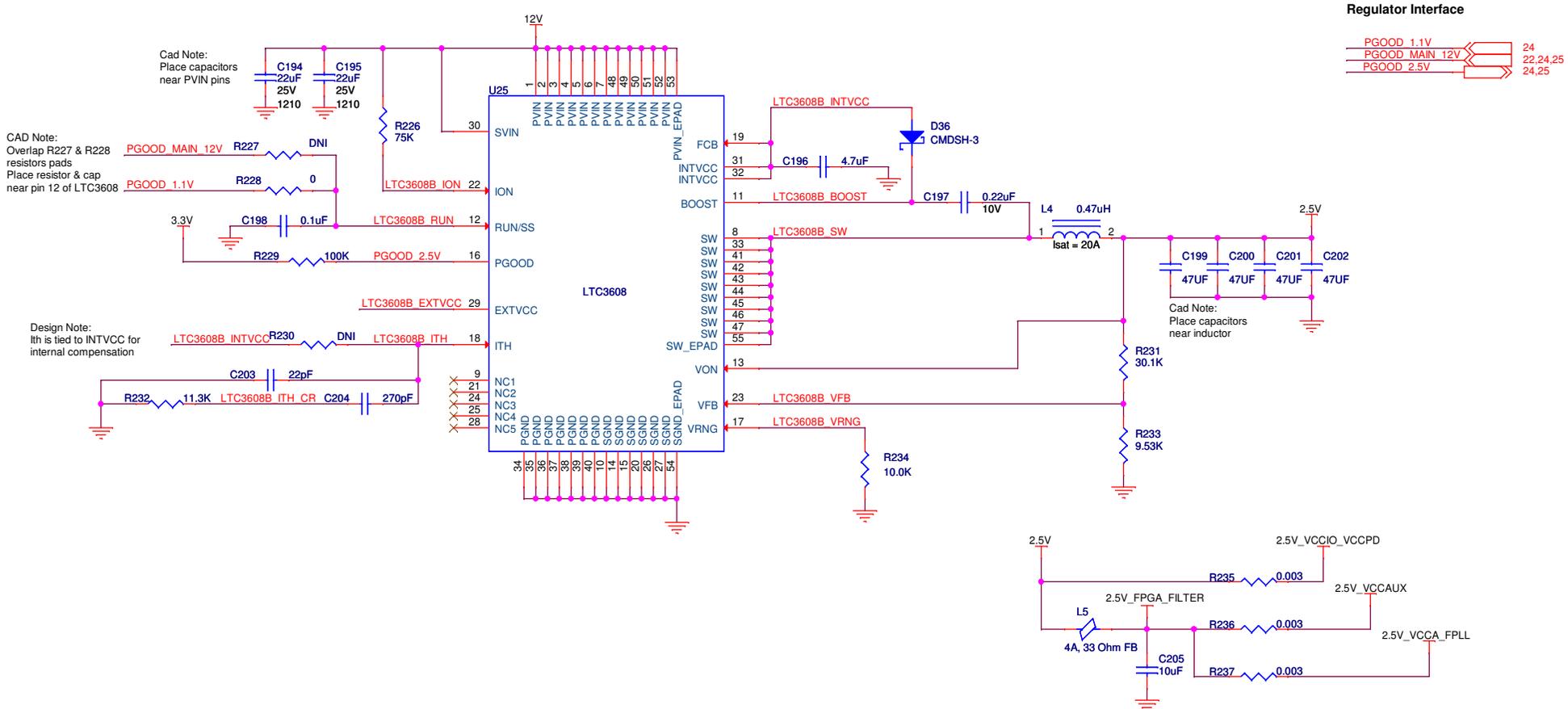


Power 1 - DC Input & 12V, 3.3V Output



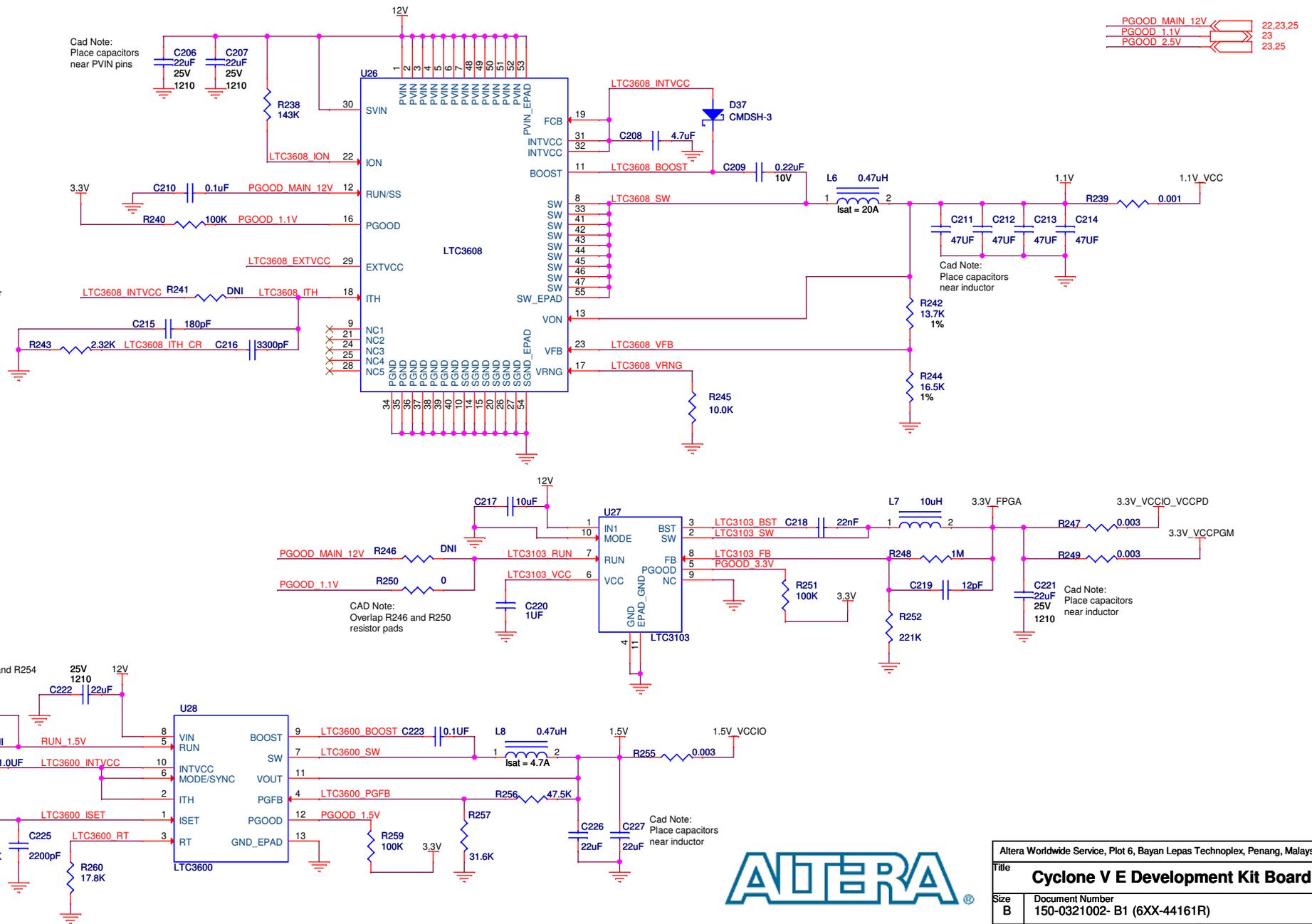
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Power 2 - 2.5V



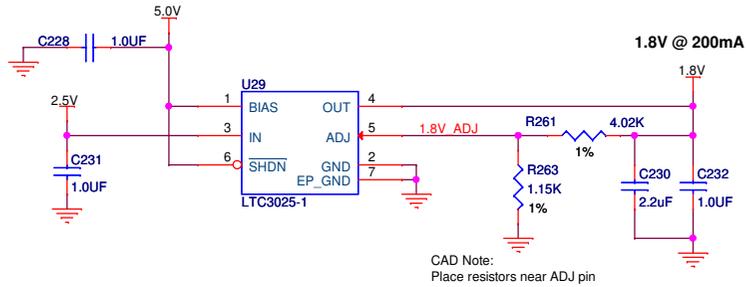
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Power 3 - FPGA 1.1V, 3.3V and 1.5V Output

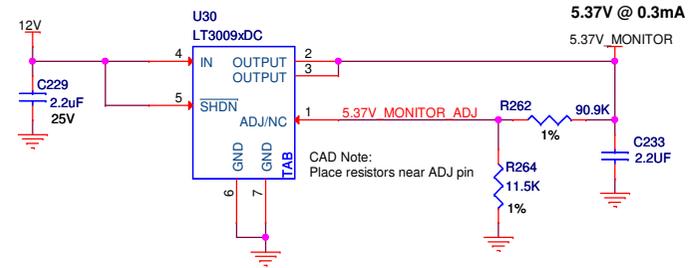


Power 4 - Linear Regulators

Flash VCC/VPP, MAXV/MAXII VCCINT & LPDDR2 VDD1

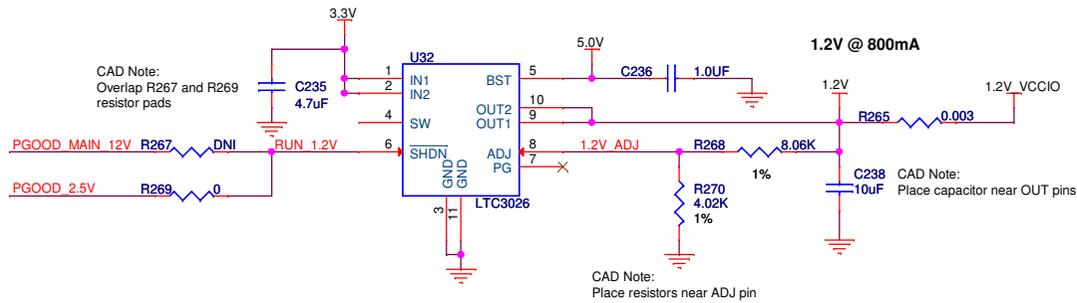


Power Monitor VIN

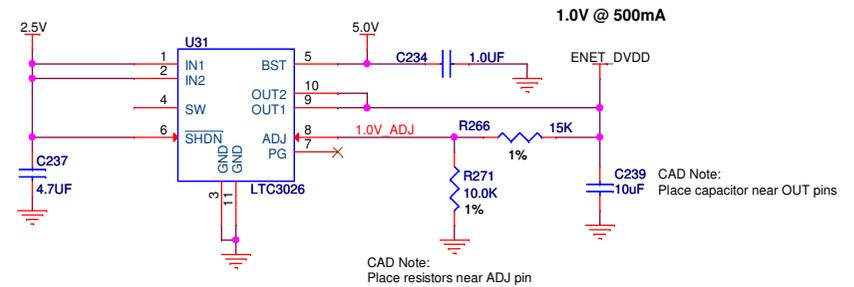


PGOOD MAIN 12V 22,23,24
PGOOD 2.5V 23,24

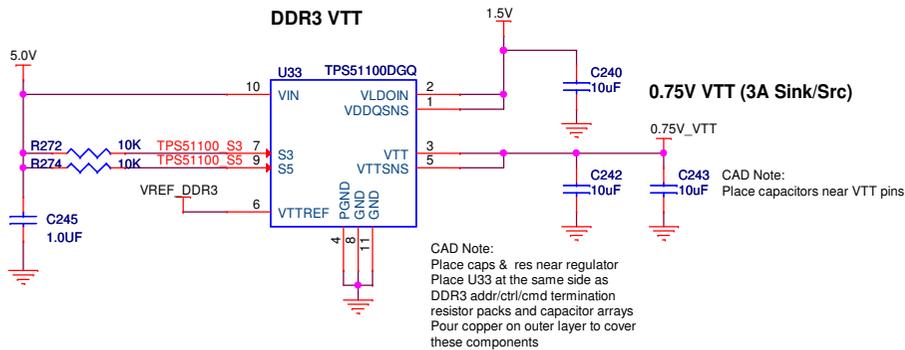
LPDDR2 VDD2, VDDQ, VDDCA, FPGA VCCIO_1.2V



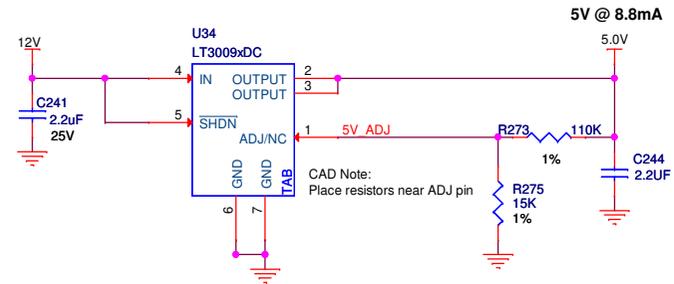
Ethernet PHY DVDD/VDDO



DDR3 VTT

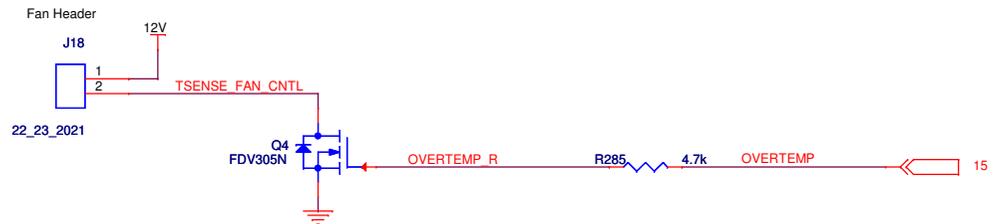
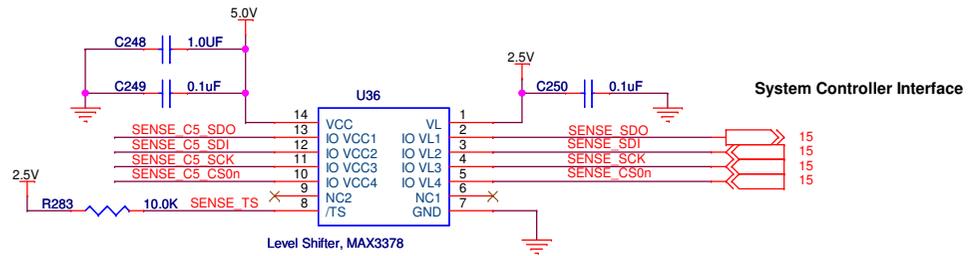
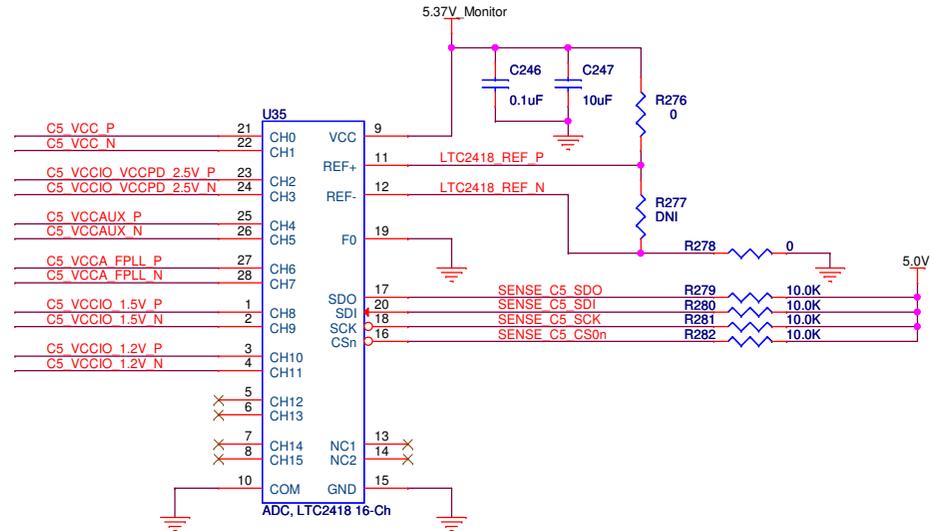
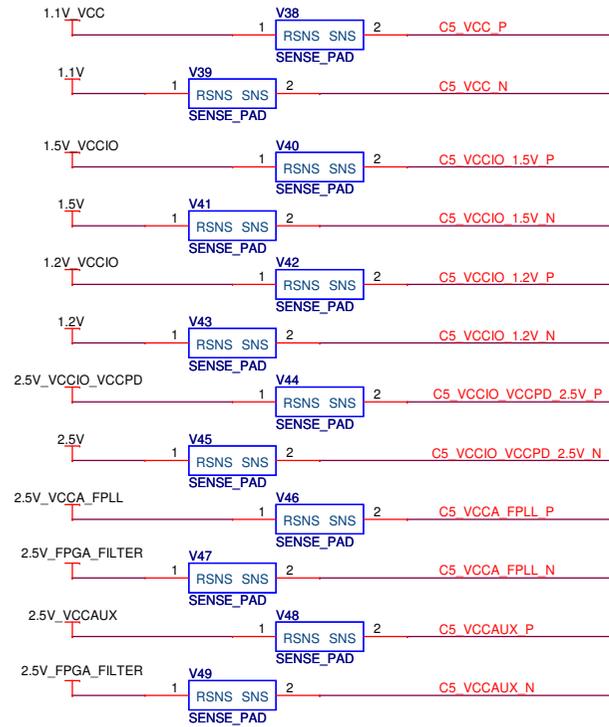


VTT LDO, LCD Character, SPI Level Shifter



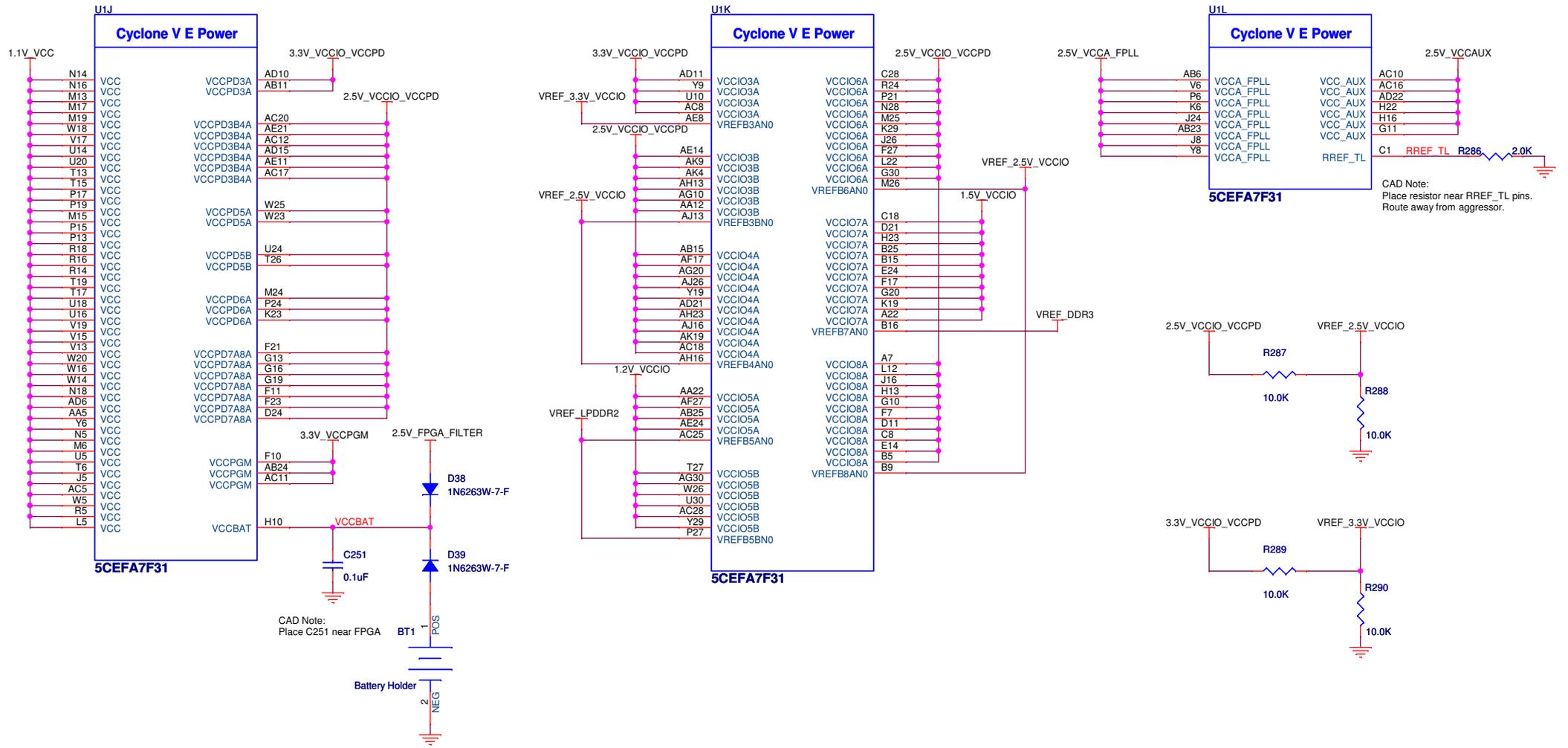
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Power Monitor



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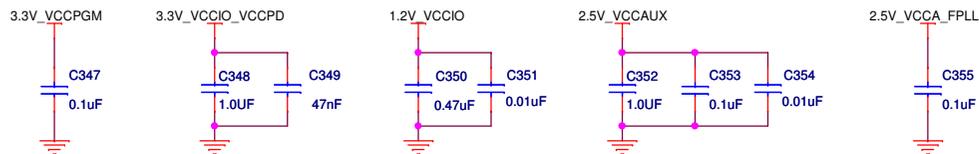
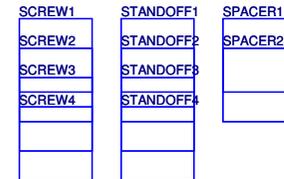
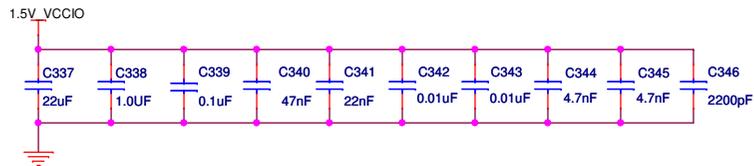
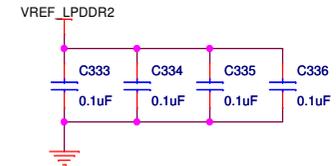
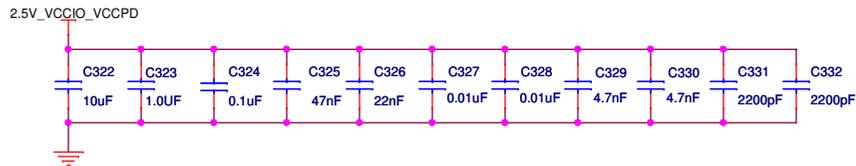
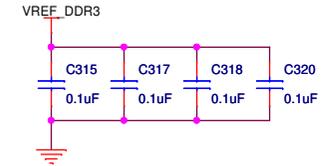
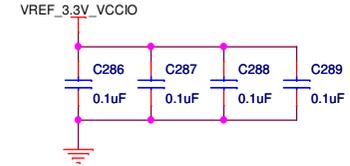
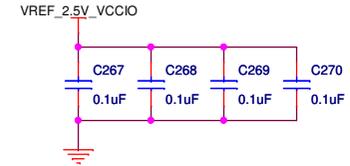
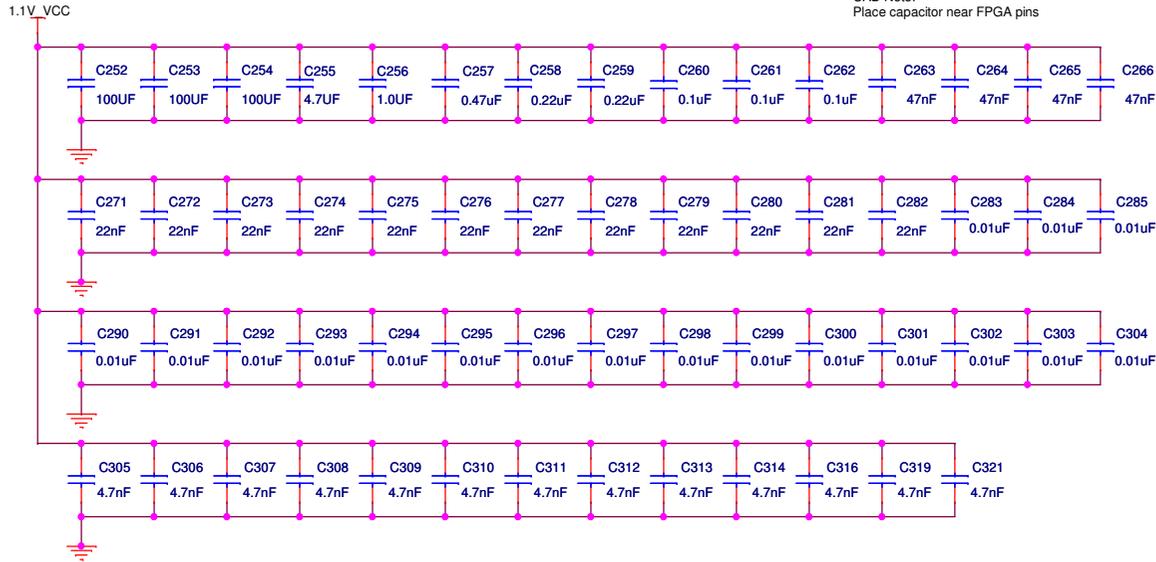
Cyclone V E Bank 3 and Bank 4



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Cyclone V E Decoupling

CAD Note:
Place capacitor near FPGA pins



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