

# **Modular SGDMA Read Master Core**

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## Core Overview

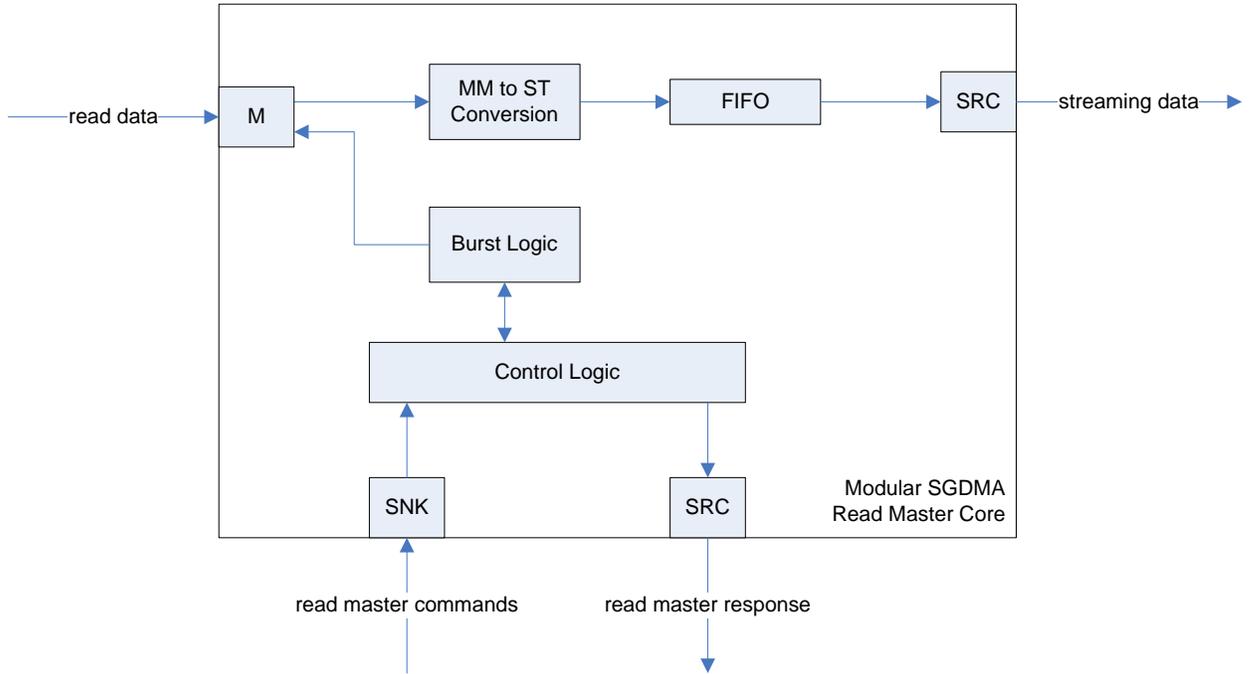
The modular scatter-gather direct memory access (SGDMA) read master module is responsible for reading data from memory and forwarding it to an Avalon-Streaming (ST) port. The read master module is designed to be connected to the modular SGDMA dispatcher module but you can supply your own controller as well. The read master module is controlled by a ST command port and optional response data is sent via a ST response port.

There are various options that can be enabled to add functionality to the read master module. The read master module supports the following options:

- 8 to 1024 bit data width
- Up to 4 GB transfer lengths
- Unaligned accesses
- Burst transactions
- Stride addressing
- ST packet support
- ST channel support
- ST error support

# Block Diagram

Figure 1 shows the significant blocks that make up the read master core.



*Figure 1. Modular SGDMA Read Master Core*

## Read Master Port Listing

This section will discuss the various Avalon-MM and ST ports that are exposed by the modular SGDMA read master module. Some of the signals that are exposed are not used by the dispatcher module and are documented for completeness.

### ***Read Commands Sink Port***

<b>Bits</b>	<b>Signal Information</b>
31-0	Read Address [31:0]
63-32	Length [31:0]
71-64	Transmit Channel [7:0]
72	Generate SOP
73	Generate EOP
74	Stop <sup>1</sup>
75	Reset <sup>1</sup>
83-76	Read Burst Count [7:0]
99-84	Read Stride [15:0]
107-100	Transmit Error [7:0]
108	Early Done Enable
255-109	<reserved> <sup>2</sup>

*Table 1. Read Commands Sink Port Bitfields*

<sup>1</sup> Combinational signals that don't obey flow control

<sup>2</sup> Reserved bits driven to ground

### ***Read Response Source Port***

<b>Bits</b>	<b>Signal Information</b>
0	Reset Delayed <sup>1</sup>
1	Stop State <sup>1</sup>
2	Early Done Strobe
3	Done Strobe <sup>2</sup>
255-4	<reserved>

*Table 2. Read Response Source Port Bitfields*

<sup>1</sup> Combinational signals that don't obey flow control

<sup>2</sup> Asserted when all data has been read

## ***Data Master Port***

The data master port is responsible for reading data from memory which the read master module then passes to the data sink port. The data master port supports pipeline read transfers and optional burst transactions. You are provided options for configuring the data width, burst length, and memory alignment. To learn more about the configuration options refer to the configuration options section of this document.

## ***Data Sink Port***

The data sink port is responsible for sending data to the write master module or any component that contains a streaming sink port. The port includes support for packets, channels, and errors. To learn more about the configuration options refer to the configuration options section of this document.

## **Configuration Options**

The modular SGDMA has numerous configuration options to enable various functional units. Unnecessary functionality can be disabled to save resources and increase the frequency of the read master module. This section will discuss the various options for the read master module. Important to note are the options that require that the modular SGDMA dispatcher module to have the extended features support enabled.

## Transfer Options

Parameter	Legal Values	Description
Data Width	8, 16, 32, 64, 128, 256, 512, 1024	Data width of the master and streaming ports.
Length Width	10-32	Transfer length in bytes.
FIFO Depth	16, 32, 64, 128, 256, 512, 1024, 2048, 4096	The FIFO depth setting must be at least twice the maximum burst count setting. To maximize the read master module efficiency you should set the FIFO depth to be at least twice the maximum read latency of all the memories connected to the data master. The FIFO depth must be at least four times the maximum burst count
Stride Addressing Enable <sup>1</sup>	On/Off	Enable stride addressing if you want the read master module to perform fixed or non-sequential memory accesses. This feature is not supported when burst or unaligned accesses support is enabled.
Stride Width <sup>1</sup>	1-16	Stride width is specified in words. The following are examples of various stride addressing:  0 – Fixed read address 1 – Sequential read address 2 – Read every other word  The stride width must be set to at least $\text{floor}(\log_2(\text{maximum stride})) + 1$ .
Burst Enable	On/Off	Enable burst support when you connect the read master module to burst capable slave ports.
Maximum Burst Count	2, 4, 8, 16, 32, 64, 128, 256, 512, 1024	The maximum burst count must be less than or equal to a quarter of the FIFO depth setting.
Programmable Burst Enable <sup>1</sup>	On/Off	Programmable burst support allows you to program on a per descriptor basis a burst count of 1, 2, 4, 8, 16, 32, 64, or 128. The burst count that is programmed must be less than or equal to the maximum burst count.
Force Burst Alignment Enable	On/Off	When connecting the read master module to burst wrapping slave ports (SDRAM) you must enable this setting. This setting will force the master to post single beat burst transactions until the next burst boundary has been reached to avoid memory corruption.

*Table 3. Transfer Options*

<sup>1</sup> Modular SGDMA dispatcher module must have extended features enabled

## **Memory Access Options**

<b>Parameter</b>	<b>Legal Values</b>	<b>Description</b>
Full Word Accesses Only	On/Off	When full word accesses only is enabled you must provide a read address that is aligned. You must also provide a transfer length is that is a multiple of the data width. This memory access mode results in the smallest hardware footprint and highest frequency.
Aligned Accesses	On/Off	When aligned accesses is enabled you must provide a read address that is aligned. You can provide any transfer length.
Unaligned Accesses	On/Off	When unaligned accesses is enabled you can provide any read address or transfer length. This memory access mode results in the largest hardware footprint and lowest frequency.

*Table 4. Memory Access Options*

## **Streaming Options**

<b>Parameter</b>	<b>Legal Values</b>	<b>Description</b>
Packet Support Enable	On/Off	When packet support is enabled the data streaming port will include the start of packet (SOP), end of packet (EOP), and empty signals.
Error Enable	On/Off	When error support is enabled the data streaming port will include the error signal.
Error Width	1-8	This setting will adjust the width of the error signal. The error width must be set to at least $\text{floor}(\log_2(\text{maximum error})) + 1$ .
Channel Enable	On/Off	When channel support is enabled the data streaming port will include the channel signal.
Channel Width	1-8	This setting will adjust the width of the channel signal. The channel width must be set to at least $\text{floor}(\log_2(\text{maximum channel})) + 1$ .

*Table 5. Streaming Options*