

1. Project Drawing Numbers:		
Raw PCB	100-0321002-	B1
Gerber Files	110-0321002-	B1
PCB Design Files	120-0321002-	B1
Assembly Drawing	130-0321002-	B1
Fab Drawing	140-0321002-	B1
Schematic Drawing	150-0321002-	B1
PCB Film	160-0321002-	B1
Bill of Materials	170-0321002-	B1
Schematic Design Files	180-0321002-	B1
Functional Specification	210-0321002-	B1
PCB Layout Guidelines	220-0321002-	B1
Assembly Rework	320-0321002-	B1

[illegible]

PAGE	DESCRIPTION	PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Rev. History		
2	FPGA Package Top		
3	Power Tree		
4	Clock Tree		
5	Cyclone V E Bank 3 & 4		
6	Cyclone V E Bank 5 & 6		
7	Cyclone V E Bank 7 & 8		
8	Cyclone V E Configuration		
9	Cyclone V E Clocks		
10	PLL		
11	JTAG		
12	DDR3 SDRAM		
13	LPDDR2 SDRAM		
14	Flash, SRAM and EEPROM		
15	5M2210 System Controller		
16	HSMC		
17	Ethernet PHY A & RJ-45		
18	Ethernet PHY B & RJ-45		
19	On-Board USB Blaster II		
20	UART		
21	User I/O and Connector		
22	Power 1 (DC IN, 3.3V MAIN, 12V MAIN)		
23	Power 2 (2.5V)		
24	Power 3 (1.1V,1.5V,3.3V FPGA)		
25	Power 4 (Linear Regulator)		
26	Power Monitor		
27	Cyclone V E Power		
28	Cyclone V E GND		
29	Cyclone V E Decoupling		



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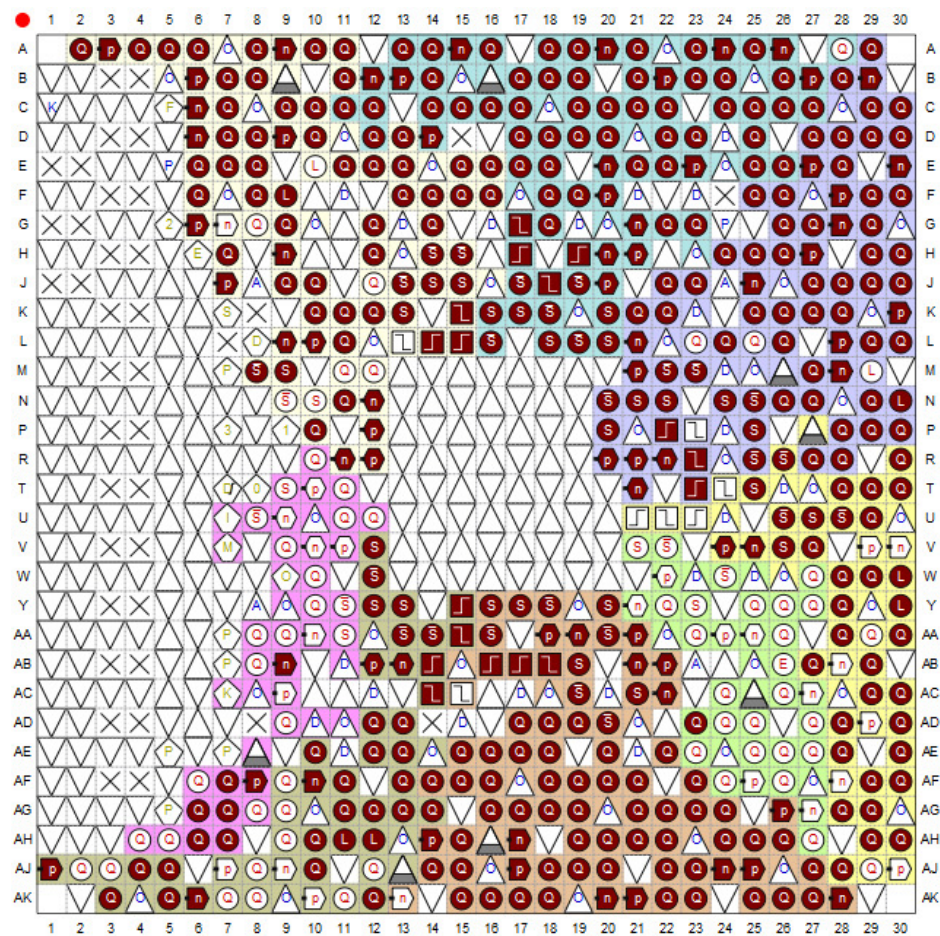
Title	<b>Cyclone V E Development Kit Board</b>
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Size B	Document Number 150-0321002- B1 (6XX-44161R)
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Rev	B1
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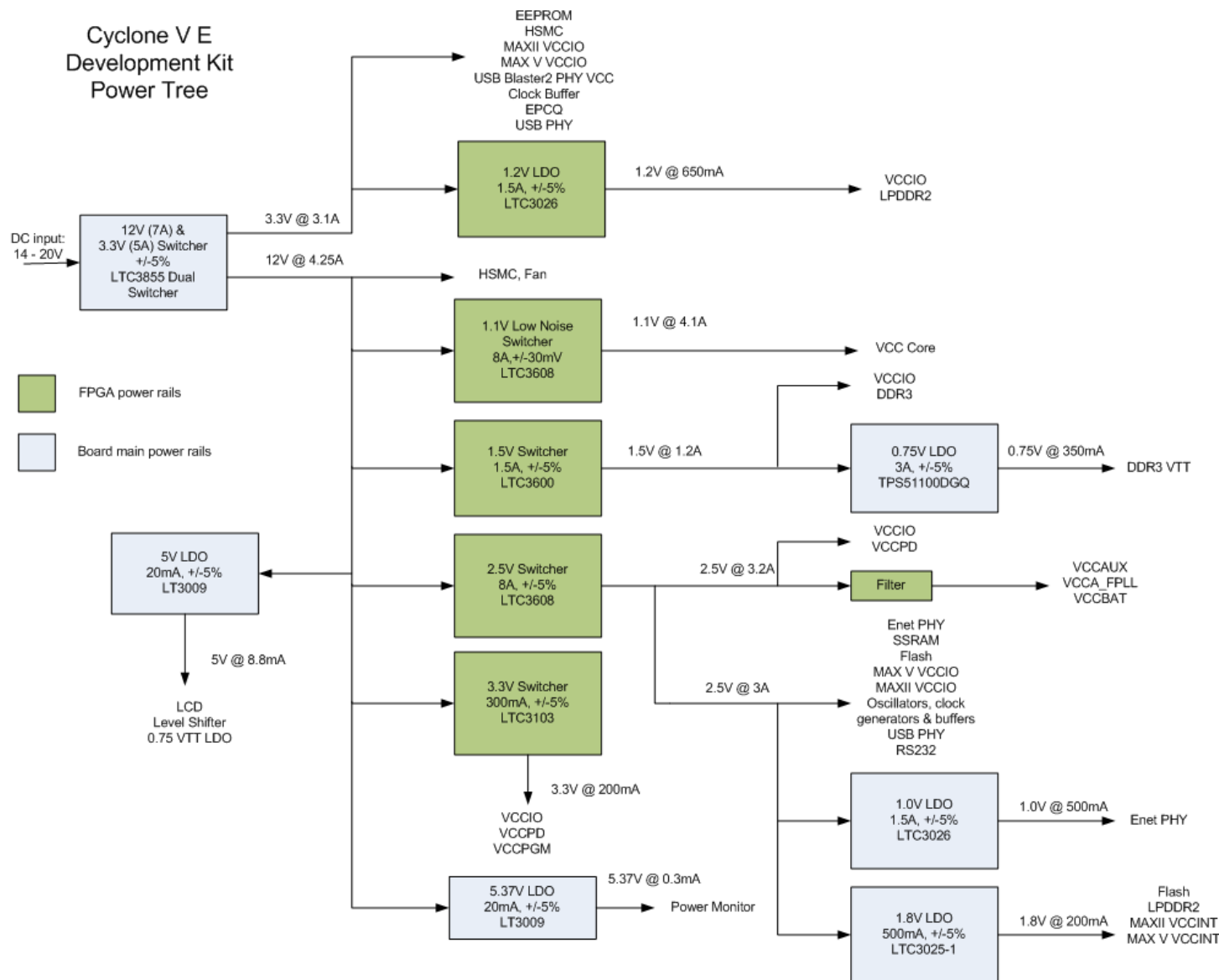
Date: Tuesday, November 27, 2012 Sheet 1 of 29

# FPGA Package Top View



Altera Worldwide Service, Plot 6, Bayan Lepas Technoplex, Penang, Malaysia			
Title		<b>Cyclone V E Development Kit Board</b>	
Size	Document Number	Rev	
B	150-0321002- B1 (6XX-44161R)	B1	
Date:	Thursday, November 15, 2012	Sheet	2 of 29

# Cyclone V E Development Kit Power Tree



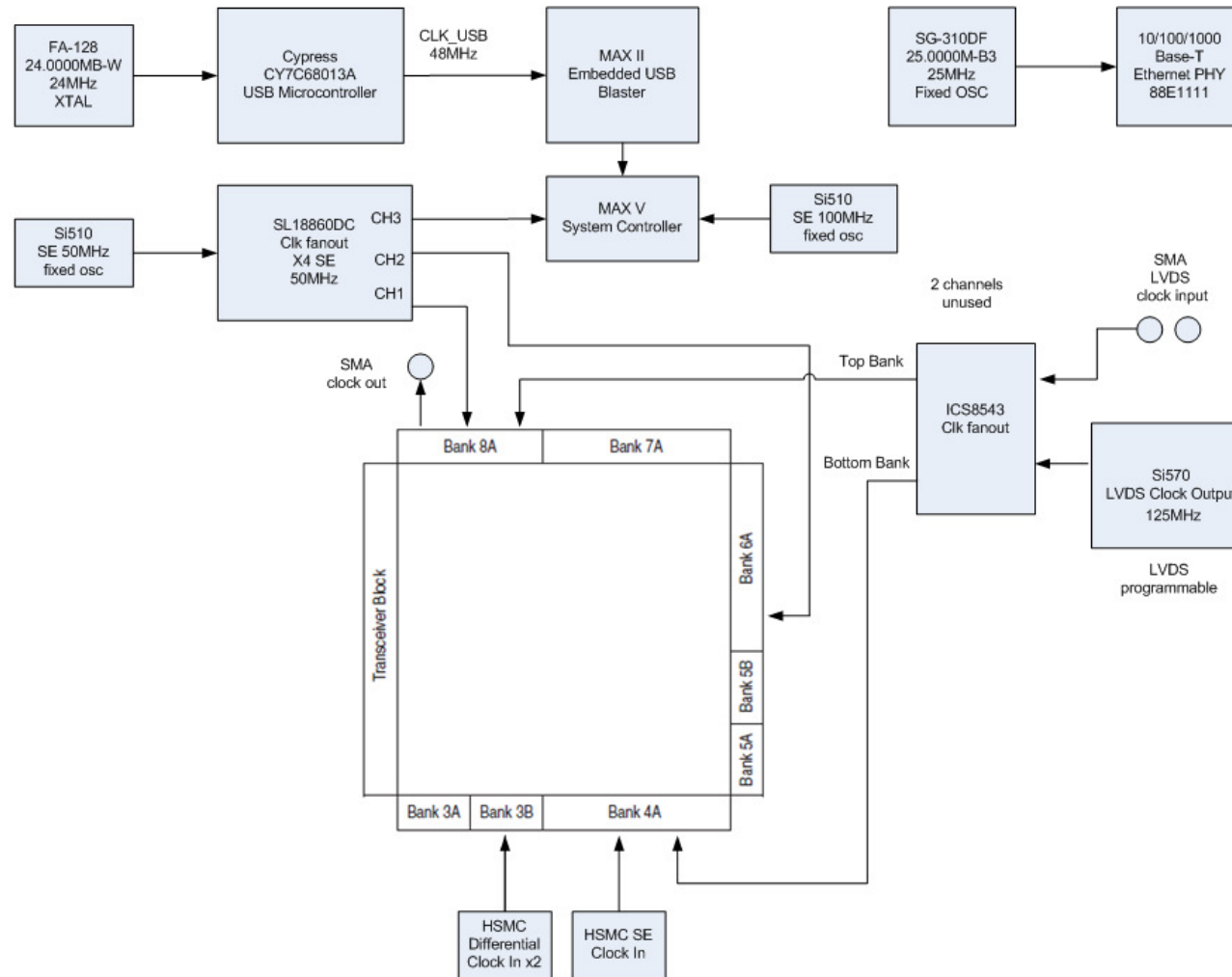
Altera Worldwide Service, Plot 6, Bayan Lepas Technoplex, Penang, Malaysia

Title **Cyclone V E Development Kit Board**

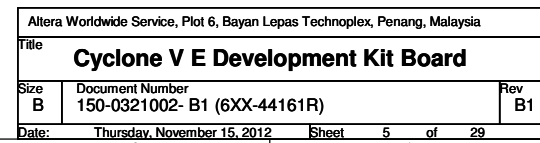
Size B Document Number 150-0321002- B1 (6XX-44161R) Rev B1

Date: Thursday, November 15, 2012 Sheet 3 of 29

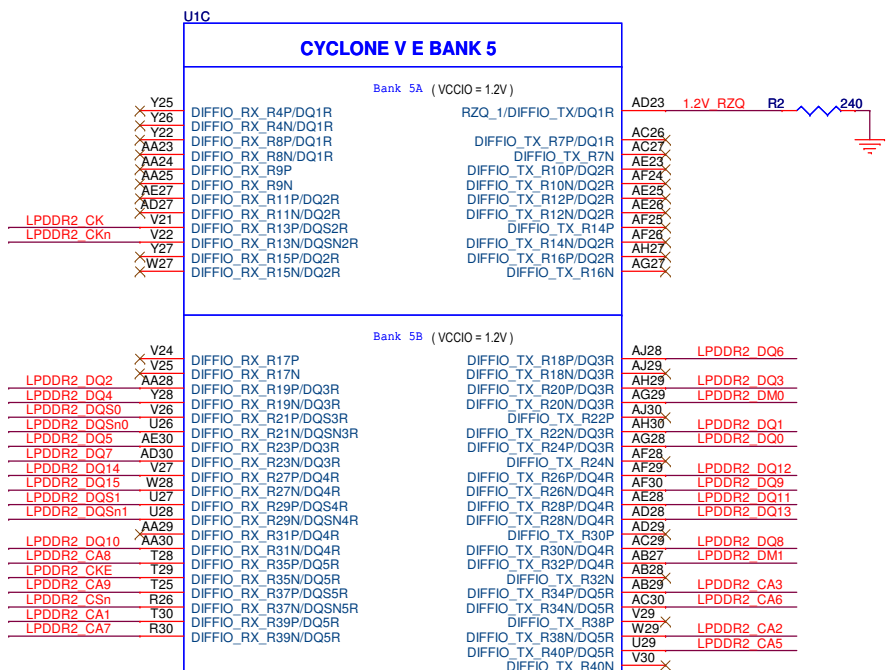
# Cyclone V E Development Kit Clock Tree



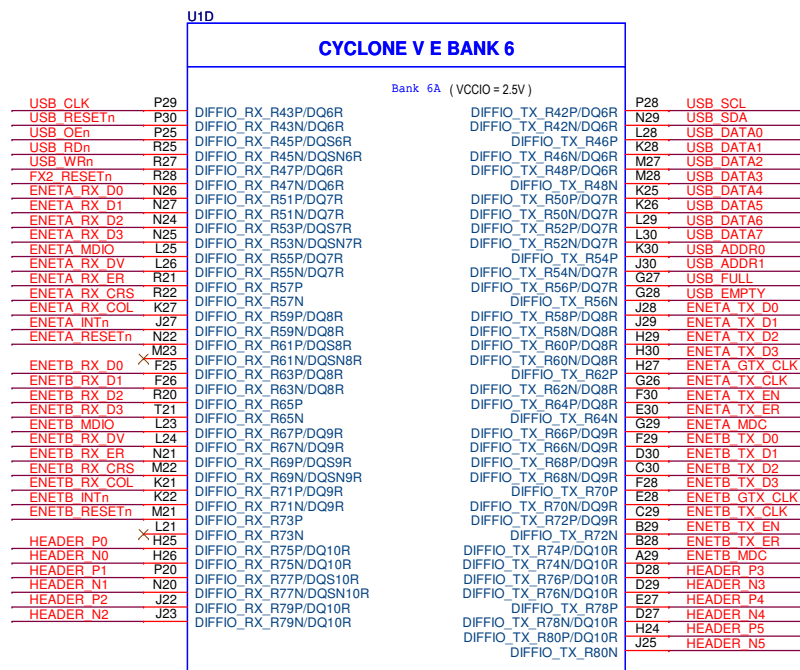
Altera Worldwide Service, Plot 6, Bayan Lepas Technoplex, Penang, Malaysia			
Title <b>Cyclone V E Development Kit Board</b>			
Size <b>B</b>	Document Number <b>150-0321002- B1 (6XX-44161R)</b>	Rev <b>B1</b>	
Date: <b>Thursday, November 15, 2012</b>	Sheet <b>4</b>	of <b>29</b>	



# Cyclone V E Bank 5 and Bank 6

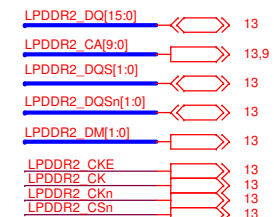


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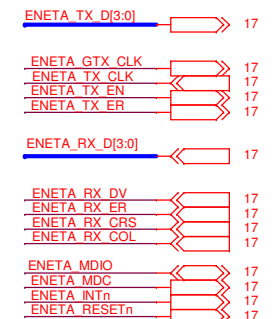


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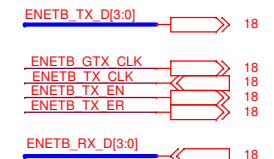
## LPDDR2 Interface



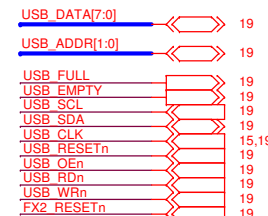
## Ethernet PHY A Interface



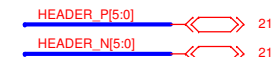
## Ethernet PHY B Interface



## USB Blaster II Interface



## DEBUG HEADER INTERFACE



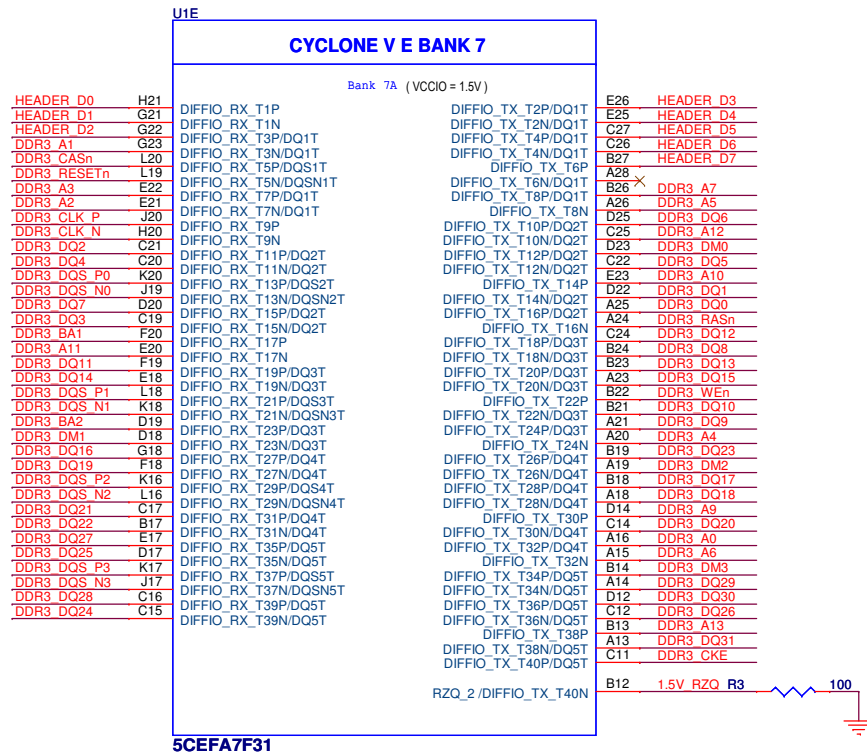
Altera Worldwide Service, Plot 6, Bayan Lepas Technoplex, Penang, Malaysia

Title **Cyclone V E Development Kit Board**

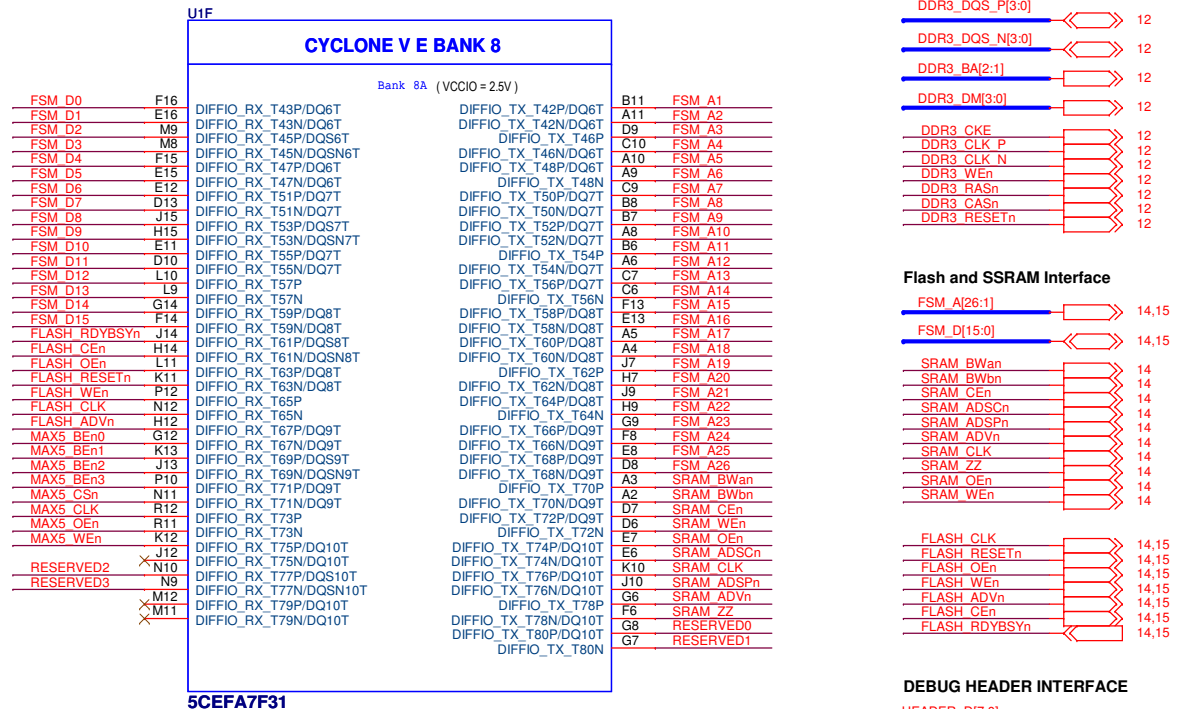
Size B Document Number 150-0321002- B1 (6XX-44161R) Rev B1

Date: Thursday, November 15, 2012 Sheet 6 of 29

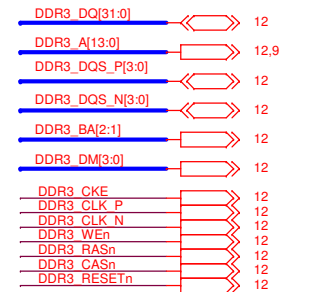
# Cyclone V E Bank 7 and Bank 8



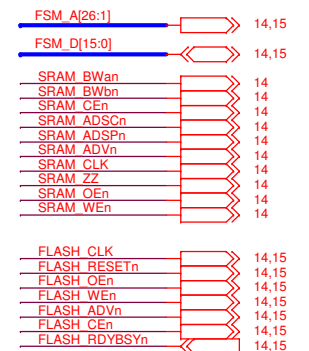
5CEFA7F31



## DDR3 Interface



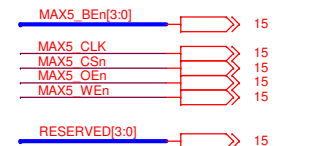
## Flash and SSRAM Interface

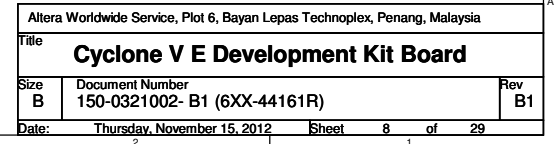


## DEBUG HEADER INTERFACE

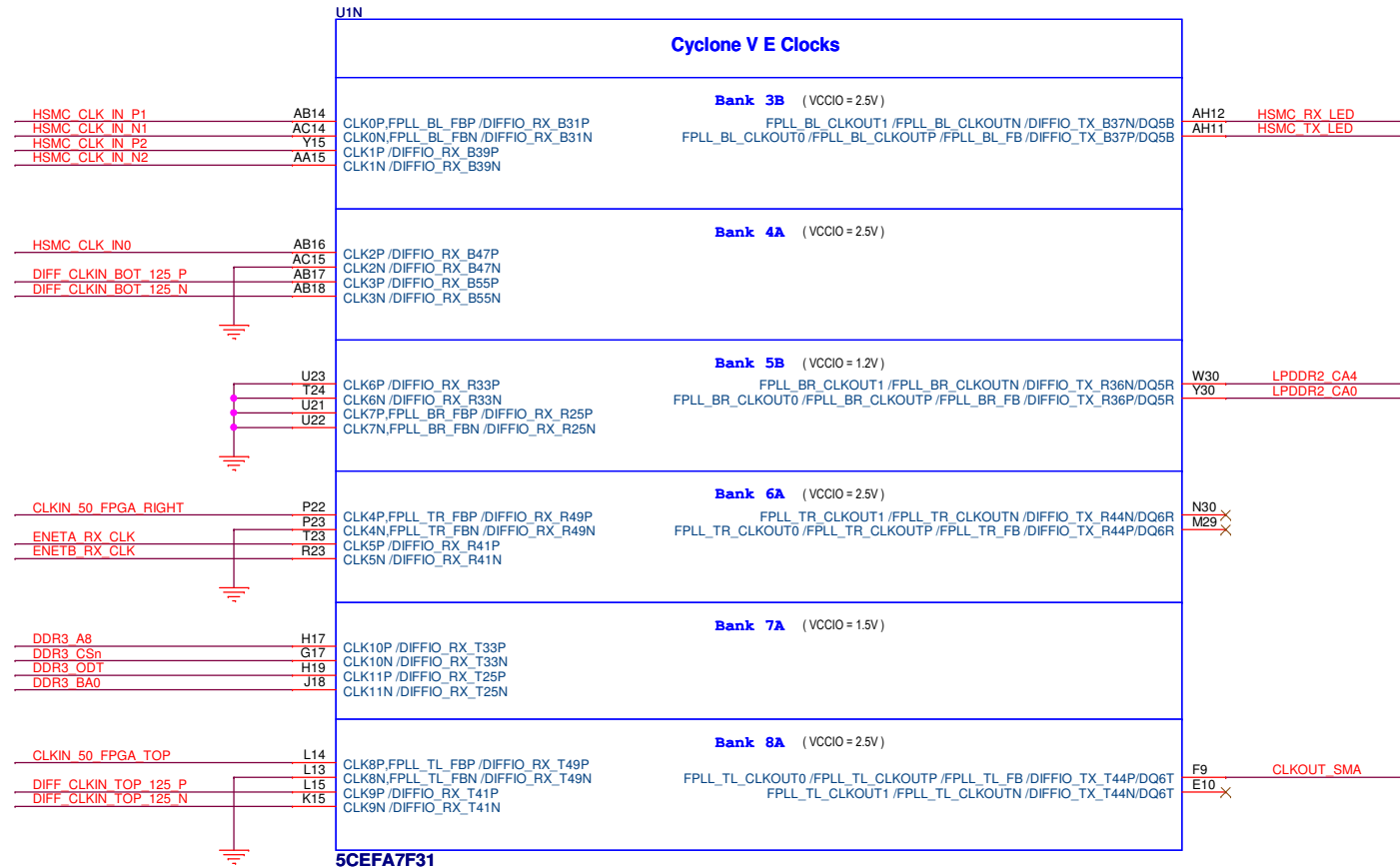


## MAX V System Controller Interface

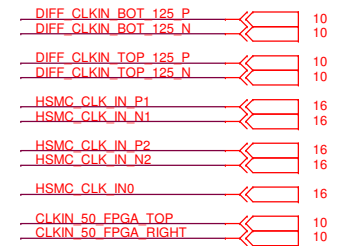




# Cyclone V E Clocks



## PLL INTERFACE



## HSMC LED INTERFACE



## DDR3 INTERFACE



## LPDDR2 INTERFACE

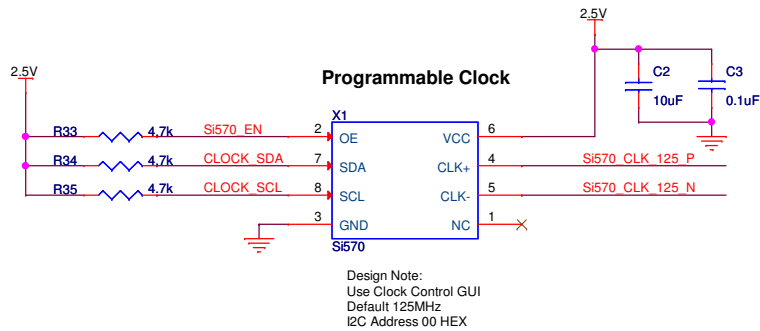


## ETHERNET INTERFACE

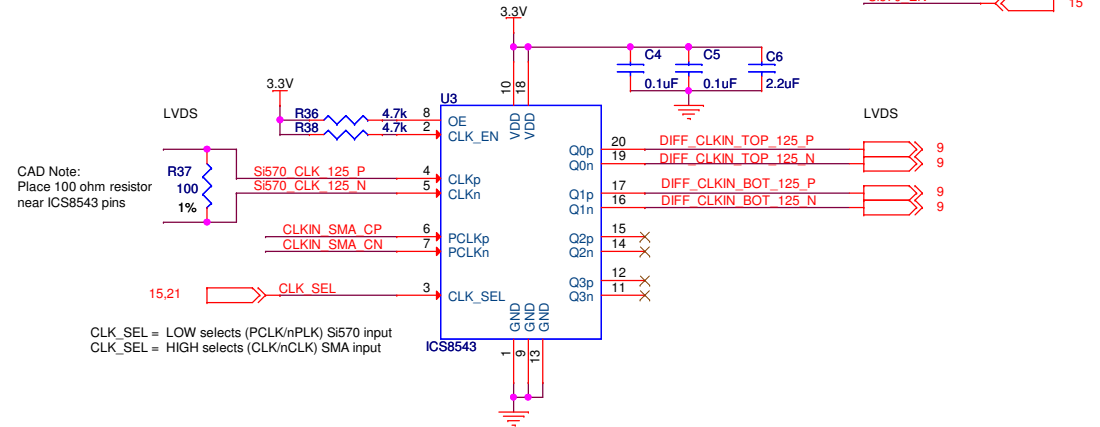


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Title		Cyclone V E Development Kit Board	
Size	Document Number	Rev	
B	150-0321002- B1 (6XX-44161R)	B1	
Date:	Thursday, November 15, 2012	Sheet	9 of 29

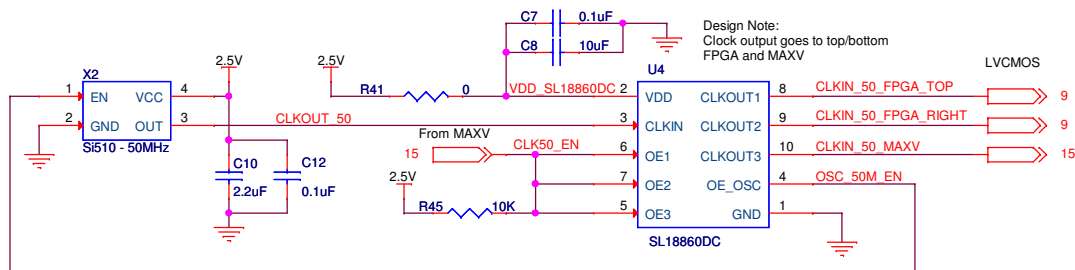
# PLL



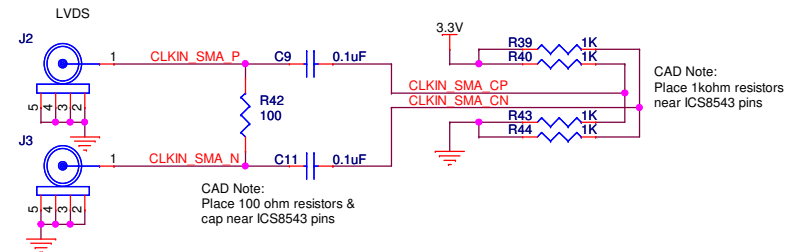
## Differential Clock Distribution to Top, Bottom & Right Banks



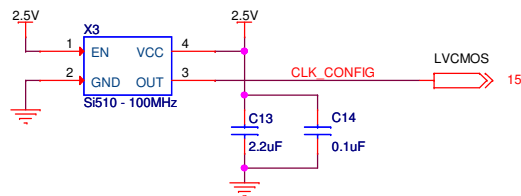
## 50MHz LVCMOS Clocks for FPGA and MAXV



## User Clock Input



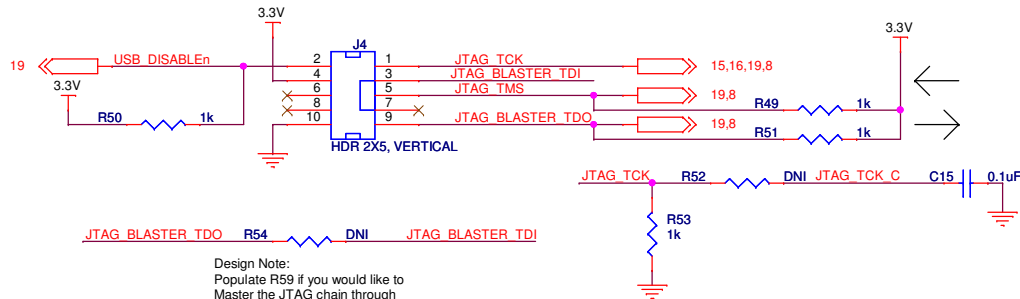
## 100MHz Configuration Clock



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Title		<b>Cyclone V E Development Kit Board</b>	
Size	Document Number	Rev	
B	150-0321002- B1 (6XX-44161R)	B1	
Date:	Thursday, November 15, 2012	Sheet	10 of 29

# JTAG

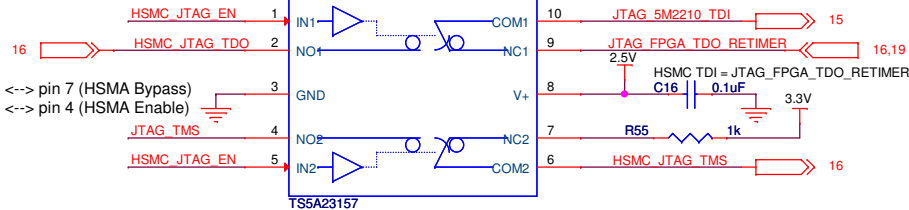
## USB Blaster Programming Header (uses JTAG mode only)



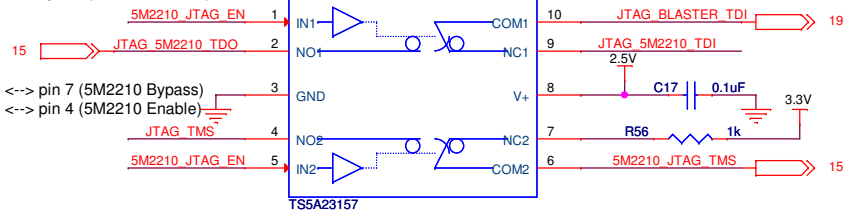
## TS5A23157 Switch Functions

When Pins 1 & 5 are:  
 LOW -> NC to/from COM = ON and NO to/from COM = OFF  
 HIGH -> NC to/from COM = OFF and NO to/from COM = ON

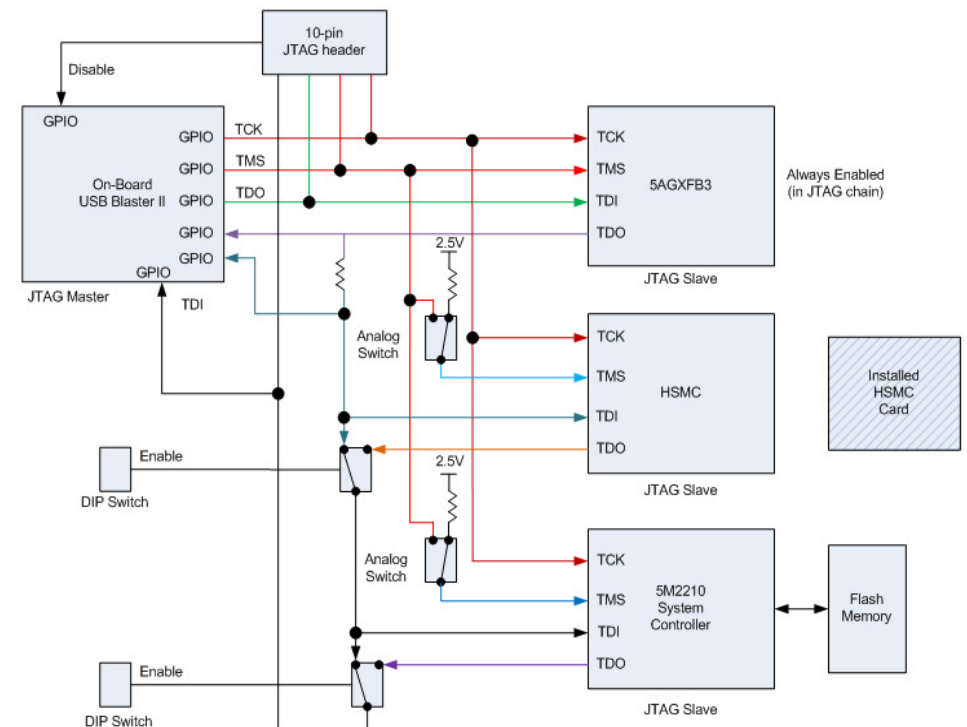
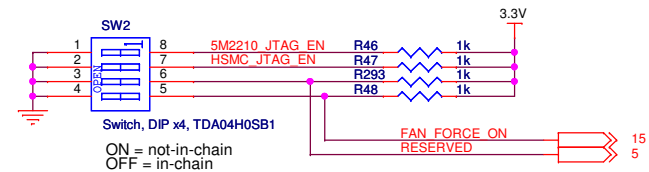
Logic 0 = pin 10 <-> pin 9 (HSMC Bypass)  
 Logic 1 = pin 10 <-> pin 2 (HSMC Enable)



Logic 0 = pin 10 <-> pin 9 (5M2210 Bypass)  
 Logic 1 = pin 10 <-> pin 2 (5M2210 Enable)



## JTAG Chain Control



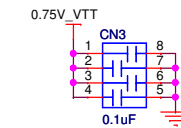
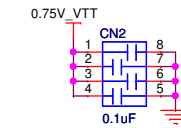
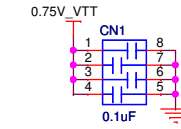
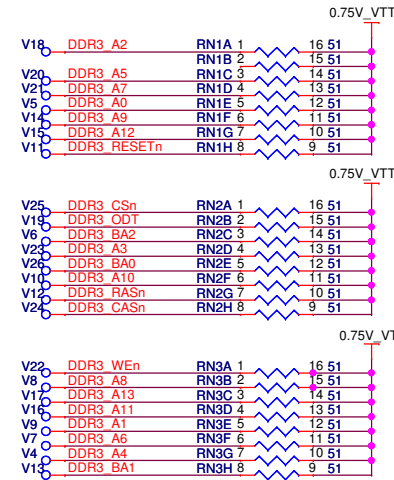
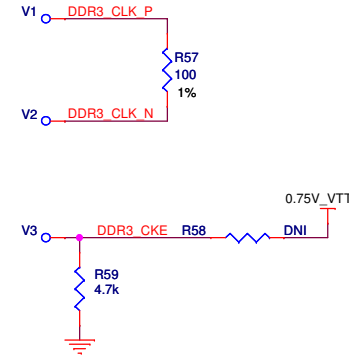
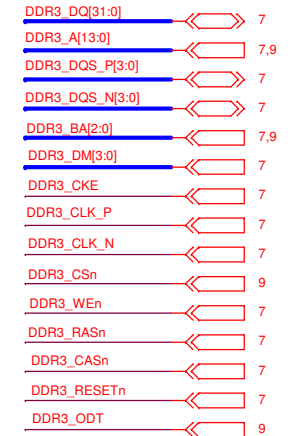
Altera Worldwide Service, Plot 6, Bayan Lepas Technoplex, Penang, Malaysia			
Title		Cyclone V E Development Kit Board	
Size	Document Number	Rev	
B	150-0321002- B1 (6XX-44161R)	B1	
Date:	Thursday, November 15, 2012	Sheet	11 of 29

# DDR3 SDRAM x32

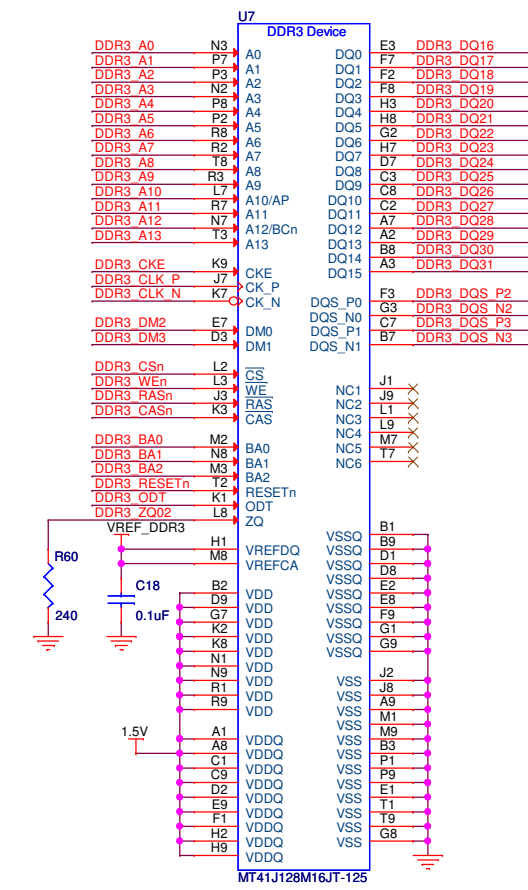
DDR3 SDRAM B (16M X 16 X 8)

DDR3 SDRAM A (16M X 16 X 8)

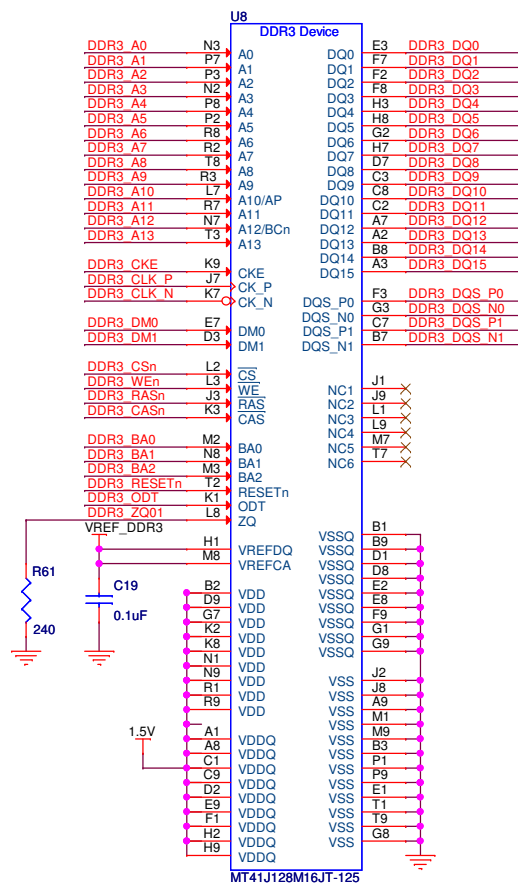
## FPGA Interface



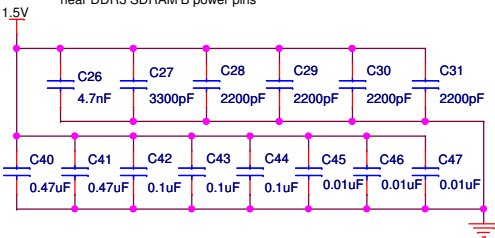
CAD Note:  
Use tree-topology for termination signals  
Use star via to branch out address/  
command/control signals from FPGA  
to memory devices and termination resistors



CAD Note:  
Place decoupling caps  
near DDR3 SDRAM A power pins

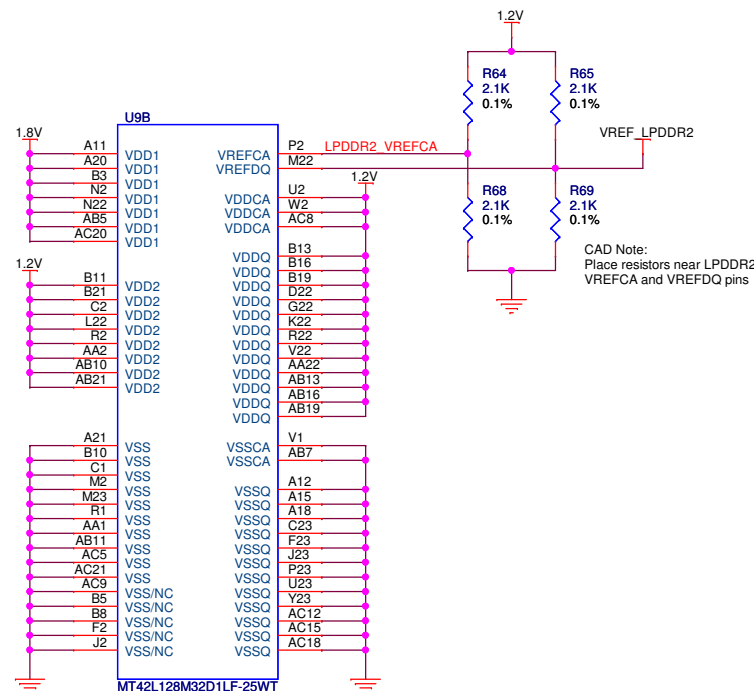
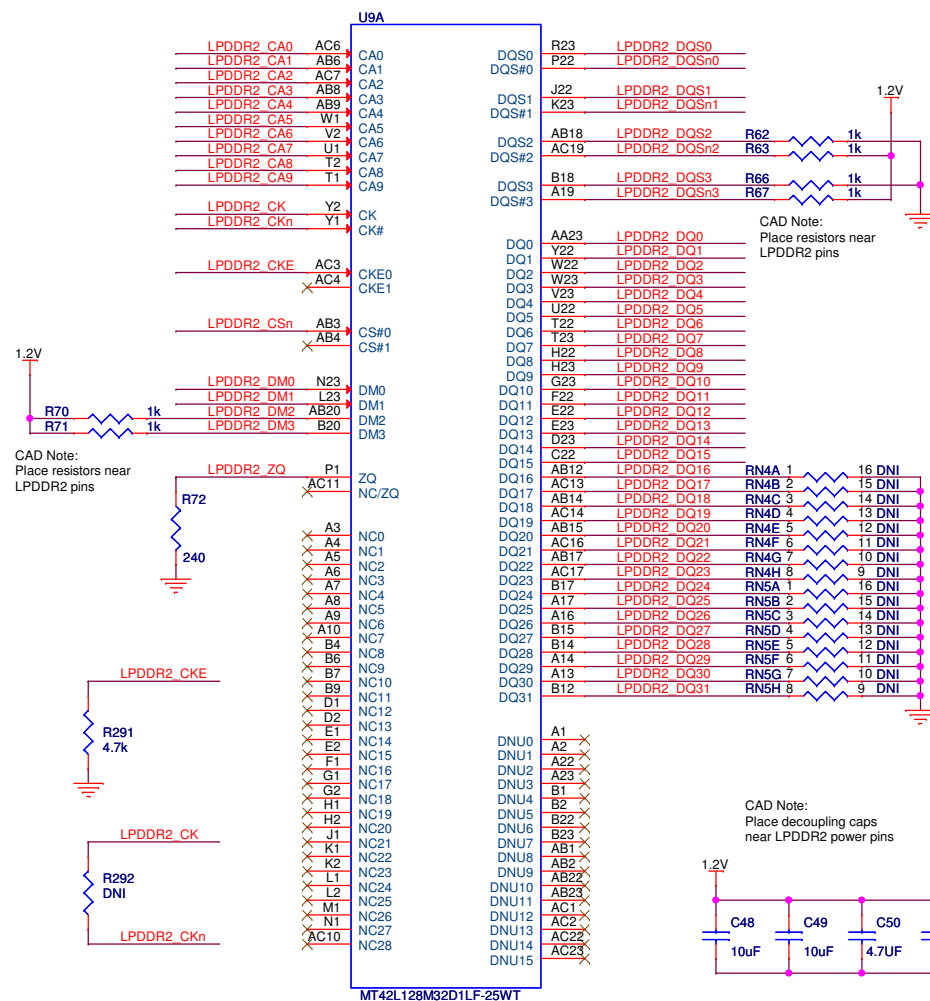


CAD Note:  
Place decoupling caps  
near DDR3 SDRAM B power pins

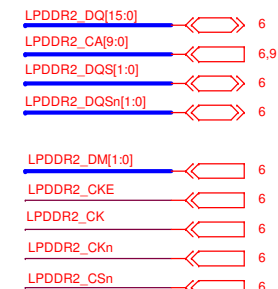


**LPDDR2 SDRAM x16**

LPDDR2 SDRAM (16M X 32 X 8 banks x 1 die)



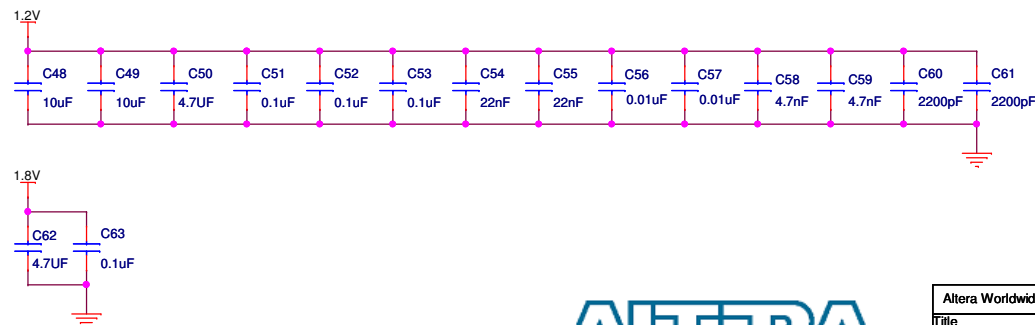
## FPGA Interface



Design Note:  
Only x16 configuration is used on the x32 device

CAD Note:  
Place decoupling caps  
near LPDDR2 power pins

**Design Note:**  
Pin compatible between MT42L128M32D1LF-25 and MT42L64M32D1KQ  
Pins AC9, B5, B8, F2 and J2 can be VSS/NC

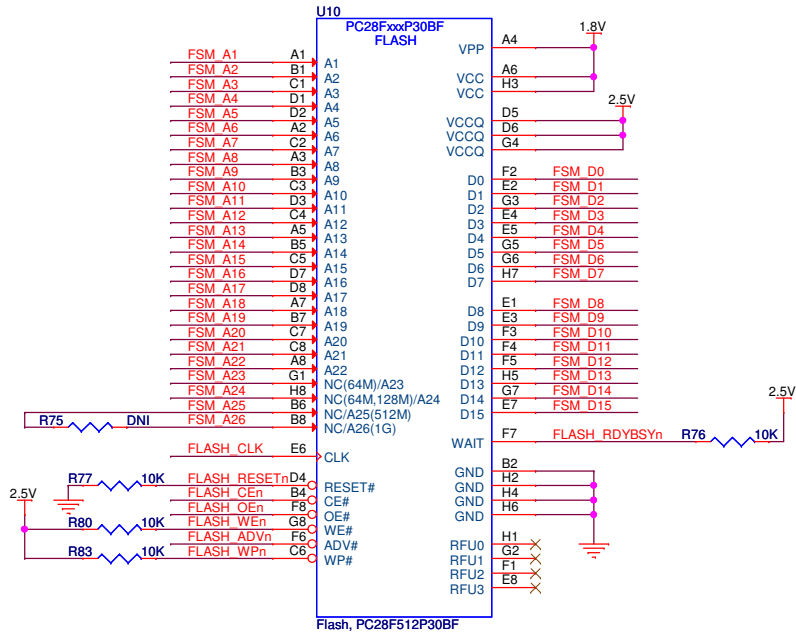


# Flash/SRAM/EEPROM

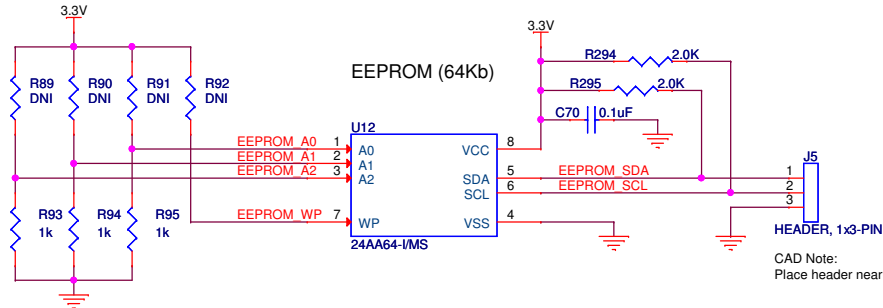
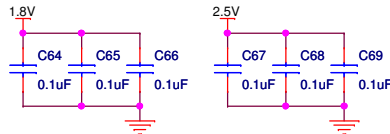
FLASH 512Mb (32M X 16)

SRAM (1M X 18)

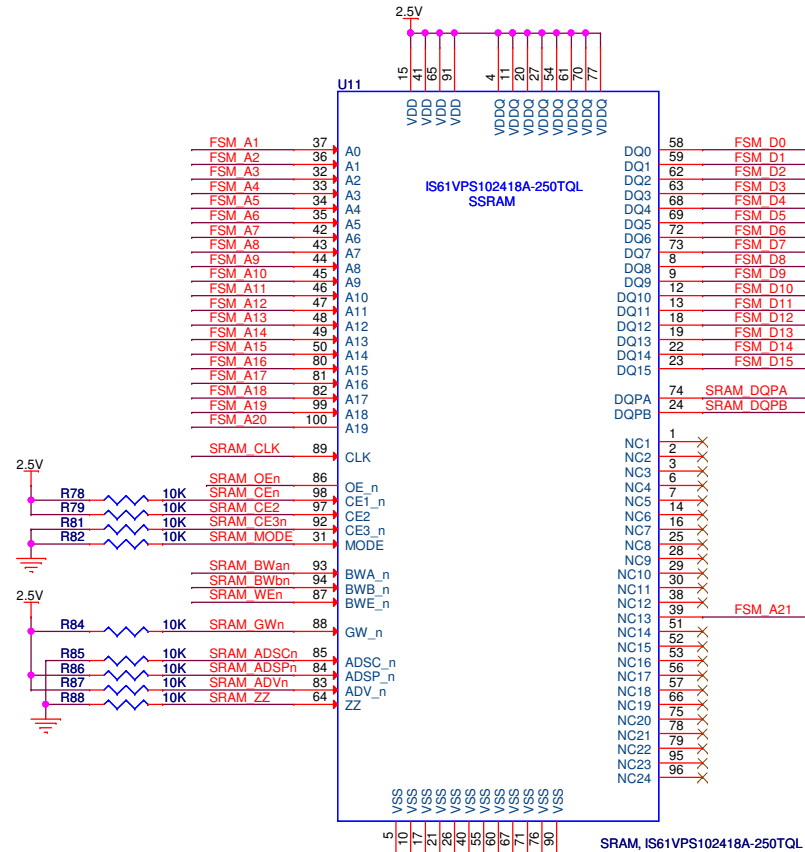
FPGA and MAX V Interface



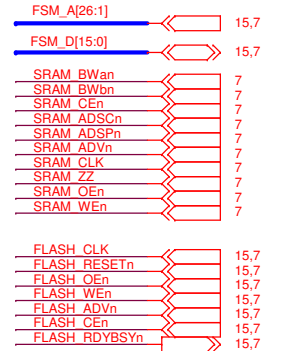
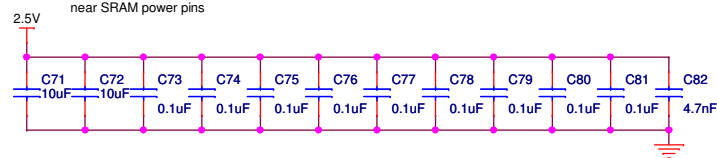
CAD Note:  
Place decoupling caps  
near Flash power pins



CAD Note:  
Place header near EEPROM device

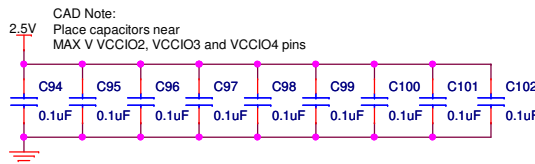
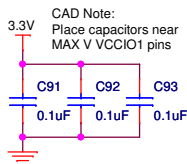
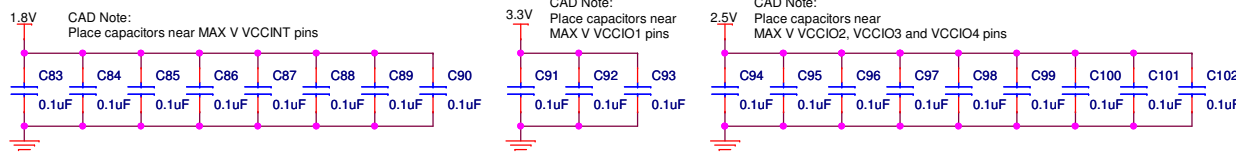
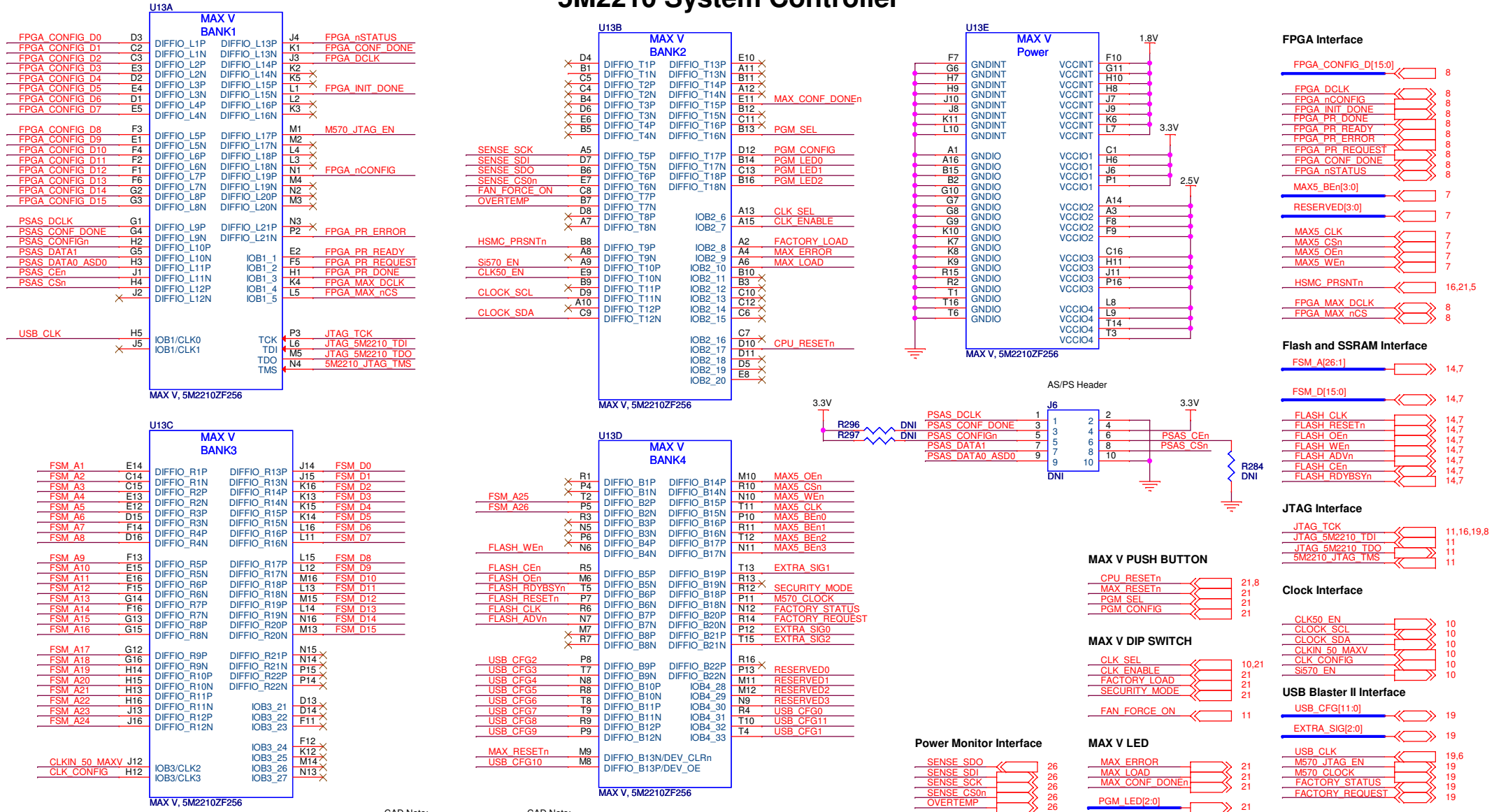


CAD Note:  
Place decoupling caps  
near SRAM power pins

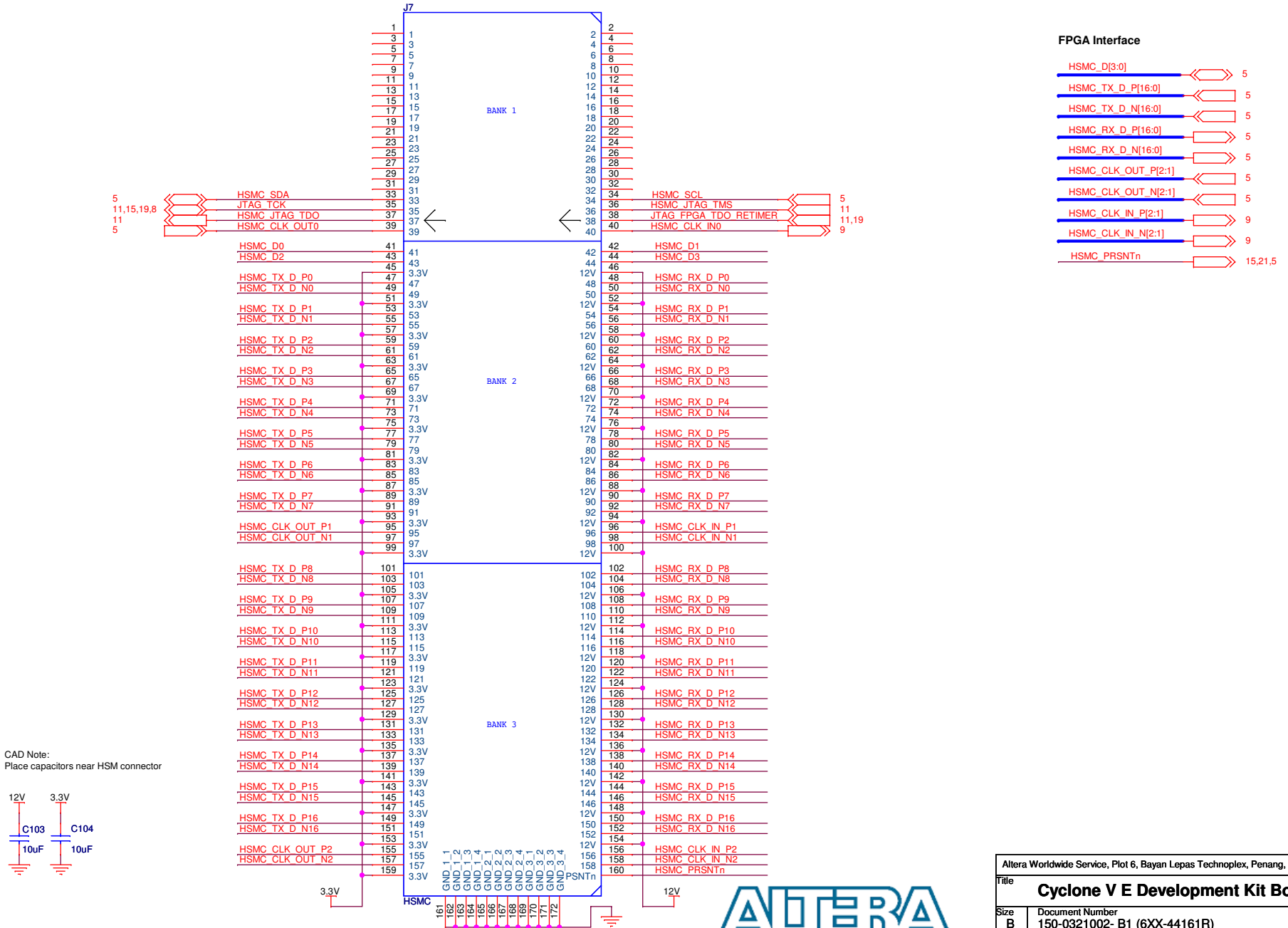


Altera Worldwide Service, Plot 6, Bayan Lepas Technoplex, Penang, Malaysia			
Title Cyclone V E Development Kit Board			
Size B	Document Number 150-0321002- B1 (6XX-44161R)	Rev B1	
Date: Thursday, November 15, 2012	Sheet 14	of 29	

# 5M2210 System Controller



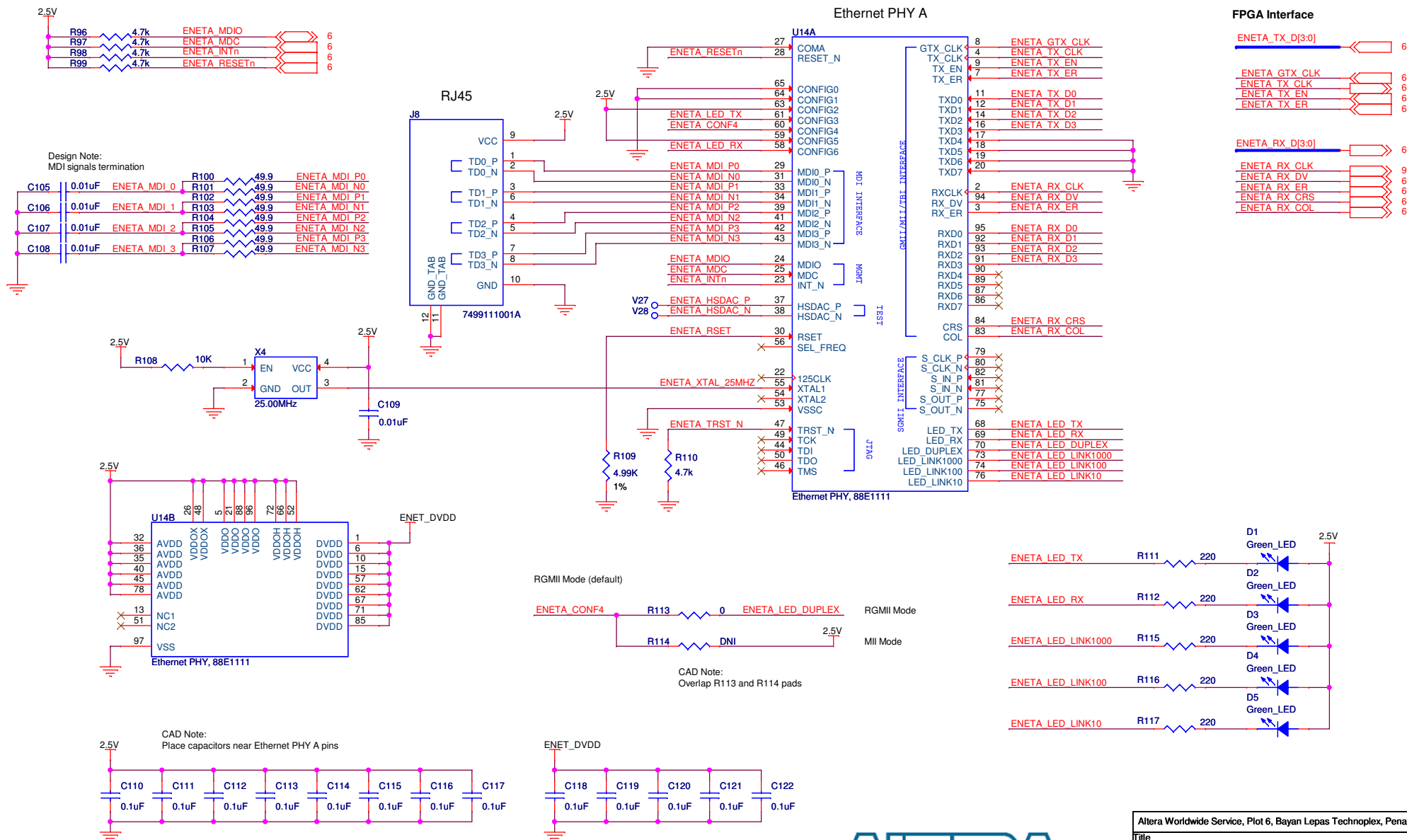
# HSMC Port



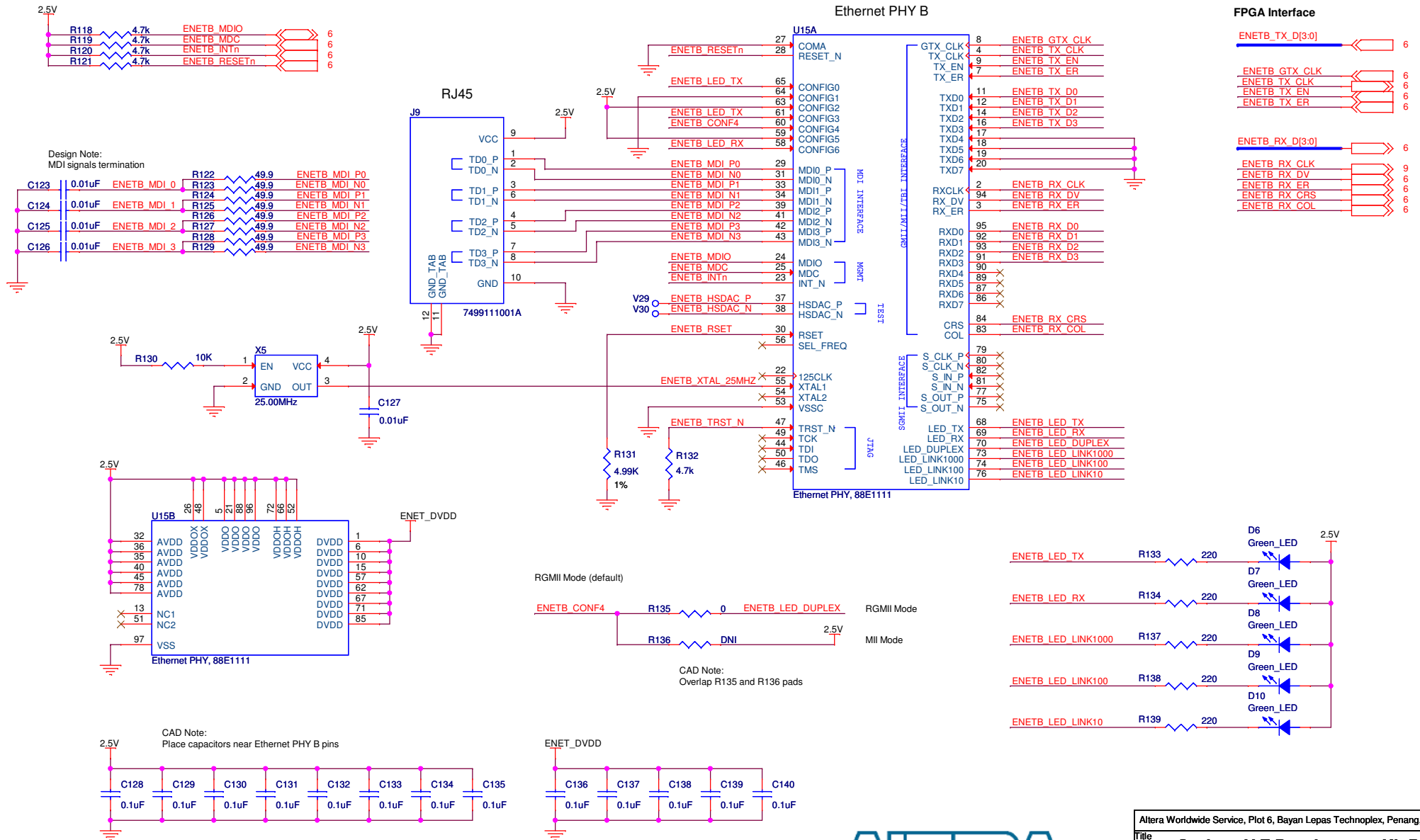
ALTERA

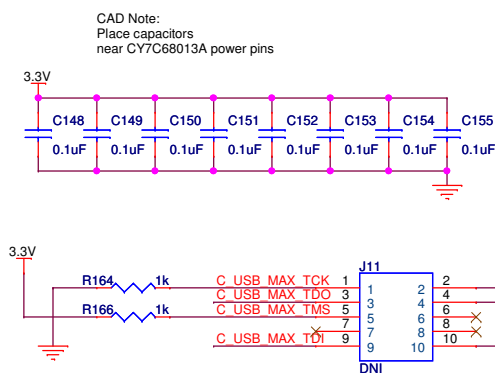
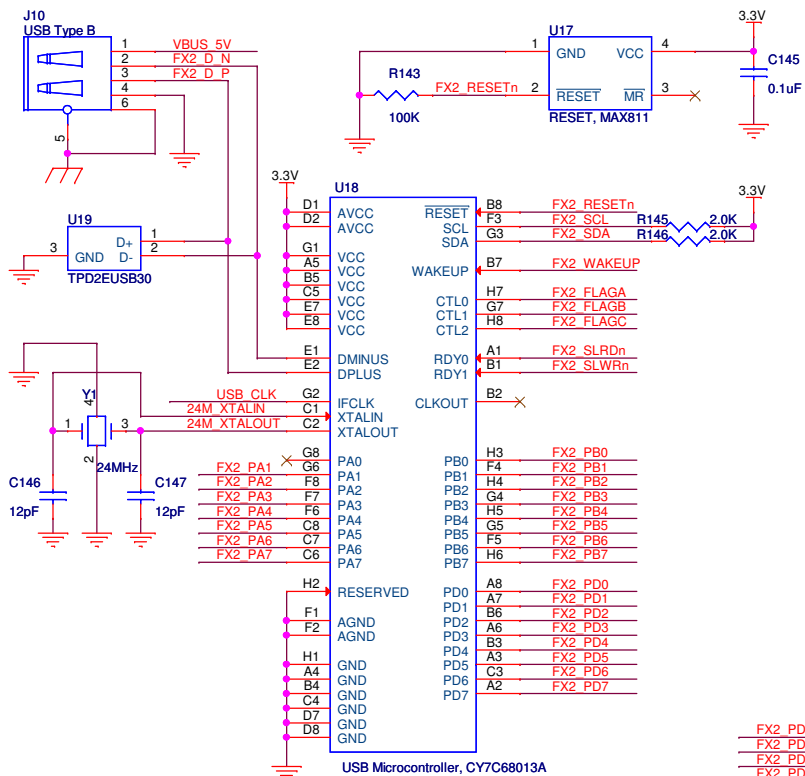
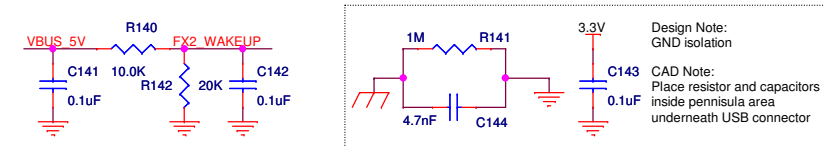
Altera Worldwide Service, Plot 6, Bayan Lepas Technoplex, Penang, Malaysia			
Title Cyclone V E Development Kit Board			
Size B	Document Number 150-0321002- B1 (6XX-44161R)	Rev B1	
Date: Thursday, November 15, 2012	Sheet 16	of 29	

## 10/100/1000 Ethernet A



# 10/100/1000 Ethernet B

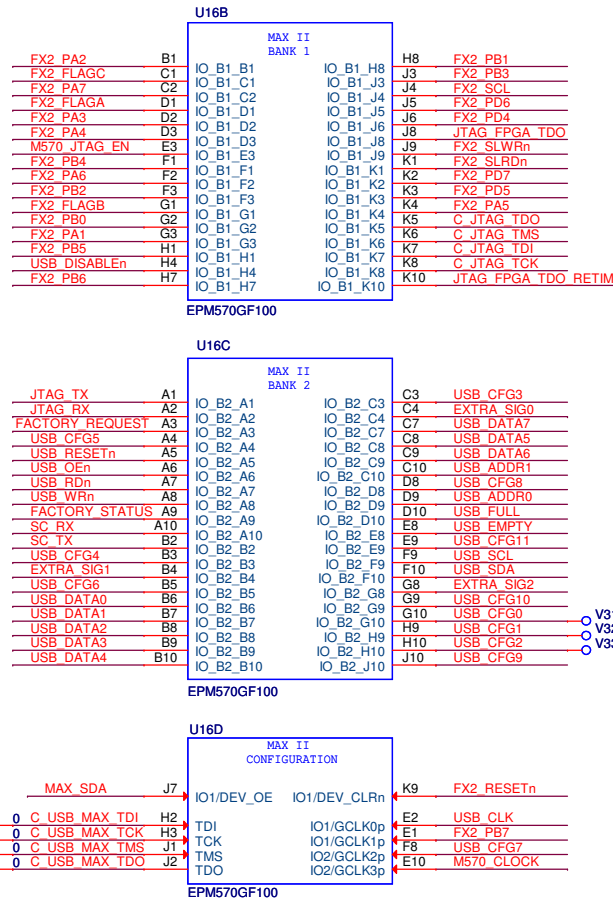




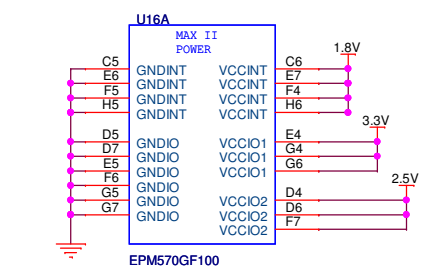
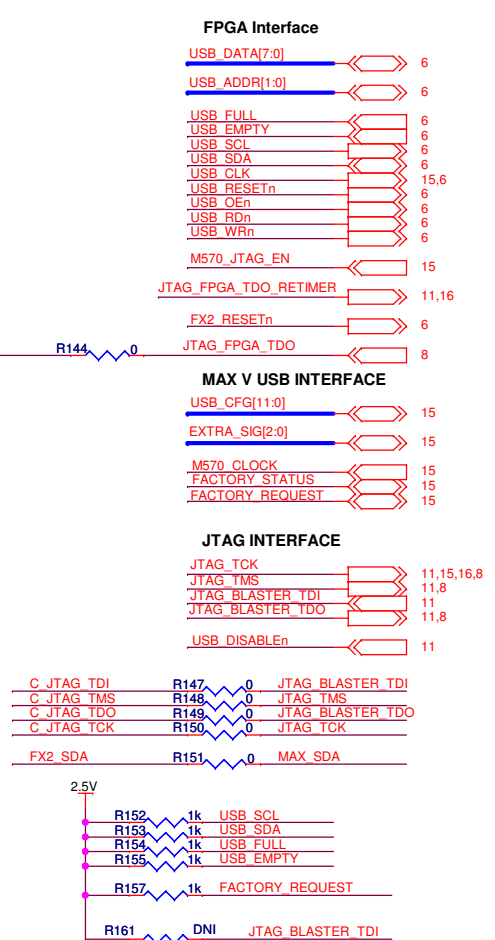
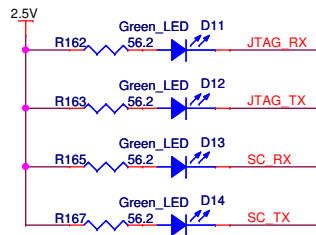
Design Note:  
GND isolation

CAD Note:  
Place resistor and capacitors  
inside peninsula area  
underneath USB connector

## USB Blaster II

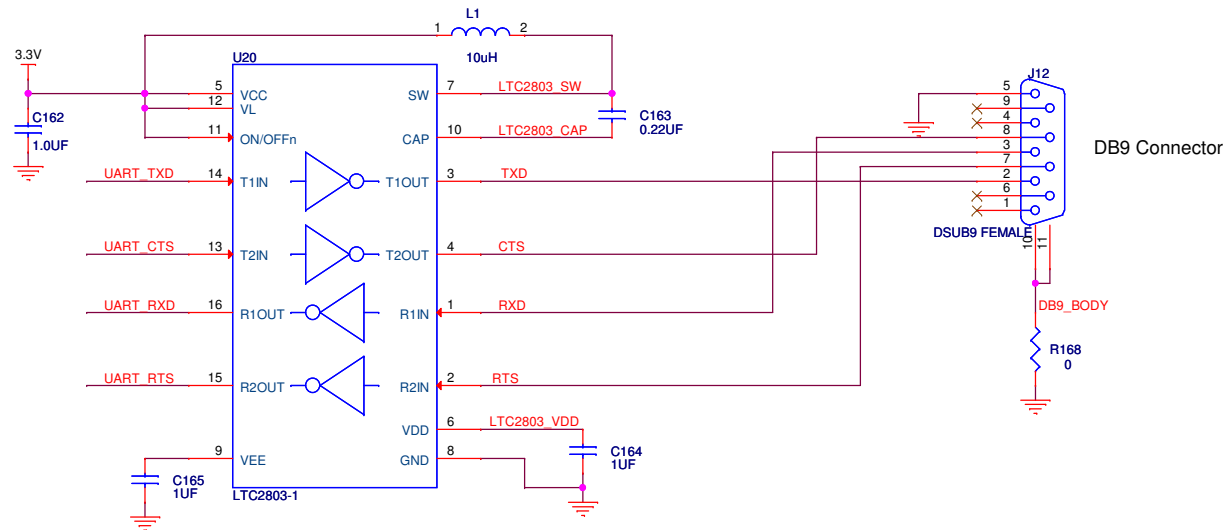


CAD Note:  
Place capacitors  
near MAXII EPM570 power pins



# UART

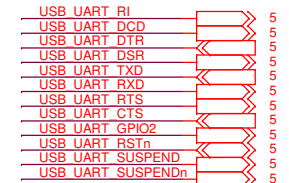
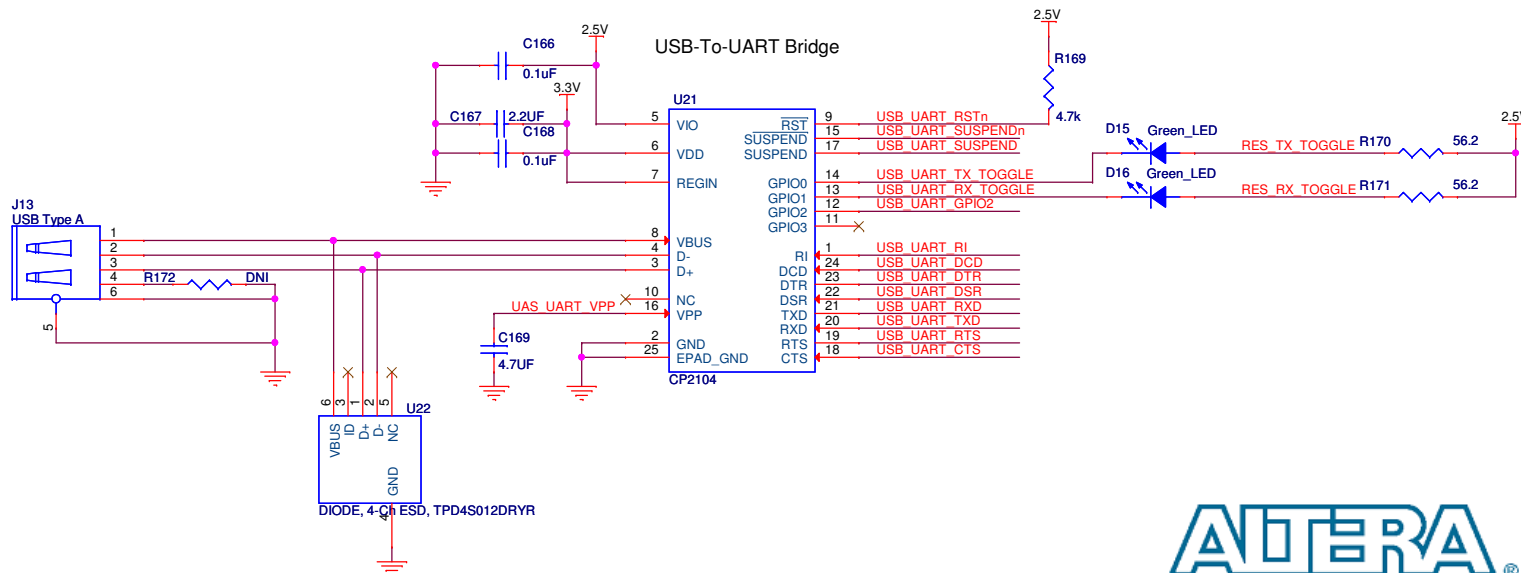
## RS-232 Transceiver



## FPGA Interface

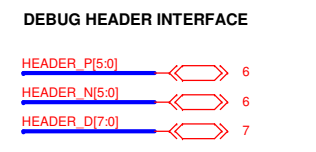
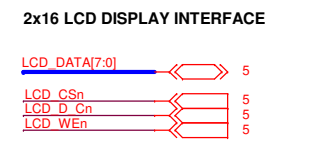
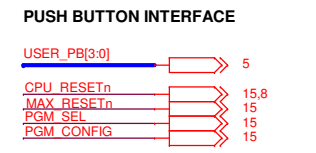
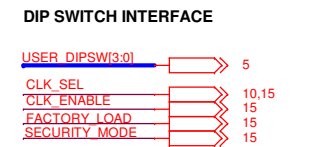
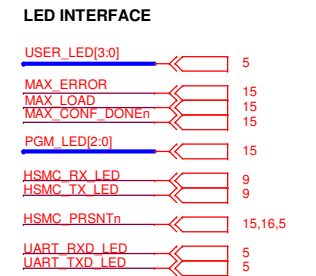
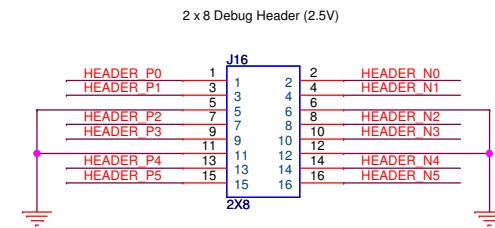
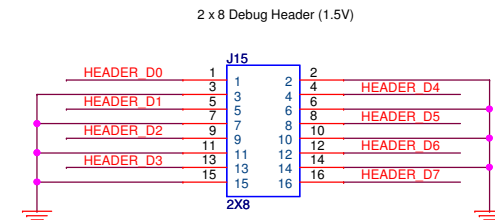
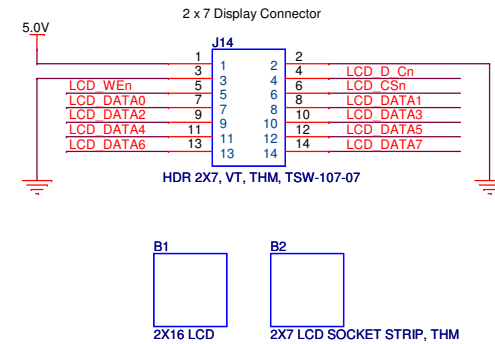
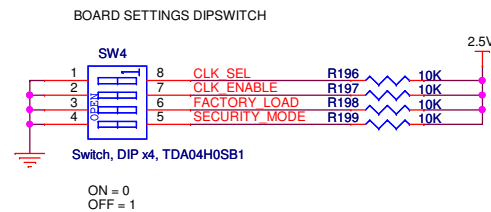
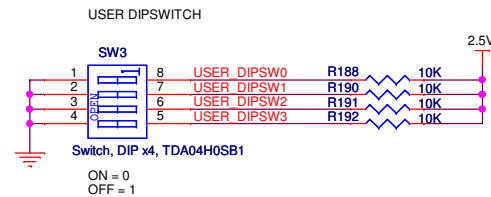
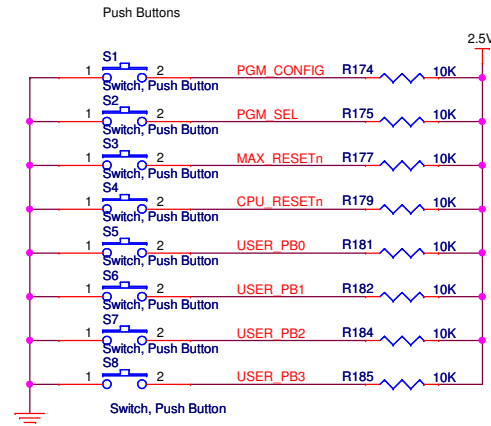
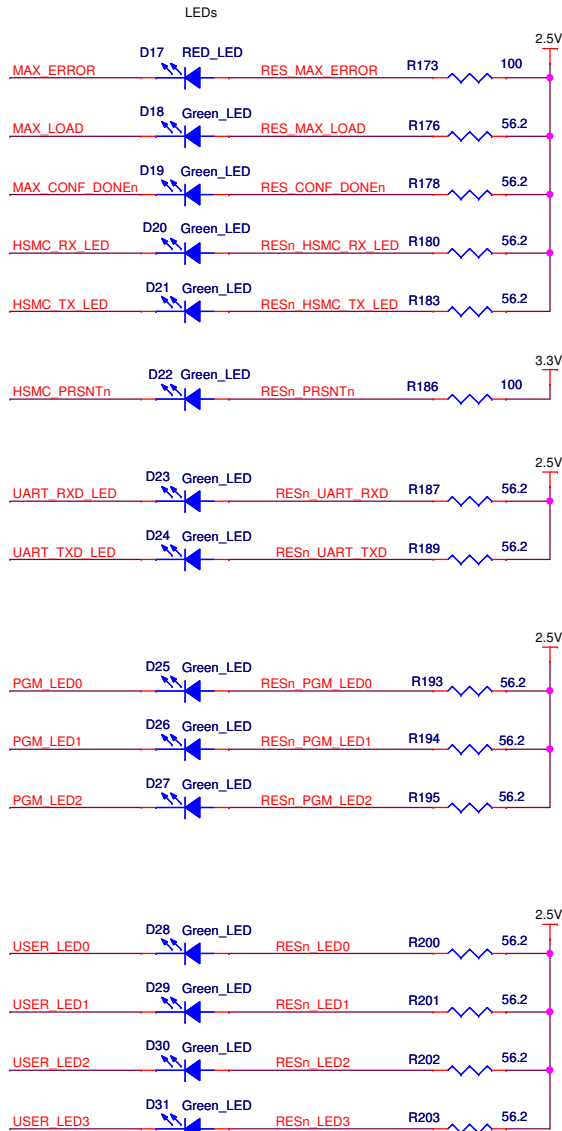


## USB-To-UART Bridge

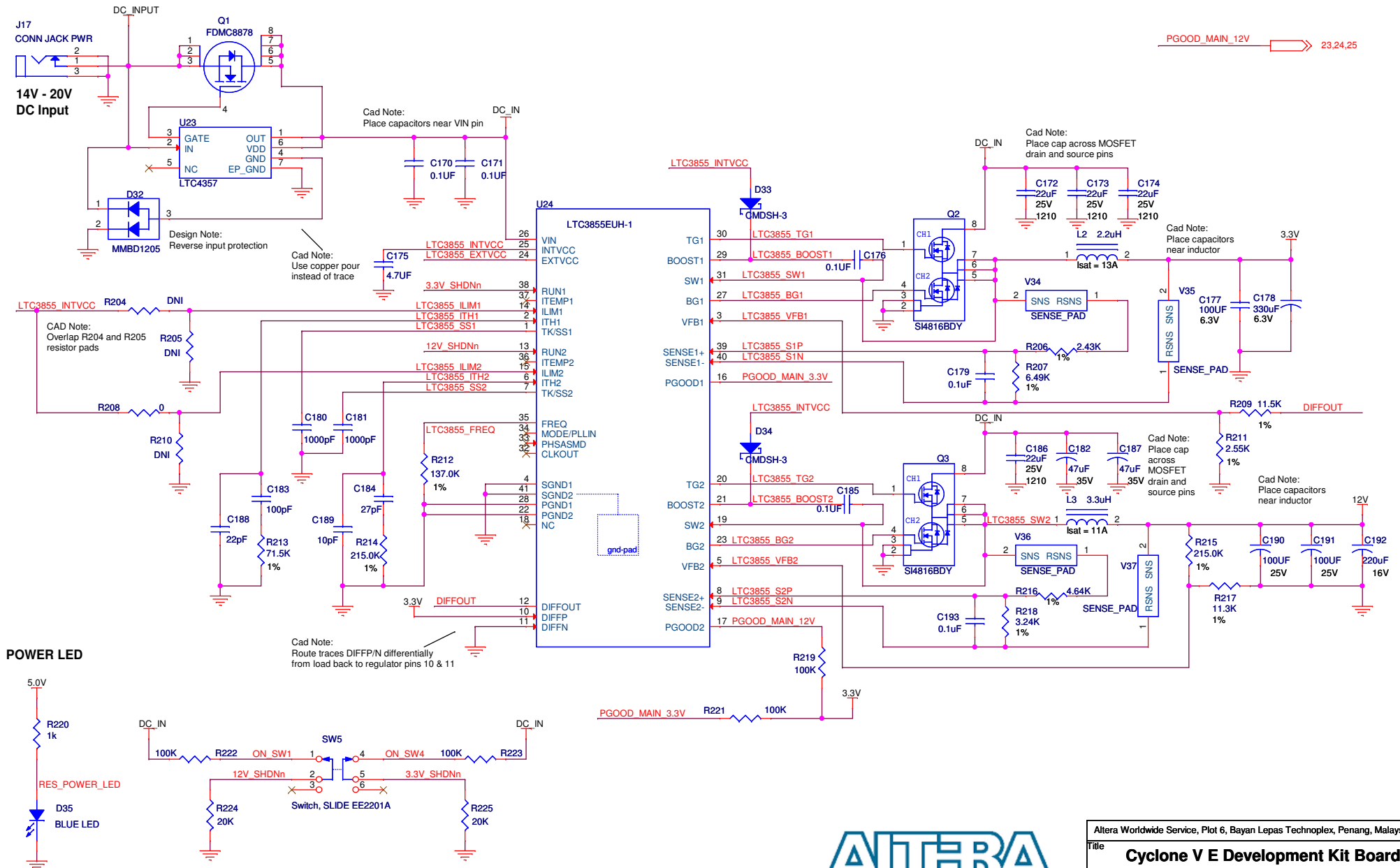


Altera Worldwide Service, Plot 6, Bayan Lepas Technoplex, Penang, Malaysia			
Title		Cyclone V E Development Kit Board	
Size	Document Number	Rev	
B	150-0321002- B1 (6XX-44161R)	B1	
Date:	Thursday, November 15, 2012	Sheet	20 of 29

# User I/O and Connector

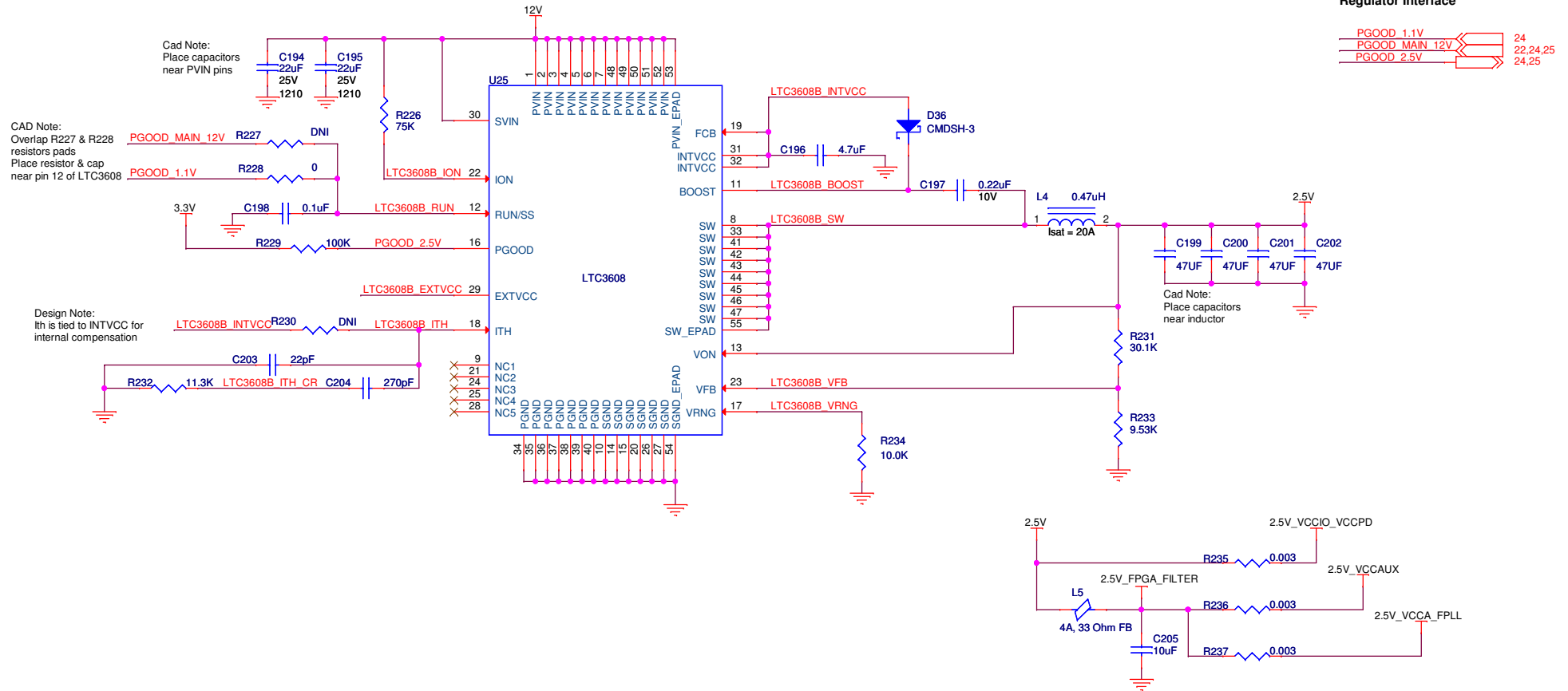


# Power 1 - DC Input & 12V, 3.3V Output

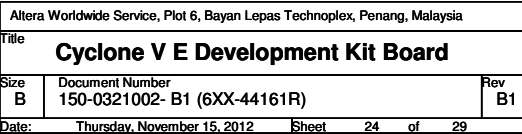


Altera Worldwide Service, Plot 6, Bayan Lepas Technoplex, Penang, Malaysia		
Title Cyclone V E Development Kit Board		
Size B	Document Number 150-0321002- B1 (6XX-44161R)	Rev B1
Date: Thursday, November 15, 2012	Sheet 22	of 29

# Power 2 - 2.5V

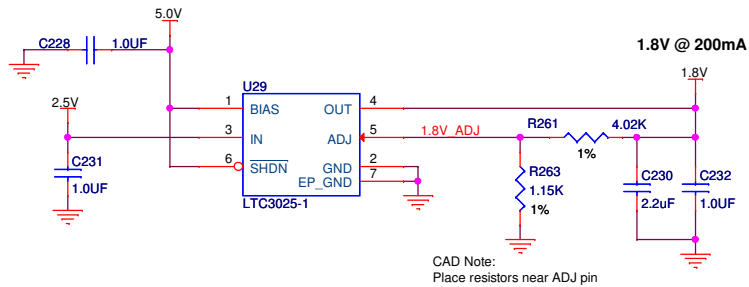


Altera Worldwide Service, Plot 6, Bayan Lepas Technoplex, Penang, Malaysia			
Title Cyclone V E Development Kit Board			
Size B	Document Number 150-0321002- B1 (6XX-44161R)	Rev B1	
Date: Thursday, November 15, 2012	Sheet 23	of 29	

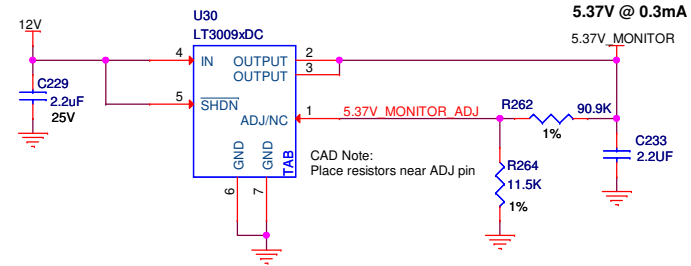


# Power 4 - Linear Regulators

Flash VCC/VPP, MAXV/MAXII VCCINT & LPDDR2 VDD1

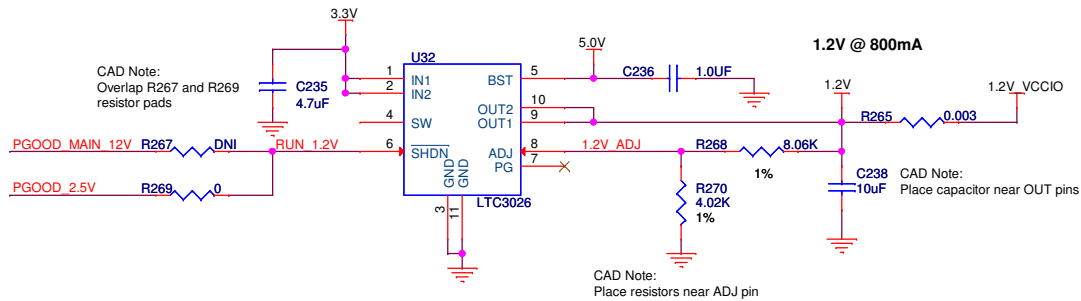


Power Monitor VIN

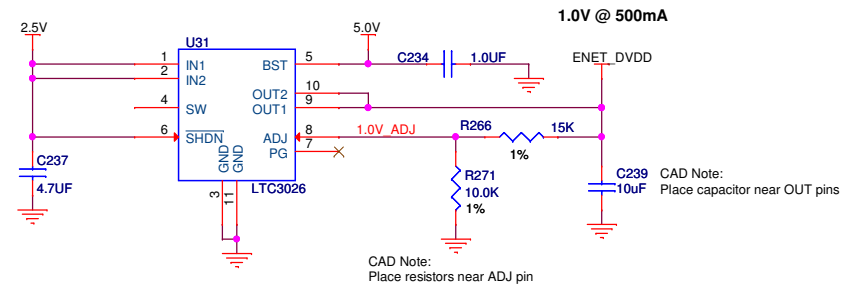


PGOOD MAIN 12V 22,23,24  
PGOOD 2.5V 23,24

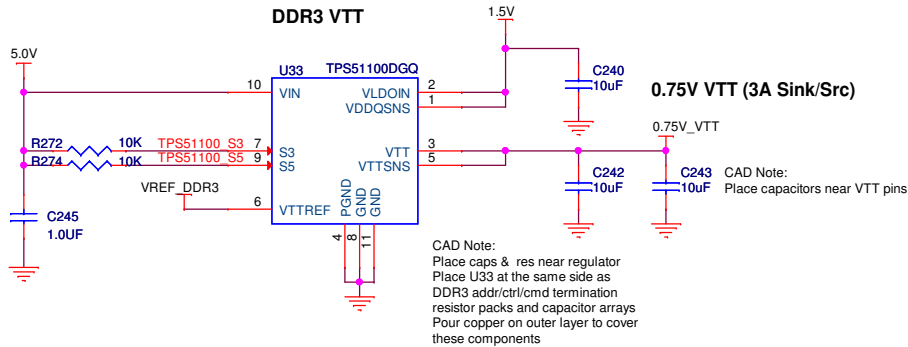
LPDDR2 VDD2, VDDQ, VDDCA, FPGA VCCIO\_1.2V



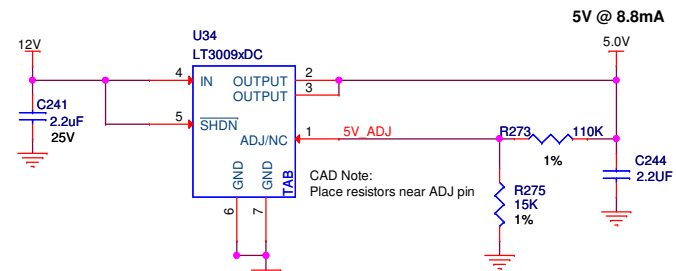
Ethernet PHY DVDD/VDDO



DDR3 VTT

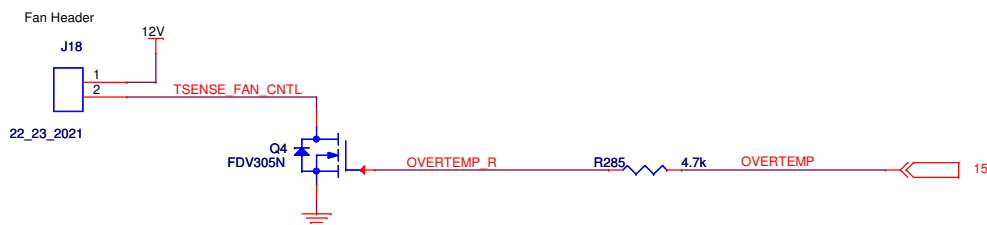
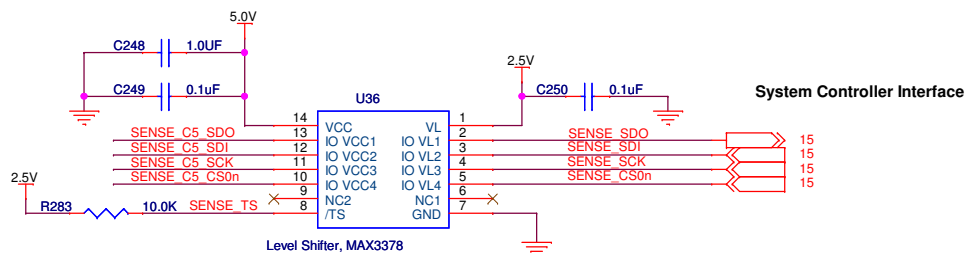
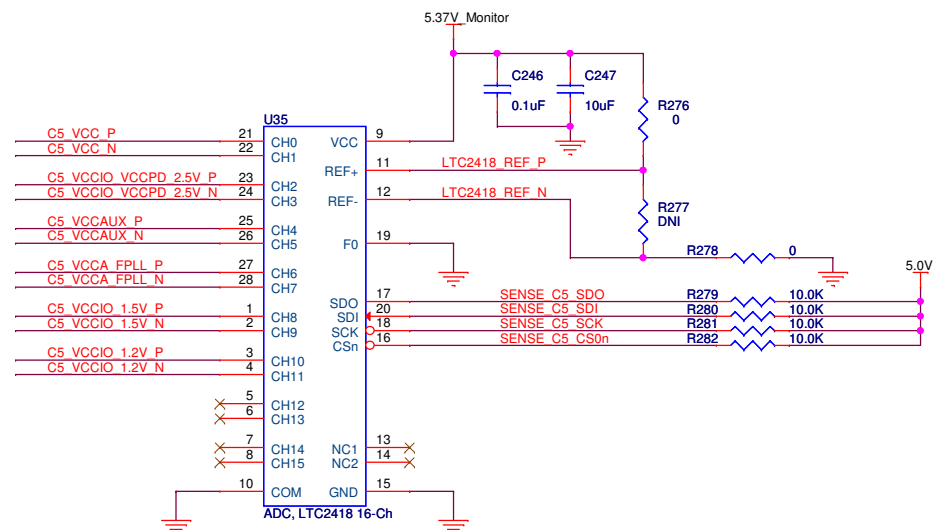
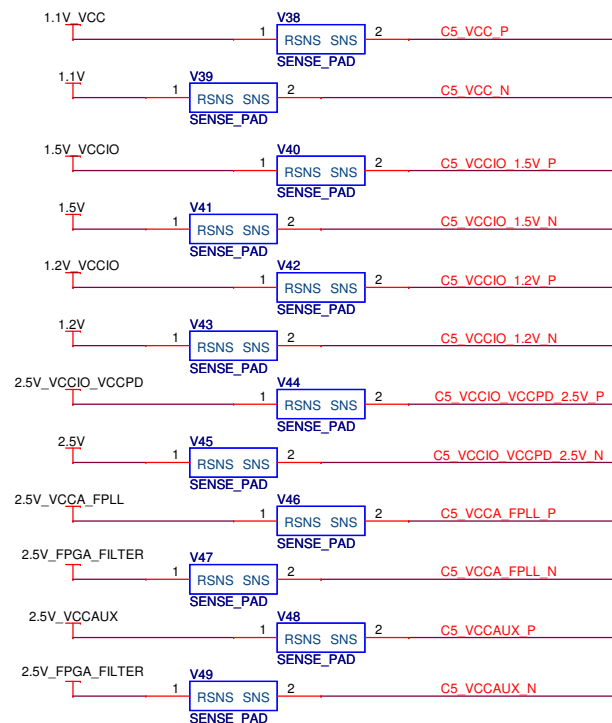


VTT LDO, LCD Character, SPI Level Shifter



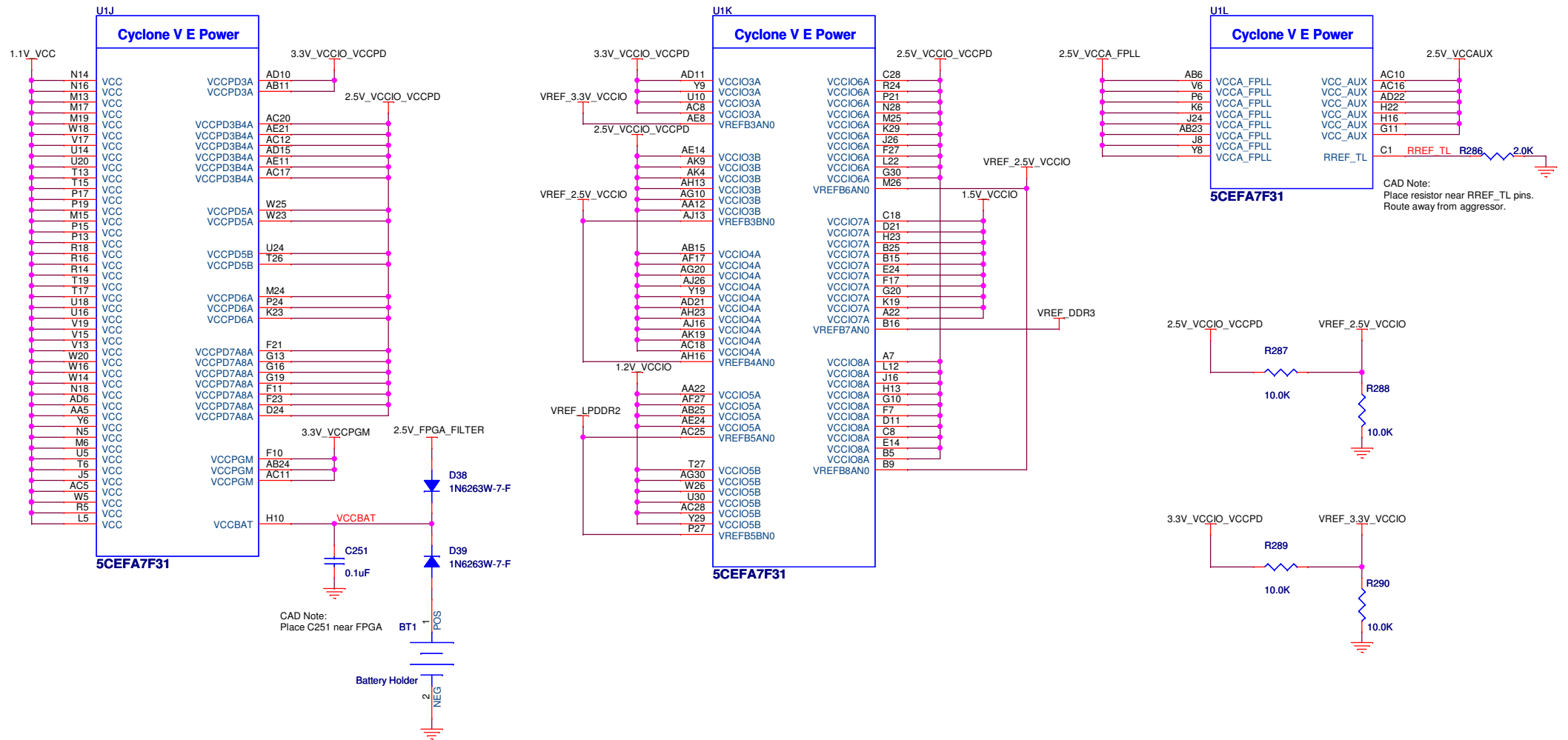
Altera Worldwide Service, Plot 6, Bayan Lepas Technoplex, Penang, Malaysia			
Title Cyclone V E Development Kit Board			
Size B	Document Number 150-0321002- B1 (6XX-44161R)	Rev B1	
Date: Thursday, November 15, 2012	Sheet 25	of 29	

# Power Monitor



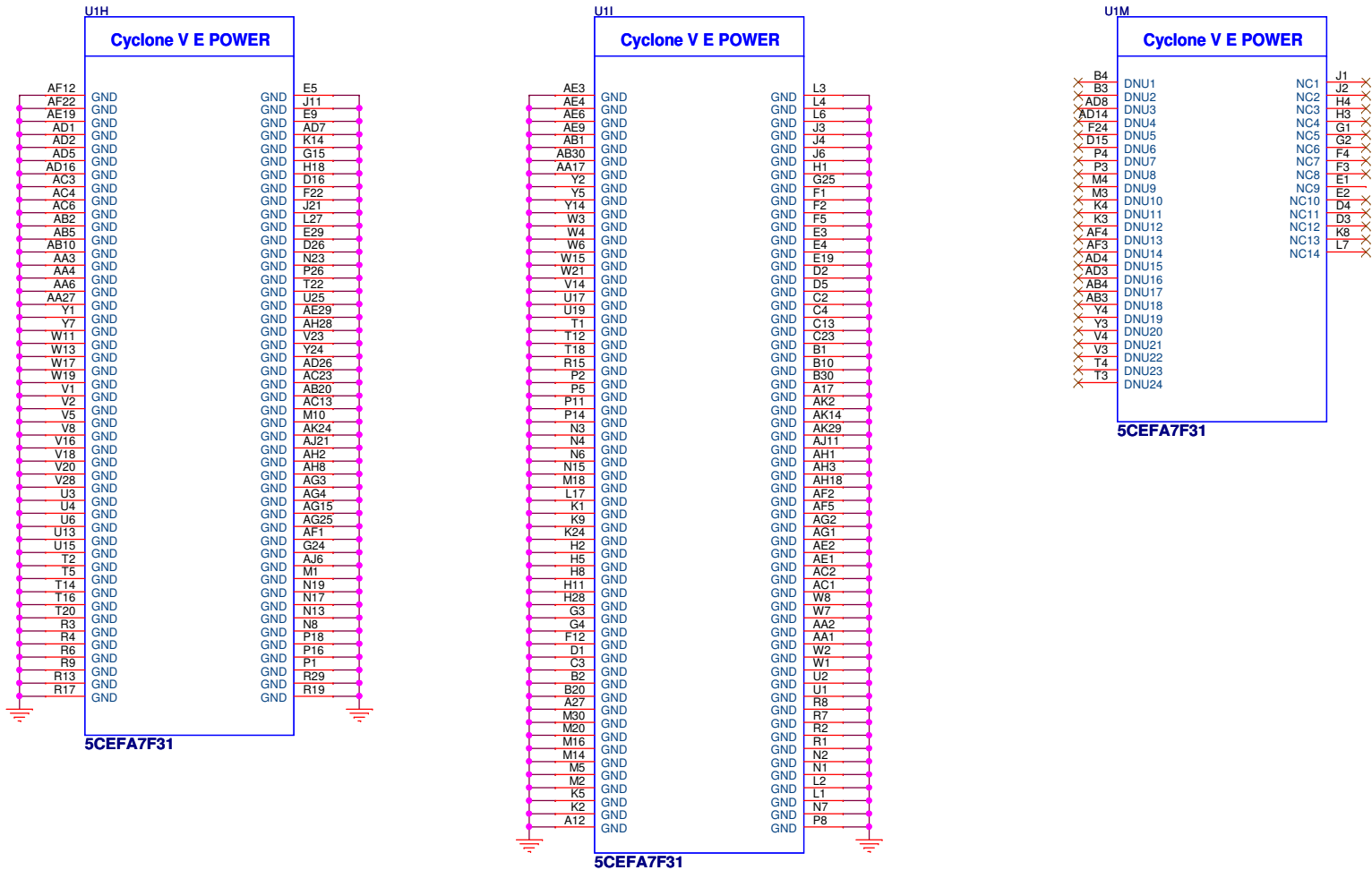
Altera Worldwide Service, Plot 6, Bayan Lepas Technoplex, Penang, Malaysia			
Title <b>Cyclone V E Development Kit Board</b>			
Size <b>B</b>	Document Number <b>150-0321002- B1 (6XX-44161R)</b>	Rev <b>B1</b>	
Date: <b>Thursday, November 15, 2012</b>	Sheet <b>26</b>	of <b>29</b>	

# Cyclone V E Bank 3 and Bank 4



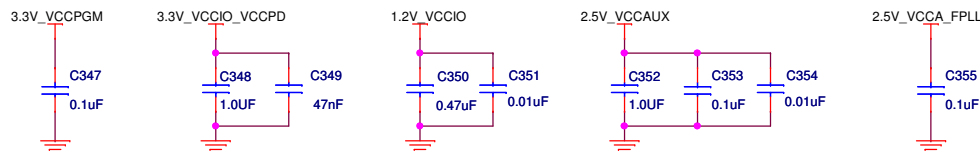
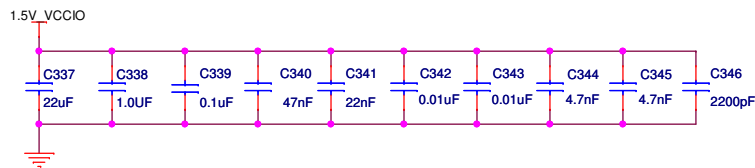
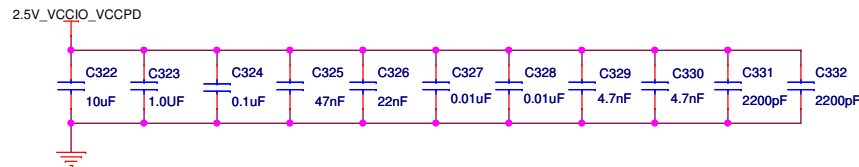
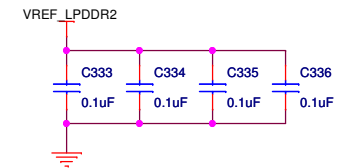
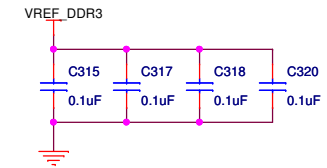
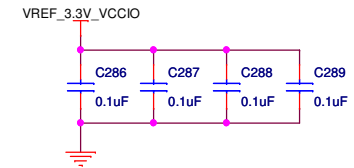
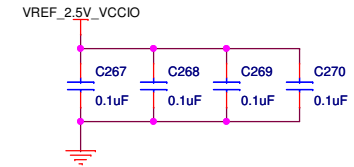
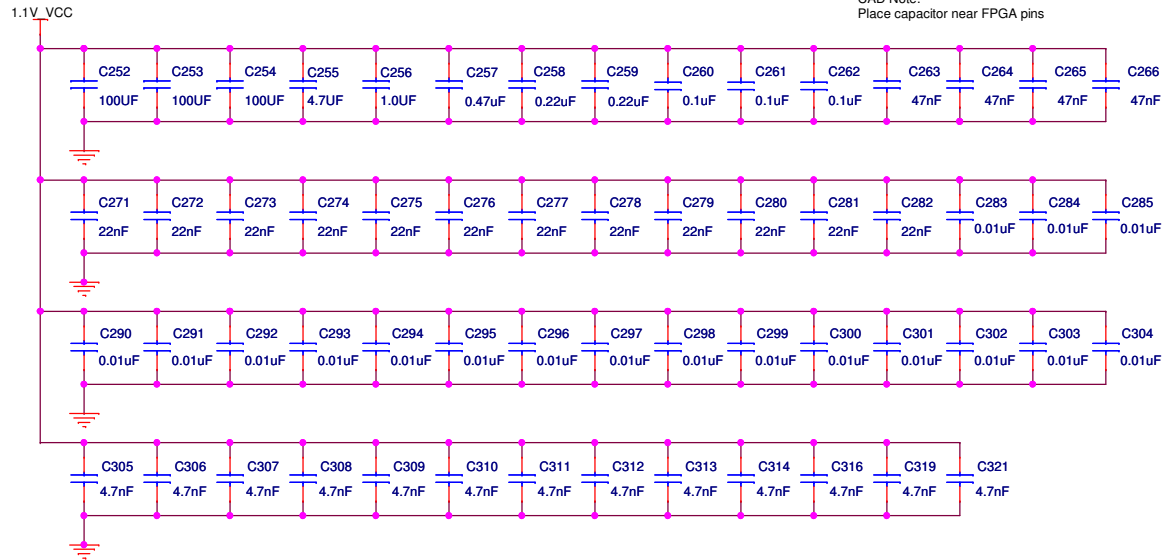
Altera Worldwide Service, Plot 6, Bayan Lepas Technoplex, Penang, Malaysia			
Title <b>Cyclone V E Development Kit Board</b>			
Size <b>B</b>	Document Number <b>150-0321002- B1 (6XX-44161R)</b>	Rev <b>B1</b>	
Date: <b>Thursday, November 15, 2012</b>	Sheet <b>27</b>	of <b>29</b>	

# Cyclone V E Bank 3 and Bank 4



# Cyclone V E Decoupling

CAD Note:  
Place capacitor near FPGA pins



SCREW1	STANDOFF1	SPACER1
SCREW2	STANDOFF2	SPACER2
SCREW3	STANDOFF3	
SCREW4	STANDOFF4	



Altera Worldwide Service, Plot 6, Bayan Lepas Technoplex, Penang, Malaysia		
Title Cyclone V E Development Kit Board		
Size B	Document Number 150-0321002- B1 (6XX-44161R)	Rev B1
Date: Thursday, November 15, 2012	Sheet 29	of 29