



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U62	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		MSEL4		MSEL4			K3								
		GND					F8								
		GND					A10								
		GND					K3								
		GND					AA1								
		GND					AA7								
		GND					AA2								
		GND					AA3								
		GND					AA9								
		GND					AB4								
		GND					AB27								
		GND					AB3								
		GND					AC1								
		GND					AC2								
		GND					AC3								
		GND					AD14								
		GND					AD22								
		GND					AD35								
		GND					AD3								
		GND					AD6								
		GND					AD8								
		GND					AE1								
		GND					AE16								
		GND					AE16								
		GND					AE2								
		GND					AE3								
		GND					AF34								
		GND					AF3								
		GND					AG1								
		GND					AG17								
		GND					AG2								
		GND					AG27								
		GND					AG3								
		GND					AG7								
		GND					AH10								
		GND					AH20								
		GND					B15								
		GND					B17								
		GND					B20								
		GND					B22								
		GND					B25								
		GND					B27								
		GND					B3								
		GND					B5								
		GND					B7								
		GND					C1								
		GND					C11								
		GND					C2								
		GND					C3								
		GND					D10								
		GND					D13								
		GND					D16								
		GND					D3								
		GND					E1								
		GND					E19								
		GND					E2								
		GND					E22								
		GND					E24								
		GND					E27								
		GND					E3								
		GND					E9								
		GND					F3								
		GND					F51								
		GND					G2								
		GND					G3								
		GND					H11								
		GND					H15								
		GND					H16								
		GND					H20								
		GND					H24								
		GND					H27								
		GND					H5								
		GND					V3								
		GND					V20								
		GND					V20								
		GND					J1								
		GND					J5								
		GND					J5								
		GND					J5								
		GND					J8								
		GND					K11								
		GND					K12								
		GND					K14								
		GND					K16								
		GND					K20								
		GND					K3								
		GND					K4								
		GND					Y14								
		GND					L1								
		GND					Y12								
		GND					L13								
		GND					L15								
		GND					L17								
		GND					L19								
		GND					L2								
		GND					L24								
		GND					L27								
		GND					L3								
		GND					L5								
		GND					U4								
		GND					U5								
		GND					M10								
		GND					M11								
		GND					M14								
		GND					M16								
		GND					M20								
		GND					M3								
		GND					M8								
		GND					N1								
		GND					N13								
		GND					N15								
		GND					N17								
		GND					N19								
		GND					N2								
		GND					N3								
		GND					N6								
		GND					P10								
		GND					P16								
		GND					P18								
		GND					P20								
		GND					P25								
		GND					P3								
		GND					P5								
		GND					P5								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U62	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					R1								
		GND					R11								
		GND					R13								
		GND					R15								
		GND					R2								
		GND					R3								
		GND					R8								
		GND					T10								
		GND					T14								
		GND					T3								
		GND					U1								
		GND					U12								
		GND					U17								
		GND					U2								
		GND					U20								
		GND					U25								
		GND					U27								
		GND					U3								
		GND					U5								
		GND					U14								
		GND					U3								
		GND					U5								
		GND					V9								
		GND					W1								
		GND					W16								
		GND					W19								
		GND					W2								
		GND					W25								
		GND					W24								
		GND					Y24								
		GND					AA26								
		GND					W20								
		GND					AE26								
		GND					W21								
		GND					U26								
		GND					U21								
		VCC					J11								
		VCC					K13								
		VCC					K15								
		VCC					L11								
		VCC					L12								
		VCC					L14								
		VCC					M12								
		VCC					M13								
		VCC					M15								
		VCC					M8								
		VCC					N10								
		VCC					N11								
		VCC					N12								
		VCC					N14								
		VCC					N8								
		VCC					P11								
		VCC					P13								
		VCC					P14								
		VCC					P15								
		VCC					R10								
		VCC					R12								
		VCC					R14								
		VCC					R9								
		VCC					T15								
		VCC					T9								
		VCC					U26								
		DNU					A2								
		DNU					B2								
		DNU					D23								
		DNU					E12								
		DNU					U8								
		DNU					AE14								
		VCCP6M					V19								
		VCCP6M					AD24								
		VCCP6M					H19								
		VCC1A1					D7								
		VCC10A					AA5								
		VCC10A					H19								
		VCC10B					AA12								
		VCC10B					AE10								
		VCC10B					AE13								
		VCC10B					AG4								
		VCC10A					AA16								
		VCC10A					AE21								
		VCC10A					AF14								
		VCC10A					AE19								
		VCC10A					AG13								
		VCC10A					AG22								
		VCC10A					AH15								
		VCC10A					AH25								
		VCC10A					W13								
		VCC10A					AC25								
		VCC10A					W17								
		VCC10A_HPS					C25								
		VCC10A_HPS					C27								
		VCC10A_HPS					F27								
		VCC10A_HPS					G24								
		VCC10A_HPS					H21								
		VCC10A_HPS					H26								
		VCC10A_HPS					L26								
		VCC10A_HPS					M21								
		VCC10B_HPS					AD27								
		VCC10B_HPS					P27								
		VCC10B_HPS					T21								
		VCC10B_HPS					T26								
		VCC10B_HPS					U18								
		VCC10B_HPS					U27								
		VCC10A_HPS					C20								
		VCC10A_HPS					D18								
		VCC10B_HPS					B13								
		VCC10B_HPS					H14								
		VCC10C_HPS					B10								
		VCC10D_HPS					D6								
		VCC10D_HPS					G6								
		VCC10A					E7								
		VCCP10A					AA10								
		VCCP10A					AA14								
		VCCP10A					AD13								
		VCCP10A					AD16								
		VCCP10A					AD18								
		VCCP10A					AD21								
		VCCP10A					AD9								
		VCCP10A					V21								
		VCCP10A_HPS					K21								
		VCCP10A_HPS					K24								
		VCCP10A_HPS					M24								
		VCCP10A_HPS					P21								
		VCCP10A_HPS					P24								
		VCCP10A_HPS					E21								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U072	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCCPDY0_HPS					E17								
		VCCPDY0_HPS					E14								
		VCCPDY0_HPS					E15								
		VCCPDY0_HPS					E19								
3A	VREFB3AND	VREFB3AND					A65								
3B	VREFB3BND	VREFB3BND					AF12								
4A	VREFB4AND	VREFB4AND					AF16								
5A	VREFB5AND	VREFB5AND					AC26								
		VREFB7A/B/C/D/E/G_HPS	VREFB7A/B/C/D/E/G_HPS				D19								
8A	VREFB8AND	VREFB8AND					D9								
		NC					W25								
		NC					AA25								
		NC					W19								
		VCC4_GXB1					M4								
		VCC4_GXB1					R4								
		VCC4_GXB1					L4								
		VCC4_GXB1					T4								
		VCC4_GXB1					F22								
		NRSTCLK_HPS					B1								
		NRSTCLK_HPS					K5								
		NRSTCLK_HPS					R4								
		NRSTCLK_HPS					U4								
		NRSTCLK_HPS					U5								
		NRSTCLK_HPS					J4								
		NRSTCLK_HPS					AA21								
		VCC_AUX					AC21								
		VCC_AUX					AC6								
		VCC_AUX					AD15								
		VCC_AUX					E16								
		VCC_AUX					F8								
		VCC_AUX_SHARED					F21								
		VCC4_GXB1					M5								
		VCC4_GXB1					N5								
		VCC4_GXB1					R5								
		VCC4_GXB1					T5								
		VCC4_GXB1					H23								
		VCC_HPS					U21								
		VCC_HPS					K17								
		VCC_HPS					L16								
		VCC_HPS					L18								
		VCC_HPS					M17								
		VCC_HPS					M19								
		VCC_HPS					M19								
		VCC_HPS					N16								
		VCC_HPS					N19								
		VCC_HPS					P17								
		VCC_HPS					P19								

Notes:

- (1) For more information about pin definitions and pin connection guidelines, refer to the [Cyclone V Device Family Pin Connection Guidelines](#).
- (2) HPS DDR pins are for memory interface only. For the dedicated pin function corresponding with the respective memory interfaces, refer to the HMC columns.
- (3) RESET pin is only applicable for DDR3 device.



Pin Information for the Cyclone® V 5CSXFC2 Device
Version 1.2

Version Number	Date	Changes Made
1.0	7/8/2013	Initial release.
1.1	9/30/2014	Remove corresponding bank number from VCCRSTCLK_HPS pin.
1.2	12/23/2016	-Renamed SDMMC_FB_CLK_IN to HPS_GPIO44.