



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
SA		MSEL3		MSEL3			C4							
SA		I2CONF0		I2CONF0			B2							
SA		MSEL4		MSEL4			C2							
		GND					C1							
		GND					A14							
		GND					A4							
		GND					AA14							
		GND					AA4							
		GND					AB1							
		GND					AB11							
		GND					AB21							
		GND					B1							
		GND					B11							
		GND					B21							
		GND					B6							
		GND					C18							
		GND					C3							
		GND					C6							
		GND					D1							
		GND					D15							
		GND					E1							
		GND					E12							
		GND					E2							
		GND					E22							
		GND					E3							
		GND					F14							
		GND					F19							
		GND					F2							
		GND					F3							
		GND					F4							
		GND					F9							
		GND					G1							
		GND					G16							
		GND					G2							
		GND					G4							
		GND					G5							
		GND					G6							
		GND					H19							
		GND					H2							
		GND					H4							
		GND					H5							
		GND					I10							
		GND					I20							
		GND					J3							
		GND					J6							
		GND					J7							
		GND					K1							
		GND					K11							
		GND					K13							
		GND					K17							
		GND					K2							
		GND					K4							
		GND					K6							
		GND					K8							
		GND					K9							
		GND					L10							
		GND					L12							
		GND					L14							
		GND					L2							
		GND					L3							
		GND					L5							
		GND					L7							
		GND					L8							
		GND					M1							
		GND					M11							
		GND					M2							
		GND					M21							
		GND					M4							
		GND					M6							
		GND					M9							
		GND					N1							
		GND					N10							
		GND					N12							
		GND					N18							
		GND					N2							
		GND					N3							
		GND					N5							
		GND					N7							
		GND					N8							
		GND					P11							
		GND					P15							
		GND					P2							
		GND					P4							
		GND					P6							
		GND					P9							
		GND					R1							
		GND					R12							
		GND					R14							
		GND					R2							
		GND					R22							
		GND					R3							
		GND					R5							
		GND					R7							
		GND					R9							
		GND					T1							
		GND					T13							
		GND					T15							
		GND					T19							
		GND					T2							
		GND					T4							
		GND					T6							
		GND					T8							
		GND					U11							
		GND					U12							
		GND					U13							
		GND					U14							
		GND					U15							
		GND					U16							
		GND					U2							
		GND					U3							
		GND					U5							
		GND					U8							
		GND					U9							
		GND					V1							
		GND					V13							
		GND					V3							
		GND					V8							
		GND					W10							



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					W15							
		GND					W20							
		GND					Y1							
		GND					Y17							
		GND					Y2							
		GND					Y7							
		GND					R16							
		GND					P13							
		VCC					H8							
		VCC					J4							
		VCC					J8							
		VCC					J8							
		VCC					K3							
		VCC					K5							
		VCC					K7							
		VCC					L4							
		VCC					L8							
		VCC					M3							
		VCC					M5							
		VCC					M7							
		VCC					M8							
		VCC					N4							
		VCC					N6							
		VCC					P3							
		VCC					P5							
		VCC					P7							
		VCC					P8							
		VCC					R4							
		VCC					R6							
		VCC					R8							
		VCC					T3							
		VCC					T5							
		VCC					T7							
		VCC					P17							
		DNU					I2							
		DNU					H1							
		DNU					H1							
		DNU					W2							
		DNU					H8							
		DNU					C17							
		DNU					G8							
		VCCP6M					Y4							
		VCCP6M					T18							
		VCCP6M					D4							
		VCCBAT					D2							
		VCCD3A					A86							
		VCCD3A					W5							
		VCCD3B					AA9							
		VCCD3A					AA10							
		VCCD3A					AB16							
		VCCD3A					Y12							
		VCCD3A					Y18							
		VCCD3A					Y22							
		VCCD3A HPS					D20							
		VCCD3A HPS					E17							
		VCCD3A HPS					G21							
		VCCD3A HPS					H18							
		VCCD3A HPS					J15							
		VCCD3A HPS					M22							
		VCCD3A HPS					L13							
		VCCD3A HPS					L19							
		VCCD3B HPS					M16							
		VCCD3B HPS					N13							
		VCCD3B HPS					P20							
		VCCD3B HPS					R17							
		VCCD3B HPS					T14							
		VCCD3B HPS					U21							
		VCCD3A HPS					A19							
		VCCD3A HPS					B16							
		VCCD3A HPS					C13							
		VCCD3A HPS					G11							
		VCCD3A HPS					D10							
		VCCD3A HPS					A9							
		VCCD3A HPS					E7							
		VCCD3A					D8							
		VCCD3A					H8							
		VCCP3B4A					AA12							
		VCCP3B4A					V12							
		VCCP3B4A					V14							
		VCCP3B4A					W13							
		VCCP3B4A					W9							
		VCCP3A					T16							
		VCCP3A6B HPS					H16							
		VCCP3A6B HPS					J17							
		VCCP3A6B HPS					L17							
		VCCP3A6B HPS					M18							
		VCCP3A HPS					G13							
		VCCP3B HPS					F12							
		VCCP3B HPS					E10							
		VCCP3B HPS					G9							
		VCCP3A					D8							
3A	VREFBAND	VREFBAND					AB4							
3B	VREFBAND	VREFBAND					AA10							
4A	VREFBAND	VREFBAND					AA20							
5A	VREFBAND	VREFBAND					W19							
	VREFBAND[CTDNO]_HPS	VREFBAND[CTDNO]_HPS					B7							
8A	VREFBAND	VREFBAND					B5							
	NC						G3							
	NC						H3							
	NC						R10							
	NC						R11							
	NC						T10							
	NC						T11							
	NC						T12							
	NC						T9							
	VCCRSTCLK_HPS						D16							
	BREF_TL						J1							
	VCCA_FPLL						L1							
	VCCA_FPLL						P1							
	VCCA_FPLL						U1							
	VCCA_FPLL						W1							
	VCCA_FPLL						F1							
	VCCA_FPLL						W17							
	VCC_AUX						AA17							
	VCC_AUX						AA3							
	VCC_AUX						D3							
	VCC_AUX						D9							
	VCC_AUX						Y10							
	VCC_AUX_SHARED						E16							



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCCDLL_HPS					F18							
		VCC_HPS					R13							
		VCC_HPS					K10							
		VCC_HPS					K12							
		VCC_HPS					L11							
		VCC_HPS					L9							
		VCC_HPS					M10							
		VCC_HPS					M9							
		VCC_HPS					N11							
		VCC_HPS					N9							
		VCC_HPS					P10							
		VCC_HPS					P12							

Notes:
 (1) For more information about pin definitions and pin connection guidelines, refer to the [Cyclone V Device Family Pin Connection Guidelines](#).
 (2) HPS_DDR pins are for memory interface only. For the dedicated pin function corresponding with the respective memory interfaces, refer to the HMC columns.
 (3) RESET pin is only applicable for DDR3 device.



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U6/2	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 /3/	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0	
		GND					V5									
		GND					V4									
		GND					A10									
		GND					A3									
		GND					AA1									
		GND					AA17									
		GND					AA2									
		GND					AA3									
		GND					AA9									
		GND					AB24									
		GND					AB27									
		GND					AB3									
		GND					AC1									
		GND					AC2									
		GND					AC3									
		GND					AD14									
		GND					AD22									
		GND					AD25									
		GND					AD3									
		GND					AD6									
		GND					AD8									
		GND					AE1									
		GND					AE16									
		GND					AE18									
		GND					AE2									
		GND					AE3									
		GND					AF24									
		GND					AF3									
		GND					AG1									
		GND					AG17									
		GND					AG2									
		GND					AG27									
		GND					AG3									
		GND					AG7									
		GND					AH10									
		GND					AH20									
		GND					B15									
		GND					B17									
		GND					B20									
		GND					B22									
		GND					B25									
		GND					B27									
		GND					B3									
		GND					B5									
		GND					B7									
		GND					C1									
		GND					C11									
		GND					C2									
		GND					C3									
		GND					D10									
		GND					D13									
		GND					D16									
		GND					D3									
		GND					E1									
		GND					E19									
		GND					E2									
		GND					E22									
		GND					E24									
		GND					E27									
		GND					E3									
		GND					E8									
		GND					F3									
		GND					G1									
		GND					G2									
		GND					G3									
		GND					H11									
		GND					H15									
		GND					H18									
		GND					H20									
		GND					H24									
		GND					H27									
		GND					H3									
		GND					H4									
		GND					H5									
		GND					H6									
		GND					I1									
		GND					I2									
		GND					I3									
		GND					I5									
		GND					I9									
		GND					K11									
		GND					K12									
		GND					K14									
		GND					K16									
		GND					K20									
		GND					K3									
		GND					K4									
		GND					K8									
		GND					L1									
		GND					L10									
		GND					L13									
		GND					L15									
		GND					L17									
		GND					L19									
		GND					L2									
		GND					L24									
		GND					L27									
		GND					L3									
		GND					L5									
		GND					L8									
		GND					M10									
		GND					M11									
		GND					M14									
		GND					M16									
		GND					M20									
		GND					M3									
		GND					M8									
		GND					N1									
		GND					N13									
		GND					N15									
		GND					N17									
		GND					N19									
		GND					N6									
		GND					N3									
		GND					N4									
		GND					P10									
		GND					P12									
		GND					P16									
		GND					P18									
		GND					P20									



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 /3/	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0	
		GND					P28									
		GND					P3									
		GND					P5									
		GND					P9									
		GND					R1									
		GND					R11									
		GND					R10									
		GND					R15									
		GND					R2									
		GND					R3									
		GND					R8									
		GND					T10									
		GND					T14									
		GND					T3									
		GND					U1									
		GND					U12									
		GND					U17									
		GND					U2									
		GND					U20									
		GND					U24									
		GND					U27									
		GND					U3									
		GND					U5									
		GND					V14									
		GND					V3									
		GND					V8									
		GND					V9									
		GND					W1									
		GND					W16									
		GND					W18									
		GND					W2									
		GND					W3									
		GND					W4									
		GND					Y12									
		GND					Y14									
		GND					Y26									
		GND					Y28									
		GND					Y3									
		GND					Y29									
		GND					V21									
		VCC					J11									
		VCC					K13									
		VCC					K16									
		VCC					L11									
		VCC					L12									
		VCC					L14									
		VCC					M12									
		VCC					M13									
		VCC					M15									
		VCC					M9									
		VCC					N10									
		VCC					N11									
		VCC					N12									
		VCC					N14									
		VCC					N9									
		VCC					P11									
		VCC					P12									
		VCC					P14									
		VCC					P15									
		VCC					R10									
		VCC					R12									
		VCC					R14									
		VCC					R9									
		VCC					T15									
		VCC					T9									
		VCC					L4									
		VCC					T4									
		VCC					M5									
		VCC					N5									
		VCC					R5									
		VCC					T5									
		VCC					U26									
		DNU					A2									
		DNU					B2									
		DNU					D1									
		DNU					D3									
		DNU					H1									
		DNU					H2									
		DNU					M1									
		DNU					M2									
		DNU					T1									
		DNU					T2									
		DNU					Y1									
		DNU					Y2									
		DNU					AD1									
		DNU					AD2									
		DNU					UB									
		DNU					AE14									
		DNU					D23									
		DNU					E12									
		VCCPGM					Y10									
		VCCPGM					AD24									
		VCCPGM					H10									
		VCCBAT					D7									
		VCCIO3A					AA5									
		VCCIO3A					W8									
		VCCIO3B					AA12									
		VCCIO3B					AE10									
		VCCIO3B					AE13									
		VCCIO3B					AG4									
		VCCIO4A					AA16									
		VCCIO4A					AE21									
		VCCIO4A					AF14									
		VCCIO4A					AF19									
		VCCIO4A					AG12									
		VCCIO4A					AG22									
		VCCIO4A					AH15									
		VCCIO4A					AH25									
		VCCIO4A					W13									
		VCCIO4A					AC25									
		VCCIO4A					W17									
		VCCIO4B					W25									
		VCCIO4A_HPS					C25									
		VCCIO4A_HPS					C27									
		VCCIO4A_HPS					F27									
		VCCIO4A_HPS					G24									
		VCCIO4A_HPS					H21									
		VCCIO4A_HPS					H26									
		VCCIO4A_HPS					L26									
		VCCIO4A_HPS					M21									
		VCCIO4B_HPS					AD27									



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U6/2	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2/3/3	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCCIO8B_HPS					P27								
		VCCIO8B_HPS					T21								
		VCCIO8B_HPS					T25								
		VCCIO8B_HPS					U18								
		VCCIO8B_HPS					W27								
		VCCIO7A_HPS					C20								
		VCCIO7A_HPS					D16								
		VCCIO7B_HPS					B13								
		VCCIO7B_HPS					H14								
		VCCIO7C_HPS					B10								
		VCCIO7D_HPS					D6								
		VCCIO7D_HPS					G5								
		VCCIO8A					E7								
		VCCPD3A					AA10								
		VCCPD3B4A					AA14								
		VCCPD3B4A					AD13								
		VCCPD3B4A					AD16								
		VCCPD3B4A					AD18								
		VCCPD3B4A					AD21								
		VCCPD3A					AD9								
		VCCPD5A					V21								
		VCCPD5B					W19								
		VCCPD6A8B_HPS					K21								
		VCCPD6A8B_HPS					K24								
		VCCPD6A8B_HPS					M24								
		VCCPD6A8B_HPS					P21								
		VCCPD6A8B_HPS					P24								
		VCCPD7A_HPS					E21								
		VCCPD7B_HPS					E17								
		VCCPD7C_HPS					E14								
		VCCPD7D_HPS					E13								
		VCCPD8A					E10								
3A	VREFB3A00	VREFB3A00					A65								
3B	VREFB3B00	VREFB3B00					AF12								
4A	VREFB4A00	VREFB4A00					AF16								
5A	VREFB5A00	VREFB5A00					AC06								
5B	VREFB5B00	VREFB5B00					AA25								
		VREFB7A/B/C	VREFB7A/B/C/D00_HPS				D19								
8A	VREFB8A00	VREFB8A00					D6								
		VCCRSTCLK_HPS					F22								
		RREF_TL					B1								
		VCCA_FPLL					K5								
		VCCA_FPLL					P4								
		VCCA_FPLL					U6								
		VCCA_FPLL					W5								
		VCCA_FPLL					J4								
		VCCA_FPLL					AA21								
		VCCA_FPLL					M4								
		VCCA_FPLL					R4								
		VCC_AUX					AC21								
		VCC_AUX					AC8								
		VCC_AUX					AD15								
		VCC_AUX					E15								
		VCC_AUX					F8								
		VCC_AUX_SHARED					F21								
		VCCPLL_HPS					H23								
		VCC_HPS					U21								
		VCC_HPS					K17								
		VCC_HPS					L16								
		VCC_HPS					L18								
		VCC_HPS					M17								
		VCC_HPS					M18								
		VCC_HPS					M19								
		VCC_HPS					N16								
		VCC_HPS					N18								
		VCC_HPS					P17								
		VCC_HPS					P19								

Notes:
(1) For more information about pin definitions and pin connection guidelines, refer to the [Cyclone V Device Family Pin Connection Guidelines](#).
(2) HPS_DDR pins are for memory interface only. For the dedicated pin function corresponding with the respective memory interfaces, refer to the HMC columns.
(3) RESET pin is only applicable for DDR3 device.



Pin Information for the Cyclone® V 5CSEBA6S Device
Version 1.5

Version Number	Date	Changes Made
1.0	10/18/2012	Initial release.
1.1	1/17/2013	A pin that was marked as VCC_HPS has been corrected to VCCRSTCLK_HPS
1.2	3/25/2013	Updated the following pin names: - Changed SDMMC_CLK_IN to SDMMC_FB_CLK_IN - Changed SDMMC_CLK to SDMMC_CCLK_OUT
1.3	9/30/2014	- Remove corresponding bank number from VCCRSTCLK_HPS pin. - Changed HMC Pin Assignment for DDR3 to HMC Pin Assignment for DDR3/DDR2. - Added note 3.
1.4	1/4/2016	Removed the USB0 pin from Pin List U19.
1.5	12/23/2016	-Renamed SDMMC_FB_CLK_IN to HPS_GPIO44.