



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	MU2	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
3A		TDO		TDO			Y9								
3A		IC30		DATA4			A46								
3A		TMS		TMS			A47								
3A		AS_DATA3		DATA3			A86								
3A		TCK		TCK			A85								
3A		AS_DATA2		DATA2			ACK								
3A		TDI		TDI			W10								
3A		AS_DATA1		DATA1			AC8								
3A		CLKX		CLKX			A48								
3A		AS_DATA0,ASD0		DATA0			A07								
3A	VREFB3AND	IO		DATA6	DIFFO_RX_B1n	DIFFOUT_B1n	Y8	DQ1B							
3A	VREFB3AND	IO		DATA5	DIFFO_RX_B2n	DIFFOUT_B2n	Y4								
3A	VREFB3AND	IO		DATA8	DIFFO_RX_B1p	DIFFOUT_B1p	W8	DQ1B							
3A	VREFB3AND	IO		DATA7	DIFFO_TX_B2p	DIFFOUT_B2p	Y5	DQ1B							
3A	VREFB3AND	IO		DATA10	DIFFO_RX_B3n	DIFFOUT_B3n	Y8	DQS#1B							
3A	VREFB3AND	IO		DATA9	DIFFO_TX_B4n	DIFFOUT_B4n	A84	DQ1B							
3A	VREFB3AND	IO		DATA12	DIFFO_RX_B3p	DIFFOUT_B3p	U9	DQS1B							
3A	VREFB3AND	IO		DATA11	DIFFO_TX_B4p	DIFFOUT_B4p	A44								
3A	VREFB3AND	IO		DATA14	DIFFO_RX_B5n	DIFFOUT_B5n	V10	DQ1B							
3A	VREFB3AND	IO		DATA13	DIFFO_TX_B6p	DIFFOUT_B6p	A10	DQ1B							
3A	VREFB3AND	IO		CLKUSR	DIFFO_RX_B5p	DIFFOUT_B5p	U10	DQ1B							
3A	VREFB3AND	IO		DATA15	DIFFO_TX_B6p	DIFFOUT_B6p	AC4	DQ1B							
3A	VREFB3AND	IO		PR_DONE	DIFFO_RX_B7n	DIFFOUT_B7n	A41								
3A	VREFB3AND	IO		PR_READY	DIFFO_TX_B8n	DIFFOUT_B8n	A6	DQ1B							
3A	VREFB3AND	IO		PR_ERROR	DIFFO_RX_B7p	DIFFOUT_B7p	Y11								
3A	VREFB3AND	IO			DIFFO_TX_B8p	DIFFOUT_B8p	A06	DQ1B							
3B	VREFB3BND	IO			DIFFO_TX_B25n	DIFFOUT_B25n	AF4			GND	GND				
3B	VREFB3BND	IO			DIFFO_RX_B26n	DIFFOUT_B26n	AE9	DQ2B		B_A_15					
3B	VREFB3BND	IO			DIFFO_TX_B25p	DIFFOUT_B25p	AE4	DQ2B		B_WEP					
3B	VREFB3BND	IO			DIFFO_RX_B26p	DIFFOUT_B26p	AD10	DQ2B		B_A_14					
3B	VREFB3BND	IO			DIFFO_RX_B27n	DIFFOUT_B27n	U11	DQS#2B		B_CS#_0		B_CS#_1			
3B	VREFB3BND	IO			DIFFO_TX_B28n	DIFFOUT_B28n	AF8	DQ2B		B_A_13					
3B	VREFB3BND	IO			DIFFO_RX_B27p	DIFFOUT_B27p	T11	DQS2B		B_CS#_0					
3B	VREFB3BND	IO			DIFFO_TX_B28p	DIFFOUT_B28p	AE7			B_A_12					
3B	VREFB3BND	IO			DIFFO_TX_B29n	DIFFOUT_B29n	AF9	DQ2B		B_A_11					
3B	VREFB3BND	IO			DIFFO_RX_B30n	DIFFOUT_B30n	AE11	DQ2B		B_A_9		B_CA_9			
3B	VREFB3BND	IO			DIFFO_TX_B30p	DIFFOUT_B30p	A08	DQ2B		B_A_10					
3B	VREFB3BND	IO			DIFFO_RX_B30p	DIFFOUT_B30p	AD11	DQ2B		B_A_8		B_CA_8			
3B	VREFB3BND	IO	CLK0n,FPLL_BL_FBn		DIFFO_RX_B31n	DIFFOUT_B31n	W11								
3B	VREFB3BND	IO			DIFFO_TX_B32n	DIFFOUT_B32n	V11	DQ2B		B_RAS#					
3B	VREFB3BND	IO			DIFFO_RX_B31p	DIFFOUT_B31p	V11								
3B	VREFB3BND	IO			DIFFO_TX_B32p	DIFFOUT_B32p	AF5	DQ2B		B_CAS#					
3B	VREFB3BND	IO			DIFFO_TX_B33n	DIFFOUT_B33n	A08			GND	GND				
3B	VREFB3BND	IO			DIFFO_RX_B34n	DIFFOUT_B34n	AF10	DQ3B		B_BA_2					
3B	VREFB3BND	IO			DIFFO_TX_B33p	DIFFOUT_B33p	AF7			B_BA_0					
3B	VREFB3BND	IO			DIFFO_RX_B34p	DIFFOUT_B34p	AE11	DQ3B		B_BA_4					
3B	VREFB3BND	IO			DIFFO_RX_B35n	DIFFOUT_B35n	T12	DQS#3B		B_CKE		B_CKE			
3B	VREFB3BND	IO			DIFFO_TX_B36n	DIFFOUT_B36n	AH2	DQ3B		B_A_7		B_CA_7			
3B	VREFB3BND	IO			DIFFO_RX_B35p	DIFFOUT_B35p	T13	DQS3B		B_CK		B_CK			
3B	VREFB3BND	IO			DIFFO_TX_B36p	DIFFOUT_B36p	AH3			B_A_6		B_CA_6			
3B	VREFB3BND	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFO_TX_B37n	DIFFOUT_B37n	AH4	DQ3B		B_A_3		B_CA_3			
3B	VREFB3BND	IO			DIFFO_RX_B38n	DIFFOUT_B38n	AD12	DQ3B		B_A_5		B_CA_5			
3B	VREFB3BND	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFO_TX_B37p	DIFFOUT_B37p	A08	DQ3B		B_A_2		B_CA_2			
3B	VREFB3BND	IO			DIFFO_RX_B38p	DIFFOUT_B38p	AE12	DQ3B		B_A_4		B_CA_4			
3B	VREFB3BND	IO	CLK1n		DIFFO_RX_B39n	DIFFOUT_B39n	W12								
3B	VREFB3BND	IO			DIFFO_TX_B40n	DIFFOUT_B40n	AH5	DQ3B		B_A_1		B_CA_1			
3B	VREFB3BND	IO	CLK1p		DIFFO_RX_B39p	DIFFOUT_B39p	V12								
3B	VREFB3BND	IO			DIFFO_TX_B40p	DIFFOUT_B40p	AH6	DQ3B		B_A_0		B_CA_0			
4A	VREFB4AND	IO	R20_0		DIFFO_TX_B41n	DIFFOUT_B41n	AH7								
4A	VREFB4AND	IO			DIFFO_RX_B42n	DIFFOUT_B42n	AG4	DQ4B		B_DQ_0		B_DM_0			
4A	VREFB4AND	IO			DIFFO_TX_B41p	DIFFOUT_B41p	AG8	DQ4B		B_DQ_2		B_DM_2			
4A	VREFB4AND	IO			DIFFO_RX_B42p	DIFFOUT_B42p	AG13	DQ4B		B_DQ_1		B_DM_1			
4A	VREFB4AND	IO			DIFFO_RX_B43n	DIFFOUT_B43n	U13	DQS#4B		B_DQS#_0		B_DM_0			
4A	VREFB4AND	IO			DIFFO_TX_B44n	DIFFOUT_B44n	AH8	DQ4B		B_DQS#_0					
4A	VREFB4AND	IO			DIFFO_RX_B43p	DIFFOUT_B43p	U14	DQS4B		B_DQS_0					
4A	VREFB4AND	IO			DIFFO_TX_B44p	DIFFOUT_B44p	AG9			B_DQ_0		B_DQ_0			
4A	VREFB4AND	IO			DIFFO_TX_B45n	DIFFOUT_B45n	AH9	DQ4B		B_DQ_1		B_DQ_1			
4A	VREFB4AND	IO			DIFFO_RX_B45n	DIFFOUT_B45n	AE15	DQ4B		B_DQ_4		B_DQ_4			
4A	VREFB4AND	IO			DIFFO_TX_B45p	DIFFOUT_B45p	AG10	DQ4B		B_DQ_6		B_DQ_6			
4A	VREFB4AND	IO			DIFFO_RX_B46n	DIFFOUT_B46n	AF15	DQ4B		B_DQ_8		B_DQ_8			
4A	VREFB4AND	IO	CLK2n		DIFFO_TX_B47n	DIFFOUT_B47n	AA13			B_DQ_9					
4A	VREFB4AND	IO			DIFFO_TX_B48n	DIFFOUT_B48n	AH11	DQ4B		B_DQ_7					
4A	VREFB4AND	IO	CLK2p		DIFFO_RX_B47p	DIFFOUT_B47p	Y13								
4A	VREFB4AND	IO			DIFFO_TX_B48p	DIFFOUT_B48p	AG11	DQ4B		B_DM_0		B_DM_0			
4A	VREFB4AND	IO			DIFFO_RX_B50n	DIFFOUT_B50n	AG16	DQ5B	DQ1B	B_DM_8		B_DM_8			
4A	VREFB4AND	IO			DIFFO_TX_B49p	DIFFOUT_B49p	AH12	DQ5B	DQ1B	B_DQ_10		B_DQ_10			
4A	VREFB4AND	IO			DIFFO_RX_B50p	DIFFOUT_B50p	AF17	DQ5B	DQ1B	B_DQ_9		B_DQ_9			
4A	VREFB4AND	IO			DIFFO_RX_B51n	DIFFOUT_B51n	V13	DQS#5B	DQ1B	B_DQS#_1		B_DQS#_1			
4A	VREFB4AND	IO			DIFFO_TX_B52n	DIFFOUT_B52n	AH13	DQ5B	DQ1B	B_DM_11		B_DM_11			
4A	VREFB4AND	IO			DIFFO_RX_B51p	DIFFOUT_B51p	W14	DQS#5B	DQ1B	B_DQS_1		B_DQS_1			
4A	VREFB4AND	IO			DIFFO_TX_B52p	DIFFOUT_B52p	AG14			B_CKE_1		B_CKE_1			
4A	VREFB4AND	IO			DIFFO_TX_B53n	DIFFOUT_B53n	AH14	DQ5B	DQ1B	B_CKE_0		B_CKE_0			
4A	VREFB4AND	IO			DIFFO_RX_B54n	DIFFOUT_B54n	AE17	DQ5B	DQ1B	B_DQ_12		B_DQ_12			
4A	VREFB4AND	IO			DIFFO_TX_B53p	DIFFOUT_B53p	AD15	DQ5B	DQ1B	B_DQ_14		B_DQ_14			
4A	VREFB4AND	IO			DIFFO_RX_B54p	DIFFOUT_B54p	AD17	DQ5B	DQ1B	B_DQ_13		B_DQ_13			
4A	VREFB4AND	IO	CLK3n		DIFFO_RX_B55n	DIFFOUT_B55n	AA15								
4A	VREFB4AND	IO			DIFFO_TX_B56n	DIFFOUT_B56n	AH16	DQ5B	DQ1B	B_DQ_15		B_DQ_15			
4A	VREFB4AND	IO	CLK3p		DIFFO_RX_B55p	DIFFOUT_B55p	Y15								
4A	VREFB4AND	IO			DIFFO_TX_B56p	DIFFOUT_B56p	AH17	DQ5B	DQ1B	B_DM_1		B_DM_1			
4A	VREFB4AND	IO			DIFFO_RX_B58n	DIFFOUT_B58n	AD19	DQ6B	DQ1B	B_DM_16		B_DM_16			
4A	VREFB4AND	IO			DIFFO_TX_B57p	DIFFOUT_B57p	AF19	DQ6B	DQ1B	B_DM_18		B_DM_18			
4A	VREFB4AND	IO			DIFFO_RX_B58p	DIFFOUT_B58p	AE19	DQ6B	DQ1B	B_DQ_17		B_DQ_17			
4A	VREFB4AND	IO			DIFFO_RX_B59n	DIFFOUT_B59n	AA18	DQS#6B	DQS#1B	B_DQS#_2		B_DQS#_2			
4A	VREFB4AND	IO			DIFFO_TX_B60n	DIFFOUT_B60n	AH19	DQ6B	DQ1B	B_DQ_19		B_DQ_19			
4A	VREFB4AND	IO			DIFFO_RX_B59p	DIFFOUT_B59p	AA19	DQS#6B	DQS1B	B_DQS_2		B_DQS_2			
4A	VREFB4AND	IO			DIFFO_TX_B60p	DIFFOUT_B60p	AG18			B_RESETr		B_RESETr			
4A	VREFB4AND	IO			DIFFO_TX_B61n	DIFFOUT_B61n	AH19	DQ6B	DQ1B	GND		GND			
4A	VREFB4AND	IO			DIFFO_RX_B60n	DIFFOUT_B60n	AD20	DQ6B	DQ1B	B_DM_20		B_DM_20			
4A	VREFB4AND	IO			DIFFO_TX_B61p	DIFFOUT_B61p	AG19	DQ6B	DQ1B	B_DM_22		B_DM_22			
4A	VREFB4AND	IO			DIFFO_RX_B62p	DIFFOUT_B62p	AE20	DQ6B	DQ1B	B_DM_21		B_DM_21			
4A	VREFB4AND	IO			DIFFO_TX_B64n	DIFFOUT_B64n	AG20	DQ6B	DQ1B	B_DM_23		B_DM_23			
4A	VREFB4AND	IO			DIFFO_TX_B64p	DIFFOUT_B64p	AF20	DQ6B	DQ1B	B_DM_2		B_DM_2			
4A	VREFB4AND	IO			DIFFO_RX_B66n	DIFFOUT_B66n	AF21	DQ7B	DQ2B	B_DM_24		B_DM_24			
4A	VREFB4AND	IO			DIFFO_TX_B65p	DIFFOUT_B65p	AA21	DQ7B	DQ2B	B_DM_26		B_DM_26			
4A	VREFB4AND	IO			DIFFO_RX_B66p	DIFFOUT_B66p	AF22	DQ7B	DQ2B	B_DM_25		B_DM_25			
4A	VREFB4AND	IO			DIFFO_RX_B67n	DIFFOUT_B67n	AE22	DQS#7B	DQ2B	B_DQS#_3		B_DQS#_3			
4A	VREFB4AND	IO			DIFFO_TX_B68n	DIFFOUT_B68n	AH21	DQ7B	DQ2B	B_DQ_27		B_DQ_27			
4A	VREFB4AND	IO			DIFFO_RX_B67p	DIFFOUT_B67p	AD21	DQ7B	DQ2B	B_DQ_3		B_DQ_3			
4A	VREFB4AND	IO			DIFFO_TX_B69n	DIFFOUT_B69n	AH22	DQ7B	DQ2B	GND		GND			
4A	VREFB4AND	IO			DIFFO_RX_B70n	DIFFOUT_B70n	AF23	DQ7B	DQ2B	B_DM_28		B_DM_28			
4A	VREFB4AND	IO			DIFFO_TX_B69p	DIFFOUT_B69p	AH23	DQ7B	DQ2B	B_DM_30		B_DM_30			
4A	VREFB4AND	IO			DIFFO_RX_B70p	DIFFOUT_B70p	AG23	DQ7B	DQ2B	B_DM_29		B_DM_29			
4A	VREFB4AND	IO			DIFFO_TX_B72n	DIFFOUT_B72n									



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	MU2	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
4A	VREFB4AND	IO			DIFFIO_TX_B73p	DIFFOUT_B73p	AG26	DQ8B	DQ2B	B_DQ_34	B_DQ_34				
4A	VREFB4AND	IO			DIFFIO_RX_B74p	DIFFOUT_B74p	AE24	DQ8B	DQ2B	B_DQ_33	B_DQ_33				
4A	VREFB4AND	IO			DIFFIO_TX_B76m	DIFFOUT_B76m	AG27	DQ8B	DQ2B	B_DQS#_4	B_DQS#_4				
4A	VREFB4AND	IO			DIFFIO_TX_B76m	DIFFOUT_B76m	AH26	DQ8B	DQ2B	B_DQ_35	B_DQ_35				
4A	VREFB4AND	IO			DIFFIO_RX_B75p	DIFFOUT_B75p	AC22	DQ8B	DQ2B	B_DQS_4	B_DQS_4				
4A	VREFB4AND	IO			DIFFIO_TX_B77n	DIFFOUT_B77n	AH27	DQ8B	DQ2B	GND	GND				
4A	VREFB4AND	IO			DIFFIO_RX_B78n	DIFFOUT_B78n	AG25	DQ8B	DQ2B	B_DQ_36	B_DQ_36				
4A	VREFB4AND	IO			DIFFIO_TX_B77p	DIFFOUT_B77p	AG28	DQ8B	DQ2B	B_DQ_38	B_DQ_38				
4A	VREFB4AND	IO			DIFFIO_RX_B78p	DIFFOUT_B78p	AF28	DQ8B	DQ2B	B_DQ_37	B_DQ_37				
4A	VREFB4AND	IO			DIFFIO_TX_B80n	DIFFOUT_B80n	AF38	DQ8B	DQ2B	B_DQ_39	B_DQ_39				
4A	VREFB4AND	IO			DIFFIO_TX_B80p	DIFFOUT_B80p	AF27	DQ8B	DQ2B	B_DM_4	B_DM_4				
5A	VREFB5AND	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	AF26	DQ1R							
5A	VREFB5AND	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	AA20								
5A	VREFB5AND	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	AE26	DQ1R							
5A	VREFB5AND	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	Y19								
5A	VREFB5AND	IO		ICEO	DIFFIO_TX_R3p	DIFFOUT_R3p	AE26	DQ1R							
5A	VREFB5AND	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	Y17	DQ1R							
5A	VREFB5AND	IO		C/P_CONF_DONE	DIFFIO_TX_R3n	DIFFOUT_R3n	AD26	DQ1R							
5A	VREFB5AND	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	V18	DQ1R							
5A	VREFB5AND	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	AC24								
5A	VREFB5AND	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	Y16	DQS1R							
5A	VREFB5AND	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	AB23	DQ1R							
5A	VREFB5AND	IO			DIFFIO_RX_R6n	DIFFOUT_R6n	V15	DQS1R							
5A	VREFB5AND	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	AA24	DQ1R							
5A	VREFB5AND	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	V16	DQ1R							
5A	VREFB5AND	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	AA23								
5A	VREFB5AND	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	V15	DQ1R							
5B	VREFB5AND	IO			DIFFIO_RX_R21p	DIFFOUT_R21p	W21								
5B	VREFB5AND	IO		P/LL_BR_CLKOUT0/P/LL_BR_CLKOUTn/P/LL_BR_FB	DIFFIO_TX_R22p	DIFFOUT_R22p	AB26								
5B	VREFB5AND	IO		CLK0p	DIFFIO_RX_R21n	DIFFOUT_R21n	W20								
5B	VREFB5AND	IO		P/LL_BR_CLKOUT1/P/LL_BR_CLKOUTn	DIFFIO_TX_R22n	DIFFOUT_R22n	AA26								
5B	VREFB5AND	IO		CLK0n/P/LL_BR_FBn	DIFFIO_RX_R23p	DIFFOUT_R23p	Y24								
5B	VREFB5AND	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	W24								
5B	VREFB5AND	IO	RZQ_2		DIFFIO_TX_R24n	DIFFOUT_R24n	AB25								
6B	VREFB6AND_HPS	HPS_DDR					AE28			HPS_DM_4	HPS_DM_4				
6B	VREFB6AND_HPS	HPS_DDR					AD28			HPS_DQ_39	HPS_DQ_39				
6B	VREFB6AND_HPS	HPS_DDR					V20			HPS_DQ_37	HPS_DQ_37				
6B	VREFB6AND_HPS	HPS_DDR					AE27			HPS_DQ_38	HPS_DQ_38				
6B	VREFB6AND_HPS	HPS_DDR					V19			HPS_DQ_36	HPS_DQ_36				
6B	VREFB6AND_HPS	HPS_DDR					V18			HPS_DQS_4	HPS_DQS_4				
6B	VREFB6AND_HPS	HPS_GPI13					V24								
6B	VREFB6AND_HPS	HPS_DDR					V17			HPS_DQS#_4	HPS_DQS#_4				
6B	VREFB6AND_HPS	HPS_DDR					U26			HPS_DQ_35	HPS_DQ_35				
6B	VREFB6AND_HPS	HPS_DDR					U25			HPS_DQ_33	HPS_DQ_33				
6B	VREFB6AND_HPS	HPS_DDR					U25			HPS_DQ_33	HPS_DQ_33				
6B	VREFB6AND_HPS	HPS_DDR					AC28			HPS_DQ_34	HPS_DQ_34				
6B	VREFB6AND_HPS	HPS_DDR					Z26			HPS_DQ_32	HPS_DQ_32				
6B	VREFB6AND_HPS	HPS_GPI12					AC27								
6B	VREFB6AND_HPS	HPS_GPI11					U16								
6B	VREFB6AND_HPS	HPS_DDR					AB26			HPS_DM_3	HPS_DM_3				
6B	VREFB6AND_HPS	HPS_GPI10					U16								
6B	VREFB6AND_HPS	HPS_DDR					AA27			HPS_DQ_31	HPS_DQ_31				
6B	VREFB6AND_HPS	HPS_DDR					T24			HPS_DQ_29	HPS_DQ_29				
6B	VREFB6AND_HPS	HPS_DDR					T27			HPS_DQ_30	HPS_DQ_30				
6B	VREFB6AND_HPS	HPS_DDR					S24			HPS_DQ_28	HPS_DQ_28				
6B	VREFB6AND_HPS	VREFB6AND_HPS					T27								
6B	VREFB6AND_HPS	HPS_DDR					U19			HPS_DQS_3	HPS_DQS_3				
6B	VREFB6AND_HPS	HPS_GPI9					T20			HPS_DQS#_3	HPS_DQS#_3				
6B	VREFB6AND_HPS	HPS_DDR					W26			HPS_DQ_27	HPS_DQ_27				
6B	VREFB6AND_HPS	HPS_DDR					R26			HPS_DQ_25	HPS_DQ_25				
6B	VREFB6AND_HPS	HPS_DDR					AA28			HPS_DQ_26	HPS_DQ_26				
6B	VREFB6AND_HPS	HPS_DDR					R26			HPS_DQ_24	HPS_DQ_24				
6B	VREFB6AND_HPS	HPS_GPI8					T26								
6B	VREFB6AND_HPS	HPS_GPI7					T16								
6B	VREFB6AND_HPS	HPS_DDR					W28			HPS_DM_2	HPS_DM_2				
6B	VREFB6AND_HPS	HPS_GPI6					T17								
6B	VREFB6AND_HPS	HPS_DDR					N27			HPS_DQ_23	HPS_DQ_23				
6B	VREFB6AND_HPS	HPS_DDR					N27			HPS_DQ_21	HPS_DQ_21				
6B	VREFB6AND_HPS	HPS_DDR					R27			HPS_DQ_22	HPS_DQ_22				
6B	VREFB6AND_HPS	HPS_DDR					R26			HPS_DQ_20	HPS_DQ_20				
6B	VREFB6AND_HPS	HPS_GPI5					T26								
6B	VREFB6AND_HPS	HPS_DDR					T19			HPS_DQS_2	HPS_DQS_2				
6B	VREFB6AND_HPS	HPS_DDR					Y28			HPS_RESET#	HPS_RESET#				
6B	VREFB6AND_HPS	HPS_DDR					T19			HPS_DQS#_2	HPS_DQS#_2				
6B	VREFB6AND_HPS	HPS_DDR					U28			HPS_DQ_19	HPS_DQ_19				
6B	VREFB6AND_HPS	HPS_DDR					N25			HPS_DQ_17	HPS_DQ_17				
6B	VREFB6AND_HPS	HPS_DDR					T28			HPS_DQ_18	HPS_DQ_18				
6B	VREFB6AND_HPS	HPS_DDR					N24			HPS_DQ_16	HPS_DQ_16				
6B	VREFB6AND_HPS	HPS_GPI4					R28								
6A	VREFB6AND_HPS	HPS_GPI3					R21								
6A	VREFB6AND_HPS	HPS_DDR					T28			HPS_DM_1	HPS_DM_1				
6A	VREFB6AND_HPS	HPS_GPI2					R20								
6A	VREFB6AND_HPS	HPS_DDR					N28			HPS_DQ_15	HPS_DQ_15				
6A	VREFB6AND_HPS	HPS_DDR					M26			HPS_DQ_13	HPS_DQ_13				
6A	VREFB6AND_HPS	HPS_DDR					M28			HPS_DQ_14	HPS_DQ_14				
6A	VREFB6AND_HPS	HPS_DDR					M27			HPS_DQ_12	HPS_DQ_12				
6A	VREFB6AND_HPS	HPS_DDR					L26			HPS_CKE_0	HPS_CKE_0				
6A	VREFB6AND_HPS	HPS_DDR					R19			HPS_DQS_1	HPS_DQS_1				
6A	VREFB6AND_HPS	HPS_DDR					K28			HPS_CKE_1	HPS_CKE_1				
6A	VREFB6AND_HPS	HPS_DDR					R18			HPS_DQS#_1	HPS_DQS#_1				
6A	VREFB6AND_HPS	HPS_DDR					U28			HPS_DQ_11	HPS_DQ_11				
6A	VREFB6AND_HPS	HPS_DDR					L26			HPS_DQ_9	HPS_DQ_9				
6A	VREFB6AND_HPS	HPS_DDR					J27			HPS_DQ_10	HPS_DQ_10				
6A	VREFB6AND_HPS	HPS_DDR					K25			HPS_DQ_8	HPS_DQ_8				
6A	VREFB6AND_HPS	HPS_GPI1					K27								
6A	VREFB6AND_HPS	HPS_GPI0					M25								
6A	VREFB6AND_HPS	HPS_DDR					G28			HPS_DM_0	HPS_DM_0				
6A	VREFB6AND_HPS	HPS_DDR					Z28			HPS_DQ_7	HPS_DQ_7				
6A	VREFB6AND_HPS	HPS_DDR					K26			HPS_DQ_5	HPS_DQ_5				
6A	VREFB6AND_HPS	HPS_DDR					S27			HPS_DQ_6	HPS_DQ_6				
6A	VREFB6AND_HPS	HPS_DDR					J26			HPS_DQ_4	HPS_DQ_4				
6A	VREFB6AND_HPS	HPS_DDR					G26			HPS_ODT_1	HPS_ODT_1				
6A	VREFB6AND_HPS	HPS_DDR					R17			HPS_DQS_0	HPS_DQS_0				
6A	VREFB6AND_HPS	HPS_DDR					Z28			HPS_ODT_0	HPS_ODT_0				
6A	VREFB6AND_HPS	HPS_DDR					R16			HPS_DQS#_0	HPS_DQS#_0				
6A	VREFB6AND_HPS	HPS_DDR					D27			HPS_DQ_3	HPS_DQ_3				
6A	VREFB6AND_HPS	HPS_DDR					J24			HPS_DQ_1	HPS_DQ_1				
6A	VREFB6AND_HPS	HPS_DDR					E28			HPS_DQ_2	HPS_DQ_2				
6A	VREFB6AND_HPS	HPS_DDR					J25			HPS_DQ_0	HPS_DQ_0				
6A	VREFB6AND_HPS	VREFB6AND_HPS					H28								
6A	VREFB6AND_HPS	HPS_DDR					C28			HPS_CA_0	HPS_CA_0				
6A	VREFB6AND_HPS	HPS_DDR					B28			HPS_CA_1	HPS_CA_1				
6A	VREFB6AND_HPS	HPS_DDR					J21			HPS_CA_4	HPS_CA_4				
6A	VREFB6AND_HPS	HPS_DDR					E26			HPS_CA_2	HPS_CA_2				
6A	VREFB6AND_HPS	HPS_DDR					L20			HPS_CA_5	HPS_CA_5				



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	MU2	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
6A	VREFB8A0_HPS	HPS_DDR					D26			HPS_A_3	HPS_CA_3				
6A	VREFB8A0_HPS	HPS_DDR					N21			HPS_CK	HPS_CK				
6A	VREFB8A0_HPS	HPS_DDR					C26			HPS_A_6	HPS_CA_6				
6A	VREFB8A0_HPS	HPS_DDR					N20			HPS_CK#	HPS_CK#				
6A	VREFB8A0_HPS	HPS_DDR					B26			HPS_A_7	HPS_CA_7				
6A	VREFB8A0_HPS	HPS_DDR					H25			HPS_BA_1					
6A	VREFB8A0_HPS	HPS_DDR					A27			HPS_BA_0					
6A	VREFB8A0_HPS	HPS_DDR					G25			HPS_BA_2					
6A	VREFB8A0_HPS	HPS_DDR					A26			HPS_CAS#					
6A	VREFB8A0_HPS	HPS_DDR					A25			HPS_RAS#					
6A	VREFB8A0_HPS	HPS_DDR					F26			HPS_A_8	HPS_CA_8				
6A	VREFB8A0_HPS	HPS_DDR					A24			HPS_A_10					
6A	VREFB8A0_HPS	HPS_DDR					F25			HPS_A_9	HPS_CA_9				
6A	VREFB8A0_HPS	HPS_DDR					B24			HPS_A_11					
6A	VREFB8A0_HPS	HPS_DDR					L21			HPS_CS#_0	HPS_CS#_0				
6A	VREFB8A0_HPS	HPS_DDR					D24			HPS_A_12					
6A	VREFB8A0_HPS	HPS_DDR					L20			HPS_CS#_1	HPS_CS#_1				
6A	VREFB8A0_HPS	HPS_DDR					C24			HPS_A_13					
6A	VREFB8A0_HPS	HPS_DDR					S23			HPS_A_14					
6A	VREFB8A0_HPS	HPS_DDR					E25			HPS_WIE#					
6A	VREFB8A0_HPS	HPS_DDR					F24			HPS_A_15					
6A	VREFB8A0_HPS	HPS_R2Q_0					D25								
		GND					F21								
		GND					E23								
7A		HPS_nRST					A23								
7A		HPS_nPOR					H19								
7A		HPS_TDO					B23								
		VCCRSTCLK_HPS					J19								
7A		HPS_TMS					C23								
7A		HPS_TCK					K19								
7A		HPS_TRST					C22								
7A		HPS_TDI					D22								
		GND					D21								
7A		HPS_PORSEL					E18								
7A		HPS_CLK1					E20								
7A		HPS_CLK2					D20								
7A	VREFB7A7B7C7D0_HPS	TRACE_CLK					C21					TRACE_CLK			HPS_GPIO48
7A	VREFB7A7B7C7D0_HPS	TRACE_D0					A22					TRACE_D0	SPIS0_CLK	UART0_RX	HPS_GPIO49
7A	VREFB7A7B7C7D0_HPS	TRACE_D1					B21					TRACE_D1	SPIS0_MOSI	UART0_TX	HPS_GPIO50
7A	VREFB7A7B7C7D0_HPS	TRACE_D2					A21					TRACE_D2	SPIS0_MISO	PC1_SDA	HPS_GPIO51
7A	VREFB7A7B7C7D0_HPS	TRACE_D3					K18					TRACE_D3	SPIS0_SS0	PC1_SCL	HPS_GPIO52
7A	VREFB7A7B7C7D0_HPS	TRACE_D4					A20					TRACE_D4	SPIS1_CLK	CAN1_RX	HPS_GPIO53
7A	VREFB7A7B7C7D0_HPS	TRACE_D5					J18					TRACE_D5	SPIS1_MOSI	CAN1_TX	HPS_GPIO54
7A	VREFB7A7B7C7D0_HPS	TRACE_D6					A19					TRACE_D6	SPIS1_SS0	PC0_SDA	HPS_GPIO55
7A	VREFB7A7B7C7D0_HPS	TRACE_D7					C18					TRACE_D7	SPIS1_MISO	PC0_SCL	HPS_GPIO56
7A	VREFB7A7B7C7D0_HPS	SPIM0_CLK					A18					SPIM0_CLK	PC1_SDA	UART0_CTS	HPS_GPIO57
7A	VREFB7A7B7C7D0_HPS	SPIM0_MOSI					C17					SPIM0_MOSI	PC1_SCL	UART0_RTS	HPS_GPIO58
7A	VREFB7A7B7C7D0_HPS	SPIM0_MISO					B18					SPIM0_MISO	CAN1_RX	UART1_CTS	HPS_GPIO59
7A	VREFB7A7B7C7D0_HPS	SPIM0_SS0					J17					SPIM0_SS0	CAN1_TX	UART1_RTS	HPS_GPIO60
7A	VREFB7A7B7C7D0_HPS	UART0_RX					A17					UART0_RX	CAN0_RX	SPIM0_SS1	HPS_GPIO61
7A	VREFB7A7B7C7D0_HPS	UART0_TX_CLKSEL1					H17					UART0_TX	CAN0_TX	SPIM1_SS1	HPS_GPIO62
7A	VREFB7A7B7C7D0_HPS	IC01_SDA					C19					IC01_SDA	UART1_RX	SPIM1_CLK	HPS_GPIO63
7A	VREFB7A7B7C7D0_HPS	IC01_SCL					B16					IC01_SCL	UART1_TX	SPIM1_MOSI	HPS_GPIO64
7A	VREFB7A7B7C7D0_HPS	CAN0_RX					B18					CAN0_RX	UART0_TX	SPIM1_MISO	HPS_GPIO65
7A	VREFB7A7B7C7D0_HPS	CAN0_TX_CLKSEL0					C16					CAN0_TX	UART0_TX	SPIM1_SS0	HPS_GPIO66
7B	VREFB7A7B7C7D0_HPS	NAND_ALE					J15					NAND_ALE	RGMI1_TX_CLK	GSPI_SS3	HPS_GPIO14
7B	VREFB7A7B7C7D0_HPS	NAND_CE					A16					NAND_CE	RGMI1_TXD0	USBI_D0	HPS_GPIO15
7B	VREFB7A7B7C7D0_HPS	NAND_CLE					J14					NAND_CLE	RGMI1_TXD1	USBI_D1	HPS_GPIO16
7B	VREFB7A7B7C7D0_HPS	NAND_RE					A15					NAND_RE	RGMI1_TXD2	USBI_D2	HPS_GPIO17
7B	VREFB7A7B7C7D0_HPS	NAND_RB					D17					NAND_RB	RGMI1_TXD3	USBI_D3	HPS_GPIO18
7B	VREFB7A7B7C7D0_HPS	NAND_DQ0					A14					NAND_DQ0	RGMI1_RXD0		HPS_GPIO19
7B	VREFB7A7B7C7D0_HPS	NAND_DQ1					E16					NAND_DQ1	RGMI1_MDIO	PC3_SDA	HPS_GPIO20
7B	VREFB7A7B7C7D0_HPS	NAND_DQ2					A13					NAND_DQ2	RGMI1_MDC	PC3_SCL	HPS_GPIO21
7B	VREFB7A7B7C7D0_HPS	NAND_DQ3					H13					NAND_DQ3	RGMI1_RX_CTL	USBI_D4	HPS_GPIO22
7B	VREFB7A7B7C7D0_HPS	NAND_DQ4					A12					NAND_DQ4	RGMI1_TX_CTL	USBI_D5	HPS_GPIO23
7B	VREFB7A7B7C7D0_HPS	NAND_DQ5					J12					NAND_DQ5	RGMI1_RX_CLK	USBI_D6	HPS_GPIO24
7B	VREFB7A7B7C7D0_HPS	NAND_DQ6					A11					NAND_DQ6	RGMI1_RXD1	USBI_D7	HPS_GPIO25
7B	VREFB7A7B7C7D0_HPS	NAND_DQ7					C15					NAND_DQ7	RGMI1_RXD2		HPS_GPIO26
7B	VREFB7A7B7C7D0_HPS	NAND_WP					A9					NAND_WP	RGMI1_RXD3	GSPI_SS2	HPS_GPIO27
7B	VREFB7A7B7C7D0_HPS	NAND_WE_BOOTSEL2					D15					NAND_WE	GSPI_SS1		HPS_GPIO28
7B	VREFB7A7B7C7D0_HPS	GSPI_IO0					A8					GSPI_IO0		USBI_CLK	HPS_GPIO29
7B	VREFB7A7B7C7D0_HPS	GSPI_IO1					H16					GSPI_IO1		USBI_STP	HPS_GPIO30
7B	VREFB7A7B7C7D0_HPS	GSPI_IO2					A7					GSPI_IO2		USBI_DR	HPS_GPIO31
7B	VREFB7A7B7C7D0_HPS	GSPI_IO3					J16					GSPI_IO3		USBI_NXT	HPS_GPIO32
7B	VREFB7A7B7C7D0_HPS	GSPI_SS0					A6					GSPI_SS0			HPS_GPIO33
7B	VREFB7A7B7C7D0_HPS	GSPI_CLK					C14					GSPI_CLK			HPS_GPIO34
7B	VREFB7A7B7C7D0_HPS	GSPI_SBI					B14					GSPI_SBI			HPS_GPIO35
7C	VREFB7A7B7C7D0_HPS	SDMMC_CMD					D14					SDMMC_CMD	USB0_D0		HPS_GPIO36
7C	VREFB7A7B7C7D0_HPS	SDMMC_PWREN					A5					SDMMC_PWREN	USB0_D1		HPS_GPIO37
7C	VREFB7A7B7C7D0_HPS	SDMMC_D0					C13					SDMMC_D0	USB0_D2		HPS_GPIO38
7C	VREFB7A7B7C7D0_HPS	SDMMC_D1					B6					SDMMC_D1	USB0_D3		HPS_GPIO39
7C	VREFB7A7B7C7D0_HPS	SDMMC_D4					H13					SDMMC_D4	USB0_D4		HPS_GPIO40
7C	VREFB7A7B7C7D0_HPS	SDMMC_D5					A4					SDMMC_D5	USB0_D5		HPS_GPIO41
7C	VREFB7A7B7C7D0_HPS	SDMMC_D6					H12					SDMMC_D6	USB0_D6		HPS_GPIO42
7C	VREFB7A7B7C7D0_HPS	SDMMC_D7					B4					SDMMC_D7	USB0_D7		HPS_GPIO43
7C	VREFB7A7B7C7D0_HPS	SDMMC_FB_CLK_IN					B12					SDMMC_FB_CLK_IN	USB0_CLK		HPS_GPIO44
7C	VREFB7A7B7C7D0_HPS	SDMMC_CLK_OUT					B6					SDMMC_CLK_OUT	USB0_STP		HPS_GPIO45
7C	VREFB7A7B7C7D0_HPS	SDMMC_D2					B11					SDMMC_D2	USB0_DP		HPS_GPIO46
7C	VREFB7A7B7C7D0_HPS	SDMMC_D3					B9					SDMMC_D3	USB0_NXT		HPS_GPIO47
7D	VREFB7A7B7C7D0_HPS	RGMI0_TX_CLK					E4					RGMI0_TX_CLK			HPS_GPIO0
7D	VREFB7A7B7C7D0_HPS	RGMI0_TXD0					C10					RGMI0_TXD0	USBI_D0		HPS_GPIO1
7D	VREFB7A7B7C7D0_HPS	RGMI0_TXD1					F5					RGMI0_TXD1	USBI_D1		HPS_GPIO2
7D	VREFB7A7B7C7D0_HPS	RGMI0_TXD2					C9					RGMI0_TXD2	USBI_D2		HPS_GPIO3
7D	VREFB7A7B7C7D0_HPS	RGMI0_TXD3					C4					RGMI0_TXD3	USBI_D3		HPS_GPIO4
7D	VREFB7A7B7C7D0_HPS	RGMI0_RXD0					C8					RGMI0_RXD0	USBI_D4		HPS_GPIO5
7D	VREFB7A7B7C7D0_HPS	RGMI0_MDIO					D4					RGMI0_MDIO	USBI_D5	PC2_SDA	HPS_GPIO6
7D	VREFB7A7B7C7D0_HPS	RGMI0_MDC					C7					RGMI0_MDC	USBI_D6	PC2_SCL	HPS_GPIO7
7D	VREFB7A7B7C7D0_HPS	RGMI0_RX_CTL					F4					RGMI0_RX_CTL	USBI_D7		HPS_GPIO8
7D	VREFB7A7B7C7D0_HPS	RGMI0_TX_CTL					C6					RGMI0_TX_CTL			HPS_GPIO9
7D	VREFB7A7B7C7D0_HPS	RGMI0_RX_CLK					G4					RGMI0_RX_CLK	USBI_CLK		HPS_GPIO10
7D	VREFB7A7B7C7D0_HPS	RGMI0_RXD1					C2					RGMI0_RXD1	USBI_STP		HPS_GPIO11
7D	VREFB7A7B7C7D0_HPS	RGMI0_RXD2					E5					RGMI0_RXD2	USBI_DR		HPS_GPIO12
7D	VREFB7A7B7C7D0_HPS	RGMI0_RXD3					D5					RGMI0_RXD3	USBI_NXT		HPS_GPIO13
8A	VREFB8A0	IO				CLK0p		DIFF0_RX_T1p	DIFFOUT_T1p						
8A	VREFB8A0	IO				CLK0n		DIFF0_RX_T1n	DIFFOUT_T1n						
8A	VREFB8A0	IO				FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFF0_TX_T4p	DIFFOUT_T4p						
8A	VREFB8A0	IO				FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFF0_TX_T4n	DIFFOUT_T4n						
8A	VREFB8A0	IO				CLK0a,FPLL_TL_FBp		DIFF0_RX_T9p	DIFFOUT_T9p						
8A	VREFB8A0	IO				CLK0a,FPLL_TL_FBn		DIFF0_RX_T9n	DIFFOUT_T9n						
8A		MSEL0													
8A		CONF_DONE													
8A		MSEL1													
8A		nSTATUS													
8A		nCE													
8A		MSEL2													



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
9A		MSEL3		MSEL3			K10								
9A		KCONFIG		KCONFIG			F7								
9A		MSEL4		MSEL4			K9								
		GND					F6								
		GND					N8								
		GND					P9								
		GND					F2								
		GND					F1								
		GND					K2								
		GND					K1								
		GND					P2								
		GND					P1								
		GND					V2								
		GND					V1								
		GND					AB2								
		GND					AB1								
		GND					AF2								
		GND					AF1								
		GND					V5								
		GND					V4								
		GND					A10								
		GND					A3								
		GND					AA1								
		GND					AA17								
		GND					AA2								
		GND					AA3								
		GND					AA9								
		GND					AB24								
		GND					AB27								
		GND					AB3								
		GND					AC1								
		GND					AC2								
		GND					AC3								
		GND					AD14								
		GND					AD22								
		GND					AD26								
		GND					AD3								
		GND					AD6								
		GND					AD8								
		GND					AE1								
		GND					AE16								
		GND					AE18								
		GND					AE2								
		GND					AE3								
		GND					AF24								
		GND					AF3								
		GND					AG1								
		GND					AG17								
		GND					AG2								
		GND					AG27								
		GND					AG3								
		GND					AG7								
		GND					AH10								
		GND					AH20								
		GND					B15								
		GND					B17								
		GND					B20								
		GND					B22								
		GND					B26								
		GND					B29								
		GND					B3								
		GND					B5								
		GND					B7								
		GND					C1								
		GND					C11								
		GND					C2								
		GND					C3								
		GND					D10								
		GND					D13								
		GND					D16								
		GND					D3								
		GND					E1								
		GND					E19								
		GND					E2								
		GND					E22								
		GND					E24								
		GND					E27								
		GND					E3								
		GND					E9								
		GND					F3								
		GND					G1								
		GND					G2								
		GND					G3								
		GND					H11								
		GND					H15								
		GND					H18								
		GND					H20								
		GND					H24								
		GND					H27								
		GND					H3								
		GND					H4								
		GND					H5								
		GND					H6								
		GND					H								
		GND					J2								
		GND					J3								
		GND					J5								
		GND					J9								
		GND					K11								
		GND					K12								
		GND					K14								
		GND					K16								
		GND					K20								
		GND					K3								
		GND					K4								
		GND					K8								
		GND					L1								
		GND					L10								
		GND					L13								
		GND					L15								
		GND					L17								
		GND					L19								
		GND					L2								
		GND					L24								
		GND					L27								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					L3								
		GND					L5								
		GND					L8								
		GND					L9								
		GND					M10								
		GND					M11								
		GND					M14								
		GND					M16								
		GND					M20								
		GND					M3								
		GND					M8								
		GND					N1								
		GND					N13								
		GND					N15								
		GND					N17								
		GND					N19								
		GND					N2								
		GND					N3								
		GND					N4								
		GND					P10								
		GND					P12								
		GND					P16								
		GND					P18								
		GND					P20								
		GND					P25								
		GND					P3								
		GND					P5								
		GND					P9								
		GND					R1								
		GND					R11								
		GND					R13								
		GND					R15								
		GND					R2								
		GND					R3								
		GND					R8								
		GND					T10								
		GND					T14								
		GND					T3								
		GND					U1								
		GND					U12								
		GND					U20								
		GND					U24								
		GND					U27								
		GND					U3								
		GND					U5								
		GND					V14								
		GND					V3								
		GND					V8								
		GND					V9								
		GND					W1								
		GND					W16								
		GND					W18								
		GND					W2								
		GND					W3								
		GND					W4								
		GND					Y12								
		GND					Y14								
		GND					Y20								
		GND					Y25								
		GND					Y3								
		GND					V26								
		GND					V21								
		VCC					J11								
		VCC					K13								
		VCC					K15								
		VCC					L11								
		VCC					L12								
		VCC					L14								
		VCC					M12								
		VCC					M13								
		VCC					M15								
		VCC					M9								
		VCC					N10								
		VCC					N11								
		VCC					N12								
		VCC					N14								
		VCC					N9								
		VCC					P11								
		VCC					P13								
		VCC					P14								
		VCC					P15								
		VCC					R10								
		VCC					R12								
		VCC					R14								
		VCC					R9								
		VCC					T15								
		VCC					T9								
		VCC					U4								
		VCC					U4								
		VCC					M5								
		VCC					N5								
		VCC					N5								
		VCC					T5								
		VCC					U26								
		DNLU					A2								
		DNLU					B2								
		DNLU					D1								
		DNLU					D2								
		DNLU					H1								
		DNLU					H2								
		DNLU					M1								
		DNLU					M2								
		DNLU					T1								
		DNLU					T2								
		DNLU					V1								
		DNLU					V2								
		DNLU					AD1								
		DNLU					AD2								
		DNLU					L8								
		DNLU					AE14								
		DNLU					D23								
		DNLU					E12								
		VCCPGM					F10								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M72	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0	
		VCCPQM					AD24									
		VCCPQM					H10									
		VCCBAT					D7									
		VCCIOA					AA5									
		VCCIOA					W9									
		VCCIOB					AA12									
		VCCIOB					AE10									
		VCCIOB					AE13									
		VCCIOB					AS4									
		VCCIOA					AA16									
		VCCIOA					AE21									
		VCCIOA					AF14									
		VCCIOA					AF19									
		VCCIOA					AG12									
		VCCIOA					AG22									
		VCCIOA					AH16									
		VCCIOA					AH25									
		VCCIOA					W13									
		VCCIOA					HC26									
		VCCIOA					W17									
		VCCIOB					W26									
		VCCIOA_HPS					C26									
		VCCIOA_HPS					C27									
		VCCIOA_HPS					F27									
		VCCIOA_HPS					G24									
		VCCIOA_HPS					H21									
		VCCIOA_HPS					H26									
		VCCIOA_HPS					L26									
		VCCIOA_HPS					M21									
		VCCIOB_HPS					AD27									
		VCCIOB_HPS					P27									
		VCCIOB_HPS					T21									
		VCCIOB_HPS					T26									
		VCCIOB_HPS					U18									
		VCCIOB_HPS					W27									
		VCCIO7A_HPS					C20									
		VCCIO7A_HPS					D18									
		VCCIO7B_HPS					B13									
		VCCIO7B_HPS					H14									
		VCCIO7C_HPS					B10									
		VCCIO7D_HPS					D6									
		VCCIO7D_HPS					G6									
		VCCIO8A					E7									
		VCCPD3A					AA10									
		VCCPD3B4A					AA14									
		VCCPD3B4A					AD13									
		VCCPD3B4A					AD16									
		VCCPD3B4A					AD18									
		VCCPD3B4A					AD21									
		VCCPD3B4A					AD9									
		VCCPD6A					Y21									
		VCCPD6B					W19									
		VCCPD6A6B_HPS					M21									
		VCCPD6A6B_HPS					M24									
		VCCPD6A6B_HPS					M24									
		VCCPD6A6B_HPS					P21									
		VCCPD6A6B_HPS					P24									
		VCCPD7A_HPS					E21									
		VCCPD7B_HPS					E17									
		VCCPD7C_HPS					E14									
		VCCPD7D_HPS					E13									
		VCCPD8A					E10									
3A	VREFB3A0	VREFB3A0					AE5									
3B	VREFB3B0	VREFB3B0					AF22									
4A	VREFB4A0	VREFB4A0					AF16									
5A	VREFB5A0	VREFB5A0					AC26									
5B	VREFB5B0	VREFB5B0					AA26									
	VREFB7A7B7C7D0_HPS	VREFB7A7B7C7D0_HPS					D19									
8A	VREFB8A0	VREFB8A0					D9									
	VCCRS1CLK_HPS						P22									
	VREF_TL						B1									
	VCCA_FPLL						K5									
	VCCA_FPLL						P4									
	VCCA_FPLL						U4									
	VCCA_FPLL						W5									
	VCCA_FPLL						J4									
	VCCA_FPLL						AA21									
	VCCA_FPLL						M4									
	VCCA_FPLL						R4									
	VCC_AUX						AC21									
	VCC_AUX						AC8									
	VCC_AUX						AD15									
	VCC_AUX						E15									
	VCC_AUX						F8									
	VCC_AUX_SHARED						F21									
	VCCPLL_HPS						H23									
	VCC_HPS						U21									
	VCC_HPS						N17									
	VCC_HPS						L16									
	VCC_HPS						L18									
	VCC_HPS						M17									
	VCC_HPS						M18									
	VCC_HPS						M19									
	VCC_HPS						M16									
	VCC_HPS						N15									
	VCC_HPS						P17									
	VCC_HPS						P19									

Notes:
 (1) For more information about pin definitions and pin connection guidelines, refer to the [Cyclone V Device Family Pin Connection Guidelines](#).
 (2) HPS_DDR pins are for memory interface only. For the dedicated pin function corresponding with the respective memory interfaces, refer to the HMC columns.
 (3) RESET pin is only applicable for DDR3 devices.



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
3A		TDO		TDO			AB9								
3A		HC30		DATA4			AB8								
3A		TMS		TMS			V9								
3A		AS_DATA3		DATA3			AC7								
3A		TCK		TCK			AC5								
3A		AS_DATA2		DATA2			AE8								
3A		TDI		TDI			U8								
3A		AS_DATA1		DATA1			AE5								
3A		CLKX		CLKX			U7								
3A		AS_DATA0,ASD0		DATA0			AE6								
3A	VREFB3AND	IO		DATA6	DIFFD_RX_B1n	DIFFOUT_B1n	AE12	DQ1B							
3A	VREFB3AND	IO		DATA5	DIFFD_RX_B2n	DIFFOUT_B2n	AE9	DQ1B							
3A	VREFB3AND	IO		DATA8	DIFFD_RX_B1p	DIFFOUT_B1p	AD11	DQ1B							
3A	VREFB3AND	IO		DATA7	DIFFD_TX_B2p	DIFFOUT_B2p	AD9	DQ1B							
3A	VREFB3AND	IO		DATA10	DIFFD_RX_B3n	DIFFOUT_B3n	AD10	DQS#1B							
3A	VREFB3AND	IO		DATA9	DIFFD_TX_B2n	DIFFOUT_B2n	AD10	DQ1B							
3A	VREFB3AND	IO		DATA12	DIFFD_RX_B3p	DIFFOUT_B3p	AC3	DQS1B							
3A	VREFB3AND	IO		DATA11	DIFFD_TX_B4p	DIFFOUT_B4p	AE11	DQ1B							
3A	VREFB3AND	IO		DATA14	DIFFD_RX_B5n	DIFFOUT_B5n	AE7	DQ1B							
3A	VREFB3AND	IO		DATA13	DIFFD_TX_B6p	DIFFOUT_B6p	AH4	DQ1B							
3A	VREFB3AND	IO		CLKUSR	DIFFD_RX_B5p	DIFFOUT_B5p	AD7	DQ1B							
3A	VREFB3AND	IO		DATA15	DIFFD_TX_B6p	DIFFOUT_B6p	AG3	DQ1B							
3A	VREFB3AND	IO		PR_DONE	DIFFD_RX_B7n	DIFFOUT_B7n	AK9	DQ1B							
3A	VREFB3AND	IO		PR_READY	DIFFD_TX_B8n	DIFFOUT_B8n	AG8	DQ1B							
3A	VREFB3AND	IO		PR_ERROR	DIFFD_RX_B7p	DIFFOUT_B7p	AF4	DQ1B							
3A	VREFB3AND	IO			DIFFD_TX_B8p	DIFFOUT_B8p	AK9	DQ1B							
3A	VREFB3AND	IO			DIFFD_TX_B9n	DIFFOUT_B9n	AG7	DQ2B							
3A	VREFB3AND	IO			DIFFD_RX_B10n	DIFFOUT_B10n	AH2	DQ2B							
3A	VREFB3AND	IO			DIFFD_TX_B9p	DIFFOUT_B9p	AF8	DQ2B							
3A	VREFB3AND	IO			DIFFD_RX_B10p	DIFFOUT_B10p	AG1	DQ2B							
3A	VREFB3AND	IO			DIFFD_RX_B11n	DIFFOUT_B11n	AB12	DQS#2B							
3A	VREFB3AND	IO			DIFFD_TX_B12n	DIFFOUT_B12n	AG6	DQ2B							
3A	VREFB3AND	IO			DIFFD_RX_B11p	DIFFOUT_B11p	AA12	DQS#2B							
3A	VREFB3AND	IO			DIFFD_TX_B12p	DIFFOUT_B12p	AF6	DQ2B							
3A	VREFB3AND	IO			DIFFD_TX_B13n	DIFFOUT_B13n	AH5	DQ2B							
3A	VREFB3AND	IO			DIFFD_RX_B14n	DIFFOUT_B14n	AJ2	DQ2B							
3A	VREFB3AND	IO			DIFFD_TX_B13p	DIFFOUT_B13p	AG8	DQ2B							
3A	VREFB3AND	IO			DIFFD_RX_B14p	DIFFOUT_B14p	AJ1	DQ2B							
3A	VREFB3AND	IO			DIFFD_RX_B15n	DIFFOUT_B15n	AD12	DQ2B							
3A	VREFB3AND	IO			DIFFD_TX_B16n	DIFFOUT_B16n	AK9	DQ2B							
3A	VREFB3AND	IO			DIFFD_RX_B15p	DIFFOUT_B15p	AC12	DQ2B							
3A	VREFB3AND	IO			DIFFD_TX_B16p	DIFFOUT_B16p	AG2	DQ2B							
3B	VREFB3AND	IO			DIFFD_TX_B17n	DIFFOUT_B17n	AH8	DQ1B							
3B	VREFB3AND	IO			DIFFD_RX_B18n	DIFFOUT_B18n	AG11	DQ3B	DQ1B						
3B	VREFB3AND	IO			DIFFD_TX_B17p	DIFFOUT_B17p	AG10	DQ3B	DQ1B						
3B	VREFB3AND	IO			DIFFD_RX_B18p	DIFFOUT_B18p	AF11	DQ3B	DQ1B						
3B	VREFB3AND	IO			DIFFD_RX_B19n	DIFFOUT_B19n	AB13	DQS#3B	DQ1B						
3B	VREFB3AND	IO			DIFFD_TX_B20n	DIFFOUT_B20n	AK3	DQ3B	DQ1B						
3B	VREFB3AND	IO			DIFFD_RX_B19p	DIFFOUT_B19p	AA13	DQS#3B	DQ1B						
3B	VREFB3AND	IO			DIFFD_TX_B20p	DIFFOUT_B20p	AK4	DQ3B	DQ1B						
3B	VREFB3AND	IO			DIFFD_RX_B22n	DIFFOUT_B22n	AF13	DQ3B	DQ1B						
3B	VREFB3AND	IO			DIFFD_TX_B21n	DIFFOUT_B21n	AJ4	DQ3B	DQ1B						
3B	VREFB3AND	IO			DIFFD_RX_B21p	DIFFOUT_B21p	AE13	DQ3B	DQ1B						
3B	VREFB3AND	IO			DIFFD_RX_B23n	DIFFOUT_B23n	AE14	DQ3B	DQ1B						
3B	VREFB3AND	IO			DIFFD_TX_B24n	DIFFOUT_B24n	AK6	DQ3B	DQ1B						
3B	VREFB3AND	IO			DIFFD_RX_B23p	DIFFOUT_B23p	AD14	DQ3B	DQ1B						
3B	VREFB3AND	IO			DIFFD_TX_B24p	DIFFOUT_B24p	AJ5	DQ3B	DQ1B						
3B	VREFB3AND	IO			DIFFD_TX_B25n	DIFFOUT_B25n	AJ7	DQ4B	DQ1B	GND	GND				
3B	VREFB3AND	IO			DIFFD_RX_B26n	DIFFOUT_B26n	AG13	DQ4B	DQ1B	B_A_15					
3B	VREFB3AND	IO			DIFFD_TX_B25p	DIFFOUT_B25p	AJ6	DQ4B	DQ1B	B_WE#					
3B	VREFB3AND	IO			DIFFD_RX_B26p	DIFFOUT_B26p	AG12	DQ4B	DQ1B	B_A_14					
3B	VREFB3AND	IO			DIFFD_RX_B27n	DIFFOUT_B27n	AC14	DQS#4B	DQ1B	B_CS#_1	B_CS#_1				
3B	VREFB3AND	IO			DIFFD_TX_B28n	DIFFOUT_B28n	AG8	DQ4B	DQ1B	B_A_13					
3B	VREFB3AND	IO			DIFFD_RX_B27p	DIFFOUT_B27p	AB15	DQS#4B	DQ1B	B_CS#_0	B_CS#_0				
3B	VREFB3AND	IO			DIFFD_TX_B28p	DIFFOUT_B28p	AK7	DQ4B	DQ1B	B_A_12					
3B	VREFB3AND	IO			DIFFD_TX_B29n	DIFFOUT_B29n	AK9	DQ4B	DQ1B	B_A_11					
3B	VREFB3AND	IO			DIFFD_RX_B30n	DIFFOUT_B30n	AH14	DQ4B	DQ1B	B_A_9	B_CA_9				
3B	VREFB3AND	IO			DIFFD_TX_B29p	DIFFOUT_B29p	AJ9	DQ4B	DQ1B	B_A_10					
3B	VREFB3AND	IO			DIFFD_RX_B30p	DIFFOUT_B30p	AH13	DQ4B	DQ1B	B_A_8	B_CA_8				
3B	VREFB3AND	IO	CLK0n,FPLL_BL_FBn		DIFFD_TX_B32n	DIFFOUT_B32n	AH8	DQ4B	DQ1B	B_RAS#					
3B	VREFB3AND	IO	CLK0p,FPLL_BL_F#p		DIFFD_RX_B31p	DIFFOUT_B31p	AF14	DQ4B	DQ1B	B_CAS#					
3B	VREFB3AND	IO			DIFFD_TX_B32p	DIFFOUT_B32p	AH7	DQ4B	DQ1B	GND	GND				
3B	VREFB3AND	IO			DIFFD_TX_B33n	DIFFOUT_B33n	AJ10	DQ4B	DQ1B	B_CK#					
3B	VREFB3AND	IO			DIFFD_RX_B34n	DIFFOUT_B34n	AK11	DQ5B	DQ1B	B_BA_2					
3B	VREFB3AND	IO			DIFFD_TX_B33p	DIFFOUT_B33p	AH10	DQ5B	DQ1B	B_BA_0					
3B	VREFB3AND	IO			DIFFD_RX_B34p	DIFFOUT_B34p	AJ11	DQ5B	DQ1B	B_BA_1					
3B	VREFB3AND	IO			DIFFD_RX_B35n	DIFFOUT_B35n	AA15	DQS#5B	DQ1B	B_CK#	B_CK#				
3B	VREFB3AND	IO			DIFFD_TX_B36n	DIFFOUT_B36n	AK13	DQ5B	DQ1B	B_A_7	B_CS#_7				
3B	VREFB3AND	IO			DIFFD_RX_B35p	DIFFOUT_B35p	AH14	DQS#5B	DQ1B	B_CK#	B_CK#				
3B	VREFB3AND	IO			DIFFD_TX_B36p	DIFFOUT_B36p	AK12	DQ5B	DQ1B	B_A_6	B_CA_6				
3B	VREFB3AND	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFD_TX_B37n	DIFFOUT_B37n	AJ12	DQ5B	DQ1B	B_A_3	B_CA_3				
3B	VREFB3AND	IO			DIFFD_RX_B38n	DIFFOUT_B38n	AH15	DQ5B	DQ1B	B_A_5	B_CS#_5				
3B	VREFB3AND	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFD_TX_B37p	DIFFOUT_B37p	AH12	DQ5B	DQ1B	B_A_2	B_CA_2				
3B	VREFB3AND	IO			DIFFD_RX_B38p	DIFFOUT_B38p	AG15	DQ5B	DQ1B	B_A_4	B_CA_4				
3B	VREFB3AND	IO	CLK1n		DIFFD_RX_B39n	DIFFOUT_B39n	W16	DQ5B	DQ1B	B_A_1					
3B	VREFB3AND	IO	CLK1p		DIFFD_TX_B40n	DIFFOUT_B40n	AK14	DQ5B	DQ1B	B_CA_1					
3B	VREFB3AND	IO			DIFFD_RX_B39p	DIFFOUT_B39p	W15	DQ5B	DQ1B						
3B	VREFB3AND	IO			DIFFD_TX_B40p	DIFFOUT_B40p	AJ14	DQ5B	DQ1B	B_A_0	B_CA_0				
4A	VREFB4AND	IO	RZQ_0		DIFFD_RX_B42n	DIFFOUT_B42n	AF18	DQ6B	DQ2B	B_DQ_0					
4A	VREFB4AND	IO			DIFFD_TX_B41p	DIFFOUT_B41p	AG16	DQ6B	DQ2B	B_DQ_2					
4A	VREFB4AND	IO			DIFFD_RX_B42p	DIFFOUT_B42p	AE17	DQ6B	DQ2B	B_DQ_1					
4A	VREFB4AND	IO			DIFFD_TX_B43n	DIFFOUT_B43n	W16	DQS#6B	DQ2B	B_DQS#_0					
4A	VREFB4AND	IO			DIFFD_RX_B44n	DIFFOUT_B44n	AF16	DQ6B	DQ2B	B_DQ_3	B_DQ_3				
4A	VREFB4AND	IO			DIFFD_TX_B43p	DIFFOUT_B43p	V16	DQS#6B	DQ2B	B_DQS_0					
4A	VREFB4AND	IO			DIFFD_TX_B44p	DIFFOUT_B44p	AE16	DQ6B	DQ2B	B_ODT_0					
4A	VREFB4AND	IO			DIFFD_RX_B45n	DIFFOUT_B45n	AK16	DQ6B	DQ2B	B_ODT_1	B_ODT_1				
4A	VREFB4AND	IO			DIFFD_RX_B46n	DIFFOUT_B46n	AH20	DQ6B	DQ2B	B_DQ_4	B_DQ_4				
4A	VREFB4AND	IO			DIFFD_TX_B45p	DIFFOUT_B45p	AJ16	DQ6B	DQ2B	B_DQ_5	B_DQ_5				
4A	VREFB4AND	IO			DIFFD_RX_B46p	DIFFOUT_B46p	AG21	DQ6B	DQ2B	B_DQ_5	B_DQ_5				
4A	VREFB4AND	IO	CLK2n		DIFFD_RX_B47n	DIFFOUT_B47n	AB17	DQ6B	DQ2B	B_DQ_7	B_DQ_7				
4A	VREFB4AND	IO			DIFFD_TX_B48n	DIFFOUT_B48n	AH18	DQ6B	DQ2B	B_DM_7	B_DM_7				
4A	VREFB4AND	IO	CLK2p		DIFFD_RX_B47p	DIFFOUT_B47p	AA16	DQ6B	DQ2B	B_DM_0					
4A	VREFB4AND	IO			DIFFD_TX_B48p	DIFFOUT_B48p	AH17	DQ6B	DQ2B	B_DM_0					
4A	VREFB4AND	IO			DIFFD_TX_B49n	DIFFOUT_B49n	AH19	DQ6B	DQ2B	GND	GND				
4A	VREFB4AND	IO			DIFFD_RX_B50n	DIFFOUT_B50n	AK17	DQ7B	DQ2B	B_DQ_8					
4A	VREFB4AND	IO			DIFFD_TX_B49p	DIFFOUT_B49p	AG18	DQ7B	DQ2B	B_DQ_10					
4A	VREFB4AND	IO			DIFFD_RX_B50p	DIFFOUT_B50p	AJ17	DQ7B	DQ2B	B_DQ_9	B_DQ_9				
4A	VREFB4AND	IO			DIFFD_RX_B51n	DIFFOUT_B51n	V17	DQS#7B	DQ2B	B_DQS#_1					
4A	VREFB4AND	IO			DIFFD_TX_B52n	DIFFOUT_B52n	AK19	DQ7B	DQ2B	B_DQ_11	B_DQ_11				
4A	VREFB4AND	IO			DIFFD_RX_B51p	DIFFOUT_B51p	V17	DQS#7B	DQ2B	B_DQS_1	B_DQS_1				
4A	VREFB4AND	IO			DIFFD_TX_B52p	DIFFOUT_B52p	AJ19	DQ7B	DQ2B	B_CKE_1	B_CKE_1				
4A	VREFB4AND	IO			DIFFD_TX_B53n	DIFFOUT_B53n	AC15	DQ7B	DQ2B	B_CKE_0	B_CKE_0				



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for D0R3/D0R2 (2)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
4A	VREFB4ND	IO			DIFFD_RX_B54n	DIFFOUT_B54n	AQ20	DQ7B	DQ2B		B_DQ_12				
4A	VREFB4ND	IO			DIFFD_TX_B53p	DIFFOUT_B53p	AJ20	DQ7B	DQ2B	B_DQ_14	B_DQ_14				
4A	VREFB4ND	IO			DIFFD_RX_B54p	DIFFOUT_B54p	AF17	DQ7B	DQ2B		B_DQ_13				
4A	VREFB4ND	IO	CLK3n		DIFFD_RX_B55n	DIFFOUT_B55n	AD17								
4A	VREFB4ND	IO			DIFFD_TX_B55n	DIFFOUT_B55n	AH24	DQ7B	DQ2B	B_DQ_15	B_DQ_15				
4A	VREFB4ND	IO	CLK3p		DIFFD_TX_B55p	DIFFOUT_B55p	AC18								
4A	VREFB4ND	IO			DIFFD_TX_B56p	DIFFOUT_B56p	AG23	DQ7B	DQ2B		B_DM_1				
4A	VREFB4ND	IO			DIFFD_TX_B57n	DIFFOUT_B57n	AH22			GND	GND				
4A	VREFB4ND	IO			DIFFD_RX_B58n	DIFFOUT_B58n	AE19	DQ8B	DQ2B	B_DQ_16	B_DQ_16				
4A	VREFB4ND	IO			DIFFD_TX_B57p	DIFFOUT_B57p	AG22	DQ8B	DQ2B	B_DQ_18	B_DQ_18				
4A	VREFB4ND	IO			DIFFD_RX_B58p	DIFFOUT_B58p	AE18	DQ8B	DQ2B	B_DQ_17	B_DQ_17				
4A	VREFB4ND	IO			DIFFD_RX_B59n	DIFFOUT_B59n	AA18	DQS#8B	DQS#2B	B_DQS_2	B_DQS_2				
4A	VREFB4ND	IO			DIFFD_TX_B60n	DIFFOUT_B60n	AQ22	DQ8B	DQ2B	B_DQ_19	B_DQ_19				
4A	VREFB4ND	IO			DIFFD_RX_B59p	DIFFOUT_B59p	Y17	DQS#8B	DQS#2B	B_DQS_2	B_DQS_2				
4A	VREFB4ND	IO			DIFFD_TX_B60p	DIFFOUT_B60p	AK21	DQ8B	DQ2B	GND	B_RESET#	B_RESET#			
4A	VREFB4ND	IO			DIFFD_RX_B62n	DIFFOUT_B62n	AF21	DQ8B	DQ2B	B_DQ_20	B_DQ_20				
4A	VREFB4ND	IO			DIFFD_TX_B61p	DIFFOUT_B61p	AH23	DQ8B	DQ2B	B_DQ_22	B_DQ_22				
4A	VREFB4ND	IO			DIFFD_RX_B62p	DIFFOUT_B62p	AF20	DQ8B	DQ2B	B_DQ_21	B_DQ_21				
4A	VREFB4ND	IO			DIFFD_RX_B63n	DIFFOUT_B63n	AA19			GND	GND				
4A	VREFB4ND	IO			DIFFD_TX_B64n	DIFFOUT_B64n	AK24	DQ8B	DQ2B	B_DQ_23	B_DQ_23				
4A	VREFB4ND	IO			DIFFD_RX_B63p	DIFFOUT_B63p	Y18			GND	GND				
4A	VREFB4ND	IO			DIFFD_TX_B64p	DIFFOUT_B64p	AQ23	DQ8B	DQ2B	B_DM_2	B_DM_2				
4A	VREFB4ND	IO			DIFFD_TX_B65n	DIFFOUT_B65n	AJ25			GND	GND				
4A	VREFB4ND	IO			DIFFD_RX_B66n	DIFFOUT_B66n	AF24	DQ9B	DQ3B	B_DQ_24	B_DQ_24				
4A	VREFB4ND	IO			DIFFD_TX_B65p	DIFFOUT_B65p	AJ24	DQ9B	DQ3B	B_DQ_26	B_DQ_26				
4A	VREFB4ND	IO			DIFFD_RX_B66p	DIFFOUT_B66p	AF23	DQ9B	DQ3B	B_DQ_25	B_DQ_25				
4A	VREFB4ND	IO			DIFFD_RX_B67n	DIFFOUT_B67n	AD19	DQS#9B	DQS#3B	B_DQS#_3	B_DQS#_3				
4A	VREFB4ND	IO			DIFFD_TX_B68n	DIFFOUT_B68n	AK26	DQ9B	DQ3B	B_DQ_27	B_DQ_27				
4A	VREFB4ND	IO			DIFFD_RX_B67p	DIFFOUT_B67p	AC27	DQS#9B	DQS#3B	B_DQS_3	B_DQS_3				
4A	VREFB4ND	IO			DIFFD_TX_B68p	DIFFOUT_B68p	AJ26			GND	GND				
4A	VREFB4ND	IO			DIFFD_TX_B69n	DIFFOUT_B69n	AH25	DQ9B	DQ3B	GND	GND				
4A	VREFB4ND	IO			DIFFD_RX_B70n	DIFFOUT_B70n	AE21	DQ9B	DQ3B	B_DQ_28	B_DQ_28				
4A	VREFB4ND	IO			DIFFD_TX_B69p	DIFFOUT_B69p	AG25	DQ9B	DQ3B	B_DQ_30	B_DQ_30				
4A	VREFB4ND	IO			DIFFD_RX_B70p	DIFFOUT_B70p	AE22	DQ9B	DQ3B	B_DQ_29	B_DQ_29				
4A	VREFB4ND	IO			DIFFD_RX_B71n	DIFFOUT_B71n	V19			GND	GND				
4A	VREFB4ND	IO			DIFFD_TX_B72n	DIFFOUT_B72n	AK27	DQ9B	DQ3B	B_DQ_31	B_DQ_31				
4A	VREFB4ND	IO			DIFFD_RX_B71p	DIFFOUT_B71p	V18			GND	GND				
4A	VREFB4ND	IO			DIFFD_TX_B72p	DIFFOUT_B72p	AJ27	DQ9B	DQ3B	B_DM_3	B_DM_3				
4A	VREFB4ND	IO			DIFFD_RX_B74n	DIFFOUT_B74n	AD21	DQ10B	DQ3B	GND	GND				
4A	VREFB4ND	IO			DIFFD_TX_B73p	DIFFOUT_B73p	AK28	DQ10B	DQ3B	B_DQ_32	B_DQ_32				
4A	VREFB4ND	IO			DIFFD_RX_B74p	DIFFOUT_B74p	AD20	DQ10B	DQ3B	B_DQ_34	B_DQ_34				
4A	VREFB4ND	IO			DIFFD_RX_B75n	DIFFOUT_B75n	AA20	DQS#10B	DQS#3B	B_DQS#_4	B_DQS#_4				
4A	VREFB4ND	IO			DIFFD_TX_B76n	DIFFOUT_B76n	AH27	DQ10B	DQ3B	B_DQ_35	B_DQ_35				
4A	VREFB4ND	IO			DIFFD_RX_B75p	DIFFOUT_B75p	Y19	DQS#10B	DQS#3B	B_DQS_4	B_DQS_4				
4A	VREFB4ND	IO			DIFFD_TX_B76p	DIFFOUT_B76p	AQ28			GND	GND				
4A	VREFB4ND	IO			DIFFD_TX_B77n	DIFFOUT_B77n	AF26	DQ10B	DQ3B	GND	GND				
4A	VREFB4ND	IO			DIFFD_RX_B78n	DIFFOUT_B78n	AC23	DQ10B	DQ3B	B_DQ_36	B_DQ_36				
4A	VREFB4ND	IO			DIFFD_TX_B77p	DIFFOUT_B77p	AF25	DQ10B	DQ3B	B_DQ_38	B_DQ_38				
4A	VREFB4ND	IO			DIFFD_RX_B78p	DIFFOUT_B78p	AC22	DQ10B	DQ3B	B_DQ_37	B_DQ_37				
4A	VREFB4ND	IO			DIFFD_RX_B79n	DIFFOUT_B79n	AB21			GND	GND				
4A	VREFB4ND	IO			DIFFD_TX_B80n	DIFFOUT_B80n	AH24	DQ10B	DQ3B	B_DQ_39	B_DQ_39				
4A	VREFB4ND	IO			DIFFD_RX_B79p	DIFFOUT_B79p	AA21			GND	GND				
4A	VREFB4ND	IO			DIFFD_TX_B80p	DIFFOUT_B80p	AD24	DQ10B	DQ3B	B_DM_4	B_DM_4				
5A	VREFB5ND	IO	R20_1		DIFFD_TX_R1p	DIFFOUT_R1p	AG27	DQ1R							
5A	VREFB5ND	IO		INT_DONE	DIFFD_RX_R2n	DIFFOUT_R2n	AD25								
5A	VREFB5ND	IO		PR_REQUEST	DIFFD_TX_R1n	DIFFOUT_R1n	AH28	DQ1R							
5A	VREFB5ND	IO		CRC_ERROR	DIFFD_RX_R2n	DIFFOUT_R2n	AC25								
5A	VREFB5ND	IO		ACE0	DIFFD_TX_R3n	DIFFOUT_R3n	AF29	DQ1R							
5A	VREFB5ND	IO			DIFFD_RX_R4p	DIFFOUT_R4p	W20	DQ1R							
5A	VREFB5ND	IO		C/P_CONF_DONE	DIFFD_TX_R3n	DIFFOUT_R3n	AH29	DQ1R							
5A	VREFB5ND	IO			DIFFD_RX_R4n	DIFFOUT_R4n	Y21	DQ1R							
5A	VREFB5ND	IO		DEV_OE	DIFFD_TX_R5p	DIFFOUT_R5p	AE26								
5A	VREFB5ND	IO			DIFFD_RX_R6p	DIFFOUT_R6p	W21	DQS1R							
5A	VREFB5ND	IO		DEV_CLRn	DIFFD_TX_R5n	DIFFOUT_R5n	AD27	DQ1R							
5A	VREFB5ND	IO			DIFFD_RX_R6n	DIFFOUT_R6n	W22	DQS1R							
5A	VREFB5ND	IO			DIFFD_TX_R7p	DIFFOUT_R7p	AA25	DQ1R							
5A	VREFB5ND	IO			DIFFD_RX_R8p	DIFFOUT_R8p	AB22	DQ1R							
5A	VREFB5ND	IO			DIFFD_TX_R7n	DIFFOUT_R7n	AB26								
5A	VREFB5ND	IO			DIFFD_RX_R8n	DIFFOUT_R8n	W23	DQ1R							
5A	VREFB5ND	IO			DIFFD_RX_R9p	DIFFOUT_R9p	AA24								
5A	VREFB5ND	IO			DIFFD_TX_R10p	DIFFOUT_R10p	AE27	DQ2R							
5A	VREFB5ND	IO			DIFFD_RX_R9n	DIFFOUT_R9n	AB25								
5A	VREFB5ND	IO			DIFFD_TX_R10n	DIFFOUT_R10n	AE28	DQ2R							
5A	VREFB5ND	IO			DIFFD_RX_R11p	DIFFOUT_R11p	Y23	DQ2R							
5A	VREFB5ND	IO			DIFFD_TX_R12p	DIFFOUT_R12p	AQ28	DQ2R							
5A	VREFB5ND	IO			DIFFD_RX_R11n	DIFFOUT_R11n	Y24	DQ2R							
5A	VREFB5ND	IO			DIFFD_TX_R12n	DIFFOUT_R12n	AF28	DQ2R							
5A	VREFB5ND	IO			DIFFD_RX_R13p	DIFFOUT_R13p	Y23	DQS2R							
5A	VREFB5ND	IO			DIFFD_TX_R14p	DIFFOUT_R14p	AF29								
5A	VREFB5ND	IO			DIFFD_RX_R13n	DIFFOUT_R13n	W24	DQS#2R							
5A	VREFB5ND	IO			DIFFD_TX_R14n	DIFFOUT_R14n	AF30	DQ2R							
5A	VREFB5ND	IO			DIFFD_RX_R15p	DIFFOUT_R15p	AD29	DQ2R							
5A	VREFB5ND	IO			DIFFD_TX_R15p	DIFFOUT_R15p	AH30	DQ2R							
5A	VREFB5ND	IO			DIFFD_RX_R15n	DIFFOUT_R15n	AC27	DQ2R							
5A	VREFB5ND	IO			DIFFD_TX_R16p	DIFFOUT_R16p	AG30								
5B	VREFB5ND	IO			DIFFD_RX_R17p	DIFFOUT_R17p	W25								
5B	VREFB5ND	IO			DIFFD_TX_R18p	DIFFOUT_R18p	AC28	DQ3R							
5B	VREFB5ND	IO			DIFFD_RX_R17n	DIFFOUT_R17n	Y25								
5B	VREFB5ND	IO			DIFFD_TX_R18n	DIFFOUT_R18n	AC29	DQ3R							
5B	VREFB5ND	IO			DIFFD_RX_R19p	DIFFOUT_R19p	AB30	DQ3R							
5B	VREFB5ND	IO			DIFFD_TX_R20p	DIFFOUT_R20p	AB28	DQ3R							
5B	VREFB5ND	IO			DIFFD_RX_R19n	DIFFOUT_R19n	AA30	DQ3R							
5B	VREFB5ND	IO			DIFFD_TX_R20n	DIFFOUT_R20n	AA30	DQ3R							
5B	VREFB5ND	IO			DIFFD_RX_R21p	DIFFOUT_R21p	AA28	DQS3R							
5B	VREFB5ND	IO			DIFFD_TX_R22p	DIFFOUT_R22p	AE29								
5B	VREFB5ND	IO		CLK6n	DIFFD_RX_R21n	DIFFOUT_R21n	AB27	DQS#3R							
5B	VREFB5ND	IO		FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn	DIFFD_TX_R22n	DIFFOUT_R22n	AD29	DQ3R							
5B	VREFB5ND	IO		CLK4n,FPLL_BR_Fb0	DIFFD_RX_R23p	DIFFOUT_R23p	Y26	DQ3R							
5B	VREFB5ND	IO			DIFFD_TX_R24p	DIFFOUT_R24p	AD30	DQ3R							
5B	VREFB5ND	IO		CLK4n,FPLL_BR_Fb1n	DIFFD_RX_R23n	DIFFOUT_R23n	Y27	DQ3R							
5B	VREFB5ND	IO		R20_2	DIFFD_TX_R24n	DIFFOUT_R24n	AC30								
5B	VREFB5ND_HPS	HPS_DDR					W27			HPS_DM_4	HPS_DM_4				
5B	VREFB5ND_HPS	HPS_DDR					Y29			HPS_DQ_39	HPS_DQ_39				
5B	VREFB5ND_HPS	HPS_DDR					U26			HPS_DQ_37	HPS_DQ_37				
5B	VREFB5ND_HPS	HPS_DDR					Y27			HPS_DQ_38	HPS_DQ_38				
5B	VREFB5ND_HPS	HPS_DDR					T26			HPS_DQ_36	HPS_DQ_36				
5B	VREFB5ND_HPS	HPS_DDR					T24			HPS_DQS_4	HPS_DQS_4				
5B	VREFB5ND_HPS	HPS_GPI3					Y28								
5B	VREFB5ND_HPS	HPS_DDR					T23			HPS_DQS#_4	HPS_DQS#_4				
5B	VREFB5ND_HPS	HPS_DDR					V28			HPS_DQ_35	HPS_DQ_35				
5B	VREFB5ND_HPS	HPS_DDR					R24			HPS_DQ_33	HPS_DQ_33				
5B	VREFB5ND_HPS	HPS_DDR					U27			HPS_DQ_34	HPS_DQ_34				
5B	VREFB5ND_HPS	HPS_DDR					W26								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
6B	VREFB6N0_HPS	HPS_GP12					V29								
6B	VREFB6N0_HPS	HPS_GP11					V20								
6B	VREFB6N0_HPS	HPS_DDR					V30			HPS_DM_3	HPS_DM_3				
6B	VREFB6N0_HPS	HPS_GP10					T21								
6B	VREFB6N0_HPS	HPS_DDR					W29			HPS_DO_31	HPS_DO_31				
6B	VREFB6N0_HPS	HPS_DDR					P26			HPS_DO_29	HPS_DO_29				
6B	VREFB6N0_HPS	HPS_DDR					V30			HPS_DO_30	HPS_DO_30				
6B	VREFB6N0_HPS	HPS_DDR					R27			HPS_DO_28	HPS_DO_28				
6B	VREFB6N0_HPS	HPS_DDR					L30								
6B	VREFB6N0_HPS	HPS_DDR					R27			HPS_DQS_3	HPS_DQS_3				
6B	VREFB6N0_HPS	HPS_GP9					U28								
6B	VREFB6N0_HPS	HPS_DDR					R21			HPS_DQS#_3	HPS_DQS#_3				
6B	VREFB6N0_HPS	HPS_DDR					T28			HPS_DO_27	HPS_DO_27				
6B	VREFB6N0_HPS	HPS_DDR					P25			HPS_DO_25	HPS_DO_25				
6B	VREFB6N0_HPS	HPS_DDR					T29			HPS_DO_26	HPS_DO_26				
6B	VREFB6N0_HPS	HPS_DDR					P24			HPS_DO_24	HPS_DO_24				
6B	VREFB6N0_HPS	HPS_GP8					T30								
6B	VREFB6N0_HPS	HPS_GP7					V20			HPS_DM_2	HPS_DM_2				
6B	VREFB6N0_HPS	HPS_DDR					R28			HPS_DM_2	HPS_DM_2				
6B	VREFB6N0_HPS	HPS_SBR#					P22								
6B	VREFB6N0_HPS	HPS_DDR					R29			HPS_DQ_23	HPS_DQ_23				
6B	VREFB6N0_HPS	HPS_DDR					P27			HPS_DQ_21	HPS_DQ_21				
6B	VREFB6N0_HPS	HPS_DDR					K27			HPS_DQ_22	HPS_DQ_22				
6B	VREFB6N0_HPS	HPS_DDR					P26			HPS_DO_20	HPS_DO_20				
6B	VREFB6N0_HPS	HPS_SBR#					P29								
6B	VREFB6N0_HPS	HPS_DDR					R19			HPS_DQS_2	HPS_DQS_2				
6B	VREFB6N0_HPS	HPS_DDR					P30			HPS_RESET#	HPS_RESET#				
6B	VREFB6N0_HPS	HPS_DDR					R18			HPS_DQS#_2	HPS_DQS#_2				
6B	VREFB6N0_HPS	HPS_DDR					N28			HPS_DO_19	HPS_DO_19				
6B	VREFB6N0_HPS	HPS_DDR					T26			HPS_DO_17	HPS_DO_17				
6B	VREFB6N0_HPS	HPS_DDR					N29			HPS_DO_18	HPS_DO_18				
6B	VREFB6N0_HPS	HPS_DDR					U26			HPS_DO_16	HPS_DO_16				
6B	VREFB6N0_HPS	HPS_GP4					N30								
6A	VREFB6A0_HPS	HPS_GP3					M22								
6A	VREFB6A0_HPS	HPS_DDR					M28			HPS_DM_1	HPS_DM_1				
6A	VREFB6A0_HPS	HPS_GP2					N23								
6A	VREFB6A0_HPS	HPS_DDR					M30			HPS_DO_15	HPS_DO_15				
6A	VREFB6A0_HPS	HPS_DDR					M27			HPS_DQ_13	HPS_DQ_13				
6A	VREFB6A0_HPS	HPS_DDR					L28			HPS_DO_14	HPS_DO_14				
6A	VREFB6A0_HPS	HPS_DDR					M25			HPS_DO_12	HPS_DO_12				
6A	VREFB6A0_HPS	HPS_DDR					L29			HPS_CKE_0	HPS_CKE_0				
6A	VREFB6A0_HPS	HPS_DDR					N25			HPS_DQS_1	HPS_DQS_1				
6A	VREFB6A0_HPS	HPS_DDR					L30			HPS_CKE_1	HPS_CKE_1				
6A	VREFB6A0_HPS	HPS_DDR					N24			HPS_DQS#_1	HPS_DQS#_1				
6A	VREFB6A0_HPS	HPS_DDR					K27			HPS_DO_11	HPS_DO_11				
6A	VREFB6A0_HPS	HPS_DDR					L26			HPS_DO_9	HPS_DO_9				
6A	VREFB6A0_HPS	HPS_DDR					K29			HPS_DO_10	HPS_DO_10				
6A	VREFB6A0_HPS	HPS_DDR					K26			HPS_DO_8	HPS_DO_8				
6A	VREFB6A0_HPS	HPS_SBR#					J26								
6A	VREFB6A0_HPS	HPS_GP0					M25								
6A	VREFB6A0_HPS	HPS_DDR					K28			HPS_DM_0	HPS_DM_0				
6A	VREFB6A0_HPS	HPS_DDR					J29			HPS_DO_7	HPS_DO_7				
6A	VREFB6A0_HPS	HPS_DDR					L24			HPS_DO_5	HPS_DO_5				
6A	VREFB6A0_HPS	HPS_DDR					J30			HPS_DO_6	HPS_DO_6				
6A	VREFB6A0_HPS	HPS_DDR					L25			HPS_DQ_4	HPS_DQ_4				
6A	VREFB6A0_HPS	HPS_DDR					H29			HPS_ODT_1	HPS_ODT_1				
6A	VREFB6A0_HPS	HPS_DDR					M18			HPS_DQS_0	HPS_DQS_0				
6A	VREFB6A0_HPS	HPS_DDR					H28			HPS_ODT_0	HPS_ODT_0				
6A	VREFB6A0_HPS	HPS_DDR					K22			HPS_DO_3	HPS_DO_3				
6A	VREFB6A0_HPS	HPS_DDR					K22			HPS_DO_1	HPS_DO_1				
6A	VREFB6A0_HPS	HPS_DDR					H30			HPS_DO_2	HPS_DO_2				
6A	VREFB6A0_HPS	HPS_DDR					K23			HPS_DO_0	HPS_DO_0				
6A	VREFB6A0_HPS	HPS_SBR#					C27								
6A	VREFB6A0_HPS	HPS_DDR					F26			HPS_CA_0	HPS_CA_0				
6A	VREFB6A0_HPS	HPS_DDR					G30			HPS_CA_1	HPS_CA_1				
6A	VREFB6A0_HPS	HPS_DDR					J25			HPS_CA_4	HPS_CA_4				
6A	VREFB6A0_HPS	HPS_DDR					F28			HPS_CA_2	HPS_CA_2				
6A	VREFB6A0_HPS	HPS_DDR					J27			HPS_CA_5	HPS_CA_5				
6A	VREFB6A0_HPS	HPS_DDR					F30			HPS_CA_3	HPS_CA_3				
6A	VREFB6A0_HPS	HPS_DDR					M23			HPS_CK	HPS_CK				
6A	VREFB6A0_HPS	HPS_DDR					F29			HPS_CA_6	HPS_CA_6				
6A	VREFB6A0_HPS	HPS_DDR					L23			HPS_CK#	HPS_CK#				
6A	VREFB6A0_HPS	HPS_DDR					F28			HPS_A_7	HPS_A_7				
6A	VREFB6A0_HPS	HPS_DDR					J24			HPS_BA_1	HPS_BA_1				
6A	VREFB6A0_HPS	HPS_DDR					E29			HPS_BA_0	HPS_BA_0				
6A	VREFB6A0_HPS	HPS_DDR					J23			HPS_BA_2	HPS_BA_2				
6A	VREFB6A0_HPS	HPS_DDR					E27			HPS_CAS#	HPS_CAS#				
6A	VREFB6A0_HPS	HPS_DDR					D30			HPS_RAS#	HPS_RAS#				
6A	VREFB6A0_HPS	HPS_DDR					H27			HPS_A_8	HPS_A_8				
6A	VREFB6A0_HPS	HPS_DDR					D29			HPS_A_10	HPS_A_10				
6A	VREFB6A0_HPS	HPS_DDR					G26			HPS_A_9	HPS_A_9				
6A	VREFB6A0_HPS	HPS_DDR					C30			HPS_A_11	HPS_A_11				
6A	VREFB6A0_HPS	HPS_DDR					H24			HPS_CSA_0	HPS_CSA_0				
6A	VREFB6A0_HPS	HPS_DDR					B30			HPS_A_12	HPS_A_12				
6A	VREFB6A0_HPS	HPS_DDR					K21			HPS_CSA_1	HPS_CSA_1				
6A	VREFB6A0_HPS	HPS_DDR					C28			HPS_A_13	HPS_A_13				
6A	VREFB6A0_HPS	HPS_DDR					H25			HPS_A_14	HPS_A_14				
6A	VREFB6A0_HPS	HPS_DDR					C28			HPS_WE#	HPS_WE#				
6A	VREFB6A0_HPS	HPS_DDR					G25			HPS_A_15	HPS_A_15				
6A	VREFB6A0_HPS	HPS_RZQ_0					J27								
6A	VREFB6A0_HPS	GND					J22								
6A	VREFB6A0_HPS	GND					D26								
7A	HPS_nRST						C27								
7A	HPS_nPOR						F23								
7A	HPS_TDO						B28								
7A	VCCSR1CLK_HPS						G23								
7A	HPS_TMS						A29								
7A	HPS_TCK						H22								
7A	HPS_TRST						A28								
7A	HPS_TDI						B27								
7A	GND						A26								
7A	HPS_PORSEL						F24								
7A	HPS_CLK3						D26								
7A	HPS_CLK2						F26								
7A	VREFB7A7B7C7D0_HPS	TRACE_CLK					B26					TRACE_CLK			HPS_GPD48
7A	VREFB7A7B7C7D0_HPS	TRACE_D0					B25					TRACE_D0			HPS_GPD49
7A	VREFB7A7B7C7D0_HPS	TRACE_D1					C25					TRACE_D1			HPS_GPD50
7A	VREFB7A7B7C7D0_HPS	TRACE_D2					A25					TRACE_D2			HPS_GPD51
7A	VREFB7A7B7C7D0_HPS	TRACE_D3					H23					TRACE_D3			HPS_GPD52
7A	VREFB7A7B7C7D0_HPS	TRACE_D4					A24					TRACE_D4			HPS_GPD53
7A	VREFB7A7B7C7D0_HPS	TRACE_D5					G21					TRACE_D5			HPS_GPD54
7A	VREFB7A7B7C7D0_HPS	TRACE_D6					C24					TRACE_D6			HPS_GPD55
7A	VREFB7A7B7C7D0_HPS	TRACE_D7					E23					TRACE_D7			HPS_GPD56
7A	VREFB7A7B7C7D0_HPS	SPIN0_CLK					A23					SPIN0_CLK			HPS_GPD57



Pin Information for the Cyclone® V 5CSEMA5 Device
Version 1.3
Note (1)

Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
7A	VREFB7A7B7C7D0	HPS	SPIM0_MOSI				C22					SPIM0_MOSI	IC21_SCL	UART0_RTS	HPS_GPD58
7A	VREFB7A7B7C7D0	HPS	SPIM0_MISO				B23					SPIM0_MISO	CANN_RX	UART1_CTS	HPS_GPD59
7A	VREFB7A7B7C7D0	HPS	SPIM0_SS0				F00					SPIM0_SS0	CANN_TX	UART1_RTS	HPS_GPD60
7A	VREFB7A7B7C7D0	HPS	UART0_RX				B22					UART0_RX	CANN_RX	SPIM0_SS1	HPS_GPD61
7A	VREFB7A7B7C7D0	HPS	UART0_TX_CLKSEL1				D22					UART0_TX	CANN_TX	SPIM1_SS1	HPS_GPD62
7A	VREFB7A7B7C7D0	HPS	IC20_SDA				C23					IC20_SDA	UART1_RX	SPIM1_CLK	HPS_GPD63
7A	VREFB7A7B7C7D0	HPS	IC20_SCL				D22					IC20_SCL	UART1_TX	SPIM1_MOSI	HPS_GPD64
7B	VREFB7A7B7C7D0	HPS	CANN_RX				E24					CANN_RX	UART0_RX	SPIM1_MISO	HPS_GPD65
7A	VREFB7A7B7C7D0	HPS	CANN_TX_CLKSEL0				D24					CANN_TX	UART0_TX	SPIM1_SS0	HPS_GPD66
7B	VREFB7A7B7C7D0	HPS	NAND_ALE				H19					NAND_ALE	RGMI1_TX_CLK	OSPI_SS3	HPS_GPD14
7B	VREFB7A7B7C7D0	HPS	NAND_CE				F20					NAND_CE	RGMI1_TXD0	USB1_D0	HPS_GPD15
7B	VREFB7A7B7C7D0	HPS	NAND_CLE				J19					NAND_CLE	RGMI1_TXD1	USB1_D1	HPS_GPD16
7B	VREFB7A7B7C7D0	HPS	NAND_RE				F21					NAND_RE	RGMI1_TXD2	USB1_D2	HPS_GPD17
7B	VREFB7A7B7C7D0	HPS	NAND_RB				F19					NAND_RB	RGMI1_TXD3	USB1_D3	HPS_GPD18
7B	VREFB7A7B7C7D0	HPS	NAND_DQ0				A21					NAND_DQ0	RGMI1_RXD0	USB1_D4	HPS_GPD19
7B	VREFB7A7B7C7D0	HPS	NAND_DQ1				E21					NAND_DQ1	RGMI1_MISO	IC23_SDA	HPS_GPD20
7B	VREFB7A7B7C7D0	HPS	NAND_DQ2				B21					NAND_DQ2	RGMI1_MDC	IC23_SCL	HPS_GPD21
7B	VREFB7A7B7C7D0	HPS	NAND_DQ3				K17					NAND_DQ3	RGMI1_RX_CTL	USB1_D4	HPS_GPD22
7B	VREFB7A7B7C7D0	HPS	NAND_DQ4				A20					NAND_DQ4	RGMI1_TX_CTL	USB1_D6	HPS_GPD23
7B	VREFB7A7B7C7D0	HPS	NAND_DQ5				B20					NAND_DQ5	RGMI1_RX_CLK	USB1_D6	HPS_GPD24
7B	VREFB7A7B7C7D0	HPS	NAND_DQ6				B20					NAND_DQ6	RGMI1_RXD1	USB1_D7	HPS_GPD25
7B	VREFB7A7B7C7D0	HPS	NAND_DQ7				B18					NAND_DQ7	RGMI1_RXD2	USB1_D7	HPS_GPD26
7B	VREFB7A7B7C7D0	HPS	NAND_WIP				D23					NAND_WIP	RGMI1_RXD3	USB1_D2	HPS_GPD27
7B	VREFB7A7B7C7D0	HPS	NAND_WE_BOOTSEL2				D20					NAND_WE	OSPI_SS1	OSPI_SS2	HPS_GPD28
7B	VREFB7A7B7C7D0	HPS	OSPI_I00				C20					OSPI_I00	USB1_CLK	USB1_CLK	HPS_GPD29
7B	VREFB7A7B7C7D0	HPS	OSPI_I01				H18					OSPI_I01	USB1_STP	USB1_STP	HPS_GPD30
7B	VREFB7A7B7C7D0	HPS	OSPI_I02				A19					OSPI_I02	USB1_DR	USB1_DR	HPS_GPD31
7B	VREFB7A7B7C7D0	HPS	OSPI_I03				E19					OSPI_I03	USB1_NXT	USB1_NXT	HPS_GPD32
7B	VREFB7A7B7C7D0	HPS	OSPI_SS0_BOOTSEL1				A18					OSPI_SS0			HPS_GPD33
7B	VREFB7A7B7C7D0	HPS	OSPI_CLK				D19					OSPI_CLK			HPS_GPD34
7B	VREFB7A7B7C7D0	HPS	OSPI_SS1				C19					OSPI_SS1			HPS_GPD35
7C	VREFB7A7B7C7D0	HPS	SDMMC_CMD				F18					SDMMC_CMD	USBS0_D0	USBS0_D0	HPS_GPD36
7C	VREFB7A7B7C7D0	HPS	SDMMC_PWREN				B17					SDMMC_PWREN	USBS0_D1	USBS0_D1	HPS_GPD37
7C	VREFB7A7B7C7D0	HPS	SDMMC_D0				G18					SDMMC_D0	USBS0_D2	USBS0_D2	HPS_GPD38
7C	VREFB7A7B7C7D0	HPS	SDMMC_D1				C17					SDMMC_D1	USBS0_D3	USBS0_D3	HPS_GPD39
7C	VREFB7A7B7C7D0	HPS	SDMMC_D4				H17					SDMMC_D4	USBS0_D4	USBS0_D4	HPS_GPD40
7C	VREFB7A7B7C7D0	HPS	SDMMC_D5				C18					SDMMC_D5	USBS0_D5	USBS0_D5	HPS_GPD41
7C	VREFB7A7B7C7D0	HPS	SDMMC_D6				G17					SDMMC_D6	USBS0_D6	USBS0_D6	HPS_GPD42
7C	VREFB7A7B7C7D0	HPS	SDMMC_D7				E18					SDMMC_D7	USBS0_D7	USBS0_D7	HPS_GPD43
7C	VREFB7A7B7C7D0	HPS	SDMMC_FB_CLK_IN				E17					SDMMC_FB_CLK_IN	USBS0_CLK	USBS0_CLK	HPS_GPD44
7C	VREFB7A7B7C7D0	HPS	SDMMC_CCLK_OUT				A16					SDMMC_CCLK_OUT	USBS0_STP	USBS0_STP	HPS_GPD45
7C	VREFB7A7B7C7D0	HPS	SDMMC_D2				D17					SDMMC_D2	USBS0_DIR	USBS0_DIR	HPS_GPD46
7C	VREFB7A7B7C7D0	HPS	SDMMC_D3				B16					SDMMC_D3	USBS0_NKT	USBS0_NKT	HPS_GPD47
7D	VREFB7A7B7C7D0	HPS	RGMI0_TX_CLK				F16					RGMI0_TX_CLK			HPS_GPD00
7D	VREFB7A7B7C7D0	HPS	RGMI0_TXD0				E16					RGMI0_TXD0	USB1_D0	USB1_D0	HPS_GPD01
7D	VREFB7A7B7C7D0	HPS	RGMI0_TXD1				G16					RGMI0_TXD1	USB1_D1	USB1_D1	HPS_GPD02
7D	VREFB7A7B7C7D0	HPS	RGMI0_TXD2				D16					RGMI0_TXD2	USB1_D2	USB1_D2	HPS_GPD03
7D	VREFB7A7B7C7D0	HPS	RGMI0_TXD3				D14					RGMI0_TXD3	USB1_D3	USB1_D3	HPS_GPD04
7D	VREFB7A7B7C7D0	HPS	RGMI0_RXD0				A15					RGMI0_RXD0	USB1_D4	USB1_D4	HPS_GPD05
7D	VREFB7A7B7C7D0	HPS	RGMI0_MISO				C14					RGMI0_MISO	USB1_D5	IC22_SDA	HPS_GPD06
7D	VREFB7A7B7C7D0	HPS	RGMI0_MDC				D15					RGMI0_MDC	USB1_D6	IC22_SCL	HPS_GPD07
7D	VREFB7A7B7C7D0	HPS	RGMI0_RX_CTL				M17					RGMI0_RX_CTL	USB1_D7	USB1_D7	HPS_GPD08
7D	VREFB7A7B7C7D0	HPS	RGMI0_TX_CTL				B15					RGMI0_TX_CTL			HPS_GPD09
7D	VREFB7A7B7C7D0	HPS	RGMI0_RX_CLK				R16					RGMI0_RX_CLK	USB1_CLK	USB1_CLK	HPS_GPD10
7D	VREFB7A7B7C7D0	HPS	RGMI0_RXD1				C15					RGMI0_RXD1	USB1_STP	USB1_STP	HPS_GPD11
7D	VREFB7A7B7C7D0	HPS	RGMI0_RXD2				E14					RGMI0_RXD2	USB1_DIR	USB1_DIR	HPS_GPD12
7D	VREFB7A7B7C7D0	HPS	RGMI0_RXD3				A14					RGMI0_RXD3	USB1_NKT	USB1_NKT	HPS_GPD13
8A	VREFB8A0	IO	CLK0p		DIFF0_RX_T1p	DIFF0_T1p	H15								
8A	VREFB8A0	IO			DIFF0_RX_T2p	DIFF0_T2p	B13	DQ1T							
8A	VREFB8A0	IO	CLK0n		DIFF0_RX_T1n	DIFF0_T1n	G16								
8A	VREFB8A0	IO			DIFF0_RX_T2n	DIFF0_T2n	A13	DQ1T							
8A	VREFB8A0	IO			DIFF0_RX_T3p	DIFF0_T3p	C13	DQ1T							
8A	VREFB8A0	IO		FPLL_TL_CLKOUT0,FPLL_TL_CLKOUT1,FPLL_TL_FB	DIFF0_RX_T4p	DIFF0_T4p	A11	DQ1T							
8A	VREFB8A0	IO			DIFF0_RX_T5p	DIFF0_T5p	B12	DQ1T							
8A	VREFB8A0	IO		FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn	DIFF0_RX_T6n	DIFF0_T6n	A10	DQ1T							
8A	VREFB8A0	IO			DIFF0_RX_T5p	DIFF0_T5p	F15	DQS1T							
8A	VREFB8A0	IO			DIFF0_RX_T6p	DIFF0_T6p	C12	DQ1T							
8A	VREFB8A0	IO			DIFF0_RX_T5n	DIFF0_T5n	F14	DQS1T							
8A	VREFB8A0	IO			DIFF0_RX_T6n	DIFF0_T6n	B11	DQ1T							
8A	VREFB8A0	IO			DIFF0_RX_T7p	DIFF0_T7p	D11	DQ1T							
8A	VREFB8A0	IO			DIFF0_RX_T8p	DIFF0_T8p	A9	DQ1T							
8A	VREFB8A0	IO			DIFF0_RX_T7n	DIFF0_T7n	D10	DQ1T							
8A	VREFB8A0	IO			DIFF0_RX_T8n	DIFF0_T8n	A8	DQ1T							
8A	VREFB8A0	IO	CLK0p,FPLL_TL_FBp		DIFF0_RX_T9p	DIFF0_T9p	A14	DQ2T							
8A	VREFB8A0	IO			DIFF0_RX_T10p	DIFF0_T10p	C7	DQ2T	DQ1T						
8A	VREFB8A0	IO	CLK0n,FPLL_TL_FBn		DIFF0_RX_T9n	DIFF0_T9n	J14	DQ2T							
8A	VREFB8A0	IO			DIFF0_RX_T10n	DIFF0_T10n	B7	DQ2T	DQ1T						
8A	VREFB8A0	IO			DIFF0_RX_T11p	DIFF0_T11p	E9	DQ2T	DQ1T						
8A	VREFB8A0	IO			DIFF0_RX_T12p	DIFF0_T12p	C8	DQ2T	DQ1T						
8A	VREFB8A0	IO			DIFF0_RX_T11n	DIFF0_T11n	D9	DQ2T	DQ1T						
8A	VREFB8A0	IO			DIFF0_RX_T12n	DIFF0_T12n	B8	DQ2T	DQ1T						
8A	VREFB8A0	IO			DIFF0_RX_T13p	DIFF0_T13p	H14	DQS2T	DQS1T						
8A	VREFB8A0	IO			DIFF0_RX_T14p	DIFF0_T14p	C10	DQ2T	DQ1T						
8A	VREFB8A0	IO			DIFF0_RX_T13n	DIFF0_T13n	C13	DQS2T	DQS1T						
8A	VREFB8A0	IO			DIFF0_RX_T14n	DIFF0_T14n	C9	DQ2T	DQ1T						
8A	VREFB8A0	IO			DIFF0_RX_T15p	DIFF0_T15p	F13	DQ2T	DQ1T						
8A	VREFB8A0	IO			DIFF0_RX_T16p	DIFF0_T16p	A8	DQ2T	DQ1T						
8A	VREFB8A0	IO			DIFF0_RX_T15n	DIFF0_T15n	E13	DQ2T	DQ1T						
8A	VREFB8A0	IO			DIFF0_RX_T16n	DIFF0_T16n	A5	DQ2T	DQ1T						
8A	VREFB8A0	IO			DIFF0_RX_T17p	DIFF0_T17p	H8	DQ2T	DQ1T						
8A	VREFB8A0	IO			DIFF0_RX_T18p	DIFF0_T18p	A4	DQ3T	DQ2T						
8A	VREFB8A0	IO			DIFF0_RX_T17n	DIFF0_T17n	G8	DQ2T	DQ1T						
8A	VREFB8A0	IO			DIFF0_RX_T18n	DIFF0_T18n	A3	DQ3T	DQ2T						
8A	VREFB8A0	IO			DIFF0_RX_T19p	DIFF0_T19p	F12	DQ3T	DQ2T						
8A	VREFB8A0	IO			DIFF0_RX_T20p	DIFF0_T20p	D6	DQ3T	DQ2T						
8A	VREFB8A0	IO			DIFF0_RX_T19n	DIFF0_T19n	D12	DQ3T	DQ2T						
8A	VREFB8A0	IO			DIFF0_RX_T20n	DIFF0_T20n	C3	DQ3T	DQ2T						
8A	VREFB8A0	IO			DIFF0_RX_T21p	DIFF0_T21p	H13	DQS3T	DQS2T						
8A	VREFB8A0	IO			DIFF0_RX_T22p	DIFF0_T22p	D5	DQ3T	DQ2T						
8A	VREFB8A0	IO			DIFF0_RX_T21n	DIFF0_T21n	H12	DQS3T	DQS2T						
8A	VREFB8A0	IO			DIFF0_RX_T22n	DIFF0_T22n	C4	DQ3T	DQ2T						
8A	VREFB8A0	IO			DIFF0_RX_T23p	DIFF0_T23p	F11	DQ3T	DQ2T						
8A	VREFB8A0	IO			DIFF0_RX_T24p	DIFF0_T24p	E8	DQ3T	DQ2T						
8A	VREFB8A0	IO			DIFF0_RX_T23n	DIFF0_T23n	E11	DQ3T	DQ2T						
8A	VREFB8A0	IO			DIFF0_RX_T24n	DIFF0_T24n	D7	DQ3T	DQ2T						
8A	VREFB8A0	IO			DIFF0_RX_T25p	DIFF0_T25p	J7	DQ4T	DQ3T						
8A	VREFB8A0	IO			DIFF0_RX_T26p	DIFF0_T26p	B2	DQ4T	DQ3T						
8A	VREFB8A0	IO			DIFF0_RX_T25n	DIFF0_T25n	H7	DQ3T	DQ2T						
8A	VREFB8A0	IO			DIFF0_RX_T26n	DIFF0_T26n	B1	DQ4T	DQ3T						
8A	VREFB8A0	IO			DIFF0_RX_T27p										



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
BA	VREFBAND	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	J12	DQSx4T	DQSx2T						
BA	VREFBAND	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	C2	DQ4T	DQ2T						
BA	VREFBAND	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	G13	DQ4T	DQ2T						
BA	VREFBAND	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	E4	DQ4T	DQ2T						
BA	VREFBAND	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	G11	DQ4T	DQ2T						
BA	VREFBAND	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	D4								
BA	VREFBAND	IO			DIFFIO_RX_T33p	DIFFOUT_T33p	K7								
BA	VREFBAND	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	E3	DQ5T	DQ2T						
BA	VREFBAND	IO			DIFFIO_RX_T33n	DIFFOUT_T33n	M8								
BA	VREFBAND	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	E2	DQ5T	DQ2T						
BA	VREFBAND	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	G10	DQ5T	DQ2T						
BA	VREFBAND	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	E1	DQ5T	DQ2T						
BA	VREFBAND	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	F10	DQ5T	DQ2T						
BA	VREFBAND	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	D1	DQ5T	DQ2T						
BA	VREFBAND	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	J10	DQSxT	DQ2T						
BA	VREFBAND	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	E7								
BA	VREFBAND	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	J9	DQSxT	DQ2T						
BA	VREFBAND	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	E6	DQ5T	DQ2T						
BA	VREFBAND	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	F9	DQ5T	DQ2T						
BA	VREFBAND	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	G7	DQ5T	DQ2T						
BA	VREFBAND	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	F8	DQ5T	DQ2T						
BA	VREFBAND	IO			DIFFIO_TX_T40n	DIFFOUT_T40n	F6								
BA		MSEL0		MSEL0			L4								
BA		CONF_DONE		CONF_DONE			F3								
BA		MSEL1		MSEL1			K6								
BA		INSTATUS		INSTATUS			F4								
BA		IC		IC			G5								
BA		MSEL2		MSEL2			G6								
BA		MSEL3		MSEL3			L7								
BA		ICCONF0		ICCONF0			J6								
BA		MSEL4		MSEL4			L9								
		GND					J8								
		GND					J2								
		GND					J1								
		GND					L2								
		GND					L1								
		GND					N2								
		GND					N1								
		GND					P9								
		GND					P8								
		GND					T8								
		GND					T9								
		GND					R2								
		GND					R1								
		GND					L2								
		GND					U1								
		GND					W2								
		GND					W1								
		GND					AA2								
		GND					AA1								
		GND					AC2								
		GND					AC1								
		GND					AE2								
		GND					AE1								
		GND					W8								
		GND					W7								
		GND					A12								
		GND					A17								
		GND					A2								
		GND					A22								
		GND					A27								
		GND					AA11								
		GND					AA22								
		GND					AA3								
		GND					AA4								
		GND					AA6								
		GND					AA9								
		GND					AB1								
		GND					AB19								
		GND					AB2								
		GND					AB29								
		GND					AB5								
		GND					AB7								
		GND					AC16								
		GND					AC28								
		GND					AC3								
		GND					ACA								
		GND					AC5								
		GND					AC8								
		GND					AD1								
		GND					AD2								
		GND					AD23								
		GND					AD5								
		GND					AE10								
		GND					AE20								
		GND					AE3								
		GND					AE4								
		GND					AF1								
		GND					AF12								
		GND					AF17								
		GND					AF2								
		GND					AF27								
		GND					AF3								
		GND					AG14								
		GND					AG24								
		GND					AG9								
		GND					AH1								
		GND					AH11								
		GND					AH21								
		GND					AH6								
		GND					AJ18								
		GND					AJ28								
		GND					AJ3								
		GND					AJ38								
		GND					AK16								
		GND					AK26								
		GND					AK5								
		GND					B14								
		GND					B19								
		GND					B24								
		GND					B29								
		GND					B9								
		GND					C1								
		GND					C16								
		GND					C21								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	FB96	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0	
		GND					C26									
		GND					C8									
		GND					D13									
		GND					D23									
		GND					D3									
		GND					E10									
		GND					E25									
		GND					E30									
		GND					F17									
		GND					F2									
		GND					F27									
		GND					F5									
		GND					F7									
		GND					G24									
		GND					G3									
		GND					G4									
		GND					H1									
		GND					H11									
		GND					H2									
		GND					H5									
		GND					H18									
		GND					J8									
		GND					J3									
		GND					J4									
		GND					J8									
		GND					K1									
		GND					K10									
		GND					K15									
		GND					K2									
		GND					K20									
		GND					K25									
		GND					K5									
		GND					L11									
		GND					L13									
		GND					L15									
		GND					L17									
		GND					L19									
		GND					L22									
		GND					L3									
		GND					L4									
		GND					L6									
		GND					M1									
		GND					M10									
		GND					M12									
		GND					M14									
		GND					M16									
		GND					M18									
		GND					M2									
		GND					M20									
		GND					M29									
		GND					M5									
		GND					M7									
		GND					M8									
		GND					N11									
		GND					N13									
		GND					N15									
		GND					N17									
		GND					N19									
		GND					N26									
		GND					N3									
		GND					N4									
		GND					N6									
		GND					N8									
		GND					N9									
		GND					P1									
		GND					P10									
		GND					P12									
		GND					P14									
		GND					P16									
		GND					P18									
		GND					P2									
		GND					P20									
		GND					P5									
		GND					P7									
		GND					R11									
		GND					R13									
		GND					R16									
		GND					R17									
		GND					R3									
		GND					R30									
		GND					R4									
		GND					R6									
		GND					R8									
		GND					R9									
		GND					T1									
		GND					T10									
		GND					T12									
		GND					T14									
		GND					T15									
		GND					T16									
		GND					T2									
		GND					T20									
		GND					T27									
		GND					T5									
		GND					T7									
		GND					U11									
		GND					U13									
		GND					U15									
		GND					U17									
		GND					U24									
		GND					U29									
		GND					U3									
		GND					U4									
		GND					U6									
		GND					U9									
		GND					V1									
		GND					V10									
		GND					V12									
		GND					V14									
		GND					V19									
		GND					V2									
		GND					V21									
		GND					V5									
		GND					V7									
		GND					W11									



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					W13								
		GND					W18								
		GND					W26								
		GND					W3								
		GND					W4								
		GND					W6								
		GND					W9								
		GND					Y1								
		GND					Y10								
		GND					Y12								
		GND					Y14								
		GND					Y15								
		GND					Y2								
		GND					Y20								
		GND					Y25								
		GND					Y29								
		GND					Y5								
		GND					Y7								
		GND					Y6								
		GND					U22								
		GND					T18								
		VCC					M11								
		VCC					M3								
		VCC					M9								
		VCC					N10								
		VCC					N12								
		VCC					N14								
		VCC					P11								
		VCC					P13								
		VCC					R10								
		VCC					R12								
		VCC					R14								
		VCC					T11								
		VCC					T13								
		VCC					U10								
		VCC					U12								
		VCC					U14								
		VCC					V11								
		VCC					V13								
		VCC					V15								
		VCC					W10								
		VCC					W12								
		VCC					W14								
		VCC					Y11								
		VCC					Y13								
		VCC					Y9								
		VCC					L5								
		VCC					R5								
		VCC					W5								
		VCC					A5								
		VCC					M6								
		VCC					N5								
		VCC					T6								
		VCC					U5								
		VCC					Y6								
		VCC					U21								
		DNU					F1								
		DNU					G2								
		DNU					H3								
		DNU					H4								
		DNU					K3								
		DNU					K4								
		DNU					M3								
		DNU					M4								
		DNU					P3								
		DNU					P4								
		DNU					T3								
		DNU					T4								
		DNU					V3								
		DNU					V4								
		DNU					Y3								
		DNU					Y4								
		DNU					AB3								
		DNU					AB4								
		DNU					AD3								
		DNU					AD4								
		DNU					AA7								
		DNU					AD15								
		DNU					E26								
		DNU					J15								
		VCCPGM					AB10								
		VCCPGM					AA23								
		VCCPGM					J11								
		VCCIOA					H9								
		VCCIOA					AC11								
		VCCIOA					AD8								
		VCCIOA					AF7								
		VCCIOA					AG4								
		VCCIOB					AB14								
		VCCIOB					AD13								
		VCCIOB					AE15								
		VCCIOB					AJ13								
		VCCIOB					AJ8								
		VCCIOB					AK10								
		VCCIOA					AA17								
		VCCIOA					AC21								
		VCCIOA					AD18								
		VCCIOA					AE25								
		VCCIOA					AF22								
		VCCIOA					AG19								
		VCCIOA					AH16								
		VCCIOA					AH26								
		VCCIOA					AJ23								
		VCCIOA					AK20								
		VCCIOA					AB24								
		VCCIOA					AD28								
		VCCIOA					AG29								
		VCCIOA					W23								
		VCCIOB					AA27								
		VCCIOB					AE30								
		VCCIOA_HPS					G28								
		VCCIOA_HPS					G29								
		VCCIOA_HPS					H26								
		VCCIOA_HPS					K24								
		VCCIOA_HPS					K30								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0	
		VCCIO6A_HPS					L27									
		VCCIO6A_HPS					M24									
		VCCIO6A_HPS					N21									
		VCCIO6B_HPS					P23									
		VCCIO6B_HPS					P26									
		VCCIO6B_HPS					R25									
		VCCIO6B_HPS					T22									
		VCCIO6B_HPS					U19									
		VCCIO6B_HPS					V26									
		VCCIO7A_HPS					F22									
		VCCIO7A_HPS					H21									
		VCCIO7B_HPS					E20									
		VCCIO7B_HPS					G19									
		VCCIO7C_HPS					D18									
		VCCIO7D_HPS					E15									
		VCCIO7D_HPS					H16									
		VCCIO8A					A7									
		VCCIO8A					B4									
		VCCIO8A					C11									
		VCCIO8A					D8									
		VCCIO8A					E5									
		VCCIO8A					F12									
		VCCIO8A					G14									
		VCCIO8A					H9									
		VCCIO8A					HB									
		VCCIO8A					J13									
		VCCPD3A					AA10									
		VCCPD3A					AC10									
		VCCPD384A					AB18									
		VCCPD384A					AB20									
		VCCPD384A					AC13									
		VCCPD384A					AC15									
		VCCPD384A					AC17									
		VCCPD384A					AC19									
		VCCPD384A					AD16									
		VCCPD384A					AE21									
		VCCPD6A					V24									
		VCCPD6B					U23									
		VCCPD6A6B_HPS					M21									
		VCCPD6A6B_HPS					N22									
		VCCPD6A6B_HPS					P21									
		VCCPD6A6B_HPS					R20									
		VCCPD6A6B_HPS					R23									
		VCCPD7A_HPS					K19									
		VCCPD7B_HPS					K18									
		VCCPD7C_HPS					J17									
		VCCPD7D_HPS					K16									
		VCCPD8A					K11									
		VCCPD8A					K13									
		VCCPD8A					L10									
		VCCPD8A					L12									
		VCCPD8A					L14									
3A	VREFB3AN0	VREFB3AN0					AD5									
3B	VREFB3BN0	VREFB3BN0					AJ15									
4A	VREFB4AN0	VREFB4AN0					AK17									
5A	VREFB5AN0	VREFB5AN0					AC24									
5B	VREFB5BN0	VREFB5BN0					AA29									
	VREFB7A7B7C7D0_HPS	VREFB7A7B7C7D0_HPS					E22									
8A	VREFB8AN0	VREFB8AN0					E10									
		VCCRSTCLK_HPS					J20									
		RREF_TL					G1									
		VCCA_FPLL					N7									
		VCCA_FPLL					R7									
		VCCA_FPLL					V8									
		VCCA_FPLL					AA8									
		VCCA_FPLL					K9									
		VCCA_FPLL					Y22									
		VCCA_FPLL					AB6									
		VCCA_FPLL					JP									
		VCCA_FPLL					V6									
		VCC_AUX					AB11									
		VCC_AUX					AB16									
		VCC_AUX					AD22									
		VCC_AUX					H10									
		VCC_AUX					J16									
		VCC_AUX_SHARED					J21									
		VCCPLL_HPS					L21									
		VCC_HPS					U18									
		VCC_HPS					L16									
		VCC_HPS					L18									
		VCC_HPS					L20									
		VCC_HPS					M15									
		VCC_HPS					N20									
		VCC_HPS					P15									
		VCC_HPS					P17									
		VCC_HPS					P19									
		VCC_HPS					R16									
		VCC_HPS					T17									
		VCC_HPS					T19									
		VCC_HPS					U16									

Notes:
(1) For more information about pin definitions and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.
(2) HPS_DDR pins are for memory interface only. For the dedicated pin function corresponding with the respective memory interfaces, refer to the HMC columns.
(3) RESET pin is only applicable for DDR3 device.



Pin Information for the Cyclone® V 5CSEMA5 Device
Version 1.3

Version Number	Date	Changes Made
1.0	10/18/2012	Initial release.
1.1	1/17/2013	A pin that was marked as VCC_HPS has been corrected to VCCRSTCLK_HPS
1.2	3/25/2013	Updated the following pin names: - Changed SDMMC_CLK_IN to SDMMC_FB_CLK_IN - Changed SDMMC_CLK to SDMMC_CCLK_OUT
1.3	9/30/2014	- Remove corresponding bank number from VCCRSTCLK_HPS pin. - Changed HMC Pin Assignment for DDR3 to HMC Pin Assignment for DDR3/DDR2. - Added note 3.