

# Stratix 10 SoC FPGA Development Kit Board

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REV	DATE	PAGES	DESCRIPTION
A.0 release			
		50,58,59,60,61,64	Modified from 150-0321319 RevA1
		35	Change M12Vto3V3,VCCERAM,VCC_HPS,VCCPT,VCCT,VCCR using Empirion devices
		56	Swap SDI_SDA_SDI_SCL
		30	Connect S10_VCCFAULT for U55 (pin25,26)
		38	Change FPGA symbol based on new pinout for TSD0 and TSD1
		38	Add new temp sense chip U116 for TSD1
		38	Group EM2130 I2C bus and add dip switch SW8 for isolation
	10/12/17	50,60	Change C1677,C1678,C1771,C1772 to 22uF Cer cap 16V
B.0 release			
		50	Change R5246 to 12K and I2C address to 4B
		9	Ground MT1 to MT3
		58	Change C1698 Capacitor to diff Agile number
		40	REMOVED Parrallel Flash



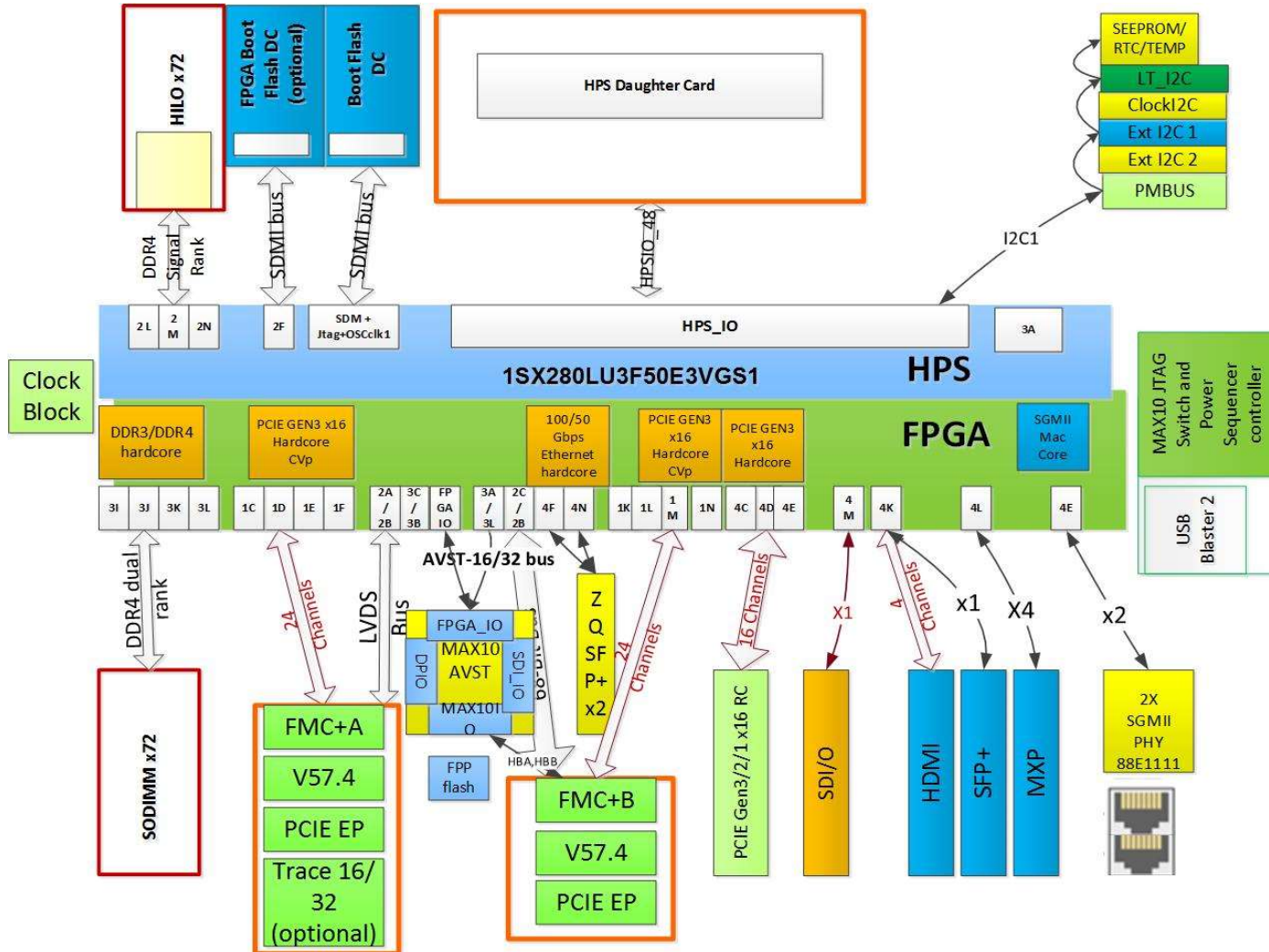
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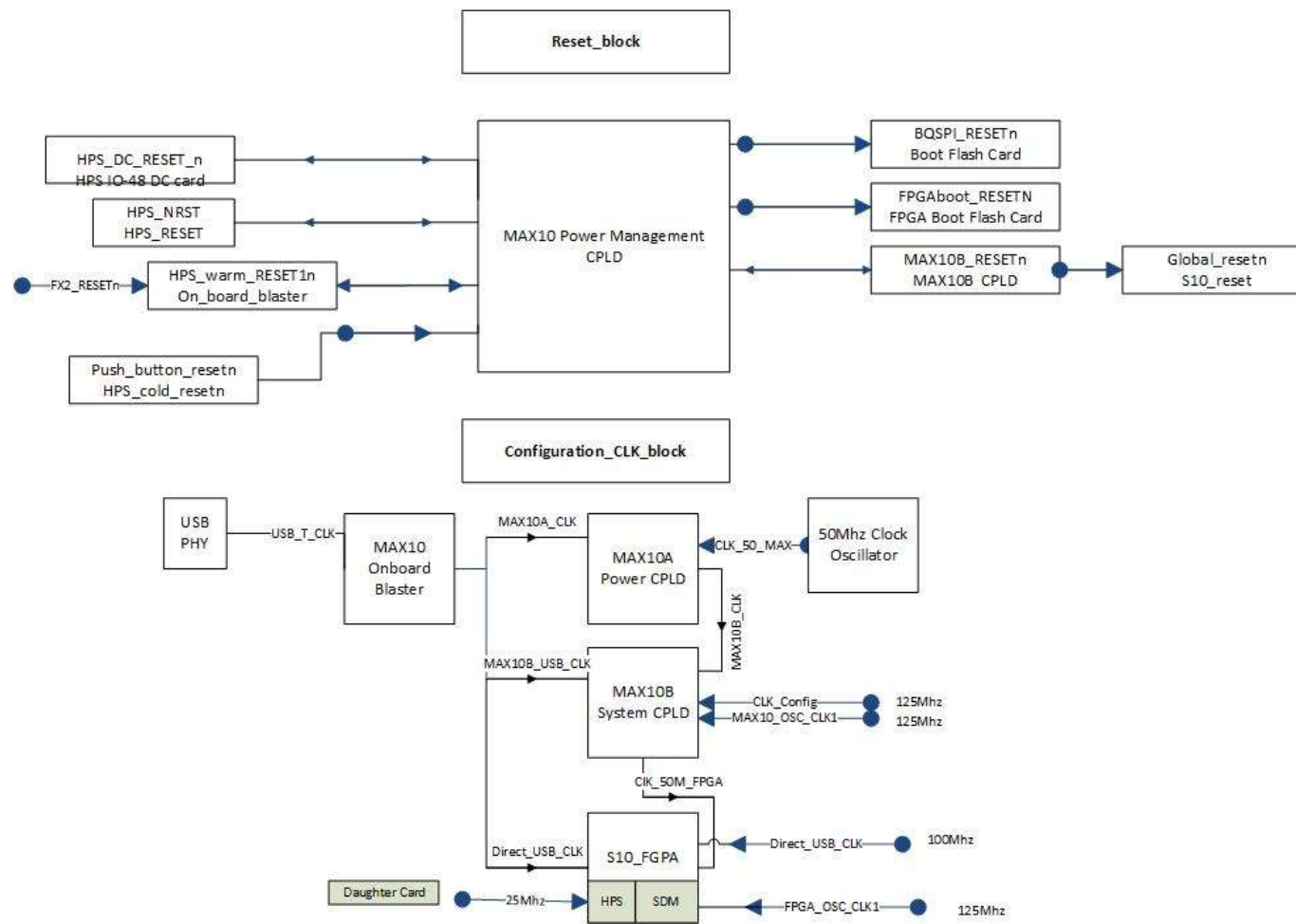
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# Stratix 10 Dev Kit Block Diagram



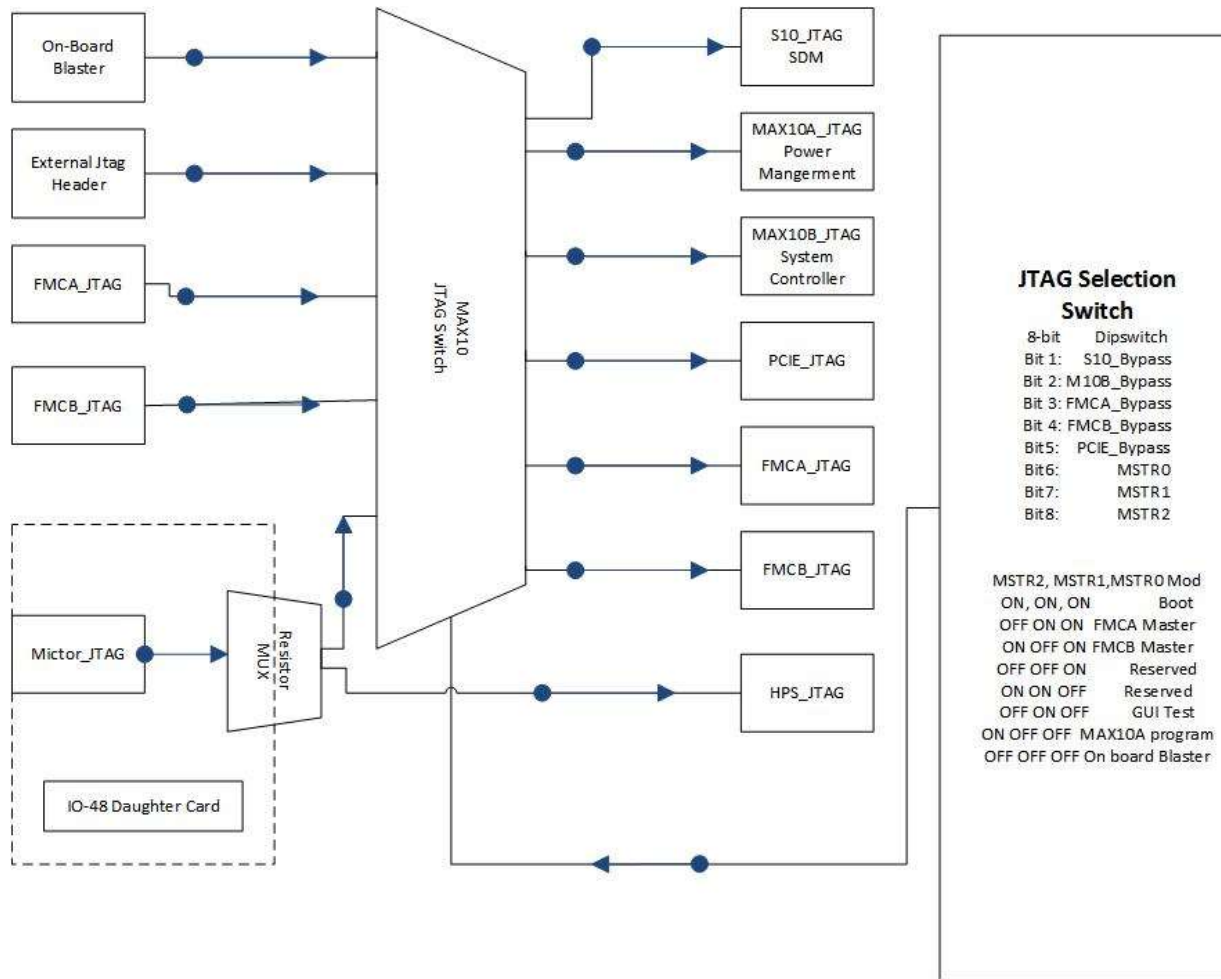
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# S10soc Dev Kit Reset Block



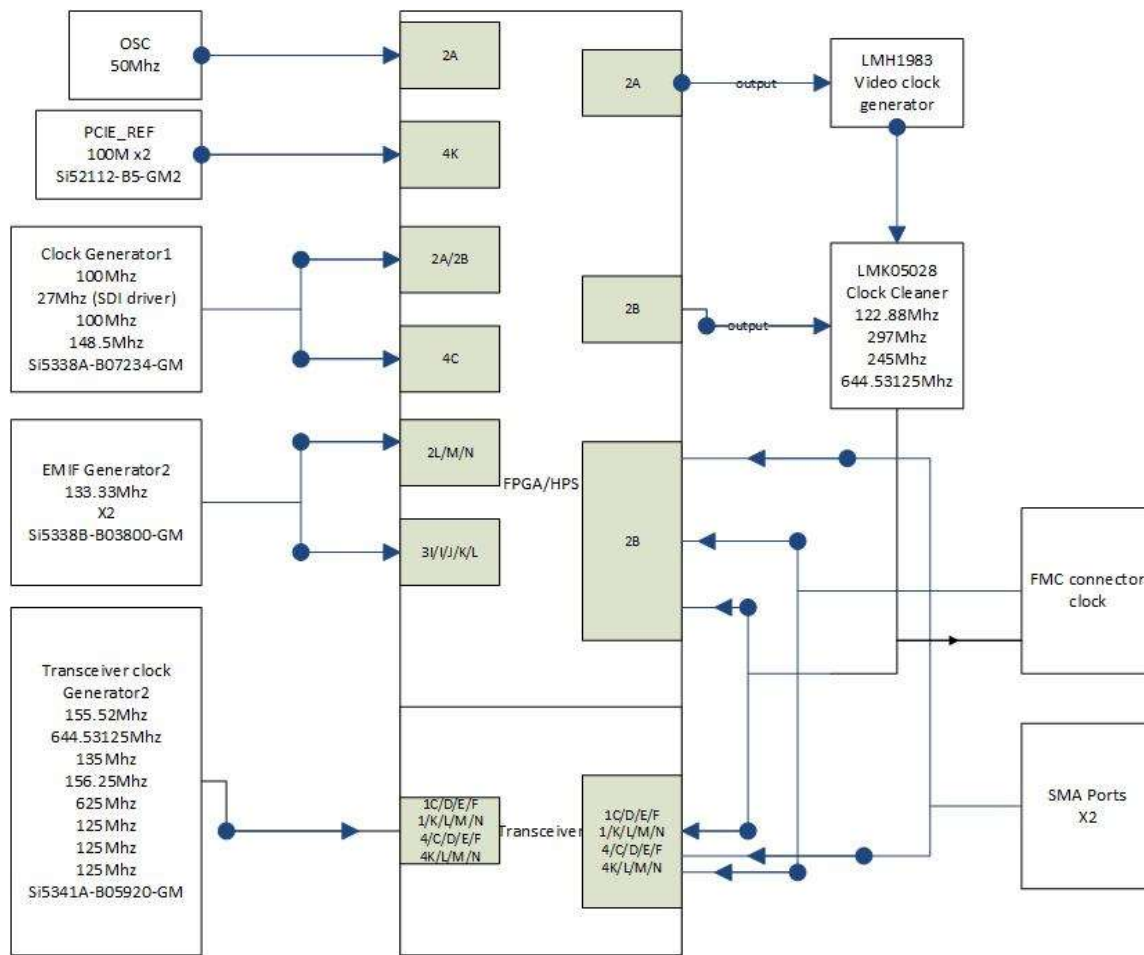
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# JTAG Connection Diagram



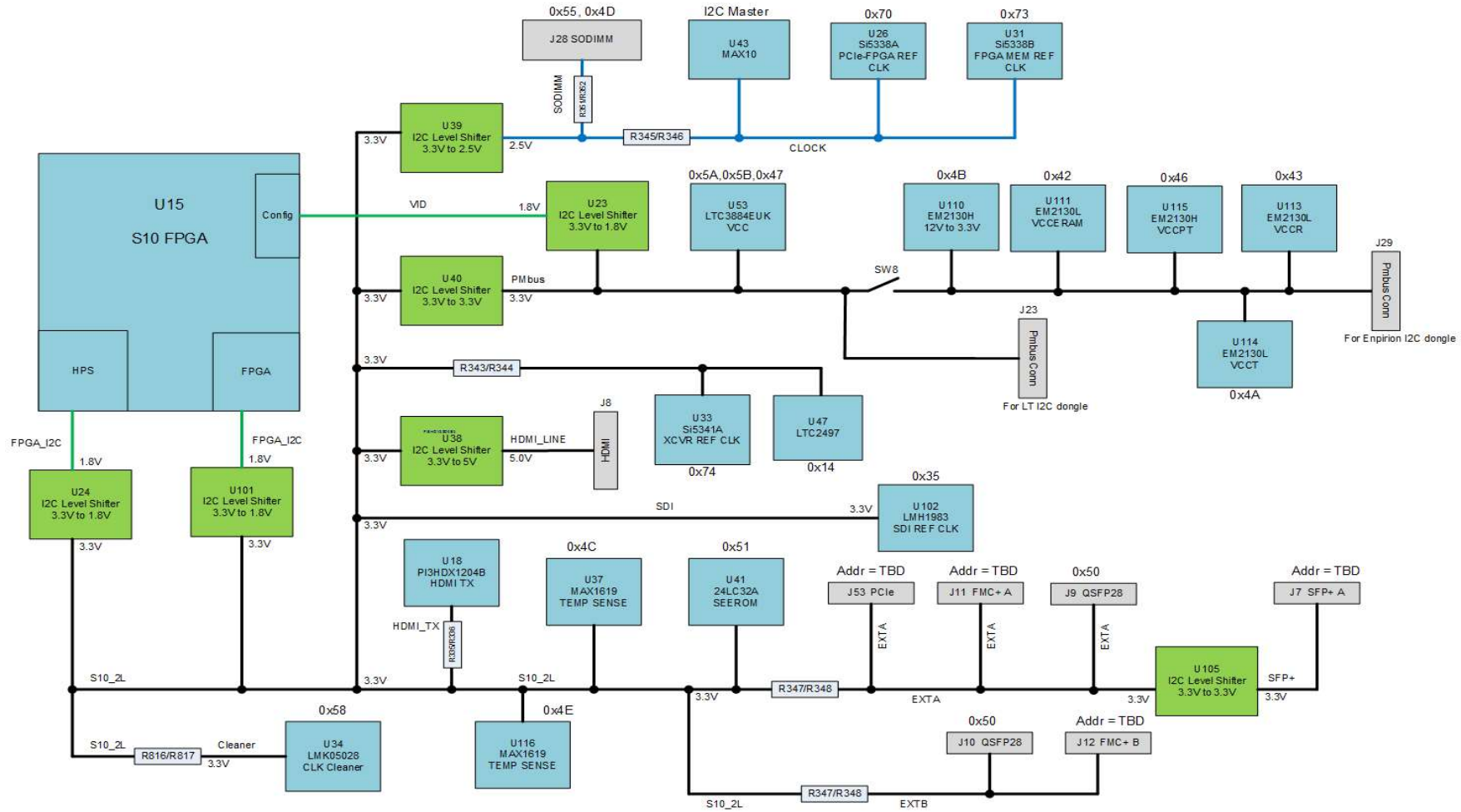
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# Stratix 10 Dev Kit Clock Connection



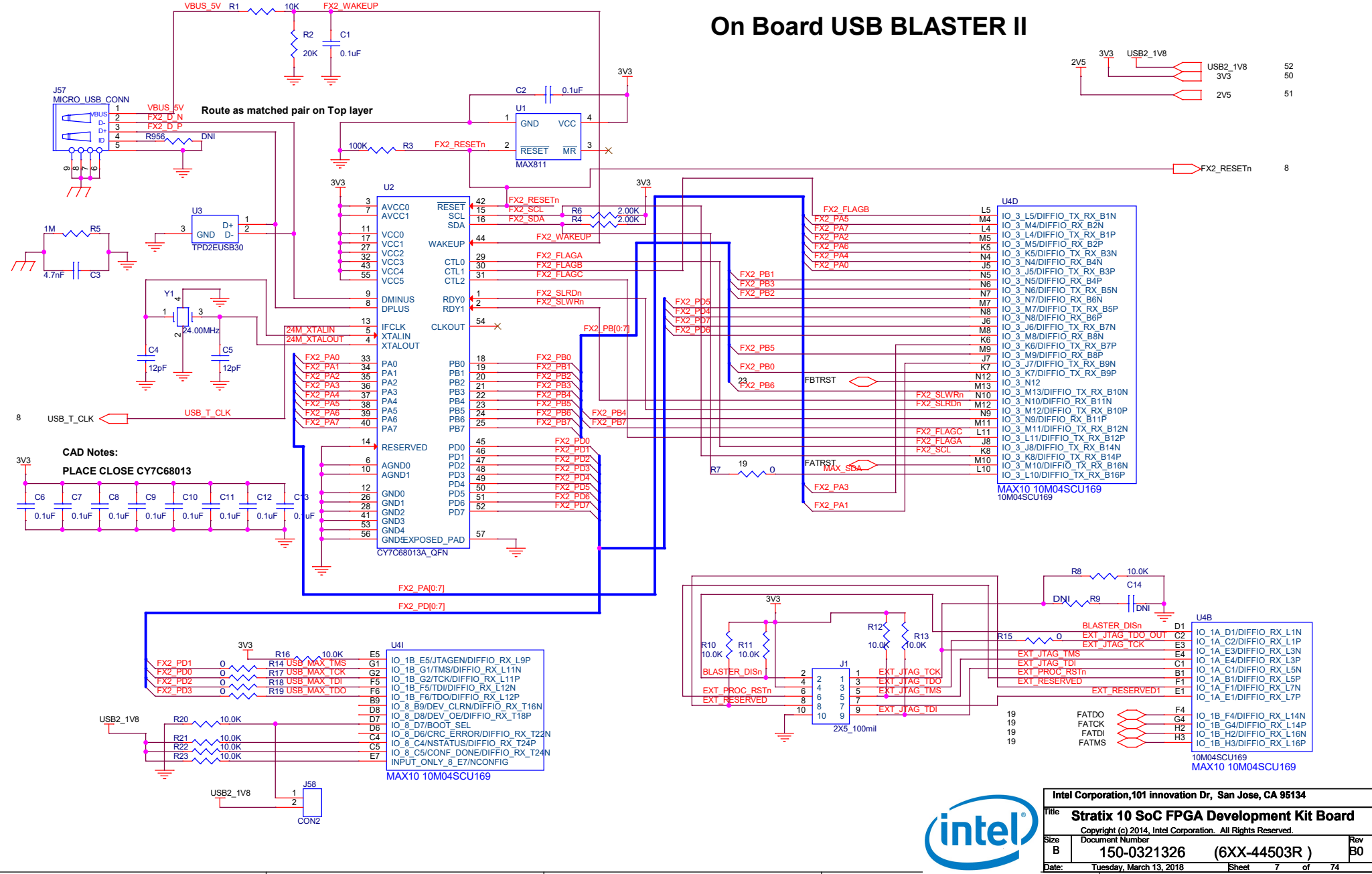
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# S10 SoC I2C Bus Connection



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# On Board USB BLASTER II



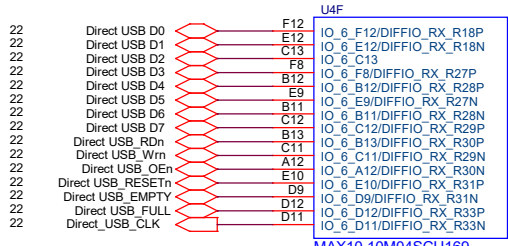
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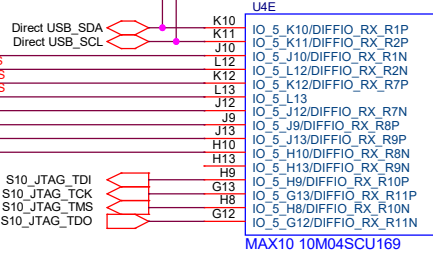
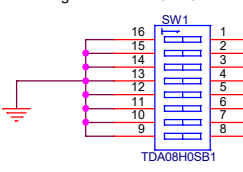
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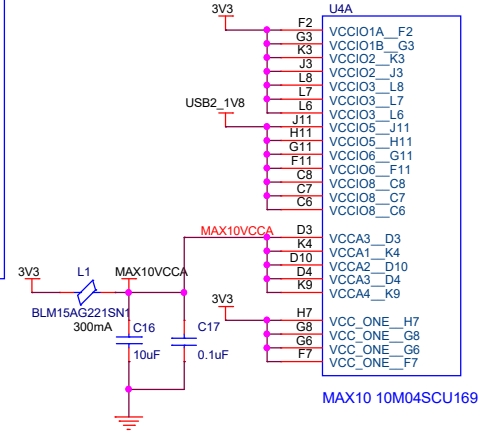
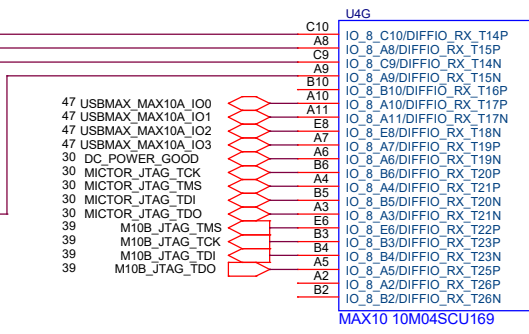
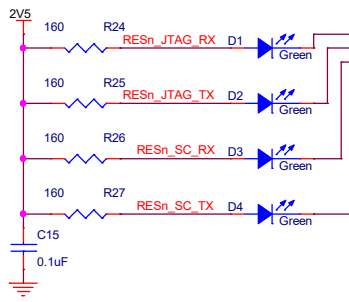
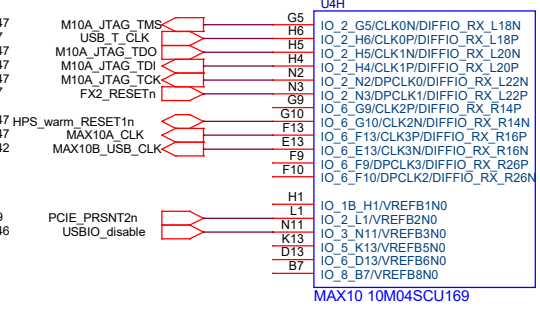
# On Board USB BLASTER II 2, JTAGSwitch



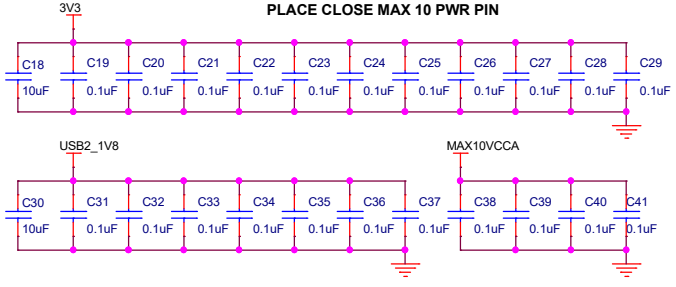
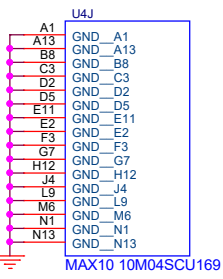
Logic 0 = Device JTAG Bypass  
Logic 1 = Device JTAG Enable



MSTR2	MSTR1	MSTR0	Mode
ON	ON	ON	BOOT
OFF	ON	ON	FMCA Master
ON	OFF	ON	FMCB Master
OFF	ON	ON	RESERVED
ON	ON	OFF	RESERVED
OFF	ON	OFF	GUI Test
ON	OFF	OFF	MAX10A Progrom Mode
OFF	OFF	OFF	ON-board UBII



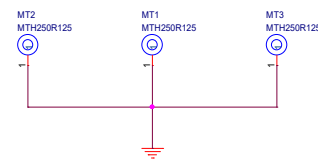
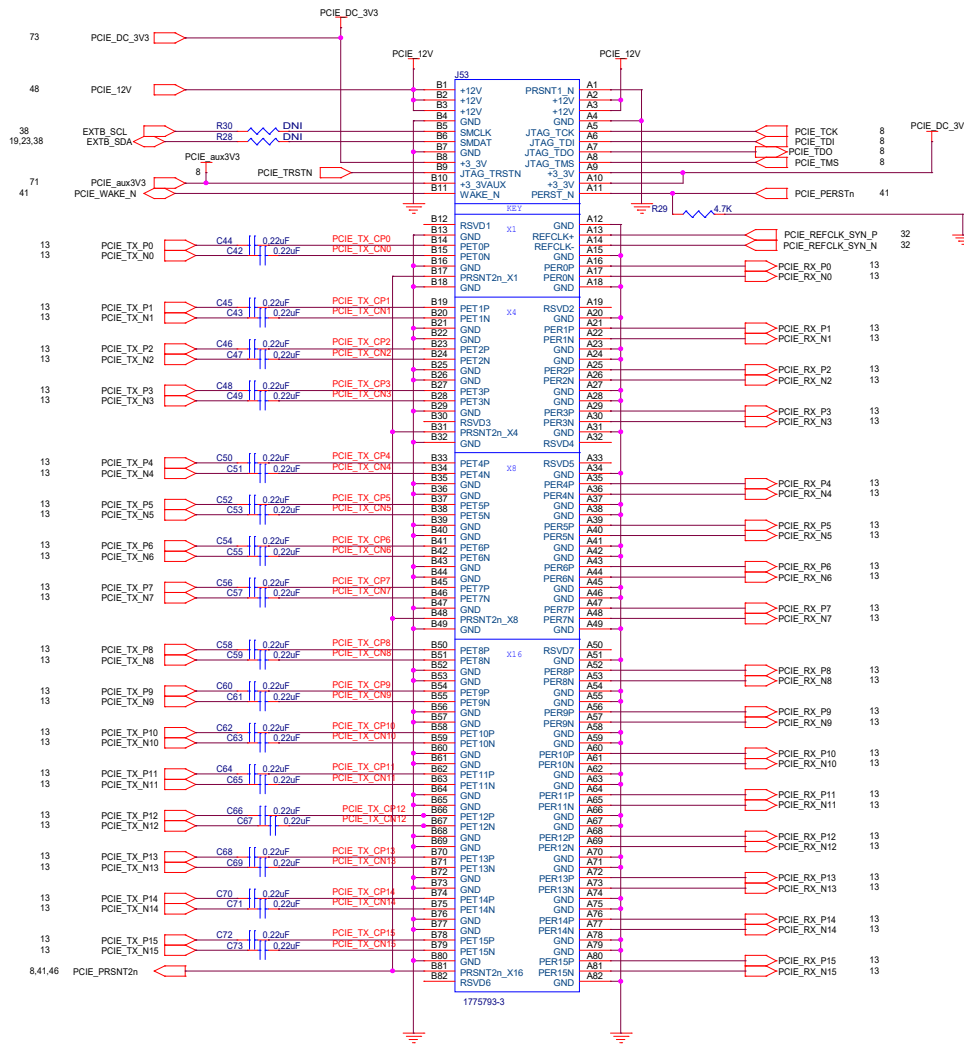
CAD Notes:  
PLACE CLOSE MAX 10 PWR PIN



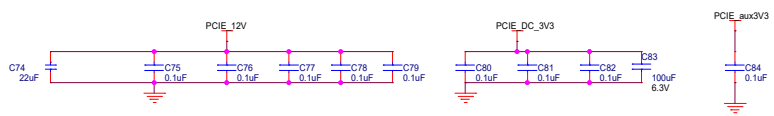
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# PCI Express GEN3 X 16 Connector

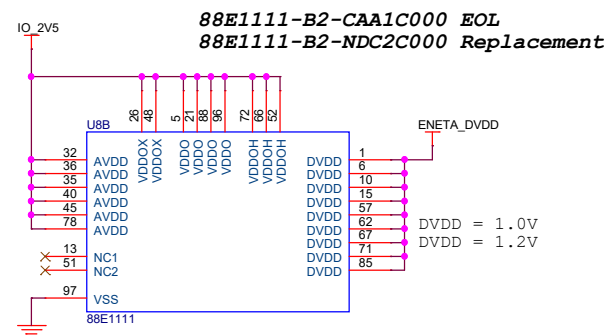
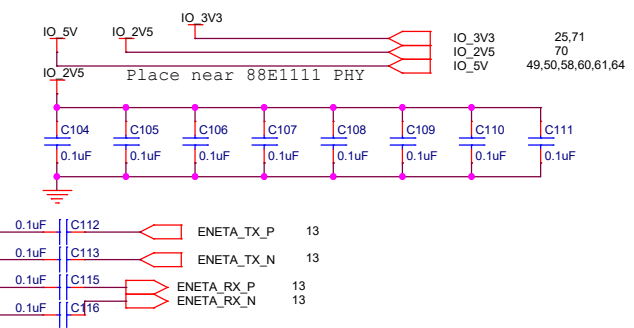
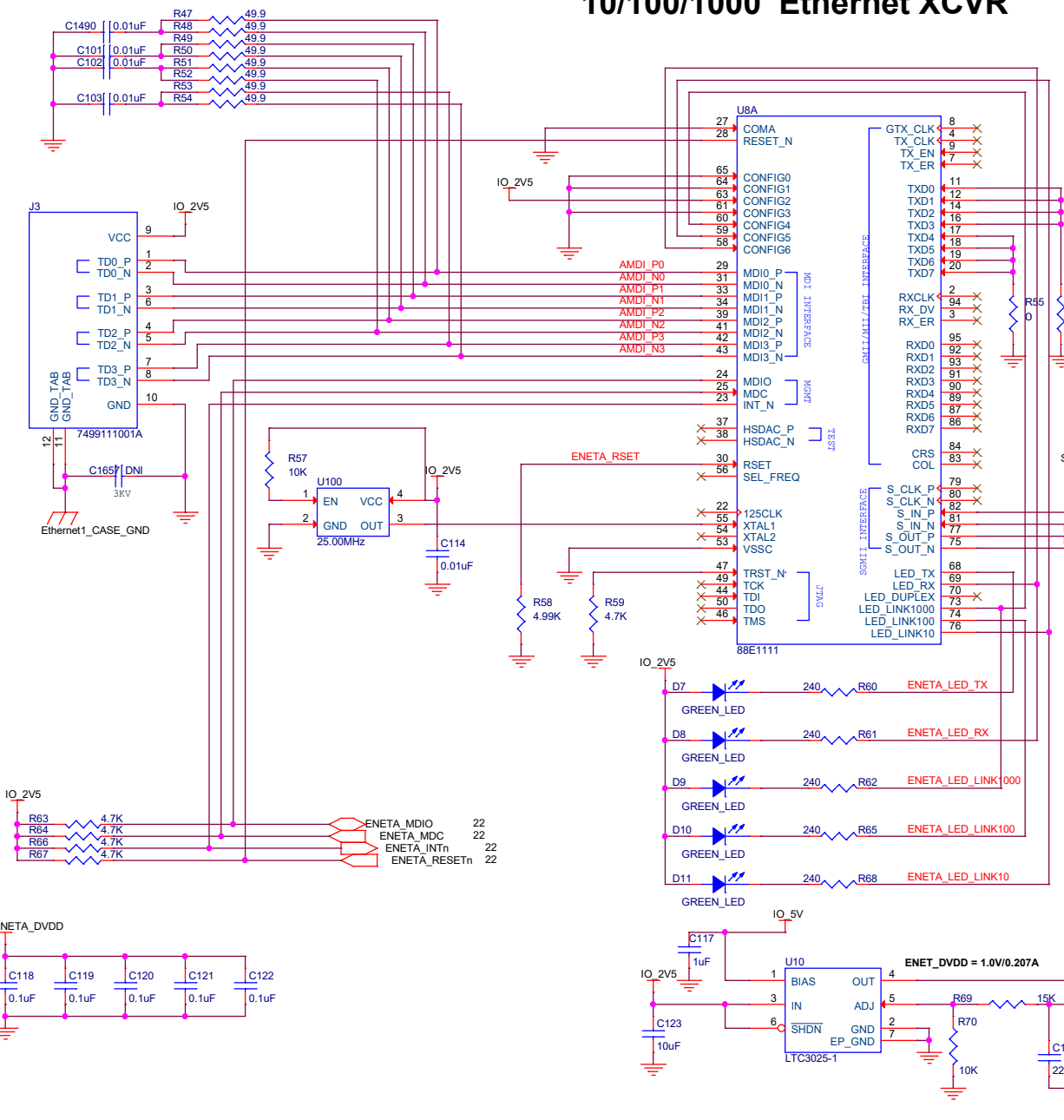


75-ohm to 100-ohm XCVR traces.



# 10/100/1000 Ethernet XCVR

Pin	Pin Connection	Setting Bit[2:0]	Definition
CONFIG0	GND	000	MDIO PHY Address bit (2:0) = 000
CONFIG1	GND	000	Enable Pause, PHY Address bits (4:3) = 00
CONFIG2	VDDO (2.5V or 3.3V)	111	1110 = Auto-negotiate, advertise all capabilities, prefer Master 100BASE-x FULL-DUPLEX/Auto-Negotiation enabled, 100BASE-X half-duplex
CONFIG3	GND	000	Disable crossover, Enable 125CLK
CONFIG4	LED_LINK1000	100	Hardware Config Mode Reg (2:0) = 100 SGMII without Clock with SGMII Auto-Neg to copper
CONFIG5	LED_LINK10	110	Disable fiber/copper autoselect, disable sleep mode (enable energy detect), Hardware Config Mode Reg (3) = 0
CONFIG6	LED_RX	010	Select MDIO (over 2-wire serial), interrupt polarity = active low, 50-ohm termination for fiber



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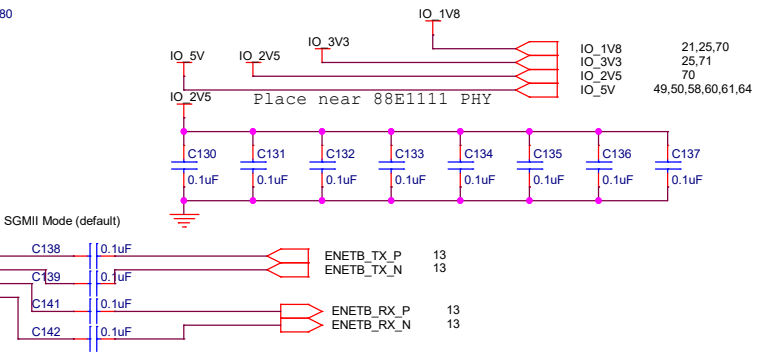
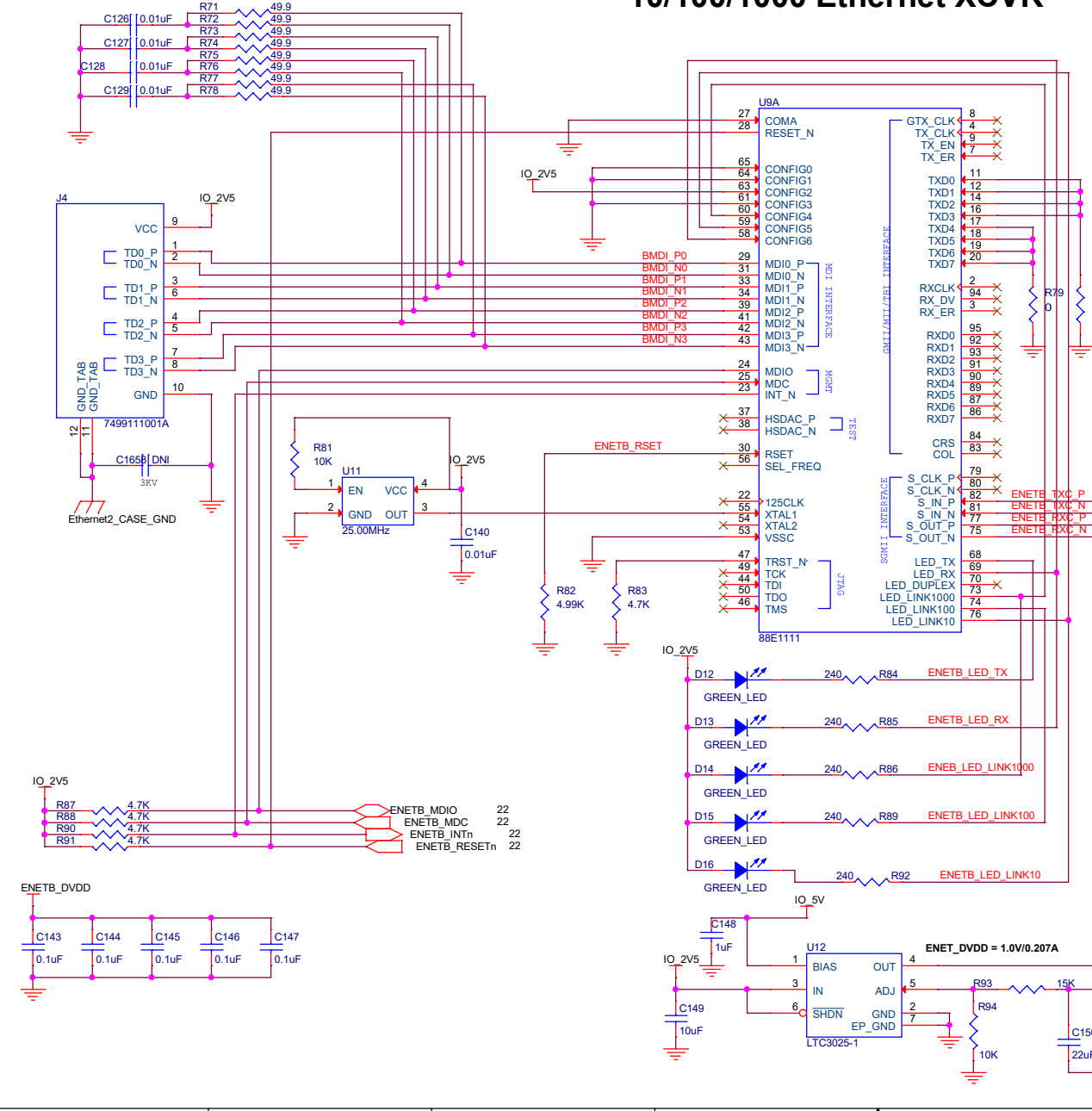
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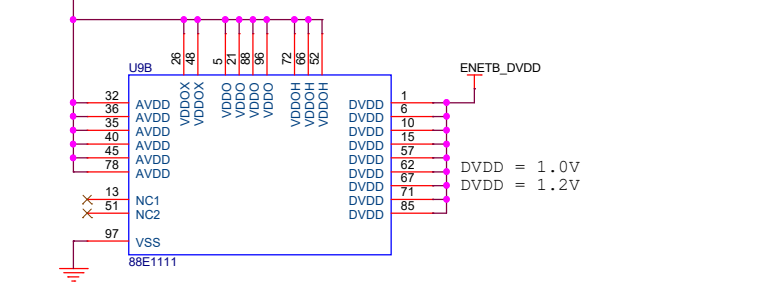
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# 10/100/1000 Ethernet XCVR

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CONFIG0	GND	000	MDIO PHY Address bit (2:0) = 000
CONFIG1	GND	000	Enable Pause, PHY Address bits (4:3) = 00
CONFIG2	VDDO (2.5V or 3.3V)	111	1110 = Auto-negotiate, advertise all capabilities, prefer Master 100BASE-x FULL-DUPLEX/Auto-Negotiation enabled, 100BASE-X half-duplex
CONFIG3	GND	000	Disable crossover, Enable 125CLK
CONFIG4	LED_LINK1000	100	Hardware Config Mode Reg (2:0) = 100 SGMII without Clock with SGMII Auto-Neg to copper
CONFIG5	LED_LINK10	110	Disable fiber/copper autoselect, disable sleep mode (enable energy detect), Hardware Config Mode Reg (3) = 0
CONFIG6	LED_RX	010	Select MDIO (over 2-wire serial), interrupt polarity = active low, 50-ohm termination for fiber



**88E1111-B2-CAA1C000 EOL**  
**88E1111-B2-NDC2C000 Replacement**



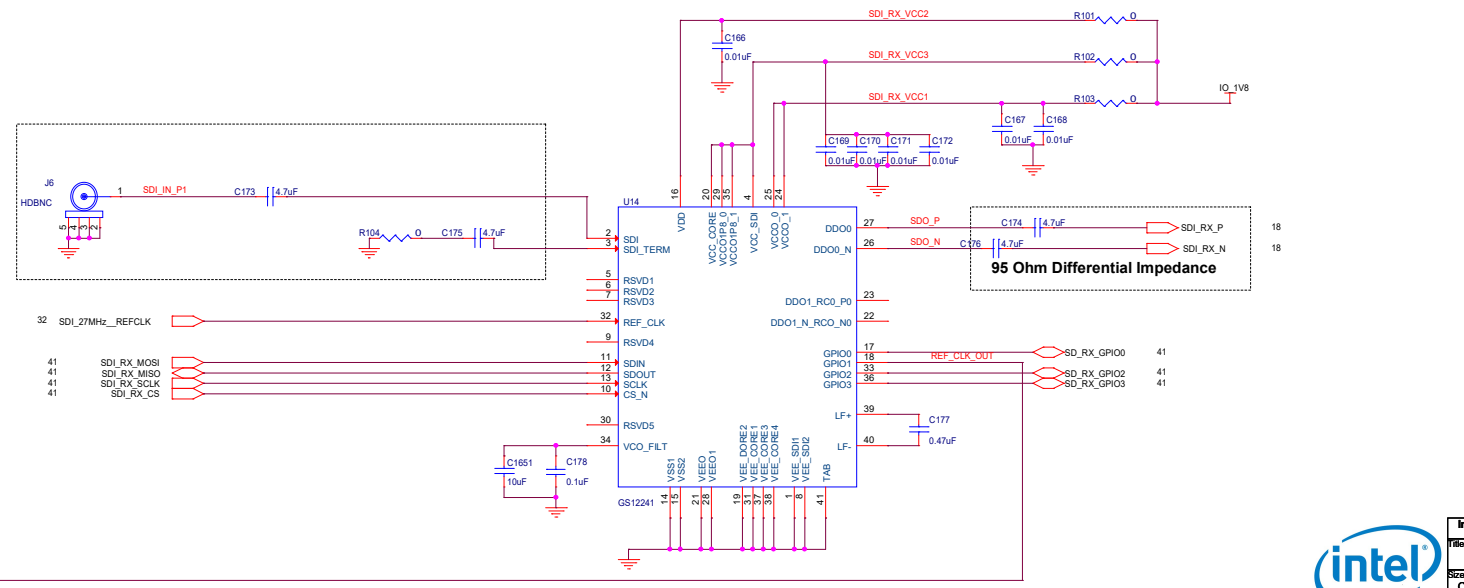
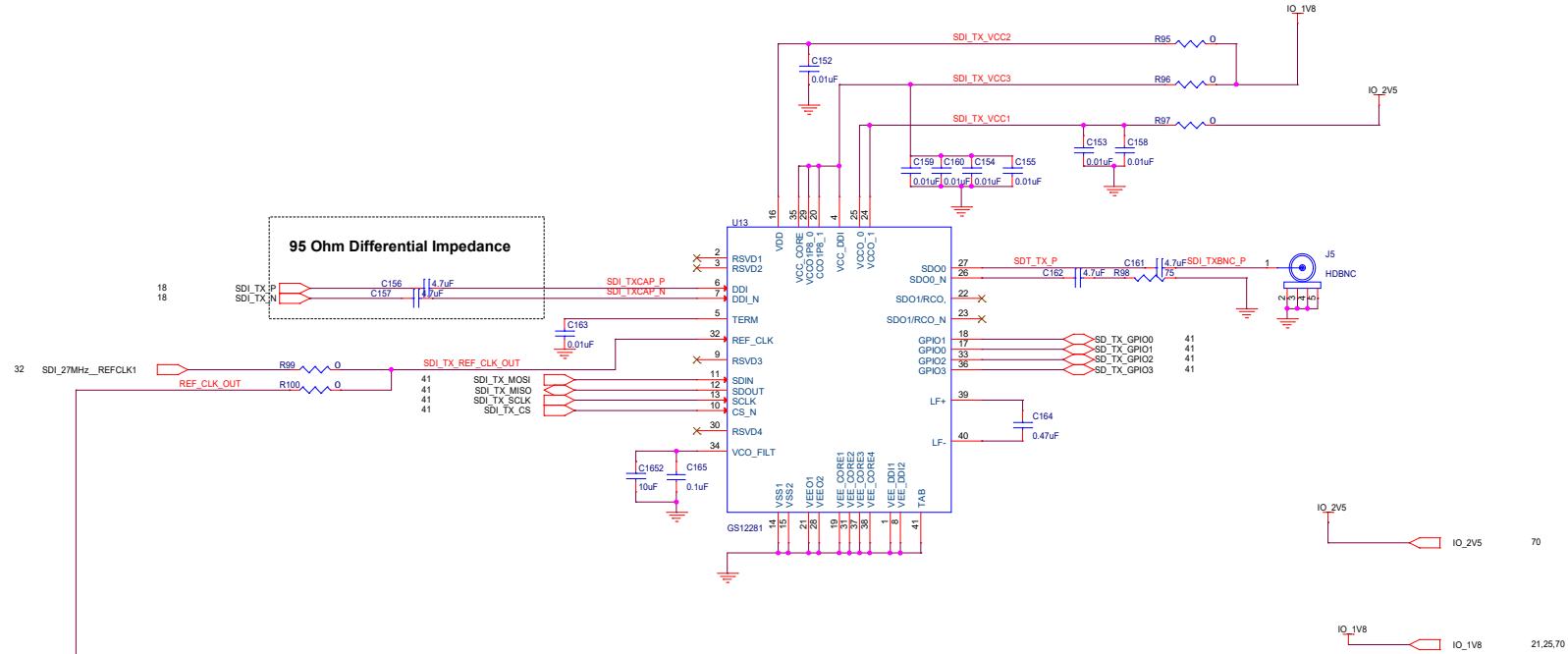
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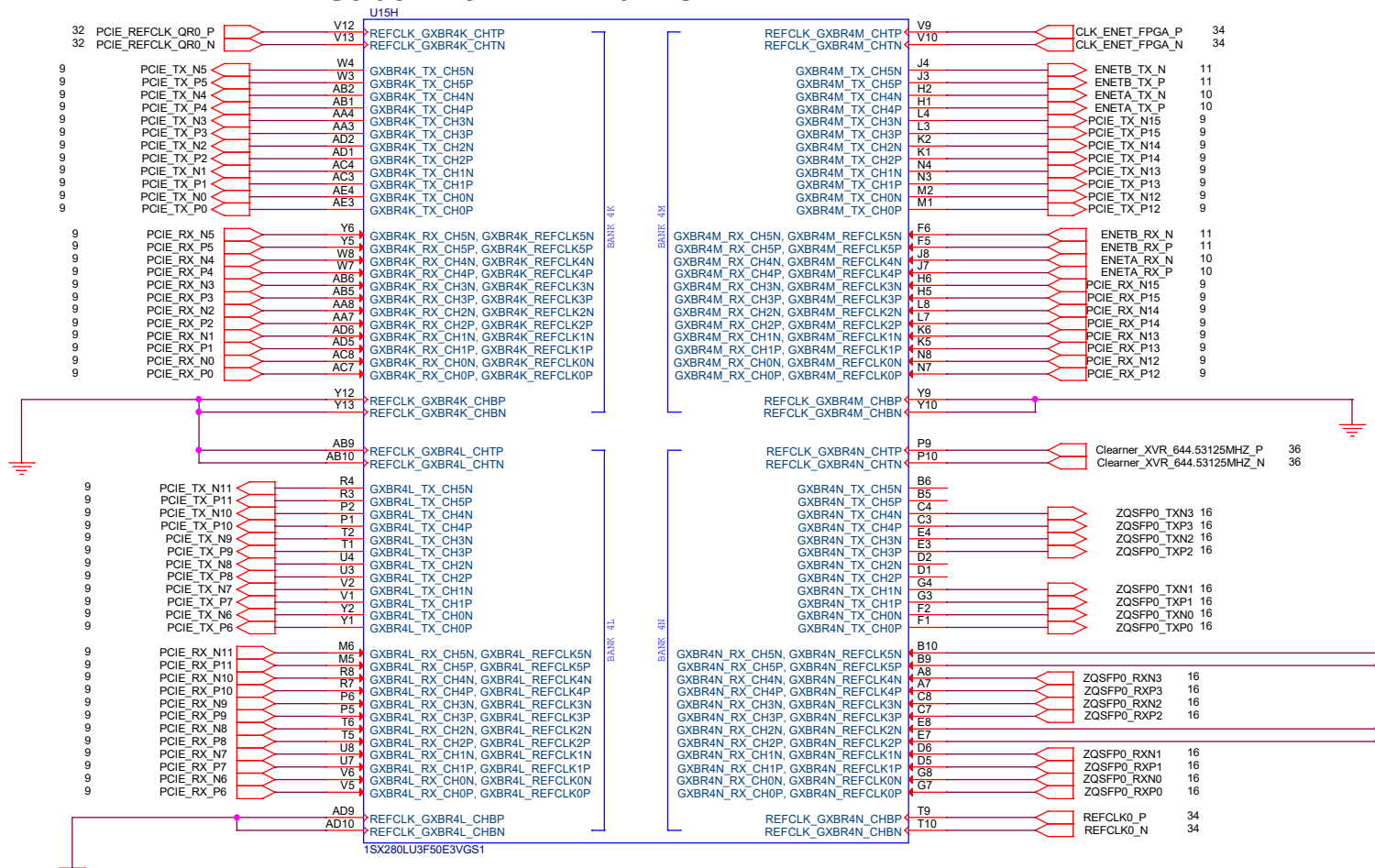
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# SDI Cable Driver, Equalizer, and SMB

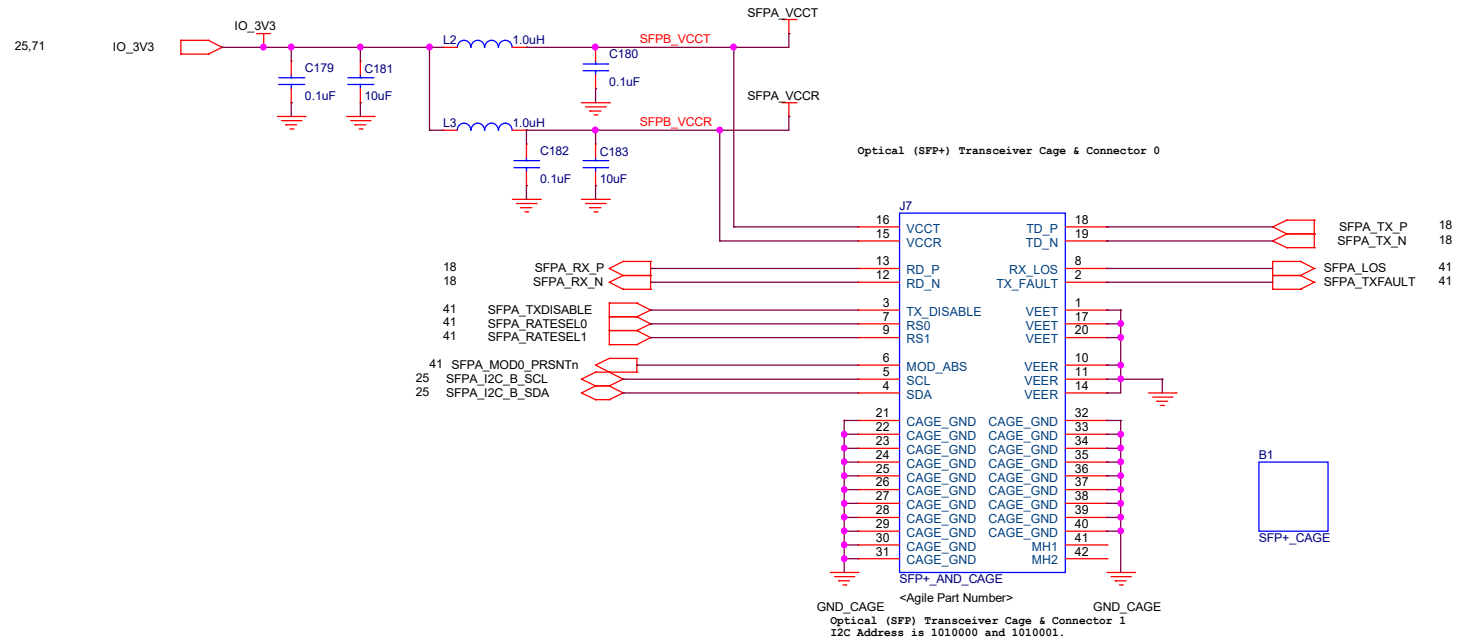


# Stratix 10 XCVR Banks - 4K/L/M/N



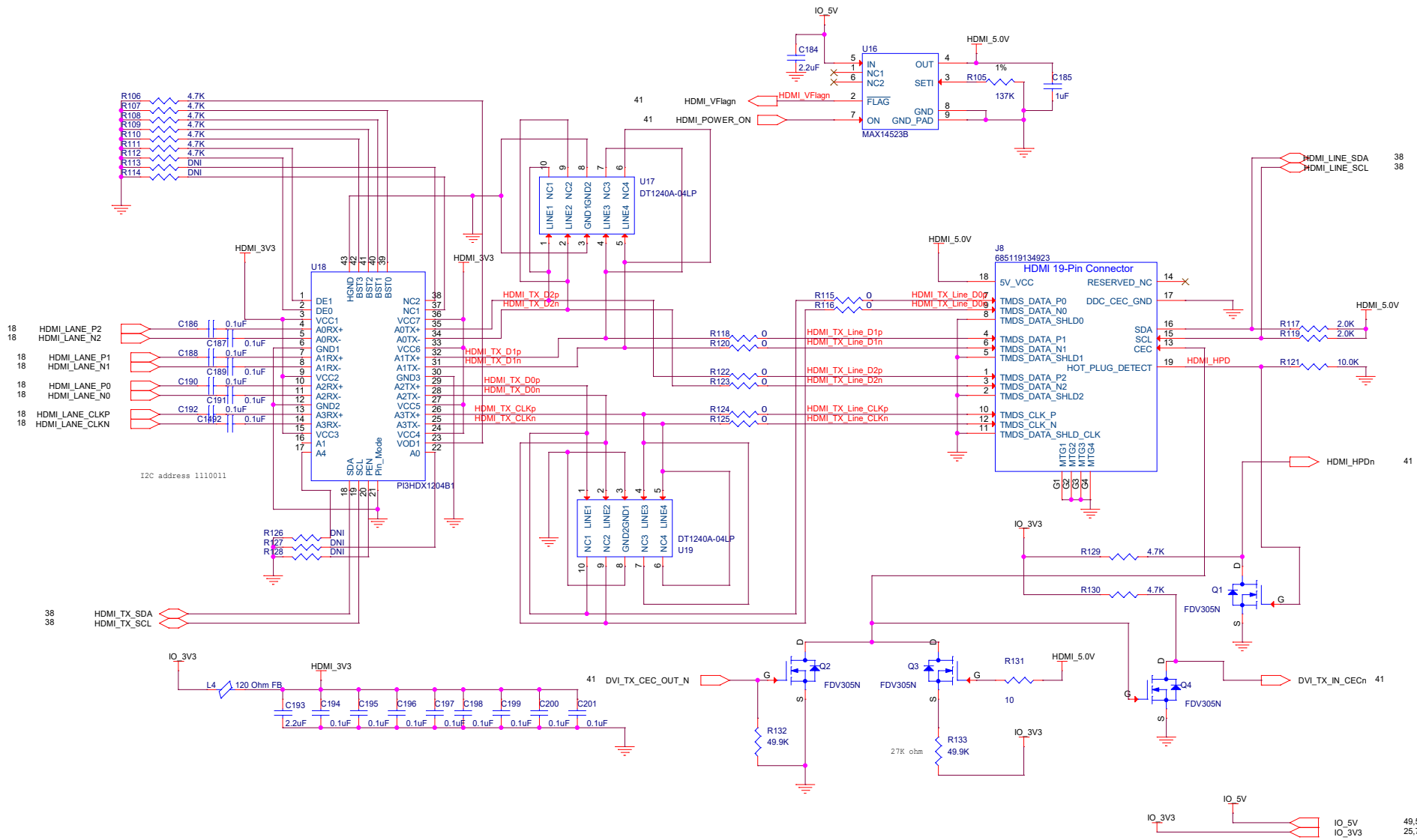
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# Small Form Factor Pluggable Plus (SFP+) Port A



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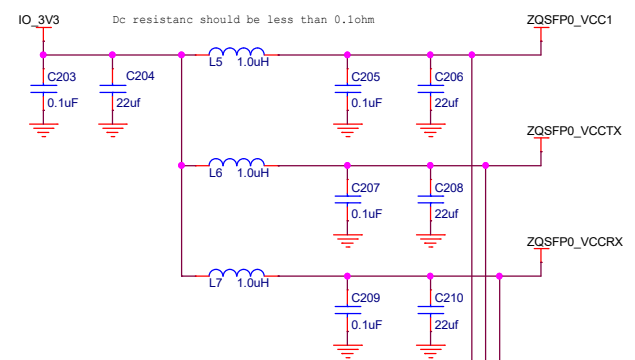
# HDMI (VIDEO ONLY)



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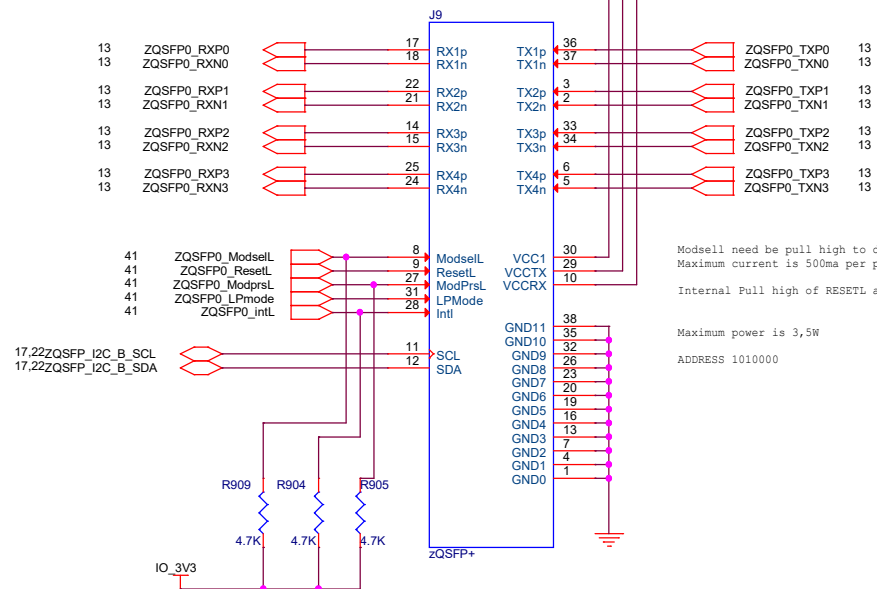
49,50,58,60,61,64  
25,71

# QSFP28 Interface 0 & MXP Cable connection

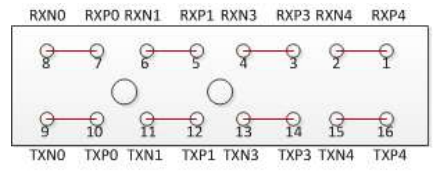
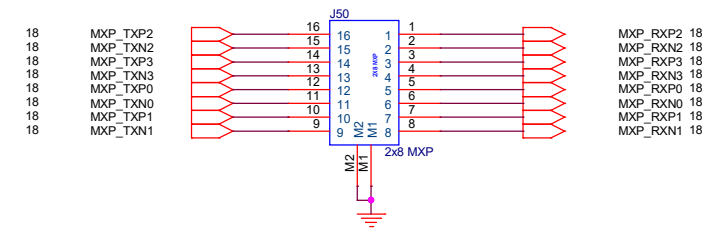
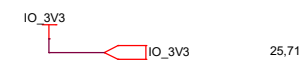
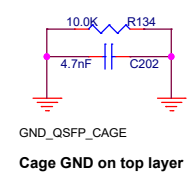
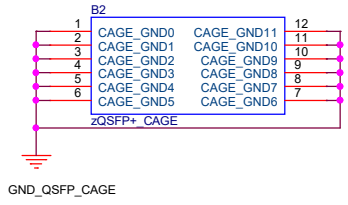


P and N can be swapped for better SI performance

## QSFP28 Interface



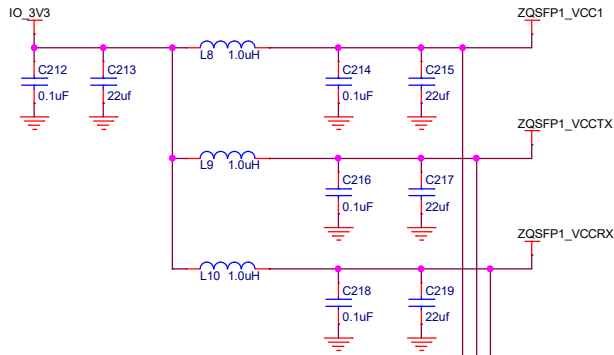
ModselL need be pull high to disabel I2C bus  
 Maximum current is 500ma per pin  
 Internal Pull high of RESETL and LPMode  
 Maximum power is 3,5W  
 ADDRESS 1010000



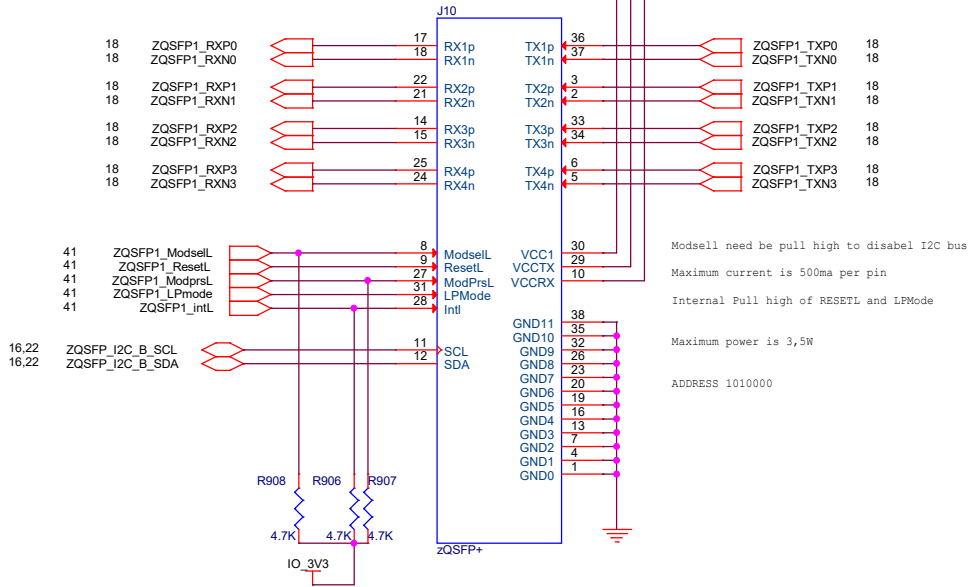


# QSFP28 Interface 1

Dc resistanc should be less than 0.1ohm

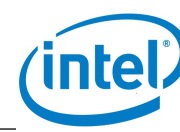
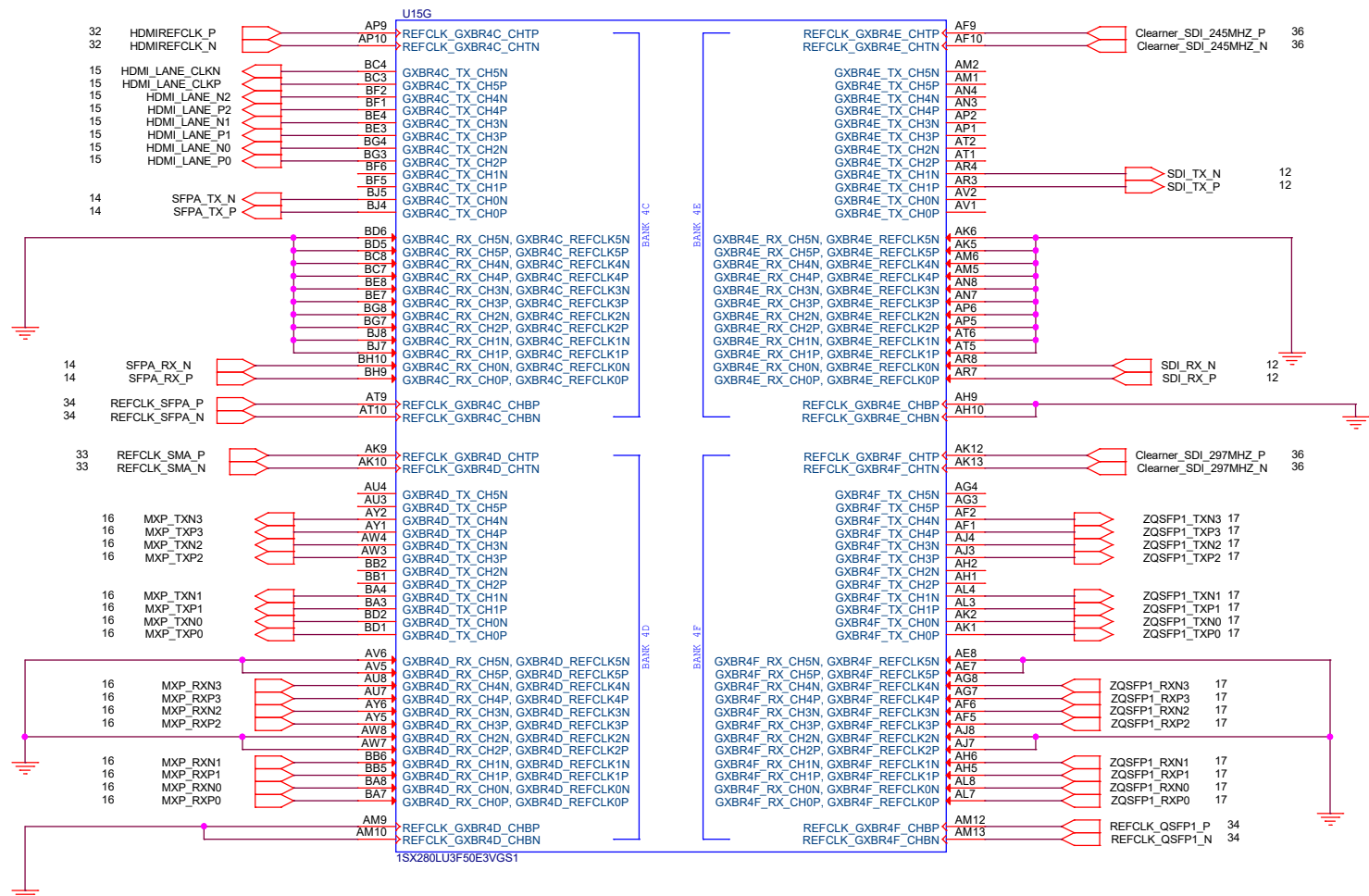


## QSFP28 Interface



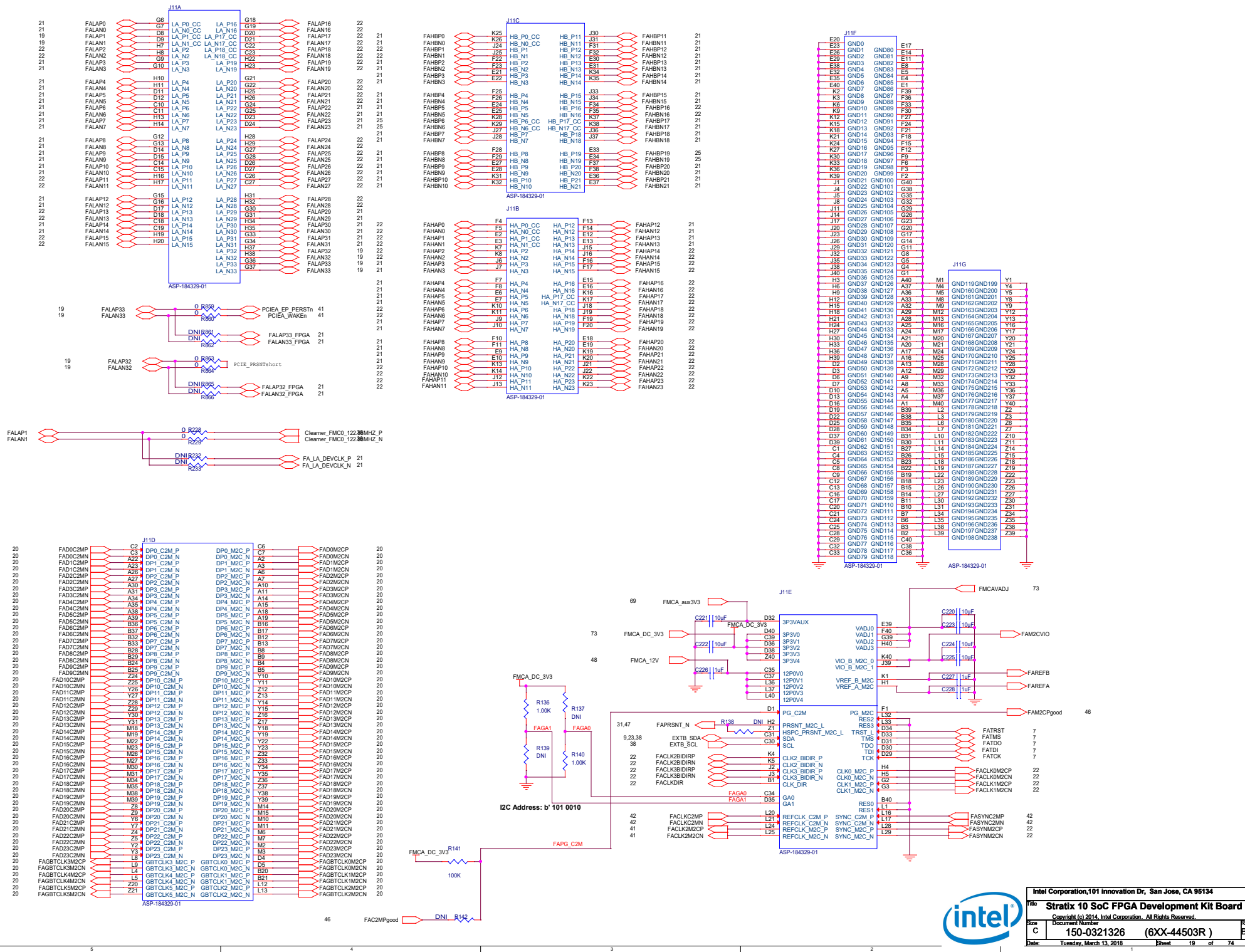
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# S10 XCVR Banks - 4C/D/E/F

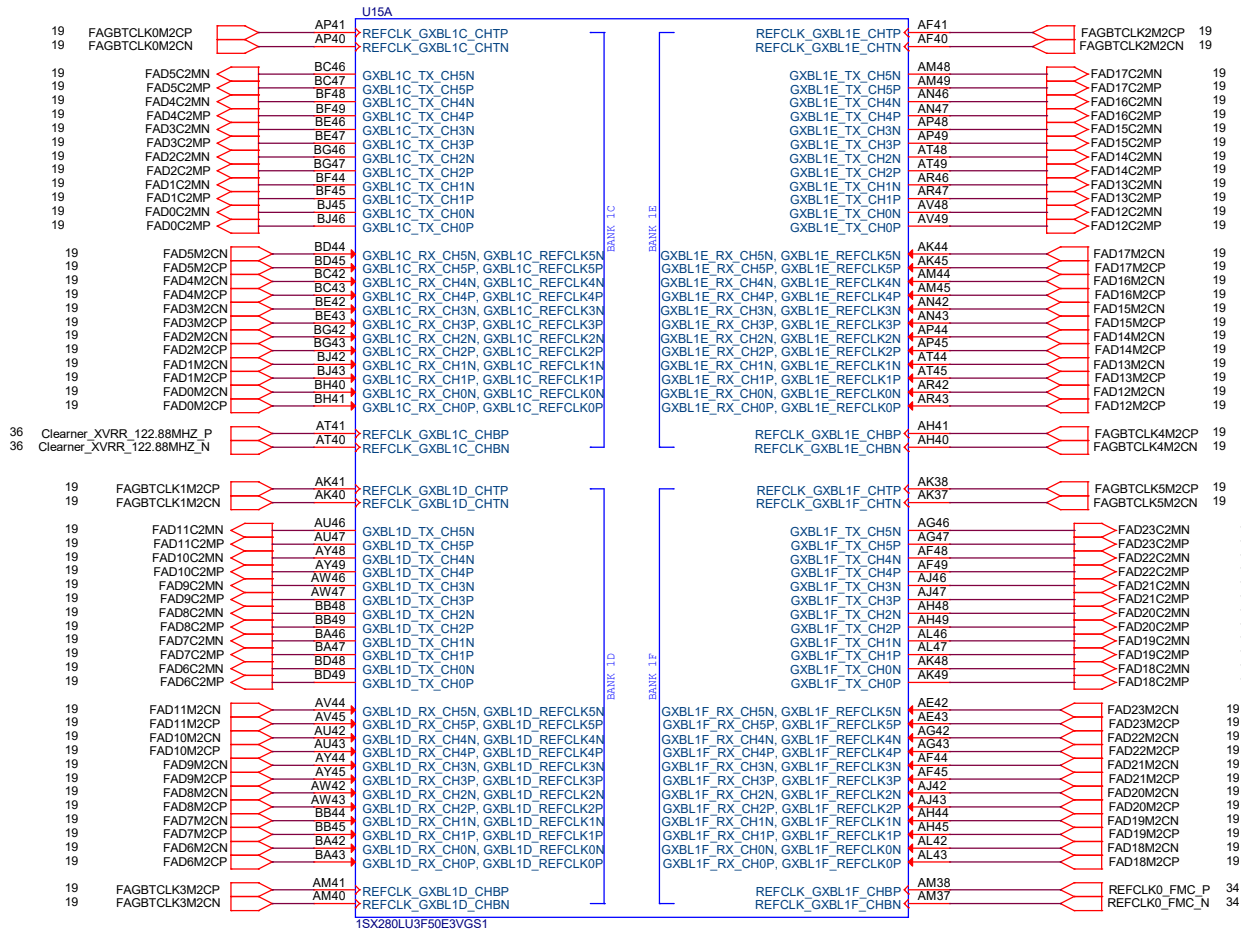


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# FMC Port A

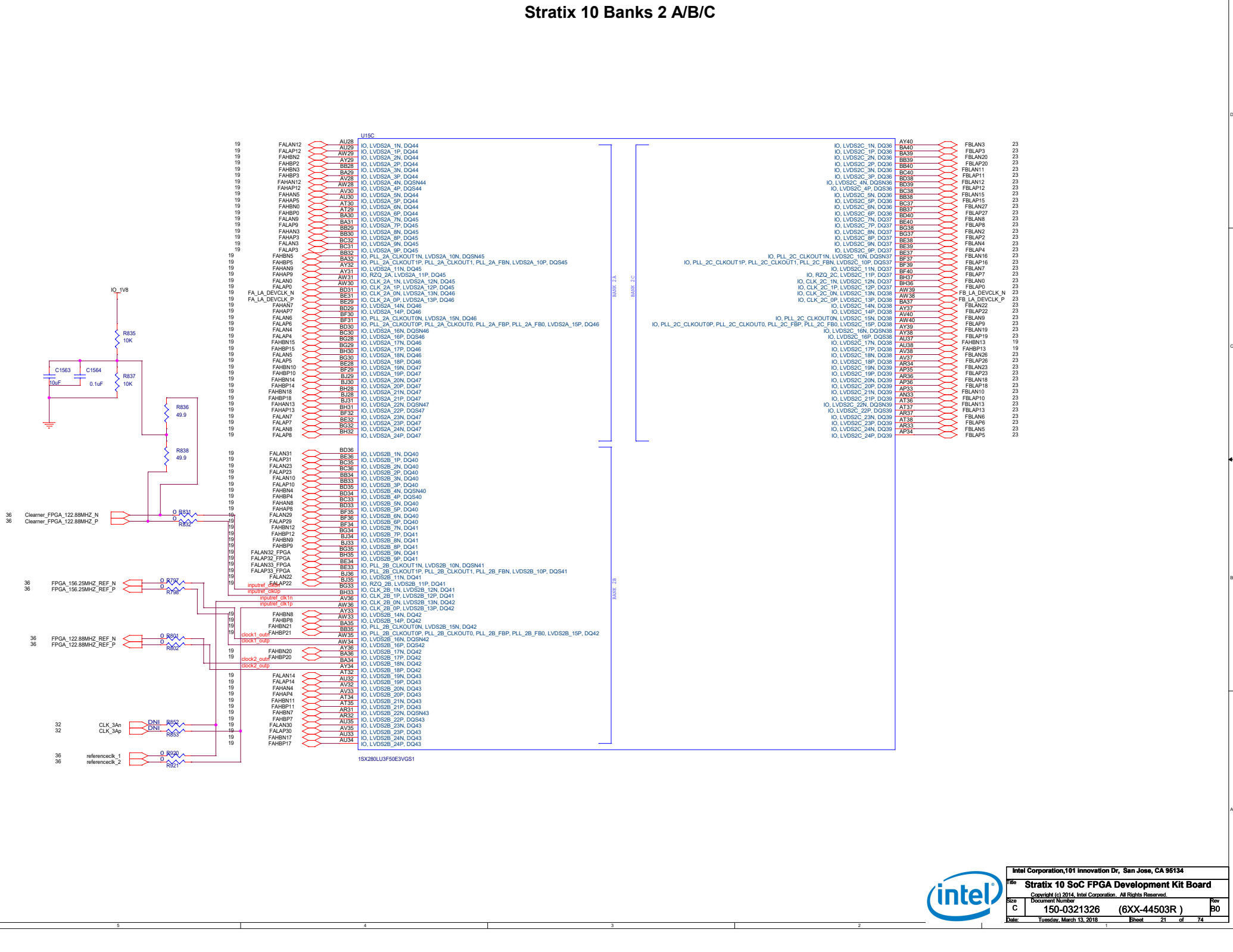


# Stratix 10 XCVR Banks - 1C/D/E/F

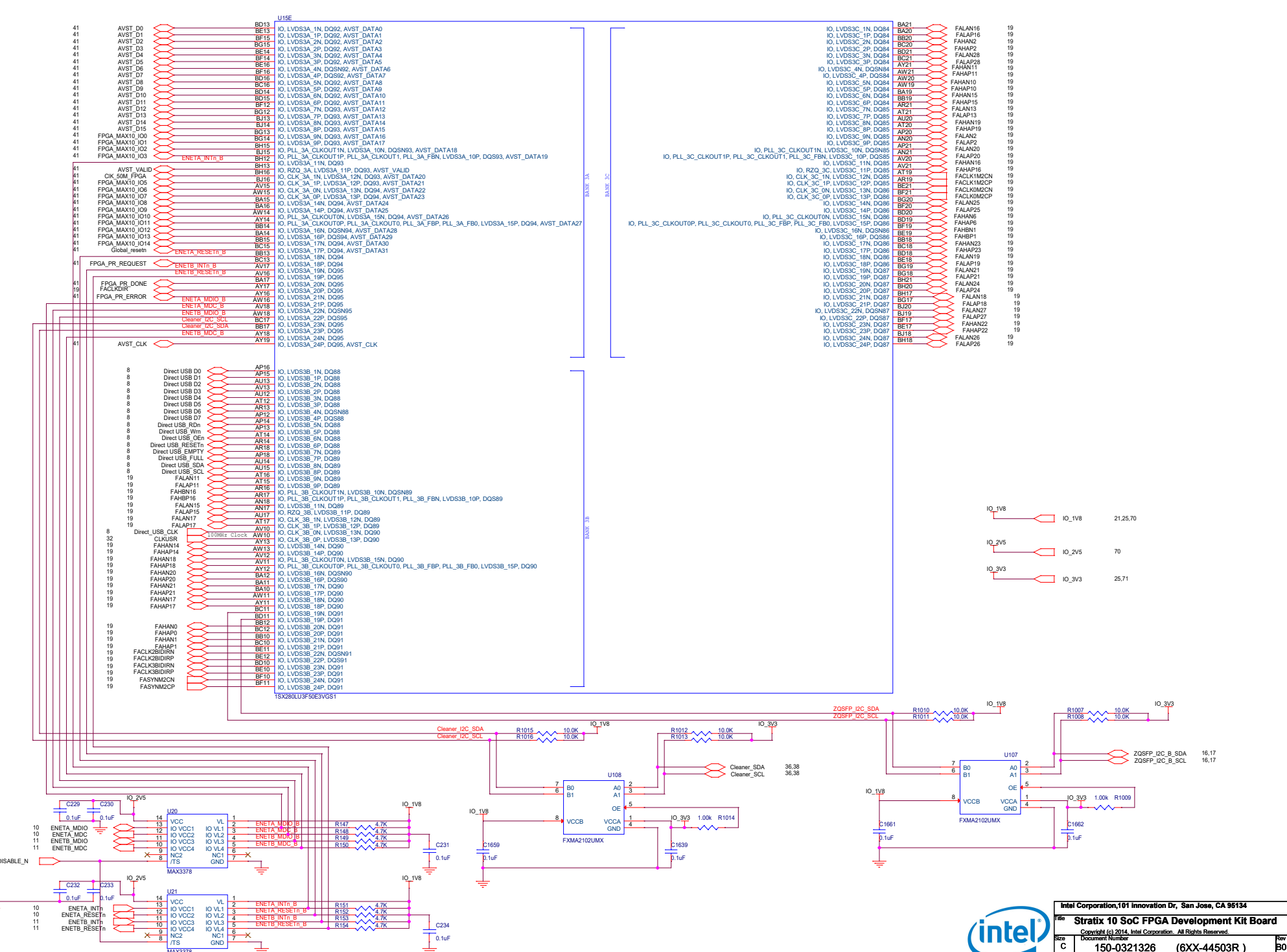


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# Stratix 10 Banks 2 A/B/C



# Stratix 10 Banks - 3 A/B/C



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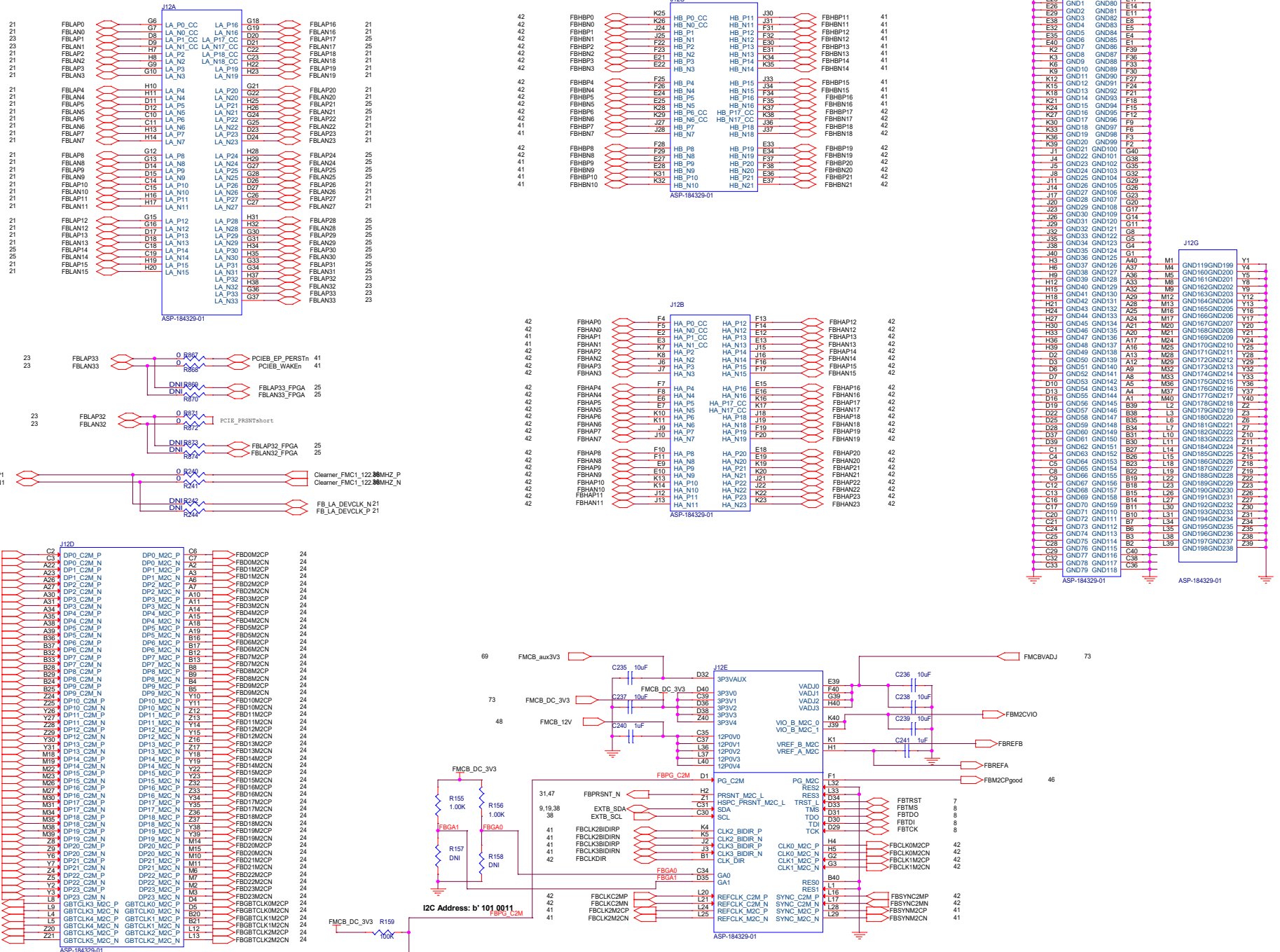
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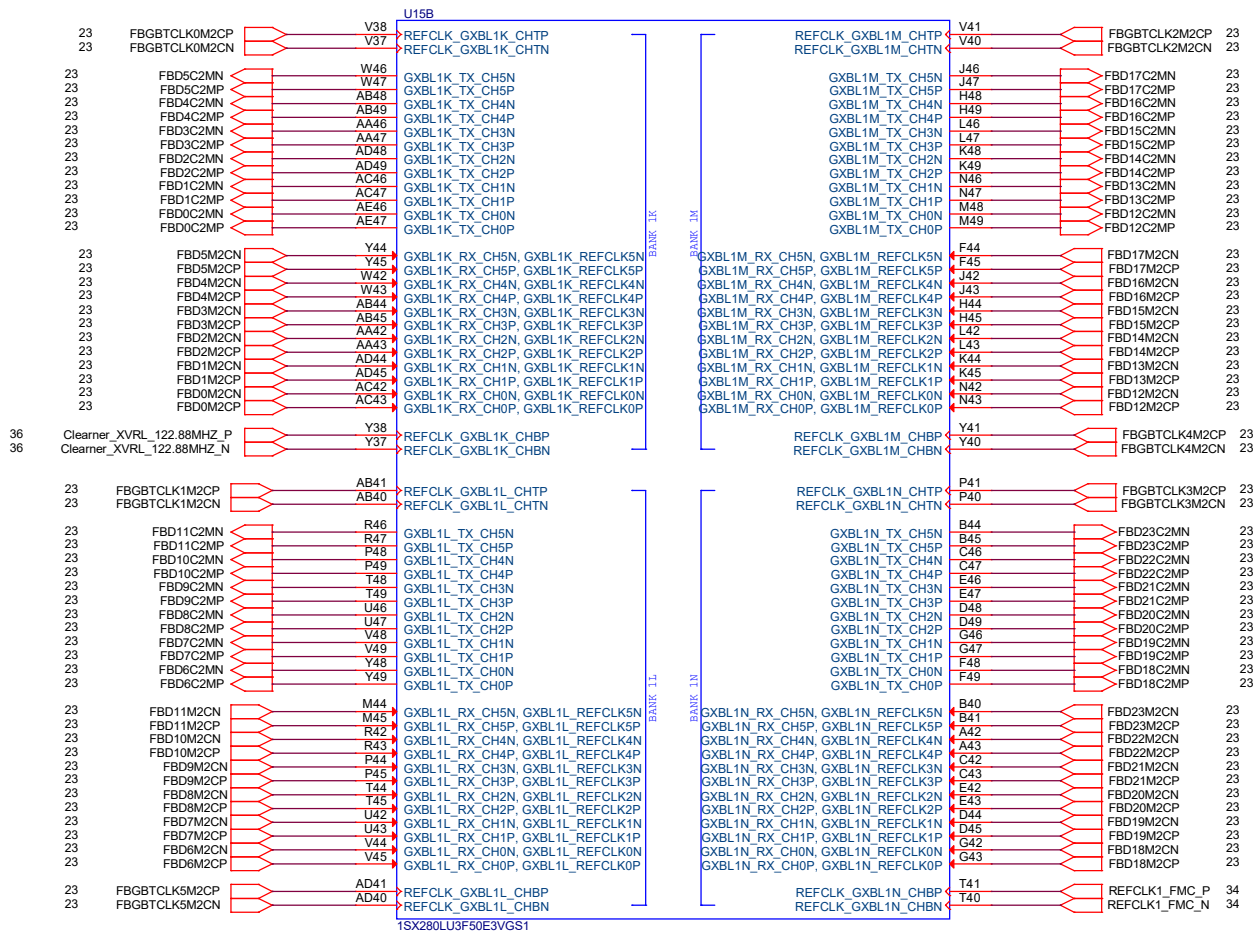
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# FMC Port B

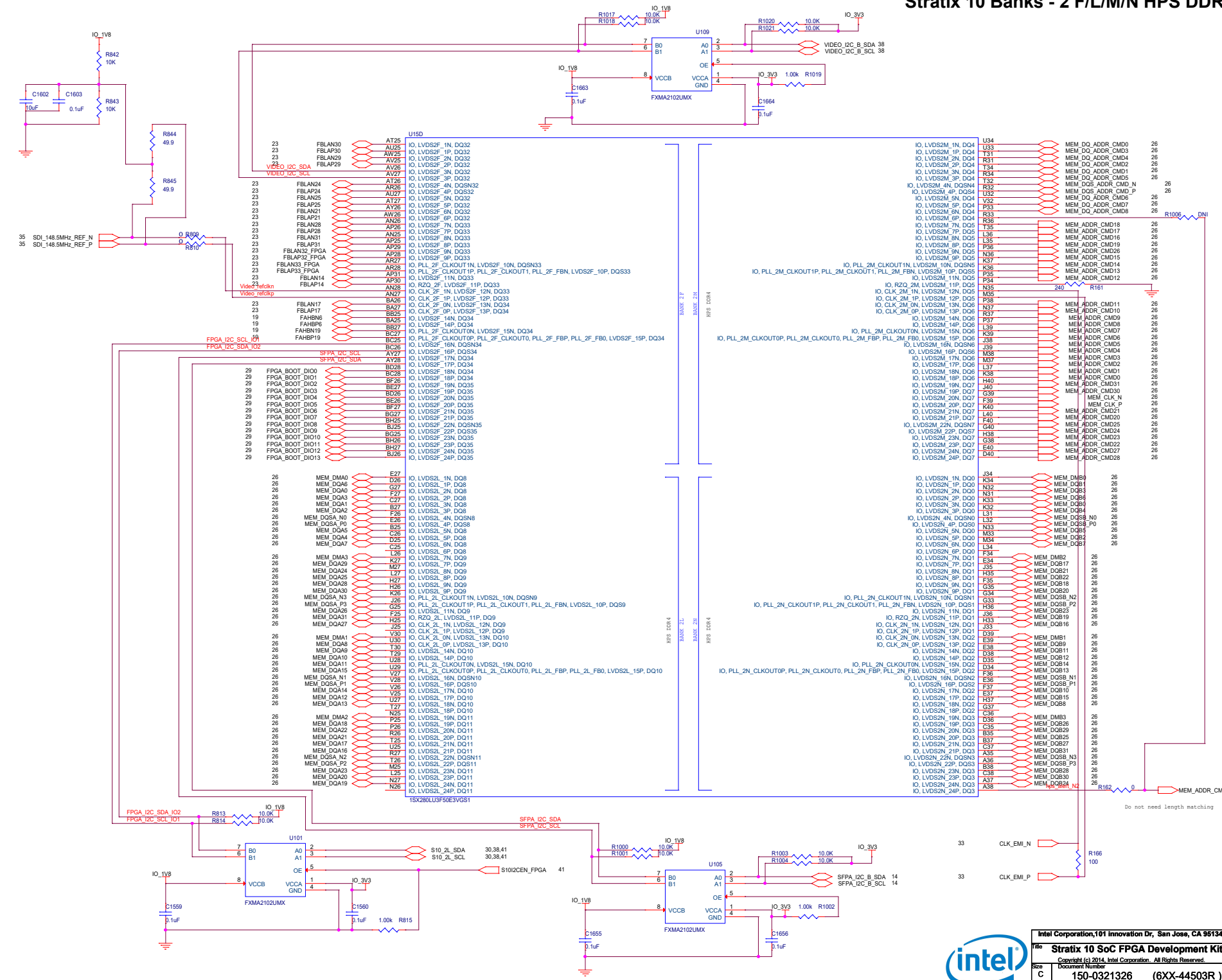


# Stratix 10 XCVR Banks - 1K/L/M/N



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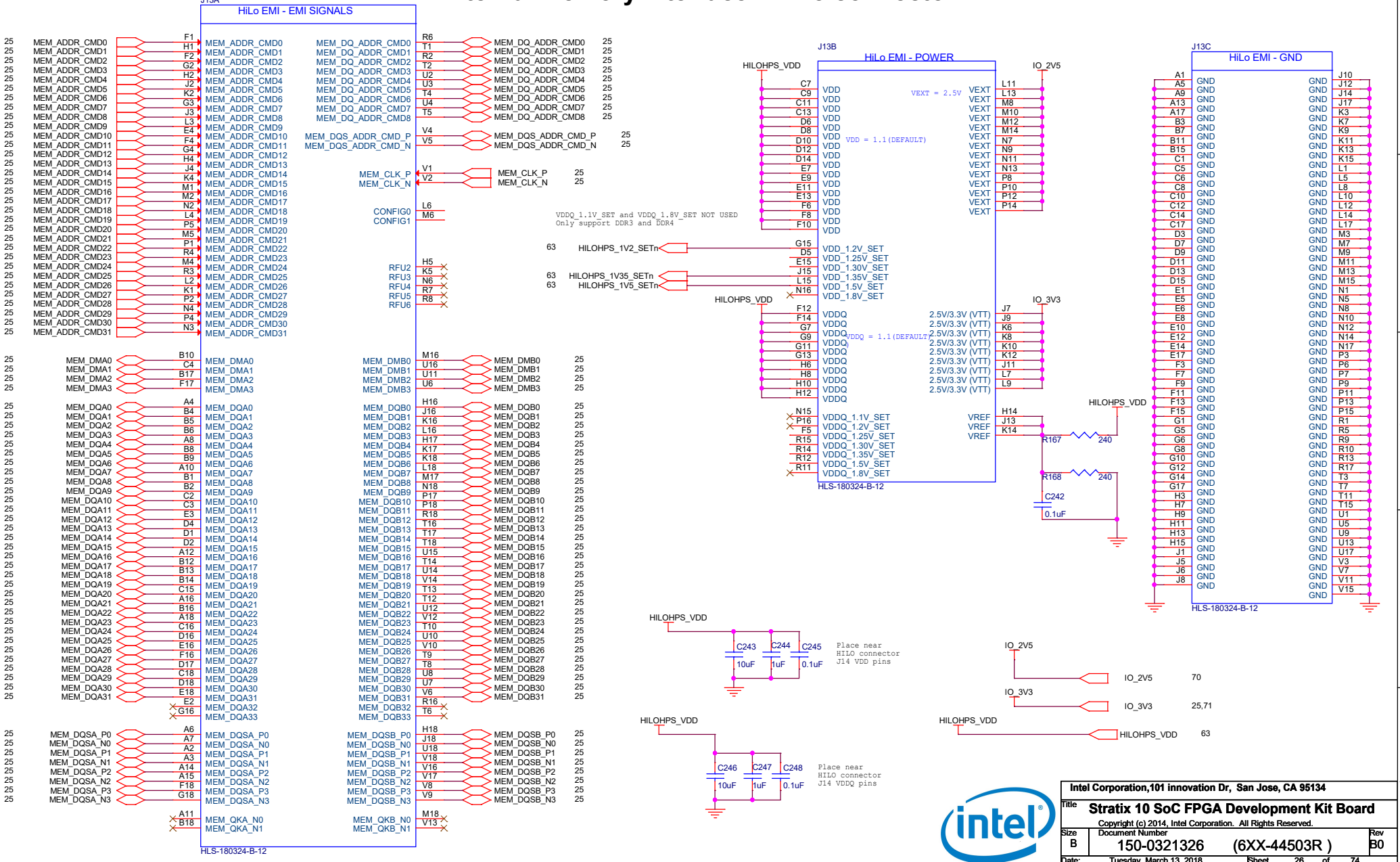
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# External Memory Interface - HiLo connector



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Size: B

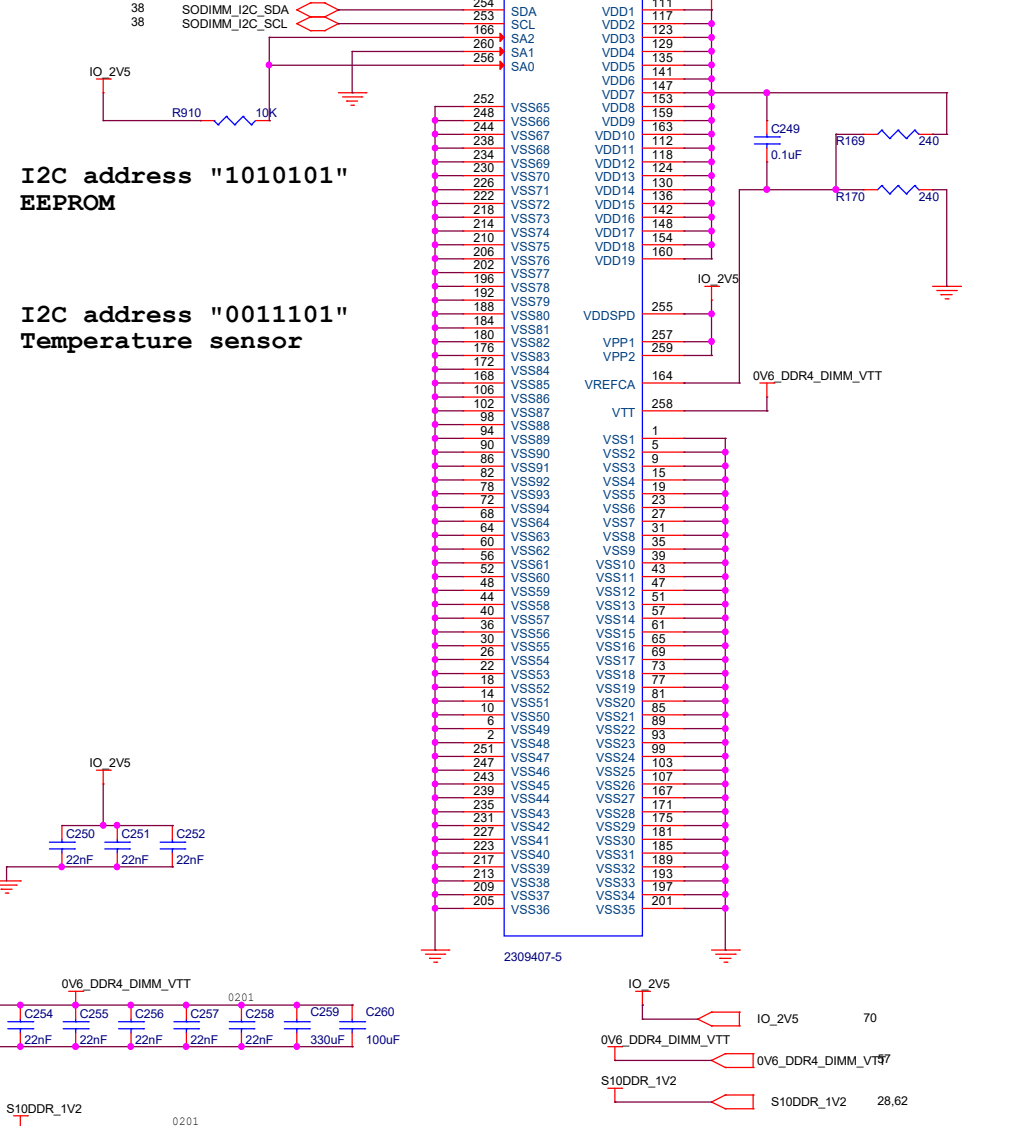
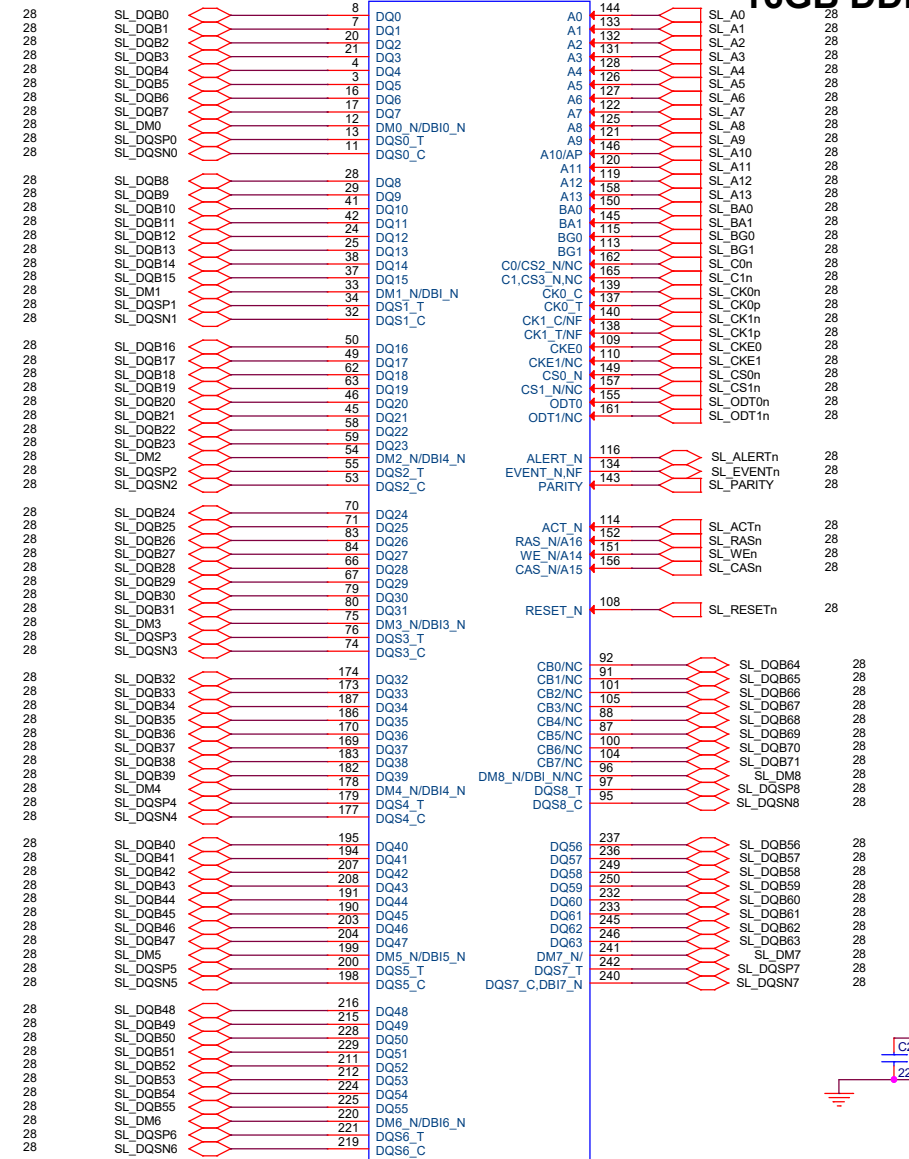
Document Number: **150-0321326**

Rev: **BO**

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# 16GB DDR4 SODIMM



I2C address "1010101"  
EEPROM

I2C address "0011101"  
Temperature sensor

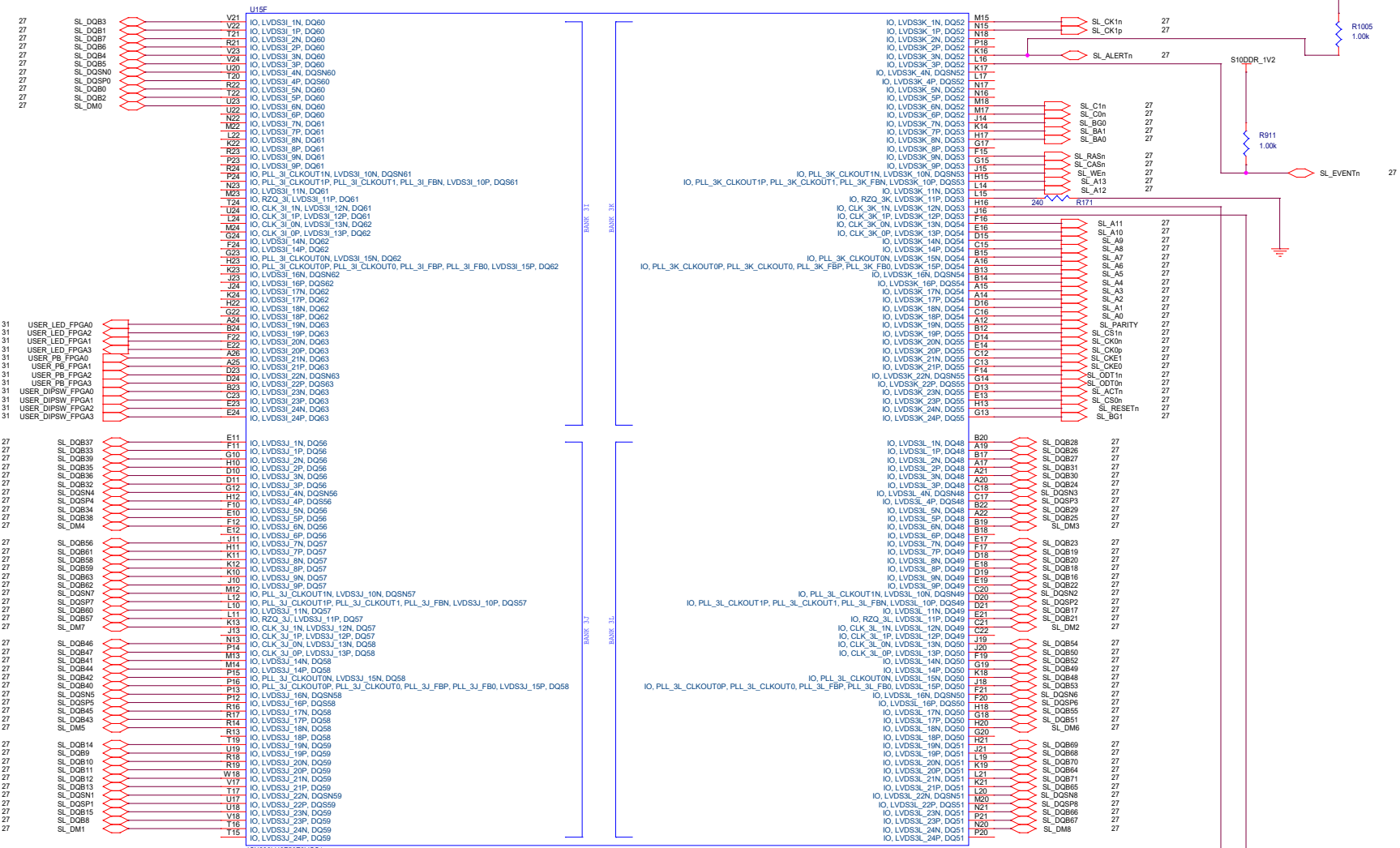


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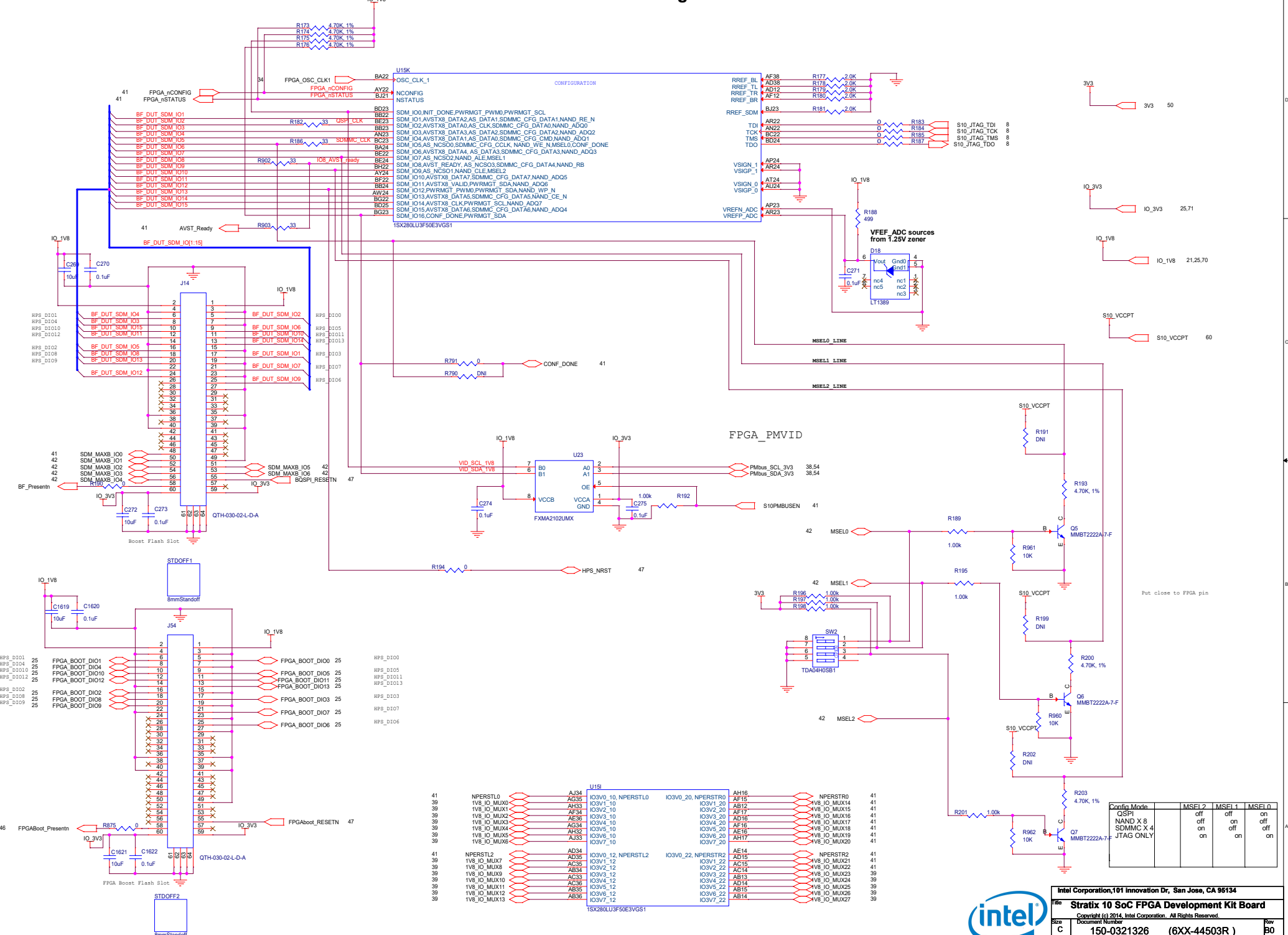
2309407-5

2309407-5

# Stratix 10 Banks - 3 I/J/L/K



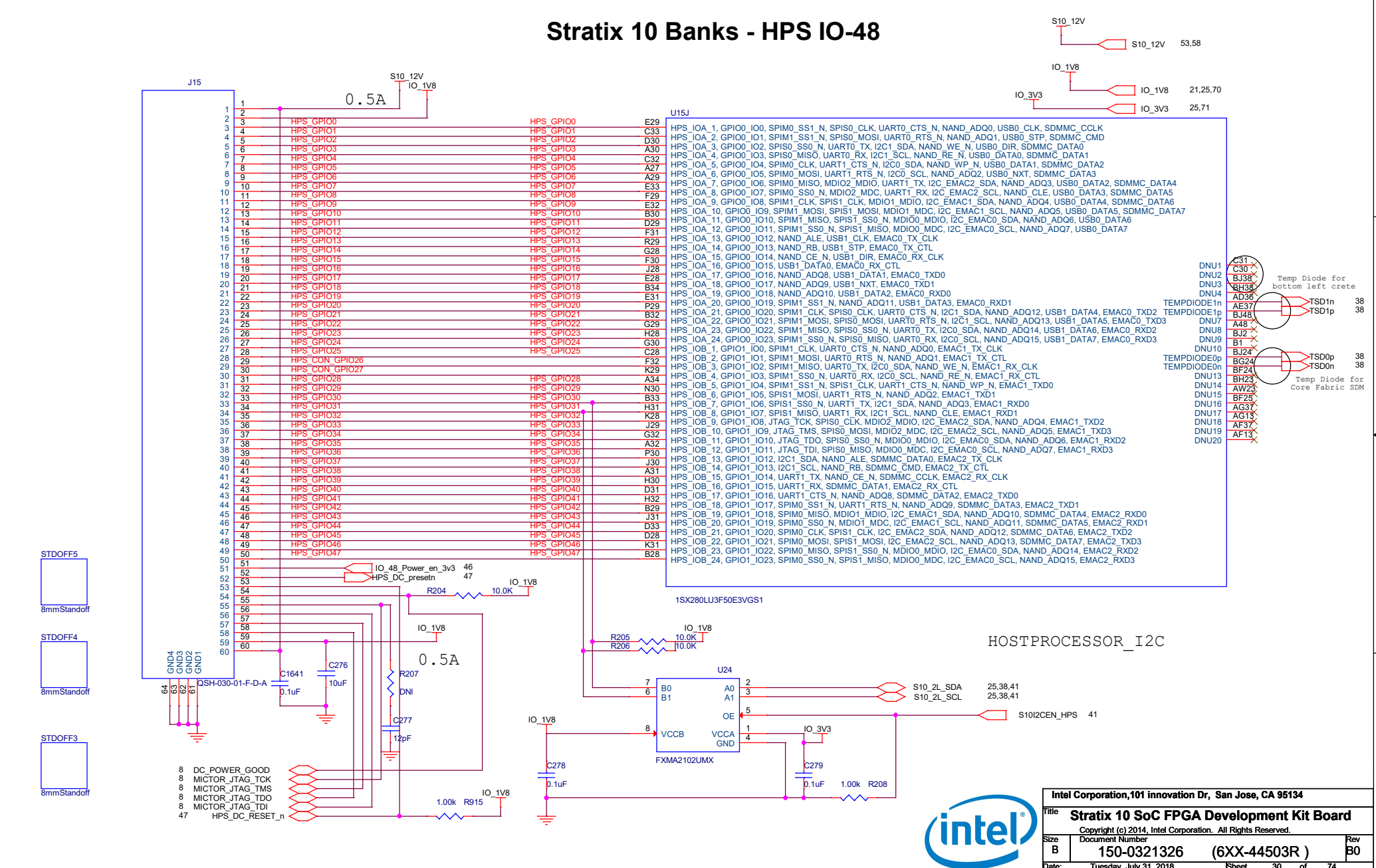
# Stratix 10 Banks - Configuration



Config Mode	MSEL2	MSEL1	MSEL0
QSPI	off	off	on
NAND X 8	off	on	off
SDMMC X 4	on	on	off
JTAG ONLY	on	off	on

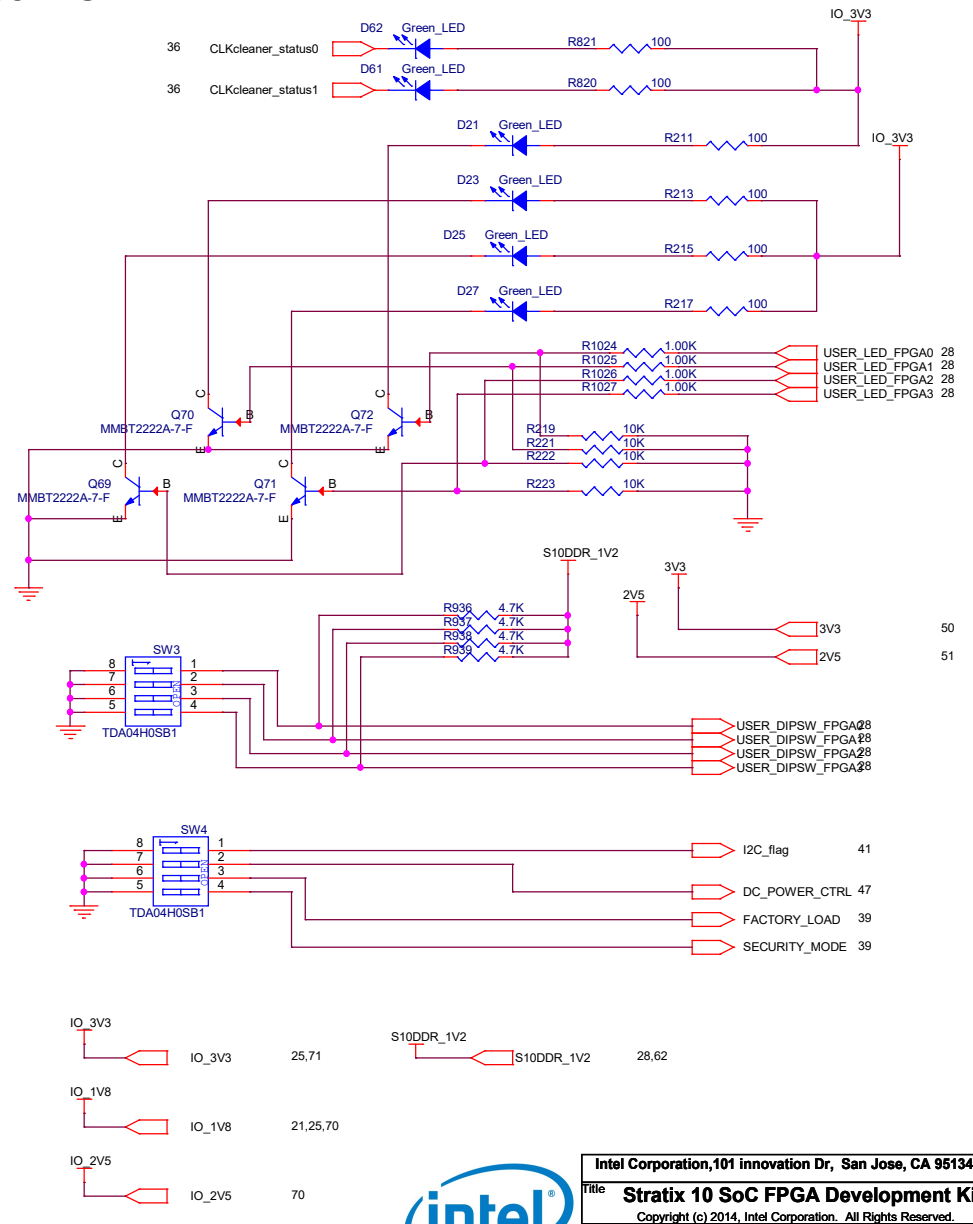
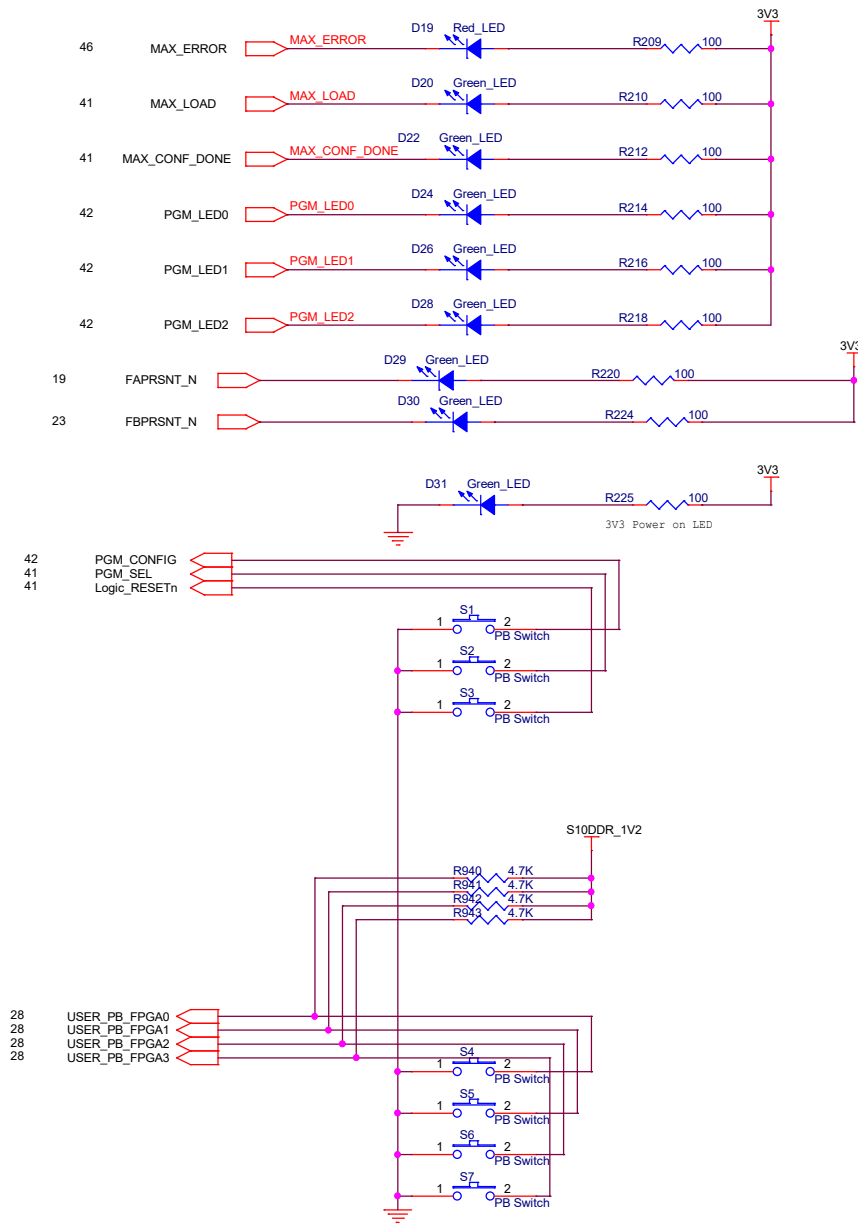


# Stratix 10 Banks - HPS IO-48



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# User I/O



- 28 USER\_PB\_FPGA0
- 28 USER\_PB\_FPGA1
- 28 USER\_PB\_FPGA2
- 28 USER\_PB\_FPGA3

- IO\_3V3
- IO\_3V3 25,71
- IO\_1V8
- IO\_1V8 21,25,70
- IO\_2V5
- IO\_2V5 70
- S10DDR\_1V2
- S10DDR\_1V2 28,62

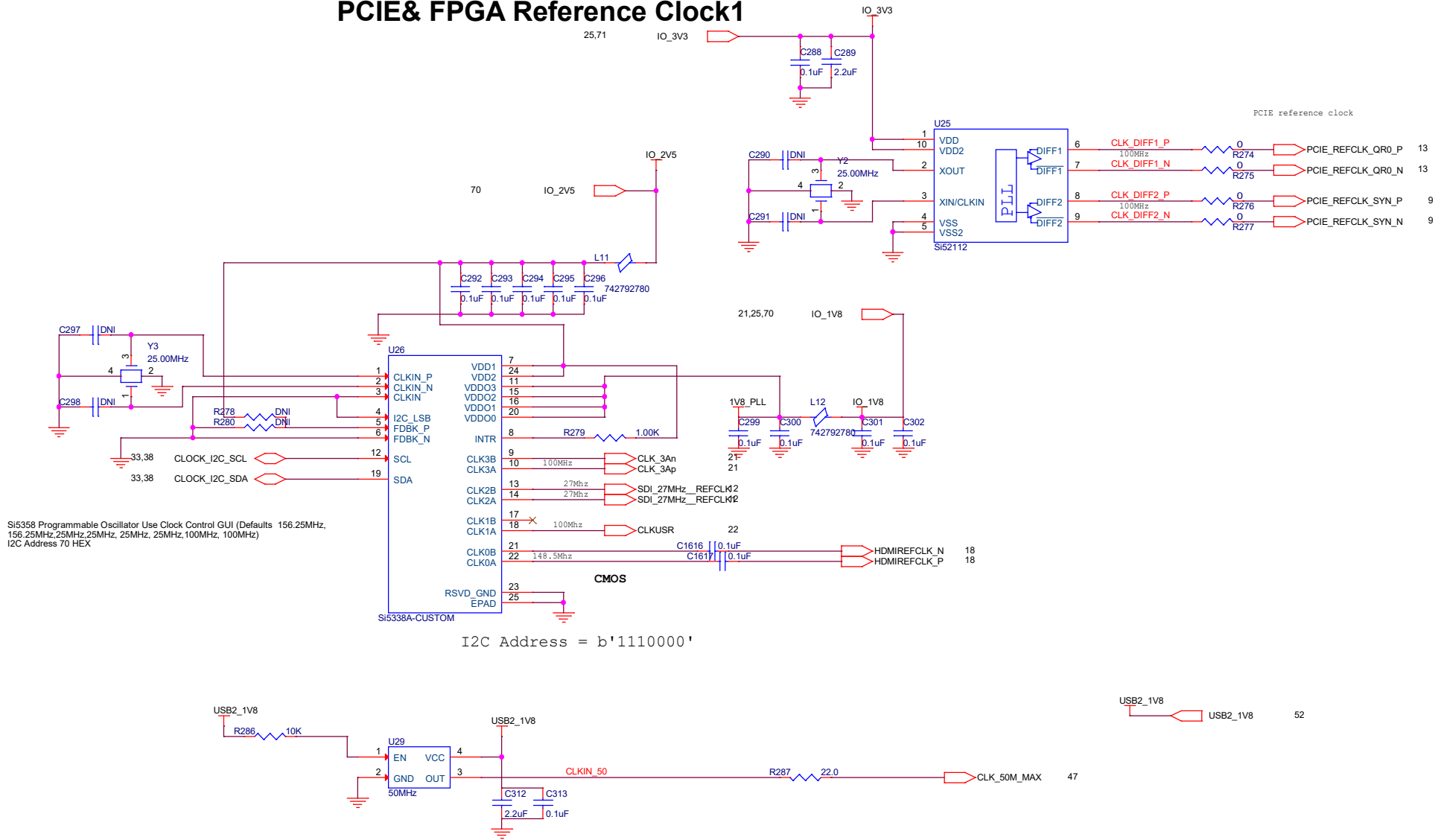


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# PCIe& FPGA Reference Clock1

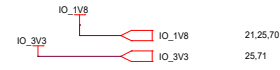
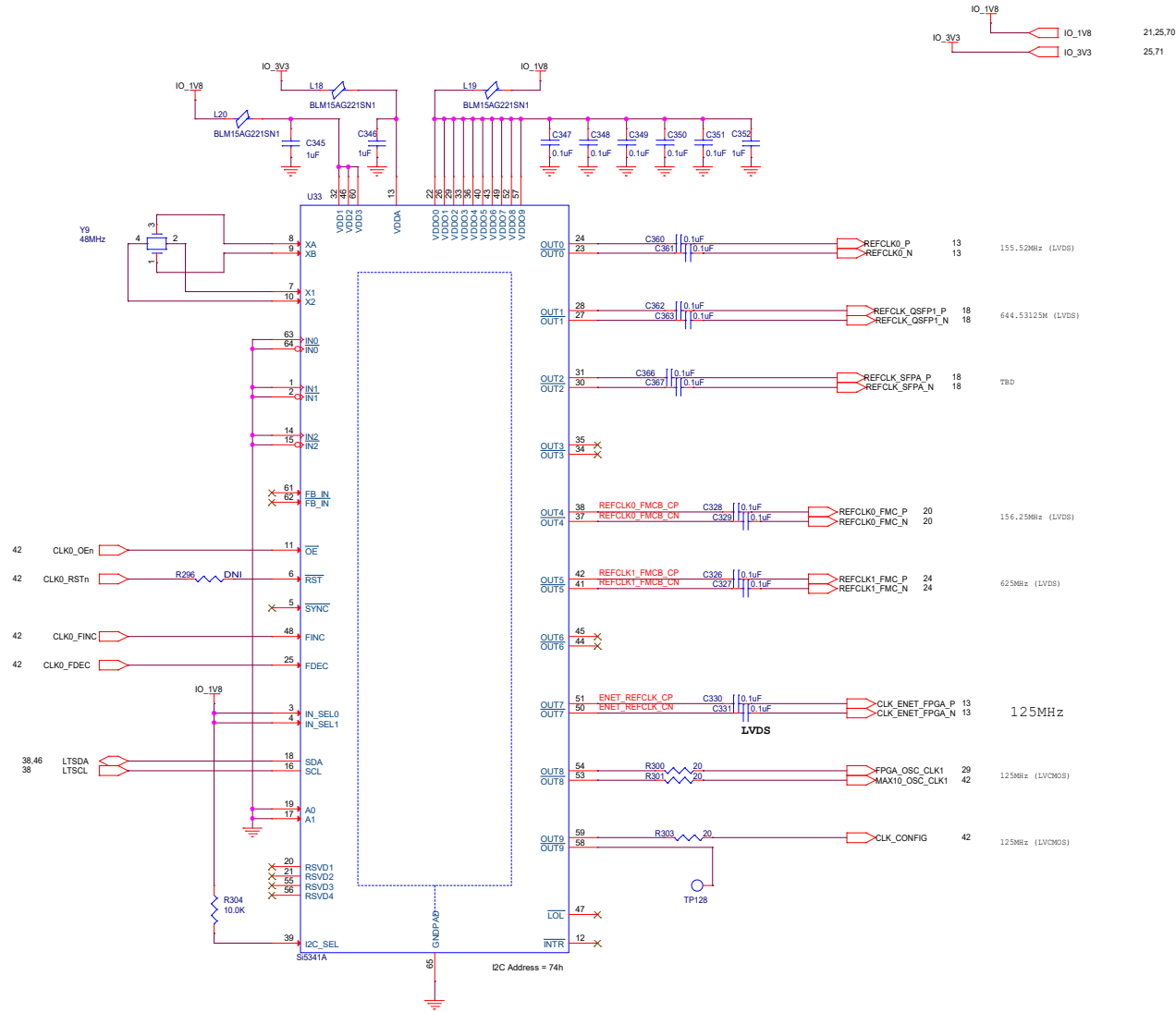


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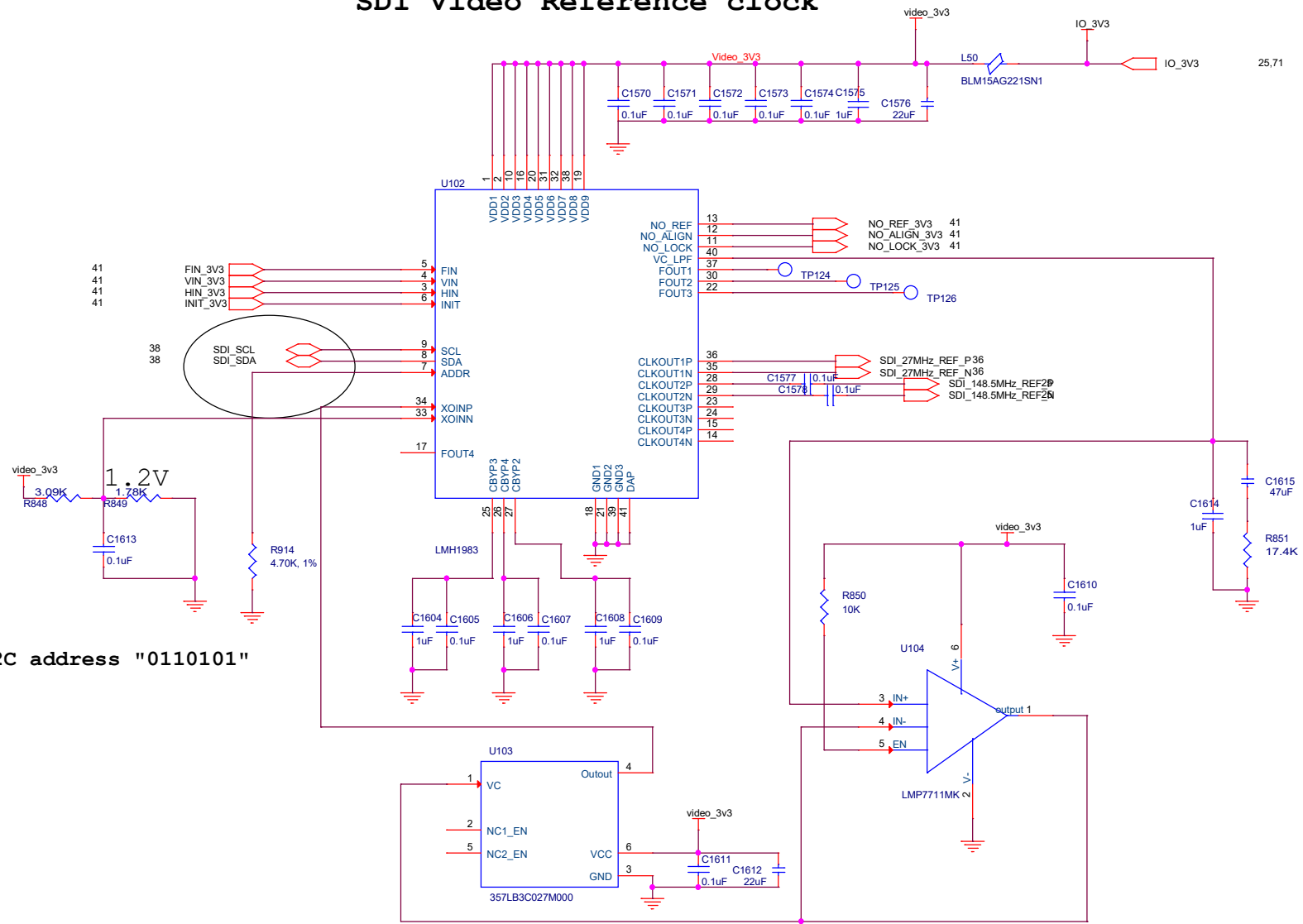


# FPGA Transceiver reference Clocks



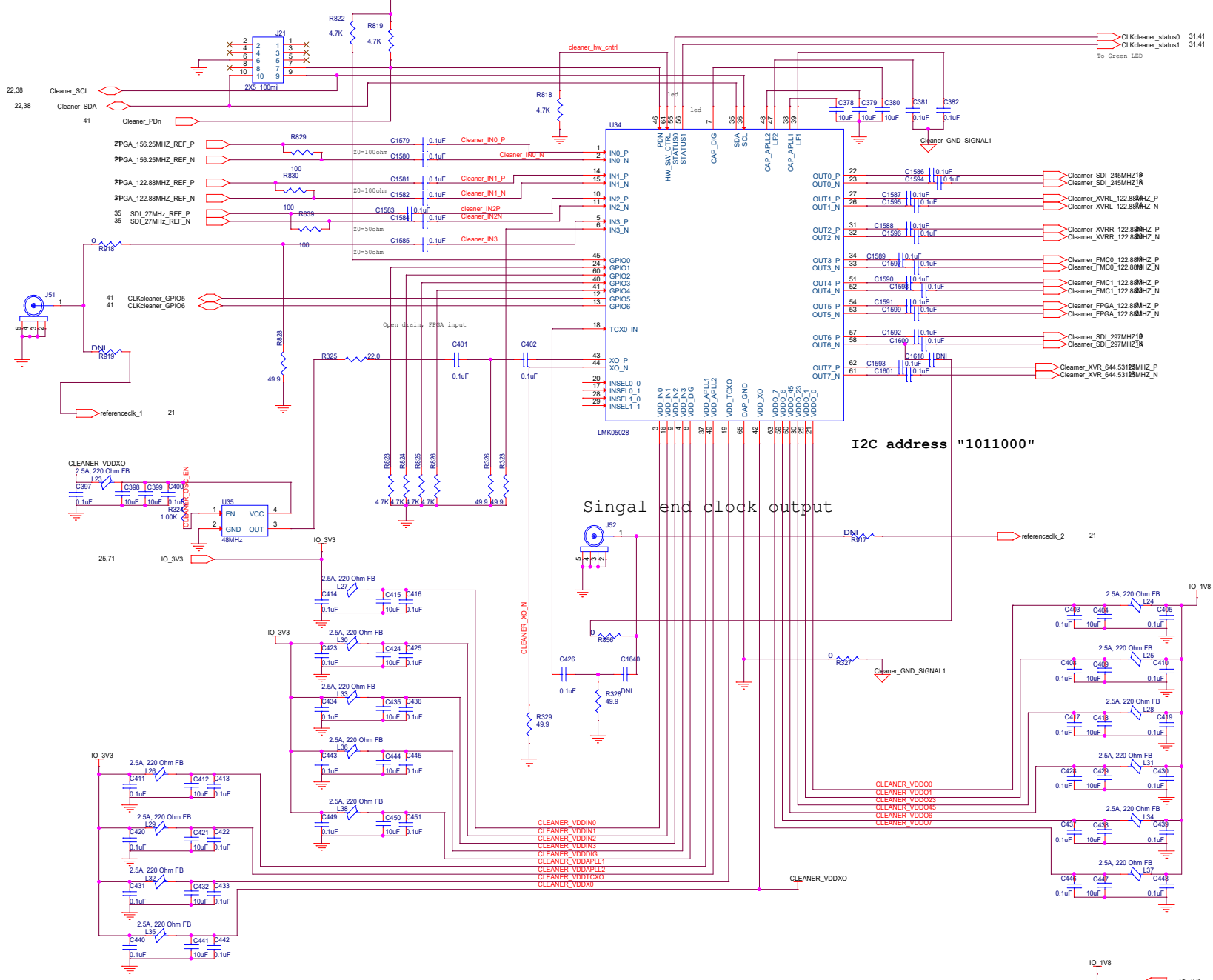
# SDI Video Reference clock

I2C address "0110101"

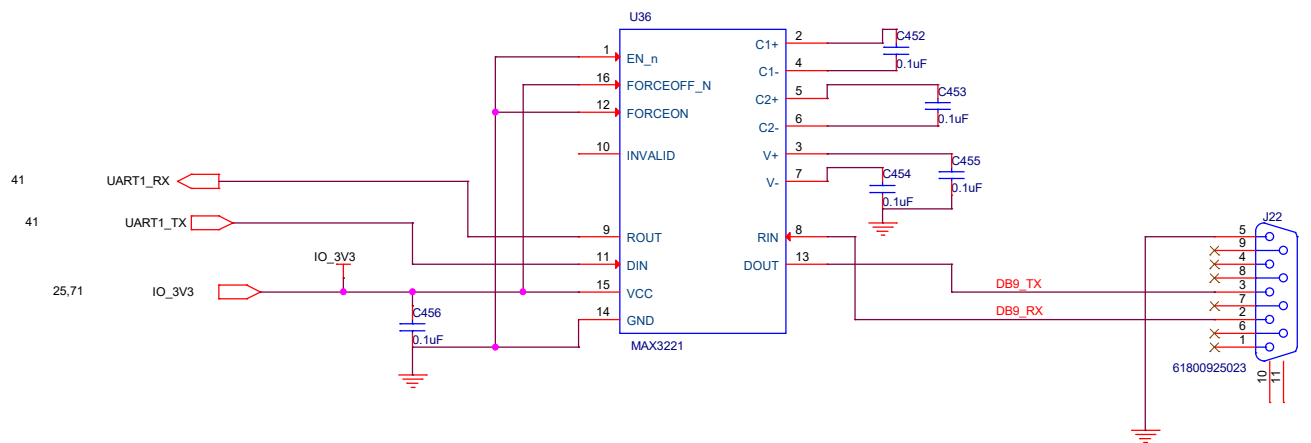


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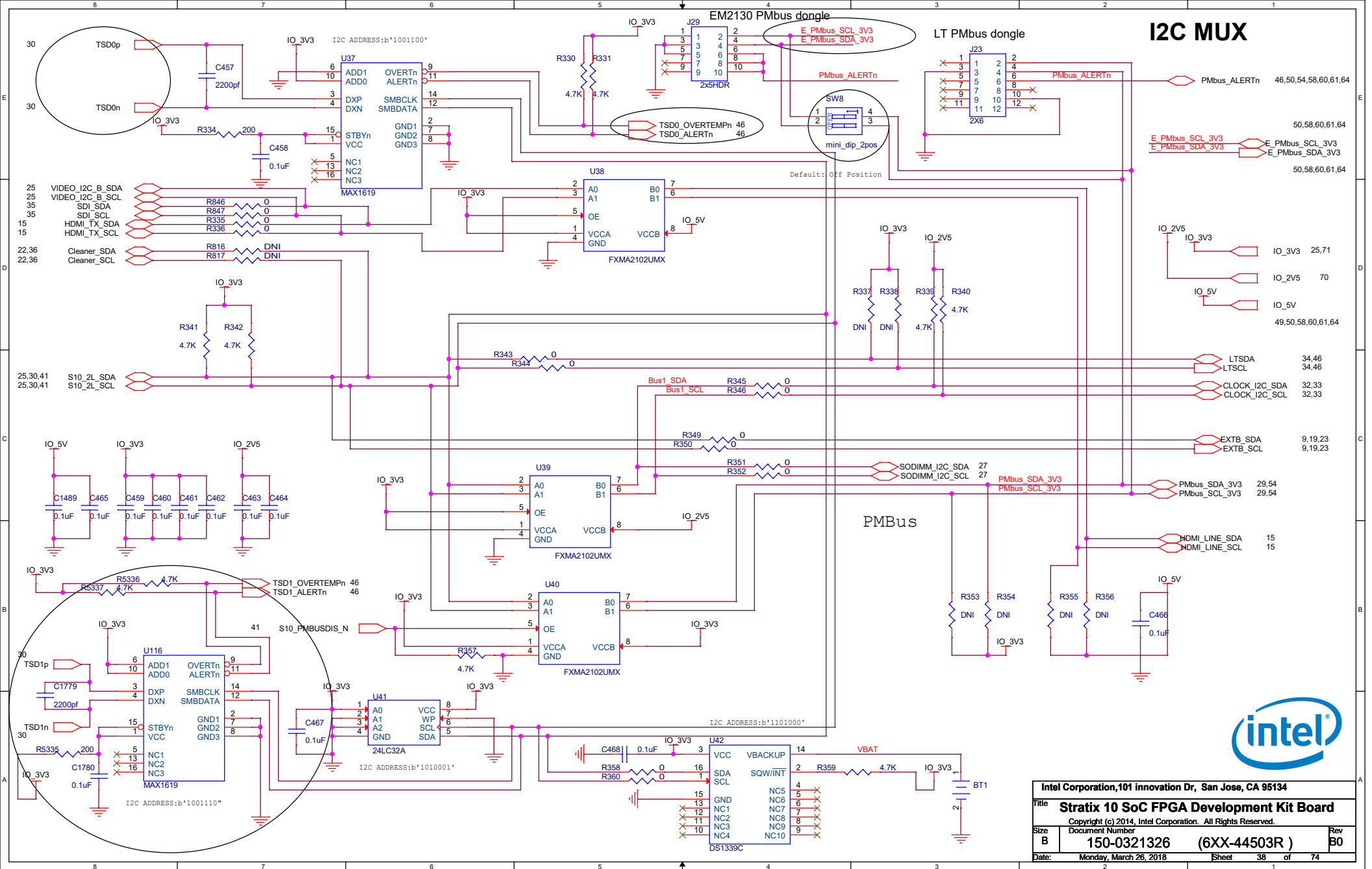
# lmk05028 CLOCK CLEANER



# UART Port B

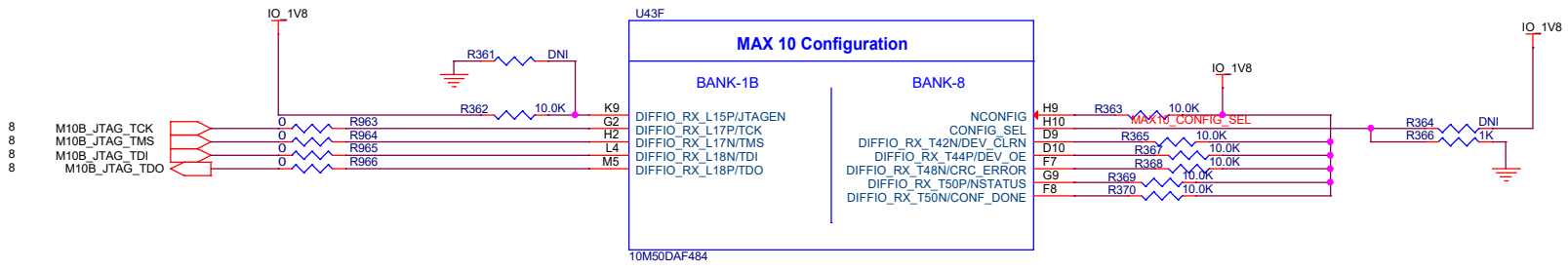
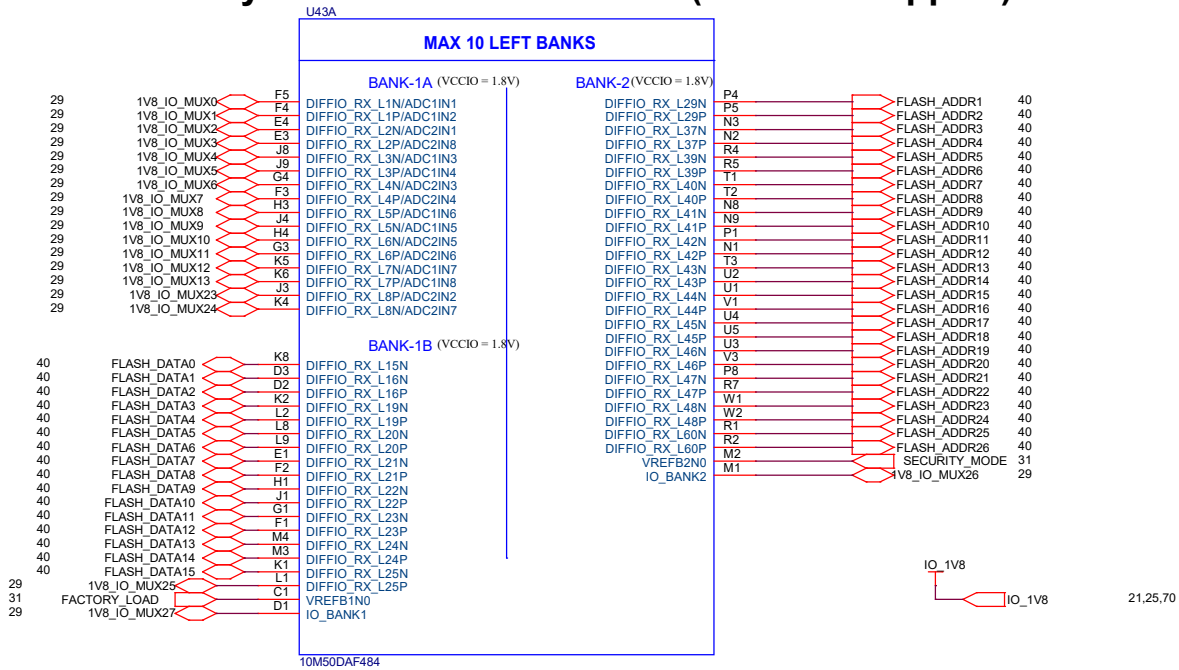


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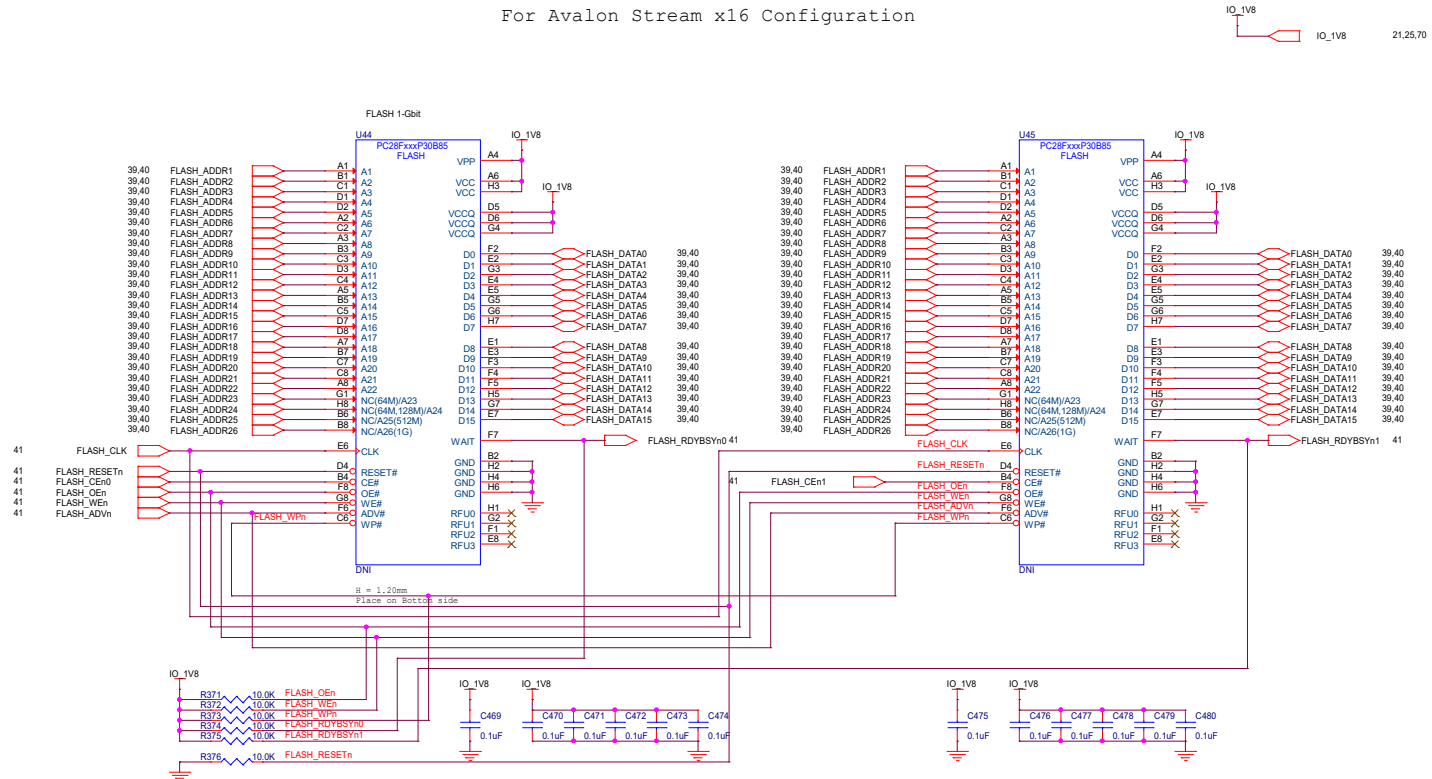
# System MAX10 Controller (NO ADC Support)



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# Flash Memory

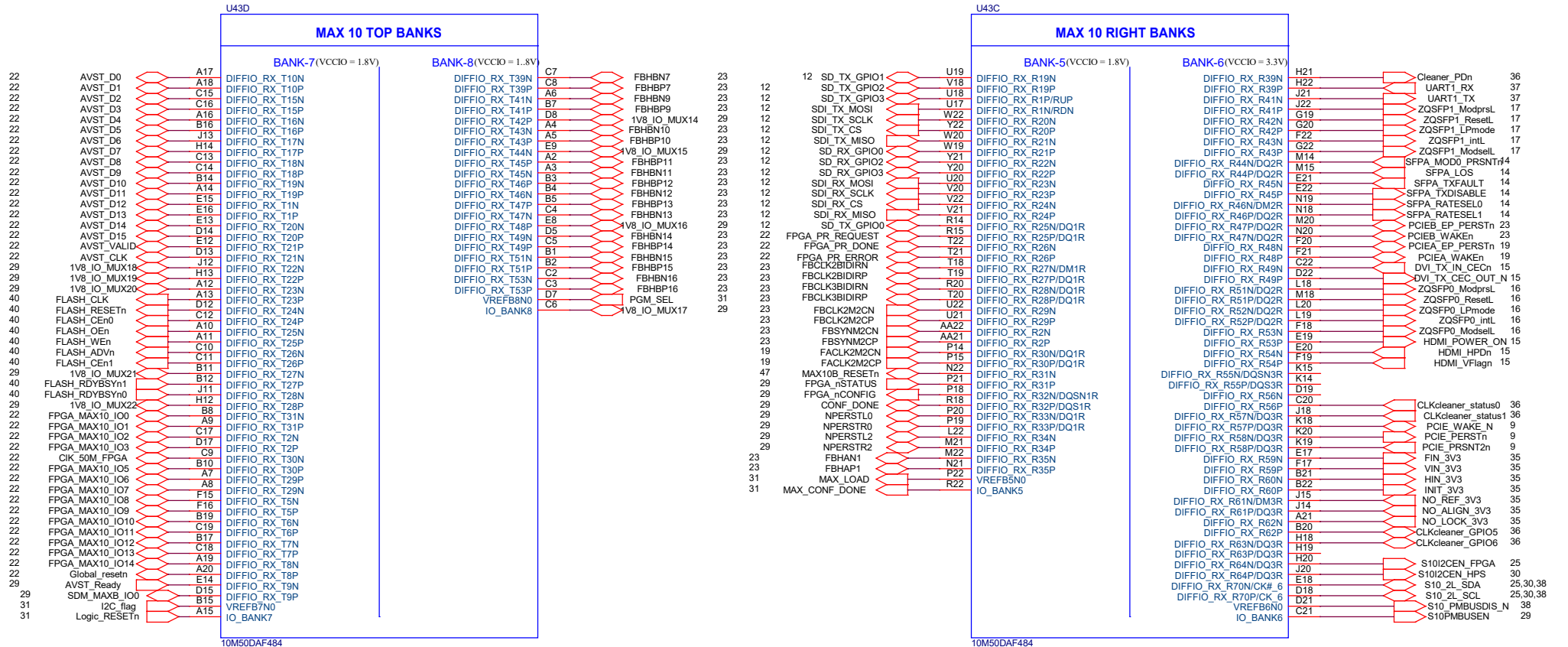
For Avalon Stream x16 Configuration



- When using a single x16 flash device a word consists of 16 data bits so addressing starts with FM\_A1 mapped to address bit 1 in software.

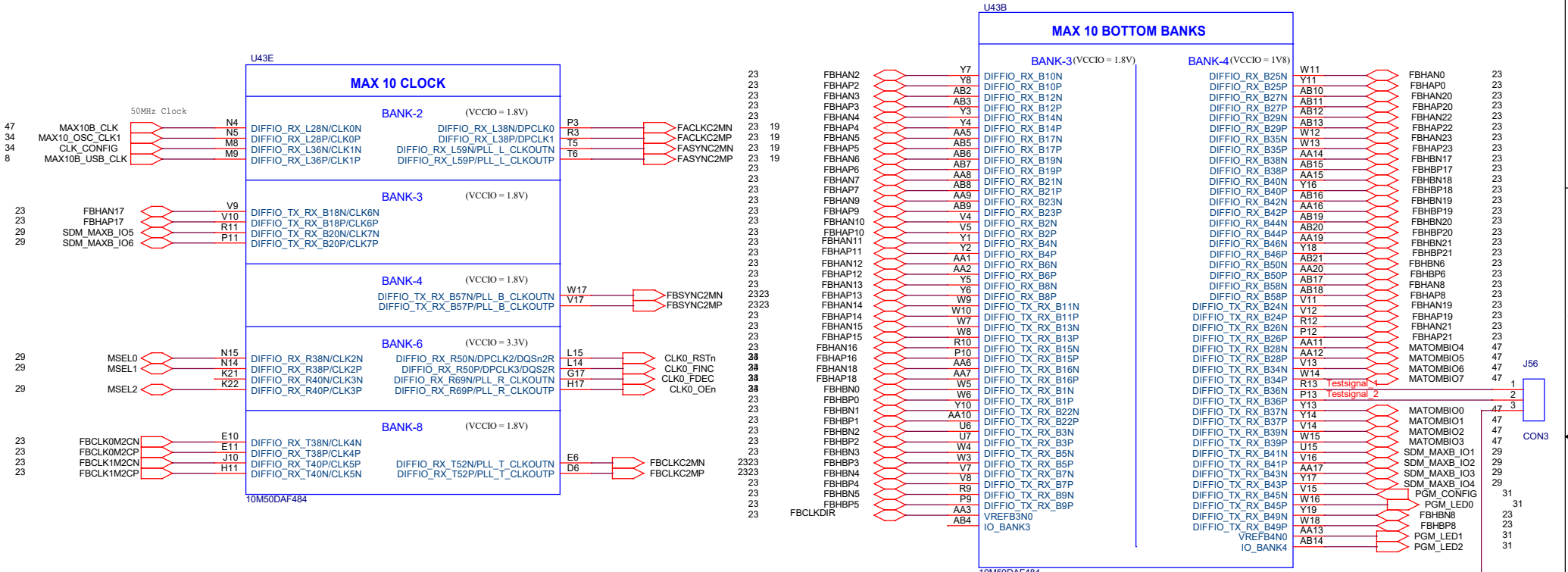


# System MAX10 Controller 2

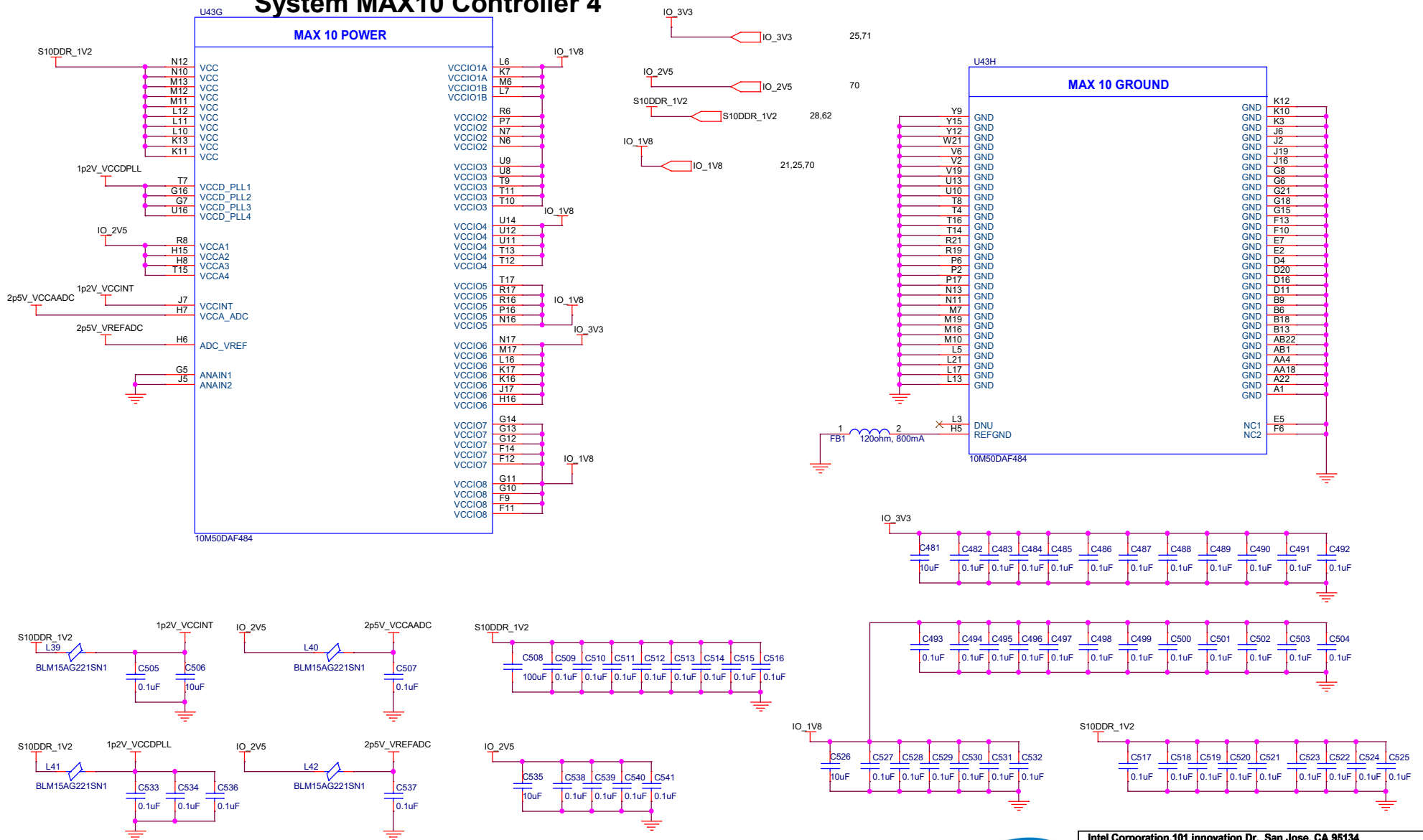


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# System MAX10 Controller 3

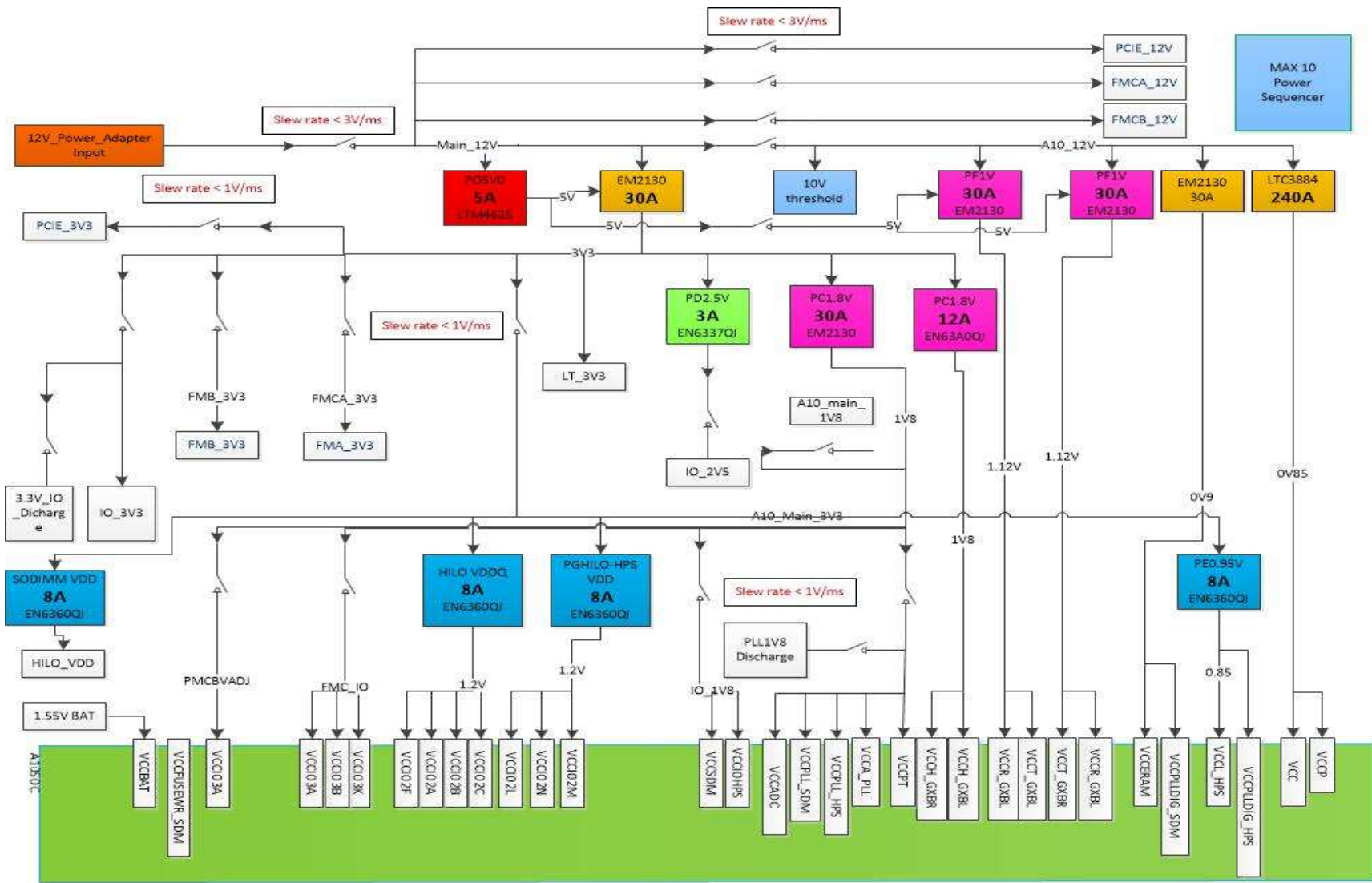


# System MAX10 Controller 4



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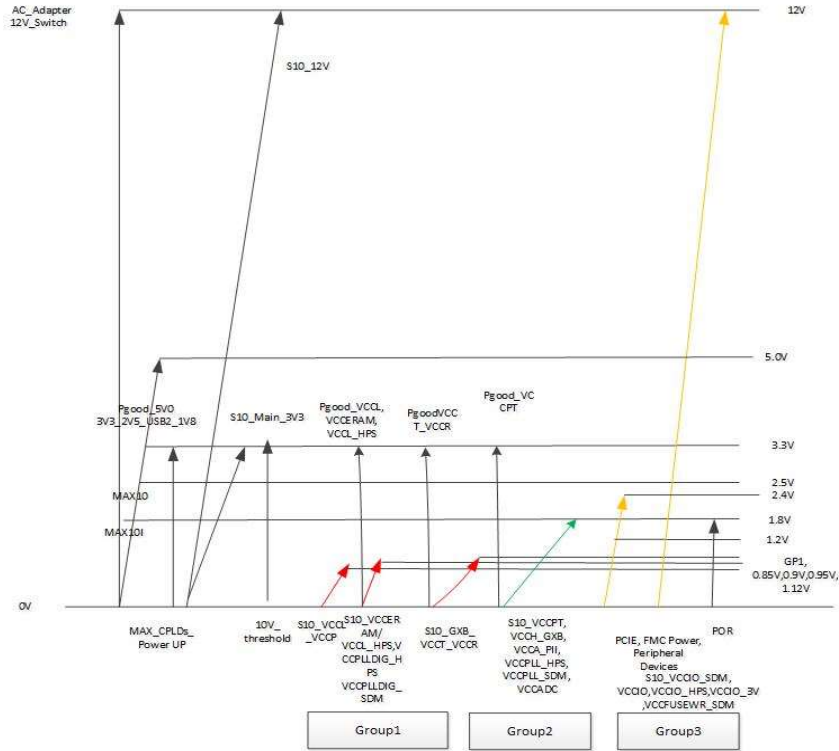
# Stratix 10 SOC DEV KIT PDN Diagram



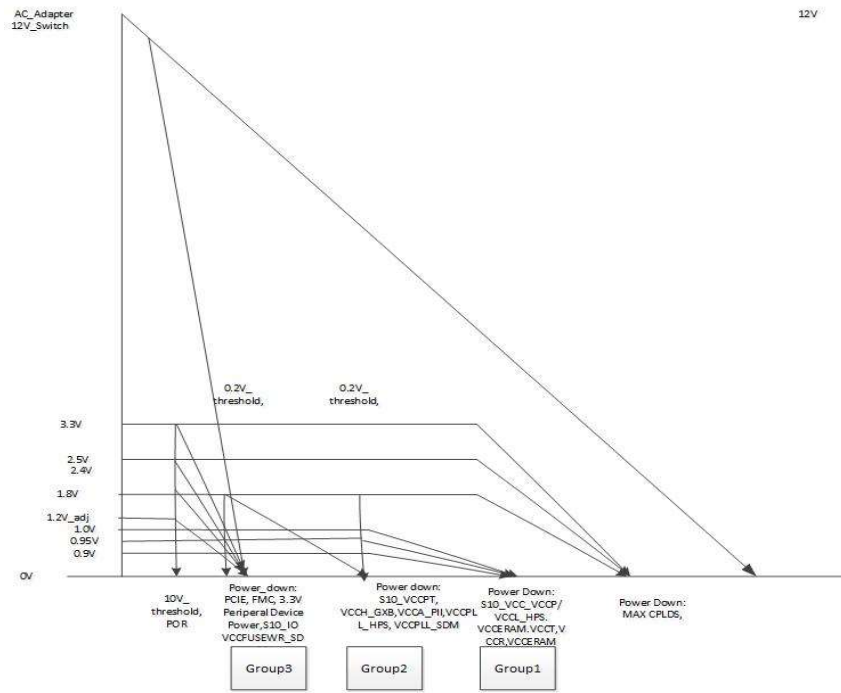
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# Stratix 10 SOC Power Sequence

## S10 Dev KIT Power UP sequence

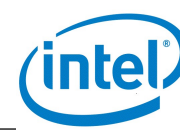
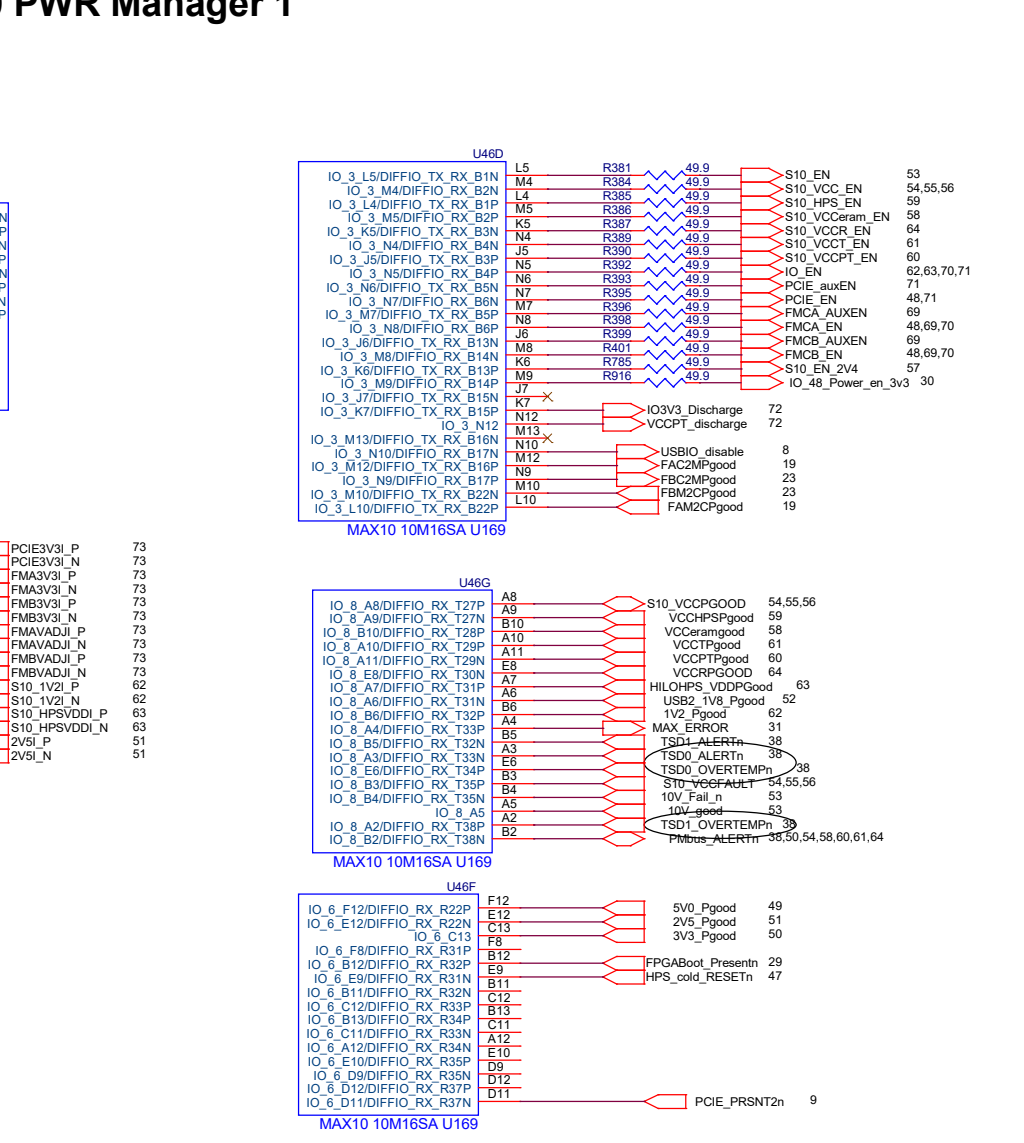
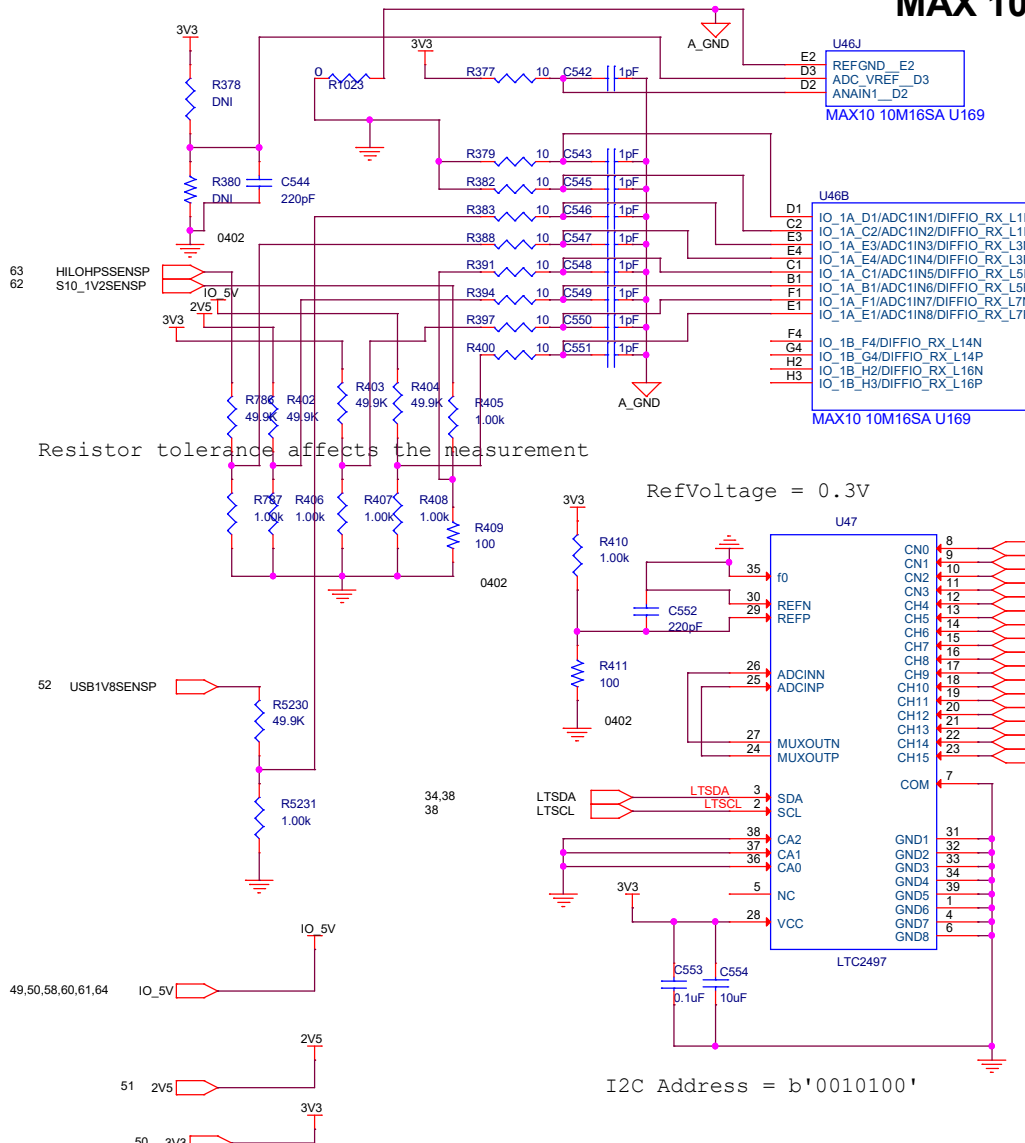


## S10 Dev KIT Power Down sequence



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# MAX 10 PWR Manager 1



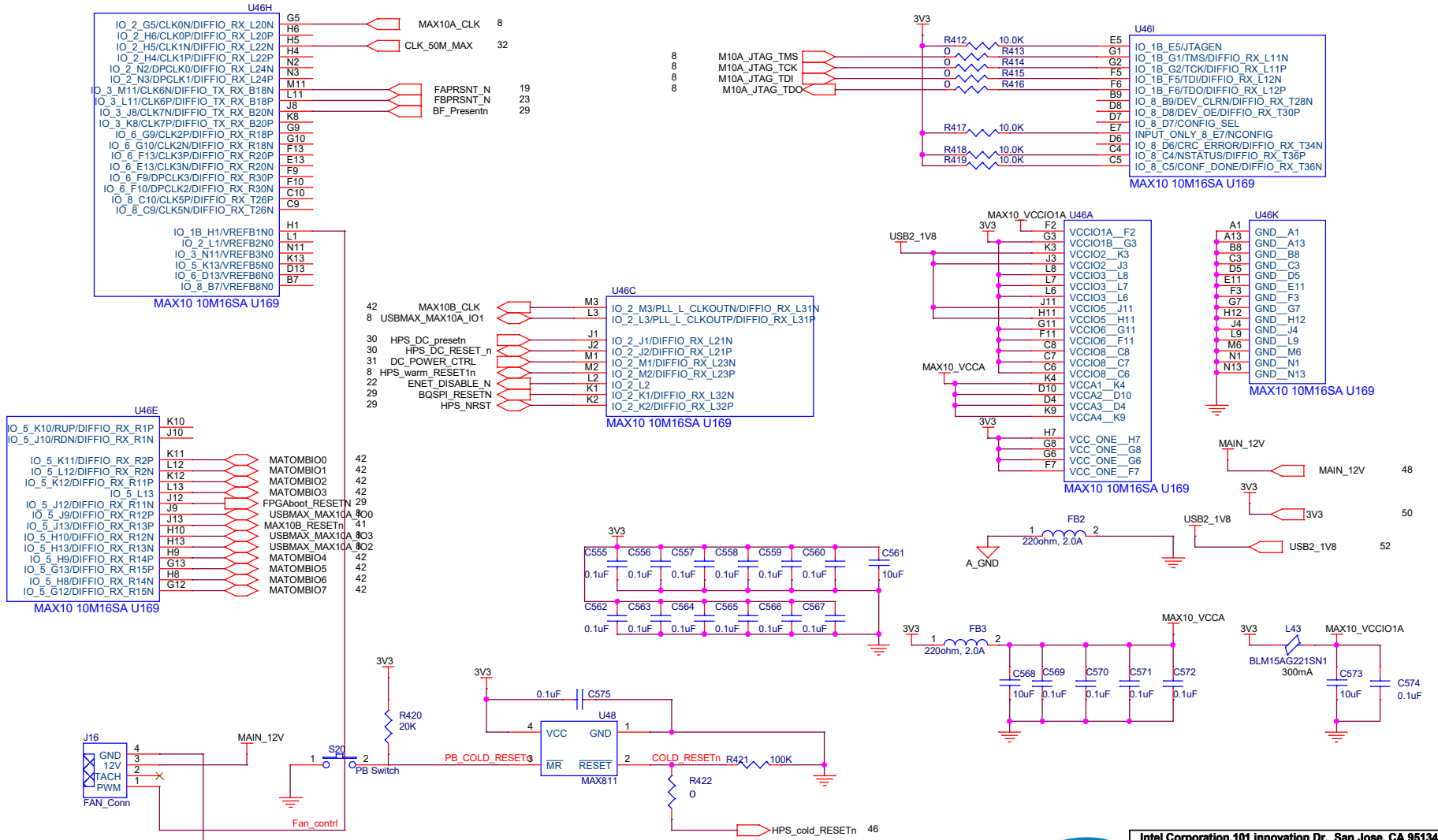
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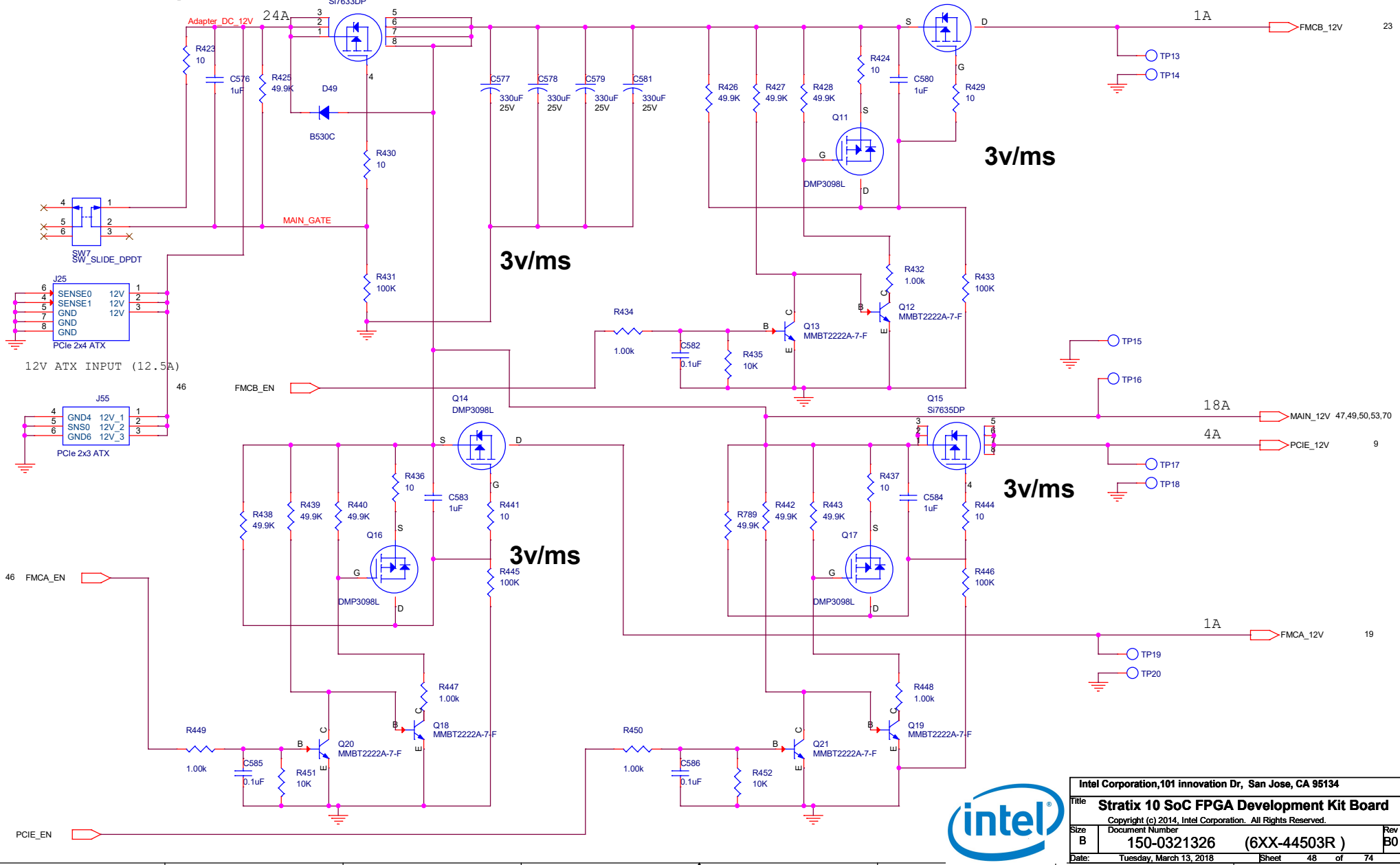


# MAX10 PWR Manager 2



Input connector for  
280 Watt AC/DC Adapter

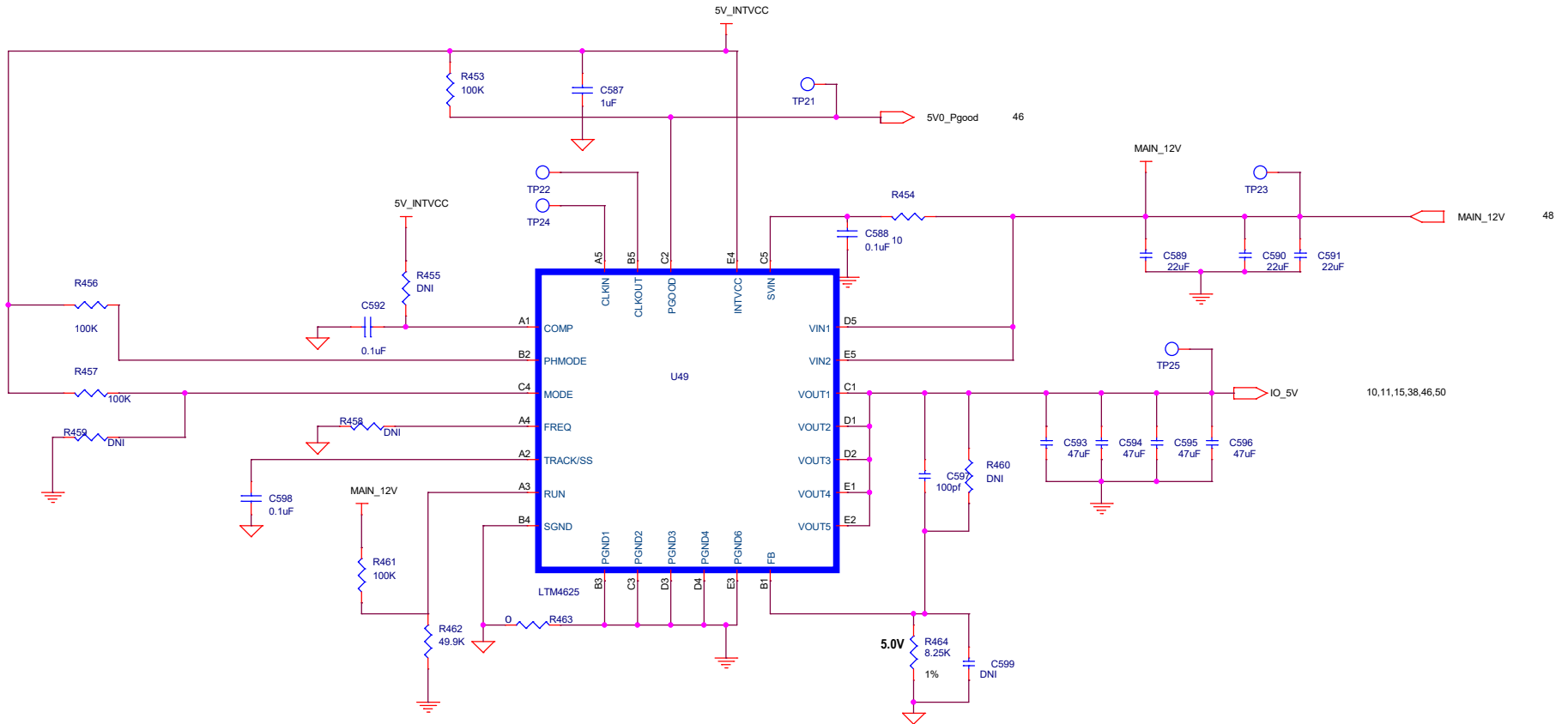
# 12V Power PMOS Switches



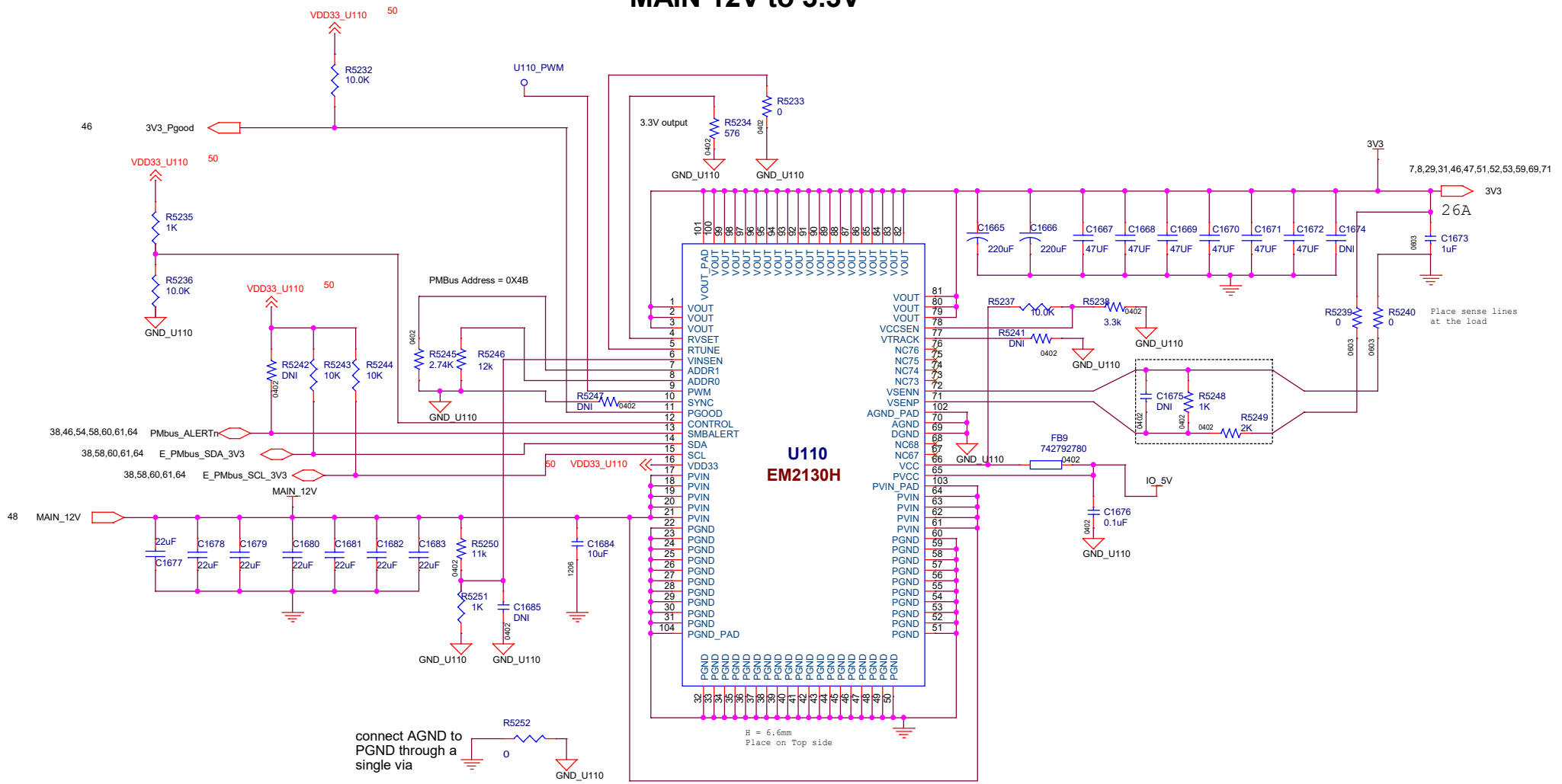
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# 12V to 5V Power Supply

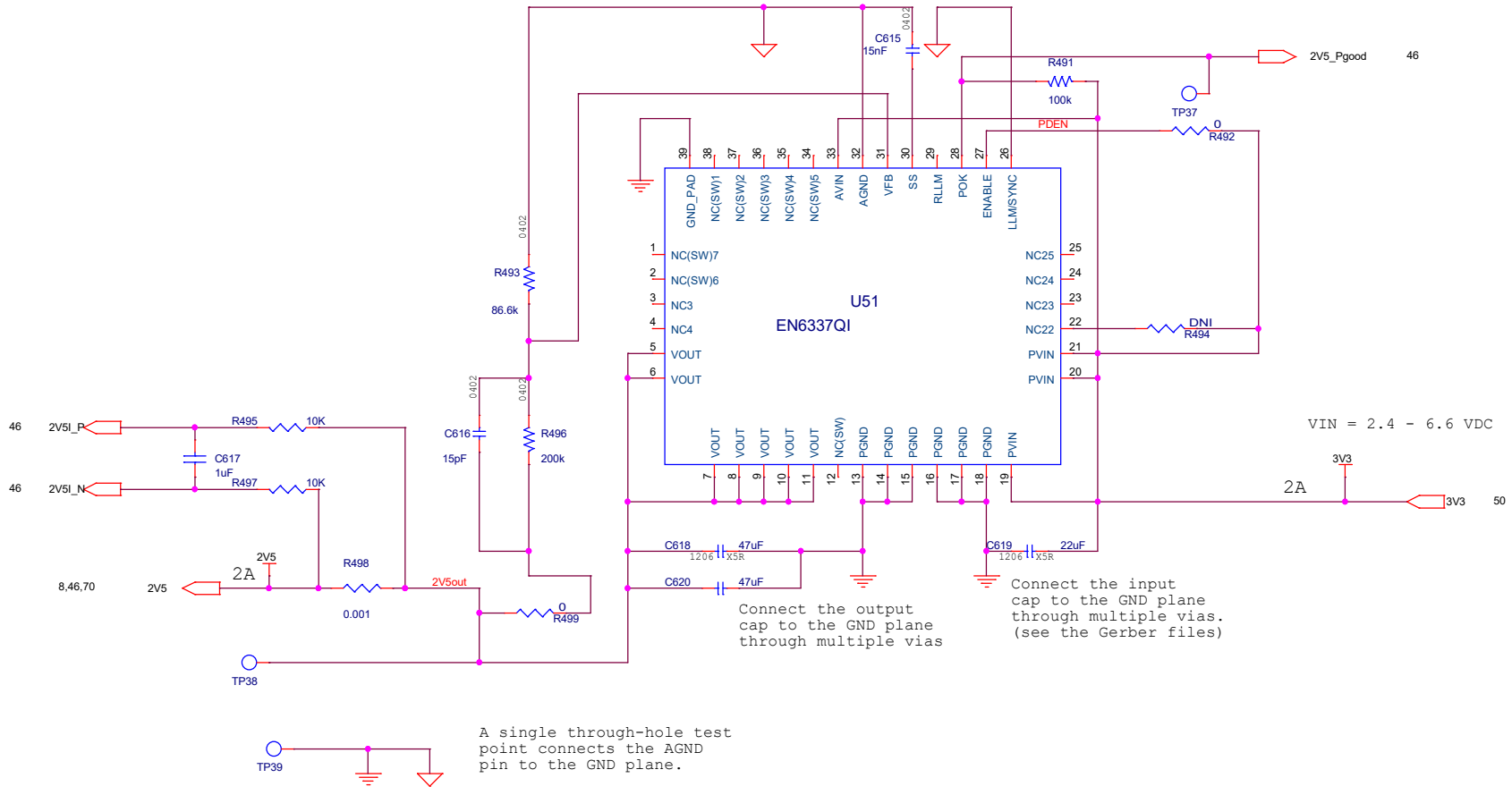


# MAIN 12V to 3.3V



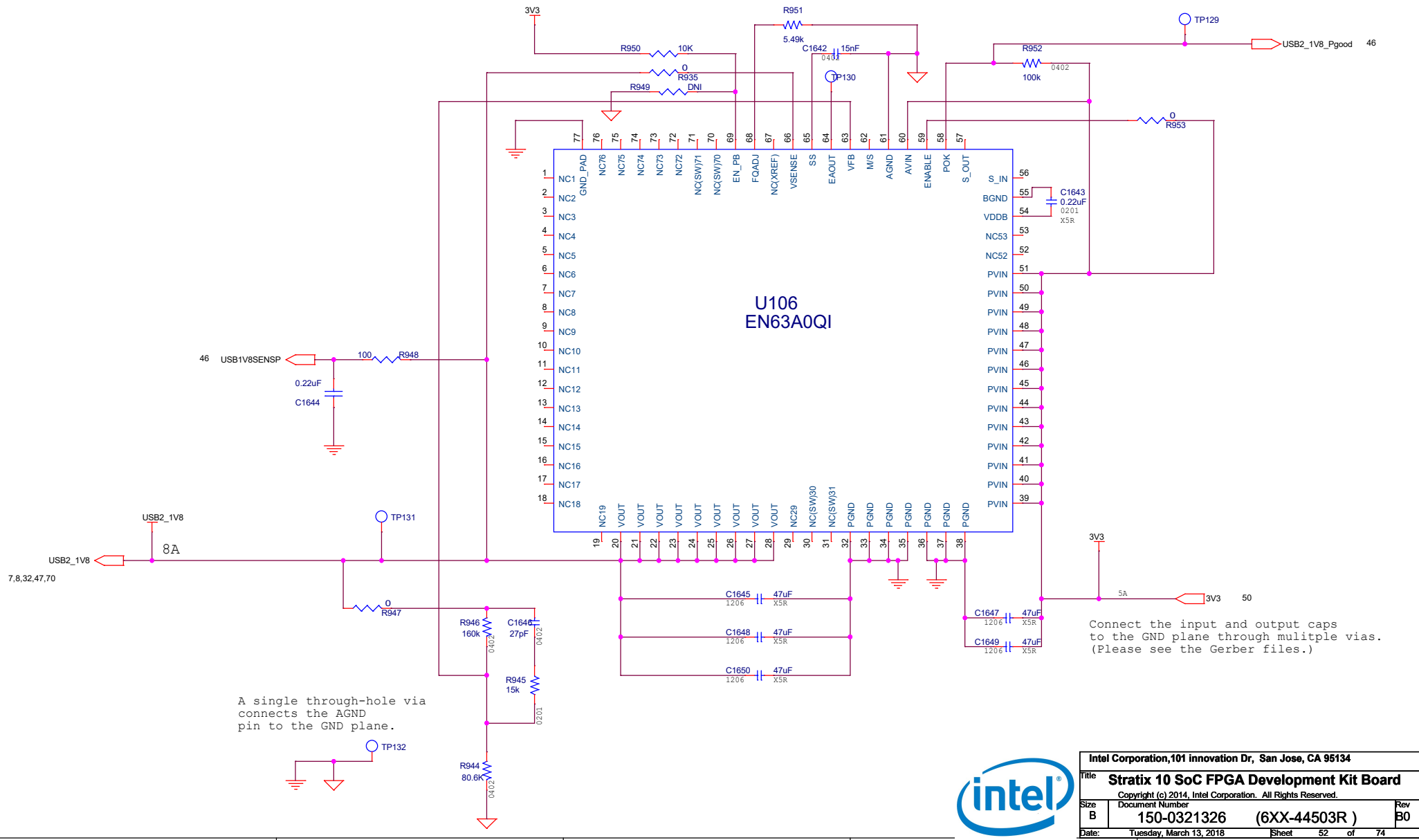
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# 3V3 to 2V5 Converter



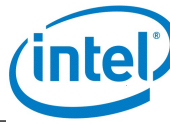
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# 3.3V to 1.8V Converter



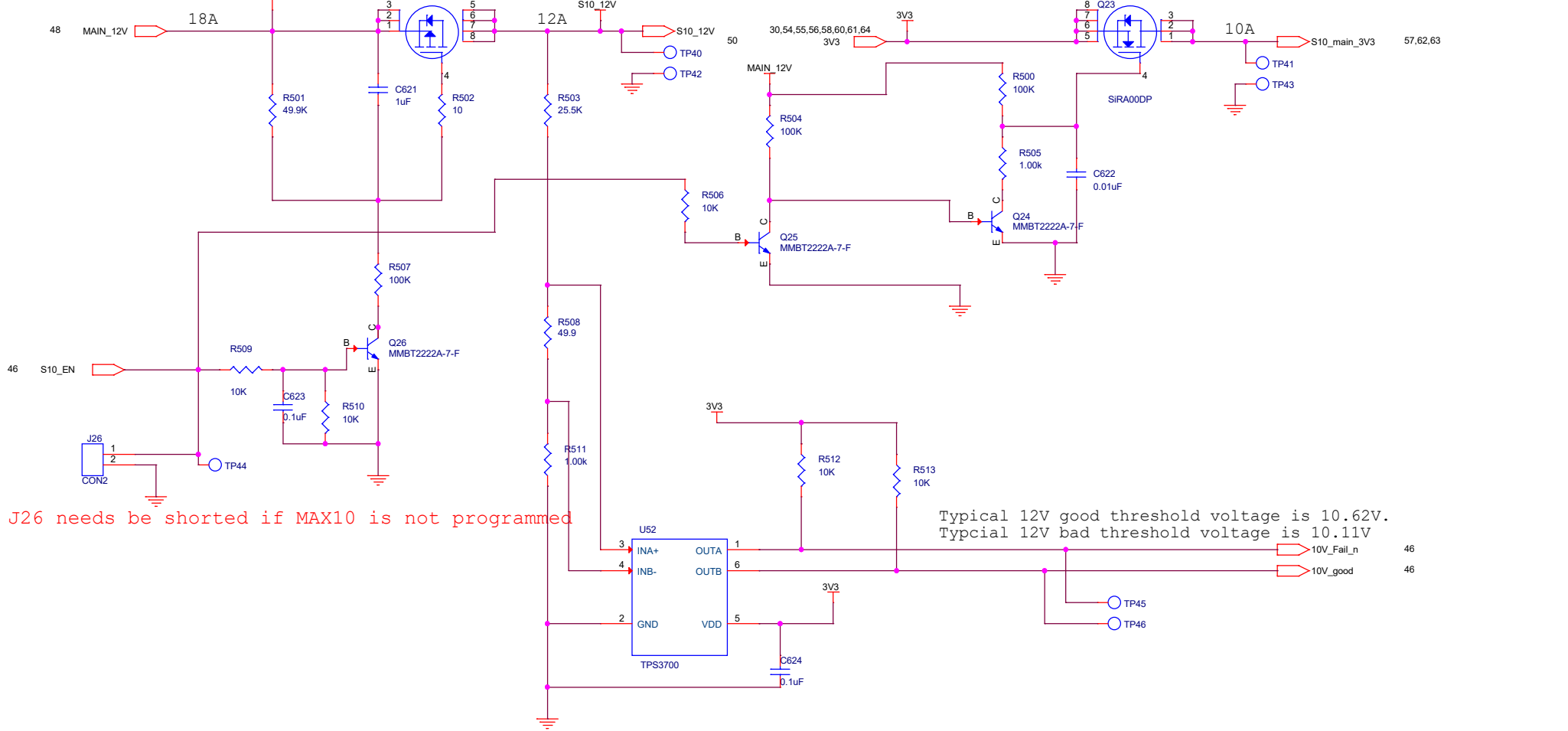
A single through-hole via connects the AGND pin to the GND plane.

Connect the input and output caps to the GND plane through multiple vias. (Please see the Gerber files.)



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# S10 12V,3V3 and 1V8 PMOS Switches



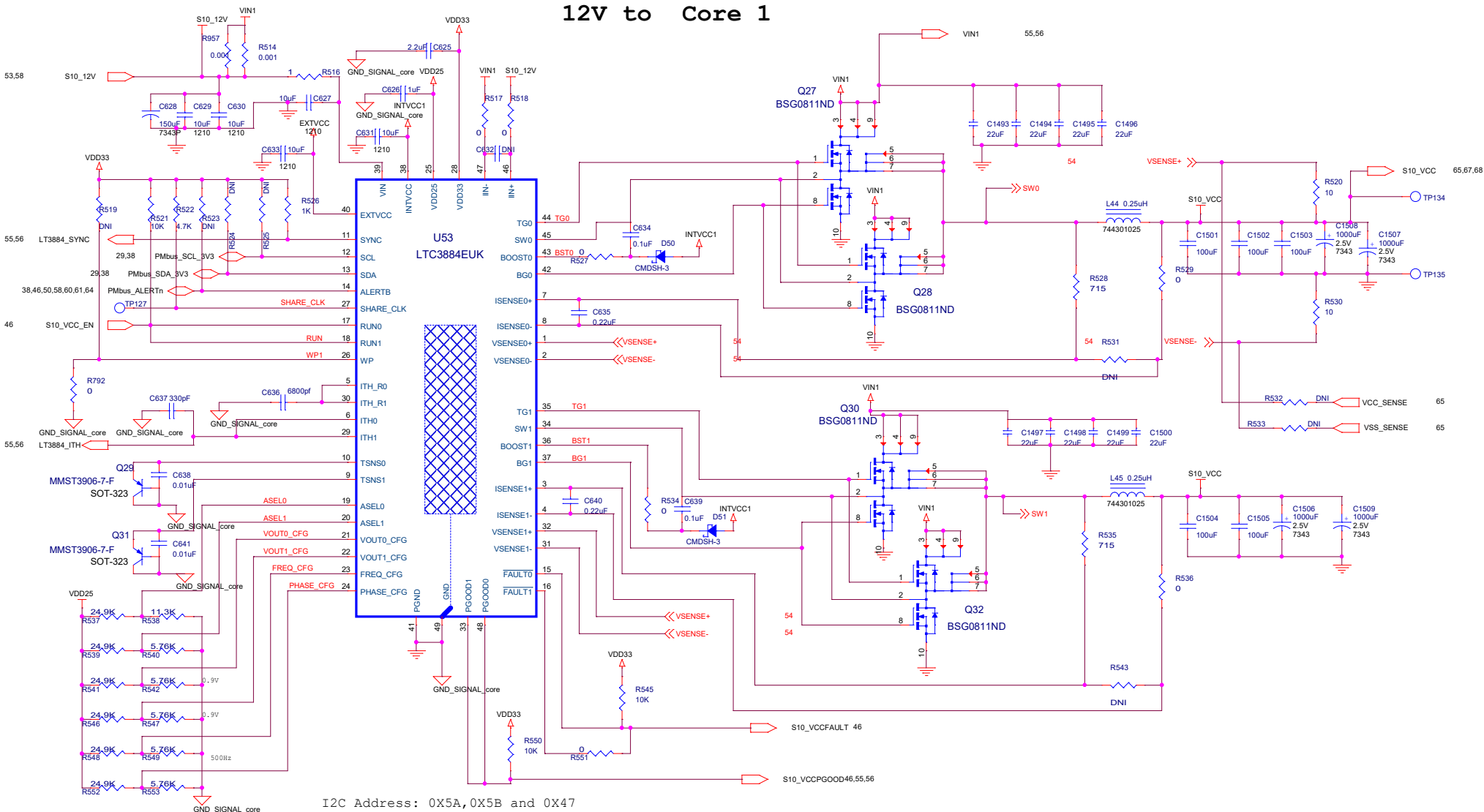
J26 needs be shorted if MAX10 is not programmed

Typical 12V good threshold voltage is 10.62V.  
 Typical 12V bad threshold voltage is 10.11V



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# 12V to Core 1



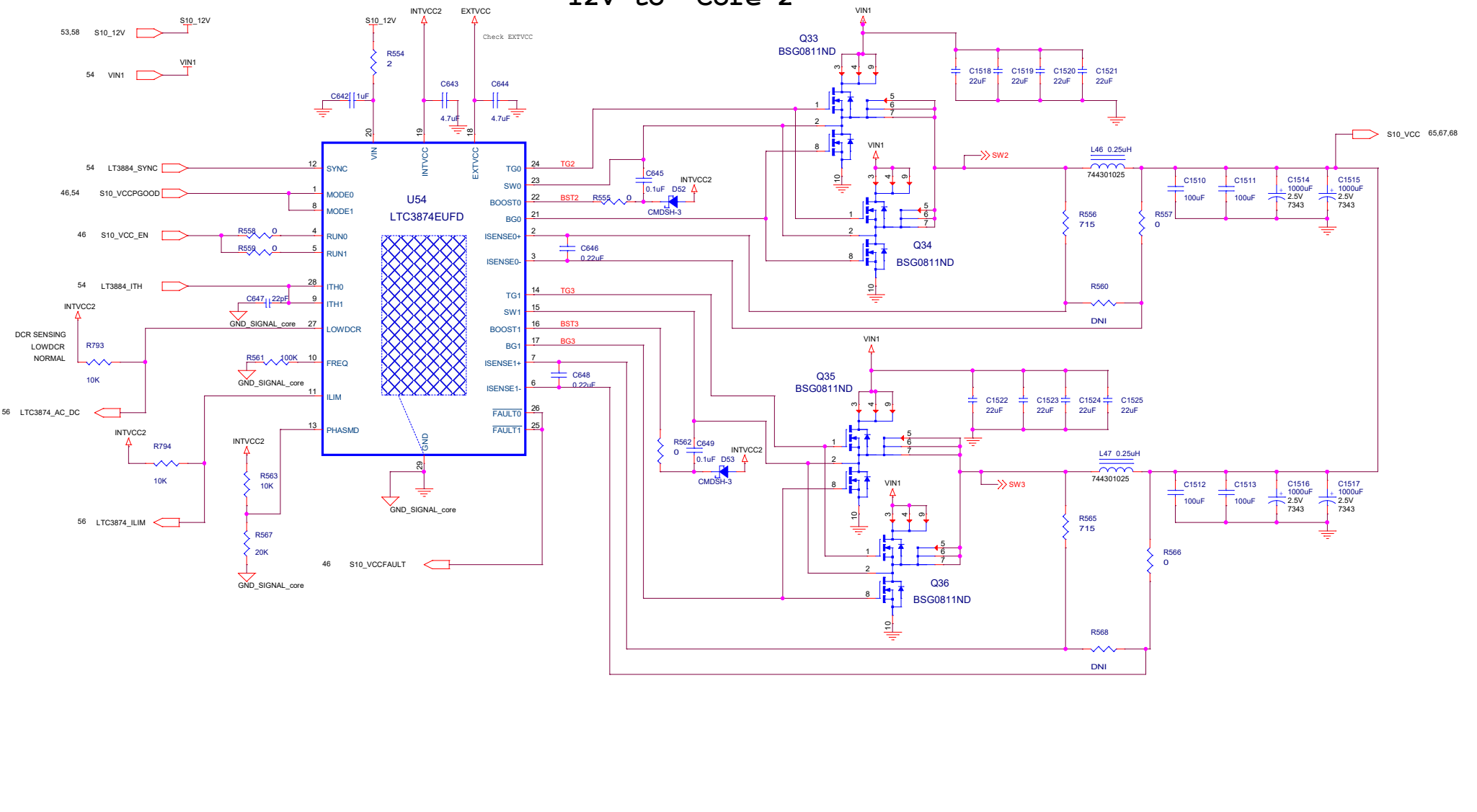
I2C Address: 0X5A, 0X5B and 0X47

Check Phase define  
Need 0.85V core voltage



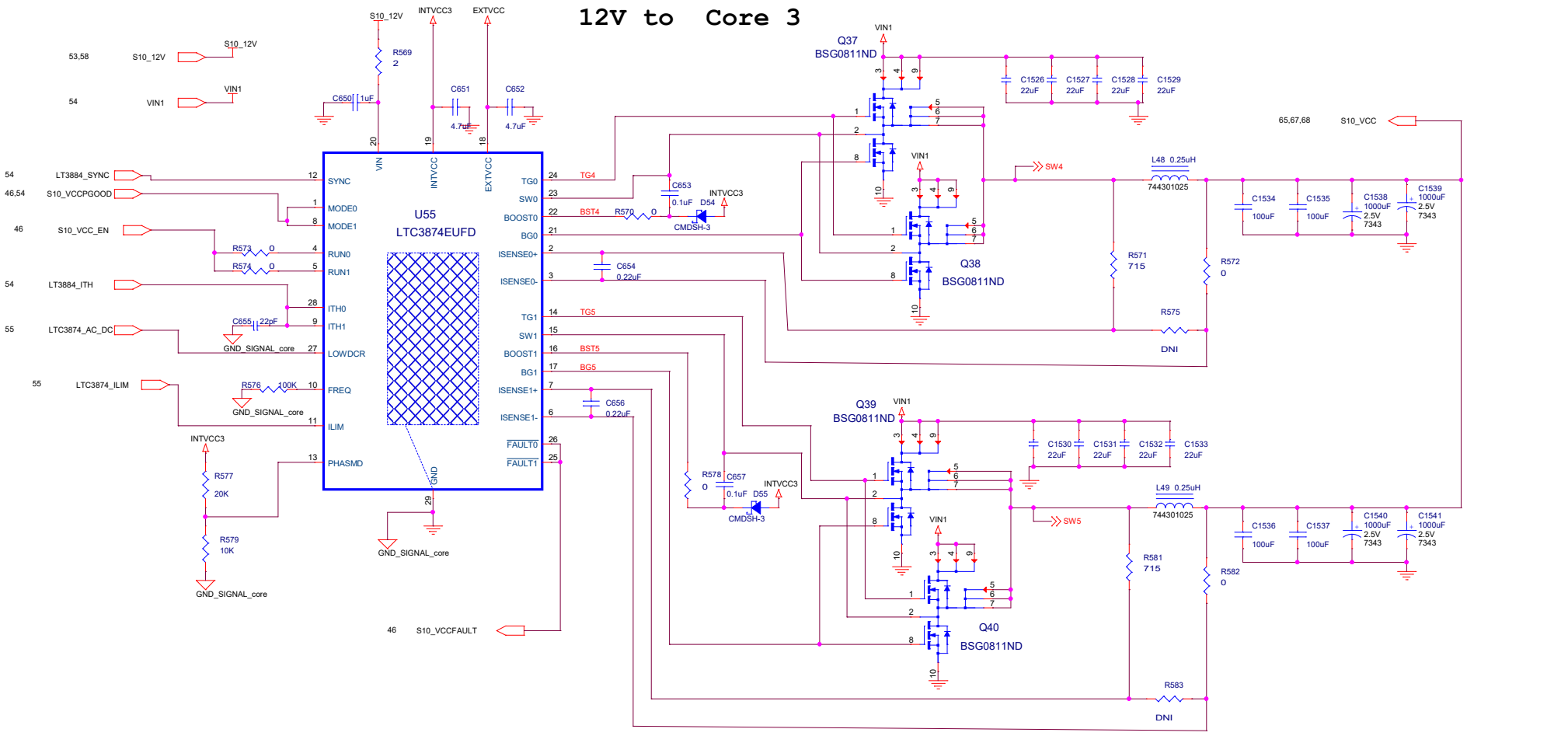
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# 12V to Core 2



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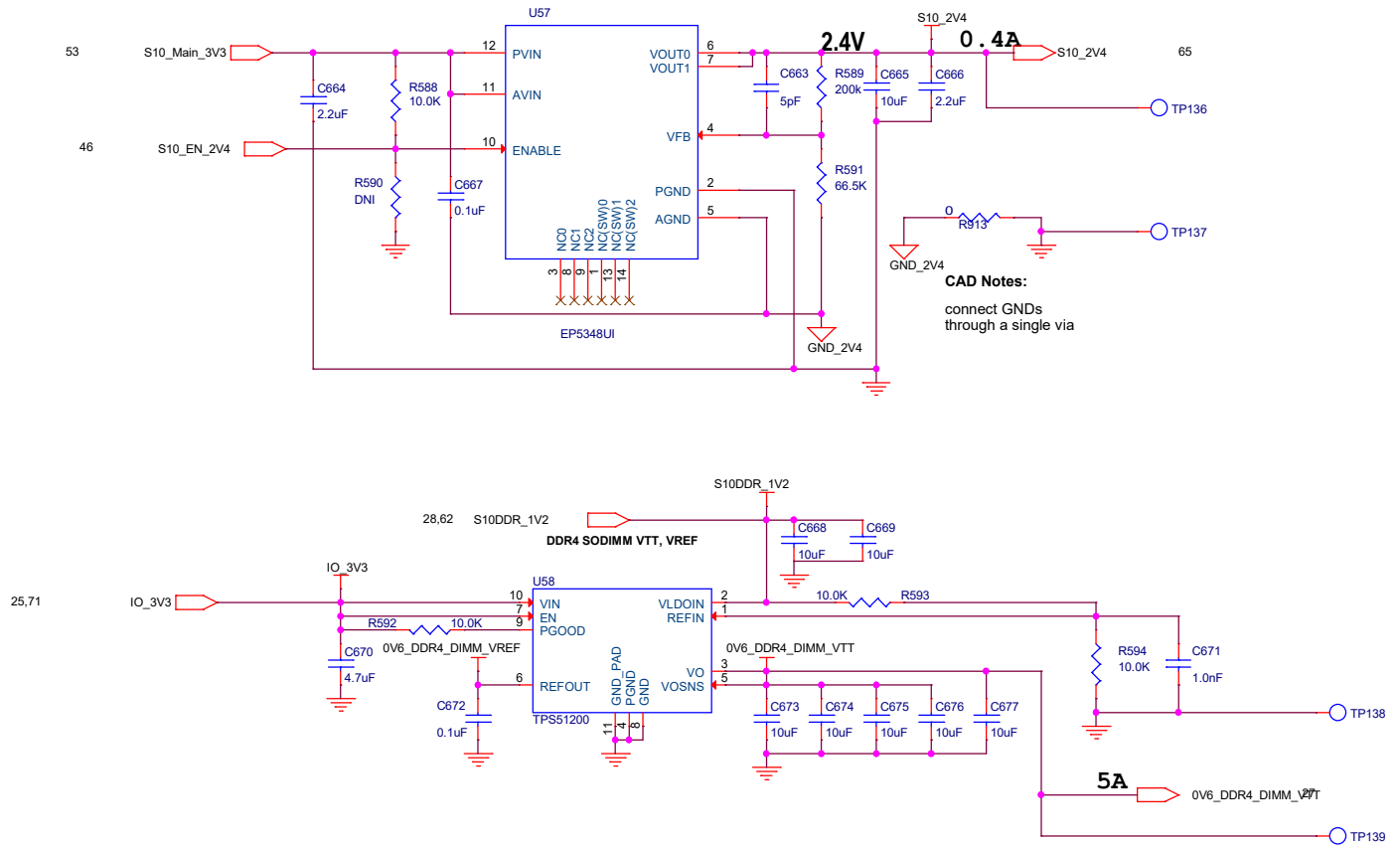
# 12V to Core 3



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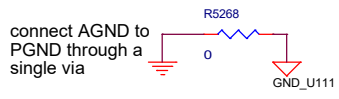
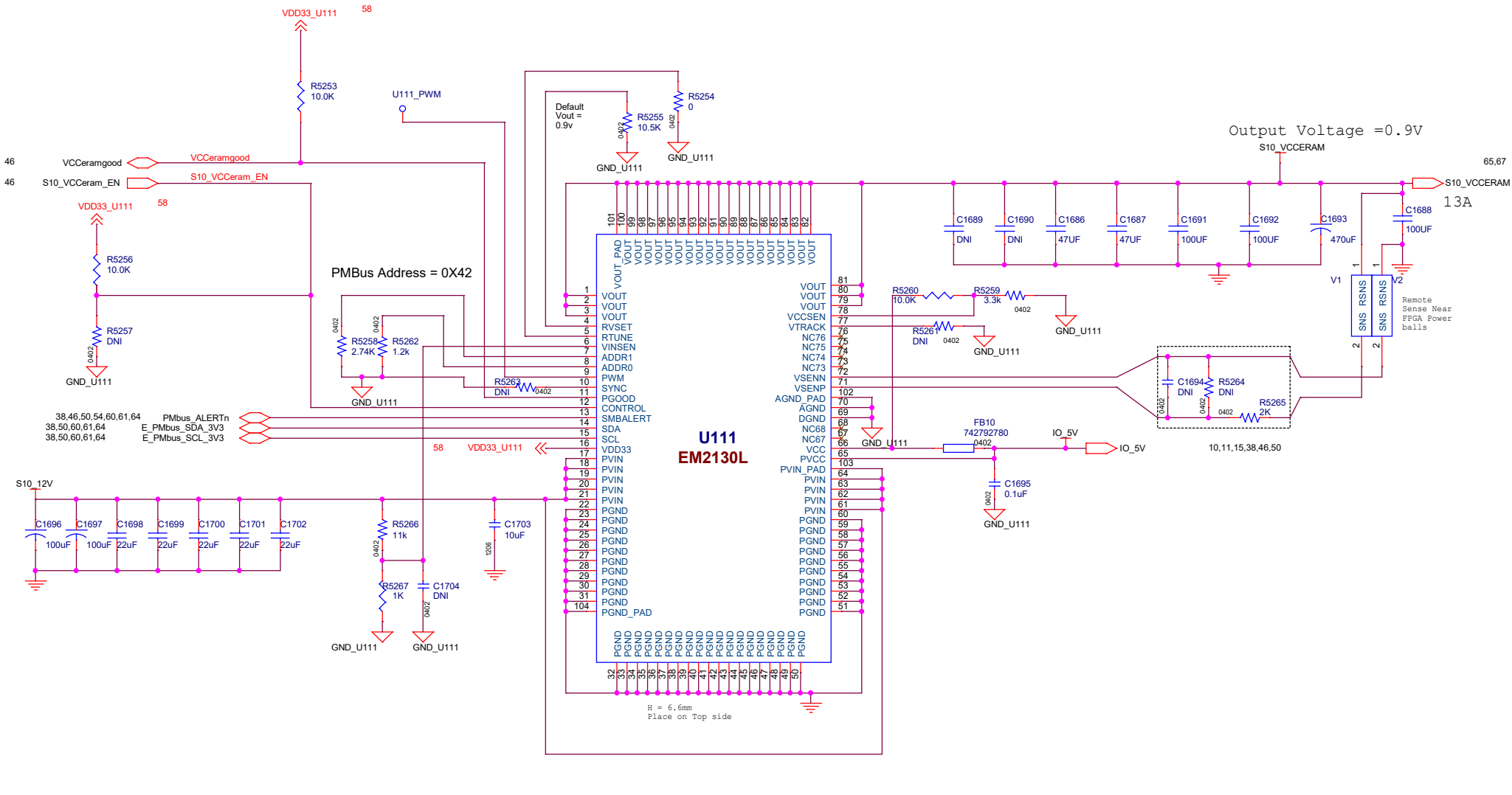


# VTT & 2V4 Power



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# Power - S10 VCCERAM



H = 6.6mm  
Place on Top side

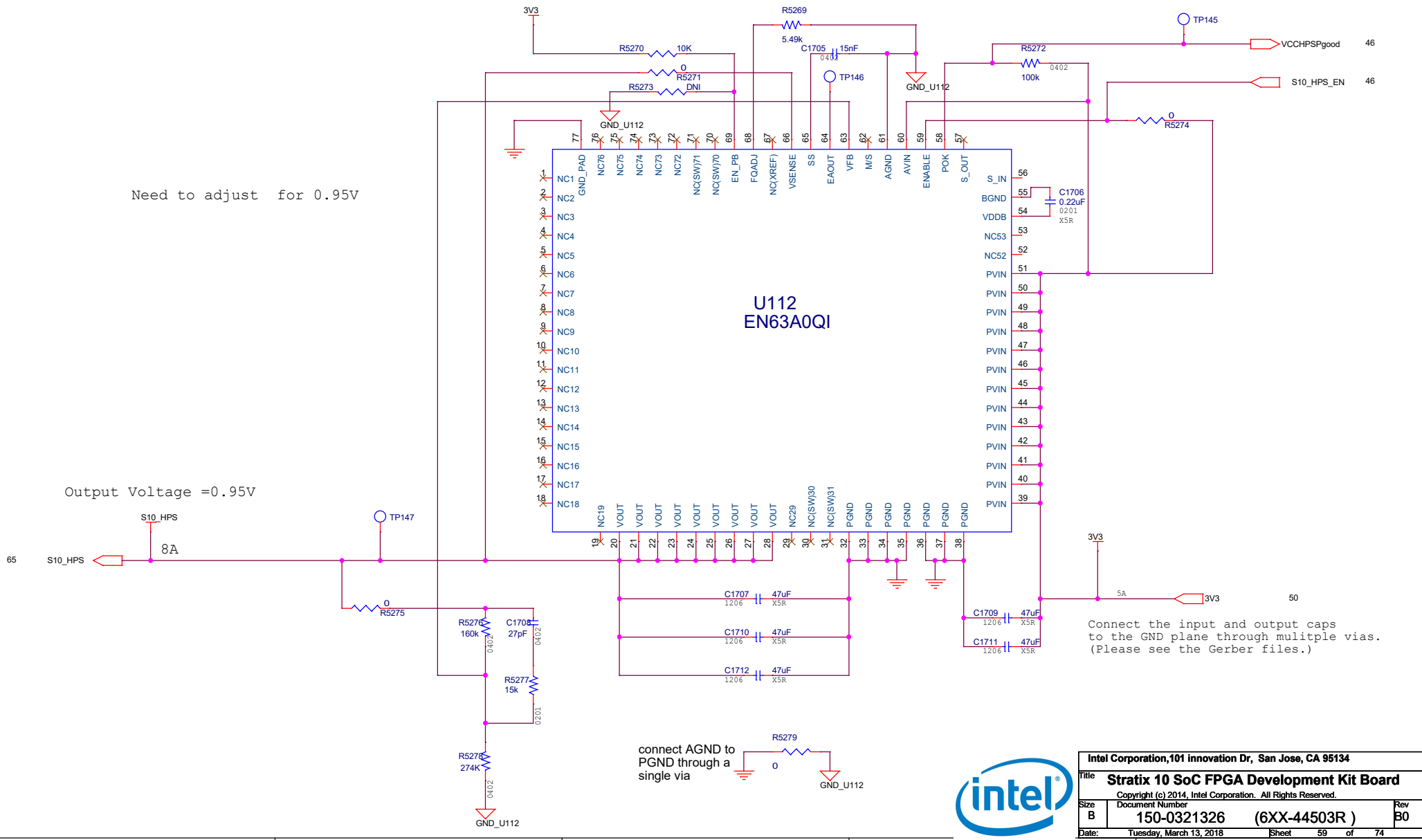


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# S10\_HPS Supply

Need to adjust for 0.95V

Output Voltage = 0.95V



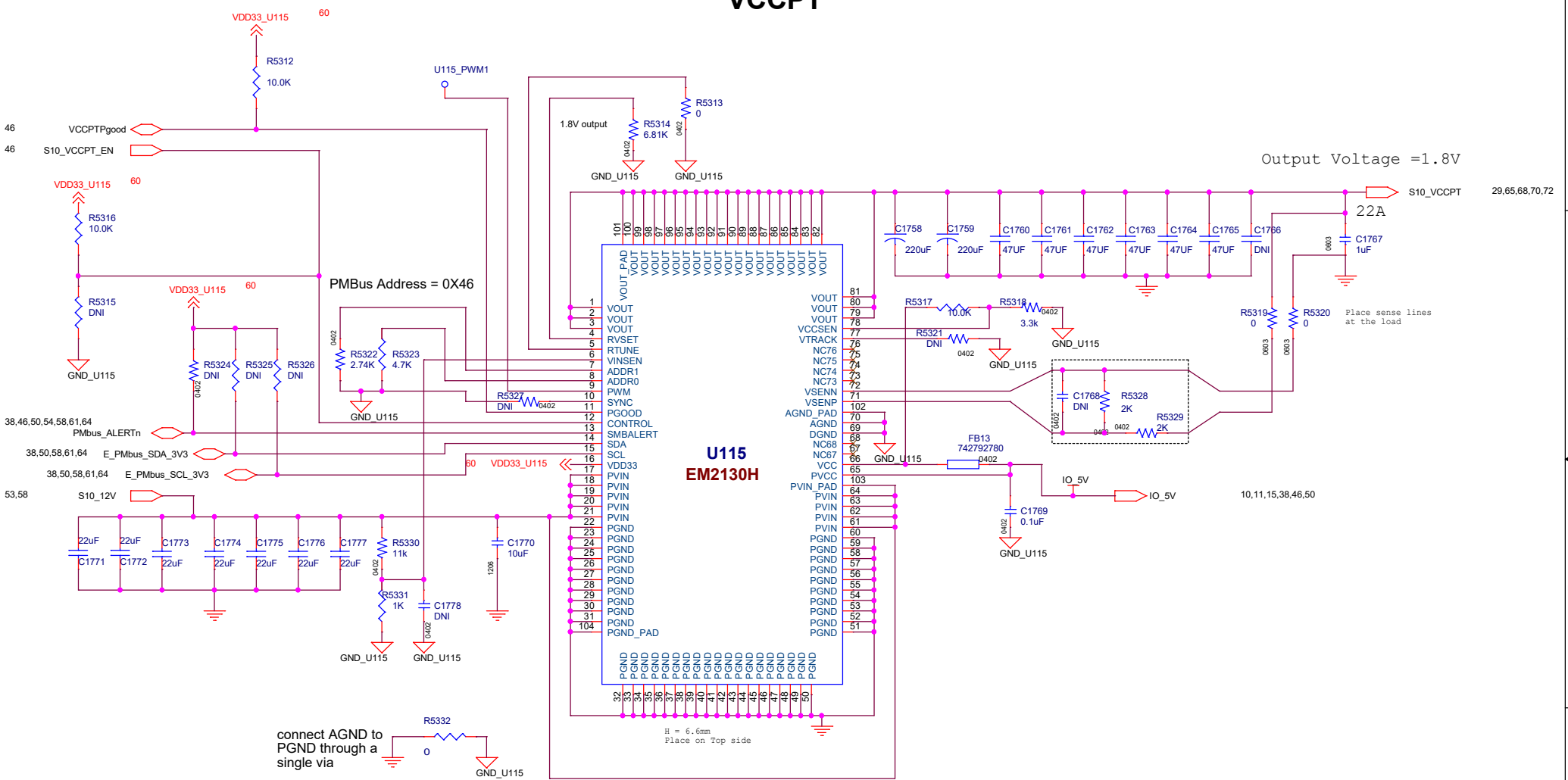
Connect the input and output caps to the GND plane through multiple vias. (Please see the Gerber files.)

connect AGND to PGND through a single via



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# VCCPT



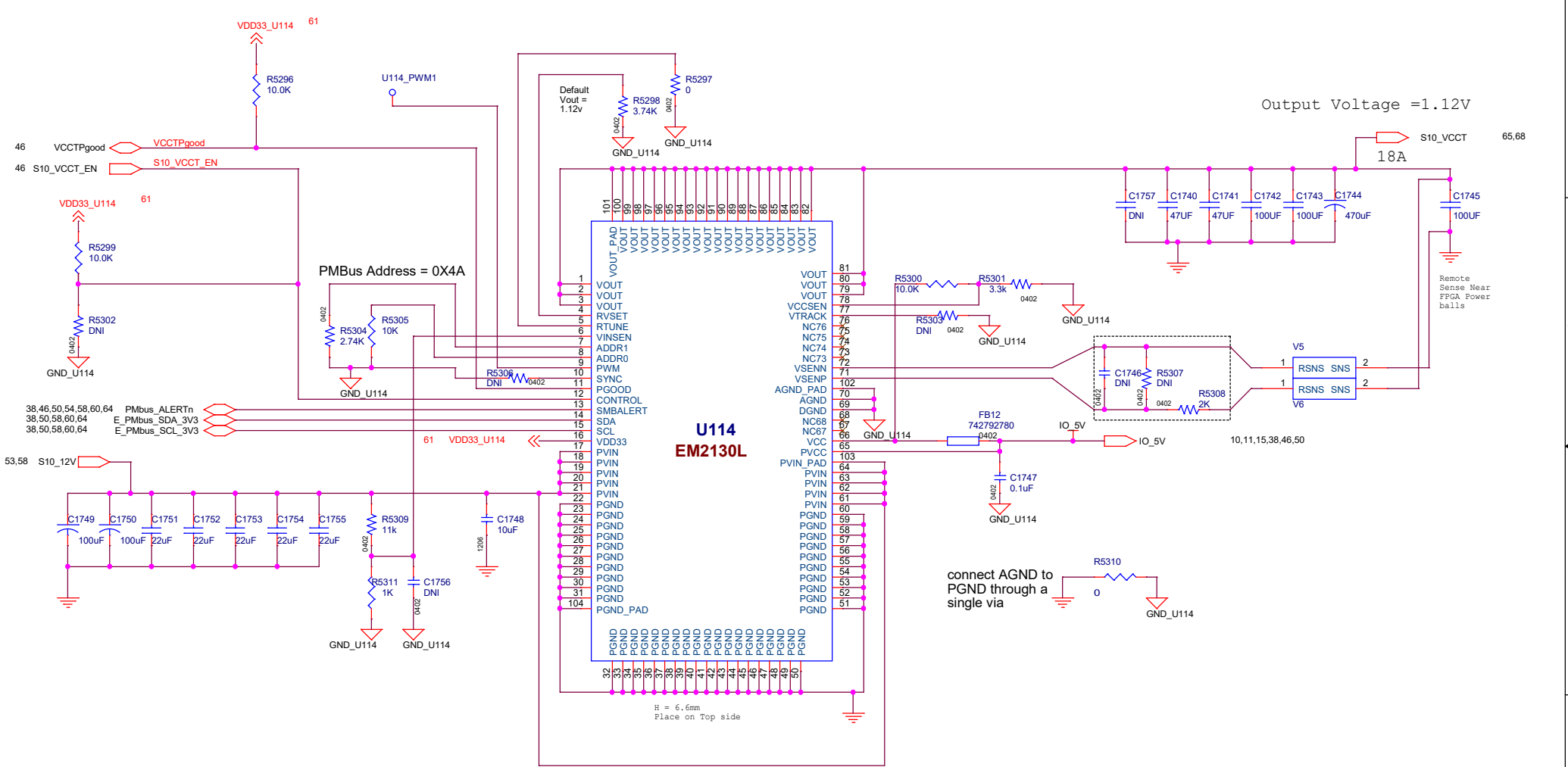
**U115**  
**EM2130H**

H = 6.6mm  
Place on Top side

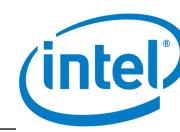


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# VCCT



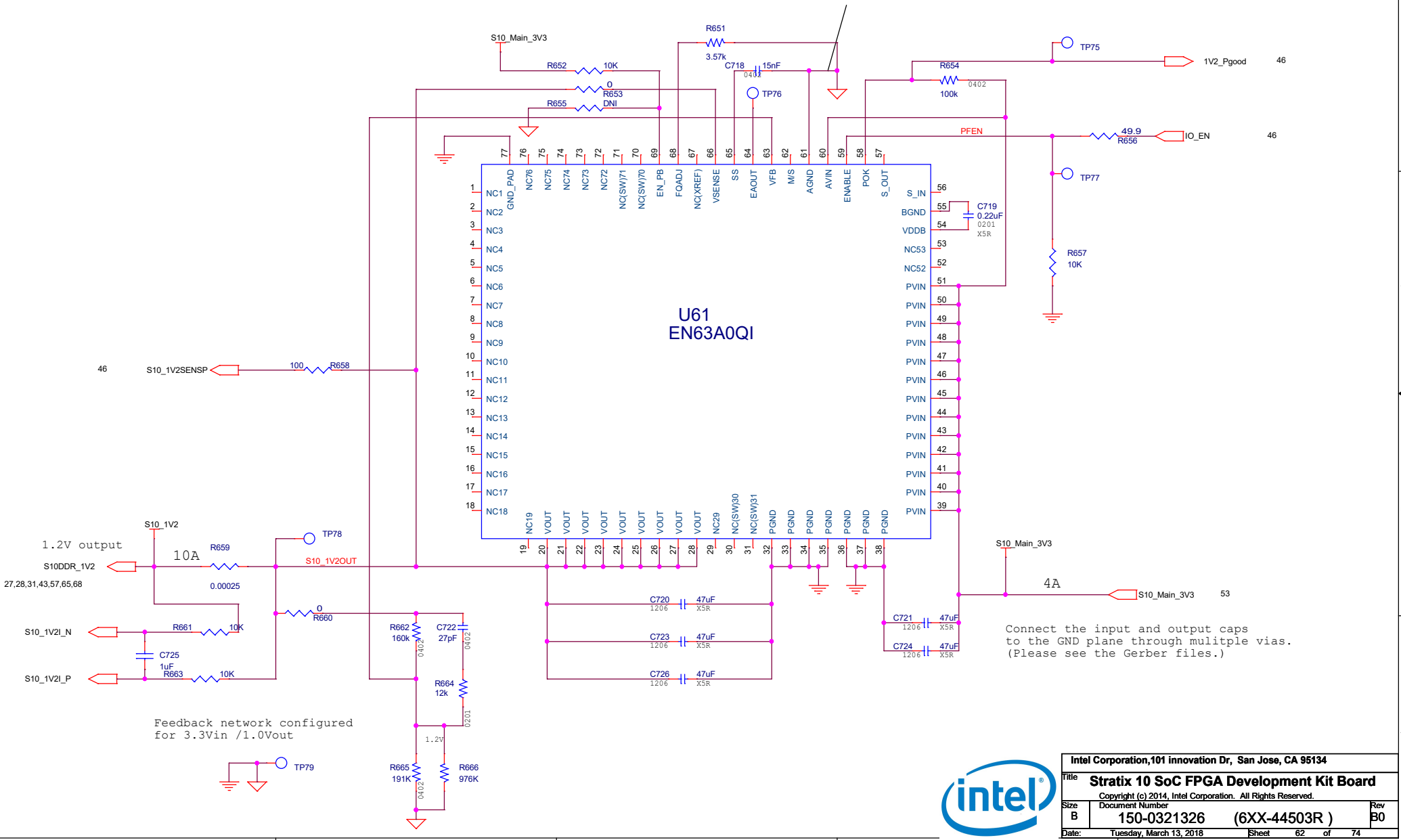
H = 6.6mm  
Place on Top side



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# 3.3V to 1.2V Converter

A single through-hole via connects the AGND pin to the GND plane.

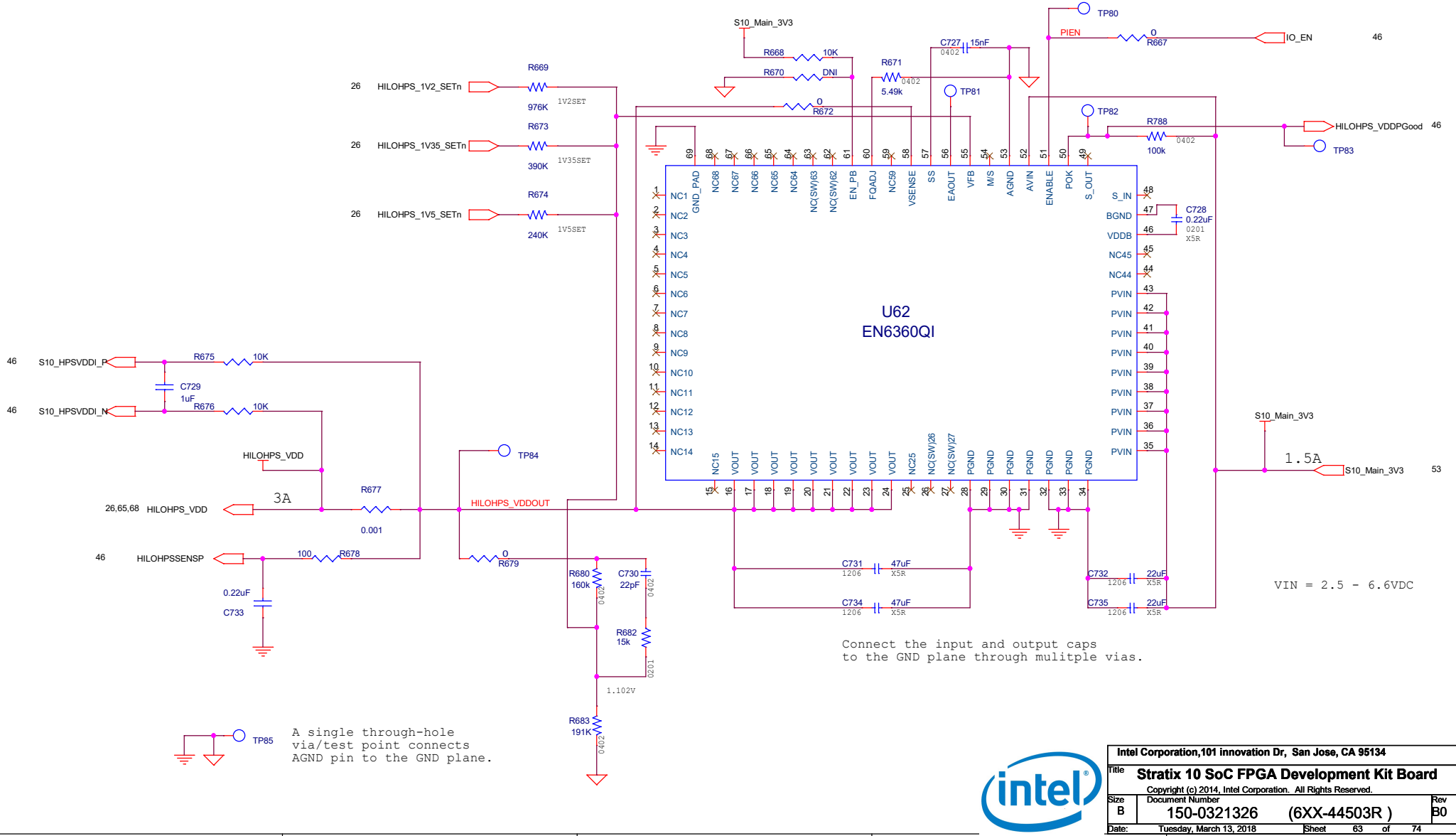


Connect the input and output caps to the GND plane through multiple vias. (Please see the Gerber files.)



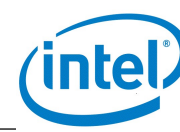
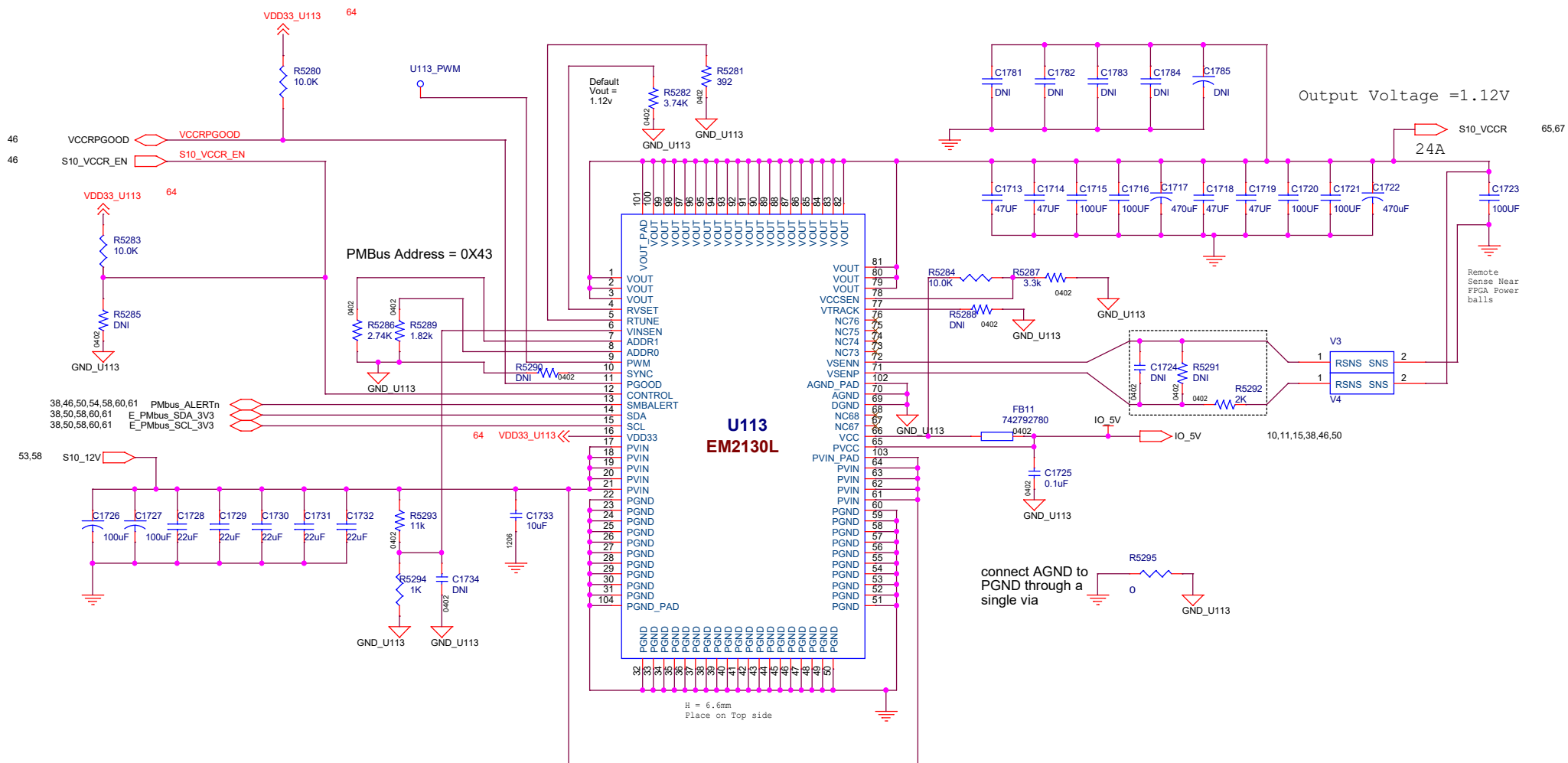
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# 3.3V to HPS HILO VDD converter

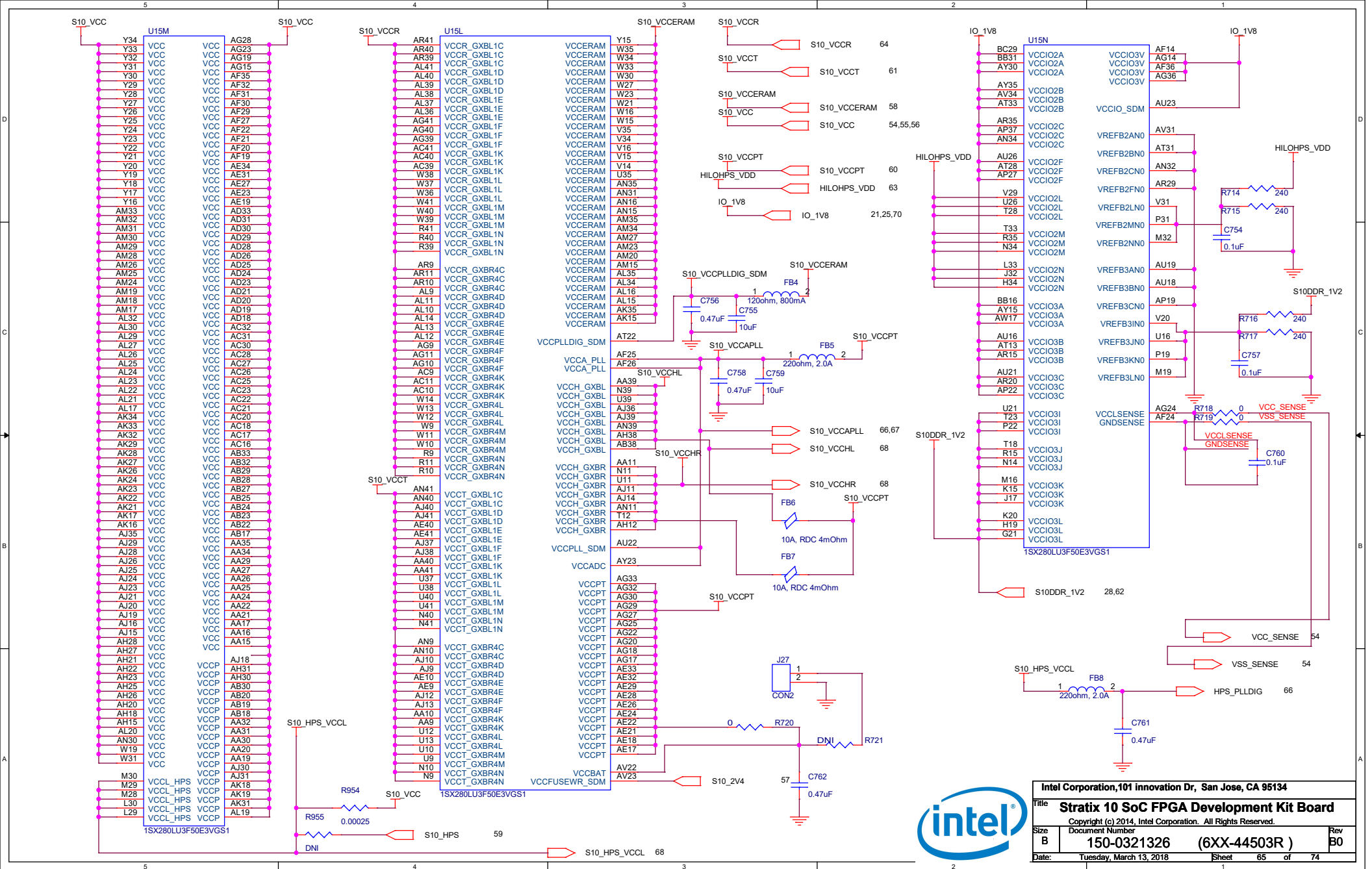


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# VCCR

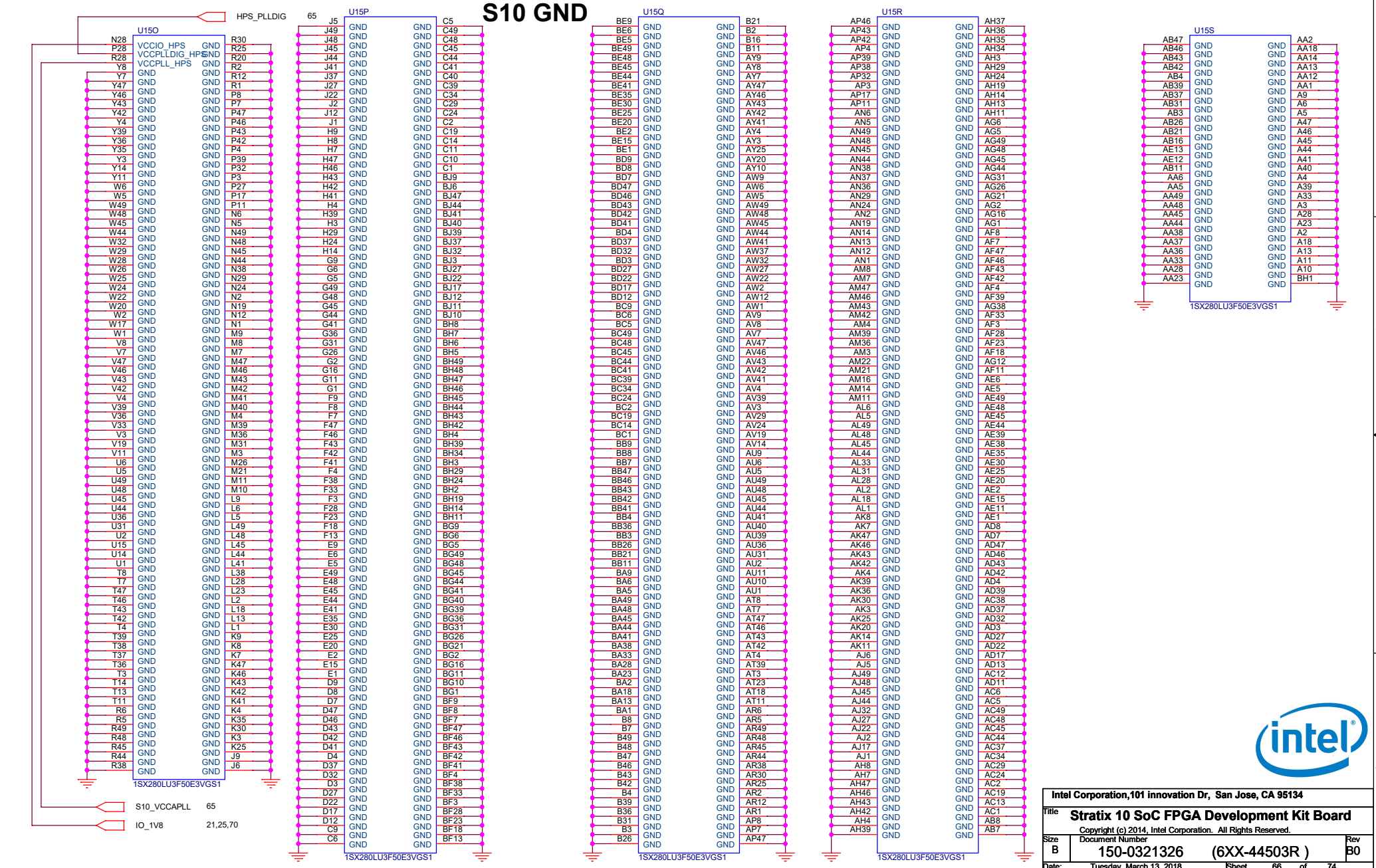






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# S10 GND



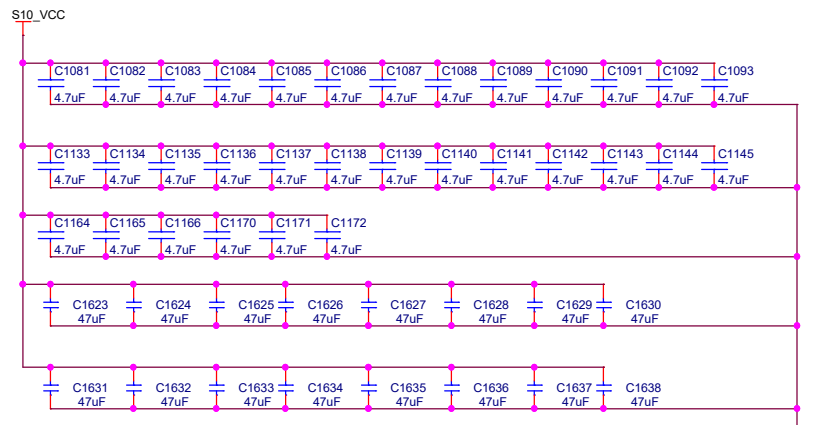
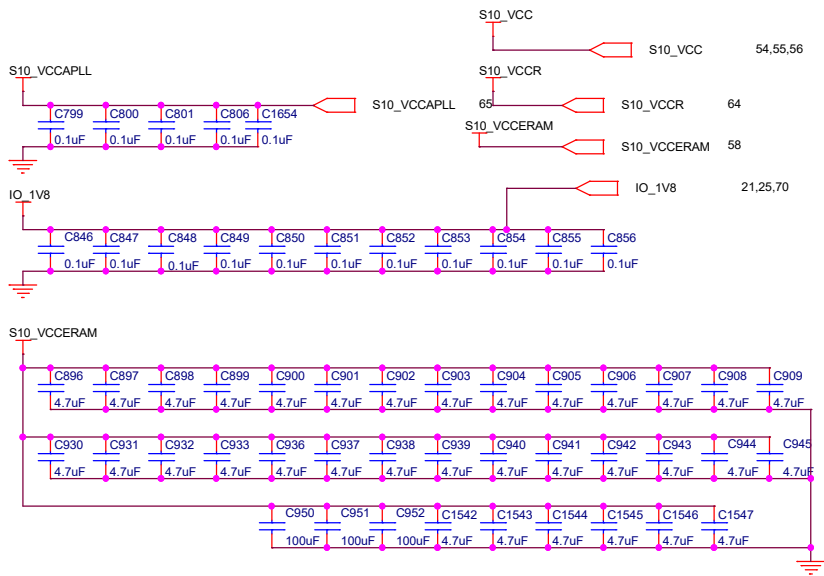
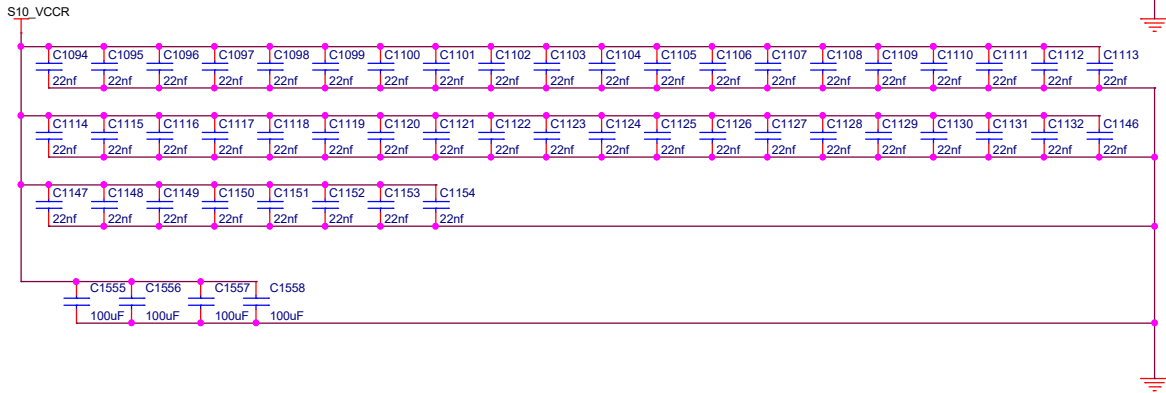
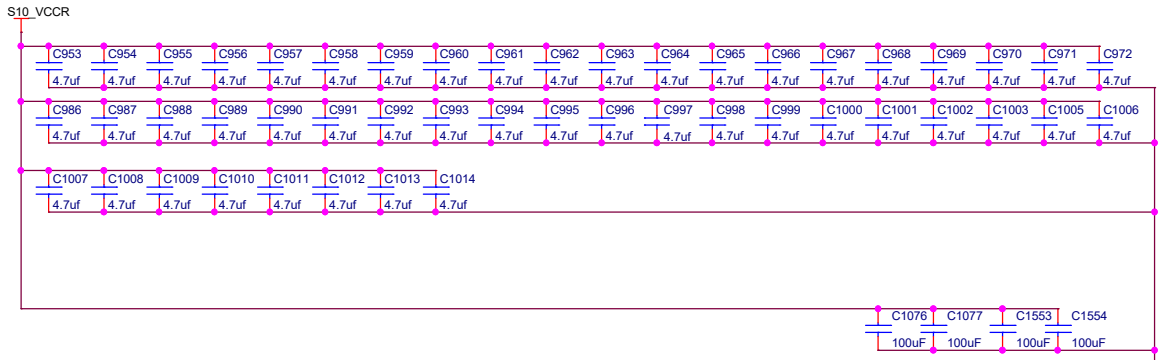
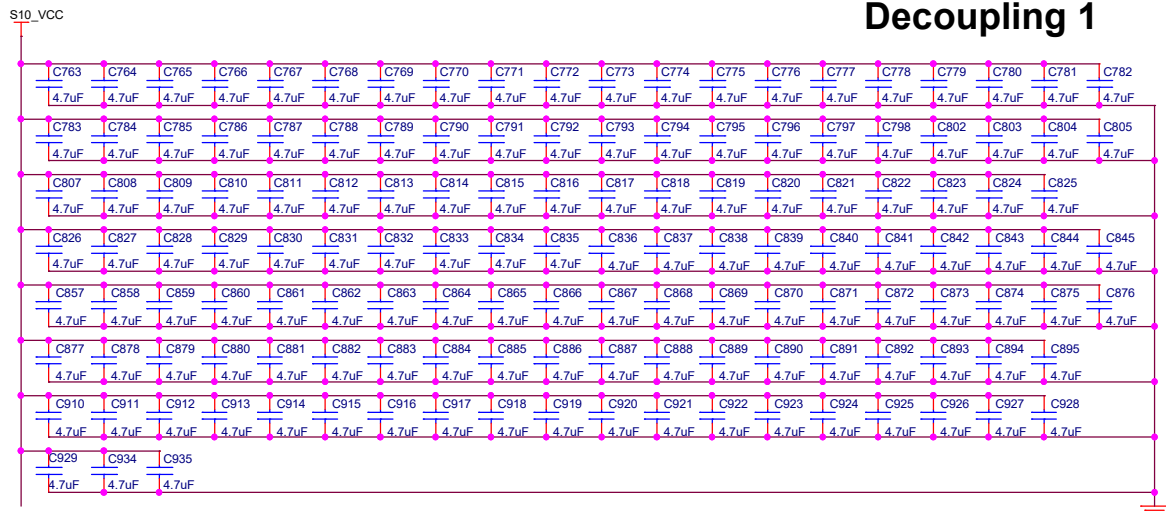
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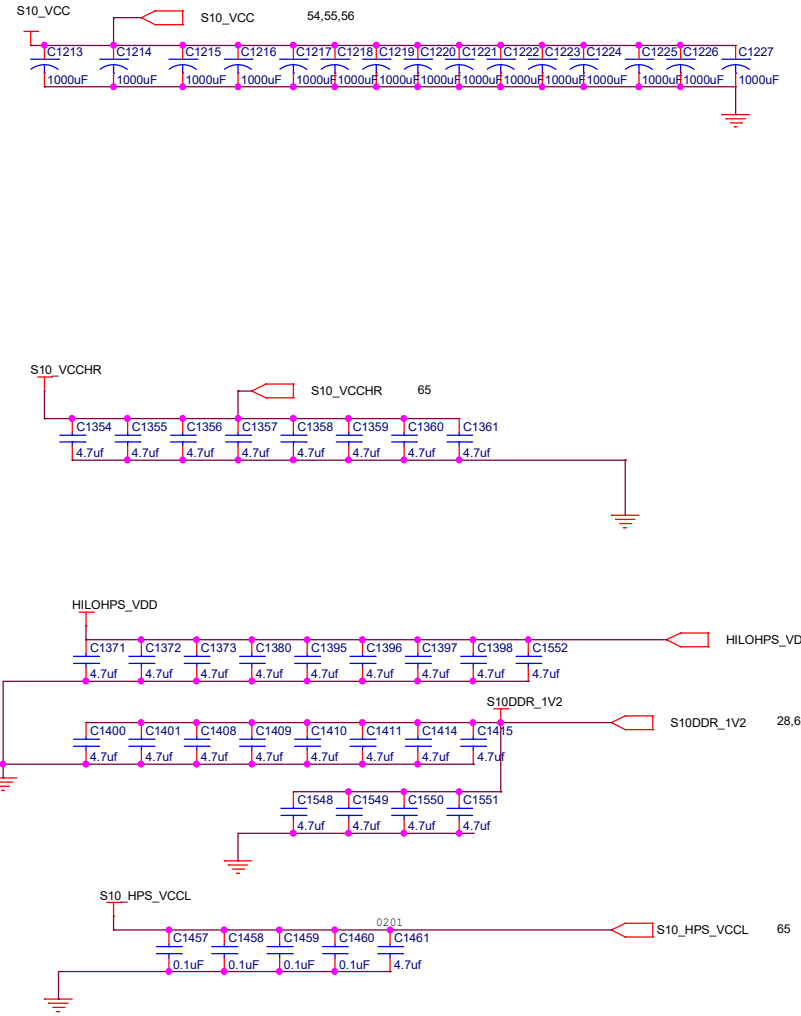
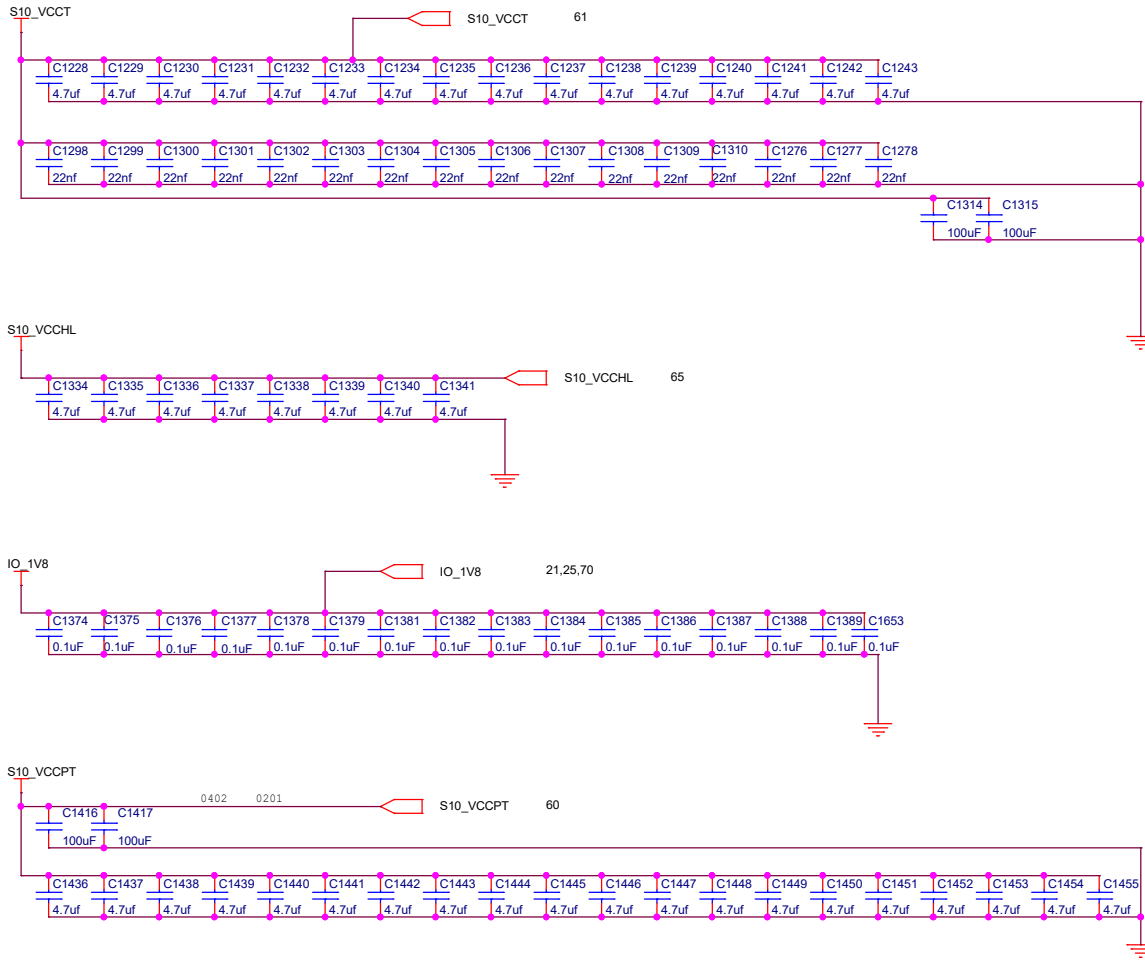
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# Decoupling 1



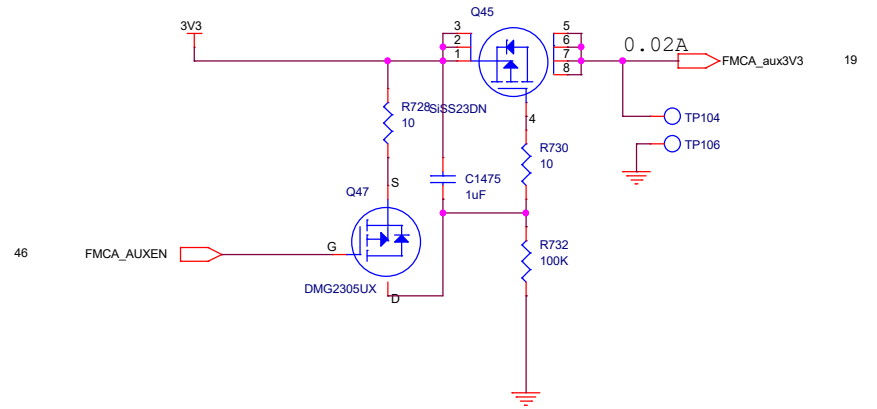
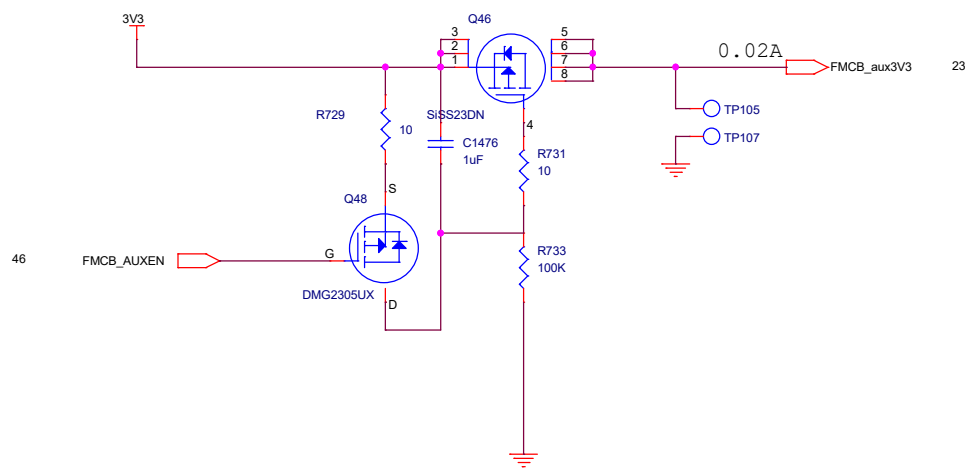
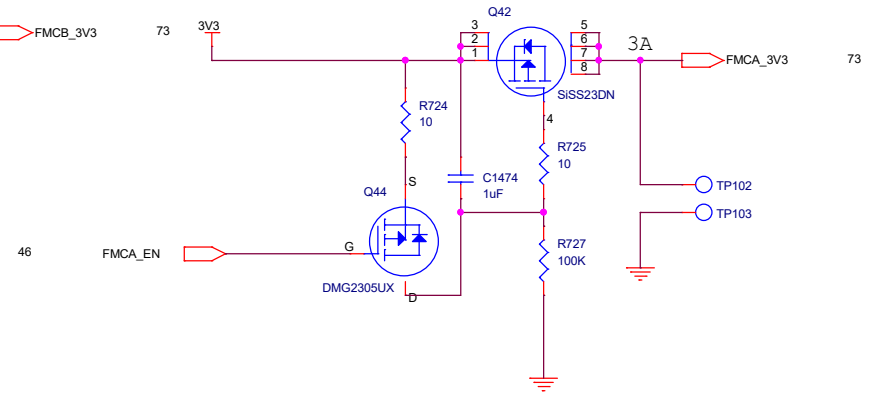
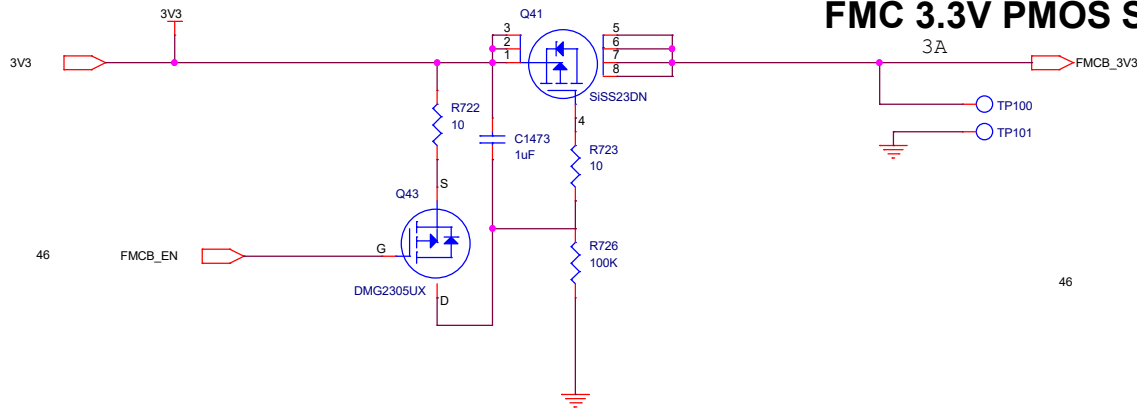
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# Decoupling 2



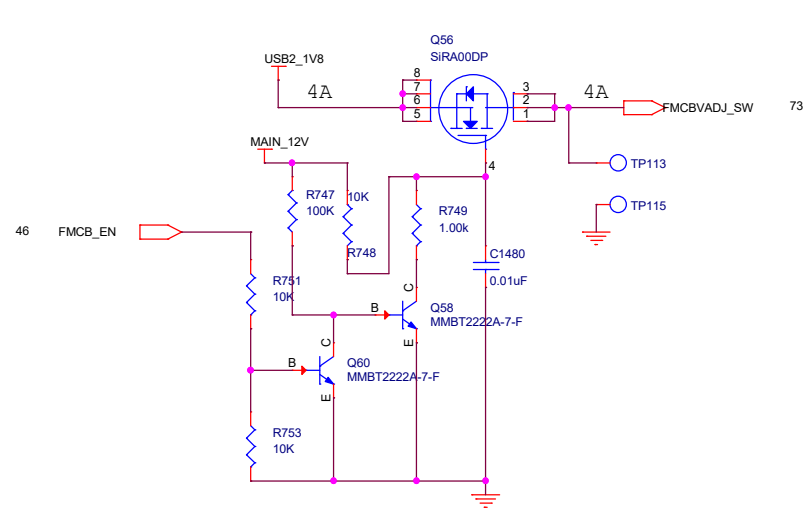
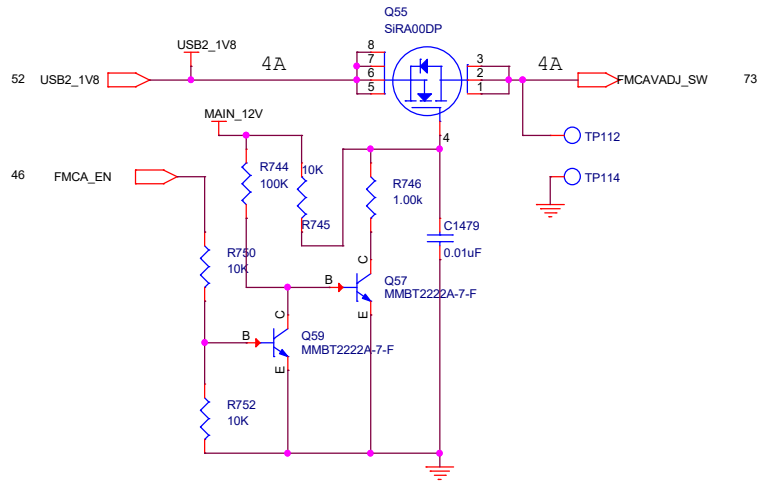
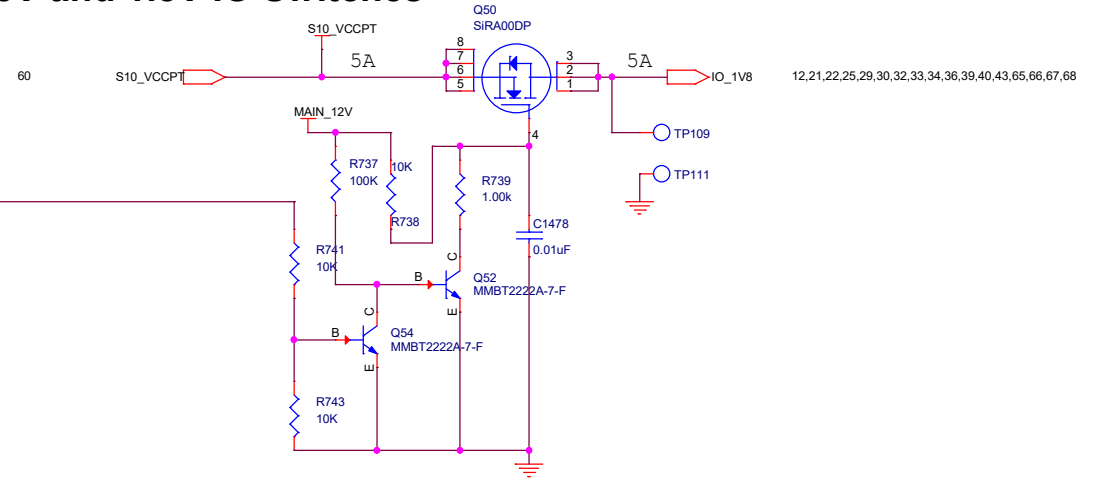
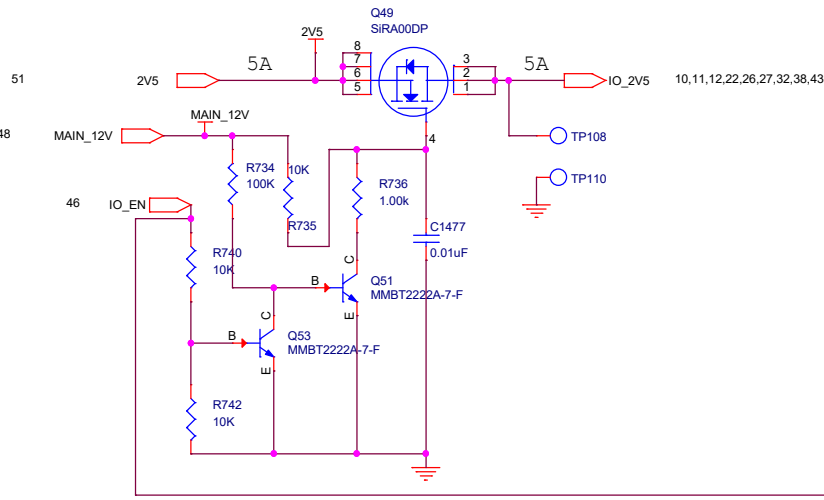
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# FMC 3.3V PMOS Switches



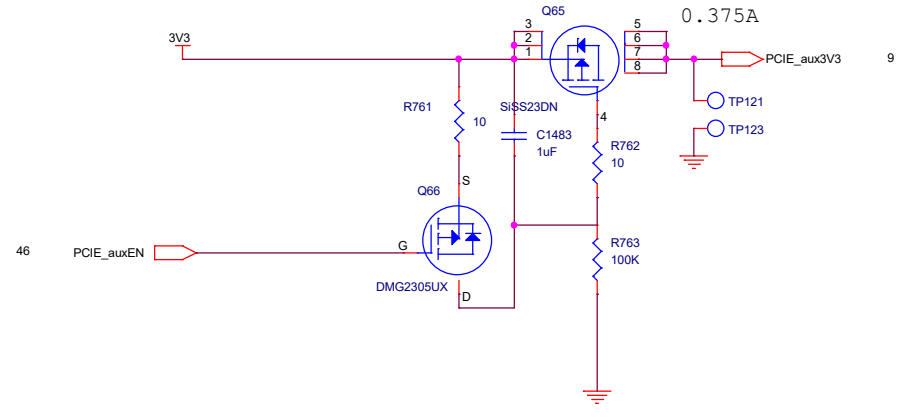
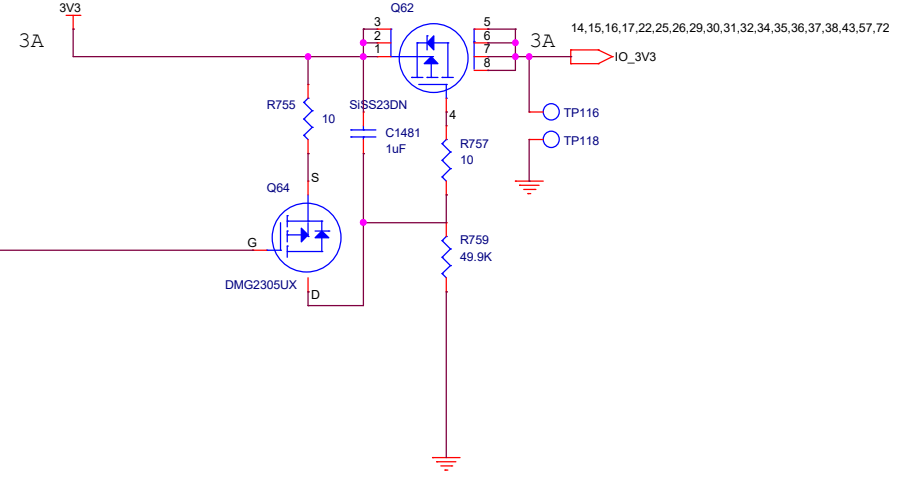
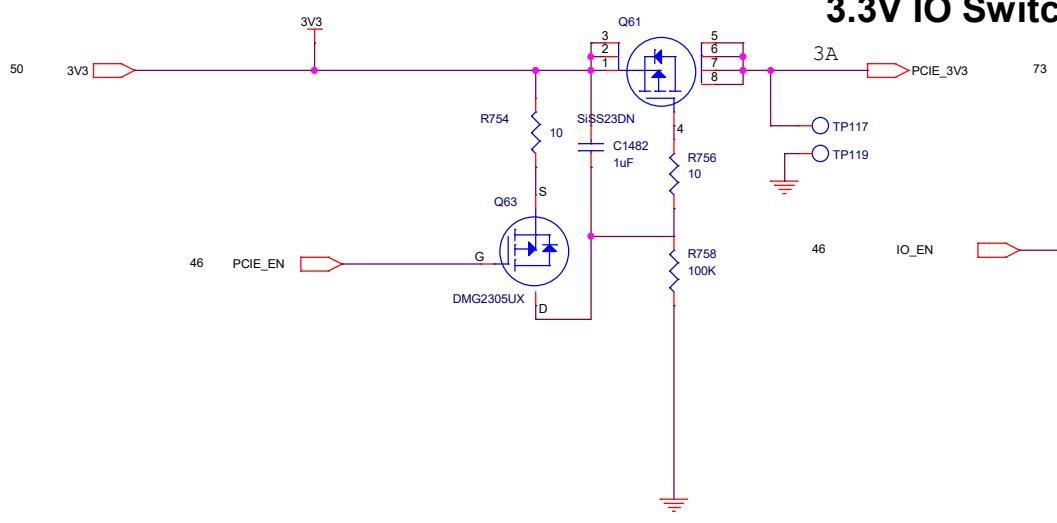
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# 2.5V and 1.8V IO Switches



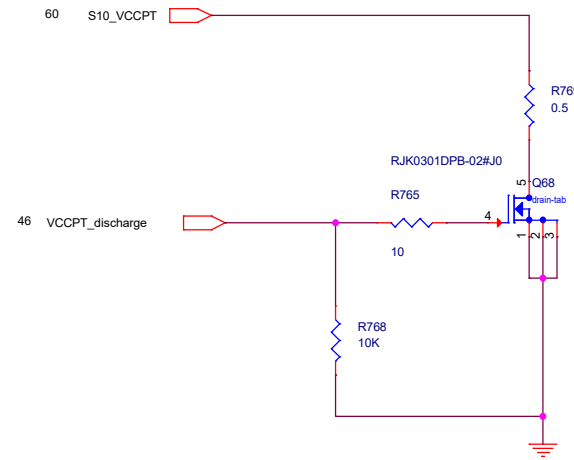
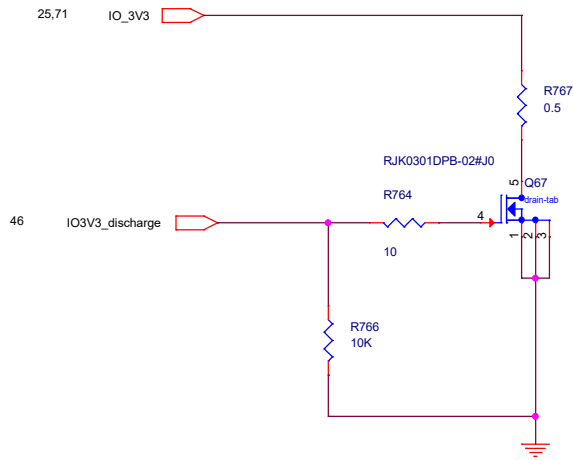
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# 3.3V IO Switches



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# 3.3V and 1.8V Discharge Load



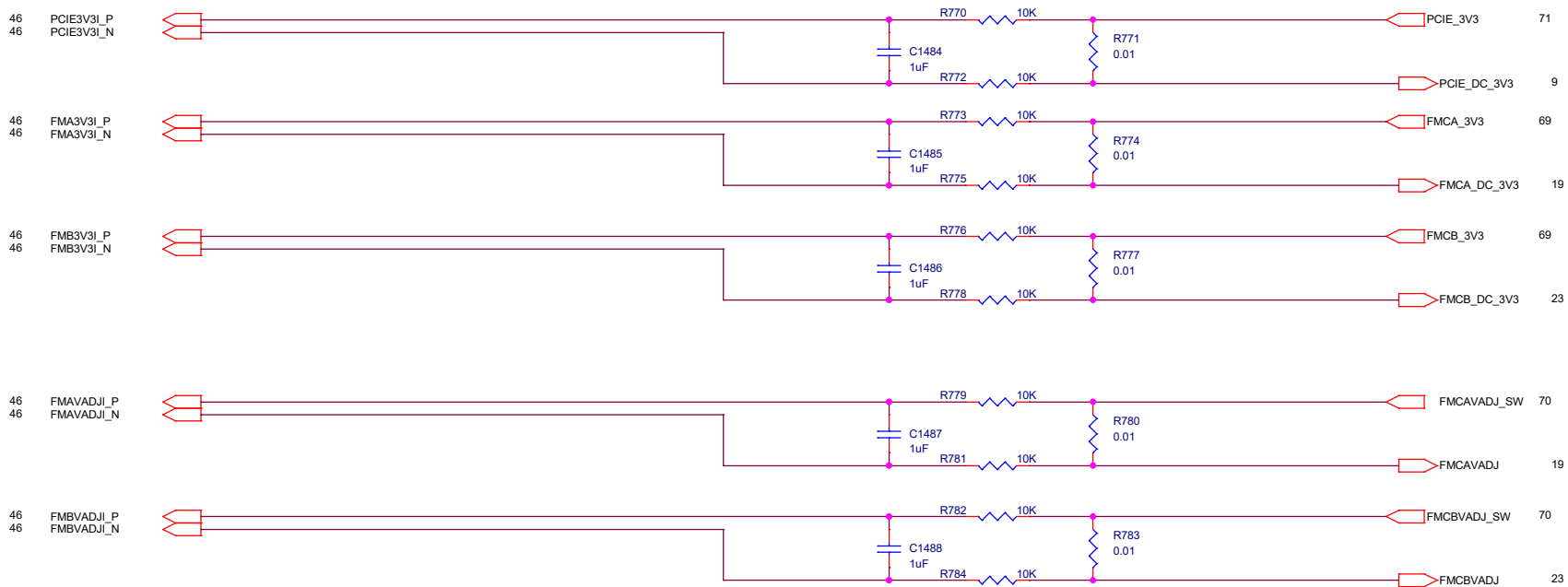
50us Discharge time



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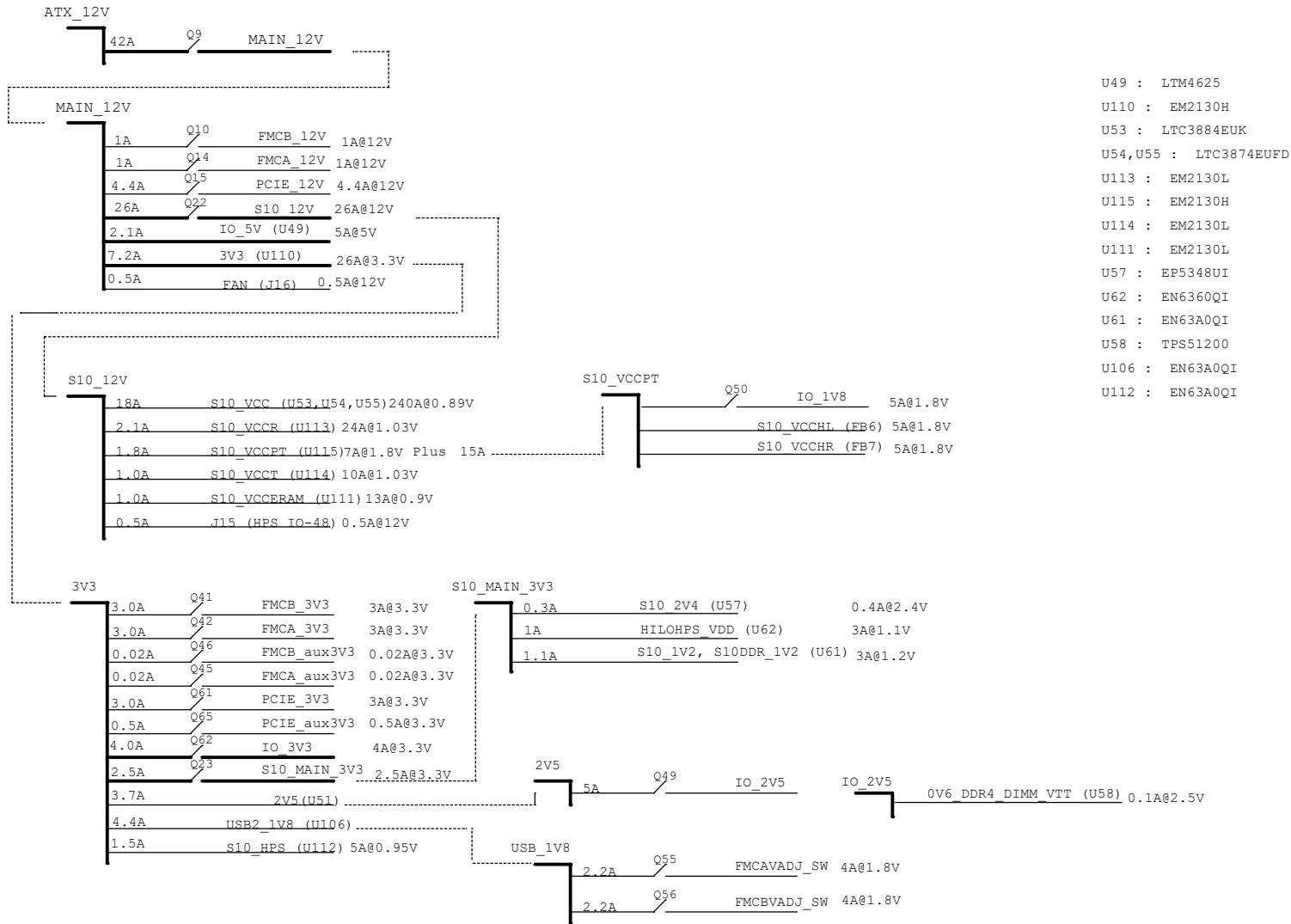


# User DC card 3.3V Current Sensors



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# System Power Connection Chart



- U49 : LTM4625
- U110 : EM2130H
- U53 : LTC3884EUK
- U54,U55 : LTC3874EUFD
- U113 : EM2130L
- U115 : EM2130H
- U114 : EM2130L
- U111 : EM2130L
- U57 : EP5348UI
- U62 : EN6360QI
- U61 : EN63A0QI
- U58 : TPS51200
- U106 : EN63A0QI
- U112 : EN63A0QI



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