



Bank Number	REF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		DNU					E33									
		DNU					F33									
		DNU					F34									
GXB L1		REFCLK0n					R27									
GXB L1		REFCLK0p					R28									
GXB L1		GXB_TX_L1n					G31									
GXB L1		GXB_TX_L1p					G32									
GXB L1		GXB_RX_L1p_GXB_REFCLK_L1p					H34									
GXB L1		GXB_RX_L1n_GXB_REFCLK_L1n					H33									
GXB L1		GXB_TX_L1n					L31									
GXB L1		GXB_TX_L1p					L32									
GXB L1		GXB_RX_L1p_GXB_REFCLK_L1p					K34									
GXB L1		GXB_RX_L1n_GXB_REFCLK_L1n					K33									
GXB L1		GXB_TX_L1n					L31									
GXB L1		GXB_TX_L1p					L32									
GXB L1		GXB_RX_L1n_GXB_REFCLK_L1n					M33									
GXB L1		GXB_TX_L1n					N31									
GXB L1		GXB_TX_L1p					N32									
GXB L1		GXB_RX_L1p_GXB_REFCLK_L1p					P34									
GXB L1		GXB_RX_L1n_GXB_REFCLK_L1n					P33									
GXB L1		GXB_TX_L1n					R31									
GXB L1		GXB_TX_L1p					R32									
GXB L1		GXB_RX_L1p_GXB_REFCLK_L1p					T34									
GXB L1		GXB_RX_L1n_GXB_REFCLK_L1n					T33									
GXB L1		GXB_TX_L1n					U31									
GXB L1		GXB_TX_L1p					U32									
GXB L1		GXB_RX_L1p_GXB_REFCLK_L1p					V34									
GXB L1		GXB_RX_L1n_GXB_REFCLK_L1n					V33									
GXB L1		REFCLK0n					U27									
GXB L1		REFCLK0p					U28									
GXB L0		REFCLK1n					W27									
GXB L0		REFCLK1p					W28									
GXB L0		GXB_TX_L5n					W31									
GXB L0		GXB_TX_L5p					W32									
GXB L0		GXB_RX_L5p_GXB_REFCLK_L5p					Y34									
GXB L0		GXB_RX_L5n_GXB_REFCLK_L5n					Y33									
GXB L0		GXB_TX_L4n					AA31									
GXB L0		GXB_TX_L4p					AA32									
GXB L0		GXB_RX_L4p_GXB_REFCLK_L4p					AB34									
GXB L0		GXB_RX_L4n_GXB_REFCLK_L4n					AB33									
GXB L0		GXB_TX_L3n					AC31									
GXB L0		GXB_TX_L3p					AC32									
GXB L0		GXB_RX_L3p_GXB_REFCLK_L3p					AD34									
GXB L0		GXB_RX_L3n_GXB_REFCLK_L3n					AD33									
GXB L0		GXB_TX_L2n					AE31									
GXB L0		GXB_TX_L2p					AE32									
GXB L0		GXB_RX_L2p_GXB_REFCLK_L2p					AF34									
GXB L0		GXB_RX_L2n_GXB_REFCLK_L2n					AF33									
GXB L0		GXB_TX_L1n					AG31									
GXB L0		GXB_TX_L1p					AG32									
GXB L0		GXB_RX_L1p_GXB_REFCLK_L1p					AH34									
GXB L0		GXB_RX_L1n_GXB_REFCLK_L1n					AH33									
GXB L0		GXB_TX_L0n					AJ31									
GXB L0		GXB_TX_L0p					AJ32									
GXB L0		GXB_RX_L0p_GXB_REFCLK_L0p					AK34									
GXB L0		GXB_RX_L0n_GXB_REFCLK_L0n					AK33									
GXB L0		REFCLK0n					AA28									
GXB L0		REFCLK0p					AA27									
		DNU					AL32									
3A		TDO		TDO			AM33									
3A		TMS		TMS			AD30									
3A		TDK		TDK			AM34									
3A		TDI		TDI			AN34									
3A		DCLK		DCLK			AP33									
3A		ASDO		ASDO			AC08									
3A		AS_DATA3		DATA3			AL31									
3A		AS_DATA2		DATA2			AM32									
3A		AS_DATA1		DATA1			AN33									
3A		AS_DATA0_ASDO		DATA0			AL30									
3A	VREFB3A0		RZD_0		DIFF0_TX_B1n	DIFFOUT_B1n	AM30									
3A	VREFB3A0		CLK0n		DIFF0_RX_B2n	DIFFOUT_B2n	AM29									
3A	VREFB3A0		CLK0p		DIFF0_TX_B2p	DIFFOUT_B2p	AG29									
3A	VREFB3A0		CLK1n		DIFF0_RX_B4n	DIFFOUT_B4n	AH29									
3A	VREFB3A0		CLK1p		DIFF0_RX_B4p	DIFFOUT_B4p	AH28									
3A	VREFB3A0		FPLL_BL_CLKOUT1_FPLL_BL_CLKOUTn		DIFF0_TX_B5n	DIFFOUT_B5n	AJ29									
3A	VREFB3A0		FPLL_BL_CLKOUT0_FPLL_BL_CLKOUTp		DIFF0_TX_B5p	DIFFOUT_B5p	AK29									
3A	VREFB3A0		FPLL_BL_CLKOUT3_FPLL_BL_FBI		DIFF0_RX_B6n	DIFFOUT_B6n	AM31									
3A	VREFB3A0		FPLL_BL_CLKOUT2_FPLL_BL_FBI		DIFF0_RX_B6p	DIFFOUT_B6p	AN32									
3A	VREFB3A0		VREFB3A0		DIFF0_RX_B6p	DIFFOUT_B6p	AC27									
3A	VREFB3A0		CLK2n		DIFF0_RX_B7n	DIFFOUT_B7n	AG27									
3A	VREFB3A0		CLK2p		DIFF0_RX_B7p	DIFFOUT_B7p	AM27									
3A	VREFB3A0				DIFF0_TX_B8n	DIFFOUT_B8n	AP32				CS#_3A_1	CS#_3A_1				
3A	VREFB3A0				DIFF0_TX_B8p	DIFFOUT_B8p	AP31	DQ1B			CS#_3A_0	CS#_3A_0				
3A	VREFB3A0		CLK3n		DIFF0_RX_B9n	DIFFOUT_B9n	AH26	DQ1B								
3A	VREFB3A0		CLK3p		DIFF0_RX_B9p	DIFFOUT_B9p	AH26	DQ1B								
3A	VREFB3A0				DIFF0_TX_B10n	DIFFOUT_B10n	AE26	DQ1B			ODT_3A_1	ODT_3A_1				
3A	VREFB3A0				DIFF0_TX_B10p	DIFFOUT_B10p	AE26	DQ1B			ODT_3A_0	ODT_3A_0				
3A	VREFB3A0				DIFF0_RX_B11n	DIFFOUT_B11n	AL29	DQS1B/QK1B			WE#_3A					
3A	VREFB3A0				DIFF0_RX_B11p	DIFFOUT_B11p	AL28	DQS1B/CQ1B/CQn1B/QKn1B			CAS#_3A					
3A	VREFB3A0				DIFF0_TX_B12n	DIFFOUT_B12n	AN30	DQ1B			BA#_3A					
3A	VREFB3A0				DIFF0_TX_B12p	DIFFOUT_B12p	AP30	DQ1B			BA_3A_2					
3A	VREFB3A0				DIFF0_RX_B13n	DIFFOUT_B13n	AM28	DQ1B			BA_3A_1					
3A	VREFB3A0				DIFF0_RX_B13p	DIFFOUT_B13p	AM29	DQ1B			BA_3A_0					
3A	VREFB3A0				DIFF0_TX_B14n	DIFFOUT_B14n	AD27	DQ1B			A_3A_15					
3A	VREFB3A0				DIFF0_TX_B14p	DIFFOUT_B14p	AE27	DQ1B			A_3A_14					
3A	VREFB3A0				DIFF0_RX_B15n	DIFFOUT_B15n	AJ27	DQ1B			A_3A_13					
3A	VREFB3A0				DIFF0_RX_B15p	DIFFOUT_B15p	AK27	DQ1B			A_3A_12					
3A	VREFB3A0				DIFF0_TX_B16n	DIFFOUT_B16n	AP29	DQ1B			A_3A_11					
3A	VREFB3A0				DIFF0_TX_B16p	DIFFOUT_B16p	AP28	DQ2B			A_3A_10					
3A	VREFB3A0				DIFF0_RX_B17n	DIFFOUT_B17n	AL27	DQ2B			CA_3A_9					
3A	VREFB3A0				DIFF0_RX_B17p	DIFFOUT_B17p	AM27	DQ2B			CA_3A_8					
3A	VREFB3A0				DIFF0_TX_B18n	DIFFOUT_B18n	AE28	DQ1B			A_3A_7	CA_3A_7				
3A	VREFB3A0				DIFF0_TX_B18p	DIFFOUT_B18p	AE28	DQ2B			CA_3A_6	CA_3A_6				
3A	VREFB3A0				DIFF0_RX_B19n	DIFFOUT_B19n	AJ26	DQS2B/QK2B			A_3A_5	CA_3A_5				
3A	VREFB3A0				DIFF0_RX_B19p	DIFFOUT_B19p	AK26	DQS2B/CQ2B/CQn2B/QKn2B			A_3A_4	CA_3A_4				
3A	VREFB3A0				DIFF0_TX_B20n	DIFFOUT_B20n	AM27	DQ1B			A_3A_3	CA_3A_3				
3A	VREFB3A0				DIFF0_TX_B20p	DIFFOUT_B20p	AP27	DQ2B			A_3A_2	CA_3A_2				
3A	VREFB3A0				DIFF0_RX_B21n	DIFFOUT_B21n	AL26	DQ2B			A_3A_1	CA_3A_1				
3A	VREFB3A0				DIFF0_RX_B21p	DIFFOUT_B21p	AM26	DQ2B			CA_3A_0	CA_3A_0				
3A	VREFB3A0				DIFF0_TX_B22n	DIFFOUT_B22n	AD29	DQ1B			CKE_3A_1	CKE_3A_1				
3A	VREFB3A0				DIFF0_TX_B22p	DIFFOUT_B22p	AE29	DQ2B			CKE_3A_0	CKE_3A_0				
3A	VREFB3A0				DIFF0_RX_B23n	DIFFOUT_B23n	AN26	DQ2B			CKE_3A	CKE_3A				
3A	VREFB3A0				DIFF0_RX_B23p	DIFFOUT_B23p	AP26	DQ2B			CK_3A	CK_3A				
3B	VREFB3B0				DIFF0_TX_B24n	DIFFOUT_B24n	AD26	DQ1B			RESET#_3A					
3B	VREFB3B0				DIFF0_TX_B24p	DIFFOUT_B24p	AE26	DQ2B	DQ1B		DQ1_3B_2	DQ1_3B_2				
3B	VREFB3B0				DIFF0_RX_B25n	DIFFOUT_B25n	AE24	DQ2B	DQ1B		DQ1_3B_7	DQ1_3B_7				
3B	VREFB3B0				DIFF0_RX_B25p	DIFFOUT_B25p	AF24	DQ3B	DQ1B		DQ1_3B_6	DQ1_3B_6				
3B	VREFB3B0				DIFF0_TX_B26n	DIFFOUT_B26n	AB24	DQ1B			DQ1_3B_7	DQ1_3B_7				
3B	VREFB3B0				DIFF0_TX_B26p	DIFFOUT_B26p	AB25	DQ3B	DQ1B		DM1_3B	DM1_3B				



Bank Number	REF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0	
3B	VREFB3N0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	AC24	DQS3B/QK3B			DQ2B	DQ1B					
3B	VREFB3N0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	A524	DQS3B/CQ3B/CQn3B/QKn3B			DQ2B	DQ1B					
3B	VREFB3N0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AH25				DQ2B	DQ1B					
3B	VREFB3N0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AJ25				DQ2B	DQ1B					
3B	VREFB3N0	IO			DIFFIO_RX_B29n	DIFFOUT_B29n	A524				DQ2B	DQ1B					
3B	VREFB3N0	IO		VREFB3N0	DIFFIO_RX_B29p	DIFFOUT_B29p	AH24				DQ2B	DQ1B					
3B	VREFB3N0	IO					AC25										
3B	VREFB3N0	IO					AC23				DQ2B	DQ1B					
3B	VREFB3N0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	AL25				DQ2B	DQ1B					
3B	VREFB3N0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	AL24				DQ2B	DQ1B					
3B	VREFB3N0	IO			DIFFIO_TX_B31p	DIFFOUT_B31p	AJ24				DQ2B	DQ1B					
3B	VREFB3N0	IO			DIFFIO_RX_B32n	DIFFOUT_B32n	AE23				DQ2B	DQ1B					
3B	VREFB3N0	IO			DIFFIO_RX_B32p	DIFFOUT_B32p	AE23				DQ2B	DQ1B					
3B	VREFB3N0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AF23				DQ2B	DQ1B					
3B	VREFB3N0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AD23				DQ2B	DQ1B					
3B	VREFB3N0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AP25	DQS4B/QK4B			DQ2B	DQ1B					
3B	VREFB3N0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AP24	DQS4B/CQ4B/CQn4B/QKn4B			DQ2B	DQ1B					
3B	VREFB3N0	IO			DIFFIO_TX_B35p	DIFFOUT_B35p	AM25				DQ2B	DQ1B					
3B	VREFB3N0	IO			DIFFIO_RX_B36n	DIFFOUT_B36n	AM23				DQ2B	DQ1B					
3B	VREFB3N0	IO			DIFFIO_RX_B36p	DIFFOUT_B36p	AM24				DQ2B	DQ1B					
3B	VREFB3N0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	AB23				DQ2B	DQ1B					
3B	VREFB3N0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AN23				DQ2B	DQ1B					
3B	VREFB3N0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AP23				DQ2B	DQ1B					
3C	VREFB3C0	IO			DIFFIO_RX_B40n	DIFFOUT_B40n	AF25				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B40n	DIFFOUT_B40n	AS23				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B40p	DIFFOUT_B40p	AH23				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AJ22				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AJ23	DQS4B/QK5B			DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	AJ22	DQS4B/CQ5B/CQn5B/QKn5B			DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_TX_B43p	DIFFOUT_B43p	AH22				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B44n	DIFFOUT_B44n	AG21				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B44p	DIFFOUT_B44p	AG21				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	AK21				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AK22				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AK23				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	AL23				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_TX_B47p	DIFFOUT_B47p	AL22				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B48n	DIFFOUT_B48n	AM22				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B48p	DIFFOUT_B48p	AM21				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AB21				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	AE21	DQS4B/QK6B			DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	AE21	DQS4B/CQ6B/CQn6B/QKn6B			DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_TX_B51p	DIFFOUT_B51p	AL20				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B52n	DIFFOUT_B52n	AF20				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B52p	DIFFOUT_B52p	AF20				DQ3B	DQ2B					
3C	VREFB3C0	IO		VREFB3C0			AB22				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B53n	DIFFOUT_B53n	AB20				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B53p	DIFFOUT_B53p	AK21				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_TX_B54p	DIFFOUT_B54p	AH20				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B55n	DIFFOUT_B55n	AJ20				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B55p	DIFFOUT_B55p	AK20				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AC21				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B57n	DIFFOUT_B57n	AP21	DQS7B/QK7B			DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B57p	DIFFOUT_B57p	AP20	DQS7B/CQ7B/CQn7B/QKn7B			DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_TX_B58p	DIFFOUT_B58p	AM20				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	AN20				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	AP19				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_TX_B60p	DIFFOUT_B60p	AC19				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B61n	DIFFOUT_B61n	AC20				DQ3B	DQ2B					
3C	VREFB3C0	IO			DIFFIO_RX_B61p	DIFFOUT_B61p	AD20				DQ3B	DQ2B					
3D	VREFB3D0	IO		VREFB3D0			AD18										
3D	VREFB3D0	IO		CLK4n	DIFFIO_RX_B76n	DIFFOUT_B76n	AH19										
3D	VREFB3D0	IO		CLK4p	DIFFIO_RX_B76p	DIFFOUT_B76p	AJ19										
3D	VREFB3D0	IO		CLK5n	DIFFIO_RX_B78n	DIFFOUT_B78n	AL19										
3D	VREFB3D0	IO		CLK5p	DIFFIO_RX_B78p	DIFFOUT_B78p	AM19										
3D	VREFB3D0	IO		FPLL_BC_CLKOUT1/FPLL_BC_CLKOUT1n	DIFFIO_TX_B79n	DIFFOUT_B79n	AE19										
3D	VREFB3D0	IO		FPLL_BC_CLKOUT0/FPLL_BC_CLKOUT0n/FPLL_BC_FB0	DIFFIO_TX_B79p	DIFFOUT_B79p	AF19										
3D	VREFB3D0	IO		FPLL_BC_CLKOUT2/FPLL_BC_FBn	DIFFIO_RX_B80n	DIFFOUT_B80n	AM18										
3D	VREFB3D0	IO		FPLL_BC_CLKOUT2/FPLL_BC_FBp/FPLL_BC_FB1	DIFFIO_RX_B80p	DIFFOUT_B80p	AN18										
3D	VREFB3D0	IO		CLK6n	DIFFIO_RX_B82n	DIFFOUT_B82n	AJ18										
3D	VREFB3D0	IO		CLK6p	DIFFIO_RX_B82p	DIFFOUT_B82p	AK18										
3D	VREFB3D0	IO		CLK7n	DIFFIO_RX_B84n	DIFFOUT_B84n	AF18										
3D	VREFB3D0	IO		CLK7p	DIFFIO_RX_B84p	DIFFOUT_B84p	AG18										
3E	VREFB3E0	IO		VCCD_FPLL			AA17										
3E	VREFB3E0	IO		VCCA_FPLL			AA18										
3E	VREFB3E0	IO		DM1			AB19										
4D	VREFB4D0	IO			DIFFIO_TX_B99n	DIFFOUT_B99n	AD17				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_TX_B99p	DIFFOUT_B99p	AE17				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_RX_B94n	DIFFOUT_B94n	AE16				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_RX_B94p	DIFFOUT_B94p	AF16				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_TX_B95n	DIFFOUT_B95n	AB18				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_RX_B96n	DIFFOUT_B96n	AC18				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_RX_B96n	DIFFOUT_B96n	AF17	DQS4B/QK9B			DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_RX_B96p	DIFFOUT_B96p	AG17	DQS4B/CQ9B/CQn9B/QKn9B			DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_TX_B97n	DIFFOUT_B97n	AH17				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_TX_B97p	DIFFOUT_B97p	AH16				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_RX_B98n	DIFFOUT_B98n	AJ16				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_RX_B98p	DIFFOUT_B98p	AJ17				DQ4B	DQ3B					
4D	VREFB4D0	IO		VREFB4D0			AB17				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_RX_B99n	DIFFOUT_B99n	AC17				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_RX_B99p	DIFFOUT_B99p	AK17				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_RX_B99p	DIFFOUT_B99p	AL16				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_TX_B100n	DIFFOUT_B100n	AL17				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_TX_B100p	DIFFOUT_B100p	AM17				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_RX_B101n	DIFFOUT_B101n	AP17				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_RX_B101p	DIFFOUT_B101p	AP18				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_TX_B102n	DIFFOUT_B102n	AB16				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_TX_B102p	DIFFOUT_B102p	AC16				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_RX_B103n	DIFFOUT_B103n	AP16	DQS4B/QK9B			DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_RX_B103p	DIFFOUT_B103p	AP15	DQS4B/CQ9B/CQn9B/QKn9B			DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_TX_B104p	DIFFOUT_B104p	AG15				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_TX_B104p	DIFFOUT_B104p	AH15				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_RX_B105n	DIFFOUT_B105n	AK15				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_RX_B105p	DIFFOUT_B105p	AL15				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_TX_B106p	DIFFOUT_B106p	AD15				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_TX_B107n	DIFFOUT_B107n	AE15				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_RX_B107n	DIFFOUT_B107n	AM16				DQ4B	DQ3B					
4D	VREFB4D0	IO			DIFFIO_RX_B107p	DIFFOUT_B107p	AN15										



Bank Number	REF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
4C	VREFB4C0	IO			DIFF0_RX_B114n	DIFFOUT_B114n	AC14	DQ10B	DQ6B	DQ2B	DQ4_4C_1	DQ4_4C_1				
4C	VREFB4C0	IO			DIFF0_RX_B114p	DIFFOUT_B114p	AD14	DQ10B	DQ6B	DQ2B	DQ4_4C_0	DQ4_4C_0				
4C	VREFB4C0	IO			DIFF0_TX_B115p	DIFFOUT_B115p	AF14	DQ11B	DQ7B	DQ3B	DQ4_4C_8	DQ4_4C_8				
4C	VREFB4C0	IO			DIFF0_RX_B116n	DIFFOUT_B116n	AL13	DQ11B	DQ7B	DQ3B	DQ4_4C_7	DQ4_4C_7				
4C	VREFB4C0	IO			DIFF0_RX_B116p	DIFFOUT_B116p	AM13	DQ11B	DQ7B	DQ3B	DQ4_4C_6	DQ4_4C_6				
4C	VREFB4C0	IO			DIFF0_TX_B117p	DIFFOUT_B117p	AB14	DQ11B	DQ7B	DQ3B	DM4_4C	DM4_4C				
4C	VREFB4C0	IO			DIFF0_RX_B118n	DIFFOUT_B118n	AJ12	DQ12B	DQ8B	DQ4B	DQ4_4C_9	DQ4_4C_9				
4C	VREFB4C0	IO			DIFF0_RX_B118p	DIFFOUT_B118p	AK12	DQS11B/CQ11B/CQn11B/OKn11B	DQS11B/CQn11B/OKn11B	DQ2B	DQ2_4C	DQ2_4C				
4C	VREFB4C0	IO			DIFF0_TX_B119n	DIFFOUT_B119n	AG14	DQ11B	DQ7B	DQ3B	DQ4_4C_5	DQ4_4C_5				
4C	VREFB4C0	IO			DIFF0_RX_B120n	DIFFOUT_B120n	AE14	DQ11B	DQ7B	DQ3B	DQ4_4C_4	DQ4_4C_4				
4C	VREFB4C0	IO			DIFF0_TX_B120p	DIFFOUT_B120p	AF13	DQ11B	DQ7B	DQ3B	DQ4_4C_3	DQ4_4C_3				
4C	VREFB4C0	IO			DIFF0_RX_B122n	DIFFOUT_B122n	AE12	DQ11B	DQ7B	DQ3B	DQ4_4C_1	DQ4_4C_1				
4C	VREFB4C0	IO			DIFF0_RX_B122p	DIFFOUT_B122p	AG12	DQ11B	DQ7B	DQ3B	DQ4_4C_0	DQ4_4C_0				
4B	VREFB4B0	IO			DIFF0_TX_B123p	DIFFOUT_B123p	AP13	DQ12B	DQ8B	DQ4B	DQ4_4B_8	DQ4_4B_8				
4B	VREFB4B0	IO			DIFF0_RX_B124n	DIFFOUT_B124n	AN12	DQ12B	DQ8B	DQ4B	DQ4_4B_7	DQ4_4B_7				
4B	VREFB4B0	IO			DIFF0_RX_B124p	DIFFOUT_B124p	AP12	DQ12B	DQ8B	DQ4B	DQ4_4B_6	DQ4_4B_6				
4B	VREFB4B0	IO			DIFF0_TX_B125p	DIFFOUT_B125p	AE12	DQ12B	DQ8B	DQ4B	DM3_4B	DM3_4B				
4B	VREFB4B0	IO			DIFF0_RX_B126n	DIFFOUT_B126n	AM12	DQS12B/CQ12B/OK12B	DQS12B/CQn12B/OKn12B	DQ2B	DQ2_4B	DQ2_4B				
4B	VREFB4B0	IO			DIFF0_RX_B126p	DIFFOUT_B126p	AN11	DQS12B/CQ12B/CQn12B/OKn12B	DQS12B/CQn12B/OKn12B	DQ2B	DQ2_4B	DQ2_4B				
4B	VREFB4B0	IO			DIFF0_TX_B127p	DIFFOUT_B127p	AL11	DQ12B	DQ8B	DQ4B	DQ4_4B_5	DQ4_4B_5				
4B	VREFB4B0	IO			DIFF0_RX_B128n	DIFFOUT_B128n	AD11	DQ12B	DQ8B	DQ4B	DQ4_4B_4	DQ4_4B_4				
4B	VREFB4B0	IO			DIFF0_RX_B128p	DIFFOUT_B128p	AE11	DQ12B	DQ8B	DQ4B	DQ4_4B_3	DQ4_4B_3				
4B	VREFB4B0	IO			DIFF0_TX_B129p	DIFFOUT_B129p	AD12	DQ12B	DQ8B	DQ4B	DQ4_4B_2	DQ4_4B_2				
4B	VREFB4B0	IO			DIFF0_RX_B130n	DIFFOUT_B130n	AL10	DQ12B	DQ8B	DQ4B	DQ4_4B_1	DQ4_4B_1				
4B	VREFB4B0	IO			DIFF0_RX_B130p	DIFFOUT_B130p	AM11	DQ12B	DQ8B	DQ4B	DQ4_4B_0	DQ4_4B_0				
4B	VREFB4B0	IO			DIFF0_TX_B131n	DIFFOUT_B131n	AP11	DQ13B	DQ9B	DQ5B						
4B	VREFB4B0	IO			DIFF0_TX_B131p	DIFFOUT_B131p	AP10	DQ13B	DQ9B	DQ5B	DQ4_4B_8	DQ4_4B_8				
4B	VREFB4B0	IO			DIFF0_RX_B132n	DIFFOUT_B132n	AJ11	DQ13B	DQ9B	DQ5B	DQ4_4B_7	DQ4_4B_7				
4B	VREFB4B0	IO			DIFF0_RX_B132p	DIFFOUT_B132p	AK11	DQ13B	DQ9B	DQ5B	DQ4_4B_6	DQ4_4B_6				
4B	VREFB4B0	IO			DIFF0_TX_B133p	DIFFOUT_B133p	AB12	DQ13B	DQ9B	DQ5B	DM4_4B	DM4_4B				
4B	VREFB4B0	IO			DIFF0_RX_B134n	DIFFOUT_B134n	AL9	DQS13B/CQ13B/OK13B	DQS13B/CQn13B/OKn13B	DQ2B	DQ2_4B	DQ2_4B				
4B	VREFB4B0	IO			DIFF0_RX_B134p	DIFFOUT_B134p	AM10	DQS13B/CQ13B/CQn13B/OKn13B	DQS13B/CQn13B/OKn13B	DQ2B	DQ2_4B	DQ2_4B				
4B	VREFB4B0	IO			DIFF0_TX_B135p	DIFFOUT_B135p	AF11	DQ13B	DQ9B	DQ5B	DQ4_4B_5	DQ4_4B_5				
4B	VREFB4B0	IO			DIFF0_RX_B136n	DIFFOUT_B136n	AG10	DQ13B	DQ9B	DQ5B	DQ4_4B_4	DQ4_4B_4				
4B	VREFB4B0	IO		VREFB4B0	DIFF0_RX_B136p	DIFFOUT_B136p	AG9	DQ13B	DQ9B	DQ5B	DQ4_4B_3	DQ4_4B_3				
4B	VREFB4B0	IO					AA12									
4B	VREFB4B0	IO			DIFF0_RX_B137n	DIFFOUT_B137n	AD9	DQ13B	DQ9B	DQ5B	DQ4_4B_2	DQ4_4B_2				
4B	VREFB4B0	IO			DIFF0_RX_B137p	DIFFOUT_B137p	AE10	DQ13B	DQ9B	DQ5B	DQ4_4B_1	DQ4_4B_1				
4B	VREFB4B0	IO			DIFF0_TX_B138n	DIFFOUT_B138n	AE11	DQ14B	DQ10B	DQ6B	DQ4_4B_0	DQ4_4B_0				
4B	VREFB4B0	IO			DIFF0_TX_B138p	DIFFOUT_B138p	AJ9	DQ14B	DQ10B	DQ6B	DQ4_4B_8	DQ4_4B_8				
4B	VREFB4B0	IO			DIFF0_RX_B139n	DIFFOUT_B139n	AK9	DQ14B	DQ10B	DQ6B	DQ4_4B_7	DQ4_4B_7				
4B	VREFB4B0	IO			DIFF0_TX_B140p	DIFFOUT_B140p	AB10	DQ14B	DQ10B	DQ6B	DQ4_4B_6	DQ4_4B_6				
4B	VREFB4B0	IO			DIFF0_RX_B141n	DIFFOUT_B141n	AH10	DQS14B/OK14B	DQS14B/OKn14B	DQ2B	DM5_4B	DM5_4B				
4B	VREFB4B0	IO			DIFF0_RX_B141p	DIFFOUT_B141p	AH9	DQS14B/CQ14B/CQn14B/OKn14B	DQS14B/CQn14B/OKn14B	DQ2B	DQ5_4B	DQ5_4B				
4B	VREFB4B0	IO			DIFF0_TX_B142p	DIFFOUT_B142p	AE9	DQ14B	DQ10B	DQ6B	DQ4_4B_5	DQ4_4B_5				
4B	VREFB4B0	IO			DIFF0_RX_B143n	DIFFOUT_B143n	AG9	DQ14B	DQ10B	DQ6B	DQ4_4B_4	DQ4_4B_4				
4B	VREFB4B0	IO			DIFF0_RX_B143p	DIFFOUT_B143p	AG8	DQ14B	DQ10B	DQ6B	DQ4_4B_3	DQ4_4B_3				
4B	VREFB4B0	IO			DIFF0_TX_B144p	DIFFOUT_B144p	AC11	DQ14B	DQ10B	DQ6B	DQ4_4B_2	DQ4_4B_2				
4B	VREFB4B0	IO			DIFF0_RX_B145n	DIFFOUT_B145n	AB10	DQ14B	DQ10B	DQ6B	DQ4_4B_1	DQ4_4B_1				
4B	VREFB4B0	IO			DIFF0_RX_B145p	DIFFOUT_B145p	AC10	DQ14B	DQ10B	DQ6B	DQ4_4B_0	DQ4_4B_0				
4A	VREFB4A0	IO			DATA10	DIFF0_TX_B146p	DIFFOUT_B146p	AP2	DQ15B	DQ11B						
4A	VREFB4A0	IO			DATA11	DIFF0_RX_B147n	DIFFOUT_B147n	AN8	DQ15B	DQ11B						
4A	VREFB4A0	IO			DATA12	DIFF0_RX_B147p	DIFFOUT_B147p	AN9	DQ15B	DQ11B						
4A	VREFB4A0	IO			DATA16	DIFF0_TX_B148p	DIFFOUT_B148p	AF8	DQ15B	DQ11B						
4A	VREFB4A0	IO			DATA19	DIFF0_RX_B149n	DIFFOUT_B149n	AL8	DQS15B/OK15B	DQS15B/OKn15B						
4A	VREFB4A0	IO			DATA13	DIFF0_RX_B149p	DIFFOUT_B149p	AM6	DQS15B/CQ15B/CQn15B/OKn15B	DQS15B/CQn15B/OKn15B						
4A	VREFB4A0	IO			DATA7	DIFF0_TX_B150n	DIFFOUT_B150n	AP8	DQ15B	DQ11B						
4A	VREFB4A0	IO			DATA8	DIFF0_TX_B150p	DIFFOUT_B150p	AP7	DQ15B	DQ11B						
4A	VREFB4A0	IO			DATA14	DIFF0_RX_B151n	DIFFOUT_B151n	AN6	DQ15B	DQ11B						
4A	VREFB4A0	IO			DATA15	DIFF0_RX_B151p	DIFFOUT_B151p	AP6	DQ15B	DQ11B						
4A	VREFB4A0	IO			DATA9	DIFF0_TX_B152n	DIFFOUT_B152n	AE7	DQ15B	DQ11B						
4A	VREFB4A0	IO			CLKUSR	DIFF0_TX_B152p	DIFFOUT_B152p	AF7	DQ15B	DQ11B						
4A	VREFB4A0	IO				DIFF0_RX_B153n	DIFFOUT_B153n	AL7	DQ15B	DQ11B						
4A	VREFB4A0	IO				DIFF0_RX_B153p	DIFFOUT_B153p	AM7	DQ15B	DQ11B						
4A	VREFB4A0	IO			PR_ERROR	DIFF0_TX_B154n	DIFFOUT_B154n	AJ8								
4A	VREFB4A0	IO			PR_READY	DIFF0_TX_B154p	DIFFOUT_B154p	AK8	DQ16B							
4A	VREFB4A0	IO			PR_DONE	DIFF0_RX_B155n	DIFFOUT_B155n	AN8								
4A	VREFB4A0	IO			PR_REQUEST	DIFF0_RX_B155p	DIFFOUT_B155p	AP5	DQ16B							
4A	VREFB4A0	IO			PERSTR0	DIFF0_TX_B156n	DIFFOUT_B156n	AD6								
4A	VREFB4A0	IO			PERSTR1	DIFF0_TX_B156p	DIFFOUT_B156p	AE6	DQ16B							
4A	VREFB4A0	IO			CP_CONF_DONE	DIFF0_RX_B157n	DIFFOUT_B157n	AF4	DQS16B/OK16B							
4A	VREFB4A0	IO			CRC_ERROR	DIFF0_RX_B157p	DIFFOUT_B157p	AP3	DQS16B/CQ16B/CQn16B/OKn16B							
4A	VREFB4A0	IO			DEV_OK	DIFF0_TX_B158n	DIFFOUT_B158n	AM6								
4A	VREFB4A0	IO			DEV_OKn	DIFF0_TX_B158p	DIFFOUT_B158p	AM5	DQ16B							
4A	VREFB4A0	IO			INT_DONE	DIFF0_RX_B159n	DIFFOUT_B159n	AK6	DQ16B							
4A	VREFB4A0	IO		VREFB4A0	DIFF0_RX_B159p	DIFFOUT_B159p	AL6	DQ16B								
4A	VREFB4A0	IO					AK7									
4A	VREFB4A0	IO					AD8	DQ16B								
4A	VREFB4A0	IO			CLK10n	DIFF0_RX_B160n	DIFFOUT_B160n	AH7	DQ16B							
4A	VREFB4A0	IO			CLK10p	DIFF0_RX_B160p	DIFFOUT_B160p	AJ7	DQ16B							
4A	VREFB4A0	IO			FPLL_BR_CLKOUT1_FPLL_BR_CLKOUTn	DIFF0_TX_B161n	DIFFOUT_B161n	AG8								
4A	VREFB4A0	IO			FPLL_BR_CLKOUT1_FPLL_BR_CLKOUTp	DIFF0_TX_B161p	DIFFOUT_B161p	AH8								
4A	VREFB4A0	IO			FPLL_BR_CLKOUT2_FPLL_BR_Fb	DIFF0_RX_B162n	DIFFOUT_B162n	AN3								
4A	VREFB4A0	IO			FPLL_BR_CLKOUT2_FPLL_BR_Fb	DIFF0_RX_B162p	DIFFOUT_B162p	AP2								
4A	VREFB4A0	IO			CLK10n	DIFF0_RX_B164n	DIFFOUT_B164n	AM4								
4A	VREFB4A0	IO			CLK10p	DIFF0_RX_B164p	DIFFOUT_B164p	AM5								
4A	VREFB4A0	IO			CLK9n	DIFF0_RX_B166n	DIFFOUT_B166n	AL4								
4A	VREFB4A0	IO			CLK9p	DIFF0_RX_B166p	DIFFOUT_B166p	AL5								
4A	VREFB4A0	IO			RZQ_1	DIFF0_TX_B167n	DIFFOUT_B167n	AF5								
4A	VREFB4A0	IO			RZQ_1	DIFF0_TX_B167p	DIFFOUT_B167p	AG5								
4A	VREFB4A0	IO			CLK8n	DIFF0_RX_B168n	DIFFOUT_B168n	AH6								
4A	VREFB4A0	IO			CLK8p	DIFF0_RX_B168p	DIFFOUT_B168p	AJ6								
				RREF_BR			AM1									
				DN1			AM2									
				DN2			AN6									
				REFCLK0p			AN8									
				REFCLK0n			AA7									
				GXB_RX_R0n			AK2									



Bank Number	REF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
GXB_R0		GXB_RX_R56:GXB_REFCLK_R56					Y1									
GXB_R0		GXB_TX_R56					W3									
GXB_R0		GXB_TX_R56					W4									
GXB_R0		REFCLK1R0					W6									
GXB_R0		REFCLK1R0					W7									
6B	VREFB6N0	HPS_DDR					T7				HPS_DM_4	HPS_DM_4				
6B	VREFB6N0	HPS_DDR					T8				HPS_DO_28	HPS_DO_28				
6B	VREFB6N0	HPS_DDR					U2				HPS_DO_37	HPS_DO_37				
6B	VREFB6N0	HPS_DDR					V1				HPS_DO_38	HPS_DO_38				
6B	VREFB6N0	HPS_DDR					U3				HPS_DO_36	HPS_DO_36				
6B	VREFB6N0	HPS_DDR					T3				HPS_DQS_4	HPS_DQS_4				
6B	VREFB6N0	HPS_GPI3					T1									
6B	VREFB6N0	HPS_DDR					T4				HPS_DQS#_4	HPS_DQS#_4				
6B	VREFB6N0	HPS_DDR					U1				HPS_DO_35	HPS_DO_35				
6B	VREFB6N0	HPS_DDR					R1				HPS_DO_33	HPS_DO_33				
6B	VREFB6N0	HPS_DDR					T6				HPS_DO_34	HPS_DO_34				
6B	VREFB6N0	HPS_DDR					R2				HPS_DO_32	HPS_DO_32				
6B	VREFB6N0	HPS_GPI2					T6									
6B	VREFB6N0	HPS_GPI1					P1									
6B	VREFB6N0	HPS_DDR					P2				HPS_DM_3	HPS_DM_3				
6B	VREFB6N0	HPS_GPI0					N1									
6B	VREFB6N0	HPS_DDR					R3				HPS_DO_31	HPS_DO_31				
6B	VREFB6N0	HPS_DDR					N4				HPS_DO_29	HPS_DO_29				
6B	VREFB6N0	HPS_DDR					P7				HPS_DO_30	HPS_DO_30				
6B	VREFB6N0	HPS_DDR					P4				HPS_DO_28	HPS_DO_28				
6B	VREFB6N0	VREFB6N0_HPS					R7									
6B	VREFB6N0	HPS_DDR					L1				HPS_DQS_3	HPS_DQS_3				
6B	VREFB6N0	HPS_GPI3					M3									
6B	VREFB6N0	HPS_DDR					M2				HPS_DQS#_3	HPS_DQS#_3				
6B	VREFB6N0	HPS_DDR					N3				HPS_DO_27	HPS_DO_27				
6B	VREFB6N0	HPS_DDR					K1				HPS_DO_25	HPS_DO_25				
6B	VREFB6N0	HPS_DDR					R4				HPS_DO_26	HPS_DO_26				
6B	VREFB6N0	HPS_DDR					L2				HPS_DO_24	HPS_DO_24				
6B	VREFB6N0	HPS_GPI3					P5									
6B	VREFB6N0	HPS_GPI2					H2									
6B	VREFB6N0	HPS_DDR					H1				HPS_DM_2	HPS_DM_2				
6B	VREFB6N0	HPS_GPI0					J2									
6B	VREFB6N0	HPS_DDR					J1				HPS_DO_23	HPS_DO_23				
6B	VREFB6N0	HPS_DDR					J3				HPS_DO_21	HPS_DO_21				
6B	VREFB6N0	HPS_DDR					N5				HPS_DO_22	HPS_DO_22				
6B	VREFB6N0	HPS_DDR					K3				HPS_DO_20	HPS_DO_20				
6B	VREFB6N0	HPS_GPI5					P6									
6B	VREFB6N0	HPS_DDR					K4				HPS_DQS_2	HPS_DQS_2				
6B	VREFB6N0	HPS_DDR					L3				HPS_DQS#_2	HPS_DQS#_2				
6B	VREFB6N0	HPS_DDR					L5				HPS_DQS#_2	HPS_DQS#_2				
6B	VREFB6N0	HPS_DDR					M4				HPS_DO_19	HPS_DO_19				
6B	VREFB6N0	HPS_DDR					L6				HPS_DO_17	HPS_DO_17				
6B	VREFB6N0	HPS_DDR					N6				HPS_DO_18	HPS_DO_18				
6B	VREFB6N0	HPS_DDR					M6				HPS_DO_16	HPS_DO_16				
6A	VREFBA0N0	HPS_GPI4					N7									
6A	VREFBA0N0	HPS_GPI3					G3									
6A	VREFBA0N0	HPS_DDR					F1				HPS_DM_1	HPS_DM_1				
6A	VREFBA0N0	HPS_GPI2					H3									
6A	VREFBA0N0	HPS_DDR					G1				HPS_DO_15	HPS_DO_15				
6A	VREFBA0N0	HPS_DDR					H4				HPS_DO_13	HPS_DO_13				
6A	VREFBA0N0	HPS_DDR					K5				HPS_DO_14	HPS_DO_14				
6A	VREFBA0N0	HPS_DDR					J4				HPS_DO_12	HPS_DO_12				
6A	VREFBA0N0	HPS_DDR					K6				HPS_CKE_0	HPS_CKE_0				
6A	VREFBA0N0	HPS_DDR					D1				HPS_DQS_1	HPS_DQS_1				
6A	VREFBA0N0	HPS_DDR					E1				HPS_CKE_1	HPS_CKE_1				
6A	VREFBA0N0	HPS_DDR					C1				HPS_DQS#_1	HPS_DQS#_1				
6A	VREFBA0N0	HPS_DDR					E2				HPS_DO_11	HPS_DO_11				
6A	VREFBA0N0	HPS_DDR					F3				HPS_DO_9	HPS_DO_9				
6A	VREFBA0N0	HPS_DDR					J6				HPS_DO_10	HPS_DO_10				
6A	VREFBA0N0	HPS_GPI1					F4				HPS_DO_8	HPS_DO_8				
6A	VREFBA0N0	HPS_GPI0					J7									
6A	VREFBA0N0	HPS_DDR					C2									
6A	VREFBA0N0	HPS_DDR					G4				HPS_DM_0	HPS_DM_0				
6A	VREFBA0N0	HPS_DDR					G6				HPS_DO_7	HPS_DO_7				
6A	VREFBA0N0	HPS_DDR					A2				HPS_DO_5	HPS_DO_5				
6A	VREFBA0N0	HPS_DDR					K7				HPS_DO_6	HPS_DO_6				
6A	VREFBA0N0	HPS_DDR					B1				HPS_DO_4	HPS_DO_4				
6A	VREFBA0N0	HPS_DDR					L7				HPS_ODT_1	HPS_ODT_1				
6A	VREFBA0N0	HPS_DDR					C3				HPS_DQS_0	HPS_DQS_0				
6A	VREFBA0N0	HPS_DDR					E3				HPS_ODT_0	HPS_ODT_0				
6A	VREFBA0N0	HPS_DDR					D4				HPS_DQS#_0	HPS_DQS#_0				
6A	VREFBA0N0	HPS_DDR					E4				HPS_DO_3	HPS_DO_3				
6A	VREFBA0N0	HPS_DDR					A4				HPS_DO_1	HPS_DO_1				
6A	VREFBA0N0	HPS_DDR					M8				HPS_DO_2	HPS_DO_2				
6A	VREFBA0N0	HPS_DDR					A3				HPS_DO_0	HPS_DO_0				
6A	VREFBA0N0	VREFBA0N0_HPS					N9									
6A	VREFBA0N0	HPS_DDR					B4				HPS_A_0	HPS_CA_0				
6A	VREFBA0N0	HPS_DDR					C4				HPS_A_1	HPS_CA_1				
6A	VREFBA0N0	HPS_DDR					D5				HPS_A_4	HPS_CA_4				
6A	VREFBA0N0	HPS_DDR					J8				HPS_A_2	HPS_CA_2				
6A	VREFBA0N0	HPS_DDR					E5				HPS_A_5	HPS_CA_5				
6A	VREFBA0N0	HPS_DDR					K8				HPS_A_3	HPS_CA_3				
6A	VREFBA0N0	HPS_DDR					A6				HPS_CK#	HPS_CK#				
6A	VREFBA0N0	HPS_DDR					B5				HPS_A_6	HPS_CA_6				
6A	VREFBA0N0	HPS_DDR					B7				HPS_CK#	HPS_CK#				
6A	VREFBA0N0	HPS_DDR					B6				HPS_A_7	HPS_CA_7				
6A	VREFBA0N0	HPS_DDR					C7				HPS_BA_1	HPS_BA_1				
6A	VREFBA0N0	HPS_DDR					G7				HPS_BA_0	HPS_BA_0				
6A	VREFBA0N0	HPS_DDR					D6				HPS_BA_3	HPS_BA_3				
6A	VREFBA0N0	HPS_DDR					G6				HPS_CAS#	HPS_CAS#				
6A	VREFBA0N0	HPS_DDR					H6				HPS_RAS#	HPS_RAS#				
6A	VREFBA0N0	HPS_DDR					F5				HPS_A_9	HPS_CA_9				
6A	VREFBA0N0	HPS_DDR					G8				HPS_A_10	HPS_CA_10				
6A	VREFBA0N0	HPS_DDR					F7				HPS_A_8	HPS_CA_8				
6A	VREFBA0N0	HPS_DDR					G9				HPS_A_11	HPS_CA_11				
6A	VREFBA0N0	HPS_DDR					C8				HPS_CSA_0	HPS_CSA_0				
6A	VREFBA0N0	HPS_DDR					E7				HPS_A_12	HPS_CA_12				
6A	VREFBA0N0	HPS_DDR					D7				HPS_CSA_1	HPS_CSA_1				
6A	VREFBA0N0	HPS_DDR					F9				HPS_A_13	HPS_CA_13				
6A	VREFBA0N0	HPS_DDR					A8				HPS_A_14	HPS_CA_14				
6A	VREFBA0N0	HPS_DDR					J9				HPS_WIE#	HPS_WIE#				
6A	VREFBA0N0	HPS_DDR					A7				HPS_A_15	HPS_CA_15				
6A	VREFBA0N0	HPS_DDR					K9									
6A	VREFBA0N0	DNU					J4									
6A	VREFBA0N0	GND					G10									
6A	VREFBA0N0	GND					H10									
7A		HPS_ARST					P11									
7A		HPS_APC#					E9									
7A		HPS_TDI					P10									
7A		VCCRCSTCLK_HPS					E9									
7A		HPS_TMS					A8									
7A		HPS_TCK					C9									
7A		HPS_TRST					B10									
7A		HPS_TDI					D9									
7A		GND					N10									



Bank Number	REF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
7A		HPS_PORSEL					C10									
7A		HPS_CLKI					L9									
7A		HPS_CLKO					D10									
7A	VREFB7A/B7C/D7END	TRACE_CLK					A10						TRACE_CLK			HPS GPIO48
7A	VREFB7A/B7C/D7END	TRACE_D0					K10						TRACE_D0	SPIS0_CLK	UART0_RX	HPS GPIO49
7A	VREFB7A/B7C/D7END	TRACE_D1					A11						TRACE_D1	SPIS0_MOSI	UART0_TX	HPS GPIO50
7A	VREFB7A/B7C/D7END	TRACE_D2					I10						TRACE_D2	SPIS0_MISO	IC21_SDA	HPS GPIO51
7A	VREFB7A/B7C/D7END	TRACE_D3					A13						TRACE_D3	SPIS0_SSD	IC21_SCL	HPS GPIO52
7A	VREFB7A/B7C/D7END	TRACE_D4					B12						TRACE_D4	SPIS1_CLK		HPS GPIO53
7A	VREFB7A/B7C/D7END	TRACE_D5					A12						TRACE_D5	SPIS0_MOSI		HPS GPIO54
7A	VREFB7A/B7C/D7END	TRACE_D6					C13						TRACE_D6	SPIS1_SSD	IC20_SDA	HPS GPIO55
7A	VREFB7A/B7C/D7END	TRACE_D7					C11						TRACE_D7	SPIS1_MISO	IC20_SCL	HPS GPIO56
7A	VREFB7A/B7C/D7END	SPIM0_CLK					L10						SPIM0_CLK	IC21_SDA	UART0_CTS	HPS GPIO57
7A	VREFB7A/B7C/D7END	SPIM0_MOSI					C12						SPIM0_MOSI	IC21_SCL	UART0_RTS	HPS GPIO58
7A	VREFB7A/B7C/D7END	SPIM0_MISO					L11						SPIM0_MISO		UART1_CTS	HPS GPIO59
7A	VREFB7A/B7C/D7END	SPIM0_SS0/BOOTSEL0					E10						SPIM0_SS0		UART1_RTS	HPS GPIO60
7A	VREFB7A/B7C/D7END	UART0_RX					E11						UART0_RX	SPIM0_SS1		HPS GPIO61
7A	VREFB7A/B7C/D7END	UART0_TX_CLKSEL1					F10						UART0_TX	SPIM1_SS1		HPS GPIO62
7A	VREFB7A/B7C/D7END	IC20_SDA					F11						IC20_SDA	UART1_RX	SPIM1_CLK	HPS GPIO63
7A	VREFB7A/B7C/D7END	IC20_SCL					H11						IC20_SCL	UART1_TX	SPIM1_MOSI	HPS GPIO64
7A	VREFB7A/B7C/D7END	UART0_RX*					M10						UART0_RX		SPIM1_MISO	HPS GPIO65
7A	VREFB7A/B7C/D7END	UART0_TX_CLKSEL0					J11						UART0_TX	SPIM1_SS0		HPS GPIO66
7A	VREFB7A/B7C/D7END	SPIS1_CLK					M11						SPIS1_CLK	SPIM1_CLK		HPS GPIO67
7A	VREFB7A/B7C/D7END	SPIS1_MOSI					D12						SPIS1_MOSI	SPIM1_MOSI		HPS GPIO68
7A	VREFB7A/B7C/D7END	SPIS1_MISO					E12						SPIS1_MISO	SPIM1_MISO		HPS GPIO69
7A	VREFB7A/B7C/D7END	SPIS1_SSD					D13						SPIS1_SSD	SPIS1_SSD		HPS GPIO70
7A	VREFB7A/B7C/D7END	UART1_RX					F12						UART1_RX	SPIM1_SS1		HPS GPIO72
7A	VREFB7A/B7C/D7END	UART1_TX					J12						UART1_TX	SPIM0_CLK		HPS GPIO73
7A	VREFB7A/B7C/D7END	IC21_SDA					I12						IC21_SDA	SPIM0_MOSI		HPS GPIO74
7A	VREFB7A/B7C/D7END	IC21_SCL					K12						IC21_SCL	SPIM0_MISO		HPS GPIO75
7A	VREFB7A/B7C/D7END	SPIM0_SS0					M12						SPIM0_SS0			HPS GPIO76
7A	VREFB7A/B7C/D7END	SPIS0_CLK					F13						SPIS0_CLK	SPIM0_SS1		HPS GPIO78
7A	VREFB7A/B7C/D7END	SPIS0_MOSI					G12						SPIS0_MOSI			HPS GPIO79
7A	VREFB7A/B7C/D7END	SPIS0_MISO					G13						SPIS0_MISO			HPS GPIO80
7A	VREFB7A/B7C/D7END	SPIS0_SSD					H12						SPIS0_SSD			HPS GPIO81
7B	VREFB7A/B7C/D7END	NAND_ALE					A14						NAND_ALE	RGMIH_TX_CLK	QSPI_SS3	HPS GPIO14
7B	VREFB7A/B7C/D7END	NAND_CE					M13						NAND_CE	RGMIH_TXD0	USB1_D0	HPS GPIO15
7B	VREFB7A/B7C/D7END	NAND_CLE					B14						NAND_CLE	RGMIH_TXD1	USB1_D1	HPS GPIO16
7B	VREFB7A/B7C/D7END	NAND_BE					N13						NAND_BE	RGMIH_TXD2	USB1_D2	HPS GPIO17
7B	VREFB7A/B7C/D7END	NAND_RB					B15						NAND_RB	RGMIH_TXD3	USB1_D3	HPS GPIO18
7B	VREFB7A/B7C/D7END	NAND_DQ0					C14						NAND_DQ0	RGMIH_RXD0		HPS GPIO19
7B	VREFB7A/B7C/D7END	NAND_DQ1					C15						NAND_DQ1	RGMIH_MDIO	IC23_SDA	HPS GPIO20
7B	VREFB7A/B7C/D7END	NAND_DQ2					D14						NAND_DQ2	RGMIH_MDC	IC23_SCL	HPS GPIO21
7B	VREFB7A/B7C/D7END	NAND_DQ3					O14						NAND_DQ3	RGMIH_RX_CTL	USB1_D4	HPS GPIO22
7B	VREFB7A/B7C/D7END	NAND_DQ4					N12						NAND_DQ4	RGMIH_TX_CTL	USB1_D5	HPS GPIO23
7B	VREFB7A/B7C/D7END	NAND_DQ5					H14						NAND_DQ5	RGMIH_RX_CLK	USB1_D6	HPS GPIO24
7B	VREFB7A/B7C/D7END	NAND_DQ6					P12						NAND_DQ6	RGMIH_RXD1	USB1_D7	HPS GPIO25
7B	VREFB7A/B7C/D7END	NAND_DQ7					K13						NAND_DQ7	RGMIH_RXD2		HPS GPIO26
7B	VREFB7A/B7C/D7END	NAND_WP					J14						NAND_WP	RGMIH_RXD3	QSPI_SS2	HPS GPIO27
7B	VREFB7A/B7C/D7END	NAND_WE/BOOTSEL2					L14						NAND_WE	QSPI_SS1		HPS GPIO28
7B	VREFB7A/B7C/D7END	QSPI_I00					K14						QSPI_I00	USB1_CLK		HPS GPIO29
7B	VREFB7A/B7C/D7END	QSPI_I01					M14						QSPI_I01	USB1_STP		HPS GPIO30
7B	VREFB7A/B7C/D7END	QSPI_I02					P14						QSPI_I02	USB1_DRP		HPS GPIO31
7B	VREFB7A/B7C/D7END	QSPI_I03					N14						QSPI_I03	USB1_NXT		HPS GPIO32
7B	VREFB7A/B7C/D7END	QSPI_SS0/BOOTSEL1					R15						QSPI_SS0			HPS GPIO33
7B	VREFB7A/B7C/D7END	QSPI_CLK					F14						QSPI_CLK			HPS GPIO34
7B	VREFB7A/B7C/D7END	QSPI_SS1					D15						QSPI_SS1			HPS GPIO35
7C	VREFB7A/B7C/D7END	SDMMC_CMD					E15						SDMMC_CMD	USB0_D0		HPS GPIO36
7C	VREFB7A/B7C/D7END	SDMMC_PWREN					J15						SDMMC_PWREN	USB0_D1		HPS GPIO37
7C	VREFB7A/B7C/D7END	SDMMC_D0					C16						SDMMC_D0	USB0_D2		HPS GPIO38
7C	VREFB7A/B7C/D7END	SDMMC_D1					K15						SDMMC_D1	USB0_D3		HPS GPIO39
7C	VREFB7A/B7C/D7END	SDMMC_D4					E16						SDMMC_D4	USB0_D4		HPS GPIO40
7C	VREFB7A/B7C/D7END	SDMMC_D5					G15						SDMMC_D5	USB0_D5		HPS GPIO41
7C	VREFB7A/B7C/D7END	SDMMC_D6					F16						SDMMC_D6	USB0_D6		HPS GPIO42
7C	VREFB7A/B7C/D7END	SDMMC_D7					G16						SDMMC_D7	USB0_D7		HPS GPIO43
7C	VREFB7A/B7C/D7END	HPS_GPIO44					H16						SDMMC_CLK	USB0_CLK		HPS GPIO44
7C	VREFB7A/B7C/D7END	SDMMC_CCLK_OUT					M15						SDMMC_CCLK_OUT	USB0_STP		HPS GPIO45
7C	VREFB7A/B7C/D7END	SDMMC_D2					L16						SDMMC_D2	USB0_DIR		HPS GPIO46
7C	VREFB7A/B7C/D7END	SDMMC_D3					H16						SDMMC_D3	USB0_NXT		HPS GPIO47
7D	VREFB7A/B7C/D7END	RGMIH_TX_CLK					A16						RGMIH_TX_CLK			HPS GPIO0
7D	VREFB7A/B7C/D7END	RGMIH_TXD0					A17						RGMIH_TXD0	USB1_D0		HPS GPIO1
7D	VREFB7A/B7C/D7END	RGMIH_TXD1					A15						RGMIH_TXD1	USB1_D1		HPS GPIO2
7D	VREFB7A/B7C/D7END	RGMIH_TXD2					B17						RGMIH_TXD2	USB1_D2		HPS GPIO3
7D	VREFB7A/B7C/D7END	RGMIH_TXD3					C16						RGMIH_TXD3	USB1_D3		HPS GPIO4
7D	VREFB7A/B7C/D7END	RGMIH_RXD0					L16						RGMIH_RXD0	USB1_D4		HPS GPIO5
7D	VREFB7A/B7C/D7END	RGMIH_MDIO					C17						RGMIH_MDIO	IC22_SDA		HPS GPIO6
7D	VREFB7A/B7C/D7END	RGMIH_MDC					M16						RGMIH_MDC	IC22_SCL		HPS GPIO7
7D	VREFB7A/B7C/D7END	RGMIH_RX_CTL					D17						RGMIH_RX_CTL	USB1_D7		HPS GPIO8
7D	VREFB7A/B7C/D7END	RGMIH_TX_CTL					E18						RGMIH_TX_CTL			HPS GPIO9
7D	VREFB7A/B7C/D7END	RGMIH_RX_CLK					D16						RGMIH_RX_CLK	USB1_CLK		HPS GPIO10
7D	VREFB7A/B7C/D7END	RGMIH_RXD1					F18						RGMIH_RXD1	USB1_STP		HPS GPIO11
7D	VREFB7A/B7C/D7END	RGMIH_RXD2					F17						RGMIH_RXD2	USB1_DRP		HPS GPIO12
7D	VREFB7A/B7C/D7END	RGMIH_RXD3					P16						RGMIH_RXD3	USB1_NXT		HPS GPIO13
7D	VREFB7A/B7C/D7END	RGMIH_TX_CLK					G17						RGMIH_TX_CLK			HPS GPIO48
7D	VREFB7A/B7C/D7END	RGMIH_TXD0					N16						RGMIH_TXD0			HPS GPIO49
7D	VREFB7A/B7C/D7END	RGMIH_TXD1					J17						RGMIH_TXD1			HPS GPIO50
7D	VREFB7A/B7C/D7END	RGMIH_TX_CTL					G18						RGMIH_TX_CTL			HPS GPIO51
7D	VREFB7A/B7C/D7END	RGMIH_RXD0					H17						RGMIH_RXD0			HPS GPIO52
7D	VREFB7A/B7C/D7END	RGMIH_RXD1					H17						RGMIH_RXD1			HPS GPIO53
7E	VREFB7A/B7C/D7END	RGMIH_MDIO					L17						RGMIH_MDIO	SPIM0_CLK	SPIS0_CLK	HPS GPIO54
7E	VREFB7A/B7C/D7END	RGMIH_MDC					N18						RGMIH_MDC	SPIM0_MOSI	SPIS0_MOSI	HPS GPIO55
7E	VREFB7A/B7C/D7END	RGMIH_TXD2					M17						RGMIH_TXD2	SPIM0_MISO	SPIS0_MISO	HPS GPIO56
7E	VREFB7A/B7C/D7END	RGMIH_TXD3					N18						RGMIH_TXD3	SPIM0_SSD	SPIS0_SSD	HPS GPIO57
7E	VREFB7A/B7C/D7END	RGMIH_RX_CLK					M18						RGMIH_RX_CLK	SPIS1_CLK	SPIM1_CLK	HPS GPIO58
7E	VREFB7A/B7C/D7END	RGMIH_RX_CTL					J18						RGMIH_RX_CTL	SPIS1_MOSI	SPIM1_MOSI	HPS GPIO59
7E	VREFB7A/B7C/D7END	RGMIH_RXD2					N17						RGMIH_RXD2	SPIS1_MISO	SPIM1_MISO	HPS GPIO60
7E	VREFB7A/B7C/D7END	RGMIH_RXD3					I18						RGMIH_RXD3	SPIS1_SSD	SPIM1_SSD	HPS GPIO61
		VCC0_PPLL					T17									
		VCC0_PPLL					T16									
8D	VREFB8D0	IO	CLK19b					DIFF0_RX_T31p	DIFFOUT_T31p							
8D	VREFB8D0	IO	CLK19a					DIFF0_RX_T31n	DIFFOUT_T31n							
8D	VREFB8D0	IO	CLK18b					DIFF0_RX_T33p	DIFFOUT_T33p							
8D	VREFB8D0	IO	CLK18a					DIFF0_RX_T33n	DIFFOUT_T33n							
8D	VREFB8D0	IO						DIFF0_RX_T35p	DIFFOUT_T35p							
8D	VREFB8D0	IO	FPLL_TC_CLKOUT2/FPLL_TC_F0p/FPLL_TC_FB1					DIFF0_RX_T35p	DIFFOUT_T35p							
8D	VREFB8D0	IO						FPLL_TC_CLKOUT3/FPLL_TC_FBn								
8D	VREFB8D0	IO						FPLL_TC_CLKOUT1/FPLL_TC_CLKOUT0/FPLL_TC_FB0								
8D	VREFB8D0	IO	CLK17p					DIFF0_RX_T37p	DIFFOUT_T37p							
8D	VREFB8D0	IO	CLK17n					DIFF0_RX_T37n	DIFFOUT_T37n					</		



Bank Number	REF	PinName/Function (2, 3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 (4)	QDS for X8/X9	QDS for X16/X18	QDS for X32/X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2 (6)	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
BC	VREFBNC0	IO			DIFFIO_RX_T58b	DIFFOUT_T58b	B21	DQS1TCQ1TCQn1TQKx1T			DQS5_8C	DQS5_8C				
BC	VREFBNC0	IO			DIFFIO_RX_T58b	DIFFOUT_T58b	C21	DQS4TQK1T			DQS4_8C	DQS4_8C				
BC	VREFBNC0	IO			DIFFIO_RX_T59b	DIFFOUT_T59b	M20	DO1T			DM5_8C	DM5_8C				
BC	VREFBNC0	IO			DIFFIO_RX_T60b	DIFFOUT_T60b	H41	DO1T			DO4_8C_6	DO4_8C_6				
BC	VREFBNC0	IO			DIFFIO_RX_T60b	DIFFOUT_T60b	J20	DO1T			DO5_8C_7	DO5_8C_7				
BC	VREFBNC0	IO			DIFFIO_TX_T61a	DIFFOUT_T61a	E21	DO1T			DO5_8C_8	DO5_8C_8				
BC	VREFBNC0	IO			DIFFIO_RX_T62a	DIFFOUT_T62a	J21	DO2T	DO1T		DO4_8C_0	DO4_8C_0				
BC	VREFBNC0	IO			DIFFIO_RX_T62a	DIFFOUT_T62a	K21	DO2T	DO1T		DO4_8C_1	DO4_8C_1				
BC	VREFBNC0	IO					N21	DO2T	DO1T		DO4_8C_2	DO4_8C_2				
BC	VREFBNC0	IO		VREFBNC0			F21									
BC	VREFBNC0	IO			DIFFIO_RX_T63b	DIFFOUT_T63b	M21	DO2T	DO1T		DO4_8C_3	DO4_8C_3				
BC	VREFBNC0	IO			DIFFIO_RX_T63b	DIFFOUT_T63b	M20	DO2T	DO1T		DO4_8C_4	DO4_8C_4				
BC	VREFBNC0	IO			DIFFIO_TX_T64b	DIFFOUT_T64b	F21	DO2T	DO1T		DO4_8C_5	DO4_8C_5				
BC	VREFBNC0	IO			DIFFIO_RX_T65b	DIFFOUT_T65b	D22	DQS2TCQ2TCQn2TQKx2T	DQS1TCQ1TCQn1TQKx1T		DO54_8C	DO54_8C				
BC	VREFBNC0	IO			DIFFIO_RX_T65b	DIFFOUT_T65b	E22	DO54TQK2T	DO54TQK1T		DO544_8C	DO544_8C				
BC	VREFBNC0	IO			DIFFIO_TX_T66b	DIFFOUT_T66b	N22	DO2T	DO1T		DO4_8C	DO4_8C				
BC	VREFBNC0	IO			DIFFIO_RX_T67b	DIFFOUT_T67b	A24	DO2T	DO1T		DO4_8C_6	DO4_8C_6				
BC	VREFBNC0	IO			DIFFIO_RX_T67b	DIFFOUT_T67b	A23	DO2T	DO1T		DO4_8C_7	DO4_8C_7				
BC	VREFBNC0	IO			DIFFIO_TX_T68b	DIFFOUT_T68b	F23	DO2T	DO1T		DO4_8C_8	DO4_8C_8				
BC	VREFBNC0	IO			DIFFIO_TX_T68b	DIFFOUT_T68b	F23									
BC	VREFBNC0	IO			DIFFIO_RX_T69b	DIFFOUT_T69b	G23	DO3T	DO1T		DO3_8C_0	DO3_8C_0				
BC	VREFBNC0	IO			DIFFIO_RX_T69b	DIFFOUT_T69b	H23	DO3T	DO1T		DO3_8C_1	DO3_8C_1				
BC	VREFBNC0	IO			DIFFIO_TX_T70b	DIFFOUT_T70b	F24	DO3T	DO1T		DO3_8C_2	DO3_8C_2				
BC	VREFBNC0	IO			DIFFIO_RX_T71b	DIFFOUT_T71b	G22	DO3T	DO1T		DO3_8C_3	DO3_8C_3				
BC	VREFBNC0	IO			DIFFIO_RX_T71b	DIFFOUT_T71b	H22	DO3T	DO1T		DO3_8C_4	DO3_8C_4				
BC	VREFBNC0	IO			DIFFIO_TX_T72b	DIFFOUT_T72b	J23	DO3T	DO1T		DO3_8C_5	DO3_8C_5				
BC	VREFBNC0	IO			DIFFIO_RX_T73b	DIFFOUT_T73b	K22	DQS3TCQ3TCQn3TQKx3T	DQS1TCQ1TCQn1TQKx1T		DO53_8C	DO53_8C				
BC	VREFBNC0	IO			DIFFIO_RX_T73b	DIFFOUT_T73b	L22	DO53TQK3T	DO53TQK1T		DO534_8C	DO534_8C				
BC	VREFBNC0	IO			DIFFIO_TX_T74b	DIFFOUT_T74b	N23	DO3T	DO1T		DO3_8C	DO3_8C				
BC	VREFBNC0	IO			DIFFIO_RX_T75b	DIFFOUT_T75b	L23	DO3T	DO1T		DO3_8C_6	DO3_8C_6				
BC	VREFBNC0	IO			DIFFIO_RX_T75b	DIFFOUT_T75b	M23	DO3T	DO1T		DO3_8C_7	DO3_8C_7				
BC	VREFBNC0	IO			DIFFIO_TX_T76b	DIFFOUT_T76b	K23	DO3T	DO1T		DO3_8C_8	DO3_8C_8				
BB	VREFBBAN0	IO			DIFFIO_RX_T77b	DIFFOUT_T77b	B23	DO4T	DO2T		DO2_8B_0	DO2_8B_0				
BB	VREFBBAN0	IO			DIFFIO_RX_T77b	DIFFOUT_T77b	C24	DO4T	DO2T		DO2_8B_1	DO2_8B_1				
BB	VREFBBAN0	IO			DIFFIO_TX_T78b	DIFFOUT_T78b	M24	DO4T	DO2T		DO2_8B_2	DO2_8B_2				
BB	VREFBBAN0	IO			DIFFIO_RX_T79b	DIFFOUT_T79b	C23	DO4T	DO2T		DO2_8B_3	DO2_8B_3				
BB	VREFBBAN0	IO			DIFFIO_RX_T79b	DIFFOUT_T79b	D23	DO4T	DO2T		DO2_8B_4	DO2_8B_4				
BB	VREFBBAN0	IO			DIFFIO_TX_T80b	DIFFOUT_T80b	C24	DO4T	DO2T		DO2_8B_5	DO2_8B_5				
BB	VREFBBAN0	IO			DIFFIO_RX_T81b	DIFFOUT_T81b	C25	DQS4TCQ4TCQn4TQKx4T	DQS2TCQ2TCQn2TQKx2T		DO52_8B	DO52_8B				
BB	VREFBBAN0	IO			DIFFIO_RX_T81b	DIFFOUT_T81b	D24	DO54TQK4T	DO54TQK2T		DO542_8B	DO542_8B				
BB	VREFBBAN0	IO			DIFFIO_TX_T82b	DIFFOUT_T82b	E24	DO4T	DO2T		DO2_8B_6	DO2_8B_6				
BB	VREFBBAN0	IO			DIFFIO_RX_T83b	DIFFOUT_T83b	E25	DO4T	DO2T		DO2_8B_7	DO2_8B_7				
BB	VREFBBAN0	IO			DIFFIO_TX_T84b	DIFFOUT_T84b	H24	DO4T	DO2T		DO2_8B_8	DO2_8B_8				
BB	VREFBBAN0	IO			DIFFIO_RX_T85b	DIFFOUT_T85b	A25	DO5T	DO3T		DO1_8B_0	DO1_8B_0				
BB	VREFBBAN0	IO			DIFFIO_RX_T85b	DIFFOUT_T85b	A26	DO5T	DO3T		DO1_8B_1	DO1_8B_1				
BB	VREFBBAN0	IO					M25	DO5T	DO3T		DO1_8B_2	DO1_8B_2				
BB	VREFBBAN0	IO		VREFBBAN0			N25									
BB	VREFBBAN0	IO			DIFFIO_RX_T86b	DIFFOUT_T86b	B26	DO5T	DO3T		DO1_8B_3	DO1_8B_3				
BB	VREFBBAN0	IO			DIFFIO_RX_T86b	DIFFOUT_T86b	C26	DO5T	DO3T		DO1_8B_4	DO1_8B_4				
BB	VREFBBAN0	IO			DIFFIO_TX_T87b	DIFFOUT_T87b	A27	DO5T	DO3T		DO1_8B_5	DO1_8B_5				
BB	VREFBBAN0	IO			DIFFIO_TX_T87b	DIFFOUT_T87b	A28									
BB	VREFBBAN0	IO			DIFFIO_RX_T88b	DIFFOUT_T88b	D26	DQS5TCQ5TCQn5TQKx5T	DO5T		DO51_8B	DO51_8B				
BB	VREFBBAN0	IO			DIFFIO_RX_T88b	DIFFOUT_T88b	E26	DO5T	DO3T		DO514_8B	DO514_8B				
BB	VREFBBAN0	IO			DIFFIO_TX_T89b	DIFFOUT_T89b	K24	DO5T	DO3T		DM1_8B	DM1_8B				
BB	VREFBBAN0	IO			DIFFIO_TX_T89b	DIFFOUT_T89b	L24	DO5T	DO3T							
BB	VREFBBAN0	IO			DIFFIO_RX_T90b	DIFFOUT_T90b	F26	DO5T	DO3T		DO1_8B_6	DO1_8B_6				
BB	VREFBBAN0	IO			DIFFIO_RX_T90b	DIFFOUT_T90b	F25	DO5T	DO3T		DO1_8B_7	DO1_8B_7				
BB	VREFBBAN0	IO			DIFFIO_TX_T91b	DIFFOUT_T91b	G26	DO5T	DO3T		DO1_8B_8	DO1_8B_8				
BB	VREFBBAN0	IO			DIFFIO_TX_T91b	DIFFOUT_T91b	G26									
BA	VREFBBAN0	IO			DIFFIO_RX_T92b	DIFFOUT_T92b	B27	DO6T	DO3T		CK_8A	CK_8A				
BA	VREFBBAN0	IO			DIFFIO_RX_T92b	DIFFOUT_T92b	C28	DO6T	DO3T		CK4_8A	CK4_8A				
BA	VREFBBAN0	IO			DIFFIO_TX_T93b	DIFFOUT_T93b	J26	DO6T	DO3T		CKE_8A_0	CKE_8A_0				
BA	VREFBBAN0	IO			DIFFIO_TX_T93b	DIFFOUT_T93b	K25	DO6T	DO3T		CKE_8A_1	CKE_8A_1				
BA	VREFBBAN0	IO			DIFFIO_RX_T94b	DIFFOUT_T94b	B29	DO6T	DO3T		A_8A_0	CA_8A_0				
BA	VREFBBAN0	IO			DIFFIO_RX_T94b	DIFFOUT_T94b	C29	DO6T	DO3T		A_8A_1	CA_8A_1				
BA	VREFBBAN0	IO			DIFFIO_TX_T95b	DIFFOUT_T95b	A29	DO6T	DO3T		A_8A_2	CA_8A_2				
BA	VREFBBAN0	IO			DIFFIO_TX_T95b	DIFFOUT_T95b	A30	DO6T	DO3T		A_8A_3	CA_8A_3				
BA	VREFBBAN0	IO			DIFFIO_RX_T96b	DIFFOUT_T96b	A31	DQS6TCQ6TCQn6TQKx6T	DQS5TCQ5TCQn5TQKx5T		A_8A_4	CA_8A_4				
BA	VREFBBAN0	IO			DIFFIO_RX_T96b	DIFFOUT_T96b	B30	DQS6TQK6T	DO6T		A_8A_5	CA_8A_5				
BA	VREFBBAN0	IO			DIFFIO_TX_T97b	DIFFOUT_T97b	J26	DO6T	DO3T		A_8A_6	CA_8A_6				
BA	VREFBBAN0	IO			DIFFIO_TX_T97b	DIFFOUT_T97b	K26	DO6T	DO3T		A_8A_7	CA_8A_7				
BA	VREFBBAN0	IO			DIFFIO_RX_T98b	DIFFOUT_T98b	A33	DO6T	DO3T		A_8A_8	CA_8A_8				
BA	VREFBBAN0	IO			DIFFIO_RX_T98b	DIFFOUT_T98b	A32	DO6T	DO3T		A_8A_9	CA_8A_9				
BA	VREFBBAN0	IO			DIFFIO_TX_T99b	DIFFOUT_T99b	C33	DO6T	DO3T		A_8A_10					
BA	VREFBBAN0	IO			DIFFIO_TX_T99b	DIFFOUT_T99b	D27	DO6T	DO3T		A_8A_11					
BA	VREFBBAN0	IO			DIFFIO_RX_T100b	DIFFOUT_T100b	D28	DO6T	DO3T		A_8A_12					
BA	VREFBBAN0	IO			DIFFIO_TX_T101b	DIFFOUT_T101b	L26	DO6T	DO3T		A_8A_13					
BA	VREFBBAN0	IO			DIFFIO_TX_T101b	DIFFOUT_T101b	L26				A_8A_14					
BA	VREFBBAN0	IO			DIFFIO_TX_T101b	DIFFOUT_T101b	M26				A_8A_15					
BA	VREFBBAN0	IO			DIFFIO_RX_T102b	DIFFOUT_T102b	E27	DO7T	DO3T		BA_8A_0					
BA	VREFBBAN0	IO			DIFFIO_RX_T102b	DIFFOUT_T102b	F27	DO7T	DO3T		BA_8A_1					
BA	VREFBBAN0	IO			DIFFIO_TX_T103b	DIFFOUT_T103b	F28	DO7T	DO3T		BA_8A_2					
BA	VREFBBAN0	IO			DIFFIO_TX_T103b	DIFFOUT_T103b	G28				RAS2_8A					
BA	VREFBBAN0	IO			DIFFIO_RX_T104b	DIFFOUT_T104b	C32	DQS7TCQ7TCQn7TQKx7T	DO7T		CAS2_8A					
BA	VREFBBAN0	IO			DIFFIO_RX_T104b	DIFFOUT_T104b	C31	DQS7TQK7T	DO7T		WE2_8A					
BA	VREFBBAN0	IO			DIFFIO_TX_T105b	DIFFOUT_T105b	L27	DO7T	DO3T		ODT_8A_0	ODT_8A_0				
BA	VREFBBAN0	IO			DIFFIO_TX_T105b	DIFFOUT_T105b	M28				ODT_8A_1	ODT_8A_1				
BA	VREFBBAN0	IO		CLK23b	DIFFIO_RX_T106b	DIFFOUT_T106b	D31	DO7T	DO3T							
BA	VREFBBAN0	IO		CLK23b	DIFFIO_RX_T106b	DIFFOUT_T106b	E31	DO7T	DO3T							
BA	VREFBBAN0	IO			DIFFIO_TX_T107b	DIFFOUT_T107b	F30	DO7T	DO3T		CSA_8A_0	CSA_8A_0				
BA	VREFBBAN0	IO			DIFFIO_TX_T107b	DIFFOUT_T107b	F29				CSA_8A_1	CSA_8A_1				
BA	VREFBBAN0	IO			DIFFIO_RX_T108b	DIFFOUT_T108b	G29									
BA	VREFBBAN0	IO			DIFFIO_RX_T108b	DIFFOUT_T108b	H28									
BA	VREFBBAN0	IO		VREFBBAN0			N28									
BA	VREFBBAN0	IO		FPLL_TL_CLKOUT3_FPPLL_TL_FB0_FPPLL_TL_FB1	DIFFIO_RX_T109b	DIFFOUT_T109b	J29									
BA	VREFBBAN0	IO		FPLL_TL_CLKOUT3_FPPLL_TL_FB0	DIFFIO_RX_T109b	DIFFOUT_T109b	J28									
BA	VREFBBAN0	IO		FPLL_TL_CLKOUT3_FPPLL_TL_CLKOUT3_FPPLL_TL_FB0	DIFFIO_RX_T109b	DIFFOUT_T109b	K29									
BA	VREFBBAN0	IO		FPLL_TL_CLKOUT3_FPPLL_TL_CLKOUT3	DIFFIO_TX_T110b	DIFFOUT_T110b	L29									
BA	VREFBBAN0	IO		CLK23b	DIFFIO_RX_T111b	DIFFOUT_T111b	J27									
BA	VREFBBAN0	IO		CLK23b	DIFFIO_RX_T111b	DIFFOUT_T111b	K28									



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					AB27									
		GND					AB28									
		GND					AB30									
		GND					AB31									
		GND					AB32									
		GND					AC30									
		GND					AC33									
		GND					AC34									
		GND					AD31									
		GND					AD32									
		GND					AE30									
		GND					AE33									
		GND					AE34									
		GND					AF31									
		GND					AF32									
		GND					AG30									
		GND					AG33									
		GND					AG34									
		GND					AH31									
		GND					AH32									
		GND					AJ30									
		GND					AJ33									
		GND					AJ34									
		GND					AK31									
		GND					AK32									
		GND					AL33									
		GND					AL34									
		GND					E34									
		GND					F31									
		GND					F32									
		GND					G30									
		GND					G33									
		GND					G34									
		GND					H31									
		GND					H32									
		GND					J30									
		GND					J33									
		GND					J34									
		GND					K31									
		GND					K32									
		GND					L30									
		GND					L33									
		GND					L34									
		GND					M30									
		GND					M31									
		GND					M32									
		GND					N28									
		GND					N29									
		GND					N33									
		GND					N34									
		GND					P27									
		GND					P31									
		GND					P32									
		GND					P28									
		GND					R30									
		GND					R33									
		GND					R34									
		GND					T27									
		GND					T29									
		GND					T31									
		GND					T32									
		GND					U28									
		GND					U33									
		GND					U34									
		GND					V27									
		GND					V31									
		GND					V32									
		GND					W28									
		GND					W30									
		GND					W33									
		GND					W34									
		GND					Y27									
		GND					Y29									
		GND					Y31									
		GND					Y32									
		GND					AA1									
		GND					AA2									
		GND					AB3									
		GND					AB4									
		GND					AC1									
		GND					AC2									
		GND					AC3									
		GND					AD3									
		GND					AD4									
		GND					AE1									
		GND					AE2									
		GND					AE3									
		GND					AF4									
		GND					AG1									
		GND					AG2									
		GND					AG3									
		GND					AH3									
		GND					AH4									
		GND					AJ1									
		GND					AJ2									
		GND					AJ3									
		GND					AK4									
		GND					AL1									
		GND					AL2									
		GND					AL3									
		GND					AN1									
		GND					V3									
		GND					V4									
		GND					V7									
		GND					W1									
		GND					W2									
		GND					W6									
		GND					Y3									
		GND					Y4									
		GND					Y8									
		GND					Y8									
		VCCP					R18									
		VCCP					T21									
		VCCP					U26									
		VCCP					W10									
		VCCP					Y10									
		VCCP					Y12									
		VCCP					Y22									



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCCP					Y24									
		VCCP					Y25									
		VCCA_FPLL					V26									
		VCCA_FPLL					V9									
		VCCA_FPLL					T26									
		VCCPLL_HPS					M9									
		VCCBATT					M27									
		VCC_AUX					AA24									
		VCC_AUX					F11									
		VCC_AUX					E24									
		VCC_AUX_SHARED					R12									
		VCCD_FPLL					V26									
		VCCD_FPLL					V9									
		VCCD_FPLL					P26									
		VCCA_GXBLO					V28									
		VCCA_GXBRO					V7									
		VCCA_GXBL1					T28									
		VCCCH_GXBLO					V28									
		VCCCH_GXBRO					V16									
		VCCCH_GXBL1					P28									
		VCCCL_GXBLO					V29									
		VCCCL_GXBRO					V30									
		VCCCL_GXBRO					V5									
		VCCCL_GXBL1					V5									
		VCCCL_GXBL1					P29									
		VCCCL_GXBL1					P30									
		VCCCR_GXBL					AA30									
		VCCCR_GXBL					AB29									
		VCCCR_GXBL					V30									
		VCCCR_GXBL					R29									
		VCCCR_GXBR					AA5									
		VCCCR_GXBR					AB6									
		VCCCR_GXBR					AB6									
		VCCCT_GXBLO					T30									
		VCCCT_GXBLO					U29									
		VCCCT_GXBLO					U30									
		VCCCT_GXBRO					W6									
		VCCCT_GXBRO					A8									
		VCCCT_GXBL1					W29									
		VCCCT_GXBL1					V30									
		VCC					AA30									
		VCC					T19									
		VCC					T23									
		VCC					T26									
		VCC					V24									
		VCC					U18									
		VCC					U20									
		VCC					U22									
		VCC					U24									
		VCC					V15									
		VCC					V17									
		VCC					V19									
		VCC					V20									
		VCC					V21									
		VCC					V22									
		VCC					V23									
		VCC					W16									
		VCC					W14									
		VCC					W20									
		VCC					W22									
		VCC					W24									
		VCC					Y13									
		VCC					Y14									
		VCC					Y15									
		VCC					Y16									
		VCC					Y17									
		VCC					Y19									
		VCC					Y21									
		VCC					Y23									
		VCC					W18									
		VCC_HPS					T11									
		VCC_HPS					U10									
		VCC_HPS					U12									
		VCC_HPS					U14									
		VCC_HPS					V11									
		VCC_HPS					V12									
		VCC_HPS					V13									
		VCC_HPS					W12									
		VCC_HPS					W27									
		VCC00A					AF30									
		VCC00A					AH30									
		VCC00A					AJ29									
		VCC00A					AK30									
		VCC00A					AN29									
		VCC00B					AF25									
		VCC00B					AK24									
		VCC00B					AN24									
		VCC00C					AD21									
		VCC00C					AF21									
		VCC00C					AJ21									
		VCC00C					AM21									
		VCC00D					AE18									
		VCC00D					AH18									
		VCC00D					AL18									
		VCC00A					AD5									
		VCC00A					AEB									
		VCC00A					AF5									
		VCC00A					AH5									
		VCC00A					AK5									
		VCC00B					AD11									
		VCC00B					AF10									
		VCC00B					AJ10									
		VCC00B					AM10									
		VCC00C					AE13									
		VCC00C					AH12									
		VCC00C					AL12									
		VCC00D					AF15									
		VCC00D					AJ15									
		VCC00D					AM15									
		VCC00D					AN17									
		VCC00A_HPS					B3									
		VCC00A_HPS					CB									
		VCC00A_HPS					DB									
		VCC00A_HPS					EB									
		VCC00A_HPS					FB									
		VCC00A_HPS					H5									
		VCC00A_HPS					H7									
		VCC00A_HPS					M7									
		VCC00B_HPS					L4									





Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCC0B8 HPS					M1									
		VCC0B8 HPS					N8									
		VCC0B8 HPS					P3									
		VCC0B8 HPS					R6									
		VCC0B8 HPS					U5									
		VCC0B8 HPS					V2									
		VCC07A HPS					B9									
		VCC07A HPS					D11									
		VCC07A HPS					E13									
		VCC07A HPS					K11									
		VCC07B HPS					B13									
		VCC07B HPS					L13									
		VCC07C HPS					H15									
		VCC07D HPS					E17									
		VCC07D HPS					H18									
		VCC07E HPS					L18									
		VCC08A					C27									
		VCC08A					C30									
		VCC08A					F29									
		VCC08A					E32									
		VCC08A					G27									
		VCC08B					K27									
		VCC08B					B24									
		VCC08B					F24									
		VCC08B					J24									
		VCC08C					B22									
		VCC08C					D21									
		VCC08C					G21									
		VCC08C					L21									
		VCC08D					B18									
		VCC08D					B20									
		VCC08D					H20									
		VCCPD3					AA21									
		VCCPD3					AA23									
		VCCPD3					AB26									
		VCCPD3					AC28									
		VCCPD4					AB8									
		VCCPD4BCD					AA11									
		VCCPD4BCD					AA14									
		VCCPD4BCD					AA15									
		VCCPD4BCD					AB8									
		VCCPD6A8B HPS					P9									
		VCCPD6A8B HPS					R8									
		VCCPD6A8B HPS					U7									
		VCCPD6A8B HPS					U8									
		VCCPD7A HPS					R11									
		VCCPD7B HPS					B13									
		VCCPD7C HPS					T15									
		VCCPD7D HPS					R16									
		VCCPD7E HPS					P17									
		VCCPD8					P23									
		VCCPD8					P25									
		VCCPD8					R20									
		VCCPD8					R22									
		VCCPGM					H13									
		VCCPGM					AC29									
		VCCRSTDLK HPS					H6									
		VCC HPS					R10									
		VCC HPS					R14									
		VCC HPS					T13									
		VCC HPS					T9									
	VREFB7A/B7C/D7/E0 HPS	VREFB7A/B7C/D7/E0 HPS					P15									
		GND					A18									
		GND					A22									
		GND					A5									
		GND					AA10									
		GND					AA13									
		GND					AA16									
		GND					AA19									
		GND					AA22									
		GND					AA25									
		GND					AA8									
		GND					AB7									
		GND					AC6									
		GND					AD10									
		GND					AD13									
		GND					AD16									
		GND					AD19									
		GND					AD22									
		GND					AD25									
		GND					AD28									
		GND					AD7									
		GND					AG10									
		GND					AG13									
		GND					AG16									
		GND					AG19									
		GND					AG22									
		GND					AG25									
		GND					AG28									
		GND					AG7									
		GND					AK10									
		GND					AK13									
		GND					AK16									
		GND					AK19									
		GND					AK22									
		GND					AK25									
		GND					AK28									
		GND					AK7									
		GND					AN10									
		GND					AN13									
		GND					AN16									
		GND					AN19									
		GND					AN22									
		GND					AN25									
		GND					AN28									
		GND					AN31									
		GND					AN4									
		GND					AN7									
		GND					B11									
		GND					B16									
		GND					B2									
		GND					B25									
		GND					B28									
		GND					B31									
		GND					B33									
		GND					B8									
		GND					C19									
		GND					C22									
		GND					C5									
		GND					D2									



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					D30									
		GND					E14									
		GND					E25									
		GND					E28									
		GND					E8									
		GND					F19									
		GND					F22									
		GND					F5									
		GND					G11									
		GND					G2									
		GND					H25									
		GND					H28									
		GND					H8									
		GND					J13									
		GND					J19									
		GND					J22									
		GND					J5									
		GND					K16									
		GND					K2									
		GND					L25									
		GND					L28									
		GND					L8									
		GND					M18									
		GND					M22									
		GND					M5									
		GND					N11									
		GND					N15									
		GND					N2									
		GND					N24									
		GND					P13									
		GND					P18									
		GND					P8									
		GND					V18									
		GND					V14									
		GND					V16									
		GND					V8									
		GND					W11									
		GND					W13									
		GND					W15									
		GND					W17									
		GND					W19									
		GND					W21									
		GND					W23									
		GND					W28									
		GND					W9									
		GND					Y18									
		GND					Z20									
		GND					Z17									
		GND					R19									
		GND					R21									
		GND					R23									
		GND					R25									
		GND					R5									
		GND					R8									
		GND					T10									
		GND					T12									
		GND					T14									
		GND					T18									
		GND					T2									
		GND					T20									
		GND					T22									
		GND					T24									
		GND					U11									
		GND					U13									
		GND					U17									
		GND					U19									
		GND					U21									
		GND					U23									
		GND					U25									
		GND					U6									
		GND					U9									
		GND					V10									

Notes:  
 (1) For more information about pin definitions and pin connection guidelines, refer to the [Altera V Device Family Pin Connection Guidelines](#).  
 (2) GND, REFCLK pin is not supported in current Quartus II version, but will be supported in future Quartus II release version.  
 (3) Pins with \* contains similar name with other pins in the same column. For the selection of the HPS pins, refer to the "HPS Pin Mux Select x" columns.  
 (4) Pins with \* are the 10 Gbps transceiver channels. For more information about the 10 Gbps transceiver channels clocking recommendation, refer to the [Transceiver Clocking in Arria V Devices chapter](#).  
 (5) RESET pin is only applicable for DDR3 device.



Bank Number	VREF	PinName/Function (Z1, Z3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for BDK3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		DNU					A38									
		DNU					B38									
		DNU					B39									
		DNU					U32									
		DNU					U31									
		DNU					C38									
		DNU					E37									
		DNU					D39									
		DNU					D38									
		DNU					E36									
		DNU					E37									
		DNU					F39									
		DNU					F38									
		DNU					G36									
		DNU					G37									
		DNU					H38									
		DNU					H38									
		DNU					J36									
		DNU					J37									
		DNU					K39									
		DNU					K38									
		DNU					L36									
		DNU					L37									
		DNU					M39									
		DNU					M38									
		DNU					N36									
		DNU					N37									
		DNU					P39									
		DNU					P38									
		DNU					W32									
		DNU					W31									
		DNU					AA32									
		DNU					AA31									
		DNU					R36									
		DNU					R37									
		DNU					T39									
		DNU					T38									
		DNU					U36									
		DNU					U37									
		DNU					V39									
		DNU					V38									
		DNU					W36									
		DNU					W37									
		DNU					Y39									
		DNU					Y38									
		DNU					AA36									
		DNU					AA37									
		DNU					AR39									
		DNU					AR38									
		DNU					AC36									
		DNU					AC37									
		DNU					AD39									
		DNU					AD38									
		DNU					AE36									
		DNU					AE37									
		DNU					AF39									
		DNU					AF38									
		DNU					AC32									
		DNU					AC31									
		DNU					AE32									
		DNU					AE31									
		DNU					AG36									
		DNU					AG37									
		DNU					AH39									
		DNU					AH38									
		DNU					AJ36									
		DNU					AJ37									
		DNU					AK39									
		DNU					AK38									
		DNU					AL36									
		DNU					AL37									
		DNU					AM39									
		DNU					AM38									
		DNU					AN36									
		DNU					AN37									
		DNU					AP39									
		DNU					AP38									
		DNU					AR36									
		DNU					AR37									
		DNU					AT39									
		DNU					AT38									
		DNU					AU36									
		DNU					AU37									
		DNU					AW37									
		DNU					AW36									
		DNU					AG33									
		DNU					AG32									
		DNU					AK31									
		DNU					AT34									
		DNU					AM35									
		DNU					AK34									
		DNU					AT33									
		DNU					AW34									
		DNU					AR34									
		DNU					AL34									
		DNU					AR33									
		DNU					AU33									
		DNU					AV33									
		DNU					AV32									
		DNU					AN33									
		DNU					AN33									
		DNU					AP33									
		DNU					AN34									
		DNU					AP34									
		DNU					AK32									
		DNU					AL32									
		DNU					AJ34									
		DNU					AK34									
		DNU					AL34									
		DNU					AM34									
		DNU					AJ33									
		DNU					AK33									
		DNU					AJ31									
		DNU					AK31									
		DNU					AL33									
		DNU					AM33									
		DNU					AN32									
		DNU					AP32									
		DNU					AT32									
		DNU					AK32									
		DNU					AL31									
		DNU					AK31									
		DNU					AL31									
		DNU					AK31									



Pin Information for the Arria® V 5ASXFB3 Device  
Version 1.3  
Note (1)

Bank Number	VREF	PinName/Function (Z1, Z)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DQS3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
5A	VREFBAND	ID			DIFFO_RX_B11n	DFFOUT_B11n	AW33	DQS2B/QK2B	DQ1B		WEA_3A					
5A	VREFBAND	ID			DIFFO_RX_B11p	DFFOUT_B11p	AW32	DQS2B/CQ2B/CO2B/QK2B	DQ1B		CASE_3A					
5A	VREFBAND	ID			DIFFO_TX_B12n	DFFOUT_B12n	AN31				RASS_3A					
5A	VREFBAND	ID			DIFFO_TX_B12p	DFFOUT_B12p	AP31	DO2B			BA_3A_2					
5A	VREFBAND	ID			DIFFO_RX_B13n	DFFOUT_B13n	AR31	DO2B			BA_3A_1					
5A	VREFBAND	ID			DIFFO_RX_B13p	DFFOUT_B13p	AT31	DO2B			BA_3A_0					
5A	VREFBAND	ID			DIFFO_TX_B14n	DFFOUT_B14n	AE29				A_3A_15					
5A	VREFBAND	ID			DIFFO_TX_B14p	DFFOUT_B14p	AE29	DO2B			A_3A_14					
5A	VREFBAND	ID			DIFFO_RX_B15n	DFFOUT_B15n	AG30	DO2B			A_3A_13					
5A	VREFBAND	ID			DIFFO_RX_B15p	DFFOUT_B15p	AH30	DO2B			A_3A_12					
5A	VREFBAND	ID			DIFFO_TX_B16n	DFFOUT_B16n	AL31				A_3A_11					
5A	VREFBAND	ID			DIFFO_TX_B16p	DFFOUT_B16p	AV31	DO2B			A_3A_10					
5A	VREFBAND	ID			DIFFO_RX_B17n	DFFOUT_B17n	AW30	DO2B			A_3A_9	CA_3A_9				
5A	VREFBAND	ID			DIFFO_RX_B17p	DFFOUT_B17p	AW31	DO2B			A_3A_8	CA_3A_8				
5A	VREFBAND	ID			DIFFO_TX_B18n	DFFOUT_B18n	AK30				A_3A_7	CA_3A_7				
5A	VREFBAND	ID			DIFFO_TX_B18p	DFFOUT_B18p	AL30	DO2B			A_3A_6	CA_3A_6				
5A	VREFBAND	ID			DIFFO_RX_B19n	DFFOUT_B19n	AR30	DQS2B/QK3B	DQS1B/QK1B		A_3A_5	CA_3A_5				
5A	VREFBAND	ID			DIFFO_RX_B19p	DFFOUT_B19p	AT30	DQS2B/CQ2B/CO2B/QK2B	DQS1B/CQ1B/CO1B/QK1B		A_3A_4	CA_3A_4				
5A	VREFBAND	ID			DIFFO_TX_B20n	DFFOUT_B20n	AL30				A_3A_3	CA_3A_3				
5A	VREFBAND	ID			DIFFO_TX_B20p	DFFOUT_B20p	AV30	DO2B			A_3A_2	CA_3A_2				
5A	VREFBAND	ID			DIFFO_RX_B21n	DFFOUT_B21n	AT29	DO2B			A_3A_1	CA_3A_1				
5A	VREFBAND	ID			DIFFO_RX_B21p	DFFOUT_B21p	AL29	DO2B			CA_3A_0	CA_3A_0				
5A	VREFBAND	ID			DIFFO_TX_B22n	DFFOUT_B22n	AN30				CKE_3A_1	CKE_3A_1				
5A	VREFBAND	ID			DIFFO_TX_B22p	DFFOUT_B22p	AP30	DO2B			CKE_3A_0	CKE_3A_0				
5A	VREFBAND	ID			DIFFO_RX_B23n	DFFOUT_B23n	AN29	DO2B			CKE_3A	CKE_3A				
5A	VREFBAND	ID			DIFFO_RX_B23p	DFFOUT_B23p	AP29	DO2B			CK_3A	CK_3A				
5A	VREFBAND	ID			DIFFO_TX_B24n	DFFOUT_B24n	AR29				RESETP_3A					
5B	VREFBAND	ID			DIFFO_TX_B24p	DFFOUT_B24p	AC29	DO4B		DO1B	DO1_3B_8	DO1_3B_8				
5B	VREFBAND	ID			DIFFO_RX_B25n	DFFOUT_B25n	AF28	DO2B		DO1B	DO1_3B_7	DO1_3B_7				
5B	VREFBAND	ID			DIFFO_RX_B25p	DFFOUT_B25p	AG28	DO4B		DO1B	DO1_3B_6	DO1_3B_6				
5B	VREFBAND	ID			DIFFO_TX_B26n	DFFOUT_B26n	AK29									
5B	VREFBAND	ID			DIFFO_TX_B26p	DFFOUT_B26p	AL29	DO4B		DO1B	DM1_3B	DM1_3B				
5B	VREFBAND	ID			DIFFO_RX_B27n	DFFOUT_B27n	AH28	DQS4B/QK4B		DO1B	DQS4_3B	DQS4_3B				
5B	VREFBAND	ID			DIFFO_RX_B27p	DFFOUT_B27p	AJ28	DQS4B/CQ4B/CO4B/QK4B		DO1B	DQS1_3B	DQS1_3B				
5B	VREFBAND	ID			DIFFO_TX_B28n	DFFOUT_B28n	AK29									
5B	VREFBAND	ID			DIFFO_TX_B28p	DFFOUT_B28p	AE28	DO4B		DO1B	DO1_3B_5	DO1_3B_5				
5B	VREFBAND	ID			DIFFO_RX_B29n	DFFOUT_B29n	AM27	DO4B		DO1B	DO1_3B_4	DO1_3B_4				
5B	VREFBAND	ID		VREFBAND	DIFFO_RX_B29p	DFFOUT_B29p	AL28	DO4B		DO1B	DO1_3B_3	DO1_3B_3				
5B	VREFBAND	ID					AM28	DO4B		DO1B	DO1_3B_2	DO1_3B_2				
5B	VREFBAND	ID			DIFFO_RX_B30n	DFFOUT_B30n	AC28	DO2B		DO1B	DO1_3B_1	DO1_3B_1				
5B	VREFBAND	ID			DIFFO_RX_B30p	DFFOUT_B30p	AD27	DO4B		DO1B	DO1_3B_0	DO1_3B_0				
5B	VREFBAND	ID			DIFFO_TX_B31n	DFFOUT_B31n	AF28									
5B	VREFBAND	ID			DIFFO_TX_B31p	DFFOUT_B31p	AG28	DO2B		DO1B	DO2_3B_8	DO2_3B_8				
5B	VREFBAND	ID			DIFFO_RX_B32n	DFFOUT_B32n	AL28	DO2B		DO1B	DO2_3B_7	DO2_3B_7				
5B	VREFBAND	ID			DIFFO_RX_B32p	DFFOUT_B32p	AM28	DO2B		DO1B	DO2_3B_6	DO2_3B_6				
5B	VREFBAND	ID			DIFFO_TX_B33n	DFFOUT_B33n	AK27									
5B	VREFBAND	ID			DIFFO_TX_B33p	DFFOUT_B33p	AL27	DO2B		DO1B	DM2_3B	DM2_3B				
5B	VREFBAND	ID			DIFFO_RX_B34n	DFFOUT_B34n	AW29	DQS2B/QK2B		DO1B	DQS2_3B	DQS2_3B				
5B	VREFBAND	ID			DIFFO_RX_B34p	DFFOUT_B34p	AW28	DQS2B/CQ2B/CO2B/QK2B	DQS2B/CQ2B/CO2B/QK2B		DQS2_3B	DQS2_3B				
5B	VREFBAND	ID			DIFFO_TX_B35n	DFFOUT_B35n	AE27				DO2_3B_4	DO2_3B_4				
5B	VREFBAND	ID			DIFFO_TX_B35p	DFFOUT_B35p	AR27	DO2B		DO1B	DO2_3B_5	DO2_3B_5				
5B	VREFBAND	ID			DIFFO_RX_B36n	DFFOUT_B36n	AT27	DO2B		DO1B	DO2_3B_4	DO2_3B_4				
5B	VREFBAND	ID			DIFFO_RX_B36p	DFFOUT_B36p	AK27	DO2B		DO1B	DO2_3B_3	DO2_3B_3				
5B	VREFBAND	ID			DIFFO_TX_B37n	DFFOUT_B37n	AM27									
5B	VREFBAND	ID			DIFFO_TX_B37p	DFFOUT_B37p	AN27	DO2B		DO1B	DO2_3B_2	DO2_3B_2				
5B	VREFBAND	ID			DIFFO_RX_B38n	DFFOUT_B38n	AV27	DO2B		DO1B	DO2_3B_1	DO2_3B_1				
5B	VREFBAND	ID			DIFFO_RX_B38p	DFFOUT_B38p	AW27	DO2B		DO1B	DO2_3B_0	DO2_3B_0				
5C	VREFBAND	ID			DIFFO_TX_B39n	DFFOUT_B39n	AE27	DO2B		DO1B	DO3_3C_8	DO3_3C_8				
5C	VREFBAND	ID			DIFFO_RX_B40n	DFFOUT_B40n	AG26	DO2B		DO1B	DO3_3C_7	DO3_3C_7				
5C	VREFBAND	ID			DIFFO_RX_B40p	DFFOUT_B40p	AK26	DO2B		DO1B	DO3_3C_6	DO3_3C_6				
5C	VREFBAND	ID			DIFFO_TX_B41n	DFFOUT_B41n	AE27									
5C	VREFBAND	ID			DIFFO_TX_B41p	DFFOUT_B41p	AF27	DO2B		DO1B	DM3_3C	DM3_3C				
5C	VREFBAND	ID			DIFFO_RX_B42n	DFFOUT_B42n	AE26	DQS4B/QK4B		DO1B	DQS4_3C	DQS4_3C				
5C	VREFBAND	ID			DIFFO_RX_B42p	DFFOUT_B42p	AF26	DQS4B/CQ4B/CO4B/QK4B	DQS4B/CQ4B/CO4B/QK4B		DQS4_3C	DQS4_3C				
5C	VREFBAND	ID			DIFFO_TX_B43n	DFFOUT_B43n	AC24									
5C	VREFBAND	ID			DIFFO_TX_B43p	DFFOUT_B43p	AD25	DO2B		DO1B	DO3_3C_5	DO3_3C_5				
5C	VREFBAND	ID			DIFFO_RX_B44n	DFFOUT_B44n	AG26	DO2B		DO1B	DO3_3C_4	DO3_3C_4				
5C	VREFBAND	ID			DIFFO_RX_B44p	DFFOUT_B44p	AH26	DO2B		DO1B	DO3_3C_3	DO3_3C_3				
5C	VREFBAND	ID			DIFFO_TX_B45n	DFFOUT_B45n	AD26	DO2B		DO1B	DO3_3C_2	DO3_3C_2				
5C	VREFBAND	ID			DIFFO_TX_B45p	DFFOUT_B45p	AE26	DO2B		DO1B	DO3_3C_1	DO3_3C_1				
5C	VREFBAND	ID			DIFFO_RX_B46n	DFFOUT_B46n	AG25	DO2B		DO1B	DO3_3C_0	DO3_3C_0				
5C	VREFBAND	ID			DIFFO_RX_B46p	DFFOUT_B46p	AH25	DO2B		DO1B	DO3_3C_0	DO3_3C_0				
5C	VREFBAND	ID			DIFFO_TX_B47n	DFFOUT_B47n	AM26									
5C	VREFBAND	ID			DIFFO_RX_B47p	DFFOUT_B47p	AP26	DO7B		DO3B	DO4_3C_8	DO4_3C_8				
5C	VREFBAND	ID			DIFFO_RX_B48n	DFFOUT_B48n	AM25	DO7B		DO3B	DO4_3C_7	DO4_3C_7				
5C	VREFBAND	ID			DIFFO_TX_B48p	DFFOUT_B48p	AN25	DO7B		DO3B	DO4_3C_6	DO4_3C_6				
5C	VREFBAND	ID			DIFFO_TX_B49n	DFFOUT_B49n	AL25									
5C	VREFBAND	ID			DIFFO_TX_B49p	DFFOUT_B49p	AK25	DO2B		DO1B	DM4_3C	DM4_3C				
5C	VREFBAND	ID			DIFFO_RX_B50n	DFFOUT_B50n	AT26	DQS7B/QK7B	DQS3B/QK3B		DQS4_3C	DQS4_3C				
5C	VREFBAND	ID			DIFFO_RX_B50p	DFFOUT_B50p	AL26	DQS7B/CQ7B/CO7B/QK7B	DQS3B/CQ3B/CO3B/QK3B		DQS4_3C	DQS4_3C				
5C	VREFBAND	ID			DIFFO_TX_B51n	DFFOUT_B51n	AR25									
5C	VREFBAND	ID			DIFFO_TX_B51p	DFFOUT_B51p	AT25	DO7B		DO3B	DO4_3C_5	DO4_3C_5				
5C	VREFBAND	ID			DIFFO_RX_B52n	DFFOUT_B52n	AV25	DO7B		DO3B	DO4_3C_4	DO4_3C_4				
5C	VREFBAND	ID			DIFFO_RX_B52p	DFFOUT_B52p	AW26	DO7B		DO3B	DO4_3C_3	DO4_3C_3				
5C	VREFBAND	ID					AK26									
5C	VREFBAND	ID					AL26	DO7B		DO3B	DO4_3C_2	DO4_3C_2				
5C	VREFBAND	ID			DIFFO_RX_B53n	DFFOUT_B53n	AV25	DO2B		DO3B	DO4_3C_1	DO4_3C_1				
5C	VREFBAND	ID			DIFFO_RX_B53p	DFFOUT_B53p	AV24	DO7B		DO3B	DO4_3C_0	DO4_3C_0				
5C	VREFBAND	ID			DIFFO_TX_B54n	DFFOUT_B54n	AD24									
5C	VREFBAND	ID			DIFFO_TX_B54p	DFFOUT_B54p	AD24	DO2B		DO4B	DQS_3C_8	DQS_3C_8				
5C	VREFBAND	ID			DIFFO_RX_B55n	DFFOUT_B55n	AT24	DO2B		DO4B	DQS_3C_7	DQS_3C_7				
5C	VREFBAND	ID			DIFFO_RX_B55p	DFFOUT_B55p	AL24	DO2B		DO4B	DQS_3C_6	DQS_3C_6				
5C	VREFBAND	ID			DIFFO_TX_B56n	DFFOUT_B56n	AK24									
5C	VREFBAND	ID			DIFFO_TX_B56p	DFFOUT_B56p	AL24	DO2B		DO4B	DQS_3C_5	DQS_3C_5				
5C	VREFBAND	ID			DIFFO_RX_B57n	DFFOUT_B57n	AE24	DQS4B/QK4B		DO4B	DQS4_3C	DQS4_3C				
5C	VREFBAND	ID			DIFFO_RX_B57p	DFFOUT_B57p	AF24	DQS4B/CQ4B/CO4B/QK4B	DQS4B/CQ4B/CO4B/QK4B		DQS4_3C	DQS4_3C				
5C	VREFBAND	ID			DIFFO_TX_B58n	DFFOUT_B58n	AG24									
5C	VREFBAND	ID			DIFFO_TX_B58p	DFFOUT_B58p	AW24	DO2B		DO4B	DQS_3C_5	DQS_3C_5				
5C	VREFBAND	ID			DIFFO_RX_B59n	DFFOUT_B59n	AV23	DO2B		DO4B	DO5_3C_4	DO5_3C_4				
5C	VREFBAND	ID			DIFFO_RX_B59p	DFFOUT_B59p	AW24	DO2B		DO4B	DO5_3C_3	DO5_3C_3				
5C	VREFBAND	ID			DIFFO_TX_B60n	DFFOUT_B60n	AN24									
5C	VREFBAND	ID			DIFFO_TX_B60p	DFFOUT_B60p	AP24	DO2B		DO2B	DO5_3C_					



Bank Number	VREF	PinName/Function (Z1, Z)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DQK3 (S)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
3D	VREFB3D0	IO			DIFFO_RX_B68n	DIFFOUT_B68n	AE22	DQ6B	DQ4B	DQ2B						
3D	VREFB3D0	IO			DIFFO_RX_B69p	DIFFOUT_B69p	AF22	DQ6B	DQ4B	DQ2B						
3D	VREFB3D0	IO			DIFFO_TX_B70n	DIFFOUT_B70n	AN22	DQ0B								
3D	VREFB3D0	IO			DIFFO_TX_B70p	DIFFOUT_B70p	AF22	DQ0B								
3D	VREFB3D0	IO			DIFFO_RX_B71n	DIFFOUT_B71n	AW19	DQ10B	DQ5B	DQ2B						
3D	VREFB3D0	IO			DIFFO_RX_B71p	DIFFOUT_B71p	AW20	DQ10B	DQ5B	DQ2B						
3D	VREFB3D0	IO			DIFFO_TX_B72n	DIFFOUT_B72n	AE22	DQ0B								
3D	VREFB3D0	IO			DIFFO_TX_B72p	DIFFOUT_B72p	AL22	DQ10B	DQ5B	DQ2B						
3D	VREFB3D0	IO			DIFFO_RX_B73n	DIFFOUT_B73n	AR21	DQ5n10B/Ck10B	DQ5B	DQ5n2B/Ck2B						
3D	VREFB3D0	IO			DIFFO_RX_B73p	DIFFOUT_B73p	AT21	DQ5n10B/CQ10B/CQn10B/Ck10B	DQ5B	DQ5n2B/Ck2B/CQn2B/Ck2B						
3D	VREFB3D0	IO			DIFFO_TX_B74n	DIFFOUT_B74n	AG22	DQ0B								
3D	VREFB3D0	IO			DIFFO_TX_B74p	DIFFOUT_B74p	AH22	DQ10B	DQ5B	DQ2B						
3D	VREFB3D0	IO			DIFFO_RX_B75n	DIFFOUT_B75n	AT20	DQ0B								
3D	VREFB3D0	IO		VREFB3D0	DIFFO_RX_B75p	DIFFOUT_B75p	AU20	DQ10B	DQ5B	DQ2B						
3D	VREFB3D0	IO					AJ21	DQ10B	DQ5B	DQ2B						
3D	VREFB3D0	IO					AK21	DQ10B	DQ5B	DQ2B						
3D	VREFB3D0	IO	CLK4n		DIFFO_RX_B76n	DIFFOUT_B76n	AL19	DQ10B	DQ5B	DQ2B						
3D	VREFB3D0	IO	CLK4p		DIFFO_RX_B76p	DIFFOUT_B76p	AV19	DQ10B	DQ5B	DQ2B						
3D	VREFB3D0	IO			DIFFO_TX_B77n	DIFFOUT_B77n	AM21	DQ11B	DQ6B	DQ3B						
3D	VREFB3D0	IO			DIFFO_TX_B77p	DIFFOUT_B77p	AN21	DQ11B	DQ6B	DQ3B						
3D	VREFB3D0	IO	CLK5n		DIFFO_RX_B78n	DIFFOUT_B78n	AE21	DQ11B	DQ6B	DQ3B						
3D	VREFB3D0	IO	CLK5p		DIFFO_RX_B78p	DIFFOUT_B78p	AF21	DQ11B	DQ6B	DQ3B						
3D	VREFB3D0	IO	FPLL_BC_CLKOUT0,FPLL_BC_CLKOUTn		DIFFO_TX_B79n	DIFFOUT_B79n	AG21	DQ11B	DQ6B	DQ3B						
3D	VREFB3D0	IO	FPLL_BC_CLKOUT0,FPLL_BC_CLKOUTn,FPLL_BC_FB0		DIFFO_TX_B79p	DIFFOUT_B79p	AC22	DQ11B	DQ6B	DQ3B						
3D	VREFB3D0	IO	FPLL_BC_CLKOUT0,FPLL_BC_FBn		DIFFO_RX_B80n	DIFFOUT_B80n	AG21	DQ5n11B/Ck11B	DQ5B	DQ5n2B/Ck2B						
3D	VREFB3D0	IO	FPLL_BC_CLKOUT0,FPLL_BC_FBn,FPLL_BC_FB1		DIFFO_RX_B80p	DIFFOUT_B80p	AN21	DQ5n11B/CQ11B/CQn11B/Ck11B	DQ5B	DQ5n2B/Ck2B/CQn2B/Ck2B						
3D	VREFB3D0	IO			DIFFO_TX_B81n	DIFFOUT_B81n	AN20	DQ11B	DQ6B	DQ3B						
3D	VREFB3D0	IO			DIFFO_TX_B81p	DIFFOUT_B81p	AP20	DQ11B	DQ6B	DQ3B						
3D	VREFB3D0	IO			DIFFO_RX_B82n	DIFFOUT_B82n	AG21	DQ11B	DQ6B	DQ3B						
3D	VREFB3D0	IO			DIFFO_RX_B82p	DIFFOUT_B82p	AD20	DQ11B	DQ6B	DQ3B						
3D	VREFB3D0	IO	CLK6n		DIFFO_TX_B83n	DIFFOUT_B83n	AG20	DQ11B	DQ6B	DQ3B						
3D	VREFB3D0	IO	CLK6p		DIFFO_TX_B83p	DIFFOUT_B83p	AK20	DQ11B	DQ6B	DQ3B						
3D	VREFB3D0	IO			DIFFO_RX_B84n	DIFFOUT_B84n	AK20	DQ11B	DQ6B	DQ3B						
3D	VREFB3D0	IO	CLK7n		DIFFO_RX_B84p	DIFFOUT_B84p	AL20	DQ11B	DQ6B	DQ3B						
3D	VREFB3D0	IO	CLK7p				AE20	DQ11B	DQ6B	DQ3B						
3D	VREFB3D0	IO	VCC0,FPLL,VCCA,FPLL				AE21									
3D	VREFB3D0	IO	DN0				AE20									
3D	VREFB3D0	IO			DIFFO_TX_B85n	DIFFOUT_B85n	AV18									
3D	VREFB3D0	IO			DIFFO_TX_B85p	DIFFOUT_B85p	AW18	DQ12B								
3D	VREFB3D0	IO			DIFFO_RX_B86n	DIFFOUT_B86n	AG19	DQ12B								
3D	VREFB3D0	IO			DIFFO_RX_B86p	DIFFOUT_B86p	AH19	DQ12B								
3D	VREFB3D0	IO			DIFFO_TX_B87n	DIFFOUT_B87n	AN19	DQ12B								
3D	VREFB3D0	IO			DIFFO_TX_B87p	DIFFOUT_B87p	AP19	DQ12B								
3D	VREFB3D0	IO			DIFFO_RX_B88n	DIFFOUT_B88n	AN19	DQ5n12B/Ck12B								
3D	VREFB3D0	IO			DIFFO_RX_B88p	DIFFOUT_B88p	AL19	DQ5n12B/CQ12B/CQn12B/Ck12B								
3D	VREFB3D0	IO			DIFFO_TX_B89n	DIFFOUT_B89n	AH18									
3D	VREFB3D0	IO			DIFFO_TX_B89p	DIFFOUT_B89p	AJ18	DQ12B								
3D	VREFB3D0	IO			DIFFO_RX_B90n	DIFFOUT_B90n	AU18	DQ12B								
3D	VREFB3D0	IO			DIFFO_RX_B90p	DIFFOUT_B90p	AT19	DQ12B								
3D	VREFB3D0	IO			DIFFO_TX_B91n	DIFFOUT_B91n	AE19									
3D	VREFB3D0	IO			DIFFO_TX_B91p	DIFFOUT_B91p	AF19	DQ12B								
3D	VREFB3D0	IO			DIFFO_RX_B92n	DIFFOUT_B92n	AW17	DQ12B								
3D	VREFB3D0	IO			DIFFO_RX_B92p	DIFFOUT_B92p	AW16	DQ12B								
3D	VREFB3D0	IO			DIFFO_TX_B93n	DIFFOUT_B93n	AK17	DQ12B								
3D	VREFB3D0	IO			DIFFO_TX_B93p	DIFFOUT_B93p	AL17	DQ13B	DQ6B							
3D	VREFB3D0	IO			DIFFO_RX_B94n	DIFFOUT_B94n	AT17	DQ13B	DQ6B							
3D	VREFB3D0	IO			DIFFO_RX_B94p	DIFFOUT_B94p	AU17	DQ13B	DQ6B							
3D	VREFB3D0	IO			DIFFO_TX_B95n	DIFFOUT_B95n	AC19	DQ13B	DQ6B							
3D	VREFB3D0	IO			DIFFO_TX_B95p	DIFFOUT_B95p	AD19	DQ13B	DQ6B							
3D	VREFB3D0	IO			DIFFO_RX_B96n	DIFFOUT_B96n	AF18	DQ5n13B/Ck13B	DQ5B							
3D	VREFB3D0	IO			DIFFO_RX_B96p	DIFFOUT_B96p	AR18	DQ5n13B/CQ13B/CQn13B/Ck13B	DQ5B							
3D	VREFB3D0	IO			DIFFO_TX_B97n	DIFFOUT_B97n	AD17	DQ13B	DQ6B							
3D	VREFB3D0	IO			DIFFO_TX_B97p	DIFFOUT_B97p	AG18	DQ13B	DQ6B							
3D	VREFB3D0	IO			DIFFO_RX_B98n	DIFFOUT_B98n	AD18	DQ13B	DQ6B							
3D	VREFB3D0	IO			DIFFO_RX_B98p	DIFFOUT_B98p	AE18	DQ13B	DQ6B							
3D	VREFB3D0	IO		VREFB3D0			AF18									
3D	VREFB3D0	IO					AG18	DQ13B	DQ6B							
3D	VREFB3D0	IO			DIFFO_RX_B99n	DIFFOUT_B99n	AL18	DQ13B	DQ6B							
3D	VREFB3D0	IO			DIFFO_RX_B99p	DIFFOUT_B99p	AM18	DQ13B	DQ6B							
3D	VREFB3D0	IO			DIFFO_TX_B100n	DIFFOUT_B100n	AG17	DQ13B	DQ6B							
3D	VREFB3D0	IO			DIFFO_TX_B100p	DIFFOUT_B100p	AH17	DQ14B	DQ6B							
3D	VREFB3D0	IO			DIFFO_RX_B101n	DIFFOUT_B101n	AN17	DQ14B	DQ6B							
3D	VREFB3D0	IO			DIFFO_RX_B101p	DIFFOUT_B101p	AP17	DQ14B	DQ6B							
3D	VREFB3D0	IO			DIFFO_TX_B102n	DIFFOUT_B102n	AR16	DQ14B	DQ6B							
3D	VREFB3D0	IO			DIFFO_TX_B102p	DIFFOUT_B102p	AT16	DQ14B	DQ6B							
3D	VREFB3D0	IO			DIFFO_RX_B103n	DIFFOUT_B103n	AU16	DQ5n14B/Ck14B	DQ5B							
3D	VREFB3D0	IO			DIFFO_RX_B103p	DIFFOUT_B103p	AV16	DQ5n14B/CQ14B/CQn14B/Ck14B	DQ5B							
3D	VREFB3D0	IO			DIFFO_TX_B104n	DIFFOUT_B104n	AJ16	DQ14B	DQ6B							
3D	VREFB3D0	IO			DIFFO_TX_B104p	DIFFOUT_B104p	AK16	DQ14B	DQ6B							
3D	VREFB3D0	IO			DIFFO_RX_B105n	DIFFOUT_B105n	AN16	DQ14B	DQ6B							
3D	VREFB3D0	IO			DIFFO_RX_B105p	DIFFOUT_B105p	AP16	DQ14B	DQ6B							
3D	VREFB3D0	IO			DIFFO_TX_B106n	DIFFOUT_B106n	AL16	DQ14B	DQ6B							
3D	VREFB3D0	IO			DIFFO_TX_B106p	DIFFOUT_B106p	AM16	DQ14B	DQ6B							
3D	VREFB3D0	IO			DIFFO_RX_B107n	DIFFOUT_B107n	AE17	DQ14B	DQ6B							
3D	VREFB3D0	IO			DIFFO_RX_B107p	DIFFOUT_B107p	AF16	DQ14B	DQ6B							
3D	VREFB3D0	IO			DIFFO_TX_B108n	DIFFOUT_B108n	AN15	DQ14B	DQ6B							
3D	VREFB3D0	IO			DIFFO_TX_B108p	DIFFOUT_B108p	AP15	DQ15B	DQ7B							
3D	VREFB3D0	IO			DIFFO_RX_B109n	DIFFOUT_B109n	AW14	DQ15B	DQ7B							
3D	VREFB3D0	IO			DIFFO_RX_B109p	DIFFOUT_B109p	AW15	DQ15B	DQ7B							
3D	VREFB3D0	IO			DIFFO_TX_B110n	DIFFOUT_B110n	AC18	DQ15B	DQ7B							
3D	VREFB3D0	IO			DIFFO_TX_B110p	DIFFOUT_B110p	AD16	DQ15B	DQ7B							
3D	VREFB3D0	IO			DIFFO_RX_B111n	DIFFOUT_B111n	AG16	DQ5n15B/Ck15B	DQ5B							
3D	VREFB3D0	IO			DIFFO_RX_B111p	DIFFOUT_B111p	AH16	DQ5n15B/CQ15B/CQn15B/Ck15B	DQ5B							
3D	VREFB3D0	IO			DIFFO_TX_B112n	DIFFOUT_B112n	AK15	DQ15B	DQ7B							
3D	VREFB3D0	IO			DIFFO_TX_B112p	DIFFOUT_B112p	AL15	DQ15B	DQ7B							
3D	VREFB3D0	IO			DIFFO_RX_B113n	DIFFOUT_B113n	AV13	DQ15B	DQ7B							
3D	VREFB3D0	IO		VREFB3D0	DIFFO_RX_B113p	DIFFOUT_B113p	AW13	DQ15B	DQ7B							
3D	VREFB3D0	IO					AG15									
3D	VREFB3D0	IO					AH15	DQ15B	DQ7B							
3D	VREFB3D0	IO			DIFFO_RX_B114n	DIFFOUT_B114n	AT15	DQ15B	DQ7B							
3D	VREFB3D0	IO			DIFFO_RX_B114p	DIFFOUT_B114p	AU15	DQ15B	DQ7B							
3D	VREFB3D0	IO			DIFFO_TX_B115n	DIFFOUT_B115n	AC15	DQ15B	DQ7B							
3D	VREFB3D0	IO			DIFFO_TX_B115p	DIFFOUT_B115p	AD14	DQ16B	DQ7B							
3D	VREFB3D0	IO			DIFFO_RX_B116n	DIFFOUT_B116n	AT14	DQ16B	DQ7B							
3D	VREFB3D0	IO			DIFFO_RX_B116p	DIFFOUT_B116p	AU14	DQ1								





Bank Number	VREF	PinName/Function (Z1 (3))	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DQS3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
GXB_R0		GXB_TX_R5p					AF3									
GXB_R0		GXB_TX_R5n					AF4									
GXB_R0		REFCLK19p					AB9									
GXB_R0		REFCLK19n					AB8									
GXB_R1		REFCLK29p					AB9									
GXB_R1		REFCLK29n					AB8									
GXB_R1		GXB_RX_R6p.GXB_REFCLK_R6n					AE2									
GXB_R1		GXB_RX_R6p.GXB_REFCLK_R6p					AE1									
GXB_R1		GXB_TX_R6p					AD3									
GXB_R1		GXB_TX_R6n					AE4									
GXB_R1		GXB_RX_R7n.GXB_REFCLK_R7n					AC2									
GXB_R1		GXB_RX_R7p.GXB_REFCLK_R7p					AC1									
GXB_R1		GXB_TX_R7p					AB3									
GXB_R1		GXB_TX_R7n					AB4									
GXB_R1		GXB_RX_R8n.GXB_REFCLK_R8n					AA2									
GXB_R1		GXB_RX_R8p.GXB_REFCLK_R8p					AA1									
GXB_R1		GXB_TX_R8p					Y3									
GXB_R1		GXB_TX_R8n					Y4									
GXB_R1		GXB_RX_R9n.GXB_REFCLK_R9n					W3									
GXB_R1		GXB_RX_R9p.GXB_REFCLK_R9p					W1									
GXB_R1		GXB_TX_R9p					V3									
GXB_R1		GXB_TX_R9n					V4									
GXB_R1		GXB_RX_R10n.GXB_REFCLK_R10n					U3									
GXB_R1		GXB_RX_R10p.GXB_REFCLK_R10p					U1									
GXB_R1		GXB_TX_R10p					T3									
GXB_R1		GXB_TX_R10n					T4									
GXB_R1		GXB_RX_R11n.GXB_REFCLK_R11n					R2									
GXB_R1		GXB_RX_R11p.GXB_REFCLK_R11p					R1									
GXB_R1		GXB_TX_R11p					P3									
GXB_R1		GXB_TX_R11n					P4									
GXB_R1		REFCLK39p					Y9									
GXB_R1		REFCLK39n					Y8									
GB	VREFBAND_HPS	HPS_DDR					T7				HPS_DM_4	HPS_DM_4				
GB	VREFBAND_HPS	HPS_DDR					R6				HPS_DQ_39	HPS_DQ_39				
GB	VREFBAND_HPS	HPS_DDR					M1				HPS_DQ_37	HPS_DQ_37				
GB	VREFBAND_HPS	HPS_DDR					N1				HPS_DQ_38	HPS_DQ_38				
GB	VREFBAND_HPS	HPS_DDR					M2				HPS_DQ_36	HPS_DQ_36				
GB	VREFBAND_HPS	HPS_DDR					J1				HPS_DQS_4	HPS_DQS_4				
GB	VREFBAND_HPS	HPS_GPI13					K1									
GB	VREFBAND_HPS	HPS_DDR					H1				HPS_DQS#_4	HPS_DQS#_4				
GB	VREFBAND_HPS	HPS_DDR					L4				HPS_DQ_35	HPS_DQ_35				
GB	VREFBAND_HPS	HPS_DDR					F1				HPS_DQ_33	HPS_DQ_33				
GB	VREFBAND_HPS	HPS_DDR					P6				HPS_DQ_34	HPS_DQ_34				
GB	VREFBAND_HPS	HPS_DDR					G1				HPS_DQ_32	HPS_DQ_32				
GB	VREFBAND_HPS	HPS_GPI12					R7									
GB	VREFBAND_HPS	HPS_GPI11					J2									
GB	VREFBAND_HPS	HPS_DDR					D1				HPS_DM_3	HPS_DM_3				
GB	VREFBAND_HPS	HPS_GPI10					K2									
GB	VREFBAND_HPS	HPS_DDR					E1				HPS_DQ_31	HPS_DQ_31				
GB	VREFBAND_HPS	HPS_DDR					I2				HPS_DQ_29	HPS_DQ_29				
GB	VREFBAND_HPS	HPS_DDR					M3				HPS_DQ_30	HPS_DQ_30				
GB	VREFBAND_HPS	HPS_DDR					G2				HPS_DQ_28	HPS_DQ_28				
GB	VREFBAND_HPS	VREFBAND_HPS					MA									
GB	VREFBAND_HPS	HPS_DDR					C2				HPS_DQS_3	HPS_DQS_3				
GB	VREFBAND_HPS	HPS_GPI9					B1									
GB	VREFBAND_HPS	HPS_DDR					D2				HPS_DQS#_3	HPS_DQS#_3				
GB	VREFBAND_HPS	HPS_DDR					C1				HPS_DQ_27	HPS_DQ_27				
GB	VREFBAND_HPS	HPS_DDR					A3				HPS_DQ_25	HPS_DQ_25				
GB	VREFBAND_HPS	HPS_DDR					P7				HPS_DQ_26	HPS_DQ_26				
GB	VREFBAND_HPS	HPS_DDR					A2				HPS_DQ_24	HPS_DQ_24				
GB	VREFBAND_HPS	HPS_GPI7					K3									
GB	VREFBAND_HPS	HPS_DDR					D3				HPS_DM_2	HPS_DM_2				
GB	VREFBAND_HPS	HPS_GPI6					K4									
GB	VREFBAND_HPS	HPS_DDR					C3				HPS_DQ_23	HPS_DQ_23				
GB	VREFBAND_HPS	HPS_DDR					J4				HPS_DQ_21	HPS_DQ_21				
GB	VREFBAND_HPS	HPS_DDR					M5				HPS_DQ_22	HPS_DQ_22				
GB	VREFBAND_HPS	HPS_DDR					H3				HPS_DQ_20	HPS_DQ_20				
GB	VREFBAND_HPS	HPS_GPI8					L4									
GB	VREFBAND_HPS	HPS_DDR					G4				HPS_DQS_2	HPS_DQS_2				
GB	VREFBAND_HPS	HPS_DDR					E3				HPS_RESET#	HPS_RESET#				
GB	VREFBAND_HPS	HPS_DDR					H5				HPS_DQ_13	HPS_DQ_13				
GB	VREFBAND_HPS	HPS_DDR					F3				HPS_DQS#_2	HPS_DQS#_2				
GB	VREFBAND_HPS	HPS_DDR					C4				HPS_DQ_19	HPS_DQ_19				
GB	VREFBAND_HPS	HPS_DDR					K5				HPS_DQ_17	HPS_DQ_17				
GB	VREFBAND_HPS	HPS_DDR					N7				HPS_DQ_18	HPS_DQ_18				
GB	VREFBAND_HPS	HPS_DDR					J5				HPS_DQ_16	HPS_DQ_16				
GB	VREFBAND_HPS	HPS_GPI4					M6									
GA	VREFBAND_HPS	HPS_GPI3					C4									
GA	VREFBAND_HPS	HPS_DDR					E4				HPS_DM_1	HPS_DM_1				
GA	VREFBAND_HPS	HPS_GPI2					B4									
GA	VREFBAND_HPS	HPS_DDR					F4				HPS_DQ_15	HPS_DQ_15				
GA	VREFBAND_HPS	HPS_DDR					K5				HPS_DQ_13	HPS_DQ_13				
GA	VREFBAND_HPS	HPS_DDR					R9				HPS_DQ_14	HPS_DQ_14				
GA	VREFBAND_HPS	HPS_DDR					A4				HPS_DQ_12	HPS_DQ_12				
GA	VREFBAND_HPS	HPS_DDR					R8				HPS_CKE_0	HPS_CKE_0				
GA	VREFBAND_HPS	HPS_DDR					D5				HPS_DQS_1	HPS_DQS_1				
GA	VREFBAND_HPS	HPS_DDR					F5				HPS_CKE_1	HPS_CKE_1				
GA	VREFBAND_HPS	HPS_DDR					E6				HPS_DQS#_1	HPS_DQS#_1				
GA	VREFBAND_HPS	HPS_DDR					G5				HPS_DQ_11	HPS_DQ_11				
GA	VREFBAND_HPS	HPS_DDR					G6				HPS_DQ_9	HPS_DQ_9				
GA	VREFBAND_HPS	HPS_DDR					N8				HPS_DQ_10	HPS_DQ_10				
GA	VREFBAND_HPS	HPS_DDR					H6				HPS_DQ_8	HPS_DQ_8				
GA	VREFBAND_HPS	HPS_GPI1					M7									
GA	VREFBAND_HPS	HPS_GPI0					B8									
GA	VREFBAND_HPS	HPS_DDR					C6				HPS_DM_0	HPS_DM_0				
GA	VREFBAND_HPS	HPS_DDR					D6				HPS_DQ_7	HPS_DQ_7				
GA	VREFBAND_HPS	HPS_DDR					A7				HPS_DQ_5	HPS_DQ_5				
GA	VREFBAND_HPS	HPS_DDR					L6				HPS_DQ_6	HPS_DQ_6				
GA	VREFBAND_HPS	HPS_DDR					L6				HPS_DQ_4	HPS_DQ_4				
GA	VREFBAND_HPS	HPS_DDR					A6				HPS_DQ_4	HPS_DQ_4				
GA	VREFBAND_HPS	HPS_DDR					K6				HPS_ODT_1	HPS_ODT_1				
GA	VREFBAND_HPS	HPS_DDR					F7				HPS_DQS_0	HPS_DQS_0				
GA	VREFBAND_HPS	HPS_DDR					H7				HPS_ODT_0	HPS_ODT_0				
GA	VREFBAND_HPS	HPS_DDR					E7				HPS_DQS#_0	HPS_DQS#_0				
GA	VREFBAND_HPS	HPS_DDR					C7				HPS_DQ_3	HPS_DQ_3				
GA	VREFBAND_HPS	HPS_DDR					C7				HPS_DQ_1	HPS_DQ_1				
GA	VREFBAND_HPS	HPS_DDR					R10				HPS_DQ_2	HPS_DQ_2				
GA	VREFBAND_HPS	HPS_DDR					D7				HPS_DQ_0	HPS_DQ_0				
GA	VREFBAND_HPS	VREFBAND_HPS					P10									
GA	VREFBAND_HPS	HPS_DDR					N9				HPS_A_0	HPS_CA_0				
GA	VREFBAND_HPS	HPS_DDR					M9				HPS_A_1	HPS_CA_1				
GA	VREFBAND_HPS	HPS_DDR					A8				HPS_A_4	HPS_CA_4				
GA	VREFBAND_HPS	HPS_DDR					N10				HPS_A_2	HPS_CA_2				
GA	VREFBAND_HPS	HPS_DDR					B7				HPS_A_5	HPS_CA_5				
GA	VREFBAND_HPS	HPS_DDR					M10				HPS_A_3	HPS_CA_3				
GA	VREFBAND_HPS	HPS_DDR					A11				HPS_CK	HPS_CK				
GA	VREFBAND_HPS	HPS_DDR					B9				HPS_A_6	HPS_CA_6				
GA	VREFBAND_HPS	HPS_DDR					B10				HPS_CK#	HPS_CK#				
GA	VREFBAND_HPS	HPS_DDR					A9				HPS_A_7	HPS_CA_7				
GA	VREFBAND_HPS	HPS_DDR					C9				HPS_BA_1	HPS_BA_1				
GA	VREFBAND_HPS	HPS_DDR					L7				HPS_BA_0	HPS_BA_0				



Pin Information for the Arria® V 5ASXFB3 Device  
Version 1.3  
Note (1)

Bank Number	VREF	PinName/Function (Z1, Z)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for BDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
6A	VREFB6A0	HPS_DDR					D8				HPS_BA_2					
6A	VREFB6A0	HPS_DDR					S9				HPS_CAS#					
6A	VREFB6A0	HPS_DDR					S8				HPS_RAS#					
6A	VREFB6A0	HPS_DDR					6A				HPS_A_8	HPS_CA_8				
6A	VREFB6A0	HPS_DDR					K7				HPS_A_9					
6A	VREFB6A0	HPS_DDR					C10				HPS_A_9	HPS_CA_9				
6A	VREFB6A0	HPS_DDR					J				HPS_A_11					
6A	VREFB6A0	HPS_DDR					H9				HPS_CS#_0	HPS_CS#_0				
6A	VREFB6A0	HPS_DDR					F9				HPS_A_12					
6A	VREFB6A0	HPS_DDR					JF				HPS_CS#_1	HPS_CS#_1				
6A	VREFB6A0	HPS_DDR					E9				HPS_A_13					
6A	VREFB6A0	HPS_DDR					D11				HPS_A_14					
6A	VREFB6A0	HPS_DDR					J8				HPS_W#					
6A	VREFB6A0	HPS_RZQ_0					D10				HPS_A_15					
		DN1					K9									
		GND					B12									
		GND					C11									
		GND					A12									
		HPS_HRST					R11									
7A		HPS_IPOR					K10									
7A		HPS_TDO					T11									
		ICCRSTCLK_HPS					J10									
		HPS_TMS					F10									
7A		HPS_TCK					G10									
7A		HPS_IRST					P11									
7A		HPS_TX					H10									
		GND					M11									
7A		HPS_PORSEL					C12									
7A		HPS_CLK1					N11									
7A		HPS_CLK2					D12									
7A	VREFB7A7	TRACE_CLK					J11						TRACE_CLK			HPS_GPIO48
7A	VREFB7A7	TRACE_D0					K12						TRACE_D0	SPIS0_CLK	UART0_RX	HPS_GPIO49
7A	VREFB7A7	TRACE_D1					K11						TRACE_D1	SPIS0_MOSI	UART0_TX	HPS_GPIO50
7A	VREFB7A7	TRACE_D2					J12						TRACE_D2	SPIS0_MISO	DCI_SDA	HPS_GPIO51
7A	VREFB7A7	TRACE_D3					H12						TRACE_D3	SPIS0_SSI	DCI_SCL	HPS_GPIO52
7A	VREFB7A7	TRACE_D4					E12						TRACE_D4	SPIS1_CLK		HPS_GPIO53
7A	VREFB7A7	TRACE_D5					G11						TRACE_D5	SPIS1_MOSI		HPS_GPIO54
7A	VREFB7A7	TRACE_D6					F12						TRACE_D6	SPIS1_SSI	DCI_SDA	HPS_GPIO55
7A	VREFB7A7	TRACE_D7					A13						TRACE_D7	SPIS1_MISO	DCI_SCL	HPS_GPIO56
7A	VREFB7A7	SPIM0_CLK					P12						SPIM0_CLK	DCI_SDA	UART0_CTS	HPS_GPIO57
7A	VREFB7A7	SPIM0_MOSI					A14						SPIM0_MOSI	DCI_SCL	UART0_RTS	HPS_GPIO58
7A	VREFB7A7	SPIM0_MISO					N12						SPIM0_MISO		UART1_CTS	HPS_GPIO59
7A	VREFB7A7	SPIM0_SSD_BOOTSEL0					B15						SPIM0_SSD		UART1_RTS	HPS_GPIO60
7A	VREFB7A7	UART0_RX					B14						UART0_RX		SPIM0_SSI	HPS_GPIO61
7A	VREFB7A7	UART0_TX					A15						UART0_TX		SPM1_SSI	HPS_GPIO62
7A	VREFB7A7	DCI_SDA					C13						DCI_SDA	UART1_RX	SPM1_CLK	HPS_GPIO63
7A	VREFB7A7	DCI_SCL					L13						DCI_SCL	UART1_TX	SPM1_MOSI	HPS_GPIO64
7A	VREFB7A7	UART0_RX*					M12						UART0_RX		SPM1_MISO	HPS_GPIO65
7A	VREFB7A7	UART0_TX* CLKSEL0					M13						UART0_TX		SPM1_SSD	HPS_GPIO66
7A	VREFB7A7	SPIS1_CLK					L12						SPIS1_CLK		SPM1_CLK	HPS_GPIO67
7A	VREFB7A7	SPIS1_MOSI					K13						SPIS1_MOSI		SPM1_MOSI	HPS_GPIO68
7A	VREFB7A7	SPIS1_MISO					F13						SPIS1_MISO		SPM1_MISO	HPS_GPIO69
7A	VREFB7A7	SPIS1_SSD					D13						SPIS1_SSD		SPM1_SSD	HPS_GPIO70
7A	VREFB7A7	UART1_RX					H13						UART1_RX		SPM1_SSI	HPS_GPIO71
7A	VREFB7A7	UART1_TX					G13						UART1_TX		SPM1_CLK	HPS_GPIO72
7A	VREFB7A7	DCI_SDA					R13						DCI_SDA	SPIM0_MOSI		HPS_GPIO73
7A	VREFB7A7	DCI_SCL					M14						DCI_SCL	SPIM0_MISO		HPS_GPIO74
7A	VREFB7A7	SPIM0_SSD					H13						SPIM0_SSD		SPM1_SSD	HPS_GPIO75
7A	VREFB7A7	SPIS0_CLK					P13						SPIS0_CLK		SPM1_SSI	HPS_GPIO76
7A	VREFB7A7	SPIS0_MOSI					C14						SPIS0_MOSI			HPS_GPIO77
7A	VREFB7A7	SPIS0_MISO					J13						SPIS0_MISO			HPS_GPIO78
7A	VREFB7A7	SPIS0_SSD					D14						SPIS0_SSD			HPS_GPIO79
7B	VREFB7A7	NAND_A1E					A16						NAND_A1E	RGMI1_TX_CLK	OSPI_S3	HPS_GPIO14
7B	VREFB7A7	NAND_CE					P16						NAND_CE	RGMI1_TXD0	USB1_D0	HPS_GPIO15
7B	VREFB7A7	NAND_C1E					A17						NAND_C1E	RGMI1_TXD1	USB1_D1	HPS_GPIO16
7B	VREFB7A7	NAND_RE					R16						NAND_RE	RGMI1_TXD2	USB1_D2	HPS_GPIO17
7B	VREFB7A7	NAND_RB					C16						NAND_RB	RGMI1_TXD3	USB1_D3	HPS_GPIO18
7B	VREFB7A7	NAND_DQ0					G14						NAND_DQ0	RGMI1_RXD0		HPS_GPIO19
7B	VREFB7A7	NAND_DQ1					C17						NAND_DQ1	RGMI1_MDI0	DCI_SDA	HPS_GPIO20
7B	VREFB7A7	NAND_DQ2					H14						NAND_DQ2	RGMI1_MDC	DCI_SCL	HPS_GPIO21
7B	VREFB7A7	NAND_DQ3					L15						NAND_DQ3	RGMI1_RX_CTL	USB1_D4	HPS_GPIO22
7B	VREFB7A7	NAND_DQ4					P14						NAND_DQ4	RGMI1_TX_CTL	USB1_D5	HPS_GPIO23
7B	VREFB7A7	NAND_DQ6					K15						NAND_DQ6	RGMI1_RX_CLK	USB1_D6	HPS_GPIO24
7B	VREFB7A7	NAND_DQ6					R14						NAND_DQ6	RGMI1_RXD1	USB1_D7	HPS_GPIO25
7B	VREFB7A7	NAND_DQ7					K14						NAND_DQ7	RGMI1_RXD2		HPS_GPIO26
7B	VREFB7A7	NAND_WP					C15						NAND_WP	RGMI1_RXD3	OSPI_S2	HPS_GPIO27
7B	VREFB7A7	NAND_WE_BOOTSEL2					L14						NAND_WE	OSPI_S1		HPS_GPIO28
7B	VREFB7A7	OSPI_I0					D15						OSPI_I0		USB1_CLK	HPS_GPIO29
7B	VREFB7A7	OSPI_I1					S15						OSPI_I1		USB1_STP	HPS_GPIO30
7B	VREFB7A7	OSPI_I02					M15						OSPI_I02		USB1_DR	HPS_GPIO31
7B	VREFB7A7	OSPI_I03					H15						OSPI_I03		USB1_NXT	HPS_GPIO32
7B	VREFB7A7	OSPI_S0					C17						OSPI_S0			HPS_GPIO33
7B	VREFB7A7	OSPI_CLK					F16						OSPI_CLK			HPS_GPIO34
7B	VREFB7A7	OSPI_S1					E15						OSPI_S1			HPS_GPIO35
7C	VREFB7A7	SDMMC_CMD					D16						SDMMC_CMD	USB0_D0		HPS_GPIO36
7C	VREFB7A7	SDMMC_PWREN					P16						SDMMC_PWREN	USB0_D1		HPS_GPIO37
7C	VREFB7A7	SDMMC_D0					C17						SDMMC_D0	USB0_D2		HPS_GPIO38
7C	VREFB7A7	SDMMC_D1					N16						SDMMC_D1	USB0_D3		HPS_GPIO39
7C	VREFB7A7	SDMMC_D4					F16						SDMMC_D4	USB0_D4		HPS_GPIO40
7C	VREFB7A7	SDMMC_D5					G16						SDMMC_D5	USB0_D5		HPS_GPIO41
7C	VREFB7A7	SDMMC_D6					E16						SDMMC_D6	USB0_D6		HPS_GPIO42
7C	VREFB7A7	SDMMC_D7					H16						SDMMC_D7	USB0_D7		HPS_GPIO43
7C	VREFB7A7	HPS_GPI04					K16						HPS_GPI04	USB0_STP		HPS_GPIO44
7C	VREFB7A7	SDMMC_CLK_OUT					L16						SDMMC_CLK_OUT	USB0_CLK		HPS_GPIO45
7C	VREFB7A7	SDMMC_D2					J16						SDMMC_D2	USB0_DR		HPS_GPIO46
7C	VREFB7A7	SDMMC_D3					M16						SDMMC_D3	USB0_NXT		HPS_GPIO47
7D	VREFB7A7	RGMI0_TX_CLK					R17						RGMI0_TX_CLK			HPS_GPIO48
7D	VREFB7A7	RGMI0_TXD0					F17						RGMI0_TXD0	USB1_D0		HPS_GPIO1
7D	VREFB7A7	RGMI0_TXD1					P17						RGMI0_TXD1	USB1_D1		HPS_GPIO2
7D	VREFB7A7	RGMI0_TXD2					F18						RGMI0_TXD2	USB1_D2		HPS_GPIO3
7D	VREFB7A7	RGMI0_TXD3					E17						RGMI0_TXD3	USB1_D3		HPS_GPIO4
7D	VREFB7A7	RGMI0_RXD0					J17						RGMI0_RXD0	USB1_D4		HPS_GPIO5
7D	VREFB7A7	RGMI0_MDI0					D18						RGMI0_MDI0	USB1_D5	DCI_SDA	HPS_GPIO6
7D	VREFB7A7	RGMI0_MDC					C17						RGMI0_MDC	USB1_D6	DCI_SCL	HPS_GPIO7
7D	VREFB7A7	RGMI0_RX_CTL					B19						RGMI0_RX_CTL	USB1_D7		HPS_GPIO8
7D	VREFB7A7	RGMI0_TX_CTL					A18						RGMI0_TX_CTL			HPS_GPIO9
7D	VREFB7A7	RGMI0_RX_CLK					C18						RGMI0_RX_CLK	USB1_CLK		HPS_GPIO10
7D	VREFB7A7	RGMI0_RXD1					A19						RGMI0_RXD1	USB1_STP		HPS_GPIO11
7D	VREFB7A7	RGMI0_RXD2					C19						RGMI0_RXD2	USB1_DR		HPS_GPIO12
7D	VREFB7A7	RGMI0_RXD3					D19						RGMI0_RXD3	USB1_NXT		HPS_GPIO13
7D	VREFB7A7	RGMI1_TX_CLK					D19						RGMI1_TX_CLK			HPS_GPIO48
7D	VREFB7A7	RGMI1_TXD0					H18						RGMI1_TXD0			HPS_GPIO49
7D	VREFB7A7	RGMI1_TXD1					F19						RGMI1_TXD1			HPS_GPIO50
7D	VREFB7A7	RGMI1_TX_CTL					N18						RGMI1_TX_CTL			HPS_GPIO51
7D	VREFB7A7	RGMI1_RXD0					E19						RGMI1_RXD0			HPS_GPIO52
7D	VREFB7A7	RGMI1_RXD1					M17						RGMI1_RXD1			HPS_GPIO53
7E	VREFB7A7	RGMI1_MDI0					J18						RGMI1_MDI0	SPIM0_CLK	SPIS0_CLK	HPS_GPIO54
7E	VREFB7A7	RGMI1_MDC					L18									





Pin Information for the Arria® V 5ASXFB3 Device  
Version 1.3  
Note (1)

Bank Number	VREF	PinName/Function (Z1, Z3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DQS3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
ZE		VREFB7A/B7C/D7E/N0_HPS	RGMIH1_RX_CLK				G21						RGMIH1_RX_CLK	SPIS1_CLK	SPIM1_CLK	HPS_GP0D8
ZE		VREFB7A/B7C/D7E/N0_HPS	RGMIH1_RX_CTL				H19						RGMIH1_RX_CTL	SPIS1_MOSI	SPIM1_MOSI	HPS_GP0D9
ZE		VREFB7A/B7C/D7E/N0_HPS	RGMIH1_RXD2				G19						RGMIH1_RXD2	SPIS1_MISO	SPIM1_MISO	HPS_GP0D0
ZE		VREFB7A/B7C/D7E/N0_HPS	RGMIH1_RXD3				G19						RGMIH1_RXD3	SPIS1_SS0	SPIM1_SS0	HPS_GP0D1
ZG		VREFB7G/N0	ID		DIFFRO_RX_T16p	DIFFOUT_T16p	R19									
ZG		VREFB7G/N0	ID		DIFFRO_RX_T16n	DIFFOUT_T16n	T19									
ZG		VREFB7G/N0	ID	VREFB7G/N0			N19									
ZG		VREFB7G/N0	ID				P19									
ZG		VREFB7G/N0	ID		DIFFRO_RX_T17p	DIFFOUT_T17p	U19									
ZG		VREFB7G/N0	ID		DIFFRO_RX_T17n	DIFFOUT_T17n	L20									
ZG		VREFB7G/N0	ID		DIFFRO_TX_T18p	DIFFOUT_T18p	L19									
ZG		VREFB7G/N0	ID		DIFFRO_RX_T19p	DIFFOUT_T19p	P20									
ZG		VREFB7G/N0	ID		DIFFRO_RX_T19n	DIFFOUT_T19n	R20									
ZG		VREFB7G/N0	ID		DIFFRO_TX_T20p	DIFFOUT_T20p	M19									
ZG		VREFB7G/N0	ID		DIFFRO_RX_T21p	DIFFOUT_T21p	L20									
ZG		VREFB7G/N0	ID		DIFFRO_RX_T21n	DIFFOUT_T21n	M20									
ZG		VREFB7G/N0	ID		DIFFRO_RX_T21n	DIFFOUT_T21n	V20									
ZG		VREFB7G/N0	ID				V19									
ZG		VREFB7G/N0	ID				F20									
SD		VREFB8D/N0	ID	CLK19p	DIFFRO_RX_T31p	DIFFOUT_T31p	C20	DQ1T			DQ1T					
SD		VREFB8D/N0	ID	CLK19n	DIFFRO_RX_T31n	DIFFOUT_T31n	D20	DQ1T			DQ1T					
SD		VREFB8D/N0	ID		DIFFRO_TX_T32p	DIFFOUT_T32p	N21	DQ1T			DQ1T					
SD		VREFB8D/N0	ID		DIFFRO_TX_T32n	DIFFOUT_T32n	D21	DQ1T			DQ1T					
SD		VREFB8D/N0	ID	CLK18p	DIFFRO_RX_T33p	DIFFOUT_T33p	H21	DQ1T			DQ1T					
SD		VREFB8D/N0	ID	CLK18n	DIFFRO_RX_T33n	DIFFOUT_T33n	J21	DQ1T			DQ1T					
SD		VREFB8D/N0	ID		DIFFRO_TX_T34p	DIFFOUT_T34p	D21	DQ1T			DQ1T					
SD		VREFB8D/N0	ID		DIFFRO_TX_T34n	DIFFOUT_T34n	E21	DQ1T			DQ1T					
SD		VREFB8D/N0	ID	FPLL_TC_CLKOUT2/FPLL_TC_FBp/FPLL_TC_FB1	DIFFRO_RX_T35p	DIFFOUT_T35p	A20	DQS1TCQ1TCQn1TQKx1T		DQS1TCQ1TCQn1TQKx1T						
SD		VREFB8D/N0	ID	FPLL_TC_CLKOUT3/FPLL_TC_FBn	DIFFRO_RX_T35n	DIFFOUT_T35n	R21	DQS1TCQ1TCQn1TQKx1T		DQS1TCQ1TCQn1TQKx1T						
SD		VREFB8D/N0	ID	FPLL_TC_CLKOUT0/FPLL_TC_CLKOUTp/FPLL_TC_FB0	DIFFRO_TX_T36p	DIFFOUT_T36p	K21	DQ1T			DQ1T					
SD		VREFB8D/N0	ID	FPLL_TC_CLKOUT1/FPLL_TC_CLKOUTn	DIFFRO_TX_T36n	DIFFOUT_T36n	L21	DQ1T			DQ1T					
SD		VREFB8D/N0	ID	CLK17p	DIFFRO_RX_T37p	DIFFOUT_T37p	A22	DQ1T			DQ1T					
SD		VREFB8D/N0	ID	CLK17n	DIFFRO_RX_T37n	DIFFOUT_T37n	A21	DQ1T			DQ1T					
SD		VREFB8D/N0	ID		DIFFRO_TX_T38p	DIFFOUT_T38p	R21	DQ1T			DQ1T					
SD		VREFB8D/N0	ID		DIFFRO_TX_T38n	DIFFOUT_T38n	T21	DQ1T			DQ1T					
SD		VREFB8D/N0	ID	CLK16p	DIFFRO_RX_T39p	DIFFOUT_T39p	B22	DQ2T			DQ2T					
SD		VREFB8D/N0	ID	CLK16n	DIFFRO_RX_T39n	DIFFOUT_T39n	C22	DQ2T			DQ2T					
SD		VREFB8D/N0	ID				J22	DQ2T			DQ2T					
SD		VREFB8D/N0	ID	VREFB8D/N0			H22	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_RX_T40p	DIFFOUT_T40p	E22	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_RX_T40n	DIFFOUT_T40n	F22	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_TX_T41p	DIFFOUT_T41p	A23	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_TX_T41n	DIFFOUT_T41n	A24	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_RX_T42p	DIFFOUT_T42p	C23	DQS2TCQ2TCQn2TQKx2T		DQS2TCQ2TCQn2TQKx2T						
SD		VREFB8D/N0	ID		DIFFRO_RX_T42n	DIFFOUT_T42n	D23	DQS2TCQ2TCQn2TQKx2T		DQS2TCQ2TCQn2TQKx2T						
SD		VREFB8D/N0	ID		DIFFRO_TX_T43p	DIFFOUT_T43p	L22	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_TX_T43n	DIFFOUT_T43n	M22	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_RX_T44p	DIFFOUT_T44p	N22	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_RX_T44n	DIFFOUT_T44n	P22	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_TX_T45p	DIFFOUT_T45p	B22	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_TX_T45n	DIFFOUT_T45n	T22	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_RX_T46p	DIFFOUT_T46p	F23	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_RX_T46n	DIFFOUT_T46n	G23	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_TX_T47p	DIFFOUT_T47p	R23	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_TX_T47n	DIFFOUT_T47n	T23	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_RX_T48p	DIFFOUT_T48p	B24	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_RX_T48n	DIFFOUT_T48n	C24	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_TX_T49p	DIFFOUT_T49p	M23	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_TX_T49n	DIFFOUT_T49n	N23	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_RX_T50p	DIFFOUT_T50p	M24	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_RX_T50n	DIFFOUT_T50n	E24	DQS3TCQ3TCQn3TQKx3T		DQS3TCQ3TCQn3TQKx3T						
SD		VREFB8D/N0	ID		DIFFRO_TX_T51p	DIFFOUT_T51p	J23	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_TX_T51n	DIFFOUT_T51n	K23	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_RX_T52p	DIFFOUT_T52p	F24	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_RX_T52n	DIFFOUT_T52n	G24	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_TX_T53p	DIFFOUT_T53p	H24	DQ2T			DQ2T					
SD		VREFB8D/N0	ID		DIFFRO_TX_T53n	DIFFOUT_T53n	J24	DQ2T			DQ2T					
SC		VREFB8C/N0	ID		DIFFRO_RX_T54p	DIFFOUT_T54p	T26	DQ4T			DQ4T	DQ5_8C_0	DQ5_8C_0			
SC		VREFB8C/N0	ID		DIFFRO_RX_T54n	DIFFOUT_T54n	T26	DQ4T			DQ4T	DQ5_8C_1	DQ5_8C_1			
SC		VREFB8C/N0	ID		DIFFRO_TX_T55p	DIFFOUT_T55p	G25	DQ4T			DQ4T	DQ5_8C_2	DQ5_8C_2			
SC		VREFB8C/N0	ID		DIFFRO_TX_T55n	DIFFOUT_T55n	H25	DQ4T			DQ4T	DQ5_8C_3	DQ5_8C_3			
SC		VREFB8C/N0	ID		DIFFRO_RX_T56p	DIFFOUT_T56p	N24	DQ4T			DQ4T	DQ5_8C_4	DQ5_8C_4			
SC		VREFB8C/N0	ID		DIFFRO_RX_T56n	DIFFOUT_T56n	P24	DQ4T			DQ4T	DQ5_8C_5	DQ5_8C_5			
SC		VREFB8C/N0	ID		DIFFRO_TX_T57p	DIFFOUT_T57p	R24	DQ4T			DQ4T	DQ5_8C_6	DQ5_8C_6			
SC		VREFB8C/N0	ID		DIFFRO_TX_T57n	DIFFOUT_T57n	T24	DQ4T			DQ4T	DQ5_8C_7	DQ5_8C_7			
SC		VREFB8C/N0	ID		DIFFRO_RX_T58p	DIFFOUT_T58p	A25	DQS4TCQ4TCQn4TQKx4T		DQS4TCQ4TCQn4TQKx4T						
SC		VREFB8C/N0	ID		DIFFRO_RX_T58n	DIFFOUT_T58n	B25	DQS4TCQ4TCQn4TQKx4T		DQS4TCQ4TCQn4TQKx4T						
SC		VREFB8C/N0	ID		DIFFRO_TX_T59p	DIFFOUT_T59p	K24	DQ4T			DQ4T	DQ5_8C_8	DQ5_8C_8			
SC		VREFB8C/N0	ID		DIFFRO_TX_T59n	DIFFOUT_T59n	L24	DQ4T			DQ4T	DQ5_8C_9	DQ5_8C_9			
SC		VREFB8C/N0	ID		DIFFRO_RX_T60p	DIFFOUT_T60p	D25	DQ4T			DQ4T	DQ5_8C_6	DQ5_8C_6			
SC		VREFB8C/N0	ID		DIFFRO_RX_T60n	DIFFOUT_T60n	E25	DQ4T			DQ4T	DQ5_8C_7	DQ5_8C_7			
SC		VREFB8C/N0	ID		DIFFRO_TX_T61p	DIFFOUT_T61p	P25	DQ4T			DQ4T	DQ5_8C_1	DQ5_8C_1			
SC		VREFB8C/N0	ID		DIFFRO_TX_T61n	DIFFOUT_T61n	R25	DQ4T			DQ4T	DQ5_8C_2	DQ5_8C_2			
SC		VREFB8C/N0	ID		DIFFRO_RX_T62p	DIFFOUT_T62p	C26	DQ4T			DQ4T	DQ5_8C_0	DQ5_8C_0			
SC		VREFB8C/N0	ID		DIFFRO_RX_T62n	DIFFOUT_T62n	D26	DQ4T			DQ4T	DQ5_8C_1	DQ5_8C_1			
SC		VREFB8C/N0	ID		DIFFRO_RX_T62n	DIFFOUT_T62n	K25	DQ4T			DQ4T	DQ5_8C_2	DQ5_8C_2			
SC		VREFB8C/N0	ID	VREFB8C/N0			L25	DQ4T			DQ4T	DQ5_8C_3	DQ5_8C_3			
SC		VREFB8C/N0	ID		DIFFRO_RX_T63p	DIFFOUT_T63p	R26	DQ4T			DQ4T	DQ5_8C_4	DQ5_8C_4			
SC		VREFB8C/N0	ID		DIFFRO_RX_T63n	DIFFOUT_T63n	T27	DQ4T			DQ4T	DQ5_8C_5	DQ5_8C_5			
SC		VREFB8C/N0	ID		DIFFRO_TX_T64p	DIFFOUT_T64p	A26	DQ4T			DQ4T	DQ5_8C_6	DQ5_8C_6			
SC		VREFB8C/N0	ID		DIFFRO_TX_T64n	DIFFOUT_T64n	A27	DQ4T			DQ4T	DQ5_8C_7	DQ5_8C_7			
SC		VREFB8C/N0	ID		DIFFRO_RX_T65p	DIFFOUT_T65p	M26	DQS5TCQ5TCQn5TQKx5T		DQS5TCQ5TCQn5TQKx5T						
SC		VREFB8C/N0	ID		DIFFRO_RX_T65n	DIFFOUT_T65n	N26	DQS5TCQ5TCQn5TQKx5T		DQS5TCQ5TCQn5TQKx5T						
SC		VREFB8C/N0	ID		DIFFRO_TX_T66p	DIFFOUT_T66p	L26	DQ4T			DQ4T	DQ5_8C_8	DQ5_8C_8			
SC		VREFB8C/N0	ID		DIFFRO_TX_T66n	DIFFOUT_T66n	K26	DQ4T			DQ4T	DQ5_8C_9	DQ5_8C_9			
SC		VREFB8C/N0	ID		DIFFRO_RX_T67p	DIFFOUT_T67p	F26	DQ4T			DQ4T	DQ5_8C_6	DQ5_8C_6			
SC		VREFB8C/N0	ID		DIFFRO_RX_T67n	DIFFOUT_T67n	G26	DQ4T			DQ4T	DQ5_8C_7	DQ5_8C_7			
SC		VREFB8C/N0	ID		DIFFRO_TX_T68p	DIFFOUT_T68p	M25	DQ4T			DQ4T	DQ5_8C_8	DQ5_8C_8			
SC		VREFB8C/N0	ID		DIFFRO_TX_T68n	DIFFOUT_T68n	N25	DQ4T			DQ4T	DQ5_8C_9	DQ5_8C_9			
SC		VREFB8C/N0	ID		DIFFRO_RX_T69p	DIFFOUT_T69p	P27	DQ4T			DQ4T	DQ5_8C_0	DQ5_8C_0			
SC		VREFB8C/N0	ID		DIFFRO_RX_T69n	DIFFOUT_T69n	R27	DQ4T			DQ4T	DQ5_8C_1	DQ5_8C_1			
SC		VREFB8C/N0	ID		DIFFRO_TX_T70p	DIFFOUT_T70p	H27	DQ4T			DQ4T	DQ5_8C_2	DQ5_8C_2			
SC		VREFB8C/N0	ID		DIFFRO_TX_T70n	DIFFOUT_T70n	J27	DQ4T			DQ4T	DQ5_8C_3	DQ5_8C_3			
SC		VREFB8C/N0	ID		DIFFRO_RX_T71p	DIFFOUT_T71p	B27	DQ4T			DQ4T	DQ5_8C_4	DQ5_8C_4			



Bank Number	VREF	PinName/Function (Z1, Z3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
SB	VREFBAND0	I0			DIFFIO_RX_T78n	DIFFOUT_T78n	D28	DQ7T	DQ4T	DQ2T	DQ2_8B_4	DQ2_8B_4				
SB	VREFBAND0	I0			DIFFIO_TX_T80p	DIFFOUT_T80p	F28	DQ7T	DQ4T	DQ2T	DQ2_8B_5	DQ2_8B_5				
SB	VREFBAND0	I0			DIFFIO_RX_T80n	DIFFOUT_T80n	G28									
SB	VREFBAND0	I0			DIFFIO_TX_T82p	DIFFOUT_T82p	R29	DQS17TCQ1TCQn1TQKwH7	DQS4TCQ4TCQn4TQKwH7	DQ2T	DQ2_8B	DQ2_8B				
SB	VREFBAND0	I0			DIFFIO_RX_T81n	DIFFOUT_T81n	T29	DQS8n7TQK7T	DQS4n4TQK4T	DQ2T	DQS2_8B	DQS2_8B				
SB	VREFBAND0	I0			DIFFIO_TX_T82n	DIFFOUT_T82n	J29	DQ7T	DQ4T	DQ2T	DM2_8B	DM2_8B				
SB	VREFBAND0	I0			DIFFIO_RX_T82p	DIFFOUT_T82p	K29									
SB	VREFBAND0	I0			DIFFIO_TX_T83p	DIFFOUT_T83p	M29	DQ7T	DQ4T	DQ2T	DQ2_8B_6	DQ2_8B_6				
SB	VREFBAND0	I0			DIFFIO_RX_T83n	DIFFOUT_T83n	N29	DQ7T	DQ4T	DQ2T	DQ2_8B_7	DQ2_8B_7				
SB	VREFBAND0	I0			DIFFIO_TX_T84p	DIFFOUT_T84p	F29	DQ7T	DQ4T	DQ2T	DQ2_8B_8	DQ2_8B_8				
SB	VREFBAND0	I0			DIFFIO_RX_T84n	DIFFOUT_T84n	G29									
SB	VREFBAND0	I0			DIFFIO_TX_T85p	DIFFOUT_T85p	B28	DQ8T	DQ4T	DQ2T	DO1_8B_0	DO1_8B_0				
SB	VREFBAND0	I0			DIFFIO_RX_T85n	DIFFOUT_T85n	C29	DQ8T	DQ4T	DQ2T	DO1_8B_1	DO1_8B_1				
SB	VREFBAND0	I0	VREFBAND0		R30	DQ8T		DQ4T	DQ2T	DO1_8B_2	DO1_8B_2					
SB	VREFBAND0	I0			DIFFIO_RX_T86p	DIFFOUT_T86p	A29	DQ8T	DQ4T	DQ2T	DO1_8B_3	DO1_8B_3				
SB	VREFBAND0	I0			DIFFIO_TX_T86n	DIFFOUT_T86n	A28	DQ8T	DQ4T	DQ2T	DO1_8B_4	DO1_8B_4				
SB	VREFBAND0	I0			DIFFIO_RX_T87p	DIFFOUT_T87p	L30	DQ8T	DQ4T	DQ2T	DO1_8B_5	DO1_8B_5				
SB	VREFBAND0	I0			DIFFIO_TX_T87n	DIFFOUT_T87n	M30									
SB	VREFBAND0	I0			DIFFIO_RX_T88p	DIFFOUT_T88p	N30	DQS8T/CQ8T/CQn8TQKw8T	DQ4T	DQ2T	DQS1_8B	DQS1_8B				
SB	VREFBAND0	I0			DIFFIO_TX_T88n	DIFFOUT_T88n	P30	DQS8n8TQK8T	DQ4T	DQ2T	DQS1_8B	DQS1_8B				
SB	VREFBAND0	I0			DIFFIO_RX_T89p	DIFFOUT_T89p	J30	DQ8T	DQ4T	DQ2T	DM1_8B	DM1_8B				
SB	VREFBAND0	I0			DIFFIO_TX_T89n	DIFFOUT_T89n	K30									
SB	VREFBAND0	I0			DIFFIO_RX_T90p	DIFFOUT_T90p	D30	DQ8T	DQ4T	DQ2T	DO1_8B_6	DO1_8B_6				
SB	VREFBAND0	I0			DIFFIO_TX_T90n	DIFFOUT_T90n	D29	DQ8T	DQ4T	DQ2T	DO1_8B_7	DO1_8B_7				
SB	VREFBAND0	I0			DIFFIO_RX_T91p	DIFFOUT_T91p	F30	DQ8T	DQ4T	DQ2T	DO1_8B_8	DO1_8B_8				
SB	VREFBAND0	I0			DIFFIO_TX_T91n	DIFFOUT_T91n	G30				RESETB_8A					
SA	VREFBAND0	I0			DIFFIO_RX_T92p	DIFFOUT_T92p	B30	DQ8T	DQ5T		CKE_8A	CKE_8A				
SA	VREFBAND0	I0			DIFFIO_TX_T92n	DIFFOUT_T92n	C30	DQ8T	DQ5T		CKE_8A	CKE_8A				
SA	VREFBAND0	I0			DIFFIO_RX_T93p	DIFFOUT_T93p	E31	DQ8T	DQ5T		CKE_8A_0	CKE_8A_0				
SA	VREFBAND0	I0			DIFFIO_TX_T93n	DIFFOUT_T93n	F31				CKE_8A_1	CKE_8A_1				
SA	VREFBAND0	I0			DIFFIO_RX_T94p	DIFFOUT_T94p	B31	DQ8T	DQ5T		CA_8A_0	CA_8A_0				
SA	VREFBAND0	I0			DIFFIO_TX_T94n	DIFFOUT_T94n	A30	DQ8T	DQ5T		A_8A_1	CA_8A_1				
SA	VREFBAND0	I0			DIFFIO_RX_T95p	DIFFOUT_T95p	A31	DQ8T	DQ5T		A_8A_2	CA_8A_2				
SA	VREFBAND0	I0			DIFFIO_TX_T95n	DIFFOUT_T95n	A32				A_8A_3	CA_8A_3				
SA	VREFBAND0	I0			DIFFIO_RX_T96p	DIFFOUT_T96p	A33	DQS8T/CQ8T/CQn8TQKw8T	DQS5T/CQ5T/CQn5TQKw5T		A_8A_4	CA_8A_4				
SA	VREFBAND0	I0			DIFFIO_TX_T96n	DIFFOUT_T96n	B33	DQS8n8TQK8T	DQS5n5TQK5T		A_8A_5	CA_8A_5				
SA	VREFBAND0	I0			DIFFIO_RX_T97p	DIFFOUT_T97p	H31	DQ8T	DQ5T		A_8A_6	CA_8A_6				
SA	VREFBAND0	I0			DIFFIO_TX_T97n	DIFFOUT_T97n	J31				A_8A_7	CA_8A_7				
SA	VREFBAND0	I0			DIFFIO_RX_T98p	DIFFOUT_T98p	C31	DQ8T	DQ5T		A_8A_8	CA_8A_8				
SA	VREFBAND0	I0			DIFFIO_TX_T98n	DIFFOUT_T98n	D31				A_8A_9	CA_8A_9				
SA	VREFBAND0	I0			DIFFIO_RX_T99p	DIFFOUT_T99p	C32	DQ8T	DQ5T		A_8A_10					
SA	VREFBAND0	I0			DIFFIO_TX_T99n	DIFFOUT_T99n	D32				A_8A_11					
SA	VREFBAND0	I0			DIFFIO_RX_T100p	DIFFOUT_T100p	N31	DQ10T	DQ5T		A_8A_12					
SA	VREFBAND0	I0			DIFFIO_TX_T100n	DIFFOUT_T100n	P31	DQ10T	DQ5T		A_8A_13					
SA	VREFBAND0	I0			DIFFIO_RX_T101p	DIFFOUT_T101p	J32	DQ10T	DQ5T		A_8A_14					
SA	VREFBAND0	I0			DIFFIO_TX_T101n	DIFFOUT_T101n	K32				A_8A_15					
SA	VREFBAND0	I0			DIFFIO_RX_T102p	DIFFOUT_T102p	M32	DQ10T	DQ5T		BA_8A_0					
SA	VREFBAND0	I0			DIFFIO_TX_T102n	DIFFOUT_T102n	N32	DQ10T	DQ5T		BA_8A_1					
SA	VREFBAND0	I0			DIFFIO_RX_T103p	DIFFOUT_T103p	J34	DQ10T	DQ5T		BA_8A_2					
SA	VREFBAND0	I0			DIFFIO_TX_T103n	DIFFOUT_T103n	K34				BASE_8A					
SA	VREFBAND0	I0			DIFFIO_RX_T104p	DIFFOUT_T104p	L33	DQS10T/CQ10T/CQn10TQKw10T	DQ5T		CASE_8A					
SA	VREFBAND0	I0			DIFFIO_TX_T104n	DIFFOUT_T104n	M33	DQS10n10TQK10T	DQ5T		WEF_8A					
SA	VREFBAND0	I0			DIFFIO_RX_T105p	DIFFOUT_T105p	L31	DQ10T	DQ5T		ODT_8A_0	ODT_8A_0				
SA	VREFBAND0	I0			DIFFIO_TX_T105n	DIFFOUT_T105n	M31				ODT_8A_1	ODT_8A_1				
SA	VREFBAND0	I0	CLK23p		DIFFIO_RX_T106p	DIFFOUT_T106p	N34	DQ10T	DQ5T							
SA	VREFBAND0	I0	CLK23n		DIFFIO_TX_T106n	DIFFOUT_T106n	N33	DQ10T	DQ5T							
SA	VREFBAND0	I0			DIFFIO_RX_T107p	DIFFOUT_T107p	L34	DQ10T	DQ5T		CS#_8A_0	CS#_8A_0				
SA	VREFBAND0	I0	CLK22p		DIFFIO_TX_T107n	DIFFOUT_T107n	M34				CS#_8A_1	CS#_8A_1				
SA	VREFBAND0	I0	CLK22n		DIFFIO_RX_T108p	DIFFOUT_T108p	E34	DQ11T								
SA	VREFBAND0	I0	CLK22n		DIFFIO_TX_T108n	DIFFOUT_T108n	F34	DQ11T								
SA	VREFBAND0	I0		VREFBAND0		J33	DQ11T									
SA	VREFBAND0	I0				H33										
SA	VREFBAND0	I0	FPLL_TL_CLKOUT2_FPLL_TL_FBn_FPLL_TL_FB1		DIFFIO_RX_T109p	DIFFOUT_T109p	B34	DQ11T								
SA	VREFBAND0	I0	FPLL_TL_CLKOUT3_FPLL_TL_FBn		DIFFIO_TX_T109n	DIFFOUT_T109n	A35	DQ11T								
SA	VREFBAND0	I0	FPLL_TL_CLKOUT0_FPLL_TL_CLKOUT5_FPLL_TL_FB0		DIFFIO_RX_T110p	DIFFOUT_T110p	C33	DQ11T								
SA	VREFBAND0	I0	FPLL_TL_CLKOUT1_FPLL_TL_CLKOUT6		DIFFIO_TX_T110n	DIFFOUT_T110n	D33									
SA	VREFBAND0	I0	CLK21p		DIFFIO_RX_T111p	DIFFOUT_T111p	G34	DQS11T/CQ11T/CQn11TQKw11T								
SA	VREFBAND0	I0	CLK21n		DIFFIO_TX_T111n	DIFFOUT_T111n	H34	DQS11n11TQK11T								
SA	VREFBAND0	I0			DIFFIO_RX_T112p	DIFFOUT_T112p	F32	DQ11T								
SA	VREFBAND0	I0			DIFFIO_TX_T112n	DIFFOUT_T112n	G32									
SA	VREFBAND0	I0	CLK20p		DIFFIO_RX_T113p	DIFFOUT_T113p	D34	DQ11T								
SA	VREFBAND0	I0	CLK20n		DIFFIO_TX_T113n	DIFFOUT_T113n	D34	DQ11T								
SA	VREFBAND0	I0		R20_6	DIFFIO_RX_T114p	DIFFOUT_T114p	E33	DQ11T								
SA	VREFBAND0	I0			DIFFIO_TX_T114n	DIFFOUT_T114n	F33									
SA	MSEL0			MSEL0	H35											
SA	MSEL1			MSEL1	A34											
SA	MSEL2			MSEL2	D35											
SA	MSEL3			MSEL3	A37											
SA	MSEL4			MSEL4	P34											
SA	CONF_DONE			CONF_DONE	K35											
SA	INSTATIS			INSTATIS	F35											
SA	HCE			HCE	M35											
SA	ACONFIG			ACONFIG	A36											
SA					P35											
SA	VCC_HPS				V16											
SA	GND				W16											
SA	GND				AA33											
SA	GND				AA35											
SA	GND				AA38											
SA	GND				AA39											
SA	GND				AB31											
SA	GND				AB32											
SA	GND				AB34											
SA	GND				AB36											
SA	GND				AB37											
SA	GND				AC33											
SA	GND				AC38											
SA	GND				AC39											
SA	GND				AD32											
SA	GND				AD36											
SA	GND				AD37											
SA	GND				AE33											
SA	GND				AE35											
SA	GND				AE38											
SA	GND				AE39											
SA	GND				AF31											
SA	GND				AF32											
SA	GND				AF34											
SA	GND				AF36											
SA	GND				AF37											
SA	GND				AG38											
SA	GND				AG39											
SA	GND				AH32											
SA	GND				A											



Bank Number	VREF	PinName/Function (Z1) (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for BDRK3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					AJ38									
		GND					AJ99									
		GND					AK36									
		GND					AK37									
		GND					AL35									
		GND					AL38									
		GND					AL39									
		GND					AM36									
		GND					AM37									
		GND					AN35									
		GND					AN38									
		GND					AN39									
		GND					AP36									
		GND					AP37									
		GND					AR35									
		GND					AR38									
		GND					AR39									
		GND					AT36									
		GND					AT37									
		GND					AL35									
		GND					AU38									
		GND					AU39									
		GND					AV36									
		GND					AV37									
		GND					AV38									
		GND					AV39									
		GND					AW35									
		GND					AW38									
		GND					B36									
		GND					B37									
		GND					C36									
		GND					C38									
		GND					C39									
		GND					D36									
		GND					D37									
		GND					E35									
		GND					E38									
		GND					E39									
		GND					F36									
		GND					F37									
		GND					G35									
		GND					G38									
		GND					G39									
		GND					H36									
		GND					H37									
		GND					J35									
		GND					J38									
		GND					J39									
		GND					K36									
		GND					K37									
		GND					L35									
		GND					L38									
		GND					L39									
		GND					M36									
		GND					M37									
		GND					N35									
		GND					N38									
		GND					N39									
		GND					P36									
		GND					P37									
		GND					R34									
		GND					R38									
		GND					R39									
		GND					T32									
		GND					T36									
		GND					T37									
		GND					U33									
		GND					U36									
		GND					U38									
		GND					U39									
		GND					V32									
		GND					V34									
		GND					V36									
		GND					V37									
		GND					W33									
		GND					W38									
		GND					W39									
		GND					Y31									
		GND					Y32									
		GND					Y36									
		GND					Y37									
		GND					AA3									
		GND					AA4									
		GND					AA6									
		GND					AA8									
		GND					AB1									
		GND					AB2									
		GND					AB7									
		GND					AC3									
		GND					AC4									
		GND					AC5									
		GND					AD1									
		GND					AD2									
		GND					AD5									
		GND					AD7									
		GND					AE3									
		GND					AE4									
		GND					AE6									
		GND					AE8									
		GND					AF1									
		GND					AF2									
		GND					AF9									
		GND					AG3									
		GND					AG4									
		GND					AG5									
		GND					AG6									
		GND					AG7									
		GND					AG8									
		GND					AH1									
		GND					AH2									
		GND					AH5									
		GND					AJ3									
		GND					AJ4									
		GND					AK1									
		GND					AK2									
		GND					AK5									
		GND					AL3									
		GND					AL4									
		GND					AM1									



Bank Number	VREF	PinName/Function (2) (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for BDRK3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					AM2									
		GND					AM5									
		GND					AN3									
		GND					AN4									
		GND					AP1									
		GND					AP2									
		GND					AP5									
		GND					AR3									
		GND					AR4									
		GND					AT1									
		GND					AT2									
		GND					AT5									
		GND					AU3									
		GND					AU4									
		GND					AV1									
		GND					AV2									
		GND					N3									
		GND					N4									
		GND					P1									
		GND					P2									
		GND					P5									
		GND					R3									
		GND					R4									
		GND					R5									
		GND					T1									
		GND					T2									
		GND					T5									
		GND					U3									
		GND					U4									
		GND					U5									
		GND					U6									
		GND					V1									
		GND					V2									
		GND					V7									
		GND					W3									
		GND					W4									
		GND					W8									
		GND					Y1									
		GND					Y2									
		GND					Y5									
		GND					Y7									
		VCCP					AA21									
		VCCP					AA25									
		VCCP					AB15									
		VCCP					U70									
		VCCP					U16									
		VCCP					V26									
		VCCP					V27									
		VCCP					W10									
		VCCP					V27									
		VCCA_FPLL					AC30									
		VCCA_FPLL					AC9									
		VCCA_FPLL					Y30									
		VCCA_FPLL					AA9									
		VCCA_FPLL					V31									
		VCCPLL_HPS					U8									
		VCCBAT					RS3									
		VCC_AUX					AB14									
		VCC_AUX					AB26									
		VCC_AUX					U9									
		VCC_AUX_SHARED					U15									
		VCCD_FPLL					AD31									
		VCCD_FPLL					AE9									
		VCCD_FPLL					W30									
		VCCD_FPLL					W9									
		VCCD_FPLL					T31									
		VCCA_GXBL0					AF33									
		VCCA_GXBR0					AE7									
		VCCA_GXBL1					AB33									
		VCCA_GXBR1					AA7									
		VCCA_GXBL2					V33									
		VCCM_GXBL0					AD33									
		VCCM_GXBR0					AC7									
		VCCM_GXBL1					Y33									
		VCCM_GXBR1					W7									
		VCCM_GXBL2					T33									
		VCCM_GXBR2					AD34									
		VCCM_GXBL0					AD35									
		VCCM_GXBR0					AC5									
		VCCM_GXBR0					AC6									
		VCCM_GXBL1					V34									
		VCCM_GXBR1					Y35									
		VCCM_GXBR1					W5									
		VCCM_GXBR1					W6									
		VCCM_GXBL2					T34									
		VCCM_GXBL2					T35									
		VCCR_GXBL					U34									
		VCCR_GXBL					W34									
		VCCR_GXBL					AA34									
		VCCR_GXBL					AB35									
		VCCR_GXBL					AC35									
		VCCR_GXBL					AE34									
		VCCR_GXBL					AF35									
		VCCR_GXBR					U5									
		VCCR_GXBR					V5									
		VCCR_GXBR					Y5									
		VCCR_GXBR					AB5									
		VCCR_GXBR					AB6									
		VCCM_GXBL0					AG35									
		VCCM_GXBL0					AG34									
		VCCM_GXBR0					AD6									
		VCCM_GXBR0					AE5									
		VCCM_GXBL1					W35									
		VCCM_GXBL1					V35									
		VCCM_GXBR1					AF5									
		VCCM_GXBR1					AF6									
		VCCM_GXBL2					R35									
		VCCM_GXBL2					AC34									
		VCC					AA10									
		VCC					AA12									
		VCC					AA14									
		VCC					AA16									
		VCC					AA18									
		VCC					AA20									
		VCC					AA22									
		VCC					AA24									
		VCC					AA26									
		VCC					AB11									
		VCC					AB17									



Bank Number	VREF	PinName/Function (Z1) (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for BDK3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCC					U18									
		VCC					V17									
		VCC					V22									
		VCC					V23									
		VCC					V29									
		VCC					W20									
		VCC					W18									
		VCC					W22									
		VCC					W24									
		VCC					W26									
		VCC					W28									
		VCC					Y11									
		VCC					Y16									
		VCC					Y17									
		VCC					Y19									
		VCC					Y28									
		VCC					Y26									
		VCC					Y29									
		VCC					Y21									
		VCC_HPS					U12									
		VCC_HPS					V11									
		VCC_HPS					V12									
		VCC_HPS					V13									
		VCC_HPS					V15									
		VCC_HPS					W12									
		VCC_HPS					W14									
		VCC_HPS					Y13									
		VCCIO3A					AK29									
		VCCIO3A					AJ30									
		VCCIO3A					AK35									
		VCCIO3A					AM30									
		VCCIO3A					AP35									
		VCCIO3A					AT35									
		VCCIO3B					AK28									
		VCCIO3B					AL27									
		VCCIO3B					AN28									
		VCCIO3B					AT28									
		VCCIO3C					AL24									
		VCCIO3C					AL25									
		VCCIO3C					AM24									
		VCCIO3C					AP24									
		VCCIO3C					AS24									
		VCCIO3C					AU25									
		VCCIO3D					AJ22									
		VCCIO3D					AL21									
		VCCIO3D					AM22									
		VCCIO3D					AP21									
		VCCIO3D					AS22									
		VCCIO3D					AL21									
		VCCIO4A					AG10									
		VCCIO4A					AJ5									
		VCCIO4A					AL5									
		VCCIO4A					AN5									
		VCCIO4A					AS5									
		VCCIO4A					AU5									
		VCCIO4B					AK13									
		VCCIO4B					AK12									
		VCCIO4B					AN10									
		VCCIO4B					AN13									
		VCCIO4B					AR12									
		VCCIO4C					AT10									
		VCCIO4C					AJ15									
		VCCIO4C					AM15									
		VCCIO4C					AR15									
		VCCIO4C					AV15									
		VCCIO4D					AJ18									
		VCCIO4D					AK18									
		VCCIO4D					AM19									
		VCCIO4D					AN18									
		VCCIO4D					AR19									
		VCCIO4D					AT18									
		VCCIO6A_HPS					AT0									
		VCCIO6A_HPS					CS									
		VCCIO6A_HPS					C8									
		VCCIO6A_HPS					F6									
		VCCIO6A_HPS					F8									
		VCCIO6A_HPS					J6									
		VCCIO6A_HPS					K8									
		VCCIO6A_HPS					M8									
		VCCIO6A_HPS					P8									
		VCCIO6B_HPS					B3									
		VCCIO6B_HPS					D4									
		VCCIO6B_HPS					G3									
		VCCIO6B_HPS					J3									
		VCCIO6B_HPS					L3									
		VCCIO6B_HPS					N2									
		VCCIO6B_HPS					N5									
		VCCIO7A_HPS					B13									
		VCCIO7A_HPS					E10									
		VCCIO7A_HPS					G12									
		VCCIO7A_HPS					K13									
		VCCIO7B_HPS					E14									
		VCCIO7B_HPS					J15									
		VCCIO7B_HPS					D17									
		VCCIO7B_HPS					B18									
		VCCIO7B_HPS					G17									
		VCCIO7B_HPS					J20									
		VCCIO7B					K19									
		VCCIO8A					B35									
		VCCIO8A					G31									
		VCCIO8A					G33									
		VCCIO8A					K31									
		VCCIO8A					K33									
		VCCIO8A					P33									
		VCCIO8B					E28									
		VCCIO8B					E30									
		VCCIO8B					H30									
		VCCIO8B					K28									
		VCCIO8C					C25									
		VCCIO8C					D27									
		VCCIO8C					F25									
		VCCIO8C					G27									
		VCCIO8C					H25									
		VCCIO8C					M24									
		VCCIO8D					C21									
		VCCIO8D					D23									
		VCCIO8D					F21									
		VCCIO8D					G22									
		VCCIO8D					K22									
		VCCIO8D					M21									



Bank Number	VREF	PinName/Function (Z1 (3))	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for BDRK3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCCPD3					AA27									
		VCCPD3					AA28									
		VCCPD3					AA29									
		VCCPD3					AB22									
		VCCPD3					AB23									
		VCCPD3					AB24									
		VCCPD3					AB30									
		VCCPD4A					AC10									
		VCCPD4A					AE10									
		VCCPD4BCD					AB12									
		VCCPD4BCD					AB13									
		VCCPD4BCD					AB16									
		VCCPD4BCD					AB18									
		VCCPD4BCD					AB19									
		VCCPD4AB6_HPS					L9									
		VCCPD4AB6_HPS					T10									
		VCCPD4AB6_HPS					T5									
		VCCPD4AB6_HPS					T8									
		VCCPD7A_HPS					R12									
		VCCPD7B_HPS					T14									
		VCCPD7C_HPS					R16									
		VCCPD7D_HPS					T17									
		VCCPD7E_HPS					R18									
		VCCPD7FG					U21									
		VCCPD8					B32									
		VCCPD8					T30									
		VCCPD8					U22									
		VCCPD8					U24									
		VCCPD8					U26									
		VCCPD8					U29									
		VCCPD8M					J19									
		VCCPD8M					AG29									
		VCCORSTCLK_HPS					L10									
		VCC_HPS					T13									
		VCC_HPS					L14									
		VCC_HPS					U9									
		VCC_HPS					V10									
		VREFB7A/B/C/D7END_HPS					F18									
		GND					AA11									
		GND					AA13									
		GND					AA15									
		GND					AA17									
		GND					AA19									
		GND					AA23									
		GND					AA30									
		GND					AB10									
		GND					AC11									
		GND					AC14									
		GND					AC17									
		GND					AC20									
		GND					AC23									
		GND					AC26									
		GND					AC28									
		GND					AD10									
		GND					AD30									
		GND					AE30									
		GND					AF11									
		GND					AF14									
		GND					AF17									
		GND					AF20									
		GND					AF23									
		GND					AF26									
		GND					AF29									
		GND					AF30									
		GND					AG31									
		GND					AG9									
		GND					AJ11									
		GND					AJ14									
		GND					AJ17									
		GND					AJ20									
		GND					AJ23									
		GND					AJ26									
		GND					AJ29									
		GND					AJ32									
		GND					AJ8									
		GND					AM11									
		GND					AM14									
		GND					AM17									
		GND					AM20									
		GND					AM23									
		GND					AM26									
		GND					AM29									
		GND					AM32									
		GND					AM8									
		GND					AR11									
		GND					AR14									
		GND					AR17									
		GND					AR20									
		GND					AR23									
		GND					AR26									
		GND					AR29									
		GND					AR32									
		GND					AR8									
		GND					AV11									
		GND					AV14									
		GND					AV17									
		GND					AV20									
		GND					AV23									
		GND					AV26									
		GND					AV29									
		GND					AV32									
		GND					AV5									
		GND					AV8									
		GND					B11									
		GND					B16									
		GND					B2									
		GND					B20									
		GND					B23									
		GND					B26									
		GND					B29									
		GND					B32									
		GND					B5									
		GND					B8									
		GND					E11									
		GND					E17									
		GND					E2									
		GND					E20									
		GND					E23									
		GND					E26									
		GND					E29									



Bank Number	VREF	PinName/Function (2) (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DQR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					E32									
		GND					E5									
		GND					E9									
		GND					F14									
		GND					H11									
		GND					H17									
		GND					H5									
		GND					H20									
		GND					H23									
		GND					H26									
		GND					H29									
		GND					H32									
		GND					H5									
		GND					H8									
		GND					J14									
		GND					K20									
		GND					L11									
		GND					L17									
		GND					L2									
		GND					L23									
		GND					L26									
		GND					L29									
		GND					L32									
		GND					L5									
		GND					L8									
		GND					N14									
		GND					N17									
		GND					N20									
		GND					P11									
		GND					P23									
		GND					P26									
		GND					P29									
		GND					P32									
		GND					P8									
		GND					W21									
		GND					T12									
		GND					T15									
		GND					T16									
		GND					T18									
		GND					T20									
		GND					T8									
		GND					U11									
		GND					U13									
		GND					U17									
		GND					U23									
		GND					U25									
		GND					U27									
		GND					U30									
		GND					U7									
		GND					V14									
		GND					V8									
		GND					V18									
		GND					V21									
		GND					V24									
		GND					V26									
		GND					V28									
		GND					V30									
		GND					V8									
		GND					W27									
		GND					W11									
		GND					W13									
		GND					W15									
		GND					W17									
		GND					W19									
		GND					W23									
		GND					W25									
		GND					W29									
		GND					Y10									
		GND					Y12									
		GND					Y14									
		GND					Y16									
		GND					Y18									
		GND					Y20									
		GND					Y22									
		GND					Y24									
		GND					Y26									
		GND					Y28									

Notes:  
(1) For more information about pin definitions and pin connection guidelines, refer to the [Arria V Device Family Pin Connection Guidelines](#).  
(2) GNB\_REFCLK pin is not supported in current Quartus II version, but will be supported in future Quartus II release version.  
(3) Pins with \* contains similar name with other pins in the same column. For the selection of the HPS pins, refer to the "HPS Pin Mux Select x" columns.  
(4) Pins with # are the 10 Gbps transceiver channels. For more information about the 10 Gbps transceiver channels clocking recommendation, refer to the [Transceiver Clocking in Arria V Devices chapter](#).  
(5) RESET pin is only applicable for DQR3 device.



**Pin Information for the Arria® V 5ASXFB3 Device  
Version 1.3**

<b>Version Number</b>	<b>Date</b>	<b>Changes Made</b>
1.0	4/19/2013	Initial release.
1.1	9/30/2014	Remove corresponding bank number from VCCRSTCLK_HPS pin.
1.2	7/31/2015	Renamed the following columns: - Renamed "DDR3/DDR2 hard memory PHY" to "HMC pin assignment for DDR3". - Renamed "LPDDR2 hard memory PHY" to "HMC pin assignment for LPDDR2".
1.3	12/23/2016	-Renamed SDMMC_FB_CLK_IN to HPS_GPIO44.