Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	HMC Pin Assignment for DDR3/DDR2 *(3)*	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
3A		TDO		TDO			U4							
3A		nCSO		DATA4			AA1							
3A		TMS		TMS			V2							
3A		AS_DATA3		DATA3			AB2							
3A		TCK		TCK			W3							
3A		AS_DATA2		DATA2			Y3							
3A		TDI		TDI			W4							
3A		AS_DATA1		DATA1			AA2							
3A		DCLK		DCLK			V4							
3A		AS_DATA0,ASDO		DATA0			AB3							
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	Y5	DQ1B						
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	AB5							
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	W6	DQ1B						
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	AA5	DQ1B						
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	V5	DQSn1B						
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	AB7	DQ1B						
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	U6	DQS1B						
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	AA6							
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	V7	DQ1B						
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	AA7	DQ1B						
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	U7	DQ1B						
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	Y8	DQ1B						
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	W7							
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	W8	DQ1B						
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	V6							
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	V9	DQ1B						
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B31n	DIFFOUT_B31n	V10							
3B	VREFB3BN0	IO	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B31p	DIFFOUT_B31p	U10							
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B37n	DIFFOUT_B37n	AB10							
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B37p	DIFFOUT_B37p	AB9							
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B39n	DIFFOUT_B39n	AB8							
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B39p	DIFFOUT_B39p	AA8							
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B41n	DIFFOUT_B41n	AA11							
4A	VREFB4AN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AB13	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	Y11	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	AB12	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	W11	DQSn2B						
4A	VREFB4AN0	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	AB14	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	V11	DQS2B						
4A	VREFB4AN0	IO			DIFFIO_TX_B44p	DIFFOUT_B44p	AA13							
4A	VREFB4AN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	AB17	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AB15	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	AA16	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	AA15	DQ2B						
4A	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B47n	DIFFOUT_B47n	Y14							
4A	VREFB4AN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	AB20	DQ2B						
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B47p	DIFFOUT_B47p	W14							
4A	VREFB4AN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	AB19	DQ2B						
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B55n	DIFFOUT_B55n	Y13							
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B55p	DIFFOUT_B55p	W12							
4A	VREFB4AN0	IO			DIFFIO_TX_B69n	DIFFOUT_B69n	AB18							
4A	VREFB4AN0	IO			DIFFIO_RX_B70n	DIFFOUT_B70n	Y16							
4A	VREFB4AN0	IO			DIFFIO_TX_B69p	DIFFOUT_B69p	AA18							
4A	VREFB4AN0	IO			DIFFIO_RX_B70p	DIFFOUT_B70p	Y15							
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	Y19	DQ1R						
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	V17							
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	Y20	DQ1R						
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	W18							
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	AA21	DQ1R						
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	U18	DQ1R						
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	Y21	DQ1R						
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	V19	DQ1R						
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	AB22							
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	V16	DQS1R						
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	AA22	DQ1R						
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R6n	U17	DQSn1R						
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	V20	DQ1R						
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	V15	DQ1R						
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	W21							
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	W16	DQ1R						
6B	VREFB6BN0_HPS	HPS_DDR					R18		HPS_DM_3	HPS_DM_3				
6B	VREFB6BN0_HPS	HPS_DDR					T17		HPS_DQ_31	HPS_DQ_31				
6B	VREFB6BN0_HPS	HPS_DDR					P18		HPS_DQ_29	HPS_DQ_29				
6B	VREFB6BN0_HPS	HPS_DDR					T18		HPS_DQ_30	HPS_DQ_30				
6B	VREFB6BN0_HPS	HPS_DDR					P19		HPS_DQ_28	HPS_DQ_28				
6B	VREFB6BN0_HPS	VREFB6BN0_HPS					U20							
6B	VREFB6BN0_HPS	HPS_DDR					M15		HPS_DQS_3	HPS_DQS_3				
6B	VREFB6BN0_HPS	HPS_DDR					N15		HPS_DQS#_3	HPS_DQS#_3				
6B	VREFB6BN0_HPS	HPS_DDR					V22		HPS_DQ_27	HPS_DQ_27				
6B	VREFB6BN0_HPS	HPS_DDR					R15		HPS_DQ_25	HPS_DQ_25				
6B	VREFB6BN0_HPS	HPS_DDR					T20		HPS_DQ_26	HPS_DQ_26				
6B	VREFB6BN0_HPS	HPS_DDR					N17		HPS_DQ_24	HPS_DQ_24				
6B	VREFB6BN0_HPS	HPS_DDR					U19		HPS_DM_2	HPS_DM_2				
6B	VREFB6BN0_HPS	HPS_DDR					R20		HPS_DQ_23	HPS_DQ_23				
6B	VREFB6BN0_HPS	HPS_DDR					N16		HPS_DQ_21	HPS_DQ_21				
6B	VREFB6BN0_HPS	HPS_DDR					V21		HPS_DQ_22	HPS_DQ_22				
6B	VREFB6BN0_HPS	HPS_DDR					P16		HPS_DQ_20	HPS_DQ_20				
6B	VREFB6BN0_HPS	HPS_DDR					N14		HPS_DQS_2	HPS_DQS_2				
6B	VREFB6BN0_HPS	HPS_DDR					W22		HPS_RESET#	HPS_RESET#				
6B	VREFB6BN0_HPS	HPS_DDR					P14		HPS_DQS#_2	HPS_DQS#_2				
6B	VREFB6BN0_HPS	HPS_DDR					U22		HPS_DQ_19	HPS_DQ_19				
6B	VREFB6BN0_HPS	HPS_DDR					M19		HPS_DQ_17	HPS_DQ_17				
6B	VREFB6BN0_HPS	HPS_DDR					R19		HPS_DQ_18	HPS_DQ_18				
6B	VREFB6BN0_HPS	HPS_DDR					M17		HPS_DQ_16	HPS_DQ_16				
6A	VREFB6AN0_HPS	HPS_DDR					T22		HPS_DM_1	HPS_DM_1				
6A	VREFB6AN0_HPS	HPS_DDR					P21		HPS_DQ_15	HPS_DQ_15				
6A	VREFB6AN0_HPS	HPS_DDR					L18		HPS_DQ_13	HPS_DQ_13				
6A	VREFB6AN0_HPS	HPS_DDR					P22		HPS_DQ_14	HPS_DQ_14				
6A	VREFB6AN0_HPS	HPS_DDR					L16		HPS_DQ_12	HPS_DQ_12				
6A	VREFB6AN0_HPS	HPS_DDR					T21		HPS_CKE_0	HPS_CKE_0				
6A	VREFB6AN0_HPS	HPS_DDR					M14		HPS_DQS_1	HPS_DQS_1				
6A	VREFB6AN0_HPS	HPS_DDR					R21		HPS_CKE_1	HPS_CKE_1				
6A	VREFB6AN0_HPS	HPS_DDR					M13		HPS_DQS#_1	HPS_DQS#_1				
6A	VREFB6AN0_HPS	HPS_DDR					N20		HPS_DQ_11	HPS_DQ_11				
6A	VREFB6AN0_HPS	HPS_DDR					K19		HPS_DQ_9	HPS_DQ_9				
6A	VREFB6AN0_HPS	HPS_DDR					N21		HPS_DQ_10	HPS_DQ_10				
6A	VREFB6AN0_HPS	HPS_DDR					K20		HPS_DQ_8	HPS_DQ_8				
6A	VREFB6AN0_HPS	HPS_DDR					M22		HPS_DM_0	HPS_DM_0				
6A	VREFB6AN0_HPS	HPS_DDR					N22		HPS_DQ_7	HPS_DQ_7				
6A	VREFB6AN0_HPS	HPS_DDR					K16		HPS_DQ_5	HPS_DQ_5				
6A	VREFB6AN0_HPS	HPS_DDR					L22		HPS_DQ_6	HPS_DQ_6				
6A	VREFB6AN0_HPS	HPS_DDR					K18		HPS_DQ_4	HPS_DQ_4				
6A	VREFB6AN0_HPS	HPS_DDR					N19		HPS_ODT_1	HPS_ODT_1				
6A	VREFB6AN0_HPS	HPS_DDR					L15		HPS_DQS_0	HPS_DQS_0				

Copyright © 2016 Altera Corp.

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	HMC Pin Assignment for DDR3/DDR2 *(3)*	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
6A	VREFB6AN0_HPS	HPS_DDR					L20		HPS_ODT_0	HPS_ODT_0				
6A	VREFB6AN0_HPS	HPS_DDR					K14		HPS_DQS# 0	HPS_DQS# 0				
6A	VREFB6AN0_HPS	HPS_DDR					K21		HPS_DQ_3	HPS_DQ_3				
6A	VREFB6AN0_HPS	HPS_DDR					J19		HPS_DQ_1	HPS_DQ_1				
6A	VREFB6AN0_HPS	HPS_DDR					M20		HPS_DQ_2	HPS_DQ_2				
6A	VREFB6AN0_HPS	HPS_DDR					J18		HPS_DQ_0	HPS_DQ_0				
6A	VREFB6AN0_HPS	VREFB6AN0_HPS					H19							
6A	VREFB6AN0_HPS	HPS_DDR					L21		HPS_A_0	HPS_CA_0				
6A	VREFB6AN0_HPS	HPS_DDR					J22		HPS_A_1	HPS_CA_1				
6A	VREFB6AN0_HPS	HPS_DDR					H17		HPS_A_4	HPS_CA_4				
6A	VREFB6AN0_HPS	HPS_DDR					J21		HPS_A_2	HPS_CA_2				
6A	VREFB6AN0_HPS	HPS_DDR					G19		HPS_A_5	HPS_CA_5				
6A	VREFB6AN0_HPS	HPS_DDR					H20		HPS_A_3	HPS_CA_3				
6A	VREFB6AN0_HPS	HPS_DDR					K15		HPS_CK	HPS_CK				
6A	VREFB6AN0_HPS	HPS_DDR					H22		HPS_A_6	HPS_CA_6				
6A	VREFB6AN0_HPS	HPS_DDR					J14		HPS_CK#	HPS_CK#				
6A	VREFB6AN0_HPS	HPS_DDR					H21		HPS_A_7	HPS_CA_7				
6A	VREFB6AN0_HPS	HPS_DDR					G20		HPS_BA_1					
6A	VREFB6AN0_HPS	HPS_DDR					G22		HPS_BA_0					
6A	VREFB6AN0_HPS	HPS_DDR					G18		HPS_BA_2					
6A	VREFB6AN0_HPS	HPS_DDR					F20		HPS_CAS#					
6A	VREFB6AN0_HPS	HPS_DDR					F21		HPS_RAS#					
6A	VREFB6AN0_HPS	HPS_DDR					C22		HPS_A_8	HPS_CA_8				
6A	VREFB6AN0_HPS	HPS_DDR					F22		HPS_A_10					
6A	VREFB6AN0_HPS	HPS_DDR					B22		HPS_A_9	HPS_CA_9				
6A	VREFB6AN0_HPS	HPS_DDR					E19		HPS_A_11					
6A	VREFB6AN0_HPS	HPS_DDR					H15		HPS_CS# 0	HPS_CS# 0				
6A	VREFB6AN0_HPS	HPS_DDR					E20		HPS_A_12					
6A	VREFB6AN0_HPS	HPS_DDR					J16		HPS_CS# 1	HPS_CS# 1				
6A	VREFB6AN0_HPS	HPS_DDR					E21		HPS_A_13					
6A	VREFB6AN0_HPS	HPS_DDR					C21		HPS_A_14					
6A	VREFB6AN0_HPS	HPS_DDR					D22		HPS_WE#					
6A	VREFB6AN0_HPS	HPS_DDR					E18		HPS_A_15					
6A	VREFB6AN0_HPS	HPS_RZQ_0					D21							
		GND					G17							
		GND					F17							
7A		HPS_nRST					D18							
7A		HPS_nPOR					E15							
7A		HPS_TDO					B18							
		VCCRSTCLK_HPS					G15							
7A		HPS_TMS					D17							
7A		HPS_TCK					J13							
7A		HPS_TRST					H14							
7A		HPS_TDI					F16							
		GND					F15							
7A		HPS_PORSEL					G14							
7A		HPS_CLK1					C16							
7A		HPS_CLK2					E14							
7A	VREFB7A7B7C7DN0_HPS	TRACE_CLK					B15				TRACE_CLK			HPS_GPIO48
7A	VREFB7A7B7C7DN0_HPS	TRACE_D0					D19				TRACE_D0	SPIS0_CLK	UART0_RX	HPS_GPIO49
7A	VREFB7A7B7C7DN0_HPS	TRACE_D1					C15				TRACE_D1	SPIS0_MOSI	UART0_TX	HPS_GPIO50
7A	VREFB7A7B7C7DN0_HPS	TRACE_D2					C20				TRACE_D2	SPIS0_MISO	I2C1_SDA	HPS_GPIO51
7A	VREFB7A7B7C7DN0_HPS	TRACE_D3					F13				TRACE_D3	SPIS0_SS0	I2C1_SCL	HPS_GPIO52
7A	VREFB7A7B7C7DN0_HPS	TRACE_D4					C19				TRACE_D4	SPIS1_CLK	CAN1_RX	HPS_GPIO53
7A	VREFB7A7B7C7DN0_HPS	TRACE_D5					C14				TRACE_D5	SPIS1_MOSI	CAN1_TX	HPS_GPIO54
7A	VREFB7A7B7C7DN0_HPS	TRACE_D6					B19				TRACE_D6	SPIS1_SS0	I2C0_SDA	HPS_GPIO55
7A	VREFB7A7B7C7DN0_HPS	TRACE_D7					B20				TRACE_D7	SPIS1_MISO	I2C0_SCL	HPS_GPIO56
7A	VREFB7A7B7C7DN0_HPS	SPIM0_CLK					A21				SPIM0_CLK	I2C1_SDA	UART0_CTS	HPS_GPIO57
7A	VREFB7A7B7C7DN0_HPS	SPIM0_MOSI					A22				SPIM0_MOSI	I2C1_SCL	UART0_RTS	HPS_GPIO58
7A	VREFB7A7B7C7DN0_HPS	SPIM0_MISO					A20				SPIM0_MISO	CAN1_RX	UART1_CTS	HPS_GPIO59
7A	VREFB7A7B7C7DN0_HPS	SPIM0_SS0,BOOTSEL0					D14				SPIM0_SS0	CAN1_TX	UART1_RTS	HPS_GPIO60
7A	VREFB7A7B7C7DN0_HPS	UART0_RX					A16				UART0_RX	CAN0_RX	SPIM0_SS1	HPS_GPIO61
7A	VREFB7A7B7C7DN0_HPS	UART0_TX,CLKSEL1					E13				UART0_TX	CAN0_TX	SPIM1_SS1	HPS_GPIO62
7A	VREFB7A7B7C7DN0_HPS	I2C0_SDA					A15				I2C0_SDA	UART1_RX	SPIM1_CLK	HPS_GPIO63
7A	VREFB7A7B7C7DN0_HPS	I2C0_SCL					A18				I2C0_SCL	UART1_TX	SPIM1_MOSI	HPS_GPIO64
7A	VREFB7A7B7C7DN0_HPS	CAN0_RX					B14				CAN0_RX	UART0_RX	SPIM1_MISO	HPS_GPIO65
7A	VREFB7A7B7C7DN0_HPS	CAN0_TX,CLKSEL0					A17				CAN0_TX	UART0_TX	SPIM1_SS0	HPS_GPIO66
7B	VREFB7A7B7C7DN0_HPS	NAND_ALE					J11				NAND_ALE	RGMII1_TX_CLK	QSPI_SS3	HPS_GPIO14
7B	VREFB7A7B7C7DN0_HPS	NAND_CE					J12				NAND_CE	RGMII1_TXD0	USB1_D0	HPS_GPIO15
7B	VREFB7A7B7C7DN0_HPS	NAND_CLE					J9				NAND_CLE	RGMII1_TXD1	USB1_D1	HPS_GPIO16
7B	VREFB7A7B7C7DN0_HPS	NAND_RE					D13				NAND_RE	RGMII1_TXD2	USB1_D2	HPS_GPIO17
7B	VREFB7A7B7C7DN0_HPS	NAND_RB					H12				NAND_RB	RGMII1_TXD3	USB1_D3	HPS_GPIO18
7B	VREFB7A7B7C7DN0_HPS	NAND_DQ0					B13				NAND_DQ0	RGMII1_RXD0		HPS_GPIO19
7B	VREFB7A7B7C7DN0_HPS	NAND_DQ1					H10				NAND_DQ1	RGMII1_MDIO	I2C3_SDA	HPS_GPIO20
7B	VREFB7A7B7C7DN0_HPS	NAND_DQ2					C12				NAND_DQ2	RGMII1_MDC	I2C3_SCL	HPS_GPIO21
7B	VREFB7A7B7C7DN0_HPS	NAND_DQ3					H11				NAND_DQ3	RGMII1_RX_CTL	USB1_D4	HPS_GPIO22
7B	VREFB7A7B7C7DN0_HPS	NAND_DQ4					A13				NAND_DQ4	RGMII1_TX_CTL	USB1_D5	HPS_GPIO23
7B	VREFB7A7B7C7DN0_HPS	NAND_DQ5					G12				NAND_DQ5	RGMII1_RX_CLK	USB1_D6	HPS_GPIO24
7B	VREFB7A7B7C7DN0_HPS	NAND_DQ6					G10				NAND_DQ6	RGMII1_RXD1	USB1_D7	HPS_GPIO25
7B	VREFB7A7B7C7DN0_HPS	NAND_DQ7					E11				NAND_DQ7	RGMII1_RXD2		HPS_GPIO26
7B	VREFB7A7B7C7DN0_HPS	NAND_WP					A12				NAND_WP	RGMII1_RXD3	QSPI_SS2	HPS_GPIO27
7B	VREFB7A7B7C7DN0_HPS	NAND_WE,BOOTSEL2					B12				NAND_WE	QSPI_SS1		HPS_GPIO28
7B	VREFB7A7B7C7DN0_HPS	QSPI_IO0					D11				QSPI_IO0		USB1_CLK	HPS_GPIO29
7B	VREFB7A7B7C7DN0_HPS	QSPI_IO1					D12				QSPI_IO1		USB1_STP	HPS_GPIO30
7B	VREFB7A7B7C7DN0_HPS	QSPI_IO2					F10				QSPI_IO2		USB1_DIR	HPS_GPIO31
7B	VREFB7A7B7C7DN0_HPS	QSPI_IO3					E11				QSPI_IO3		USB1_NXT	HPS_GPIO32
7B	VREFB7A7B7C7DN0_HPS	QSPI_SS0,BOOTSEL1					A11				QSPI_SS0			HPS_GPIO33
7B	VREFB7A7B7C7DN0_HPS	QSPI_CLK					C11				QSPI_CLK			HPS_GPIO34
7C	VREFB7A7B7C7DN0_HPS	IO					G9				SDMMC_CMD			HPS_GPIO36
7C	VREFB7A7B7C7DN0_HPS	IO					E8				SDMMC_PWREN			HPS_GPIO37
7C	VREFB7A7B7C7DN0_HPS	IO					B10				SDMMC_D0			HPS_GPIO38
7C	VREFB7A7B7C7DN0_HPS	IO					A10				SDMMC_D1			HPS_GPIO39
7C	VREFB7A7B7C7DN0_HPS	IO					C10							HPS_GPIO44
7C	VREFB7A7B7C7DN0_HPS	IO					E9				SDMMC_CCLK_OUT			HPS_GPIO45
7C	VREFB7A7B7C7DN0_HPS	IO					F8				SDMMC_D2			HPS_GPIO46
7C	VREFB7A7B7C7DN0_HPS	IO					B9				SDMMC_D3			HPS_GPIO47
7D	VREFB7A7B7C7DN0_HPS	RGMII0_TX_CLK					H7				RGMII0_TX_CLK			HPS_GPIO0
7D	VREFB7A7B7C7DN0_HPS	RGMII0_TXD0					F7				RGMII0_TXD0	USB1_D0		HPS_GPIO1
7D	VREFB7A7B7C7DN0_HPS	RGMII0_TXD1					G7				RGMII0_TXD1	USB1_D1		HPS_GPIO2
7D	VREFB7A7B7C7DN0_HPS	RGMII0_TXD2					A8				RGMII0_TXD2	USB1_D2		HPS_GPIO3
7D	VREFB7A7B7C7DN0_HPS	RGMII0_TXD3					D8				RGMII0_TXD3	USB1_D3		HPS_GPIO4
7D	VREFB7A7B7C7DN0_HPS	RGMII0_RXD0					F6				RGMII0_RXD0	USB1_D4		HPS_GPIO5
7D	VREFB7A7B7C7DN0_HPS	RGMII0_MDIO					A7				RGMII0_MDIO	USB1_D5	I2C2_SDA	HPS_GPIO6
7D	VREFB7A7B7C7DN0_HPS	RGMII0_MDC					C7				RGMII0_MDC	USB1_D6	I2C2_SCL	HPS_GPIO7
7D	VREFB7A7B7C7DN0_HPS	RGMII0_RX_CTL					H6				RGMII0_RX_CTL	USB1_D7		HPS_GPIO8
7D	VREFB7A7B7C7DN0_HPS	RGMII0_TX_CTL					D7				RGMII0_TX_CTL			HPS_GPIO9
7D	VREFB7A7B7C7DN0_HPS	RGMII0_RX_CLK					H9				RGMII0_RX_CLK	USB1_CLK		HPS_GPIO10
7D	VREFB7A7B7C7DN0_HPS	RGMII0_RXD1					B7				RGMII0_RXD1	USB1_STP		HPS_GPIO11
7D	VREFB7A7B7C7DN0_HPS	RGMII0_RXD2					B8				RGMII0_RXD2	USB1_DIR		HPS_GPIO12
7D	VREFB7A7B7C7DN0_HPS	RGMII0_RXD3					E6				RGMII0_RXD3	USB1_NXT		HPS_GPIO13
8A	VREFB8AN0	IO	CLK7p		DIFFIO_RX_T1p	DIFFOUT_T1p	F5							
8A	VREFB8AN0	IO	CLK7n		DIFFIO_RX_T1n	DIFFOUT_T1n	E5							
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T4p	DIFFOUT_T4p	A6							
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T4n	DIFFOUT_T4n	A5							

Copyright © 2016 Altera Corp.

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	HMC Pin Assignment for DDR3/DDR2 *(3)*	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
8A	VREFB8AN0	IO	CLK6p,FPLL_TL_FBp		DIFFIO_RX_T9p	DIFFOUT_T9p	C6							
8A	VREFB8AN0	IO	CLK6n,FPLL_TL_FBn		DIFFIO_RX_T9n	DIFFOUT_T9n	C5							
9A		MSEL0		MSEL0			B4							
9A		CONF_DONE		CONF_DONE			A3							
9A		MSEL1		MSEL1			E4							
9A		nSTATUS		nSTATUS			B3							
9A		nCE		nCE			A2							
9A		MSEL2		MSEL2			A1							
9A		MSEL3		MSEL3			C4							
9A		nCONFIG		nCONFIG			B2							
9A		MSEL4		MSEL4			C2							
		GND					C1							
		GND					A14							
		GND					A4							
		GND					AA14							
		GND					AA4							
		GND					AB1							
		GND					AB11							
		GND					AB21							
		GND					B1							
		GND					B11							
		GND					B21							
		GND					B6							
		GND					C18							
		GND					C3							
		GND					C8							
		GND					D1							
		GND					D15							
		GND					E1							
		GND					E12							
		GND					E2							
		GND					E22							
		GND					E3							
		GND					F14							
		GND					F19							
		GND					F2							
		GND					F3							
		GND					F4							
		GND					F9							
		GND					G1							
		GND					G16							
		GND					G2							
		GND					G4							
		GND					G5							
		GND					G6							
		GND					H13							
		GND					H2							
		GND					H4							
		GND					H5							
		GND					J10							
		GND					J20							
		GND					J3							
		GND					J5							
		GND					J7							
		GND					K1							
		GND					K11							
		GND					K13							
		GND					K17							
		GND					K2							
		GND					K4							
		GND					K6							
		GND					K8							
		GND					K9							
		GND					L10							
		GND					L12							
		GND					L14							
		GND					L2							
		GND					L3							
		GND					L5							
		GND					L7							
		GND					L8							
		GND					M1							
		GND					M11							
		GND					M2							
		GND					M21							
		GND					M4							
		GND					M6							
		GND					M9							
		GND					N1							
		GND					N10							
		GND					N12							
		GND					N18							
		GND					N2							
		GND					N3							
		GND					N5							
		GND					N7							
		GND					N8							
		GND					P11							
		GND					P15							
		GND					P2							
		GND					P4							
		GND					P6							
		GND					P9							
		GND					R1							
		GND					R12							
		GND					R14							
		GND					R2							
		GND					R22							
		GND					R3							
		GND					R5							
		GND					R7							
		GND					R9							
		GND					T1							
		GND					T13							
		GND					T15							
		GND					T19							
		GND					T2							
		GND					T4							
		GND					T6							
		GND					T8							
		GND					U11							
		GND					U12							
		GND					U13							
		GND					U14							

Copyright © 2016 Altera Corp.

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	HMC Pin Assignment for DDR3/DDR2 *(3)*	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					U15							
		GND					U16							
		GND					U2							
		GND					U3							
		GND					U5							
		GND					U8							
		GND					U9							
		GND					V1							
		GND					V13							
		GND					V3							
		GND					V8							
		GND					W10							
		GND					W15							
		GND					W20							
		GND					Y1							
		GND					Y17							
		GND					Y2							
		GND					Y7							
		GND					R16							
		GND					P13							
		VCC					H8							
		VCC					J4							
		VCC					J6							
		VCC					J8							
		VCC					K3							
		VCC					K5							
		VCC					K7							
		VCC					L4							
		VCC					L6							
		VCC					M3							
		VCC					M5							
		VCC					M7							
		VCC					M8							
		VCC					N4							
		VCC					N6							
		VCC					P3							
		VCC					P5							
		VCC					P7							
		VCC					P8							
		VCC					R4							
		VCC					R6							
		VCC					R8							
		VCC					T3							
		VCC					T5							
		VCC					T7							
		VCC					P17							
		DNU					J2							
		DNU					H1							
		DNU					W2							
		DNU					Y9							
		DNU					C17							
		DNU					G8							
		VCCPGM					Y4							
		VCCPGM					Y18							
		VCCPGM					D4							
		VCCBAT					D2							
		VCCIO3A					AB6							
		VCCIO3A					W5							
		VCCIO3B					AA9							
		VCCIO4A					AA19							
		VCCIO4A					AB16							
		VCCIO4A					Y12							
		VCCIO5A					V18							
		VCCIO5A					Y22							
		VCCIO6A_HPS					D20							
		VCCIO6A_HPS					E17							
		VCCIO6A_HPS					G21							
		VCCIO6A_HPS					H18							
		VCCIO6A_HPS					J15							
		VCCIO6A_HPS					K22							
		VCCIO6A_HPS					L13							
		VCCIO6A_HPS					L19							
		VCCIO6B_HPS					M16							
		VCCIO6B_HPS					N13							
		VCCIO6B_HPS					P20							
		VCCIO6B_HPS					R17							
		VCCIO6B_HPS					T14							
		VCCIO6B_HPS					U21							
		VCCIO7A_HPS					A19							
		VCCIO7A_HPS					B16							
		VCCIO7B_HPS					C13							
		VCCIO7B_HPS					G11							
		VCCIO7C_HPS					D10							
		VCCIO7D_HPS					A9							
		VCCIO7D_HPS					E7							
		VCCIO8A					D5							
		VCCPD3A					Y6							
		VCCPD3B4A					AA12							
		VCCPD3B4A					V12							
		VCCPD3B4A					V14							
		VCCPD3B4A					W13							
		VCCPD3B4A					W9							
		VCCPD5A					T16							
		VCCPD6A6B_HPS					H16							
		VCCPD6A6B_HPS					J17							
		VCCPD6A6B_HPS					L17							
		VCCPD6A6B_HPS					M18							
		VCCPD7A_HPS					G13							
		VCCPD7B_HPS					F12							
		VCCPD7C_HPS					E10							
		VCCPD7D_HPS					C9							
		VCCPD8A					D6							
3A	VREFB3AN0	VREFB3AN0					AB4							
3B	VREFB3BN0	VREFB3BN0					AA10							
4A	VREFB4AN0	VREFB4AN0					AA20							
5A	VREFB5AN0	VREFB5AN0					W19							
	VREFB7A7B7C7DN0_HPS	VREFB7A7B7C7DN0_HPS					B17							
8A	VREFB8AN0	VREFB8AN0					B5							
		NC					G3							
		NC					H3							
		NC					R10							
		NC					R11							
		NC					T10							
		NC					T11							

Copyright © 2016 Altera Corp.

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	HMC Pin Assignment for DDR3/DDR2 *(3)*	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		NC					T12							
		NC					T9							
		VCCRSTCLK_HPS					D16							
		RREF_TL					J1							
		VCCA_FPLL					L1							
		VCCA_FPLL					P1							
		VCCA_FPLL					U1							
		VCCA_FPLL					W1							
		VCCA_FPLL					F1							
		VCCA_FPLL					W17							
		VCC_AUX					AA17							
		VCC_AUX					AA3							
		VCC_AUX					D3							
		VCC_AUX					D9							
		VCC_AUX					Y10							
		VCC_AUX_SHARED					E16							
		VCCPLL_HPS					F18							
		VCC_HPS					R13							
		VCC_HPS					K10							
		VCC_HPS					K12							
		VCC_HPS					L11							
		VCC_HPS					L9							
		VCC_HPS					M10							
		VCC_HPS					M12							
		VCC_HPS					N11							
		VCC_HPS					N9							
		VCC_HPS					P10							
		VCC_HPS					P12							

Notes:
(1) For more information about pin definitions and pin connection guidelines, refer to the
Cyclone V Device Family Pin Connection Guidelines.
(2) HPS_DDR pins are for memory interface only. For the dedicated pin function corresponding with the respective memory interfaces, refer to the HMC columns.
(3) RESET pin is only applicable for DDR3 device.

Copyright © 2016 Altera Corp.

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(3)*	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
3A		TDO		TDO			Y9								
3A		nCSO		DATA4			AA6								
3A		TMS		TMS			AC7								
3A		AS_DATA3		DATA3			AB6								
3A		TCK		TCK			AB5								
3A		AS_DATA2		DATA2			AC5								
3A		TDI		TDI			W10								
3A		AS_DATA1		DATA1			AC6								
3A		DCLK		DCLK			AA8								
3A		AS_DATA0,ASDO		DATA0			AD7								
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	Y8	DQ1B							
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	Y4								
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	W8	DQ1B							
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	Y5	DQ1B							
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	T8	DQSn1B							
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	AB4	DQ1B							
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	U9	DQS1B							
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	AA4								
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	V10	DQ1B							
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	AD4	DQ1B							
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	U10	DQ1B							
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	AC4	DQ1B							
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	AA11								
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	AE6	DQ1B							
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	Y11								
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AD5	DQ1B							
3B	VREFB3BN0	IO			DIFFIO_TX_B25n	DIFFOUT_B25n	AF4								
3B	VREFB3BN0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	AE9	DQ2B							
3B	VREFB3BN0	IO			DIFFIO_TX_B25p	DIFFOUT_B25p	AE4	DQ2B							
3B	VREFB3BN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	AD10	DQ2B							
3B	VREFB3BN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	U11	DQSn2B							
3B	VREFB3BN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AF8	DQ2B							
3B	VREFB3BN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	T11	DQS2B							
3B	VREFB3BN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AE7								
3B	VREFB3BN0	IO			DIFFIO_TX_B29n	DIFFOUT_B29n	AF9	DQ2B							
3B	VREFB3BN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	AE11	DQ2B							
3B	VREFB3BN0	IO			DIFFIO_TX_B29p	DIFFOUT_B29p	AE8	DQ2B							
3B	VREFB3BN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	AD11	DQ2B							
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B31n	DIFFOUT_B31n	W11								
3B	VREFB3BN0	IO			DIFFIO_TX_B32n	DIFFOUT_B32n	AF6	DQ2B							
3B	VREFB3BN0	IO	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B31p	DIFFOUT_B31p	V11								
3B	VREFB3BN0	IO			DIFFIO_TX_B32p	DIFFOUT_B32p	AF5	DQ2B							
3B	VREFB3BN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AG6								
3B	VREFB3BN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AF10	DQ3B							
3B	VREFB3BN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AF7	DQ3B							
3B	VREFB3BN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AF11	DQ3B							
3B	VREFB3BN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	T12	DQSn3B							
3B	VREFB3BN0	IO			DIFFIO_TX_B36n	DIFFOUT_B36n	AH2	DQ3B							
3B	VREFB3BN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	T13	DQS3B							
3B	VREFB3BN0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	AH3								
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B37n	DIFFOUT_B37n	AH4	DQ3B							
3B	VREFB3BN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AD12	DQ3B							
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B37p	DIFFOUT_B37p	AG5	DQ3B							
3B	VREFB3BN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AE12	DQ3B							
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B39n	DIFFOUT_B39n	W12								
3B	VREFB3BN0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	AH5	DQ3B							
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B39p	DIFFOUT_B39p	V12								
3B	VREFB3BN0	IO			DIFFIO_TX_B40p	DIFFOUT_B40p	AH6	DQ3B							
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B41n	DIFFOUT_B41n	AH7								
4A	VREFB4AN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AF13	DQ4B							
4A	VREFB4AN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AG8	DQ4B							
4A	VREFB4AN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	AG13	DQ4B							
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	U13	DQSn4B							
4A	VREFB4AN0	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	AH8	DQ4B							
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	U14	DQS4B							
4A	VREFB4AN0	IO			DIFFIO_TX_B44p	DIFFOUT_B44p	AG9								
4A	VREFB4AN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	AH9	DQ4B							
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AE15	DQ4B							
4A	VREFB4AN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	AG10	DQ4B							
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	AF15	DQ4B							
4A	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B47n	DIFFOUT_B47n	AA13								
4A	VREFB4AN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	AH11	DQ4B							
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B47p	DIFFOUT_B47p	Y13								
4A	VREFB4AN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	AG11	DQ4B							
4A	VREFB4AN0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	AG16	DQ5B	DQ1B						
4A	VREFB4AN0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AH12	DQ5B	DQ1B						
4A	VREFB4AN0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	AF17	DQ5B	DQ1B						
4A	VREFB4AN0	IO			DIFFIO_RX_B51n	DIFFOUT_B51n	V13	DQSn5B	DQ1B						
4A	VREFB4AN0	IO			DIFFIO_TX_B52n	DIFFOUT_B52n	AH13	DQ5B	DQ1B						
4A	VREFB4AN0	IO			DIFFIO_RX_B51p	DIFFOUT_B51p	W14	DQS5B	DQ1B						
4A	VREFB4AN0	IO			DIFFIO_TX_B52p	DIFFOUT_B52p	AG14								
4A	VREFB4AN0	IO			DIFFIO_TX_B53n	DIFFOUT_B53n	AH14	DQ5B	DQ1B						
4A	VREFB4AN0	IO			DIFFIO_RX_B54n	DIFFOUT_B54n	AE17	DQ5B	DQ1B						
4A	VREFB4AN0	IO			DIFFIO_TX_B53p	DIFFOUT_B53p	AG15	DQ5B	DQ1B						
4A	VREFB4AN0	IO			DIFFIO_RX_B54p	DIFFOUT_B54p	AD17	DQ5B	DQ1B						
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B55n	DIFFOUT_B55n	AA15								
4A	VREFB4AN0	IO			DIFFIO_TX_B56n	DIFFOUT_B56n	AH16	DQ5B	DQ1B						
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B55p	DIFFOUT_B55p	Y15								
4A	VREFB4AN0	IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AH17	DQ5B	DQ1B						
4A	VREFB4AN0	IO			DIFFIO_RX_B58n	DIFFOUT_B58n	AD19	DQ6B	DQ1B						
4A	VREFB4AN0	IO			DIFFIO_TX_B57p	DIFFOUT_B57p	AF18	DQ6B	DQ1B						
4A	VREFB4AN0	IO			DIFFIO_RX_B58p	DIFFOUT_B58p	AE19	DQ6B	DQ1B						
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	AA18	DQSn6B	DQSn1B						
4A	VREFB4AN0	IO			DIFFIO_TX_B60n	DIFFOUT_B60n	AH18	DQ6B	DQ1B						
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	AA19	DQS6B	DQS1B						
4A	VREFB4AN0	IO			DIFFIO_TX_B60p	DIFFOUT_B60p	AG18								
4A	VREFB4AN0	IO			DIFFIO_TX_B61n	DIFFOUT_B61n	AH19	DQ6B	DQ1B						
4A	VREFB4AN0	IO			DIFFIO_RX_B62n	DIFFOUT_B62n	AD20	DQ6B	DQ1B						
4A	VREFB4AN0	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	AG19	DQ6B	DQ1B						
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B62p	AE20	DQ6B	DQ1B						
4A	VREFB4AN0	IO			DIFFIO_TX_B64n	DIFFOUT_B64n	AG20	DQ6B	DQ1B						
4A	VREFB4AN0	IO			DIFFIO_TX_B64p	DIFFOUT_B64p	AF20	DQ6B	DQ1B						
4A	VREFB4AN0	IO			DIFFIO_RX_B66n	DIFFOUT_B66n	AF21	DQ7B	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_TX_B65p	DIFFOUT_B65p	AG21	DQ7B	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_RX_B66p	DIFFOUT_B66p	AF22	DQ7B	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_RX_B67n	DIFFOUT_B67n	AE22	DQSn7B	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_TX_B68n	DIFFOUT_B68n	AH21	DQ7B	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_RX_B67p	DIFFOUT_B67p	AD23	DQS7B	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_TX_B69n	DIFFOUT_B69n	AH22	DQ7B	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_RX_B70n	DIFFOUT_B70n	AF23	DQ7B	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_TX_B69p	DIFFOUT_B69p	AH23	DQ7B	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_RX_B70p	DIFFOUT_B70p	AG23	DQ7B	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_TX_B72n	DIFFOUT_B72n	AH24	DQ7B	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_TX_B72p	DIFFOUT_B72p	AG24	DQ7B	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_RX_B74n	DIFFOUT_B74n	AE23	DQ8B	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_TX_B73p	DIFFOUT_B73p	AG26	DQ8B	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_RX_B74p	DIFFOUT_B74p	AE24	DQ8B	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_RX_B75n	DIFFOUT_B75n	AC23	DQSn8B	DQSn2B						
4A	VREFB4AN0	IO			DIFFIO_TX_B76n	DIFFOUT_B76n	AH26	DQ8B	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_RX_B75p	DIFFOUT_B75p	AC22	DQS8B	DQS2B						
4A	VREFB4AN0	IO			DIFFIO_TX_B77n	DIFFOUT_B77n	AH27	DQ8B	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_RX_B78n	DIFFOUT_B78n	AG25	DQ8B	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_TX_B77p	DIFFOUT_B77p	AG28	DQ8B	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_RX_B78p	DIFFOUT_B78p	AF25	DQ8B	DQ2B						
4A	VREFB4AN0	IO			DIFFIO_TX_B80n	DIFFOUT_B80n	AF28	DQ8B	DQ2B						

Copyright © 2016 Altera Corp.

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(3)*	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
4A	VREFB4AN0	IO			DIFFIO_TX_B80p	DIFFOUT_B80p	AF27	DQ8B	DQ2B						
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	AF26	DQ1R							
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	AA20								
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	AE26	DQ1R							
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	Y19								
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	AE25	DQ1R							
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	Y17	DQ1R							
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	AD26	DQ1R							
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	Y18	DQ1R							
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	AC24								
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	Y16	DQS1R							
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	AB23	DQ1R							
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R6n	W15	DQSn1R							
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	AA24	DQ1R							
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	V16	DQ1R							
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	AA23								
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	V15	DQ1R							
5B	VREFB5BN0	IO	CLK5p		DIFFIO_RX_R21p	DIFFOUT_R21p	W21								
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R22p	DIFFOUT_R22p	AB26								
5B	VREFB5BN0	IO	CLK5n		DIFFIO_RX_R21n	DIFFOUT_R21n	W20								
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R22n	DIFFOUT_R22n	AA26								
5B	VREFB5BN0	IO	CLK4p,FPLL_BR_FBp		DIFFIO_RX_R23p	DIFFOUT_R23p	Y24								
5B	VREFB5BN0	IO	CLK4n,FPLL_BR_FBn		DIFFIO_RX_R23n	DIFFOUT_R23n	W24								
5B	VREFB5BN0	IO	RZQ_2		DIFFIO_TX_R24n	DIFFOUT_R24n	AB25								
6B	VREFB6BN0_HPS	HPS_DDR					AE28			HPS_DM_4	HPS_DM_4				
6B	VREFB6BN0_HPS	HPS_DDR					AD28			HPS_DQ_39	HPS_DQ_39				
6B	VREFB6BN0_HPS	HPS_DDR					V20			HPS_DQ_37	HPS_DQ_37				
6B	VREFB6BN0_HPS	HPS_DDR					AE27			HPS_DQ_38	HPS_DQ_38				
6B	VREFB6BN0_HPS	HPS_DDR					V19			HPS_DQ_36	HPS_DQ_36				
6B	VREFB6BN0_HPS	HPS_DDR					V18			HPS_DQS_4	HPS_DQS_4				
6B	VREFB6BN0_HPS	HPS_GPI13					V24								
6B	VREFB6BN0_HPS	HPS_DDR					V17			HPS_DQS#_4	HPS_DQS#_4				
6B	VREFB6BN0_HPS	HPS_DDR					V25			HPS_DQ_35	HPS_DQ_35				
6B	VREFB6BN0_HPS	HPS_DDR					U25			HPS_DQ_33	HPS_DQ_33				
6B	VREFB6BN0_HPS	HPS_DDR					AC28			HPS_DQ_34	HPS_DQ_34				
6B	VREFB6BN0_HPS	HPS_DDR					T26			HPS_DQ_32	HPS_DQ_32				
6B	VREFB6BN0_HPS	HPS_GPI12					AC27								
6B	VREFB6BN0_HPS	HPS_GPI11					U16								
6B	VREFB6BN0_HPS	HPS_DDR					AB28			HPS_DM_3	HPS_DM_3				
6B	VREFB6BN0_HPS	HPS_GPI10					U15								
6B	VREFB6BN0_HPS	HPS_DDR					AA27			HPS_DQ_31	HPS_DQ_31				
6B	VREFB6BN0_HPS	HPS_DDR					T24			HPS_DQ_29	HPS_DQ_29				
6B	VREFB6BN0_HPS	HPS_DDR					Y27			HPS_DQ_30	HPS_DQ_30				
6B	VREFB6BN0_HPS	HPS_DDR					R24			HPS_DQ_28	HPS_DQ_28				
6B	VREFB6BN0_HPS	VREFB6BN0_HPS					T27								
6B	VREFB6BN0_HPS	HPS_DDR					U19			HPS_DQS_3	HPS_DQS_3				
6B	VREFB6BN0_HPS	HPS_GPI9					Y26								
6B	VREFB6BN0_HPS	HPS_DDR					T20			HPS_DQS#_3	HPS_DQS#_3				
6B	VREFB6BN0_HPS	HPS_DDR					W26			HPS_DQ_27	HPS_DQ_27				
6B	VREFB6BN0_HPS	HPS_DDR					R25			HPS_DQ_25	HPS_DQ_25				
6B	VREFB6BN0_HPS	HPS_DDR					AA28			HPS_DQ_26	HPS_DQ_26				
6B	VREFB6BN0_HPS	HPS_DDR					R26			HPS_DQ_24	HPS_DQ_24				
6B	VREFB6BN0_HPS	HPS_GPI8					Y28								
6B	VREFB6BN0_HPS	HPS_GPI7					T16								
6B	VREFB6BN0_HPS	HPS_DDR					W28			HPS_DM_2	HPS_DM_2				
6B	VREFB6BN0_HPS	HPS_GPI6					T17								
6B	VREFB6BN0_HPS	HPS_DDR					V27			HPS_DQ_23	HPS_DQ_23				
6B	VREFB6BN0_HPS	HPS_DDR					N27			HPS_DQ_21	HPS_DQ_21				
6B	VREFB6BN0_HPS	HPS_DDR					R27			HPS_DQ_22	HPS_DQ_22				
6B	VREFB6BN0_HPS	HPS_DDR					N26			HPS_DQ_20	HPS_DQ_20				
6B	VREFB6BN0_HPS	HPS_GPI5					P26								
6B	VREFB6BN0_HPS	HPS_DDR					T19			HPS_DQS_2	HPS_DQS_2				
6B	VREFB6BN0_HPS	HPS_DDR					V28			HPS_RESET#	HPS_RESET#				
6B	VREFB6BN0_HPS	HPS_DDR					T18			HPS_DQS#_2	HPS_DQS#_2				
6B	VREFB6BN0_HPS	HPS_DDR					U28			HPS_DQ_19	HPS_DQ_19				
6B	VREFB6BN0_HPS	HPS_DDR					N25			HPS_DQ_17	HPS_DQ_17				
6B	VREFB6BN0_HPS	HPS_DDR					T28			HPS_DQ_18	HPS_DQ_18				
6B	VREFB6BN0_HPS	HPS_DDR					N24			HPS_DQ_16	HPS_DQ_16				
6B	VREFB6BN0_HPS	HPS_GPI4					R28								
6A	VREFB6AN0_HPS	HPS_GPI3					R21								
6A	VREFB6AN0_HPS	HPS_DDR					P28			HPS_DM_1	HPS_DM_1				
6A	VREFB6AN0_HPS	HPS_GPI2					R20								
6A	VREFB6AN0_HPS	HPS_DDR					N28			HPS_DQ_15	HPS_DQ_15				
6A	VREFB6AN0_HPS	HPS_DDR					M26			HPS_DQ_13	HPS_DQ_13				
6A	VREFB6AN0_HPS	HPS_DDR					M28			HPS_DQ_14	HPS_DQ_14				
6A	VREFB6AN0_HPS	HPS_DDR					M27			HPS_DQ_12	HPS_DQ_12				
6A	VREFB6AN0_HPS	HPS_DDR					L28			HPS_CKE_0	HPS_CKE_0				
6A	VREFB6AN0_HPS	HPS_DDR					R19			HPS_DQS_1	HPS_DQS_1				
6A	VREFB6AN0_HPS	HPS_DDR					K28			HPS_CKE_1	HPS_CKE_1				
6A	VREFB6AN0_HPS	HPS_DDR					R18			HPS_DQS#_1	HPS_DQS#_1				
6A	VREFB6AN0_HPS	HPS_DDR					J28			HPS_DQ_11	HPS_DQ_11				
6A	VREFB6AN0_HPS	HPS_DDR					L25			HPS_DQ_9	HPS_DQ_9				
6A	VREFB6AN0_HPS	HPS_DDR					J27			HPS_DQ_10	HPS_DQ_10				
6A	VREFB6AN0_HPS	HPS_DDR					K25			HPS_DQ_8	HPS_DQ_8				
6A	VREFB6AN0_HPS	HPS_GPI1					K27								
6A	VREFB6AN0_HPS	HPS_GPI0					M25								
6A	VREFB6AN0_HPS	HPS_DDR					G28			HPS_DM_0	HPS_DM_0				
6A	VREFB6AN0_HPS	HPS_DDR					F28			HPS_DQ_7	HPS_DQ_7				
6A	VREFB6AN0_HPS	HPS_DDR					K26			HPS_DQ_5	HPS_DQ_5				
6A	VREFB6AN0_HPS	HPS_DDR					G27			HPS_DQ_6	HPS_DQ_6				
6A	VREFB6AN0_HPS	HPS_DDR					J26			HPS_DQ_4	HPS_DQ_4				
6A	VREFB6AN0_HPS	HPS_DDR					G26			HPS_ODT_1	HPS_ODT_1				
6A	VREFB6AN0_HPS	HPS_DDR					R17			HPS_DQS_0	HPS_DQS_0				
6A	VREFB6AN0_HPS	HPS_DDR					D28			HPS_ODT_0	HPS_ODT_0				
6A	VREFB6AN0_HPS	HPS_DDR					R16			HPS_DQS#_0	HPS_DQS#_0				
6A	VREFB6AN0_HPS	HPS_DDR					D27			HPS_DQ_3	HPS_DQ_3				
6A	VREFB6AN0_HPS	HPS_DDR					J24			HPS_DQ_1	HPS_DQ_1				
6A	VREFB6AN0_HPS	HPS_DDR					E28			HPS_DQ_2	HPS_DQ_2				
6A	VREFB6AN0_HPS	HPS_DDR					J25			HPS_DQ_0	HPS_DQ_0				
6A	VREFB6AN0_HPS	VREFB6AN0_HPS					H28								
6A	VREFB6AN0_HPS	HPS_DDR					C28			HPS_A_0	HPS_CA_0				
6A	VREFB6AN0_HPS	HPS_DDR					B28			HPS_A_1	HPS_CA_1				
6A	VREFB6AN0_HPS	HPS_DDR					J21			HPS_A_4	HPS_CA_4				
6A	VREFB6AN0_HPS	HPS_DDR					E26			HPS_A_2	HPS_CA_2				
6A	VREFB6AN0_HPS	HPS_DDR					J20			HPS_A_5	HPS_CA_5				
6A	VREFB6AN0_HPS	HPS_DDR					D26			HPS_A_3	HPS_CA_3				
6A	VREFB6AN0_HPS	HPS_DDR					N21			HPS_CK	HPS_CK				
6A	VREFB6AN0_HPS	HPS_DDR					C26			HPS_A_6	HPS_CA_6				
6A	VREFB6AN0_HPS	HPS_DDR					N20			HPS_CK#	HPS_CK#				
6A	VREFB6AN0_HPS	HPS_DDR					B26			HPS_A_7	HPS_CA_7				
6A	VREFB6AN0_HPS	HPS_DDR					H25			HPS_BA_1					
6A	VREFB6AN0_HPS	HPS_DDR					A27			HPS_BA_0					
6A	VREFB6AN0_HPS	HPS_DDR					G25			HPS_BA_2					
6A	VREFB6AN0_HPS	HPS_DDR					A26			HPS_CAS#					
6A	VREFB6AN0_HPS	HPS_DDR					A25			HPS_RAS#					
6A	VREFB6AN0_HPS	HPS_DDR					F26			HPS_A_8	HPS_CA_8				
6A	VREFB6AN0_HPS	HPS_DDR					A24			HPS_A_10					
6A	VREFB6AN0_HPS	HPS_DDR					F25			HPS_A_9	HPS_CA_9				
6A	VREFB6AN0_HPS	HPS_DDR					B24			HPS_A_11					
6A	VREFB6AN0_HPS	HPS_DDR					L21			HPS_CS#_0	HPS_CS#_0				
6A	VREFB6AN0_HPS	HPS_DDR					D24			HPS_A_12					
6A	VREFB6AN0_HPS	HPS_DDR					L20			HPS_CS#_1	HPS_CS#_1				
6A	VREFB6AN0_HPS	HPS_DDR					C24			HPS_A_13					
6A	VREFB6AN0_HPS	HPS_DDR					G23			HPS_A_14					
6A	VREFB6AN0_HPS	HPS_DDR					E25			HPS_WE#					

Copyright © 2016 Altera Corp.

Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
6A	VREFB6AN0_HPS	HPS_DDR					F24								
6A	VREFB6AN0_HPS	HPS_RZQ_0					D25								
		GND					F23								
		GND					E23								
7A		HPS_nRST					A23								
7A		HPS_nPOR					H19								
7A		HPS_TDO					B23								
		VCCRSTCLK_HPS					J19								
7A		HPS_TMS					C23								
7A		HPS_TCK					K19								
7A		HPS_TRST					C22								
7A		HPS_TDI					D22								
		GND					D21								
7A		HPS_PORSEL					E18								
7A		HPS_CLK1					E20								
7A		HPS_CLK2					D20								
7A	VREFB7A7B7C7DN0_HPS	TRACE_CLK					C21					TRACE_CLK			HPS_GPIO48
7A	VREFB7A7B7C7DN0_HPS	TRACE_D0					A22					TRACE_D0	SPIS0_CLK	UART0_RX	HPS_GPIO49
7A	VREFB7A7B7C7DN0_HPS	TRACE_D1					B21					TRACE_D1	SPIS0_MOSI	UART0_TX	HPS_GPIO50
7A	VREFB7A7B7C7DN0_HPS	TRACE_D2					A21					TRACE_D2	SPIS0_MISO	I2C1_SDA	HPS_GPIO51
7A	VREFB7A7B7C7DN0_HPS	TRACE_D3					K18					TRACE_D3	SPIS0_SS0	I2C1_SCL	HPS_GPIO52
7A	VREFB7A7B7C7DN0_HPS	TRACE_D4					A20					TRACE_D4	SPIS1_CLK	CAN1_RX	HPS_GPIO53
7A	VREFB7A7B7C7DN0_HPS	TRACE_D5					J18					TRACE_D5	SPIS1_MOSI	CAN1_TX	HPS_GPIO54
7A	VREFB7A7B7C7DN0_HPS	TRACE_D6					A19					TRACE_D6	SPIS1_SS0	I2C0_SDA	HPS_GPIO55
7A	VREFB7A7B7C7DN0_HPS	TRACE_D7					C18					TRACE_D7	SPIS1_MISO	I2C0_SCL	HPS_GPIO56
7A	VREFB7A7B7C7DN0_HPS	SPIM0_CLK					A18					SPIM0_CLK	I2C1_SDA	UART0_CTS	HPS_GPIO57
7A	VREFB7A7B7C7DN0_HPS	SPIM0_MOSI					C17					SPIM0_MOSI	I2C1_SCL	UART0_RTS	HPS_GPIO58
7A	VREFB7A7B7C7DN0_HPS	SPIM0_MISO					B18					SPIM0_MISO	CAN1_RX	UART1_CTS	HPS_GPIO59
7A	VREFB7A7B7C7DN0_HPS	SPIM0_SS0,BOOTSEL0					J17					SPIM0_SS0	CAN1_TX	UART1_RTS	HPS_GPIO60
7A	VREFB7A7B7C7DN0_HPS	UART0_RX					A17					UART0_RX	CAN0_RX	SPIM0_SS1	HPS_GPIO61
7A	VREFB7A7B7C7DN0_HPS	UART0_TX,CLKSEL1					H17					UART0_TX	CAN0_TX	SPIM1_SS1	HPS_GPIO62
7A	VREFB7A7B7C7DN0_HPS	I2C0_SDA					C19					I2C0_SDA	UART1_RX	SPIM1_CLK	HPS_GPIO63
7A	VREFB7A7B7C7DN0_HPS	I2C0_SCL					B16					I2C0_SCL	UART1_TX	SPIM1_MOSI	HPS_GPIO64
7A	VREFB7A7B7C7DN0_HPS	CAN0_RX					B19					CAN0_RX	UART0_RX	SPIM1_MISO	HPS_GPIO65
7A	VREFB7A7B7C7DN0_HPS	CAN0_TX,CLKSEL0					C16					CAN0_TX	UART0_TX	SPIM1_SS0	HPS_GPIO66
7B	VREFB7A7B7C7DN0_HPS	NAND_ALE					J15					NAND_ALE	RGMII1_TX_CLK	QSPI_SS3	HPS_GPIO14
7B	VREFB7A7B7C7DN0_HPS	NAND_CE					A16					NAND_CE	RGMII1_TXD0	USB1_D0	HPS_GPIO15
7B	VREFB7A7B7C7DN0_HPS	NAND_CLE					J14					NAND_CLE	RGMII1_TXD1	USB1_D1	HPS_GPIO16
7B	VREFB7A7B7C7DN0_HPS	NAND_RE					A15					NAND_RE	RGMII1_TXD2	USB1_D2	HPS_GPIO17
7B	VREFB7A7B7C7DN0_HPS	NAND_RB					D17					NAND_RB	RGMII1_TXD3	USB1_D3	HPS_GPIO18
7B	VREFB7A7B7C7DN0_HPS	NAND_DQ0					A14					NAND_DQ0	RGMII1_RXD0		HPS_GPIO19
7B	VREFB7A7B7C7DN0_HPS	NAND_DQ1					E16					NAND_DQ1	RGMII1_MDIO	I2C3_SDA	HPS_GPIO20
7B	VREFB7A7B7C7DN0_HPS	NAND_DQ2					A13					NAND_DQ2	RGMII1_MDC	I2C3_SCL	HPS_GPIO21
7B	VREFB7A7B7C7DN0_HPS	NAND_DQ3					J13					NAND_DQ3	RGMII1_RX_CTL	USB1_D4	HPS_GPIO22
7B	VREFB7A7B7C7DN0_HPS	NAND_DQ4					A12					NAND_DQ4	RGMII1_TX_CTL	USB1_D5	HPS_GPIO23
7B	VREFB7A7B7C7DN0_HPS	NAND_DQ5					J12					NAND_DQ5	RGMII1_RX_CLK	USB1_D6	HPS_GPIO24
7B	VREFB7A7B7C7DN0_HPS	NAND_DQ6					A11					NAND_DQ6	RGMII1_RXD1	USB1_D7	HPS_GPIO25
7B	VREFB7A7B7C7DN0_HPS	NAND_DQ7					C15					NAND_DQ7	RGMII1_RXD2		HPS_GPIO26
7B	VREFB7A7B7C7DN0_HPS	NAND_WP					A9					NAND_WP	RGMII1_RXD3	QSPI_SS2	HPS_GPIO27
7B	VREFB7A7B7C7DN0_HPS	NAND_WE,BOOTSEL2					D15					NAND_WE	QSPI_SS1		HPS_GPIO28
7B	VREFB7A7B7C7DN0_HPS	QSPI_IO0					A8					QSPI_IO0		USB1_CLK	HPS_GPIO29
7B	VREFB7A7B7C7DN0_HPS	QSPI_IO1					H16					QSPI_IO1		USB1_STP	HPS_GPIO30
7B	VREFB7A7B7C7DN0_HPS	QSPI_IO2					A7					QSPI_IO2		USB1_DIR	HPS_GPIO31
7B	VREFB7A7B7C7DN0_HPS	QSPI_IO3					J16					QSPI_IO3		USB1_NXT	HPS_GPIO32
7B	VREFB7A7B7C7DN0_HPS	QSPI_SS0,BOOTSEL1					A6					QSPI_SS0			HPS_GPIO33
7B	VREFB7A7B7C7DN0_HPS	QSPI_CLK					C14					QSPI_CLK			HPS_GPIO34
7B	VREFB7A7B7C7DN0_HPS	QSPI_SS1					B14					QSPI_SS1			HPS_GPIO35
7C	VREFB7A7B7C7DN0_HPS	SDMMC_CMD					D14					SDMMC_CMD	USB0_D0		HPS_GPIO36
7C	VREFB7A7B7C7DN0_HPS	SDMMC_PWREN					A5					SDMMC_PWREN	USB0_D1		HPS_GPIO37
7C	VREFB7A7B7C7DN0_HPS	SDMMC_D0					C13					SDMMC_D0	USB0_D2		HPS_GPIO38
7C	VREFB7A7B7C7DN0_HPS	SDMMC_D1					B6					SDMMC_D1	USB0_D3		HPS_GPIO39
7C	VREFB7A7B7C7DN0_HPS	SDMMC_D4					H13					SDMMC_D4	USB0_D4		HPS_GPIO40
7C	VREFB7A7B7C7DN0_HPS	SDMMC_D5					A4					SDMMC_D5	USB0_D5		HPS_GPIO41
7C	VREFB7A7B7C7DN0_HPS	SDMMC_D6					H12					SDMMC_D6	USB0_D6		HPS_GPIO42
7C	VREFB7A7B7C7DN0_HPS	SDMMC_D7					B4					SDMMC_D7	USB0_D7		HPS_GPIO43
7C	VREFB7A7B7C7DN0_HPS	HPS_GPIO44					B12						USB0_CLK		HPS_GPIO44
7C	VREFB7A7B7C7DN0_HPS	SDMMC_CCLK_OUT					B8					SDMMC_CCLK_OUT	USB0_STP		HPS_GPIO45
7C	VREFB7A7B7C7DN0_HPS	SDMMC_D2					B11					SDMMC_D2	USB0_DIR		HPS_GPIO46
7C	VREFB7A7B7C7DN0_HPS	SDMMC_D3					B9					SDMMC_D3	USB0_NXT		HPS_GPIO47
7D	VREFB7A7B7C7DN0_HPS	RGMII0_TX_CLK					E4					RGMII0_TX_CLK			HPS_GPIO0
7D	VREFB7A7B7C7DN0_HPS	RGMII0_TXD0					C10					RGMII0_TXD0	USB1_D0		HPS_GPIO1
7D	VREFB7A7B7C7DN0_HPS	RGMII0_TXD1					F5					RGMII0_TXD1	USB1_D1		HPS_GPIO2
7D	VREFB7A7B7C7DN0_HPS	RGMII0_TXD2					C9					RGMII0_TXD2	USB1_D2		HPS_GPIO3
7D	VREFB7A7B7C7DN0_HPS	RGMII0_TXD3					C4					RGMII0_TXD3	USB1_D3		HPS_GPIO4
7D	VREFB7A7B7C7DN0_HPS	RGMII0_RXD0					C8					RGMII0_RXD0	USB1_D4		HPS_GPIO5
7D	VREFB7A7B7C7DN0_HPS	RGMII0_MDIO					D4					RGMII0_MDIO	USB1_D5	I2C2_SDA	HPS_GPIO6
7D	VREFB7A7B7C7DN0_HPS	RGMII0_MDC					C7					RGMII0_MDC	USB1_D6	I2C2_SCL	HPS_GPIO7
7D	VREFB7A7B7C7DN0_HPS	RGMII0_RX_CTL					F4					RGMII0_RX_CTL	USB1_D7		HPS_GPIO8
7D	VREFB7A7B7C7DN0_HPS	RGMII0_TX_CTL					C6					RGMII0_TX_CTL			HPS_GPIO9
7D	VREFB7A7B7C7DN0_HPS	RGMII0_RX_CLK					G4					RGMII0_RX_CLK	USB1_CLK		HPS_GPIO10
7D	VREFB7A7B7C7DN0_HPS	RGMII0_RXD1					C5					RGMII0_RXD1	USB1_STP		HPS_GPIO11
7D	VREFB7A7B7C7DN0_HPS	RGMII0_RXD2					E5					RGMII0_RXD2	USB1_DIR		HPS_GPIO12
7D	VREFB7A7B7C7DN0_HPS	RGMII0_RXD3					D5					RGMII0_RXD3	USB1_NXT		HPS_GPIO13
8A	VREFB8AN0	IO	CLK7p		DIFFIO_RX_T1p	DIFFOUT_T1p	D12								
8A	VREFB8AN0	IO	CLK7n		DIFFIO_RX_T1n	DIFFOUT_T1n	C12								
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T4p	DIFFOUT_T4p	E8								
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T4n	DIFFOUT_T4n	D8								
8A	VREFB8AN0	IO	CLK6p,FPLL_TL_FBp		DIFFIO_RX_T9p	DIFFOUT_T9p	E11								
8A	VREFB8AN0	IO	CLK6n,FPLL_TL_FBn		DIFFIO_RX_T9n	DIFFOUT_T9n	D11								
9A		MSEL0		MSEL0			J10								
9A		CONF_DONE		CONF_DONE			J8								
9A		MSEL1		MSEL1			H9								
9A		nSTATUS		nSTATUS			H8								
9A		nCE		nCE			E6								
9A		MSEL2		MSEL2			G6								
9A		MSEL3		MSEL3			K10								
9A		nCONFIG		nCONFIG			F7								
9A		MSEL4		MSEL4			K9								
		GND					F6								
		GND					N8								
		GND					P8								
		GND					F2								
		GND					F1								
		GND					K2								
		GND					K1								
		GND					P2								
		GND					P1								
		GND					V2								
		GND					V1								
		GND					AB2								
		GND					AB1								
		GND					AF2								
		GND					AF1								
		GND					V5								
		GND					V4								
		GND					A10								
		GND					A3								
		GND					AA1								
		GND					AA17								
		GND					AA2								
		GND					AA3								
		GND					AA9								
		GND					AB24								
		GND					AB27								
		GND					AB3								

Copyright © 2016 Altera Corp.

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(3)*	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					AC1								
		GND					AC2								
		GND					AC3								
		GND					AD14								
		GND					AD22								
		GND					AD25								
		GND					AD3								
		GND					AD6								
		GND					AD8								
		GND					AE1								
		GND					AE16								
		GND					AE18								
		GND					AE2								
		GND					AE3								
		GND					AF24								
		GND					AF3								
		GND					AG1								
		GND					AG17								
		GND					AG2								
		GND					AG27								
		GND					AG3								
		GND					AG7								
		GND					AH10								
		GND					AH20								
		GND					B15								
		GND					B17								
		GND					B20								
		GND					B22								
		GND					B25								
		GND					B27								
		GND					B3								
		GND					B5								
		GND					B7								
		GND					C1								
		GND					C11								
		GND					C2								
		GND					C3								
		GND					D10								
		GND					D13								
		GND					D16								
		GND					D3								
		GND					E1								
		GND					E19								
		GND					E2								
		GND					E22								
		GND					E24								
		GND					E27								
		GND					E3								
		GND					E9								
		GND					F3								
		GND					G1								
		GND					G2								
		GND					G3								
		GND					H11								
		GND					H15								
		GND					H18								
		GND					H20								
		GND					H24								
		GND					H27								
		GND					H3								
		GND					H4								
		GND					H5								
		GND					H6								
		GND					J1								
		GND					J2								
		GND					J3								
		GND					J5								
		GND					J9								
		GND					K11								
		GND					K12								
		GND					K14								
		GND					K16								
		GND					K20								
		GND					K3								
		GND					K4								
		GND					K8								
		GND					L1								
		GND					L10								
		GND					L13								
		GND					L15								
		GND					L17								
		GND					L19								
		GND					L2								
		GND					L24								
		GND					L27								
		GND					L3								
		GND					L5								
		GND					L8								
		GND					L9								
		GND					M10								
		GND					M11								
		GND					M14								
		GND					M16								
		GND					M20								
		GND					M3								
		GND					M8								
		GND					N1								
		GND					N13								
		GND					N15								
		GND					N17								
		GND					N19								
		GND					N2								
		GND					N3								
		GND					N4								
		GND					P10								
		GND					P12								
		GND					P16								
		GND					P18								
		GND					P20								
		GND					P25								
		GND					P3								
		GND					P5								
		GND					P9								
		GND					R1								
		GND					R11								
		GND					R13								
		GND					R15								
		GND					R2								
		GND					R3								
		GND					R8								
		GND					T10								
		GND					T14								
		GND					T3								
		GND					U1								
		GND					U12								

Copyright © 2016 Altera Corp.

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(3)*	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					U17								
		GND					U2								
		GND					U20								
		GND					U24								
		GND					U27								
		GND					U3								
		GND					U5								
		GND					V14								
		GND					V3								
		GND					V8								
		GND					V9								
		GND					W1								
		GND					W16								
		GND					W18								
		GND					W2								
		GND					W3								
		GND					W4								
		GND					Y12								
		GND					Y14								
		GND					Y20								
		GND					Y25								
		GND					Y3								
		GND					V26								
		GND					V21								
		VCC					J11								
		VCC					K13								
		VCC					K15								
		VCC					L11								
		VCC					L12								
		VCC					L14								
		VCC					M12								
		VCC					M13								
		VCC					M15								
		VCC					M9								
		VCC					N10								
		VCC					N11								
		VCC					N12								
		VCC					N14								
		VCC					N9								
		VCC					P11								
		VCC					P13								
		VCC					P14								
		VCC					P15								
		VCC					R10								
		VCC					R12								
		VCC					R14								
		VCC					R9								
		VCC					T15								
		VCC					T9								
		VCC					L4								
		VCC					T4								
		VCC					M5								
		VCC					N5								
		VCC					R5								
		VCC					T5								
		VCC					U26								
		DNU					A2								
		DNU					B2								
		DNU					D1								
		DNU					D2								
		DNU					H1								
		DNU					H2								
		DNU					M1								
		DNU					M2								
		DNU					T1								
		DNU					T2								
		DNU					Y1								
		DNU					Y2								
		DNU					AD1								
		DNU					AD2								
		DNU					U8								
		DNU					AE14								
		DNU					D23								
		DNU					E12								
		VCCPGM					Y10								
		VCCPGM					AD24								
		VCCPGM					H10								
		VCCBAT					D7								
		VCCIO3A					AA5								
		VCCIO3A					W9								
		VCCIO3B					AA12								
		VCCIO3B					AE10								
		VCCIO3B					AE13								
		VCCIO3B					AG4								
		VCCIO4A					AA16								
		VCCIO4A					AE21								
		VCCIO4A					AF14								
		VCCIO4A					AF19								
		VCCIO4A					AG12								
		VCCIO4A					AG22								
		VCCIO4A					AH15								
		VCCIO4A					AH25								
		VCCIO4A					W13								
		VCCIO5A					AC25								
		VCCIO5A					W17								
		VCCIO5B					W25								
		VCCIO6A_HPS					C25								
		VCCIO6A_HPS					C27								
		VCCIO6A_HPS					F27								
		VCCIO6A_HPS					G24								
		VCCIO6A_HPS					H21								
		VCCIO6A_HPS					H26								
		VCCIO6A_HPS					L26								
		VCCIO6A_HPS					M21								
		VCCIO6B_HPS					AD27								
		VCCIO6B_HPS					P27								
		VCCIO6B_HPS					T21								
		VCCIO6B_HPS					T25								
		VCCIO6B_HPS					U18								
		VCCIO6B_HPS					W27								
		VCCIO7A_HPS					C20								
		VCCIO7A_HPS					D18								
		VCCIO7B_HPS					B13								
		VCCIO7B_HPS					H14								
		VCCIO7C_HPS					B10								
		VCCIO7D_HPS					D6								
		VCCIO7D_HPS					G5								
		VCCIO8A					E7								
		VCCPD3A					AA10								
		VCCPD3B4A					AA14								
		VCCPD3B4A					AD13								
		VCCPD3B4A					AD16								
		VCCPD3B4A					AD18								
		VCCPD3B4A					AD21								
		VCCPD3B4A					AD9								

Copyright © 2016 Altera Corp.

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(3)*	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCCPD5A					Y21								
		VCCPD5B					W19								
		VCCPD6A6B_HPS					K21								
		VCCPD6A6B_HPS					K24								
		VCCPD6A6B_HPS					M24								
		VCCPD6A6B_HPS					P21								
		VCCPD6A6B_HPS					P24								
		VCCPD7A_HPS					E21								
		VCCPD7B_HPS					E17								
		VCCPD7C_HPS					E14								
		VCCPD7D_HPS					E13								
		VCCPD8A					E10								
3A	VREFB3AN0	VREFB3AN0					AE5								
3B	VREFB3BN0	VREFB3BN0					AF12								
4A	VREFB4AN0	VREFB4AN0					AF16								
5A	VREFB5AN0	VREFB5AN0					AC26								
5B	VREFB5BN0	VREFB5BN0					AA25								
	VREFB7A7B7C7DN0_HPS	VREFB7A7B7C7DN0_HPS					D19								
8A	VREFB8AN0	VREFB8AN0					D9								
		VCCRSTCLK_HPS					F22								
		RREF_TL					B1								
		VCCA_FPLL					K5								
		VCCA_FPLL					P4								
		VCCA_FPLL					U4								
		VCCA_FPLL					W5								
		VCCA_FPLL					J4								
		VCCA_FPLL					AA21								
		VCCA_FPLL					M4								
		VCCA_FPLL					R4								
		VCC_AUX					AC21								
		VCC_AUX					AC8								
		VCC_AUX					AD15								
		VCC_AUX					E15								
		VCC_AUX					F8								
		VCC_AUX_SHARED					F21								
		VCCPLL_HPS					H23								
		VCC_HPS					U21								
		VCC_HPS					K17								
		VCC_HPS					L16								
		VCC_HPS					L18								
		VCC_HPS					M17								
		VCC_HPS					M18								
		VCC_HPS					M19								
		VCC_HPS					N16								
		VCC_HPS					N18								
		VCC_HPS					P17								
		VCC_HPS					P19								

Notes:
(1) For more information about pin definitions and pin connection guidelines, refer to the
Cyclone V Device Family Pin Connection Guidelines.
(2) HPS_DDR pins are for memory interface only. For the dedicated pin function corresponding with the respective memory interfaces, refer to the HMC columns.
(3) RESET pin is only applicable for DDR3 device.

Copyright © 2016 Altera Corp.

Version Number	Date	Changes Made
1.0	10/18/2012	Initial release.
1.1	1/17/2013	A pin that was marked as VCC_HPS has been corrected to VCCRSTCLK_HPS
1.2	3/25/2013	Updated the following pin names: - Changed SDMMC_CLK_IN to SDMMC_FB_CLK_IN - Changed SDMMC_CLK to SDMMC_CCLK_OUT
1.3	9/30/2014	- Remove corresponding bank number from VCCRSTCLK_HPS pin. - Changed HMC Pin Assignment for DDR3 to HMC Pin Assignment for DDR3/DDR2. - Added note 3.
1.4	1/4/2016	Removed the USB0 pin from Pin List U19.
1.5	12/23/2016	-Renamed SDMMC_FB_CLK_IN to HPS_GPIO44.

Copyright © 2016 Altera Corp.