White Paper

Designing With Confidence for Military SDR Production Applications

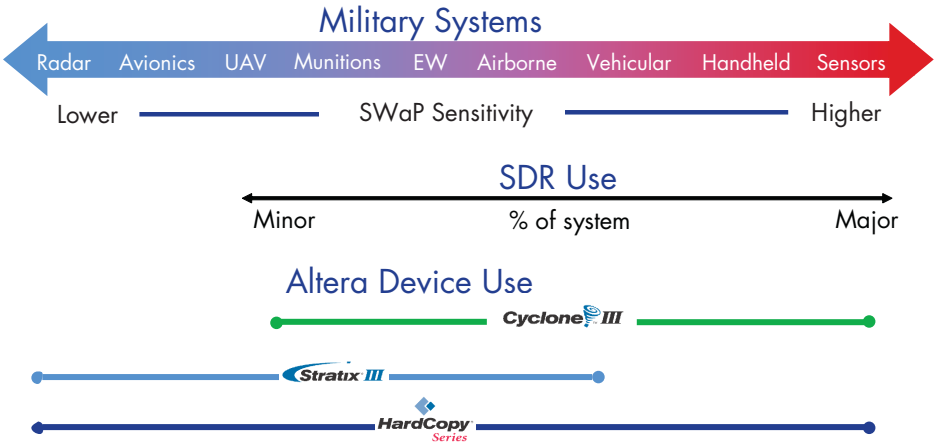
Introduction

The military community is transforming the battlefield of the 21st century around network-centric warfare. From satellite to soldier and everything in between, system size, weight, and power (SWaP) are critical. Whether in manned (ships, aircraft, and vehicles) or unmanned (missiles, sensors, air and ground vehicles (UAVs and UGVs)) equipment, secure wireless communications are central to the solution. Further, to cover multiple battlefield scenarios, add the complexity of triple-play (voice, video, and data) capabilities and multi-megabit bandwidths—the design challenges for secure communication devices are overwhelming. While airborne and maritime software-defined radios (SDRs) have functional and heat dissipation (cooling) challenges, the most demanding requirements for SWaP applications are in handheld, manpack, and small form factor (HMS) battery-operated systems.

SWaP Military Applications

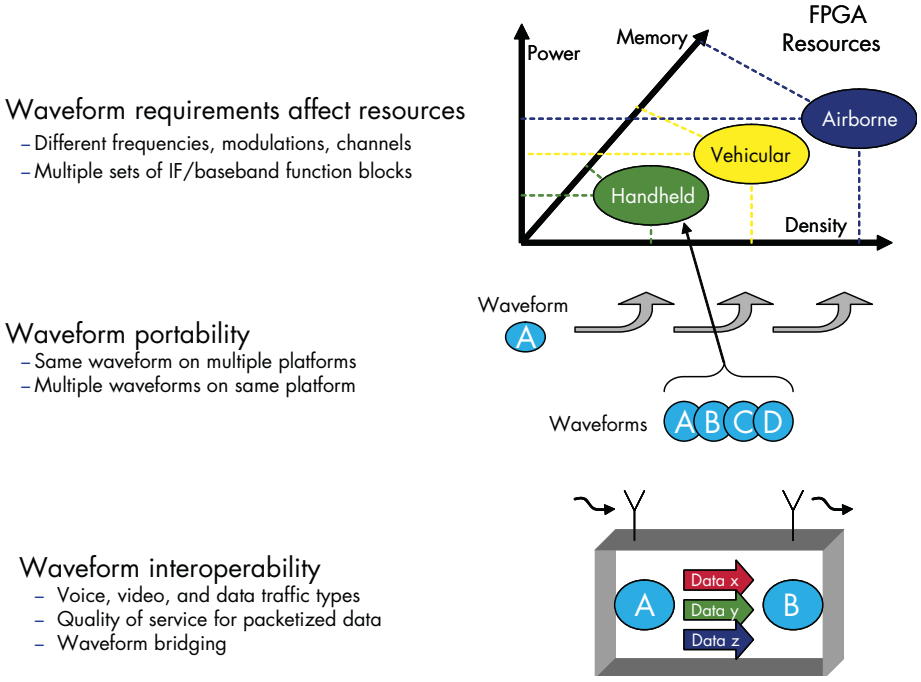
Figure 1 shows the SWaP processing spectrum of secure communications across military systems, ranging from the least (on the left) to most sensitive: from radar and electronic warfare to HMS radios and unattended ground sensors. Most radar and electronic warfare systems are generally function-critical rather than SWaP-critical, having sufficient envelopes for size and power. Wireless communications within UAV and UGV systems are SWaP sensitive, but require only a small portion of the overall power budget necessary for air and ground mobility. While munitions and missiles have extremely tight space constraints, power sensitivity is low due to their short mission life after activation. However, for HMS battery-operated radios, the SWaP stakes are progressively higher as they have tighter size, weight, and power restrictions.

Figure 1. SWaP Sensitivity Spectrum in Military Systems



Creating handheld radios is a daunting task. Soldiers need to carry more ammunition and body armor, not batteries, thus SWaP factors are critical. Facing stringent operating requirements for deployment across various battlefield scenarios, radio form factors demand the smallest implementation size using a limited number of components. As shown in Figure 2, new military waveforms like SRW and WNW require flexibility and functionality beyond low-power digital signal processing (DSP) devices. New SDR designs require programmable capabilities for advanced waveforms (processing intermediate frequency (IF), modulation, and bit-level functions at megabits per second (Mbps)), triple-play packet processing, and military software communications architecture (SCA) middleware (for hardware independence), all of which push the boundaries of FPGA resources. Ultimately, the power consumption of these SDR digital electronics adversely affects mission life or may surpass system heat dissipation limits in extreme environments.

Figure 2. Military Waveform Requirements



To summarize the SWaP design challenges for HMS battery-operated, SWaP-sensitive radios for vehicular and airborne use:

- *Severe size and weight restrictions:* The smallest implementations are less than 25 cm^3 in size.
- *Power consumption directly affects mission life:* Using typical military batteries, today's programmable electronics consume over 4 watts, and only yield a 6-hour mission life for the overall radio system.
- *Power budgets dominated by digital electronic processing:* As waveform bandwidth and complexity increases, digital processing absorbs more functionality and power within the radio.
- *Digital logic implementation trade-offs:* Choices for digital processing vary from CPU to ASIC. Typically, DSP devices and FPGAs have provided the best combination of functionality and flexibility, while suffering power trade-offs.
- *Static versus dynamic power trade-offs:* Due to the duty cycle of radio modes, standby operation typically dominates radio use by a factor of 10:1. It is therefore imperative to minimize digital leakage power during standby operation.
- *Voltage and frequency scaling trade-offs to save power:* With careful system design, both voltage and frequency can be scaled back during standby, beacon, and emergency modes, leaving only a small portion of the radio functional.
- *Software and hardware partitioning for power:* Software designers need to understand radio operational modes and intelligently manage hardware resources to minimize power use effectively.

Previous attempts to meet HMS requirements for production units have fallen short. Waveform requirements, such as variations of the soldier radio waveform (SRW), are too power sensitive for high-performance FPGAs, but beyond the capabilities of low-power DSP devices and low-cost FPGAs. As data rates move from Kbps to Mbps, low-power DSP devices no longer have the functionality for IF, modulation, bit-level processing, packet processing, and group services. Many low-cost FPGAs need multiple devices to implement the required functionality and thus limit the size and weight capability of integration.

Suppliers of high-performance FPGAs have tried to exploit features like voltage scaling and partial reconfiguration for waveform integration with little success, often causing delays in development and adding increased system risk.

Without careful control of device design and manufacturing constraints, voltage scaling (lowering voltage during radio standby conditions to reduce static power drain) can degrade verification and susceptibility of functional, timing, and I/O parameters. Partial reconfiguration (the ability to reprogram portions of logic while other functionality continues) for power reduction is ineffective in a high-power-process FPGA device, since the unused functional areas can draw several watts of static (leakage) power.

Designer Goals for Success

Designers face severe functional and schedule challenges to meet program requirements:

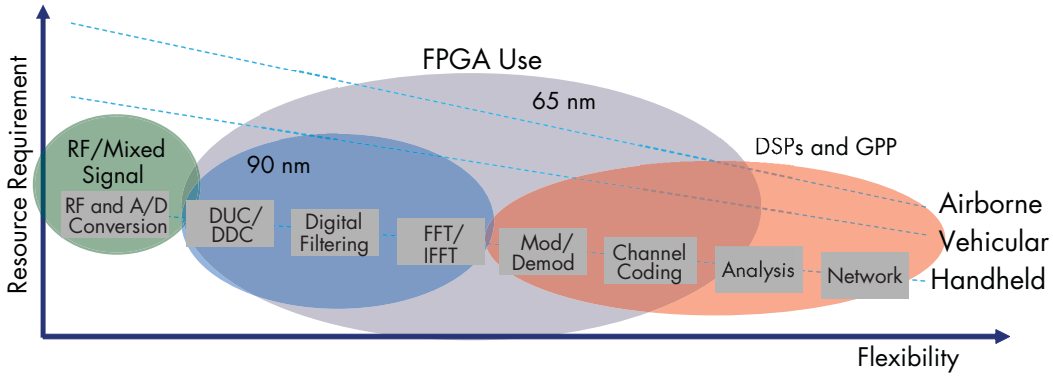
- Enabling small form factor, lightweight military solutions
- Achieving waveform integration under 1 watt to extend mission life and flexibility
- Providing optimum value for high-volume, low-cost SDR handsets

Even with these competing challenges, designers can confidently meet SWaP requirements for SDR production deployment by looking to Altera's new 65-nm FPGA devices. Altera has built on the success of its 90-nm devices for vehicular and airborne SDR implementations to create new, power-optimized Stratix® III and Cyclone® III FPGAs and tool sets for SDR battery-operated solutions, suitable for production.

Solving SDR Design Challenges

Altera's new 65-nm Stratix III and Cyclone III FPGAs have the right combination of advanced architecture capabilities, coupled with the most aggressive power reduction techniques. While prior 90-nm generation devices provided the right combination of resources to implement system development and demonstration radios (SDD programs), Altera's 65-nm families have been optimized for SWaP production applications. Figure 3 illustrates the expansion of 65-nm device capability and flexibility. Where 90-nm programmable logic devices (PLDs) implemented IF, filtering and frequency/time conversion, 65-nm devices now provide more waveform modulation and channel and packet processing functionality across all SDR application form factors

Figure 3. FPGAs Expanding in SDR Capability and Flexibility



Low-Power Devices

The newest high-performance, high-density Stratix III FPGAs provide maximum signal processing performance and multimode functionality at minimum power to address the broadest range of airborne and ground mobile radios (e.g., AMF and GMR). With device resources of up to 340K logic elements (LEs), 17 Mbits of embedded memory, and close to 900 multipliers, Stratix III FPGAs are best for function-critical SDR applications. Designers must be able to implement new high performance waveforms like WNW and JAN-TE, while also supporting low performing waveforms such as SRW without penalty. Altera's patented Programmable Power Technology minimizes heat dissipation and cooling requirements by optimizing all circuits not on critical paths, in applications where batteries are not required. For high-volume, power-sensitive applications like sensors or single-event upset (SEU)-sensitive systems in aircraft, only Altera offers a seamless path to logic-efficient HardCopy® structured ASICs, with an

ITAR-secure manufacturing process. HardCopy devices use the same Quartus® tool suite and design flow as Stratix series FPGAs, enabling fast prototyping, rapid transition to lower power, and lower cost implementations of up to 70 percent.

For the most demanding uses in small form-factor, lightweight, battery-operated SDR and special operations radios using SRW and legacy waveforms, Altera® Cyclone III devices are optimized for solving the various SWaP design challenges.

- *Severe size and weight restrictions:* For the smallest implementations under 25 cm^3, Cyclone III devices have enough resources in a single chip to process advanced waveforms like SRW-CC (soldier radio waveform, combat communicator mode). Abundant signal processing blocks and ample distributed memory eliminate power hungry external memory components. Devices are also available in die form for advanced micro-packaging options.
- *Power consumption directly affects mission life:* Cyclone III devices can implement entire waveforms under 1 watt, yielding a mission life of four times greater than current PLD implementations.
- *Power budget dominated by digital processing:* With significant increases in waveform complexity, the majority of the functionality can now be optimized in Cyclone III FPGAs, eliminating the power of DSP devices from the digital electronics power budget.
- *Digital logic implementation trade-offs:* Low-power PLDs like Cyclone III devices have far surpassed DSP devices in millions of instructions per second (MIPS) per watt, providing more efficient and lower power digital implementations.
- *Static versus dynamic power trade-offs:* Power during standby operation can be minimized by using the low static power of Cyclone III devices, with less than one-tenth the static power of other 90- and 65-nm FPGAs available.
- *Voltage and frequency scaling trade-offs to save power:* By partitioning functional areas into multiple PLD clock domains within Cyclone III devices, frequency scaling can be exploited for power savings. By following Altera guidelines and careful system design, voltage scaling (Stratix III FPGAs offer both 1.1V and 0.9V operation) and device shut-down techniques may be used to lower static leakage during standby modes.
- *Software and hardware partitioning for power:* The most efficient SWaP implementations use system and device productivity tools to optimize system usage, modes of operation, intelligent software control, and designer partitioning of functionality between GPP, PLD, DSP, and ASIC solutions. For greater power savings, intelligent system partitioning can be used across devices with software control to shut down noncritical components during standby. Additional system benefits using Altera's power-optimized PLDs enable designers to use more efficient power supplies, smaller form factor enclosures, and smaller, lighter, and less expensive batteries.

Figure 4 shows the static power for both Stratix and Cyclone series families compared to other 90- and 65-nm PLD families. These comparisons were performed using the power estimator tools of both PLD companies and normalized to 70K LEs, for typical- and worst-case devices at 85°C (Beware of static power claims at 25°C, which are significantly lower). Starting with the left column, in addition to the superior performance of Altera devices, 90-nm Cyclone II devices have 50 percent less static power than their counterparts and provide superior manufacturing tolerances for power, within 20 percent of typical for 99.9 percent of devices. Cyclone III devices (second column) have been optimized another 50 percent, providing the lowest static offering of any PLD for SWaP sensitive production applications. (Figure 5 shows static power at 25°C and 85°C for the complete Cyclone III family.) Stratix II devices (third column) were optimized for performance versus power, typically outperforming their counterparts by 25 percent and providing 35 percent lower dynamic power. Altera also provides Stratix series devices in industrial and military temperature ranges with superior power capabilities. Finally, Stratix III devices (fourth column) are optimized for maximum functionality per watt with innovative features like Programmable Power Technology and voltage scaling to 0.09V for the lowest overall power, while still outperforming competitive devices.

Figure 4. Altera's Power-Optimized PLDs vs. Competing Devices

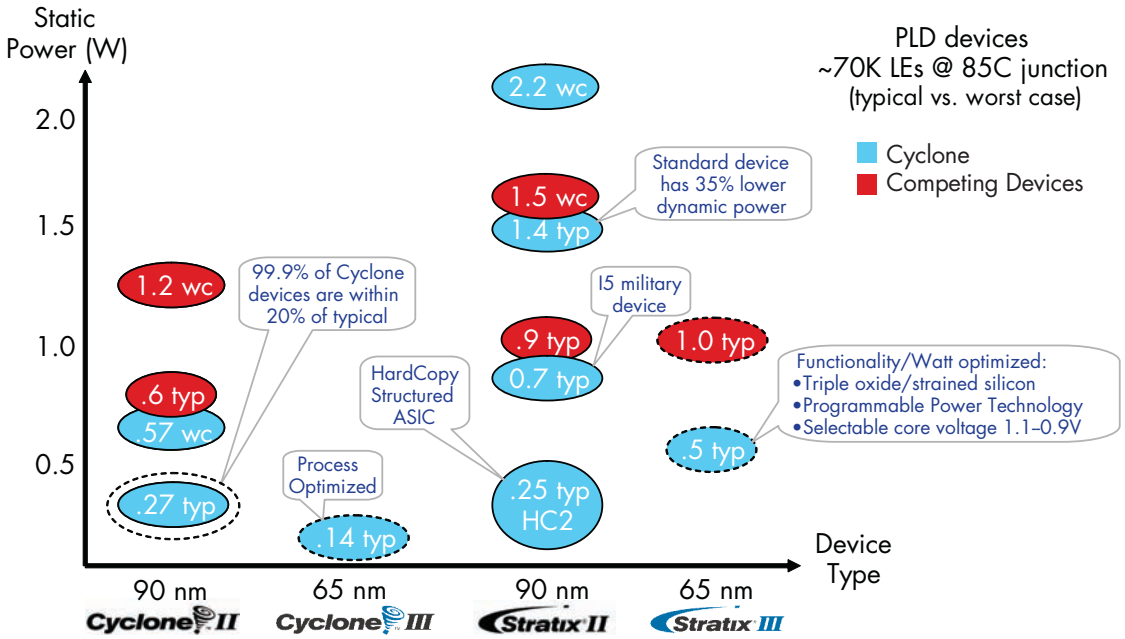
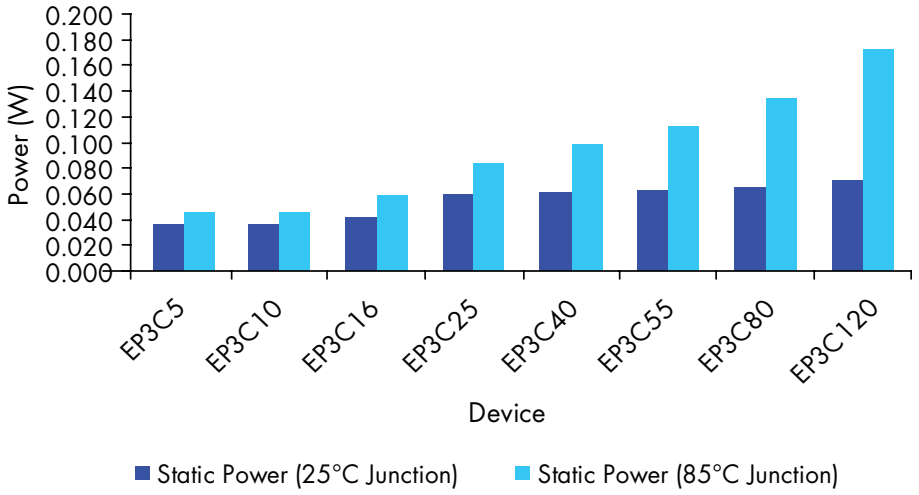


Figure 5. Cyclone III Static Power



SDR Integration Capabilities

To maximize the benefits for SWaP applications beyond power, PLDs must also provide superior integration capability. Figure 6 and Table 1 show the integration capabilities of the largest Cyclone EP3C120 device for an SDR application using advanced waveform capabilities like OFDMA and MIMO metrics. All of the bit-, symbol-, and IF-level waveform functions are implemented for the black processing portion of a 36-Mbps radio at under 200 mW (static), using 110K LEs, 500 multipliers and 3.8 Mbits of internal memory—impossible with any other low-power PLD or DSP processor.

Figure 6. Cyclone III Integration Capability Using EP3C120

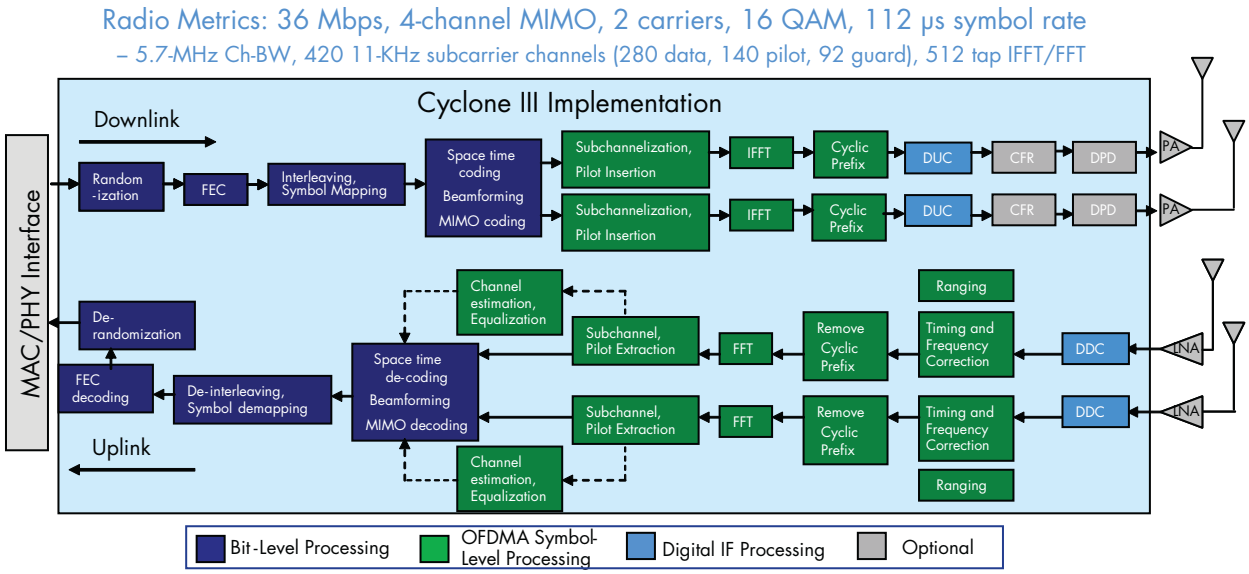


Table 1. Resource Summary

Resources	KLEs	9x9 Multipliers	M512s	M4Ks	MRAM
Interfaces	0	0	0	0	0
Nios® Processor	3.3	0	0	0	1
Bit-Level Processing	4.8	1	22	10	0
Symbol-Level Processing	64	156	4	321	0
Digital IF Processing	17.8	320	118	134	0
Control and Interfacing Overhead	18	0	0	0	0
Total	**108**	**477**	**144**	**465**	**1**

Cyclone III devices are available in the smallest possible packages and even offered in die form for special applications. The largest Cyclone III device, the EP3C120, provides 120K LEs and 3.8-Mbits embedded memory in a 23 x 23 mm package—that is, 20K more LEs in a 57 percent smaller package and one-eighth the static power of its nearest competitor. Even more important for SWaP-sensitive applications is the savings in battery size and power regulation. Due to the relaxed power needs of Cyclone III devices, instead of the large and heavy standard military brick batteries (shown in Figure 7) commonly used, much smaller cylindrical batteries can be used, yielding a 95 percent size reduction and 78 percent battery weight reduction (see Table 2).

Figure 7. Reduction in Battery Size

Table 2. Comparison of Military Batteries

SWaP	Old Battery	New Battery	Savings
Form Factor	Brick	Cylindrical	-
Size, Dimensions	12.5 cm x 11 cm x 6 cm	3 cm x 9 cm	-
Size, Volume	825 cm^3	42 cm^3	95%
Weight	1.0 Kg	0.22 Kg	78%

SDR Design Flow and Tools

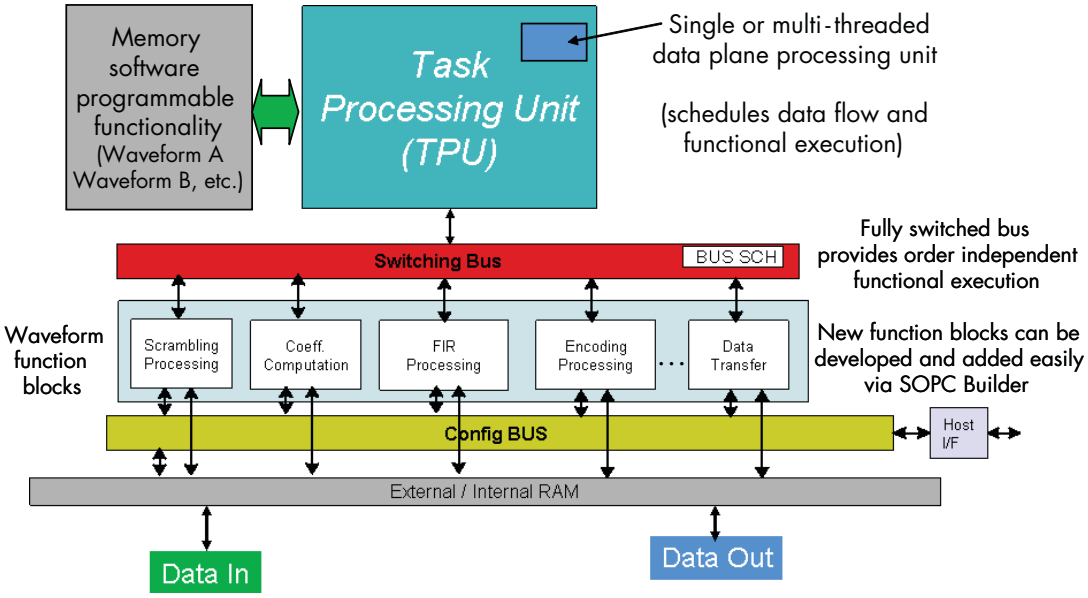
To design with confidence for SWaP, designers should leverage methodologies and tools that simplify and accelerate system design flow, integrating both newly developed intellectual property (IP) and reusing existing IP, as well as leveraging IP from FPGA and third-party vendors.

Software Programmable Reconfiguration

Software programmable reconfiguration (SPR) is a design methodology that enables the use of a variety of programmable devices (versus a single device family) across the SDR spectrum. The SPR methodology leverages Altera's SOPC Builder IP integration tool and Avalon® Streaming interface, part of the Quartus tool suite, to streamline system design for multiple application segments including packet, DSP, imaging, and radar processing.

For example, in SDR systems reconfiguration is especially important. Multiple waveforms are loaded and switched into operation, in conjunction with security subsystems that dynamically change cryptographic keys and algorithms. The SPR methodology (Figure 8) satisfies these requirements by interconnecting functional building block modules (IP blocks) required for multiple waveforms via a fully switched fabric. Then Nios II soft-core CPUs or other embedded task processors can be strategically placed wherever most efficient, to control the sequence and functionality of module operations (e.g., changing both intra- and inter-module functionality). This changes functionality in the PLD via software loads versus reloading partial hardware bit configurations, which limit designers to a single PLD family, a poor choice for SWaP-sensitive applications.

Figure 8. Software Programmable Reconfiguration



The SPR methodology is more familiar to software architects than partial reconfiguration (PR), and simplifies porting and debugging of advanced algorithms. Using SPR instead of PR, the hardware required for multiple waveforms can be verified just once as opposed to multiple times for each waveform implementation. Newly developed modules are easily added to the fabric and operated under software control, reducing verification of multiple independent waveform implementations.

With the changing requirements of SDR, an SPR methodology reduces program risk, simplifies IP reuse, and enables even lower power and lower cost solutions using Altera's FPGA-based HardCopy structured ASICs. HardCopy devices are true die shrinks (typically 70 percent smaller) of equivalent Stratix FPGA functionality, thus providing significantly lower power and cost, and even higher performance. With SPR, HardCopy devices are as flexible as other DSP and FPGA devices, yet more economically viable and power efficient.

Altera Tool Suite

For high-productivity software to assist designers in accelerating time to market, Altera's advanced tool suite offers multiple features for SWaP-sensitive SDR designs. Starting at the top of Figure 9:

1. Waveform algorithm and SDR system design can be accelerated with third-party tools from The MathWorks or Synplicity to model and evaluate high-level system trade-offs. These vendors provide synthesis of C code for CPU/DSP, as well as HDL for FPGA implementation. For example, Altera’s DSP Builder provides a blockset library of modules to map Simulink designs to Cyclone III and Stratix III devices.

2. SOPC Builder software tool automates SDR integration and reuse of new and existing waveform IP using Altera’s Avalon Streaming and Memory-Mapped interfaces. These interfaces connect Altera IP blocks, as well as provide bus sizing, interrupt control, and arbitration capabilities between blocks. User IP can be easily mapped to this fabric, enabling custom system-on-a-chip implementations in minutes via the SOPC Builder tool.

3. Quartus II design software includes new capabilities for incremental hierarchical design for waveform implementations that reduce compile times up to 70 percent, enable IP module optimizations at each design step, and streamline the methodology for SPR. Other key features for SDR designers include virtual team and project management, industry-standard SDH support, and TimeQuest timing analyzer simulation capabilities, as well as the seamless design flow to HardCopy structured ASICs.

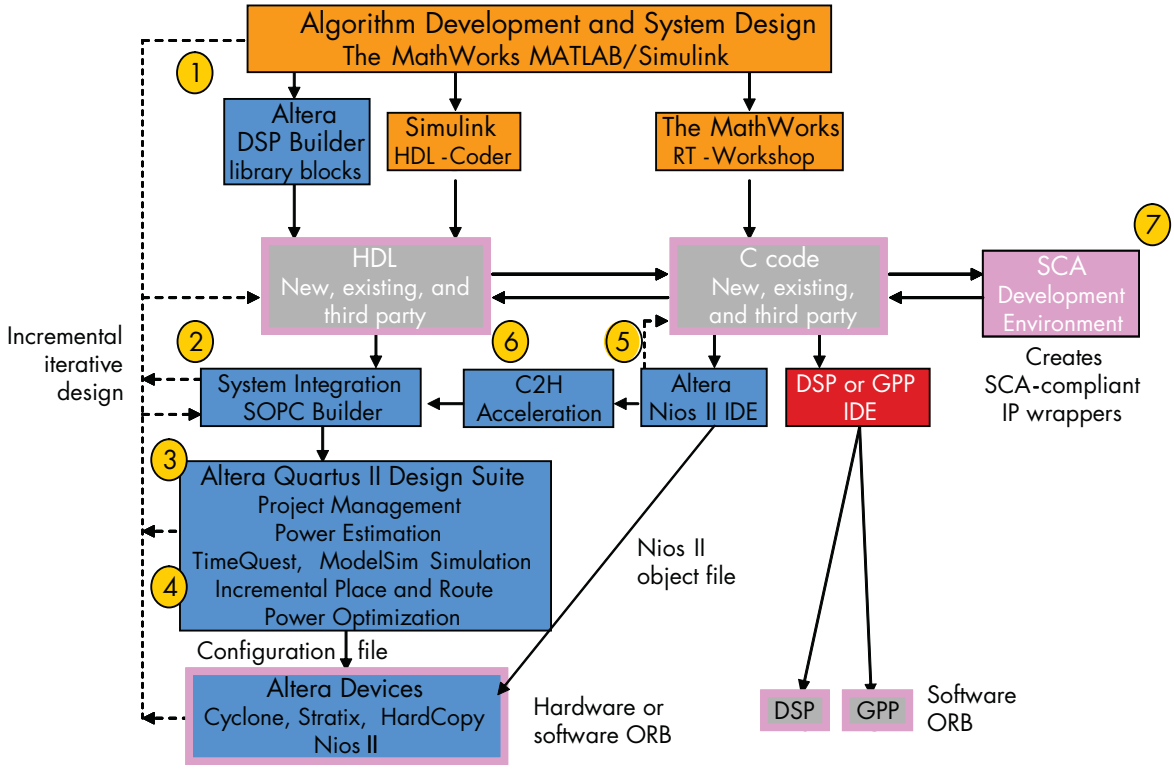
4. The PowerPlay tool suite analysis capabilities provides the most accurate power estimation and optimizations, up to 25 percent, throughout the design cycle, including pre-design estimation, pre- and post-layout simulation, and system power recommendations for low-power SDR designs.

5. Low performance legacy waveforms, as well as SCA software components can be implemented with embedded PLD CPUs. Altera's Nios II Integrated Development Environment (IDE) is a complete software tool suite for implementing one or more Nios 32-bit RISC soft-core CPUs into SDR designs. The IDE is Eclipse compatible and includes a GNU C compiler, linker, and debugger.

6. To incrementally add more performance to SDR CPU functionality, the Nios II C-to-Hardware Acceleration (C2H) Compiler accelerates application software under designer control by automatically building coprocessing modules and interconnects for existing embedded designs. Designers can profile ANSI C code and then automatically explore the performance/area trade-offs of adding hardware accelerators to their waveform design. Typical acceleration factors of 30 times are achievable with only two-to-three times more logic than the Nios CPU alone.

7. The military SDR community has adapted the SCA to provide portability of waveforms across various SDR platforms. Vendors like Prismtech, OIS, Zeligsoft, and Greenhills provide SCA components for GPP, DSP, and FPGA implementations. The pink borders indicate where SCA components affect the component design flow.

Figure 9. Productivity Tools and Design Flow for SDR SWaP With SCA Compliance

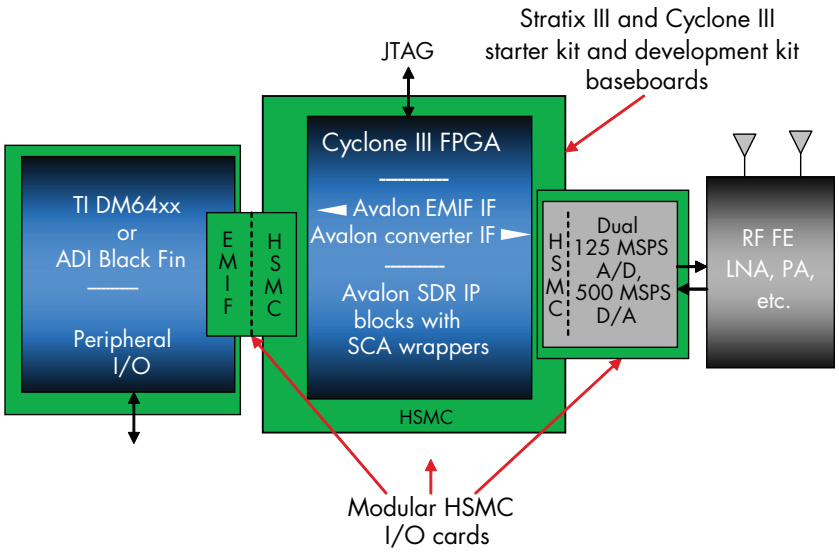


Ecosystem

To begin development of waveform and SDR application software sooner, designers can leverage modular development baseboards for Altera's PLD families. Device baseboards with high-speed I/O interfaces can extend both functionality and I/O flexibility, providing advanced prototyping capabilities for a wide variety of SWaP implementations. Altera offers both low-cost and high-capability development boards for its FPGA families, each

with high-speed mezzanine connectors (HSMC). These HSMC connectors provide flexible prototyping capabilities using Altera and third-party-developed modular daughtercards (Figure 10).

Figure 10. Altera Modular Development Kits for SDR Application-Targeted Platforms



With these I/O modules, Altera provides a wide range of platform support for SDR implementations, as well as other military imaging, DSP, and radar applications. Working with internal and third-party resources, reference designs continue to be developed to demonstrate capabilities for these applications. Altera is expanding its third-party relationships with system integrators and SCA suppliers, providing middleware, engineering, and application expertise across SDR and other military segments. For example, SDR system designers can obtain practical examples for SPR, waveform porting, and SCA compliance during 2007. Altera also partners with recognized COTS system companies, offering a wide range of industry-standard interface boards, including PCI, AMC, and VME.

Operational Excellence

Altera listens to customer input and continually improves processes to deliver the best devices, tools, and capabilities, which reduce risk and accelerate the deployment of solutions for military programs. Customer Advisory Board meetings provide direct input for next-generation silicon, while optimized business planning processes insure devices and tools meet and/or exceed product schedules, lowering device risk for military programs. Additionally, best-in-industry manufacturing partnerships and processes utilize the latest production-ready silicon technology, eliminating the program risks of using early developments in process technology.

Only Altera takes COTS silicon to the next level. Beyond SWaP solutions, Altera focuses on the special requirements of the military and aerospace markets by offering enhanced COTS (eCOTS) devices and services for military-device security encryption features for anti-tampering, bare die for MCM integration, SEU detection, availability of reliable leaded packaging and more. In addition, devices for SDR applications are qualified across industrial and military temperature ranges, including verified functionality under environmental extremes. Using eCOTS devices for defense applications ultimately enables price and life-cycle advantages, compared to dedicated military devices.

Conclusion

FPGAs continue to provide more flexibility and functionality at reduced cost. Altera's latest generation FPGAs provide an optimum solution for SWaP requirements by enabling new SDR systems with smaller footprints, lighter weight, and smaller batteries. For confident design and efficient SWaP-based SDR production implementations, explore Altera's latest 65-nm FPGAs.

Further Information

- Altera's Military Secure Communication web page:
  www.altera.com/end-markets/military-aerospace/secure/mil-secure.html
- Altera's Software Defined Radio web page:
  www.altera.com/end-markets/wireless/software/sdr/wir-sdr.html

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