



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U0F2	DQS for X8	DQS for X16	HMC Pin Assignment for DQS[ADDR2_2]	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
0		REFCLK1n					N8								
0		REFCLK1p					P8								
0		GXB TX 15n					D1								
0		GXB TX 15p					D2								
0		GXB RX 15p GXB REFCLK 15p					F2								
0		GXB RX 15n GXB REFCLK 15n					F1								
0		GXB TX 14n					H1								
0		GXB TX 14p					H2								
0		GXB RX 14p GXB REFCLK 14p					K2								
0		GXB RX 14n GXB REFCLK 14n					K1								
0		GXB TX 13n					M1								
0		GXB TX 13p					M2								
0		GXB RX 13n GXB REFCLK 13n					Q2								
0		GXB RX 13n GXB REFCLK 13n					Q1								
0		GXB TX 12n					T1								
0		GXB RX 12p GXB REFCLK 12p					V2								
0		GXB RX 12n GXB REFCLK 12n					V1								
0		GXB TX 11n					Y1								
0		GXB TX 11p					Y2								
0		GXB RX 11p GXB REFCLK 11p					AB2								
0		GXB RX 11n GXB REFCLK 11n					AB1								
0		GXB TX 10n					AD1								
0		GXB TX 10p					AD2								
0		GXB RX 10p GXB REFCLK 10p					AF2								
0		GXB RX 10n GXB REFCLK 10n					AF1								
0		REFCLK0n					U5								
0		REFCLK0p					V5								
0		TDO		TDO			Y9								
0		ASD0		DATA4			AA6								
0		TMS		TMS			AC7								
0		AS_DATA3		DATA3			AB6								
0		TCX		TCX			AB5								
0		AS_DATA2		DATA2			AC5								
0		TDI		TDI			W10								
0		AS_DATA1		DATA1			AC6								
0		DCLK		DCLK			AA8								
0		AS_DATA0 ASD0		DATA0			AD7								
0	VREFBIAND	ID		DATA5	DIFFIO_RX_B1n	DIFFIOUT_B1n	V8	DQ1B							
0	VREFBIAND	ID		DATA5	DIFFIO_TX_B2n	DIFFIOUT_B2n	V4								
0	VREFBIAND	ID		DATA8	DIFFIO_RX_B1p	DIFFIOUT_B1p	WB	DQ1B							
0	VREFBIAND	ID		DATA8	DIFFIO_TX_B2p	DIFFIOUT_B2p	V5	DQ2B							
0	VREFBIAND	ID		DATA10	DIFFIO_RX_B3n	DIFFIOUT_B3n	T8	DQS0B							
0	VREFBIAND	ID		DATA9	DIFFIO_TX_B4n	DIFFIOUT_B4n	AB4	DQ1B							
0	VREFBIAND	ID		DATA12	DIFFIO_RX_B5n	DIFFIOUT_B5n	V7	DQS1B							
0	VREFBIAND	ID		DATA11	DIFFIO_TX_B4p	DIFFIOUT_B4p	AA4								
0	VREFBIAND	ID		DATA14	DIFFIO_RX_B5n	DIFFIOUT_B5n	V10	DQ1B							
0	VREFBIAND	ID		DATA13	DIFFIO_TX_B6n	DIFFIOUT_B6n	AD4								
0	VREFBIAND	ID		CLKUSR	DIFFIO_RX_B5p	DIFFIOUT_B5p	U10	DQ1B							
0	VREFBIAND	ID		DATA15	DIFFIO_TX_B6p	DIFFIOUT_B6p	AC4	DQ1B							
0	VREFBIAND	ID		PR_DONE	DIFFIO_RX_B7n	DIFFIOUT_B7n	AA11								
0	VREFBIAND	ID		PR_READY	DIFFIO_TX_B8n	DIFFIOUT_B8n	AE6	DQ1B							
0	VREFBIAND	ID		PR_ERROR	DIFFIO_RX_B7p	DIFFIOUT_B7p	V11								
0	VREFBIAND	ID			DIFFIO_TX_B8p	DIFFIOUT_B8p	AD5	DQ1B							
0	VREFBIAND	ID			DIFFIO_TX_B25n	DIFFIOUT_B25n	AF4			GND	GND				
0	VREFBIAND	ID			DIFFIO_RX_B26n	DIFFIOUT_B26n	AE9	DQ2B		B.A.15					
0	VREFBIAND	ID			DIFFIO_TX_B26p	DIFFIOUT_B26p	AE4	DQ2B		B.VREF					
0	VREFBIAND	ID			DIFFIO_RX_B26p	DIFFIOUT_B26p	AD10	DQ2B		B.A.14					
0	VREFBIAND	ID			DIFFIO_RX_B27n	DIFFIOUT_B27n	U11	DQS2B		B.CSF.1		B.CSF.1			
0	VREFBIAND	ID			DIFFIO_TX_B27n	DIFFIOUT_B27n	AE8	DQ2B		B.A.13					
0	VREFBIAND	ID			DIFFIO_RX_B27p	DIFFIOUT_B27p	T11	DQS2B		B.CSF.0		B.CSF.0			
0	VREFBIAND	ID			DIFFIO_TX_B28n	DIFFIOUT_B28n	AE7			B.A.12					
0	VREFBIAND	ID			DIFFIO_TX_B28p	DIFFIOUT_B28p	AF9	DQ2B		B.A.11					
0	VREFBIAND	ID			DIFFIO_RX_B30n	DIFFIOUT_B30n	AE11	DQ2B		B.A.9		B.CA.9			
0	VREFBIAND	ID			DIFFIO_TX_B29p	DIFFIOUT_B29p	AE8	DQ2B		B.A.10					
0	VREFBIAND	ID			DIFFIO_RX_B30p	DIFFIOUT_B30p	AD11	DQ2B		B.A.11				B.CA.8	
0	VREFBIAND	ID	CLK0n,FPLL.BL.FBn		DIFFIO_RX_B31n	DIFFIOUT_B31n	W11			B.RAS#					
0	VREFBIAND	ID			DIFFIO_TX_B32n	DIFFIOUT_B32n	AF6	DQ2B							
0	VREFBIAND	ID	CLK0p,FPLL.BL.FBp		DIFFIO_RX_B31p	DIFFIOUT_B31p	V11								
0	VREFBIAND	ID			DIFFIO_TX_B32p	DIFFIOUT_B32p	AF5	DQ2B		B.CAF#					
0	VREFBIAND	ID			DIFFIO_TX_B33n	DIFFIOUT_B33n	AG8			GND	GND				
0	VREFBIAND	ID			DIFFIO_RX_B34n	DIFFIOUT_B34n	AF10	DQ3B		B.BA.2					
0	VREFBIAND	ID			DIFFIO_TX_B33p	DIFFIOUT_B33p	AF7	DQ3B		B.BA.0					
0	VREFBIAND	ID			DIFFIO_RX_B34p	DIFFIOUT_B34p	AF11	DQ3B		B.BA.1					
0	VREFBIAND	ID			DIFFIO_RX_B35n	DIFFIOUT_B35n	T12	DQS3B		B.CK#					
0	VREFBIAND	ID			DIFFIO_TX_B36n	DIFFIOUT_B36n	AH2	DQ3B		B.A.7		B.CA.7			
0	VREFBIAND	ID			DIFFIO_RX_B36p	DIFFIOUT_B36p	T13	DQS3B		B.CK					
0	VREFBIAND	ID			DIFFIO_TX_B36p	DIFFIOUT_B36p	AH3			B.A.6		B.CA.6			
0	VREFBIAND	ID	FPLL.BL.CLKOUT1,FPLL.BL.CLKOUTn		DIFFIO_TX_B37n	DIFFIOUT_B37n	AH4	DQ3B		B.A.3		B.CA.3			
0	VREFBIAND	ID			DIFFIO_RX_B38n	DIFFIOUT_B38n	AD12	DQ3B		B.A.4		B.CA.5			
0	VREFBIAND	ID	FPLL.BL.CLKOUT0,FPLL.BL.CLKOUTp,FPLL.BL.FB		DIFFIO_TX_B37p	DIFFIOUT_B37p	AG5	DQ3B		B.A.2		B.CA.2			
0	VREFBIAND	ID			DIFFIO_RX_B38p	DIFFIOUT_B38p	AE12	DQ3B		B.A.4		B.CA.4			
0	VREFBIAND	ID	CLK1n		DIFFIO_RX_B39n	DIFFIOUT_B39n	W12								
0	VREFBIAND	ID			DIFFIO_TX_B40n	DIFFIOUT_B40n	AH5	DQ3B		B.A.1		B.CA.1			
0	VREFBIAND	ID	CLK1p		DIFFIO_RX_B39p	DIFFIOUT_B39p	V12								
0	VREFBIAND	ID			DIFFIO_TX_B40p	DIFFIOUT_B40p	AH6	DQ3B		B.A.0		B.CA.0			
0	VREFBIAND	ID	RZ0_0		DIFFIO_TX_B41n	DIFFIOUT_B41n	AH7								
0	VREFBIAND	ID			DIFFIO_RX_B42n	DIFFIOUT_B42n	AF13	DQ4B		B.DQ.0		B.DQ.0			
0	VREFBIAND	ID			DIFFIO_TX_B41p	DIFFIOUT_B41p	AG8	DQ4B		B.DQ.2		B.DQ.2			
0	VREFBIAND	ID			DIFFIO_RX_B42p	DIFFIOUT_B42p	AG13	DQ4B		B.DQ.1		B.DQ.1			
0	VREFBIAND	ID			DIFFIO_RX_B43n	DIFFIOUT_B43n	U13	DQS4B		B.DQS.0		B.DQS.0			
0	VREFBIAND	ID			DIFFIO_TX_B43n	DIFFIOUT_B43n	AH8	DQ4B		B.DQ.3		B.DQ.3			
0	VREFBIAND	ID			DIFFIO_RX_B43p	DIFFIOUT_B43p	U14	DQS4B		B.DQS.0		B.DQS.0			
0	VREFBIAND	ID			DIFFIO_TX_B44n	DIFFIOUT_B44n	AG9			B.DQ.0		B.DQ.0			
0	VREFBIAND	ID			DIFFIO_RX_B44p	DIFFIOUT_B44p	AH9	DQ4B		B.DQ.1		B.DQ.1			
0	VREFBIAND	ID			DIFFIO_RX_B46n	DIFFIOUT_B46n	AE15	DQ4B		B.DQ.4		B.DQ.4			
0	VREFBIAND	ID			DIFFIO_TX_B45p	DIFFIOUT_B45p	AG10	DQ4B		B.DQ.6		B.DQ.6			
0	VREFBIAND	ID			DIFFIO_RX_B45n	DIFFIOUT_B45n	AF15	DQ4B		B.DQ.4		B.DQ.4			
0	VREFBIAND	ID	CLK2n		DIFFIO_RX_B47n	DIFFIOUT_B47n	AA13								
0	VREFBIAND	ID			DIFFIO_TX_B48n	DIFFIOUT_B48n	AH11	DQ4B		B.DQ.7		B.DQ.7			
0	VREFBIAND	ID	CLK2p		DIFFIO_RX_B47p	DIFFIOUT_B47p	V13								
0	VREFBIAND	ID			DIFFIO_TX_B48p	DIFFIOUT_B48p	AG11	DQ4B		B.DM.0		B.DM.0			
0	VREFBIAND	ID			DIFFIO_RX_B50n	DIFFIOUT_B50n	AG16	DQ5B		B.DQ.8		B.DQ.8			
0	VREFBIAND	ID			DIFFIO_TX_B49p	DIFFIOUT_B49p	AH12	DQ5B		B.DQ.10		B.DQ.10			
0	VREFBIAND	ID			DIFFIO_RX_B50p	DIFFIOUT_B50p	AF17	DQ5B		B.DQ.9		B.DQ.9			
0	VREFBIAND	ID			DIFFIO_RX_B51n	DIFFIOUT_B51n	V13	DQS5B		B.DQS.1		B.DQS.1			
0	VREFBIAND	ID			DIFFIO_TX_B50n	DIFFIOUT_B50n	AH13	DQ5B		B.DQ.11		B.DQ.11			
0	VREFBIAND	ID			DIFFIO_RX_B51p	DIFFIOUT_B51p	W14	DQS5B		B.DQS.1		B.DQS.1			
0	VREFBIAND	ID			DIFFIO_TX_B52n	DIFFIOUT_B52n	AG14			B.CLK.1		B.CLK.1			
0	VREFBIAND	ID			DIFFIO_TX_B53n	DIFFIOUT_B53n	AH14	DQ5B		B.CK.0		B.CK.0			
0	VREFBIAND	ID			DIFFIO_RX_B54n	DIFFIOUT_B54n	AE17	DQ5B		B.DQ.12		B.DQ.12			
0	VREFBIAND	ID			DIFFIO_TX_B53p	DIFFIOUT_B53p	AG15	DQ5B		B.DQ.14		B.DQ.14			
0	VREFBIAND	ID			DIFFIO_TX_B54p	DIFFIOUT_B54p	AD17	DQ5B		B.DQ.13		B.DQ.13			
0	VREFBIAND	ID	CLK3n		DIFFIO_RX_B55n	DIFFIOUT_B55n	AA15								
0	VREFBIAND	ID			DIFFIO_TX_B56n	DIFFIOUT_B56n	AH16	DQ5B		B.DQ.15		B.DQ.15			
0	VREFBIAND	ID	CLK3p		DIFFIO_RX_B56p	DIFFIOUT_B56p	V15								
0	VREFBIAND	ID			DIFFIO_TX_B56p	DIFFIOUT_B56p	AH17	DQ5B		B.DM.1		B.DM.1			
0	VREFBIAND	ID			DIFFIO_RX_B58n	DIFFIOUT_B58n	AD19	DQ5B		B.DQ.16		B.DQ.16			
0	VREFBIAND	ID			DIFFIO_RX_B59p	DIFFIOUT_B59p	AF18	DQ5B		B.DQ.16		B.DQ.16			
0	VREFBIAND	ID			DIFFIO_RX_B59n	DIFFIOUT_B59n	AE19	DQ5B		B.DQ.17		B.DQ.17			
0	VREFBIAND	ID			DIFFIO_RX_B60n	DIFFIOUT_B60n	AH18	DQS6B		B.DQS.2		B.DQS.2			
0	VREFBIAND	ID			DIFFIO_TX_B60n	DIFFIOUT_B60n	AH18	DQS6B		B.DQ.19		B.DQ.19			
0	VREFBIAND	ID			DIFFIO_RX_B59p	DIFFIOUT_B59p	AA19								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U02	DQS for X8	DQS for X16	HMC Pin Assignment for DDR/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
4A	VREFBIAND	ID			DIFFIO_RX_B02b	DIFFOUT_B02b	A020	DQ08		DQ18	B_DQ_20				
4A	VREFBIAND	ID			DIFFIO_TX_B01a	DIFFOUT_B01a	A019	DQ08		DQ18	B_DQ_22				
4A	VREFBIAND	ID			DIFFIO_RX_B02a	DIFFOUT_B02a	A020	DQ08		DQ18	B_DQ_21				
4A	VREFBIAND	ID			DIFFIO_TX_B04a	DIFFOUT_B04a	A020	DQ08		DQ18	B_DQ_23				
4A	VREFBIAND	ID			DIFFIO_TX_B05a	DIFFOUT_B05a	A020	DQ08		DQ18	B_DM_2				
4A	VREFBIAND	ID			DIFFIO_RX_B06a	DIFFOUT_B06a	A021	DQ07b		DQ28	B_DQ_24				
4A	VREFBIAND	ID			DIFFIO_TX_B06a	DIFFOUT_B06a	A021	DQ07b		DQ28	B_DQ_26				
4A	VREFBIAND	ID			DIFFIO_RX_B06b	DIFFOUT_B06b	A022	DQ07b		DQ28	B_DQ_25				
4A	VREFBIAND	ID			DIFFIO_TX_B07a	DIFFOUT_B07a	A022	DQ07b		DQ28	B_DQ08_3				
4A	VREFBIAND	ID			DIFFIO_TX_B07b	DIFFOUT_B07b	A021	DQ07b		DQ28	B_DQ_27				
4A	VREFBIAND	ID			DIFFIO_RX_B07b	DIFFOUT_B07b	A023	DQ07b		DQ28	B_DQ8_3				
4A	VREFBIAND	ID			DIFFIO_TX_B08a	DIFFOUT_B08a	A022	DQ07b		DQ28	QND				
4A	VREFBIAND	ID			DIFFIO_TX_B07a	DIFFOUT_B07a	A023	DQ07b		DQ28	B_DQ_28				
4A	VREFBIAND	ID			DIFFIO_TX_B09a	DIFFOUT_B09a	A023	DQ07b		DQ28	B_DQ_30				
4A	VREFBIAND	ID			DIFFIO_RX_B09a	DIFFOUT_B09a	A023	DQ07b		DQ28	B_DQ_29				
4A	VREFBIAND	ID			DIFFIO_TX_B07a	DIFFOUT_B07a	A024	DQ07b		DQ28	B_DQ_31				
4A	VREFBIAND	ID			DIFFIO_TX_B07b	DIFFOUT_B07b	A024	DQ07b		DQ28	B_DM_3				
4A	VREFBIAND	ID			DIFFIO_RX_B07a	DIFFOUT_B07a	A023	DQ08b		DQ28	B_DQ_32				
4A	VREFBIAND	ID			DIFFIO_TX_B07a	DIFFOUT_B07a	A026	DQ08b		DQ28	B_DQ_34				
4A	VREFBIAND	ID			DIFFIO_RX_B07a	DIFFOUT_B07a	A024	DQ08b		DQ28	B_DQ_33				
4A	VREFBIAND	ID			DIFFIO_RX_B07b	DIFFOUT_B07b	A023	DQ08b		DQ28	B_DQ8_4				
4A	VREFBIAND	ID			DIFFIO_TX_B07b	DIFFOUT_B07b	A026	DQ08b		DQ28	B_DQ_35				
4A	VREFBIAND	ID			DIFFIO_RX_B07b	DIFFOUT_B07b	A022	DQ08b		DQ28	B_DQ8_4				
4A	VREFBIAND	ID			DIFFIO_TX_B07b	DIFFOUT_B07b	A021	DQ08b		DQ28	QND				
4A	VREFBIAND	ID			DIFFIO_RX_B07b	DIFFOUT_B07b	A025	DQ08b		DQ28	B_DQ_36				
4A	VREFBIAND	ID			DIFFIO_TX_B07b	DIFFOUT_B07b	A028	DQ08b		DQ28	B_DQ_38				
4A	VREFBIAND	ID			DIFFIO_RX_B07b	DIFFOUT_B07b	A026	DQ08b		DQ28	B_DQ_37				
4A	VREFBIAND	ID			DIFFIO_TX_B08b	DIFFOUT_B08b	A028	DQ08b		DQ28	B_DQ_39				
4A	VREFBIAND	ID			DIFFIO_TX_B08b	DIFFOUT_B08b	A028	DQ08b		DQ28	B_DM_4				
4A	VREFBIAND	ID	RZQ_1		INT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	AA20		DQ1R					
4A	VREFBIAND	ID			PR_REQUEST	DIFFIO_TX_R1a	DIFFOUT_R1a	A026	DQ1R						
4A	VREFBIAND	ID			CRG_ERROR	DIFFIO_TX_R2b	DIFFOUT_R2b	A026	DQ1R						
4A	VREFBIAND	ID			NCIO	DIFFIO_TX_R3p	DIFFOUT_R3p	A025	DQ1R						
4A	VREFBIAND	ID				DIFFIO_RX_R4p	DIFFOUT_R4p	V17	DQ1R						
4A	VREFBIAND	ID			CIP_CONF_DONE	DIFFIO_TX_R2b	DIFFOUT_R2b	A026	DQ1R						
4A	VREFBIAND	ID			DEV_OE	DIFFIO_RX_R4b	DIFFOUT_R4b	V18	DQ1R						
4A	VREFBIAND	ID			DEV_CLRn	DIFFIO_TX_R5a	DIFFOUT_R5a	A023	DQ1R						
4A	VREFBIAND	ID			IPERST1	DIFFIO_RX_R6a	DIFFOUT_R6a	W15	DQ8n1R						
4A	VREFBIAND	ID				DIFFIO_TX_R7a	DIFFOUT_R7a	AA24	DQ1R						
4A	VREFBIAND	ID				DIFFIO_RX_R8a	DIFFOUT_R8a	V16	DQ1R						
4A	VREFBIAND	ID				DIFFIO_TX_R7b	DIFFOUT_R7b	AA23	DQ1R						
4B	VREFBIAND	ID	CLKip		DIFFIO_RX_R21p	DIFFOUT_R21p	W21								
4B	VREFBIAND	ID	FPLL_BR_CLKOUT0:FPLL_BR_CLKOUT5:FPLL_BR_FB		DIFFIO_TX_R22p	DIFFOUT_R22p	AB26								
4B	VREFBIAND	ID	CLKin		DIFFIO_TX_R19a	DIFFOUT_R19a	W20								
4B	VREFBIAND	ID	FPLL_BR_CLKOUT1:FPLL_BR_CLKOUTn		DIFFIO_TX_R22n	DIFFOUT_R22n	AA26								
4B	VREFBIAND	ID	CLK4p:FPLL_BR_FBn		DIFFIO_RX_R23p	DIFFOUT_R23p	V24								
4B	VREFBIAND	ID	CLK4n:FPLL_BR_FBn		DIFFIO_RX_R23n	DIFFOUT_R23n	W24								
4B	VREFBIAND	ID	RZQ_2		DIFFIO_TX_R24a	DIFFOUT_R24a	AB25								
4B	VREFBIAND_HPS	HPS DDR					A028				HPS_DM_4			HPS_DM_4	
4B	VREFBIAND_HPS	HPS DDR					V09				HPS_DQ_39			HPS_DQ_39	
4B	VREFBIAND_HPS	HPS DDR					V09				HPS_DQ_37			HPS_DQ_37	
4B	VREFBIAND_HPS	HPS DDR					V19				HPS_DQ_38			HPS_DQ_38	
4B	VREFBIAND_HPS	HPS DDR					V18				HPS_DQ_36			HPS_DQ_36	
4B	VREFBIAND_HPS	HPS DDR					V18				HPS_DQ8_4			HPS_DQ8_4	
4B	VREFBIAND_HPS	HPS GP13					V24								
4B	VREFBIAND_HPS	HPS DDR					V17				HPS_DQ8_4			HPS_DQ8_4	
4B	VREFBIAND_HPS	HPS DDR					V25				HPS_DQ_35			HPS_DQ_35	
4B	VREFBIAND_HPS	HPS DDR					V25				HPS_DQ_33			HPS_DQ_33	
4B	VREFBIAND_HPS	HPS DDR					V26				HPS_DQ_34			HPS_DQ_34	
4B	VREFBIAND_HPS	HPS DDR					V26				HPS_DQ_32			HPS_DQ_32	
4B	VREFBIAND_HPS	HPS GP12					AC27								
4B	VREFBIAND_HPS	HPS GP11					V16								
4B	VREFBIAND_HPS	HPS DDR					V16				HPS_DM_3			HPS_DM_3	
4B	VREFBIAND_HPS	HPS GP10					V16								
4B	VREFBIAND_HPS	HPS DDR					AA27				HPS_DQ_31			HPS_DQ_31	
4B	VREFBIAND_HPS	HPS DDR					V24				HPS_DQ_29			HPS_DQ_29	
4B	VREFBIAND_HPS	HPS DDR					V27				HPS_DQ_30			HPS_DQ_30	
4B	VREFBIAND_HPS	HPS DDR					RC24				HPS_DQ_28			HPS_DQ_28	
4B	VREFBIAND_HPS	VREFBIAND_HPS					V27								
4B	VREFBIAND_HPS	HPS DDR					V28				HPS_DQ8_3			HPS_DQ8_3	
4B	VREFBIAND_HPS	HPS DDR					V28								
4B	VREFBIAND_HPS	HPS DDR					V20				HPS_DQ8_3			HPS_DQ8_3	
4B	VREFBIAND_HPS	HPS DDR					W26				HPS_DQ_27			HPS_DQ_27	
4B	VREFBIAND_HPS	HPS DDR					R25				HPS_DQ_25			HPS_DQ_25	
4B	VREFBIAND_HPS	HPS DDR					AA28				HPS_DQ_26			HPS_DQ_26	
4B	VREFBIAND_HPS	HPS DDR					R24				HPS_DQ_24			HPS_DQ_24	
4B	VREFBIAND_HPS	HPS GP18					V28								
4B	VREFBIAND_HPS	HPS GP17					V16								
4B	VREFBIAND_HPS	HPS DDR					W28				HPS_DM_2			HPS_DM_2	
4B	VREFBIAND_HPS	HPS GP16					V17								
4B	VREFBIAND_HPS	HPS DDR					V27				HPS_DQ_23			HPS_DQ_23	
4B	VREFBIAND_HPS	HPS DDR					N07				HPS_DQ_21			HPS_DQ_21	
4B	VREFBIAND_HPS	HPS DDR					R27				HPS_DQ_22			HPS_DQ_22	
4B	VREFBIAND_HPS	HPS DDR					N06				HPS_DQ_20			HPS_DQ_20	
4B	VREFBIAND_HPS	HPS GP15					P26								
4B	VREFBIAND_HPS	HPS DDR					V19				HPS_DQ8_2			HPS_DQ8_2	
4B	VREFBIAND_HPS	HPS DDR					V28				HPS_RESETn			HPS_RESETn	
4B	VREFBIAND_HPS	HPS DDR					V18				HPS_DQ8_2			HPS_DQ8_2	
4B	VREFBIAND_HPS	HPS DDR					V28				HPS_DQ_19			HPS_DQ_19	
4B	VREFBIAND_HPS	HPS DDR					N25				HPS_DQ_17			HPS_DQ_17	
4B	VREFBIAND_HPS	HPS DDR					V28				HPS_DQ_18			HPS_DQ_18	
4B	VREFBIAND_HPS	HPS DDR					N04				HPS_DQ_16			HPS_DQ_16	
4B	VREFBIAND_HPS	HPS GP14					R28								
4B	VREFBIAND_HPS	HPS GP13					RC21								
4B	VREFBIAND_HPS	HPS DDR					P28				HPS_DM_1			HPS_DM_1	
4B	VREFBIAND_HPS	HPS GP12					R20								
4B	VREFBIAND_HPS	HPS DDR					N28				HPS_DQ_15			HPS_DQ_15	
4B	VREFBIAND_HPS	HPS DDR					M26				HPS_DQ_13			HPS_DQ_13	
4B	VREFBIAND_HPS	HPS DDR					M28				HPS_DQ_14			HPS_DQ_14	
4B	VREFBIAND_HPS	HPS DDR					M07				HPS_DQ_12			HPS_DQ_12	
4B	VREFBIAND_HPS	HPS DDR					L28				HPS_CKE_0			HPS_CKE_0	
4B	VREFBIAND_HPS	HPS DDR					R19				HPS_DQ8_1			HPS_DQ8_1	
4B	VREFBIAND_HPS	HPS DDR					R28				HPS_CKE_1			HPS_CKE_1	
4B	VREFBIAND_HPS	HPS DDR					R18				HPS_DQ8_1			HPS_DQ8_1	
4B	VREFBIAND_HPS	HPS DDR					J28				HPS_DQ_11			HPS_DQ_11	
4B	VREFBIAND_HPS	HPS DDR					K26				HPS_DQ_9			HPS_DQ_9	
4B	VREFBIAND_HPS	HPS DDR					J27				HPS_DQ_10			HPS_DQ_10	
4B	VREFBIAND_HPS	HPS DDR					K25				HPS_DQ_8			HPS_DQ_8	
4B	VREFBIAND_HPS	HPS GP11					K27								
4B	VREFBIAND_HPS	HPS GP10					M25								
4B	VREFBIAND_HPS	HPS DDR					G28				HPS_DM_0			HPS_DM_0	
4B	VREFBIAND_HPS	HPS DDR					F28				HPS_DQ_7			HPS_DQ_7	
4B	VREFBIAND_HPS	HPS DDR					K26				HPS_DQ_6			HPS_DQ_6	
4B	VREFBIAND_HPS	HPS DDR					G27				HPS_DQ_6			HPS_DQ_6	
4B	VREFBIAND_HPS	HPS DDR					K26				HPS_DQ_4			HPS_DQ_4	
4B	VREFBIAND_HPS	HPS DDR					G26				HPS_ODT_1			HPS_ODT_1	
4B	VREFBIAND_HPS	HPS DDR					R17				HPS_DQ8_0			HPS_DQ8_0	
4B	VREFBIAND_HPS	HPS DDR					R16				HPS_DQ8_0			HPS_DQ8_0	
4B	VREFBIAND_HPS	HPS DDR					D27				HPS_DQ_3			HPS_DQ_3	
4B	VREFBIAND_HPS	HPS DDR					J24				HPS_DQ_1			HPS_DQ_1	



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR#DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
6A	VREFBIAND_HPS	HPS_DDR					E28			HPS_DQ_2	HPS_DQ_2				
6A	VREFBIAND_HPS	HPS_DDR					J55			HPS_DQ_0	HPS_DQ_0				
6A	VREFBIAND_HPS	VREFBIAND_HPS					U58								
6A	VREFBIAND_HPS	HPS_DDR					C28			HPS_A_0	HPS_CA_0				
6A	VREFBIAND_HPS	HPS_DDR					B28			HPS_A_1	HPS_CA_1				
6A	VREFBIAND_HPS	HPS_DDR					Z21			HPS_A_4	HPS_CA_4				
6A	VREFBIAND_HPS	HPS_DDR					E26			HPS_A_2	HPS_CA_2				
6A	VREFBIAND_HPS	HPS_DDR					J20			HPS_A_5	HPS_CA_5				
6A	VREFBIAND_HPS	HPS_DDR					D26			HPS_A_3	HPS_CA_3				
6A	VREFBIAND_HPS	HPS_DDR					N21			HPS_A_6	HPS_CA_6				
6A	VREFBIAND_HPS	HPS_DDR					C26			HPS_A_6	HPS_CA_6				
6A	VREFBIAND_HPS	HPS_DDR					N20			HPS_C0F	HPS_C0F				
6A	VREFBIAND_HPS	HPS_DDR					R26			HPS_A_7	HPS_CA_7				
6A	VREFBIAND_HPS	HPS_DDR					H25			HPS_BA_1					
6A	VREFBIAND_HPS	HPS_DDR					A27			HPS_BA_0					
6A	VREFBIAND_HPS	HPS_DDR					O25			HPS_BA_2					
6A	VREFBIAND_HPS	HPS_DDR					A26			HPS_CAS#					
6A	VREFBIAND_HPS	HPS_DDR					A25			HPS_A15#					
6A	VREFBIAND_HPS	HPS_DDR					F26			HPS_A_8	HPS_CA_8				
6A	VREFBIAND_HPS	HPS_DDR					A24			HPS_A_10					
6A	VREFBIAND_HPS	HPS_DDR					B24			HPS_A_9					
6A	VREFBIAND_HPS	HPS_DDR					L21			HPS_CSA_0	HPS_CSA_0				
6A	VREFBIAND_HPS	HPS_DDR					D24			HPS_A_10					
6A	VREFBIAND_HPS	HPS_DDR					L20			HPS_CSA_1	HPS_CSA_1				
6A	VREFBIAND_HPS	HPS_DDR					C24			HPS_A_13					
6A	VREFBIAND_HPS	HPS_DDR					O23			HPS_A_14					
6A	VREFBIAND_HPS	HPS_DDR					E25			HPS_VEE#					
6A	VREFBIAND_HPS	HPS_DDR					F24			HPS_A_15					
6A	VREFBIAND_HPS	HPS_RDD_0					D25								
6A	VREFBIAND_HPS	GND					F23								
6A	VREFBIAND_HPS	GND					E23								
7A	VREFBIAND_HPS	HPS_HRST					A23								
7A	VREFBIAND_HPS	HPS_HPOR					H19								
7A	VREFBIAND_HPS	HPS_TDO					B23								
7A	VREFBIAND_HPS	VCC33STCLK_HPS					J18								
7A	VREFBIAND_HPS	HPS_TMS					C23								
7A	VREFBIAND_HPS	HPS_TCK					K19								
7A	VREFBIAND_HPS	HPS_HRST					C22								
7A	VREFBIAND_HPS	HPS_TDI					D22								
7A	VREFBIAND_HPS	GND					D21								
7A	VREFBIAND_HPS	HPS_PORSEL					E18								
7A	VREFBIAND_HPS	HPS_CLKI					D20								
7A	VREFBIAND_HPS	HPS_CLK2					O20								
7A	VREFBIAND_HPS	TRACE_CLK					C21					TRACE_CLK			HPS_GP048
7A	VREFBIAND_HPS	TRACE_D0					A22					TRACE_D0	SPISU_CLK	UART0_RX	HPS_GP049
7A	VREFBIAND_HPS	TRACE_D1					B21					TRACE_D1	SPISU_MOSI	UART0_TX	HPS_GP050
7A	VREFBIAND_HPS	TRACE_D2					A21					TRACE_D2	SPISU_MISO	IC1I_SDA	HPS_GP051
7A	VREFBIAND_HPS	TRACE_D3					K18					TRACE_D3	SPISU_SSD	IC1I_SCL	HPS_GP052
7A	VREFBIAND_HPS	TRACE_D4					A20					TRACE_D4	SPISU_CLK	CAN1_RX	HPS_GP053
7A	VREFBIAND_HPS	TRACE_D5					J18					TRACE_D5	SPISU_MOSI	CAN1_TX	HPS_GP054
7A	VREFBIAND_HPS	TRACE_D6					C19					TRACE_D6	SPISU_SSD	IC0L_SDA	HPS_GP055
7A	VREFBIAND_HPS	TRACE_D7					A18					TRACE_D7	SPISU_MISO	IC0L_SCL	HPS_GP056
7A	VREFBIAND_HPS	SPIM0_CLK					C17					SPIM0_CLK	IC1I_SDA	UART0_CTS	HPS_GP057
7A	VREFBIAND_HPS	SPIM0_MOSI					C17					SPIM0_MOSI	IC1I_SCL	UART0_RTS	HPS_GP058
7A	VREFBIAND_HPS	SPIM0_MISO					B18					SPIM0_MISO	CAN1_RX	UART1_CTS	HPS_GP059
7A	VREFBIAND_HPS	SPIM0_SS0/BOOTSEL0					J17					SPIM0_SS0	CAN1_TX	UART1_RTS	HPS_GP060
7A	VREFBIAND_HPS	UART0_RX					A17					UART0_RX	CAN0_RX	SPIM0_SS1	HPS_GP061
7A	VREFBIAND_HPS	UART0_TX/CLKSEL1					H17					UART0_TX	CAN0_TX	SPIM0_SS1	HPS_GP062
7A	VREFBIAND_HPS	IC0I_SDA					C19					IC0I_SDA	UART1_RX	SPIM0_CLK	HPS_GP063
7A	VREFBIAND_HPS	IC0I_SCL					B16					IC0I_SCL	UART1_TX	SPIM0_MOSI	HPS_GP064
7A	VREFBIAND_HPS	CAN1_RX					B16					CAN0_RX	UART0_RX	SPIM0_MISO	HPS_GP065
7A	VREFBIAND_HPS	CAN1_TX/CLKSEL0					C16					CAN0_TX	UART0_TX	SPIM0_SS0	HPS_GP066
7B	VREFBIAND_HPS	MAN0_ALE					A15					MAN0_ALE	RGMI1_TX_CLK	USBI_D0	HPS_GP067
7B	VREFBIAND_HPS	MAN0_CE					H15					MAN0_CE	RGMI1_TXD0	USBI_D1	HPS_GP068
7B	VREFBIAND_HPS	MAN0_CLE					J15					MAN0_CLE	RGMI1_TXD1	USBI_D2	HPS_GP069
7B	VREFBIAND_HPS	MAN0_RE					A15					MAN0_RE	RGMI1_TXD2	USBI_D3	HPS_GP070
7B	VREFBIAND_HPS	MAN0_RB					D17					MAN0_RB	RGMI1_TXD3	USBI_D4	HPS_GP071
7B	VREFBIAND_HPS	MAN0_D09					A14					MAN0_D09	RGMI1_RXD0	USBI_D5	HPS_GP072
7B	VREFBIAND_HPS	MAN0_D01					E16					MAN0_D01	RGMI1_MFIO	IC1I_SDA	HPS_GP073
7B	VREFBIAND_HPS	MAN0_D07					A13					MAN0_D07	RGMI1_MDC	IC1I_SCL	HPS_GP074
7B	VREFBIAND_HPS	MAN0_D03					J13					MAN0_D03	RGMI1_RX_CTL	USBI_D4	HPS_GP075
7B	VREFBIAND_HPS	MAN0_D04					A12					MAN0_D04	RGMI1_TX_CTL	USBI_D5	HPS_GP076
7B	VREFBIAND_HPS	MAN0_D05					H12					MAN0_D05	RGMI1_RX_CLK	USBI_D6	HPS_GP077
7B	VREFBIAND_HPS	MAN0_D06					A11					MAN0_D06	RGMI1_RXD1	USBI_D7	HPS_GP078
7B	VREFBIAND_HPS	MAN0_D07					C15					MAN0_D07	RGMI1_RXD2	USBI_D8	HPS_GP079
7B	VREFBIAND_HPS	MAN0_HIP					H6					MAN0_HIP	RGMI1_RXD3	USBI_D9	HPS_GP080
7B	VREFBIAND_HPS	MAN0_WE/BOOTSEL2					D15					MAN0_WE	USBI_D0	USBI_D0	HPS_GP081
7B	VREFBIAND_HPS	USBI_D0					A8					USBI_D0	USBI_D1	USBI_D1	HPS_GP082
7B	VREFBIAND_HPS	USBI_D1					H16					USBI_D1	USBI_D2	USBI_D2	HPS_GP083
7B	VREFBIAND_HPS	USBI_D2					A7					USBI_D2	USBI_D3	USBI_D3	HPS_GP084
7B	VREFBIAND_HPS	USBI_D3					J16					USBI_D3	USBI_D4	USBI_D4	HPS_GP085
7B	VREFBIAND_HPS	USBI_D4					H6					USBI_D4	USBI_D5	USBI_D5	HPS_GP086
7B	VREFBIAND_HPS	USBI_D5					A6					USBI_D5	USBI_D6	USBI_D6	HPS_GP087
7B	VREFBIAND_HPS	USBI_D6					C14					USBI_D6	USBI_D7	USBI_D7	HPS_GP088
7B	VREFBIAND_HPS	USBI_D7					H14					USBI_D7	USBI_D8	USBI_D8	HPS_GP089
7B	VREFBIAND_HPS	USBI_D8					B14					USBI_D8	USBI_D9	USBI_D9	HPS_GP090
7C	VREFBIAND_HPS	SDMMC_CMD					D14					SDMMC_CMD	USBI_D0		HPS_GP091
7C	VREFBIAND_HPS	SDMMC_PWREN					A5					SDMMC_PWREN	USBI_D1		HPS_GP092
7C	VREFBIAND_HPS	SDMMC_D0					C13					SDMMC_D0	USBI_D2		HPS_GP093
7C	VREFBIAND_HPS	SDMMC_D1					R6					SDMMC_D1	USBI_D3		HPS_GP094
7C	VREFBIAND_HPS	SDMMC_D4					H13					SDMMC_D4	USBI_D4		HPS_GP095
7C	VREFBIAND_HPS	SDMMC_D5					A4					SDMMC_D5	USBI_D5		HPS_GP096
7C	VREFBIAND_HPS	SDMMC_D6					H12					SDMMC_D6	USBI_D6		HPS_GP097
7C	VREFBIAND_HPS	SDMMC_D7					B4					SDMMC_D7	USBI_D7		HPS_GP098
7C	VREFBIAND_HPS	HPS_GP094					B12								
7C	VREFBIAND_HPS	SDMMC_CLK_OUT					H8					SDMMC_CLK_OUT	USBI_D8		HPS_GP099
7C	VREFBIAND_HPS	SDMMC_D2					B11					SDMMC_D2	USBI_D9		HPS_GP100
7C	VREFBIAND_HPS	SDMMC_D3					B9					SDMMC_D3	USBI_D0		HPS_GP101
7D	VREFBIAND_HPS	RGMI0_TX_CLK					E4					RGMI0_TX_CLK			HPS_GP102
7D	VREFBIAND_HPS	RGMI0_TXD0					C10					RGMI0_TXD0	USBI_D0		HPS_GP103
7D	VREFBIAND_HPS	RGMI0_TXD1					F5					RGMI0_TXD1	USBI_D1		HPS_GP104
7D	VREFBIAND_HPS	RGMI0_TXD2					C9					RGMI0_TXD2	USBI_D2		HPS_GP105
7D	VREFBIAND_HPS	RGMI0_TXD3					C4					RGMI0_TXD3	USBI_D3		HPS_GP106
7D	VREFBIAND_HPS	RGMI0_RXD0					C8					RGMI0_RXD0	USBI_D4		HPS_GP107
7D	VREFBIAND_HPS	RGMI0_RXD1					D4					RGMI0_RXD1	USBI_D5		HPS_GP108
7D	VREFBIAND_HPS	RGMI0_MDC					C7					RGMI0_MDC	USBI_D6	IC2I_SDA	HPS_GP109
7D	VREFBIAND_HPS	RGMI0_RX_CTL					F4					RGMI0_RX_CTL	USBI_D7		HPS_GP110
7D	VREFBIAND_HPS	RGMI0_TX_CTL					C9					RGMI0_TX_CTL	USBI_D8		HPS_GP111
7D	VREFBIAND_HPS	RGMI0_RX_CLK					G4					RGMI0_RX_CLK	USBI_D9		HPS_GP112
7D	VREFBIAND_HPS	RGMI0_RXD1					C5					RGMI0_RXD1	USBI_D0		HPS_GP113
7D	VREFBIAND_HPS	RGMI0_RXD2					H5					RGMI0_RXD2	USBI_D1		HPS_GP114
7D	VREFBIAND_HPS	RGMI0_RXD3					O5					RGMI0_RXD3	USBI_D2		HPS_GP115
8A	VREFBIAND	ID	CLK0p				D12								
8A	VREFBIAND	ID	CLK7n				C12								
8A	VREFBIAND	ID	FPLL_TL_CLKOUT0/FPLL_TL_CLKOUT1/FPLL_TL_FB				E8								
8A	VREFBIAND	ID	FPLL_TL_CLKOUT0/FPLL_TL_CLKOUT1n				D8								
8A	VREFBIAND	ID	CLK0n/FPLL_TL_FBn				E11								
8A	VREFBIAND	ID	CLK0n/FPLL_TL_FBn				D11								
8A	VREFBIAND	CONF_DONE	MSEL0				J10								
8A	VREFBIAND	CONF_DONE	MSEL1				H8								
8A	VREFBIAND	CONF_DONE	MSEL2				E6								
8A	VREFBIAND	CONF_DONE	MSEL3				G6								
8A	VREFBIAND	CONF_DONE	MSEL4												



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U0F2	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		MSEL4		MSEL4			K3								
		GND					F8								
		GND					A10								
		GND					K3								
		GND					AA1								
		GND					AA7								
		GND					AA2								
		GND					AA3								
		GND					AA9								
		GND					AB4								
		GND					AB27								
		GND					AB3								
		GND					AC1								
		GND					AC2								
		GND					AC3								
		GND					AD14								
		GND					AD22								
		GND					AD35								
		GND					AD3								
		GND					AD6								
		GND					AD8								
		GND					AE1								
		GND					AE16								
		GND					AE16								
		GND					AE2								
		GND					AE3								
		GND					AF34								
		GND					AF3								
		GND					AG1								
		GND					AG17								
		GND					AG2								
		GND					AG27								
		GND					AG3								
		GND					AG7								
		GND					AH10								
		GND					AH20								
		GND					B15								
		GND					B17								
		GND					B20								
		GND					B22								
		GND					B25								
		GND					B27								
		GND					B3								
		GND					B5								
		GND					B7								
		GND					C1								
		GND					C11								
		GND					C2								
		GND					C3								
		GND					D10								
		GND					D13								
		GND					D16								
		GND					D3								
		GND					E1								
		GND					E19								
		GND					E2								
		GND					E22								
		GND					E24								
		GND					E27								
		GND					E3								
		GND					E9								
		GND					F3								
		GND					F51								
		GND					G2								
		GND					G3								
		GND					H11								
		GND					H15								
		GND					H16								
		GND					H20								
		GND					H24								
		GND					H27								
		GND					H5								
		GND					H4								
		GND					H5								
		GND					H5								
		GND					H5								
		GND					J1								
		GND					J5								
		GND					J5								
		GND					J8								
		GND					J8								
		GND					K11								
		GND					K12								
		GND					K14								
		GND					K16								
		GND					K20								
		GND					K3								
		GND					K4								
		GND					K8								
		GND					L1								
		GND					L10								
		GND					L13								
		GND					L15								
		GND					L17								
		GND					L19								
		GND					L2								
		GND					L24								
		GND					L27								
		GND					L3								
		GND					L5								
		GND					L8								
		GND					L8								
		GND					M10								
		GND					M11								
		GND					M14								
		GND					M16								
		GND					M20								
		GND					M3								
		GND					M8								
		GND					N1								
		GND					N13								
		GND					N15								
		GND					N17								
		GND					N19								
		GND					N2								
		GND					N3								
		GND					N4								
		GND					P10								
		GND					P16								
		GND					P18								
		GND					P20								
		GND					P25								
		GND					P3								
		GND					P5								
		GND					P5								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U62	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					R1								
		GND					R11								
		GND					R13								
		GND					R15								
		GND					R2								
		GND					R3								
		GND					R8								
		GND					T10								
		GND					T14								
		GND					T3								
		GND					U1								
		GND					U12								
		GND					U17								
		GND					U2								
		GND					U20								
		GND					U24								
		GND					U27								
		GND					U3								
		GND					U5								
		GND					U14								
		GND					U3								
		GND					U5								
		GND					U9								
		GND					W1								
		GND					W16								
		GND					W19								
		GND					W2								
		GND					W3								
		GND					W4								
		GND					Y13								
		GND					Y14								
		GND					Y20								
		GND					Y25								
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		GND					Y26								
		GND													



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		WCCPD6B/HPS					P24								
		WCCPD7A/HPS					E21								
		WCCPD7B/HPS					E17								
		WCCPD7C/HPS					E14								
		WCCPD7D/HPS					E13								
		WCCPD8A					E10								
3A	VREFB3AND	VREFB3AND					AE5								
3B	VREFB3BND	VREFB3BND					AF12								
3A	VREFB3AND	VREFB3AND					AF16								
3A	VREFB3AND	VREFB3AND					AC06								
3B	VREFB3BND	VREFB3BND					AA26								
		VREFB7A/B/C/D/E/HPS					D19								
8A	VREFB8AND	VREFB8AND					D9								
		W0CH_GXBL					M6								
		W0CH_GXBL					R4								
		W0CL_GXBL					L4								
		W0CL_GXBL					T4								
		W0CRSTCLK/HPS					F22								
		W0REF_TL					B1								
		W0CA_FPLL					K5								
		W0CA_FPLL					R4								
		W0CA_FPLL					U4								
		W0CA_FPLL					U5								
		W0CA_FPLL					J4								
		W0CA_FPLL					AA21								
		W0C_AUX					AC21								
		W0C_AUX					AC6								
		W0C_AUX					AD15								
		W0C_AUX					E16								
		W0C_AUX					F8								
		W0C_AUX_SHARED					F21								
		W0CE_GXBL					M6								
		W0CE_GXBL					N6								
		W0CE_GXBL					R5								
		W0CE_GXBL					T5								
		W0CRLL/HPS					H23								
		W0C_HPS					U21								
		W0C_HPS					K17								
		W0C_HPS					L16								
		W0C_HPS					L18								
		W0C_HPS					M17								
		W0C_HPS					M19								
		W0C_HPS					N16								
		W0C_HPS					N19								
		W0C_HPS					P17								
		W0C_HPS					P19								

Notes:

- (1) For more information about pin definitions and pin connection guidelines, refer to the [Cyclone V Device Family Pin Connection Guidelines](#).
- (2) HPS DDR pins are for memory interface only. For the dedicated pin function corresponding with the respective memory interfaces, refer to the HMC columns.
- (3) RESET pin is only applicable for DDR3 device.



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated TriX Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DQS/ADDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
GBB_L2		GXB TX L8n					H3								
GBB_L2		GXB TX L8p					H4								
GBB_L2		GXB RX L8p.GXB REFCLK L8p					J2								
GBB_L2		GXB RX L8n.GXB REFCLK L8p					J1								
GBB_L2		GXB TX L7n					K3								
GBB_L2		GXB TX L7p					K4								
GBB_L2		GXB RX L7p.GXB REFCLK L7p					L2								
GBB_L2		GXB RX L7n.GXB REFCLK L7n					L1								
GBB_L2		GXB TX L6n					M3								
GBB_L2		GXB TX L6p					M4								
GBB_L2		GXB RX L6p.GXB REFCLK L6p					N2								
GBB_L2		GXB RX L6n.GXB REFCLK L6n					N1								
GBB_L2		REFCLKL6p					P9								
GBB_L2		REFCLKL6n					P8								
GBB_L1		REFCLKL5p					T8								
GBB_L1		REFCLKL5n					T9								
GBB_L1		GXB TX L5n					P3								
GBB_L1		GXB TX L5p					P4								
GBB_L1		GXB RX L5p.GXB REFCLK L5p					R2								
GBB_L1		GXB RX L5n.GXB REFCLK L5n					R1								
GBB_L1		GXB TX L4n					T3								
GBB_L1		GXB TX L4p					T4								
GBB_L1		GXB RX L4p.GXB REFCLK L4p					U2								
GBB_L1		GXB RX L4n.GXB REFCLK L4n					U1								
GBB_L1		GXB TX L3n					V3								
GBB_L1		GXB TX L3p					V4								
GBB_L1		GXB RX L3p.GXB REFCLK L3p					W2								
GBB_L1		GXB RX L3n.GXB REFCLK L3n					W1								
GBB_L0		GXB TX L2n					Y3								
GBB_L0		GXB TX L2p					Y4								
GBB_L0		GXB RX L2p.GXB REFCLK L2p					AA2								
GBB_L0		GXB RX L2n.GXB REFCLK L2n					AA1								
GBB_L0		GXB TX L1n					AB3								
GBB_L0		GXB TX L1p					AB4								
GBB_L0		GXB RX L1p.GXB REFCLK L1p					AC2								
GBB_L0		GXB RX L1n.GXB REFCLK L1n					AC1								
GBB_L0		GXB TX L0n					AD3								
GBB_L0		GXB TX L0p					AD4								
GBB_L0		GXB RX L0p.GXB REFCLK L0p					AE2								
GBB_L0		GXB RX L0n.GXB REFCLK L0n					AE1								
GBB_L0		REFCLKL0p					WB								
GBB_L0		REFCLKL0n					WB								
3A		TDO		TDO			AB9								
3A		nCS0		DATA4			AB8								
3A		TMS		TMS			AB9								
3A		AS_DATA3		DATA3			AC7								
3A		TCK		TCK			AC5								
3A		AS_DATA2		DATA2			AE8								
3A		TDI		TDI			UB								
3A		AS_DATA1		DATA1			AE5								
3A		CLK		CLK			U7								
3A		AS_DATA0,ASD0		DATA0			AE6								
3A	VREFBIAS0	ID		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	AE12	DD1B							
3A	VREFBIAS0	ID		DATA6	DIFFIO_TX_B0n	DIFFOUT_B0n	AE9								
3A	VREFBIAS0	ID		DATA6	DIFFIO_RX_B1p	DIFFOUT_B1p	AD11	DD1B							
3A	VREFBIAS0	ID		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	AD9	DD1B							
3A	VREFBIAS0	ID		DATA9	DIFFIO_RX_B3n	DIFFOUT_B3n	AD10	DD2n1B							
3A	VREFBIAS0	ID		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	AF10	DD1B							
3A	VREFBIAS0	ID		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	AC9	DD2n1B							
3A	VREFBIAS0	ID		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	AE11								
3A	VREFBIAS0	ID		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	AE7	DD1B							
3A	VREFBIAS0	ID		DATA13	DIFFIO_TX_B6p	DIFFOUT_B6p	AH4	DD1B							
3A	VREFBIAS0	ID		CLKUSR	DIFFIO_RX_B6p	DIFFOUT_B6p	AD7	DD1B							
3A	VREFBIAS0	ID		DATA15	DIFFIO_TX_B8p	DIFFOUT_B8p	AG3	DD1B							
3A	VREFBIAS0	ID		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	AF5								
3A	VREFBIAS0	ID		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	AG8	DD1B							
3A	VREFBIAS0	ID		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	AF4								
3A	VREFBIAS0	ID			DIFFIO_TX_B8p	DIFFOUT_B8p	AF9	DD1B							
3A	VREFBIAS0	ID			DIFFIO_TX_B9n	DIFFOUT_B9n	AG7								
3A	VREFBIAS0	ID			DIFFIO_RX_B10n	DIFFOUT_B10n	AH2	DD2n							
3A	VREFBIAS0	ID			DIFFIO_TX_B9p	DIFFOUT_B9p	AF8	DD2n							
3A	VREFBIAS0	ID			DIFFIO_RX_B10p	DIFFOUT_B10p	AG1	DD2n							
3A	VREFBIAS0	ID			DIFFIO_RX_B11n	DIFFOUT_B11n	AH12	DD2n2B							
3A	VREFBIAS0	ID			DIFFIO_TX_B10n	DIFFOUT_B10n	AG6	DD2n							
3A	VREFBIAS0	ID			DIFFIO_RX_B11p	DIFFOUT_B11p	AA12	DD2n2B							
3A	VREFBIAS0	ID			DIFFIO_TX_B12p	DIFFOUT_B12p	AF6								
3A	VREFBIAS0	ID			DIFFIO_RX_B14n	DIFFOUT_B14n	AH6	DD2n							
3A	VREFBIAS0	ID			DIFFIO_TX_B14p	DIFFOUT_B14p	AJ2	DD2n							
3A	VREFBIAS0	ID			DIFFIO_RX_B13p	DIFFOUT_B13p	AG5	DD2n							
3A	VREFBIAS0	ID			DIFFIO_TX_B14n	DIFFOUT_B14n	AJ1	DD2n							
3A	VREFBIAS0	ID			DIFFIO_RX_B15p	DIFFOUT_B15p	AD12								
3A	VREFBIAS0	ID			DIFFIO_TX_B16p	DIFFOUT_B16p	AH3	DD2n							
3A	VREFBIAS0	ID			DIFFIO_RX_B15p	DIFFOUT_B15p	AC12								
3A	VREFBIAS0	ID			DIFFIO_TX_B16p	DIFFOUT_B16p	AG2	DD2n							
3B	VREFBIAS0	ID			DIFFIO_TX_B17n	DIFFOUT_B17n	AH9								
3B	VREFBIAS0	ID			DIFFIO_RX_B18n	DIFFOUT_B18n	AG11	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_TX_B17p	DIFFOUT_B17p	AG10	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_RX_B18p	DIFFOUT_B18p	AF11	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_TX_B19n	DIFFOUT_B19n	AH3	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_RX_B20n	DIFFOUT_B20n	AK3	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_TX_B19p	DIFFOUT_B19p	AA13	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_RX_B20p	DIFFOUT_B20p	AK2								
3B	VREFBIAS0	ID			DIFFIO_TX_B21n	DIFFOUT_B21n	AK4	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_RX_B22n	DIFFOUT_B22n	AF13	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_TX_B21p	DIFFOUT_B21p	AJ4	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_RX_B22p	DIFFOUT_B22p	AE13	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_TX_B23n	DIFFOUT_B23n	AE14								
3B	VREFBIAS0	ID			DIFFIO_RX_B23p	DIFFOUT_B23p	AK5	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_TX_B23p	DIFFOUT_B23p	AD14								
3B	VREFBIAS0	ID			DIFFIO_RX_B24p	DIFFOUT_B24p	AJ5	DD3n	DD1B						
3B	VREFBIAS0	ID			DIFFIO_TX_B24p	DIFFOUT_B24p	AJ7								
3B	VREFBIAS0	ID			DIFFIO_RX_B25n	DIFFOUT_B25n	AG13	DD4n	DD1B	GND					
3B	VREFBIAS0	ID			DIFFIO_TX_B25p	DIFFOUT_B25p	AJ6	DD4n	DD1B	B_A_15					
3B	VREFBIAS0	ID			DIFFIO_RX_B26p	DIFFOUT_B26p	AG12	DD4n	DD1B	B_WEP					
3B	VREFBIAS0	ID			DIFFIO_TX_B27n	DIFFOUT_B27n	AC14	DD4n	DD1B	B_A_14					
3B	VREFBIAS0	ID			DIFFIO_RX_B27p	DIFFOUT_B27p	AK7	DD4n	DD1B	B_CSP_1					
3B	VREFBIAS0	ID			DIFFIO_TX_B28n	DIFFOUT_B28n	AK8	DD4n	DD1B	B_A_13					
3B	VREFBIAS0	ID			DIFFIO_RX_B28p	DIFFOUT_B28p	AH5	DD4n	DD1B	B_CSP_0					
3B	VREFBIAS0	ID			DIFFIO_TX_B28p	DIFFOUT_B28p	AK7			B_A_12					
3B	VREFBIAS0	ID			DIFFIO_RX_B29n	DIFFOUT_B29n	AK9	DD4n	DD1B	B_A_11					
3B	VREFBIAS0	ID			DIFFIO_TX_B29p	DIFFOUT_B29p	AH4	DD4n	DD1B	B_A_9					
3B	VREFBIAS0	ID			DIFFIO_RX_B29p	DIFFOUT_B29p	AJ9	DD4n	DD1B	B_A_10					
3B	VREFBIAS0	ID			DIFFIO_TX_B30n	DIFFOUT_B30n	AH3	DD4n	DD1B	B_A_8					
3B	VREFBIAS0	ID		CLK0n,FPLL_BL_FBn	DIFFIO_RX_B31p	DIFFOUT_B31p	AF15								
3B	VREFBIAS0	ID			DIFFIO_TX_B32n	DIFFOUT_B32n	AH8	DD4n	DD1B	B_RASP					
3B	VREFBIAS0	ID		CLK0p,FPLL_BL_FBP	DIFFIO_RX_B31p	DIFFOUT_B31p	AF14								
3B	VREFBIAS0	ID			DIFFIO_TX_B32p	DIFFOUT_B32p	AH7	DD4n	DD1B	B_CASP					
3B	VREFBIAS0	ID			DIFFIO_RX_B33n	DIFFOUT_B33n	AJ10			GND					
3B	VREFBIAS0	ID			DIFFIO_TX_B34n	DIFFOUT_B34n	AK11	DD5n	DD1B	B_BA_2					
3B	VREFBIAS0	ID			DIFFIO_RX_B34p	DIFFOUT_B34p	AH0	DD5n	DD1B	B_BA_0					
3B	VREFBIAS0	ID			DIFFIO_TX_B34p	DIFFOUT_B34p	AJ11	DD5n	DD1B	B_BA_1					
3B	VREFBIAS0	ID			DIFFIO_RX_B35n	DIFFOUT_B35n	AK6	DD5n	DD1B	B_CK					
3B	VREFBIAS0	ID			DIFFIO_TX_B35n	DIFFOUT_B35n	AK13	DD5n	DD1B	B_A_7					
3B	VREFBIAS0	ID			DIFFIO_RX_B35p	DIFFOUT_B35p	AA14	DD5n	DD1B	B_CK					
3B	VREFBIAS0	ID			DIFFIO_TX_B36n	DIFFOUT_B36n	AK12	DD5n	DD1B	B_Ck_5					
3B	VREFBIAS0	ID		FPLL_BL_CLKOUT1,FPLL_BL_CLKOUT0	DIFFIO_TX_B37n	DIFFOUT_B37n	AJ12	DD5n							



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
3B	VREFB3BN0	ID			DIFFIO_RX B39a	DIFFOUT_B39a	AH15	DQ9B							
3B	VREFB3BN0	ID			DIFFIO_TX B37a	DIFFOUT_B37a	AH12	DQ9B							
3B	VREFB3BN0	ID	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUT1,FPLL_BL_FB		DIFFIO_RX B39a	DIFFOUT_B39a	AG15	DQ9B		B.A.4				B.CA.4	
3B	VREFB3BN0	ID		CLK1n	DIFFIO_TX B37a	DIFFOUT_B37a	Y18	DQ9B							B.CA.1
3B	VREFB3BN0	ID		CLK1p	DIFFIO_RX B39a	DIFFOUT_B39a	W15	DQ9B							B.CA.1
3B	VREFB3BN0	ID		RZ0_0	DIFFIO_TX B40a	DIFFOUT_B40a	AK14	DQ9B		B.A.0				B.CA.0	
4A	VREFB4AN0	ID			DIFFIO_RX B42a	DIFFOUT_B42a	AF18	DQ9B			B.DQ.0			B.DQ.0	
4A	VREFB4AN0	ID			DIFFIO_TX B41a	DIFFOUT_B41a	AG16	DQ9B			B.DQ.2			B.DQ.2	
4A	VREFB4AN0	ID			DIFFIO_RX B42a	DIFFOUT_B42a	AE17	DQ9B			B.DQ.1			B.DQ.1	
4A	VREFB4AN0	ID			DIFFIO_RX B43a	DIFFOUT_B43a	W16	DQ9B			B.DQ9B.0			B.DQ9B.0	
4A	VREFB4AN0	ID			DIFFIO_TX B44a	DIFFOUT_B44a	AF16	DQ9B			B.DQ.3			B.DQ.3	
4A	VREFB4AN0	ID			DIFFIO_RX B43a	DIFFOUT_B43a	V16	DQ9B			B.DQ9B.0			B.DQ9B.0	
4A	VREFB4AN0	ID			DIFFIO_TX B44a	DIFFOUT_B44a	AE16	DQ9B			B.DQ0.0			B.DQ0.0	
4A	VREFB4AN0	ID			DIFFIO_TX B45a	DIFFOUT_B45a	AK16	DQ9B			B.DQ0.1			B.DQ0.1	
4A	VREFB4AN0	ID			DIFFIO_RX B46a	DIFFOUT_B46a	AH20	DQ9B			B.DQ.4			B.DQ.4	
4A	VREFB4AN0	ID			DIFFIO_TX B45a	DIFFOUT_B45a	AJ16	DQ9B			B.DQ.6			B.DQ.6	
4A	VREFB4AN0	ID			DIFFIO_RX B46a	DIFFOUT_B46a	AG21	DQ9B			B.DQ.5			B.DQ.5	
4A	VREFB4AN0	ID		CLK2n	DIFFIO_RX B47a	DIFFOUT_B47a	AB17	DQ9B		B.DQ.7				B.DQ.7	
4A	VREFB4AN0	ID		CLK2p	DIFFIO_TX B48a	DIFFOUT_B48a	AW16	DQ9B							B.DQ.7
4A	VREFB4AN0	ID			DIFFIO_TX B49a	DIFFOUT_B49a	AH17	DQ9B			B.DM.0			B.DM.0	
4A	VREFB4AN0	ID			DIFFIO_TX B49a	DIFFOUT_B49a	AH16	DQ9B			GND			GND	
4A	VREFB4AN0	ID			DIFFIO_RX B50a	DIFFOUT_B50a	AK18	DQ9B	DQ2B		B.DQ.8			B.DQ.8	
4A	VREFB4AN0	ID			DIFFIO_TX B49a	DIFFOUT_B49a	AG18	DQ9B	DQ2B		B.DQ.10			B.DQ.10	
4A	VREFB4AN0	ID			DIFFIO_RX B50a	DIFFOUT_B50a	AJ17	DQ9B	DQ2B		B.DQ.9			B.DQ.9	
4A	VREFB4AN0	ID			DIFFIO_RX B51a	DIFFOUT_B51a	W17	DQS2B	DQ2B		B.DQS2.1			B.DQS2.1	
4A	VREFB4AN0	ID			DIFFIO_TX B52a	DIFFOUT_B52a	AK19	DQ9B	DQ2B		B.DQ.11			B.DQ.11	
4A	VREFB4AN0	ID			DIFFIO_RX B51a	DIFFOUT_B51a	Y17	DQS2B	DQ2B		B.DQS.1			B.DQS.1	
4A	VREFB4AN0	ID			DIFFIO_TX B52a	DIFFOUT_B52a	AJ19	DQ9B	DQ2B		B.CKE.1			B.CKE.1	
4A	VREFB4AN0	ID			DIFFIO_TX B53a	DIFFOUT_B53a	AJ21	DQ9B	DQ2B		B.CKE.0			B.CKE.0	
4A	VREFB4AN0	ID			DIFFIO_RX B54a	DIFFOUT_B54a	AG20	DQ9B	DQ2B		B.DQ.12			B.DQ.12	
4A	VREFB4AN0	ID			DIFFIO_TX B53a	DIFFOUT_B53a	AJ20	DQ9B	DQ2B		B.DQ.14			B.DQ.14	
4A	VREFB4AN0	ID			DIFFIO_RX B54a	DIFFOUT_B54a	AF19	DQ9B	DQ2B		B.DQ.13			B.DQ.13	
4A	VREFB4AN0	ID		CLK3n	DIFFIO_RX B55a	DIFFOUT_B55a	AH17	DQ9B	DQ2B						
4A	VREFB4AN0	ID		CLK3p	DIFFIO_TX B56a	DIFFOUT_B56a	AG24	DQ9B	DQ2B		B.DQ.15			B.DQ.15	
4A	VREFB4AN0	ID			DIFFIO_RX B55a	DIFFOUT_B55a	AC18	DQ9B	DQ2B						
4A	VREFB4AN0	ID			DIFFIO_TX B56a	DIFFOUT_B56a	AG23	DQ9B	DQ2B		B.DM.1			B.DM.1	
4A	VREFB4AN0	ID			DIFFIO_TX B57a	DIFFOUT_B57a	AH22	DQ9B	DQ2B						GND
4A	VREFB4AN0	ID			DIFFIO_RX B58a	DIFFOUT_B58a	AE19	DQ9B	DQ2B		B.DQ.16			B.DQ.16	
4A	VREFB4AN0	ID			DIFFIO_TX B57a	DIFFOUT_B57a	AG23	DQ9B	DQ2B		B.DQ.18			B.DQ.18	
4A	VREFB4AN0	ID			DIFFIO_RX B59a	DIFFOUT_B59a	AE16	DQ9B	DQ2B		B.DQ.17			B.DQ.17	
4A	VREFB4AN0	ID			DIFFIO_RX B59a	DIFFOUT_B59a	AA18	DQS2B	DQS2B		B.DQS2.2			B.DQS2.2	
4A	VREFB4AN0	ID			DIFFIO_TX B60a	DIFFOUT_B60a	AK22	DQ9B	DQ2B		B.DQ.19			B.DQ.19	
4A	VREFB4AN0	ID			DIFFIO_RX B59a	DIFFOUT_B59a	Y17	DQS2B	DQS2B		B.DQS.2			B.DQS.2	
4A	VREFB4AN0	ID			DIFFIO_TX B60a	DIFFOUT_B60a	AF21	DQ9B	DQ2B		B.DQS.2			B.DQS.2	
4A	VREFB4AN0	ID			DIFFIO_TX B60a	DIFFOUT_B60a	AK21	DQ9B	DQ2B		B.RESET#			B.RESET#	
4A	VREFB4AN0	ID			DIFFIO_TX B61a	DIFFOUT_B61a	AJ22	DQ9B	DQ2B		B.DQ.20			B.DQ.20	
4A	VREFB4AN0	ID			DIFFIO_RX B62a	DIFFOUT_B62a	AF21	DQ9B	DQ2B		B.DQ.20			B.DQ.20	
4A	VREFB4AN0	ID			DIFFIO_TX B61a	DIFFOUT_B61a	AG23	DQ9B	DQ2B		B.DQ.22			B.DQ.22	
4A	VREFB4AN0	ID			DIFFIO_RX B62a	DIFFOUT_B62a	AF20	DQ9B	DQ2B		B.DQ.21			B.DQ.21	
4A	VREFB4AN0	ID			DIFFIO_RX B63a	DIFFOUT_B63a	AA19	DQ9B	DQ2B		GND			GND	
4A	VREFB4AN0	ID			DIFFIO_TX B64a	DIFFOUT_B64a	AK24	DQ9B	DQ2B		B.DQ.23			B.DQ.23	
4A	VREFB4AN0	ID			DIFFIO_TX B64a	DIFFOUT_B64a	Y18	DQ9B	DQ2B		GND			GND	
4A	VREFB4AN0	ID			DIFFIO_TX B65a	DIFFOUT_B65a	AK23	DQ9B	DQ2B		B.DM.2			B.DM.2	
4A	VREFB4AN0	ID			DIFFIO_TX B65a	DIFFOUT_B65a	AJ25	DQ9B	DQ2B		GND			GND	
4A	VREFB4AN0	ID			DIFFIO_RX B66a	DIFFOUT_B66a	AF24	DQ9B	DQ2B		B.DQ.24			B.DQ.24	
4A	VREFB4AN0	ID			DIFFIO_TX B66a	DIFFOUT_B66a	AJ24	DQ9B	DQ2B		B.DQ.26			B.DQ.26	
4A	VREFB4AN0	ID			DIFFIO_RX B66a	DIFFOUT_B66a	AF23	DQ9B	DQ2B		B.DQ.26			B.DQ.26	
4A	VREFB4AN0	ID			DIFFIO_RX B67a	DIFFOUT_B67a	AH19	DQS2B	DQS2B		B.DQS.3			B.DQS.3	
4A	VREFB4AN0	ID			DIFFIO_TX B68a	DIFFOUT_B68a	AK26	DQ9B	DQ2B		B.DQ.27			B.DQ.27	
4A	VREFB4AN0	ID			DIFFIO_RX B67a	DIFFOUT_B67a	AC20	DQS2B	DQS2B		B.DQS.3			B.DQS.3	
4A	VREFB4AN0	ID			DIFFIO_TX B68a	DIFFOUT_B68a	AJ26	DQ9B	DQ2B		GND			GND	
4A	VREFB4AN0	ID			DIFFIO_TX B69a	DIFFOUT_B69a	AH25	DQ9B	DQ2B		GND			GND	
4A	VREFB4AN0	ID			DIFFIO_RX B70a	DIFFOUT_B70a	AE23	DQ9B	DQ2B		B.DQ.28			B.DQ.28	
4A	VREFB4AN0	ID			DIFFIO_TX B69a	DIFFOUT_B69a	AG25	DQ9B	DQ2B		B.DQ.30			B.DQ.30	
4A	VREFB4AN0	ID			DIFFIO_RX B70a	DIFFOUT_B70a	AE22	DQ9B	DQ2B		B.DQ.29			B.DQ.29	
4A	VREFB4AN0	ID			DIFFIO_RX B71a	DIFFOUT_B71a	W19	DQ9B	DQ2B		GND			GND	
4A	VREFB4AN0	ID			DIFFIO_TX B72a	DIFFOUT_B72a	AK27	DQ9B	DQ2B		B.DQ.31			B.DQ.31	
4A	VREFB4AN0	ID			DIFFIO_RX B71a	DIFFOUT_B71a	V18	DQ9B	DQ2B		GND			GND	
4A	VREFB4AN0	ID			DIFFIO_TX B72a	DIFFOUT_B72a	AJ27	DQ9B	DQ2B		B.DM.3			B.DM.3	
4A	VREFB4AN0	ID			DIFFIO_TX B73a	DIFFOUT_B73a	AK29	DQ9B	DQ2B		GND			GND	
4A	VREFB4AN0	ID			DIFFIO_RX B74a	DIFFOUT_B74a	AD21	DQ10B	DQ10B		B.DQ.32			B.DQ.32	
4A	VREFB4AN0	ID			DIFFIO_TX B73a	DIFFOUT_B73a	AK28	DQ10B	DQ10B		B.DQ.34			B.DQ.34	
4A	VREFB4AN0	ID			DIFFIO_RX B74a	DIFFOUT_B74a	AD20	DQ10B	DQ10B		B.DQ.33			B.DQ.33	
4A	VREFB4AN0	ID			DIFFIO_RX B75a	DIFFOUT_B75a	AA20	DQS2B,10B	DQS2B		B.DQS2.4			B.DQS2.4	
4A	VREFB4AN0	ID			DIFFIO_TX B75a	DIFFOUT_B75a	AH27	DQ10B	DQ10B		B.DQ.35			B.DQ.35	
4A	VREFB4AN0	ID			DIFFIO_RX B75a	DIFFOUT_B75a	Y19	DQS2B,10B	DQS2B		B.DQS.4			B.DQS.4	
4A	VREFB4AN0	ID			DIFFIO_TX B76a	DIFFOUT_B76a	AG28	DQ10B	DQ10B		GND			GND	
4A	VREFB4AN0	ID			DIFFIO_RX B76a	DIFFOUT_B76a	AF26	DQ10B	DQ10B		DQ3B			DQ3B	
4A	VREFB4AN0	ID			DIFFIO_RX B76a	DIFFOUT_B76a	AC23	DQ10B	DQ10B		B.DQ.36			B.DQ.36	
4A	VREFB4AN0	ID			DIFFIO_TX B77a	DIFFOUT_B77a	AF25	DQ10B	DQ10B		B.DQ.38			B.DQ.38	
4A	VREFB4AN0	ID			DIFFIO_RX B76a	DIFFOUT_B76a	AC22	DQ10B	DQ10B		B.DQ.37			B.DQ.37	
4A	VREFB4AN0	ID			DIFFIO_RX B76a	DIFFOUT_B76a	AE21	DQ10B	DQ10B		GND			GND	
4A	VREFB4AN0	ID			DIFFIO_TX B80a	DIFFOUT_B80a	AE24	DQ10B	DQ10B		B.DQ.39			B.DQ.39	
4A	VREFB4AN0	ID			DIFFIO_RX B76a	DIFFOUT_B76a	AA21	DQ10B	DQ10B		GND			GND	
4A	VREFB4AN0	ID			DIFFIO_TX B80a	DIFFOUT_B80a	AD24	DQ10B	DQ10B		B.DM.4			B.DM.4	
5A	VREFB5AN0	ID	RZ0_1		DIFFIO_RX R1p	DIFFOUT_R1p	AG27	DQ1R							
5A	VREFB5AN0	ID		INT_DONE	DIFFIO_RX R2p	DIFFOUT_R2p	AD25	DQ1R							
5A	VREFB5AN0	ID		PR_REQUEST	DIFFIO_TX R1n	DIFFOUT_R1n	AH28	DQ1R							
5A	VREFB5AN0	ID		CRC_ERROR	DIFFIO_RX R2n	DIFFOUT_R2n	AC25	DQ1R							
5A	VREFB5AN0	ID		HCIO	DIFFIO_TX R3n	DIFFOUT_R3n	AJ29	DQ1R							
5A	VREFB5AN0	ID			DIFFIO_RX R4p	DIFFOUT_R4p	W20	DQ1R							
5A	VREFB5AN0	ID		CvP_CONFDONE	DIFFIO_TX R3n	DIFFOUT_R3n	AH29	DQ1R							
5A	VREFB5AN0	ID			DIFFIO_RX R4p	DIFFOUT_R4p	Y21	DQ1R							
5A	VREFB5AN0	ID		DEV_0E	DIFFIO_TX R5p	DIFFOUT_R5p	AE26	DQ1R							
5A	VREFB5AN0	ID		IPERSTL0	DIFFIO_RX R6p	DIFFOUT_R6p	W21	DQS1R							
5A	VREFB5AN0	ID		DEV_1L0n	DIFFIO_TX R5p	DIFFOUT_R5p	AD27	DQ1R							
5A	VREFB5AN0	ID		IPERSTL1	DIFFIO_RX R6n	DIFFOUT_R6n	W22	DQS1R							
5A	VREFB5AN0	ID			DIFFIO_TX R7p	DIFFOUT_R7p	AA25	DQ1R							
5A	VREFB5AN0	ID			DIFFIO_RX R6n	DIFFOUT_R6n	AE22	DQ1R							
5A	VREFB5AN0	ID			DIFFIO_TX R7n	DIFFOUT_R7n	AH26	DQ1R							
5A	VREFB5AN0	ID			DIFFIO_RX R6n	DIFFOUT_R6n	AB23	DQ1R							
5A	VREFB5AN0	ID			DIFFIO_TX R8p	DIFFOUT_R8p	AK24	DQ9B							
5A	VREFB5AN0	ID			DIFFIO_TX R10p	DIFFOUT_R10p	AE27	DQ2R							
5A	VREFB5AN0	ID			DIFFIO_RX R8n	DIFFOUT_R8n	AB25	DQ2R							
5A	VREFB5AN0	ID			DIFFIO_TX R10n	DIFFOUT_R10n	AE28	DQ2R							
5A	VREFB5AN0	ID			DIFFIO_RX R11p	DIFFOUT_R11p	Y23	DQ2R							
5A	VREFB5AN0	ID			DIFFIO_TX R12p	DIFFOUT_R12									







Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated TriX Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0	
7A		HPS_CLK1					D05									
7A		HPS_CLK2					D06									
7A	VREF/F87A/B7C/D0A	TRACE_CLK					B06					TRACE_CLK				HPS_GP048
7A	VREF/F87A/B7C/D0A	TRACE_D0					B07					TRACE_D0	SPIS0_CLK	UART0_RX		HPS_GP049
7A	VREF/F87A/B7C/D0A	TRACE_D1					C26					TRACE_D1	SPIS0_MOSI	UART0_TX		HPS_GP050
7A	VREF/F87A/B7C/D0A	TRACE_D2					A25					TRACE_D2	SPIS0_MISO	I2C1_SDA		HPS_GP051
7A	VREF/F87A/B7C/D0A	TRACE_D3					H03					TRACE_D3	SPIS0_SS0	I2C1_SCL		HPS_GP052
7A	VREF/F87A/B7C/D0A	TRACE_D4					A24					TRACE_D4	CAN0_RX	CAN0_RX		HPS_GP053
7A	VREF/F87A/B7C/D0A	TRACE_D6					G21					TRACE_D6	SPIS0_MOSI	CAN0_TX		HPS_GP054
7A	VREF/F87A/B7C/D0A	TRACE_D6					C24					TRACE_D6	SPIS0_SS0	I2C0_SDA		HPS_GP055
7A	VREF/F87A/B7C/D0A	TRACE_D7					E23					TRACE_D7	SPIS0_MISO	I2C0_SCL		HPS_GP056
7A	VREF/F87A/B7C/D0A	SPIM0_CLK					A23					SPIM0_CLK	I2C1_SDA	UART0_CTS		HPS_GP057
7A	VREF/F87A/B7C/D0A	SPIM0_MOSI					C22					SPIM0_MOSI	I2C1_SCL	UART0_RTS		HPS_GP058
7A	VREF/F87A/B7C/D0A	SPIM0_MISO					B23					SPIM0_MISO	CAN0_RX	UART1_CTS		HPS_GP059
7A	VREF/F87A/B7C/D0A	SPIM0_SS0/BOOTSEL0					H00					SPIM0_SS0	CAN0_TX	UART1_RTS		HPS_GP060
7A	VREF/F87A/B7C/D0A	UART0_RX					B02					UART0_RX	CAN0_RX	SPIM0_SS1		HPS_GP061
7A	VREF/F87A/B7C/D0A	UART0_TX_CLK/SEL1					G22					UART0_TX	CAN0_TX	SPIM0_SS1		HPS_GP062
7A	VREF/F87A/B7C/D0A	I2C0_SDA					C23					I2C0_SDA	UART1_RX	SPIM0_CLK		HPS_GP063
7A	VREF/F87A/B7C/D0A	I2C0_SCL					D02					I2C0_SCL	UART1_TX	SPIM0_MOSI		HPS_GP064
7A	VREF/F87A/B7C/D0A	CAN0_RX					E24					CAN0_RX	UART0_RX	SPIM0_MISO		HPS_GP065
7A	VREF/F87A/B7C/D0A	CAN0_TX_CLK/SEL0					D04					CAN0_TX	UART0_TX	SPIM0_SS0		HPS_GP066
7B	VREF/F87A/B7C/D0A	HPS					H15					NAND_ALE	OSPI_SS3			HPS_GP014
7B	VREF/F87A/B7C/D0A	NAND_CE					F20					NAND_CE	RGMI1_TXD0	USBI_D0		HPS_GP015
7B	VREF/F87A/B7C/D0A	NAND_CLE					H19					NAND_CLE	RGMI1_TXD1	USBI_D1		HPS_GP016
7B	VREF/F87A/B7C/D0A	NAND_RE					F21					NAND_RE	RGMI1_TXD2	USBI_D2		HPS_GP017
7B	VREF/F87A/B7C/D0A	NAND_RB					H18					NAND_RB	RGMI1_TXD3	USBI_D3		HPS_GP018
7B	VREF/F87A/B7C/D0A	NAND_D00					A21					NAND_D00	RGMI1_RXD0			HPS_GP019
7B	VREF/F87A/B7C/D0A	NAND_D01					B21					NAND_D01	RGMI1_MIO0	I2C1_SDA		HPS_GP020
7B	VREF/F87A/B7C/D0A	NAND_D02					E21					NAND_D02	RGMI1_MIO2	I2C1_SCL		HPS_GP021
7B	VREF/F87A/B7C/D0A	NAND_D03					H17					NAND_D03	RGMI1_RX_CTL	USBI_D4		HPS_GP022
7B	VREF/F87A/B7C/D0A	NAND_D04					A20					NAND_D04	RGMI1_TX_CTL	USBI_D5		HPS_GP023
7B	VREF/F87A/B7C/D0A	NAND_D06					G20					NAND_D06	RGMI1_RX_CLK	USBI_D6		HPS_GP024
7B	VREF/F87A/B7C/D0A	NAND_D06					B20					NAND_D06	RGMI1_RXD1	USBI_D7		HPS_GP025
7B	VREF/F87A/B7C/D0A	NAND_D07					B18					NAND_D07	RGMI1_RXD2			HPS_GP026
7B	VREF/F87A/B7C/D0A	NAND_WP					D21					NAND_WP	RGMI1_RXD3	OSPI_SS2		HPS_GP027
7B	VREF/F87A/B7C/D0A	NAND_WE/BOOTSEL2					D20					NAND_WE	OSPI_SS1			HPS_GP028
7B	VREF/F87A/B7C/D0A	OSPI_K00					C20					OSPI_K00	USBI_CLK			HPS_GP029
7B	VREF/F87A/B7C/D0A	OSPI_K01					H18					OSPI_K01	USBI_STP			HPS_GP030
7B	VREF/F87A/B7C/D0A	OSPI_K02					A19					OSPI_K02	USBI_D8			HPS_GP031
7B	VREF/F87A/B7C/D0A	OSPI_K03					E19					OSPI_K03	USBI_NXT			HPS_GP032
7B	VREF/F87A/B7C/D0A	OSPI_SS0/BOOTSEL1					A18					OSPI_SS0				HPS_GP033
7B	VREF/F87A/B7C/D0A	OSPI_CLK					H19					OSPI_CLK				HPS_GP034
7B	VREF/F87A/B7C/D0A	OSPI_SS1					C19					OSPI_SS1				HPS_GP035
7C	VREF/F87A/B7C/D0A	SDMMC_CMD					F19					SDMMC_CMD	USBI_D0			HPS_GP036
7C	VREF/F87A/B7C/D0A	SDMMC_PAREN					B17					SDMMC_PAREN	USBI_D1			HPS_GP037
7C	VREF/F87A/B7C/D0A	SDMMC_D0					G18					SDMMC_D0	USBI_D2			HPS_GP038
7C	VREF/F87A/B7C/D0A	SDMMC_D1					C17					SDMMC_D1	USBI_D3			HPS_GP039
7C	VREF/F87A/B7C/D0A	SDMMC_D4					H17					SDMMC_D4	USBI_D4			HPS_GP040
7C	VREF/F87A/B7C/D0A	SDMMC_D5					C18					SDMMC_D5	USBI_D5			HPS_GP041
7C	VREF/F87A/B7C/D0A	SDMMC_D6					G17					SDMMC_D6	USBI_D6			HPS_GP042
7C	VREF/F87A/B7C/D0A	SDMMC_D7					E18					SDMMC_D7	USBI_D7			HPS_GP043
7C	VREF/F87A/B7C/D0A	HPS_GP044					E17					SDMMC_CLK	USBI_CLK			HPS_GP044
7C	VREF/F87A/B7C/D0A	SDMMC_CCLK_OUT					A16					SDMMC_CCLK_OUT	USBI_STP			HPS_GP045
7C	VREF/F87A/B7C/D0A	SDMMC_RZ					D17					SDMMC_D2	USBI_D8			HPS_GP046
7C	VREF/F87A/B7C/D0A	SDMMC_D3					B16					SDMMC_D3	USBI_D9			HPS_GP047
7D	VREF/F87A/B7C/D0A	RGMI0_TX_CLK					F16					RGMI0_TX_CLK				HPS_GP050
7D	VREF/F87A/B7C/D0A	RGMI0_TXD0					E16					RGMI0_TXD0	USBI_D0			HPS_GP051
7D	VREF/F87A/B7C/D0A	RGMI0_TXD1					G16					RGMI0_TXD1	USBI_D1			HPS_GP052
7D	VREF/F87A/B7C/D0A	RGMI0_TXD2					D16					RGMI0_TXD2	USBI_D2			HPS_GP053
7D	VREF/F87A/B7C/D0A	RGMI0_TXD3					H16					RGMI0_TXD3	USBI_D3			HPS_GP054
7D	VREF/F87A/B7C/D0A	RGMI0_RXD0					A15					RGMI0_RXD0	USBI_D4			HPS_GP055
7D	VREF/F87A/B7C/D0A	RGMI0_MIO0					D15					RGMI0_MIO0	USBI_D5	I2C1_SDA		HPS_GP056
7D	VREF/F87A/B7C/D0A	RGMI0_MIO2					C15					RGMI0_MIO2	USBI_D6	I2C1_SCL		HPS_GP057
7D	VREF/F87A/B7C/D0A	RGMI0_RX_CTL					B15					RGMI0_RX_CTL	USBI_D7			HPS_GP058
7D	VREF/F87A/B7C/D0A	RGMI0_TX_CTL					H15					RGMI0_TX_CTL	USBI_D8			HPS_GP059
7D	VREF/F87A/B7C/D0A	RGMI0_RX_CLK					C14					RGMI0_RX_CLK	USBI_D9			HPS_GP060
7D	VREF/F87A/B7C/D0A	RGMI0_RXD1					E14					RGMI0_RXD1	USBI_STP			HPS_GP011
7D	VREF/F87A/B7C/D0A	RGMI0_RXD2					A14					RGMI0_RXD2	USBI_DK			HPS_GP012
7D	VREF/F87A/B7C/D0A	RGMI0_RXD3					H14					RGMI0_RXD3	USBI_NXT			HPS_GP013
8A	VREF/B8AND	ID	CLK7p				H15					DIFF0_T1p	DIFFOUT_T1p			
8A	VREF/B8AND	ID	CLK7n				B13					DIFF0_T1p	DIFFOUT_T9p			DDT
8A	VREF/B8AND	ID					G15					DIFF0_RX_T1p	DIFFOUT_T1p			
8A	VREF/B8AND	ID					A13					DIFF0_T1p	DIFFOUT_T2p			DDT
8A	VREF/B8AND	ID					C13					DIFF0_RX_T3p	DIFFOUT_T3p			DDT
8A	VREF/B8AND	ID	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUT5,FPLL_TL_FB				A11					DIFF0_TX_T4p	DIFFOUT_T4p			DDT
8A	VREF/B8AND	ID					B12					DIFF0_RX_T3n	DIFFOUT_T3n			DDT
8A	VREF/B8AND	ID	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUT4n				H13					DIFF0_T1n	DIFFOUT_T1n			DDT
8A	VREF/B8AND	ID					F15					DIFF0_RX_T5p	DIFFOUT_T5p			DQS1T
8A	VREF/B8AND	ID					C12					DIFF0_TX_T6p	DIFFOUT_T6p			DDT
8A	VREF/B8AND	ID					F14					DIFF0_RX_T6n	DIFFOUT_T6n			DQS0nT
8A	VREF/B8AND	ID					B11					DIFF0_TX_T6n	DIFFOUT_T6n			DDT
8A	VREF/B8AND	ID					D11					DIFF0_RX_T7p	DIFFOUT_T7p			DDT
8A	VREF/B8AND	ID					A8					DIFF0_TX_T6p	DIFFOUT_T6p			DDT
8A	VREF/B8AND	ID					D10					DIFF0_RX_T7n	DIFFOUT_T7n			DDT
8A	VREF/B8AND	ID					A8					DIFF0_TX_T8n	DIFFOUT_T8n			DDT
8A	VREF/B8AND	ID	CLK6p,FPLL_TL_FBp				K14					DIFF0_RX_T8p	DIFFOUT_T8p			DDT
8A	VREF/B8AND	ID					C7					DIFF0_TX_T10p	DIFFOUT_T10p			DDT
8A	VREF/B8AND	ID	CLK6n,FPLL_TL_FBn				J14					DIFF0_RX_T8n	DIFFOUT_T8n			DDT
8A	VREF/B8AND	ID					H7					DIFF0_TX_T10n	DIFFOUT_T10n			DDT
8A	VREF/B8AND	ID					E9					DIFF0_RX_T11p	DIFFOUT_T11p			DDT
8A	VREF/B8AND	ID					C9					DIFF0_TX_T12p	DIFFOUT_T12p			DDT
8A	VREF/B8AND	ID					D9					DIFF0_RX_T11n	DIFFOUT_T11n			DDT
8A	VREF/B8AND	ID					B8					DIFF0_TX_T12n	DIFFOUT_T12n			DDT
8A	VREF/B8AND	ID					H14					DIFF0_RX_T13p	DIFFOUT_T13p			DQS0T
8A	VREF/B8AND	ID					C10					DIFF0_TX_T14p	DIFFOUT_T14p			DDT
8A	VREF/B8AND	ID					G13					DIFF0_RX_T13n	DIFFOUT_T13n			DQS0nT
8A	VREF/B8AND	ID					C9					DIFF0_TX_T14n	DIFFOUT_T14n			DDT
8A	VREF/B8AND	ID					F13					DIFF0_RX_T15p	DIFFOUT_T15p			DDT
8A	VREF/B8AND	ID					A6					DIFF0_TX_T16p	DIFFOUT_T16p			DDT
8A	VREF/B8AND	ID					E13					DIFF0_RX_T15n	DIFFOUT_T15n			DDT
8A	VREF/B8AND	ID					H6					DIFF0_TX_T16n	DIFFOUT_T16n			DDT
8A	VREF/B8AND	ID					H8					DIFF0_RX_T17p	DIFFOUT_T17p			DDT
8A	VREF/B8AND	ID					A4					DIFF0_TX_T18p	DIFFOUT_T18p			DDT
8A	VREF/B8AND	ID					C8					DIFF0_RX_T17n	DIFFOUT_T17n			DDT
8A	VREF/B8AND	ID					A3					DIFF0_TX_T18n	DIFFOUT_T18n			DDT
8A	VREF/B8AND	ID					E12					DIFF0_RX_T19p	DIFFOUT_T19p			DDT
8A	VREF/B8AND	ID					D8					DIFF0_TX_T20p	DIFFOUT_T20p			DDT
8A	VREF/B8AND	ID					D12					DIFF0_RX_T19n	DIFFOUT_T19n			DDT
8A	VREF/B8AND	ID					C5					DIFF0_TX_T20n	DIFFOUT_T20n			DDT
8A	VREF/B8AND	ID					H13					DIFF0_RX_T21p				



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0	
BA	VREFBAND	ID			DIFFIO RX T29p	DIFFOUT T29m	K12	DQS4T	DQS2T							
BA	VREFBAND	ID			DIFFIO TX T30p	DIFFOUT T30m	D2									
BA	VREFBAND	ID			DIFFIO RX T29p	DIFFOUT T29m	J12	DQS4T	DQS2T							
BA	VREFBAND	ID			DIFFIO TX T30p	DIFFOUT T30m	I2	DQ4T	DQ2T							
BA	VREFBAND	ID			DIFFIO RX T31p	DIFFOUT T31m	G12	DQ4T	DQ2T							
BA	VREFBAND	ID			DIFFIO TX T32p	DIFFOUT T32m	E4	DQ4T	DQ2T							
BA	VREFBAND	ID			DIFFIO RX T31p	DIFFOUT T31m	G11	DQ4T	DQ2T							
BA	VREFBAND	ID			DIFFIO TX T32p	DIFFOUT T32m	D4									
BA	VREFBAND	ID			DIFFIO RX T33p	DIFFOUT T33m	K7									
BA	VREFBAND	ID			DIFFIO TX T34p	DIFFOUT T34m	E3	DQ2T	DQ2T							
BA	VREFBAND	ID			DIFFIO RX T33p	DIFFOUT T33m	K8									
BA	VREFBAND	ID			DIFFIO TX T34p	DIFFOUT T34m	E2	DQ2T	DQ2T							
BA	VREFBAND	ID			DIFFIO RX T35p	DIFFOUT T35m	G10	DQ2T	DQ2T							
BA	VREFBAND	ID			DIFFIO TX T36p	DIFFOUT T36m	E1	DQ2T	DQ2T							
BA	VREFBAND	ID			DIFFIO RX T35p	DIFFOUT T35m	F10	DQ2T	DQ2T							
BA	VREFBAND	ID			DIFFIO TX T36p	DIFFOUT T36m	D1	DQ2T	DQ2T							
BA	VREFBAND	ID			DIFFIO RX T37p	DIFFOUT T37m	J10	DQS2T	DQ2T							
BA	VREFBAND	ID			DIFFIO TX T38p	DIFFOUT T38m	E7									
BA	VREFBAND	ID			DIFFIO RX T37p	DIFFOUT T37m	J9	DQS4T	DQ2T							
BA	VREFBAND	ID			DIFFIO TX T38p	DIFFOUT T38m	E6	DQ2T	DQ2T							
BA	VREFBAND	ID			DIFFIO RX T39p	DIFFOUT T39m	F9	DQ2T	DQ2T							
BA	VREFBAND	ID			DIFFIO TX T40p	DIFFOUT T40m	G7	DQ2T	DQ2T							
BA	VREFBAND	ID			DIFFIO RX T39p	DIFFOUT T39m	F8	DQ2T	DQ2T							
BA	VREFBAND	ID			DIFFIO TX T40p	DIFFOUT T40m	F6									
BA		MSEL0		MSEL0			L5									
BA		CONF_DONE		CONF_DONE			F3									
BA		MSEL1		MSEL1			K6									
BA		HSTATUS		HSTATUS			F4									
BA		RCE		RCE			G5									
BA		MSEL2		MSEL2			C6									
BA		MSEL3		MSEL3			L7									
BA		hCONFIG		hCONFIG			J5									
BA		MSEL4		MSEL4			F9									
		GND					JF									
		GND					A12									
		GND					A17									
		GND					A2									
		GND					A22									
		GND					A27									
		GND					AA11									
		GND					AA22									
		GND					AA3									
		GND					AA4									
		GND					AA6									
		GND					AA9									
		GND					AB1									
		GND					AB19									
		GND					AB2									
		GND					AB29									
		GND					AB5									
		GND					AB7									
		GND					AC16									
		GND					AC26									
		GND					AC3									
		GND					AC4									
		GND					AC5									
		GND					AC8									
		GND					AD1									
		GND					AD2									
		GND					AD23									
		GND					AD5									
		GND					AE10									
		GND					AE20									
		GND					AE3									
		GND					AE4									
		GND					AF1									
		GND					AF12									
		GND					AF17									
		GND					AF2									
		GND					AF27									
		GND					AF3									
		GND					AG14									
		GND					AG24									
		GND					AG8									
		GND					AH1									
		GND					AH11									
		GND					AH21									
		GND					AH6									
		GND					AJ18									
		GND					AJ28									
		GND					AJ3									
		GND					AJ20									
		GND					AK15									
		GND					AK25									
		GND					AK5									
		GND					BL4									
		GND					BL19									
		GND					BL24									
		GND					BL26									
		GND					B9									
		GND					C1									
		GND					C16									
		GND					C21									
		GND					C26									
		GND					C6									
		GND					D13									
		GND					D23									
		GND					D3									
		GND					E10									
		GND					E25									
		GND					E30									
		GND					F17									
		GND					F2									
		GND					F27									
		GND					F5									
		GND					F7									
		GND					G24									
		GND					G3									
		GND					G4									
		GND					H1									
		GND					H11									
		GND					H6									
		GND					H6									
		GND					J18									
		GND					J28									
		GND					L3									
		GND					J4									
		GND					J6									
		GND					K1									
		GND					K10									
		GND					K16									
		GND					K2									
		GND					K20									
		GND					K28									
		GND					K5									



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					L11								
		GND					L13								
		GND					L15								
		GND					L17								
		GND					L19								
		GND					L22								
		GND					L3								
		GND					L4								
		GND					L6								
		GND					M1								
		GND					M10								
		GND					M12								
		GND					M14								
		GND					M16								
		GND					M18								
		GND					M2								
		GND					M20								
		GND					M29								
		GND					M5								
		GND					M7								
		GND					M8								
		GND					N11								
		GND					N13								
		GND					N16								
		GND					N17								
		GND					N19								
		GND					N26								
		GND					N3								
		GND					N4								
		GND					N6								
		GND					N8								
		GND					N9								
		GND					P1								
		GND					P10								
		GND					P12								
		GND					P14								
		GND					P16								
		GND					P18								
		GND					P2								
		GND					P20								
		GND					P5								
		GND					P7								
		GND					R11								
		GND					R13								
		GND					R15								
		GND					R17								
		GND					R3								
		GND					R30								
		GND					R4								
		GND					R6								
		GND					R8								
		GND					R9								
		GND					T1								
		GND					T10								
		GND					T12								
		GND					T14								
		GND					T15								
		GND					T16								
		GND					T2								
		GND					T20								
		GND					T27								
		GND					T5								
		GND					T7								
		GND					U11								
		GND					U13								
		GND					U15								
		GND					U17								
		GND					U21								
		GND					U29								
		GND					U3								
		GND					U4								
		GND					U6								
		GND					U9								
		GND					V1								
		GND					V10								
		GND					V12								
		GND					V14								
		GND					V19								
		GND					V2								
		GND					V21								
		GND					V5								
		GND					W7								
		GND					W11								
		GND					W13								
		GND					W18								
		GND					W28								
		GND					W3								
		GND					W4								
		GND					W6								
		GND					W9								
		GND					Y1								
		GND					Y10								
		GND					Y12								
		GND					Y14								
		GND					Y15								
		GND					Y2								
		GND					Y20								
		GND					Y25								
		GND					Y30								
		GND					Y5								
		GND					Y7								
		GND					Y8								
		GND					U22								
		GND					T18								
		VCC					M11								
		VCC					M13								
		VCC					M9								
		VCC					N10								
		VCC					N12								
		VCC					N14								
		VCC					P11								
		VCC					P10								
		VCC					R10								
		VCC					R12								
		VCC					R14								
		VCC					T11								
		VCC					T13								
		VCC					U10								
		VCC					U12								
		VCC					U14								
		VCC					U1								
		VCC					V13								
		VCC					V15								
		VCC					W10								
		VCC					W12								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCC					W14								
		VCC					Y11								
		VCC					Y13								
		VCC					Y5								
		VCC					U21								
		DNU					F1								
		DNU					G2								
		DNU					AA7								
		DNU					AD15								
		DNU					E26								
		DNU					J15								
		VCCP0M					AR10								
		VCCP0M					AA23								
		VCCP0M					J1								
		VCC0A7					HE								
		VCCIO3A					AC11								
		VCCIO3A					AD8								
		VCCIO3A					AF7								
		VCCIO3A					AG4								
		VCCIO3B					AB14								
		VCCIO3B					AD13								
		VCCIO3B					AE15								
		VCCIO3B					AJ13								
		VCCIO3B					AJ8								
		VCCIO3B					AK10								
		VCCIO4A					AA17								
		VCCIO4A					AC21								
		VCCIO4A					AD18								
		VCCIO4A					AE25								
		VCCIO4A					AF22								
		VCCIO4A					AG19								
		VCCIO4A					AH16								
		VCCIO4A					AH26								
		VCCIO4A					AJ23								
		VCCIO4A					AK20								
		VCCIO5A					AB24								
		VCCIO5A					AD28								
		VCCIO5A					AG29								
		VCCIO5B					W23								
		VCCIO5B					AA27								
		VCCIO5B					AE30								
		VCCIO6A HPS					D26								
		VCCIO6A HPS					G29								
		VCCIO6A HPS					H26								
		VCCIO6A HPS					K24								
		VCCIO6A HPS					K30								
		VCCIO6A HPS					L27								
		VCCIO6A HPS					M24								
		VCCIO6A HPS					N21								
		VCCIO6B HPS					P23								
		VCCIO6B HPS					P26								
		VCCIO6B HPS					R25								
		VCCIO6B HPS					T22								
		VCCIO6B HPS					U19								
		VCCIO6B HPS					V26								
		VCCIO7A HPS					F22								
		VCCIO7A HPS					H21								
		VCCIO7B HPS					E20								
		VCCIO7B HPS					G19								
		VCCIO7B HPS					G18								
		VCCIO7B HPS					E15								
		VCCIO7B HPS					H16								
		VCCIO8A					A7								
		VCCIO8A					B4								
		VCCIO8A					C11								
		VCCIO8A					D8								
		VCCIO8A					E5								
		VCCIO8A					F12								
		VCCIO8A					G14								
		VCCIO8A					G9								
		VCCIO8A					H6								
		VCCIO8A					J13								
		VCCPD3A					AA10								
		VCCPD3A					AC10								
		VCCPD3B4A					AB18								
		VCCPD3B4A					AB20								
		VCCPD3B4A					AC13								
		VCCPD3B4A					AC15								
		VCCPD3B4A					AC17								
		VCCPD3B4A					AC19								
		VCCPD3B4A					AD16								
		VCCPD3B4A					AE21								
		VCCPD5A					V22								
		VCCPD5A					V24								
		VCCPD5B					U23								
		VCCPD6A6B HPS					M21								
		VCCPD6A6B HPS					N22								
		VCCPD6A6B HPS					P21								
		VCCPD6A6B HPS					R20								
		VCCPD6A6B HPS					R23								
		VCCPD7A HPS					K19								
		VCCPD7B HPS					K18								
		VCCPD7C HPS					J17								
		VCCPD7D HPS					K16								
		VCCPD8A					K11								
		VCCPD8A					K13								
		VCCPD8A					L10								
		VCCPD8A					L12								
		VCCPD8A					L14								
3A	VREFB3A0	VREFB3A0					AD6								
3B	VREFB3B0	VREFB3B0					AJ15								
4A	VREFB4A0	VREFB4A0					AK17								
5A	VREFB5A0	VREFB5A0					AC24								
5B	VREFB5B0	VREFB5B0					AK23								
6A	VREFB7A7C7D0 HPS	VREFB7A7C7D0 HPS					E22								
	VREFB8A0	VREFB8A0					B10								
		VCC1 GXBL					AB6								
		VCC1 GXBL					PE								
		VCC1 GXBL					VE								
		VCC1 GXBL					LE								
		VCC1 GXBL					RE								
		VCC1 GXBL					WE								
		VCC1 CLK HPS					LD0								
		RREF TL					G1								
		VCCA FPLL					N7								
		VCCA FPLL					R7								
		VCCA FPLL					V8								
		VCCA FPLL					AA8								
		VCCA FPLL					WS								
		VCC AUX					Y22								
		VCC AUX					AB11								
		VCC AUX					AB16								
		VCC AUX					AD22								
		VCC AUX					HY0								
		VCC AUX					J16								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCC_AUX_SHARED					L21								
		VCC_GXBL					AA5								
		VCC_GXBL					ME								
		VCC_GXBL					NE								
		VCC_GXBL					TE								
		VCC_GXBL					US								
		VCC_GXBL					YE								
		VCCPLL_HPS					L21								
		VCC_HPS					U18								
		VCC_HPS					L18								
		VCC_HPS					L18								
		VCC_HPS					L20								
		VCC_HPS					M15								
		VCC_HPS					N20								
		VCC_HPS					P19								
		VCC_HPS					P17								
		VCC_HPS					P19								
		VCC_HPS					R18								
		VCC_HPS					T17								
		VCC_HPS					T19								
		VCC_HPS					U16								

Note:

- (1) For more information about pin definitions and pin connection guidelines, refer to the [Cyclone V Device Family Pin Connection Guidelines](#).
- (2) HPS DDR pins are for memory interface only. For the dedicated pin function corresponding with the respective memory interfaces, refer to the HMC columns.
- (3) RESET pin is only applicable for DDR3 device.



Pin Information for the Cyclone® V 5CSXFC6 Device  
Version 1.4

Version Number	Date	Changes Made
1.0	10/18/2012	Initial release.
1.1	1/17/2013	A pin that was marked as VCC_HPS has been corrected to VCCRSTCLK_HPS
1.2	3/25/2013	Updated the following pin names: - Changed SDMMC_CLK_IN to SDMMC_FB_CLK_IN - Changed SDMMC_CLK to SDMMC_CCLK_OUT
1.3	9/30/2014	- Remove corresponding bank number from VCCRSTCLK_HPS pin. - Changed HMC Pin Assignment for DDR3 to HMC Pin Assignment for DDR3/DDR2. - Added note 3.
1.4	12/23/2016	-Renamed SDMMC_FB_CLK_IN to HPS_GPIO44.