SOLUTION BRIEF

Data Center FPGA Heterogeneous Computing
Data Center FPGA-Based Image Processing Accelerator

CTAccel Image Processor (CIP) Running on an Intel® FPGA Greatly Improves Image Processing Performance in the Data Center

Accelerating JPEG, WebP and Lepton decoding, encoding and resizing on Intel® Xeon®-based servers by offloading all functions to the Intel FPGA.

Accelerated Functions

- JPEG to Lepton
- JPEG to WebP (M6)
- JPEG to JPEG
- JPEG to HEIF

Use Cases

- Thumbnail generation
- Resizing / cropping
- Watermarking
- Brightness / Contrast
- Sharpening
- Maincolor
- Image storage

Executive Summary

Applications that feature streaming images, processing, and storage need transcoding and image processing that keeps up with users' demands. The high-performance, powerful FPGA-based CTAccel Image Processor (CIP) benefits data centers by increasing image processing throughput, reducing computational latency, and reducing total cost of ownership (TCO). CIP redefines data center image processing with an FPGA architecture that uses massively parallel algorithms to increase computational performance.

Business Challenge: Get the Fastest Image Processing Capability with the Least Computing Resources

Internet traffic is increasing dramatically (by 24% annually[†]), and images comprise a large portion of internet data. Many companies are dealing with huge quantities of images in the data center and performing various image processing tasks (Table 1). For example, image decoding, resizing, cropping, and encoding are typical tasks that use large numbers of servers. These functions are resource intensive, and CPU performance per core is not keeping pace with demand.

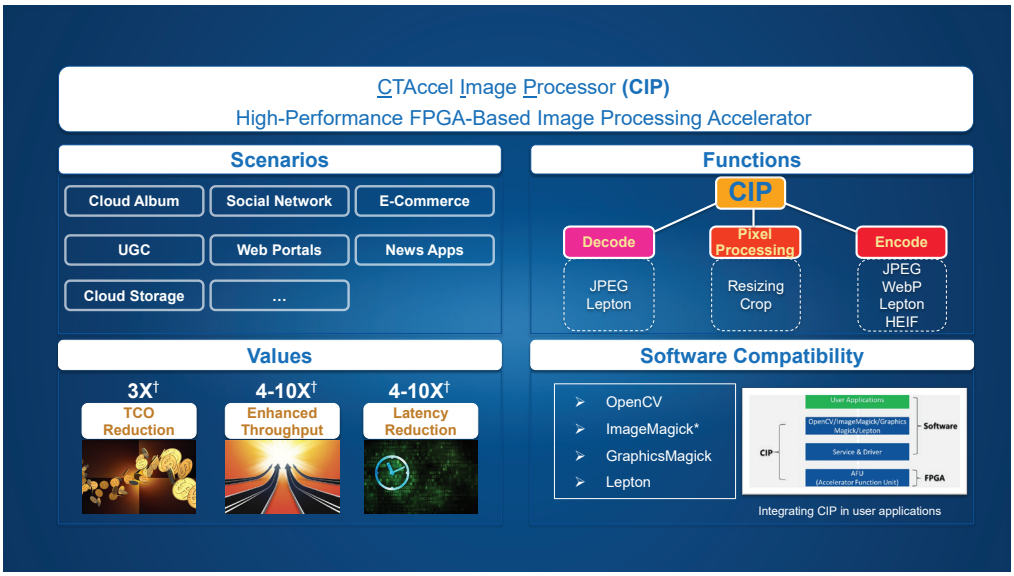
The CIP accelerator accelerates JPEG, WebP, and Lepton decoding and encoding, as well as image resizing and cropped pixel processing. The CIP accelerator effectively accelerates thumbnail generation and image transcoding, common image processing functions such as sharpening and watermarking, and image analytics.

This solution brief describes JPEG to Lepton and JPEG to WebP CIP accelerator functions.

Application	Sample Enterprises
Social Network	Facebook, Instagram, Twitter
Cloud Storage	iCloud, Dropbox, Microsoft OneDrive*
Mobile Instant Message	WhatsApp*, Snapchat*
CDN Provider	Akamai, Verizon Digital Media Services
E-Commerce	Amazon, eBay, Google

Table 1. Example Enterprises Using Image Processing

CTACCEL Accelerated Computing



Accelerating JPEG to Lepton Image Format Conversion with CIP Lepton

Lepton is an open source tool and file format for lossless compression of JPEG images. It reduces file sizes an average of 22%† yet preserves the original JPEG file, including all its metadata.

Lepton compression and decompression represent heavy computational workloads for CPUs. A conventional x86 server with dual E5-2630 processors can compress JPEG files into Lepton format at only 20 megabytes per second†.

CTAccel Image Processor Lepton (CIP Lepton) is an FPGA-based heterogeneous computing solution that offloads Lepton compression to the FPGA, increasing throughput by 3X†, shortening latency by 4X†, and reducing TCO. CIP redefines image processing in state-of-the-art data centers utilizing massively parallel data algorithms by significantly increasing their computational performance.

Accelerating JPEG to WebP Image Format Conversion with CIP WebP

WebP is a new image format for either lossless or lossy compression of web images. WebP allows web developers to create smaller, richer images for faster web pages. WebP lossy images are 25-34% smaller† than comparable JPEG images of equivalent quality.

CTAccel Image Processor WebP (CIP WebP) is an FPGA-based image processing acceleration solution that greatly improves image processing and analytics performance by transfering the CPU workload to the FPGA. CIP's powerful processing capability increases data center image processing throughput 3-4X†, reduces computational latency by 3X†, and reduces TCO.

High Performance

Increased server throughput up to 4-10X† while reducing latency is made possible by offloading all JPEG decoding, pixel-level processing, and encoding to the FPGA

Low Power

With the FPGA consuming only 20 watts†, the CIP can drastically increase compute density, translating to reduced TCO

Software Compatible

CIP is compatible with the most popular image processing software: ImageMagick*, OpenCV*, GraphicsMagick, Lepton*, and HEIF; without the need for any system software modifications

Ease of Maintenance

The FPGA accelerator can be reconfigured remotely, to easily optimize the performance of any custom usage scenario

System Configuration

The CIP accelerator features an Intel® Programmable Acceleration Card with Intel Arria® 10 GX FPGA. CTAccel used the system configurations shown in Figure 1 to generate the metrics cited in this solution brief.

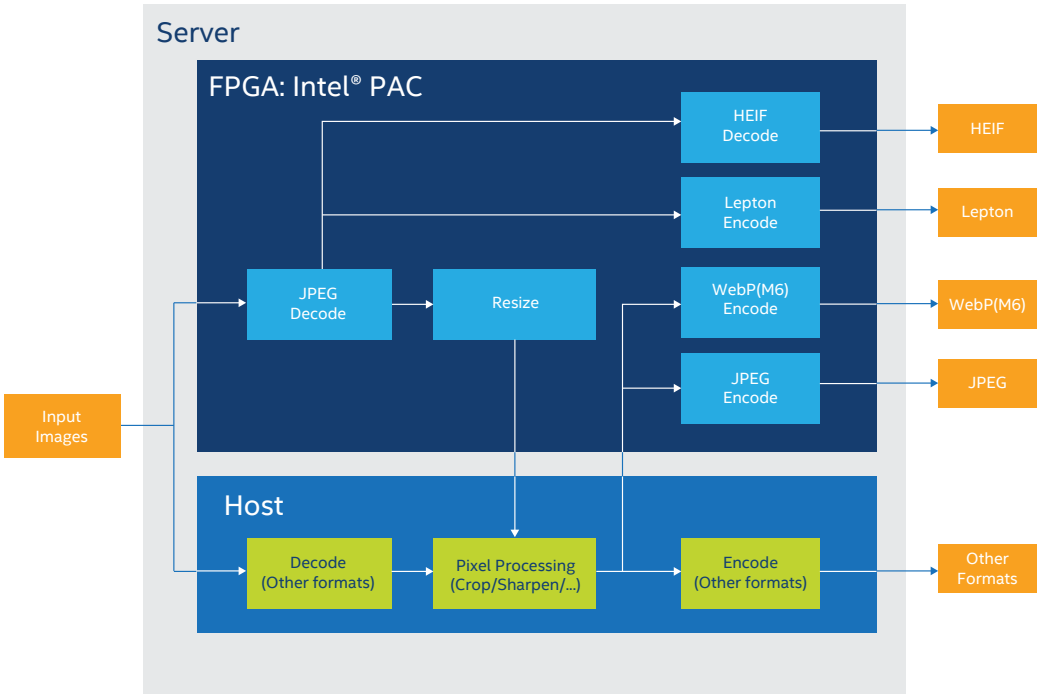


Figure 1. System Configuration

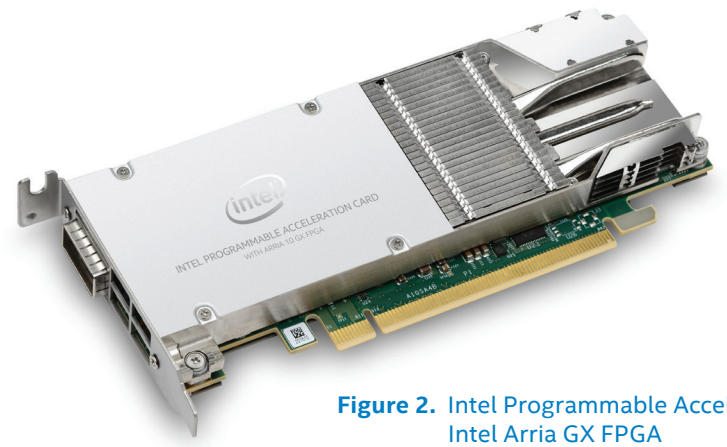


Figure 2. Intel Programmable Acceleration Card with Intel Arria GX FPGA

Function	JPEG to WebP	JPEG to Lepton	JPEG to JPEG
CPU	Two Intel® Xeon® E5-2680 v4	Two Intel® Xeon® E5-2680 v4	Two Intel® Xeon® E5-2680 v4
RAM	128 GB	128 GB	128 GB
Operating System	CentOS v7.2.1511	CentOS v7.2.1511	CentOS v7.2.1511
Kernel	3.10.0-514.2.2.el7.x86_64	3.10.0-514.2.2.el7.x86_64	3.10.0-514.2.2.el7.x86_64
Input	10,000 - 1024 x 768 images 10,000 - 4096 x 2160 images	10,000 - 1024 x 768 images	10,000 images 1024 x 768 input, 240 x 180 output

Table 2. System Configuration for Metrics

Solution Value

Adding an FPGA to an already powerful CPU provides compelling advantages. While a graphics processing unit (GPU) architecture can be ideal for some video applications, it is not as effective a computing platform for image processing.

The CIPs high-performance processing capabilities increase image processing throughput, reduce computational latency, and TCO. The customer benefits from the CIP include:

- Reduces TCO by 3X†
- Increases image processing throughput by 4-10X†
- Reduces computational latency by 4-10X†

Figure 3 illustrates the CIP's overall solution architecture. CTAccel provides powerful functions for customers who have heavy image processing loads and want to accelerate functions, such as image transcoding, JPEG thumbnail generation, sharpening, main color, watermarking, and brightness and contrast adjustments.

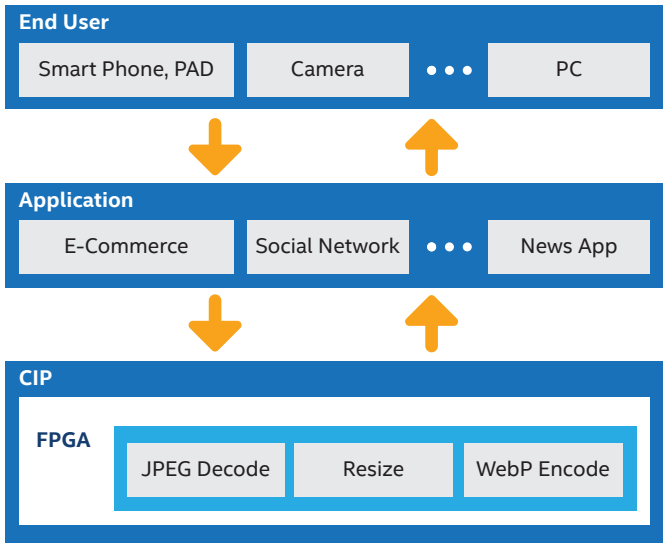


Figure 3. Solution Architecture (Example)

Conclusion

The high-performance FPGA-based CIP helps customers improve image processing performance by transferring computational workloads from CPUs to FPGAs. This increases image processing throughput, reduces computational latency, and TCO.

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- Learn more about Intel® IoT Gateway solutions at http://www.intel.com/content/www/us/en/internet-of-things/gateway-solutions.html

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