Architecture Brief

MEASURABLE ADVANTAGE™

What is an SoC FPGA?

Introduction

Processors and FPGAs (field-programmable gate arrays) are the hardworking cores of most embedded systems. Integrating the high-level management functionality of processors and the stringent, real-time operations, extreme data processing, or interface functions of an FPGA (Field Programmable Gate Array) into a single device forms an even more powerful embedded computing platform.

This Architecture Brief is designed to help system architects, engineers and managers decide if SoC FPGAs are a potential fit for their application.

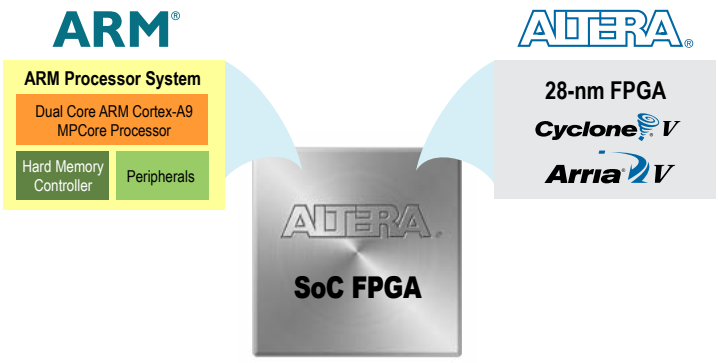
Key aspects of this paper are highlighted in an on-line video series, "A Look Inside: SoC FPGAs".

SoC FPGA devices integrate both processor and FPGA architectures into a single device. Consequently, they provide higher integration, lower power, smaller board size, and higher bandwidth communication between the processor and FPGA. They also include a rich set of peripherals, on-chip memory, an FPGA-style logic array, and high speed transceivers.

SoC FPGAs Available Today

At present, there are three sets of SoC FPGAs available on the market, as shown in Table 1. The processors in these devices are fully dedicated, "hardened" processor subsystems (not a soft IP core implemented in the FPGA fabric).

The Altera Soc FPGA model is illustrated below.



ARM + Altera = SoC FPGAs

All three industry product lines employ a full-featured ARM® processor with a memory hierarchy and dedicated peripherals that largely boot, run, and act like any "normal" ARM processor.

Table 1: Commercially-Available SoC FPGA Devices

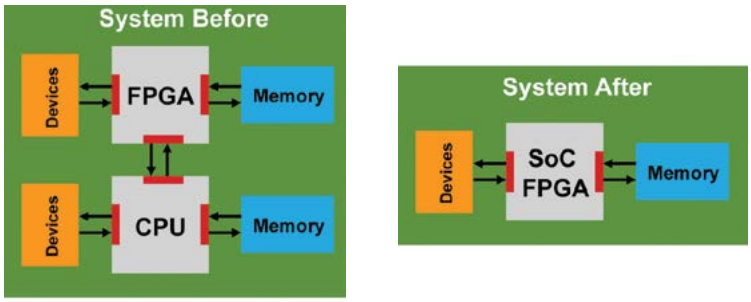
	Altera SoC	Xilinx Zynq 7000 EPP	Microsemi SmartFusion2
Processor	ARM Cortex-A9	ARM Cortex-A9	ARM Cortex-M3
Processor Class	Application processor	Application processor	Microcontroller
Single or Dual Core	Single or Dual	Dual	Single
Processor Max. Frequency	1.05 GHz	1.0 GHz	166 MHz
L1 Cache	Data: 32 KB Instruction: 32 KB	Data: 32 KB Instruction: 32 KB	No data cache Instruction: 8 KB
L2 Cache	Unified: 512 KB, with Error Correction Code	Unified: 512 KB	Not Available
Memory Management Unit (MMU)	Yes	Yes	Yes
Floating Point Unit/NEON Multimedia Engine	Yes	Yes	Not available
Acceleration Coherency Port (ACP)	Yes	Yes	Not available
Interrupt Controller	Generic (GIC)	Generic (GIC)	Nested, vectored (NVIC)
On-Chip Processor RAM	64 KB, with ECC	256 KB, no ECC	64 KB, no ECC
Direct Memory Access Controller	8-channel ARM DMA330 32 peripheral requests (FPGA + hard processor system	8-channel ARM DMA330 4 peripheral requests (FPGA only)	1-channel HPDMA 4 requests
External Memory Controller	Yes	Yes	Yes
Memory Types Supported	LPDDR2, DDR2, DDR3L, DDR3	LPDDR2, DDR2, DDR3L, DDR3	LPDDR, DDR2, DDR3
External Memory ECC	16 bit, 32 bit	16-bit	8 bit, 16 bit, 32 bit
External Memory Bus Max. Frequency	400 MHz (Cyclone V SoC), 533 MHz (Arria V SoC)	667 MHz	333 MHz
Processor Peripherals	1x Quad SPI controller 1x NAND controller 2x 10/100/1G Ethernet controller 2x USB 2.0 On the Go (OTG) controller 1x SD/MMC/SDIO controller 2x UART 4x I^2C controller 2x CAN controller 2x SPI master, 2x SPI slave controller 4x 32 bit general-purpose timers 2x 32 bit watchdog timers	1x Quad SPI controller 1x static memory controller (NAND, NOR, or SSRAM) 2x 10/100/1G Ethernet controller 2x USB 2.0 OTG controller 2x SD/SDIO controller 2x UART 2x I^2C controller 2x CAN controller 2x SPI controllers (master or slave) 2x 16 bit triple-mode timer/counters 1x 24 bit watchdog timer	1x 10/100/1G Ethernet controller 2x USB 2.0 OTG controller 2x UART 2x I^2C controller 1x CAN controller 2x SPI 2x general-purpose timers 1x watchdog timer 1x real-time clock (RTC)
FPGA Fabric	Cyclone V, Arria V	Artix-7, Kintex-7	Fusion2
FPGA Logic Density Range	25 K to 462 K LE	28K to 444 K LC	6 K to 146 K LE
Hardened Memory Controllers in FPGA	Up to 3, with ECC	Not available	Not available
High-speed Transceivers	Available at all densities	Higher-density devices only	Higher-density devices only
Analog Mixed Signal (AMS)	Not available	2 x 12-bit, 1 MSPS analog-to-digital converters (ADCs)	Not available
Boot Sequence	Processor first, FPGA first, or both simultaneous	Processor first	Processor first

To assess if an SoC FPGA make sense for an upcoming design, consider three questions:

1. Does the existing design use an FPGA and a separate microprocessor?

For designs that already use an FPGA and a separate microprocessor or DSP, an SoC FPGA should definitely be considered. It is likely to provide comparable, even superior functionality and performance, but at a lower board space, lower power, and lower system cost—as much as 50% less (see below).

Standalone processor (or DSP) and FPGA integrated into single SoC FPGA



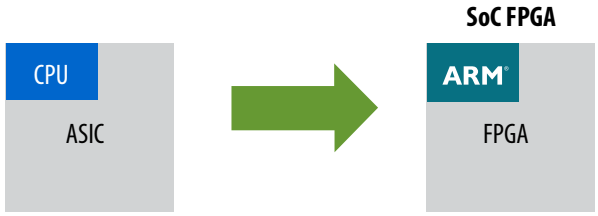
Integrating these technologies on the same piece of silicon eliminates the cost of one of the plastic packages, and saves board space. If both the CPU and FPGA use separate external memories, it may also be possible to consolidate both into one memory device, for further savings.

As the signals between the processor and the FPGA now reside on the same silicon, communication between the two consumes substantially less power compared to using separate chips. The integration of thousands of internal connections between the processor and the FPGA leads to substantially higher bandwidth and lower latency compared to a two-chip solution.

2. Does the current generation use a proprietary ASIC that includes a microprocessor?

Previously, the lack of an ARM processor had been a barrier to using FPGA technology for full production, but this new breed of SoC FPGAs delivers a fully-functional, fully-compatible, high-performance, dual-core ARM Cortex-A9 processor running up to 1GHz with today's 28nm process technology.

ASIC with CPU migrated to ARM-based SoC FPGA



SoC FPGAs leverage traditional FPGA advantages over standard ASIC technology, such as:

- No expensive NRE charges or minimum purchase requirements, for a single, SoC FPGA, or millions of devices, cost-effectively;
- Faster time to market. Devices are available off-the-shelf;
- Lower risk. The SoC FPGA can be reprogrammed at any time, even after shipping;
- Adaptable to changing markets requirements and standards, supporting for in-field updates and upgrades ;
- No additional licensing or royalty payments required for the embedded processor, high-speed transceivers, or other advanced system technology.

3. Although a microprocessor is used, would the application benefit from a tailored peripheral set?

Off-the-shelf Processor with Outdated Interfaces or Missing Peripherals vs. Customizable Peripherals and Interfaces in SoC FPGA

Rather than settle for an off-the-shelf processor that only approximately fits the application, maybe missing an Ethernet port, or interrupt lines, for example, a custom ARM microprocessor derivative can be created —instantly – and on the desktop. The design can be differentiated both in hardware and software, making it more difficult for competitors to copy.

Conclusion

This demonstrates how SoC FPGAs are applicable to many contemporary and next-generation electronic designs. This new breed of programmable devices exploits the flexibility of the FPGA architecture, to keep pace with changing standards and end-user demands, combined with the management functionality of a processor, to meet performance expectations, without the NRE, real estate or risk penalties.

Ready to Learn More?

Learn more about Altera's SoC FPGA product portfolio through the SoC FPGA Product Brochure. Available at http://www.altera.com/literature/br/br-soc-fpga.pdf.

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