Architecture Brief

SoC FPGA Main Memory Performance

Introduction

A cursory look at the memory specifications can conceal the whole story of how it will perform in an SoC FPGA-based system. It is important to check the measured memory performance, not just the bus specifications to ensure that maximum efficiency is realized, for performance, operation and power consumption benefits.

This Architecture Brief looks at memory performance considerations when selecting an SoC FPGA for a design project.

Key aspects of this Architecture Brief are highlighted in an online video: "System Performance: Performance is in the eye of the beholder"

Top Level Specs

When selecting an SoC FPGA, one would typically assume that the memory bus speed would dominate the realized system memory performance (see ***Table 1***).

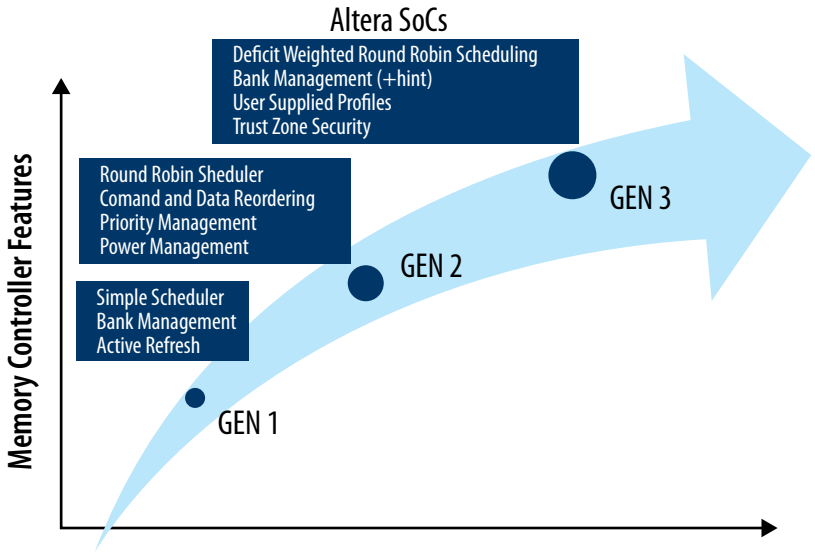
Table 1: External Memory Controller Support Comparison

Function/Feature	Altera SoC FPGA	Vendor B	Vendor C
Hardened External Memory Controller for Processor System	Yes	Yes	Yes
Maximum Supported Address Space	4G	1G	4G
Memory Types Supported	LPDDR2, DDR2, DDR3L, DDR3	LPDDR2, DDR2, DDR3L, DDR3	LPDDR, DDR2, DDR3
Data Width Configuration Modes	x8 x16 x16+ECC x32 x32+ECC	x16 x16+ECC x32	x8 x8+ECC x16 x16+ECC x32 x32+ECC
Integrated ECC Support	16 bit, 32 bit	16 bit	8 bit, 16 bit, 32 bit
External Memory Bus Maximum Frequency	400 MHz (Cyclone V SoC), 533 MHz (Arria V SoC)	533MHz	333 MHz

Memory Controller Intelligence

However, other factors - how intelligently the memory data transfers are prioritized, scheduled, and processed - can significantly impact overall memory performance. Altera SoC FPGAs utilize Altera's third generation memory controller technology which include advanced features in the areas of scheduling, bank management, command and data reordering, and more.

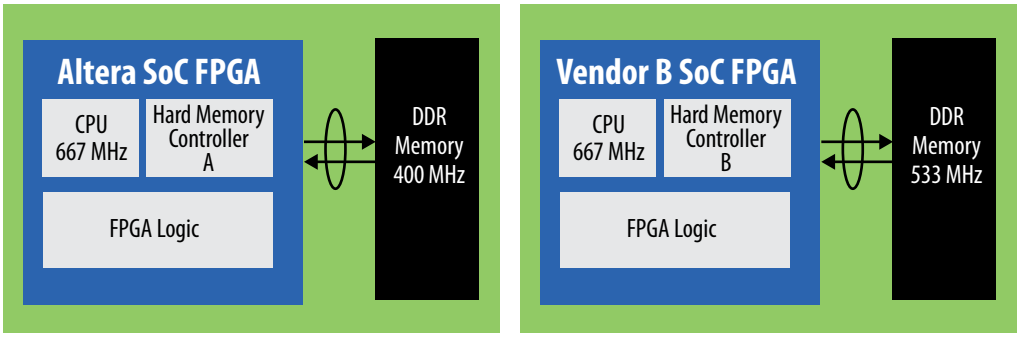
Figure 1: Altera Memory Controller Intelligence



Memory Performance Case Study: LMbench

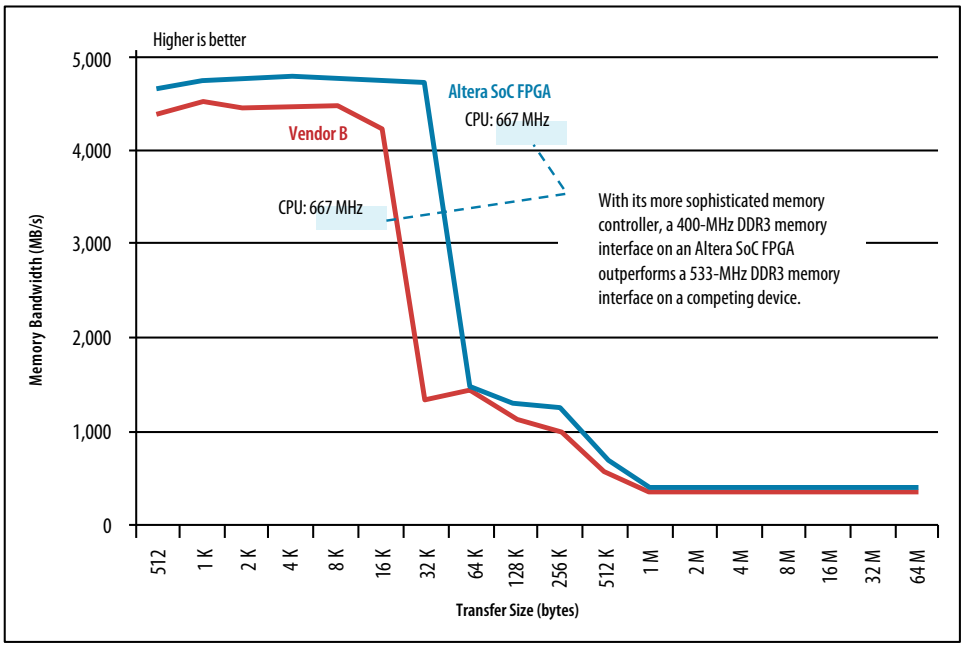
To illustrate the impact of the memory controller intelligence on system memory performance, consider two SoC FPGA devices with different memory bus speeds (shown in ***Figure 2***). The one on the left is the Altera Cyclone V SoC FPGA; the one on the right is an SoC FPGA from "Vendor B". Both have a dual-core ARM Cortex-A9 processor running at the same frequency of 667 MHz. However, one has an external memory operating at 400 MHz, while the other uses an external memory running at 533 MHz. Which one would you expect to have the better system memory performance? Initially, one would expect the system with 533 MHz memory to exhibit 33% higher performance. However, factors in the memory controller architecture produce some noticeably different results.

Figure 2: SoC FPGA Memory Performance Comparison



Turning to the system performance benchmark called LMbench, an industry-standard benchmark (www.bitmover.com/lmbench) well known for exercising the memory system performance, helps to quantify and compare the results. LMbench (ver. 3) consists of several different read/write test cases. The results for the partial read/write case are shown in ***Figure 3*** as the partial read/write case is most indicative of transfers in a typical embedded system.

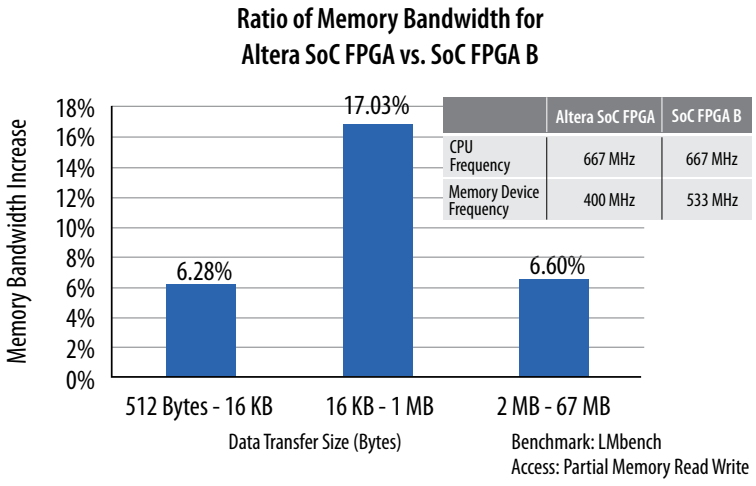
Figure 3: LMbench Partial Read/Write Memory Bandwidth Test Demonstrates Benefits of Advanced Controller



The vertical axis shows the memory bandwidth vs. the data transfer size along the horizontal axis. (Higher is better for the memory bandwidth.) The curve can be grouped into three stages as the data size moves from the L1 cache (32KB data + 32KB instruction) to the L2 cache (512KB shared) to external memory. Note that the Altera SoC FPGA significantly outperforms the Vendor B SoC FPGA on the L1 andL2 cache regions. As discussed earlier, one would expect that by the time the transfers reach the external memory (>512 KB on the curve) that the Vendor B solution would outperform the Altera SoC FPGA due to the 533 MHz external bus on SoC FPGA B vs. the 400 MHz memory bus of the Altera Cyclone V SoC FPGA. However, this is not the case as the Altera SoC FPGA exhibits comparable or better performance, even when accessing main memory at >1MB data transfer size. These results are due to the L1/L2 cache structure and external memory controller intelligence of the Altera SoC FPGA.

Grouping the data into small (512 byte to 16 KB), medium (16KB to 1MB) and large (>2MB) data transfer sizes as shown in ***Figure 4*** helps provide a numerical analysis for the three different regions of the curve.

Figure 4: LMbench Memory Bandwidth Difference Grouped by Data Transfer Size



Across the range of small, medium, and large memory accesses, the Altera SoC FPGA with a more effective cache structure and more advanced memory controller, extracts up to 17% more memory bandwidth despite a slower external memory bus operating frequency.

These results demonstrate that when comparing SoC FPGAs, it is important to check the measured memory system performance, not just the memory bus specifications. Memory controller algorithms extract maximum bandwidth by managing transaction priority, reordering command and data, and scheduling pending transactions using, for example, deficit weight round robin algorithms. Additional performance can be achieved by customizing the memory controller via software for the system's custom data profile, set priorities, assign ports or transaction channels, and even share the bandwidth between them.

Conclusion

The main memory selection is another example of where architecture matters. Memory controllers today can use sophisticated algorithms to maximize system memory efficiency. A superior memory controller can extract more bandwidth from system memory, enabling the memory to run at a lower frequency for the same throughput; thus saving system power and benefiting the whole system design.

Want to Learn More?

For a more in-depth explanation of the Altera SoC FPGA architecture and LMbench performance results, tune to the EE Journal Chalk Talk entitled: Architecture Matters: Three Architectural Insights for SoC FPGAs.

For more details on the Altera Cyclone V SoC FPGA memory controller architecture and settings, consult the SDRAM Controller Section of the Cyclone V Device Handbook, Vol. 3 Hard Processor System Technical Reference Manual.

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