Architecture Brief

Improved System Cost with SoC FPGAs

Introduction

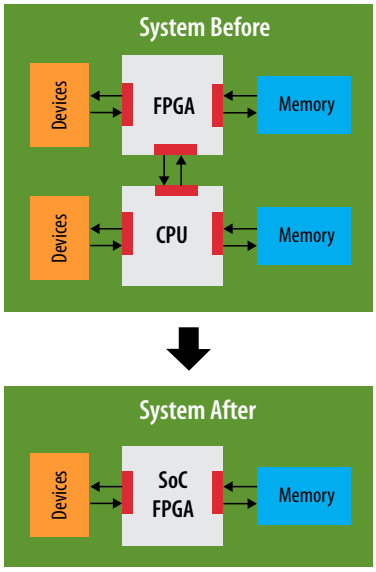
Altera has designed its SoC FPGAs with increasing customer system cost pressures in mind, both at the component and system levels. The customization and high level of integration offered by SoC FPGAs can combine to boost performance levels, and increase energy efficiency while reducing costs.

This Architecture Brief explains how an SoC FPGA can boost system performance while driving down costs.

Key aspects of this Architecture Brief are highlighted in an online video: "Cost Savings Across the Board".

A single SoC FPGA may cut costs by up to 50% below the individual components it replaces, and it is also likely to reduce system costs.

Figure 1: Integrating Processor and FPGA Reduces Component and System-Level Costs



When considering cost, it is important to look at three key areas:

- How many equivalent functions are already integrated in the SoC?
- Does the application require high-speed transceivers? If so, how many?
- What is the associated power supply cost?

Integrated Functionality

Depending on the application, a single SoC FPGA might contain the system equivalent of the processor, all of its peripherals, multiple digital signal processors (DSPs), memory controllers, high-speed transceivers, clock management, and custom logic to differentiate your design in the market.

Before selecting an SoC FPGA, consider the following:

- Does it offer both a single-core and a dual-core processor version?
- In addition to the ARM processor cores, what peripherals are integrated?
- Is the processor memory controller designed for sharing between the CPU and FPGA logic?
- Does the device include hardened memory controllers that can be dedicated to your FPGA design or do you need to allocate additional FPGA logic for the controllers?
- Does it have integrated interfaces, like PCIe?
- Are there ways to save cost with configuration options?
- Are there common package footprints to allow for platform cost optimization?

High-Speed Transceivers

High-speed transceivers can significantly impact the cost of a design. All Altera SoC FPGAs include high-speed transceivers; available as an option in the low-end, entry-level devices as well as in the largest full-featured devices. High-speed transceivers are critical for applications like PCIe - otherwise, an external interface component is needed which adds to the system bill of materials (BOM). As some embedded designs may not require high-speed transceivers, Altera offers SoC FPGA variants that do not include high-speed transceivers to reduce the SoC FPGA component cost.

Power Supply Cost

Some SoC FPGAs require stringent power-on and power-off sequencing controls that mandate more sophisticated - and thereby more expensive - power supplies. In particular, power-off sequencing becomes difficult due to all of the potential power-loss conditions that might occur. Ideally, it is best to avoid power-on or power-off conditions, especially if those requirements affect the long-term reliability of the device. Altera SoC FPGAs do not have any power-on or - off sequencing requirements. (For more details see the Architecture Brief Impact of Power-off Sequencing on SoC FPGA-based Systems.)

System Cost Factor Comparison

Table 1 provides a comparison of system cost factors for Altera SoC FPGAs with those of another SoC FPGA vendor.

Table 1: SoC FPGA System Cost Factor Comparison

Function/Feature	Altera SoC FPGA	Vendor B
Single- and Dual-Core Processor Option	Yes	No (Dual-core only)
Hardened Memory Controller in Both Processor System and FPGA Fabric	Yes (1 in processor system, up to 3 in FPGA)	No (1 in processor system, none in FPGA)
All Devices with High-Speed Transceivers (necessary for integrated PCIe)	Yes	No (2 of 6 without high speed transceivers)
Integrated Analog Mixed Signal	No	Yes (2 x 12-bit, 1 MSPS ADCs)
Spectrum of Logic Densities	25, 40, 85, 110, 350, 460 KLE	28, 74, 85, 125, 350, 444 KLC
Package Migration	Yes	Limited
Power-Off Sequencing Requirement	No	Yes (additional external circuitry required)

Application Example - Industrial Drive on Chip

Power and its associated costs are particularly significant in industrial systems, where nearly 66% of the energy consumed in a factory floor is from motor-driven equipment. Controlling motors with multiple axis control, reduces the power consumption, increases performance and efficiency, while reducing the bill of materials cost per motor.

The Altera drive-on-a-chip motor control reference design is an integrated drive system on a single Cyclone V SoC, Cyclone V FPGA, or Cyclone IV FPGA. The design implements single- and multi axis field-oriented control (FOC) supporting concurrent control of up to four permanent magnet synchronous motors.

The reference design showcases a software-centric design flow for motor control on FPGAs. It targets either the dual ARM Cortex-A9 hard processor system or the Nios II soft-core processor as the drive system host integrated with DSP co-processors and key motor control interface IP in the FPGA. This demonstrates the cost-effective scalability of integrated drive-on-a-chip designs on Altera's Cyclone families and is an excellent starting point for a designer's own drive system design.

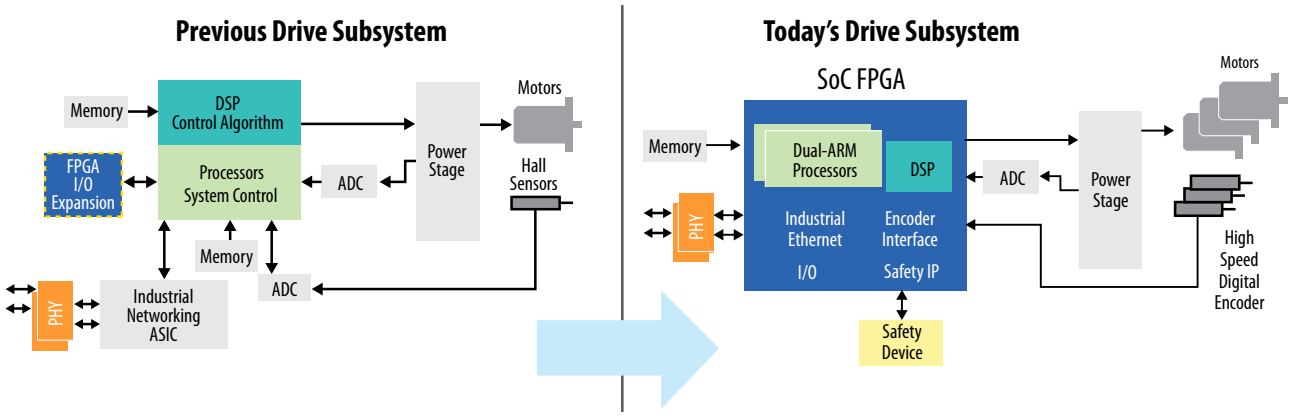
The example in ***Figure 2***, below, runs the software system on the dual ARM Cortex-A9 hard processor system (HPS), performing high-level control and configuration (in addition to closing motor position and speed loops).

Software-only and FPGA-accelerated FOC implementations integrate position and speed loops in software with an ultra-low latency, high-performance current control loop in the FPGA as a DSP coprocessor.

The optimized, software-configurable FOC IP subsystem, is customizable in DSP Builder with support for both fixed- and floating-point precision implementations.

The drive also integrates key motor control functions, such as space vector pulse-width modulation (PWM), Sigma-Delta ADC interface and filter logic, and position feedback encoder interfaces in the FPGA, all under control of software, for further cost savings.

Figure 2: Energy Efficiency for Today's Drives



Parameter	Performance
Processing & Power	480 MIPS @ 3.2 Watts
Algorithm	~65 µs control loop; Fixed Point
Axis	Single
Performance/ Efficiency	Medium
Flexibility	Software
BOM cost per motor	$$$

Parameter	Performance
Processing & Power	1500 MIPS @ 2 Watts
Algorithm	~5 µs control loop; Fixed Point
Axis	Multiple
Performance/ Efficiency	High
Flexibility	Hardware
BOM cost per motor	$

Implementing today's drive subsystem shows that the level of integration reduces power from 3.2W to just 2W. The ability to support multiple motors increases efficiency and reduces operating costs with a reduced number of components required for the automation project.

From a system cost perspective, implementing two drives using the previous solution would require duplicating the same setup per motor. Using the SoC FPGA-based solution of today, support for 2 or 3 motors can be integrated into a single chip. For the case of two motors, the BOM cost savings is >50%, for the case of 3 motors, the BOM cost savings is >66% versus the previous generation solution. All this is done while actually increasing the functionality of each drive.

Conclusion

SoC FPGAs from Altera offer integration and cost saving features to benefit a wide variety of applications. A single SoC FPGA can be extended to integrate processor, peripherals, digital signal processing, on-chip memory and more, including high-speed transceivers and PCIe interfaces. As shown by the Industrial Drive on a Chip reference design, the SoC FPGA implementation can dramatically increase system performance and functionality while decreasing system power and cost.

Want More Information?

The Industrial Drive on a Chip Motor Control reference design can be found on Altera's website here:

Drive-on-a-Chip Multi-Axis Motor Control

More information on the package migration capabilities of Altera SoC FPGAs can be found here:

SoC FPGA Package Migration and Common Platform Flexibility Architecture Brief