

Agilex™ F-Series Transceiver-SoC Development Kit

Project Drawing Numbers:	
Raw PCB	100-0321502-B
Gerber Files	110-0321502-B
PCB Design Files	120-0321502-B
Assembly Drawing	130-0321502-B
Fab Drawing	140-0321502-B
Schematic Drawing	150-0321502-B
PCB Film	160-0321502-B
Bill of Materials	170-0321502-B
Schematic Design Files	180-0321502-B
Functional Specification	210-0321502-B
PCB Layout Guidelines	220-0321502-B
Assembly Rework	320-0321502-B

[illegible]

PAGE		DESCRIPTION	PAGE	DESCRIPTION	PAGE	DESCRIPTION	
01	Title, Notes, Catalog	22	FPGA Bank - 3A	43	PWRUB2MAX 1	64	PWR - FPGA VCCPT 1.8V
02	Block Diagram	23	FPGA Bank - HPS	44	PWRUB2MAX 2	65	PWR - FPGA VCCIO 1.2V
03	Power Tree & Sequence	24	FPGA Bank - 9A E-tile	45	PWRUB2MAX 3	66	PWR - FPGA VCCL_HPS 0.9V
04	FPGA Power Group	25	FPGA Bank - 10A P-tile	46	SYSMAX 1	67	PWR - FPGA VCCL_SDM 0.8V
05	Reset Topology	26	FPGA Power 1	47	SYSMAX 2	68	PWR - FPGA VCCH_GXE 1.1V
06	Clock Tree, Bank Usage	27	FPGA Power 2	48	SYSMAX 3	69	PWR - FPGA VCCIO 1.8V
07	I2C Chain	28	FPGA GND 1	49	Temp Sense/Fan	70	PWR - FPGA VCCIO 1.5V
08	JTAG Chain	29	FPGA GND 2	50	Power Monitors	71	PWR - FPGA VCCCLK_GXE 2.5V
09	PWRUB2MAX Functional Diagram	30	FPGA NC/DNU	51	Clock 1	72	PWR - FPGA VCCFUSEWR 2.4V
10	SYSMAX Functional Diagram	31	260 Pin SO-DIMM	52	Clock 2	73	PWR - SODIMM VTT 0.6V
11	SODIMM Pin Table	32	DDR4 Component 1	53	CLOCK CLEANER	74	PWR - SODIMMVDD 1.2V-1.35V
12	E-tile Pin Swap Map	33	DDR4 Component 2	54	I2C And PMBUS	75	PWR - DDR4 VTT 0.6V
13	SDM IO Pin Map	34	DDR4 Comp Termination	55	PWR - POWER INPUT	76	PWR - 1.8V
14	FPGA Bank - SDM	35	FLASH Daughter Cards	56	PWR - 3.3V_PRE	77	PWR - 2.5V
15	FPGA Bank - 2D	36	QSFPDD1x1	57	PWR - 12V	78	PWR - 1.2V
16	FPGA Bank - 2C	37	zQSFP	58	PWR - BIAS	79	FPGA Decoupling Caps 1
17	FPGA Bank - 2B	38	MXP Connectors	59	PWR - 3.3V	80	FPGA Decoupling Caps 2
18	FPGA Bank - 2A	39	PCIe RC Connector	60	PWR - FPGA VCC VID 1	81	FPGA Decoupling Caps 3
19	FPGA Bank - 3D	40	10/100/1000 Ethernet PHY	61	PWR - FPGA VCC VID 2	82	Revision History
20	FPGA Bank - 3C	41	FPGA Test IOs	62	PWR - FPGA VCC VID 3		
21	FPGA Bank - 3B	42	On Board USB BLASTER II	63	PWR - FPGA VCCH 0.9V		



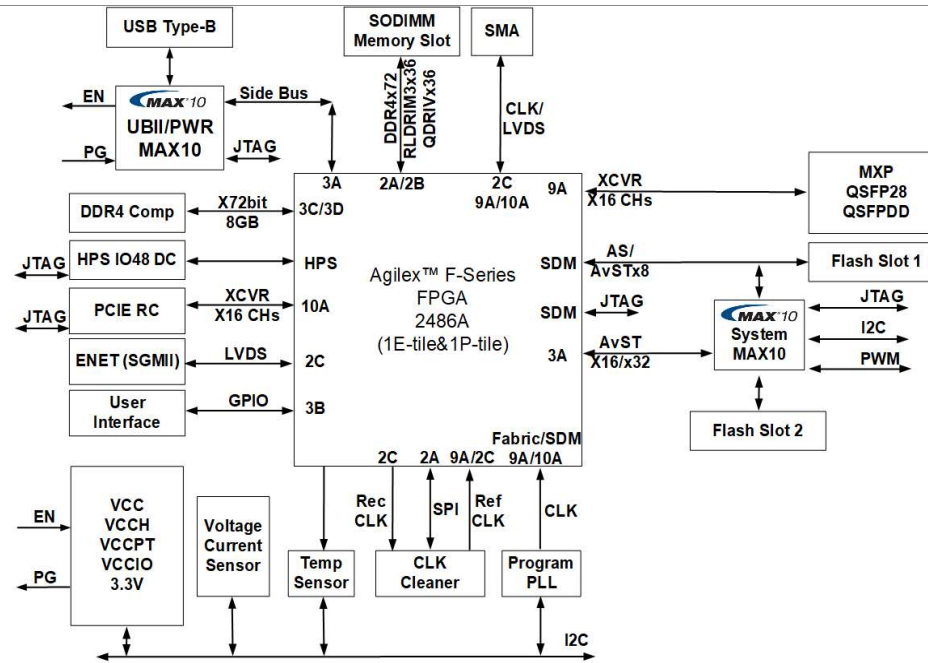
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Title

Agilex™ F-Series Transceiver-SoC Development Kit

Size B	Document Number 150-0321502-B	Rev B
Date:	Friday, November 25, 2022	Sheet 1 of 82

Block Diagram



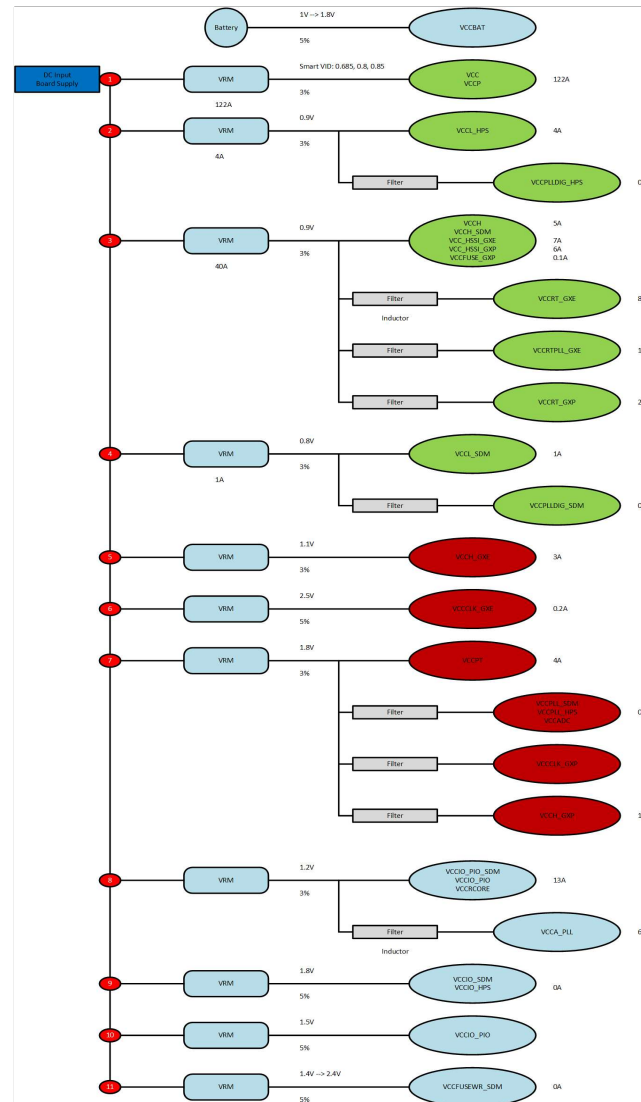
E-TILE: 9A 16CHs/9REFCLK
P-TILE: 10A 16CHs/5REFCLK
IO96: 2A/2B/2C/2D/3A/3B/3C/3D
TSD: CORE/E-TILE/P-TILE
HPS: 48 IOs
SDM: 17 IOs

Reuse the Boot Flash DC and HPS IO48 DC in S10 Gen
Flash slot 1 for FPGA AS configuration and HPS initial boot based on NAND/QSPI/SD/eMMC DC
Flash slot 2 for System MAX10 AvSTx8/16/32 configuration based on NAND/QSPI/SD/eMMC DCs
Combine flash slot 1 and 2 for System MAX10 AvSTx16/x32 configuration based on CFI NOR DC
HPS IO48 DC for HPS following boot and function expansion
UBII/PWR MAX10 manages JTAG, Side Bus, power sequence and over temp. protection, hidden for customer
System MAX handles AvST configuration, I2C manage (clock/power/monitor ICs) and fan control, open for customer
Design SODIMM memory DCs for RDRAM3 and QDRIV based on IO96A rules



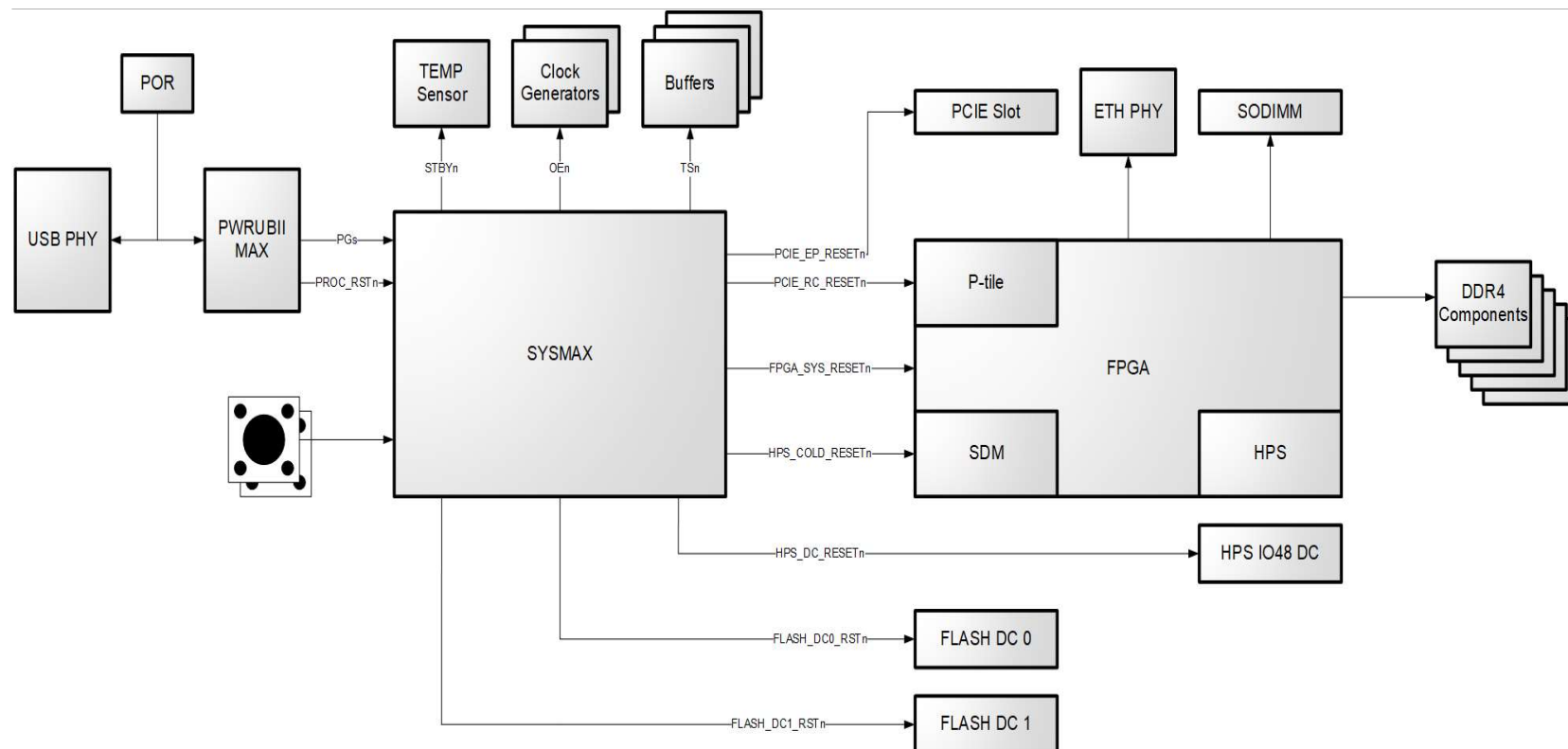
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Title Agilex™ F-Series Transceiver-SoC Development Kit			
Size B	Document Number 150-0321502-B	Rev B	
Date: Friday, November 25, 2022	Sheet 1	2	of 82

FPGA Power Group



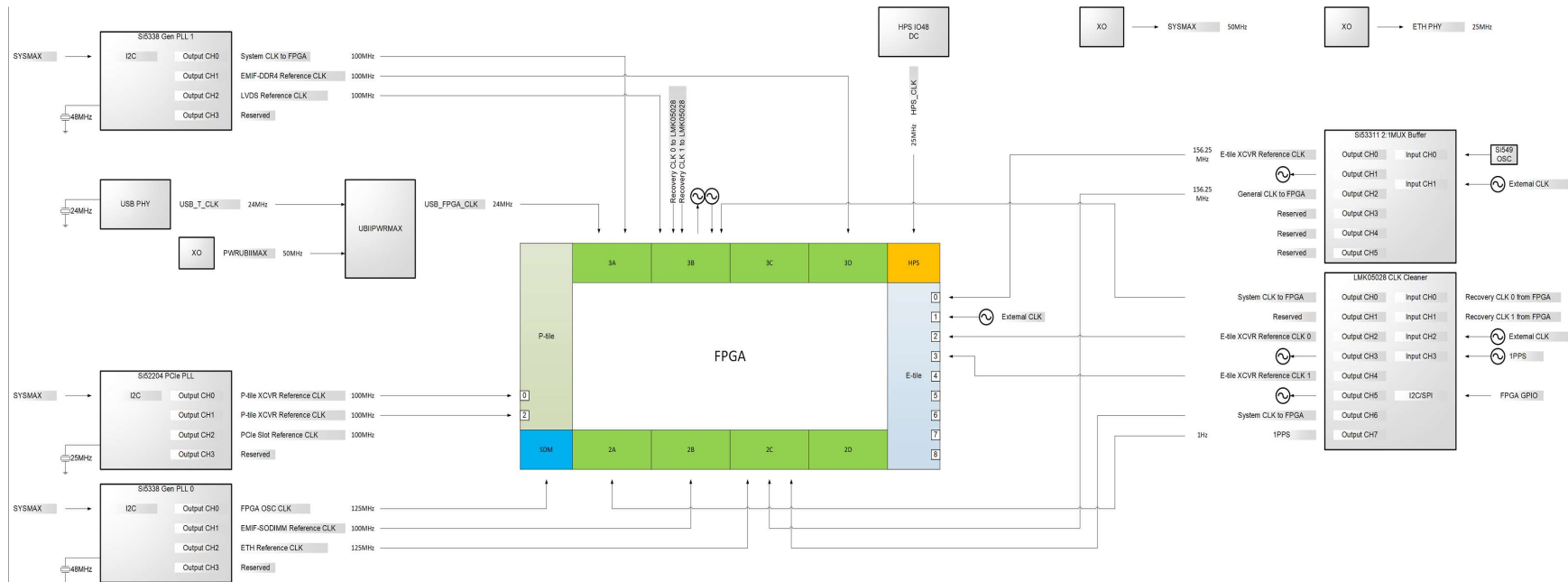
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Title			
Agilex™ F-Series Transceiver-SoC Development Kit			
Size	Document Number	Rev	
B	150-0321502-B	B	
Date:	Friday, November 25, 2022	Sheet	4 of 82

Reset Topology



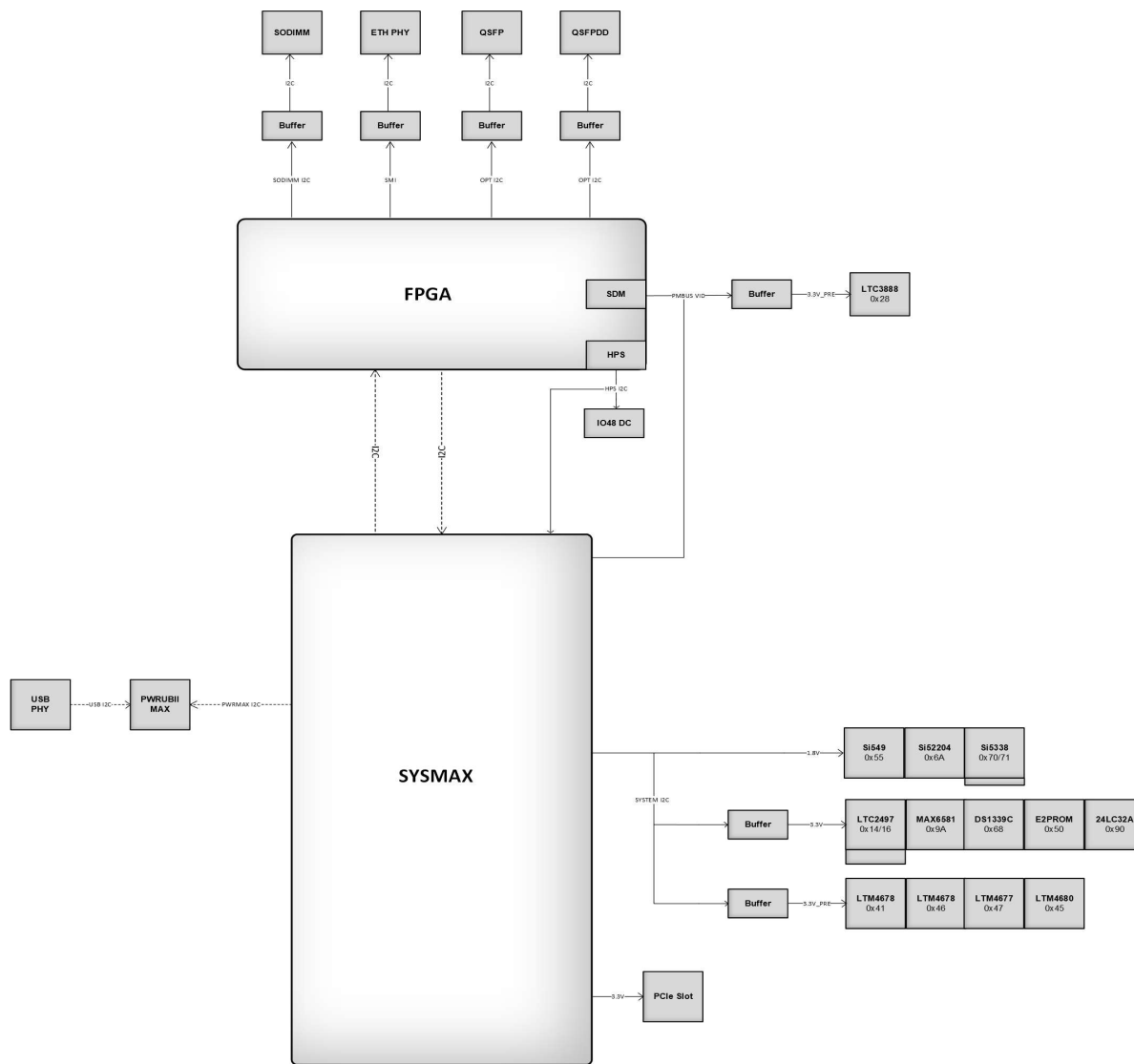
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Size	Document Number	Rev	
B	150-0321502-B	B	
Date:	Friday, November 25, 2022	Sheet	5 of 82

Clock Tree



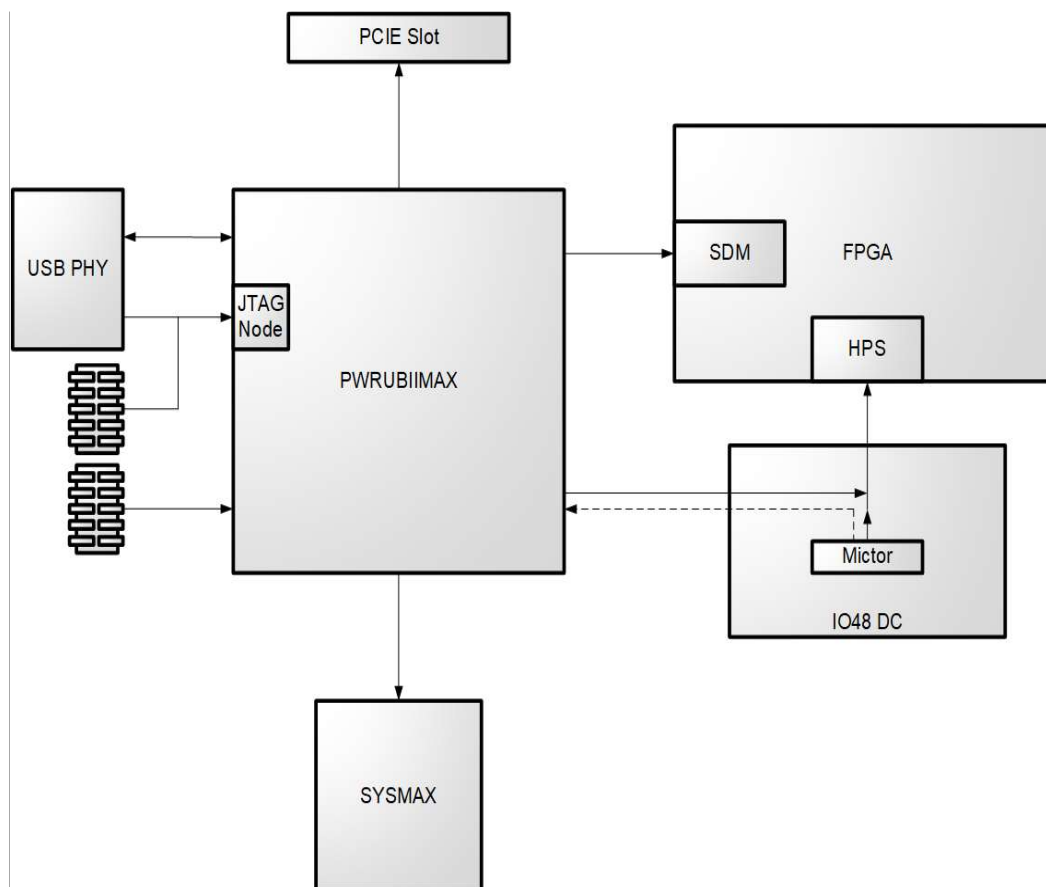
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Title			
Aglex™ F-Series Transceiver-SoC Development Kit			
Size	Document Number	Rev	
B	150-0321502-B	B	
Date:	Friday, November 25, 2022	Sheet	6 of 82

I2C Bus Topology



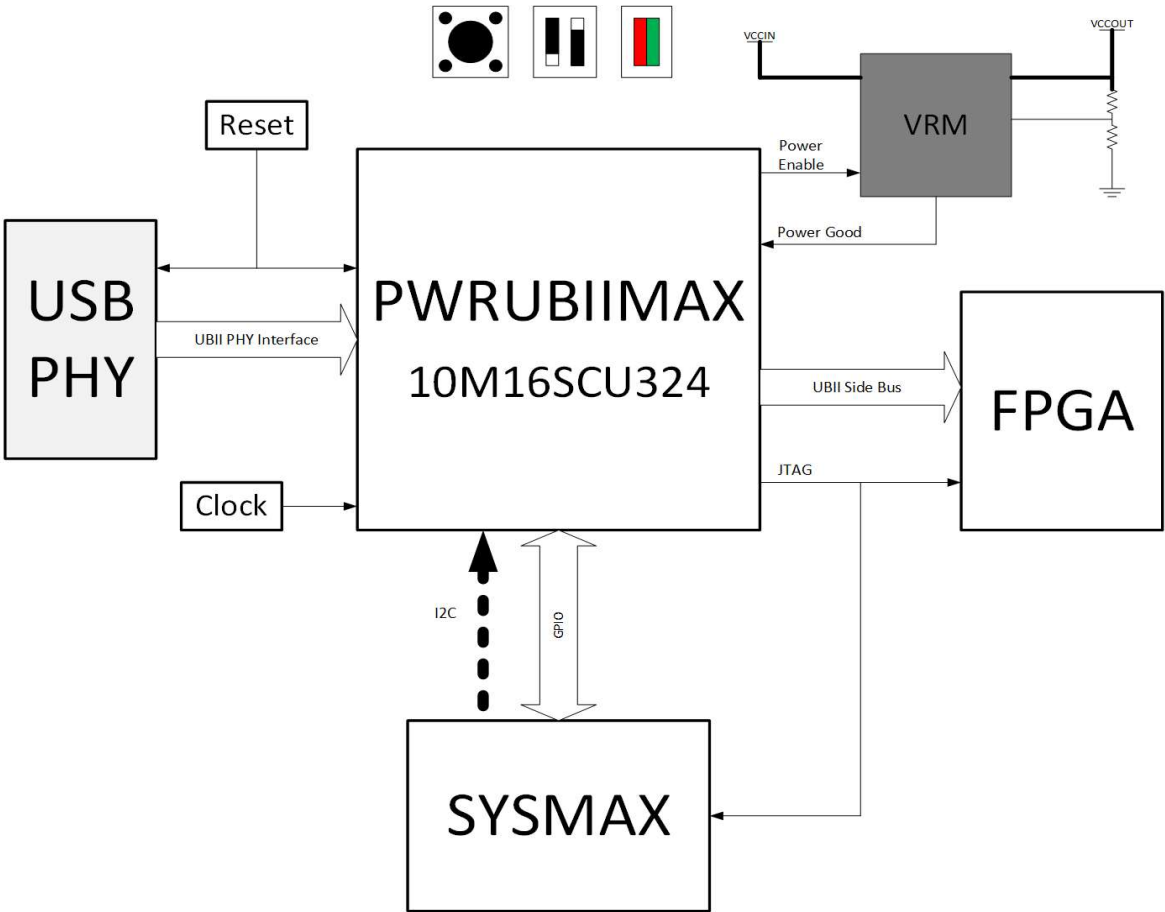
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Size	Document Number	Rev	
B	150-0321502-B	B	
Date:	Friday, November 25, 2022	Sheet	7 of 82

JTAG Chain Topology

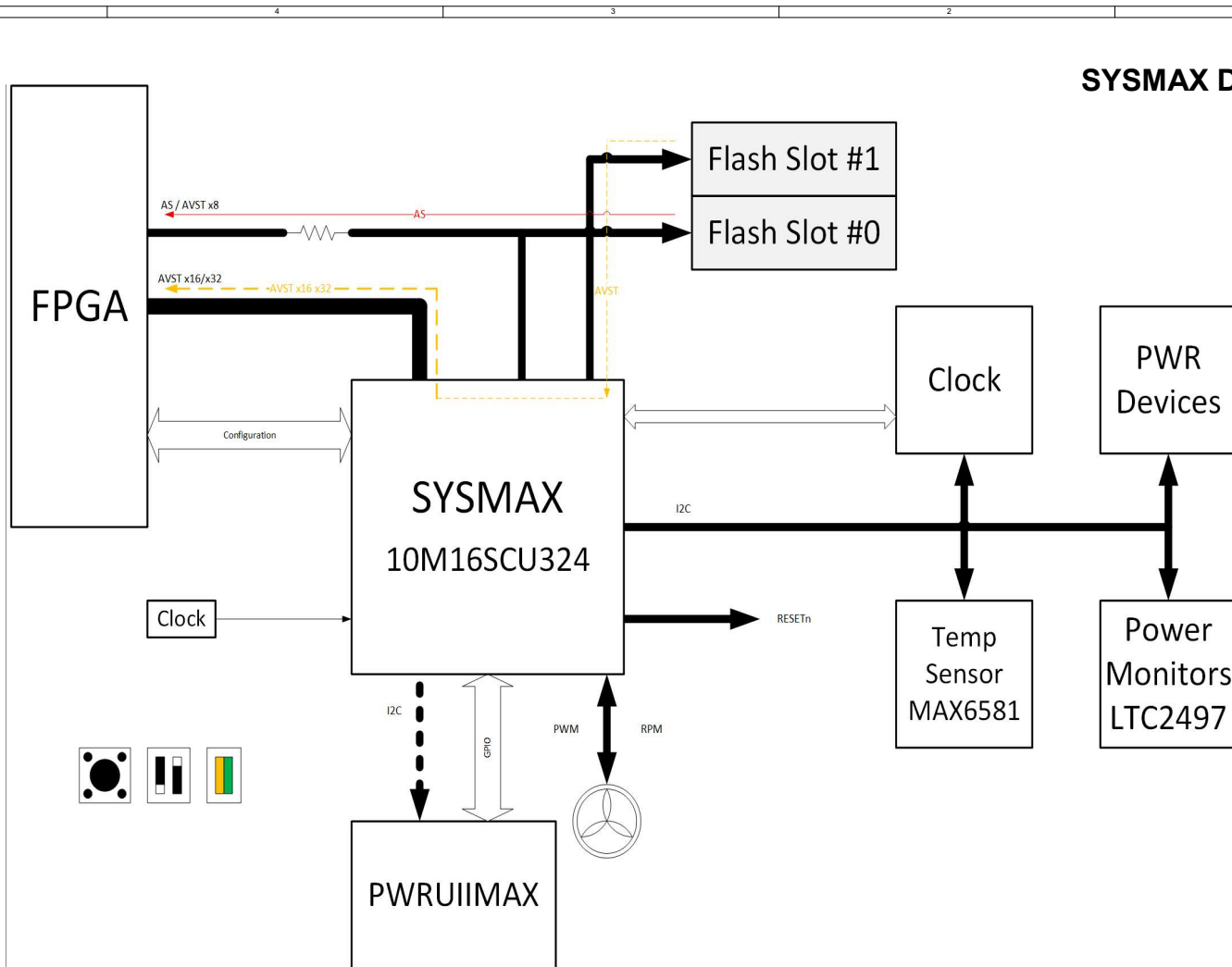


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Title			
Agilex™ F-Series Transceiver-SoC Development Kit			
Size	Document Number	Rev	
B	150-0321502-B	B	
Date:	Friday, November 25, 2022	Sheet	8 of 82

PWRUBIIMAX Diagram



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Title			
Agilex™ F-Series Transceiver-SoC Development Kit			
Size	Document Number	Rev	
B	150-0321502-B	B	
Date:	Friday, November 25, 2022	Sheet	9 of 82



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Title Agilex™ F-Series Transceiver-SoC Development Kit			
Size B	Document Number 150-0321502-B	Rev B	
Date:	Friday, November 25, 2022	Sheet	10 of 82

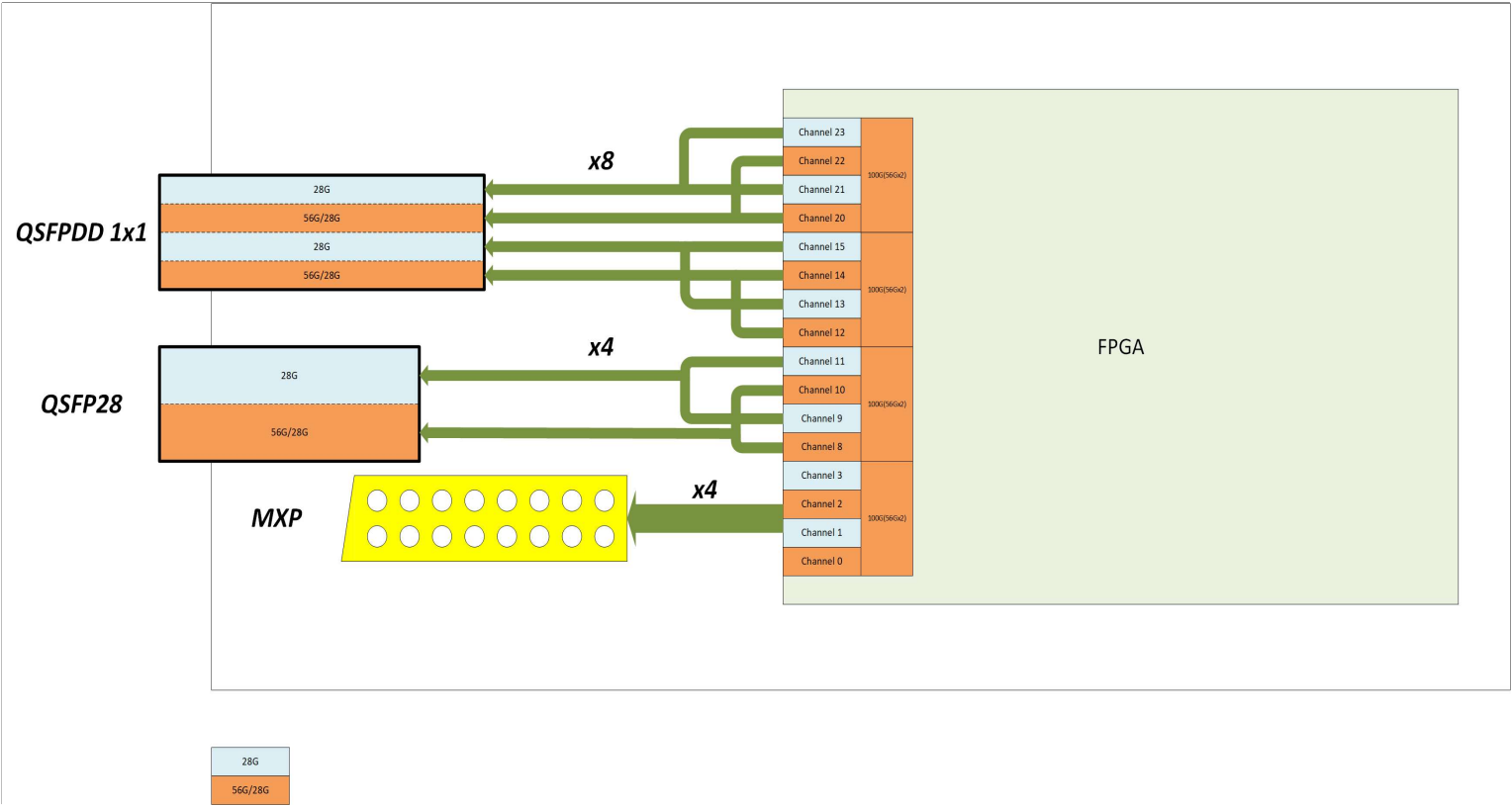
SODIMM Pin Table

DDR4 x72 (DQ3 x8 Groups) FM	BLDRAM3 x36 FM	QDRV x36 FM	HL0 Pin Name	260pin SODIMM Pin Number	SODIMM function	Lane	DDR4 x72 (DQ3 x8 Groups) FM6	BLDRAM3 x36 FM	QDRV x36 FM	HL0 Pin Name	260pin SODIMM Pin Number	SODIMM function	Lane	DDR4 x72 (DQ3 x8 Groups) FM6	BLDRAM3 x36 FM	QDRV x36 FM	HL0 Pin Name	260pin SODIMM Pin Number	SODIMM function	Lane
DQ24	DQ9	DQ40	MEM_DQ[24]	70	DQ24	00_00	BG1	BA3	RWAn	MEM_ADDR_CMD[00]	113	BG1	04_00	DQ56	DQ0	DQ80	MEM_DQB[24]	237	DQ56	08_00
DQ25	DQ10	DQ41	MEM_DQ[25]	71	DQ25	00_01	RESETn	RESETn	RW8n	MEM_ADDR_CMD[01]	108	RESETn	04_01	DQ57	DQ1	DQ81	MEM_DQB[25]	236	DQ57	08_01
DQ26	DQ11	DQ42	MEM_DQ[26]	83	DQ26	00_02	Csn0	Csn0	LDAn	MEM_ADDR_CMD[02]	149	Csn0	04_02	DQ58	DQ2	DQ82	MEM_DQB[26]	249	DQ58	08_02
DQ27	DQ12	DQ43	MEM_DQ[27]	84	DQ27	00_03	ACTn	Csn1	LD8n	MEM_ADDR_CMD[03]	114	ACTn	04_03	DQ59	DQ3	DQ83	MEM_DQB[27]	250	DQ59	08_03
DQ5_P3	QK1	QKA_P0	MEM_DQSA_P[3]	76	DQ53	00_04	ODT0	A18	CK_P	MEM_ADDR_CMD[04]	155	ODT0	04_04	DQ5_P7	QK0	QKB_N0	MEM_DQSA_P[3]	242	DQ57	08_04
DQ5_N3	QK1#	QKA_N0	MEM_DQSA_N[3]	74	DQ53#	00_05	ODT1/NC	A19	CK_N	MEM_ADDR_CMD[05]	161	ODT1	04_05	DQ5_N7	QK0#	QKB_P0	MEM_DQSA_N[3]	240	DQ57#	08_05
DM_n3	DM1	DQ48	MEM_DMA[3]	75	DM3n/DB3n	00_06	CKE0	A20	AINV_0	MEM_ADDR_CMD[06]	109	CKE0	04_06	DM_n7	DM0	DQ88	MEM_DMB[3]	241	DM7n/DB7n	08_06
	DQ17	D1NV40	MEM_DQ[33]	138	CK1	00_07	CKE1/NC	WEn	CFGn	MEM_ADDR_CMD[07]	110	CKE1	04_07		DQ8	D1NV80	MEM_DQB[33]	162	CK3n/CS2n	08_07
DQ28	DQ13	DQ44	MEM_DQ[28]	66	DQ28	00_08	CK_P0	CK_P	A0	MEM_CLK_P	137	CK0	04_08	DQ60	DQ4	DQ84	MEM_DQB[28]	232	DQ60	08_08
DQ29	DQ14	DQ45	MEM_DQ[29]	67	DQ29	00_09	CK_N0	CK_N	A1	MEM_CLK_N	139	CK0#	04_09	DQ61	DQ5	DQ85	MEM_DQB[29]	233	DQ61	08_09
DQ30	DQ15	DQ46	MEM_DQ[30]	79	DQ30	00_10	Csn1/NC	Csn2	A2	MEM_ADDR_CMD[08]	157	Csn1	04_10	DQ62	DQ6	DQ86	MEM_DQB[30]	245	DQ62	08_10
DQ31	DQ16	DQ47	MEM_DQ[31]	80	DQ31	00_11	PARITY	REFn	A3	MEM_ADDR_CMD[09]	143	PARITY	04_11	DQ63	DQ7	DQ87	MEM_DQB[31]	246	DQ63	08_11
DQ16	DQ9	MEM_DQ[16]	50	DQ16	01_00	A0	A0	A4	A4	MEM_ADDR_CMD[10]	144	A0	05_00	DQ48		DQ89	MEM_DQB[16]	216	DQ48	09_00
DQ17	DQ10	MEM_DQ[17]	49	DQ17	01_01	A1	A1	A5	A5	MEM_ADDR_CMD[11]	133	A1	05_01	DQ49		DQ90	MEM_DQB[17]	215	DQ49	09_01
DQ18	DQ11	MEM_DQ[18]	62	DQ18	01_02	A2	A2	A6	A6	MEM_ADDR_CMD[12]	132	A2	05_02	DQ50		DQ91	MEM_DQB[18]	228	DQ50	09_02
DQ19	DQ12	MEM_DQ[19]	63	DQ19	01_03	A3	A3	A7	A7	MEM_ADDR_CMD[13]	131	A3	05_03	DQ51		DQ92	MEM_DQB[19]	229	DQ51	09_03
DQ5_P2	DK1	DKA_P0	MEM_DQSA_P[2]	55	DQ52	01_04	A4	A4		MEM_ADDR_CMD[14]	128	A4	05_04	DQ5_P6	DK0	DKB_P0	MEM_DQSA_P[2]	221	DQ56	09_04
DQ5_N2	DK1#	DKA_N0	MEM_DQSA_N[2]	53	DQ52#	01_05	A5	A5		MEM_ADDR_CMD[15]	126	A5	05_05	DQ5_N6	DK0#	DKB_N0	MEM_DQSA_N[2]	219	DQ56#	09_05
DM_n2		DQ417	MEM_DMA[2]	54	DM2n/DB2n	01_06	A6	A6	A8	MEM_ADDR_CMD[16]	127	A6	05_06	DM_n6		DQ817	MEM_DMB[2]	220	DM2n/DB2n	09_06
					01_07	A7	A7	RESETn		MEM_ADDR_CMD[17]	122	A7	05_07							09_07
DQ20	DQ13	MEM_DQ[20]	46	DQ20	01_08	A8	A8	A9	A9	MEM_ADDR_CMD[18]	125	A8	05_08	DQ52		DQ913	MEM_DQB[20]	211	DQ52	09_08
DQ21	DQ14	MEM_DQ[21]	45	DQ21	01_09	A9	A9	A10	A10	MEM_ADDR_CMD[19]	121	A9	05_09	DQ53		DQ914	MEM_DQB[21]	212	DQ53	09_09
DQ22	DQ15	MEM_DQ[22]	58	DQ22	01_10	A10/AP	A10	A11	A11	MEM_ADDR_CMD[20]	146	A10/AP	05_10	DQ54		DQ915	MEM_DQB[22]	224	DQ54	09_10
DQ23	DQ16	MEM_DQ[23]	59	DQ23	01_11	A11	A11	A12	A12	MEM_ADDR_CMD[21]	120	A11	05_11	DQ55		DQ916	MEM_DQB[23]	225	DQ55	09_11
DQ8	DQ27	DQ418	MEM_DQ[08]	28	DQ8	02_00	A12	A12	A13	MEM_ADDR_CMD[22]	119	A12	06_03	DQ40	DQ18	DQ818	MEM_DQB[08]	195	DQ40	10_00
DQ9	DQ28	DQ419	MEM_DQ[09]	29	DQ9	02_01	A13	A13		MEM_ADDR_CMD[23]	158	A13	06_04	DQ41	DQ19	DQ819	MEM_DQB[09]	194	DQ41	10_01
DQ10	DQ29	DQ420	MEM_DQ[10]	41	DQ10	02_02	A14/WE_n	A14		MEM_ADDR_CMD[24]	151	WEn/A14	06_05	DQ42	DQ20	DQ820	MEM_DQB[10]	207	DQ42	10_02
DQ11	DQ30	DQ421	MEM_DQ[11]	42	DQ11	02_03	A15/CAS_n	A15	A14	MEM_ADDR_CMD[25]	156	CASn/A15	06_06	DQ43	DQ21	DQ821	MEM_DQB[11]	208	DQ43	10_03
DQ5_P1	QK3	QKA_P1	MEM_DQSA_P[1]	34	DQ51	02_04	A16/RAS_n	A16	Pe#	MEM_ADDR_CMD[26]	152	RASn/A16	06_07	DQ5_P5	QK2	QKB_N1	MEM_DQSA_P[1]	200	DQ55	10_04
DQ5_N1	QK3#	QKA_N1	MEM_DQSA_N[1]	32	DQ51#	02_05	ALERTn	A17	A15	MEM_ADDR_CMD[27]	116	Alertn	06_08	DQ5_N5	QK2#	QKB_P1	MEM_DQSA_N[1]	198	DQ55#	10_05
DM_n1		DQ426	MEM_DMA[1]	33	DM1n/DB1n	02_06	BA0	BA0	A16	MEM_ADDR_CMD[28]	150	BA0	06_09	DM_n5		DQ826	MEM_DMB[1]	199	DM5n/DB5n	10_06
	DQ35	D1NV41	MEM_DQ[32]	140	CK1#	02_07	BA1	BA1	A17	MEM_ADDR_CMD[29]	145	BA1	06_10		DQ26	D1NV81	MEM_DQB[32]	165	CK1/CS3n	10_07
DQ12	DQ31	DQ422	MEM_DQ[12]	24	DQ12	02_08	BG0	BA2	A18	MEM_ADDR_CMD[30]	115	BG0	06_11	DQ44	DQ22	DQ822	MEM_DQB[12]	191	DQ44	10_08
DQ13	DQ32	DQ423	MEM_DQ[13]	25	DQ13	02_09	DQ65	Csn3	A19	MEM_DQ_ADDR_CMD[0]	104	CB7	07_00	DQ45	DQ23	DQ823	MEM_DQB[13]	190	DQ45	10_09
DQ14	DQ33	DQ424	MEM_DQ[14]	38	DQ14	02_10	DQ71	A20		MEM_DQ_ADDR_CMD[1]	105	CB3	07_01	DQ46	DQ24	DQ824	MEM_DQB[14]	203	DQ46	10_10
DQ15	DQ34	DQ425	MEM_DQ[15]	37	DQ15	02_11	DQ70	A21		MEM_DQ_ADDR_CMD[2]	101	CB2	07_02	DQ47	DQ25	DQ825	MEM_DQB[15]	204	DQ47	10_11
DQ0		MEM_DQ[00]	8	DQ0	03_00	DQ69		A22		MEM_DQ_ADDR_CMD[3]	100	CB6	07_03	DQ32		DQ827	MEM_DQB[00]	174	DQ32	11_00
DQ1	DQ428	MEM_DQ[01]	7	DQ1	03_01	DQ5_P8				MEM_DQ5_ADDR_CMD_P	97	DQ58	07_04	DQ33		DQ828	MEM_DQB[01]	173	DQ33	11_01
DQ2	DQ429	MEM_DQ[02]	20	DQ2	03_02	DQ5_N8				MEM_DQ5_ADDR_CMD_N	95	DQ58#	07_05	DQ34		DQ829	MEM_DQB[02]	187	DQ34	11_02
DQ3	DQ430	MEM_DQ[03]	21	DQ3	03_03	DM_n8		AP		MEM_DQ_ADDR_CMD[4]	96	DM8n/DB8n	07_06	DQ35		DQ830	MEM_DQB[03]	186	DQ35	11_03
DQ5_P0	DKA_P1	MEM_DQSA_P[0]	13	DQ50	03_04								07_07	DQ5_P4		DKB_P1	MEM_DQSA_P[0]	179	DQ54	11_04
DQ5_N0	DKA_N1	MEM_DQSA_N[0]	11	DQ50#	03_05	DQ66		A23		MEM_DQ_ADDR_CMD[5]	88	CB4	07_08	DQ5_N4		DKB_N1	MEM_DQSA_N[0]	177	DQ54#	11_05
DM_n0		DQ435	MEM_DMA[0]	12	DM0n/DB0n	03_06	DQ67		A24	MEM_DQ_ADDR_CMD[6]	91	CB1	07_09	DM_n4		DQ835	MEM_DMB[0]	178	DM4n/DB4n	11_06
					03_07	DQ64			LBK0n	MEM_DQ_ADDR_CMD[7]	92	CB0	07_10							11_07
DQ4	DQ431	MEM_DQ[04]	4	DQ4	03_08	DQ68			LBK1n	MEM_DQ_ADDR_CMD[8]	87	CB5	07_11	DQ36		DQ831	MEM_DQB[04]	170	DQ36	11_08
DQ5	DQ432	MEM_DQ[05]	3	DQ5	03_09									DQ37		DQ832	MEM_DQB[05]	169	DQ37	11_09
DQ6	DQ433	MEM_DQ[06]	16	DQ6	03_10									DQ38		DQ833	MEM_DQB[06]	183	DQ38	11_10
DQ7	DQ434	MEM_DQ[07]	17	DQ7	03_11					CONFIG/Card TYPE	134	EVENTn		DQ39		DQ834	MEM_DQB[07]	182	DQ39	11_11



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Agilex™ F-Series Transceiver-Soc Development Kit			
Size B	Document Number 150-0321502-B	Rev B	
Date:	Friday, November 25, 2022	Sheet 11 of 82	

E-tile Pin Assignment



FPGA Configuration Settings

CONFIGURATION MODE		MSEL[2:0]
Passive	AVSTx32	000
	AVSTx16	101
	AVSTx8	110
	JTAG	111
	CvP	001
Active	Reserved	100
	AS - Fast	001
	AS - Normal	011

SDM Pins	MSEL Functions	Configuration Source Function			
		AVSTx8	AS	AVSTx16	AVSTx32
SDM_IO0		PWR_SCL	PWR_SCL	PWR_SCL	PWR_SCL
SDM_IO1		DATA2	DATA1		
SDM_IO2		DATA0	CLK		
SDM_IO3		DATA3	DATA2		
SDM_IO4		DATA1	DATA0		
SDM_IO5	MSEL0	HPS_CRSTn	nCS0		
SDM_IO6		DATA4	DATA3		
SDM_IO7	MSEL1		nCS02		
SDM_IO8		READY	nCS03		
SDM_IO9	MSEL2		nCS01		
SDM_IO10		DATA7			
SDM_IO11		VALID	HPS_CRSTn	HPS_CRSTn	HPS_CRSTn
SDM_IO12		PWR_SDA	PWR_SDA	PWR_SDA	PWR_SDA
SDM_IO13		DATA5			
SDM_IO14		CLK			
SDM_IO15		DATA6	nRST		
SDM_IO16		CFG_DONE	CFG_DONE	CFG_DONE	CFG_DONE



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Title Agilex™ F-Series Transceiver-SoC Development Kit			
Size B	Document Number 150-0321502-B	Rev B	
Date:	Friday, November 25, 2022	Sheet	13 of 82

FPGA Bank - SDM

FPGA_JTAG_TDO	CR62
FPGA_JTAG_TMS	CT61
FPGA_JTAG_TCK	CU62
FPGA_JTAG_TDI	CV61
FPGA_NCONFIG	CH57
FPGA_NSTATUS	CH59
FPGA_OSC_CLK_1	CC60

SDM_I00	CF59
SDM_I01	CU60
SDM_I02	CT59
SDM_I03	CK59
SDM_I04	CN60
SDM_I05	CR60
SDM_I06	CM59
SDM_I07	CL59
SDM_I08	CL60
SDM_I09	CV59
SDM_I010	CC58
SDM_I011	CE60
SDM_I012	CC56
SDM_I013	CB59
SDM_I014	CB60
SDM_I015	CA58
SDM_I016	CA60

U1A

TDO	SDM_I01, AVSTX8_DATA2, AS_DATA1, SDMMC_CFG_DATA1, NAND_RE_N
TMS	SDM_I02, AVSTX8_DATA0, AS_CLK, SDMMC_CFG_DATA0, NAND_ADQ0
TCK	SDM_I03, AVSTX8_DATA3, AS_DATA2, SDMMC_CFG_DATA2, NAND_ADQ2
TDI	SDM_I04, AVSTX8_DATA1, AS_DATA0, SDMMC_CFG_CMD, NAND_ADQ1
NCONFIG	SDM_I05, INIT_DONE, AS_NCS00, SDMMC_CFG_CCLK, NAND_WE_N, MSEL0, CONF_DONE
NSTATUS	SDM_I06, AVSTX8_DATA4, AS_DATA3, SDMMC_CFG_DATA3, NAND_ADQ3
OSC_CLK_1	SDM_I07, AS_NCS02, NAND_ALE, MSEL1
	SDM_I08, AVST_READY, AS_NCS03, SDMMC_CFG_DATA4, NAND_RB
	SDM_I09, AS_NCS01, NAND_CLE, MSEL2
	SDM_I010, AVSTX8_DATA7, SDMMC_CFG_DATA7, NAND_ADQ5
	SDM_I011, AVSTX8_VALID, PWRMGT_SDA, NAND_ADQ6
	SDM_I012, PWRMGT_PWM0, PWRMGT_SDA, NAND_WP_N
	SDM_I013, AVSTX8_DATA5, SDMMC_CFG_DATA5, NAND_CE_N
	SDM_I014, AVSTX8_CLK, PWRMGT_SCL, NAND_ADQ7
	SDM_I015, AVSTX8_DATA6, SDMMC_CFG_DATA6, NAND_ADQ4
	SDM_I016, INIT_DONE, CONF_DONE, PWRMGT_SDA

R12 2.00K CA54		RREF_SDM
FPGA_VSIGP_0	CG62	VSIGP_0
FPGA_VSIGN_0	CE62	VSIGN_0
FPGA_VSIGP_1	CN62	VSIGP_1
FPGA_VSIGN_1	CL62	VSIGN_1
	BY59	GND
FPGA_TEMP0p_49	CC52	TEMPDIODE0AP
FPGA_TEMP0n_49	CA52	TEMPDIODE0AN

FPGA_VREFP_ADC	CC62
FPGA_VREFN_ADC	CA62
	VREFP_ADC
	VREFN_ADC

FPGA_DNU_CORE0	CF61
FPGA_DNU_CORE1	CH61
FPGA_DNU_CORE2	BY65
FPGA_DNU_SDM0	CB53
FPGA_DNU_SDM1	BY53
	DNUI1
	DNUI2
	DNUI3
	DNUI4
	DNUI5

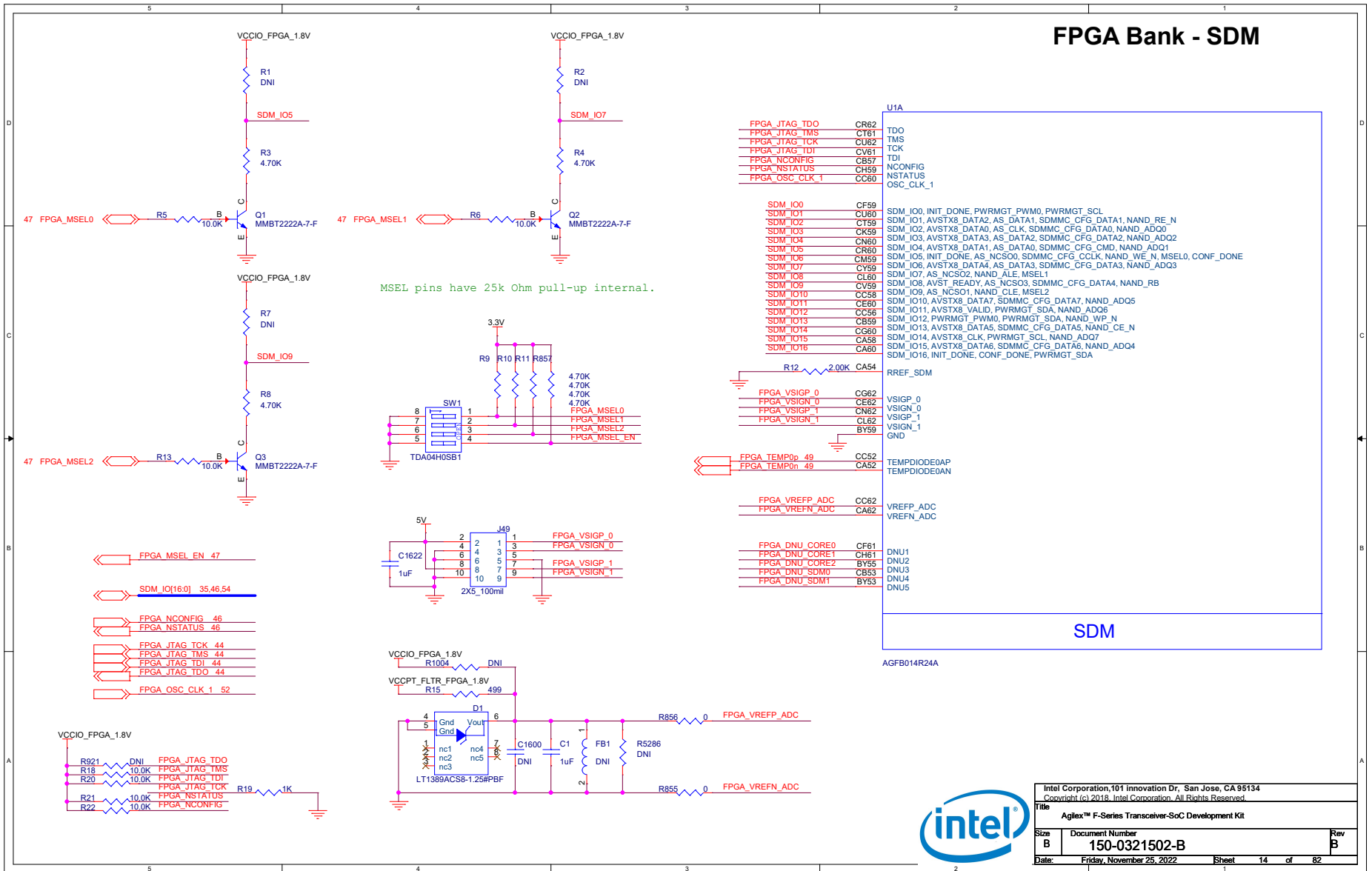
SDM

AGFB014R24A



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Title Agilex™ F-Series Transceiver-SoC Development Kit			
Size B	Document Number 150-0321502-B	Rev B	
Date: Friday, November 25, 2022	Sheet 1	of 14	82

MSEL pins have 25k Ohm pull-up internal.



FPGA Bank - 2D

U1B

CF3 IO, LVDS2D_25N, DQ4
CE4 IO, LVDS2D_25P, DQ4
CG4 IO, LVDS2D_26N, DQ4
CF5 IO, LVDS2D_26P, DQ4
CH5 IO, LVDS2D_27N, DQ4
CE6 IO, LVDS2D_27P, DQ4
CG6 IO, LVDS2D_28N, DQS4
CF7 IO, LVDS2D_28P, DQS4
CH7 IO, LVDS2D_29N, DQ4
CE8 IO, LVDS2D_29P, DQ4
CG8 IO, LVDS2D_30N, DQ4
CK3 IO, LVDS2D_30P, DQ4
CM3 IO, LVDS2D_31N, DQ5
CL4 IO, LVDS2D_31P, DQ5
CN4 IO, LVDS2D_32N, DQ5
CK5 IO, LVDS2D_32P, DQ5
CM5 IO, LVDS2D_33N, DQ5
CL6 IO, LVDS2D_33P, DQ5
CN6 IO, PLL_2D_B_CLKOUT1N, LVDS2D_34N, DQS5
CK7 IO, PLL_2D_B_CLKOUT1P, PLL_2D_B_CLKOUT1, PLL_2D_B_FB1, LVDS2D_34P, DQS5
CM7 IO, LVDS2D_35N, DQ6
CL8 IO, RZQ_B_2D, LVDS2D_35P, DQ5
CN8 IO, CLK_B_2D_1N, LVDS2D_36N, DQ5
CE10 IO, CLK_B_2D_1P, LVDS2D_36P, DQ5
CG10 IO, CLK_B_2D_0N, LVDS2D_37N, DQ6
CH11 IO, CLK_B_2D_0P, LVDS2D_37P, DQ6
CF11 IO, LVDS2D_38N, DQ6
CE12 IO, LVDS2D_38P, DQ6
CG12 IO, PLL_2D_B_CLKOUT0N, LVDS2D_39N, DQ6
CF13 IO, PLL_2D_B_CLKOUT0P, PLL_2D_B_CLKOUT0, PLL_2D_B_FB0, LVDS2D_39P, DQ6
CH13 IO, LVDS2D_40N, DQS6
CE14 IO, LVDS2D_40P, DQS6
CG14 IO, LVDS2D_41N, DQ6
CF15 IO, LVDS2D_41P, DQ6
CH15 IO, LVDS2D_42N, DQ6
CL10 IO, LVDS2D_42P, DQ6
CN10 IO, LVDS2D_43N, DQ7
CK11 IO, LVDS2D_43P, DQ7
CM11 IO, LVDS2D_44N, DQ7
CL12 IO, LVDS2D_44P, DQ7
CN12 IO, LVDS2D_45N, DQ7
CK13 IO, LVDS2D_45P, DQ7
CM13 IO, LVDS2D_46N, DQS7
CL14 IO, LVDS2D_46P, DQS7
CN14 IO, LVDS2D_47N, DQ7
CK15 IO, LVDS2D_47P, DQ7
CM15 IO, LVDS2D_48N, DQ7
IO, LVDS2D_48P, DQ7

BOT TOP

Bank 2D

AGFB014R24A

IO, LVDS2D_1N, DQ0
IO, LVDS2D_1P, DQ0
IO, LVDS2D_2N, DQ0
IO, LVDS2D_2P, DQ0
IO, LVDS2D_3N, DQ0
IO, LVDS2D_3P, DQ0
IO, LVDS2D_4N, DQS0
IO, LVDS2D_4P, DQS0
IO, LVDS2D_5N, DQ0
IO, LVDS2D_5P, DQ0
IO, LVDS2D_6N, DQ0
IO, LVDS2D_6P, DQ0
IO, LVDS2D_7N, DQ1
IO, LVDS2D_7P, DQ1
IO, LVDS2D_8N, DQ1
IO, LVDS2D_8P, DQ1
IO, LVDS2D_9N, DQ1
IO, LVDS2D_9P, DQ1
IO, PLL_2D_T_CLKOUT1N, LVDS2D_10N, DQS1
IO, PLL_2D_T_CLKOUT1P, PLL_2D_T_CLKOUT1, PLL_2D_T_FB1, LVDS2D_10P, DQS1
IO, LVDS2D_11N, DQ1
IO, RZQ_T_2D, LVDS2D_11P, DQ1
IO, CLK_T_2D_1N, LVDS2D_12N, DQ1
IO, CLK_T_2D_1P, LVDS2D_12P, DQ1
IO, CLK_T_2D_0N, LVDS2D_13N, DQ2
IO, CLK_T_2D_0P, LVDS2D_13P, DQ2
IO, LVDS2D_14N, DQ2
IO, LVDS2D_14P, DQ2
IO, PLL_2D_T_CLKOUT0N, LVDS2D_15N, DQ2
IO, PLL_2D_T_CLKOUT0P, PLL_2D_T_CLKOUT0, PLL_2D_T_FB0, LVDS2D_15P, DQ2
IO, LVDS2D_16N, DQS2
IO, LVDS2D_16P, DQS2
IO, LVDS2D_17N, DQ2
IO, LVDS2D_17P, DQ2
IO, LVDS2D_18N, DQ2
IO, LVDS2D_18P, DQ2
IO, LVDS2D_19N, DQ3
IO, LVDS2D_19P, DQ3
IO, LVDS2D_20N, DQ3
IO, LVDS2D_20P, DQ3
IO, LVDS2D_21N, DQ3
IO, LVDS2D_21P, DQ3
IO, LVDS2D_22N, DQS3
IO, LVDS2D_22P, DQS3
IO, LVDS2D_23N, DQ3
IO, LVDS2D_23P, DQ3
IO, LVDS2D_24N, DQ3
IO, LVDS2D_24P, DQ3

CT3 QSFDD_MODPRSn
CV3 QSFDD_RESEtN
CR4 QSFDD_MODESELn
CU4 QSFDD_INtN
CT5 QSFDD_INITMODE
CV5
CR6 QSFDD_MODESELn
CU6 QSFDD_RESEtN
CT7 QSFDD_MODPRSn
CV7 QSFDD_INtN
CR8 QSFDD_INITMODE
CU8
CT1 QSFDD_I2C_SCL
CV3
DA4
CY5 QSFDD_I2C_SDA
DB5
DA6
DC6
CY7 QSFDD_I2C_SCL
DB7
DA8
DC8
CR10 QSFDD_I2C_SDA
CU10
CT11
CV11
CR12
CU12
CT13
CV13
CR14
CU14
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DB13
DA14
DC14
CY15
DB15

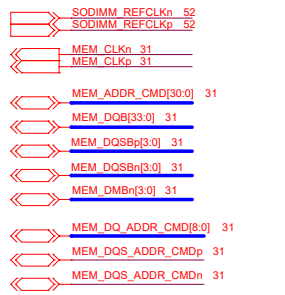
QSFDD_INITMODE 36
QSFDD_MODESELn 36
QSFDD_RESEtN 36
QSFDD_MODPRSn 36
QSFDD_INtN 36
QSFDD_I2C_SCL 36
QSFDD_I2C_SDA 36

QSFDD_INITMODE 37
QSFDD_MODESELn 37
QSFDD_RESEtN 37
QSFDD_MODPRSn 37
QSFDD_INtN 37
QSFDD_I2C_SCL 37
QSFDD_I2C_SDA 37



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Title Aglex™ F-Series Transceiver-SoC Development Kit			
Size	Document Number	Rev	
B	150-0321502-B	B	
Date:	Friday, November 25, 2022	Sheet	15 of 82

FPGA Bank - 2B



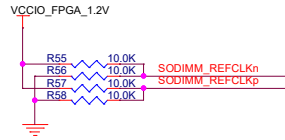
MEM_DQ_ADDR_CMD8	CF43	IO, LVDS2B_25N, DQ20
MEM_DQ_ADDR_CMD7	CH43	IO, LVDS2B_25P, DQ20
MEM_DQ_ADDR_CMD6	CE42	IO, LVDS2B_26N, DQ20
MEM_DQ_ADDR_CMD5	CG42	IO, LVDS2B_26P, DQ20
MEM_DQ_ADDR_CMD4	CF41	IO, LVDS2B_27N, DQ20
MEM_DQ_ADDR_CMD3	CH41	IO, LVDS2B_27P, DQ20
MEM_DQ_ADDR_CMD2	CE40	IO, LVDS2B_28N, DQS20
MEM_DQ_ADDR_CMD1	CG40	IO, LVDS2B_28P, DQS20
MEM_DQ_ADDR_CMD0	CF39	IO, LVDS2B_29N, DQ20
MEM_DQ_ADDR_CMD0	CH39	IO, LVDS2B_29P, DQ20
MEM_DQ_ADDR_CMD0	CE38	IO, LVDS2B_30N, DQ20
MEM_DQ_ADDR_CMD0	CG38	IO, LVDS2B_30P, DQ20
MEM_ADDR_CMD29	CK43	IO, LVDS2B_31N, DQ21
MEM_ADDR_CMD28	CM43	IO, LVDS2B_31P, DQ21
MEM_ADDR_CMD27	CL42	IO, LVDS2B_32N, DQ21
MEM_ADDR_CMD26	CK41	IO, LVDS2B_32P, DQ21
MEM_ADDR_CMD25	CM41	IO, LVDS2B_33N, DQ21
MEM_ADDR_CMD24	CL40	IO, LVDS2B_33P, DQ21
MEM_ADDR_CMD23	CK40	IO, PLL_2B_B_CLKOUT1P, LVDS2B_34N, DQS21
MEM_ADDR_CMD22	CM39	IO, PLL_2B_B_CLKOUT1P, PLL_2B_B_CLKOUT1, PLL_2B_B_FB1, LVDS2B_34P, DQS21
SODIMM_RZQ	CM39	IO, LVDS2B_35N, DQ21
SODIMM_REFCLKn	CL38	IO, RZQ_B_2B, LVDS2B_35P, DQ21
SODIMM_REFCLKp	CK38	IO, CLK_B_2B_1N, LVDS2B_36N, DQ21
MEM_ADDR_CMD21	CE36	IO, CLK_B_2B_1P, LVDS2B_36P, DQ21
MEM_ADDR_CMD20	CG36	IO, CLK_B_2B_0N, LVDS2B_37N, DQ22
MEM_ADDR_CMD19	CF35	IO, CLK_B_2B_0P, LVDS2B_37P, DQ22
MEM_ADDR_CMD18	CH35	IO, LVDS2B_38N, DQ22
MEM_ADDR_CMD17	CE34	IO, LVDS2B_38P, DQ22
MEM_ADDR_CMD16	CG34	IO, PLL_2B_B_CLKOUT0N, LVDS2B_39N, DQ22
MEM_ADDR_CMD15	CF33	IO, PLL_2B_B_CLKOUT0P, PLL_2B_B_CLKOUT0, PLL_2B_B_FB0, LVDS2B_39P, DQ22
MEM_ADDR_CMD14	CH33	IO, LVDS2B_40N, DQS22
MEM_ADDR_CMD13	CE32	IO, LVDS2B_40P, DQS22
MEM_ADDR_CMD12	CG32	IO, LVDS2B_41N, DQ22
MEM_ADDR_CMD11	CF31	IO, LVDS2B_41P, DQ22
MEM_ADDR_CMD10	CH31	IO, LVDS2B_42N, DQ22
MEM_ADDR_CMD9	CE30	IO, LVDS2B_42P, DQ22
MEM_ADDR_CMD8	CG30	IO, LVDS2B_43N, DQ23
MEM_CLKn	CK35	IO, LVDS2B_43P, DQ23
MEM_CLKp	CM35	IO, LVDS2B_44N, DQ23
MEM_ADDR_CMD7	CL34	IO, LVDS2B_44P, DQ23
MEM_ADDR_CMD6	CK34	IO, LVDS2B_45N, DQ23
MEM_ADDR_CMD5	CM33	IO, LVDS2B_45P, DQ23
MEM_ADDR_CMD4	CK33	IO, LVDS2B_46N, DQS23
MEM_ADDR_CMD3	CL32	IO, LVDS2B_46P, DQS23
MEM_ADDR_CMD2	CG32	IO, LVDS2B_47N, DQ23
MEM_ADDR_CMD1	CF31	IO, LVDS2B_47P, DQ23
MEM_ADDR_CMD0	CH31	IO, LVDS2B_48N, DQ23
MEM_ADDR_CMD0	CM31	IO, LVDS2B_48P, DQ23

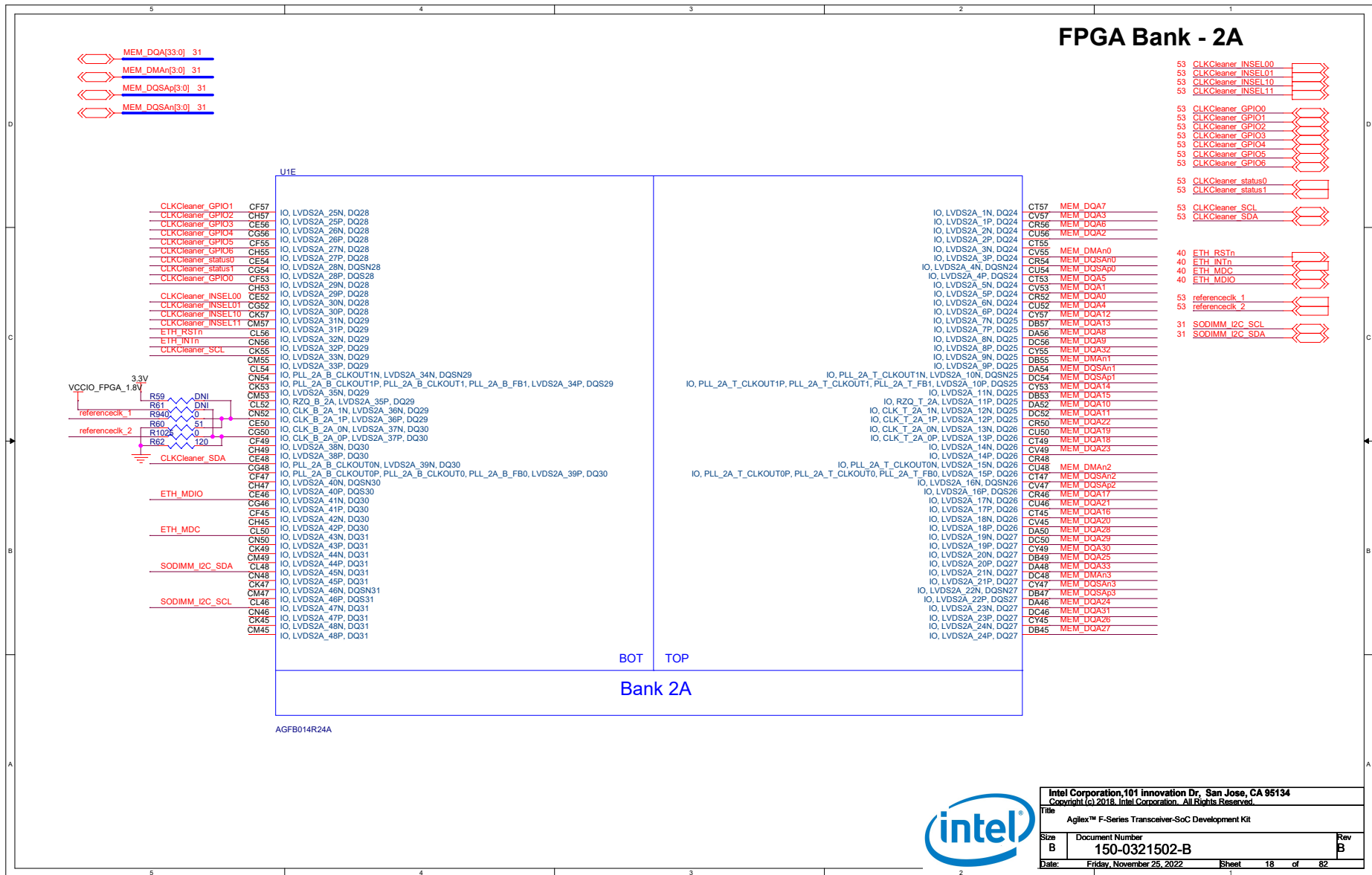
IO, LVDS2B_1N, DQ16	CT43	MEM_DQB5
IO, LVDS2B_1P, DQ16	CV43	MEM_DQB1
IO, LVDS2B_2N, DQ16	CR42	MEM_DQB4
IO, LVDS2B_2P, DQ16	CU42	MEM_DQB0
IO, LVDS2B_3N, DQ16	CT41	
IO, LVDS2B_3P, DQ16	CV41	MEM_DMbn0
IO, LVDS2B_4N, DQS16	CR40	MEM_DQSBn0
IO, LVDS2B_4P, DQS16	CU40	MEM_DQSBp0
IO, LVDS2B_5N, DQ16	CT39	MEM_DQB2
IO, LVDS2B_5P, DQ16	CV39	MEM_DQB5
IO, LVDS2B_6N, DQ16	CR38	MEM_DQB3
IO, LVDS2B_6P, DQ16	CU38	MEM_DQB7
IO, LVDS2B_7N, DQ17	CT37	MEM_DQB13
IO, LVDS2B_7P, DQ17	CV37	MEM_DQB12
IO, LVDS2B_8N, DQ17	CR36	MEM_DQB8
IO, LVDS2B_8P, DQ17	CU36	MEM_DQB9
IO, LVDS2B_9N, DQ17	CT35	MEM_DQB32
IO, LVDS2B_9P, DQ17	CV35	MEM_DQB1
IO, LVDS2B_10N, DQS17	CR34	MEM_DQSBn1
IO, LVDS2B_10P, DQS17	CU34	MEM_DQSBp1
IO, RZQ_T_2B, LVDS2B_11P, DQ17	CT33	MEM_DQB14
IO, CLK_T_2B_1N, LVDS2B_12N, DQ17	CV33	MEM_DQB15
IO, CLK_T_2B_1P, LVDS2B_12P, DQ17	CR32	MEM_DQB11
IO, CLK_T_2B_0N, LVDS2B_13N, DQ18	CU32	MEM_DQB20
IO, CLK_T_2B_0P, LVDS2B_13P, DQ18	CT31	MEM_DQB19
IO, LVDS2B_14N, DQ18	CV31	MEM_DQB21
IO, LVDS2B_14P, DQ18	CR30	MEM_DQB16
IO, PLL_2B_T_CLKOUTN, LVDS2B_15N, DQ18	CU30	
IO, PLL_2B_T_CLKOUTP, PLL_2B_T_CLKOUT0, PLL_2B_T_FB0, LVDS2B_15P, DQ18	CT29	MEM_DMbn2
IO, LVDS2B_16N, DQS18	CV29	MEM_DQSBn2
IO, LVDS2B_16P, DQS18	CR28	MEM_DQSBp2
IO, LVDS2B_17N, DQ18	CU28	MEM_DQB17
IO, LVDS2B_17P, DQ18	CT27	MEM_DQB23
IO, LVDS2B_18N, DQ18	CV27	MEM_DQB18
IO, LVDS2B_18P, DQ18	CR26	MEM_DQB22
IO, LVDS2B_19N, DQ19	CU26	MEM_DQB25
IO, LVDS2B_19P, DQ19	CT25	MEM_DQB26
IO, LVDS2B_20N, DQ19	CV25	MEM_DQB24
IO, LVDS2B_20P, DQ19	CR24	MEM_DQB29
IO, LVDS2B_21N, DQ19	CU24	MEM_DQB33
IO, LVDS2B_21P, DQ19	CT23	MEM_DQB30
IO, LVDS2B_22N, DQS19	CV23	MEM_DQBn3
IO, LVDS2B_22P, DQS19	CR22	MEM_DQSBn3
IO, LVDS2B_23N, DQ19	CU22	MEM_DQB28
IO, LVDS2B_23P, DQ19	CT21	MEM_DQB30
IO, LVDS2B_24N, DQ19	CV21	MEM_DQB27
IO, LVDS2B_24P, DQ19	CR20	MEM_DQB31

BOT TOP

Bank 2B

AGFB014R24A





FPGA Bank - 3D

DDR4_COMP_CLKn 32,33,34
DDR4_COMP_CLKp 32,33,34
DDR4_COMP_BA[1:0] 32,33,34
DDR4_COMP_AL[6:0] 32,33,34
DDR4_COMP_CSn 32,33,34
DDR4_COMP_ODT 32,33,34
DDR4_COMP_ACTn 32,33,34
DDR4_COMP_PAR 32,33,34
DDR4_COMP_CKE 32,33,34
DDR4_COMP_BG0 32,33,34
DDR4_COMP_BG1 32,33,34
DDR4_COMP_RESETn 32,33,34
DDR4_COMP_ALERTn 32,33,34
DDR4_COMP_DQ[7:0] 20,32,33,34
DDR4_COMP_DBIn[8:0] 20,32,33,34
DDR4_COMP_DQS[8:0] 20,32,33,34
DDR4_COMP_DQSn[8:0] 20,32,33,34
DDR4_COMP_REFCLKn S2
DDR4_COMP_REFCLKp S2

DDR4_COMP_DQ67 V5
DDR4_COMP_DQ65 T5
DDR4_COMP_DQ71 W6
DDR4_COMP_DQ89 U6
DDR4_COMP_DQ85 V7
DDR4_COMP_DQSn8 W8
DDR4_COMP_DQSp8 U8
DDR4_COMP_DQ88 V9
DDR4_COMP_DQ86 T9
DDR4_COMP_DQ70 W10
DDR4_COMP_DQ84 U10
DDR4_COMP_BG0 P5
DDR4_COMP_BA0 M5
DDR4_COMP_ALERTn L6
DDR4_COMP_A16 P7
DDR4_COMP_A15 M7
DDR4_COMP_A14 N8
DDR4_COMP_A13 L8
DDR4_COMP_A12 P9
DDR4_COMP_RZQ M9
DDR4_COMP_REFCLKn N10
DDR4_COMP_REFCLKp L10
DDR4_COMP_A11 W12
DDR4_COMP_A10 U12
DDR4_COMP_A9 V13
DDR4_COMP_A8 T13
DDR4_COMP_A7 W14
DDR4_COMP_A6 U14
DDR4_COMP_A5 V15
DDR4_COMP_A3 W16
DDR4_COMP_A2 U16
DDR4_COMP_A1 V17
DDR4_COMP_A0 T17
DDR4_COMP_PAR N12
DDR4_COMP_CLKn L12
DDR4_COMP_CLKp P13
DDR4_COMP_CKE N14
DDR4_COMP_ODT P15
DDR4_COMP_ACTn N16
DDR4_COMP_CSn L16
DDR4_COMP_RESETn P17
DDR4_COMP_BG1 M17

U1F

IO, LVDS3D_25N, DQ36
IO, LVDS3D_25P, DQ36
IO, LVDS3D_26N, DQ36
IO, LVDS3D_26P, DQ36
IO, LVDS3D_27N, DQ36
IO, LVDS3D_27P, DQ36
IO, LVDS3D_28N, DQSN36
IO, LVDS3D_28P, DQSN36
IO, LVDS3D_29N, DQ36
IO, LVDS3D_29P, DQ36
IO, LVDS3D_30N, DQ36
IO, LVDS3D_30P, DQ36
IO, LVDS3D_31N, DQ37
IO, LVDS3D_31P, DQ37
IO, LVDS3D_32N, DQ37
IO, LVDS3D_32P, DQ37
IO, LVDS3D_33N, DQ37
IO, LVDS3D_33P, DQ37
IO, PLL_3D_B_CLKOUT1N, LVDS3D_34N, DQSN37
IO, PLL_3D_B_CLKOUT1P, PLL_3D_B_CLKOUT1, PLL_3D_FB1, LVDS3D_34P, DQ37
IO, LVDS3D_35N, DQ37
IO, RZQ_B_3D, LVDS3D_35P, DQ37
IO, CLK_B_3D_1N, LVDS3D_36N, DQ37
IO, CLK_B_3D_1P, LVDS3D_36P, DQ37
IO, CLK_B_3D_0N, LVDS3D_37N, DQ38
IO, CLK_B_3D_0P, LVDS3D_37P, DQ38
IO, LVDS3D_38N, DQ38
IO, LVDS3D_38P, DQ38
IO, PLL_3D_B_CLKOUT0N, LVDS3D_39N, DQ38
IO, PLL_3D_B_CLKOUT0P, PLL_3D_B_CLKOUT0, PLL_3D_FB0, LVDS3D_39P, DQ38
IO, LVDS3D_40N, DQSN38
IO, LVDS3D_40P, DQSN38
IO, LVDS3D_41N, DQ38
IO, LVDS3D_41P, DQ38
IO, LVDS3D_42N, DQ38
IO, LVDS3D_42P, DQ38
IO, LVDS3D_43N, DQ39
IO, LVDS3D_43P, DQ39
IO, LVDS3D_44N, DQ39
IO, LVDS3D_44P, DQ39
IO, LVDS3D_45N, DQ39
IO, LVDS3D_45P, DQ39
IO, LVDS3D_46N, DQSN39
IO, LVDS3D_46P, DQSN39
IO, LVDS3D_47N, DQ39
IO, LVDS3D_47P, DQ39
IO, LVDS3D_48N, DQ39
IO, LVDS3D_48P, DQ39

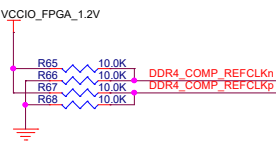
IO, LVDS3D_1N, DQ32
IO, LVDS3D_1P, DQ32
IO, LVDS3D_2N, DQ32
IO, LVDS3D_2P, DQ32
IO, LVDS3D_3N, DQ32
IO, LVDS3D_3P, DQ32
IO, LVDS3D_4N, DQSN32
IO, LVDS3D_4P, DQSN32
IO, LVDS3D_5N, DQ32
IO, LVDS3D_5P, DQ32
IO, LVDS3D_6N, DQ32
IO, LVDS3D_6P, DQ32
IO, LVDS3D_7N, DQ33
IO, LVDS3D_7P, DQ33
IO, LVDS3D_8N, DQ33
IO, LVDS3D_8P, DQ33
IO, LVDS3D_9N, DQ33
IO, LVDS3D_9P, DQ33
IO, PLL_3D_T_CLKOUT1N, LVDS3D_10N, DQSN33
IO, PLL_3D_T_CLKOUT1P, PLL_3D_T_CLKOUT1, PLL_3D_FB1, LVDS3D_10P, DQSN33
IO, LVDS3D_11N, DQ33
IO, RZQ_T_3D, LVDS3D_11P, DQ33
IO, CLK_T_3D_1N, LVDS3D_12N, DQ33
IO, CLK_T_3D_1P, LVDS3D_12P, DQ33
IO, CLK_T_3D_0N, LVDS3D_13N, DQ34
IO, CLK_T_3D_0P, LVDS3D_13P, DQ34
IO, LVDS3D_14N, DQ34
IO, LVDS3D_14P, DQ34
IO, PLL_3D_T_CLKOUT0N, LVDS3D_15N, DQ34
IO, PLL_3D_T_CLKOUT0P, PLL_3D_T_CLKOUT0, PLL_3D_FB0, LVDS3D_15P, DQ34
IO, LVDS3D_16N, DQSN34
IO, LVDS3D_16P, DQSN34
IO, LVDS3D_17N, DQ34
IO, LVDS3D_17P, DQ34
IO, LVDS3D_18N, DQ34
IO, LVDS3D_18P, DQ34
IO, LVDS3D_19N, DQ35
IO, LVDS3D_19P, DQ35
IO, LVDS3D_20N, DQ35
IO, LVDS3D_20P, DQ35
IO, LVDS3D_21N, DQ35
IO, LVDS3D_21P, DQ35
IO, LVDS3D_22N, DQSN35
IO, LVDS3D_22P, DQSN35
IO, LVDS3D_23N, DQ35
IO, LVDS3D_23P, DQ35
IO, LVDS3D_24N, DQ35
IO, LVDS3D_24P, DQ35

H5 DDR4_COMP_DQ7
F5 DDR4_COMP_DQ5
J6 DDR4_COMP_DQ3
G6 DDR4_COMP_DQ1
H7 DDR4_COMP_DBIn0
J8 DDR4_COMP_DQSn0
G8 DDR4_COMP_DQSp0
H9 DDR4_COMP_DQ4
F9 DDR4_COMP_DQ0
J10 DDR4_COMP_DQ6
G10 DDR4_COMP_DQ2
D5 DDR4_COMP_DQ9
B5 DDR4_COMP_DQ13
C6 DDR4_COMP_DQ11
A6 DDR4_COMP_DQ15
D7 DDR4_COMP_DBIn1
B7 DDR4_COMP_DQSn1
C8 DDR4_COMP_DQSp1
A8 DDR4_COMP_DQ5
D9 DDR4_COMP_DQ10
B9 DDR4_COMP_DQ12
C10 DDR4_COMP_DQ14
J12 DDR4_COMP_DQ23
G12 DDR4_COMP_DQ21
H13 DDR4_COMP_DQ17
F13 DDR4_COMP_DQ19
J14 DDR4_COMP_DBIn2
G14 DDR4_COMP_DQSn2
H15 DDR4_COMP_DQSp2
F15 DDR4_COMP_DQ5
J16 DDR4_COMP_DQ20
G16 DDR4_COMP_DQ16
H17 DDR4_COMP_DQ22
F17 DDR4_COMP_DQ18
C12 DDR4_COMP_DQ29
A12 DDR4_COMP_DQ25
D13 DDR4_COMP_DQ31
B13 DDR4_COMP_DQ27
C14 DDR4_COMP_DBIn3
D15 DDR4_COMP_DQSn3
F15 DDR4_COMP_DQSp3
C16 DDR4_COMP_DQ26
A16 DDR4_COMP_DQ24
D17 DDR4_COMP_DQ28
B17 DDR4_COMP_DQ30

BOT TOP

Bank 3D

AGFB014R24A



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Agilex™ F-Series Transceiver-SoC Development Kit			
Title			
Size	Document Number		Rev
B	150-0321502-B		B
Date:	Friday, November 25, 2022	Sheet	19 of 82

FPGA Bank - 3C

DDR4_COMP_DQ[71:0] 19,32,33,34
DDR4_COMP_DBIn[8:0] 19,32,33,34
DDR4_COMP_DQS[8:0] 19,32,33,34
DDR4_COMP_DQSn[8:0] 19,32,33,34

U1G	
DDR4_COMP_DQ35 V19	IO, LVDS3C_25N, DQ44
DDR4_COMP_DQ37 T19	IO, LVDS3C_25P, DQ44
DDR4_COMP_DQ39 W20	IO, LVDS3C_26N, DQ44
DDR4_COMP_DQ33 U20	IO, LVDS3C_26P, DQ44
DDR4_COMP_DBIn4 T21	IO, LVDS3C_27N, DQ44
DDR4_COMP_DQSn4 W22	IO, LVDS3C_27P, DQ44
DDR4_COMP_DQ36 U22	IO, LVDS3C_28N, DQSN44
DDR4_COMP_DQ35 V23	IO, LVDS3C_28P, DQSN44
DDR4_COMP_DQ32 T23	IO, LVDS3C_29N, DQ44
DDR4_COMP_DQ38 W24	IO, LVDS3C_29P, DQ44
DDR4_COMP_DQ34 U24	IO, LVDS3C_30N, DQ44
DDR4_COMP_DQ41 P19	IO, LVDS3C_30P, DQ44
DDR4_COMP_DQ45 M19	IO, LVDS3C_31N, DQ45
DDR4_COMP_DQ43 N20	IO, LVDS3C_31P, DQ45
DDR4_COMP_DQ47 L20	IO, LVDS3C_32N, DQ45
DDR4_COMP_DBIn5 M21	IO, LVDS3C_32P, DQ45
DDR4_COMP_DQSn5 N22	IO, LVDS3C_33N, DQ45
DDR4_COMP_DQSp5 L22	IO, LVDS3C_33P, DQ45
DDR4_COMP_DQ40 P23	IO, PLL_3C_B_CLKOUT1N, LVDS3C_34N, DQSN45
DDR4_COMP_DQ42 M23	IO, PLL_3C_B_CLKOUT1P, PLL_3C_B_CLKOUT1, PLL_3C_B_FB1, LVDS3C_34P, DQSN45
DDR4_COMP_DQ46 N24	IO, RZQ_B_3C, LVDS3C_35P, DQ45
DDR4_COMP_DQ44 L24	IO, CLK_B_3C_1N, LVDS3C_36N, DQ45
DDR4_COMP_DQ51 W26	IO, CLK_B_3C_1P, LVDS3C_36P, DQ45
DDR4_COMP_DQ53 U26	IO, CLK_B_3C_0N, LVDS3C_37N, DQ46
DDR4_COMP_DQ55 V27	IO, CLK_B_3C_0P, LVDS3C_37P, DQ46
DDR4_COMP_DQ49 T27	IO, LVDS3C_38N, DQ46
DDR4_COMP_DBIn6 U28	IO, LVDS3C_38P, DQ46
DDR4_COMP_DQSn6 V28	IO, PLL_3C_B_CLKOUT0N, LVDS3C_39N, DQ46
DDR4_COMP_DQSp6 T29	IO, PLL_3C_B_CLKOUT0P, PLL_3C_B_CLKOUT0, PLL_3C_B_FB0, LVDS3C_39P, DQ46
DDR4_COMP_DQ52 W30	IO, LVDS3C_40N, DQSN46
DDR4_COMP_DQ48 U30	IO, LVDS3C_40P, DQSN46
DDR4_COMP_DQ54 V31	IO, LVDS3C_41N, DQ46
DDR4_COMP_DQ50 T31	IO, LVDS3C_41P, DQ46
DDR4_COMP_DQ57 N26	IO, LVDS3C_42N, DQ46
DDR4_COMP_DQ61 L26	IO, LVDS3C_42P, DQ46
DDR4_COMP_DQ59 P27	IO, LVDS3C_43N, DQ47
DDR4_COMP_DQ63 M27	IO, LVDS3C_43P, DQ47
DDR4_COMP_DBIn7 L28	IO, LVDS3C_44N, DQ47
DDR4_COMP_DQSn7 P28	IO, LVDS3C_44P, DQ47
DDR4_COMP_DQSp7 M29	IO, LVDS3C_45N, DQ47
DDR4_COMP_DQ58 N30	IO, LVDS3C_45P, DQ47
DDR4_COMP_DQ56 L30	IO, LVDS3C_46N, DQSN47
DDR4_COMP_DQ60 P31	IO, LVDS3C_46P, DQSN47
DDR4_COMP_DQ62 M31	IO, LVDS3C_47N, DQ47
	IO, LVDS3C_47P, DQ47
	IO, LVDS3C_48N, DQ47
	IO, LVDS3C_48P, DQ47

BOT TOP

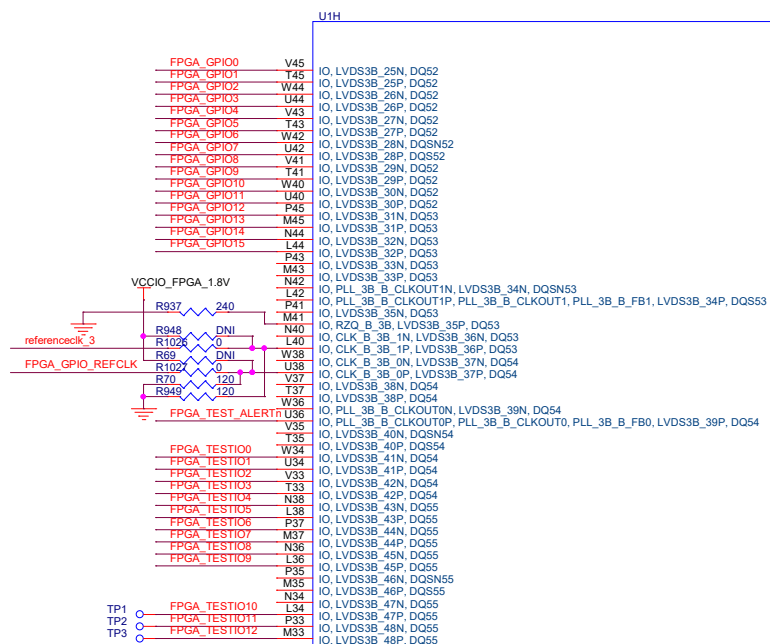
Bank 3C

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Title			
Agilex™ F-Series Transceiver-SoC Development Kit			
Size	Document Number	Rev	
B	150-0321502-B	B	
Date:	Friday, November 25, 2022	Sheet	20 of 82

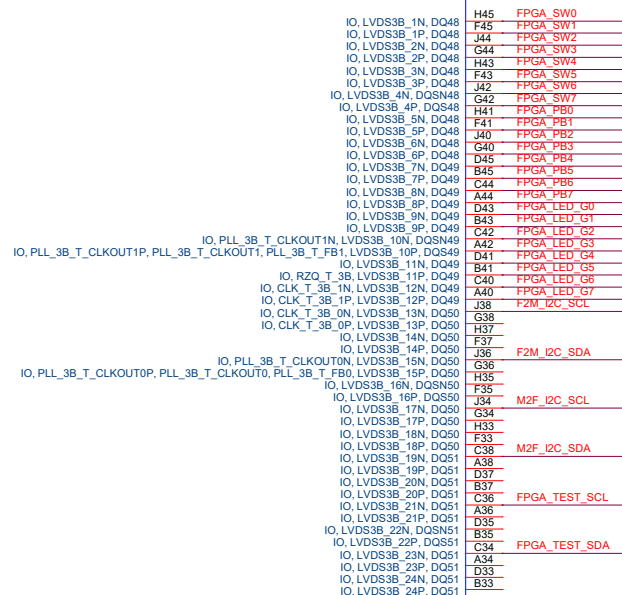
FPGA Bank - 3B



[BOT](#) | [TOP](#)

Bank 3B

AGFB014R24A



41 FPGA_PB[7:0]
41 FPGA_LED_G[7:0]
41 FPGA_SW[7:0]
47 FPGA_GPIO[15:0]
41 FPGA_TESTIO[9:0]

47 F2M I2C SCL

47 F2M I2C SDA

47 M2F I2C SCL

47 M2F I2C SDA

52 FPGA_GPIO_REFCLK

53 referenceclk 3

```

41 FPGA TEST SCL
41 FPGA TEST SDA
41 FPGA TEST ALERTn

```

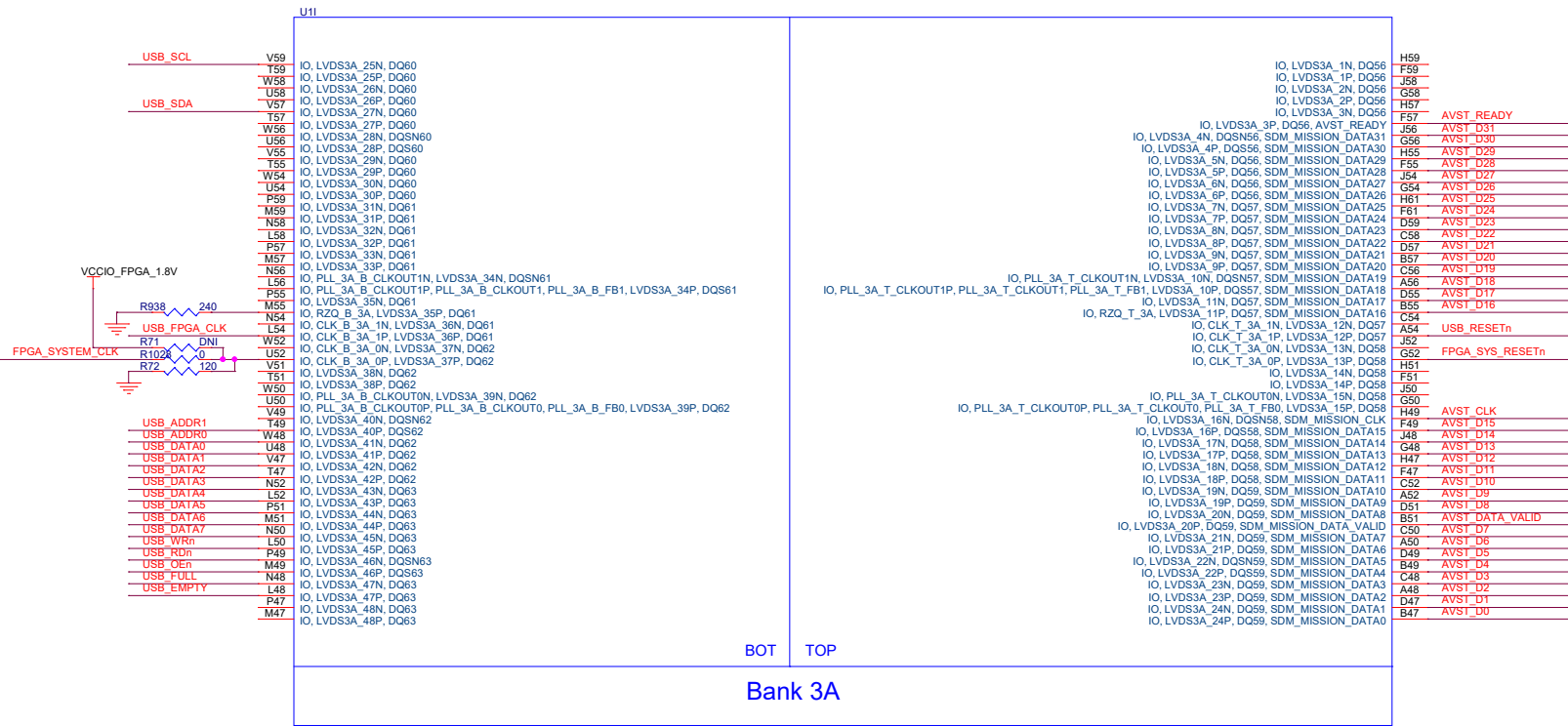
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Agilex™ F-Series Transceiver-SoC Development Kit

Size B	Document Number 150-0321502-B	Rev B
Date: Friday, November 25, 2022	Sheet 21 of 82	



FPGA Bank - 3A

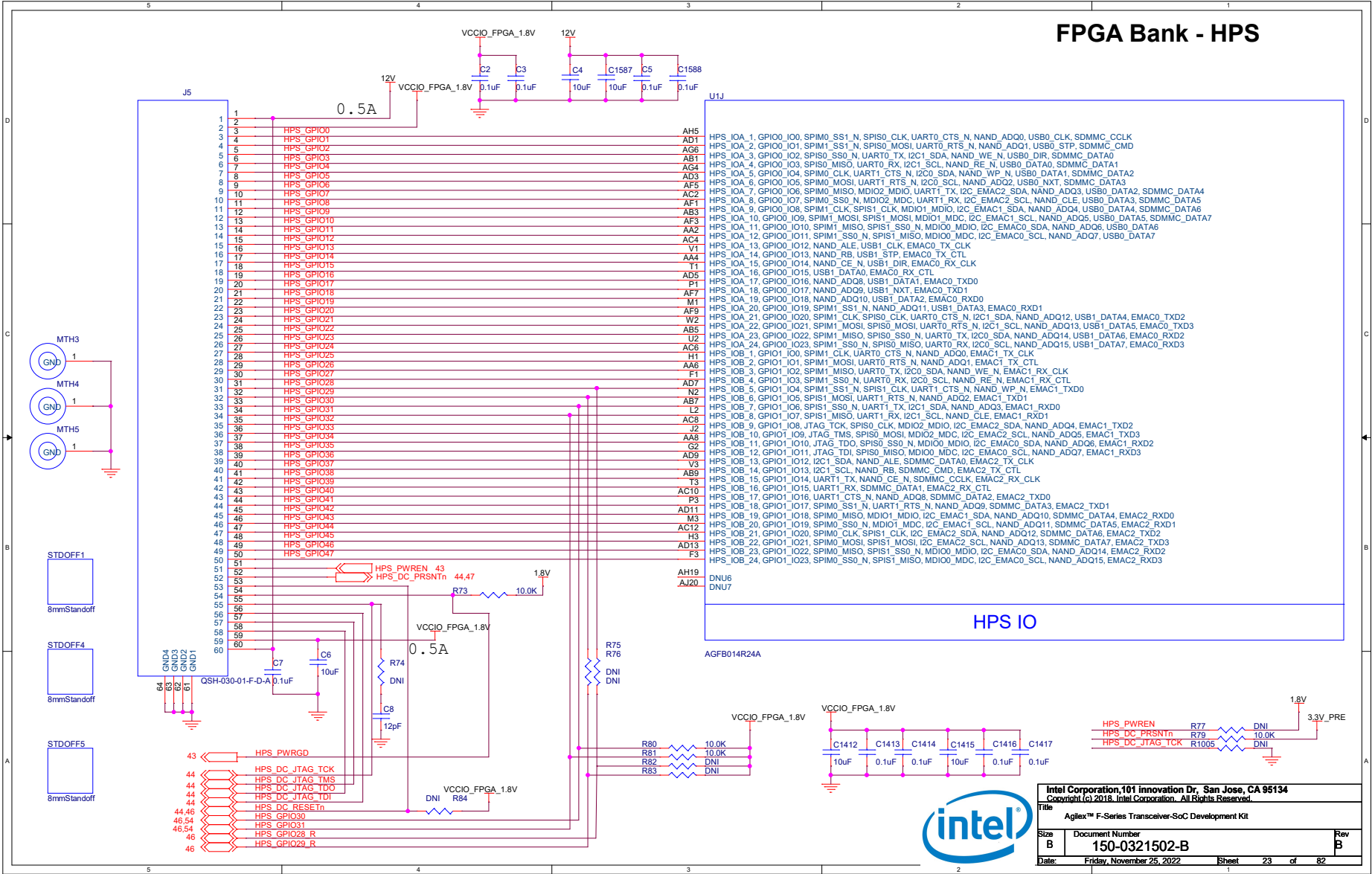


AVST D(31:0) 47
AVST CLK 47
AVST DATA VALID 47
AVST READY 47

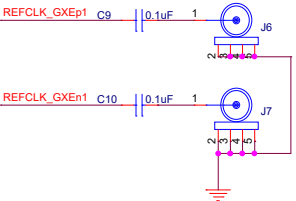
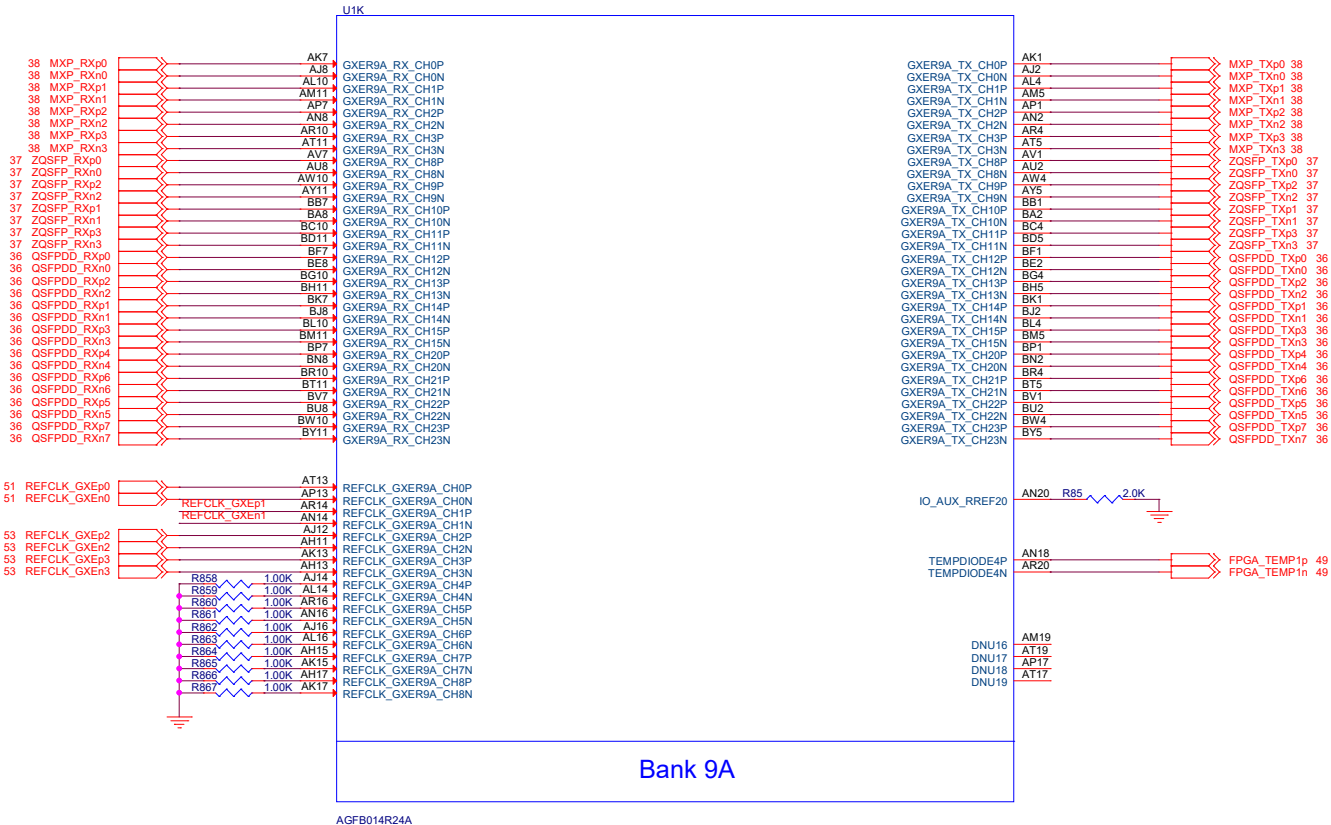
47 FPGA_SYS_RESETn
52 FPGA_SYSTEM_CLK
43 USB_RESETn
43 USB_FPGA_CLK
43 USB_ADDR(1:0)
43 USB_DATA(7:0)
43 USB_WRn
43 USB_RDn
43 USB_Cn
43 USB_FULL
43 USB_EMPTY
43 USB_SCL
43 USB_SDA



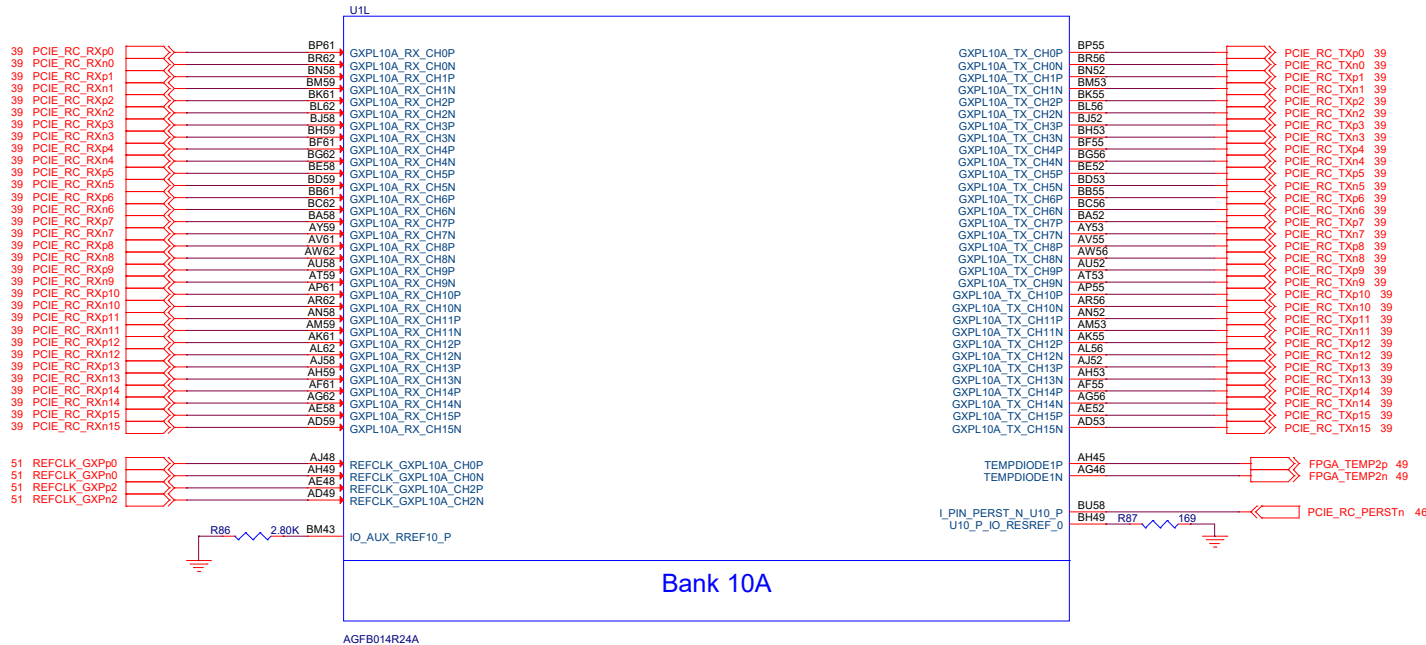
FPGA Bank - HPS



FPGA Bank - 9A E-tile



FPGA Bank - 10A P-tile



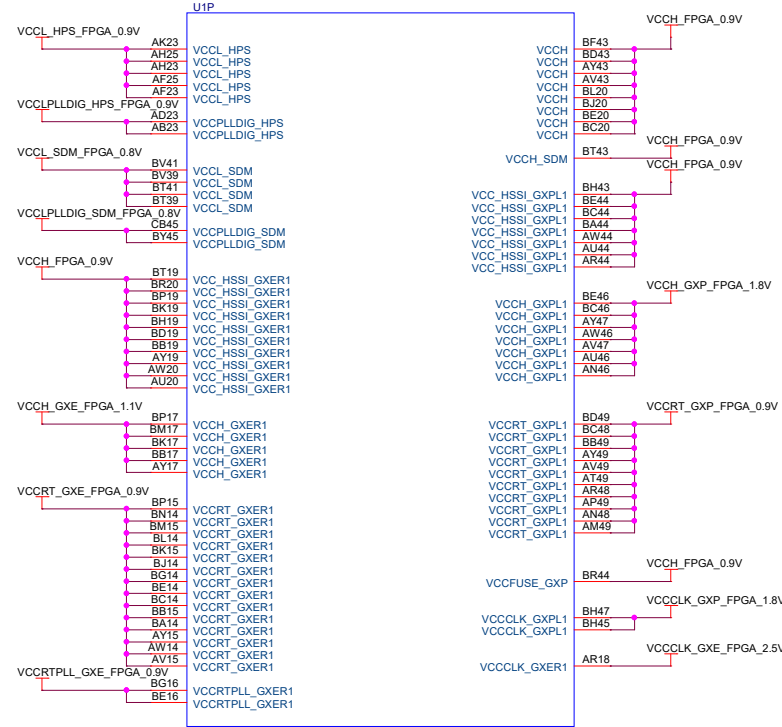
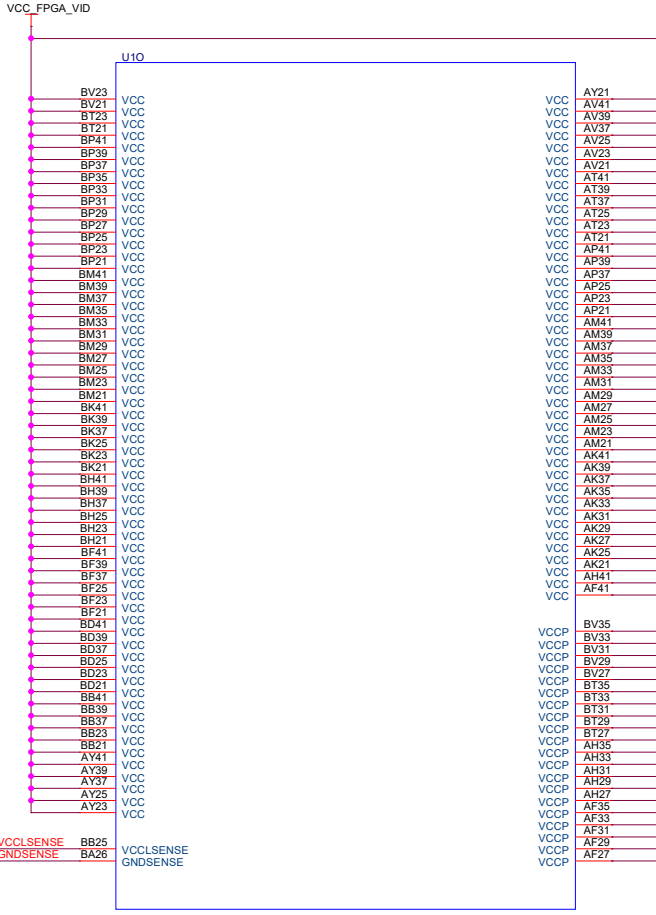
Bank 10A

AGFB014R24A



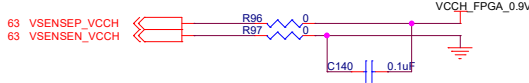
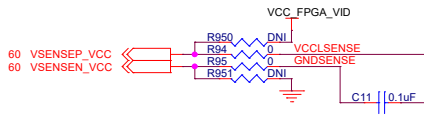
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Title Agilex™ F-Series Transceiver-SoC Development Kit			
Size B	Document Number 150-0321502-B		Rev B
Date:	Friday, November 25, 2022		Sheet 25 of 82

FPGA Power 1



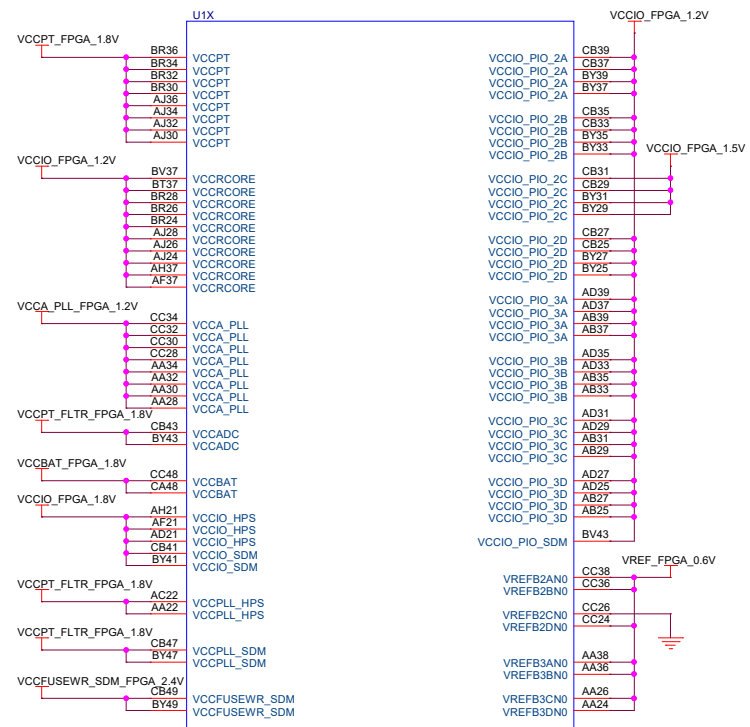
VCCLSENSE BB25
GNDSENSE BA26

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Agilex™ F-Series Transceiver-SoC Development Kit			
Size	Document Number	Rev	
B	150-0321502-B	B	
Date:	Friday, November 25, 2022	Sheet	26 of 82

FPGA Power 2

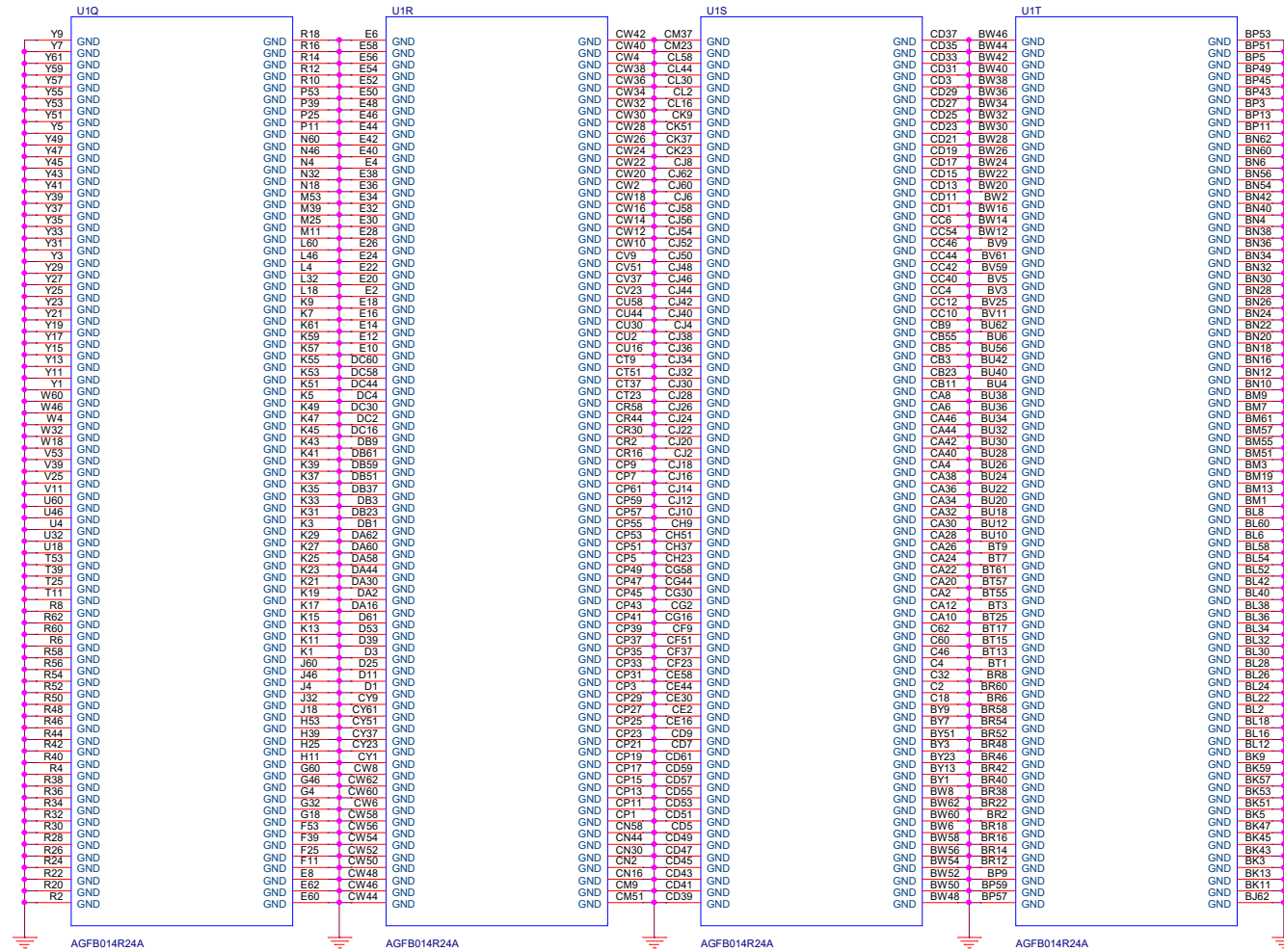


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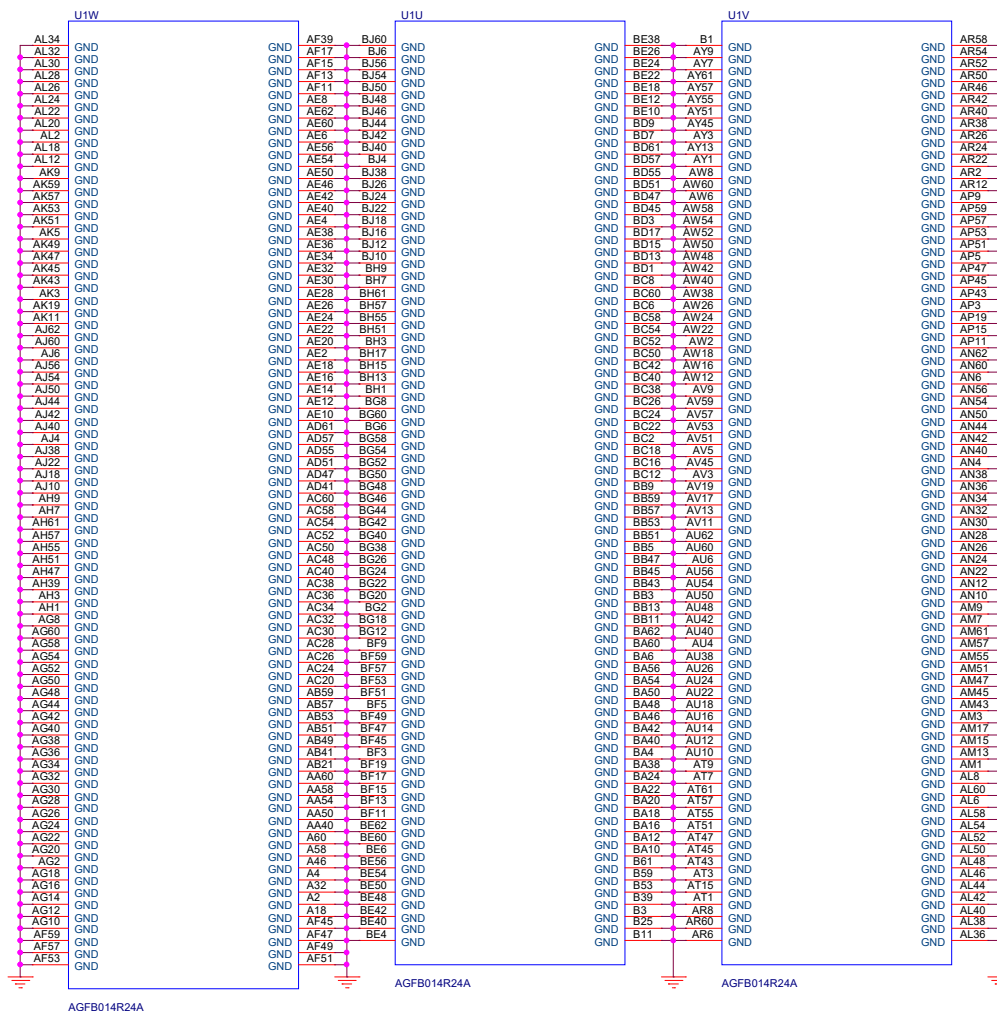
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Title			
Agilex™ F-Series Transceiver-SoC Development Kit			
Size	Document Number	Rev	
B	150-0321502-B	B	
Date:	Friday, November 25, 2022	Sheet	27 of 82

FPGA GND 1



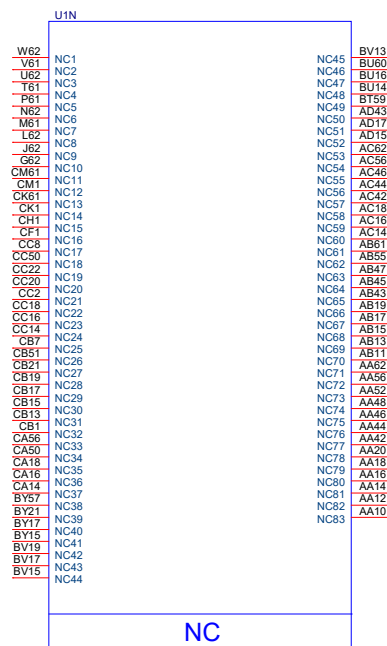
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Title: Agilix™ F-Series Transceiver-SoC Development Kit	
Size: B	Document Number: 150-0321502-B
Date: Friday, November 25, 2022	Sheet: 28 of 82

FPGA GND 2

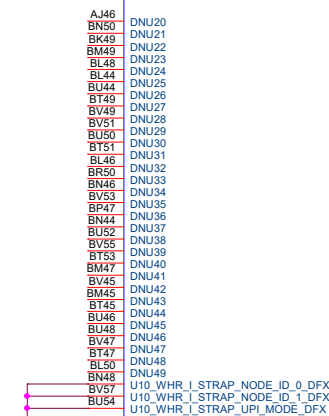
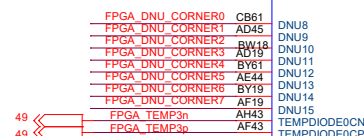


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Title: Agilent™ F-Series Transceiver-SoC Development Kit	
Size: B	Document Number: 150-0321502-B
Date: Friday, November 25, 2022	Sheet: 29 of 82

FPGA NC/DNU



AGFB014R24A



DNU

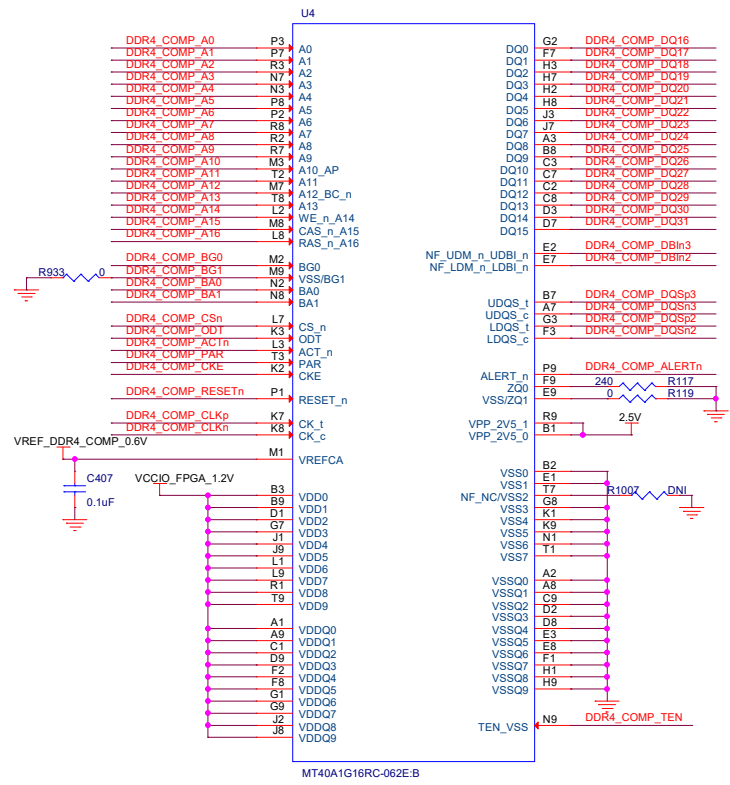
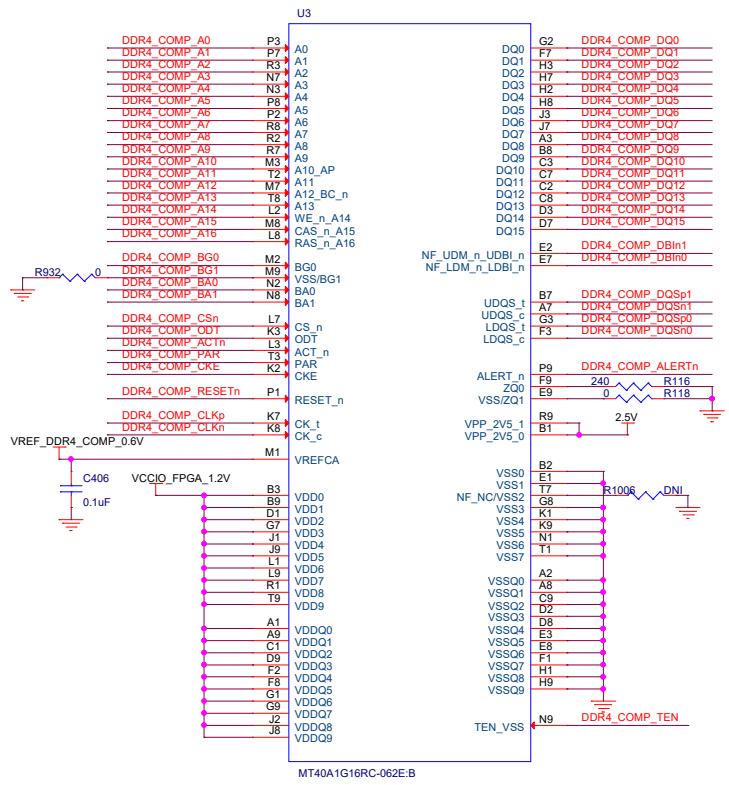
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Title: Agilix™ F-Series Transceiver-SoC Development Kit			
Size: B	Document Number: 150-0321502-B	Rev: B	
Date: Friday, November 25, 2022	Sheet: 1	30	of 82

DDR4 COMPONENT #1/#2

DDR4_COMP_CLKp 19.33.34	DDR4_COMP_DQ[7:0] 19.20.33.34
DDR4_COMP_CLKn 19.33.34	DDR4_COMP_DBI[0] 19.20.33.34
DDR4_COMP_BA[1:0] 19.33.34	DDR4_COMP_DQS[8:0] 19.20.33.34
DDR4_COMP_A[16:0] 19.33.34	DDR4_COMP_DQS[8:0] 19.20.33.34
DDR4_COMP_CSn 19.33.34	DDR4_COMP_RESETn 19.33.34
DDR4_COMP_ODT 19.33.34	DDR4_COMP_ALERTn 19.33.34
DDR4_COMP_ACTn 19.33.34	DDR4_COMP_TEN 33.34
DDR4_COMP_PAR 19.33.34	
DDR4_COMP_CKE 19.33.34	
DDR4_COMP_BG0 19.33.34	
DDR4_COMP_BG1 19.33.34	

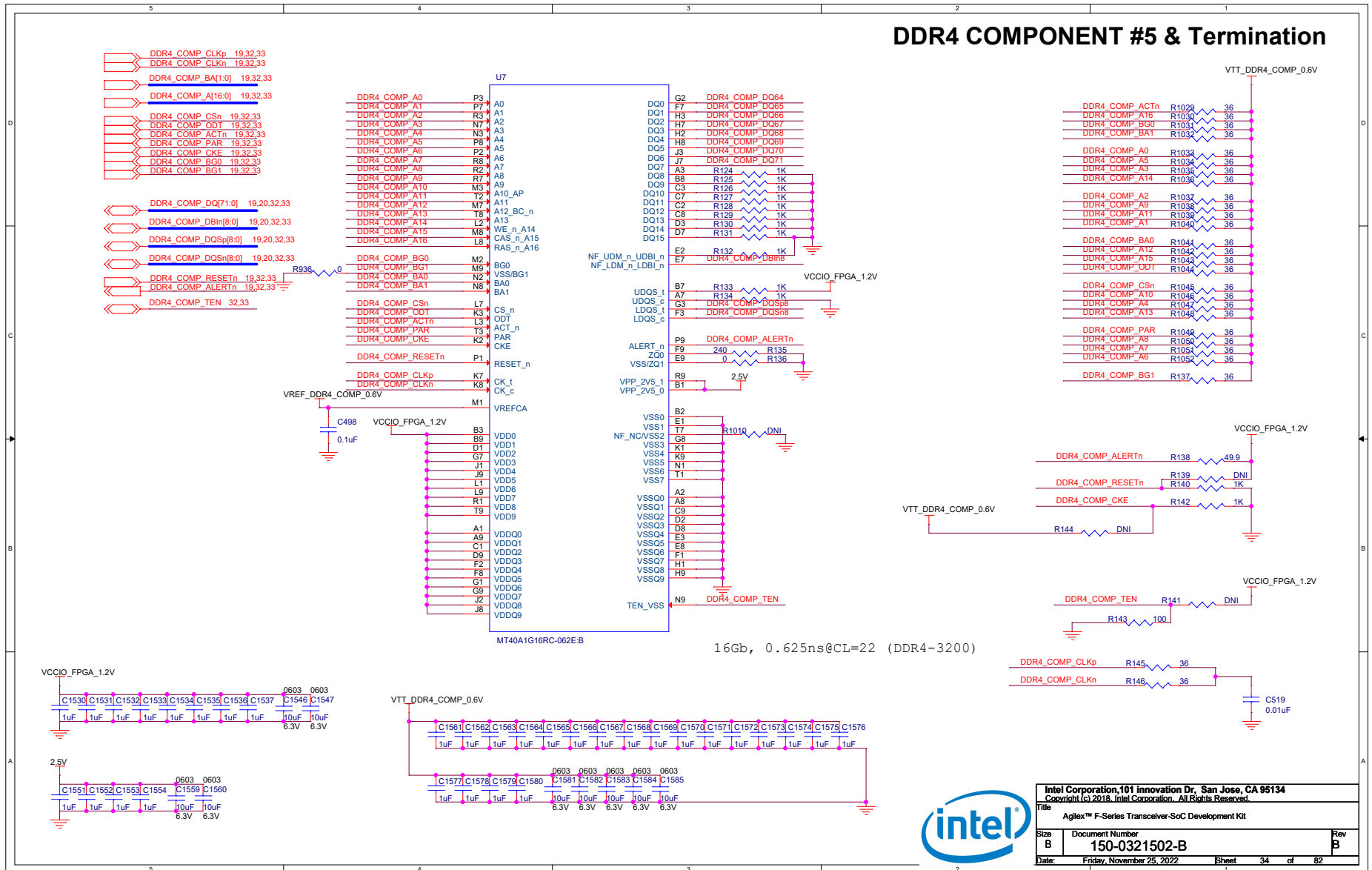


16Gb, 0.625ns@CL=22 (DDR4-3200)

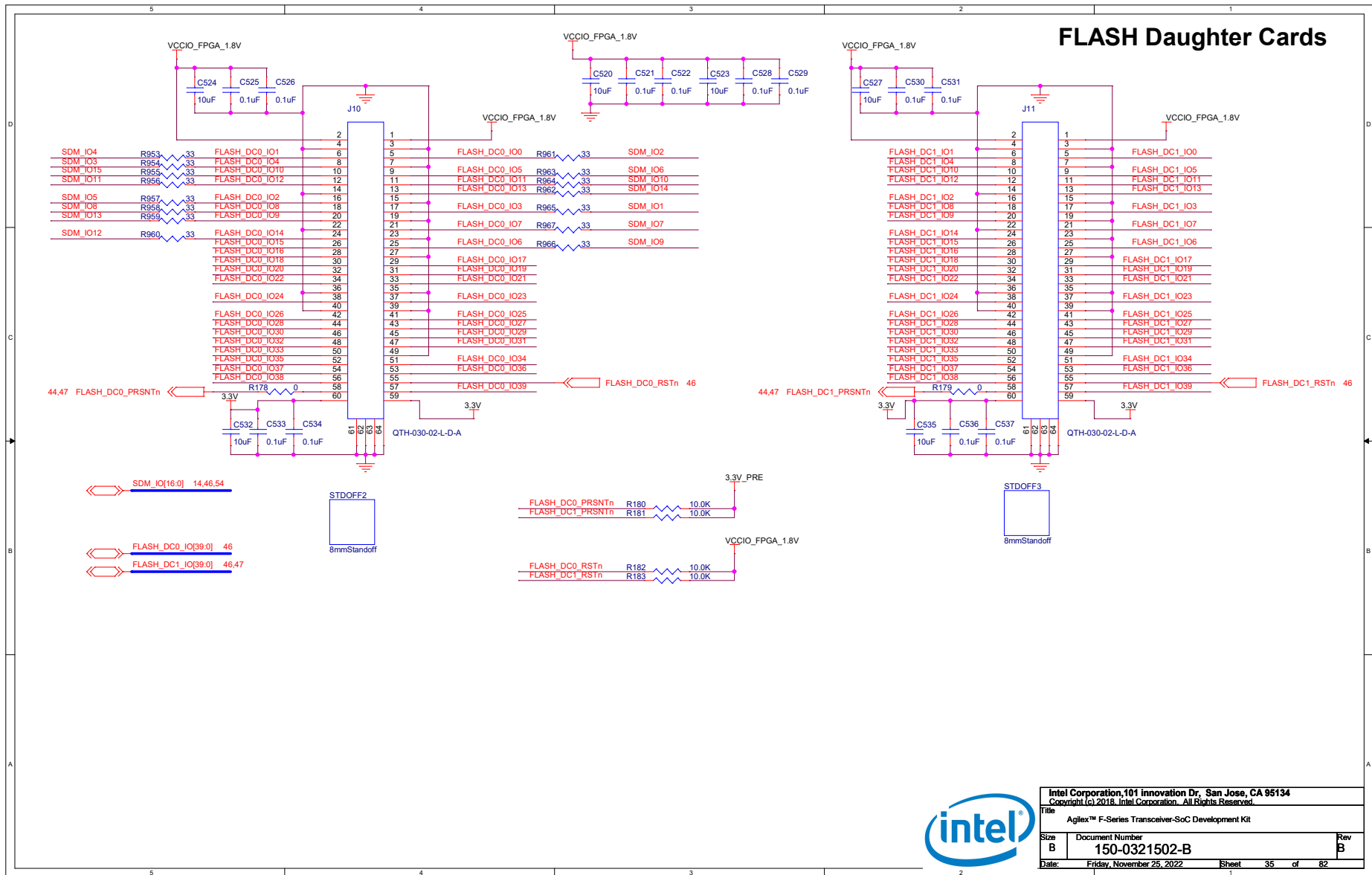


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Agilex™ F-Series Transceiver-SoC Development Kit	
Size B	Document Number 150-0321502-B
Date: Friday, November 25, 2022	Sheet 32 of 82

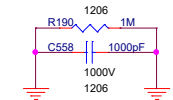
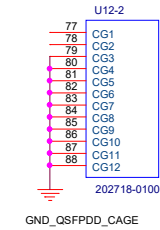
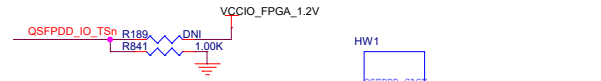
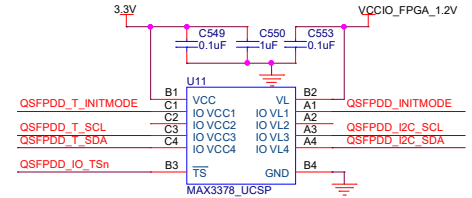
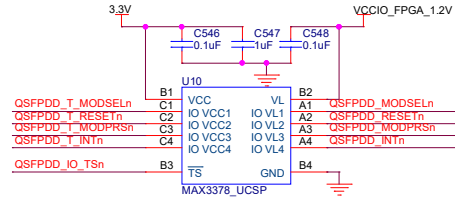
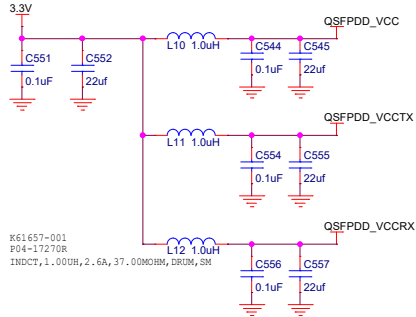
DDR4 COMPONENT #5 & Termination



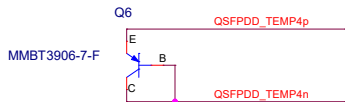
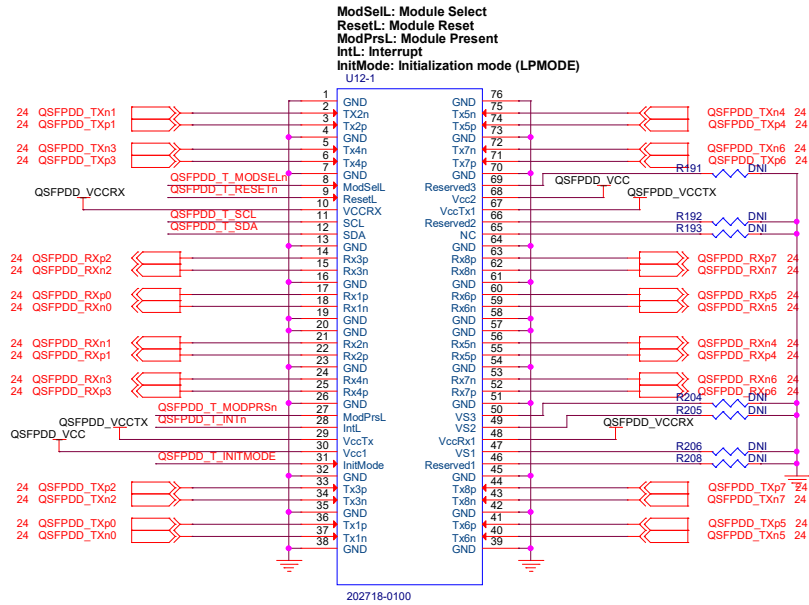
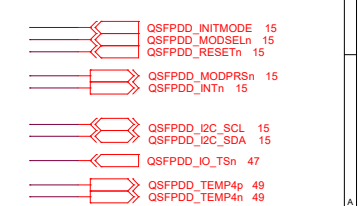
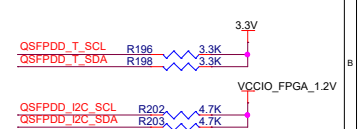
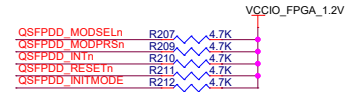
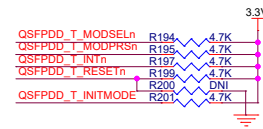
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Agilex™ F-Series Transceiver-SoC Development Kit			
Size	Document Number	Rev	
B	150-0321502-B	B	
Date:	Friday, November 25, 2022	Sheet	34 of 82



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Title: Agilix™ F-Series Transceiver-SoC Development Kit			
Size: B	Document Number: 150-0321502-B	Rev: B	
Date: Friday, November 25, 2022	Sheet: 35	of 82	

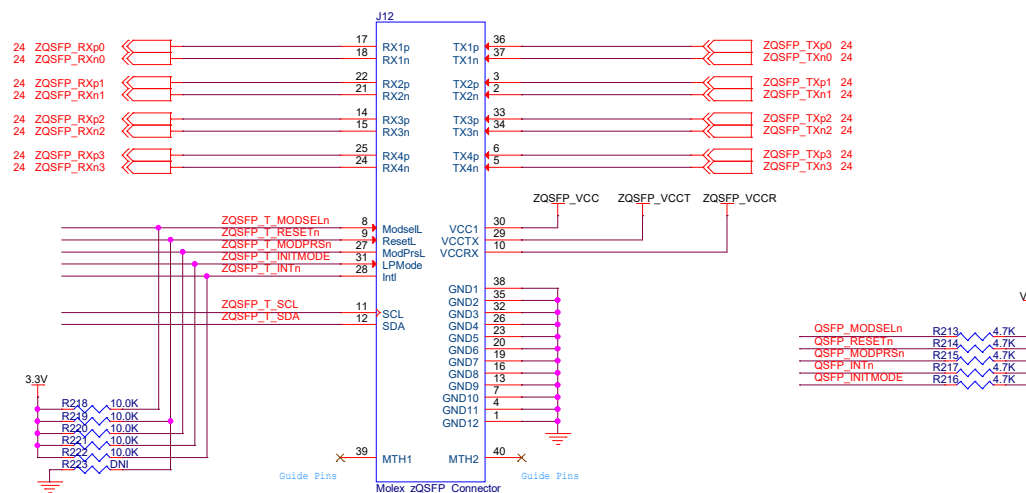
QSFPDD 1x1

Cage GND on top layer

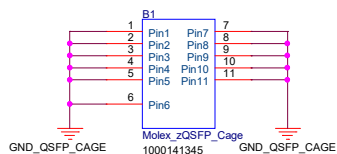
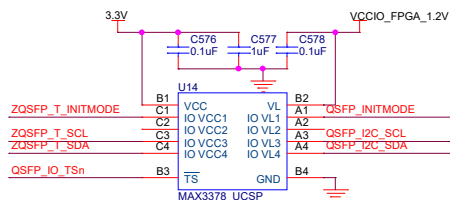
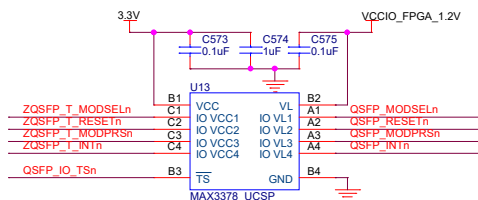


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Title Agilex™ F-Series Transceiver-SoC Development Kit			
Size B	Document Number 150-0321502-B		Rev B
Date:	Friday, November 25, 2022	Sheet	36 of 82

zQSFP

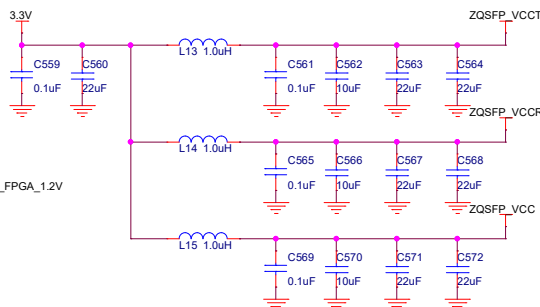


ZQSFP: Molex MPN 170432-0002

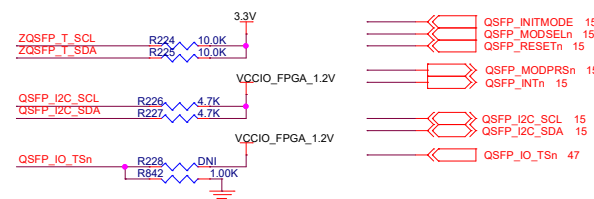


MOLEX MPN 1000141345

- NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.
- NOTE 2: zQSFP 100-ohm termination is implemented via the FPGA on-chip termination.
- NOTE 3: DC blocking capacitors are in the module for RX and TX.
- NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.

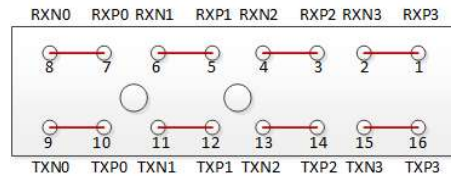
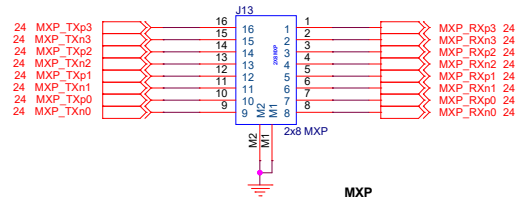


Place close to zQSFP Connector

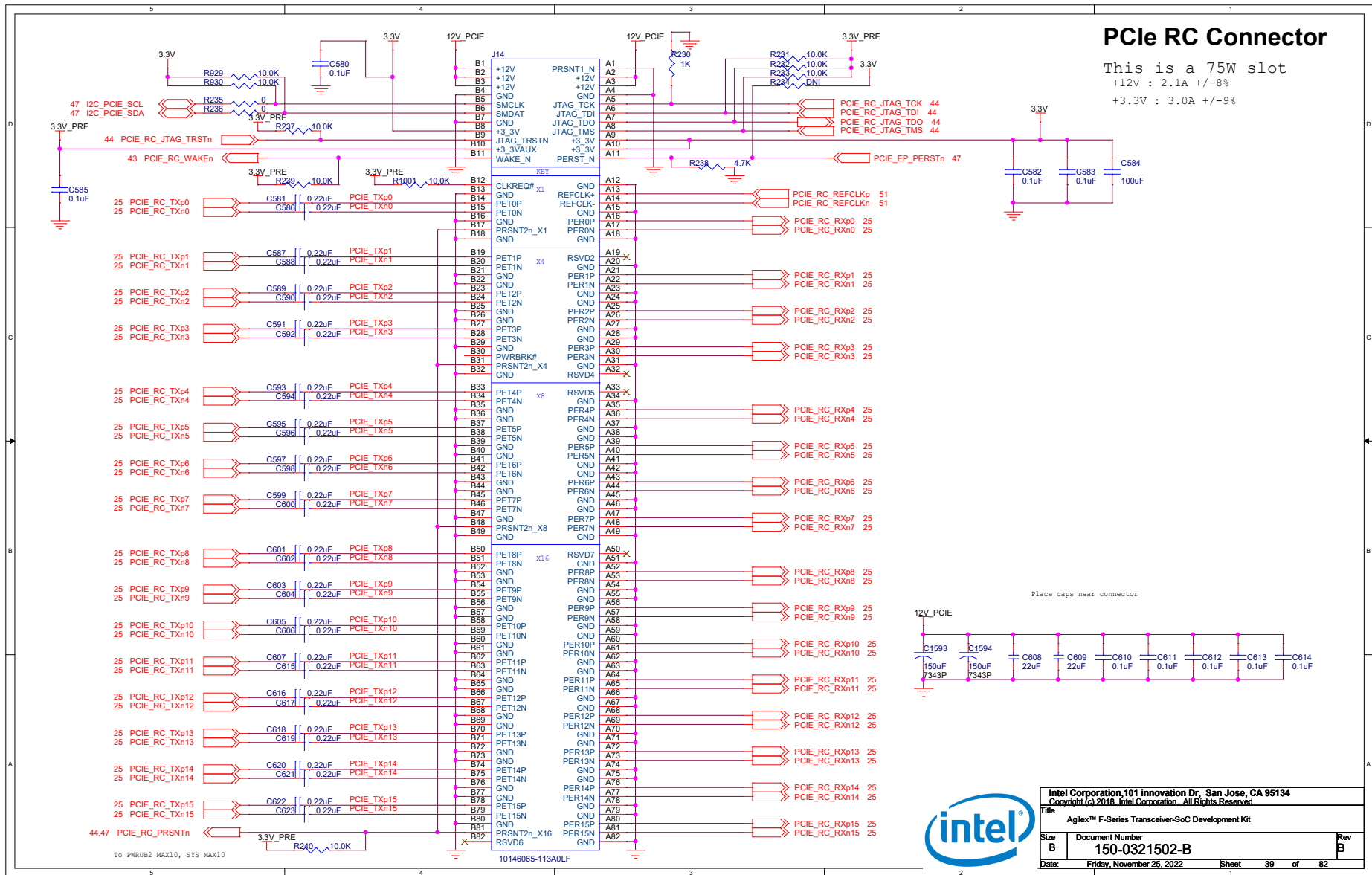


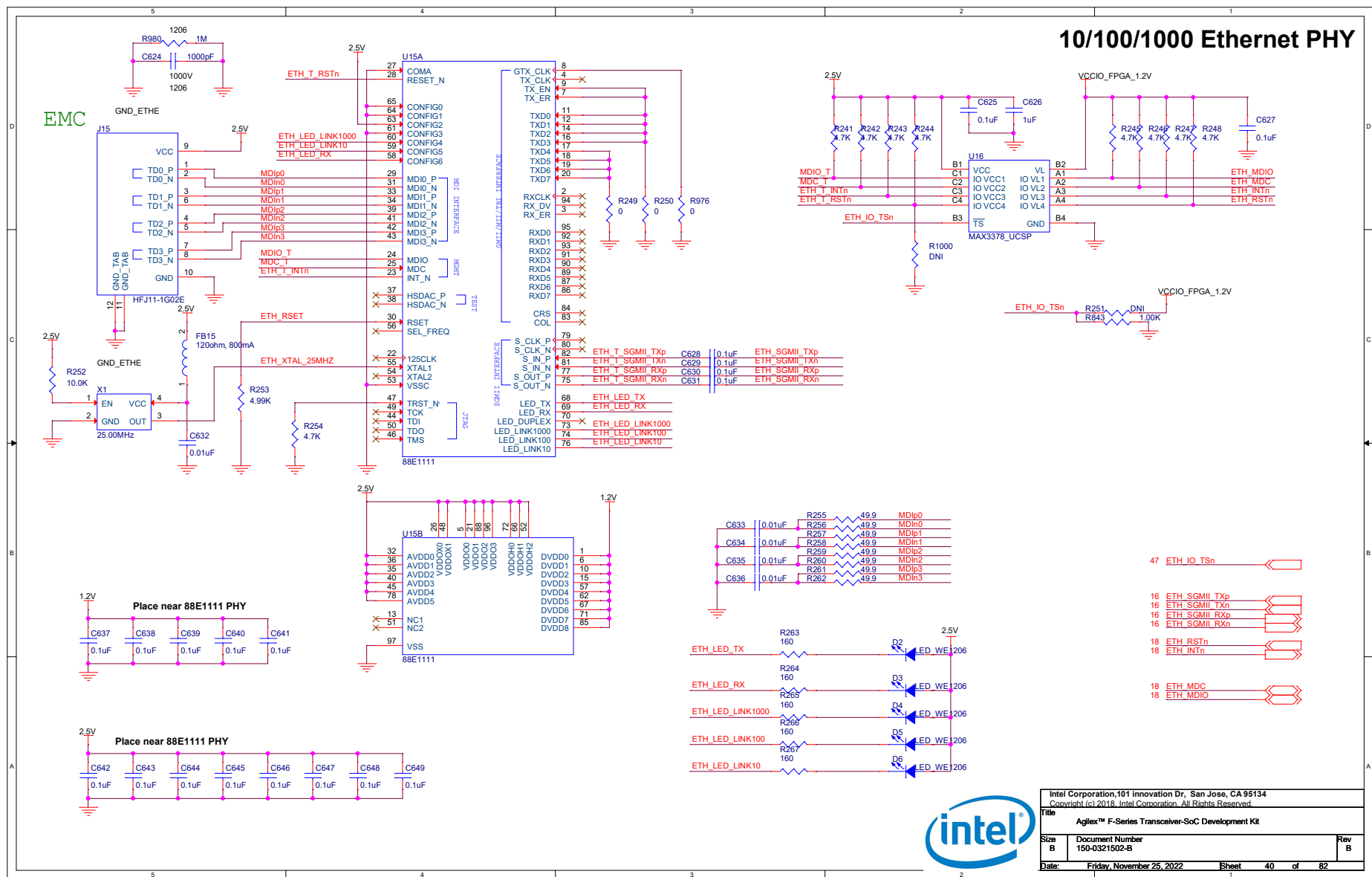
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Title: Agilix™ F-Series Transceiver-Soc Development Kit			
Size: B	Document Number: 150-0321502-B	Rev: B	
Date: Friday, November 25, 2022	Sheet: 37	of 82	

MXP / 2.4mm Connectors

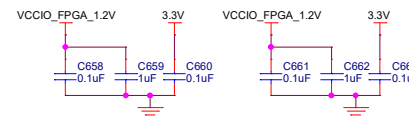
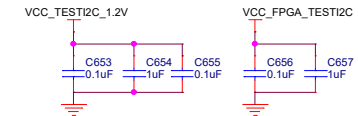
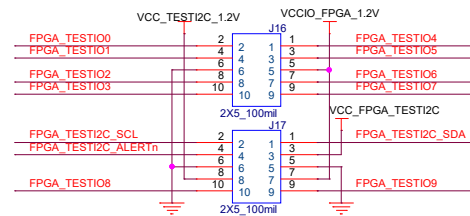
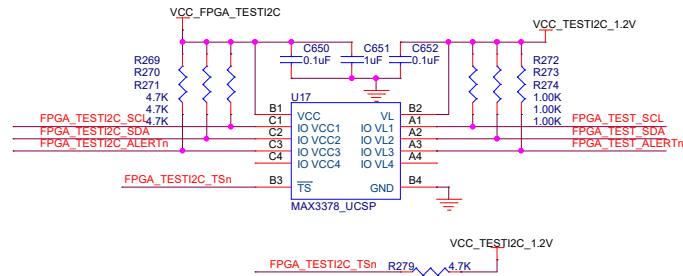
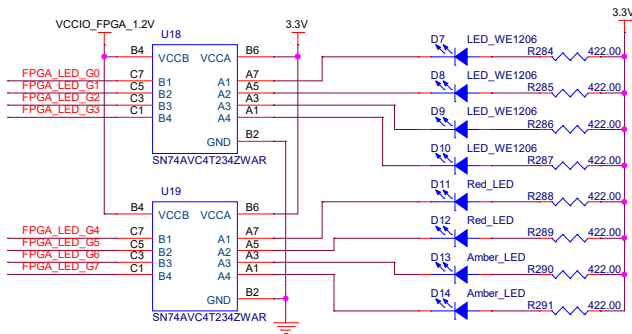
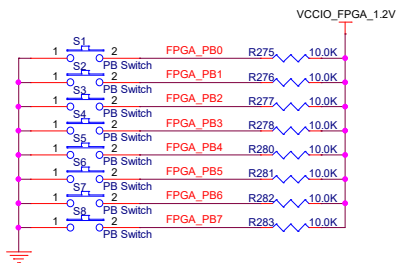
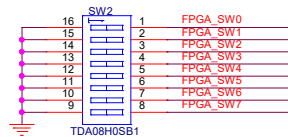
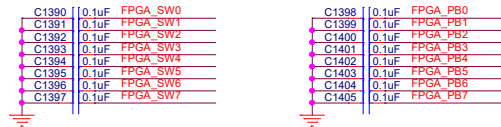


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Size B	Document Number 150-0321502-B		Rev B
Date:	Friday, November 25, 2022	Sheet	38 of 82





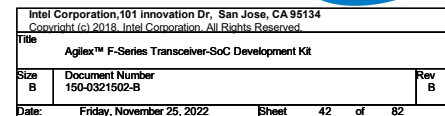
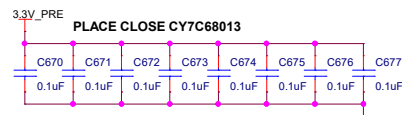
FPGA SW, PB, LED & Test IOs



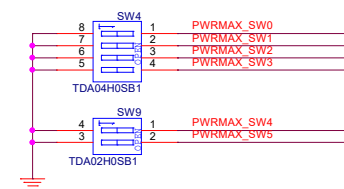
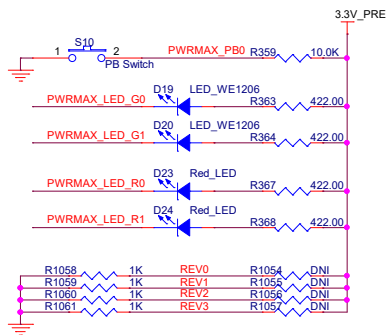
- 21 FPGA_PB[7:0]
- 21 FPGA_LED_G[7:0]
- 21 FPGA_SW[7:0]
- 21 FPGA_TESTI2C[9:0]
- 21 FPGA_TEST_SCL
- 21 FPGA_TEST_SDA
- 21 FPGA_TEST_ALERTn



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Agilex™ F-Series Transceiver-SoC Development Kit			
Size	Document Number	Rev	
B	150-0321502-B	B	
Date:	Friday, November 25, 2022	Sheet	41 of 82

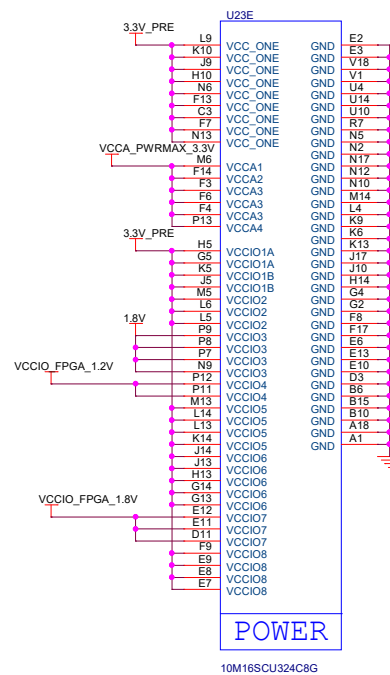


PWRMAX 10

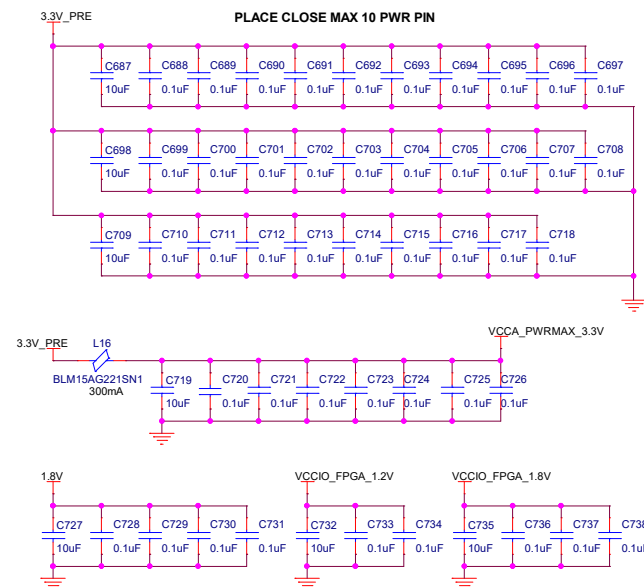


Pin	Function
SW0	Reserved
SW1	VCCFUSEWR_SDM FPGA 2.4V_SETh
SW2	VCC_L HPS_FPGA 0.9V BYPASS_M0C0m
SW3	12M05026_P0n
SW4	Reserved
SW5	Reserved

Pin	Function
G0	PG FPGA
G1	PG SYSMAX
R0	PWR_ERR
R1	Over Voltage/Current
PB0	FPGA Power Cycle



PLACE CLOSE MAX 10 PWR PIN



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Title Agilex™ F-Series Transceiver-Soc Development Kit		
Size B	Document Number 150-0321502-B	Rev B
Date: Friday, November 25, 2022	Sheet 45	of 82

1.8V

U29A

BANK 1A/1B

BANK 2

LEFT BANKS

10M16SCU324C8G

1.8V

U29B

BANK 3

BANK 4

BOTTOM BANKS

10M16SCU324C8G

1.8V

U29C

BANK 5

BANK 6

RIGHT BANKS

10M16SCU324C8G

1.8V

U29D

BANK 7

BANK 8

RIGHT BANKS

10M16SCU324C8G

1.8V

U29E

BANK 9

BANK 10

RIGHT BANKS

10M16SCU324C8G

1.8V

U29F

BANK 11

BANK 12

RIGHT BANKS

10M16SCU324C8G

1.8V

U29G

BANK 13

BANK 14

RIGHT BANKS

10M16SCU324C8G

1.8V

U29H

BANK 15

BANK 16

RIGHT BANKS

10M16SCU324C8G

1.8V

U29I

BANK 17

BANK 18

RIGHT BANKS

10M16SCU324C8G

1.8V

U29J

BANK 19

BANK 20

RIGHT BANKS

10M16SCU324C8G

1.8V

U29K

BANK 21

BANK 22

RIGHT BANKS

10M16SCU324C8G

1.8V

U29L

BANK 23

BANK 24

RIGHT BANKS

10M16SCU324C8G

1.8V

U29M

BANK 25

BANK 26

RIGHT BANKS

10M16SCU324C8G

1.8V

U29N

BANK 27

BANK 28

RIGHT BANKS

10M16SCU324C8G

1.8V

U29O

BANK 29

BANK 30

RIGHT BANKS

10M16SCU324C8G

1.8V

U29P

BANK 31

BANK 32

RIGHT BANKS

10M16SCU324C8G

1.8V

U29Q

BANK 33

BANK 34

RIGHT BANKS

10M16SCU324C8G

1.8V

U29R

BANK 35

BANK 36

RIGHT BANKS

10M16SCU324C8G

1.8V

U29S

BANK 37

BANK 38

RIGHT BANKS

10M16SCU324C8G

1.8V

U29T

BANK 39

BANK 40

RIGHT BANKS

10M16SCU324C8G

1.8V

U29U

BANK 41

BANK 42

RIGHT BANKS

10M16SCU324C8G

1.8V

U29V

BANK 43

BANK 44

RIGHT BANKS

10M16SCU324C8G

1.8V

U29W

BANK 45

BANK 46

RIGHT BANKS

10M16SCU324C8G

1.8V

U29X

BANK 47

BANK 48

RIGHT BANKS

10M16SCU324C8G

1.8V

U29Y

BANK 49

BANK 50

RIGHT BANKS

10M16SCU324C8G

1.8V

U29Z

BANK 51

BANK 52

RIGHT BANKS

10M16SCU324C8G

1.8V

U29AA

BANK 53

BANK 54

RIGHT BANKS

10M16SCU324C8G

1.8V

U29AB

BANK 55

BANK 56

RIGHT BANKS

10M16SCU324C8G

1.8V

U29AC

BANK 57

BANK 58

RIGHT BANKS

10M16SCU324C8G

1.8V

U29AD

BANK 59

BANK 60

RIGHT BANKS

10M16SCU324C8G

1.8V

U29AE

BANK 61

BANK 62

RIGHT BANKS

10M16SCU324C8G

1.8V

U29AF

BANK 63

BANK 64

RIGHT BANKS

10M16SCU324C8G

1.8V

U29AG

BANK 65

BANK 66

RIGHT BANKS

10M16SCU324C8G

1.8V

U29AH

BANK 67

BANK 68

RIGHT BANKS

10M16SCU324C8G

1.8V

U29AI

BANK 69

BANK 70

RIGHT BANKS

10M16SCU324C8G

1.8V

U29AJ

BANK 71

BANK 72

RIGHT BANKS

10M16SCU324C8G

1.8V

U29AK

BANK 73

BANK 74

RIGHT BANKS

10M16SCU324C8G

1.8V

U29AL

BANK 75

BANK 76

RIGHT BANKS

10M16SCU324C8G

1.8V

U29AM

BANK 77

BANK 78

RIGHT BANKS

10M16SCU324C8G

1.8V

U29AN

BANK 79

BANK 80

RIGHT BANKS

10M16SCU324C8G

1.8V

U29AO

BANK 81

BANK 82

RIGHT BANKS

10M16SCU324C8G

1.8V

U29AP

BANK 83

BANK 84

RIGHT BANKS

10M16SCU324C8G

1.8V

U29AQ

BANK 85

BANK 86



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Size B	Document Number 150-0321502-B			Rev B
Date:	Friday, November 25, 2022	Sheet	46	of 82

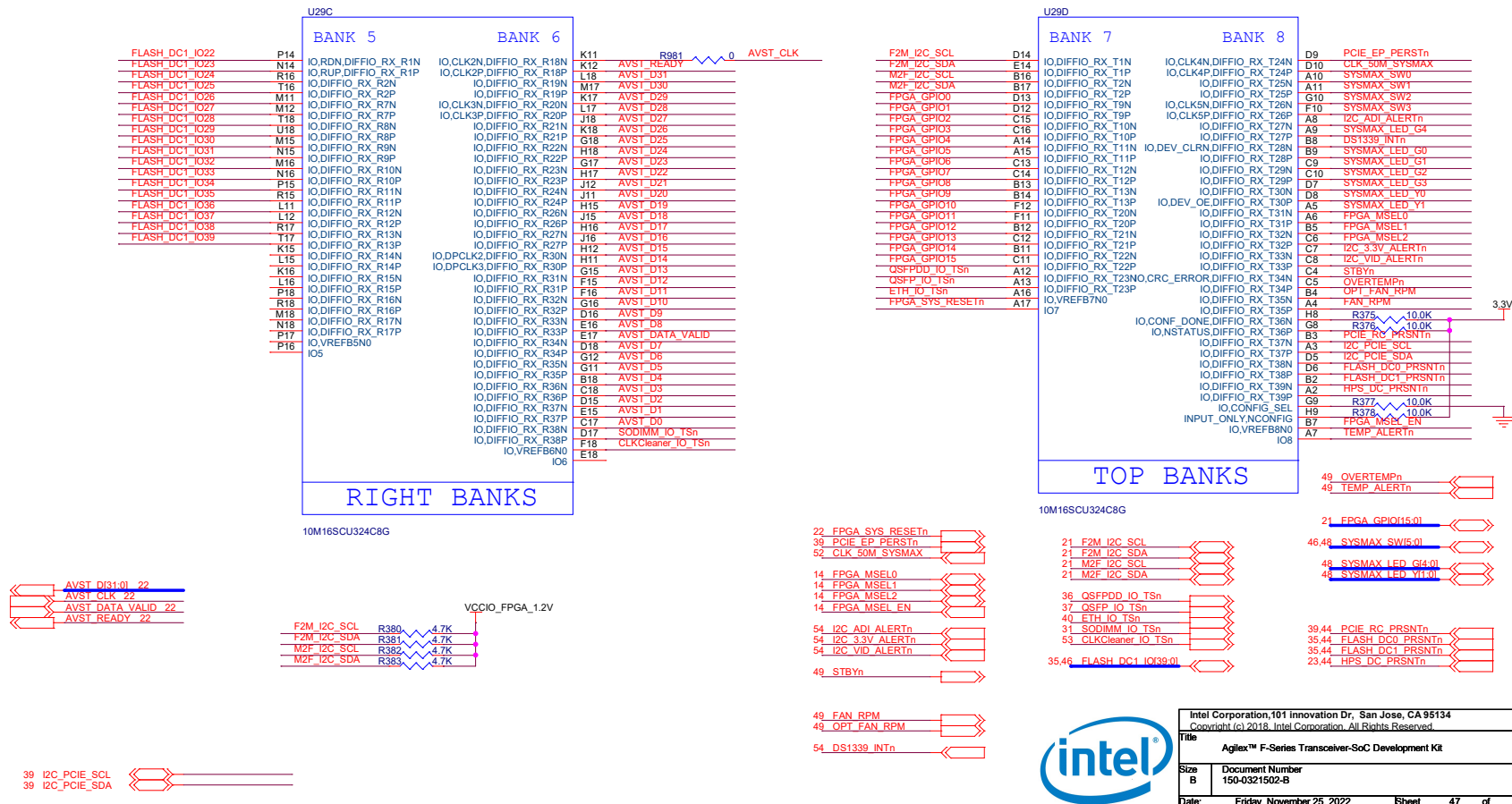
SYSMAX 10

FPGA 1.8V

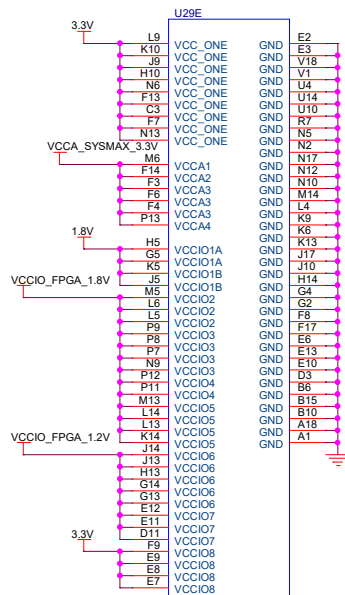
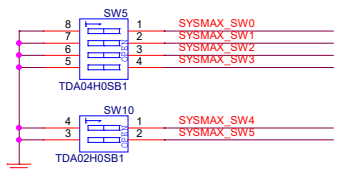
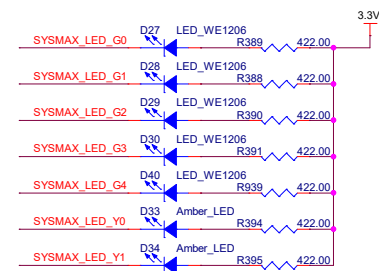
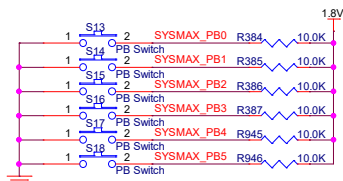
FPGA 1.2V

FPGA 1.2V

3.3V



SYSMAX 10



POWER

10M16SCU324C8G

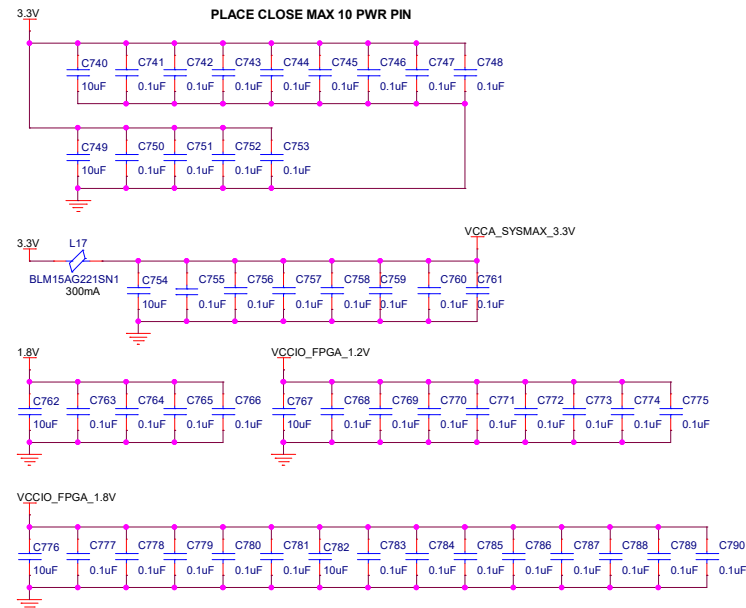
Pin	Function
SW0	FACTORY LOADn
SW1	CLKSEL 156M
SW2	Reserved
SW3	Reserved
SW4	I2C 3.3V BUS_DEBUG MODEn
SW5	CLKCleaner IO_DEBUG MODEn

Pin	Function
G0	PGM_LED0
G1	PGM_LED1
G2	PGM_LED2
G3	MAX_LOAD
G4	MAX_CONF_DONE
Y0	MAX_ERROR
Y1	OVERTEMP

Pin	Function
PB0	MAX RESETn
PB1	CPU RESETn
PB2	RFS_COLD RESETn
PB3	Reserved
PB4	PGM_SEL
PB5	PGM_CFG

46,47 SYSMAX_SW[5:0]
46 SYSMAX_PB[5:0]

47 SYSMAX_LED_G[4:0]
47 SYSMAX_LED_Y[1:0]

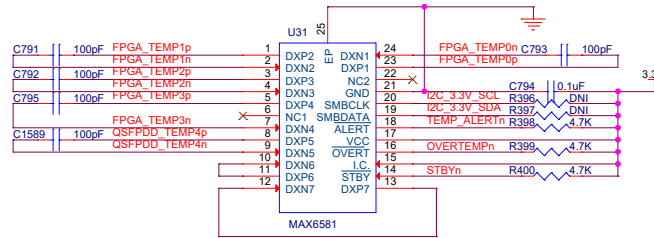


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Title Agilex™ F-Series Transceiver-Soc Development Kit			
Size B	Document Number 150-0321502-B	Rev B	
Date:	Friday, November 25, 2022	Sheet	48 of 82

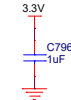
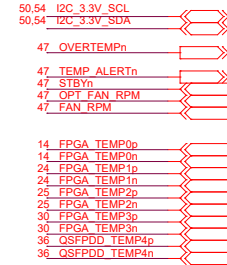
Temperature Sense/FAN

Note: TEMPDIODE instructions
 - route as diff pair and less vias
 - use GND guard traces
 - trace width = 10mils
 - trace gap = as minimum as possible
 - trace length < 6inches

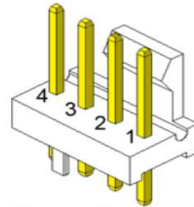
SLAVE ADDR = 1001 101



0: SDM
 1: E-tile
 2: P-tile
 3: Core
 4: QSFPPD1x1

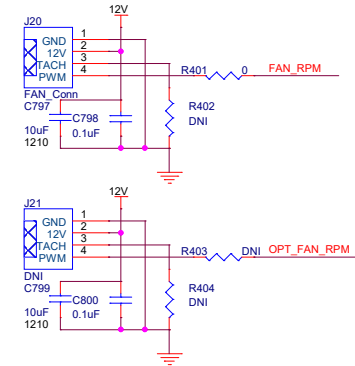
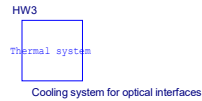
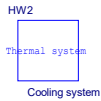


4-Wire Pulse Width Modulation (PWM) Controlled Fans

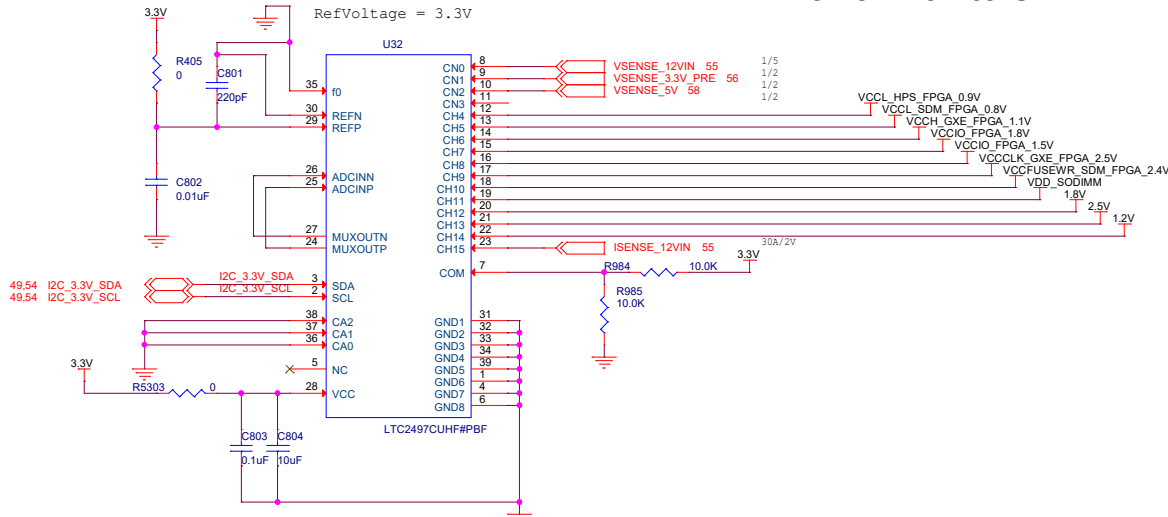


Motherboard CPU Fan 4 Pin header Connector.

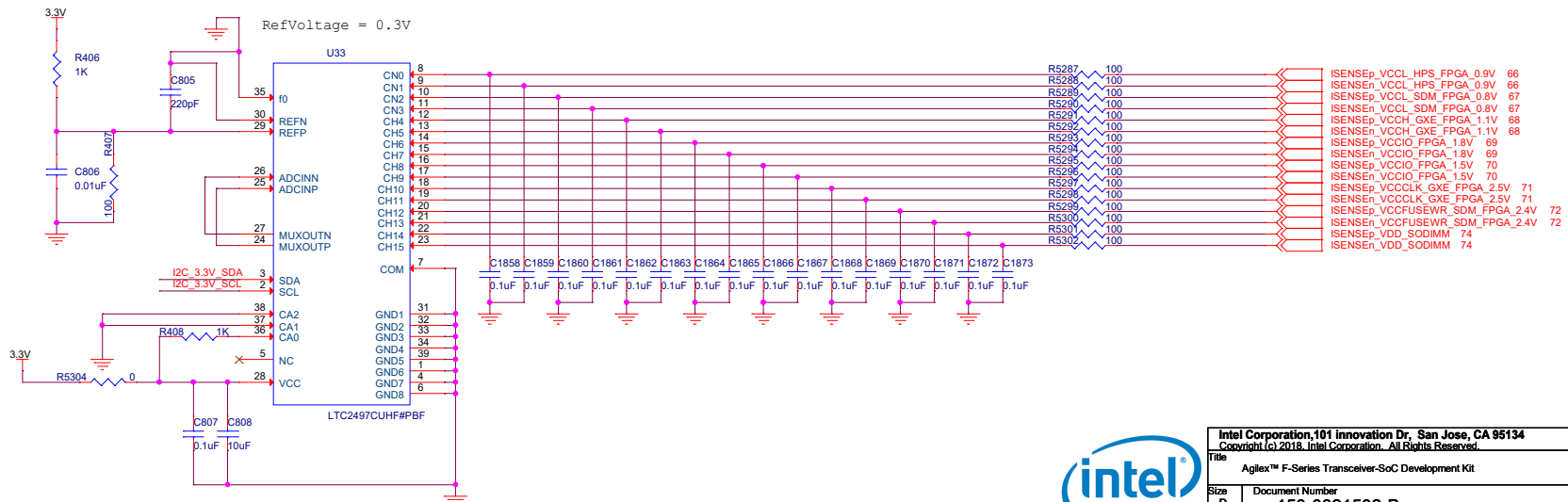
Pin	Name	Color
1	GND	black
2	+12VDC	yellow
3	Sense	green
4	Control	blue



Power Monitors



I2C Address = b'0010100'

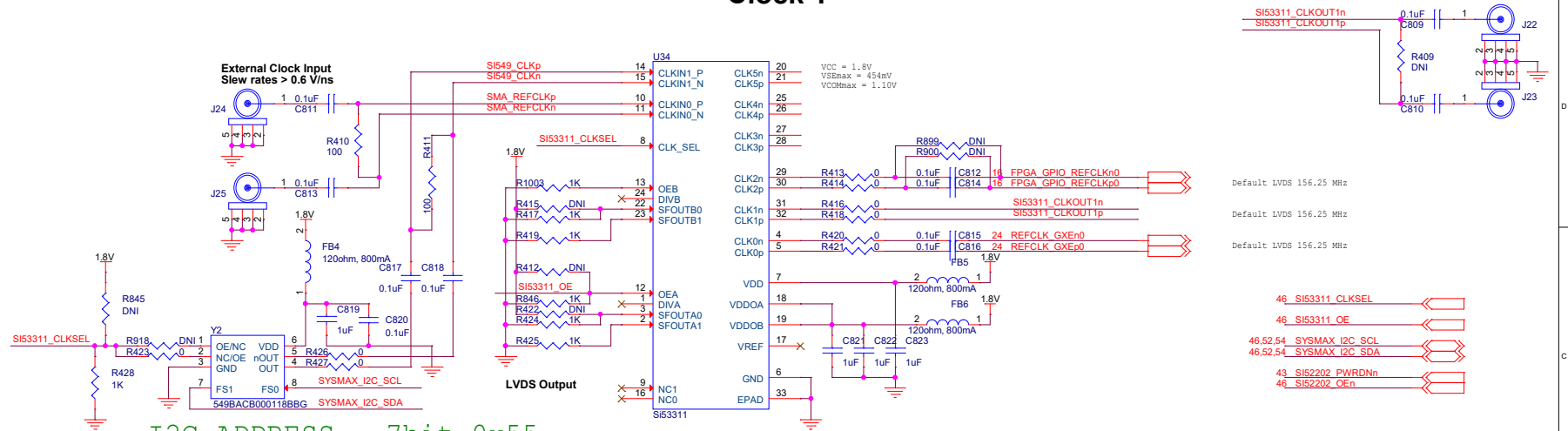


I2C Address = b'0010110'



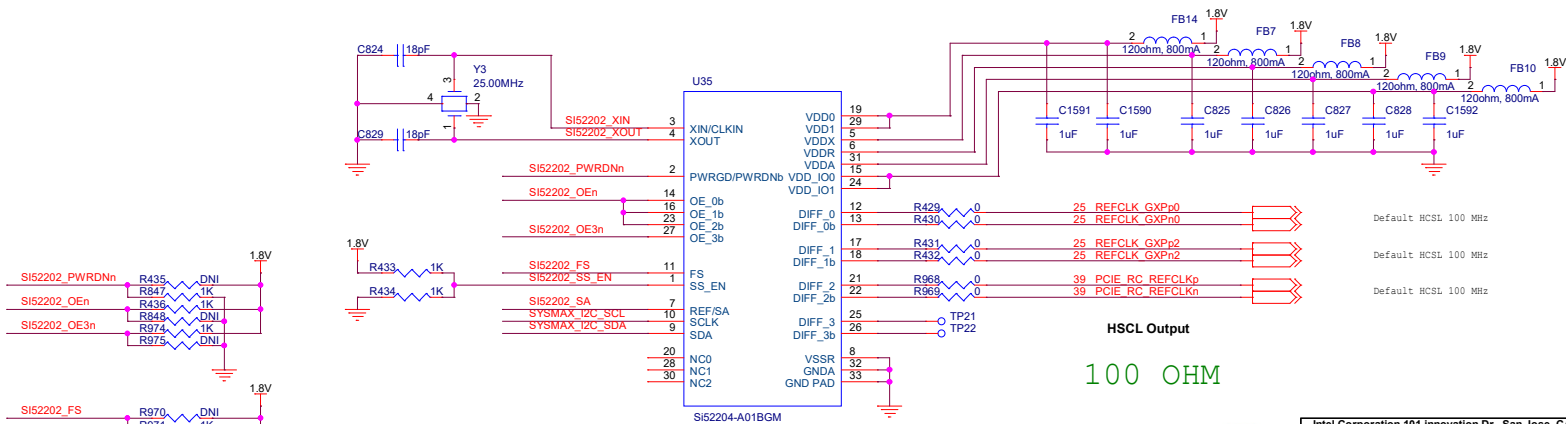
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Title: Agilix™ F-Series Transceiver-SoC Development Kit			
Size: B	Document Number: 150-0321502-B	Rev: B	
Date: Friday, November 25, 2022	Sheet: 50	of 82	

Clock 1



I2C ADDRESS = 7bit 0x55

Clock freq range 0.2M-800M
Default 156.25MHz
LVDS



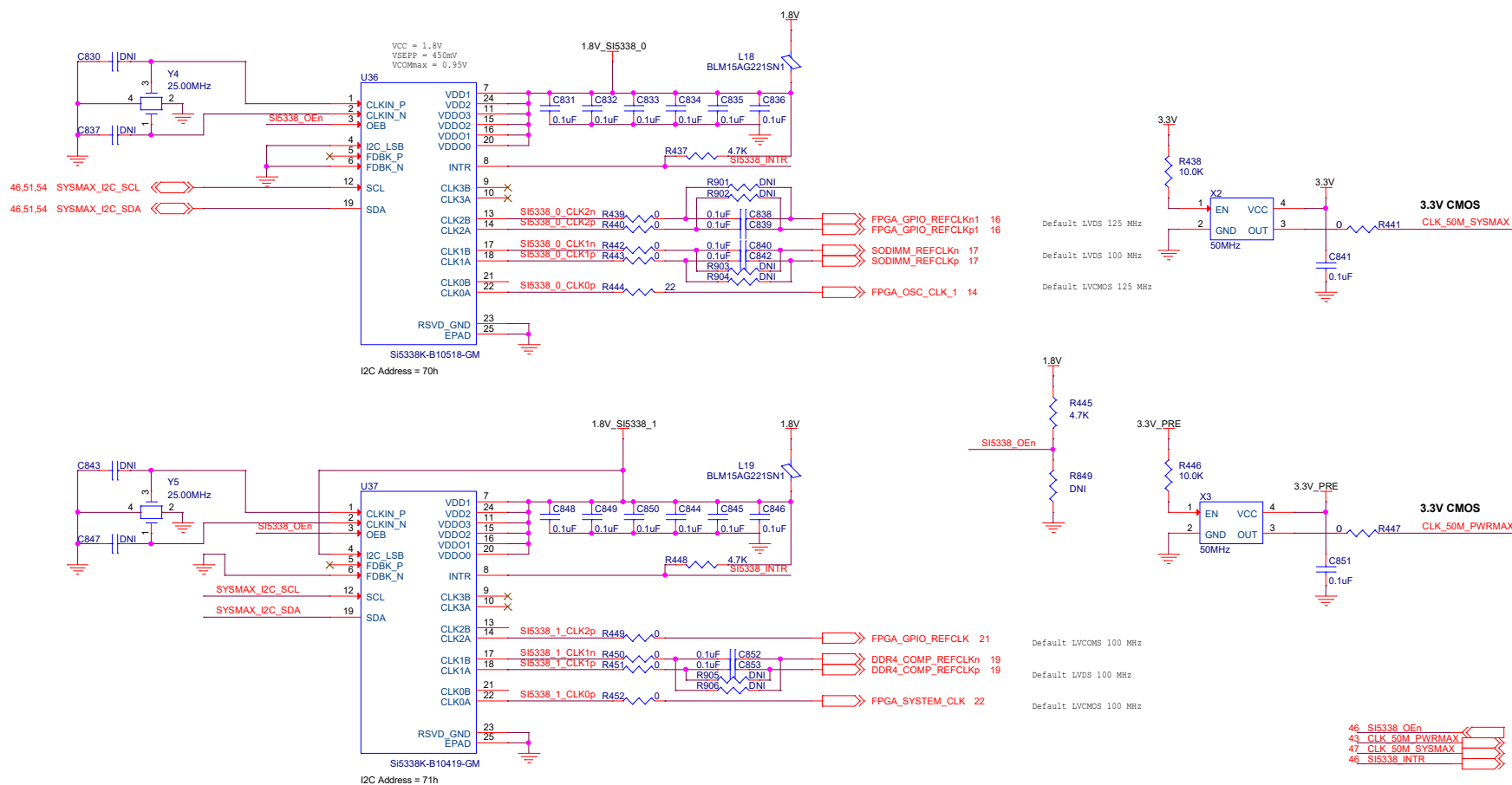
100 OHM

I2C ADDRESS = 7 BIT 6A



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Size B	Document Number 150-0321502-B	Rev B	
Date: Friday, November 25, 2022	Sheet 51	of 82	

Clock 2



LVC MOS18

$V_{OHmin} = 1.50V * 2/3 = 1.00V$

$V_{OLmax} = 0.30V * 2/3 = 0.20V$

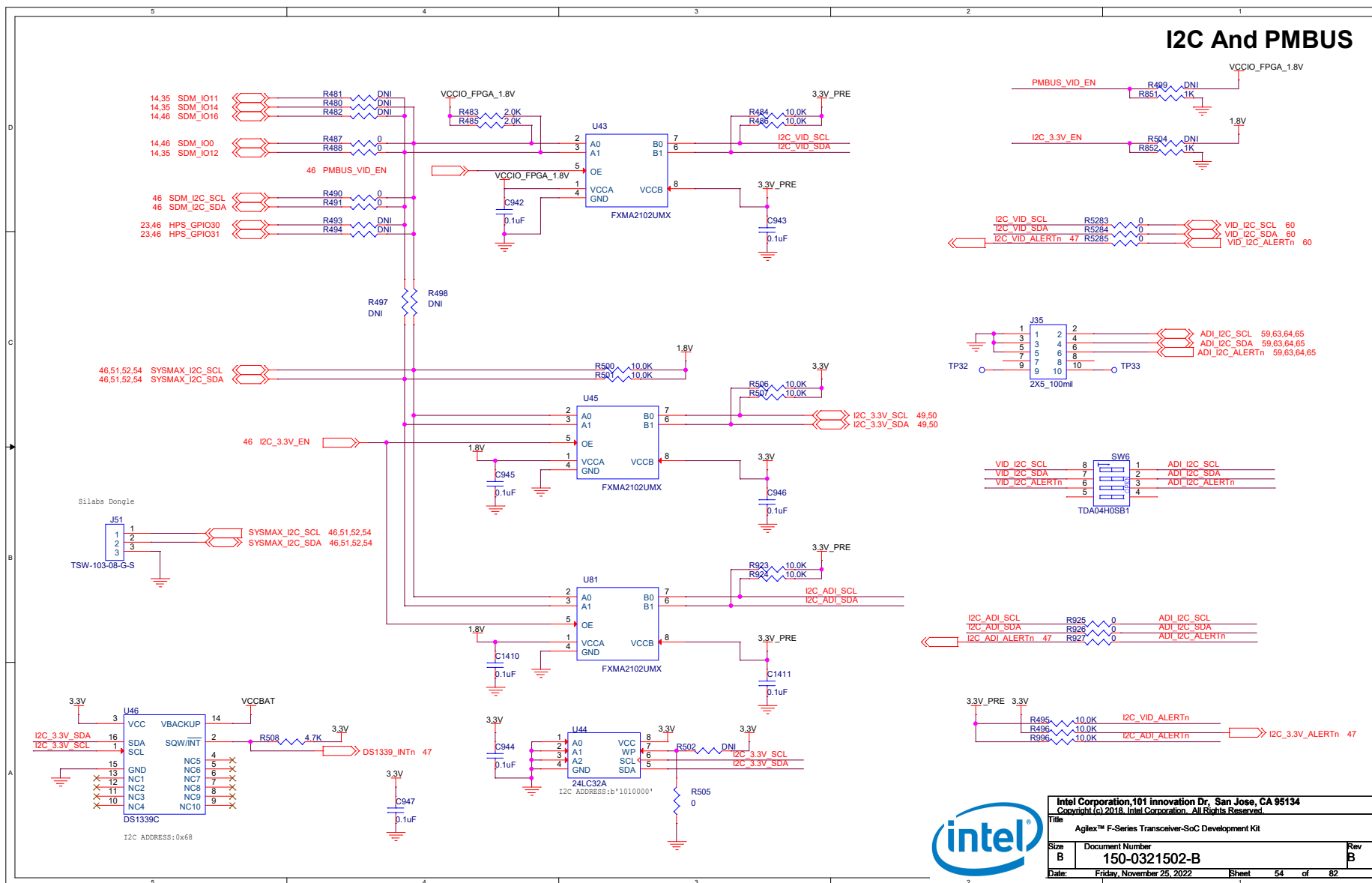


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Title	Agilix™ F-Series Transceiver-SoC Development Kit			
Size B	Document Number 150-0321502-B			Rev B
Date:	Friday, November 25, 2022	Sheet	52	of 82

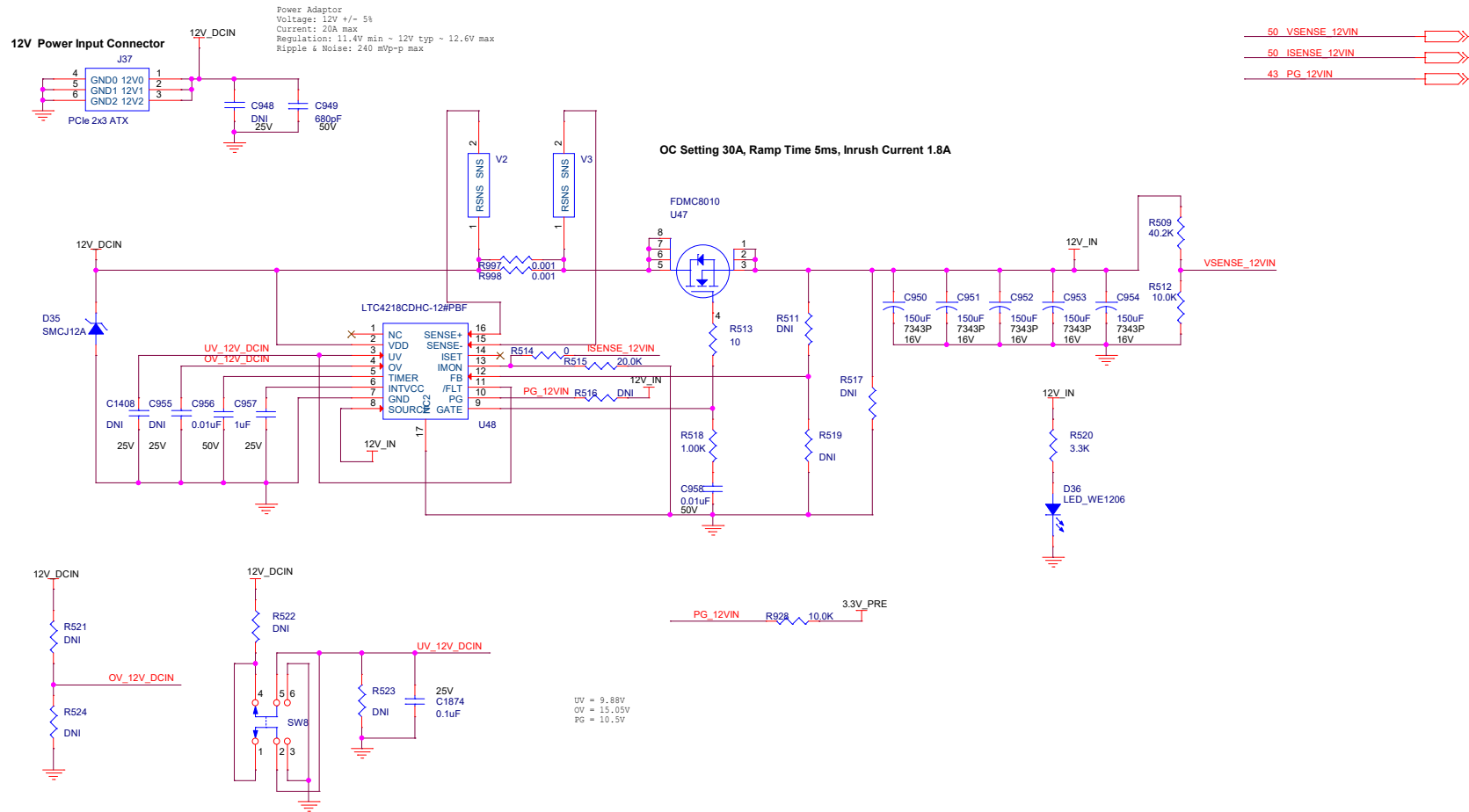
Pin	Signal
1	Cleaner_INSEL01
2	Cleaner_GPIO3
3	Cleaner_GPIO6
4	Cleaner_GPIO4
5	Cleaner_INSEL00
6	Cleaner_GPIO0
7	Cleaner_GPIO1
8	DMR0502E_PUS
9	Cleaner_WF_CTRL
10	Cleaner_STATUS1
11	Cleaner_INSEL10
12	Cleaner_GPIO5
13	Cleaner_INSEL11
14	Cleaner_GPIO2
15	Cleaner_SCL
16	Cleaner_GPIO7
17	Cleaner_GPIO8
18	Cleaner_GPIO9
19	Cleaner_GPIO4
20	Cleaner_GPIO3



I2C And PMBUS

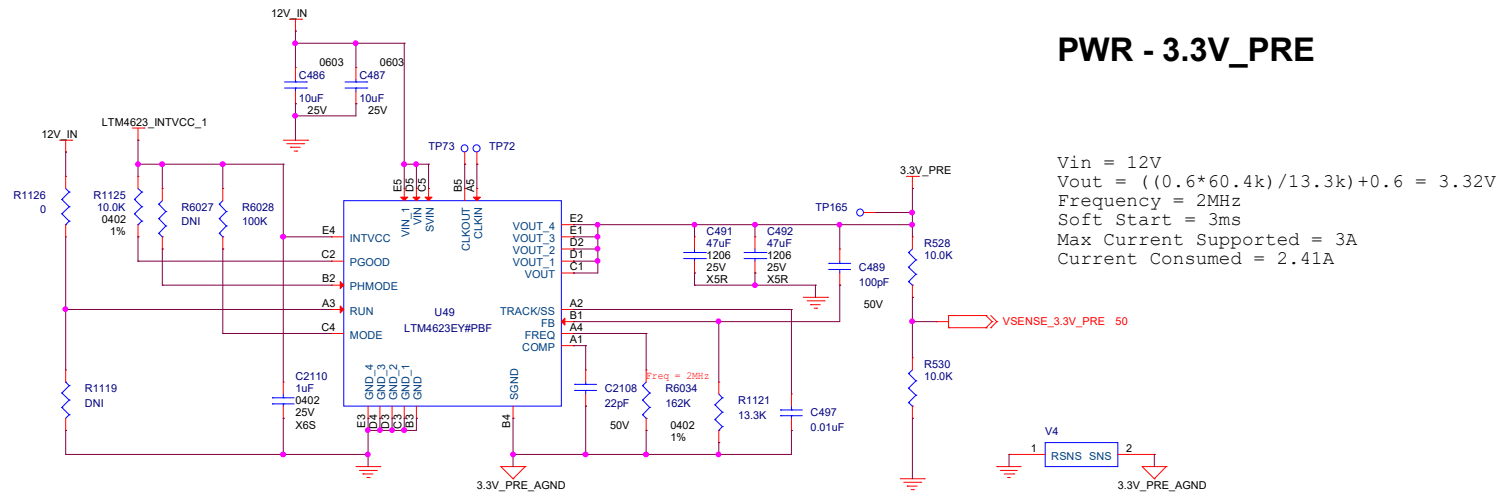


PWR - POWER INPUT



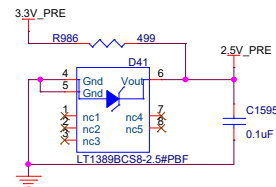
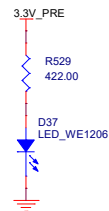
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Size	Document Number	Rev	
B	150-0321502-B	B	
Date:	Friday, November 25, 2022	Sheet	55 of 82

PWR - 3.3V_PRE



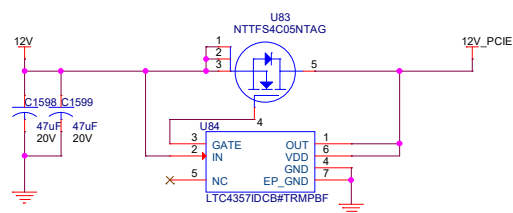
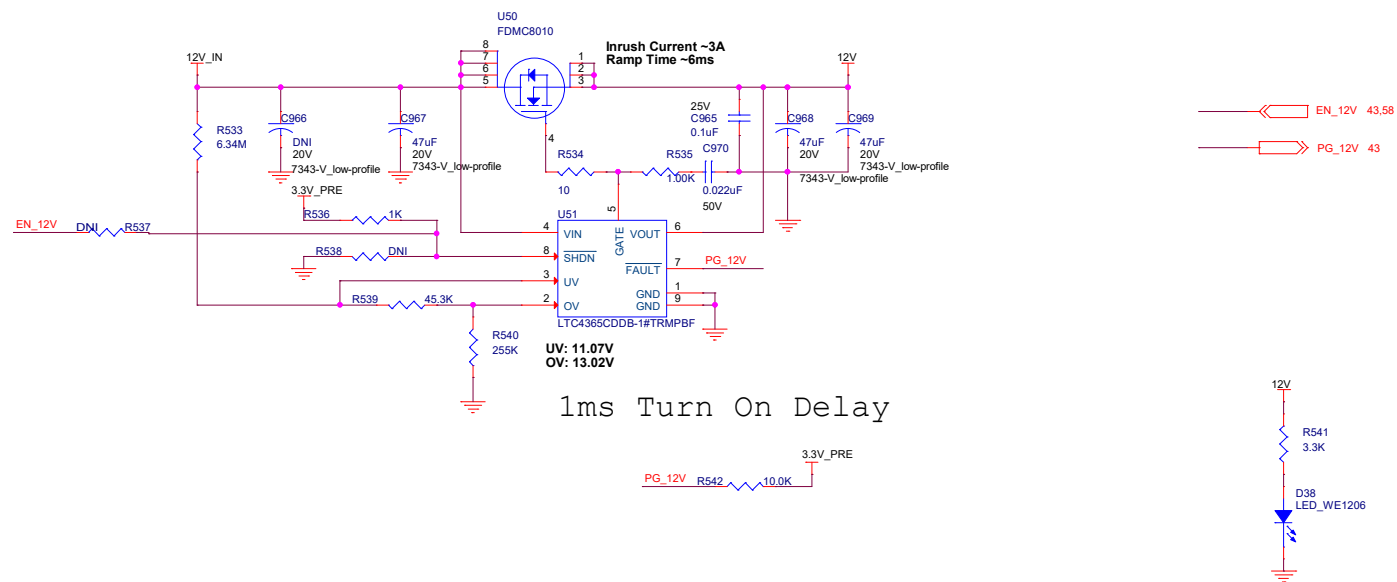
MPN: LTM4623EY#PBF
 IPN: K15502-001

GND of input/output filter and PGND shall be connected to GND layer directly, while all signal GND and AGND shall be connected together and then go to a single via away from the PGND area



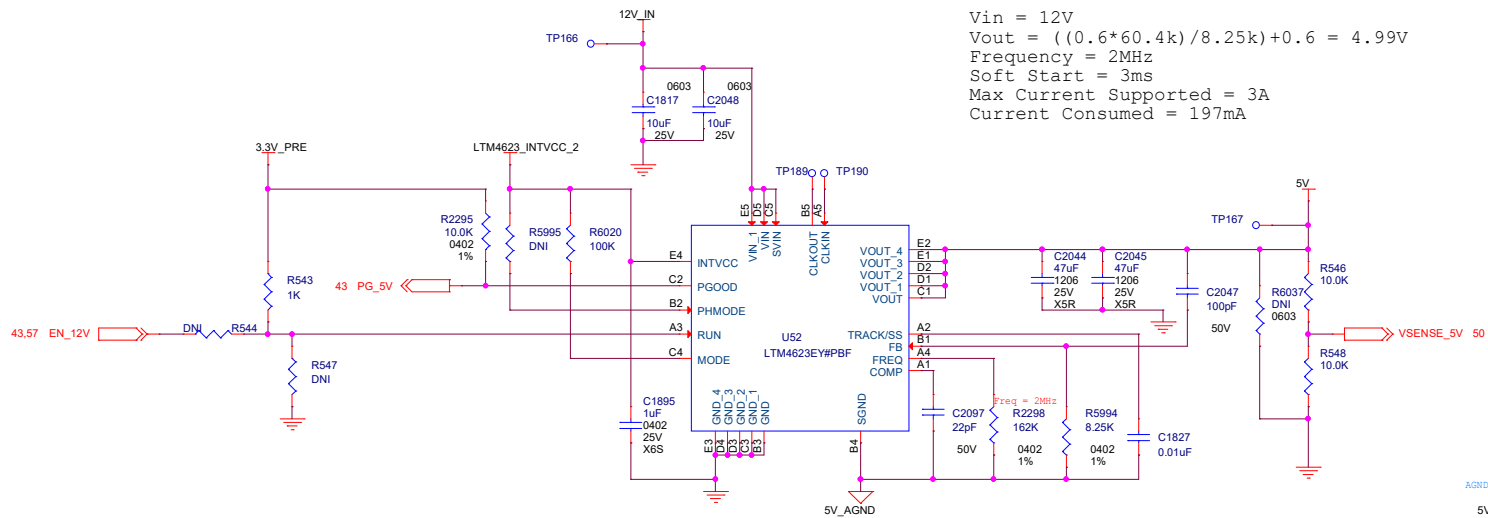
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Size: B	Document Number: 150-0321502-B	Rev: B	
Date: Friday, November 25, 2022	Sheet: 56	of: 82	

PWR - 12V



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Title	Agilex™ F-Series Transceiver-SoC Development Kit			
Size B	Document Number 150-0321502-B			Rev B
Date:	Friday, November 25, 2022	Sheet	57	of 82

PWR - BIAS



GND of input/output filter and PGND shall be connected to GND layer directly, while all signal GND and AGND shall be connected together and then go to a single via away from the PGND area

MPN: LTM4623EY#PBF
IPN: K15502-001

Diagram showing the connection of the ST18 output to the AGND and PGND pins. The ST18 output is connected to the AGND pin (pin 1) and the PGND pin (pin 2). The AGND pin is connected to the 5V_AGND pin. The PGND pin is connected to the PGND pin. The connection is labeled 'SHORT'.



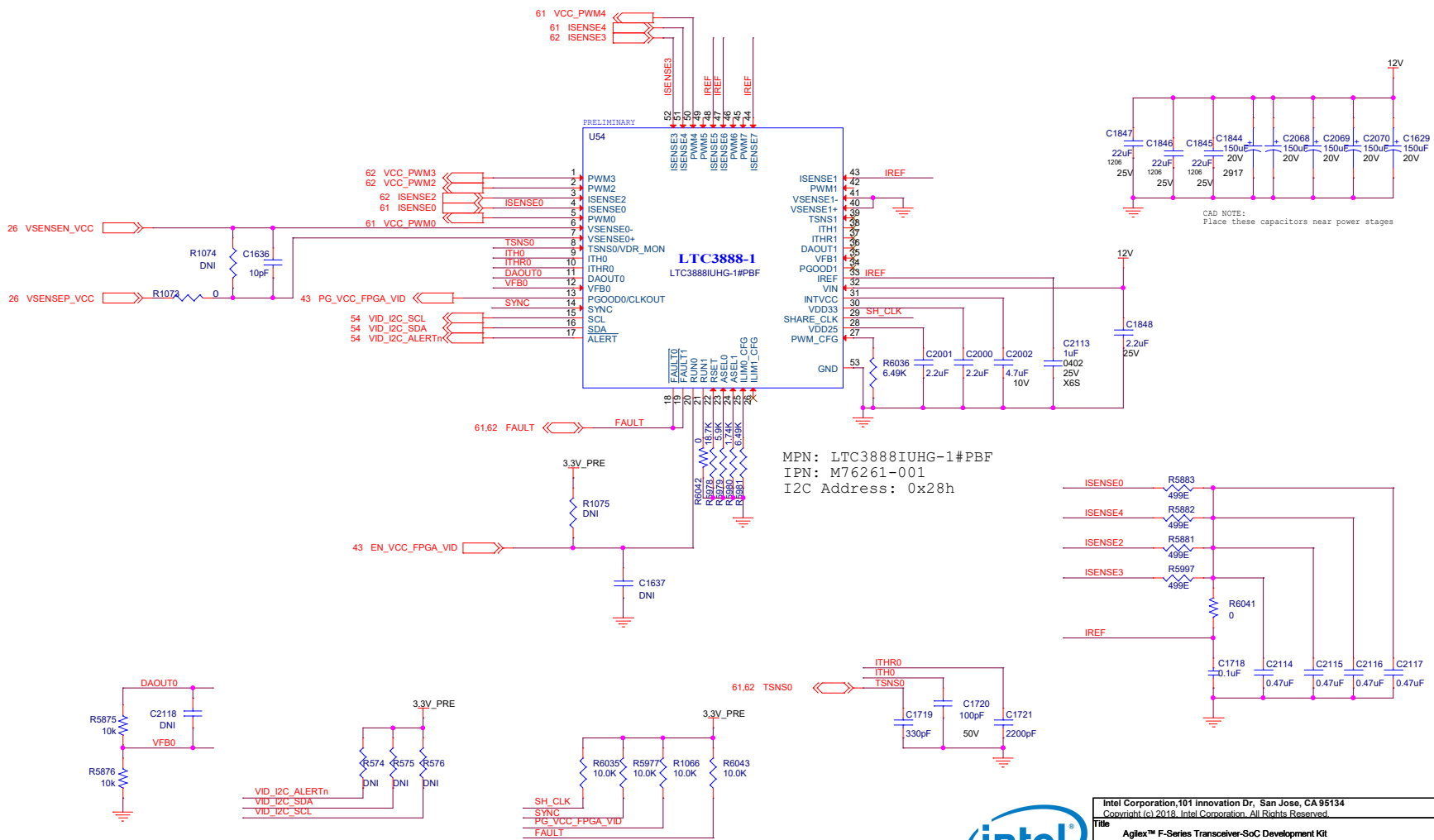
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Size B	Document Number 150-0321502-B
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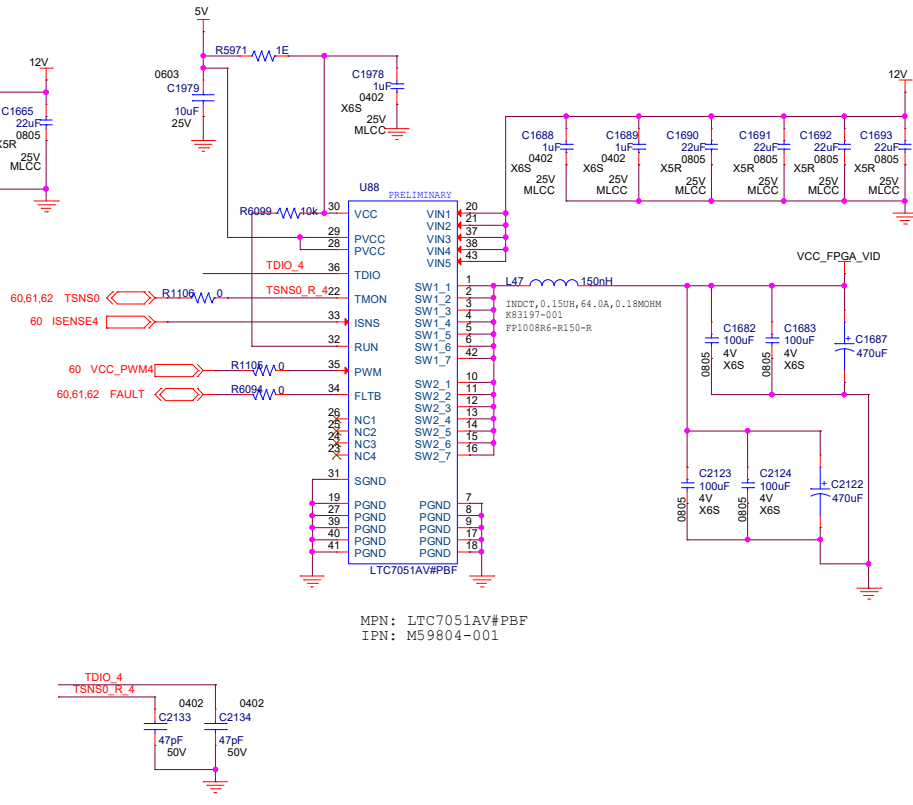
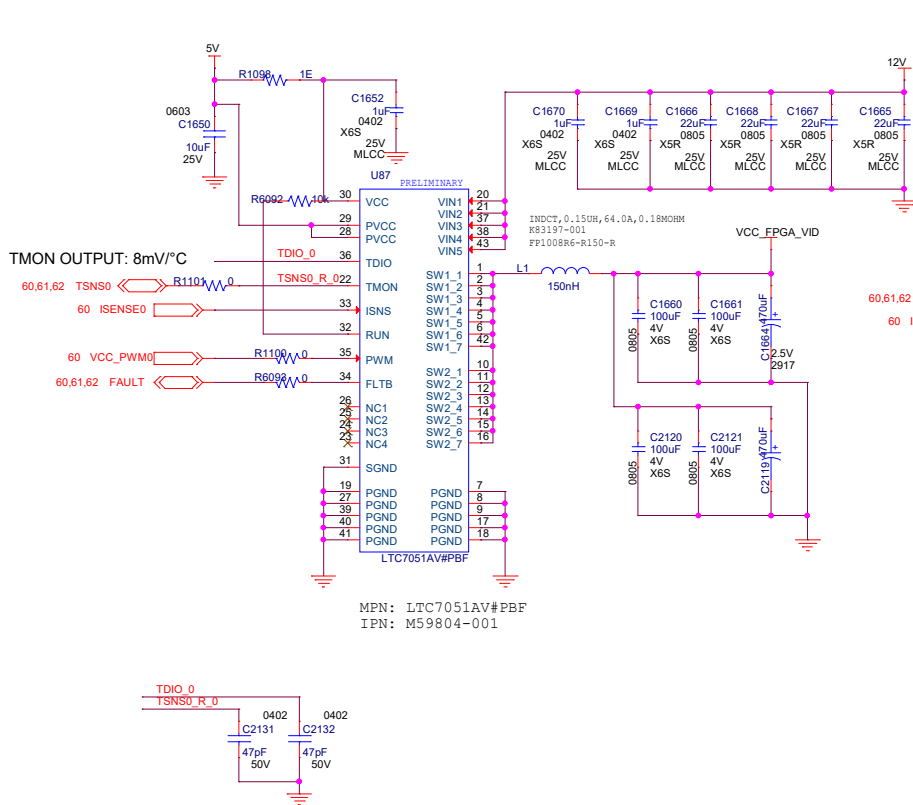
Date: Friday, November 25, 2022 Sheet 58 of 82

PWR - FPGA VCC VID 1



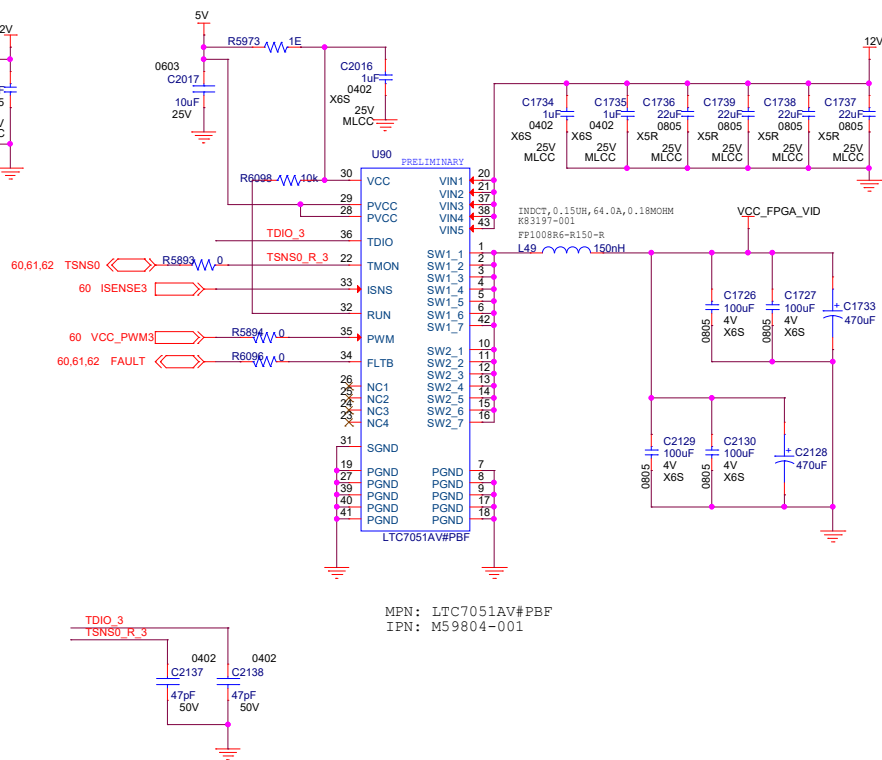
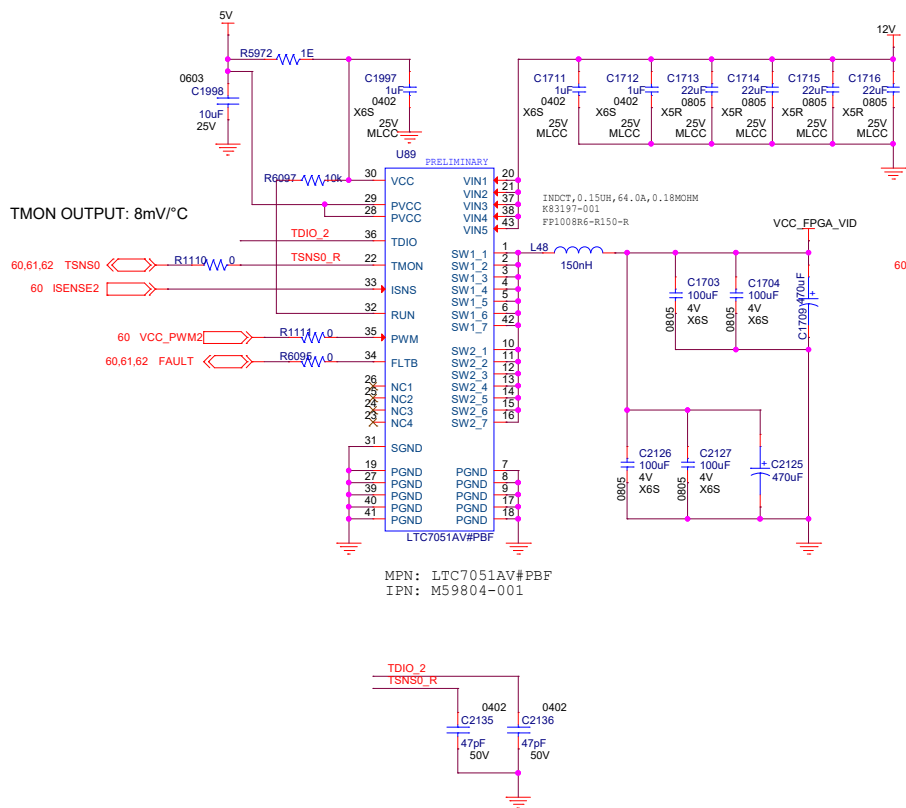
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Size B	Document Number 150-0321502-B	Rev B	
Date:	Friday, November 25, 2022	Sheet	60 of 82

PWR - FPGA VCC VID 2

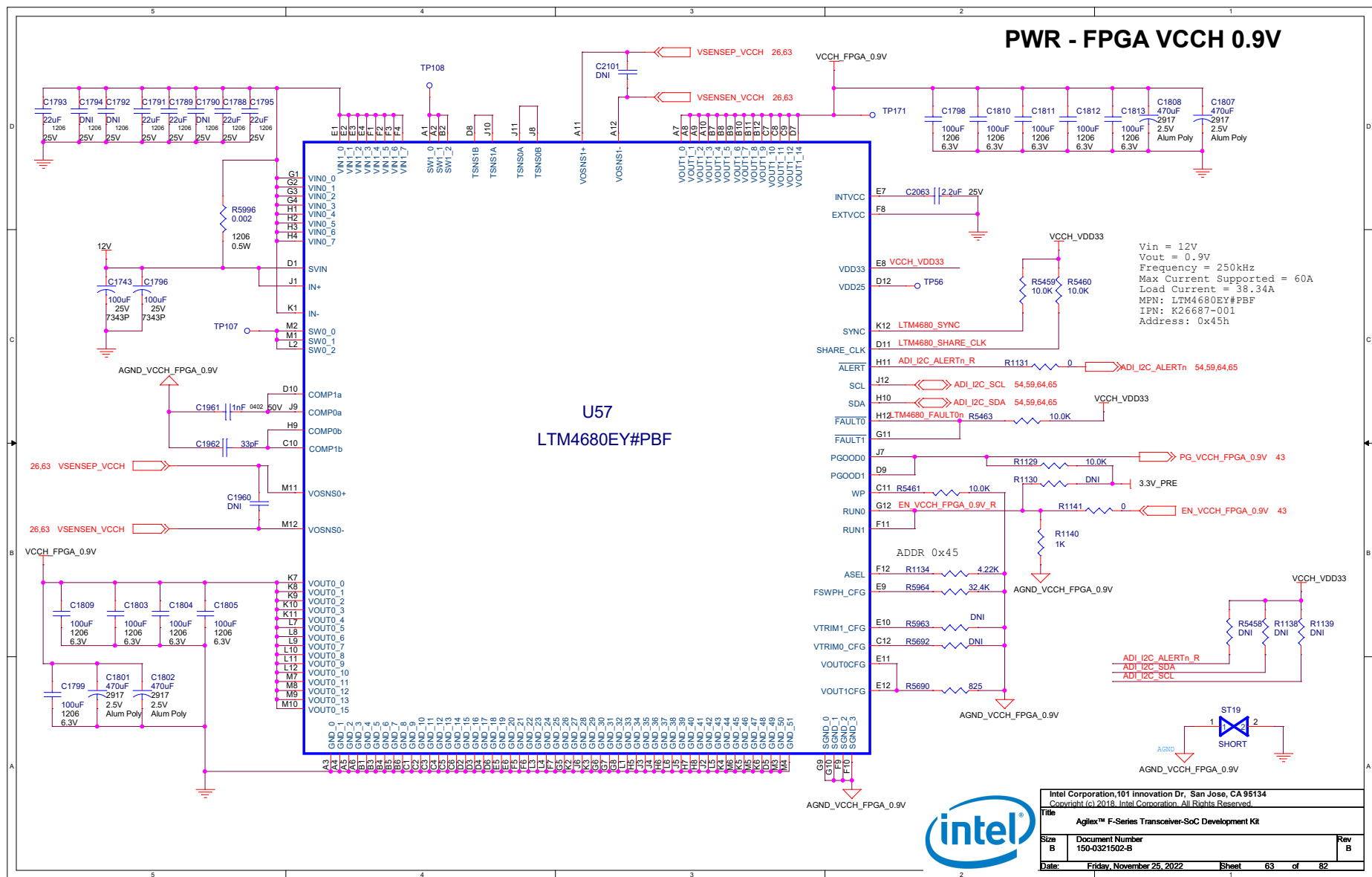


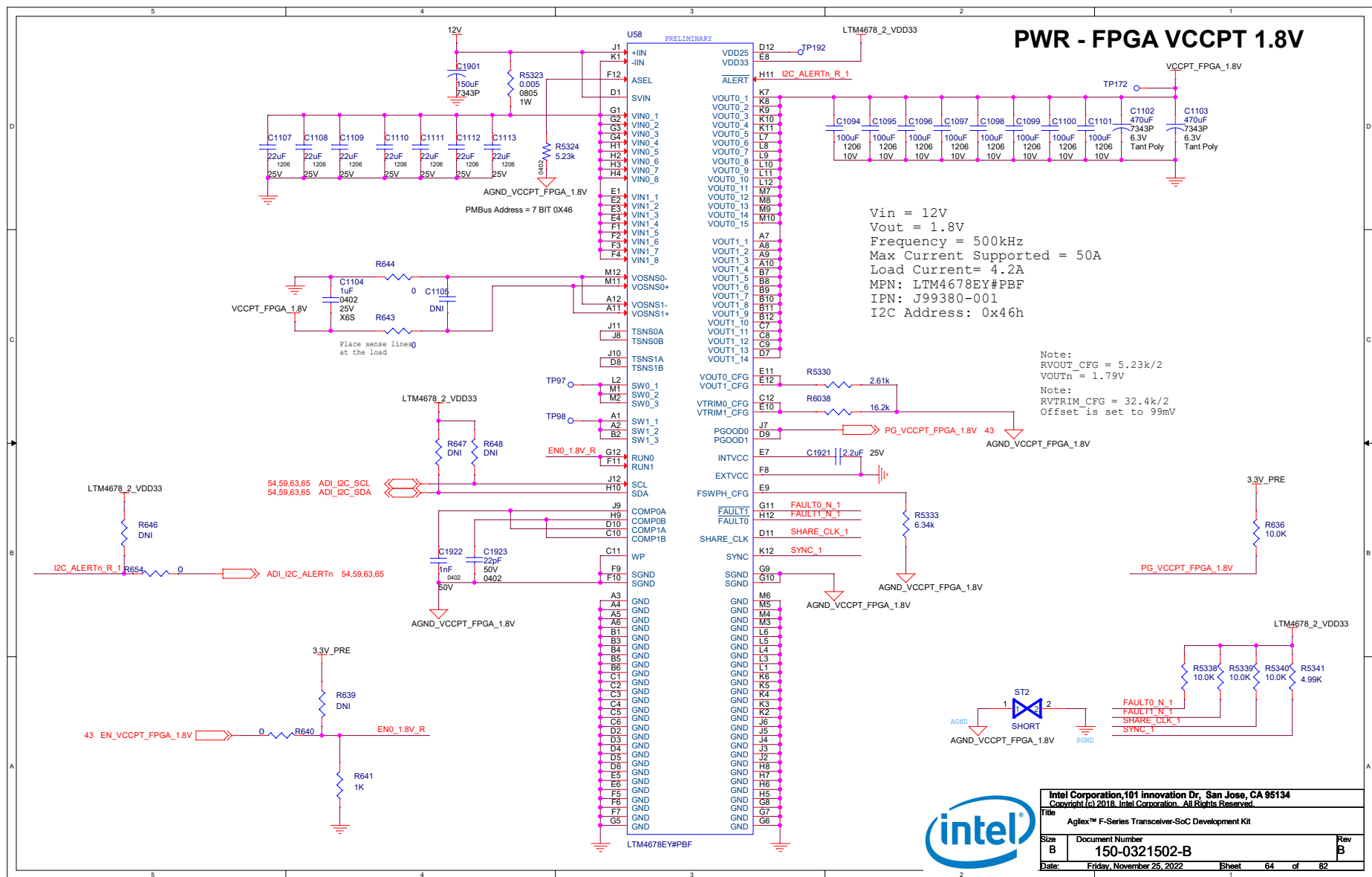
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Size B	Document Number 150-0321502-B		Rev B
Date:	Friday, November 25, 2022	Sheet 61 of 82	

PWR - FPGA VCC VID 3



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Title Agilex™ F-Series Transceiver-SoC Development Kit			
Size B	Document Number 150-0321502-B	Rev B	
Date:	Friday, November 25, 2022	Sheet	62 of 82

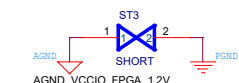




PWR - FPGA VCCIO 1.2V

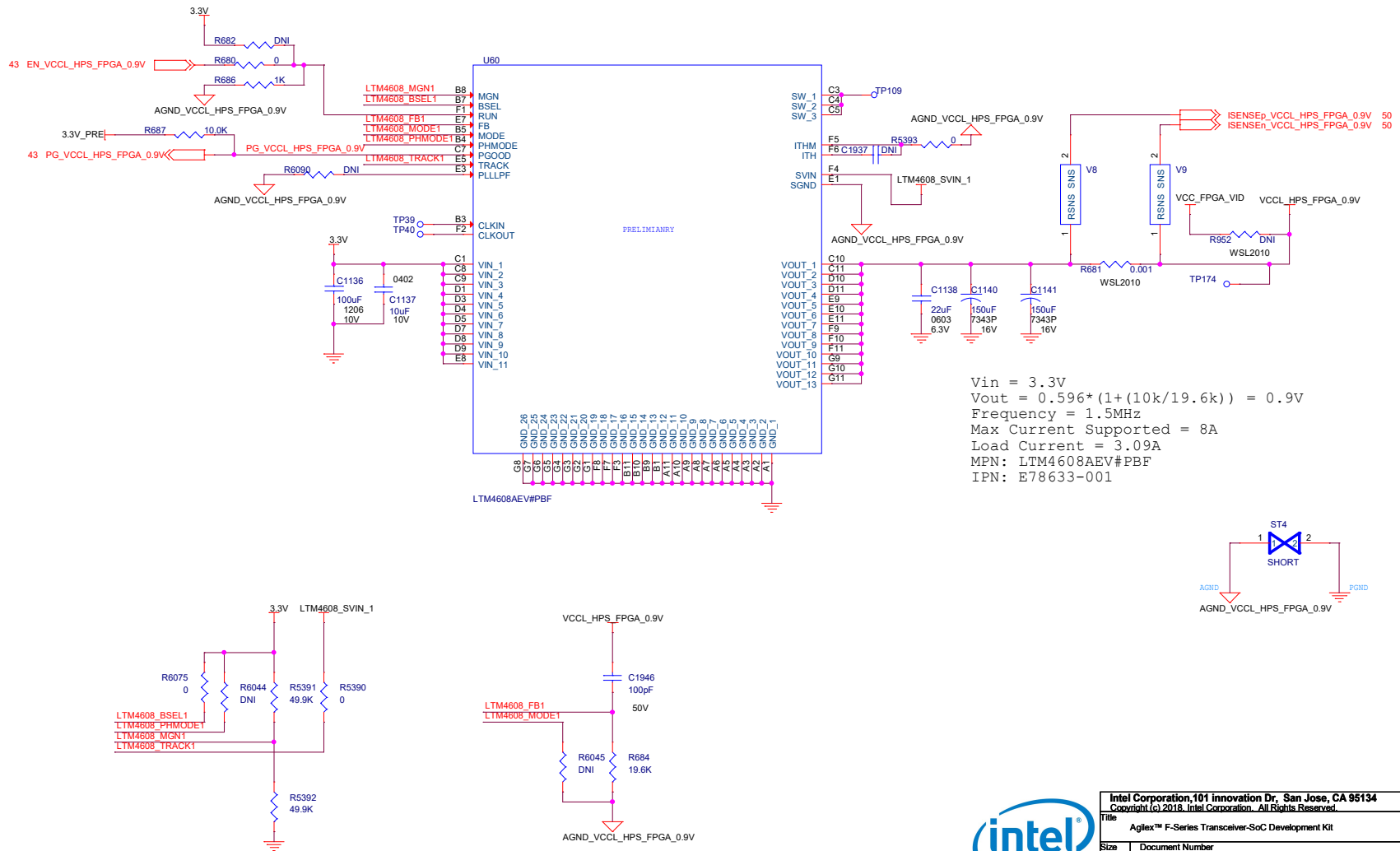
U59
LTM4677EY#PBF

Vin = 12V
Vout = 1.2V
Frequency = 350kHz
Max Current Supported = 36A
Load Current = 21A
MPN: LTM4677EY#PBF
IPN: K15467-001
I2C Address: 0x47h

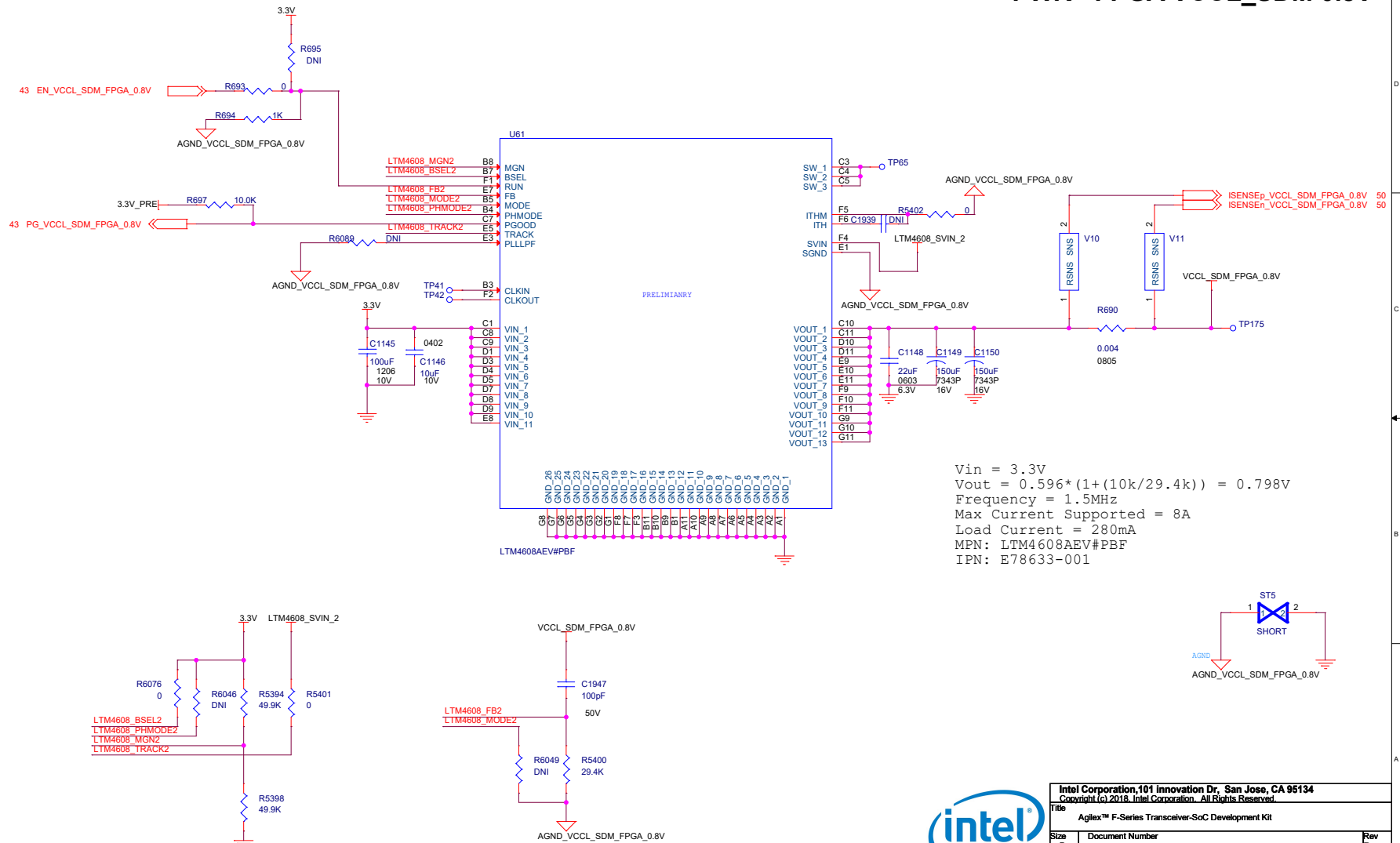


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Agilex™ F-Series Transceiver-SoC Development Kit		
Size B	Document Number 150-0321502-B	Rev B
Date:	Friday, November 25, 2022	Sheet 65 of 82

PWR - FPGA VCCL_HPS 0.9V

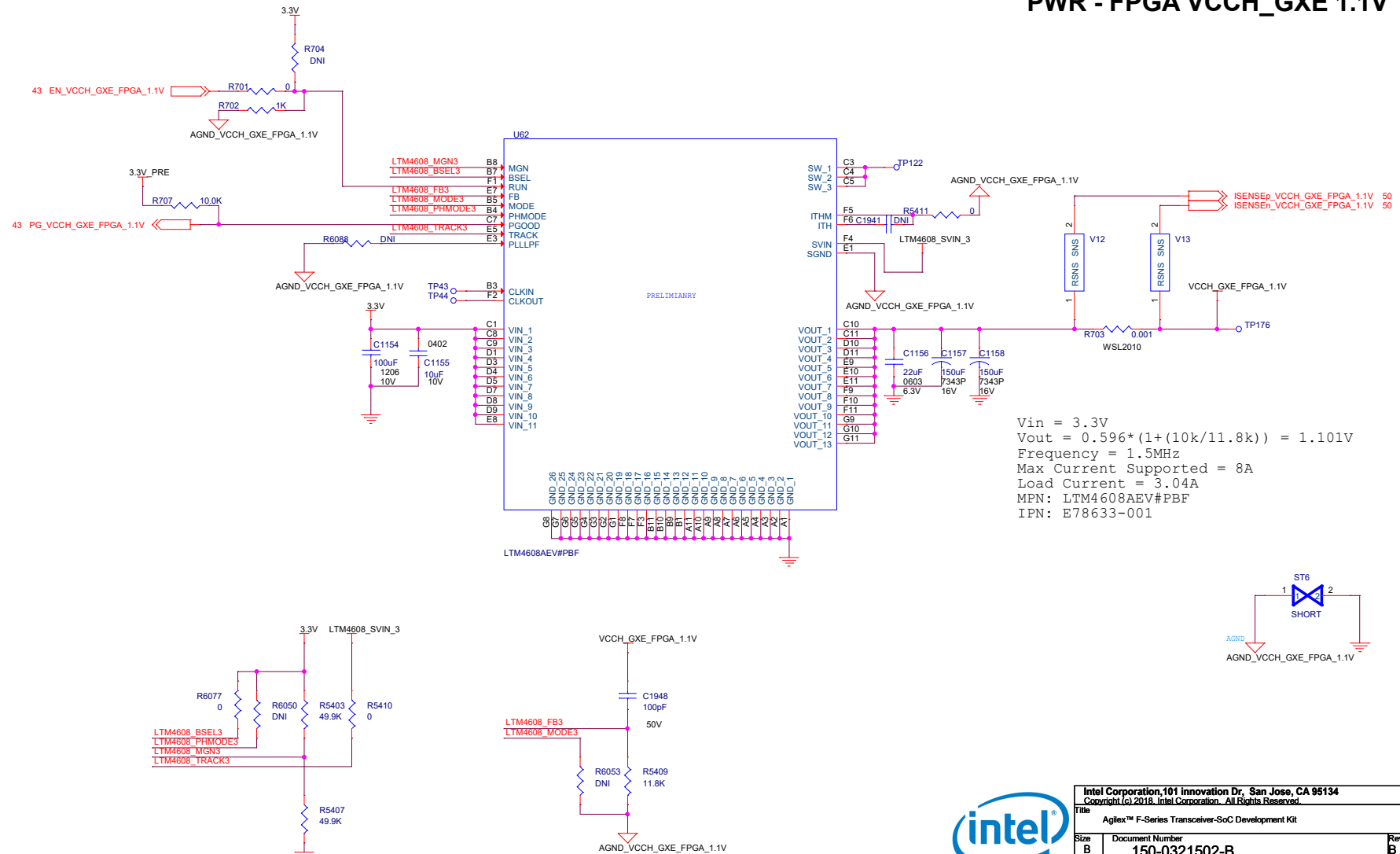


PWR - FPGA VCCL_SDM 0.8V

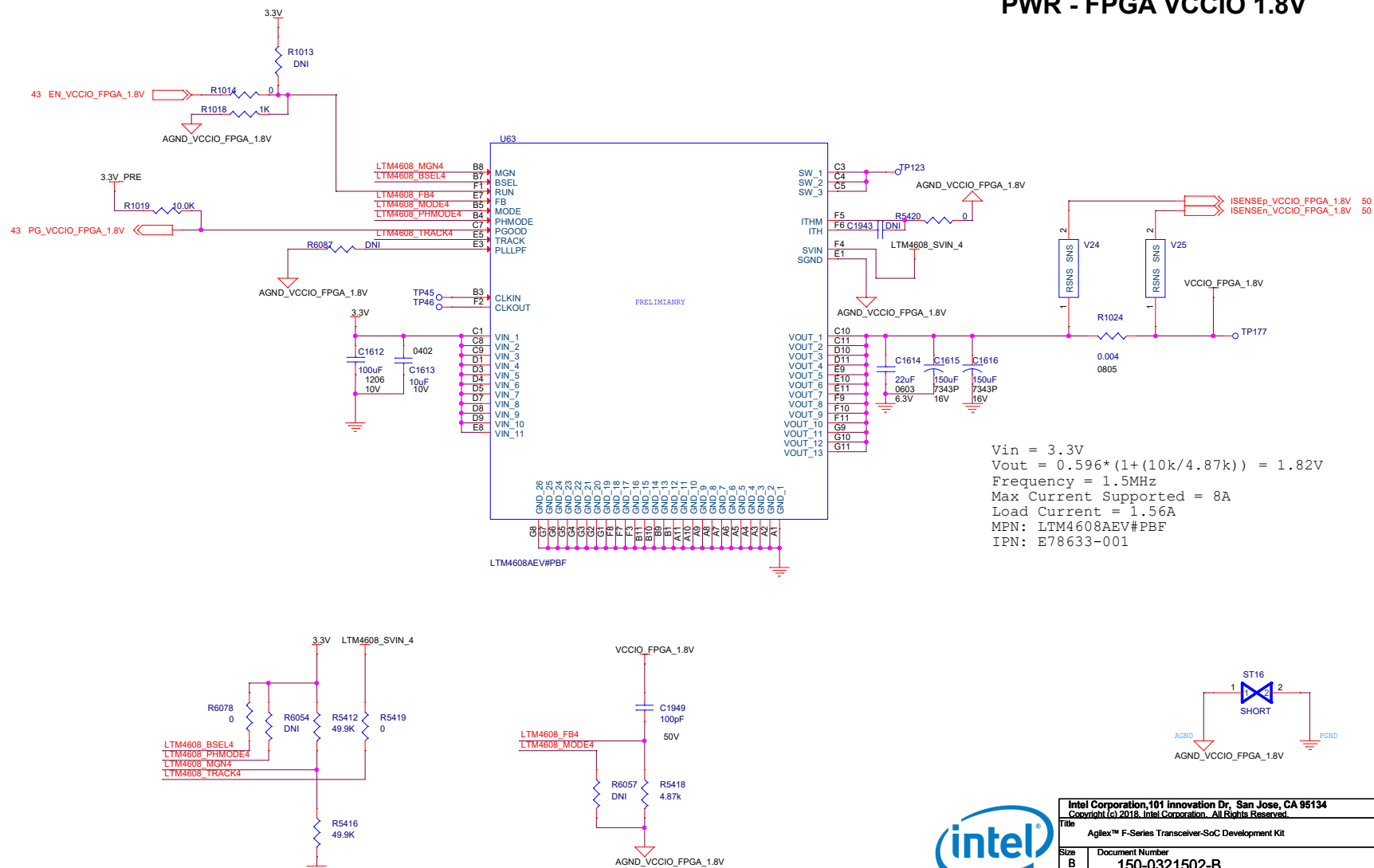


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Title Agilix™ F-Series Transceiver-SoC Development Kit			
Size B		Document Number 150-0321502-B	
Date Friday November 25, 2022		Sheet 67 of 82	
Rev B		Rev B	

PWR - FPGA VCCH_GXE 1.1V

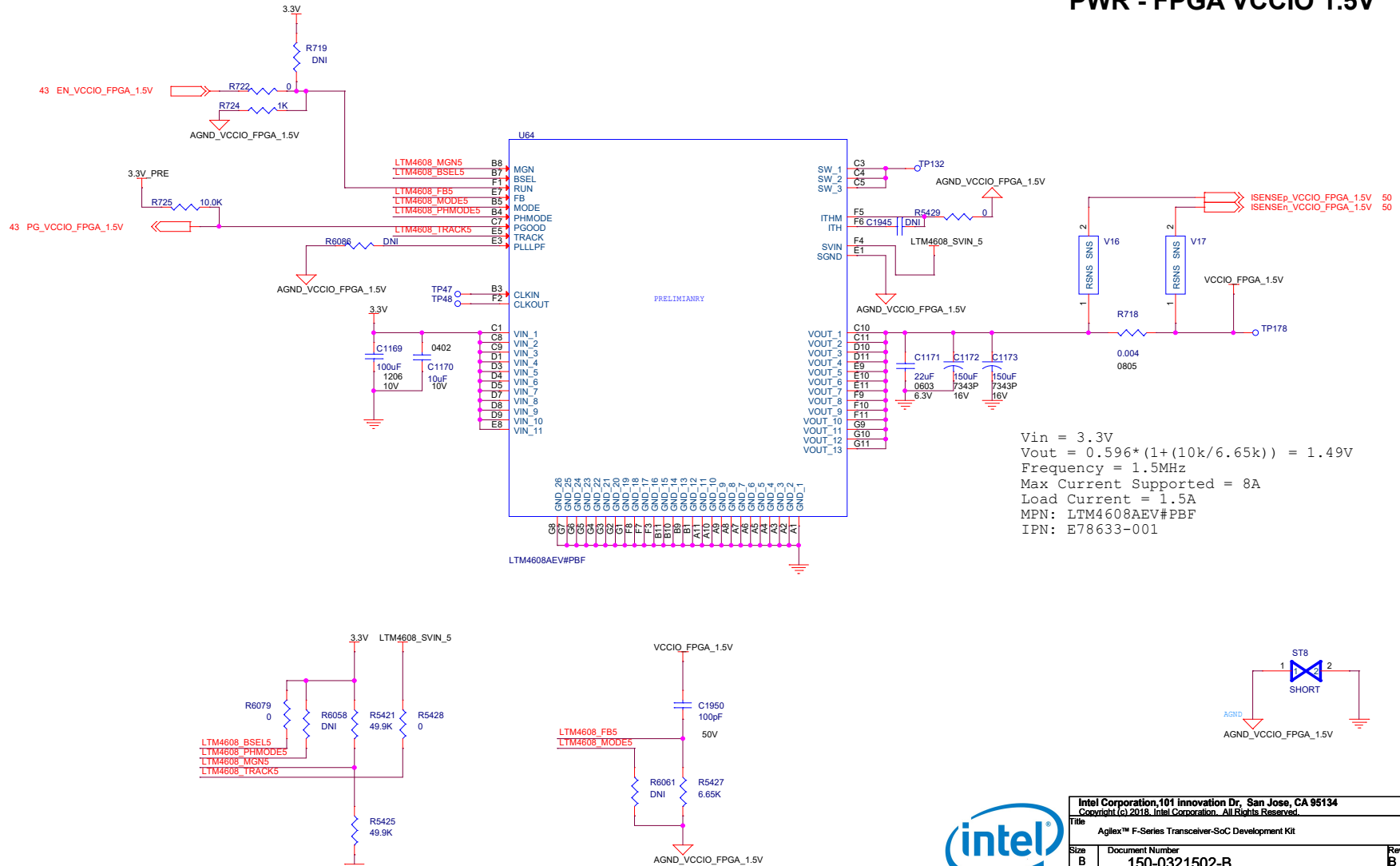


PWR - FPGA VCCIO 1.8V

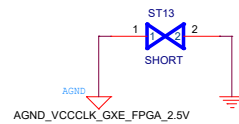
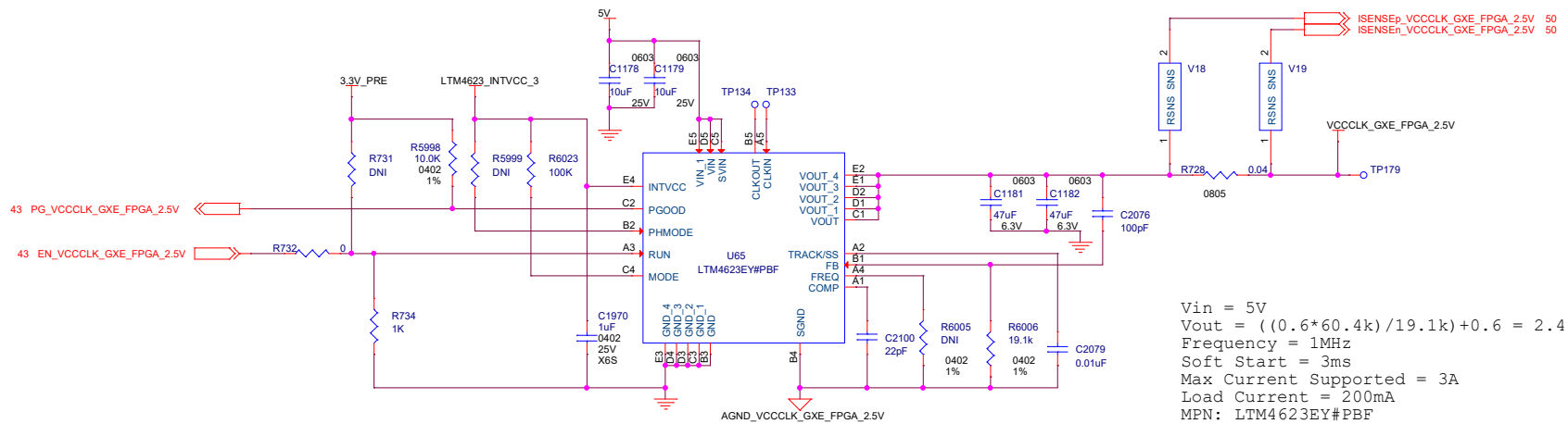


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Title Agile™ F-Series Transceiver-SoC Development Kit			
Size B	Document Number 150-032152-B		Rev B
Date	Friday, November 25, 2022	Sheet	69 of 82

PWR - FPGA VCCIO 1.5V

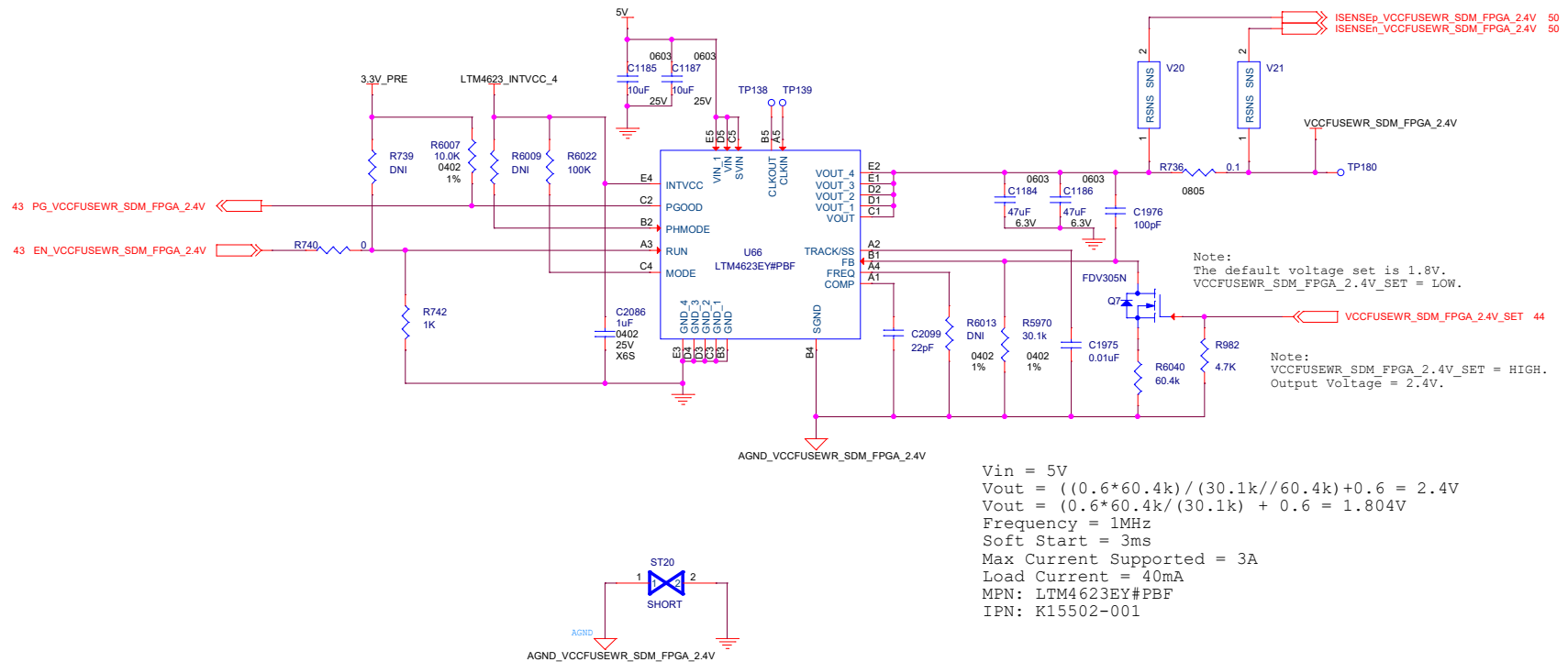


PWR - FPGA VCCCLK_GXE 2.5V



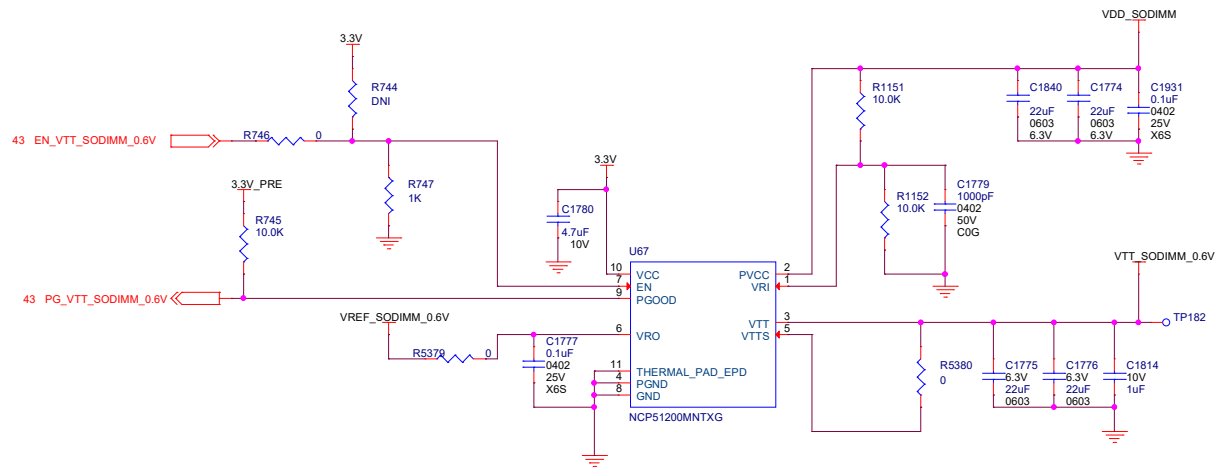
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Title Agilex™ F-Series Transceiver-SoC Development Kit			
Size B	Document Number 150-0321502-B	Rev B	
Date:	Friday, November 25, 2022	Sheet	71 of 82

PWR - FPGA VCCFUSEWR_SDM 2.4V



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Agilex™ F-Series Transceiver-SoC Development Kit			
Size	Document Number	Rev	
B	150-0321502-B	B	
Date:	Friday, November 25, 2022	Sheet	72 of 82

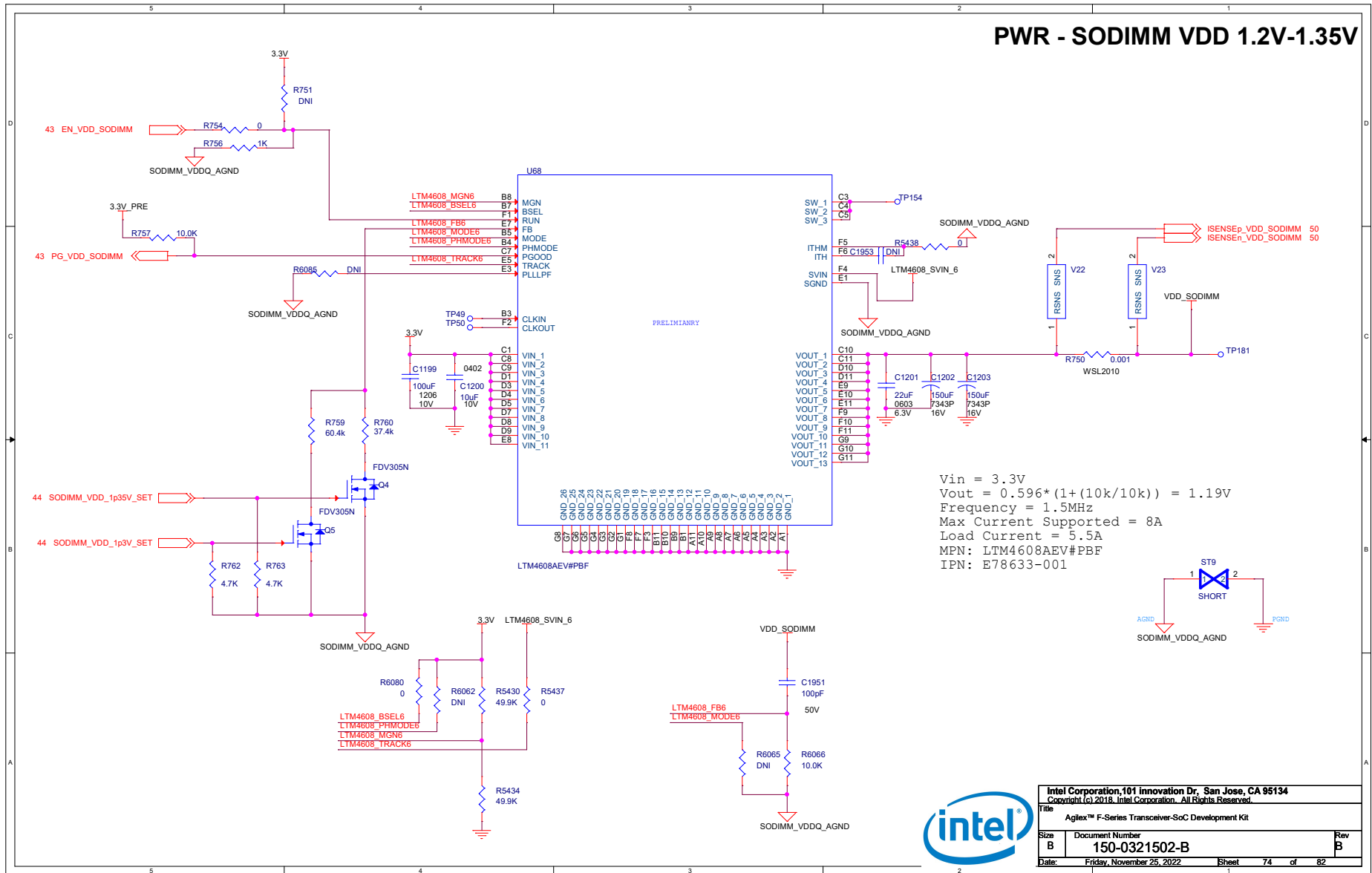
PWR - SODIMM VTT 0.6V



$V_{in} = 1.2V$
 $V_{out} = 0.6V$
 Max Current Supported = 3A
 MPN: NCP51200MNTXG
 IPN: K77668-001

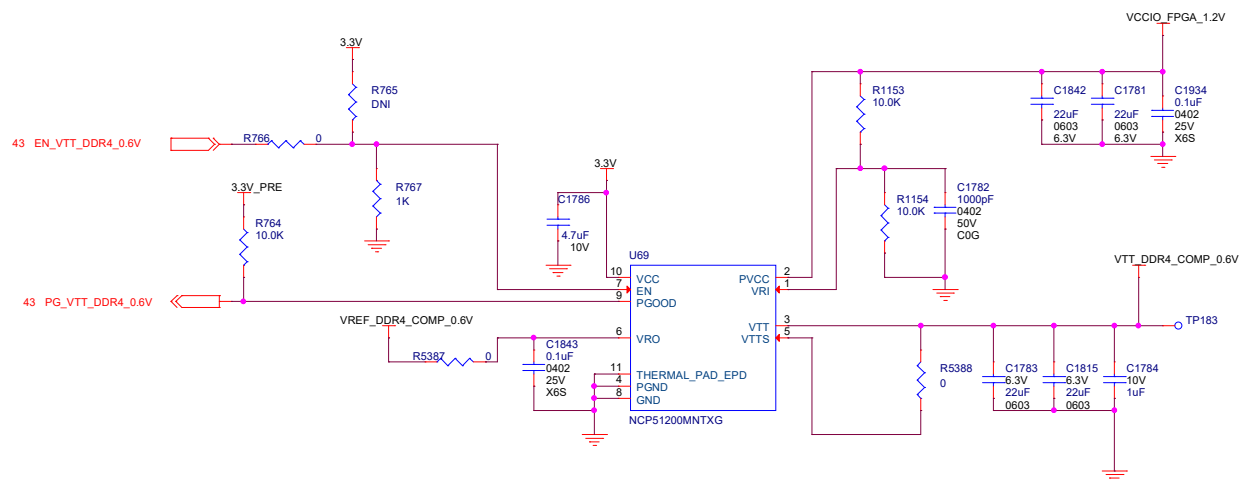
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Agilex™ F-Series Transceiver-SoC Development Kit			
Size	Document Number	Rev	
B	150-0321502-B	B	
Date:	Friday, November 25, 2022	Sheet	73 of 82

PWR - SODIMM VDD 1.2V-1.35V



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Title: Agilent F-Series Transceiver-SoC Development Kit			
Size: B	Document Number: 150-0321502-B	Rev: B	
Date: Friday, November 25, 2022	Sheet: 74	of 82	

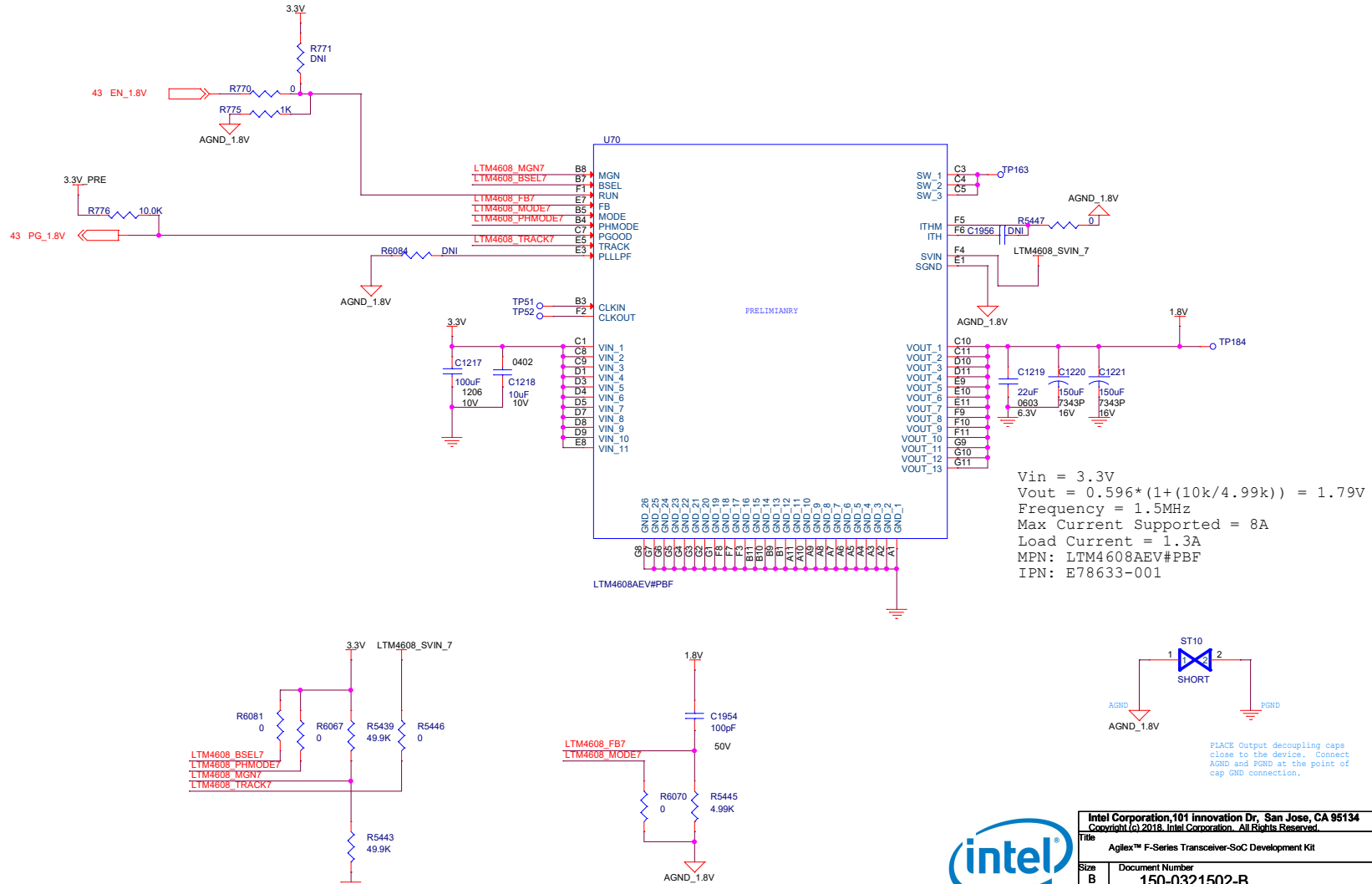
PWR - DDR4 VTT 0.6V



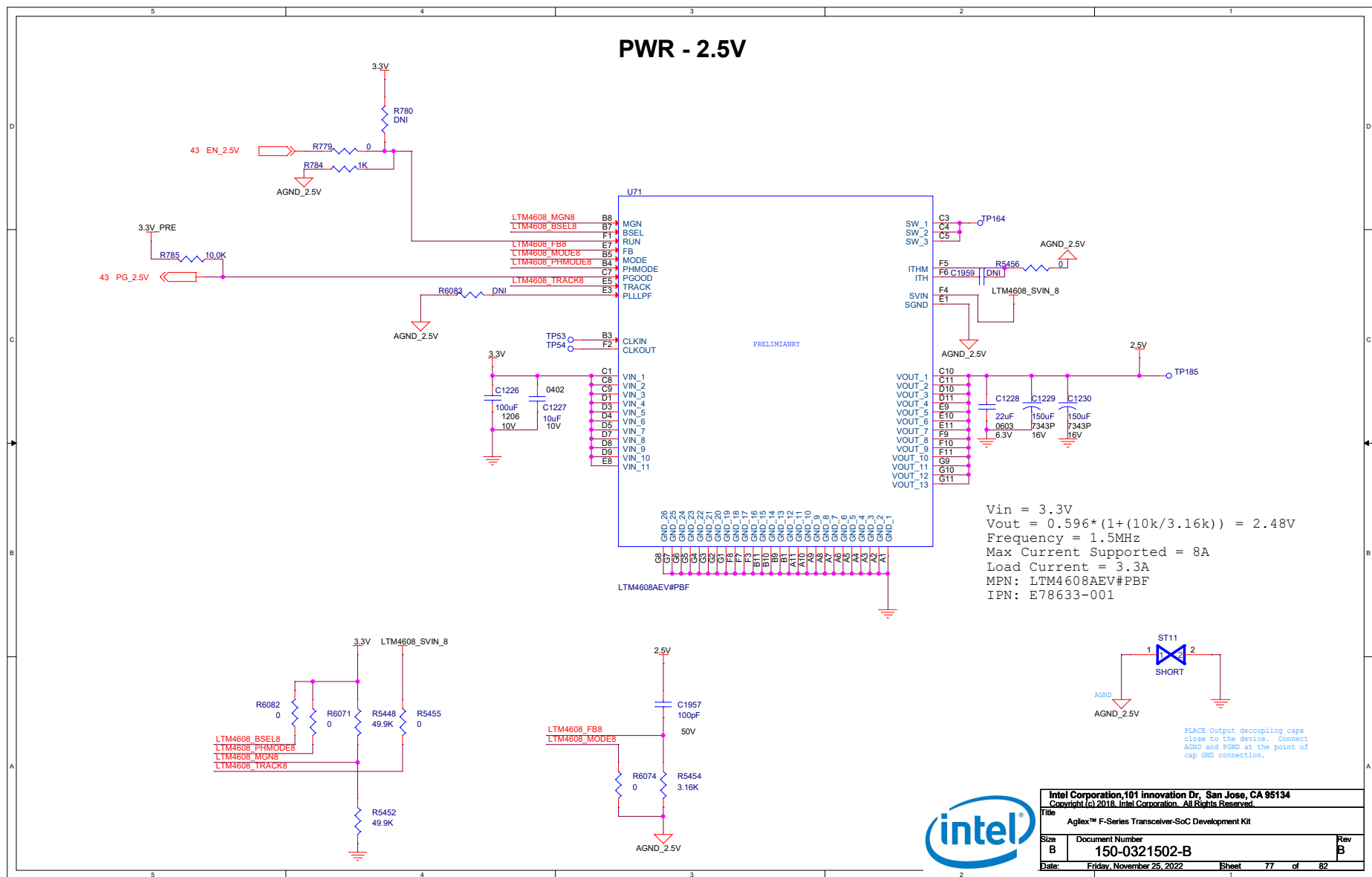
Vin = 1.2V
 Vout = 0.6V
 Max Current Supported = 3A
 MPN: NCP51200MNTXG
 IPN: K77668-001

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Title			
Agilex™ F-Series Transceiver-SoC Development Kit			
Size	Document Number	Rev	
B	150-0321502-B	B	
Date:	Friday, November 25, 2022	Sheet	75 of 82

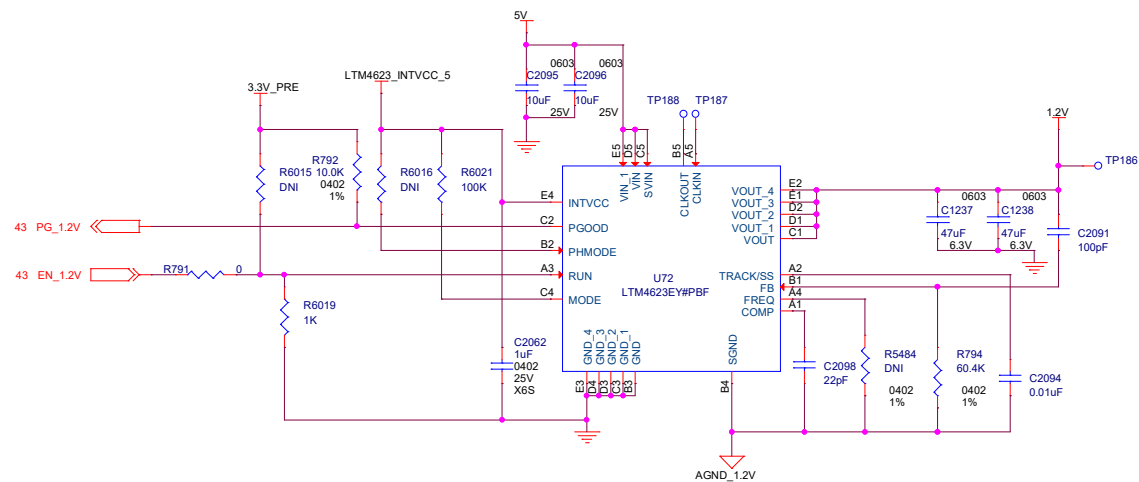
PWR - 1.8V



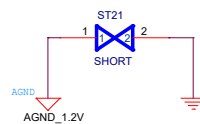
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Agilex™ F-Series Transceiver-SoC Development Kit			
Size	Document Number	Rev	
B	150-0321502-B	B	
Date:	Friday, November 25, 2022	Sheet	76 of 82



PWR - 1.2V



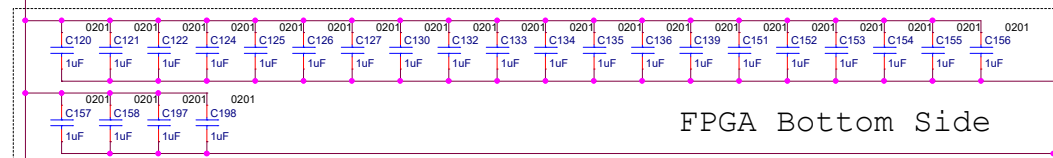
```
Vin = 5V
Vout = ((0.6*60.4k)/60.4k)+0.6 = 1.2V
Frequency = 1MHz
Soft Start = 3ms
Max Current Supported = 3A
Load Current = 253mA
MPN: LTM4623EY#PBF
IPN: K15502-001
```



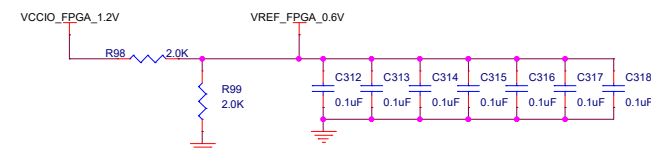
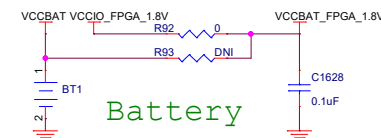
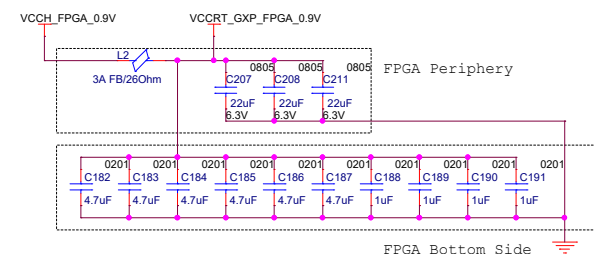
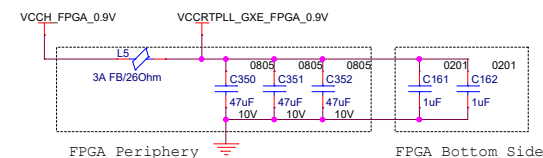
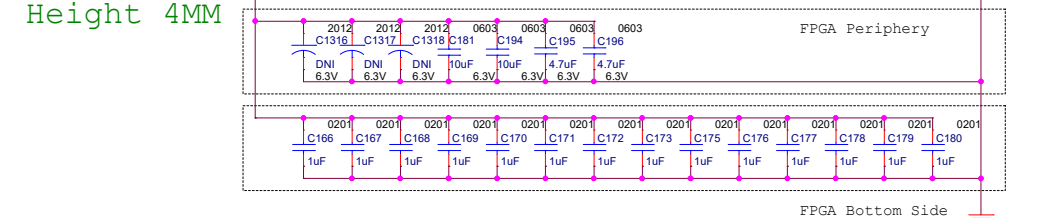
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Title	Agilix™ F-Series Transceiver-SoC Development Kit		
Size B	Document Number	Rev B	
	150-0321502-B		
Date:	Friday, November 25, 2022	Sheet	78 of 82

FPGA Decoupling 2

VCCH_FPGA_0.9V

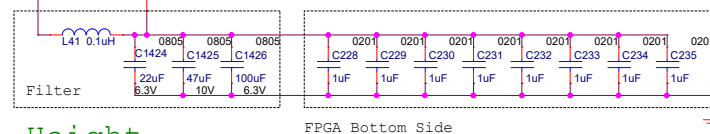
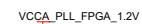
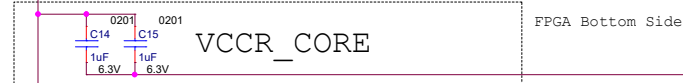
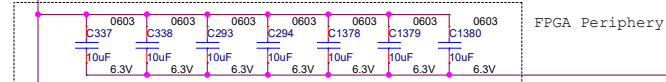
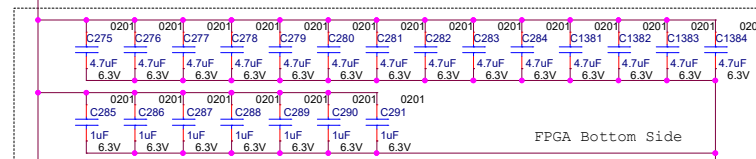
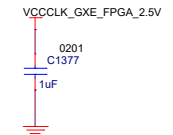
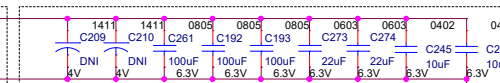
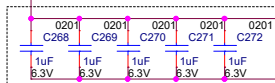
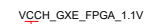
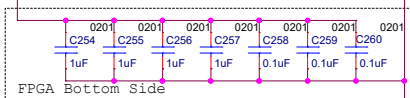
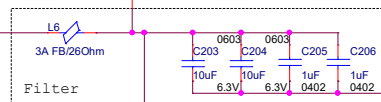
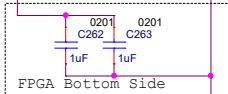
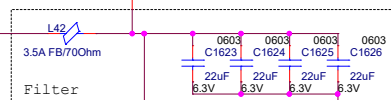
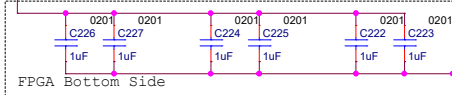
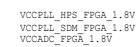
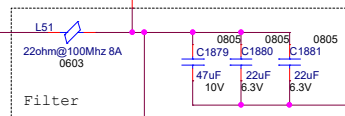
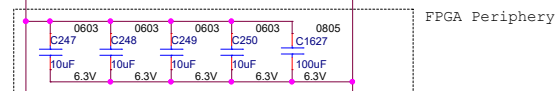
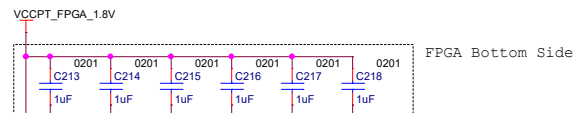


Height 4MM



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Agilex™ F-Series Transceiver-SoC Development Kit			
Size	Document Number	Rev	
B	150-0321502-B	B	
Date:	Friday, November 25, 2022	Sheet	80 of 82

FPGA Decoupling 3



Height
4MM



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Title				
Agilent™ F-Series Transceiver-SoC Development Kit				
Size				
Document Number				Rev
150-0321502-B				B
Date:	Friday, November 25, 2018	Sheet	81	of 82

REVISION HISTORY:

- 1) ADDED 1ms DELAY BETWEEN PG_VDD_SODIMM AND EN_VTT_SODIMM_0.6V
- 2) ADDED 1ms DELAY BETWEEN PG_VCCIO_FPGA_1.2V AND EN_VTT_DDR4_0.6V
- 3) CHANGED R1126 TO 0 OHMS & MADE R1119 AS DNI DUE TO BOARD SHUTTING WHEN PROBED AT RUN PIN OF U49
- 4) UPDATED FOOTPRINT OF L1, L47, L48, L49 WITH hc_tk0_sm_10800x8000_ma
- 5) MADE R537, R538 AS DNI & R536 AS 1K TO MAKE 12V AS DEFAULT ON
- 6) MADE R544, R547 AS DNI & R543 AS 1K TO MAKE 5V AS DEFAULT ON
- 7) MADE R950 & R951 AS DNI



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Title Agilex™ F-Series Transceiver-SoC Development Kit			
Size B	Document Number 150-0321502-B		Rev B
Date:	Friday, November 25, 2022	Sheet	82 of 82