

Product Brief

Intel® FPGA SmartNIC N6000-PL Platform



A SmartNIC for Accelerating Communications and Networking Workloads



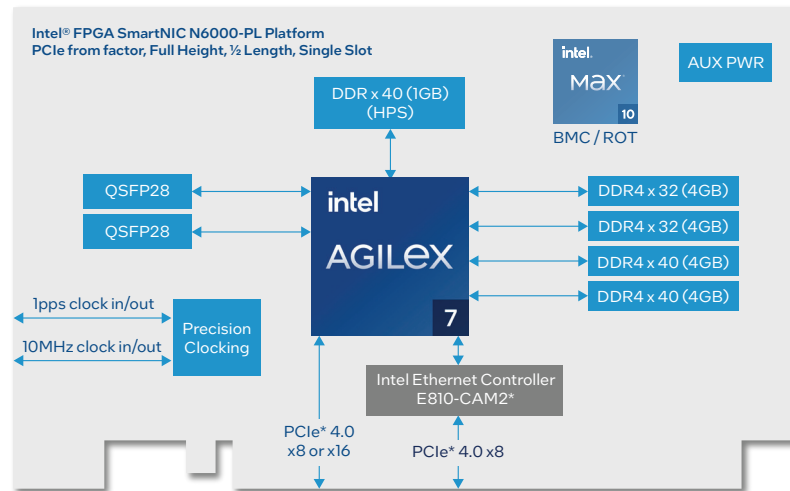
2x100Gb
Ethernet Connectivity

IEEE 1588v2 PTP
O-RAN/Broadcast

PCIe Form Factor
FHHL

**On-board Intel®
Ethernet
Controller E810***
Easy System
Integration

The Intel® FPGA SmartNIC N6000-PL Platform is Intel's 3rd generation SmartNIC providing 2x100 Gbps Ethernet connectivity. It is based on Intel Agilex® 7 FPGA F-Series family built with advanced 10 nm SuperFin technology delivering ~2X better fabric performance per watt compared to competing 7 nm FPGAs.



*The N6000-based SmartNICs come in two configurations:

- N6000-based SmartNIC with an Intel® Ethernet Controller E810 and bifurcated PCIe 4.0 x8 lanes to FPGA and x8 lanes to the Ethernet controller
- N6001-based SmartNIC without an Ethernet controller, PCIe 4.0 x16 lanes to FPGA

Accelerate Data From Edge to Cloud

Flexible and Scalable Platform

- Reference workloads available on production-ready boards
- Open FPGA Interface Manager (FIM) available for custom workload development
- Board design licensed to accelerate any custom board variant

Easy Software Integration

- SR-IOV-based standard host Interface using Intel Ethernet controller E810 requires no application code changes
- Open and standardized application programming interfaces (APIs) for Data Plane Development Kit (DPDK) PMD, and BBDev (vRAN only)

Synchronized Timing Solution

- Support 1588v2 PTP synchronization PRTC/T-GM, T-BC, T-TC, T-TSC clocks
- SyncE support
- On-board oven-controlled oscillator provides timing accuracy and extended hold-over

Use Cases

Workload designs for the N6000 Platform are developed and available through Intel and Partners.

Use cases	Configurations	Key Features
5G vRAN All-in-one architecture encompassing xHaul+ FEC + 1588 reduces total cost of ownership (TCO)	2x4x10G 2x2x25G	<ul style="list-style-type: none"> ▪ Support for Split 7-2X ORAN radios ▪ G.8273.2 1588 PTP conformance testing ▪ LDPC Gen 3.0 with URLLC support ▪ Open APIs for DPDK PMD and BBDev to ease software integration
Accelerated Virtual Cell Site Router (vCSR) All-in-one architecture encompassing vRouter + 1588 + optional FHGW ⁽¹⁾ + Optional FEC ⁽¹⁾ offering lower latency & TCO	4x25G 2x25G 7x10G	<ul style="list-style-type: none"> ▪ Control & Data Plane run on N6000 ▪ G.8273.2 PTP Conformance testing ▪ Optional hierarchical quality of service (HQoS) ▪ Open APIs for easy software integration ▪ Ready for network slicing ▪ MPLS auto provisioning
5G User Plane Function (UPF) Offload Low latency/jitter solution optimized for edge deployment where space and power are constrained	2x100GbE	<ul style="list-style-type: none"> ▪ Flow-based approach with 8M flows ▪ VLAN for N3/N6 identification, IPv4 and IPv6, GTPv1 ▪ Up to 1 million policers ▪ Each flow supports up to 2 policers ▪ Up to 8 million counters, 2 counters per flow ▪ 100G ingress NAT for IPv4
SMTE ST2110 Offload with JPEG-XS Nearly zero host core are used in professional video production workloads	2x100GbE	<ul style="list-style-type: none"> ▪ Video, audio, ancillary data and RTP header processing ▪ Packet pacer compliant with ST2110-21 (Type N, NL) ▪ Hitless protection switching (ST2022-7, up to class-C) ▪ High performant MCDMA ▪ Complete SDK including C/C++ API and Gstreamer plugin ▪ NMOS IS-04/IS-05 node application

⁽¹⁾ Additional functionality can be added depending on available device resources

Ordering Information

Production-Ready COTS Board

N6000-based SmartNIC commercial-off-the-shelf (COTS) board and workloads are available through ODM partners. Open FPGA Stack (OFS)-based FPGA Interface Manager (FIM) designs are also available to accelerate custom workload development.

			
Intel ODM Partner			
FPGA Device on Board	Intel Agilex® FPGA AGF014	Intel Agilex® FPGA AGF014	Intel Agilex® FPGA AGF027
Form Factor	FHHL	FHHL	FH3/4L
ODM/Partner Website	FPGA SmartNIC WSN6050 Series	Silicom FPGA SmartNIC	Artiza FPGA SmartNIC

Licensed Design

Accelerate custom board design by re-using the N6000 board design and tailoring it to your unique requirements. The Intel FPGA SmartNIC N6000-PL Platform consists of:

- Board design files
- OFS, FIM designs
- BMC design
- Reference workloads
- Documentation
- Sample card

To license the Intel FPGA SmartNIC N6000-PL/N6001-PL Platform design, contact an Intel sales representative.

Intel FPGA SmartNIC N6000-PL Platform Specifications

Configurations	Intel® FPGA SmartNIC N6000-PL Platform	Intel® FPGA SmartNIC N6001-PL Platform
Hardware		
FPGA	Intel Agilex FPGA F-Series AGF014 (AGFB014R24A2E2V) <ul style="list-style-type: none"> High-performance F-Series FPGAs, multi-gigabit SERDES transceivers up to 58 Gb Integrated 64-bit quad core Arm® Cortex A-53 MP core Hard Process System (HPS) 1,437K logic elements 190 Mb on-chip memory 4,510 DSP blocks 	
Onboard Memory	<ul style="list-style-type: none"> 16 GB DDR4 to FPGA <ul style="list-style-type: none"> 2 Channels x40 (x32 Data + x8ECC), 1200 MHz (2400Mbps) 4 GB (Total 8GB) 2 Channels x32 (x32 Data no ECC), 1200 MHz (2400Mbps), 4 GB (Total 8 GB) 1 GB DDR4 to HPS <ul style="list-style-type: none"> 1 Channel x40 (x32 Data + x8ECC), 1200 MHz (DDR4-2400) 1GB 	
PCIe Interface	PCIe 4.0 bifurcated x8/x8	PCIe 4.0 X16
Network Interface	<ul style="list-style-type: none"> Two QSFP 28/56 connectors 2x1x100 Gbps, 2x2x50 Gbps, 2x4x25 Gbps, 2x4x10 Gbps Support for CPRI, eCPRI 	
Network Interface Controller	<ul style="list-style-type: none"> On-board Intel E810-CAM2 Ethernet Controller <ul style="list-style-type: none"> Extensive OS support and SR-IOV enables easier system integration 100 Gbps Packet processing Pipeline and Virtualization support 	<ul style="list-style-type: none"> No on-board Ethernet controller
Timing Synchronization	<ul style="list-style-type: none"> IEEE 1588v2 support for PRTC/T-GM, T-BC, T-TSC, T-TC O-RAN S-Plane PTP support (G.8275.1) for LLS-C1, -C2, -C3, -C4 Support for Synchronous Ethernet (SyncE) Class B frequency and phase timing accuracy Integrated OCXO for holdover performance Timing interface for local PRTC support for ToD with 1PPS/10MHz SMA connectors 	
Form Factor	Full Height Half Length (FHHL) Single Slot	
Thermal/Power	<ul style="list-style-type: none"> Passively cooled Thermal design power(TDP*) – 125W Scenario design power (SDP) <100 W (Power consumption dependent on workload) NEBS Class 1 compliance support 	<ul style="list-style-type: none"> Passively cooled Thermal design power(TDP*) – 75W Scenario design power (SDP) <75 W (Power consumption dependent on workload)
ATX Connector	2x3 Pin 12V Aux Connector	Not Required
Board Management	<ul style="list-style-type: none"> Intel® MAX 10 FPGA BMC Full security implementation using Intel MAX 10 FPGA as RoT Remote update capabilities for FPGA flash memory and BMC Full card BMC solution host communication via SMBus and PCIe VDM 	
Power Management	Intelligent system power management with real-time telemetry and system health monitoring	

Configurations	Intel® FPGA SmartNIC N6000-PL Platform	Intel® FPGA SmartNIC N6001-PL Platform
Software		
Software	<ul style="list-style-type: none"> Data Plane Development Kit (DPDK) FlexRAN (BBDev (pf-bb-config)) for vRAN only Open Programmable Acceleration Engine (OPAE) Open FPGA Stack (OFS) 	<ul style="list-style-type: none"> Open Programmable Acceleration Engine (OPAE) Open FPGA Stack (OFS)
Design Entry Tools		
Design Entry Tool	<ul style="list-style-type: none"> Intel® Quartus® Prime Pro Edition Software oneAPI 	

*TDP not relevant to deployment power. TDP only used for server thermal design

Custom Workload Development

Develop custom workloads by leveraging pre-built FPGA Interface Manager (FIM) designs created by Open FPGA Stack (OFS). OFS is a scalable, source-accessible hardware and software reference infrastructure that provides all components to interface custom workloads to the host. FIMs are designed to be modular and scalable to help ease development. FIMs, OFS Software & documentation are available through Intel ODM partners.

FIMs include one or all of the following subsystems

- Platform Management
- Clocks/Resets
- HPS Subsystem
- PCIe Subsystem
- Memory Subsystem
- Transceiver Subsystem

FIM Configurations Provided

Configurations	N6000 FIMS				N6001 FIMS	
Hard Processor (HPS) Subsystem	No 1588 PTP			1588 PTP Enabled		No 1588 PTP
Transceiver Subsystem	2x4x10G	2x2x25G	2x1x100G	2x4x10G	2x2x25G	2x4x25G
PCIe Subsystem	4.0 x8					4.0 x16
Memory Subsystem	<ul style="list-style-type: none"> 2 Channels x40 (x32 Data + x8ECC), 1200 MHz (2400Mbps) 4 GB (Total 8GB) 2 Channels x32 (x32 Data no ECC), 1200 MHz (2400Mbps), 4 GB (Total 8 GB) 1 Channel x40 (x32 Data + x8ECC), 1200 MHz (DDR4-2400) 1G (for HPS) 					
SR-IOV Support	5-PF, 3-VF[PF0]					
AXIST Datapath	512b @ 350 MHz					512b @ 400 MHz
Intel E810 Ethernet Controller (100GbE)	Yes					No

Learn more at intel.com/n6000



Performance varies by use, configuration and other factors. Learn more at www.intel.com/PerformanceIndex.

Performance results are based on testing as of dates shown in configurations and may not reflect all publicly available updates. See backup for configuration details. No product or component can be absolutely secure.

Your costs and results may vary.

Intel technologies may require enabled hardware, software or service activation.

© Intel Corporation. Intel, the Intel logo, and other Intel marks are trademarks of Intel Corporation or its subsidiaries. Other names and brands may be claimed as the property of others.