

NOTES:

1. PROJECT DRAWING NUMBERS:

RAW PCB	100-0330712-A2
GERBER FILES	110-0330712-A2
PCB DESIGN FILES	120-0330712-A2
ASSEMBLY DRAWING	130-0330712-A2
FAB DRAWING	140-0330712-A2
SCHEMATIC DRAWING	150-0330712-A2
PCB FILM	160-0330712-A2
BILL OF MATERIALS	170-0330712-A2
SCHEMATIC DESIGN FILES	180-0330712-A2
FUNCTIONAL SPECIFICATION	210-0330712-A2
PCB LAYOUT GUIDELINES	220-0330712-A2
ASSEMBLY REWORK	320-0330712-A2

INTEL AGILEX® 7 FPGA I-SERIES TRANSCEIVER DEVELOPMENT KIT(6x F-TILE)

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91	VCCERT_U1x/VCCERT_U2x
92	VCCERT1_FHT_GXF_1V0_UX_G1
93	VCCERT2_FHT_GXF_1V0_UX_G1
94	POV8_G1/PIV8_G2
95	VCCERT_FHT_GXF_1V5_U1X_G2/P2V5_G2
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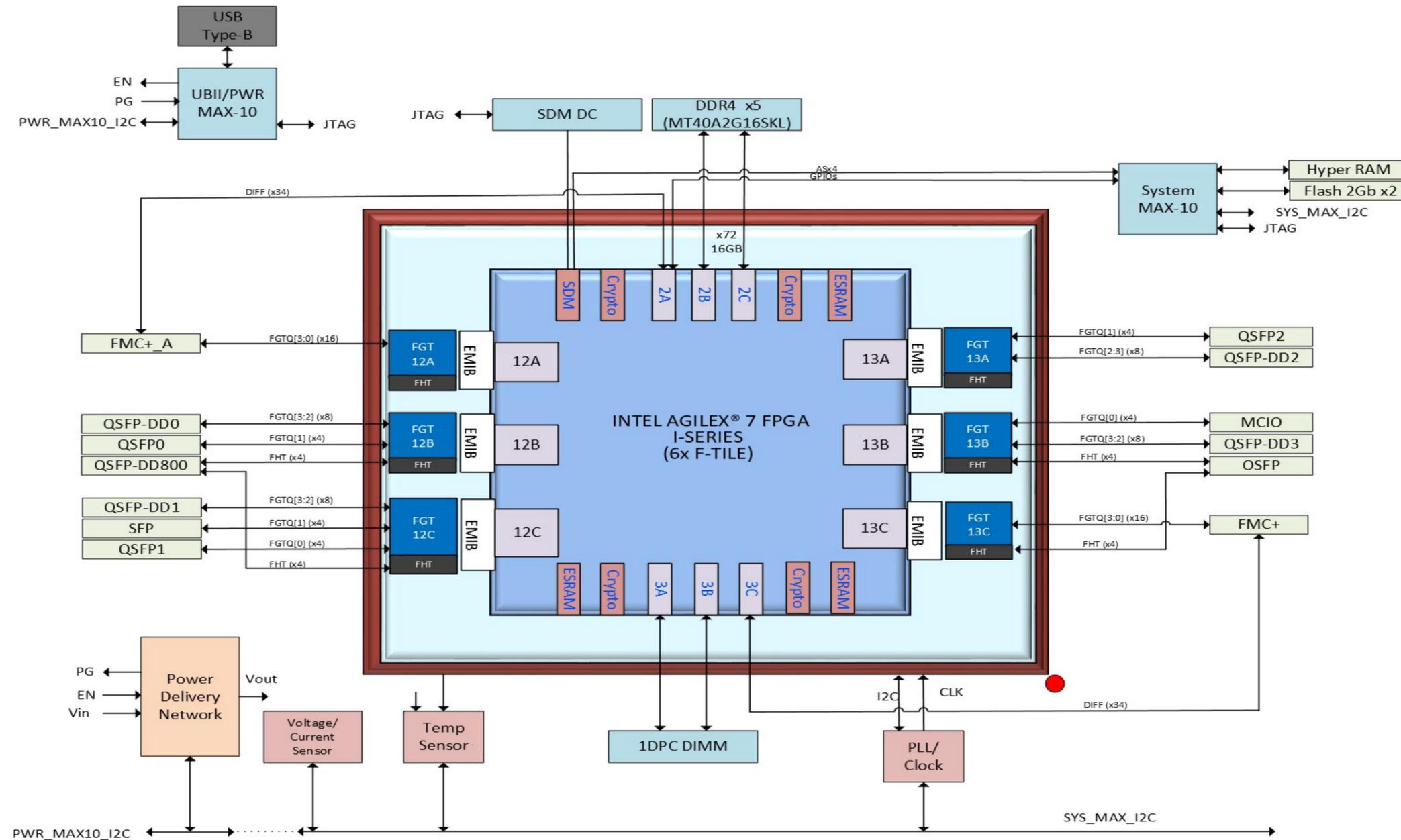
LEVEL	MMID	99C2HX
0	TA	M83887-001
1	ASSY	M77740-100
2	PB	M83888-001

Wed Aug 9 13:26:39 2023

DEPARTMENT PSG	Intel Corporation INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330690-A2	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 1 OF 105	

### BLOCK DIAGRAM

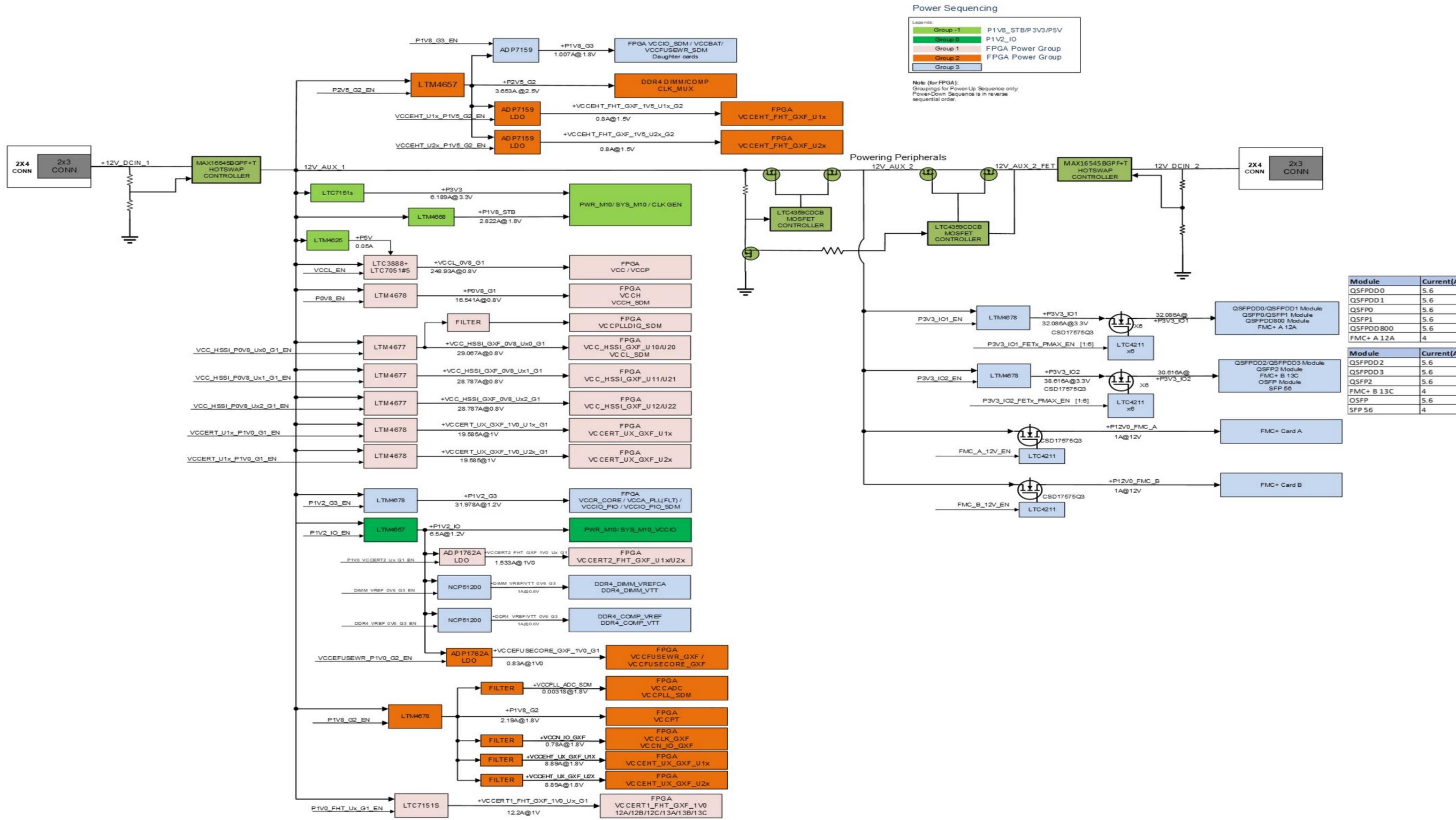
# INTEL AGILEX® 7 FPGA I-SERIES TRANSCEIVER DEVELOPMENT KIT(6x F-TILE)



Fri Sep 22 18:19:47 2023

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
P00	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 2 OF 105

# POWER TREE



Module	Current(A)
QSPFDD0	5.6
QSPFDD1	5.6
QSPF0	5.6
QSPF1	5.6
QSPFDD800	5.6
FMC+ A 12A	4

Module	Current(A)
QSPFDD2	5.6
QSPFDD3	5.6
QSPF2	5.6
FMC+ B 13C	4
OSFP	5.6
SFP 56	4

Tue Aug 8 11:15:53 2023

POWER ESTIMATION

Rail Name	Voltage (V)	Source	Efficiency	Consumption (A)	Power (W)	Voltage Regulator	Current Supported (A)	Group	RefDes
+P3V3	3.3	+12V0_AUX_1	90%	6.189	20.424	LTC7151SEV#PBF	15	Group - (-1)	U95
+P1V8_STB	1.8	+12V0_AUX_1	85%	2.822	5.079	LTM4668AIY#PBF	4.8	Group - (-1)	U79
+P5V	5	+12V0_AUX_1	85%	0.800	4.000	LTM4625EY#PBF	5	Group - (-1)	U102
+P1V2_IO	1.2	+12V0_AUX_1	85%	6.526	7.831	LTM4657EY#PBF	8	Group - 0	U47
+VCCL_OV8_G1	0.8	+12V0_AUX_1	87%	248.930	199.144	LTC3888+LTC7051(5)	300	Group - 1	U31,U32,U33,U34,U35,U181
+VCC_HSSI_GXF_OV8_Ux0_G1	0.8	+12V0_AUX_1	87%	29.067	23.254	LTM4677EY#PBF (Single)	36	Group - 1	U12
+VCC_HSSI_GXF_OV8_Ux1_G1	0.8	+12V0_AUX_1	87%	28.787	23.029	LTM4677EY#PBF (Single)	36	Group - 1	U6
+VCC_HSSI_GXF_OV8_Ux2_G1	0.8	+12V0_AUX_1	87%	28.787	23.029	LTM4677EY#PBF (Single)	36	Group - 1	U44
+VCCERT_UX_GXF_1V0_U1x_G1	1	+12V0_AUX_1	85%	19.585	19.585	LTM4678EY#PBF (Dual)	25	Group - 1	U20
+VCCERT_UX_GXF_1V0_U2x_G1	1	+12V0_AUX_1	85%	19.585	19.585	LTM4678EY#PBF (Dual)	25	Group - 1	U20
+POV8_G1	0.8	+12V0_AUX_1	87%	16.541	13.233	LTM4678EY#PBF (Dual)	25	Group - 1	U43
+VCCERT1_FHT_GXF_1V0_Ux_G1	1	+12V0_AUX_1	88%	12.200	12.200	LTC7151SEV#PBF	15	Group - 1	EU17
+VCCERT2_FHT_GXF_1V0_Ux_G1	1	+P1V2_IO	83%	1.536	1.536	ADP1762ACPZ-R7	2	Group - 1	U94
+P1V8_G2	1.8	+12V0_AUX_1	90%	20.753	37.356	LTM4678EY#PBF (Dual)	25	Group - 2	U43
+P2V5_G2	2.5	+12V0_AUX_1	85%	3.213	8.032	LTM4657EY#PBF	8	Group - 2	U21
+VCCEHT_FHT_GXF_1V5_U1x_G2	1.5	+P2V5_G2	60%	0.800	1.200	ADP7159ACPZ-01-R7	2	Group - 2	EU8
+VCCEHT_FHT_GXF_1V5_U2x_G2	1.5	+P2V5_G2	60%	0.800	1.200	ADP7159ACPZ-01-R7	2	Group - 2	EU1
+VCCEFUSECORE_GXF_1V0_G2	1	+P1V2_IO	50%	0.830	0.830	ADP1762ACPZ-R7	2	Group - 2	U24
+P3V3_IO1	3.3	+12V0_AUX_2	92%	32.086	105.884	LTM4678EY#PBF (Single)	50	Group - 3	U13
+P3V3_IO2	3.3	+12V0_AUX_2	92%	30.616	101.033	LTM4678EY#PBF (Single)	50	Group - 3	U30
+P1V2_G3	1.2	+12V0_AUX_1	90%	31.978	38.374	LTM4678EY#PBF (Single)	50	Group - 3	U10
+P12V0_FMC_A	12	+12V0_AUX_2	85%	1.000	12.000	FET/LTC4211CMS#PBF	3	Group - 3	U107/Q9
+P12V0_FMC_B	12	+12V0_AUX_2	85%	1.000	12.000	FET/LTC4211CMS#PBF	3	Group - 3	U4/Q10
+P1V8_G3	1.8	+P2V5_G2	85%	1.007	1.812	ADP7159ACPZ-01-R7	2	Group - 3	EU33
+DDR4_VTT_OV6_G3	0.6	+P1V2_IO	50%	1.000	0.600	NCP51200MNTXG	3	Group - 3	EU26
+DIMM_VREF_OV6_G3	0.6	+P1V2_IO	50%	0.100	0.060	NCP51200MNTXG	3	Group - 3	U69
+DIMM_VTT_OV6_G3	0.6	+P1V2_IO	50%	1.000	0.600	NCP51200MNTXG	3	Group - 3	U69
+DRR4_VREF_OV6_G3	0.6	+P1V2_IO	50%	0.500	0.300	NCP51200MNTXG	3	Group - 3	EU26

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POWER ESTIMATION

DEPARTMENT  
UNKNOWN

Intel Corporation  
2200 Mission College Blvd.  
P.O. BOX 58119  
Santa Clara, CA 95052-8119

SIZE  
C+

CODE  
34649

DOCUMENT NUMBER  
150-0330690-A2

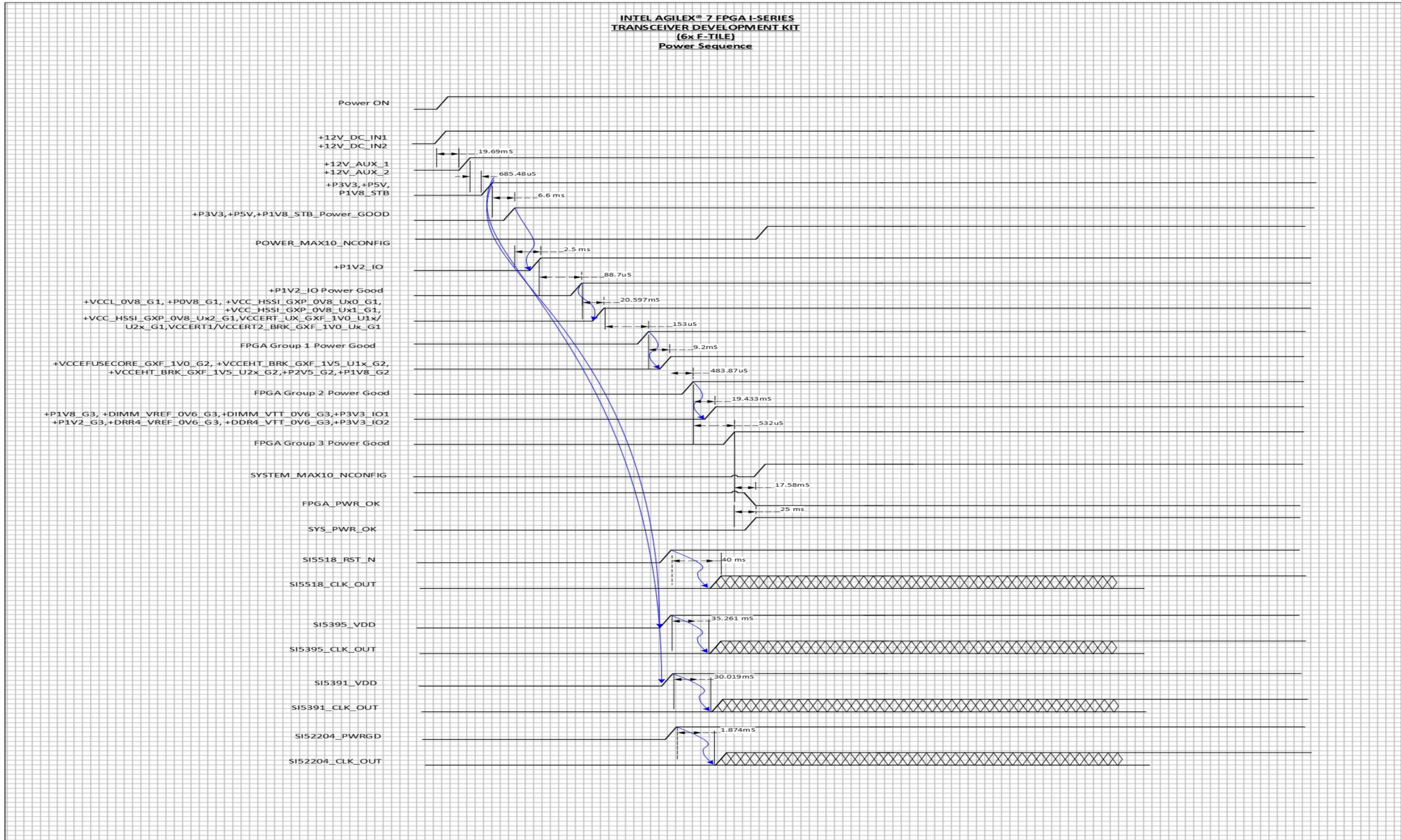
REV  
2.0

SCALE:

DO NOT SCALE DRAWING

SHEET 4 OF 105

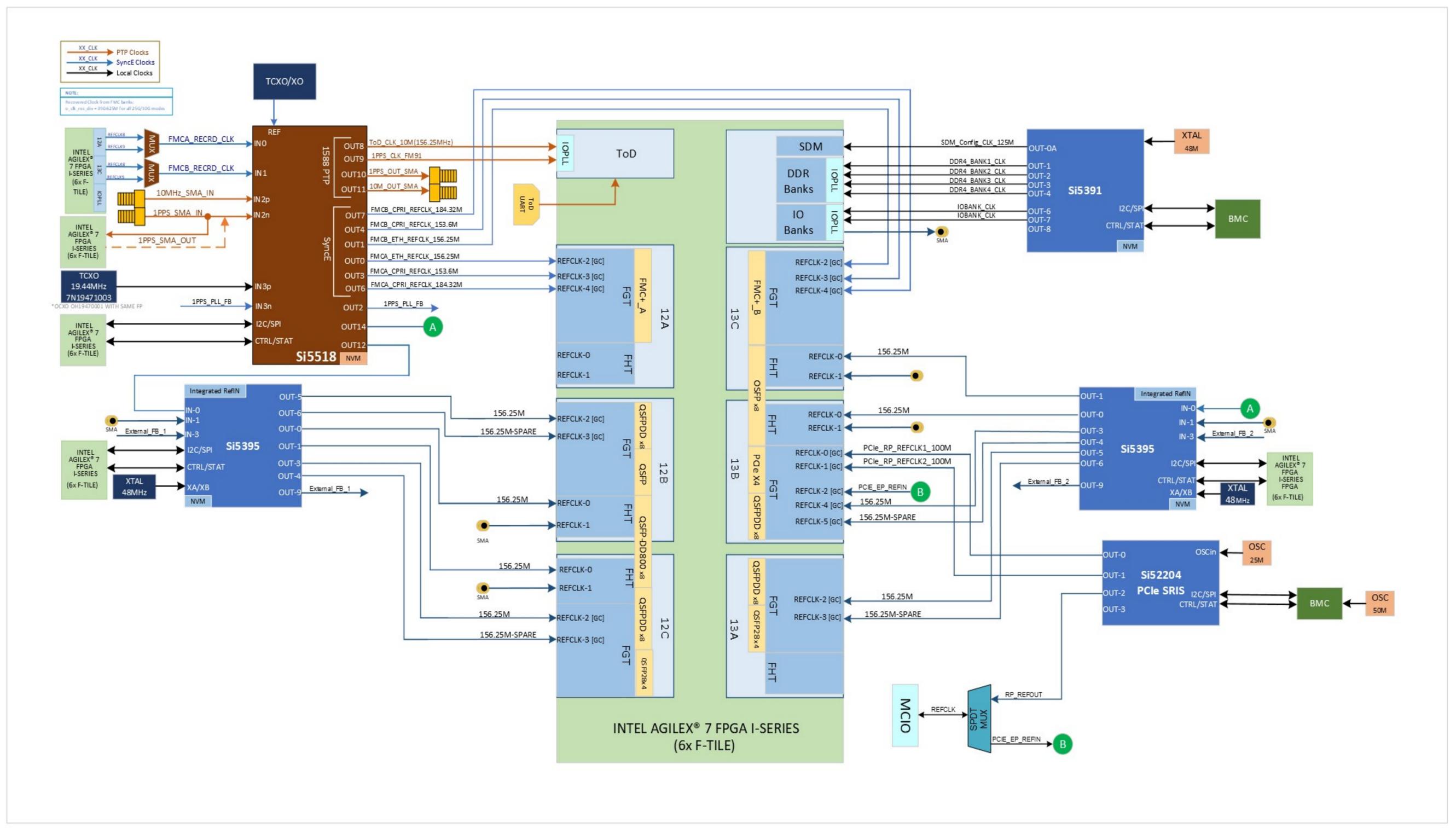
# POWER SEQUENCE GRAPH



Fri Sep 22 18:19:51 2023

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 5 OF 105	

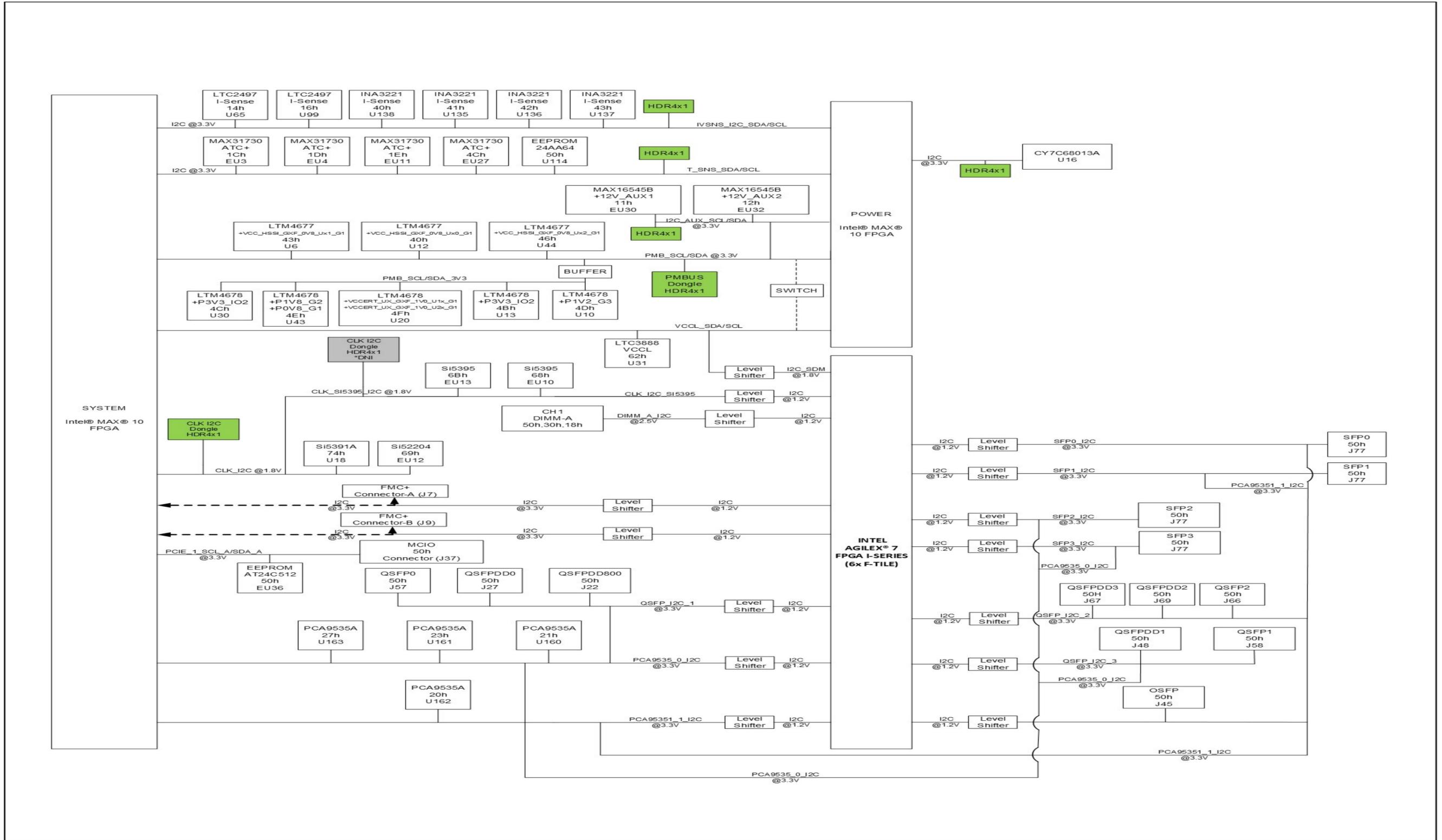
# CLOCK TREE



Tue Sep 26 11:47:16 2023

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PGG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 6 OF 105	

# I2C TREE



Fri Sep 22 18:19:51 2023

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
P00	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING			SHEET 7 OF 105

### I2C TABLE

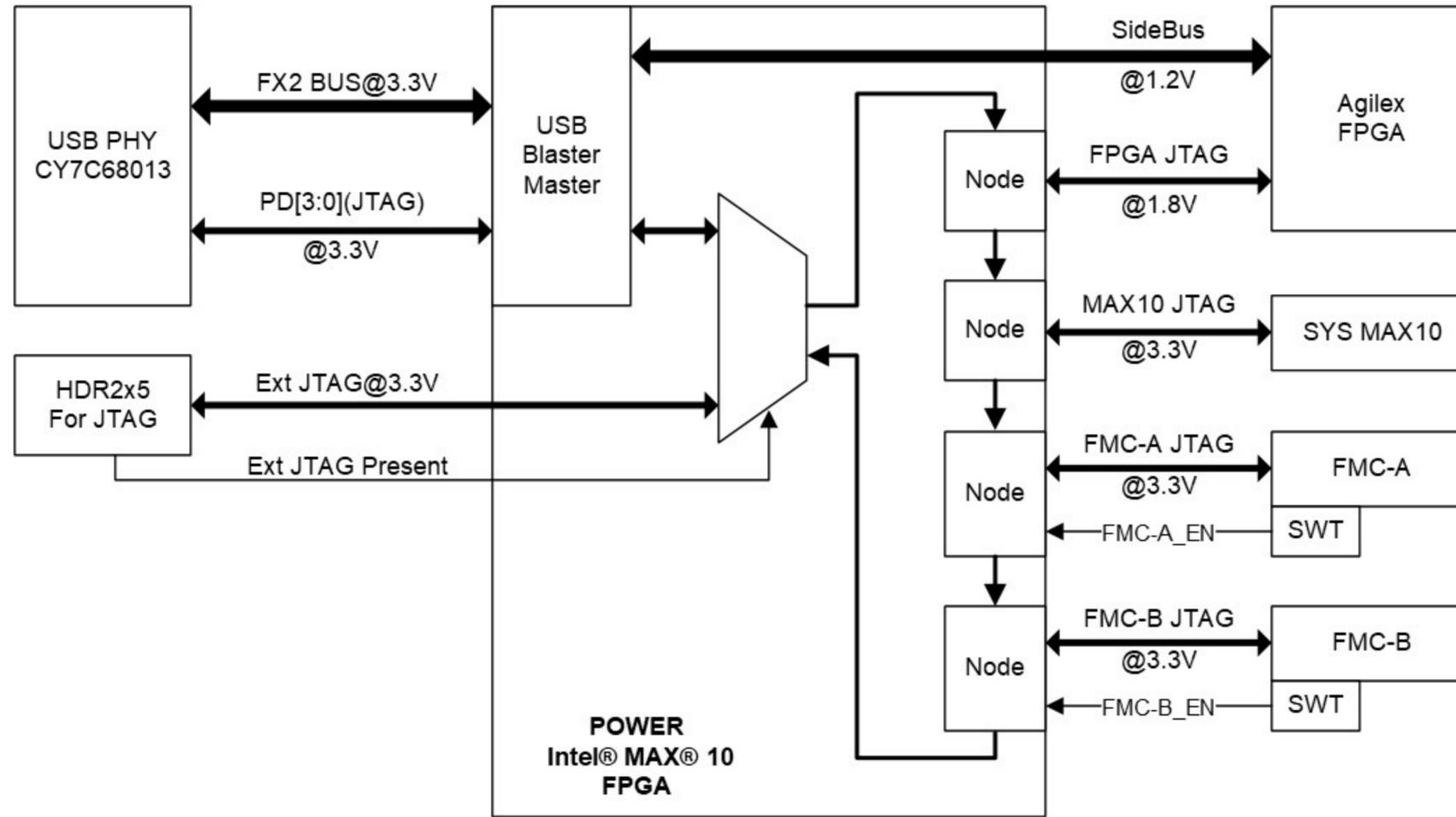
I2C NETS	MASTER 1	MASTER 2	MASTER 3	SLAVE 1	SLAVE 2	SLAVE 3	SLAVE 4	SLAVE 5	SLAVE 6	SLAVE 7	SLAVE 8	SLAVE 9	INTER I2C CONNECTION
CLK_SIS395_I2C_1V2_SDA	U1 FM91	J140 HEADER	----	EU13 SIS395 0x6B	EU10 SIS395 0x68	----	----	----	----	----	----	----	BELOW I2C ARE CONNECTED CLK_SIS395_I2C & CLK_I2C
CLK_SIS395_I2C_1V2_SCL				U18 SIS391 0x74	EU12 SIS2204_A02BGMR 0x69	----	----	----	----	----	----		
CLK_I2C_SDA	U3 SYSTEM MAX 10	J42 HDR	----	U161 PCA9535A 0x23	U160 PCA9535A 0x21	U163 PCA9535A 0x27	J77 SFP0 MOD3 0xA0	J48 QSFPDD1 0xA0	J58 QSFP1 0xA0	J22 QSFPDD800 0xA0	J27 QSFPDD0 0xA0	J57 QSFP0 0xA0	
PCA9535_0_1V2_SDA	U1 FM91	U3 SYSTEM MAX 10	----	----	----	----	J77 SFP0 MOD3 0xA0	----	----	----	----	----	PCA9535_0_I2C IS CONNECTED TO SFP0_I2C, QSFP3/1_I2C & PROVIDED OPTION FOR **SFP1_I2C MODULES WITH SAME I2C ADDRESS WILL BE CONTROLLED USING MODESEL PIN
PCA9535_0_1V2_SCL							J77 SFP1 MOD2 0xA0	----	----	----	----	----	
SFP0_MOD3_1V2_SDA	U1 FM91	U3 SYSTEM MAX 10	----	----	----	----	----	----	----	----	----	----	
SFP0_MOD3_1V2_SCL							----	----	----	----	----	----	
SFP1_MOD2_1V2_SDA	U1 FM91	**U3 SYSTEM MAX 10	----	----	----	----	----	----	----	----	----	----	
SFP1_MOD2_1V2_SCL							----	----	----	----	----	----	
I2C_QSFP_3_1V2_SDA	U1 FM91	U3 SYSTEM MAX 10	----	----	----	----	----	J48 QSFPDD1 0xA0	J58 QSFP1 0xA0	----	----	----	PCA9535_0_I2C IS CONNECTED TO SFP0_I2C, QSFP3/1_I2C & PROVIDED OPTION FOR **SFP1_I2C MODULES WITH SAME I2C ADDRESS WILL BE CONTROLLED USING MODESEL PIN
I2C_QSFP_3_1V2_SCL							----	----	----	----	----	----	
I2C_QSFP_1_1V2_SDA	U1 FM91	U3 SYSTEM MAX 10	----	----	----	----	----	----	----	J22 QSFPDD800 0xA0	J27 QSFPDD0 0xA0	J57 QSFP0 0xA0	
I2C_QSFP_1_1V2_SCL													
PCA9535_1_1V2_SDA	U1 FM91	U3 SYSTEM MAX 10	----	U162 PCA9535A 0x20	J69 QSFPDD2 0xA0	J67 QSFPDD3 0xA0	J66 QSFP2 0xA0	J77 SFP2 MOD1 0xA0	J45 QSFP 0xA0	----	----	----	PCA9535_1_I2C IS CONNECTED TO QSFP2_I2C & OSFP_I2C. PROVIDED OPTION FOR **SFP2/3_I2C MODULES WITH SAME I2C ADDRESS WILL BE CONTROLLED USING MODESEL PIN
PCA9535_1_1V2_SCL													
I2C_QSFP_2_1V2_SDA	U1 FM91	U3 SYSTEM MAX 10	----	----	J69 QSFPDD2 0xA0	J67 QSFPDD3 0xA0	J66 QSFP2 0xA0	----	----	----	----	----	
I2C_QSFP_2_1V2_SCL								----	----	----	----	----	
SFP2_MOD1_1V2_SDA	U1 FM91	**U3 SYSTEM MAX 10	----	----	----	----	----	J77 SFP2 MOD1 0xA0	----	----	----	----	
SFP2_MOD1_1V2_SCL									----	----	----	----	
SFP3_MOD0_1V2_SDA	U1 FM91	**U3 SYSTEM MAX 10	----	----	----	----	----	J77 SFP3 MOD0 0xA0	----	----	----	----	PCA9535_1_I2C IS CONNECTED TO QSFP2_I2C & OSFP_I2C. PROVIDED OPTION FOR **SFP2/3_I2C MODULES WITH SAME I2C ADDRESS WILL BE CONTROLLED USING MODESEL PIN
SFP3_MOD0_1V2_SCL									----	----	----	----	
I2C_OSFP_SDA	U1 FM91	U3 SYSTEM MAX 10	----	----	----	----	----	----	J45 OSFP 0xA0	----	----	----	
I2C_OSFP_SCL										----	----	----	
FMC_B_SDA_1V2	U1 FM91	**U3 SYSTEM MAX 10	----	J9 FMCB	----	----	----	----	----	----	----	----	
FMC_B_SCL_1V2													
FMC_A_SDA_1V2	U1 FM91	**U3 SYSTEM MAX 10	----	J7 FMC A	----	----	----	----	----	----	----	----	
FMC_A_SCL_1V2													
DDR4_DIMM_2_SDA_1V2	U1 FM91	----	----	J5 DIMM CONN EEPROM Memory- 0x50 WP settind- 0x30 Temp Sensor- 0x18	----	----	----	----	----	----	----	----	
DDR4_DIMM_2_SCL_1V2													
PCIE_1_SCL_A	U3 SYSTEM MAX 10	----	----	J37 MCIO 0x50	EU36 EEPROM 0x50	----	----	----	----	----	----	----	
PCIE_1_SDA_A													
FX2_SCL	J56-HDR	U16 CY7C68013A	----	U2 POWER MAX 10	----	----	----	----	----	----	----	----	
FX2_SDA													
VCCL_SDA	U2 POWER MAX 10	U3 SYSTEM MAX 10	----	U31 VCCL CONTROLLER 0x62	FM91 SDM	----	----	----	----	----	----	----	VCCL_I2C & PMB_I2C ARE CONNECTED THROUGH A SWITCH S21 **BY DEFAULT- OPEN
VCCL_SCL													
PMB_SDA	U2 POWER MAX 10	U3 SYSTEM MAX 10	J41 HDR	U6 LTM4677 0x43	U44 LTM4677 0x46	U12 LTM4677 0x40	U30 LTM4678 0x4C	U13 LTM4678 0x4B	U10 LTM4678 0x4D	U43 LTM4678 0x4E	U20 LTM4678 0x4F	----	
PMB_SCL													
T_SNS_SCL	**U2 POWER MAX 10	U3 SYSTEM MAX 10	J79 HDR	EU3 MAX31730 0x38	EU4 MAX31730 0x3A	EU11 MAX31730 0x3C	EU27 MAX31730 0x98	U114 EEPROM 24AA64 0x50	----	----	----	----	
T_SNS_SDA													
IVSNS_I2C_SDA	**U2 POWER MAX 10	U3 SYSTEM MAX 10	J149-HDR	U138 INA3221 0x40	U135 INA3221 0x41	U136 INA3221 0x42	U137 INA3221 0x43	U99 LTC2497 0x16	U65 LTC2497 0x14	----	----	----	
IVSNS_I2C_SCL													
I2C_AUX_SCL	U2 POWER MAX 10	J154 HDR	----	EU30 MAX16545B 0x11	EU32 MAX16545B 0x12	----	----	----	----	----	----	----	
I2C_AUX_SDA													

Fri Sep 22 19:27:18 2023

I2C\_TABLE

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
UNKNOWN	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 8 OF 105

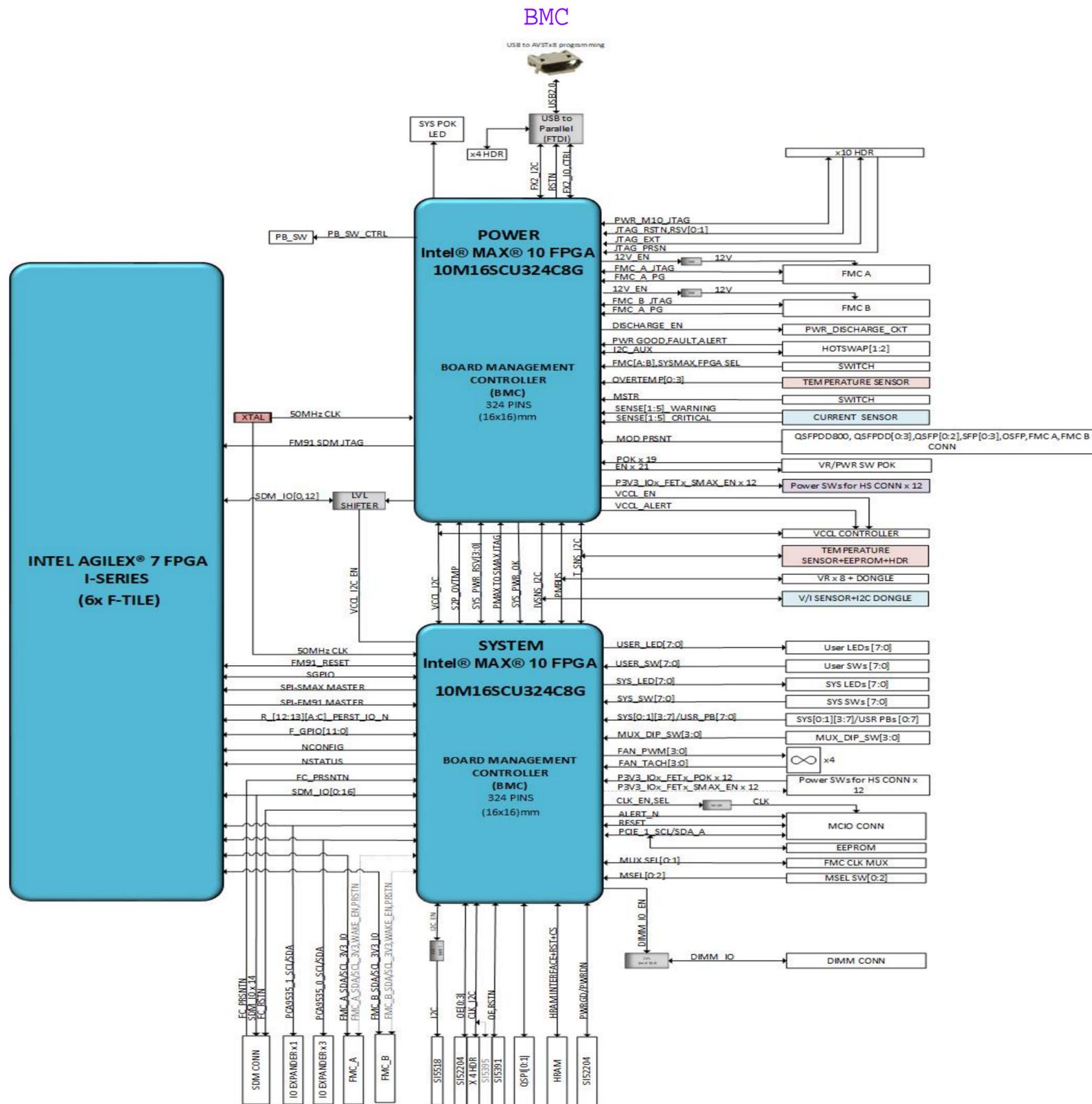
### JTAG TOPOLOGY



**Note:**  
 1. The JTAG of Agilex FPGA can't be added to the chain before fully powered up

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SCALE:		DO NOT SCALE DRAWING		SHEET 9 OF 105	



Fri Sep 22 18:19:52 2023

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
UNKNOWN	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING			SHEET 10 OF 105

4

3

2

1

### SDM IO MAPPING

SDM PINS	MSEL FUNCTIONS	CONFIGURATION SOURCE FUNCTION
		AS
SDM_IO0		PWR_SCL
SDM_IO1		DATA1
SDM_IO2		CLK
SDM_IO3		DATA2
SDM_IO4		DATA0
SDM_IO5	MSEL0	NCS00
SDM_IO6		DATA3
SDM_IO7	MSEL1	NCS02
SDM_IO8		NCS03
SDM_IO9	MSEL2	NCS01
SDM_IO10		
SDM_IO11		HPS_CRSTN
SDM_IO12		
SDM_IO13		
SDM_IO14		
SDM_IO15		RESETN
SDM_IO16		CPG_DONE

SYSTEM MAX IS THE SOURCE OF HPS\_CRSTN FUNCTION

Tue Aug 8 11:15:59 2023

4

3

2

1

DEPARTMENT

Intel Corporation

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INDIA, 560103  
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SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-A2

REV

2.0

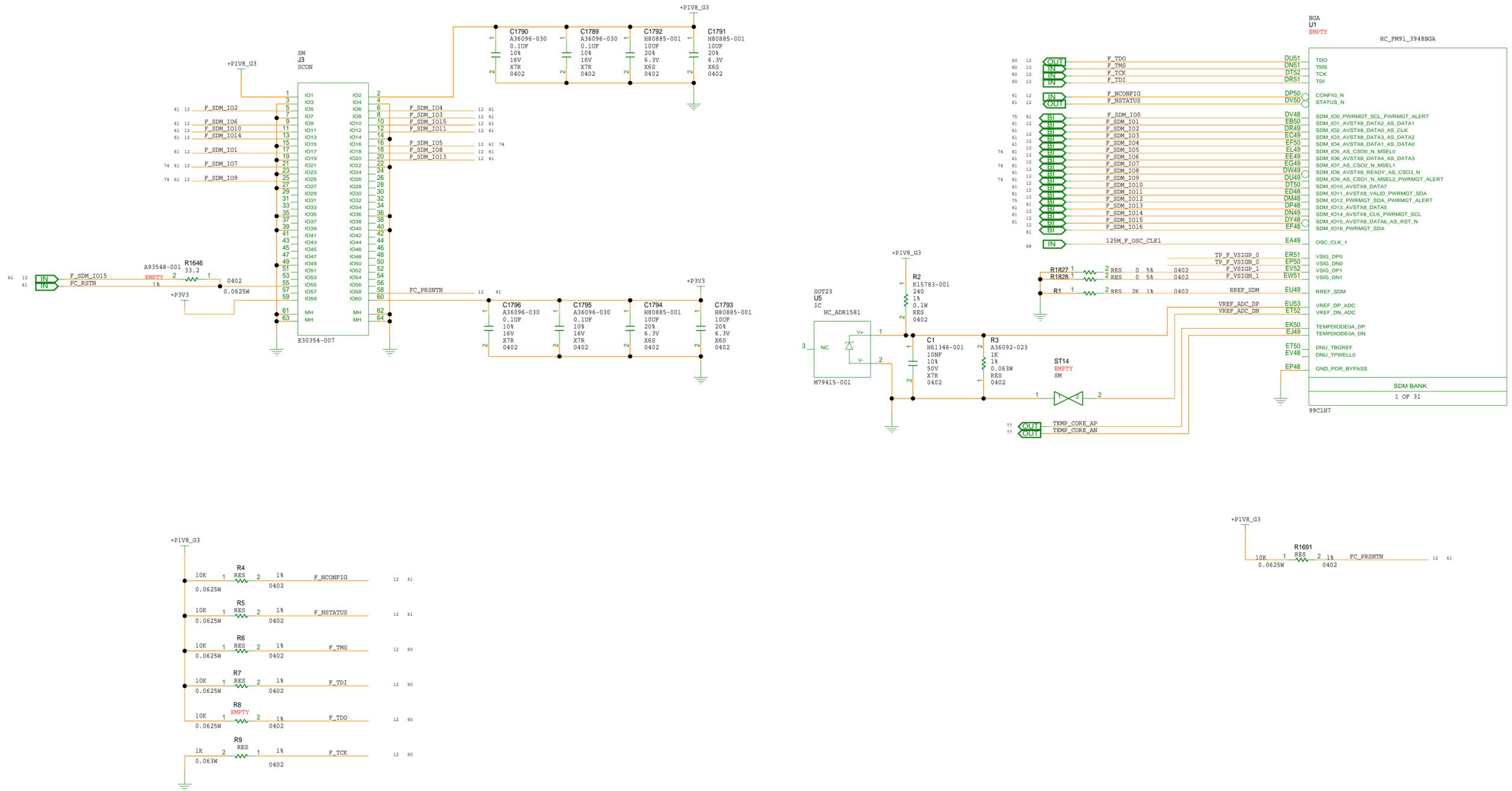
SCALE:

DO NOT SCALE DRAWING

SHEET

11 OF 105

# FPGA SDM



Wed Mar 6 15:45:14 2024

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 12 OF 105	

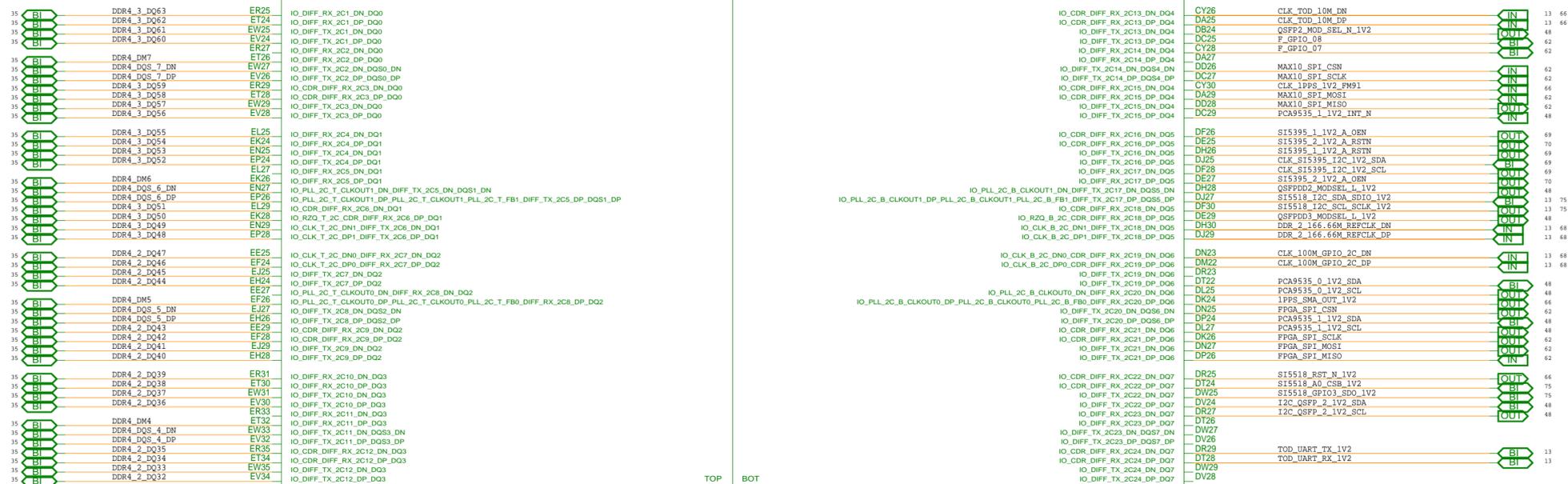
### FPGA BANK 2C

**CAD NOTE:**

BIT-SWAPPINGS ALLOWED WITHIN A BYTE.  
BYTE-SWAPPING IS ALLOWED WITH PRIOR APPROVAL  
FROM DESIGN ENGINEER

BGA  
U1  
EMPTY

HC\_FM91\_3948BGA



TOP BOT

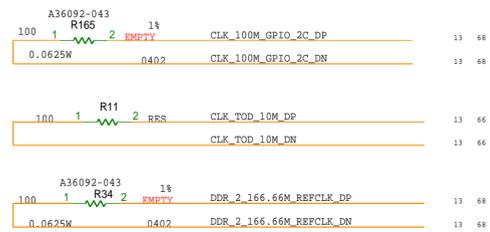
IO BANK 2C  
2 OF 31

99C1B7



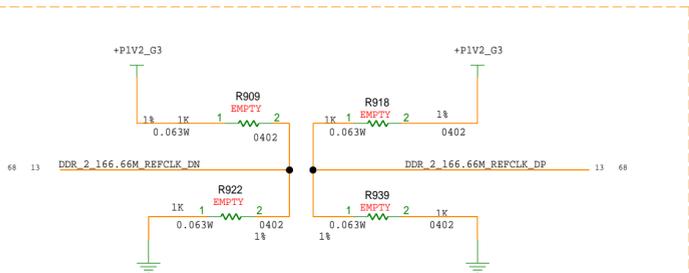
**CAD NOTE:**

PLACE THESE TERMINATION RESISTORS UNDER THE FPGA

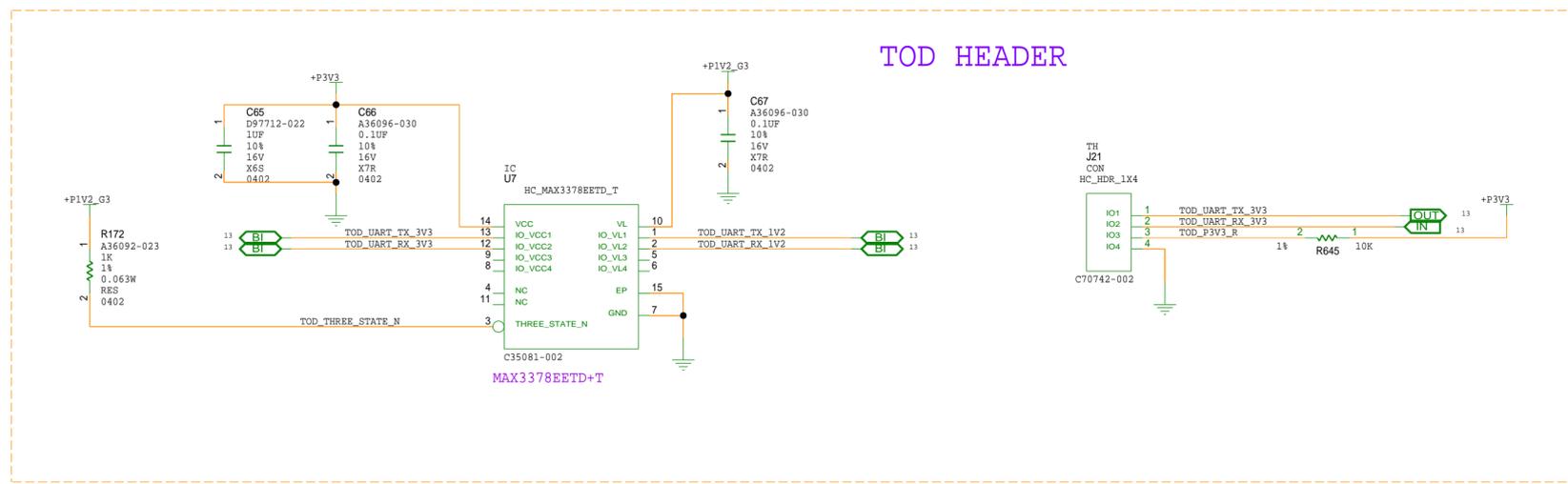


**CAD NOTE:**

PLACE THESE TERMINATION RESISTORS NEAR TO THE FPGA



### TOD HEADER



Wed Mar 6 15:45:15 2024

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 13 OF 105	

4

3

2

1

### FPGA BANK 2B

BGA  
U1  
EMPTY

HC\_FM91\_3948BGA

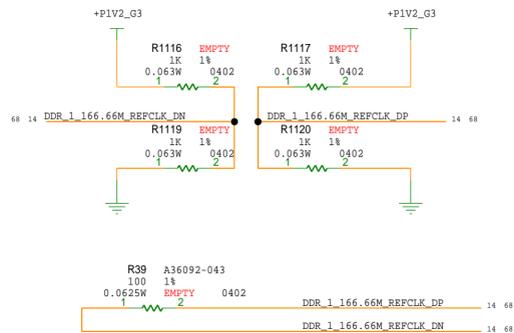


TOP BOT

IO BANK 2B

3 OF 31

99C1H7



CAD NOTE:

PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA

Wed Mar 6 15:45:15 2024

DEPARTMENT PSG	Intel Corporation INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330690-A2	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 14 OF 105	

4

3

2

1

FPGA BANK 2A

BGA  
U1  
EMPTY

HC\_F91\_3948BGA

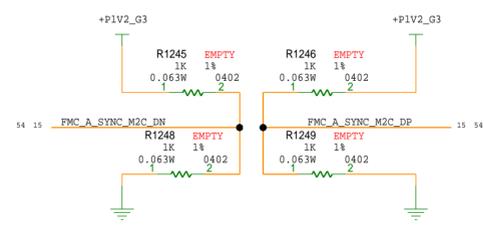


TOP BOT

IO BANK 2A

4 OF 31

99C1H7

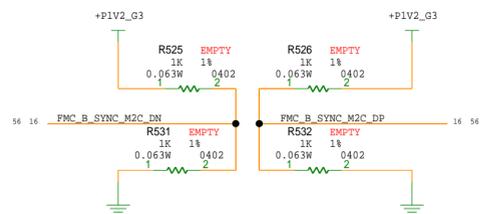
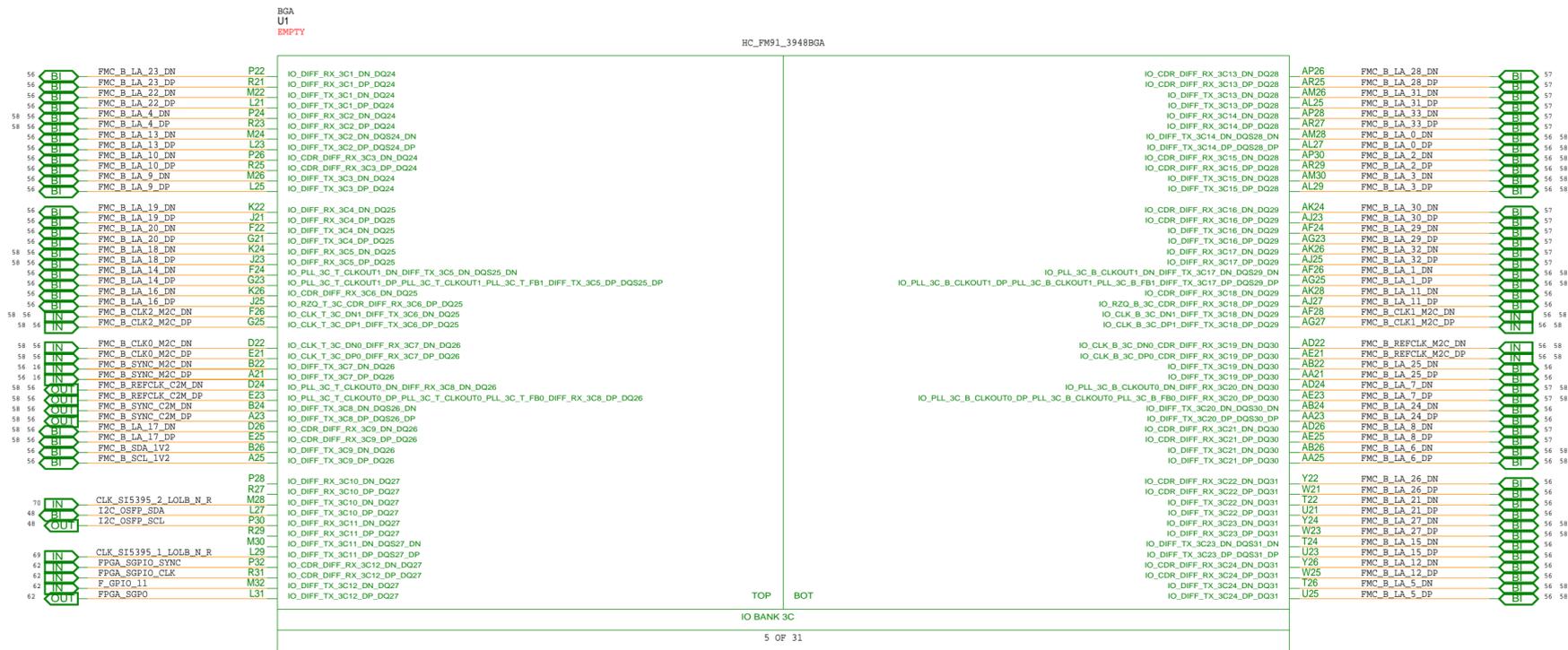


CAD NOTE:  
PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA

Wed Mar 6 15:45:16 2024

DEPARTMENT PSG	Intel Corporation INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330690-A2	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 15 OF 105	

# FPGA BANK 3C

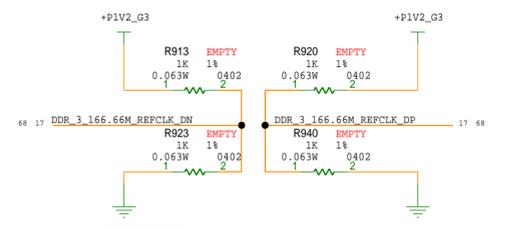
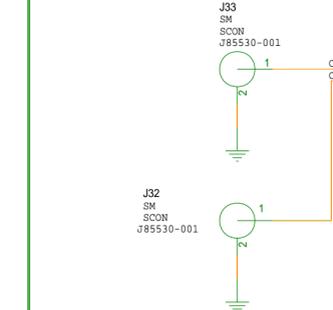
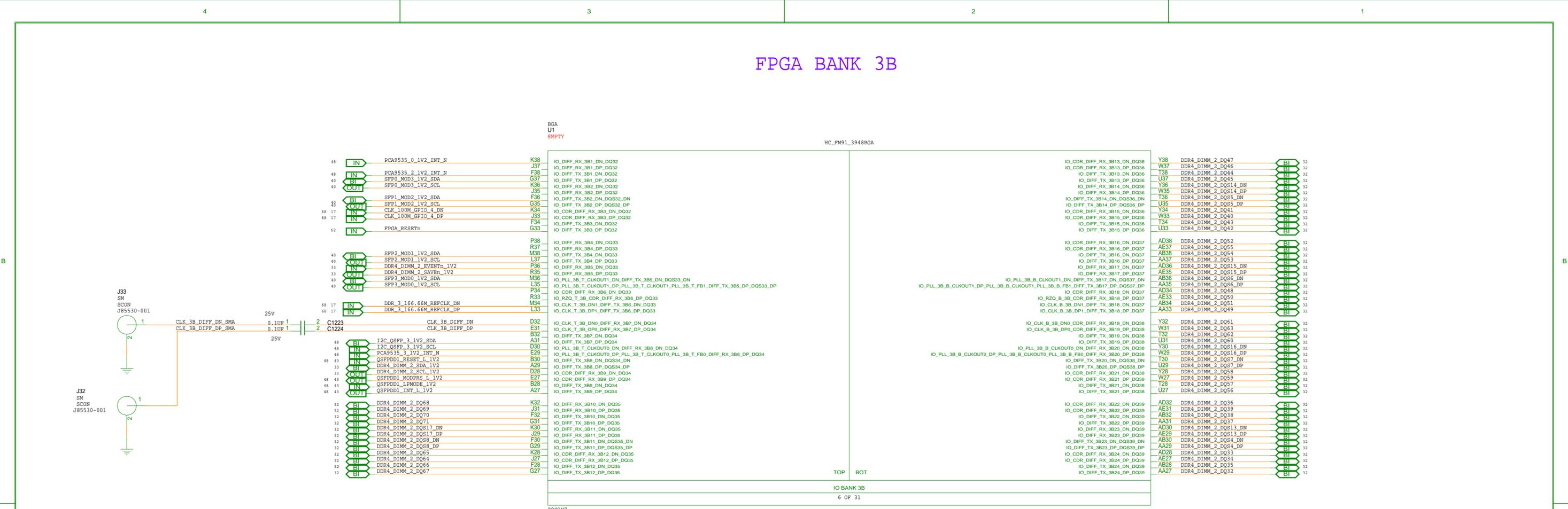


**CAD NOTE:**  
PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA

Wed Mar 6 15:45:16 2024

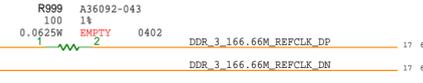
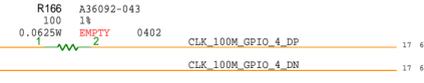
DEPARTMENT PSG	Intel Corporation INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330690-A2	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 16 OF 105	

# FPGA BANK 3B



**CAD NOTE:**  
PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA

**CAD NOTE:**  
PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA



Wed Mar 6 15:45:17 2024

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 17 OF 105	

FPGA BANK 3A

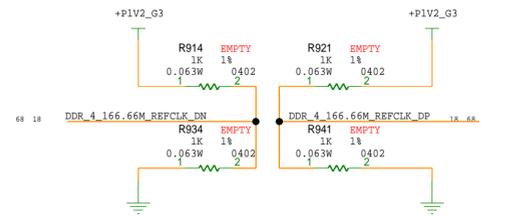
HC\_F991\_3948BGA

BGA  
U1  
EMPTY

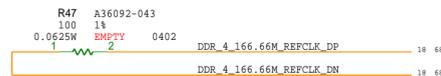


TOP BOT  
IO BANK 3A  
7 OF 31

99C1H7



CAD NOTE:  
PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA



Wed Mar 6 15:45:17 2024

DEPARTMENT PSG	Intel Corporation INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330690-A2	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 18 OF 105	

# FPGA BANK 13C

CAD NOTE:

PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS.  
FMC\_B\_RX\*

BGA

U1

EMPTY

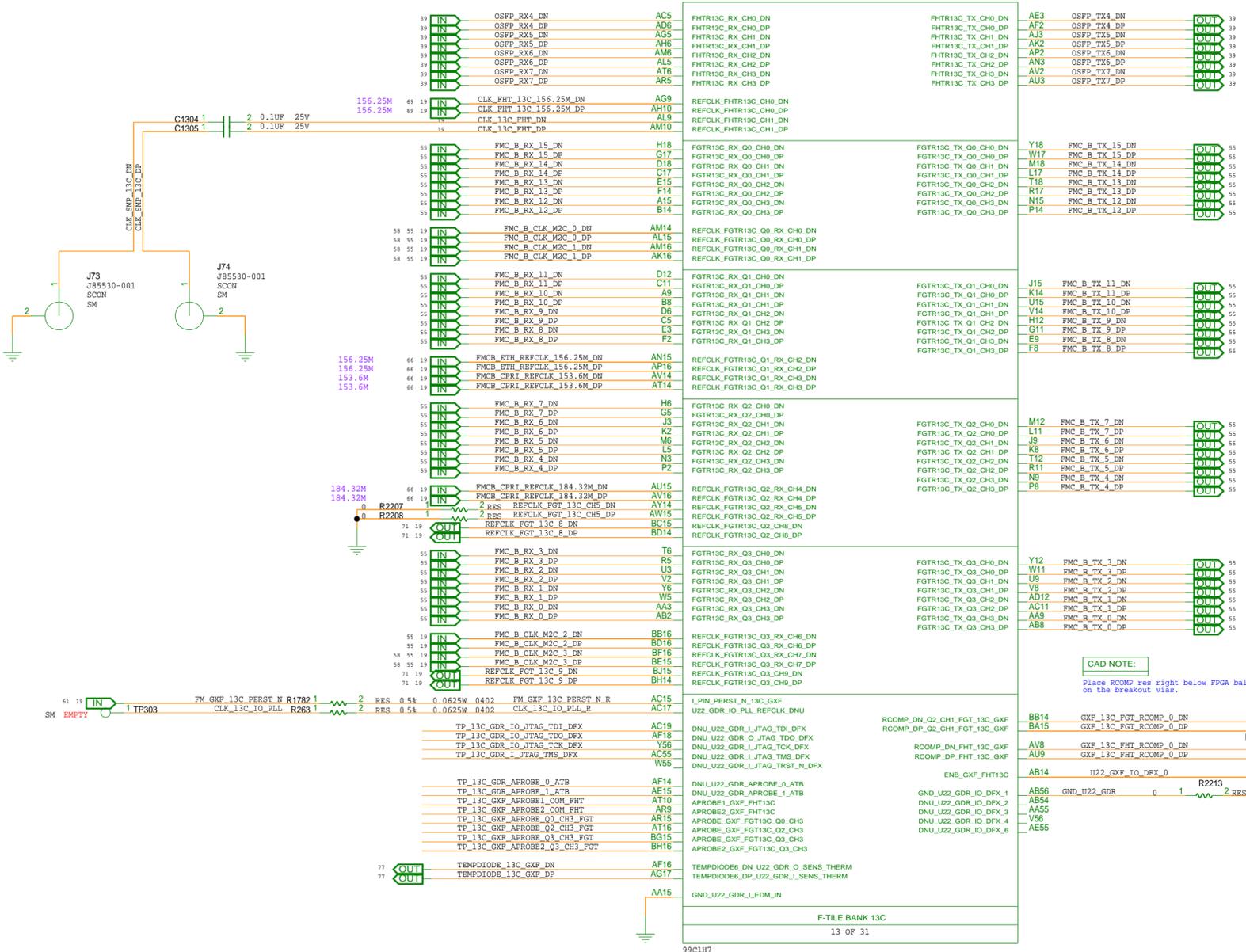
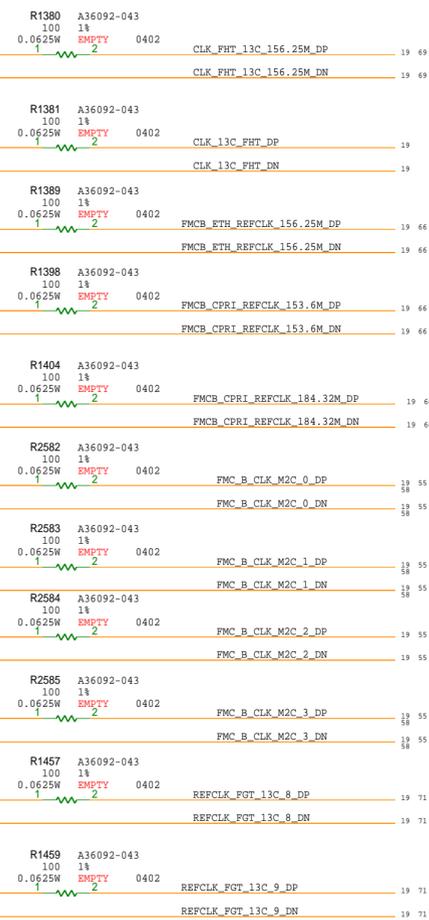
HC\_FM91\_3948BGA

CAD NOTE:

PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS

CAD NOTE:

PLACE THESE 100-OHM RES RIGHT BELOW FPGA BALLS ON THE BREAKOUT VIAS.



CAD NOTE:

Place RCOMP res right below FPGA balls on the breakout vias.

DESIGN NOTE:

Indicates BARAK\_IS\_USED

Wed Mar 6 15:45:18 2024

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	INDIA, 560103	C+	34649	150-0330690-A2	2.0
COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED		SCALE:	DO NOT SCALE DRAWING		SHEET 19 OF 105



# FPGA BANK 13A

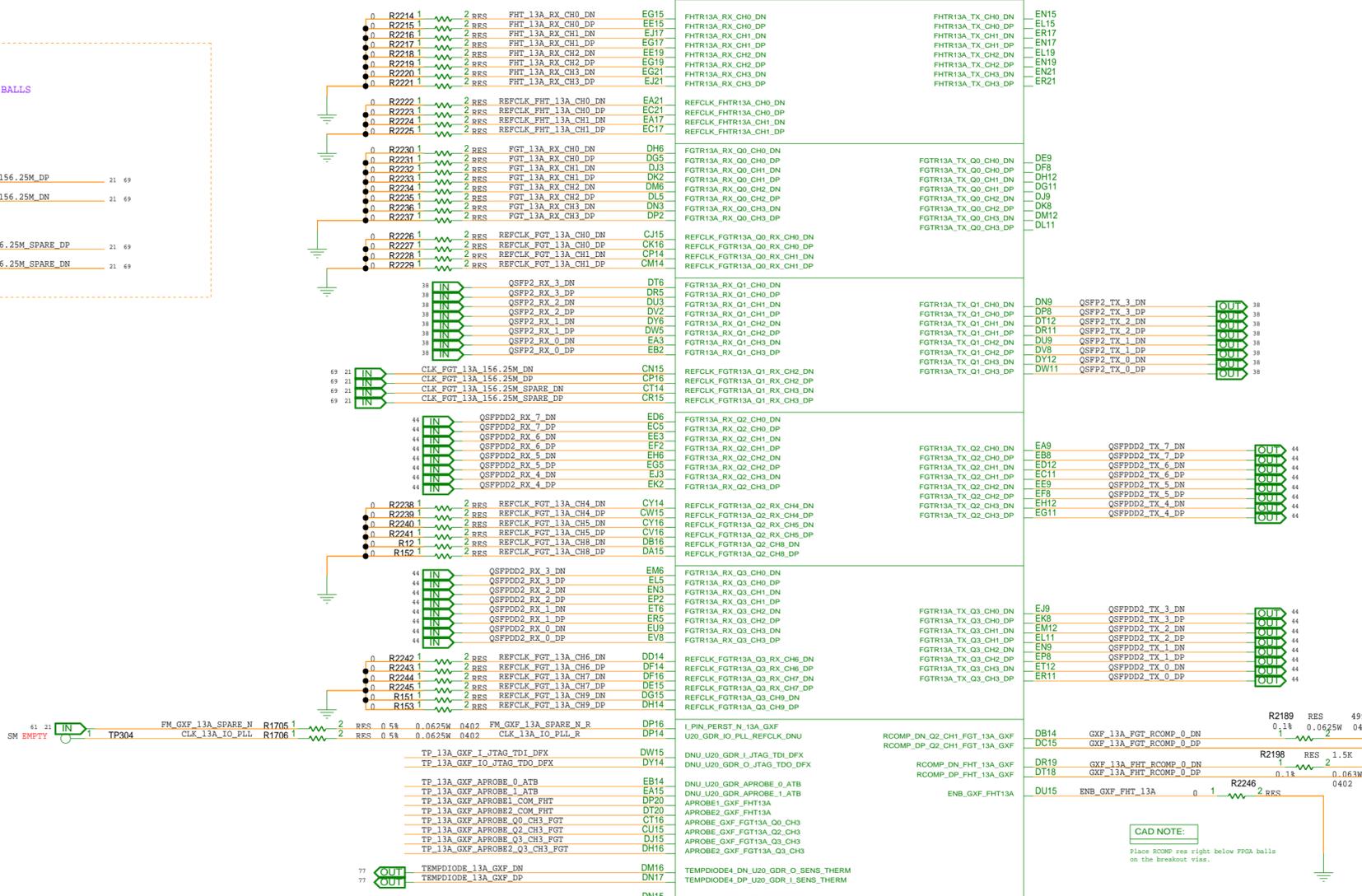
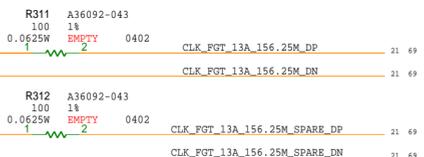
BGA U1  
EMPTY  
HC\_PM91\_3948BGA

CAD NOTE:

PLACE THESE 100-OHM RES RIGHT BELOW FPGA BALLS ON THE BREAKOUT VIAS.

CAD NOTE:

PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS



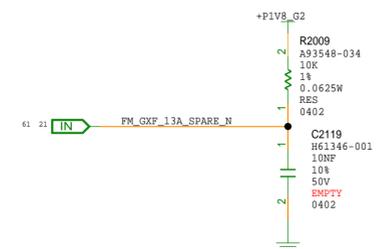
CAD NOTE:

Place RCMP res right below FPGA balls on the breakout vias.

F-TILE BANK 13A

11 OF 31

99C1H7



Wed Mar 6 15:45:19 2024

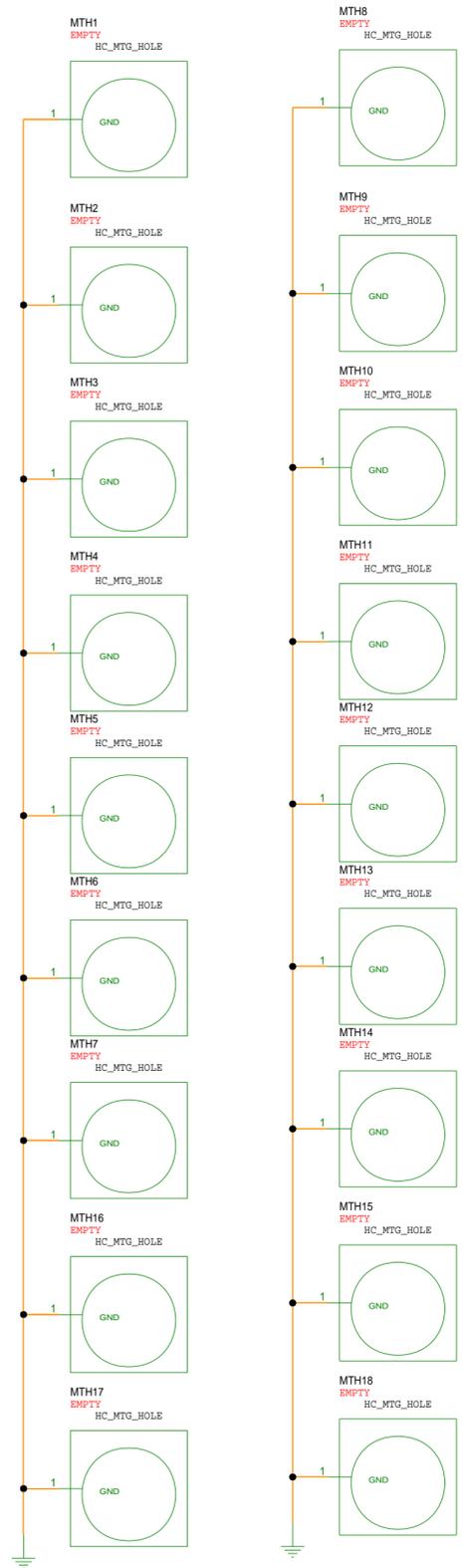
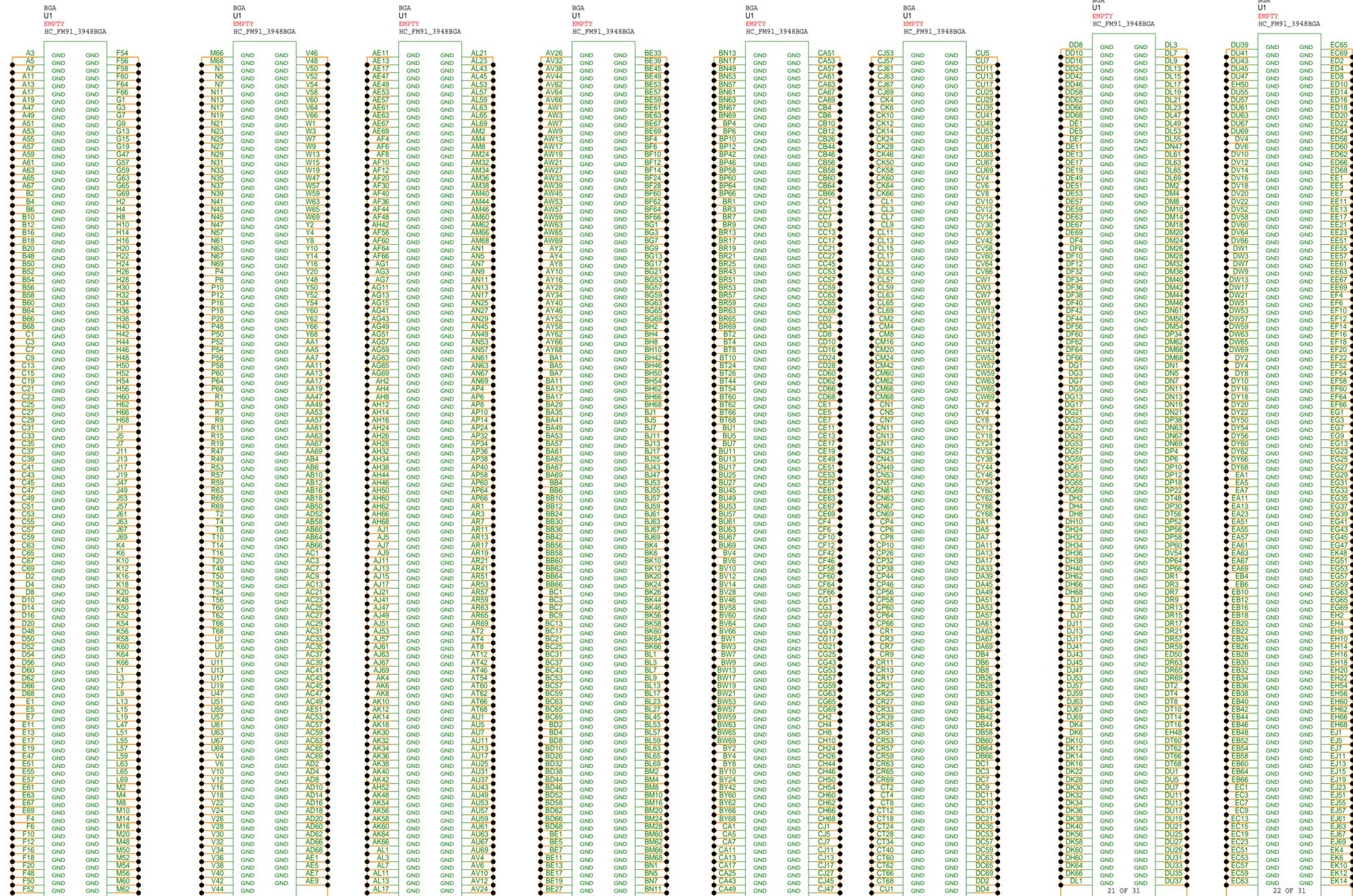
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 21 OF 105	







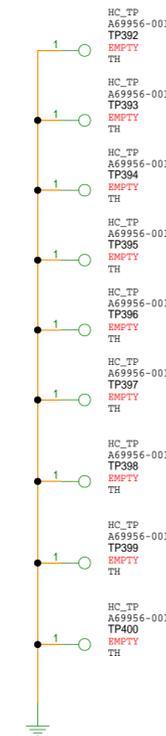
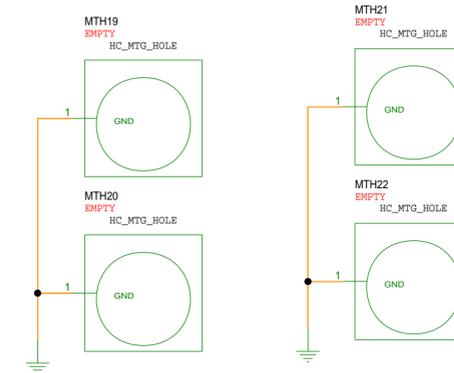
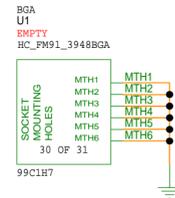
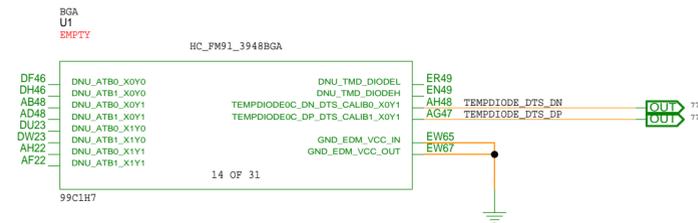
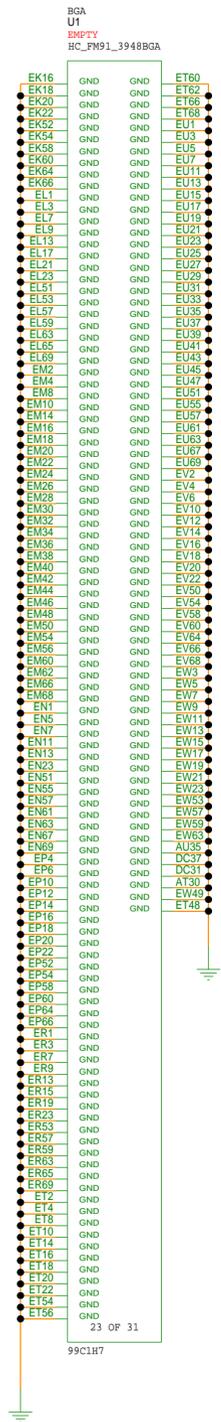
FPGA GND- I



Wed Mar 6 15:45:21 2024

DEPARTMENT	Intel Corporation	SIZE	C+	CODE	34649	DOCUMENT NUMBER	150-0330690-A2	REV	2.0
PGO	INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SCALE:				DO NOT SCALE DRAWING		SHEET	25 OF 105

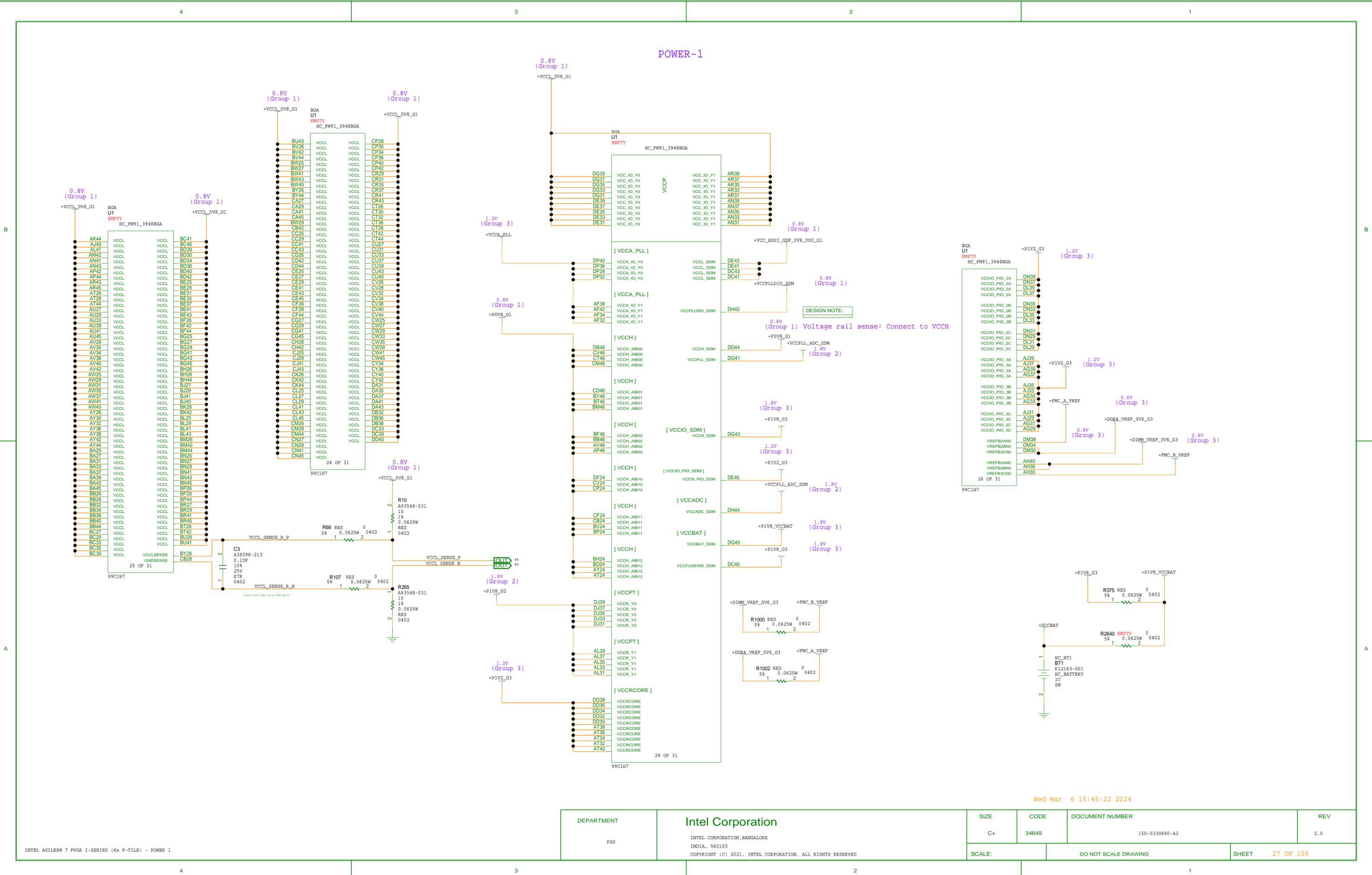
FPGA GND- II



**CAD NOTE:**  
Place these TP 's near to VR's Enable/PG/Vout TP's.

Wed Mar 6 15:45:22 2024

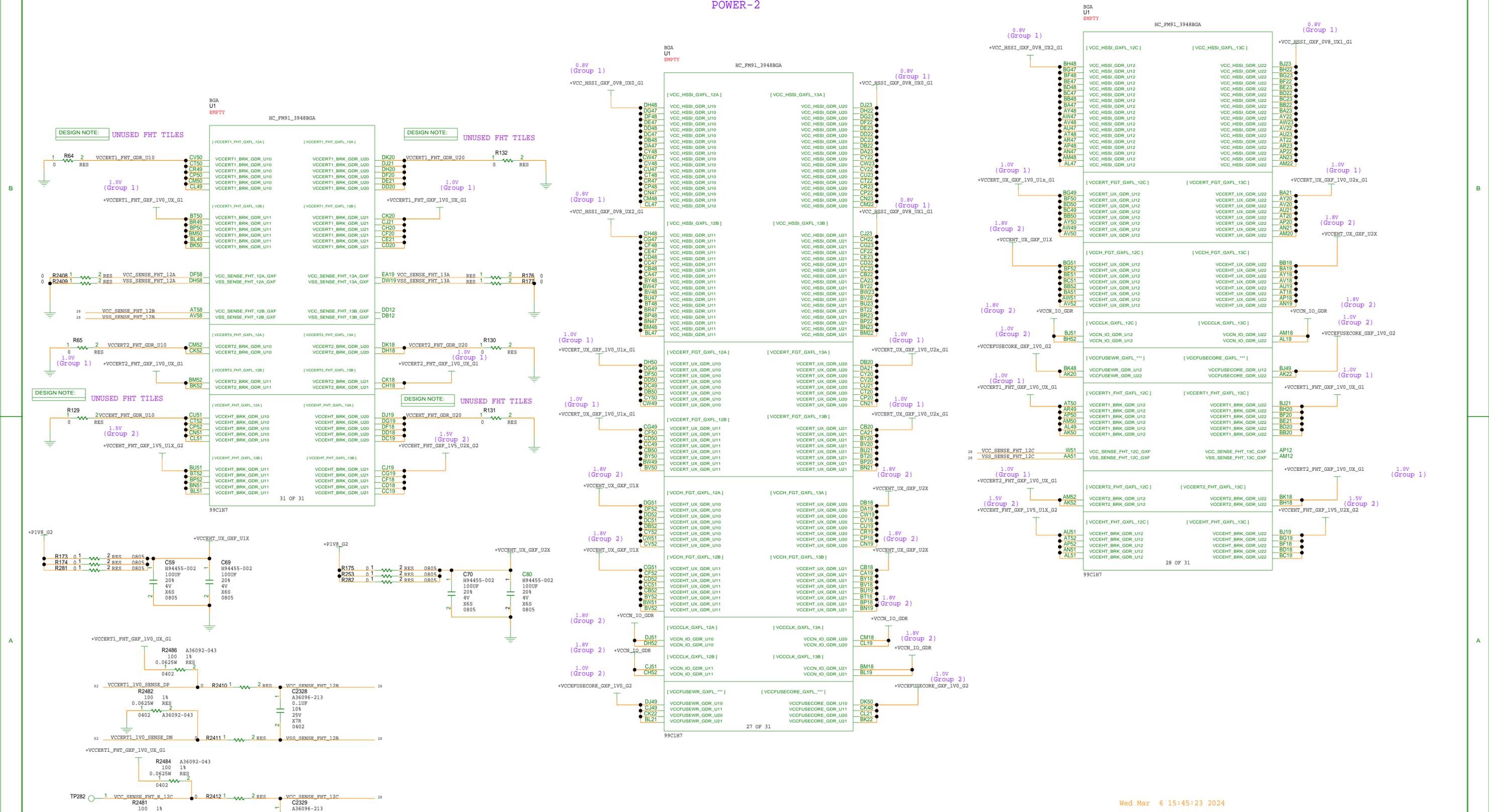
DEPARTMENT PSG	Intel Corporation INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330690-A2	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 26 OF 105	



Wed Mar 6 15:45:22 2024

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PGG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 27 OF 105	

### POWER-2



Wed Mar 6 15:45:23 2024

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PGG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 28 OF 105

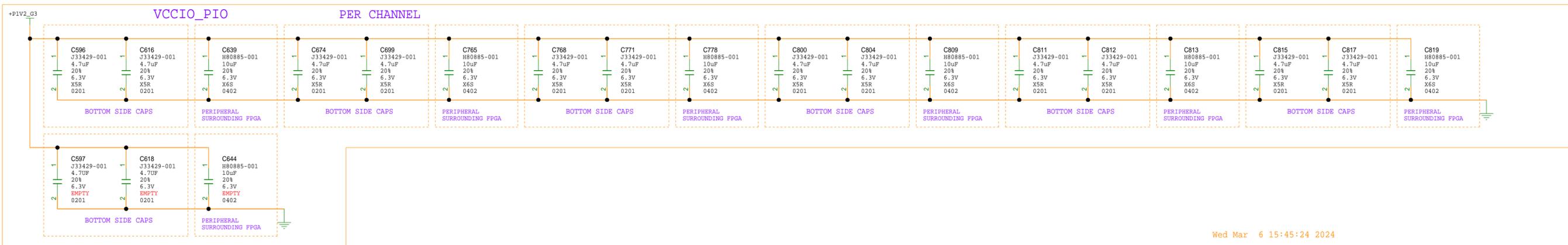
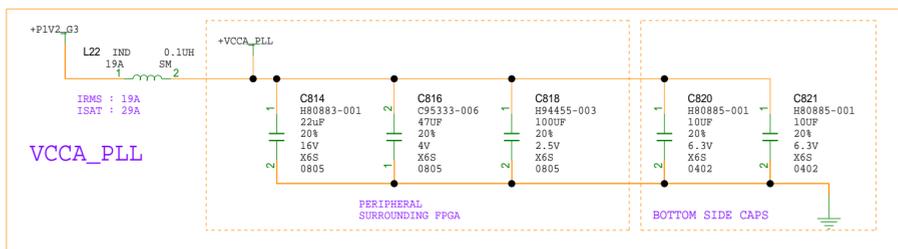
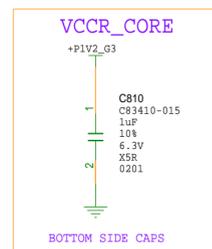
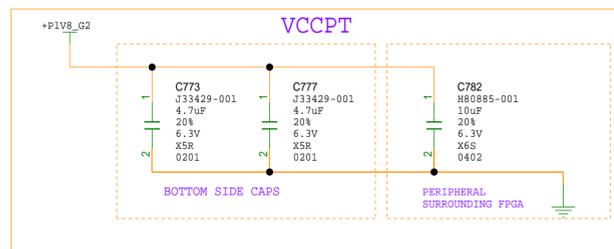
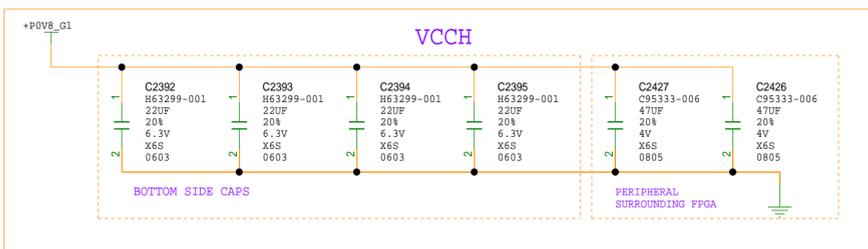
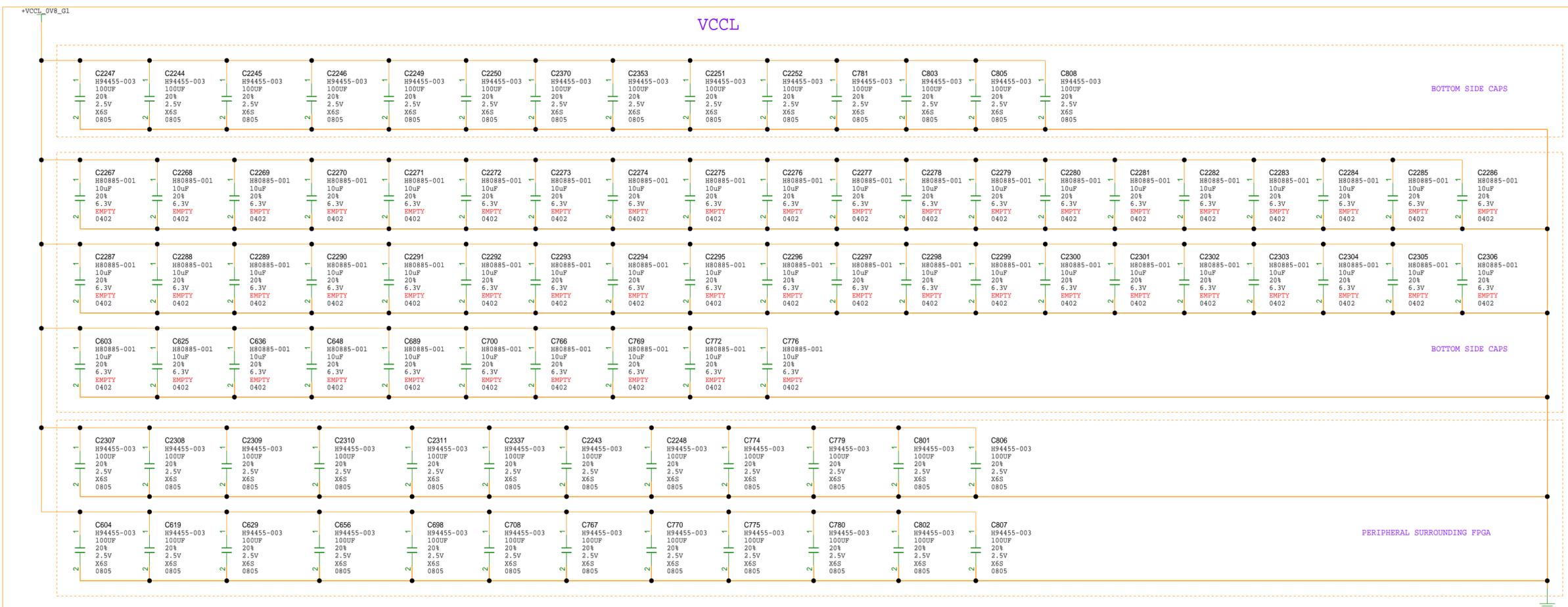
4

3

2

1

FPGA DECOUPLING - I



Wed Mar 6 15:45:24 2024

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 29 OF 105	

4

3

2

1

FPGA DECOUPLING - II



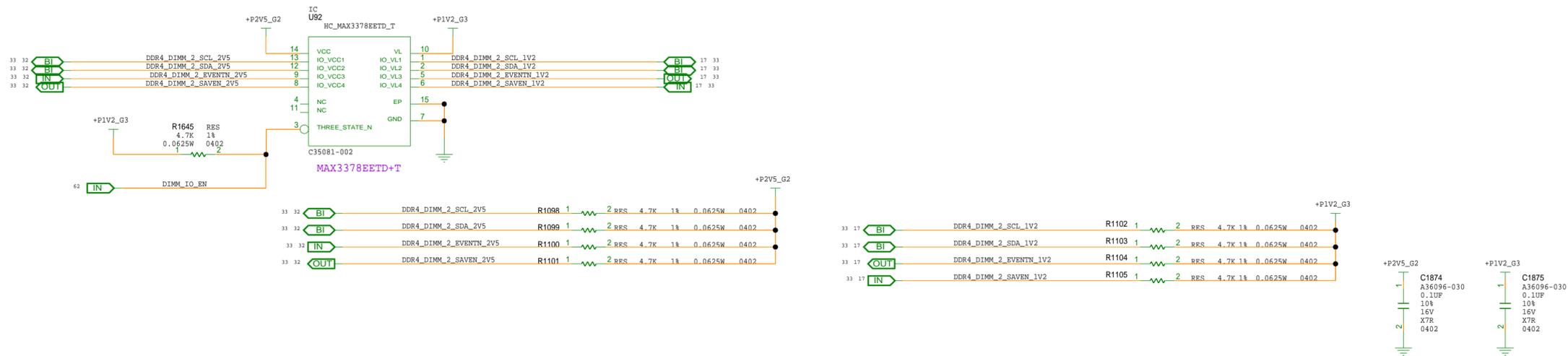
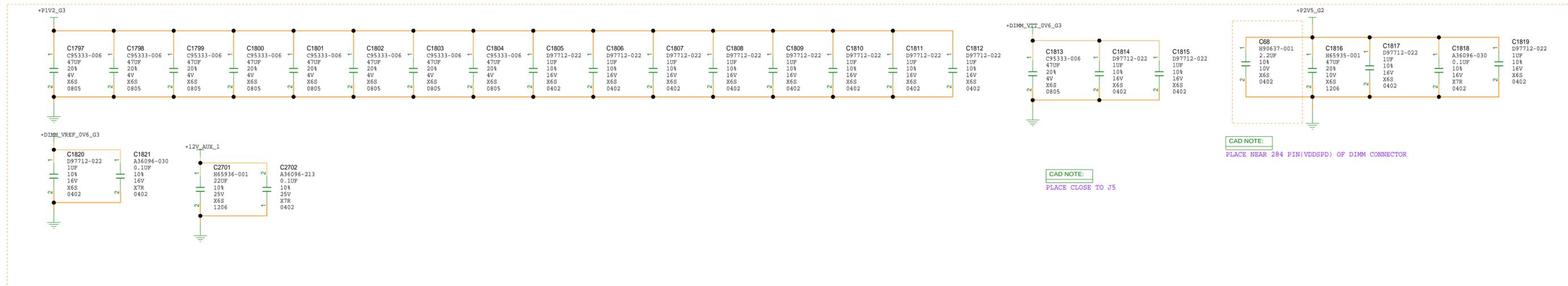
Wed Mar 6 15:45:24 2024

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 30 OF 105	



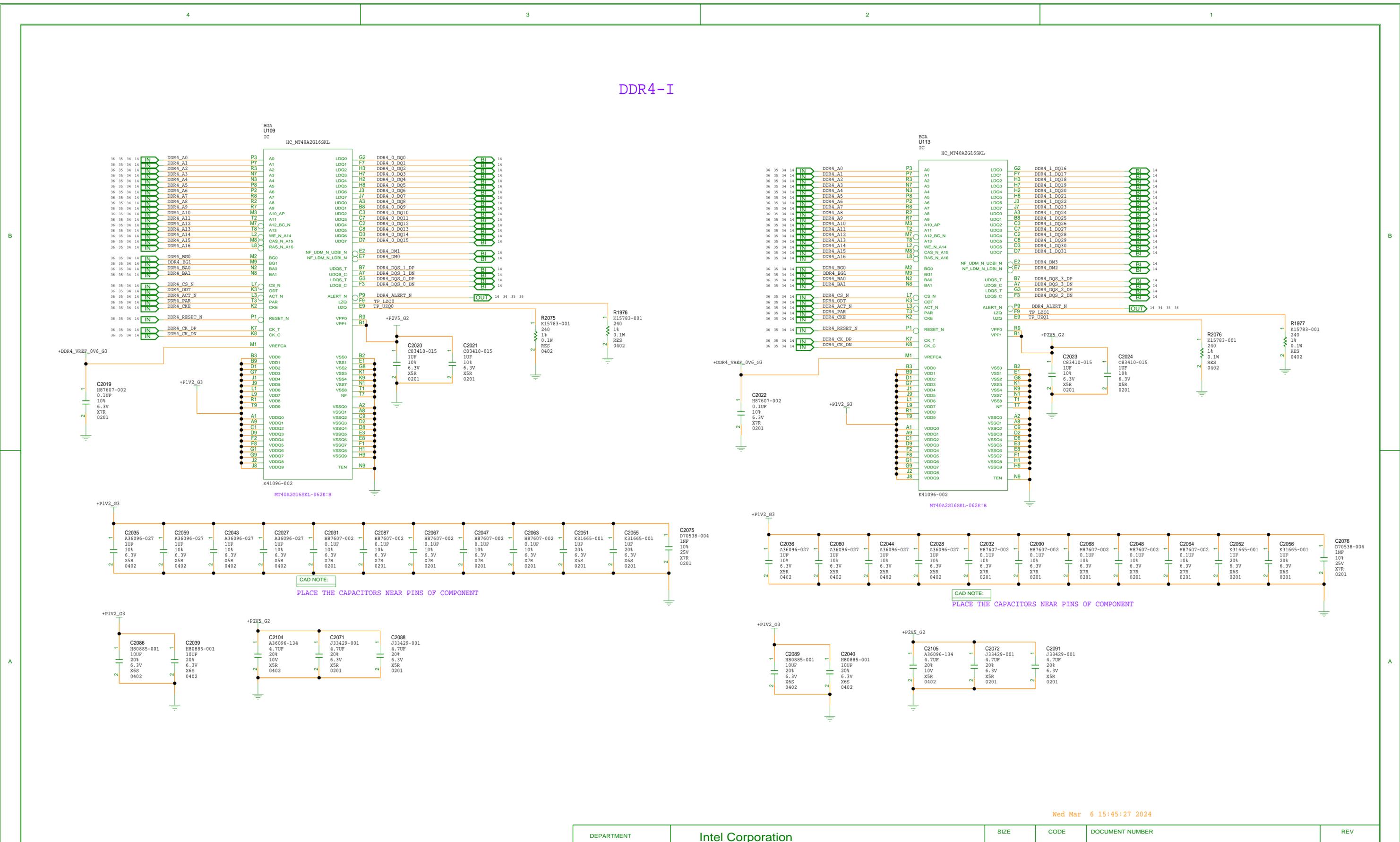


# 1DPC DIMM-FILTER AND LVL SHIFTER



Wed Mar 6 15:45:26 2024

# DDR4-I



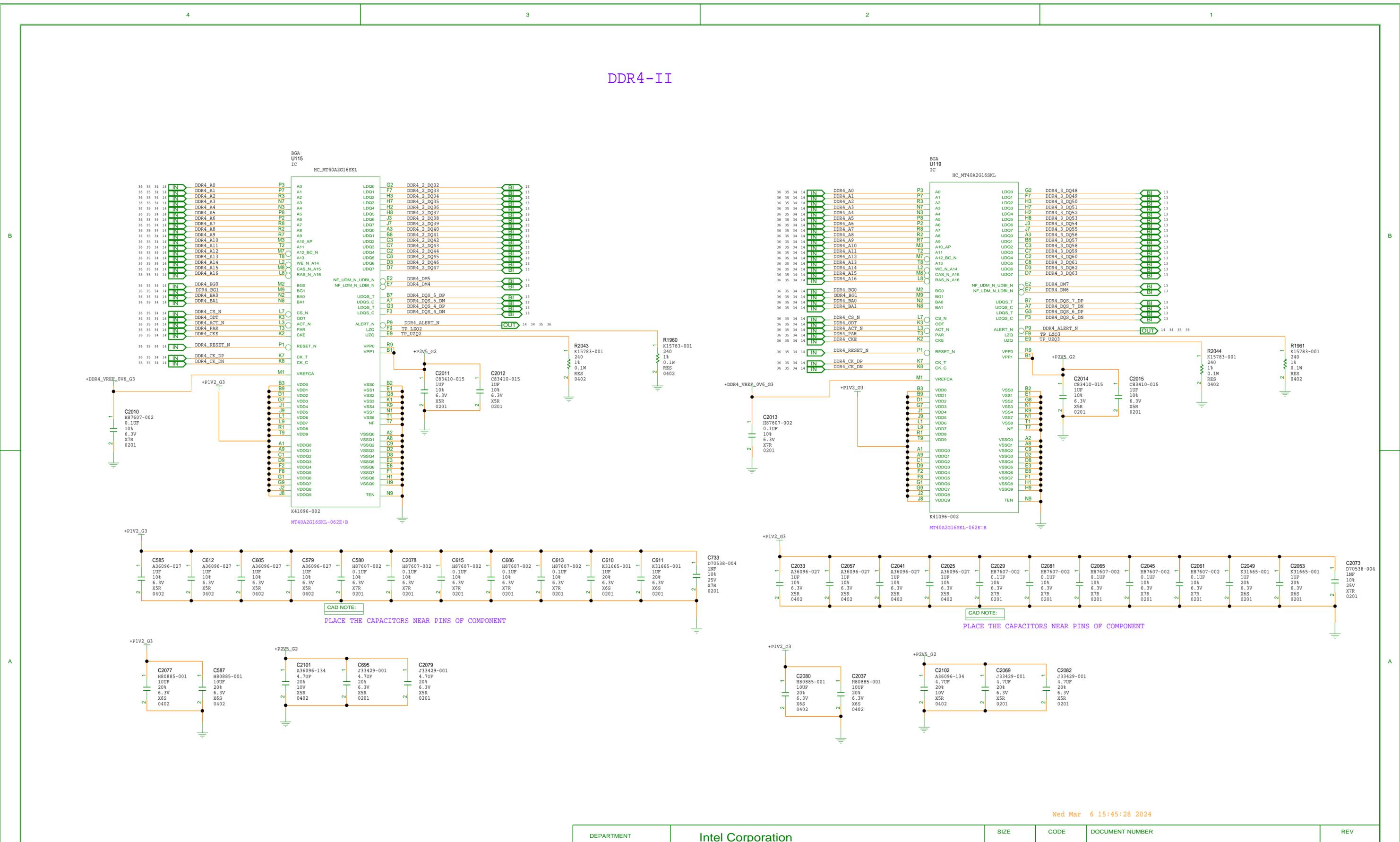
CAD NOTE: PLACE THE CAPACITORS NEAR PINS OF COMPONENT

CAD NOTE: PLACE THE CAPACITORS NEAR PINS OF COMPONENT

Wed Mar 6 15:45:27 2024

DEPARTMENT PSG	Intel Corporation INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330690-A2	REV 2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 34 OF 105

# DDR4-II



CAD NOTE:  
PLACE THE CAPACITORS NEAR PINS OF COMPONENT

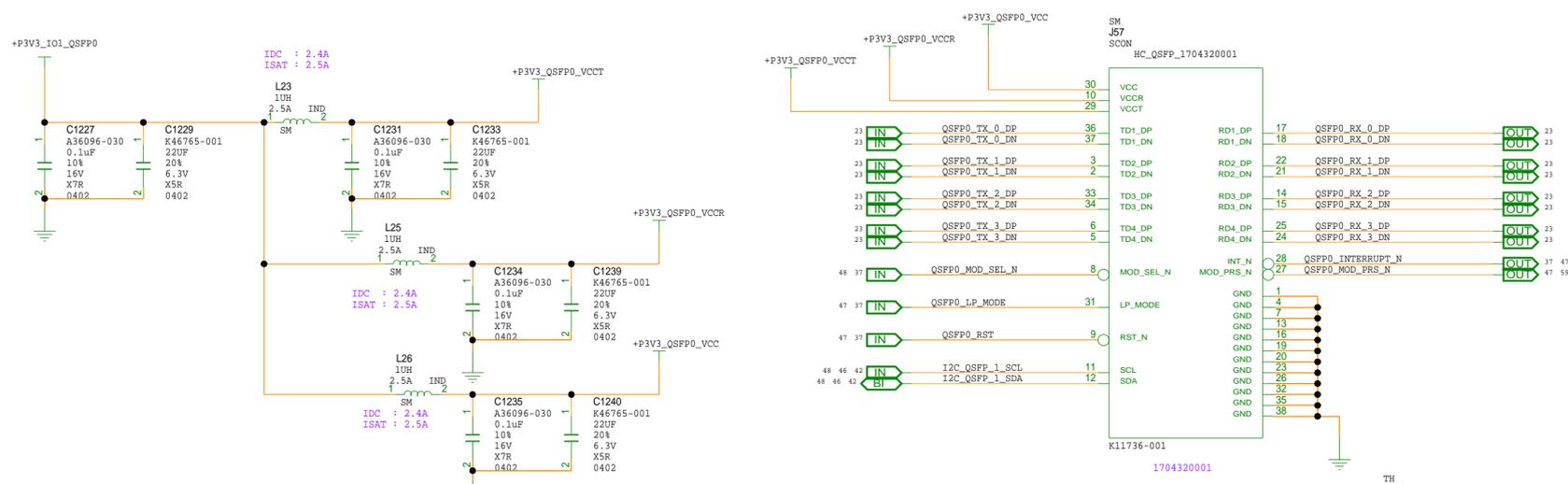
CAD NOTE:  
PLACE THE CAPACITORS NEAR PINS OF COMPONENT

Wed Mar 6 15:45:28 2024



### QSFP-0

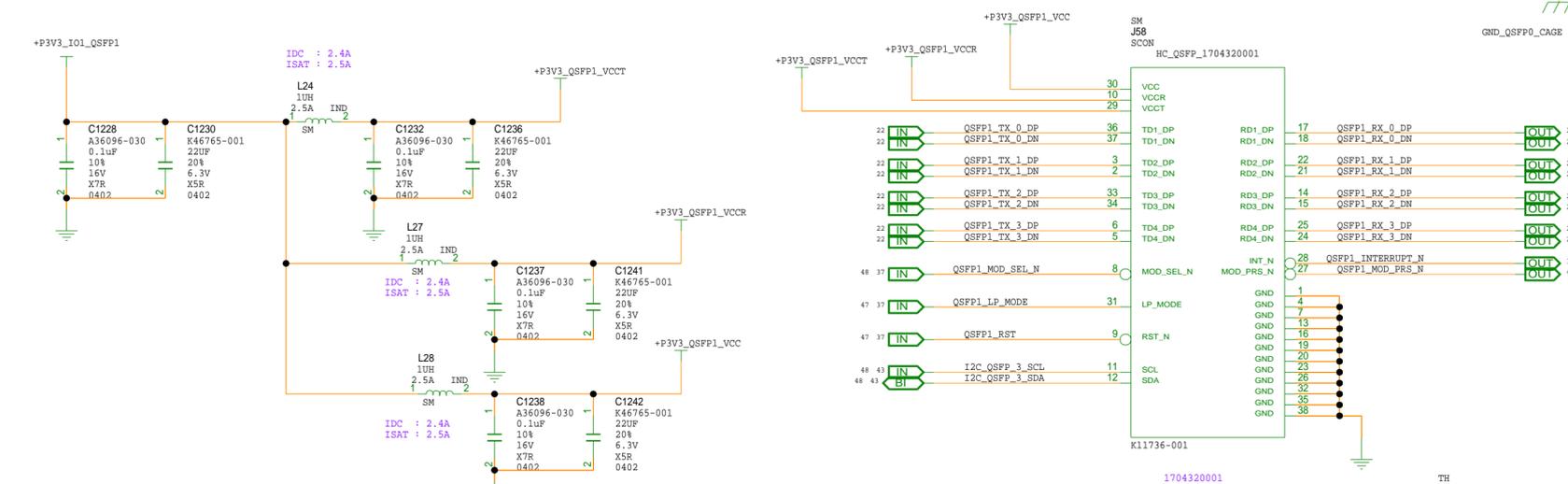
### 12B-BANK



I2C SLAVE ADDRESS: 50H

### QSFP-1

### 12C-BANK



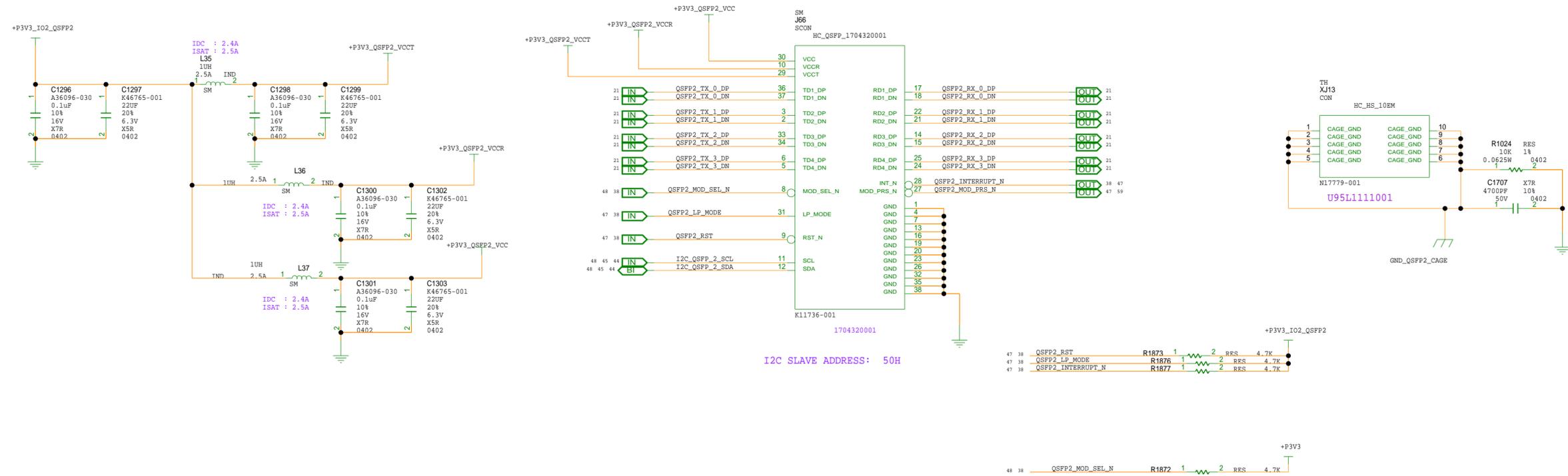
I2C SLAVE ADDRESS: 50H

Wed Mar 6 15:45:29 2024

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 37 OF 105	

# QSFP-2

13A-BANK

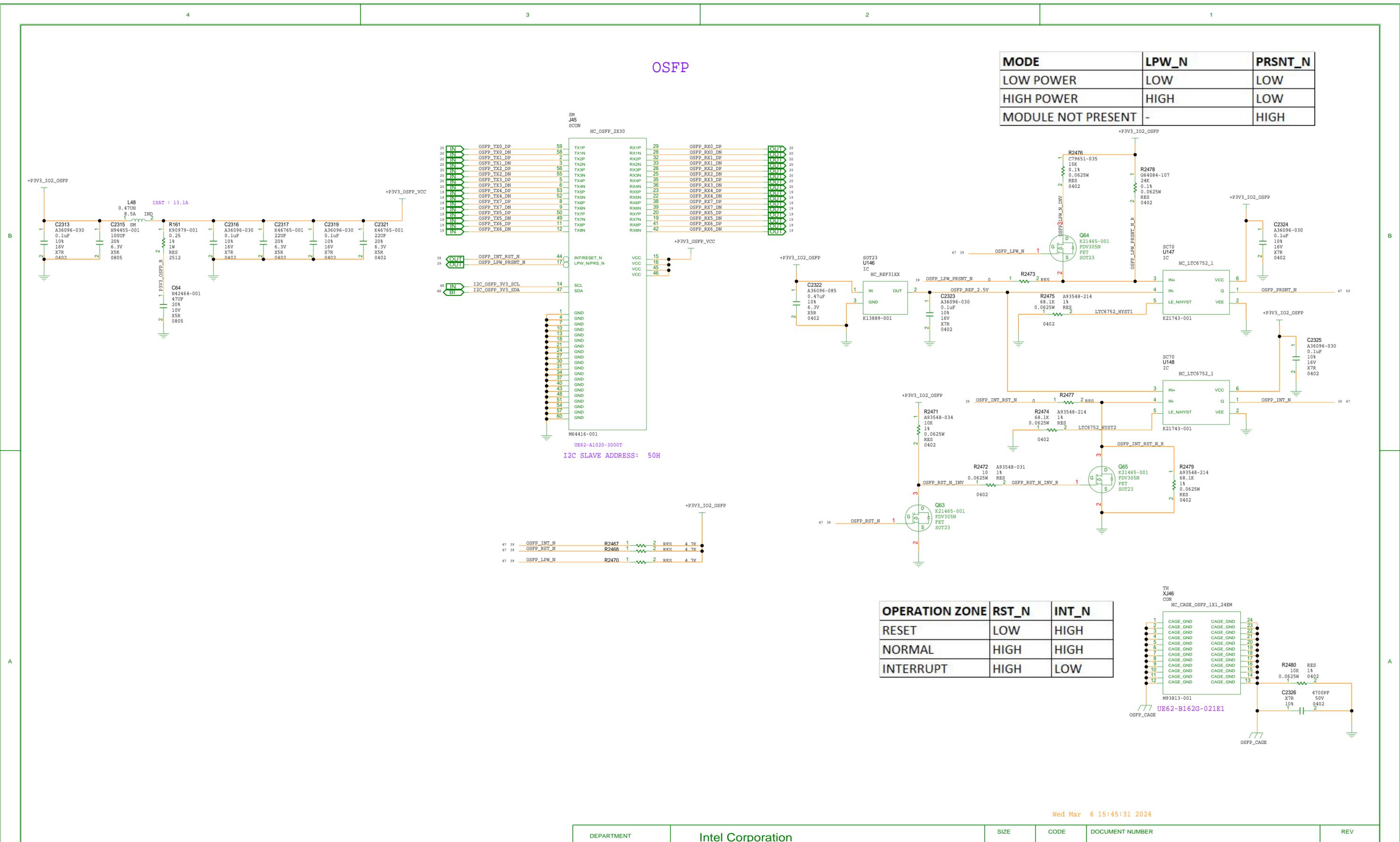


Wed Mar 6 15:45:30 2024

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 38 OF 105	

# OSFP

MODE	LPW_N	PRSNT_N
LOW POWER	LOW	LOW
HIGH POWER	HIGH	LOW
MODULE NOT PRESENT	-	HIGH



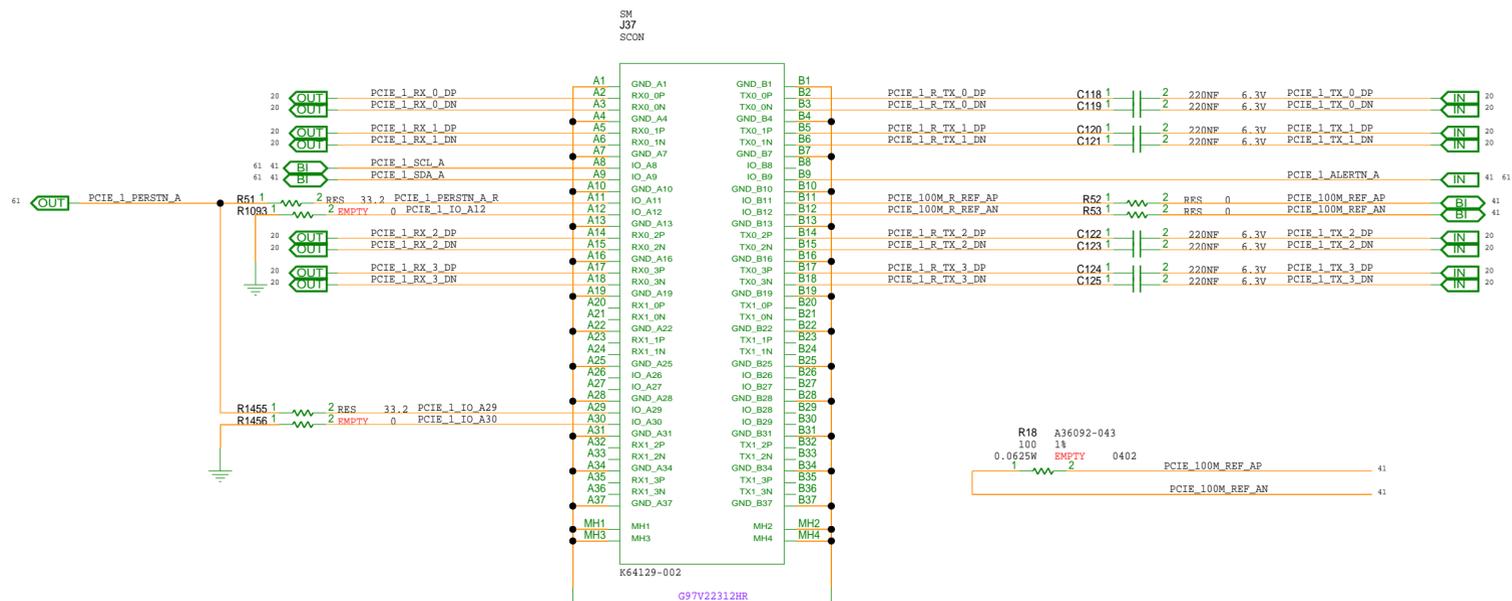
OPERATION ZONE	RST_N	INT_N
RESET	LOW	HIGH
NORMAL	HIGH	HIGH
INTERRUPT	HIGH	LOW

Wed Mar 6 15:45:31 2024

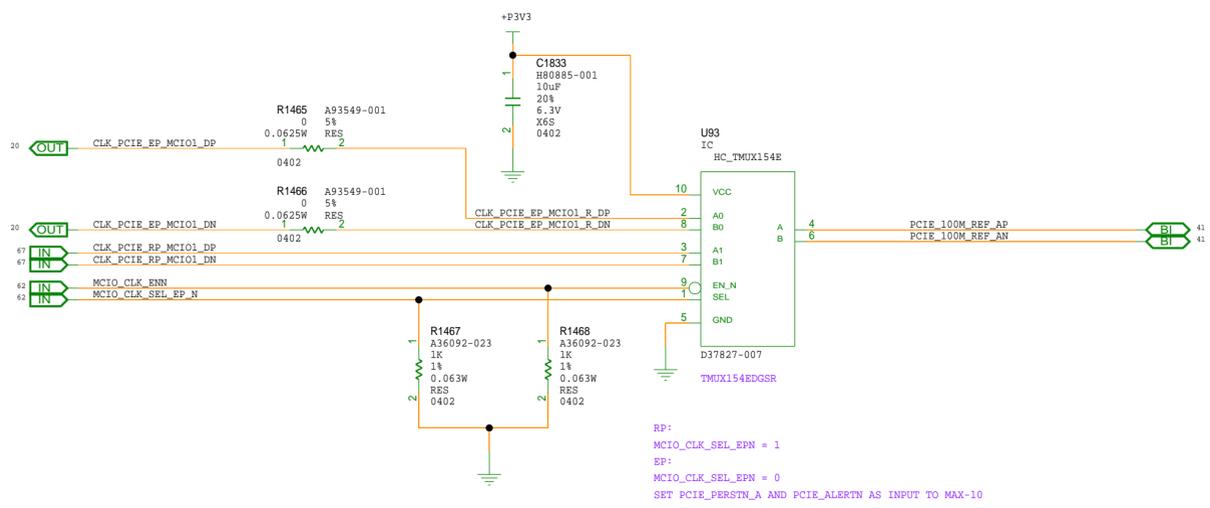
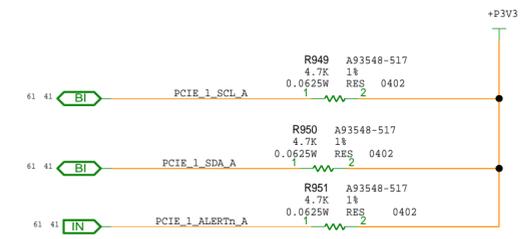
DEPARTMENT	Intel Corporation	SIZE	C+	CODE	34649	DOCUMENT NUMBER	150-0330690-A2	REV	2.0
UNKNOWN	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	SCALE:	DO NOT SCALE DRAWING			SHEET	39 OF 105		



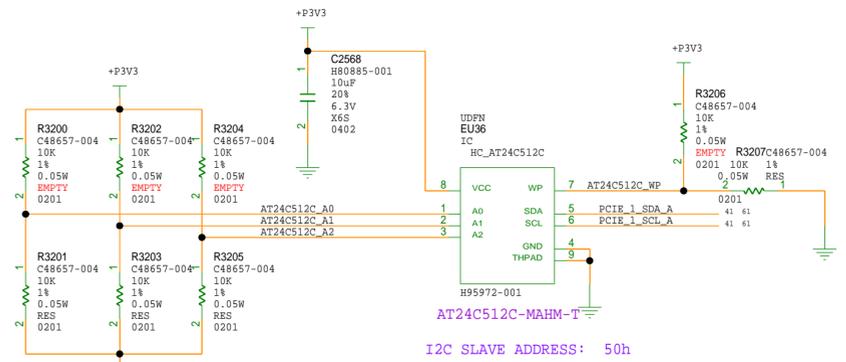
# MCIO



I2C SLAVE ADDRESS: 50H  
 DESIGN NOTE: WHEN MCIO IS MASTER, ADDRESS CONFLICT MAY OCCUR  
 SUPPORT MCIO 8X LS \* 2 TO PCIE GOLD FINGER CARD ASSEMBLY



RP:  
 MCIO\_CLK\_SEL\_EPN = 1  
 EP:  
 MCIO\_CLK\_SEL\_EPN = 0  
 SET PCIE\_PERSTN\_A AND PCIE\_ALERTN AS INPUT TO MAX-10



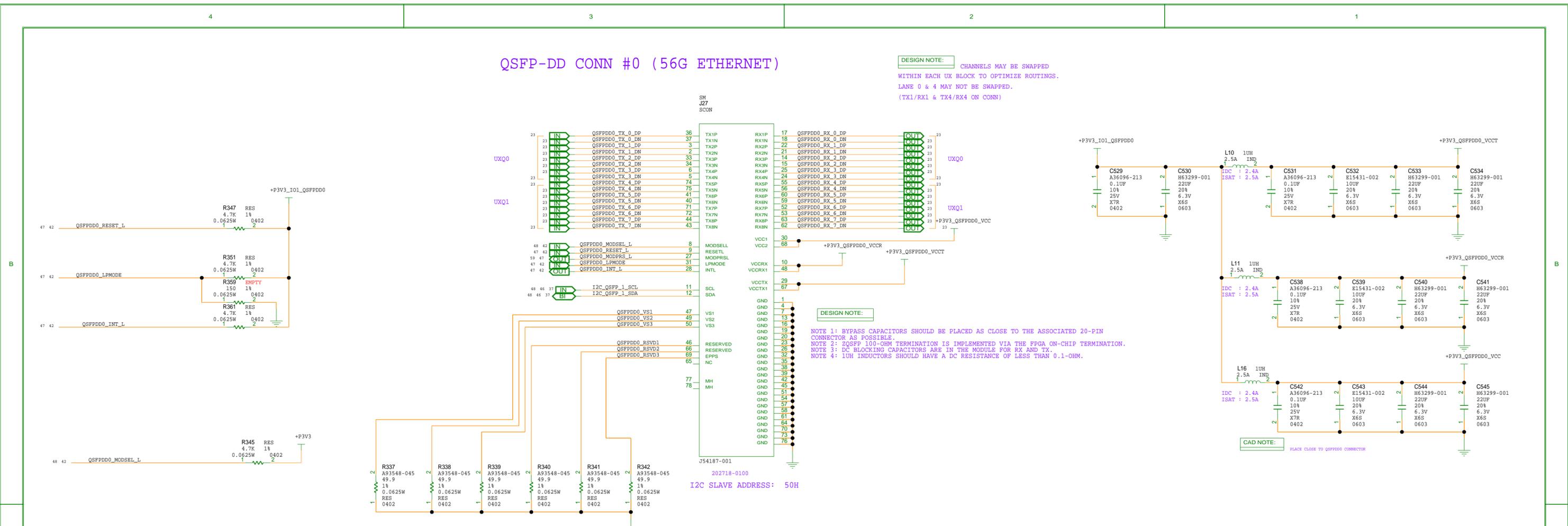
I2C SLAVE ADDRESS: 50h

Wed Mar 6 15:45:32 2024

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 41 OF 105	

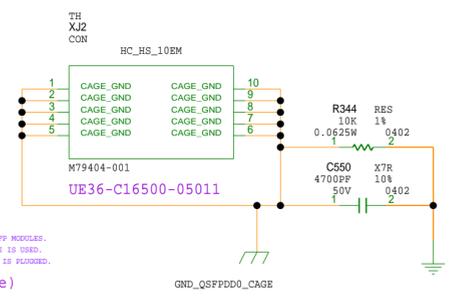
### QSFP-DD CONN #0 (56G ETHERNET)

**DESIGN NOTE:** CHANNELS MAY BE SWAPPED WITHIN EACH UX BLOCK TO OPTIMIZE ROUTINGS. LANE 0 & 4 MAY NOT BE SWAPPED. (TX1/RX1 & TX4/RX4 ON CONN)



**DESIGN NOTE:**  
 NOTE 1: BYPASS CAPACITORS SHOULD BE PLACED AS CLOSE TO THE ASSOCIATED 20-PIN CONNECTOR AS POSSIBLE.  
 NOTE 2: QSFP 100-OHM TERMINATION IS IMPLEMENTED VIA THE FPGA ON-CHIP TERMINATION.  
 NOTE 3: DC BLOCKING CAPACITORS ARE IN THE MODULE FOR RX AND TX.  
 NOTE 4: 1UH INDUCTORS SHOULD HAVE A DC RESISTANCE OF LESS THAN 0.1-OHM.

**CAD NOTE:** PLACE CLOSE TO QSFPDD CONNECTOR

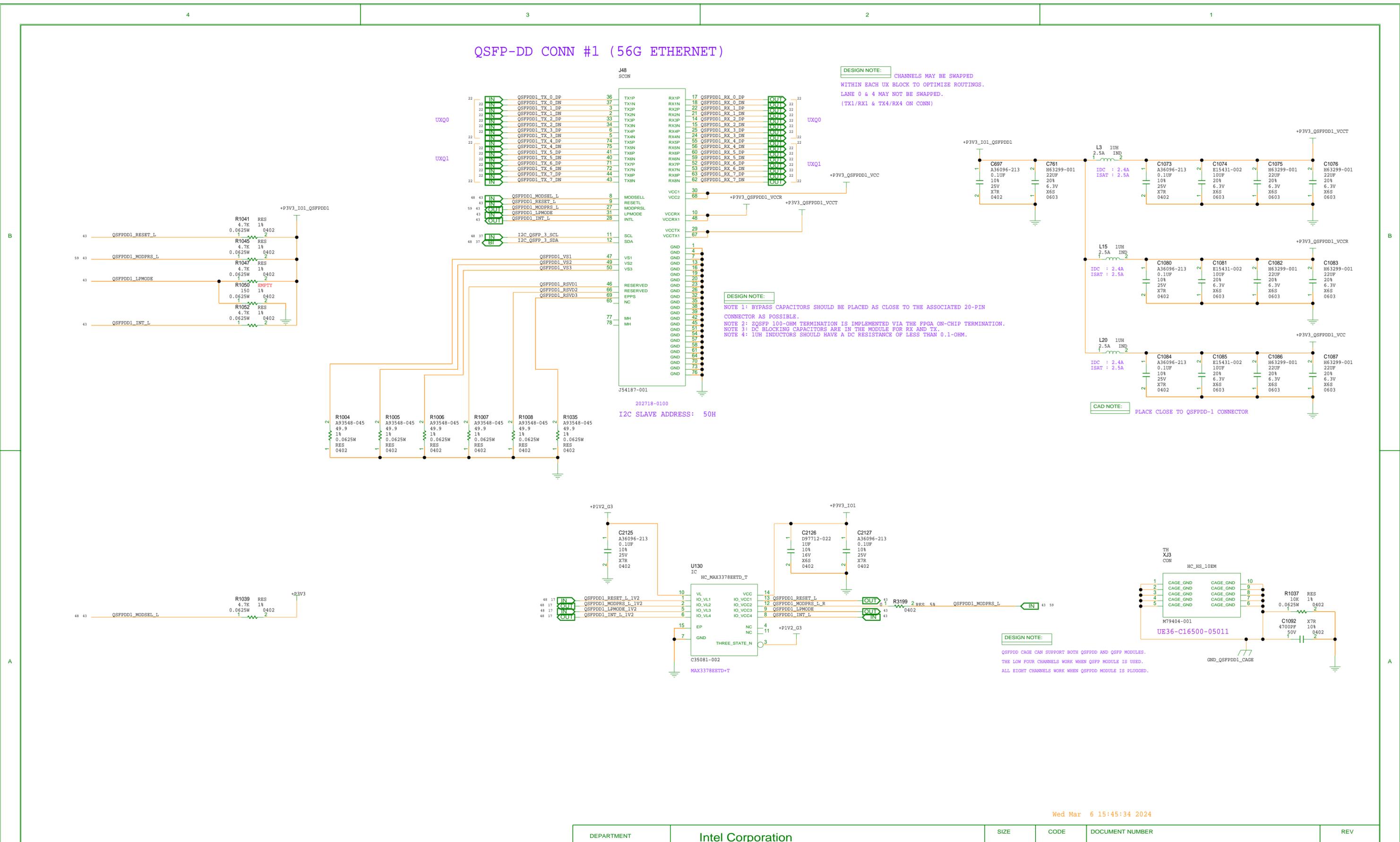


**DESIGN NOTE:**  
 QSFPDD CAGE CAN SUPPORT BOTH QSFPDD AND QSFP MODULES. THE LOW FOUR CHANNELS WORK WHEN QSFP MODULE IS USED. ALL EIGHT CHANNELS WORK WHEN QSFPDD MODULE IS PLACED. K23336-002 (Molex cage) CAN BE USED AS ALTERNATE CAGE.

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DEPARTMENT PSG	Intel Corporation INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330690-A2	REV 2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 42 OF 105

### QSFP-DD CONN #1 (56G ETHERNET)



DESIGN NOTE:

CHANNELS MAY BE SWAPPED WITHIN EACH UX BLOCK TO OPTIMIZE ROUTINGS. LANE 0 & 4 MAY NOT BE SWAPPED. (TX1/RX1 & TX4/RX4 ON CONN)

DESIGN NOTE:

NOTE 1: BYPASS CAPACITORS SHOULD BE PLACED AS CLOSE TO THE ASSOCIATED 20-PIN CONNECTOR AS POSSIBLE.  
 NOTE 2: QSFP 100-OHM TERMINATION IS IMPLEMENTED VIA THE FPGA ON-CHIP TERMINATION.  
 NOTE 3: DC BLOCKING CAPACITORS ARE IN THE MODULE FOR RX AND TX.  
 NOTE 4: 1UH INDUCTORS SHOULD HAVE A DC RESISTANCE OF LESS THAN 0.1-OHM.

CAD NOTE:

PLACE CLOSE TO QSFPDD-1 CONNECTOR

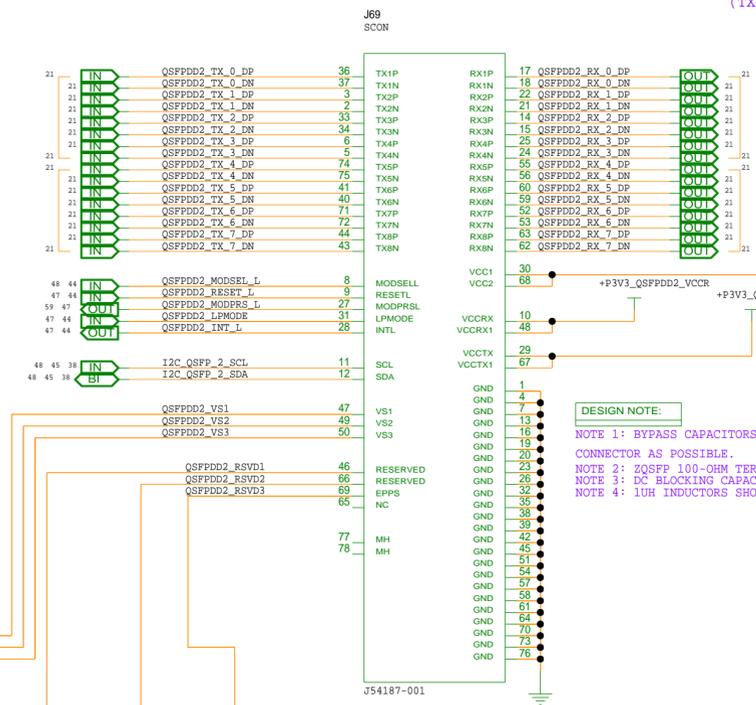
DESIGN NOTE:

QSFPDD CAGE CAN SUPPORT BOTH QSFPDD AND QSFP MODULES. THE LOW FOUR CHANNELS WORK WHEN QSFP MODULE IS USED. ALL RIGHT CHANNELS WORK WHEN QSFPDD MODULE IS PLUGGED.

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### QSFP-DD CONN #2 (56G ETHERNET)

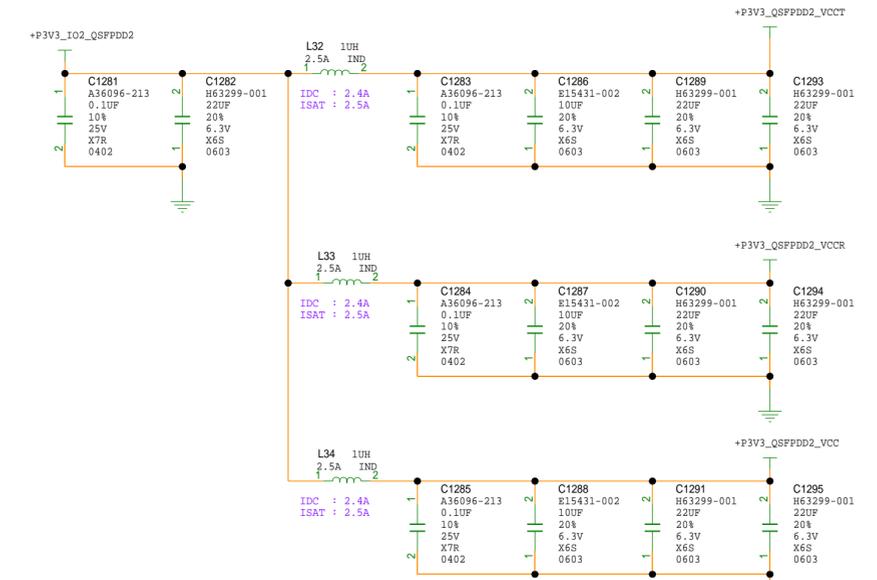
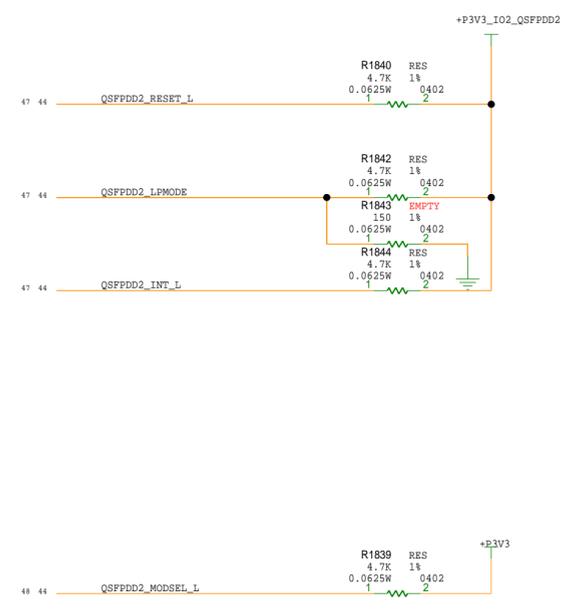
**DESIGN NOTE:** CHANNELS MAY BE SWAPPED WITHIN EACH UX BLOCK TO OPTIMIZE ROUTINGS. LANE 0 & 4 MAY NOT BE SWAPPED. (TX1/RX1 & TX4/RX4 ON CONN)



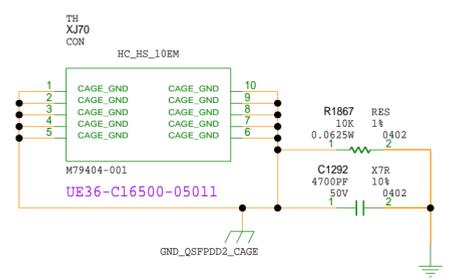
**DESIGN NOTE:**  
 NOTE 1: BYPASS CAPACITORS SHOULD BE PLACED AS CLOSE TO THE ASSOCIATED 20-PIN CONNECTOR AS POSSIBLE.  
 NOTE 2: QSFP 100-OHM TERMINATION IS IMPLEMENTED VIA THE FPGA ON-CHIP TERMINATION.  
 NOTE 3: DC BLOCKING CAPACITORS ARE IN THE MODULE FOR RX AND TX.  
 NOTE 4: 1UH INDUCTORS SHOULD HAVE A DC RESISTANCE OF LESS THAN 0.1-OHM.

202718-0100  
 I2C SLAVE ADDRESS: 50H

**DESIGN NOTE:**  
 QSFPDD CAGE CAN SUPPORT BOTH QSFPDD AND QSFP MODULES.  
 THE LOW FOUR CHANNELS WORK WHEN QSFP MODULE IS USED.  
 ALL EIGHT CHANNELS WORK WHEN QSFPDD MODULE IS PLUGGED.



**CAD NOTE:**  
 PLACE CLOSE TO QSFPDD-2 CONNECTOR

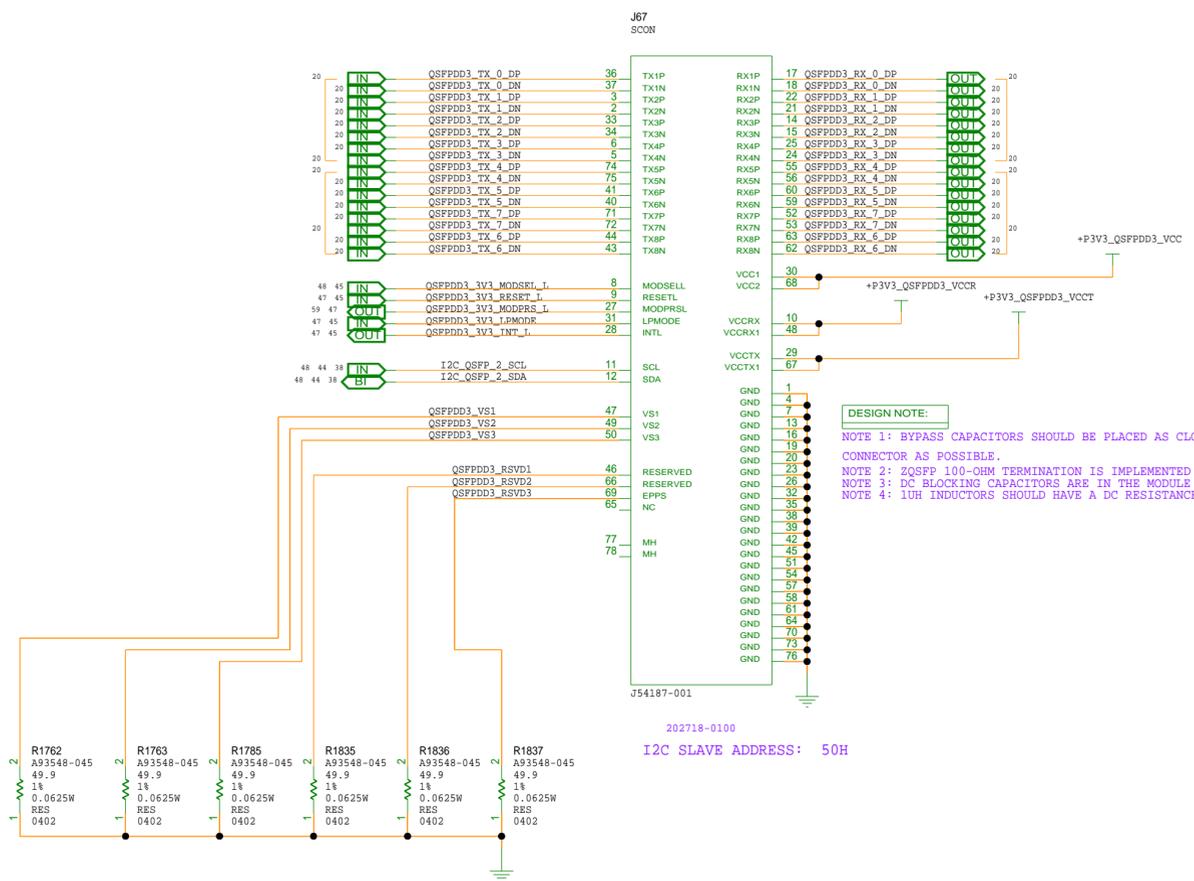


Wed Mar 6 15:45:34 2024

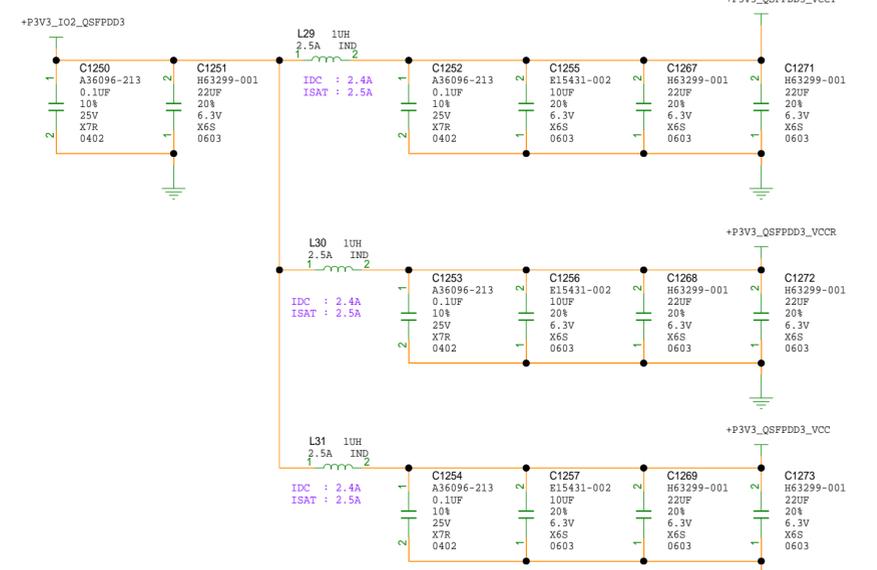
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 44 OF 105	

### QSFP-DD CONN #3 (56G ETHERNET)

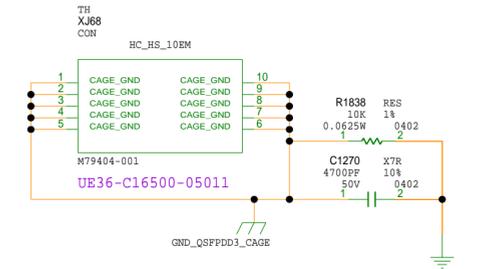
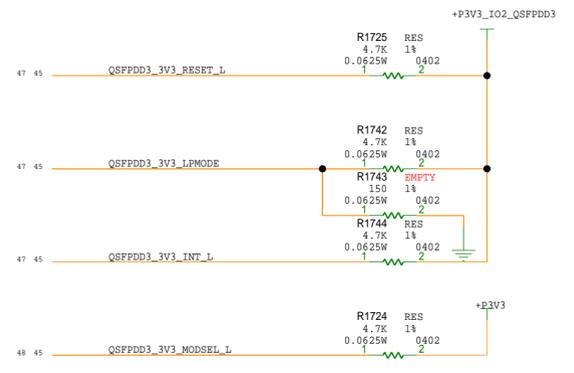
**DESIGN NOTE:**  
 CHANNELS MAY BE SWAPPED WITHIN EACH UX BLOCK TO OPTIMIZE ROUTINGS.  
 LANE 0 & 4 MAY NOT BE SWAPPED.  
 (TX1/RX1 & TX4/RX4 ON CONN)



**DESIGN NOTE:**  
 NOTE 1: BYPASS CAPACITORS SHOULD BE PLACED AS CLOSE TO THE ASSOCIATED 20-PIN CONNECTOR AS POSSIBLE.  
 NOTE 2: QSFP 100-OHM TERMINATION IS IMPLEMENTED VIA THE FPGA ON-CHIP TERMINATION.  
 NOTE 3: DC BLOCKING CAPACITORS ARE IN THE MODULE FOR RX AND TX.  
 NOTE 4: 1UH INDUCTORS SHOULD HAVE A DC RESISTANCE OF LESS THAN 0.1-OHM.



**CAD NOTE:**  
 PLACE CLOSE TO QSFPDD-3 CONNECTOR



**DESIGN NOTE:**  
 QSFPDD CAGE CAN SUPPORT BOTH QSFPDD AND QSFP MODULES.  
 THE LOW FOUR CHANNELS WORK WHEN QSFP MODULE IS USED.  
 ALL EIGHT CHANNELS WORK WHEN QSFPDD MODULE IS PLUGGED.

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PGG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:	DO NOT SCALE DRAWING	SHEET		45 OF 105	

### QSFP-DD-800 CONN (112G ETHERNET)

**DESIGN NOTE:**

CHANNELS MAY BE SWAPPED  
WITHIN EACH BK BLOCK TO OPTIMIZE ROUTINGS.  
SWAP BOTH TX & RX TOGETHER.

**DESIGN NOTE:**

NOTE 4: 1UH INDUCTORS SHOULD HAVE A DC RESISTANCE OF LESS THAN 0.1-OHM.  
NOTE 2: ZQSFP 100-OHM TERMINATION IS IMPLEMENTED VIA THE FPGA ON-CHIP TERMINATION.  
NOTE 1: BYPASS CAPACITORS SHOULD BE PLACED AS CLOSE TO THE ASSOCIATED 20-PIN CONNECTOR AS POSSIBLE.  
NOTE 3: DC BLOCKING CAPACITORS ARE IN THE MODULE FOR RX AND TX.

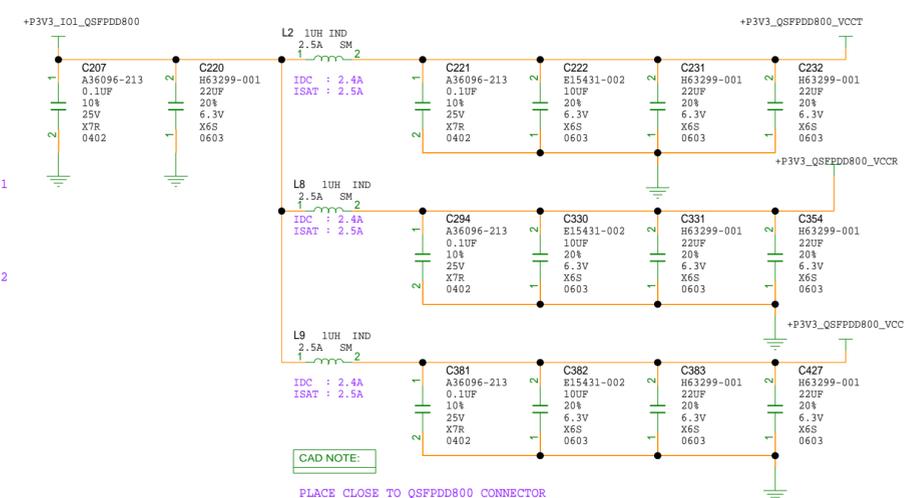
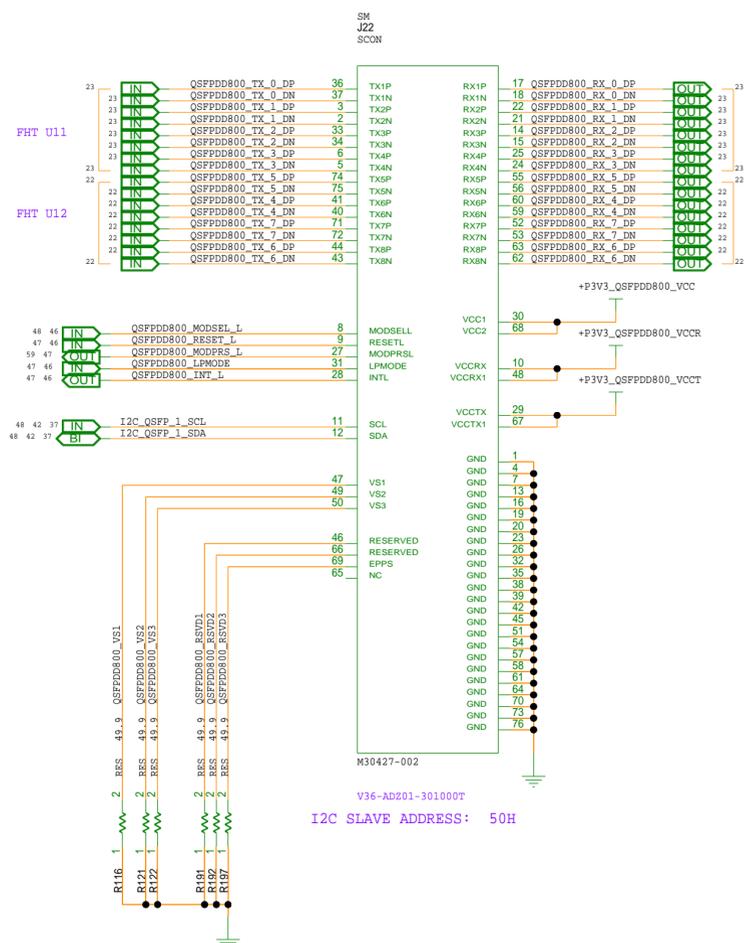
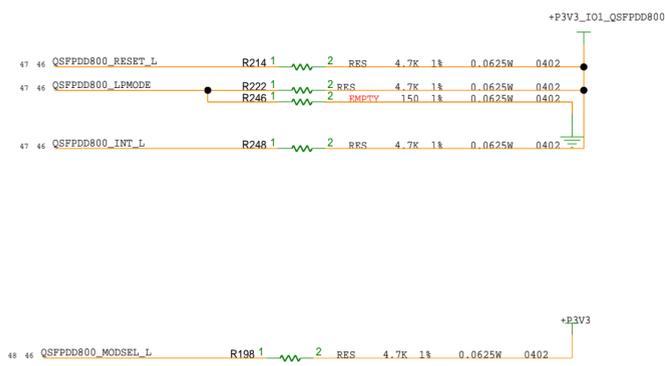
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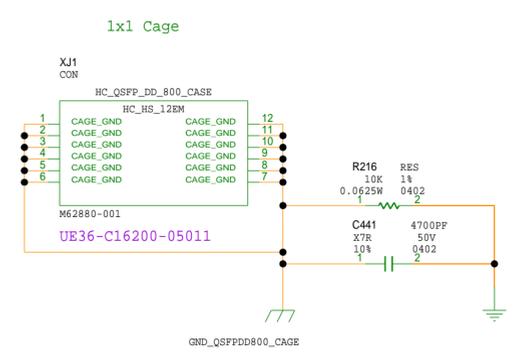
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**CAD NOTE:**

PLACE CLOSE TO QSFPDD800 CONNECTOR



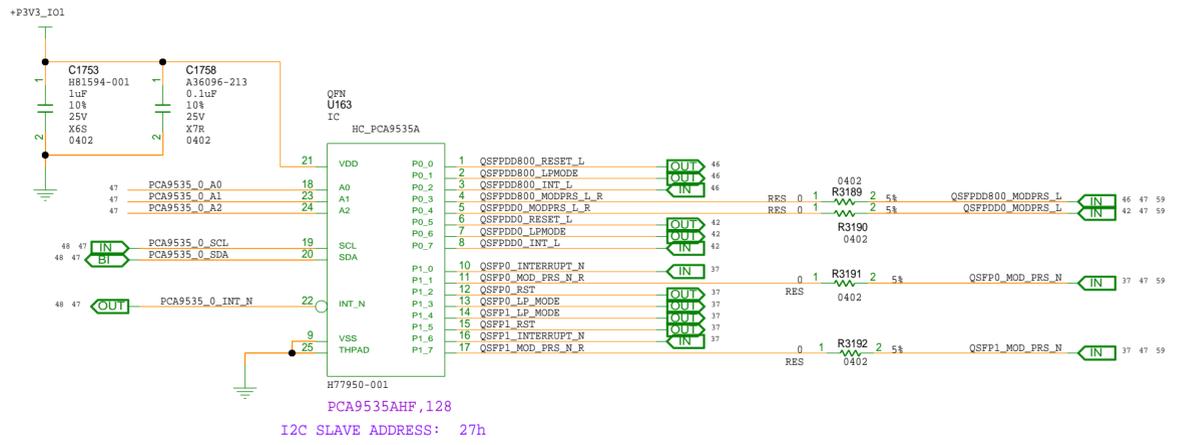
V36-ADZ01-301000T  
I2C SLAVE ADDRESS: 50H

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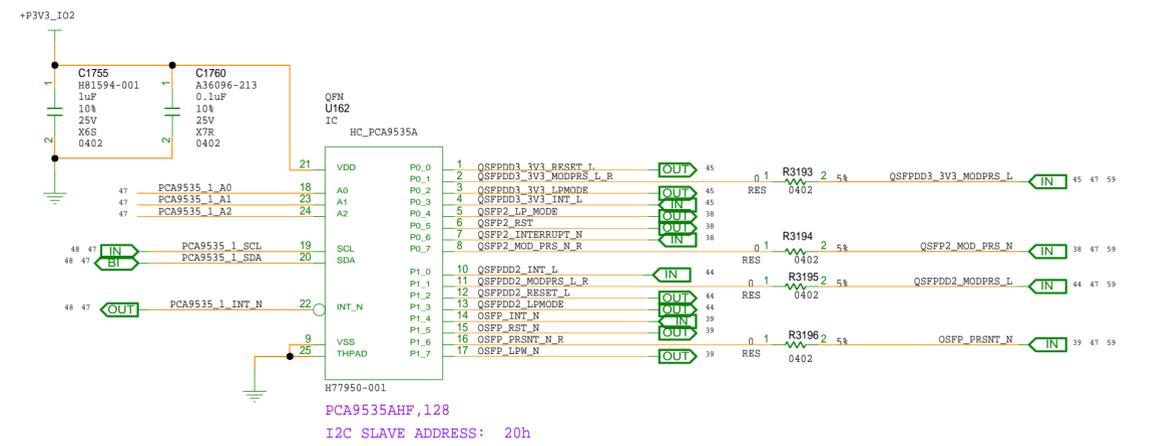
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 46 OF 105

4 3 2 1

### IO EXPANDER -0



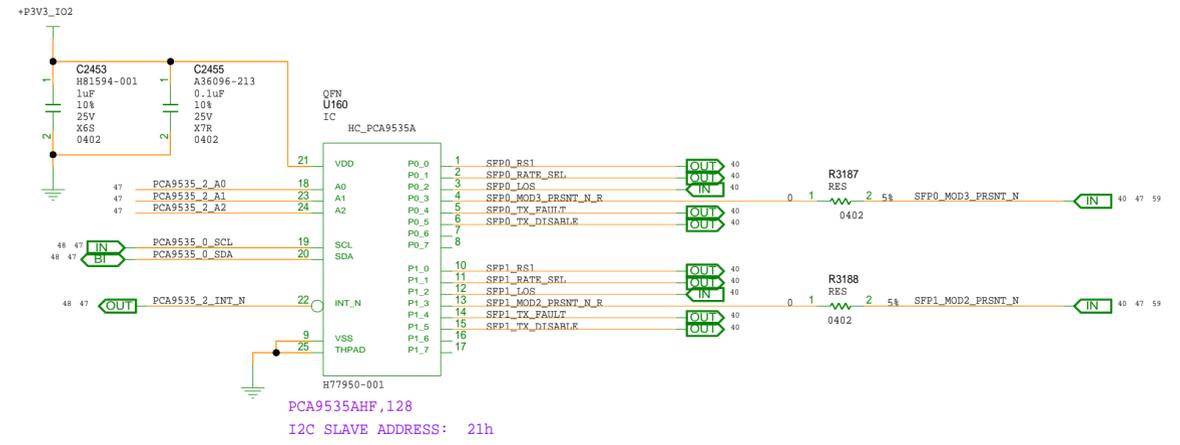
### IO EXPANDER -1



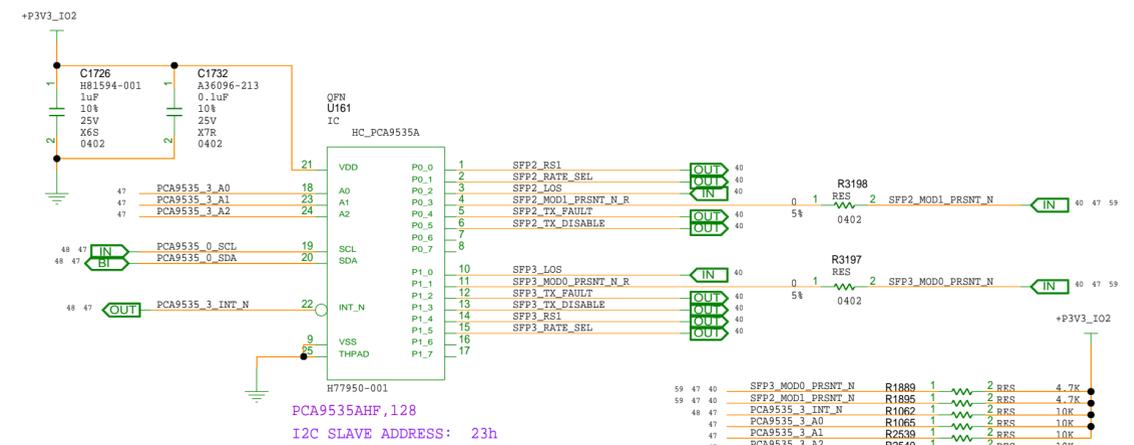
#### IO EXPANDER CONNECTION AND PLACEMENT DETAILS

CONNECTOR	IO EXPANDER	ADDRESS	I2C BUS	LAYOUT PLACEMENT
QSFDD800	IO EXPANDER 0	0X27H	PCA9535_0	LEFT
QSFP0	IO EXPANDER 0	0X27H	PCA9535_0	LEFT
QSFP1	IO EXPANDER 0	0X27H	PCA9535_0	LEFT
QSFDD0	IO EXPANDER 0	0X27H	PCA9535_0	LEFT
QSF2	IO EXPANDER 1	0X20H	PCA9535_1	RIGHT
QSFDD2	IO EXPANDER 1	0X20H	PCA9535_1	RIGHT
QSFP	IO EXPANDER 2	0X21H	PCA9535_0	LEFT
SFP1	IO EXPANDER 3	0X21H	PCA9535_0	LEFT
SFP2	IO EXPANDER 3	0X23H	PCA9535_0	LEFT
SFP3	IO EXPANDER 3	0X23H	PCA9535_0	LEFT

### IO EXPANDER -2



### IO EXPANDER-3



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PSG	INTEL CORPORATION,BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 47 OF 105	



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PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	
LOAD CURRENT	5.6A
FREQUENCY	
RIPPLE_VOLTAGE	

DESIGN NOTE:

Rsense: 7mohm  
Itrip(min): 5.65A  
Itrip(Nom): 7.1A  
Pdis: 360mW

DESIGN NOTE:

ENABLE ON THRESHOLD  
1.4V

DESIGN NOTE:

Rsense: 7mohm  
Itrip(min): 5.65A  
Itrip(Nom): 7.1A  
Pdis: 360mW

DESIGN NOTE:

ENABLE ON THRESHOLD  
1.4V

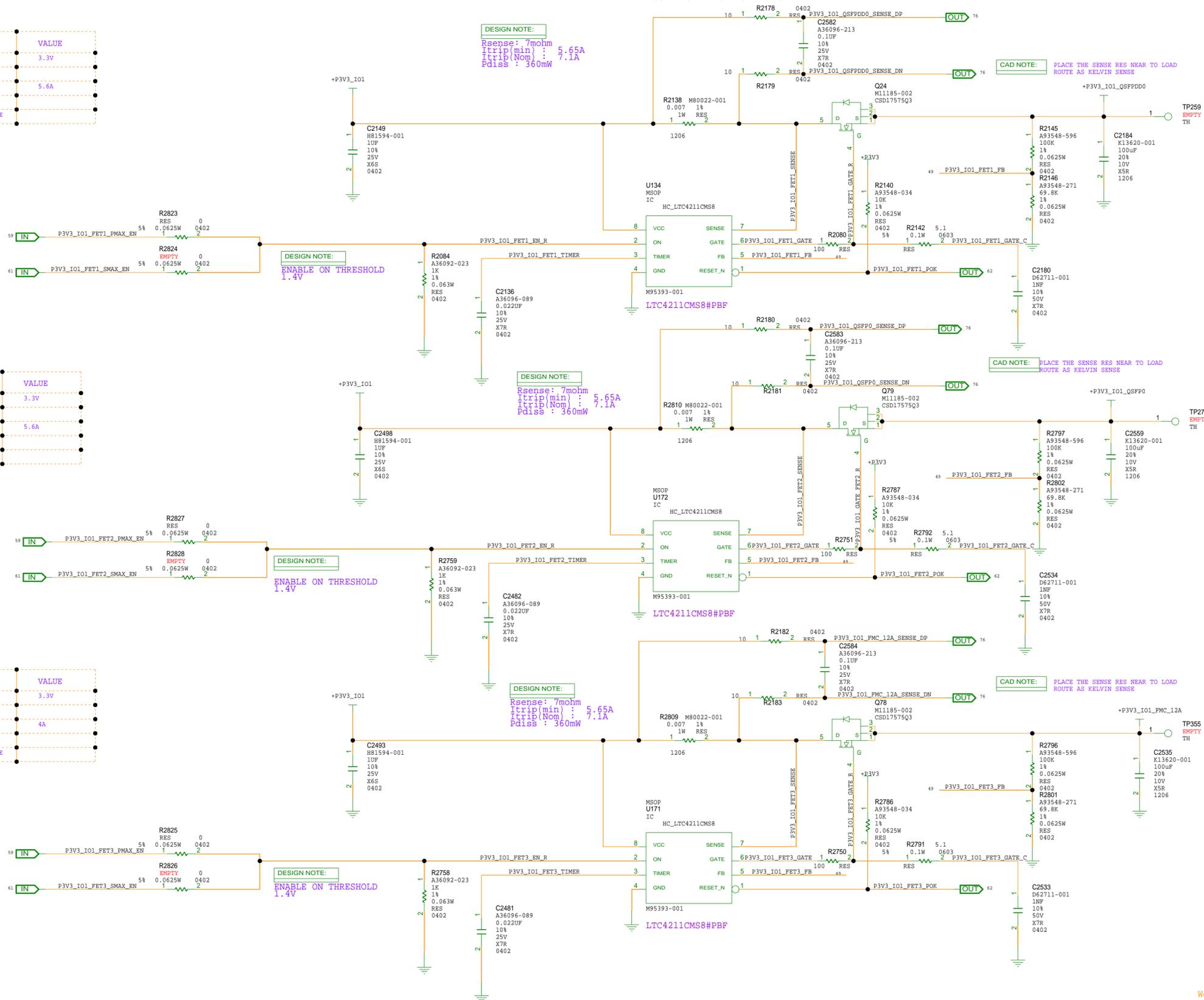
DESIGN NOTE:

Rsense: 7mohm  
Itrip(min): 5.65A  
Itrip(Nom): 7.1A  
Pdis: 360mW

DESIGN NOTE:

ENABLE ON THRESHOLD  
1.4V

CONN POWER LOAD SWITCHES-1



CAD NOTE: PLACE THE SENSE RES NEAR TO LOAD ROUTE AS KELVIN SENSE

CAD NOTE: PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB. AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

FET_PARAMETER	VALUE
VGS	±20 V
ID	60 A

CAD NOTE: PLACE THE SENSE RES NEAR TO LOAD ROUTE AS KELVIN SENSE

CAD NOTE: PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB. AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

FET_PARAMETER	VALUE
VGS	±20 V
ID	60 A

CAD NOTE: PLACE THE SENSE RES NEAR TO LOAD ROUTE AS KELVIN SENSE

CAD NOTE: PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB. AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

FET_PARAMETER	VALUE
VGS	±20 V
ID	60 A

Wed Mar 6 15:45:37 2024

DEPARTMENT	Intel Corporation	SIZE	C+	CODE	34649	DOCUMENT NUMBER	150-0330690-A2	REV	2.0
UNKNOWN	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	SCALE:		DO NOT SCALE DRAWING			SHEET	49 OF 105	

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PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	
LOAD CURRENT	5.6A
FREQUENCY	
RIPPLE_VOLTAGE	

DESIGN NOTE:  
 Rsense: 7mohm  
 Itrip(min) : 5.65A  
 Itrip(Nom) : 7.1A  
 Pdis : 360mW

CAD NOTE: PLACE THE SENSE RES NEAR TO LOAD ROUTE AS KELVIN SENSE

CONN POWER LOAD SWITCHES-2

CAD NOTE: PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB. AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

FET_PARAMETER	VALUE
VGS	±20 V
ID	60 A

PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	
LOAD CURRENT	5.6A
FREQUENCY	
RIPPLE_VOLTAGE	

DESIGN NOTE:  
 Rsense: 7mohm  
 Itrip(min) : 5.65A  
 Itrip(Nom) : 7.1A  
 Pdis : 360mW

CAD NOTE: PLACE THE SENSE RES NEAR TO LOAD ROUTE AS KELVIN SENSE

CAD NOTE: PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB. AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

FET_PARAMETER	VALUE
VGS	±20 V
ID	60 A

PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	
LOAD CURRENT	5.6A
FREQUENCY	
RIPPLE_VOLTAGE	

DESIGN NOTE:  
 Rsense: 7mohm  
 Itrip(min) : 5.65A  
 Itrip(Nom) : 7.1A  
 Pdis : 360mW

CAD NOTE: PLACE THE SENSE RES NEAR TO LOAD ROUTE AS KELVIN SENSE

CAD NOTE: PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB. AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

FET_PARAMETER	VALUE
VGS	±20 V
ID	60 A

DESIGN NOTE:  
 ENABLE ON THRESHOLD 1.4V

DESIGN NOTE:  
 ENABLE ON THRESHOLD 1.4V

DESIGN NOTE:  
 ENABLE ON THRESHOLD 1.4V

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Wed Mar 6 15:45:38 2024

CONNECTOR POWER LOAD SWITCHES

DEPARTMENT UNKNOWN	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330690-A2	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 50 OF 105	

4

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PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	
LOAD CURRENT	4A
FREQUENCY	
RIPPLE_VOLTAGE	

DESIGN NOTE:

Rsense: 7mohm  
 Itrip(min): 5.65A  
 Itrip(Nom): 7.1A  
 Pdiss: 360mW

DESIGN NOTE:

ENABLE ON THRESHOLD  
 1.4V

DESIGN NOTE:

Rsense: 7mohm  
 Itrip(min): 5.65A  
 Itrip(Nom): 7.1A  
 Pdiss: 360mW

DESIGN NOTE:

ENABLE ON THRESHOLD  
 1.4V

DESIGN NOTE:

Rsense: 7mohm  
 Itrip(min): 5.65A  
 Itrip(Nom): 7.1A  
 Pdiss: 360mW

PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	
LOAD CURRENT	5.6A
FREQUENCY	
RIPPLE_VOLTAGE	

PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	
LOAD CURRENT	4A
FREQUENCY	
RIPPLE_VOLTAGE	

CONN POWER LOAD SWITCHES-4

CAD NOTE: PLACE THE SENSE RES NEAR TO LOAD ROUTE AS KELVIN SENSE

CAD NOTE:

PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB. AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

FET_PARAMETER	VALUE
VGS	+20 V
ID	60 A

CAD NOTE: PLACE THE SENSE RES NEAR TO LOAD ROUTE AS KELVIN SENSE

CAD NOTE:

PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB. AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

FET_PARAMETER	VALUE
VGS	+20 V
ID	60 A

CAD NOTE: PLACE THE SENSE RES NEAR TO LOAD ROUTE AS KELVIN SENSE

CAD NOTE:

PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB. AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

FET_PARAMETER	VALUE
VGS	+20 V
ID	60 A

Wed Mar 6 15:45:39 2024

CONNECTOR POWER LOAD SWITCHES

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
UNKNOWN	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 52 OF 105	

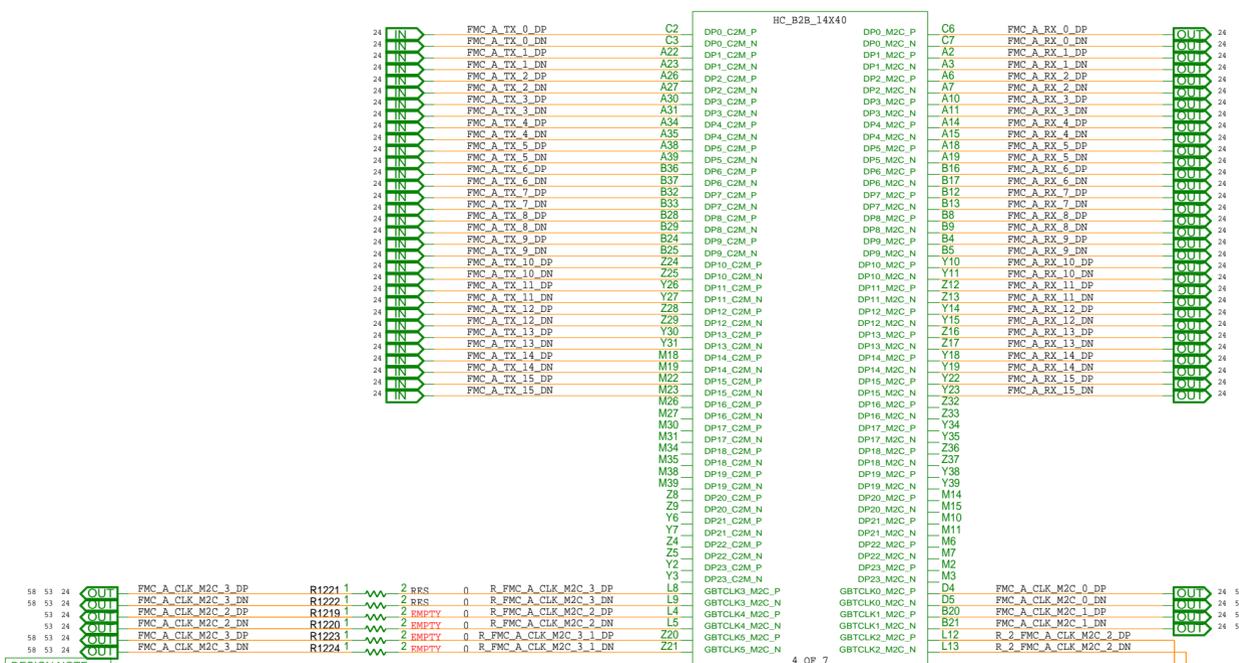
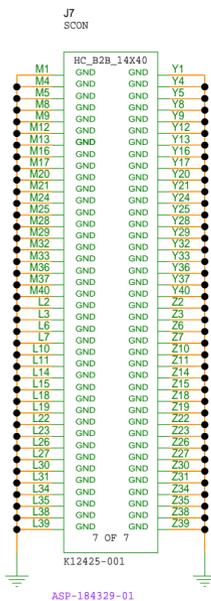
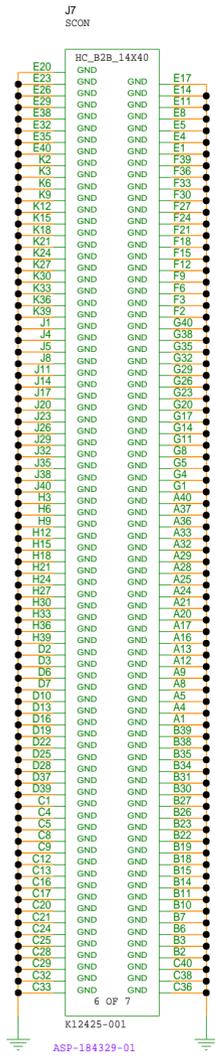
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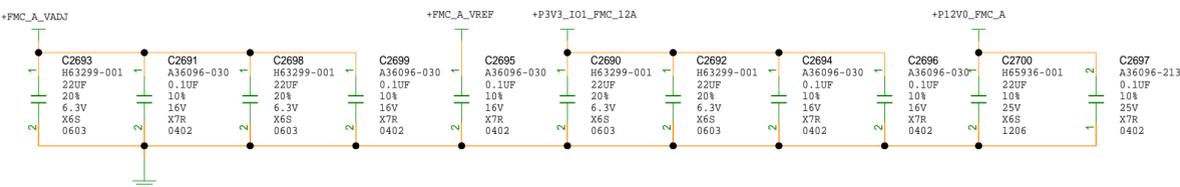
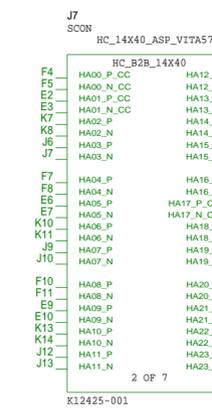
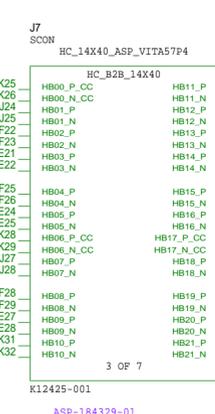
2

1

# FMC+ CONNECTOR A (NORTH)



**DESIGN NOTE:**  
 REWORK RES SHALL BE MOUNTED FOR PROVIDING REFERENCE CLOCK TO FM91 FOR SUPPORTING ADC12DJ5200RFEVM CARD

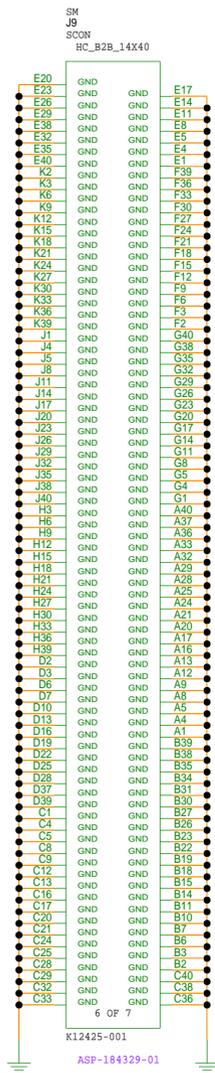


Wed Mar 6 15:45:40 2024

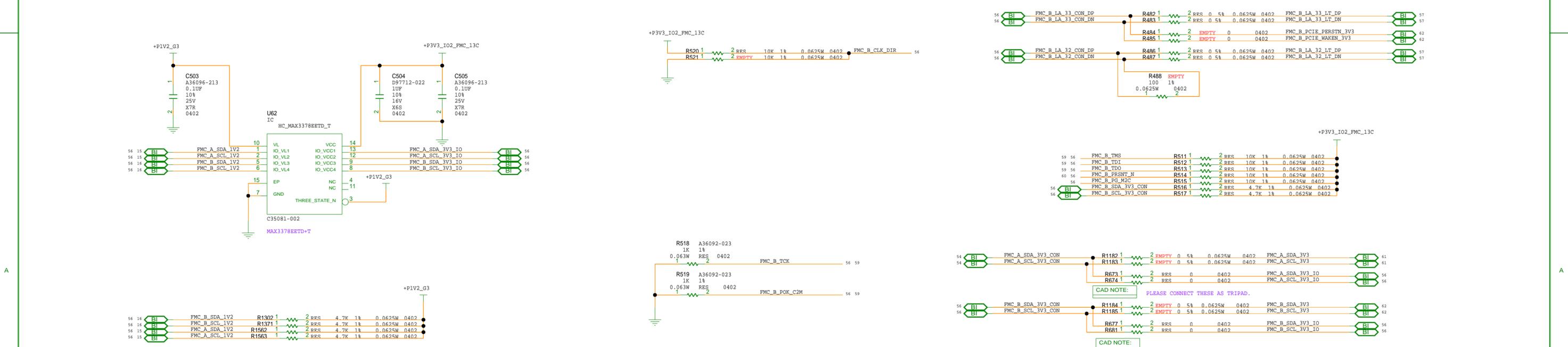
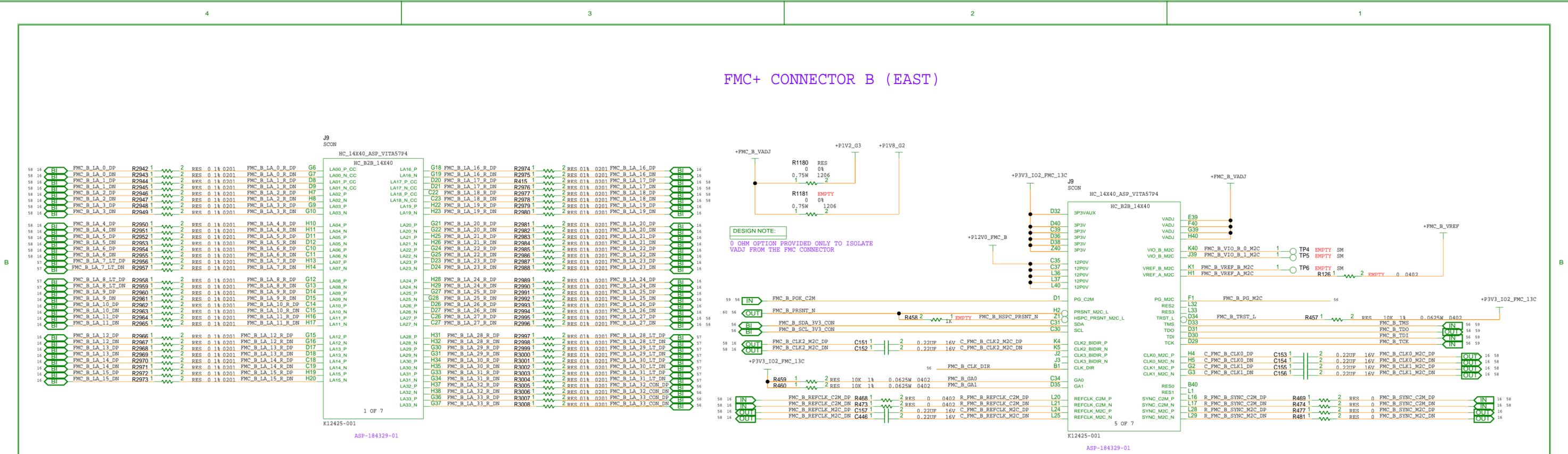
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 53 OF 105	



### FMC+ CONNECTOR B (EAST)



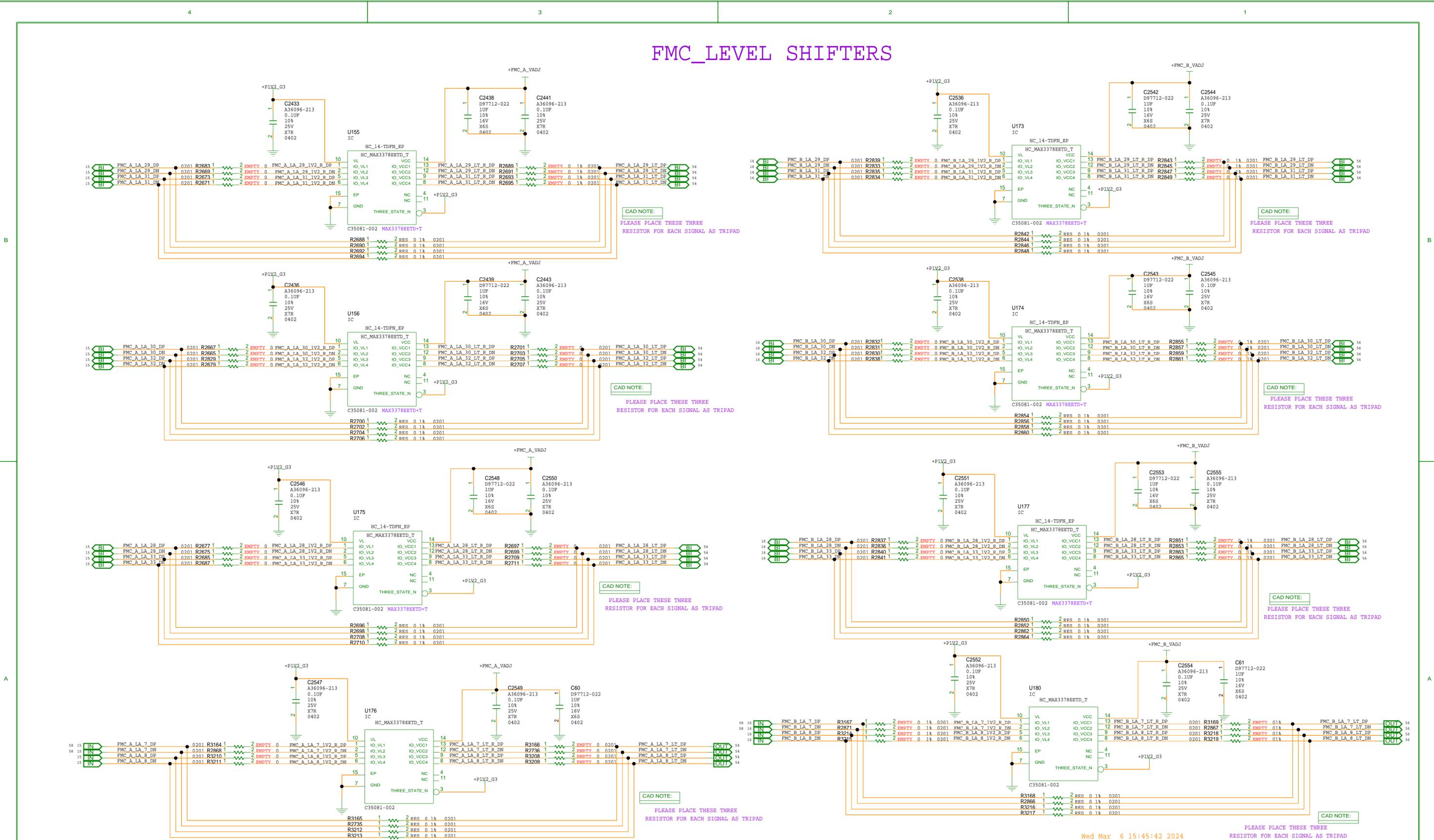
### FMC+ CONNECTOR B (EAST)



Wed Mar 6 15:45:41 2024

DEPARTMENT	Intel Corporation	SIZE	C+	CODE	34649	DOCUMENT NUMBER	150-0330690-A2	REV	2.0
PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SCALE:	DO NOT SCALE DRAWING				SHEET	56 OF 105	

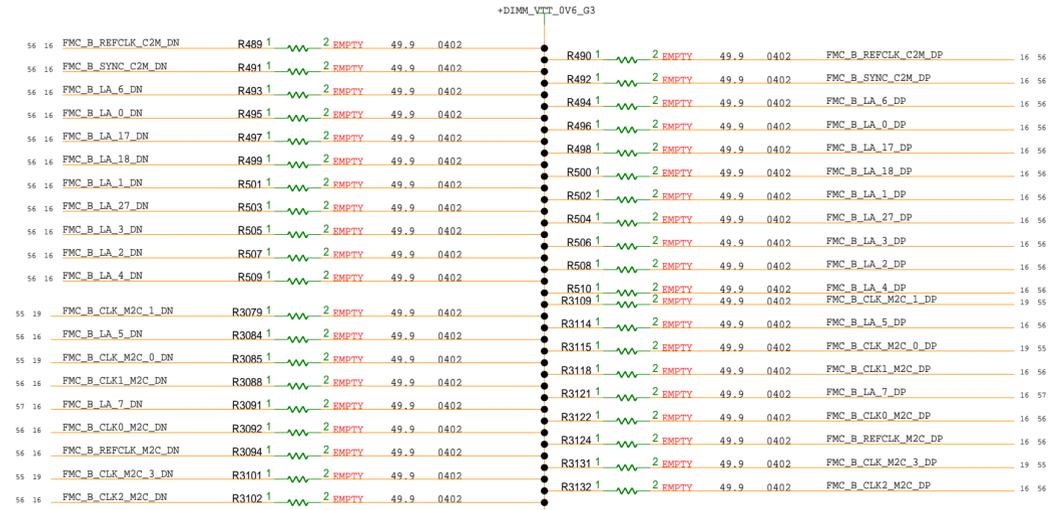
# FMC\_LEVEL SHIFTERS



Wed Mar 6 15:45:42 2024

DEPARTMENT		Intel Corporation		SIZE	CODE	DOCUMENT NUMBER	REV
UNKNOWN		2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119		C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET		57 OF 105	

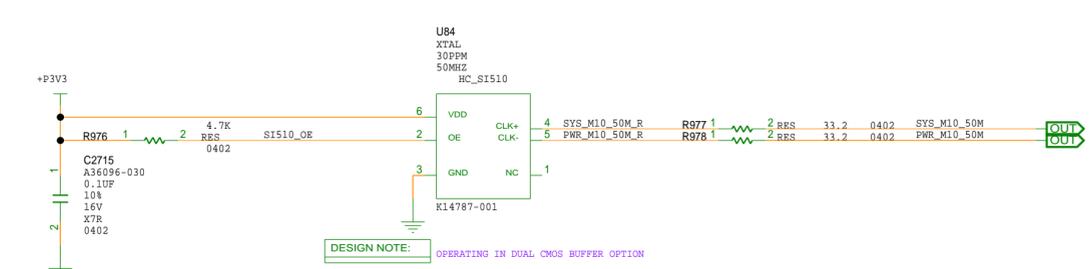
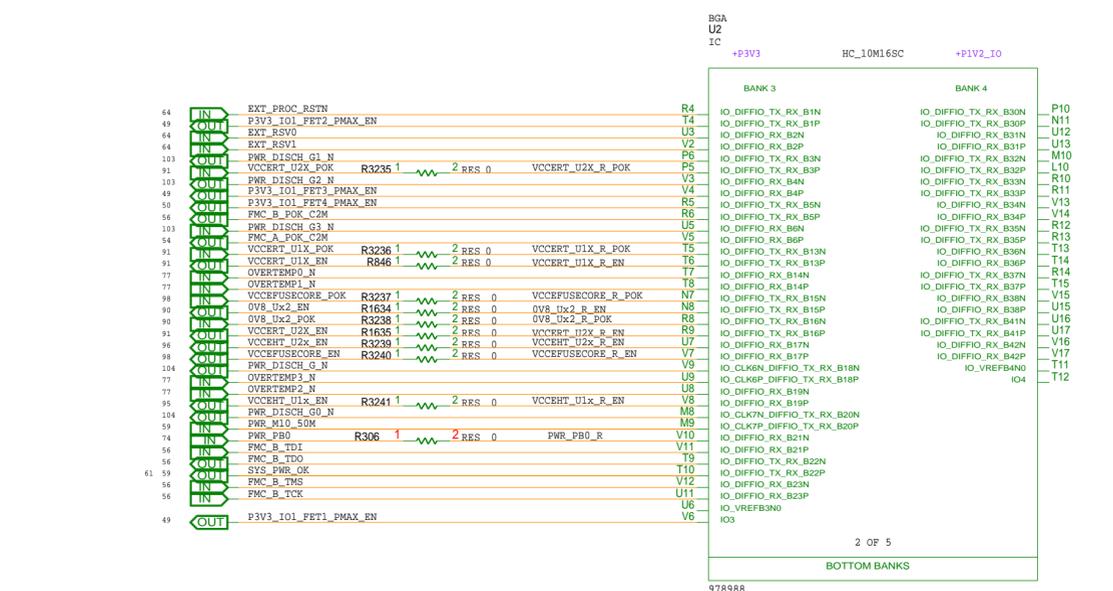
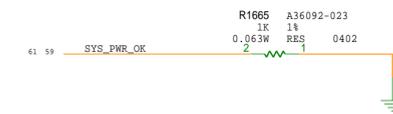
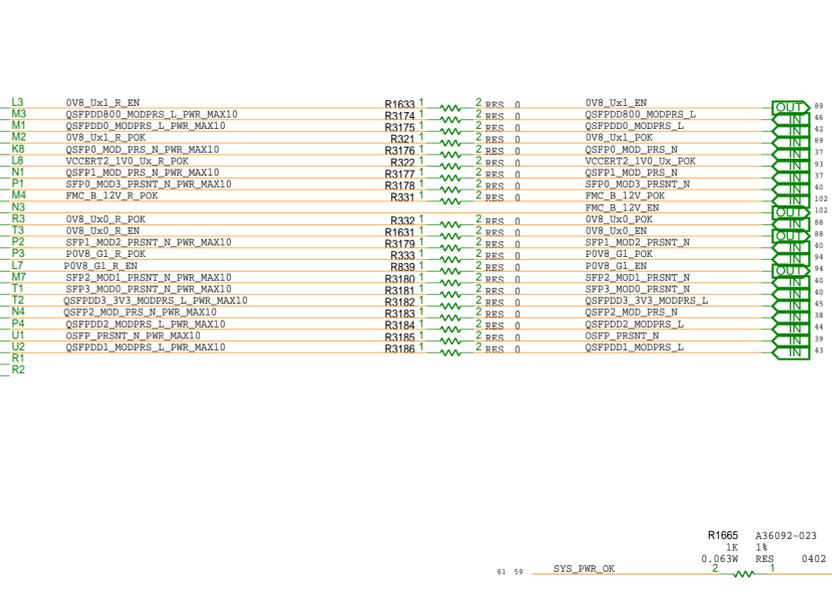
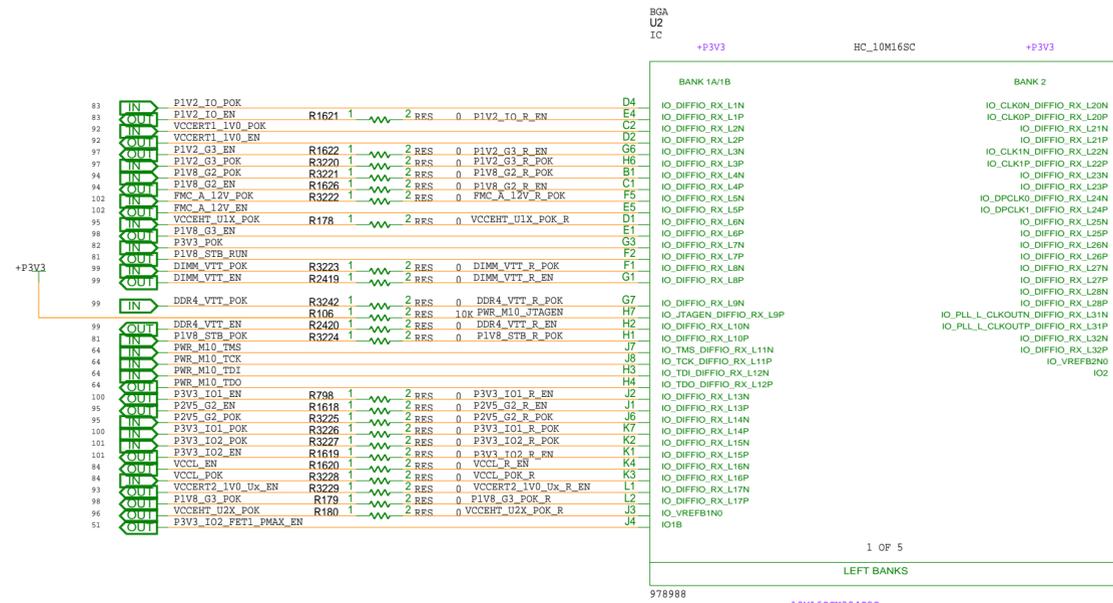
FMC\_TERMINATIONS



Wed Mar 6 15:45:42 2024

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
UNKNOWN	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 58 OF 105

# MAX10- Intel® MAX® 10 FPGA PWR MAX-10- I



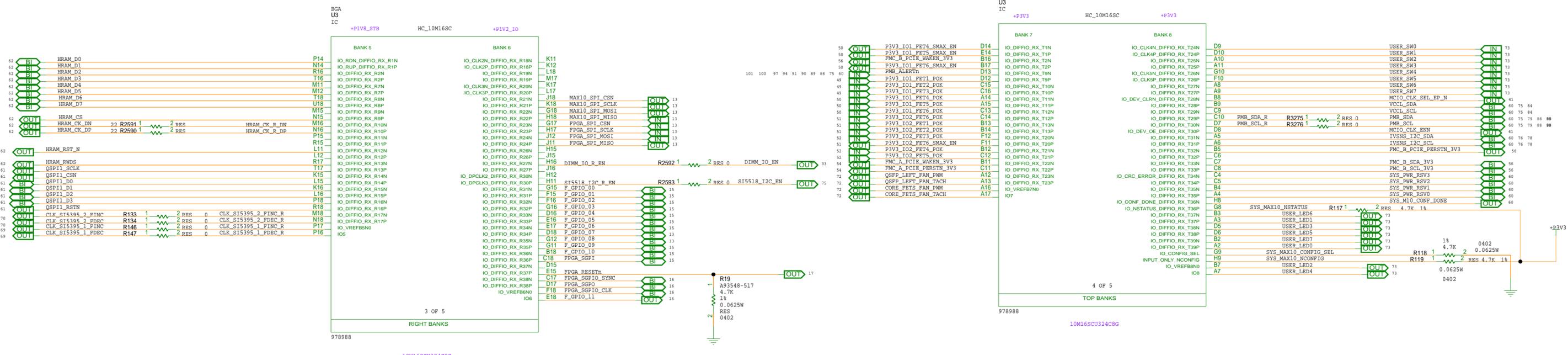
Wed Mar 6 15:45:43 2024

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
P&G	INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 59 OF 105	

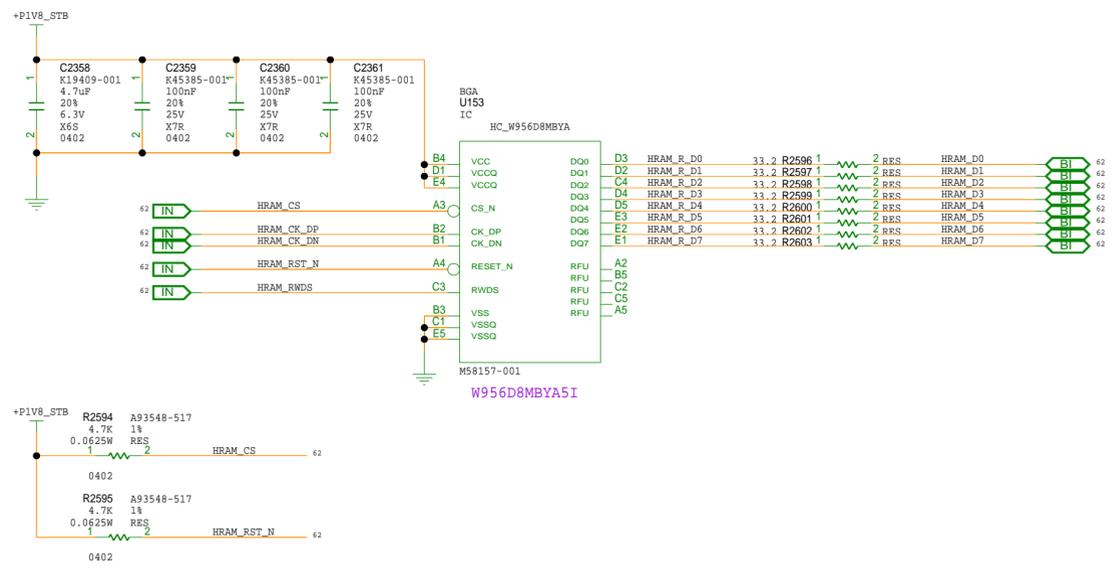




# MAX10- Intel® MAX® 10 FPGA SYS MAX-10- II



## HYPER\_RAM

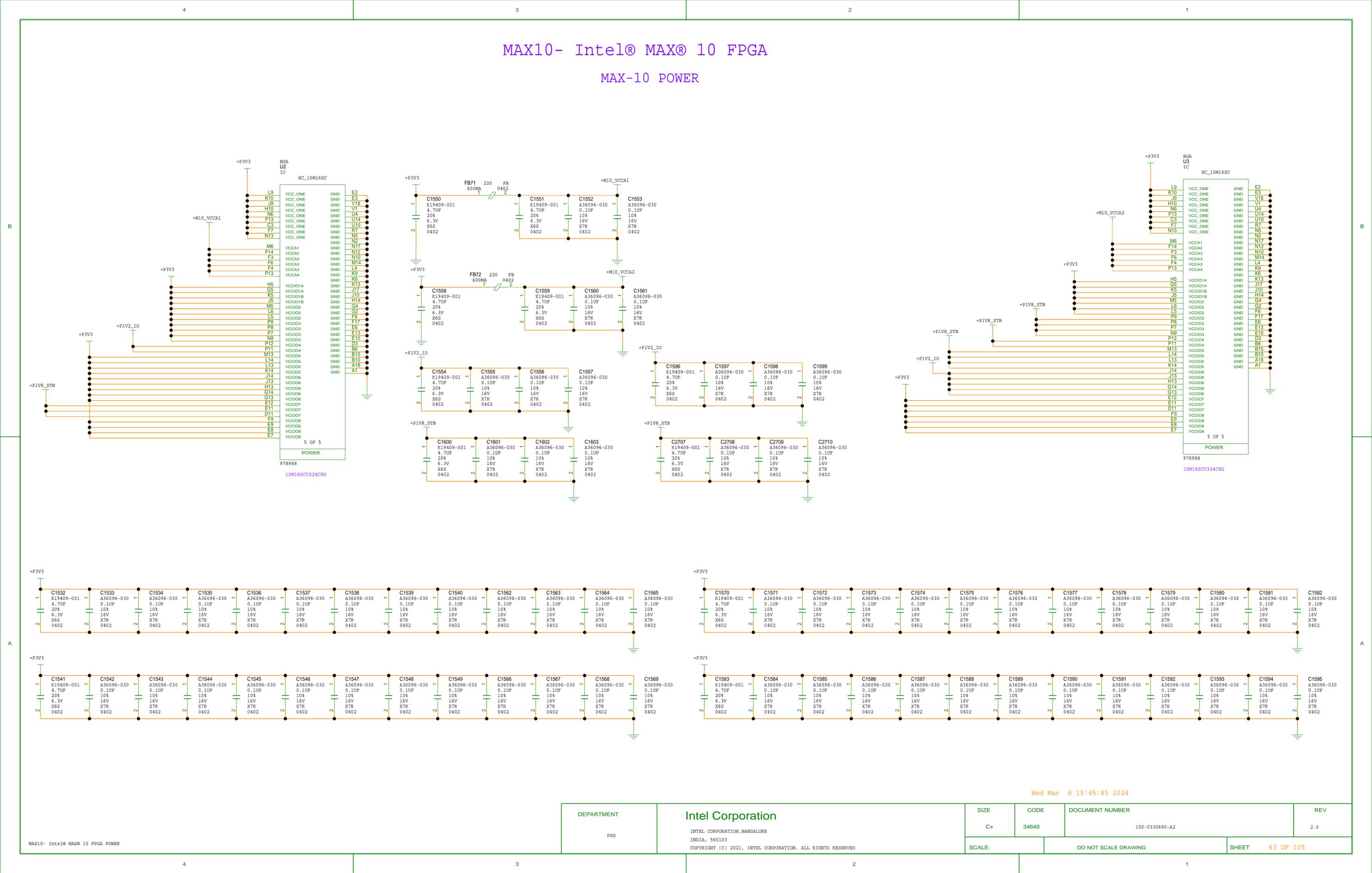


Wed Mar 6 15:45:44 2024

DEPARTMENT PSG	Intel Corporation INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330690-A2	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 62 OF 105	

# MAX10- Intel® MAX® 10 FPGA

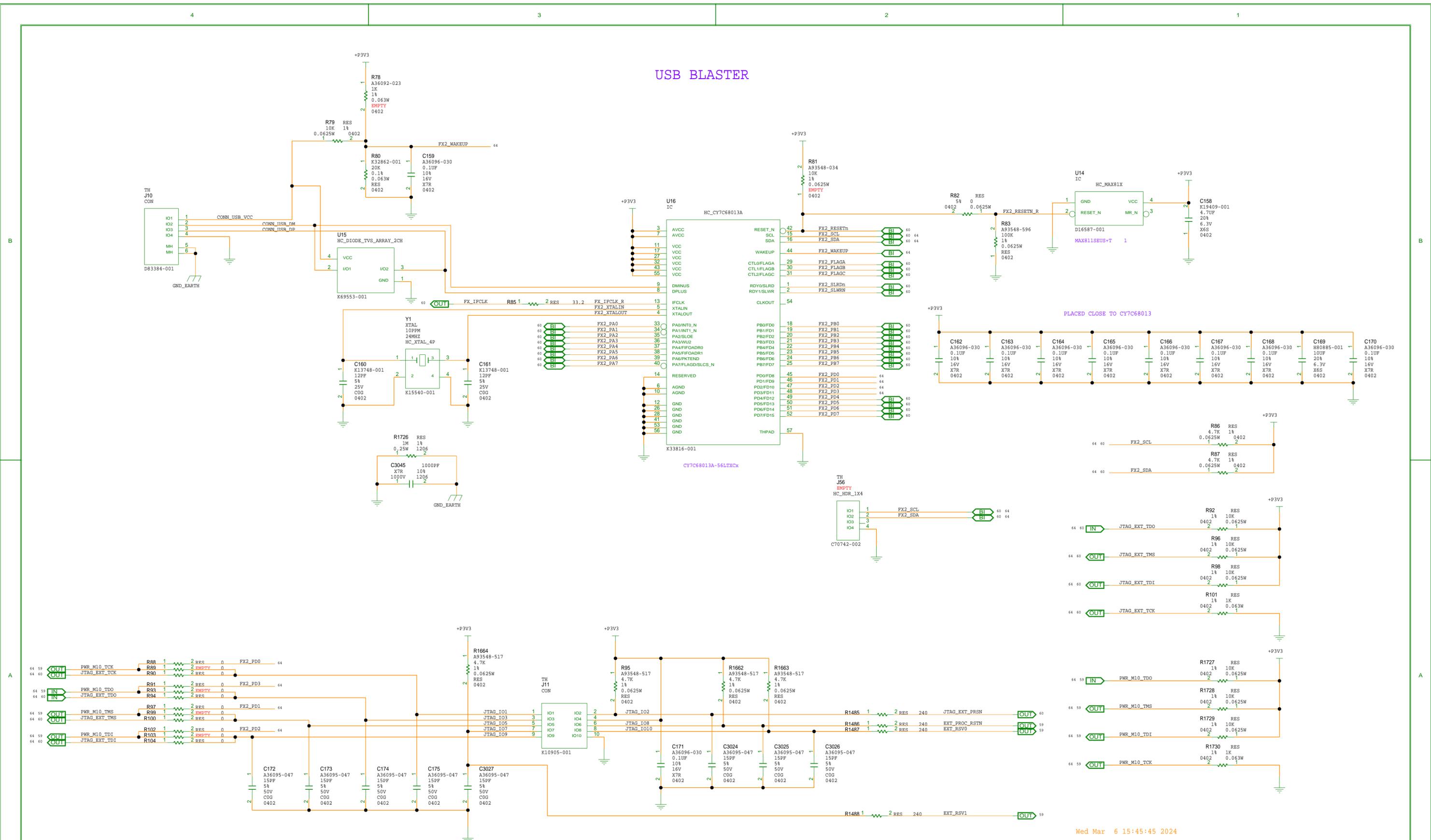
## MAX-10 POWER



Wed Mar 6 15:45:45 2024

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 63 OF 105

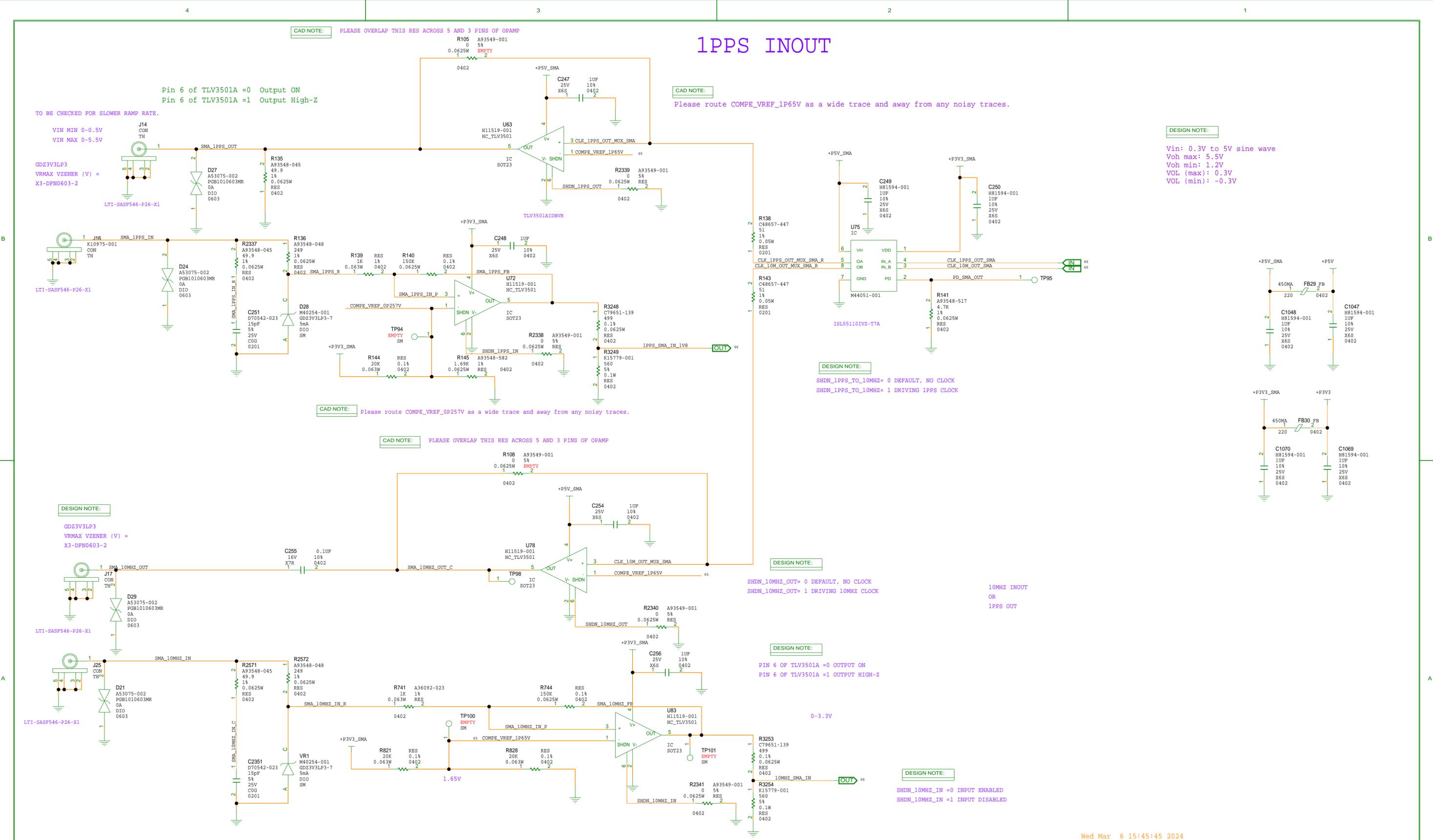
# USB BLASTER



Wed Mar 6 15:45:45 2024

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:	DO NOT SCALE DRAWING	SHEET		64 OF 105	

# 1PPS INOUT



CAD NOTE: PLEASE OVERLAP THIS RES ACROSS 5 AND 3 PINS OF OPAMP

CAD NOTE: Please route COMPE\_VREF\_1P65V as a wide trace and away from any noisy traces.

DESIGN NOTE: Vin: 0.3V to 5V sine wave  
Voh max: 5.5V  
Voh min: 1.2V  
VOL (max): 0.3V  
VOL (min): -0.3V

CAD NOTE: Please route COMPE\_VREF\_OP257V as a wide trace and away from any noisy traces.

CAD NOTE: PLEASE OVERLAP THIS RES ACROSS 5 AND 3 PINS OF OPAMP

DESIGN NOTE: SHDN\_1PPS\_TO\_10MHZ= 0 DEFAULT, NO CLOCK  
SHDN\_1PPS\_TO\_10MHZ= 1 DRIVING 1PPS CLOCK

DESIGN NOTE: GD23V3LP3  
VRMAX VZENER (V) = X3-DFN0603-2

DESIGN NOTE: SHDN\_10MHZ\_OUT= 0 DEFAULT, NO CLOCK  
SHDN\_10MHZ\_OUT= 1 DRIVING 10MHZ CLOCK

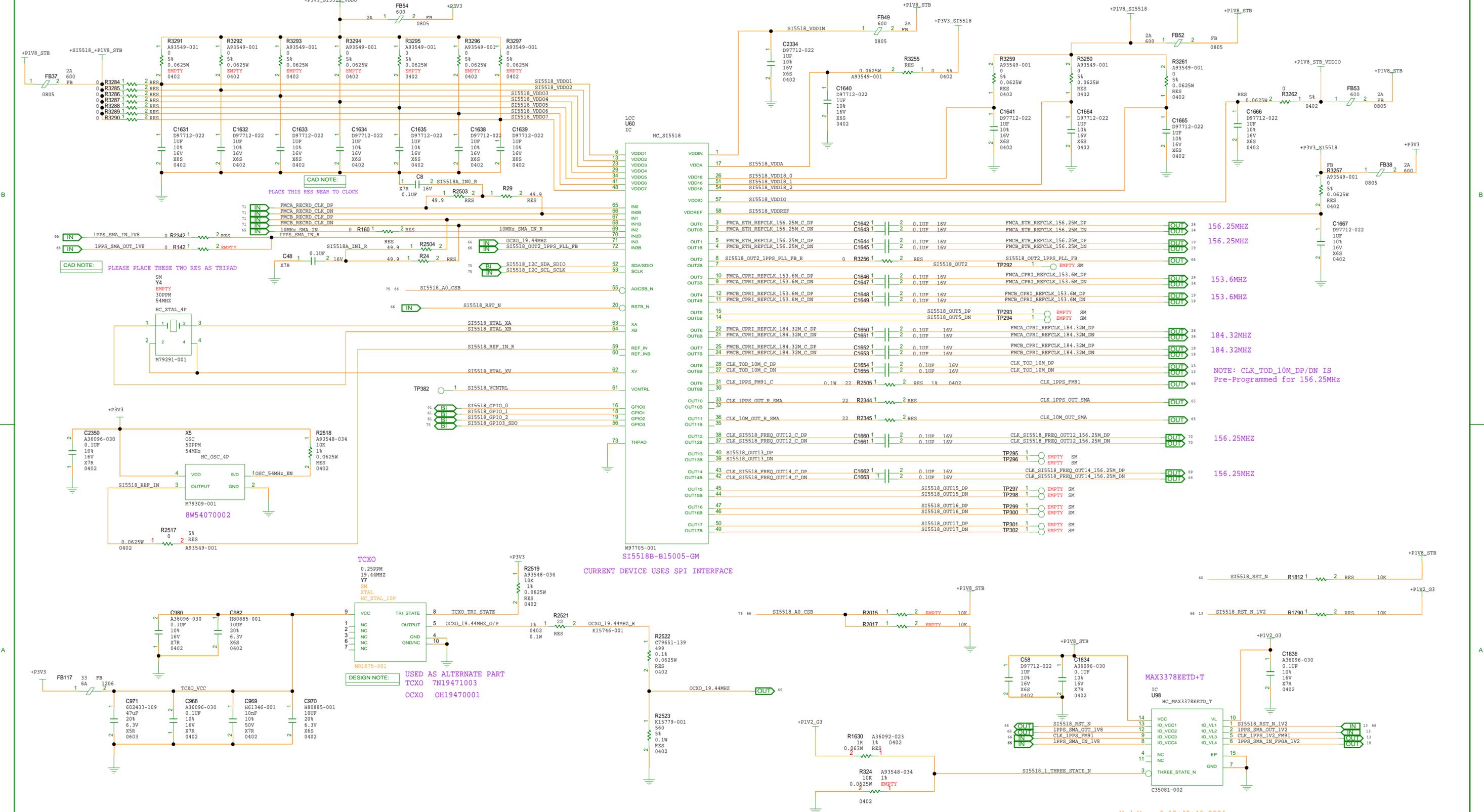
DESIGN NOTE: PIN 6 OF TLV3501A = 0 OUTPUT ON  
PIN 6 OF TLV3501A = 1 OUTPUT HIGH-Z

DESIGN NOTE: SHDN\_10MHZ\_IN = 0 INPUT ENABLED  
SHDN\_10MHZ\_IN = 1 INPUT DISABLED

Wed Mar 6 15:45:45 2024

DEPARTMENT PSG	Intel Corporation INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330690-A2	REV 2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 65 OF 105

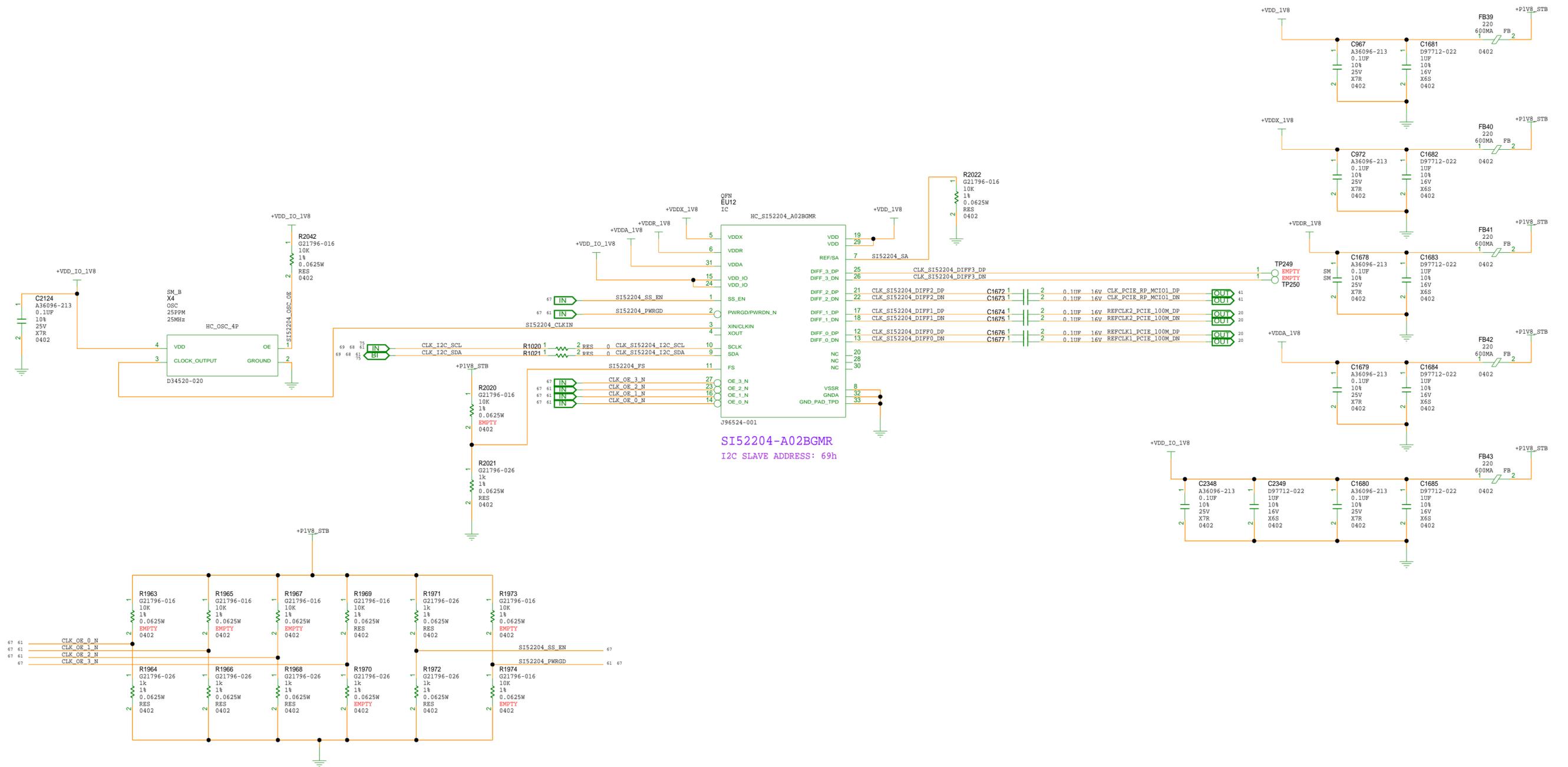
# SI5518 CLOCK GENERATOR



Wed Mar 6 15:45:46 2024

DEPARTMENT	Intel Corporation	SIZE	C+	CODE	34649	DOCUMENT NUMBER	150-0330690-A2	REV	2.0
INDIA, 560103	INTEL CORPORATION, BANGALORE	SCALE:		DO NOT SCALE DRAWING		SHEET	66 OF 105		

# SI52204 PCIE CLOCK GENERATOR



SI52204-A02BGMR  
I2C SLAVE ADDRESS: 69h

Wed Mar 6 15:45:46 2024

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 67 OF 105



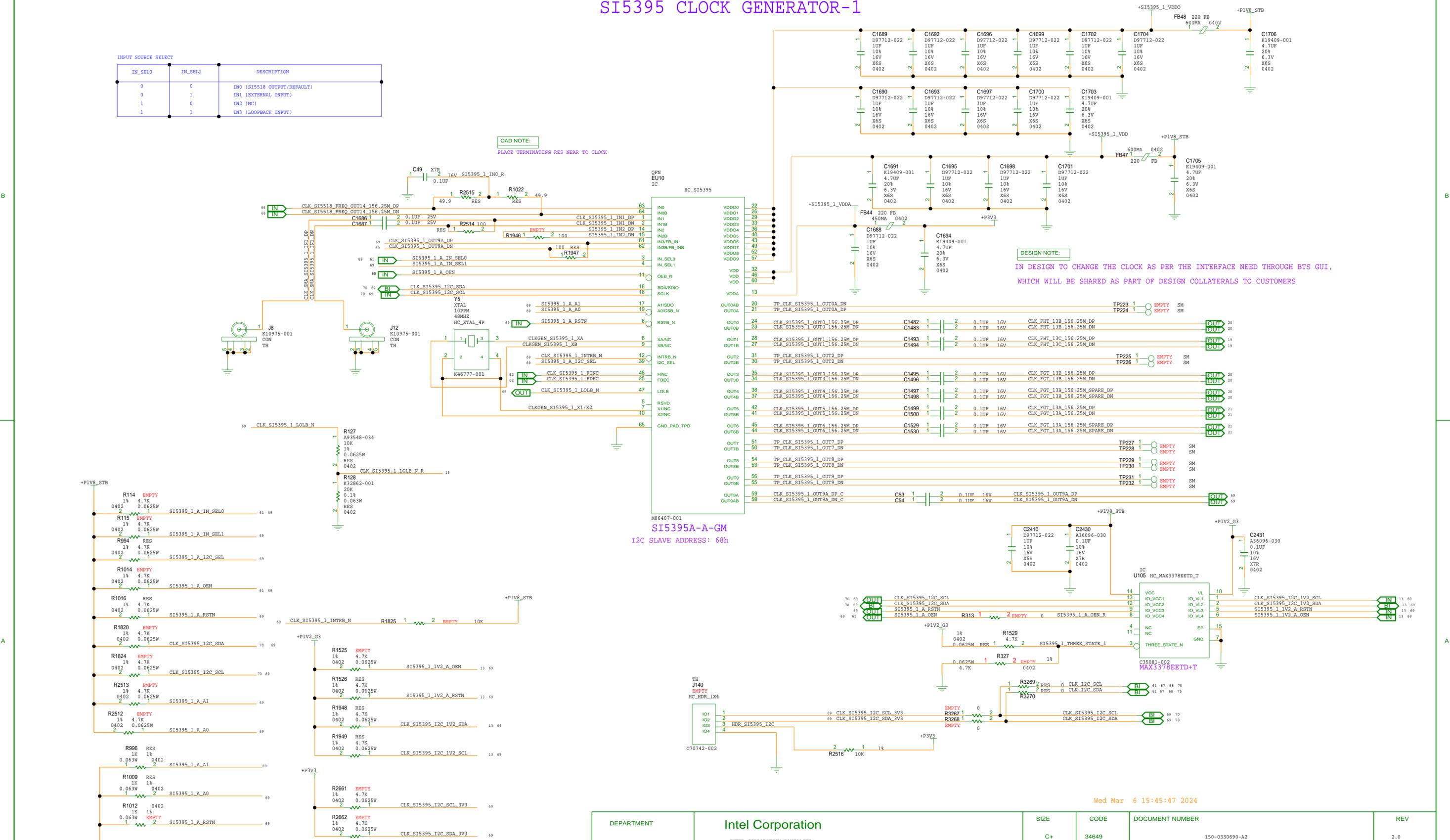
# SI5395 CLOCK GENERATOR-1

INPUT SOURCE SELECT

IN_SEL0	IN_SEL1	DESCRIPTION
0	0	IN0 (SI5518 OUTPUT/DEFAULT)
0	1	IN1 (EXTERNAL INPUT)
1	0	IN2 (NC)
1	1	IN3 (LOOPBACK INPUT)

CAD NOTE:  
PLACE TERMINATING RES NEAR TO CLOCK

DESIGN NOTE:  
IN DESIGN TO CHANGE THE CLOCK AS PER THE INTERFACE NEED THROUGH BTS GUI, WHICH WILL BE SHARED AS PART OF DESIGN COLLATERALS TO CUSTOMERS



SI5395A-A-GM  
I2C SLAVE ADDRESS: 68h

Wed Mar 6 15:45:47 2024

DEPARTMENT	Intel Corporation	SIZE	C+	CODE	34649	DOCUMENT NUMBER	150-0330690-A2	REV	2.0
PGO	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SCALE:		DO NOT SCALE DRAWING		SHEET	69 OF 105		

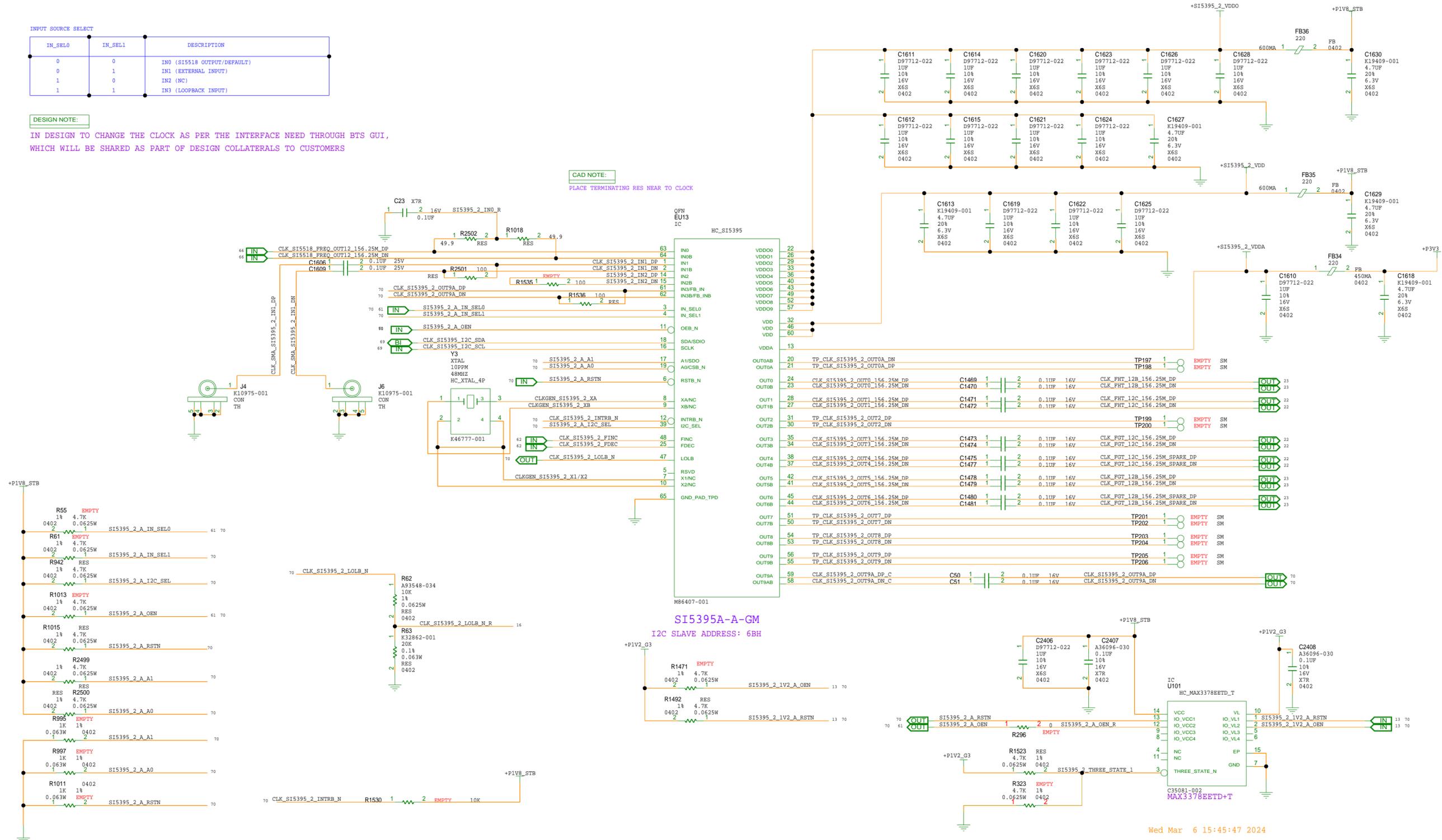
# SI5395 CLOCK GENERATOR-2

INPUT SOURCE SELECT		
IN_SEL0	IN_SEL1	DESCRIPTION
0	0	IN0 (SI5518 OUTPUT/DEFAULT)
0	1	IN1 (EXTERNAL INPUT)
1	0	IN2 (NC)
1	1	IN3 (LOOPBACK INPUT)

**DESIGN NOTE:**

IN DESIGN TO CHANGE THE CLOCK AS PER THE INTERFACE NEED THROUGH BTS GUI, WHICH WILL BE SHARED AS PART OF DESIGN COLLATERALS TO CUSTOMERS

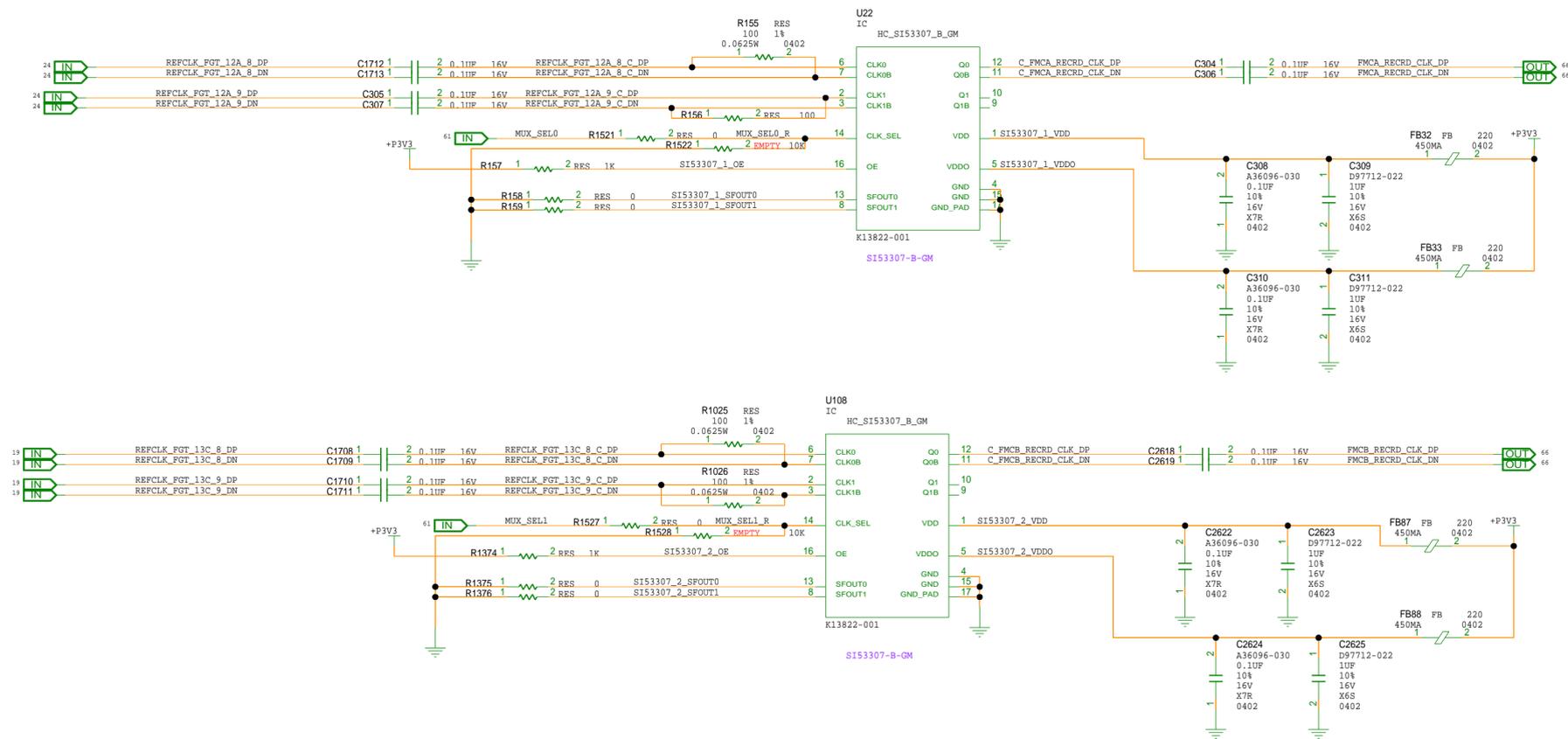
**CAD NOTE:**  
PLACE TERMINATING RES NEAR TO CLOCK



**SI5395A-A-GM**  
I2C SLAVE ADDRESS: 6BH

Wed Mar 6 15:45:47 2024

# CLOCK MUX-I



Wed Mar 6 15:45:47 2024

DEPARTMENT	Intel Corporation INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SIZE	CODE	DOCUMENT NUMBER	REV
PSG		C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 71 OF 105

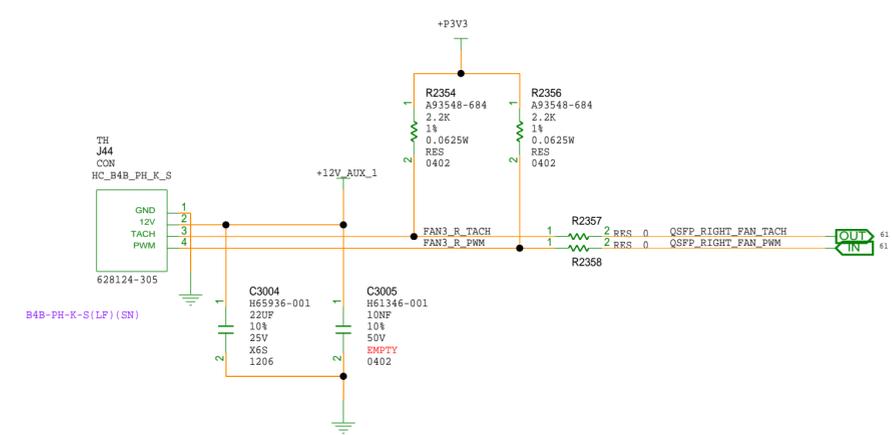
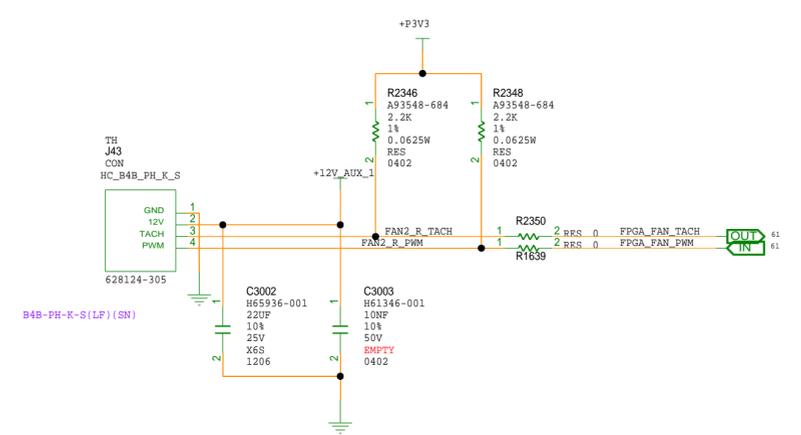
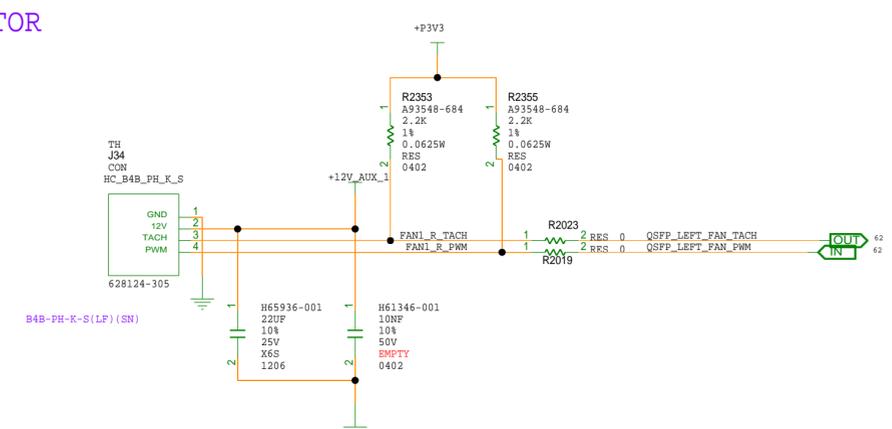
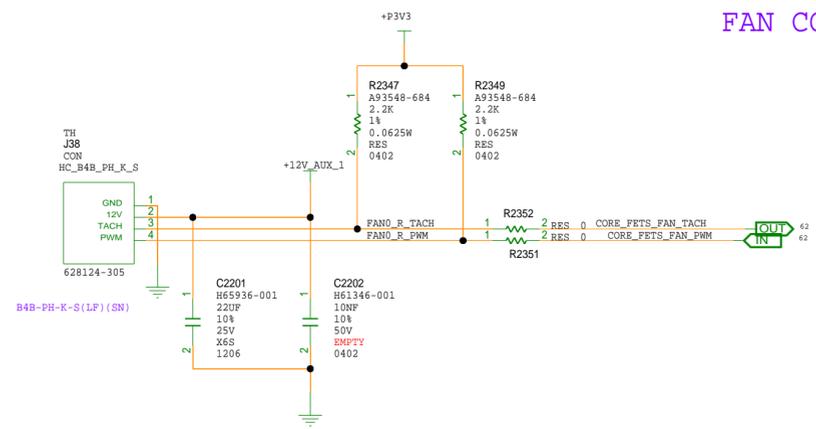
4

3

2

1

### FAN CONNECTOR



Wed Mar 6 15:45:48 2024

4

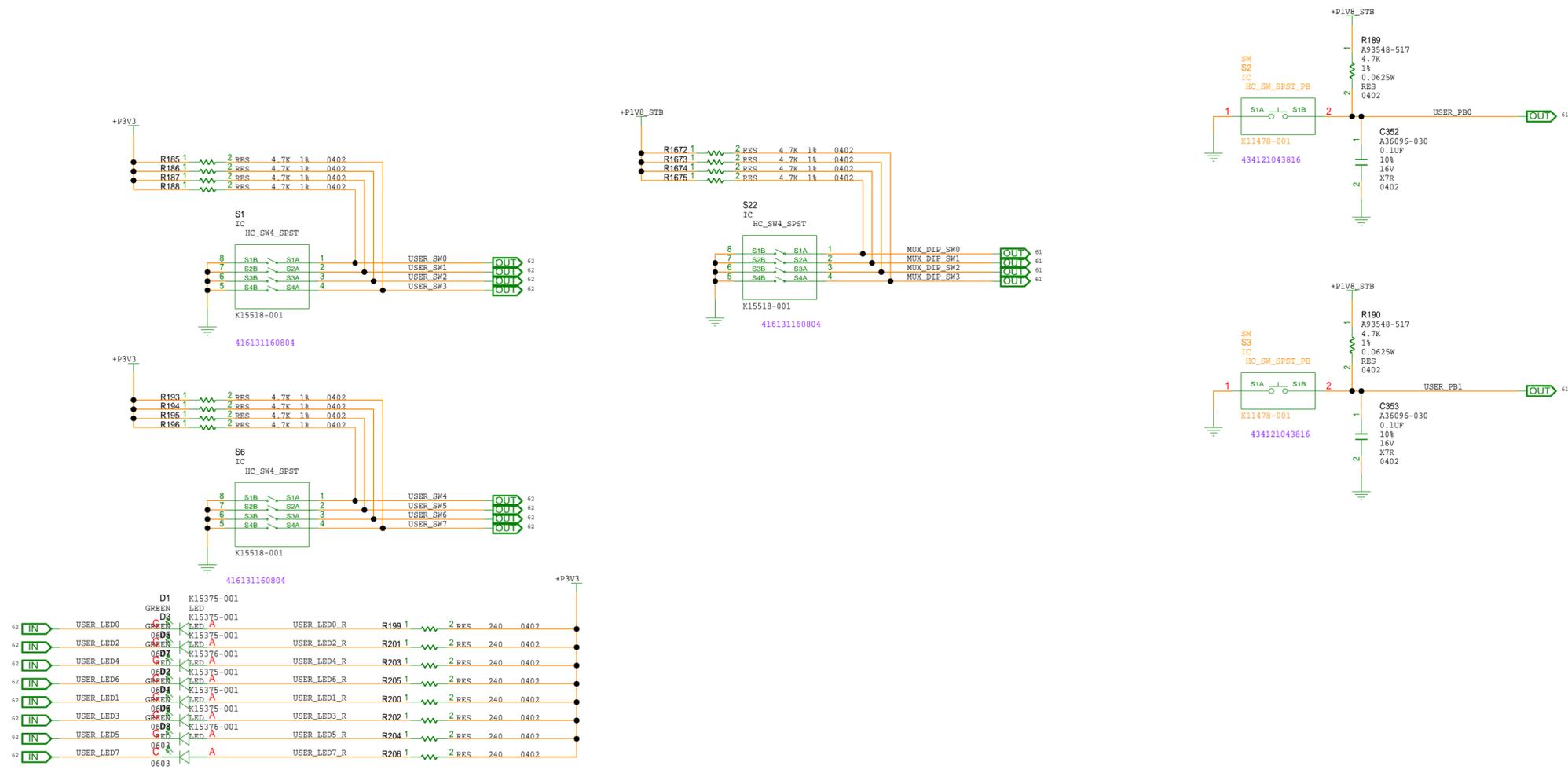
3

2

1

DEPARTMENT PSG	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330690-A2	REV 2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 72 OF 105

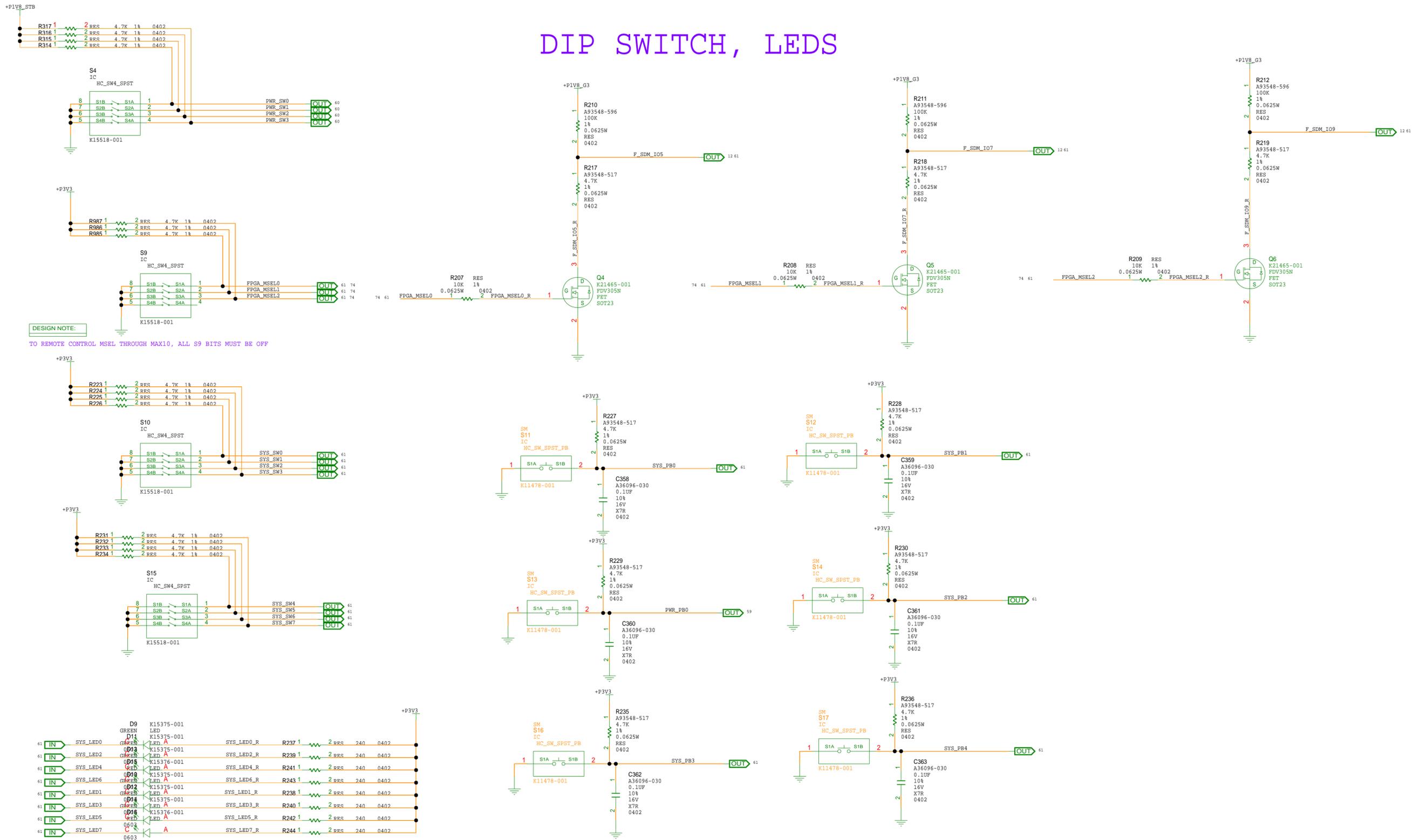
# DIP SWITCH, LEDES



Wed Mar 6 15:45:48 2024

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 73 OF 105

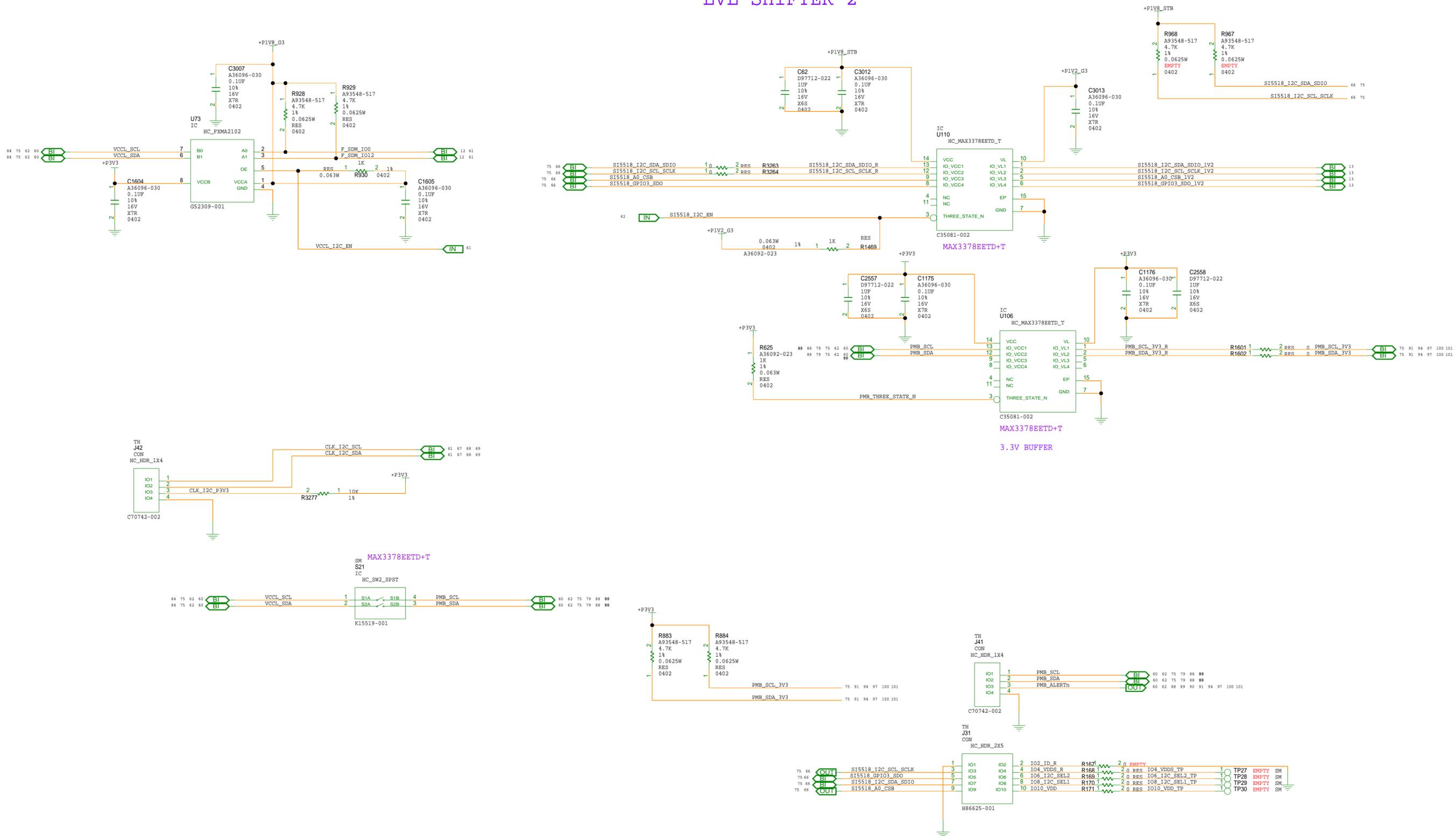
# DIP SWITCH, LEDS



Wed Mar 6 15:45:49 2024

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 74 OF 105	

# LVL SHIFTER-2



Wed Mar 6 15:45:49 2024

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 75 OF 105	

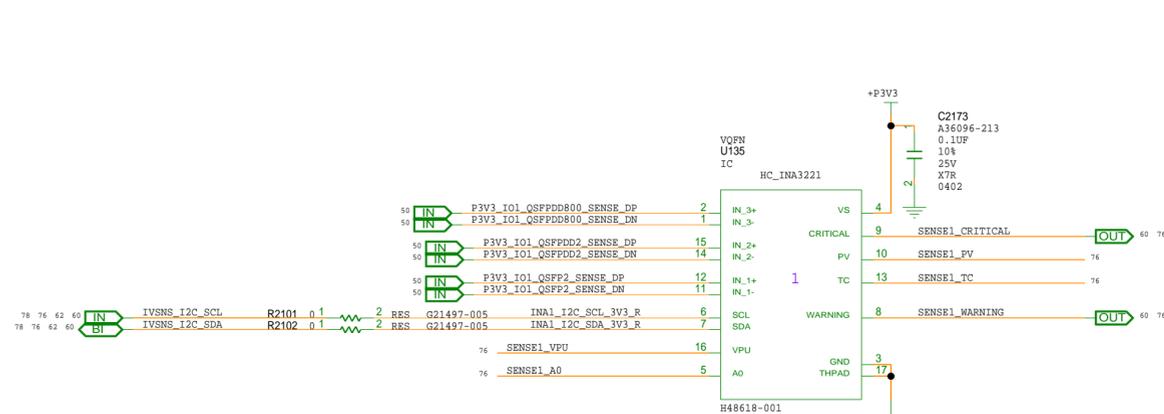
4

3

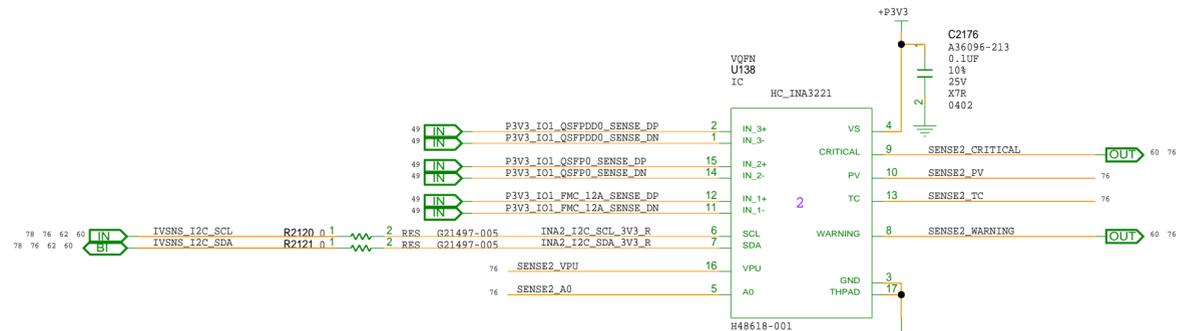
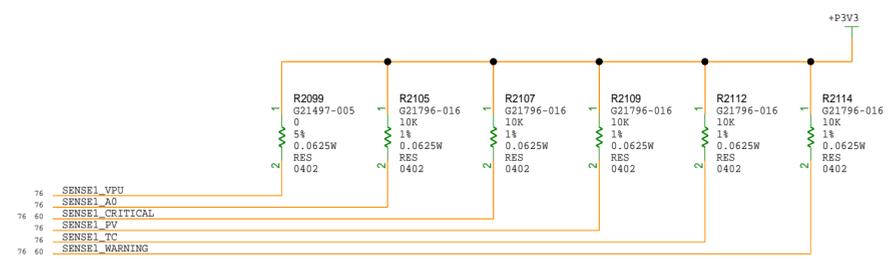
2

1

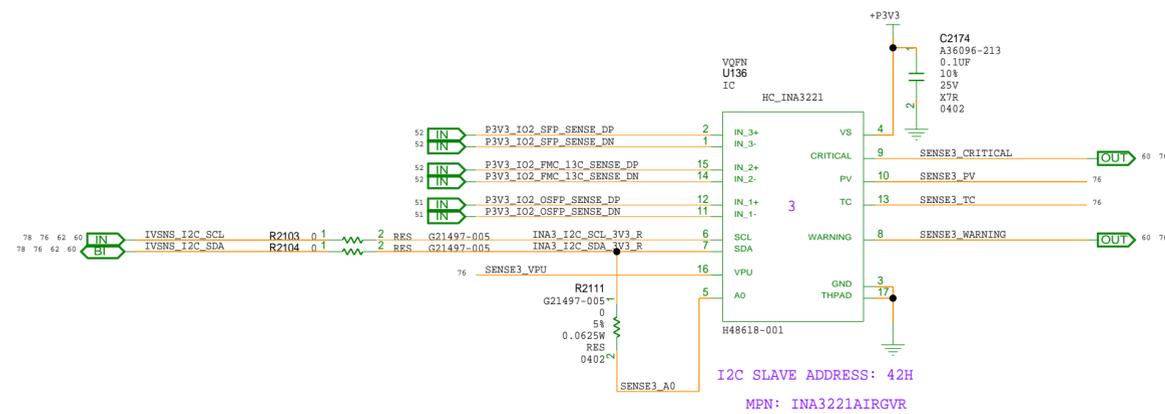
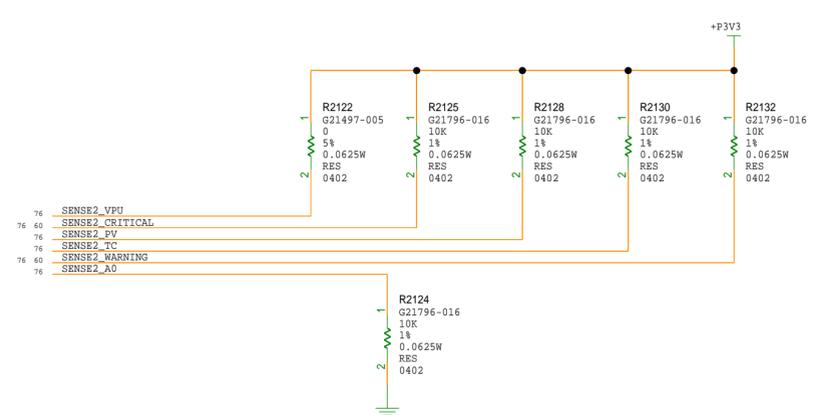
### INA3221



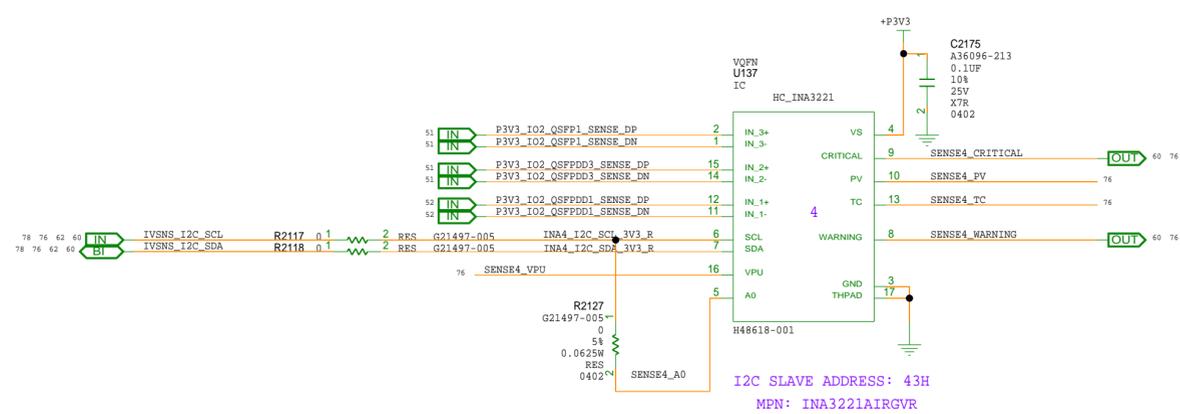
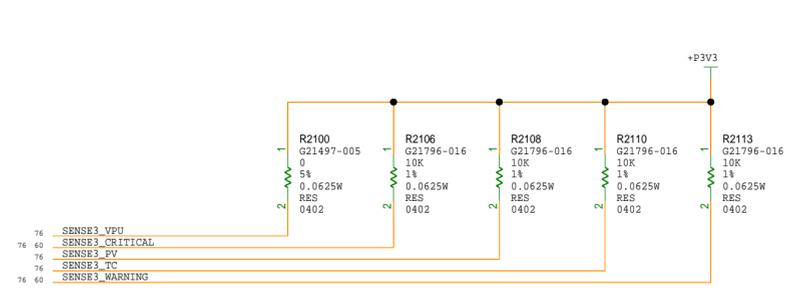
I2C SLAVE ADDRESS: 41H  
MPN: INA3221AIRGVR



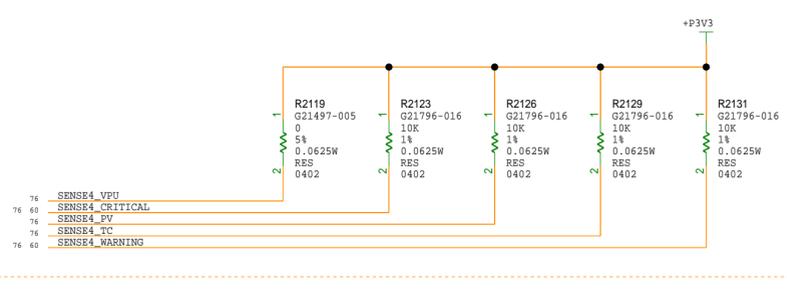
I2C SLAVE ADDRESS: 40H  
MPN: INA3221AIRGVR



I2C SLAVE ADDRESS: 42H  
MPN: INA3221AIRGVR



I2C SLAVE ADDRESS: 43H  
MPN: INA3221AIRGVR



Wed Mar 6 15:45:50 2024

4

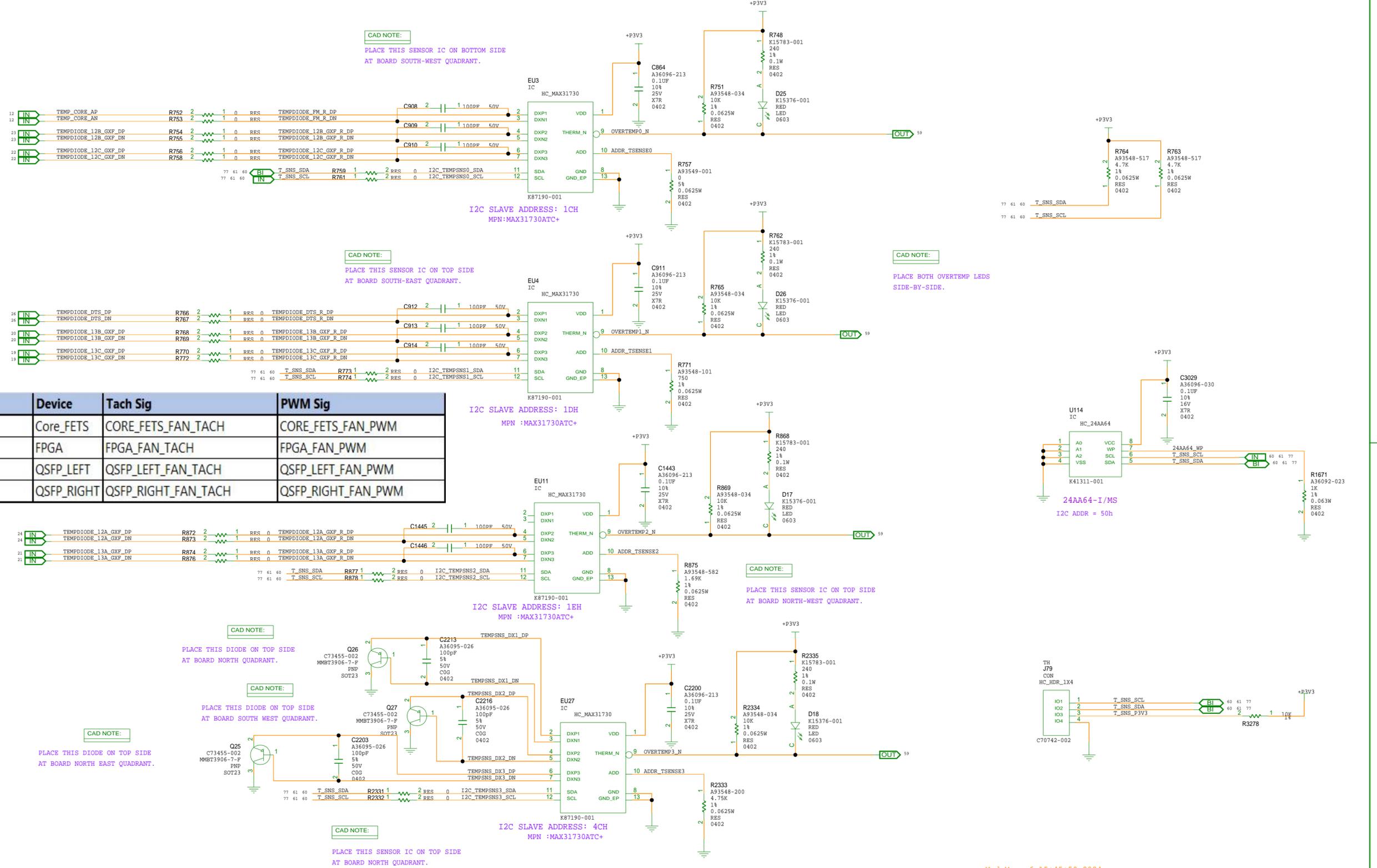
3

2

1

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	C+	34649	150-0330690-A2	2.0
SCALE:	DO NOT SCALE DRAWING			SHEET	76 OF 105

# BOARD TEMP SENSORS

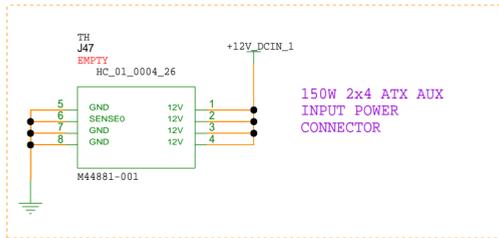


Temp Sensor	Fan Connector	Device	Tach Sig	PWM Sig
Q26/EU27.CH1	J38	Core_FETS	CORE_FETS_FAN_TACH	CORE_FETS_FAN_PWM
EU3/EU4/EU11	J43	FPGA	FPGA_FAN_TACH	FPGA_FAN_PWM
Q27/EU27.CH2	J34	QSFP_LEFT	QSFP_LEFT_FAN_TACH	QSFP_LEFT_FAN_PWM
Q25/EU27.CH3	J44	QSFP_RIGHT	QSFP_RIGHT_FAN_TACH	QSFP_RIGHT_FAN_PWM

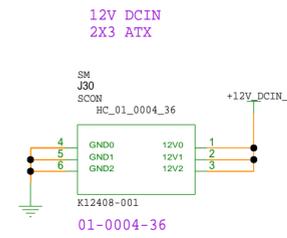
Wed Mar 6 15:45:50 2024



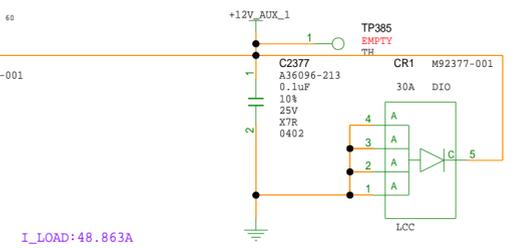
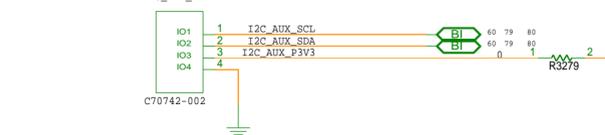
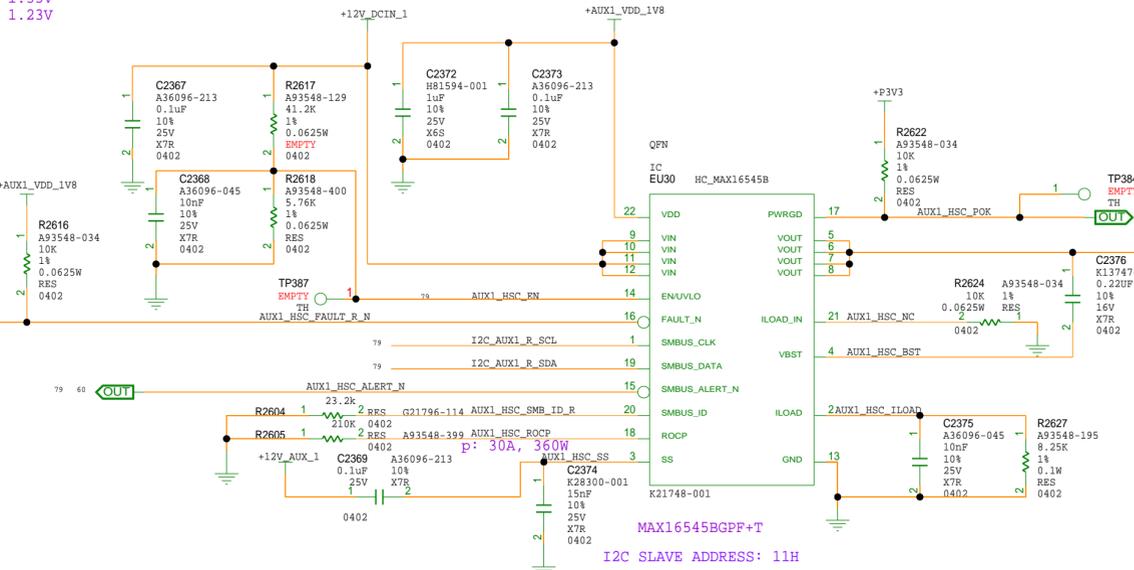
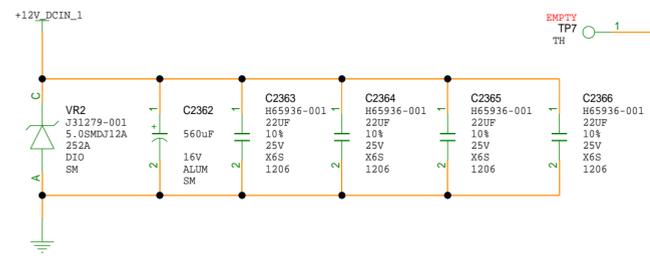
# POWER In- 12V\_AUX1 Hotswap



**DESIGN NOTE:**  
 When 16V, EN = 1.96V  
 When 15V, EN = 1.84V  
 When 14V, EN = 1.72V  
 When 13V, EN = 1.59V  
 When 12V, EN = 1.47V  
 When 11V, EN = 1.35V  
 When 10V, EN = 1.23V

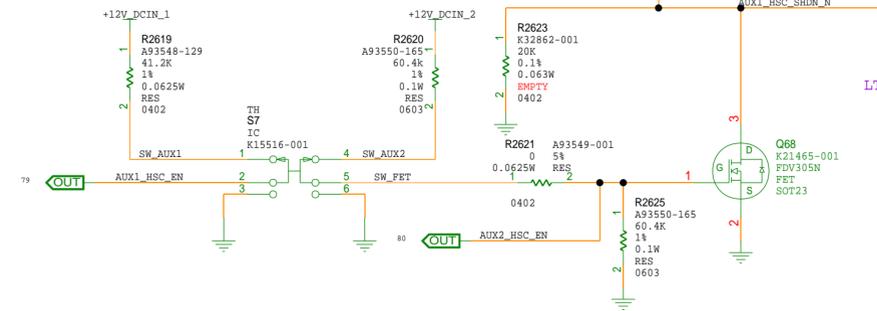
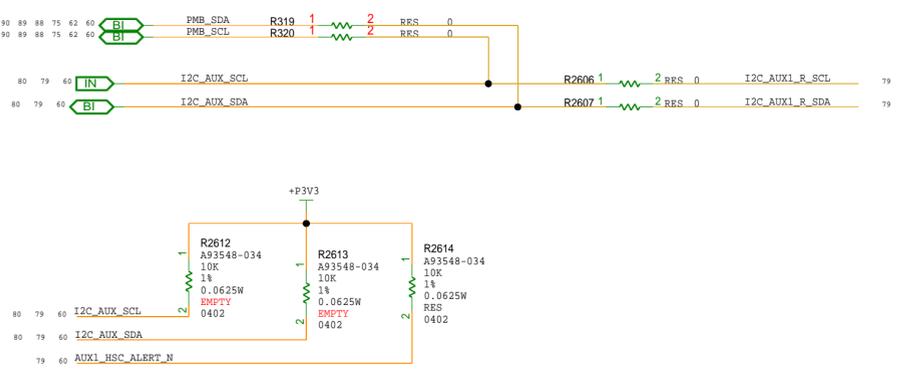
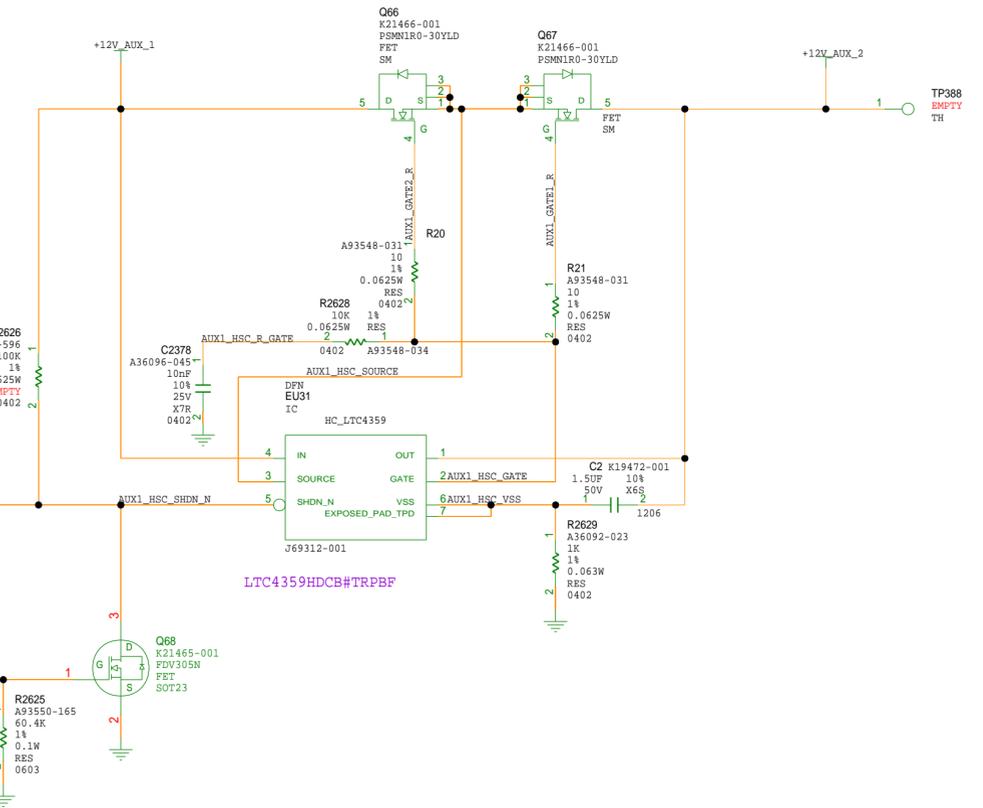


**CAD NOTE:**  
 Place close to  
 MAX1654B VIN



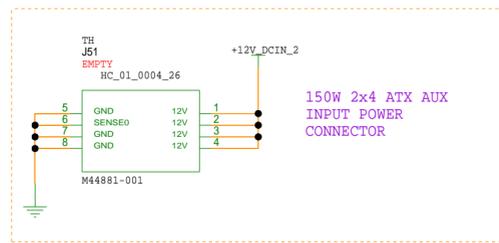
FET_PARAMETER	VALUE
VGS	+20 V
ID	300 A

Switch Position S7	+12V_DCIN_1	+12V_DCIN_2	+12V_AUX_1	+12V_AUX_2_FET	EU35	EU31	+12V_AUX_1 Shorts with +12V_AUX_2	+12V_AUX_2_FET Shorts with +12V_AUX_2	Power Up Case
2-1 (ON) & 5-4 (ON)	Present	Present	ON	ON	ON	OFF	No	Yes	High Power Case
2-1 (ON) & 5-4 (ON)	Present	Not Present	ON	OFF	OFF	ON	Yes	No	Low Power Case
2-3 & 5-6 (OFF)	Present	Present	OFF	OFF	OFF	OFF	No	No	OFF Case



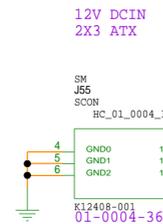
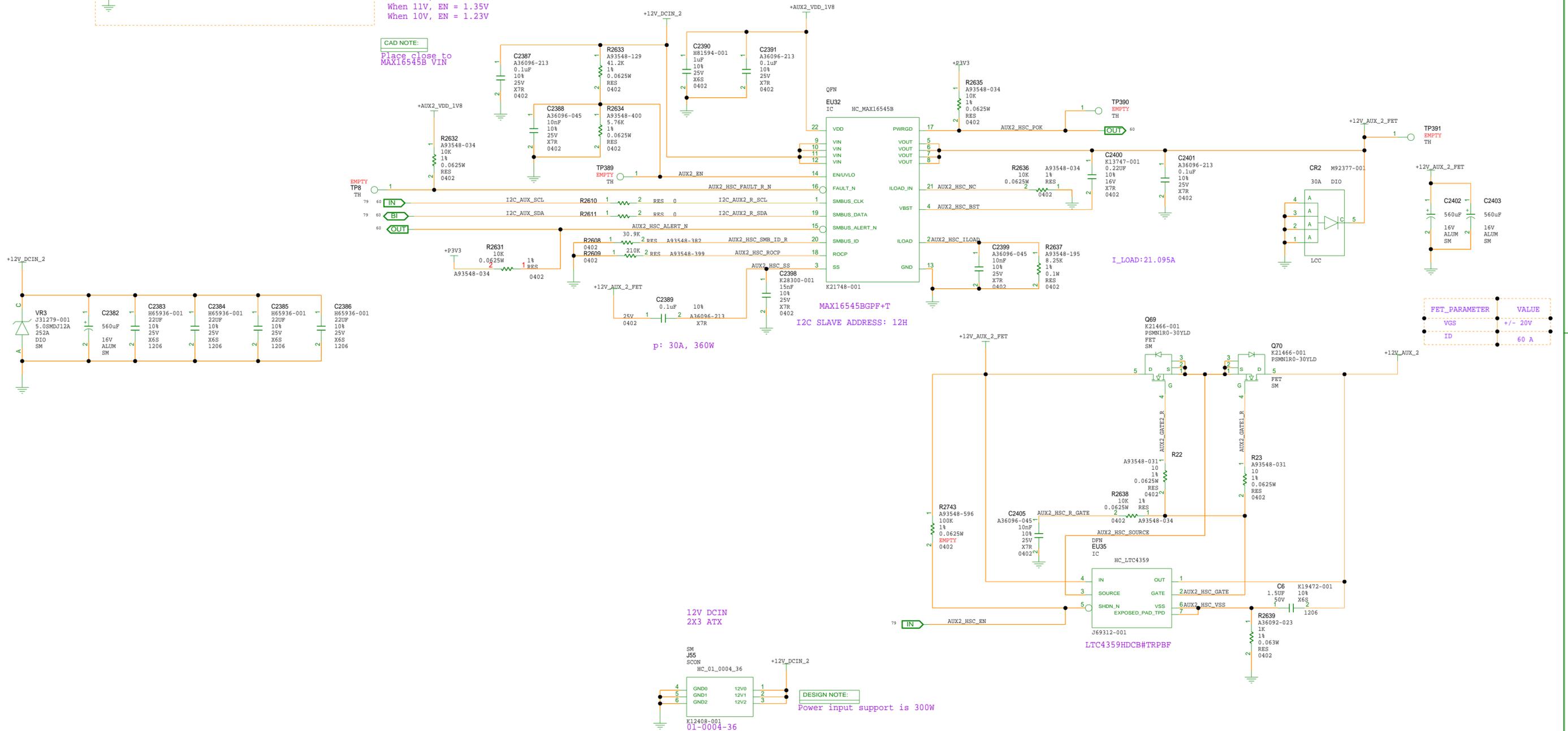
Wed Mar 6 15:45:51 2024

# POWER In- 12V\_AUX2 Hotswap



**DESIGN NOTE:**  
 When 16V, EN = 1.96V  
 When 15V, EN = 1.84V  
 When 14V, EN = 1.72V  
 When 13V, EN = 1.59V  
 When 12V, EN = 1.47V  
 When 11V, EN = 1.35V  
 When 10V, EN = 1.23V

**CAD NOTE:**  
 Place close to MAX16545B VIN



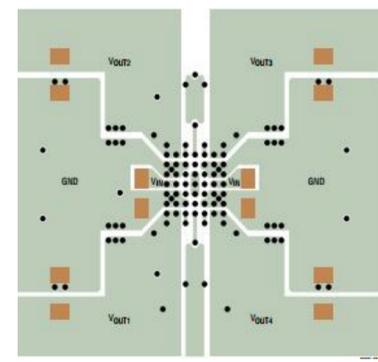
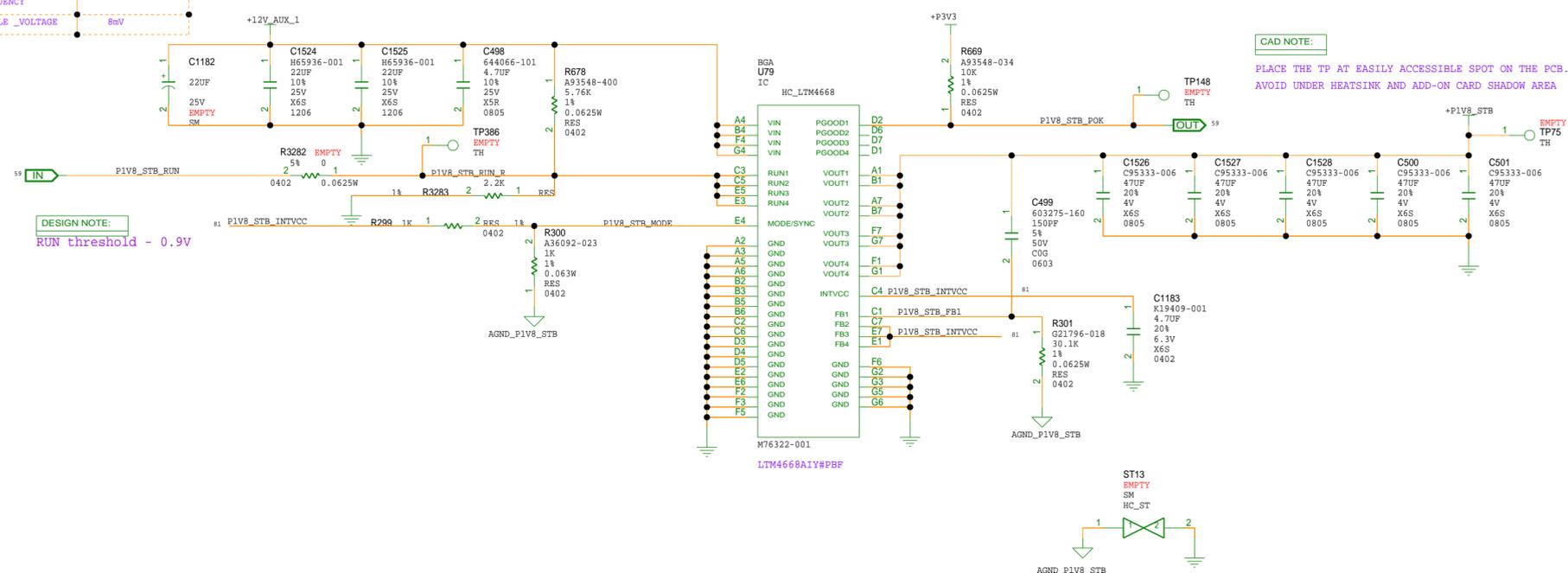
**DESIGN NOTE:**  
 Power input support is 300W

Wed Mar 6 15:45:52 2024

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
UNKNOWN	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 80 OF 105	

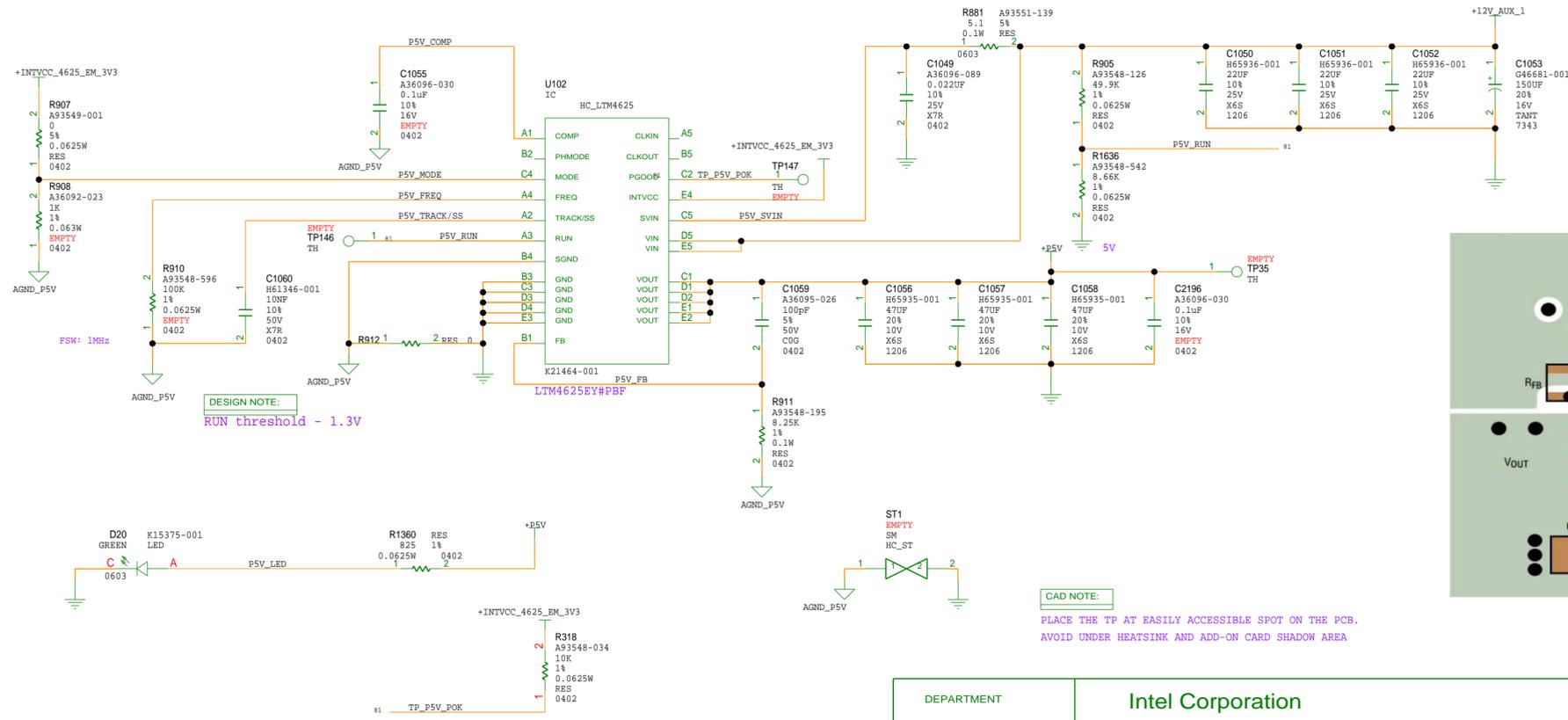
PARAMETER	VALUE
VOUT	1.8V
MAX CURRENT	4.5A
LOAD CURRENT	2.822A
FREQUENCY	
RIPPLE_VOLTAGE	8mV

### P1V8\_STB

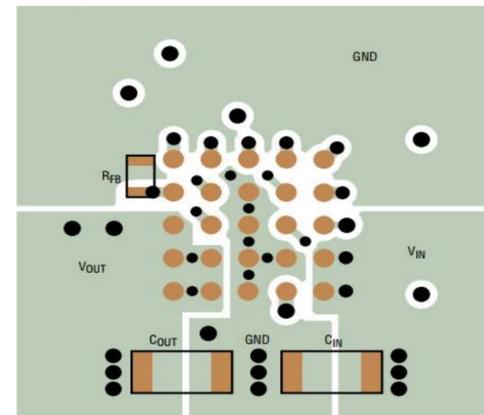


- #### RECOMMENDED LAYOUT GUIDELINES
- Use large PCB copper areas for high current paths, including  $V_{IN}$ , GND,  $V_{OUT1}$  and  $V_{OUT2}$ . It helps to minimize the PCB conduction loss and thermal stress.
  - Place high frequency ceramic input and output capacitors next to the  $V_{IN}$ , PGND and  $V_{OUT}$  pins to minimize high frequency noise.
  - Place a dedicated power ground layer underneath the unit.
  - To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
  - Do not put vias directly on the pad, unless they are capped or plated over.
  - Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
  - For parallel modules, tie the  $V_{OUT}$ ,  $V_{FB}$  and COMP pins together. Use an internal layer to closely connect these pins together. The TRACK pin can be tied a common capacitor for regulator soft-start.
  - Bring out test points on the signal pins for monitoring.

### PV5



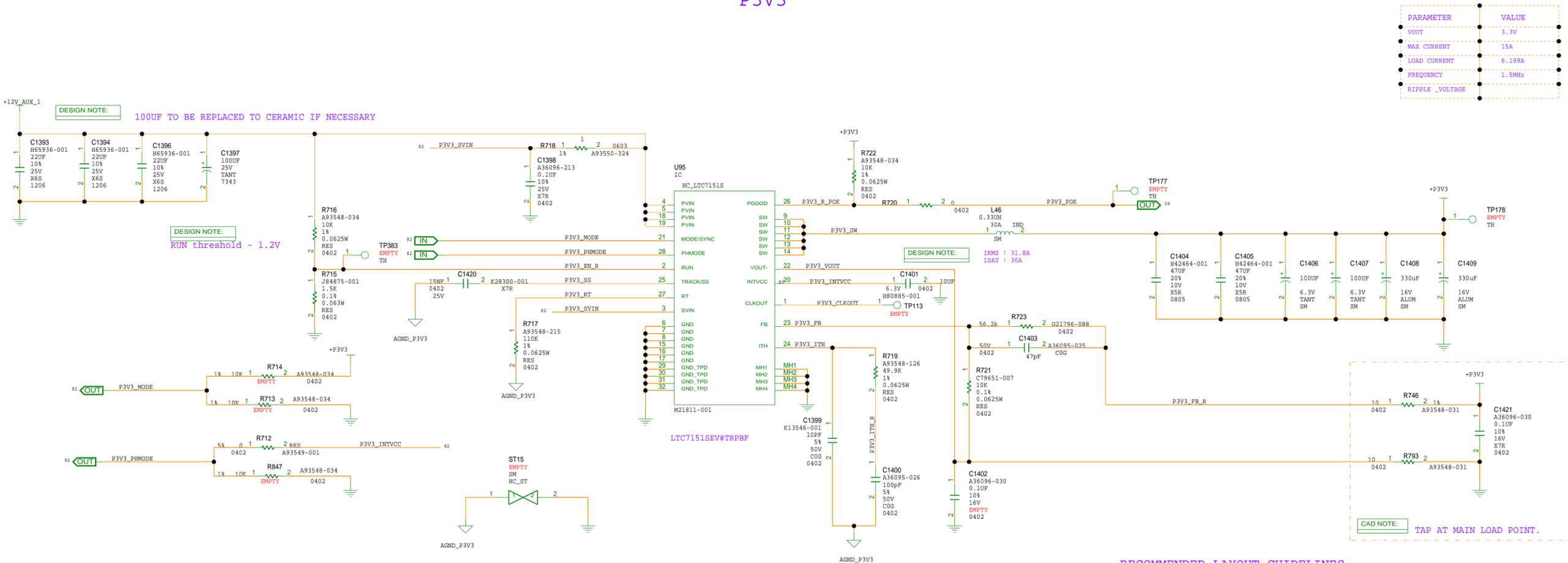
PARAMETER	VALUE
VOUT	5V
MAX CURRENT	5A
LOAD CURRENT	0.05A
FREQUENCY	1MHz
RIPPLE_VOLTAGE	5mV



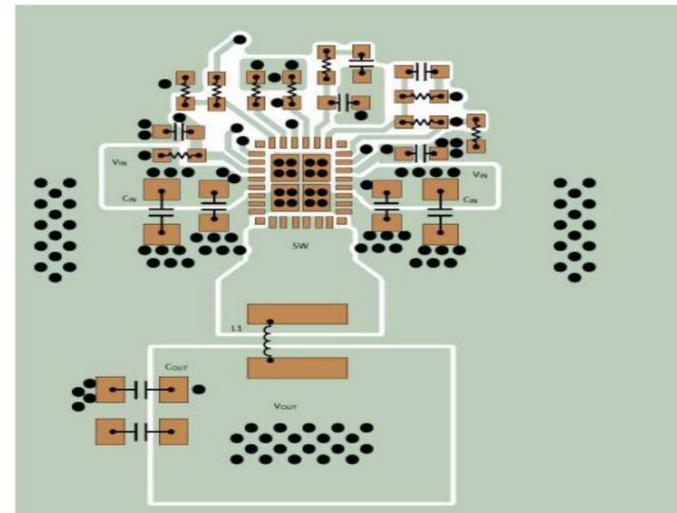
- #### RECOMMENDED LAYOUT GUIDELINES
- Use large PCB copper areas for high current paths, including  $V_{IN}$ , GND and  $V_{OUT}$ . It helps to minimize the PCB conduction loss and thermal stress.
  - Place high frequency ceramic input and output capacitors next to the  $V_{IN}$ , PGND and  $V_{OUT}$  pins to minimize high frequency noise.
  - Place a dedicated power ground layer underneath the unit.
  - To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
  - Do not put via directly on the pad, unless they are capped or plated over.
  - Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
  - Bring out test points on the signal pins for monitoring.
  - Keep separation between CLKIN, CLKOUT and FREQ pin traces to minimize possibility of noise due to crosstalk between these signals.

Wed Mar 6 15:45:52 2024

### P3V3



#### RECOMMENDED LAYOUT GUIDELINES



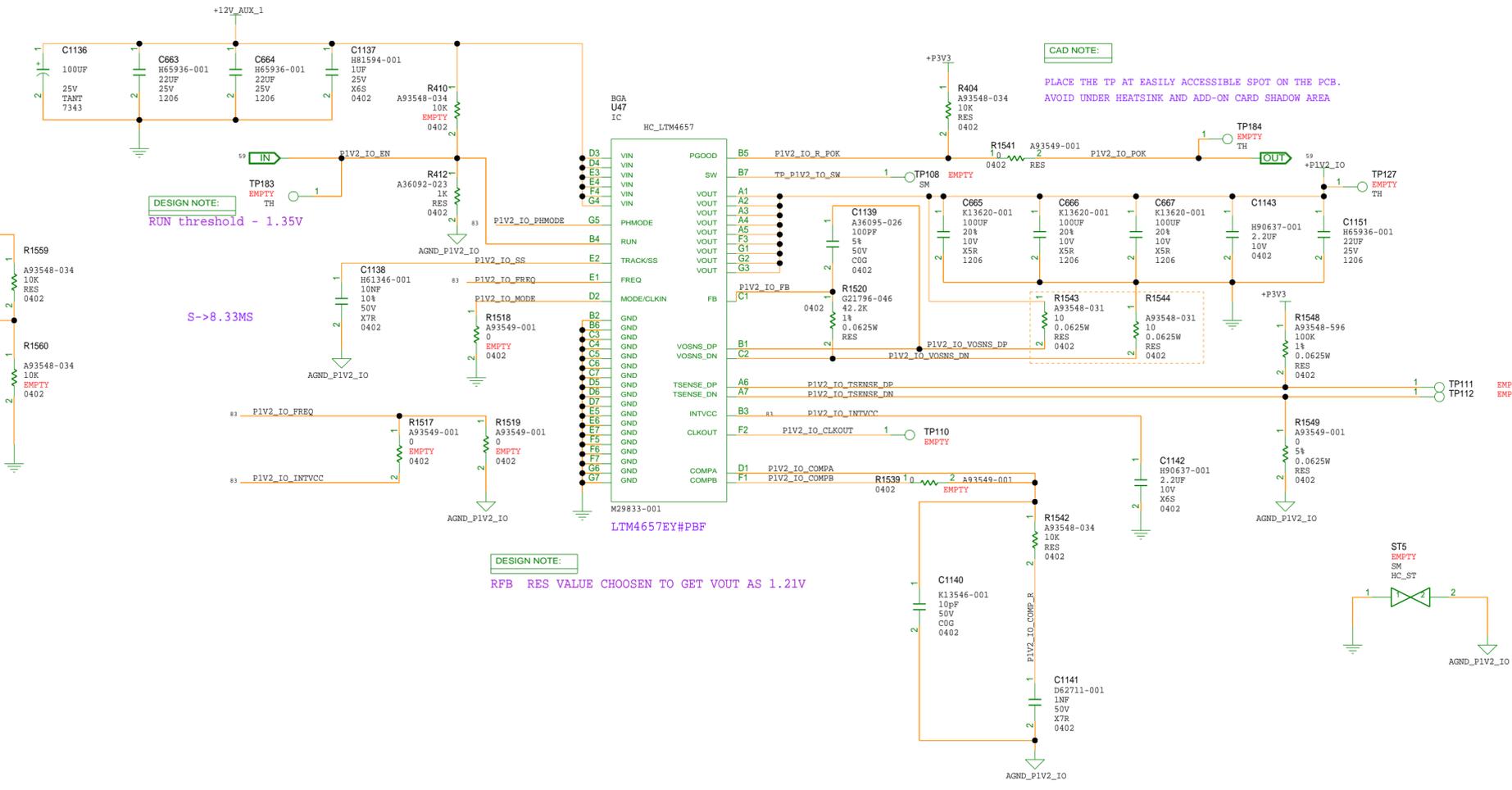
1. Are there pairs of capacitors ( $C_{IN}$ ) between  $V_{IN}$  and GND as close as possible on both sides of the package? These capacitors provide the AC current to the internal power MOSFETs and their drivers as well as minimize EMI/EMC emissions.
2. Are  $C_{OUT}$  and L closely connected? The (-) plate of  $C_{OUT}$  returns current to GND and the (-) plate of  $C_{IN}$ .
3. Place the FB dividers close to the part with Kelvin connections to  $V_{OUT}$  and  $V_{OUT-}$  at the point-of-load, for differential  $V_{OUT}$  sensing.
4. Keep sensitive components away from the SW pin. The FB resistors,  $R_T$  resistor, the compensation component, and the  $INTV_{CC}$  bypass caps should be routed away from the SW trace and the inductor.

Wed Mar 6 15:45:53 2024

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 82 OF 105	

# P1V2\_IO

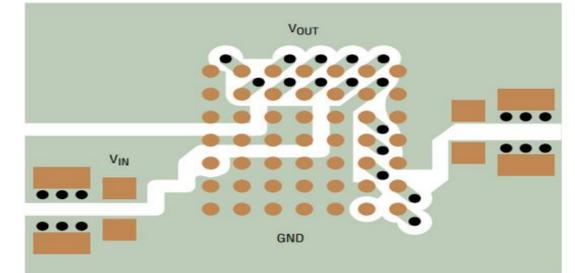
PARAMETER	VALUE
V <sub>OUT</sub>	1.2V
MAX CURRENT	8A
LOAD CURRENT	6.523A
FREQUENCY	500KHz
RIPPLE_VOLTAGE	5mV



## RECOMMENDED LAYOUT GUIDELINES

- Use large PCB copper areas for high current paths, including V<sub>IN</sub>, GND and V<sub>OUT</sub>. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V<sub>IN</sub>, PGND and V<sub>OUT</sub> pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Bring out test points on the signal pins for monitoring.
- Keep separation between CLKIN, CLKOUT and FREQ pin traces to minimize possibility of noise due to cross-talk between these signals.

Figure 22 gives a good example of the recommended layout.



Wed Mar 6 15:45:53 2024

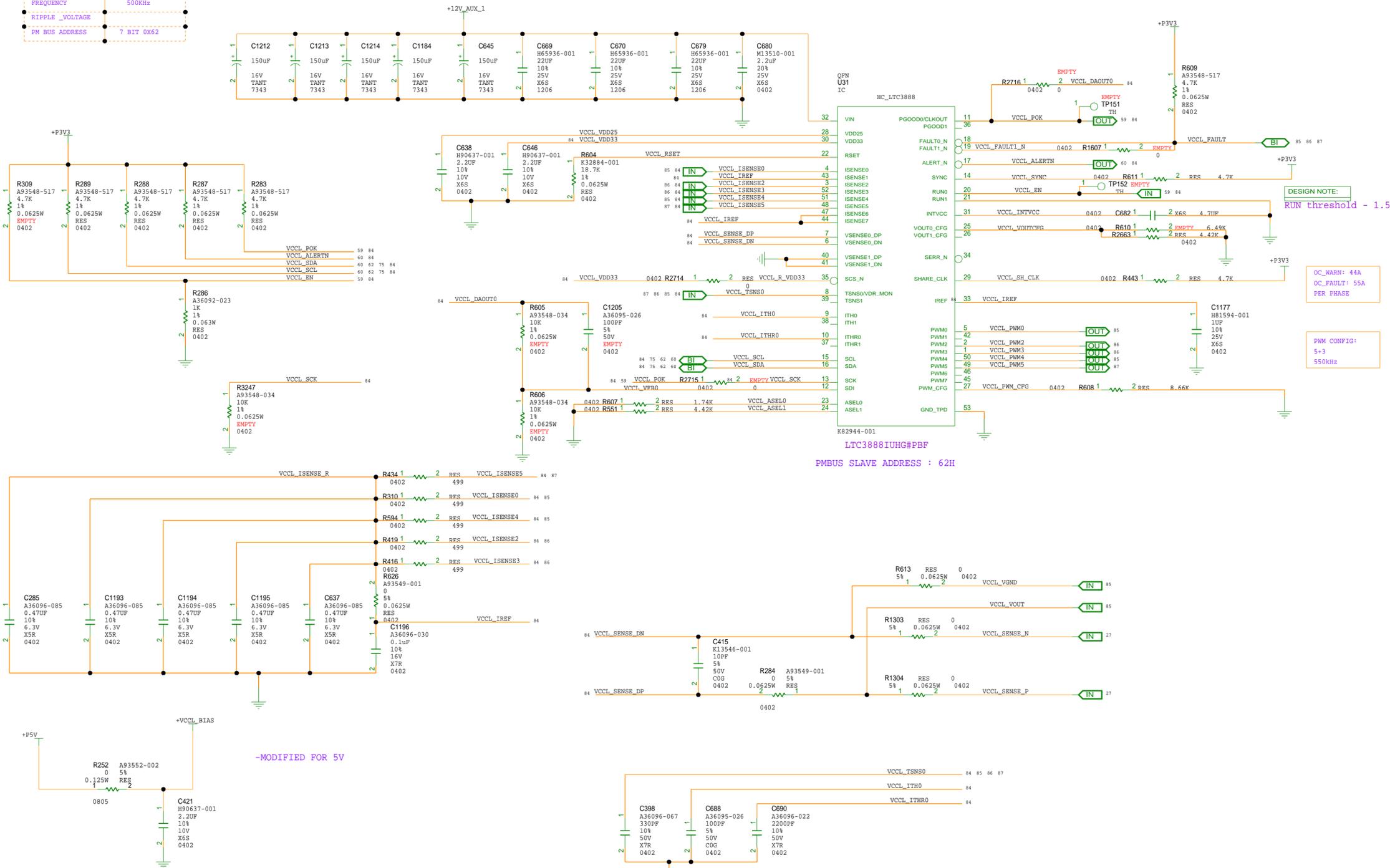
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PGG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 83 OF 105	

# VCCL CONTROLLER

PARAMETER	VALUE
VOUT	0.8V
MAX CURRENT	300A
LOAD CURRENT	248.93A
FREQUENCY	500KHz
RIPPLE_VOLTAGE	
PW BUS ADDRESS	7 BIT 0x62

**DESIGN NOTE:**

This is configured for LTC3888 with option for LTC3888-1 BOM stuffing



**RECOMMENDED LAYOUT GUIDELINES**

- Place a ground or DC voltage layer between a power layer and a small-signal layer. Generally, power planes should be placed on the top layer (4-layer PCB), or top and bottom layer if more than 4 layers are used. Use wide/short copper traces for power components and avoid improper use of thermal relief around power plane vias to minimize resistance and inductance.
- Low ESR input capacitors should be placed as close as possible to the power stage FET supply and ground connections with the shortest copper traces possible. The power stage must be on the same layer of copper as the input capacitors with a common topside power connection at C<sub>IN</sub>. Do not attempt to split the input decoupling for multiple phases, as a large resonant loop can result. Vias should not be used to make these connections. Avoid blocking forced air flow to the power stages with large size passive components.
- Place the inductor input as close as possible to the power stage. Minimize the surface area of the switch node. Make the trace width the minimum needed to support the maximum output current. Avoid copper fills or pours. Avoid running the connection on multiple copper layers in parallel. Minimize capacitance from the switch node to any other trace or plane.
- PCB traces for remote voltage sense should be run together back to the LTC3888 in pairs with the smallest spacing possible on any given layer on which they are routed. Avoid high frequency switching signals and ideally shield with ground planes. Locate any filter component on these traces next to the LTC3888, and not at the Kelvin sense location.
- PCB traces for output current sense (I<sub>SENSE</sub>, I<sub>REF</sub>) should avoid high frequency switching signals and ideally be shielded with ground planes. Filter components on these traces should return to GND (IC paddle) and not to a local PGND.
- Place low ESR output capacitors adjacent to the inductor output and ground. Output capacitor ground connections must feed into the same copper that connects to the input capacitor ground before connecting back to system ground.
- Connection of switching ground to system ground, small-signal analog ground or any internal ground plane should be single-point. If the system has an internal system ground plane, a good way to do this is to cluster vias into a single star point to make the connection. This cluster should be located directly beneath the IC GND paddle, which serves as analog signal ground. A useful CAD technique is to make separate ground nets and use a 0Ω resistor to connect them to system ground.
- Place all small-signal components away from high frequency switching nodes. Place decoupling capacitors for the LTC3888 immediately adjacent to the IC.
- A good rule of thumb for via count in a given high current path is to use 0.5A per via. Be consistent when applying this rule.
- Copper fills or pours are good for all power connections except as noted above in rule 3. Copper planes on multiple layers can also be used in parallel. This helps with thermal management and lowers trace inductance, which further improves EMI performance.

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PGO	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SCALE:		DO NOT SCALE DRAWING		SHEET	84 OF 105		

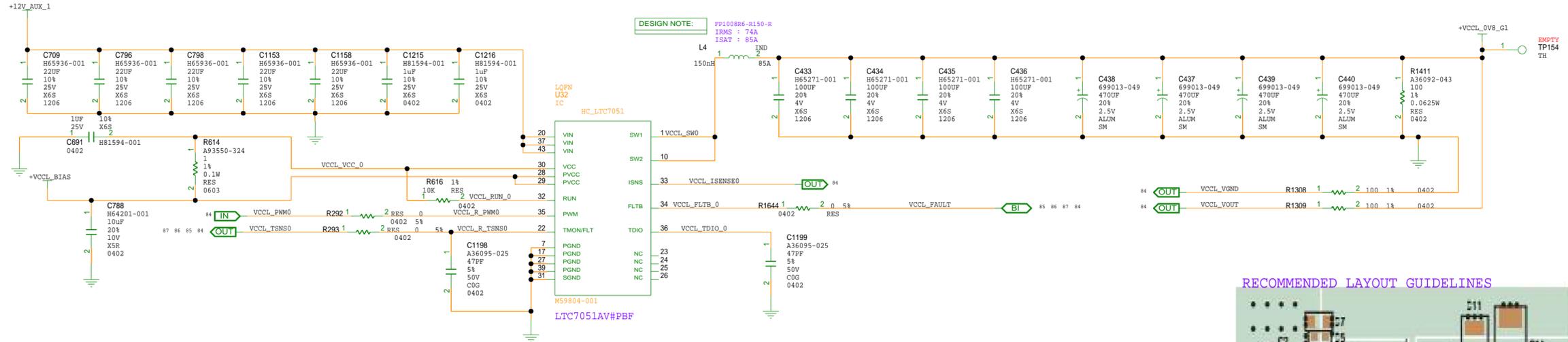
4

3

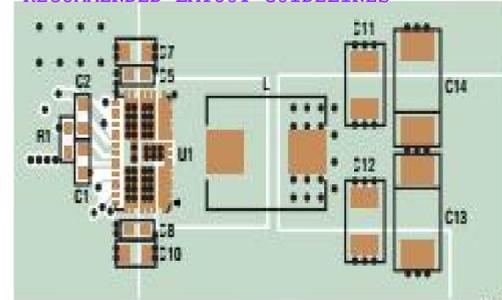
2

1

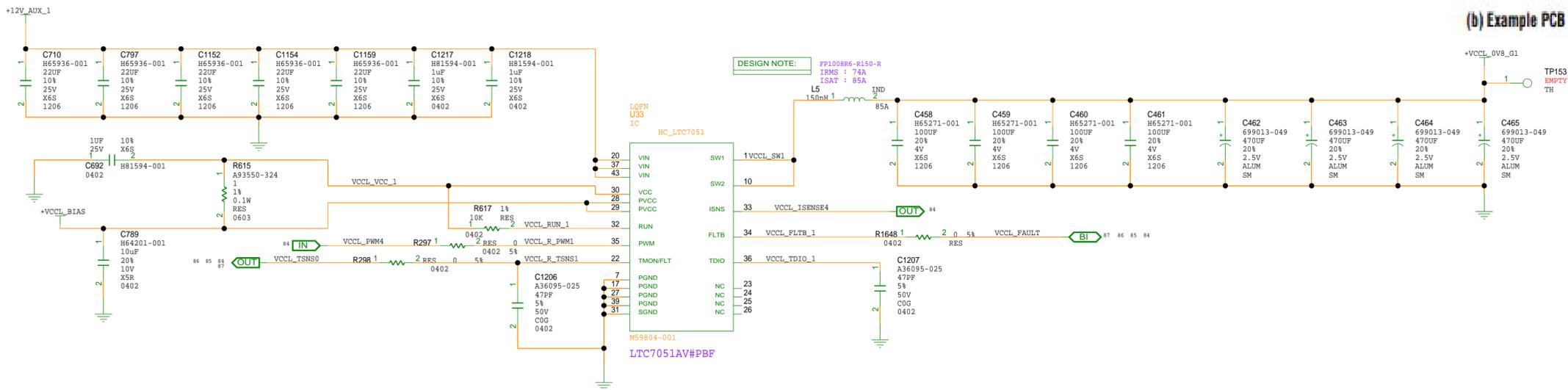
### CORE FETS



### RECOMMENDED LAYOUT GUIDELINES



(b) Example PCB Layout



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4

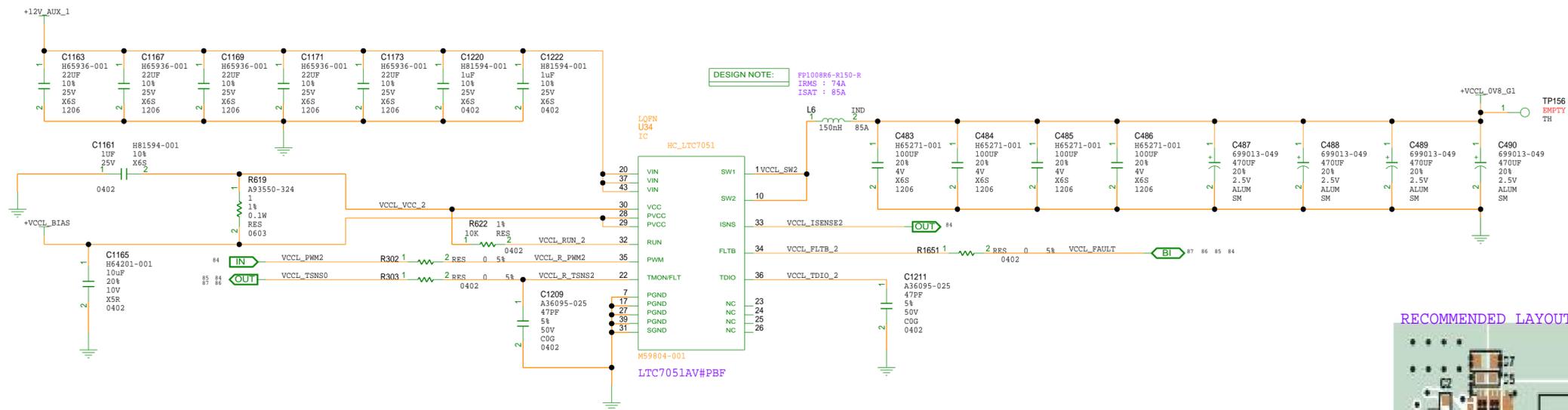
3

2

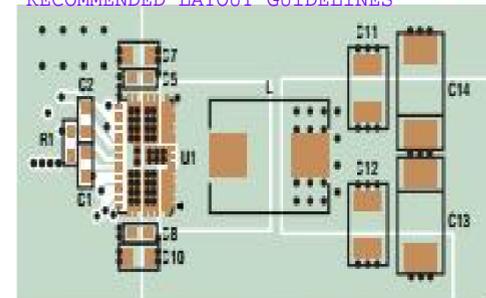
1

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PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 85 OF 105

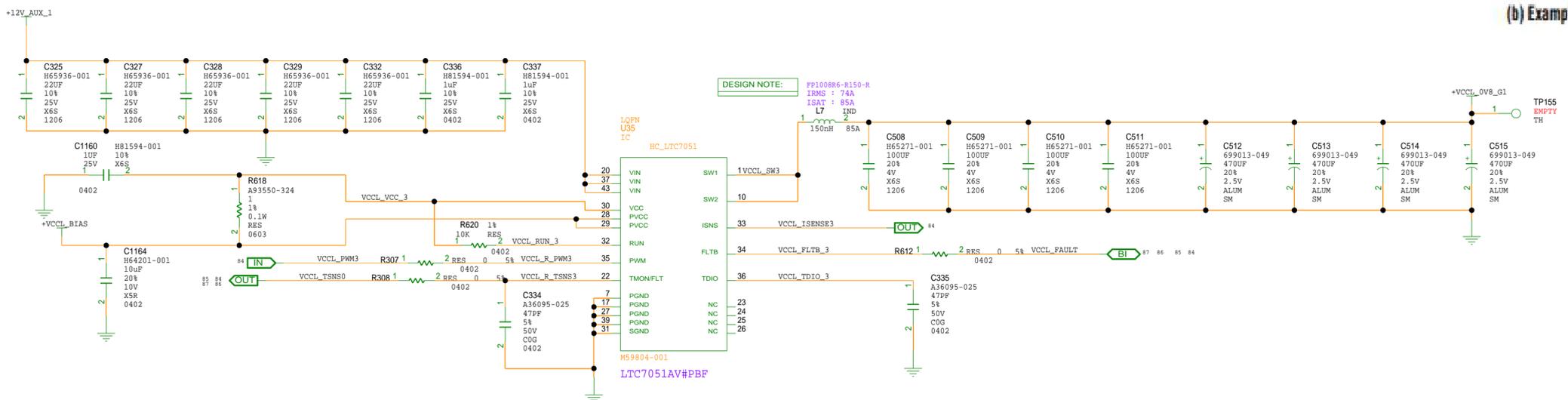
### CORE FETS



### RECOMMENDED LAYOUT GUIDELINES



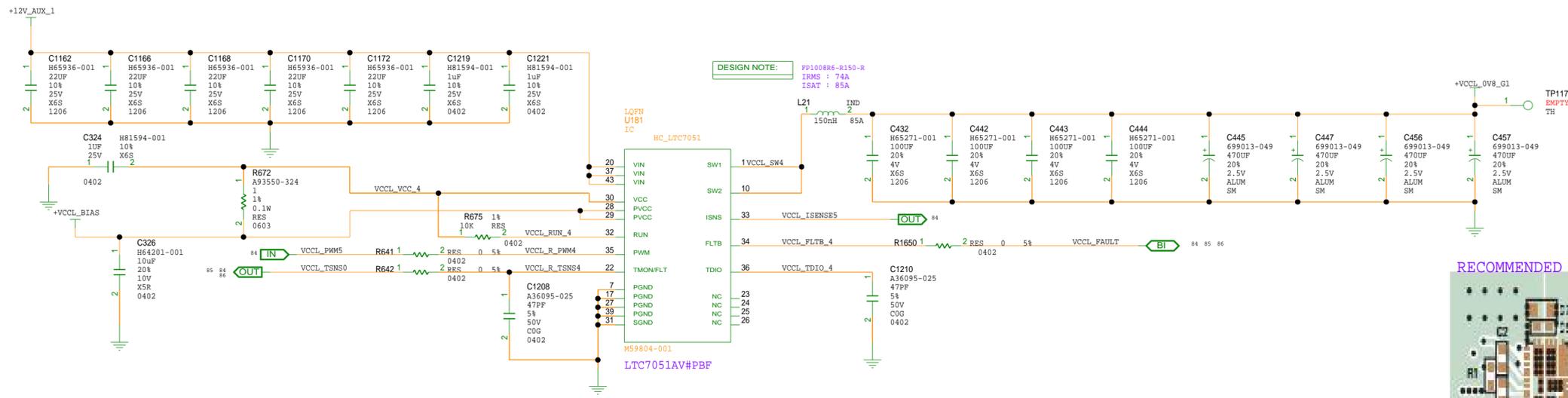
(b) Example PCB Layout



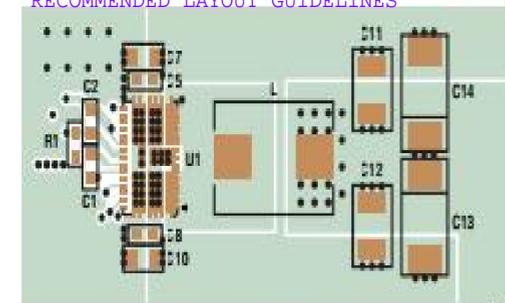
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PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 86 OF 105

### CORE FETS



### RECOMMENDED LAYOUT GUIDELINES



(b) Example PCB Layout

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DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
UNKNOWN	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 87 OF 105

### VCC\_HSSI\_GXF\_OV8\_UX0\_G1

PARAMETER	VALUE
VOUT	0.8V
MAX CURRENT	36A(SINGLE)
LOAD CURRENT	29.067A
FREQUENCY	500KHz
RIPPLE_VOLTAGE	10mV
PM BUS ADDRESS	7 BIT 0X40

I2C SLAVE ADDRESS: 40H

CAD NOTE:

PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB. AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

CAD NOTE:

PLEASE THIS BULK CAP ON THE SAME SIDE AS IC

DESIGN NOTE:

Vout config: 0.9V  
Vtrim: -99mV

CAD NOTE:

CONNECT NEAR FPGA BGA REGION. NEED TO ROUTE AS KELVIN SENSE

DESIGN NOTE:

RUN threshold - 1.35V

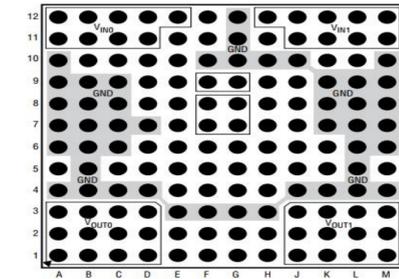
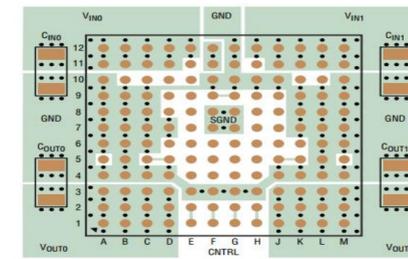
#### RECOMMENDED LAYOUT GUIDELINES

- Use large PCB copper areas for high current paths, including  $V_{INn}$ , GND and  $V_{OUTn}$ . It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the  $V_{INn}$ , GND and  $V_{OUTn}$  pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the module.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on pads, unless they are capped or plated over.

- Use a separate SGND copper plane for components connected to signal pins. Connect SGND to GND local to the LTM4677.

- For parallel modules, tie the  $V_{OUTn}$ ,  $V_{OSNS0+}/V_{OSNS-}$  and/or  $V_{OSNS1}/SGND$  voltage-sense differential pair lines,  $RUNn$ ,  $GPIO_n$ ,  $COMPn$ ,  $SYNC$  and  $SHARE\_CLK$  pins together—as shown in Figure 29.

- Bring out test points on the signal pins for monitoring. Figure 26 gives a good example of the recommended layout.



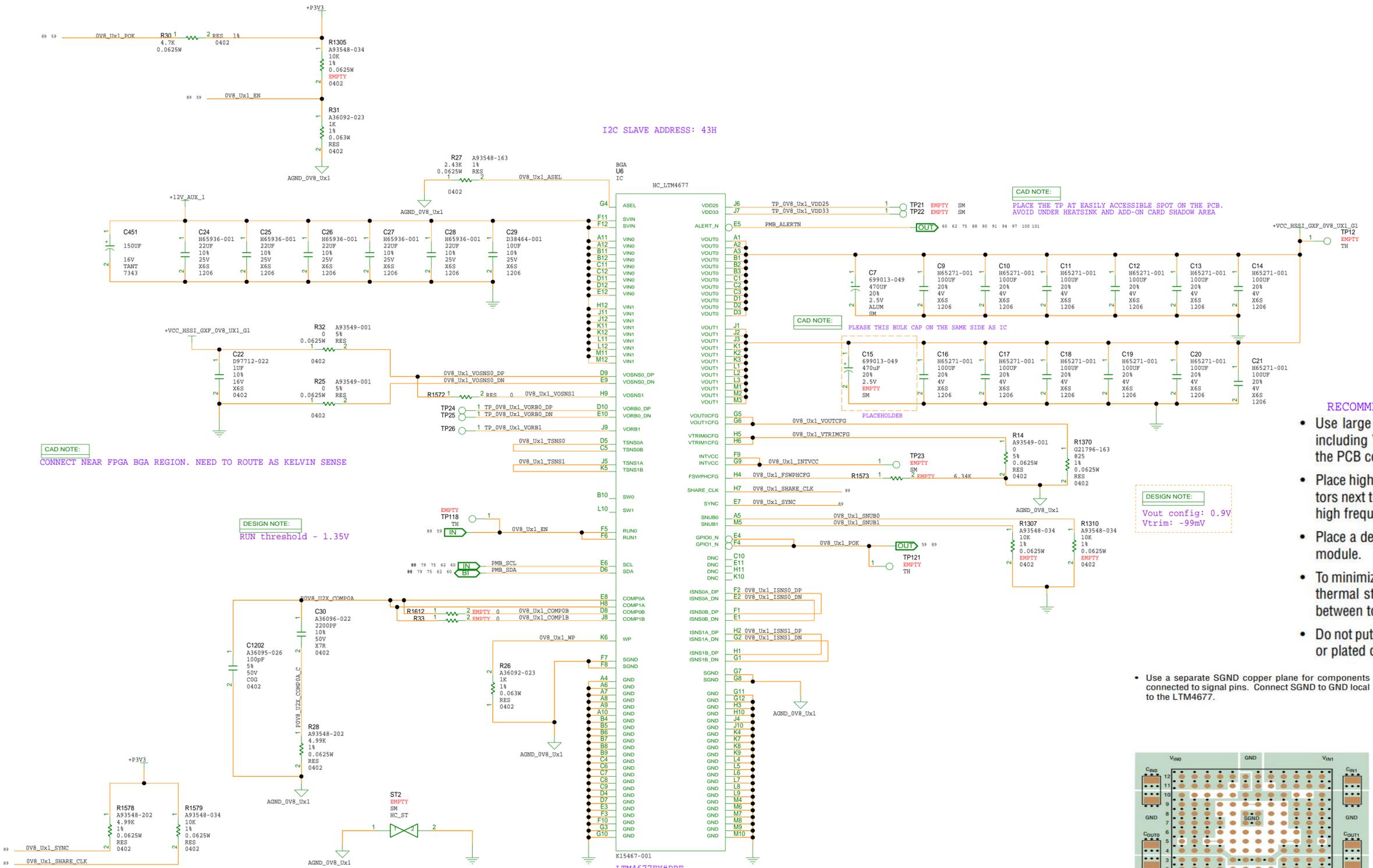
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SCALE:	DO NOT SCALE DRAWING	SHEET		88 OF 105	

# VCC\_HSSI\_GXF\_0V8\_UX1\_G1

I2C SLAVE ADDRESS: 43H

PARAMETER	VALUE
VOUT	0.8V
MAX CURRENT	36A(SINGLE)
LOAD CURRENT	28.787A
FREQUENCY	500kHz
RIPPLE_VOLTAGE	10mV
PM BUS ADDRESS	7 BIT 0x43



CAD NOTE:  
CONNECT NEAR FPGA BGA REGION. NEED TO ROUTE AS KELVIN SENSE

DESIGN NOTE:  
RUN threshold - 1.35V

CAD NOTE:  
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB. AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

CAD NOTE:  
PLEASE THIS BULK CAP ON THE SAME SIDE AS IC

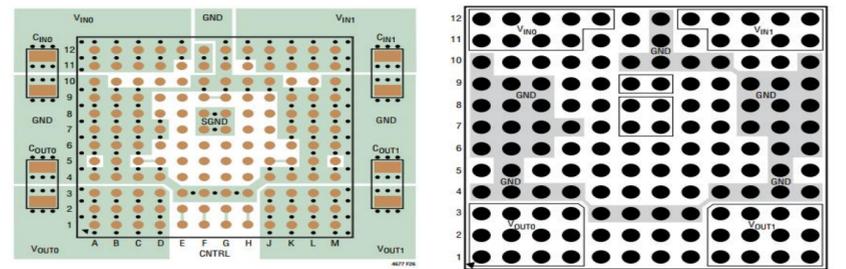
DESIGN NOTE:  
Vout config: 0.9V  
Vtrim: -99mV

### RECOMMENDED LAYOUT GUIDELINES

- Use large PCB copper areas for high current paths, including  $V_{INn}$ , GND and  $V_{OUTn}$ . It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the  $V_{INn}$ , GND and  $V_{OUTn}$  pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the module.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on pads, unless they are capped or plated over.

• Use a separate SGND copper plane for components connected to signal pins. Connect SGND to GND local to the LTM4677.

• For parallel modules, tie the  $V_{OUTn}$ ,  $V_{OSNS0+}/V_{OSNS-}$  and/or  $V_{OSNS1}/SGND$  voltage-sense differential pair lines,  $RUN_n$ ,  $GPIO_n$ ,  $COMP_{na}$ ,  $SYNC$  and  $SHARE\_CLK$  pins together—as shown in Figure 29.  
• Bring out test points on the signal pins for monitoring. Figure 26 gives a good example of the recommended layout.



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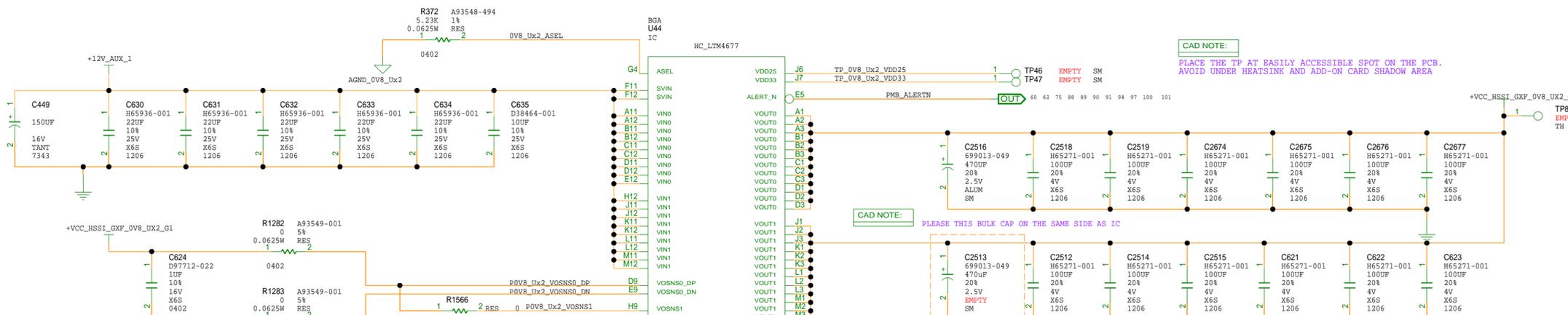
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 89 OF 105	

VCC\_HSSI\_GXF\_OV8\_UX2\_G1



I2C SLAVE ADDRESS: 46H

PARAMETER	VALUE
VOUT	0.8V
MAX CURRENT	36A(SINGLE)
LOAD CURRENT	28.787A
FREQUENCY	500KHz
RIPPLE_VOLTAGE	10mV
PM BUS ADDRESS	7 BIT 0X46



CAD NOTE: PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB. AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA.

CAD NOTE: PLEASE THIS BULK CAP ON THE SAME SIDE AS IC

CAD NOTE: CONNECT NEAR FPGA BGA REGION. NEED TO ROUTE AS KELVIN SENSE

DESIGN NOTE: RUN threshold - 1.35V

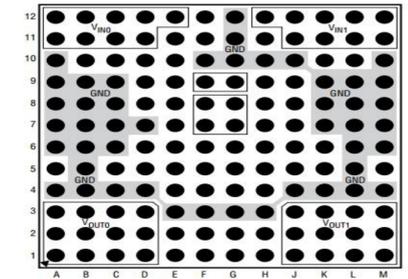
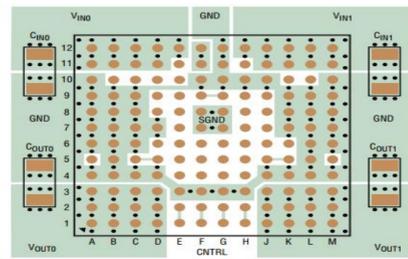
DESIGN NOTE: Vout config: 0.9V Vtrim: -99mV

RECOMMENDED LAYOUT GUIDELINES

- Use large PCB copper areas for high current paths, including  $V_{INn}$ , GND and  $V_{OUTn}$ . It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the  $V_{INn}$ , GND and  $V_{OUTn}$  pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the module.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on pads, unless they are capped or plated over.

- Use a separate SGND copper plane for components connected to signal pins. Connect SGND to GND local to the LTM4677.
- For parallel modules, tie the  $V_{OUTn}$ ,  $V_{OSNSn+}/V_{OSNSn-}$  and/or  $V_{OSNSn+}/SGND$  voltage-sense differential pair lines,  $RUNn$ ,  $GPIO_n$ ,  $COMP_n$ ,  $SYNC$  and  $SHARE\_CLK$  pins together—as shown in Figure 29.
- Bring out test points on the signal pins for monitoring.

Figure 26 gives a good example of the recommended layout.

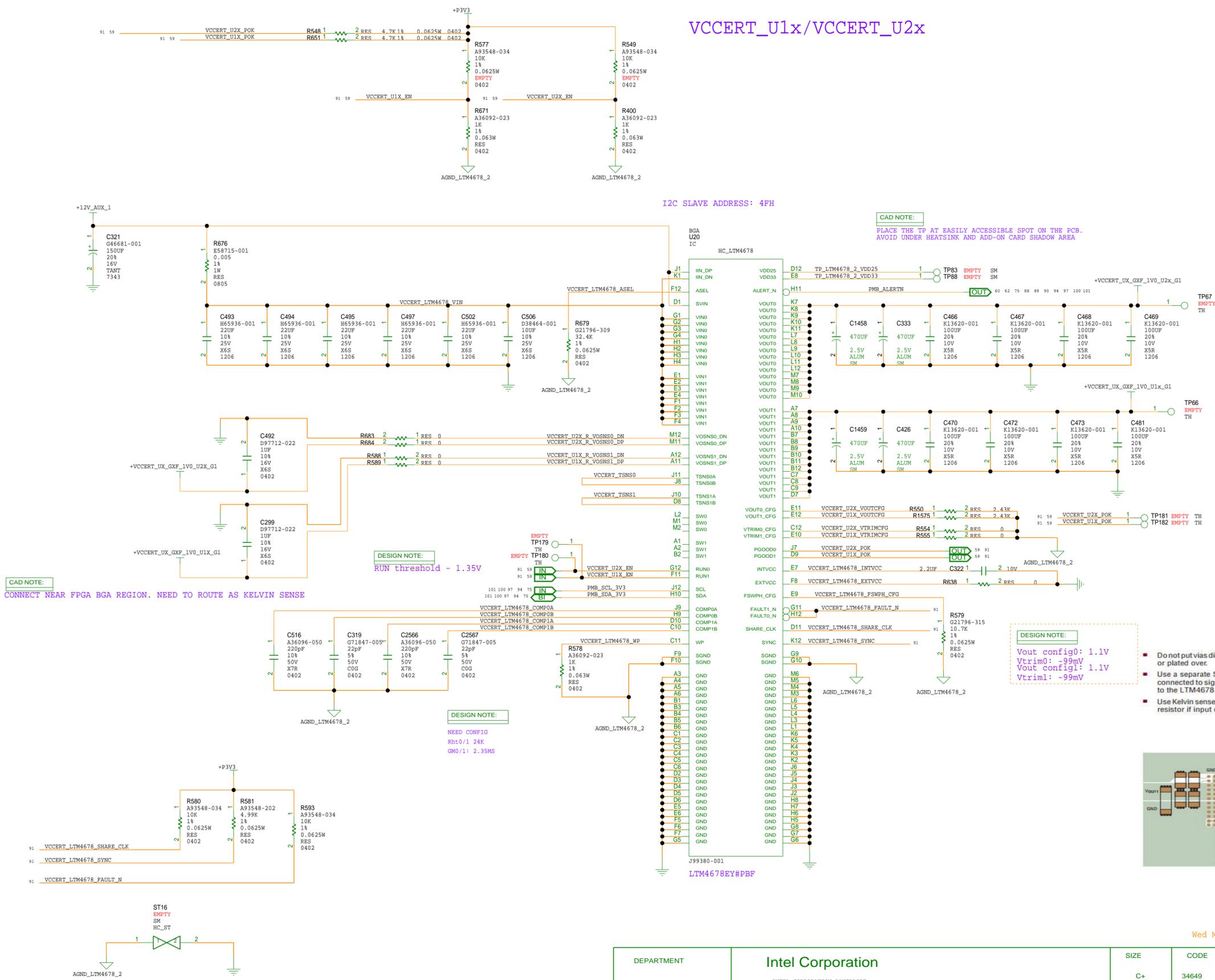


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SCALE:		DO NOT SCALE DRAWING		SHEET 90 OF 105	

### VCCERT\_U1x/VCCERT\_U2x

PARAMETER	VALUE
VOUT_1	1V
VOUT_2	1V
MAX CURRENT	25A(DUAL)
LOAD CURRENT_1	19.585A
LOAD CURRENT_2	19.585A
FREQUENCY	750KHZ
RIPPLE_VOLTAGE	10mV
PM BUS ADDRESS	7 BIT 0X4F



I2C SLAVE ADDRESS: 4FH

CAD NOTE:  
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.  
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

DESIGN NOTE:  
RUN threshold - 1.35V

DESIGN NOTE:  
Vout config0: 1.1V  
Vtrim0: -99mV  
Vout config1: 1.1V  
Vtrim1: -99mV

DESIGN NOTE:  
NEED CONFIG  
Rht:0/1 24K  
GMD/1: 2.25MS

CAD NOTE:  
CONNECT NEAR FPGA BGA REGION. NEED TO ROUTE AS KELVIN SENSE

#### RECOMMENDED LAYOUT GUIDELINES

- Use large PCB copper areas for high current paths, including  $V_{INn}$ , GND and  $V_{OUTn}$ . It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the  $V_{INn}$ , GND and  $V_{OUTn}$  pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the module.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.

- Do not put vias directly on pads, unless they are capped or plated over.
  - Use a separate SGND copper plane for components connected to signal pins. Connect SGND to GND local to the LTM4678.
  - Use Kelvin sense connections across the input  $R_{SENSE}$  resistor if input current monitoring is used.
- For parallel modules, tie the  $V_{OUTn}$ ,  $V_{OSNSn}$ ,  $V_{OSNSn}$  voltage-sense differential pair lines,  $RUNn$ ,  $COMPn$ ,  $COMPn$  pin together.
- The user must share the SYNC, SHARE\_CLK, FAULT, and ALERT pins of these parts. Be sure to use pull-up resistors on FAULT, SHARE\_CLK and ALERT.
  - Bring out test points on the signal pins for monitoring. Figure 44 gives a good example of the recommended layout.

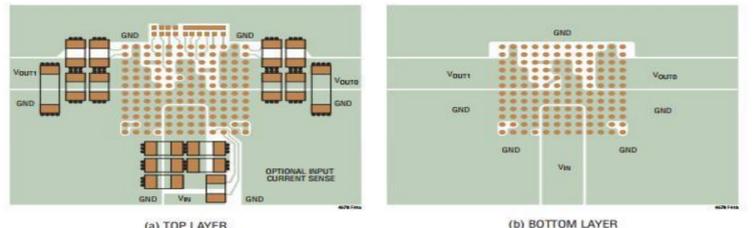


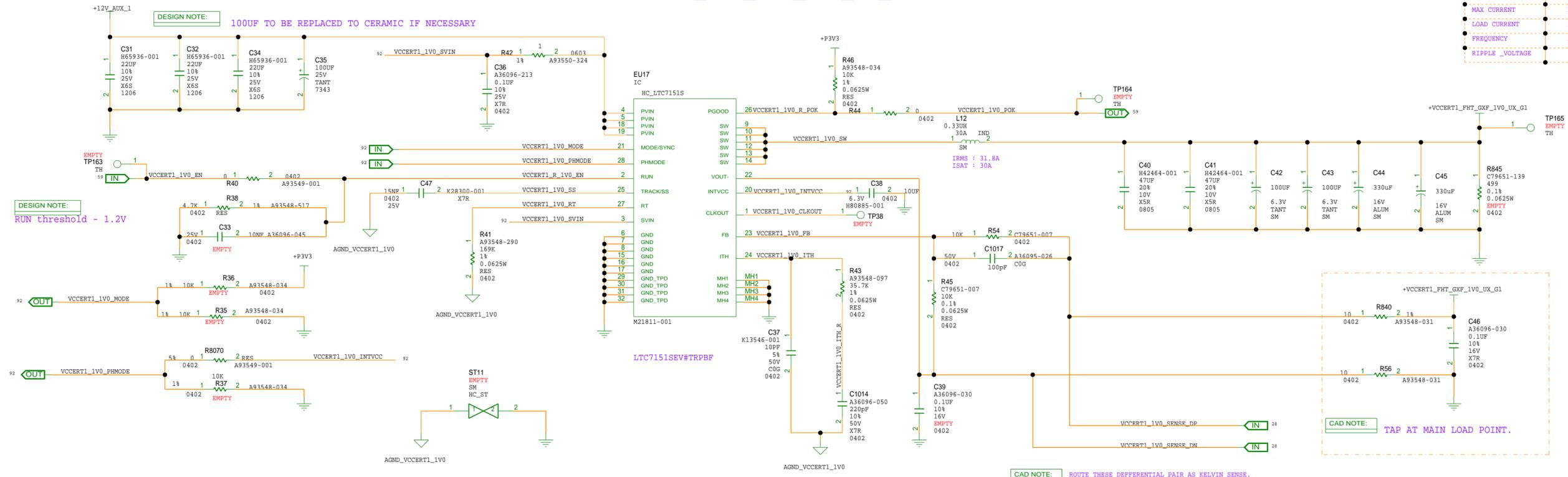
Figure 44. Recommended PCB Layout Package Top View

Wed Mar 6 15:45:57 2024

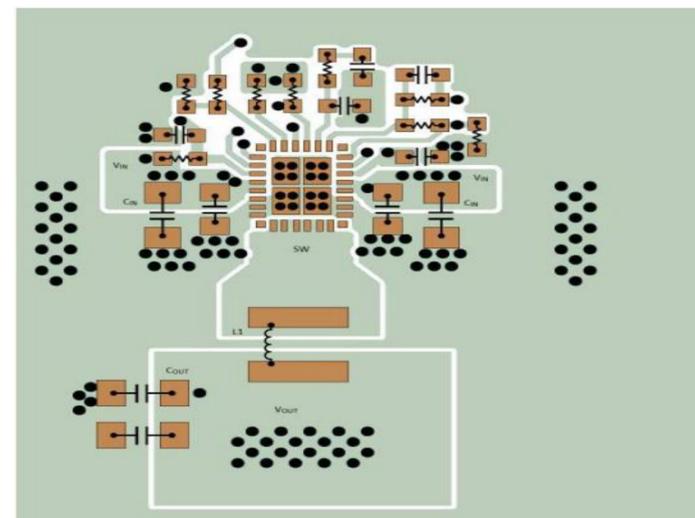
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PGG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 91 OF 105	

### VCCERT1\_FHT\_GXF\_1V0\_UX\_G1

PARAMETER	VALUE
VOUT	1V
MAX CURRENT	15A
LOAD CURRENT	12.2A
FREQUENCY	1MHz
RIPPLE_VOLTAGE	



#### RECOMMENDED LAYOUT GUIDELINES

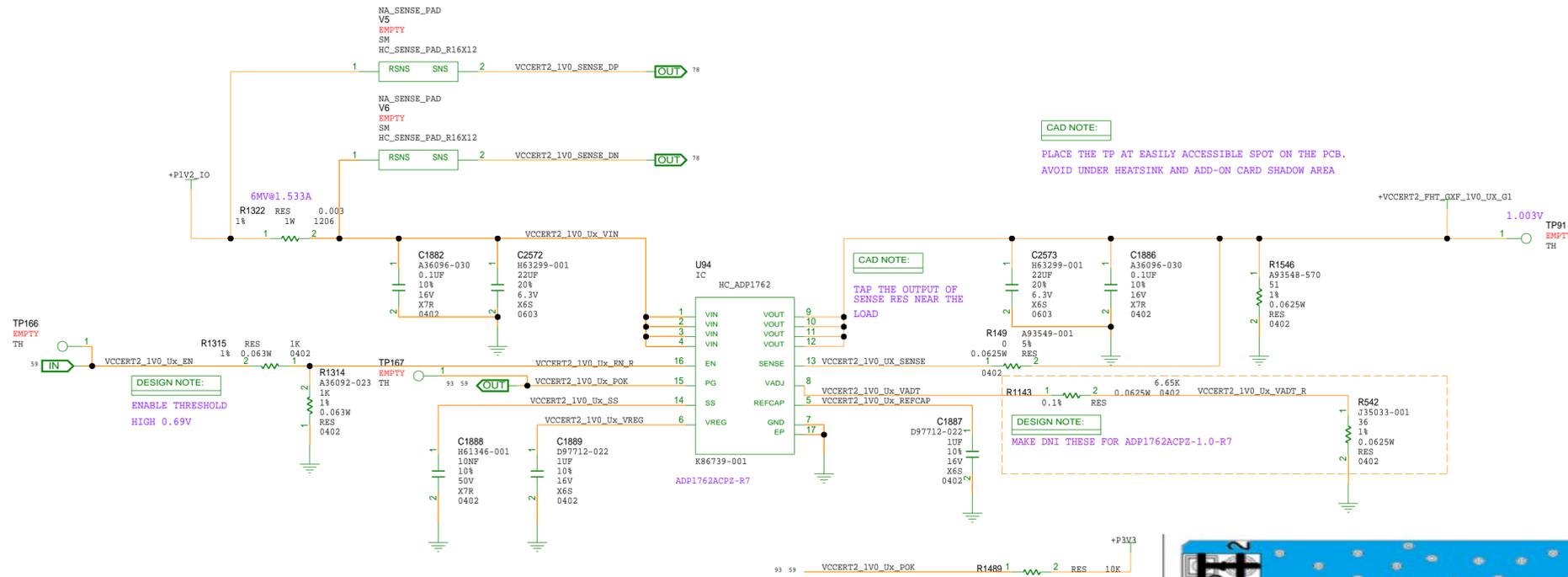


1. Are there pairs of capacitors ( $C_{IN}$ ) between  $V_{IN}$  and GND as close as possible on both sides of the package? These capacitors provide the AC current to the internal power MOSFETs and their drivers as well as minimize EUI/EMC emissions.
2. Are  $C_{OUT}$  and L closely connected? The (-) plate of  $C_{OUT}$  returns current to GND and the (-) plate of  $C_{IN}$ .
3. Place the FB dividers close to the part with Kelvin connections to  $V_{OUT}$  and  $V_{OUT-}$  at the point-of-load, for differential  $V_{OUT}$  sensing.
4. Keep sensitive components away from the SW pin. The FB resistors,  $R_T$  resistor, the compensation component, and the  $INTV_{CC}$  bypass caps should be routed away from the SW trace and the inductor.

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SCALE:		DO NOT SCALE DRAWING		SHEET 92 OF 105	

### VCCERT2\_FHT\_GXF\_1V0\_UX\_G1



PARAMETER	VALUE
VOUT	1V
MAX CURRENT	2A
LOAD CURRENT	1.533A
FREQUENCY	
RIPPLE_VOLTAGE	

#### RECOMMENDED LAYOUT GUIDELINES

- Place the input capacitor as close as possible to the VIN and GND pins.
- Place the output capacitor as close as possible to the VOUT and GND pins.
- Place the soft start capacitor (C<sub>SS</sub>) as close as possible to the SS pin.
- Place the reference capacitor (C<sub>REF</sub>) and regulator capacitor (C<sub>REG</sub>) as close as possible to the REFCAP pin and the VREG pin, respectively.
- Connect the load as close as possible to the VOUT and SENSE pins.

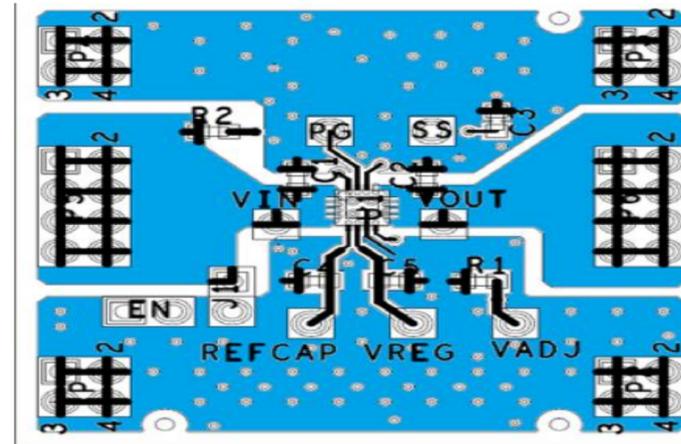


Figure 45. Typical Board Layout, Top Side

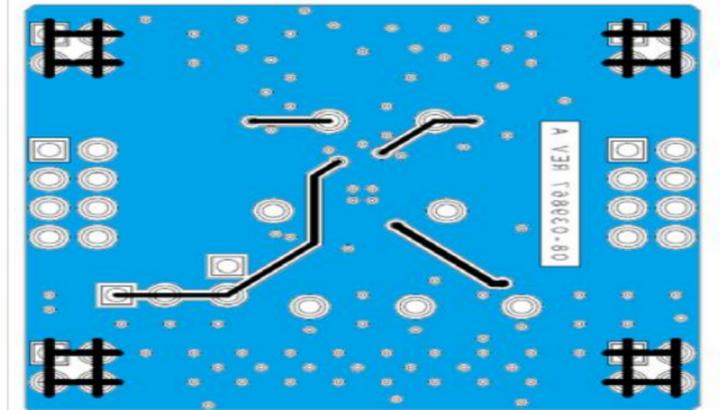


Figure 46. Typical Board Layout, Bottom Side

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PSG	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 93 OF 105



PARAMETER	VALUE
VOUT	1.5V
MAX CURRENT	2A
LOAD CURRENT	1.18A
FREQUENCY	
RIPPLE_VOLTAGE	

**DESIGN NOTE:**  
ENABLE THRESHOLD HIGH 1.31V

PARAMETER	VALUE
VOUT	2.5V
MAX CURRENT	8A
LOAD CURRENT	4.413A
FREQUENCY	1MHZ
RIPPLE_VOLTAGE	5mV

**DESIGN NOTE:**  
RUN threshold - 1.35V  
S->0.833MS

### VCCEHT\_FHT\_GXF\_1V5\_U1X\_G2

**CAD NOTE:**  
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.  
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

**CAD NOTE:**  
PLACE THESE NEAR TO VR

### P2V5\_G2

**CAD NOTE:**  
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.  
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

#### RECOMMENDED LAYOUT GUIDELINES

Place the input capacitor as close as possible between the VIN pin and ground. Place the output capacitor as close as possible between the VOUT pin and ground. Place the bypass capacitors (C<sub>REG</sub>, C<sub>REF</sub>, and C<sub>BYP</sub>) for V<sub>REG</sub>, V<sub>REF</sub>, and V<sub>BYP</sub> close to the respective pins (V<sub>REG</sub>, REF, and BYP) and ground. The use of a 0805, a 0603, or a 0402 size capacitor achieves the smallest possible footprint solution on boards where area is limited. Maximize the amount of ground metal for the exposed pad, and use as many vias as possible on the component side to improve thermal dissipation.

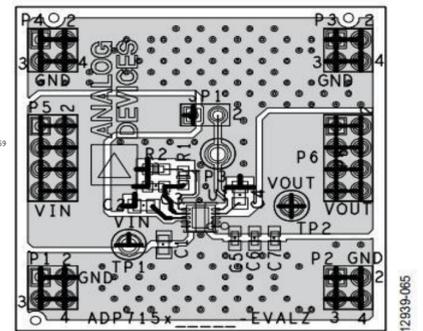
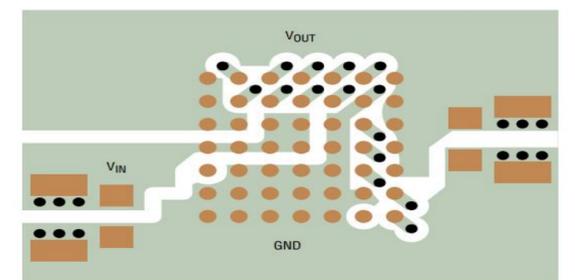


Figure 63. Sample 10-Lead LFCSP PCB Layout

#### RECOMMENDED LAYOUT GUIDELINES

- Use large PCB copper areas for high current paths, including V<sub>IN</sub>, GND and V<sub>OUT</sub>. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V<sub>IN</sub>, PGND and V<sub>OUT</sub> pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Bring out test points on the signal pins for monitoring.
- Keep separation between CLKIN, CLKOUT and FREQ pin traces to minimize possibility of noise due to crosstalk between these signals.

Figure 22 gives a good example of the recommended layout.

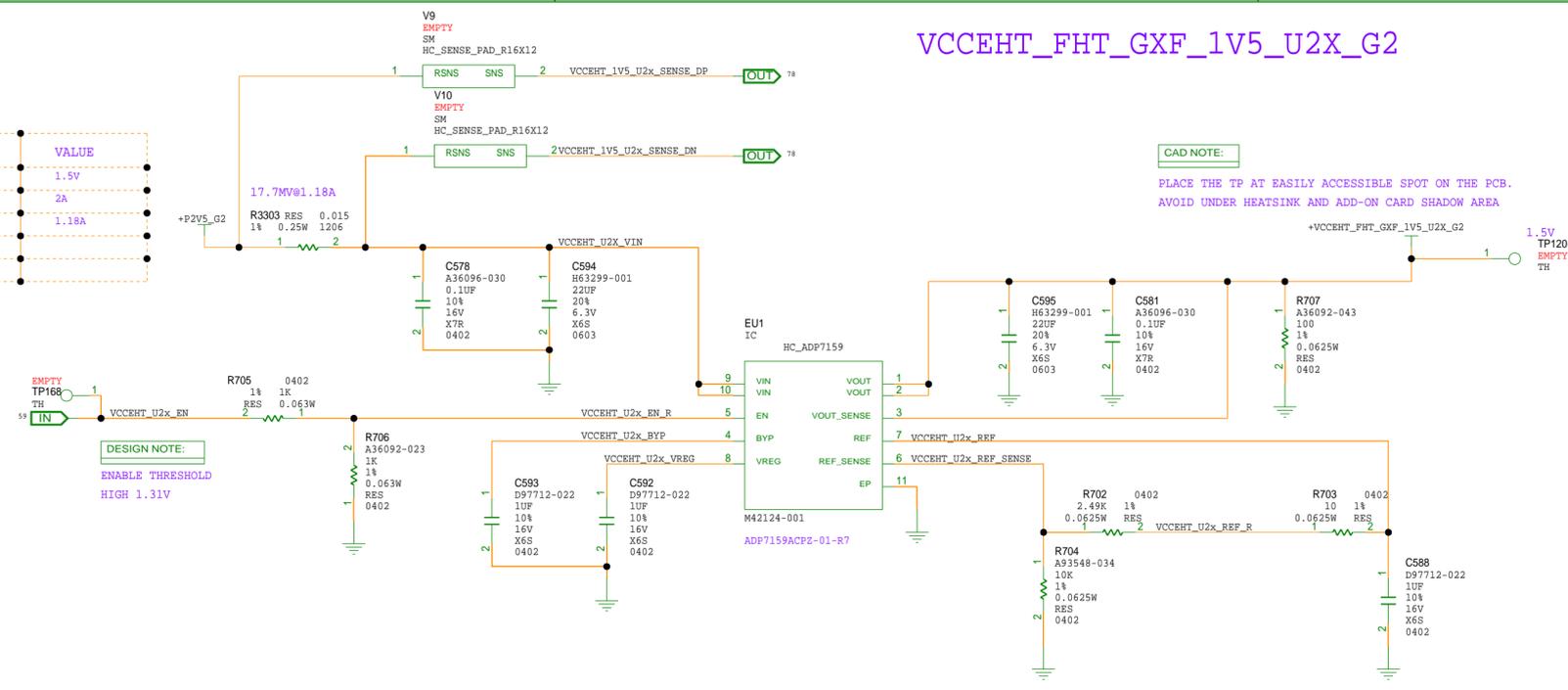


Wed Mar 6 15:45:59 2024

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PGO	INTEL CORPORATION, BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SCALE:	DO NOT SCALE DRAWING		SHEET		95 OF 105		

### VCC\_EHT\_FHT\_GXF\_1V5\_U2X\_G2

PARAMETER	VALUE
VOUT	1.5V
MAX CURRENT	2A
LOAD CURRENT	1.18A
FREQUENCY	
RIPPLE_VOLTAGE	



**CAD NOTE:**  
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.  
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

**DESIGN NOTE:**  
ENABLE THRESHOLD  
HIGH 1.31V

**CAD NOTE:**  
PLACE THESE NEAR TO VR

**RECOMMENDED LAYOUT GUIDELINES**  
Place the input capacitor as close as possible between the VIN pin and ground. Place the output capacitor as close as possible between the VOUT pin and ground. Place the bypass capacitors (C<sub>REG</sub>, C<sub>REF</sub>, and C<sub>BYP</sub>) for V<sub>REG</sub>, V<sub>REF</sub>, and V<sub>BYP</sub> close to the respective pins (V<sub>REG</sub>, V<sub>REF</sub>, and V<sub>BYP</sub>) and ground. The use of a 0805, a 0603, or a 0402 size capacitor achieves the smallest possible footprint solution on boards where area is limited. Maximize the amount of ground metal for the exposed pad, and use as many vias as possible on the component side to improve thermal dissipation.

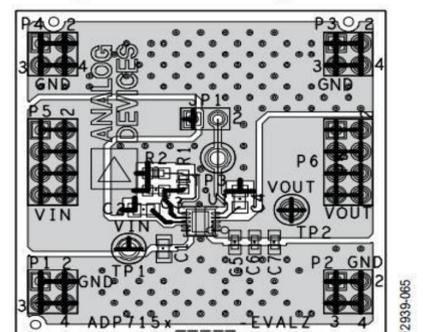
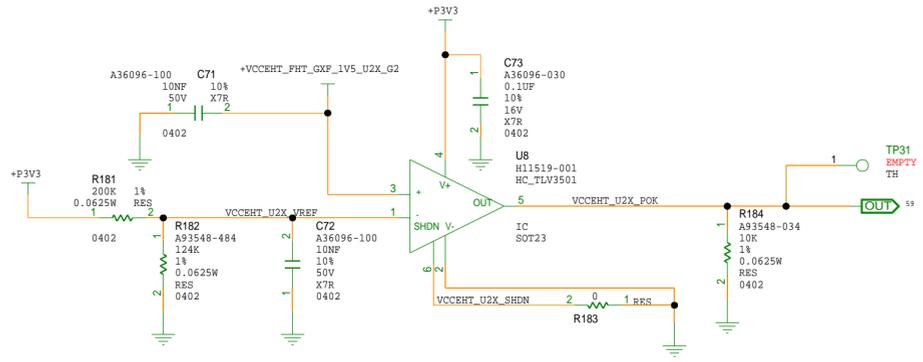


Figure 63. Sample 10-Lead LFCSP PCB Layout



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		SCALE:	DO NOT SCALE DRAWING		SHEET 96 OF 105

# P1V2\_G3

PARAMETER	VALUE
VOUT	1.2V
MAX CURRENT	50A(SINGLE)
LOAD CURRENT	31.978A
FREQUENCY	350KHz
RIPPLE_VOLTAGE	10mV
PM BUS ADDRESS	7 BIT 0X4D

I2C SLAVE ADDRESS: 4DH

CAD NOTE:  
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.  
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

DESIGN NOTE:  
Vout config: 1.3V  
Vtrim: -99mV

### RECOMMENDED LAYOUT GUIDELINES

- Use large PCB copper areas for high current paths, including  $V_{INn}$ , GND and  $V_{OUTn}$ . It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the  $V_{INn}$ , GND and  $V_{OUTn}$  pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the module.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.

- Do not put vias directly on pads, unless they are capped or plated over.
  - Use a separate SGND copper plane for components connected to signal pins. Connect SGND to GND local to the LTM4678.
  - Use Kelvin sense connections across the input  $R_{SENSE}$  resistor if input current monitoring is used.
- For parallel modules, tie the  $V_{OUTn}$ ,  $V_{OSNSn}$ / $V_{OSNSn}$  voltage-sense differential pair lines,  $RUNn$ ,  $COMPn$ ,  $COMPn$ ,  $PM$  pin together.
- The user must share the SYNC, SHARE\_CLK, FAULT, and ALERT pins of these parts. Be sure to use pull-up resistors on FAULT, SHARE\_CLK and ALERT.
  - Bring out test points on the signal pins for monitoring. Figure 44 gives a good example of the recommended layout.

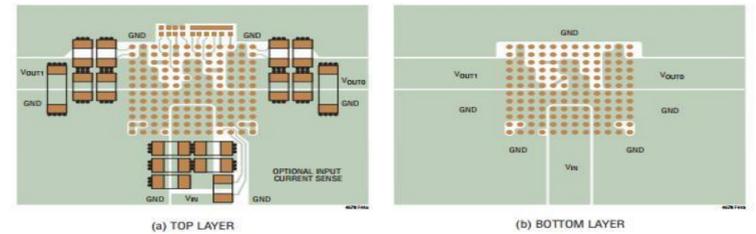


Figure 44. Recommended PCB Layout Package Top View

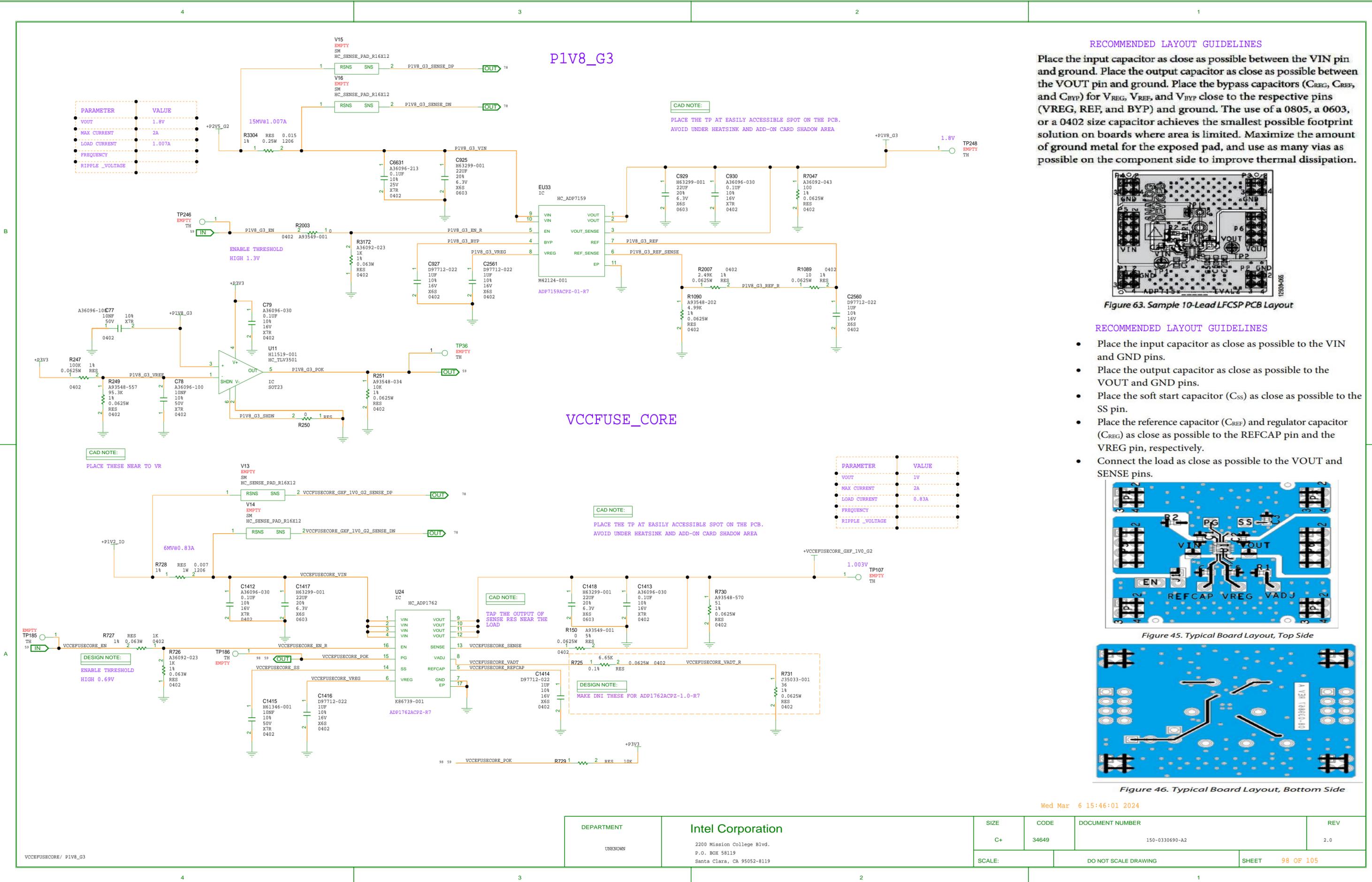
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UNKNOWN	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	C+	34649	150-0330690-A2	2.0
SCALE:	DO NOT SCALE DRAWING	SHEET	97 OF 105		

CAD NOTE:  
CONNECT NEAR FPGA BGA REGION. NEED TO ROUTE AS KELVIN SENSE

DESIGN NOTE:  
RUN threshold - 1.35V

NEED CONFIG  
Rht0 20k  
gm0: 3.69m



RECOMMENDED LAYOUT GUIDELINES

Place the input capacitor as close as possible between the VIN pin and ground. Place the output capacitor as close as possible between the VOUT pin and ground. Place the bypass capacitors (C<sub>REG</sub>, C<sub>REF</sub>, and C<sub>BYP</sub>) for V<sub>REG</sub>, V<sub>REF</sub>, and V<sub>BYP</sub> close to the respective pins (VREG, REF, and BYP) and ground. The use of a 0805, a 0603, or a 0402 size capacitor achieves the smallest possible footprint solution on boards where area is limited. Maximize the amount of ground metal for the exposed pad, and use as many vias as possible on the component side to improve thermal dissipation.

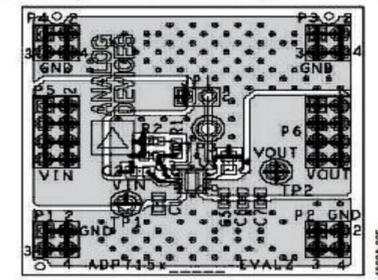


Figure 63. Sample 10-Lead LFCSP PCB Layout

RECOMMENDED LAYOUT GUIDELINES

- Place the input capacitor as close as possible to the VIN and GND pins.
- Place the output capacitor as close as possible to the VOUT and GND pins.
- Place the soft start capacitor (C<sub>SS</sub>) as close as possible to the SS pin.
- Place the reference capacitor (C<sub>REF</sub>) and regulator capacitor (C<sub>REG</sub>) as close as possible to the REFCAP pin and the VREG pin, respectively.
- Connect the load as close as possible to the VOUT and SENSE pins.

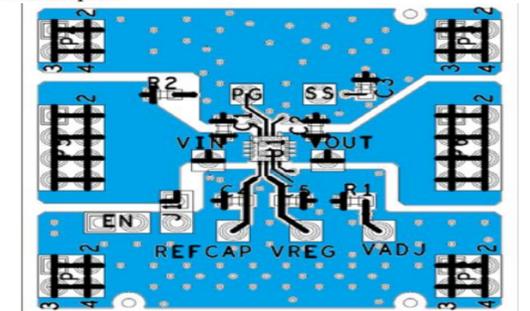


Figure 45. Typical Board Layout, Top Side

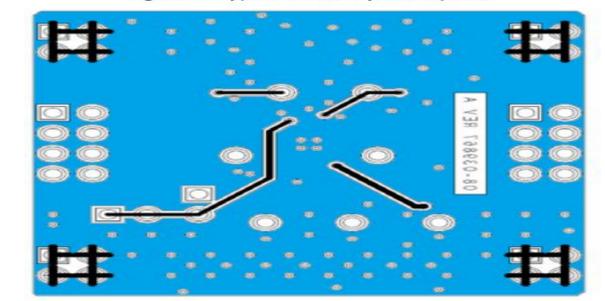


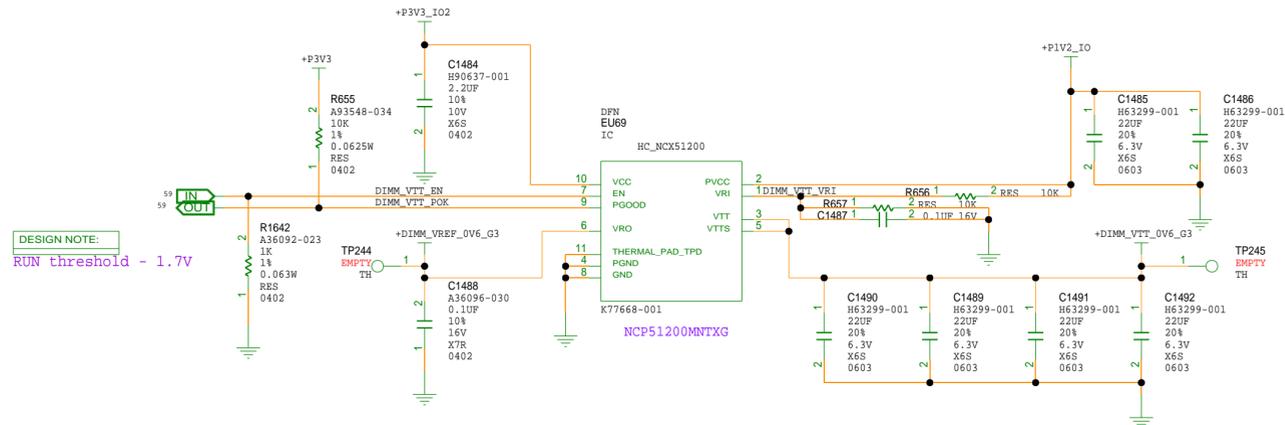
Figure 46. Typical Board Layout, Bottom Side

Wed Mar 6 15:46:01 2024

DEPARTMENT UNKNOWN	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330690-A2	REV 2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 98 OF 105

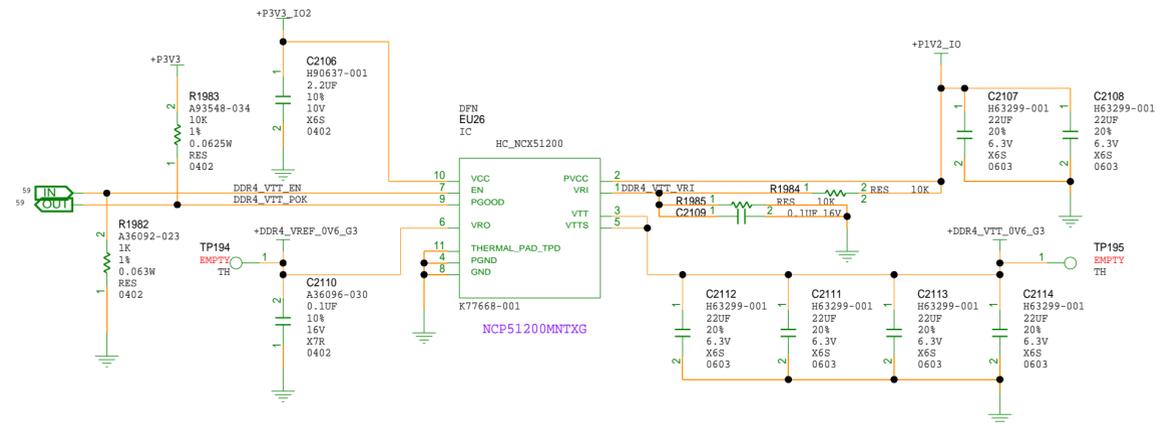
## VTT REGULATORS

PARAMETER	VALUE
VOUT	0.6V
MAX CURRENT	3A
LOAD CURRENT	1.1A
FREQUENCY	
RIPPLE_VOLTAGE	



DESIGN NOTE:  
RUN threshold - 1.7V

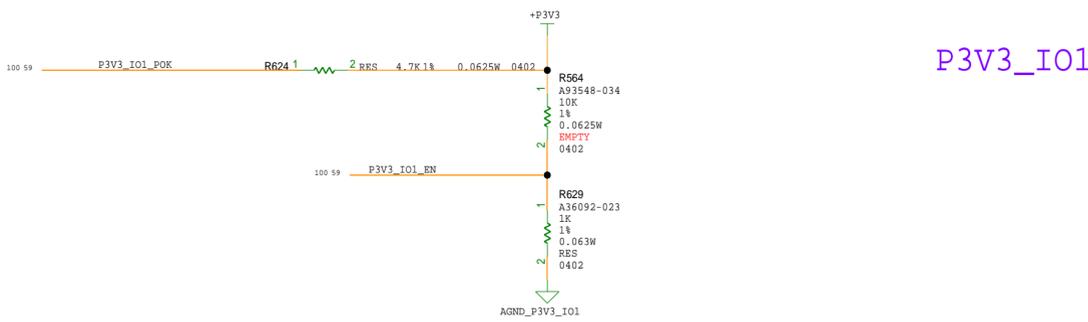
PARAMETER	VALUE
VOUT	0.6V
MAX CURRENT	3A
LOAD CURRENT	1.5A
FREQUENCY	
RIPPLE_VOLTAGE	



DESIGN NOTE:  
RUN threshold - 1.7V

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SCALE:		DO NOT SCALE DRAWING		SHEET 99 OF 105	

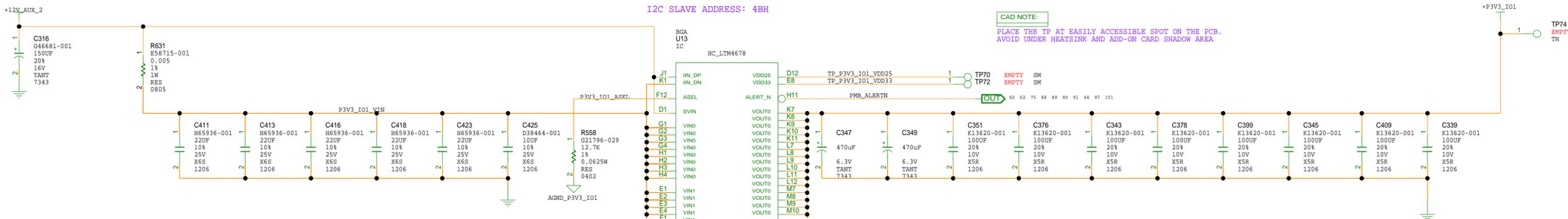


### P3V3\_I01

I2C SLAVE ADDRESS: 4BH

CAD NOTE:

PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB. AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA



CAD NOTE:

CONNECT NEAR FPGA BGA REGION. NEED TO ROUTE AS KELVIN SENSE

DESIGN NOTE:

RUN threshold - 1.35V

DESIGN NOTE:

VOUT CONFIG: 3.3V

VTRIM: -

### RECOMMENDED LAYOUT GUIDELINES

- Use large PCB copper areas for high current paths, including  $V_{INn}$ , GND and  $V_{OUTn}$ . It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the  $V_{INn}$ , GND and  $V_{OUTn}$  pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the module.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.

- Do not put vias directly on pads, unless they are capped or plated over.
  - Use a separate SGND copper plane for components connected to signal pins. Connect SGND to GND local to the LTM4678.
  - Use Kelvin sense connections across the input  $R_{SENSE}$  resistor if input current monitoring is used.
- For parallel modules, tie the  $V_{OUTn}$ ,  $V_{OSNSn}/V_{OSNSn}$  voltage-sense differential pair lines,  $RUNn$ ,  $COMPn$ ,  $COMPn$  pins together.
- The user must share the SYNC, SHARE\_CLK, FAULT, and ALERT pins of these parts. Be sure to use pull-up resistors on FAULT, SHARE\_CLK and ALERT.
  - Bring out test points on the signal pins for monitoring. Figure 44 gives a good example of the recommended layout.

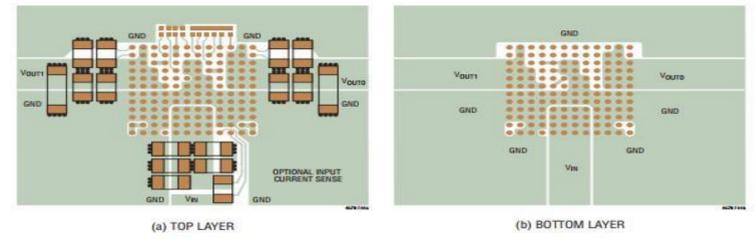
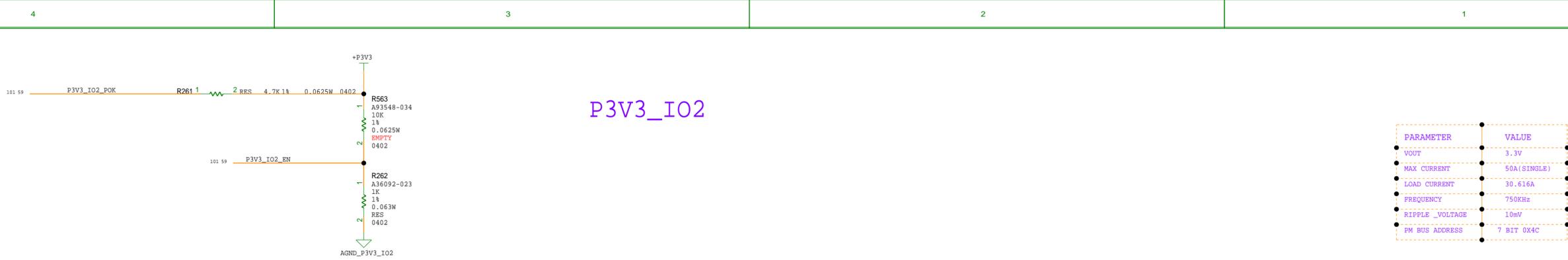


Figure 44. Recommended PCB Layout Package Top View

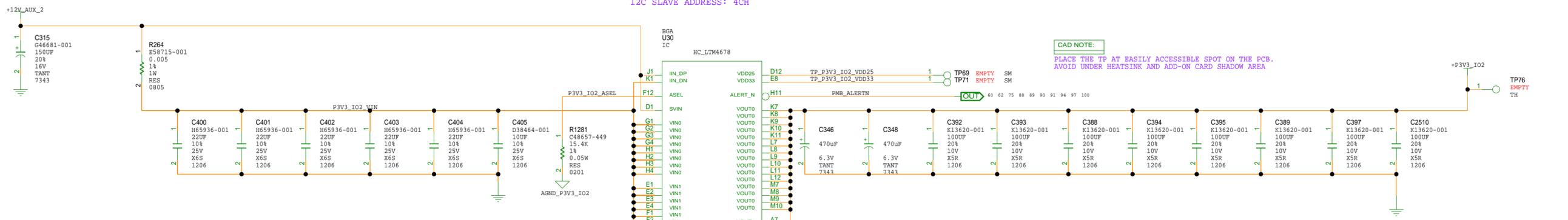
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SCALE:		DO NOT SCALE DRAWING		SHEET 100 OF 105	



### P3V3\_I02

I2C SLAVE ADDRESS: 4CH



CAD NOTE:  
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.  
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

DESIGN NOTE:  
Vout config: 3.3V  
Vtrim: -

CAD NOTE:  
CONNECT NEAR FPGA BGA REGION. NEED TO ROUTE AS KELVIN SENSE

DESIGN NOTE:  
RUN threshold - 1.35V

NEED CONFIG  
Rht: 0.20k  
gmd: 3.69m

### RECOMMENDED LAYOUT GUIDELINES

- Use large PCB copper areas for high current paths, including  $V_{INn}$ , GND and  $V_{OUTn}$ . It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the  $V_{INn}$ , GND and  $V_{OUTn}$  pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the module.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.

- Do not put vias directly on pads, unless they are capped or plated over.
  - Use a separate SGND copper plane for components connected to signal pins. Connect SGND to GND local to the LTM4678.
  - Use Kelvin sense connections across the input  $R_{SENSE}$  resistor if input current monitoring is used.
- For parallel modules, tie the  $V_{OUTn}$ ,  $V_{SNSn}$ ,  $V_{SNSn}$  voltage-sense differential pair lines,  $RUNn$ ,  $COMPn$ ,  $COMPn$  pins together.
- The user must share the SYNC, SHARE\_CLK, FAULT, and ALERT pins of these parts. Be sure to use pull-up resistors on FAULT, SHARE\_CLK and ALERT.
  - Bring out test points on the signal pins for monitoring.
- Figure 44 gives a good example of the recommended layout.

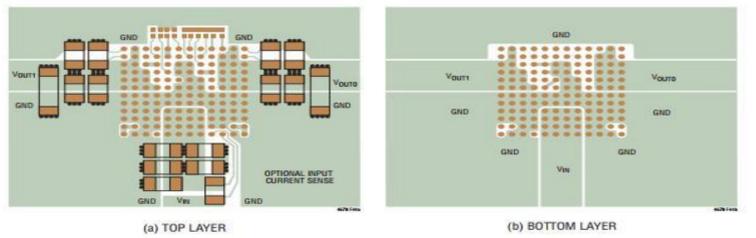


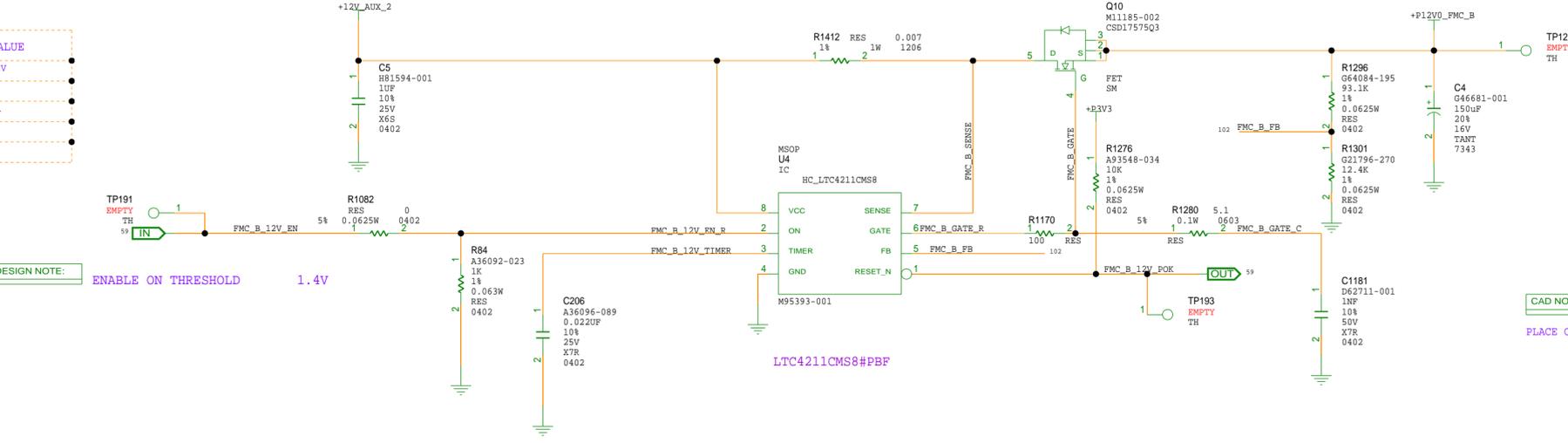
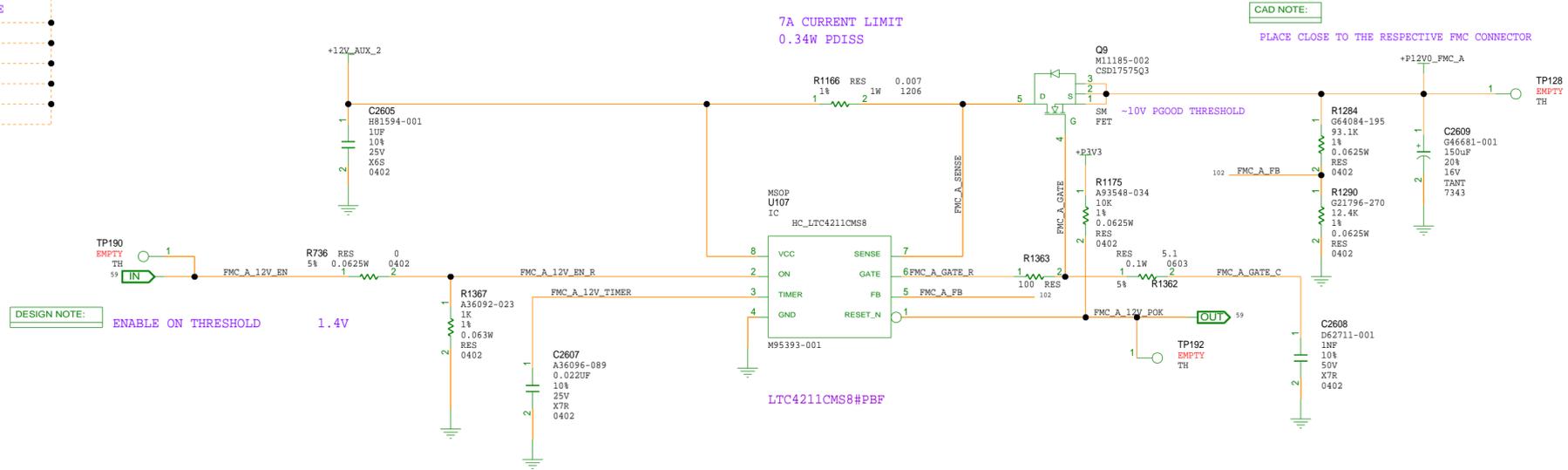
Figure 44. Recommended PCB Layout Package Top View

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SCALE:		DO NOT SCALE DRAWING		SHEET 101 OF 105	

### FMC PWR LOAD SWITCHES

PARAMETER	VALUE
VOUT	12V
MAX CURRENT	
LOAD CURRENT	1A
FREQUENCY	
RIPPLE_VOLTAGE	



PARAMETER	VALUE
VOUT	12V
MAX CURRENT	
LOAD CURRENT	1A
FREQUENCY	
RIPPLE_VOLTAGE	

FET_PARAMETER	VALUE
VGS	±20 V
ID	60 A

FET_PARAMETER	VALUE
VGS	±20 V
ID	60 A

CAD NOTE: PLACE CLOSE TO THE RESPECTIVE FMC CONNECTOR

CAD NOTE: PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB. AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

CAD NOTE: PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB. AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

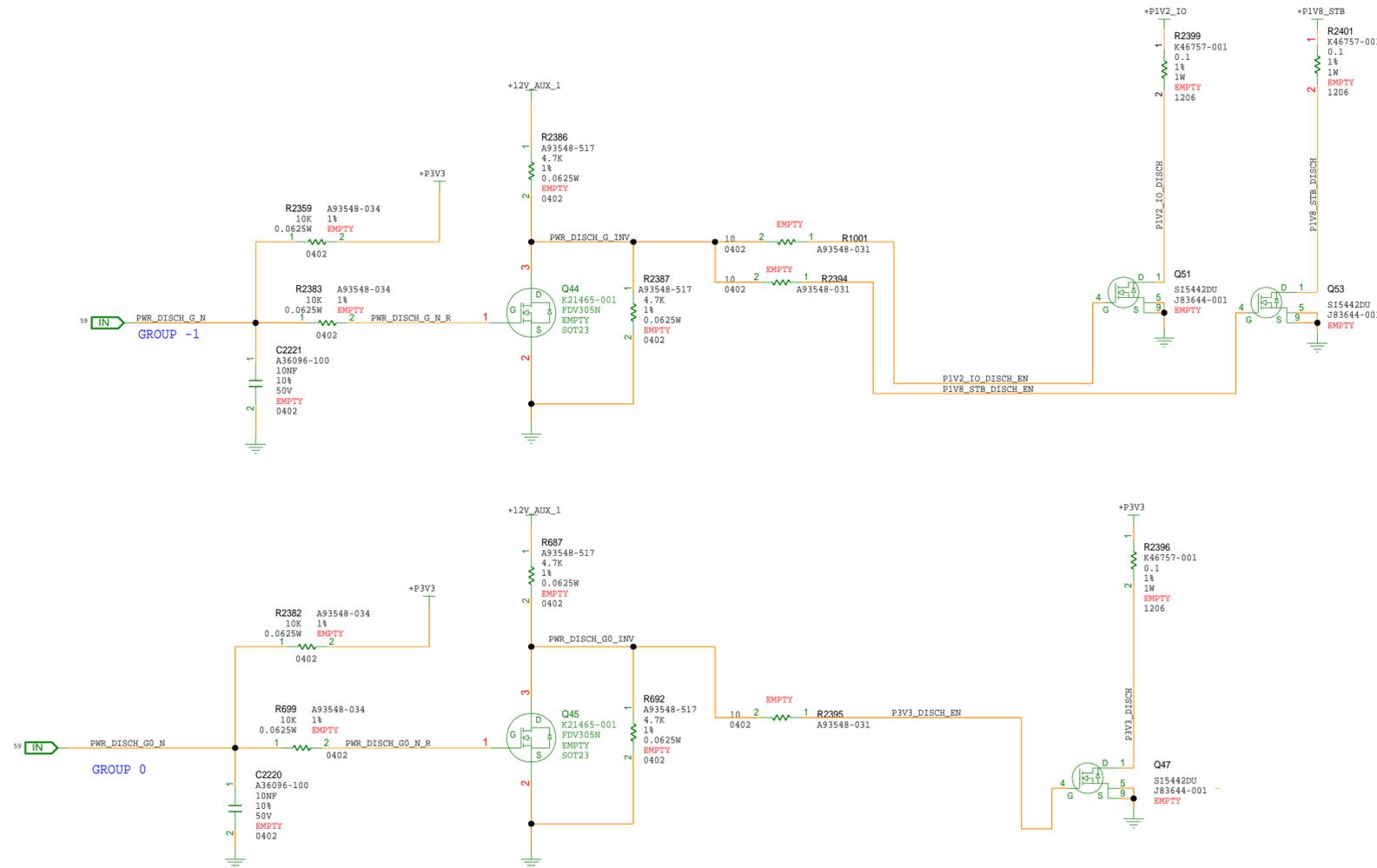
CAD NOTE: PLACE CLOSE TO THE RESPECTIVE FMC CONNECTOR

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		SCALE:	DO NOT SCALE DRAWING		SHEET 102 OF 105



# QUICK DISCHARGE 2



Wed Mar 6 15:46:04 2024

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SCALE:		DO NOT SCALE DRAWING			SHEET 104 OF 105

## REVISION \_HISTORY

UPDATED ALL DESIGN CHANGES AS PER THE CHANGE LIST AFTER VALIDATION IS COMPLETED  
 MAJOR DESIGN CHANGES WERE LISTED BELOW FOR REFERENCE.

- 1) REPLACED OCXO WITH TCXO (7N19471003 ) AT Y7.
- 2) MOUNTED R1295, R1579, R1569, R1402,R573 WITH 10K RESISTOR.
- 3) CHANGED THE EUI3 ADDRESS TO 6BH IN SCHEMATIC TEXTS & POWER TREE DOC.
- 4) USE THE AVAILABLE PB FOR POWER MAX10 RESET CONFIGURATION.
- 5) REMOVE DISCHARGE CIRCUIT FOR ALL THE GROUPS. PAGE 103 & 104 SHOULD BE REMOVED FROM SCHEMATICS.
- 6) REPLACE LTC7151SIV#PBF[-40C TO 125C] WITH LTC7151SEV#PBF[0C TO 85C].
- 7) ADDED PULL-UP TO DDR4\_ALERT\_N FOR DRR4 MEMORY COMPONENT.
- 8) UPDATED BELOW RESISTORS DNI, SINCE THOSE ARE ADDITIONAL PULL\_UPS.  
 R1906,R1907,R1912,R1913,R1890,R1891,R1896,R1897,R1038,R1049,R1076,R1077,R1845,R1846,R2465,R2466
- 9) ADDED PULL-UP TO TP\_5V\_POK.
- 10) UPDATED BELOW CAPS DNI AFTER POWER DC SIM RESULTS.  
 C597,C618,C1360,C1380,C1383,C1333,C1365,C1389,C1367,C1347
- 11) CONNECTED THE DDR4\_TEN SIGNAL DIRECTLY TO GND
- 12) ADDED VTT TERMINATION 36 OHM TO DDR4\_A3
- 13) UPDTAED QSFP CAGE AND CLIP TO [U95-L111-1001 AND U9011017060BP ] FOR QSFP CONNECTORS
- 14) CONNECTED OE PIN OF SI5395, SI5395\_1\_A\_OEN AND SI5395\_2\_OEN TO SYSTEM MAX10
- 15) UPDATED CLOCK PROGRAMMING DESIN FOR SI5518 AND SI5395 AS BELOW  
 UPDATED J31 SHOULDE BE USED FOR SI5518 SPI ONLY.  
 REMOVED R2661,R2662,R3267,R3268 RESISTORS.  
 CONNECTED R2661.1 TO R3267.2 ON PCB  
 CONNECTED R2662.1 TO R3268.2 ON PCB  
 J41 OR J140 SHOULD BE USED FOR CLK\_I2C TO PROGRAM SI5391,SI5395\_1 )EUI0),SI5395\_2 (EUI3).  
 REMOVED R2015,R3265,R3266.  
 REMOVED U150, U29 IC'S
- 16) ADDED DIP SWITCH FOR POWER MAX10.
- 17) R2626 RESISTOR IS UPDATED TO DNI.
- 18) R114 AND R55 RESISTORS IS UPDATED TO DNI.

Tue Aug 8 11:18:22 2023

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		SCALE:		DO NOT SCALE DRAWING	SHEET 105 OF 105