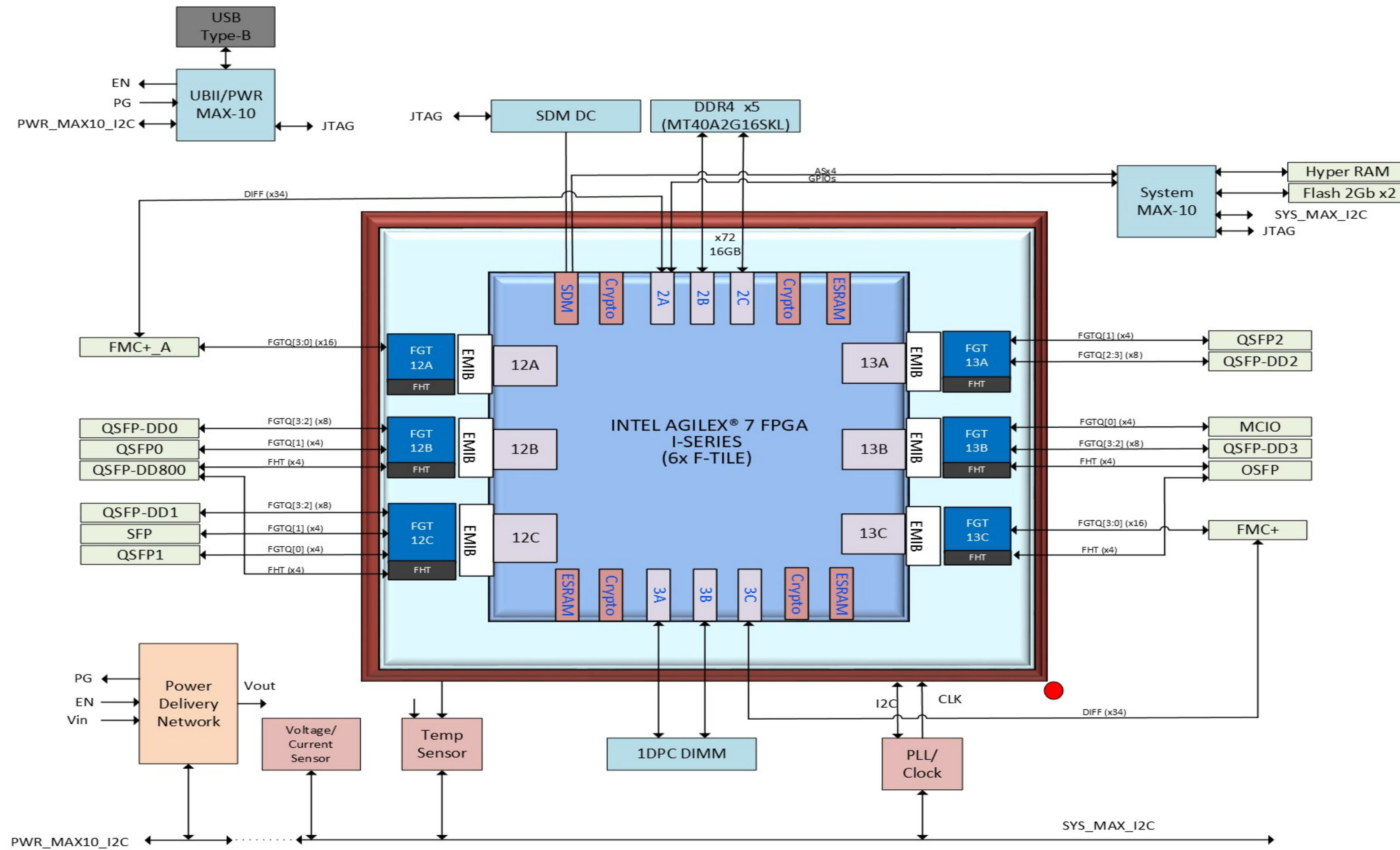


INTEL AGILEX® 7 FPGA I-SERIES TRANSCEIVER DEVELOPMENT KIT(6x F-TILE)



Fri Sep 22 18:19:47 2023

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 2 OF 105

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POWER ESTIMATION

Rail Name	Voltage (V)	Source	Efficiency	Consumption (A)	Power (W)	Voltage Regulator	Current Supported (A)	Group	RefDes
+P3V3	3.3	+12V0_AUX_1	90%	6.189	20.424	LTC7151SEV#PBF	15	Group - (-1)	U95
+P1V8_STB	1.8	+12V0_AUX_1	85%	2.822	5.079	LTM4668AIY#PBF	4.8	Group - (-1)	U79
+P5V	5	+12V0_AUX_1	85%	0.800	4.000	LTM4625EY#PBF	5	Group - (-1)	U102
+P1V2_IO	1.2	+12V0_AUX_1	85%	6.526	7.831	LTM4657EY#PBF	8	Group - 0	U47
+VCCL_OV8_G1	0.8	+12V0_AUX_1	87%	248.930	199.144	LTC3888+LTC7051(5)	300	Group - 1	U31,U32,U33,U34,U35,U181
+VCC_HSSI_GXF_OV8_Ux0_G1	0.8	+12V0_AUX_1	87%	29.067	23.254	LTM4677EY#PBF (Single)	36	Group - 1	U12
+VCC_HSSI_GXF_OV8_Ux1_G1	0.8	+12V0_AUX_1	87%	28.787	23.029	LTM4677EY#PBF (Single)	36	Group - 1	U6
+VCC_HSSI_GXF_OV8_Ux2_G1	0.8	+12V0_AUX_1	87%	28.787	23.029	LTM4677EY#PBF (Single)	36	Group - 1	U44
+VCCERT_UX_GXF_1V0_U1x_G1	1	+12V0_AUX_1	85%	19.585	19.585	LTM4678EY#PBF (Dual)	25	Group - 1	U20
+VCCERT_UX_GXF_1V0_U2x_G1	1	+12V0_AUX_1	85%	19.585	19.585	LTM4678EY#PBF (Dual)	25	Group - 1	U20
+P0V8_G1	0.8	+12V0_AUX_1	87%	16.541	13.233	LTM4678EY#PBF (Dual)	25	Group - 1	U43
+VCCERT1_FHT_GXF_1V0_Ux_G1	1	+12V0_AUX_1	88%	12.200	12.200	LTC7151SEV#PBF	15	Group - 1	EU17
+VCCERT2_FHT_GXF_1V0_Ux_G1	1	+P1V2_IO	83%	1.536	1.536	ADP1762ACPZ-R7	2	Group - 1	U94
+P1V8_G2	1.8	+12V0_AUX_1	90%	20.753	37.356	LTM4678EY#PBF (Dual)	25	Group - 2	U43
+P2V5_G2	2.5	+12V0_AUX_1	85%	3.213	8.032	LTM4657EY#PBF	8	Group - 2	U21
+VCCEHT_FHT_GXF_1V5_U1x_G2	1.5	+P2V5_G2	60%	0.800	1.200	ADP7159ACPZ-01-R7	2	Group - 2	EU8
+VCCEHT_FHT_GXF_1V5_U2x_G2	1.5	+P2V5_G2	60%	0.800	1.200	ADP7159ACPZ-01-R7	2	Group - 2	EU1
+VCCEFUSECORE_GXF_1V0_G2	1	+P1V2_IO	50%	0.830	0.830	ADP1762ACPZ-R7	2	Group - 2	U24
+P3V3_IO1	3.3	+12V0_AUX_2	92%	32.086	105.884	LTM4678EY#PBF (Single)	50	Group - 3	U13
+P3V3_IO2	3.3	+12V0_AUX_2	92%	30.616	101.033	LTM4678EY#PBF (Single)	50	Group - 3	U30
+P1V2_G3	1.2	+12V0_AUX_1	90%	31.978	38.374	LTM4678EY#PBF (Single)	50	Group - 3	U10
+P12V0_FMC_A	12	+12V0_AUX_2	85%	1.000	12.000	FET/LTC4211CMS#PBF	3	Group - 3	U107/Q9
+P12V0_FMC_B	12	+12V0_AUX_2	85%	1.000	12.000	FET/LTC4211CMS#PBF	3	Group - 3	U4/Q10
+P1V8_G3	1.8	+P2V5_G2	85%	1.007	1.812	ADP7159ACPZ-01-R7	2	Group - 3	EU33
+DDR4_VTT_OV6_G3	0.6	+P1V2_IO	50%	1.000	0.600	NCP51200MNTXG	3	Group - 3	EU26
+DIMM_VREF_OV6_G3	0.6	+P1V2_IO	50%	0.100	0.060	NCP51200MNTXG	3	Group - 3	U69
+DIMM_VTT_OV6_G3	0.6	+P1V2_IO	50%	1.000	0.600	NCP51200MNTXG	3	Group - 3	U69
+DRR4_VREF_OV6_G3	0.6	+P1V2_IO	50%	0.500	0.300	NCP51200MNTXG	3	Group - 3	EU26

Tue Aug 8 11:15:53 2023

POWER ESTIMATION

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UNKNOWN

Intel Corporation

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P.O. BOX 58119
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CODE
34649

DOCUMENT NUMBER

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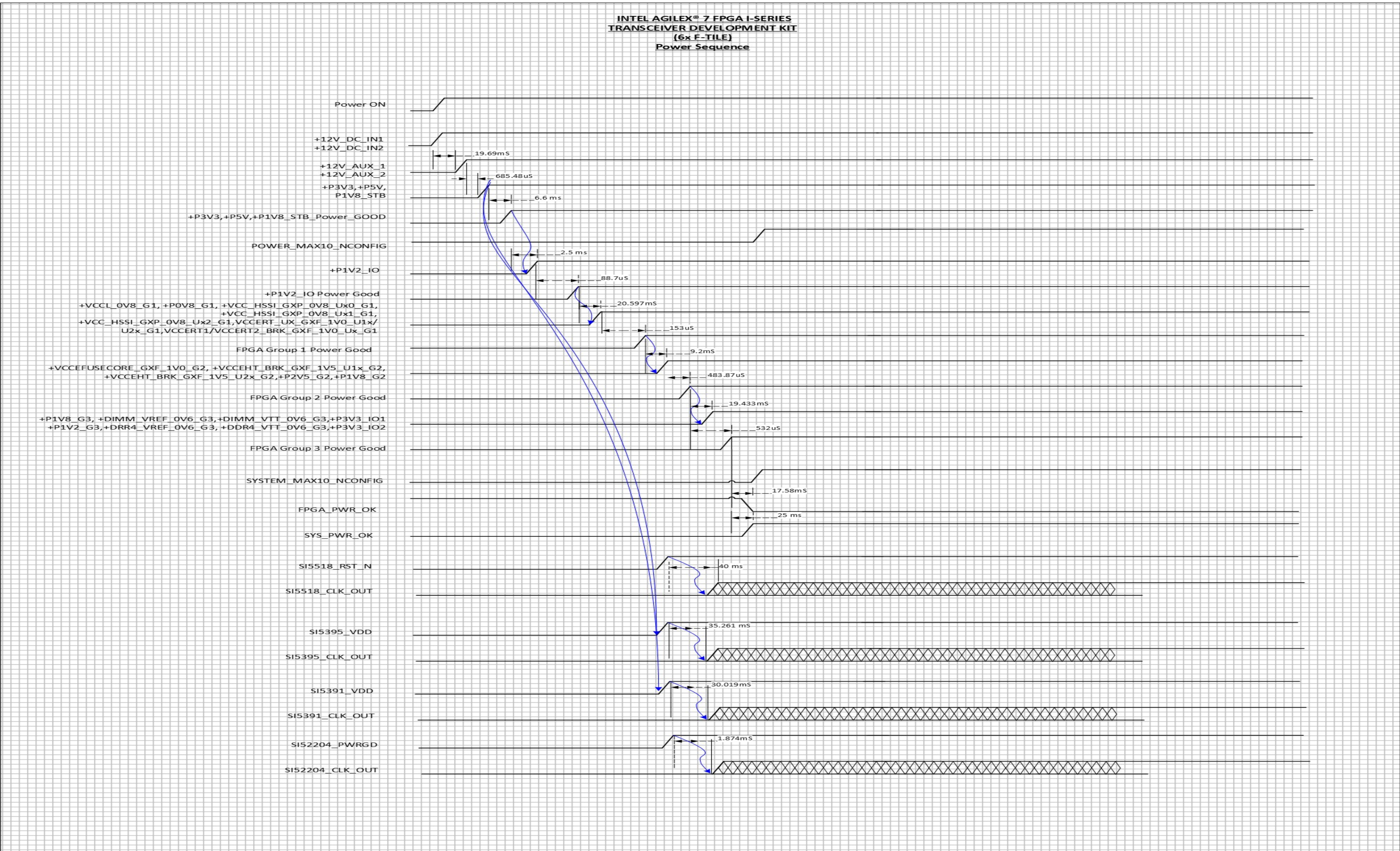
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POWER SEQUENCE GRAPH



Fri Sep 22 18:19:51 2023

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DEPARTMENT

PSG

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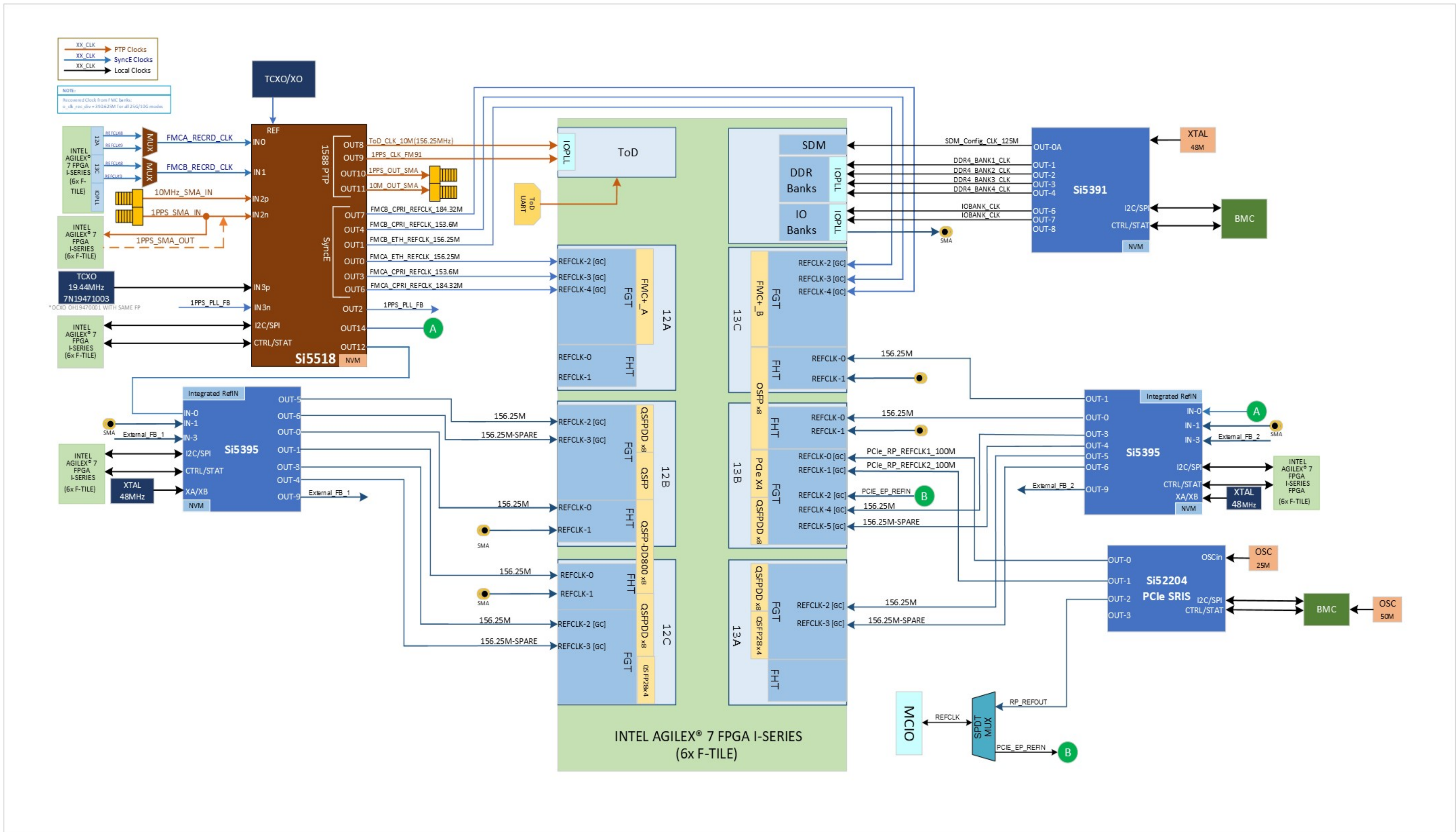
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SHEET

5 OF 105

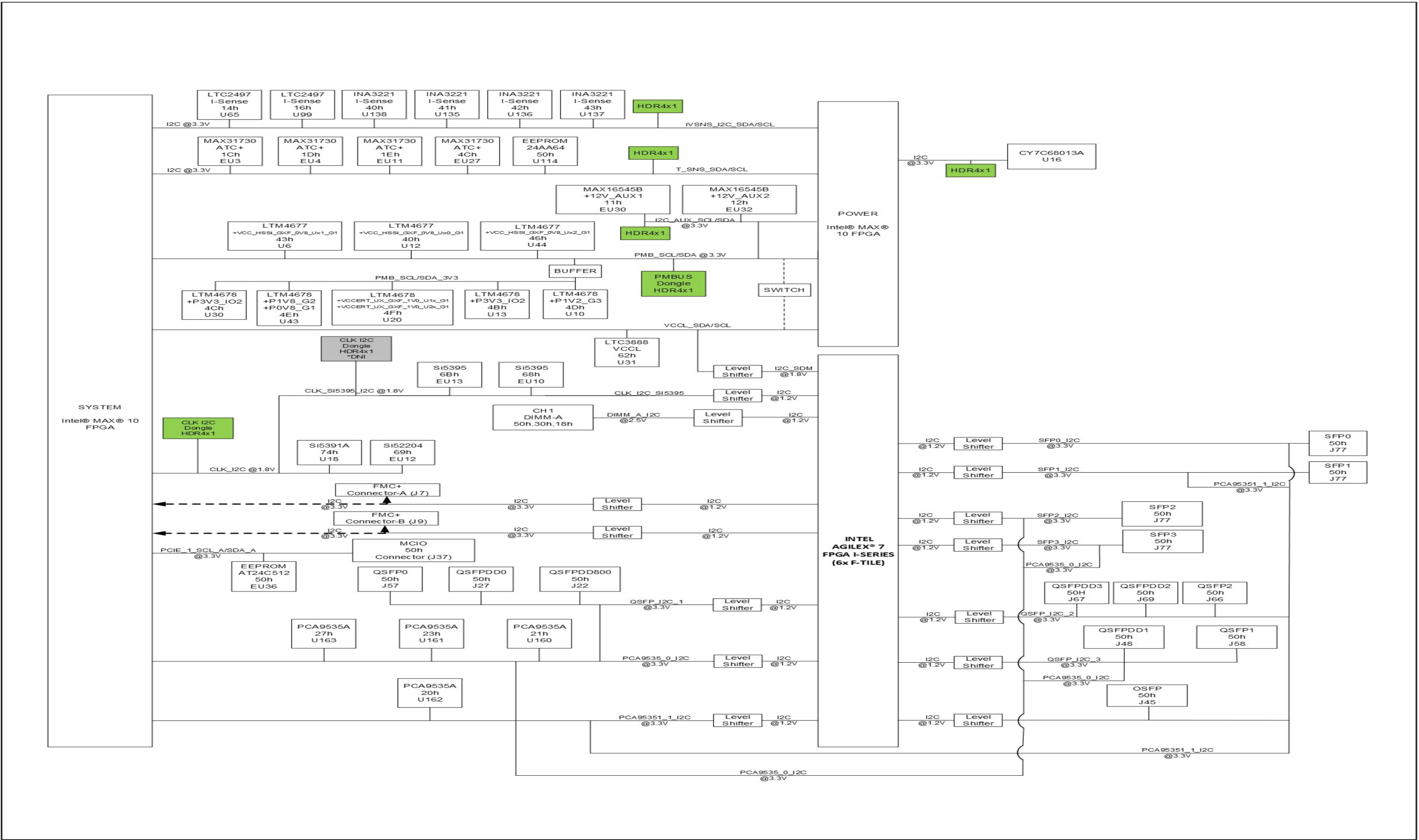
CLOCK TREE



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I2C TREE



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I2C TABLE

I2C NETS	MASTER 1	MASTER 2	MASTER 3	SLAVE 1	SLAVE 2	SLAVE 3	SLAVE 4	SLAVE 5	SLAVE 6	SLAVE 7	SLAVE 8	SLAVE 9	INTER I2C CONNECTION
CLK_SIS395_I2C_1V2_SDA	U1 FM91	J140 HEADER	-----	EU13 SIS395 0x6B	EU10 SIS395 0x6B	-----	-----	-----	-----	-----	-----	-----	BELOW I2C ARE CONNECTED CLK_SIS395_I2C & CLK_I2C
CLK_SIS395_I2C_1V2_SCL				U18 SIS391 0x74	EU12 SI52204_A02BGMR 0x69	-----	-----	-----	-----	-----	-----	-----	
CLK_I2C_SDA	U3 SYSTEM MAX 10	J42 HDR	-----	U161 PCA9535A 0x23	U160 PCA9535A 0x21	U163 PCA9535A 0x27	J77 SFP0 MOD3 0xA0	J48 QSFPDD1 0xA0	J58 QSFP1 0xA0	J22 QSFPDD800 0xA0	J27 QSFPDD0 0xA0	J57 QSFP0 0xA0	PCA9535_0_I2C IS CONNECTED TO SFP0_I2C,QSFP3/1_I2C & PROVIDED OPTION FOR **SFP1_I2C MODULES WITH SAME I2C ADDRESS WILL BE CONTROLLED USING MODEL PIN
CLK_I2C_SCL				-----	-----	-----	J77 SFP0 MOD3 0xA0	-----	-----	-----	-----	-----	
PCA9535_0_1V2_SDA	U1 FM91	U3 SYSTEM MAX 10	-----	-----	-----	-----	J77 SFP1 MOD2 0xA0	-----	-----	-----	-----	-----	
PCA9535_0_1V2_SCL	U1 FM91	**U3 SYSTEM MAX 10	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
SFP0_MOD3_1V2_SDA	U1 FM91	U3 SYSTEM MAX 10	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
SFP0_MOD3_1V2_SCL	U1 FM91	U3 SYSTEM MAX 10	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
SFP1_MOD2_1V2_SDA	U1 FM91	**U3 SYSTEM MAX 10	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	PCA9535_0_I2C IS CONNECTED TO SFP0_I2C,QSFP3/1_I2C & PROVIDED OPTION FOR **SFP1_I2C MODULES WITH SAME I2C ADDRESS WILL BE CONTROLLED USING MODEL PIN
SFP1_MOD2_1V2_SCL	U1 FM91	**U3 SYSTEM MAX 10	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
I2C_QSFP_3_1V2_SDA	U1 FM91	U3 SYSTEM MAX 10	-----	-----	-----	-----	-----	J48 QSFPDD1 0xA0	J58 QSFP1 0xA0	-----	-----	-----	
I2C_QSFP_3_1V2_SCL	U1 FM91	U3 SYSTEM MAX 10	-----	-----	-----	-----	-----	J48 QSFPDD1 0xA0	J58 QSFP1 0xA0	-----	-----	-----	
I2C_QSFP_1_1V2_SDA	U1 FM91	U3 SYSTEM MAX 10	-----	-----	-----	-----	-----	-----	-----	J22 QSFPDD800 0xA0	J27 QSFPDD0 0xA0	J57 QSFP0 0xA0	
I2C_QSFP_1_1V2_SCL	U1 FM91	U3 SYSTEM MAX 10	-----	-----	-----	-----	-----	-----	-----	J22 QSFPDD800 0xA0	J27 QSFPDD0 0xA0	J57 QSFP0 0xA0	
PCA9535_1_1V2_SDA	U1 FM91	U3 SYSTEM MAX 10	-----	U162 PCA9535A 0x20	J69 QSFPDD2 0xA0	J67 QSFPDD3 0xA0	J66 QSFP2 0xA0	J77 SFP2 MOD1 0xA0	J45 QSFP 0xA0	-----	-----	-----	PCA9535_1_I2C IS CONNECTED TO QSFP2_I2C & QSFP_I2C. PROVIDED OPTION FOR **SFP2/3_I2C MODULES WITH SAME I2C ADDRESS WILL BE CONTROLLED USING MODEL PIN
PCA9535_1_1V2_SCL	U1 FM91	U3 SYSTEM MAX 10	-----	-----	J69 QSFPDD2 0xA0	J67 QSFPDD3 0xA0	J66 QSFP2 0xA0	-----	-----	-----	-----	-----	
I2C_QSFP_2_1V2_SDA	U1 FM91	U3 SYSTEM MAX 10	-----	-----	J69 QSFPDD2 0xA0	J67 QSFPDD3 0xA0	J66 QSFP2 0xA0	-----	-----	-----	-----	-----	
I2C_QSFP_2_1V2_SCL	U1 FM91	U3 SYSTEM MAX 10	-----	-----	J69 QSFPDD2 0xA0	J67 QSFPDD3 0xA0	J66 QSFP2 0xA0	-----	-----	-----	-----	-----	
SFP2_MOD1_1V2_SDA	U1 FM91	**U3 SYSTEM MAX 10	-----	-----	-----	-----	-----	J77 SFP2 MOD1 0xA0	-----	-----	-----	-----	
SFP2_MOD1_1V2_SCL	U1 FM91	**U3 SYSTEM MAX 10	-----	-----	-----	-----	-----	J77 SFP2 MOD1 0xA0	-----	-----	-----	-----	
SFP3_MOD0_1V2_SDA	U1 FM91	**U3 SYSTEM MAX 10	-----	-----	-----	-----	-----	J77 SFP3 MOD0 0xA0	-----	-----	-----	-----	PCA9535_1_I2C IS CONNECTED TO QSFP2_I2C & QSFP_I2C. PROVIDED OPTION FOR **SFP2/3_I2C MODULES WITH SAME I2C ADDRESS WILL BE CONTROLLED USING MODEL PIN
SFP3_MOD0_1V2_SCL	U1 FM91	**U3 SYSTEM MAX 10	-----	-----	-----	-----	-----	J77 SFP3 MOD0 0xA0	-----	-----	-----	-----	
I2C_OSFP_SDA	U1 FM91	U3 SYSTEM MAX 10	-----	-----	-----	-----	-----	-----	J45 OSFP 0xA0	-----	-----	-----	
I2C_OSFP_SCL	U1 FM91	U3 SYSTEM MAX 10	-----	-----	-----	-----	-----	-----	J45 OSFP 0xA0	-----	-----	-----	
FMC_B_SDA_1V2	U1 FM91	**U3 SYSTEM MAX 10	-----	J9 FMCB	-----	-----	-----	-----	-----	-----	-----	-----	
FMC_B_SCL_1V2	U1 FM91	**U3 SYSTEM MAX 10	-----	J9 FMCB	-----	-----	-----	-----	-----	-----	-----	-----	
FMC_A_SDA_1V2	U1 FM91	**U3 SYSTEM MAX 10	-----	J7 FMCA	-----	-----	-----	-----	-----	-----	-----	-----	PCA9535_1_I2C IS CONNECTED TO QSFP2_I2C & QSFP_I2C. PROVIDED OPTION FOR **SFP2/3_I2C MODULES WITH SAME I2C ADDRESS WILL BE CONTROLLED USING MODEL PIN
FMC_A_SCL_1V2	U1 FM91	**U3 SYSTEM MAX 10	-----	J7 FMCA	-----	-----	-----	-----	-----	-----	-----	-----	
DDR4_DIMM_2_SDA_1V2	U1 FM91	-----	-----	J5 DIMM CONN EEPROM Memory- 0x50 WP settind- 0x30 Temp Sensor- 0x18	-----	-----	-----	-----	-----	-----	-----	-----	
DDR4_DIMM_2_SCL_1V2	U1 FM91	-----	-----	J5 DIMM CONN EEPROM Memory- 0x50 WP settind- 0x30 Temp Sensor- 0x18	-----	-----	-----	-----	-----	-----	-----	-----	
PCIE_1_SCL_A	U3 SYSTEM MAX 10	-----	-----	J37 MCIO 0x50	EU36 EEPROM 0x50	-----	-----	-----	-----	-----	-----	-----	
PCIE_1_SDA_A	U3 SYSTEM MAX 10	-----	-----	J37 MCIO 0x50	EU36 EEPROM 0x50	-----	-----	-----	-----	-----	-----	-----	
FX2_SCL	J56-HDR	U16 CY7C68013A	-----	U2 POWER MAX 10	-----	-----	-----	-----	-----	-----	-----	-----	VCCL_I2C & PMB_I2C ARE CONNECTED THROUGH A SWITCH 521 **BY DEFAULT- OPEN
FX2_SDA	J56-HDR	U16 CY7C68013A	-----	U2 POWER MAX 10	-----	-----	-----	-----	-----	-----	-----	-----	
VCCL_SDA	U2 POWER MAX 10	U3 SYSTEM MAX 10	-----	U31 VCCL CONTROLLER 0x62	FM91 SDM	-----	-----	-----	-----	-----	-----	-----	
VCCL_SCL	U2 POWER MAX 10	U3 SYSTEM MAX 10	-----	U31 VCCL CONTROLLER 0x62	FM91 SDM	-----	-----	-----	-----	-----	-----	-----	
PMB_SDA	U2 POWER MAX 10	U3 SYSTEM MAX 10	J41 HDR	U6 LTM4677 0x43	U44 LTM4677 0x46	U12 LTM4677 0x40	U30 LTM4678 0x4C	U13 LTM4678 0x4B	U10 LTM4678 0x4D	U43 LTM4678 0x4E	U20 LTM4678 0x4F	-----	
PMB_SCL	U2 POWER MAX 10	U3 SYSTEM MAX 10	J41 HDR	U6 LTM4677 0x43	U44 LTM4677 0x46	U12 LTM4677 0x40	U30 LTM4678 0x4C	U13 LTM4678 0x4B	U10 LTM4678 0x4D	U43 LTM4678 0x4E	U20 LTM4678 0x4F	-----	
T_SNS_SCL	**U2 POWER MAX 10	U3 SYSTEM MAX 10	J79 HDR	EU3 MAX31730 0x38	EU4 MAX31730 0x3A	EU11 MAX31730 0x3C	EU27 MAX31730 0x98	U114 EEPROM 24AA64 0x50	-----	-----	-----	-----	VCCL_I2C & PMB_I2C ARE CONNECTED THROUGH A SWITCH 521 **BY DEFAULT- OPEN
T_SNS_SDA	**U2 POWER MAX 10	U3 SYSTEM MAX 10	J79 HDR	EU3 MAX31730 0x38	EU4 MAX31730 0x3A	EU11 MAX31730 0x3C	EU27 MAX31730 0x98	U114 EEPROM 24AA64 0x50	-----	-----	-----	-----	
IVSNS_I2C_SDA	**U2 POWER MAX 10	U3 SYSTEM MAX 10	J149-HDR	U138 INA3221 0x40	U135 INA3221 0x41	U136 INA3221 0x42	U137 INA3221 0x43	U99 LTC2497 0x16	U65 LTC2497 0x14	-----	-----	-----	
IVSNS_I2C_SCL	**U2 POWER MAX 10	U3 SYSTEM MAX 10	J149-HDR	U138 INA3221 0x40	U135 INA3221 0x41	U136 INA3221 0x42	U137 INA3221 0x43	U99 LTC2497 0x16	U65 LTC2497 0x14	-----	-----	-----	
I2C_AUX_SCL	U2 POWER MAX 10	J154 HDR	-----	EU30 MAX16545B 0x11	EU32 MAX16545B 0x12	-----	-----	-----	-----	-----	-----	-----	
I2C_AUX_SDA	U2 POWER MAX 10	J154 HDR	-----	EU30 MAX16545B 0x11	EU32 MAX16545B 0x12	-----	-----	-----	-----	-----	-----	-----	

Fri Sep 22 19:27:18 2023

I2C_TABLE

DEPARTMENT
UNKNOWN

Intel Corporation

2200 Mission College Blvd.
P.O. BOX 58119
Santa Clara, CA 95052-8119

SIZE
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CODE
34649

DOCUMENT NUMBER

150-0330690-A2

REV

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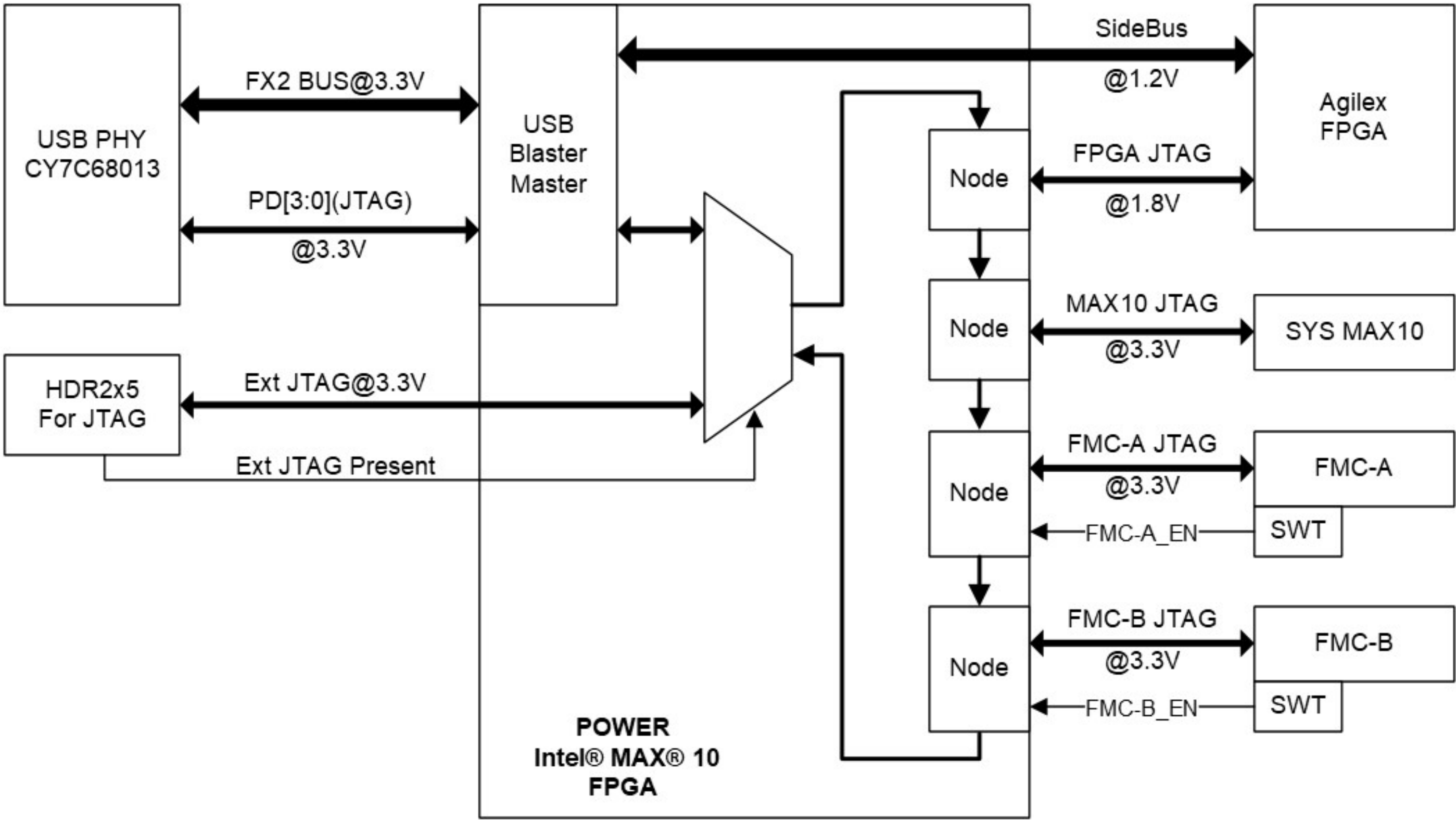
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JTAG TOPOLOGY



Note:
1. The JTAG of Agilex FPGA can't be added to the chain before fully powered up

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4

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SDM IO MAPPING

SDM PINS	MSEL FUNCTIONS	CONFIGURATION SOURCE FUNCTION
		AS
SDM_IO0		PWR_SCL
SDM_IO1		DATA1
SDM_IO2		CLK
SDM_IO3		DATA2
SDM_IO4		DATA0
SDM_IO5	MSEL0	NCS00
SDM_IO6		DATA3
SDM_IO7	MSEL1	NCS02
SDM_IO8		NCS03
SDM_IO9	MSEL2	NCS01
SDM_IO10		
SDM_IO11		HPS_CRSTN
SDM_IO12		
SDM_IO13		
SDM_IO14		
SDM_IO15		RESETN
SDM_IO16		CFG_DONE

SYSTEM MAX IS THE SOURCE OF HPS_CRSTN FUNCTION

Tue Aug 8 11:15:59 2023

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B



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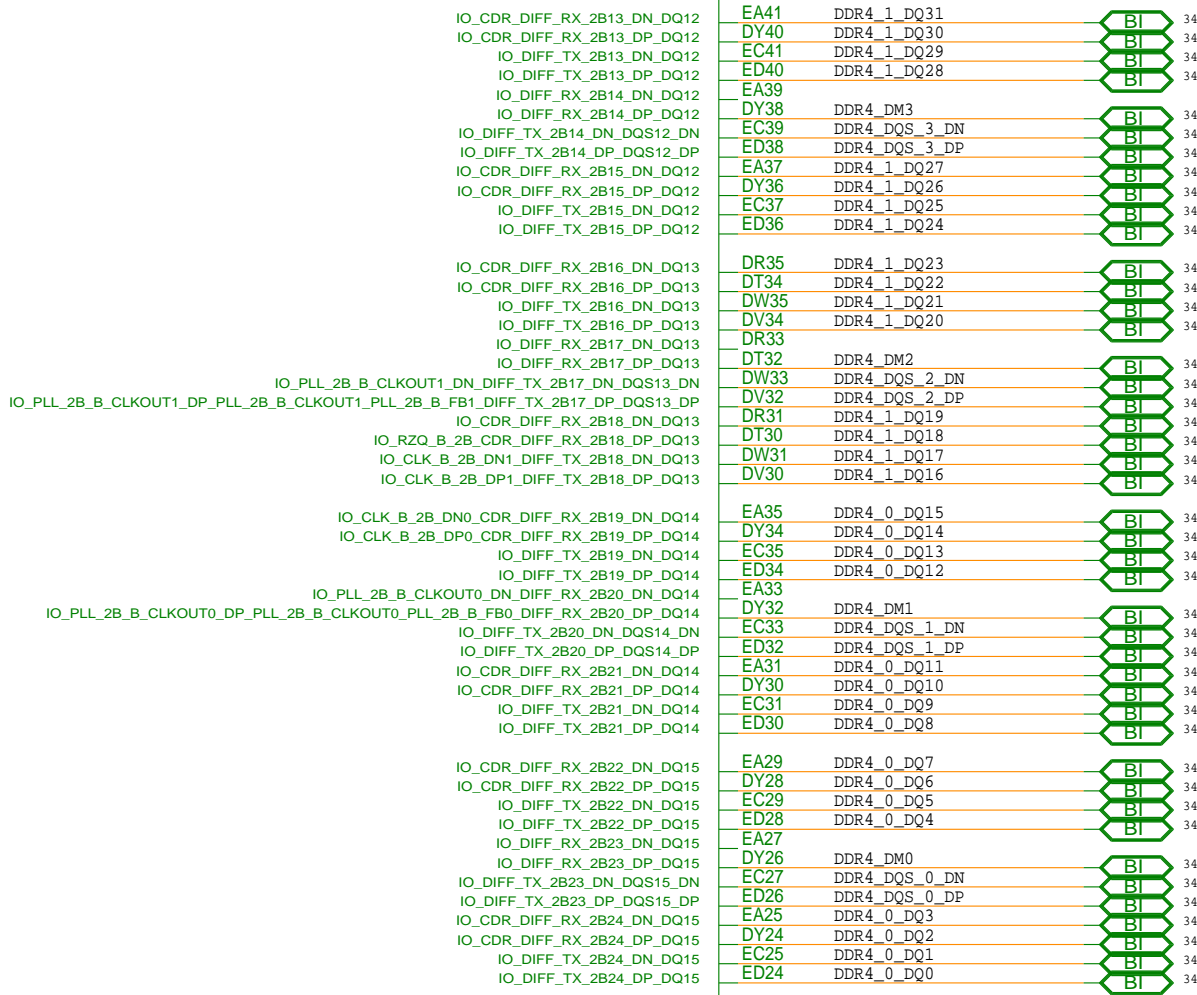
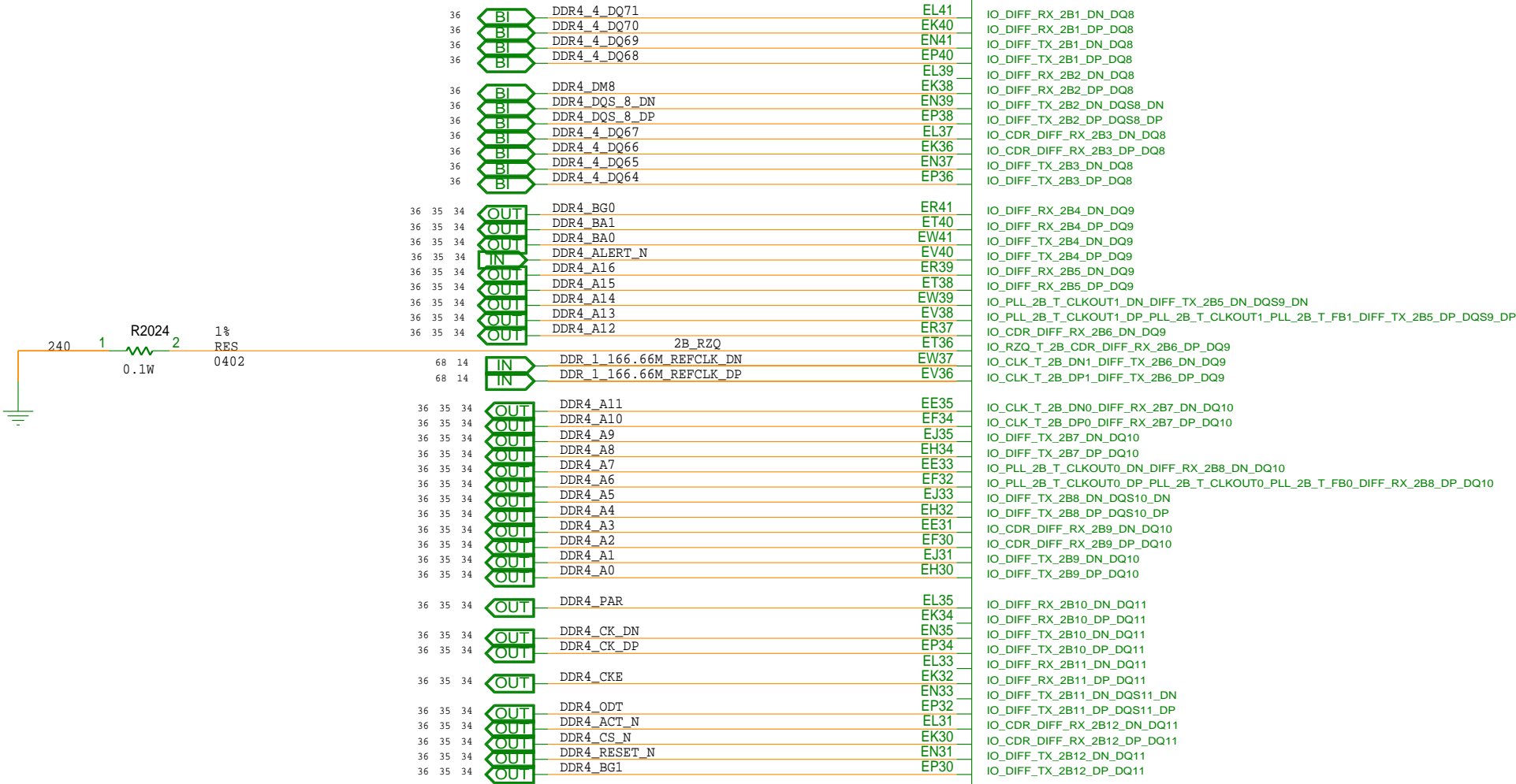
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FPGA BANK 2B

BGA
U1
EMPTY

HC_FM91_3948BGA

B



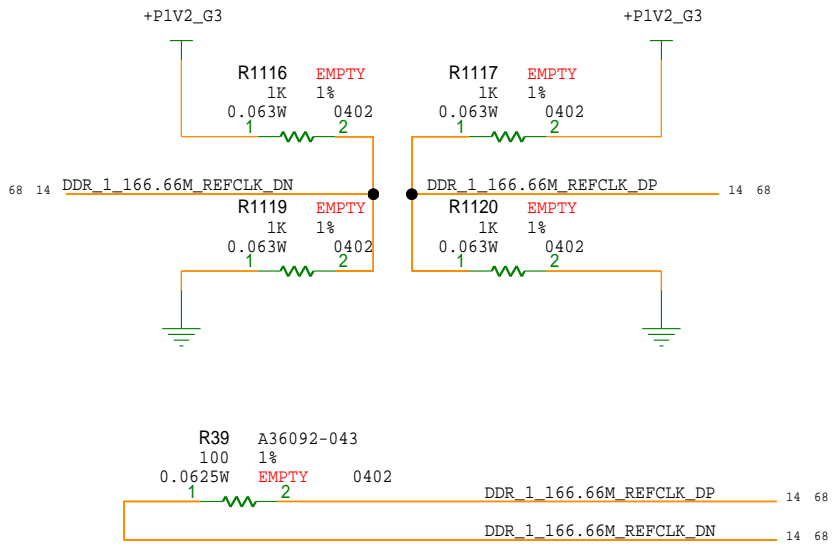
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TOP BOT

IO BANK 2B

3 OF 31

99C1H7



CAD NOTE:

PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA

Wed Mar 6 15:45:15 2024

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14 OF 105

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FPGA BANK 2A

BGA
U1
EMPTY

HC_FW91_3948BGA

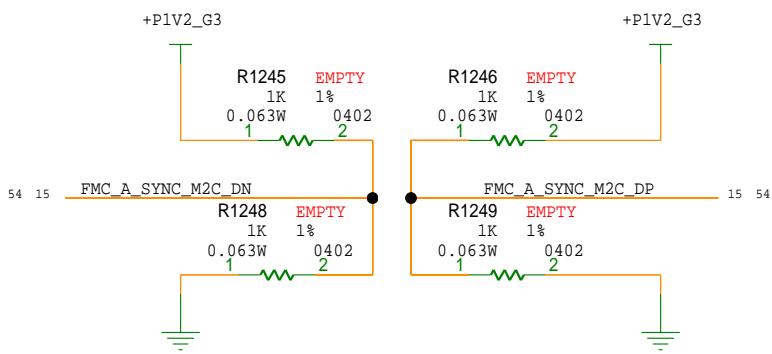


TOP BOT

IO BANK 2A

4 OF 31

99C1H7



CAD NOTE:

PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA

Wed Mar 6 15:45:16 2024

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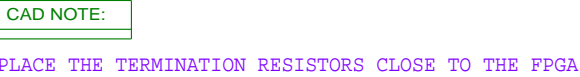


B



ANK 3B

99C1H7



PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA

R166 A36092-043
100 1%
0.0625W EMPTY 0402
1 2 CLK_100M_GPIO_4_DP 17 68
CLK_100M_GPIO_4_DN 17 68

R999 A36092-043
100 1%
0.0625W EMPTY 0402 DDR_3_166.66M_REFCLK_DP 17 68
1 2 DDR_3_166.66M_REFCLK_DN 17 68

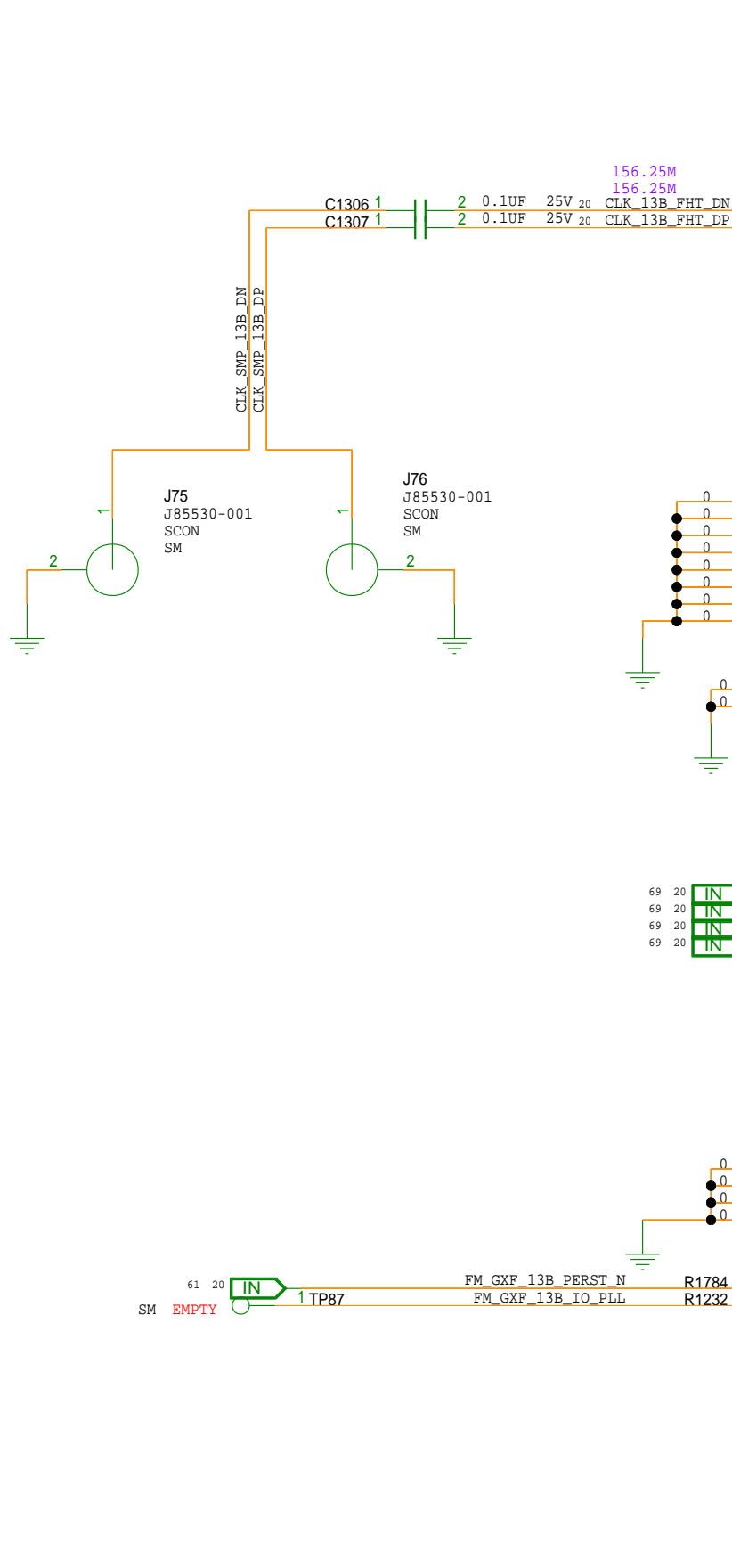
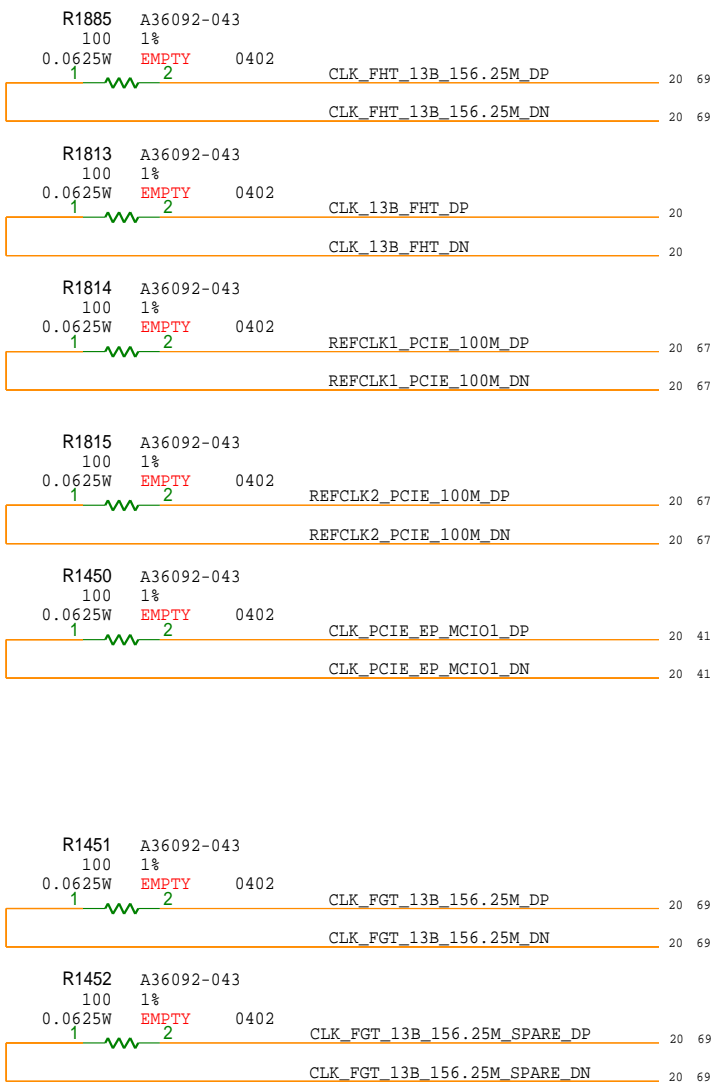
17 OF 105



FPGA BANK 13B

CAD NOTE:

PLACE THESE 100-OHM RES RIGHT BELOW FPGA BALLS
ON THE BREAKOUT VIAS.

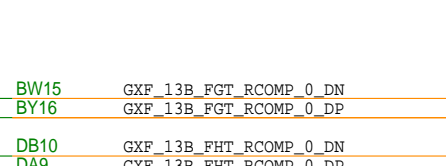
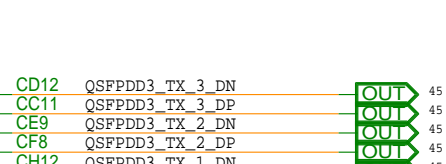
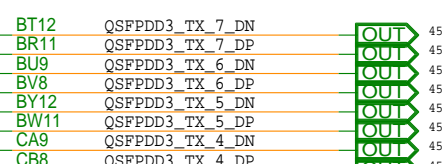
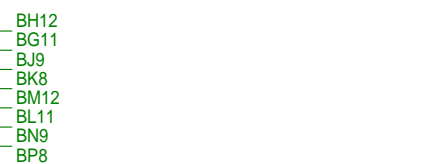
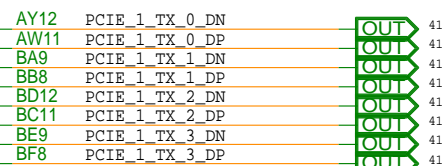
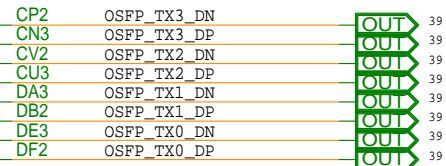


BGA
U1
EMPTY

HC_FM91_3948BGA

CAD NOTE:

PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS

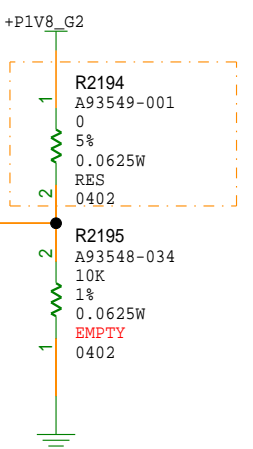


CAD NOTE:

Place RCOMP res right below FPGA balls
on the breakout vias.

DESIGN NOTE:

Indicates BARAK_18_USED



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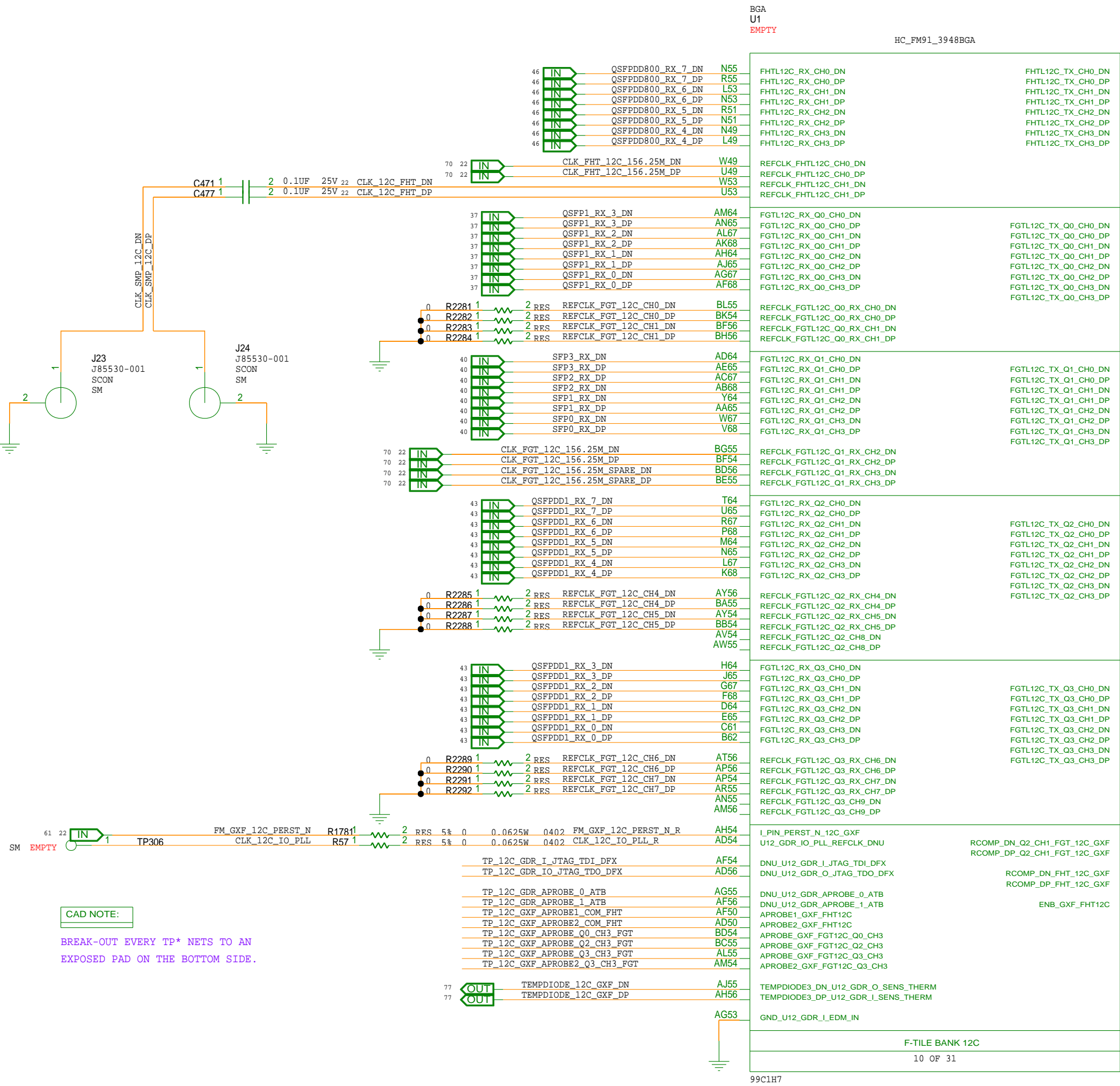
SCALE:

DO NOT SCALE DRAWING

SHEET

20 OF 105

FPGA BANK 12C



CAD NOTE:

PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS

DESIGN NOTE:

SFP2_TX/RX_DN/DP SIGNALS SWAPPED AS PER SI FEEDBACK FOR LAYOUT FESIBILITY.
NEED TO BE TAKEN CARE DURING VALIDATION.

CAD NOTE:

TRANSCEIVER PAIRS MAY BE SWAPPED
TO OPTIMIZE LAYOUT (EXCEPT UX CH0).

CAD NOTE:

Place RCOMP see right below FPGA balls
on the breakout vias.

AV56 GXP_12C_FGT_RCOMP_0_DN R2192 RES 499
AU55 GXP_12C_FGT_RCOMP_0_DP 0.1% 0.0625W 0402
AC51 GXP_12C_FHT_RCOMP_0_DN R2201 RES 1.5K
AB52 GXP_12C_FHT_RCOMP_0_DP 0.1% 0.063W 0402

AF52 U12_GXF_IO_DFX_0

DESIGN NOTE:

Indicates BAAAK_IS_USED

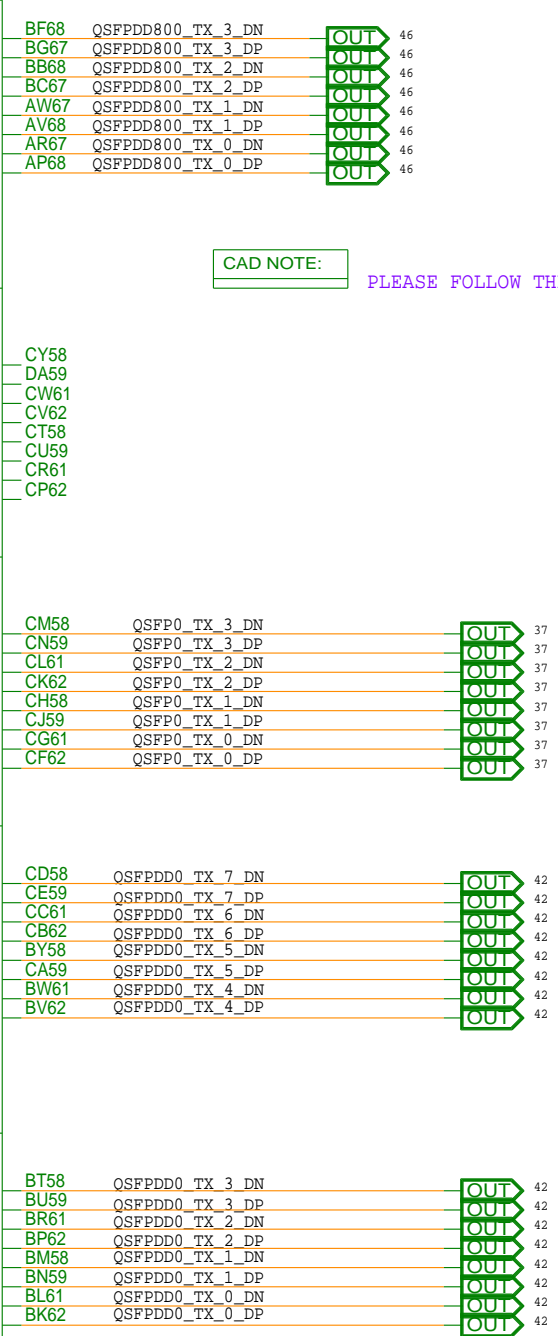
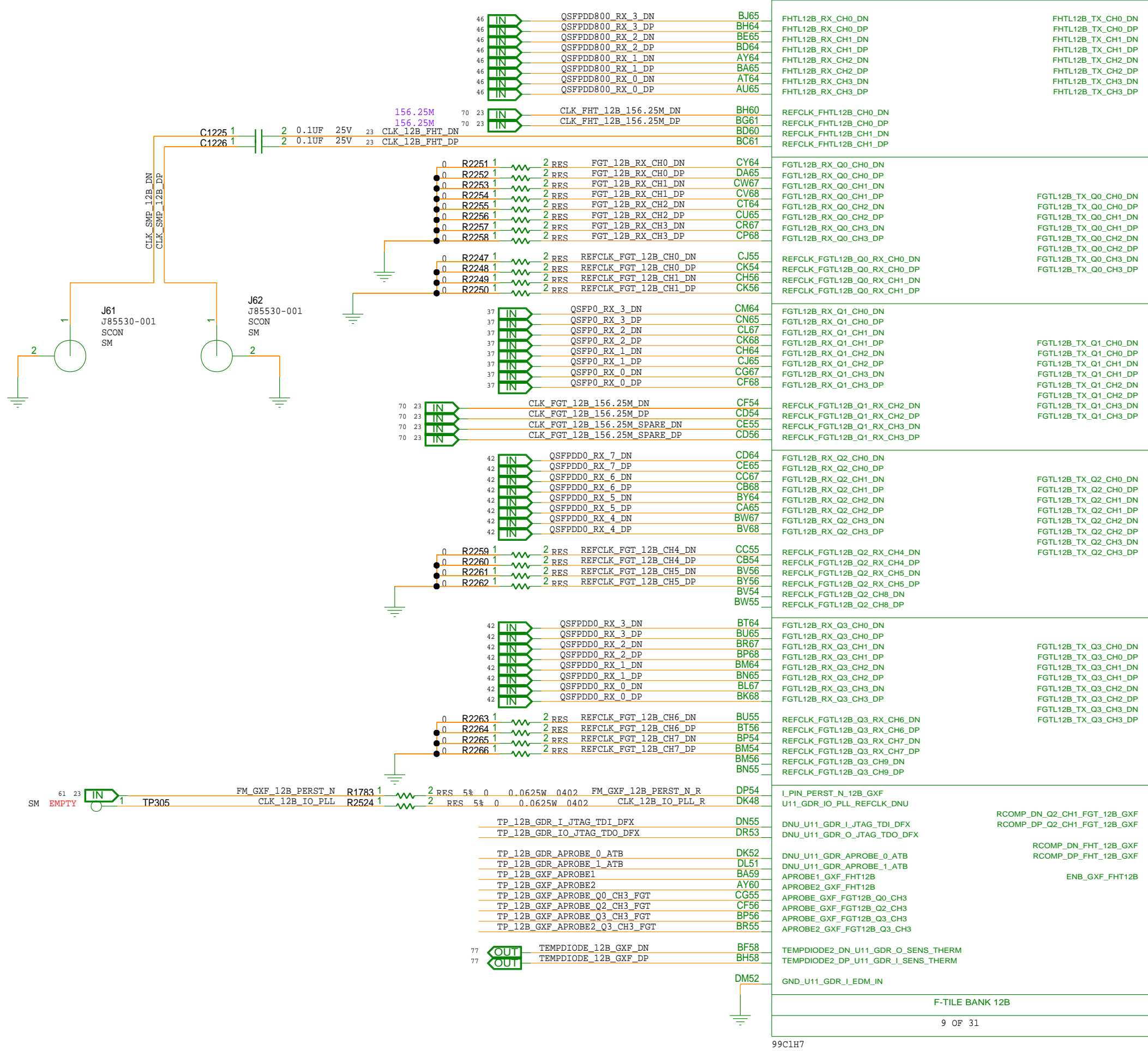
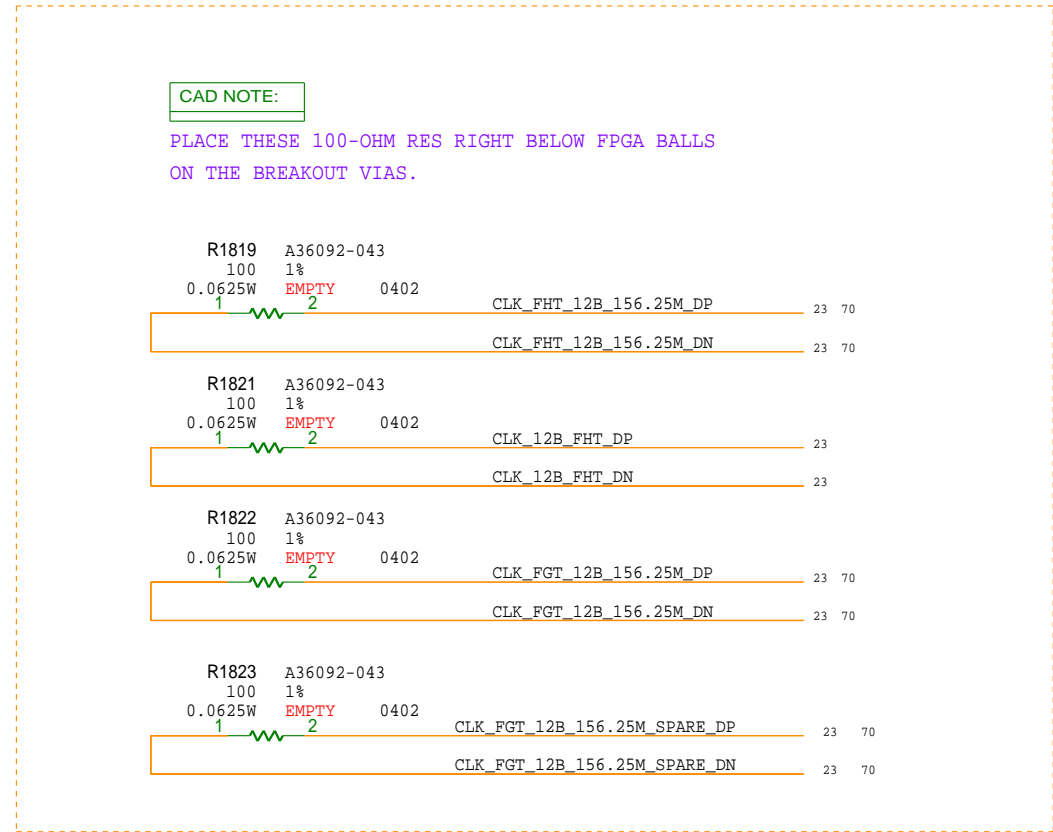
CAD NOTE:

PLACE THESE 100-OHM RES RIGHT BELOW FPGA BALLS
ON THE BREAKOUT VIAS.

R1808 A36092-043
100 1% 0.0625W EMPTY 0402 CLK_FHT_12C_156.25M_DP 22 70
CLK_FHT_12C_156.25M_DN 22 70
R1809 A36092-043
100 1% 0.0625W EMPTY 0402 CLK_12C_FHT_DP 22
CLK_12C_FHT_DN 22
R1810 A36092-043
100 1% 0.0625W EMPTY 0402 CLK_FGT_12C_156.25M_DP 22 70
CLK_FGT_12C_156.25M_DN 22 70
R998 A36092-043
100 1% 0.0625W EMPTY 0402 CLK_FGT_12C_156.25M_SPARE_DP 22 70
CLK_FGT_12C_156.25M_SPARE_DN 22 70

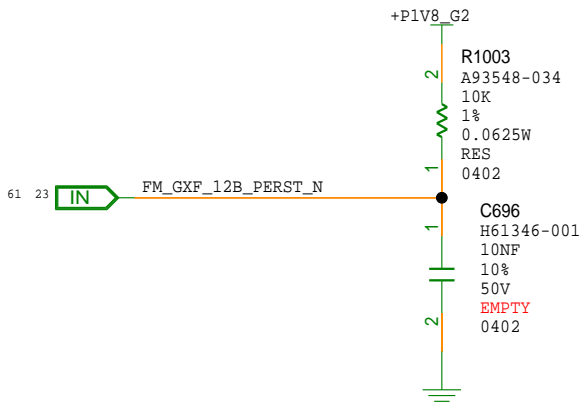
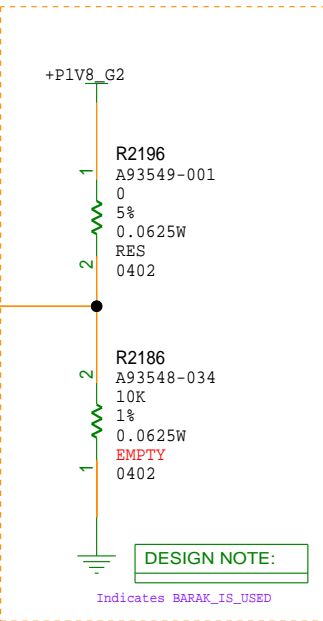
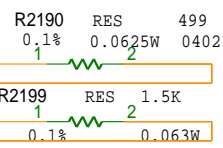
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FPGA BANK 12B



CAD NOTE:

Place RCOMP res right below FPGA balls on the breakout vias.



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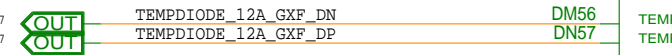
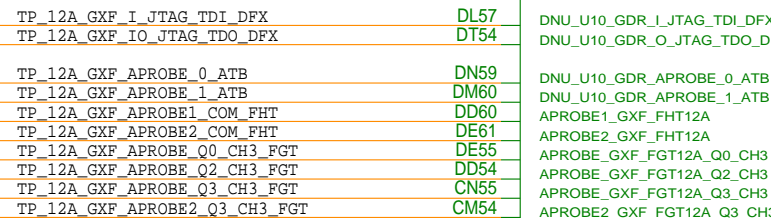
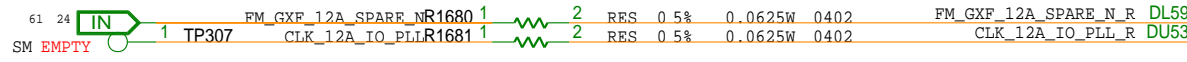
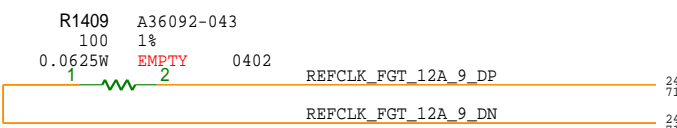
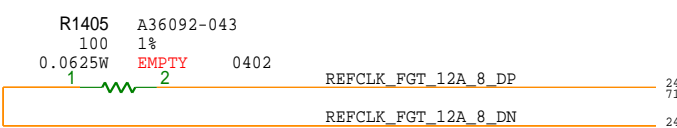
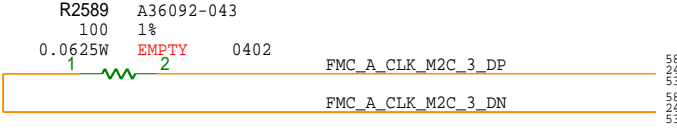
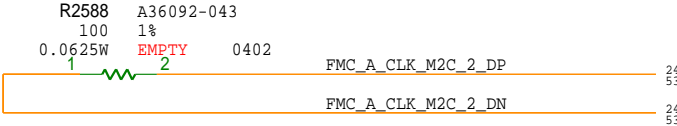
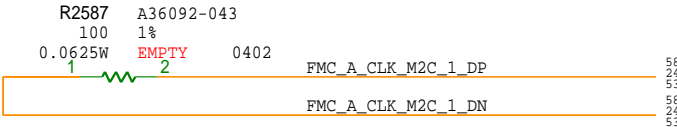
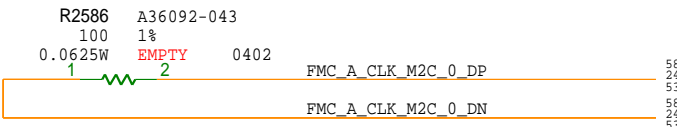
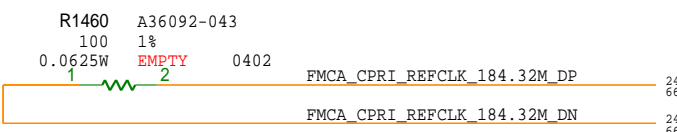
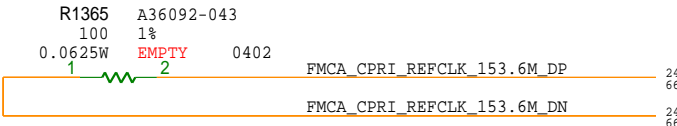
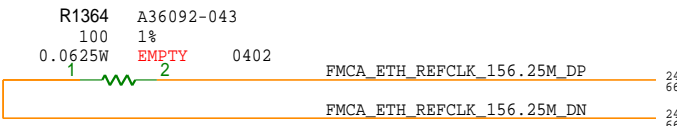
SHEET

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FPGA BANK 12A

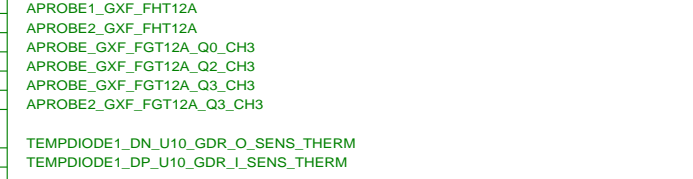
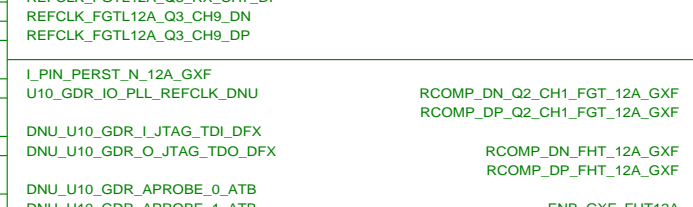
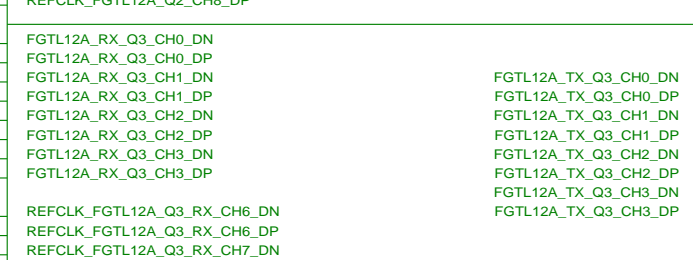
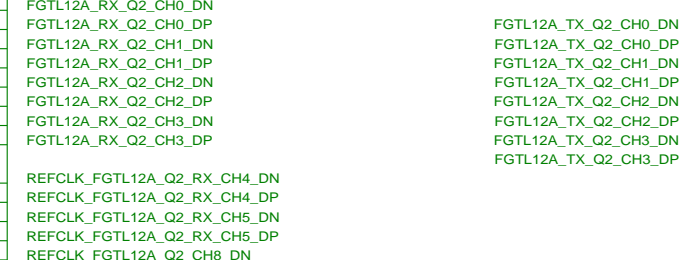
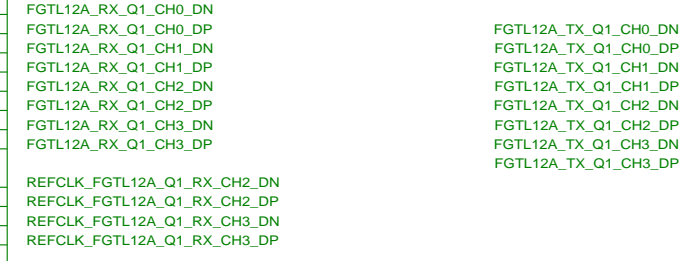
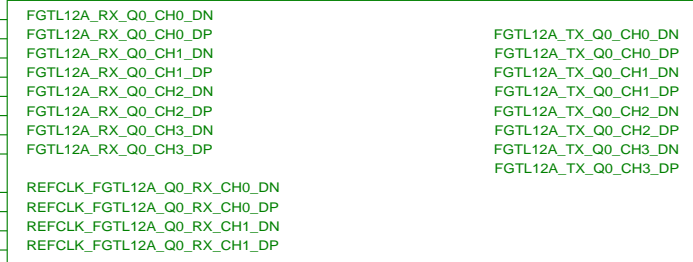
CAD NOTE:

PLACE THESE 100-OHM RES RIGHT BELOW FPGA BALLS
ON THE BREAKOUT VIAS.



BGA
U1
EMPTY

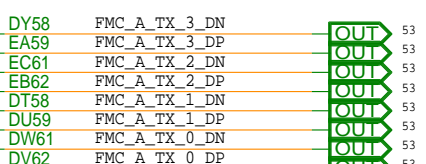
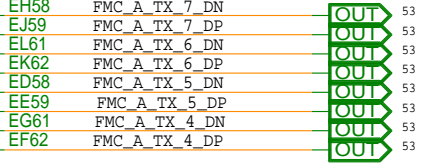
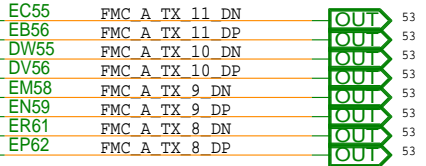
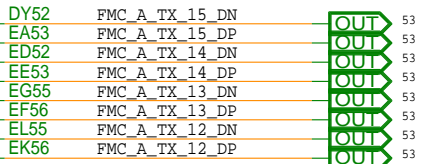
HC_FM91_3948BGA



99C1H7

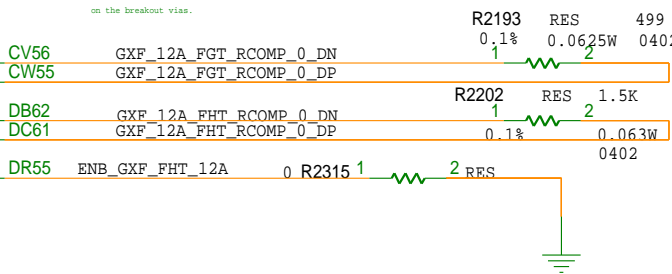
F-TILE BANK 12A

8 OF 31

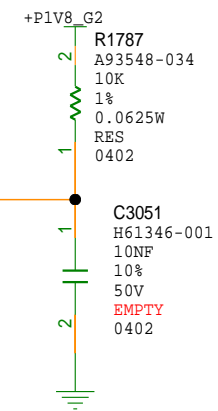


CAD NOTE:

Please follow the arc routing below FPGA balls
on the breakout vias.



CAD NOTE: PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS.



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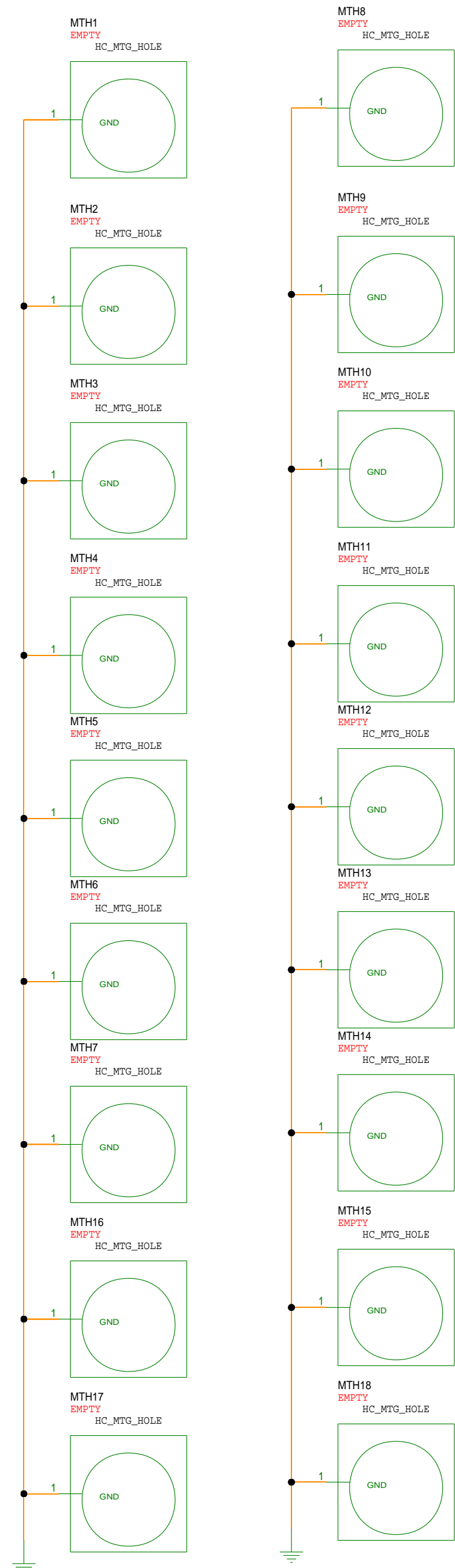
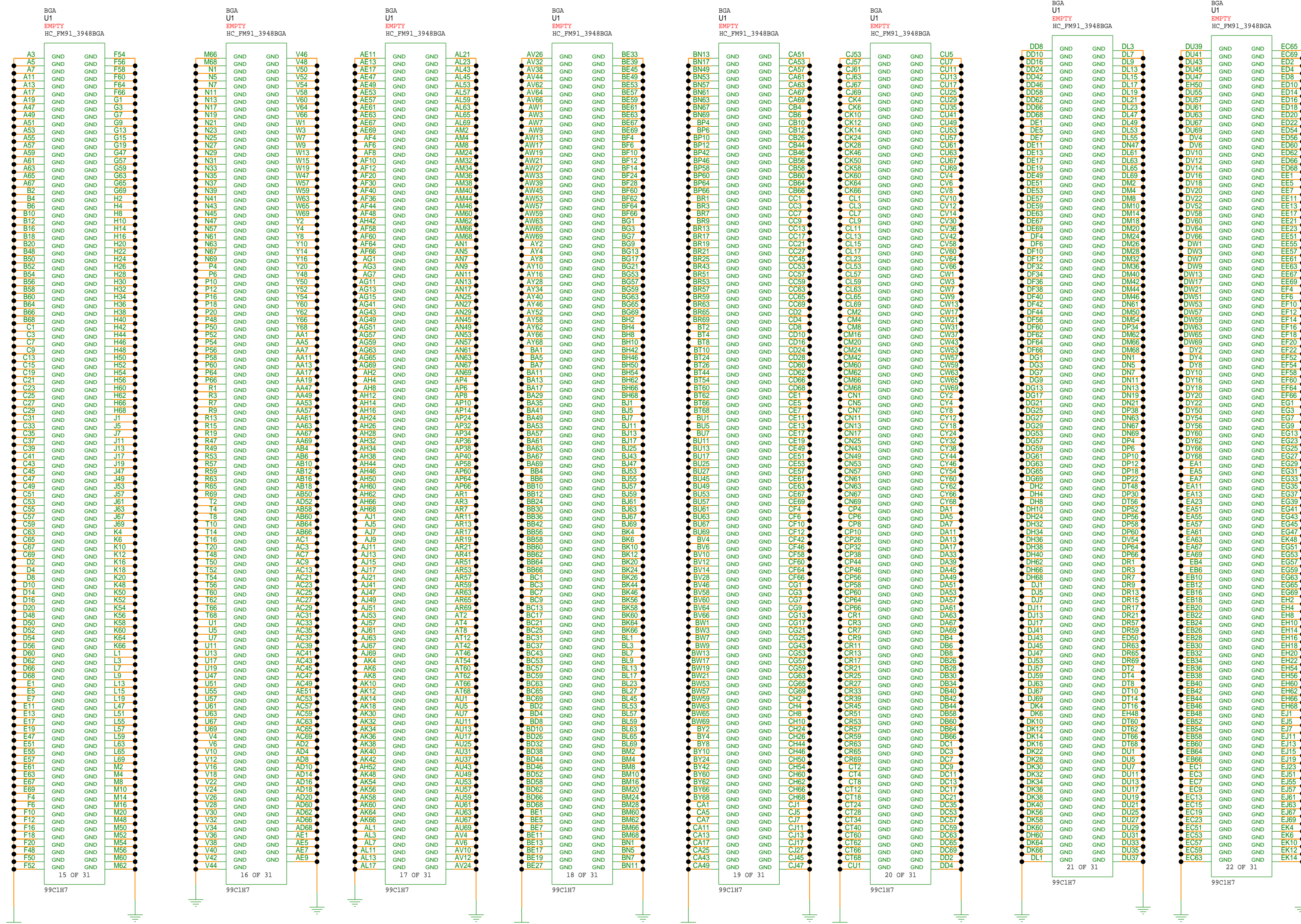
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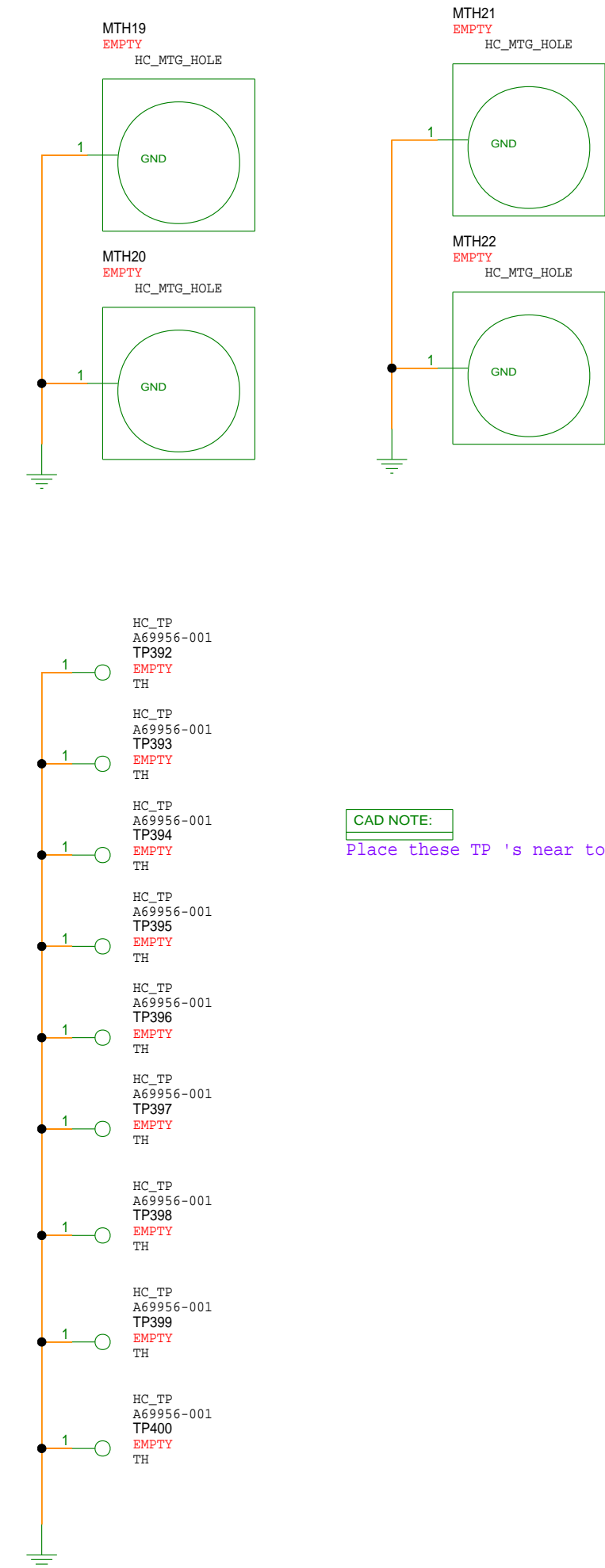
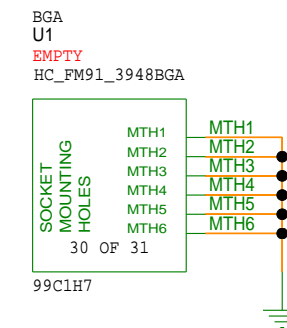
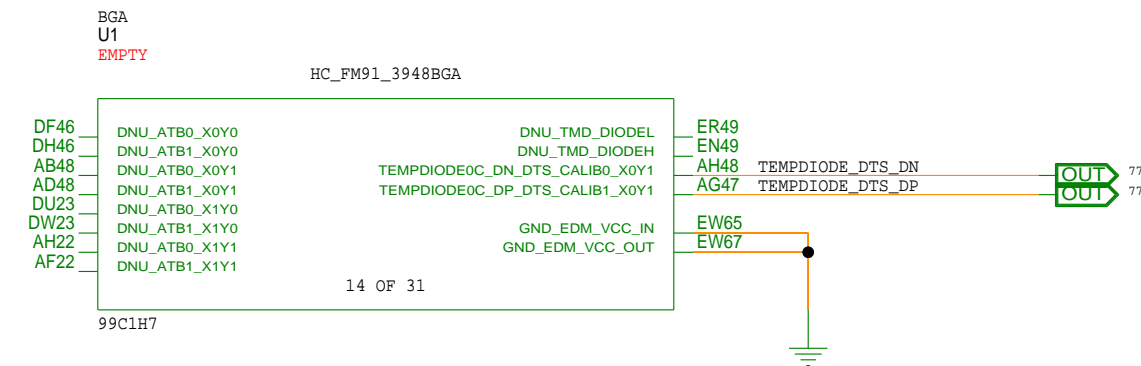
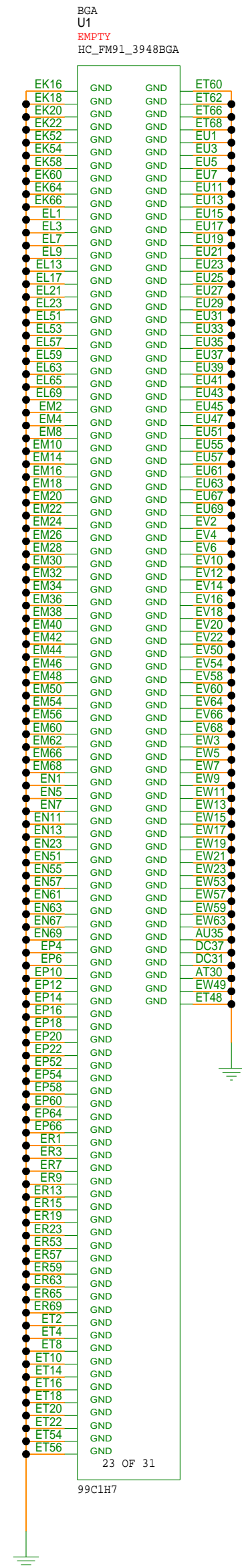
SHEET

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FPGA GND- II



CAD NOTE:
Place these TP 's near to VR's Enable/PG/Vout TP's.

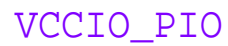
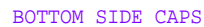
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VCCL



PER CHANNEL

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4

3

2

1

FPGA DECOUPLING - II



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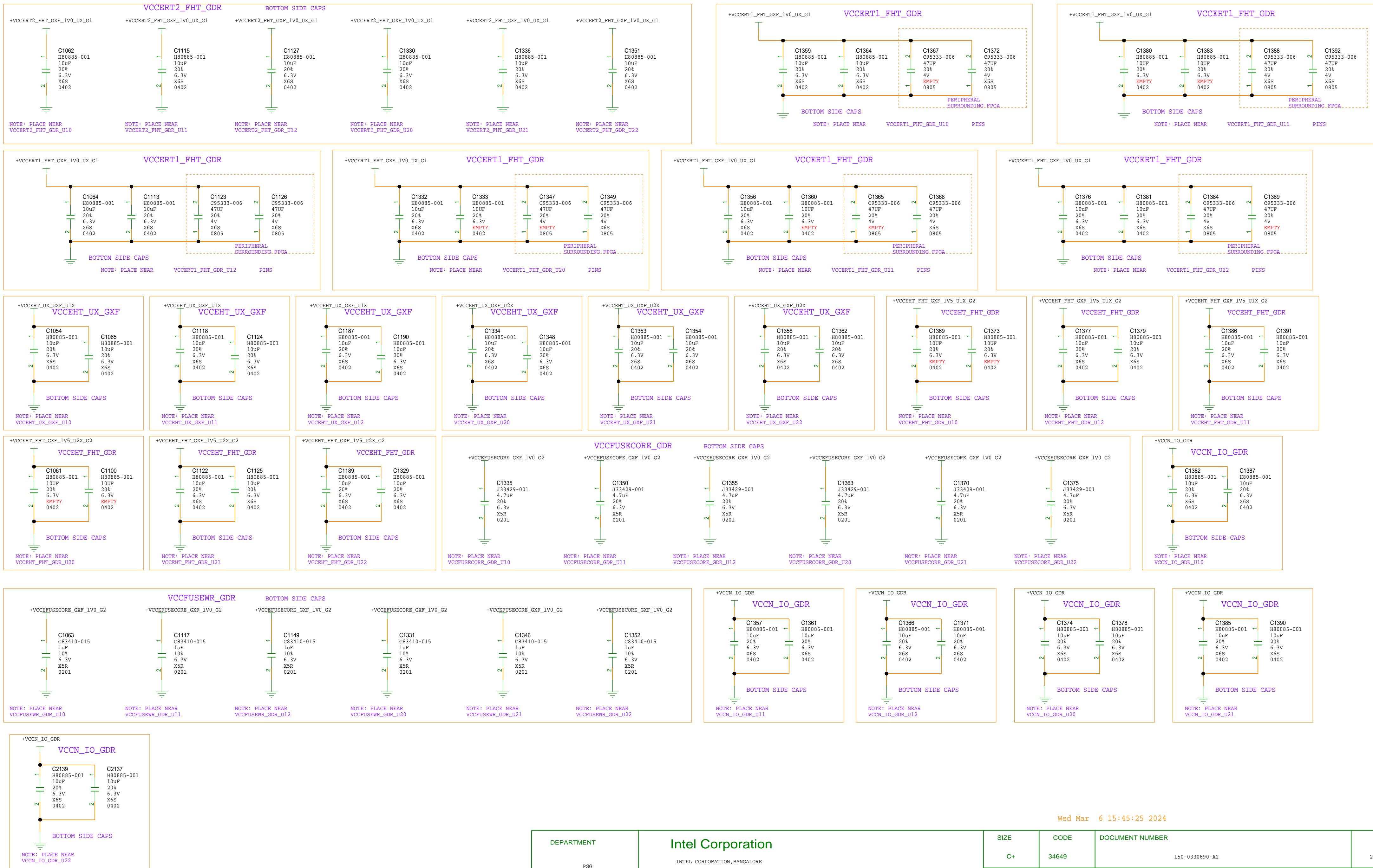
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3

2

1

FPGA DECOUPLING - III



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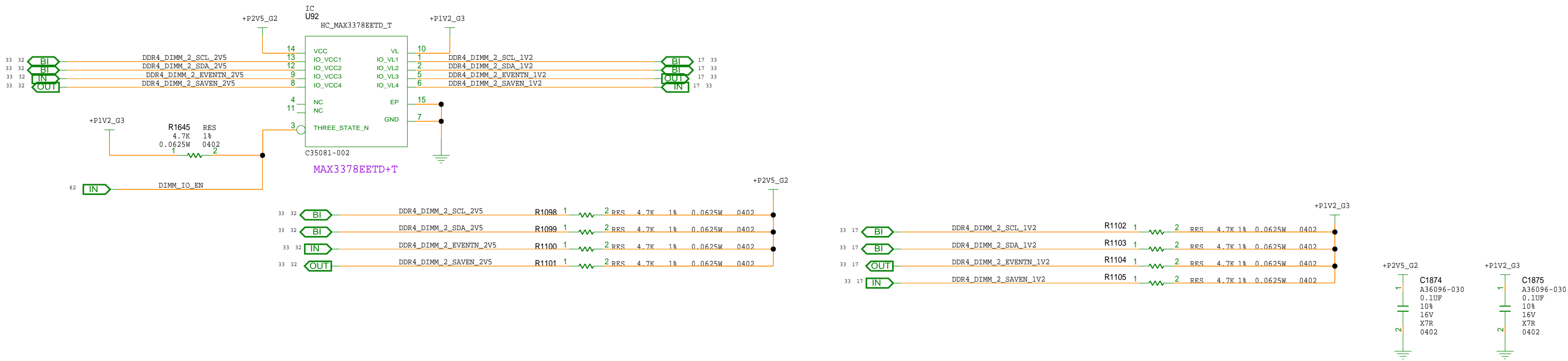
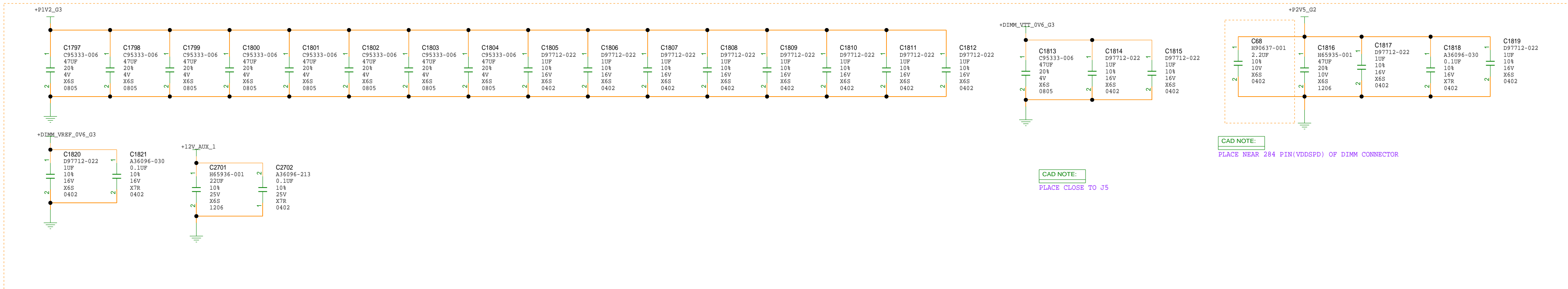


TEMPERATURE SENSOR - 18H



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1DPC DIMM-FILTER AND LVL SHIFTER



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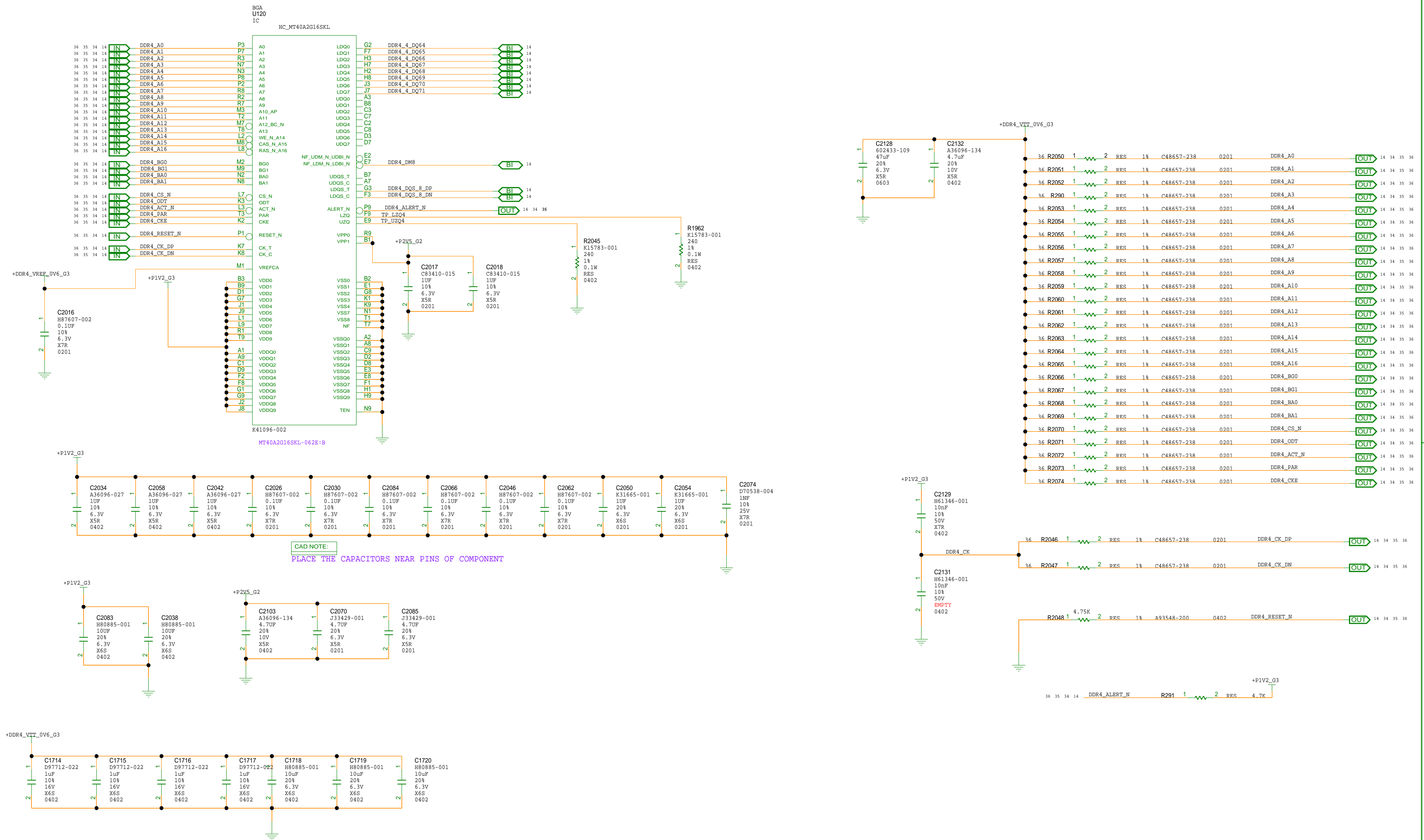
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DDR4-II

DDR4-III



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DEPARTMENT UNKNOWN	<div>Intel Corporation</div> <div>2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119</div>	SIZE	CODE	DOCUMENT NUMBER	REV
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4

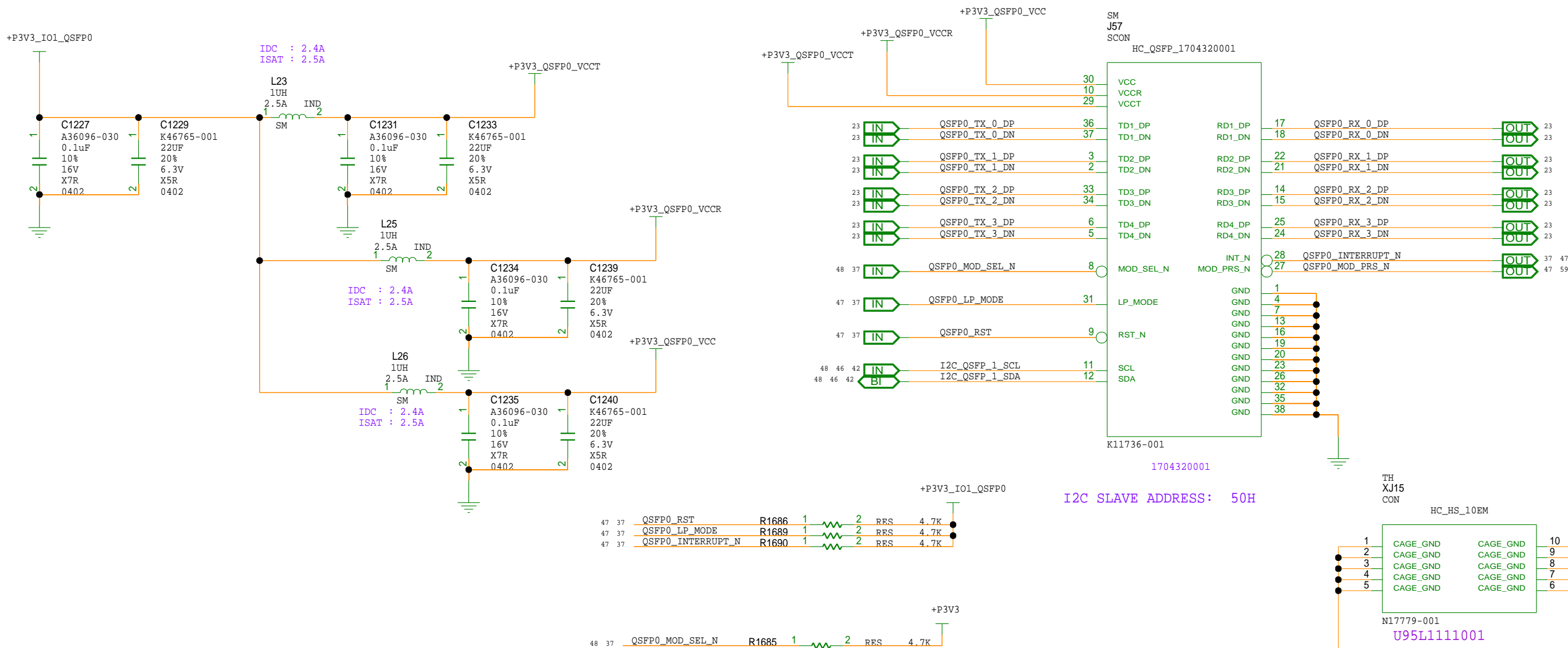
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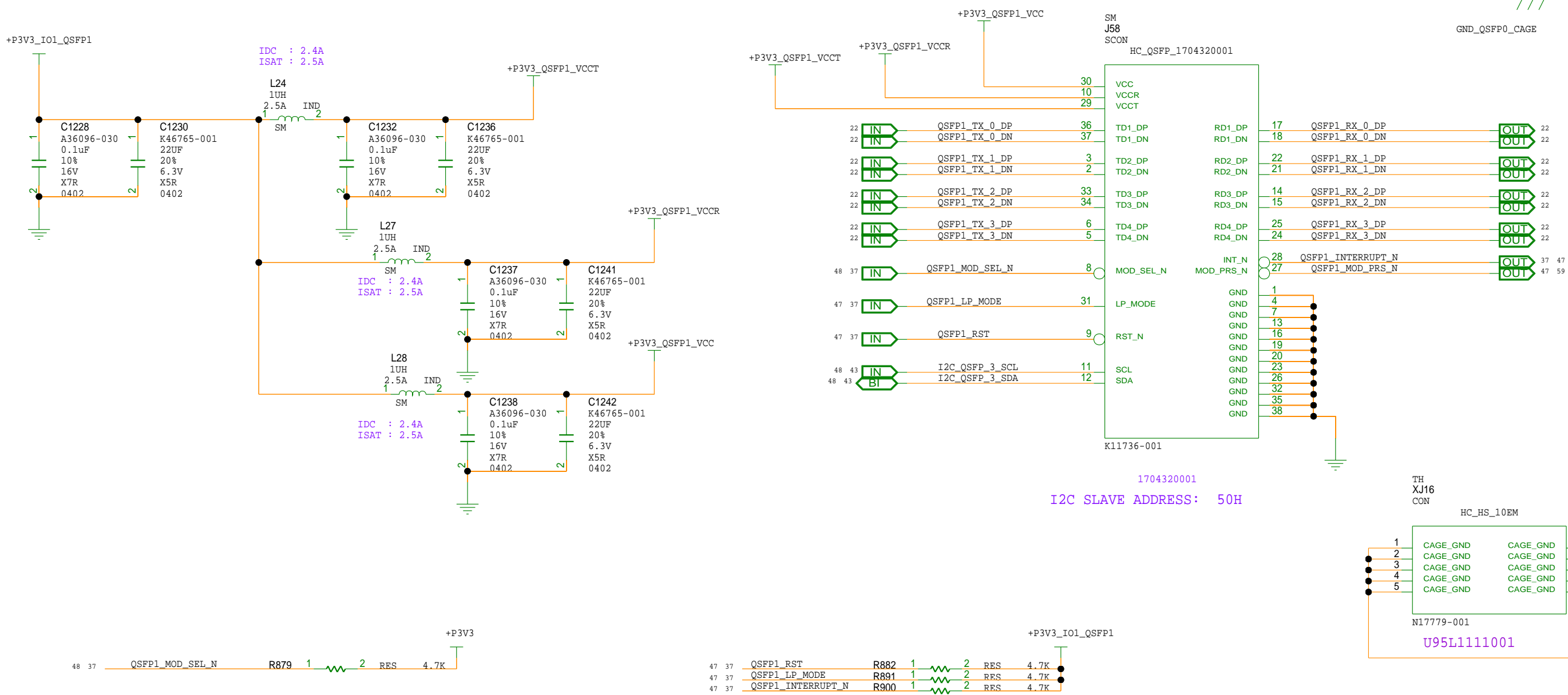
QSFP-0

12B-BANK



QSFP-1

12C-BANK



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4

3

2

1

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4

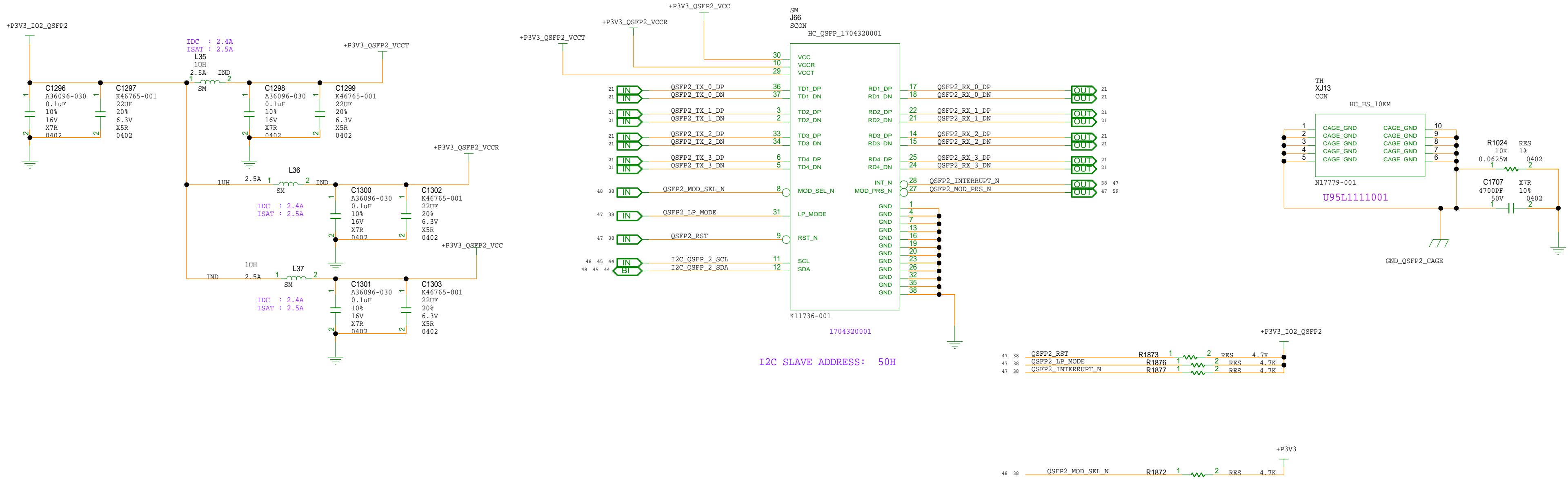
3

2

1

QSFP-2

13A-BANK



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4

3

2

1

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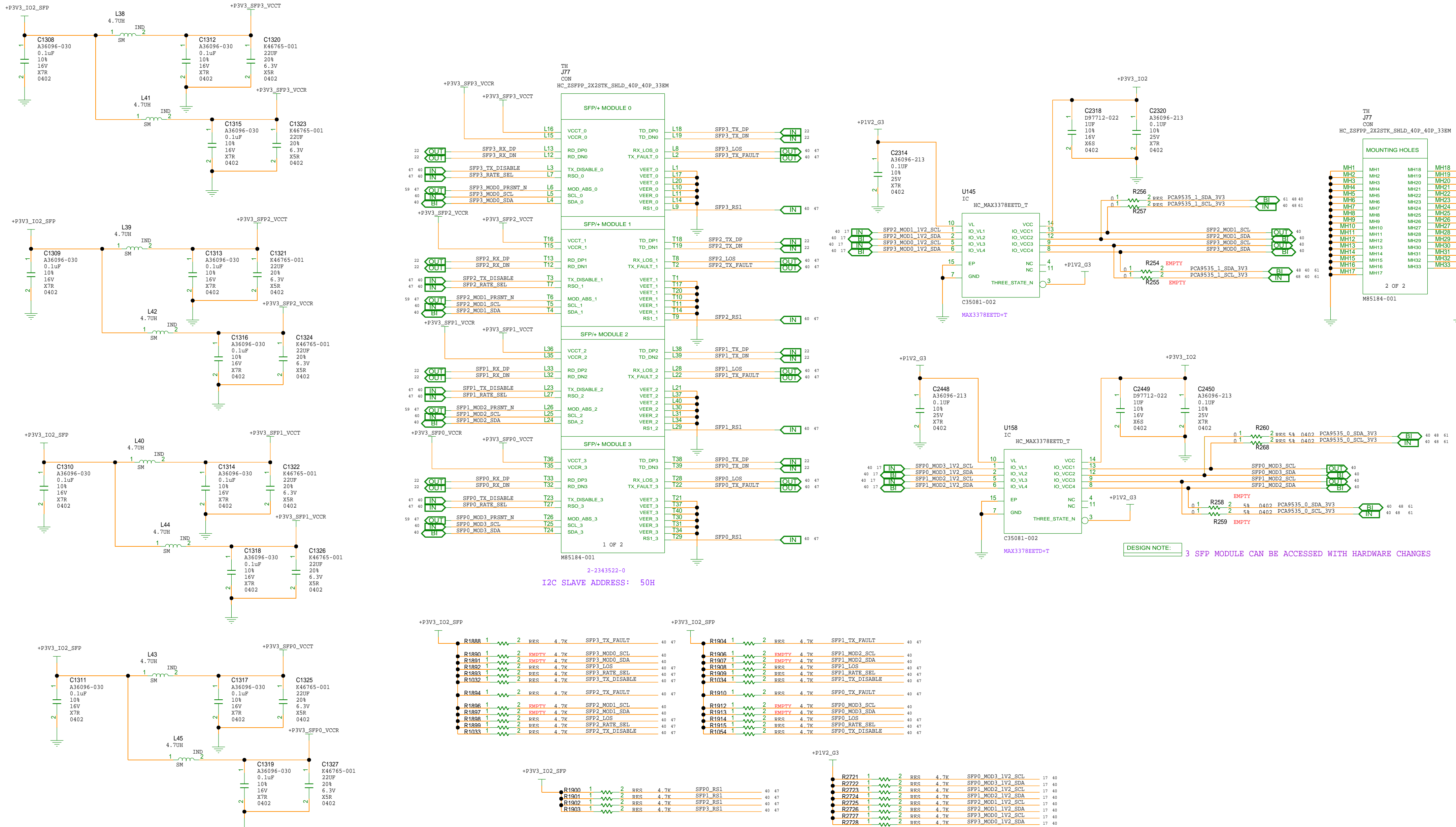
SHEET

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MODE	LPW_N	PRSNT_N
LOW POWER	LOW	LOW
HIGH POWER	HIGH	LOW
MODULE NOT PRESENT	-	HIGH



SFP CONNETCOR



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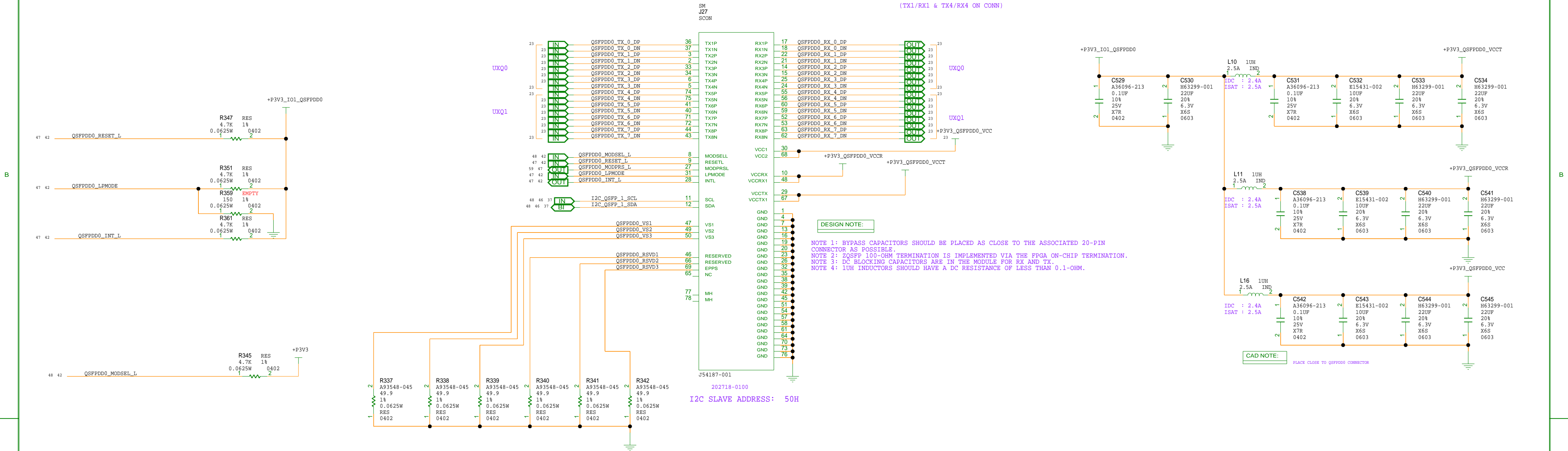
The schematic diagram illustrates the PCIe interface connections for three signals: BI, SDA, and ALERtn_A. Each signal line is connected to a resistor network (R949, R950, R951) and a pull-up resistor (+P3V3).

- BI (PCIe_1_SCL_A):** Connected to R949 (4.7K, 1%, 0.0625W) and R950 (4.7K, 1%, 0.0625W). The resistor network is connected to +P3V3.
- SDA (PCIe_1_SDA_A):** Connected to R950 (4.7K, 1%, 0.0625W) and R951 (4.7K, 1%, 0.0625W). The resistor network is connected to +P3V3.
- ALERtn_A (PCIe_1_ALERtn_A):** Connected to R951 (4.7K, 1%, 0.0625W) and R950 (4.7K, 1%, 0.0625W). The resistor network is connected to +P3V3.

The diagram shows the internal wiring of an AT24C512C I2C slave module. The HC_AT24C512C IC (pin 8 to 10) is connected to a 3V3 supply and ground. The 95972-001 IC (pin 1 to 3) is also connected to the 3V3 supply and ground. The module includes several resistors (R3200, R3202, R3204, R3201, R3203, R3205) and a pull-up resistor (R3206). The I2C slave address is 50h.

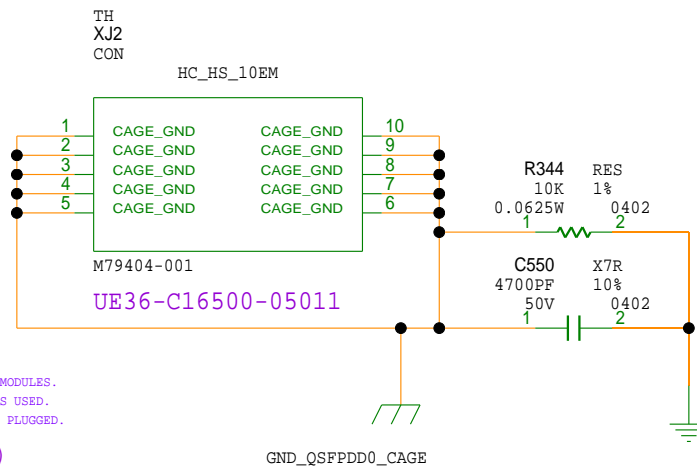
QSFP-DD CONN #0 (56G ETHERNET)

DESIGN NOTE:
CHANNELS MAY BE SWAPPED
WITHIN EACH UX BLOCK TO OPTIMIZE ROUTINGS.
LANE 0 & 4 MAY NOT BE SWAPPED.
(TX1/RX1 & TX4/RX4 ON CONN)



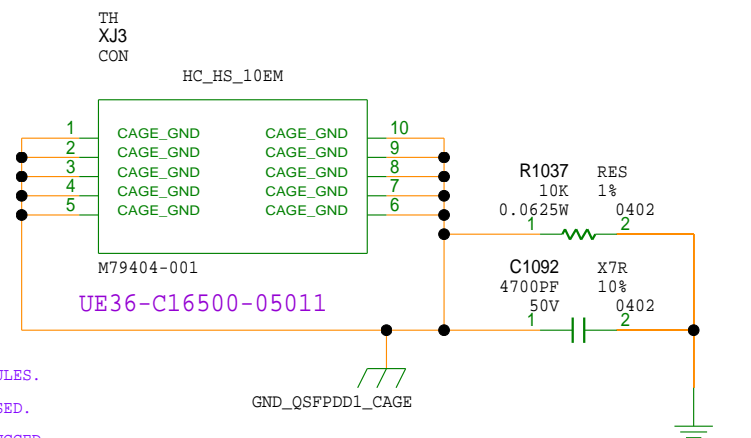
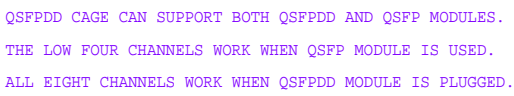
CAD NOTE:
PLACE CLOSE TO QSFPDD0 CONNECTOR

DESIGN NOTE:
QSFPDD CAGE CAN SUPPORT BOTH QSFPDD AND QSFP MODULES.
THE LOW FOUR CHANNELS WORK WHEN QSFP MODULE IS USED.
ALL EIGHT CHANNELS WORK WHEN QSFPDD MODULE IS PLUGGED.
K23336-002 (Molex cage)
CAN BE USED AS ALTERNATE CAGE.



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UXQ1

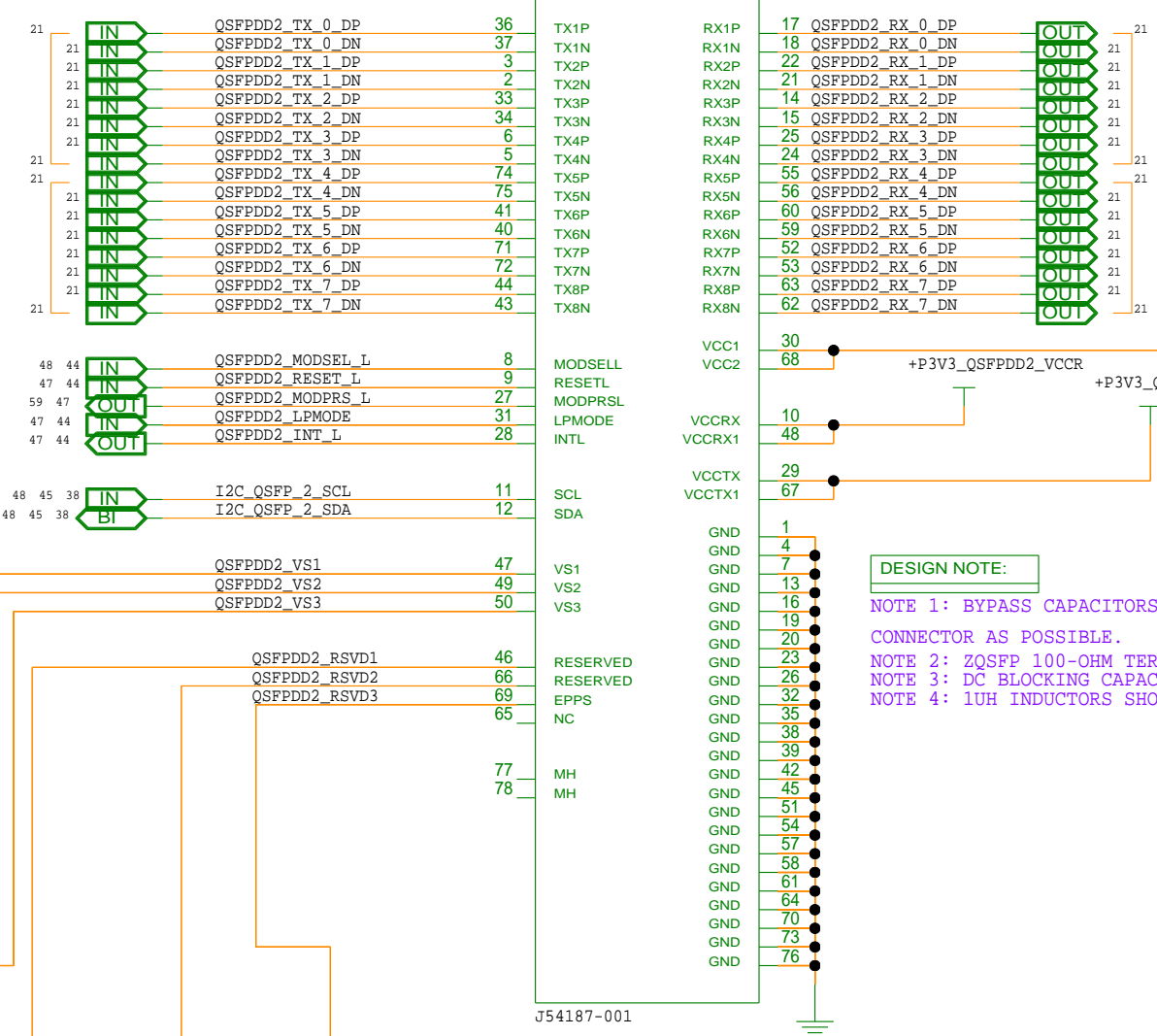


QSFP-DD CONN #2 (56G ETHERNET)

DESIGN NOTE: CHANNELS MAY BE SWAPPED WITHIN EACH UX BLOCK TO OPTIMIZE ROUTINGS. LANE 0 & 4 MAY NOT BE SWAPPED. (TX1/RX1 & TX4/RX4 ON CONN)

J69

SCON



202718-0100

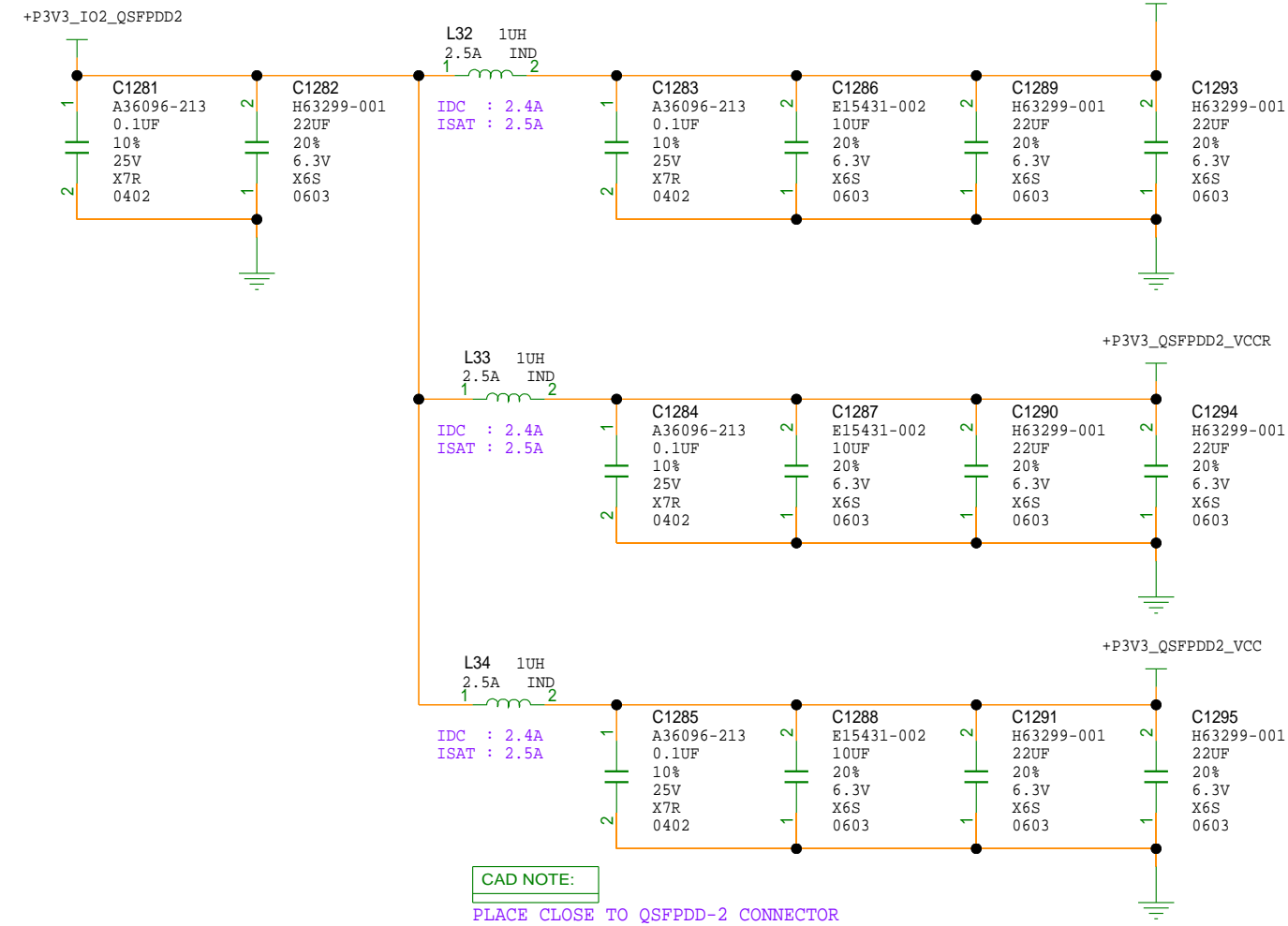
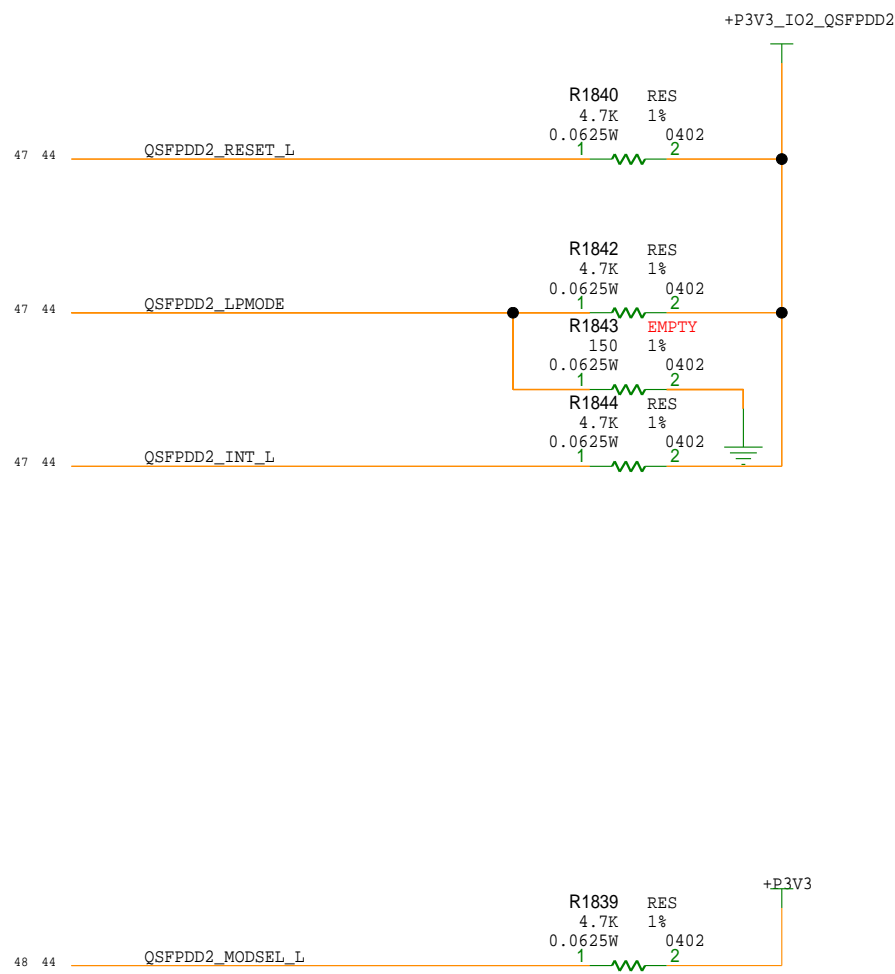
I2C SLAVE ADDRESS: 50H

DESIGN NOTE:

QSFPDD CAGE CAN SUPPORT BOTH QSFPDD AND QSFP MODULES. THE LOW FOUR CHANNELS WORK WHEN QSFP MODULE IS USED. ALL EIGHT CHANNELS WORK WHEN QSFPDD MODULE IS PLUGGED.

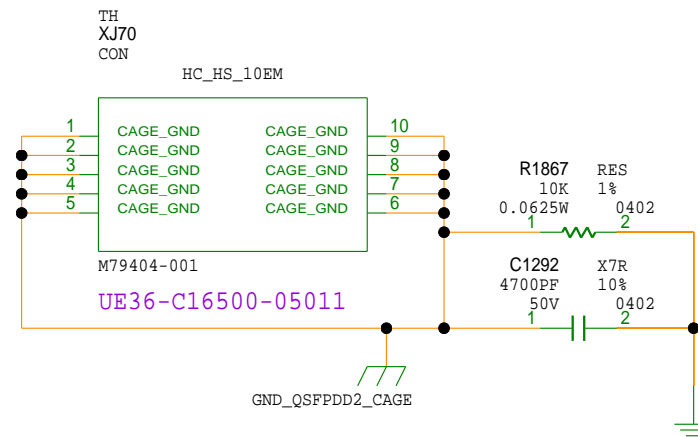
DESIGN NOTE:

NOTE 1: BYPASS CAPACITORS SHOULD BE PLACED AS CLOSE TO THE ASSOCIATED 20-PIN CONNECTOR AS POSSIBLE.
NOTE 2: ZQSFP 100-OHM TERMINATION IS IMPLEMENTED VIA THE FPGA ON-CHIP TERMINATION.
NOTE 3: DC BLOCKING CAPACITORS ARE IN THE MODULE FOR RX AND TX.
NOTE 4: 1UH INDUCTORS SHOULD HAVE A DC RESISTANCE OF LESS THAN 0.1-OHM.



CAD NOTE:

PLACE CLOSE TO QSFPDD-2 CONNECTOR



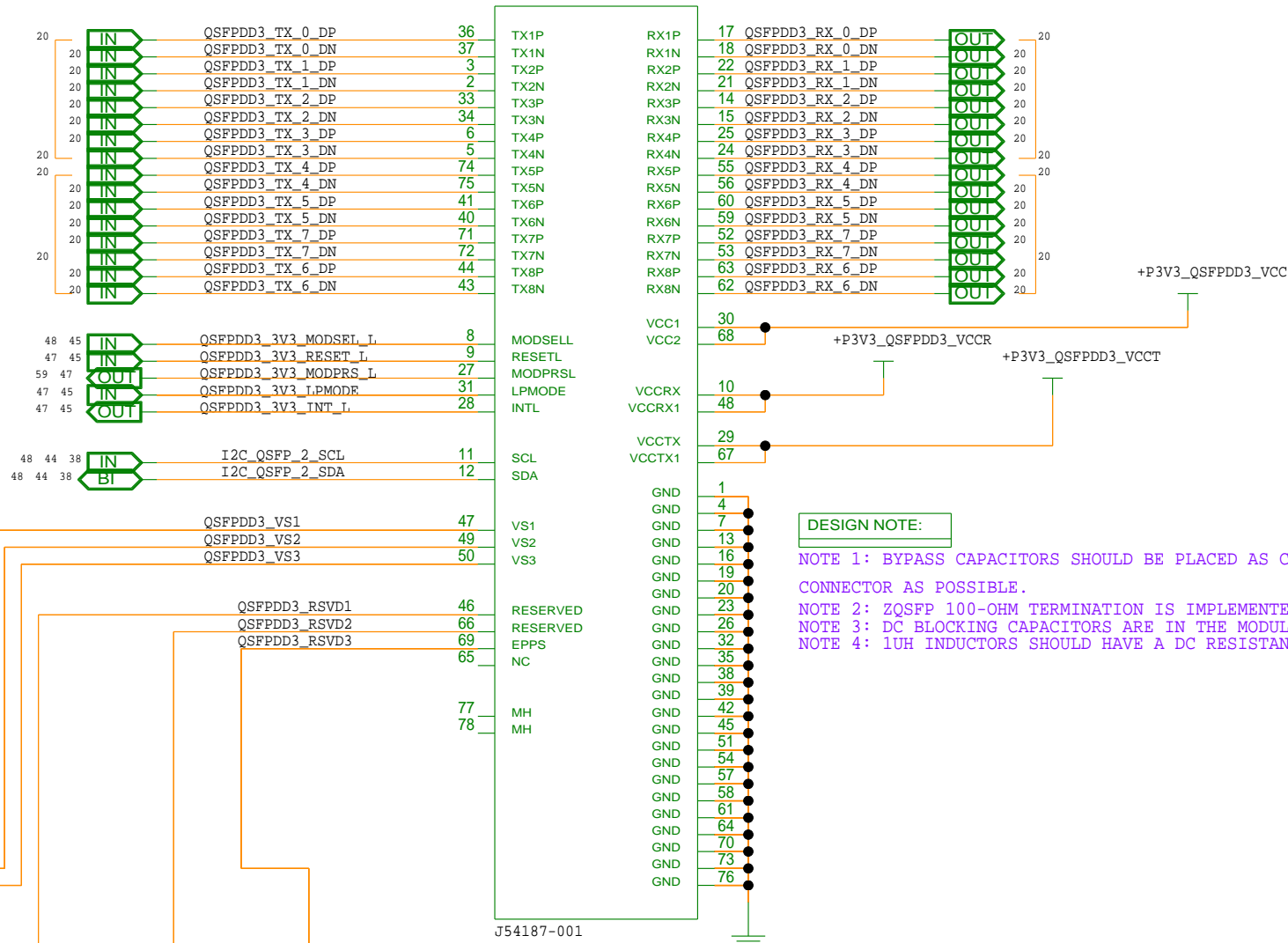
Wed Mar 6 15:45:34 2024

QSFP-DD CONN #3 (56G ETHERNET)

DESIGN NOTE:

CHANNELS MAY BE SWAPPED
WITHIN EACH UX BLOCK TO OPTIMIZE ROUTINGS.
LANE 0 & 4 MAY NOT BE SWAPPED.
(TX1/RX1 & TX4/RX4 ON CONN)

J67
SCON



DESIGN NOTE:

NOTE 1: BYPASS CAPACITORS SHOULD BE PLACED AS CLOSE TO THE ASSOCIATED 20-PIN CONNECTOR AS POSSIBLE.
NOTE 2: ZQSFP 100-OHM TERMINATION IS IMPLEMENTED VIA THE FPGA ON-CHIP TERMINATION.
NOTE 3: DC BLOCKING CAPACITORS ARE IN THE MODULE FOR RX AND TX.
NOTE 4: 1UH INDUCTORS SHOULD HAVE A DC RESISTANCE OF LESS THAN 0.1-OHM.

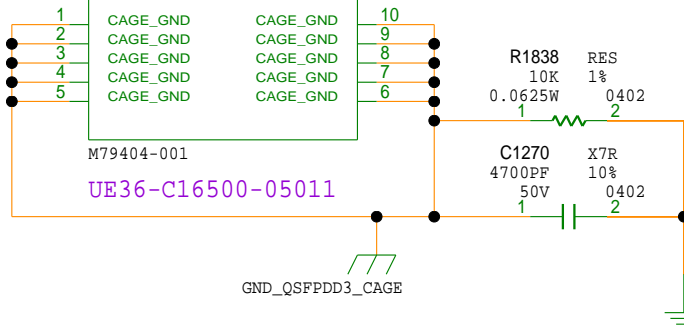
202718-0100
I2C SLAVE ADDRESS: 50H

CAD NOTE:

PLACE CLOSE TO QSFPDD-3 CONNECTOR

TH
XJ68
CON

HC_HS_10EM



DESIGN NOTE:

QSFPDD CAGE CAN SUPPORT BOTH QSFPDD AND QSFP MODULES.
THE LOW FOUR CHANNELS WORK WHEN QSFP MODULE IS USED.
ALL EIGHT CHANNELS WORK WHEN QSFPDD MODULE IS PLUGGED.

Wed Mar 6 15:45:35 2024

DEPARTMENT

Intel Corporation

SIZE

CODE

DOCUMENT NUMBER

REV

PSG

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C+

34649

150-0330690-A2

2.0

SCALE:

DO NOT SCALE DRAWING

SHEET

45 OF 105

QSFP-DD-800 CONN (112G ETHERNET)

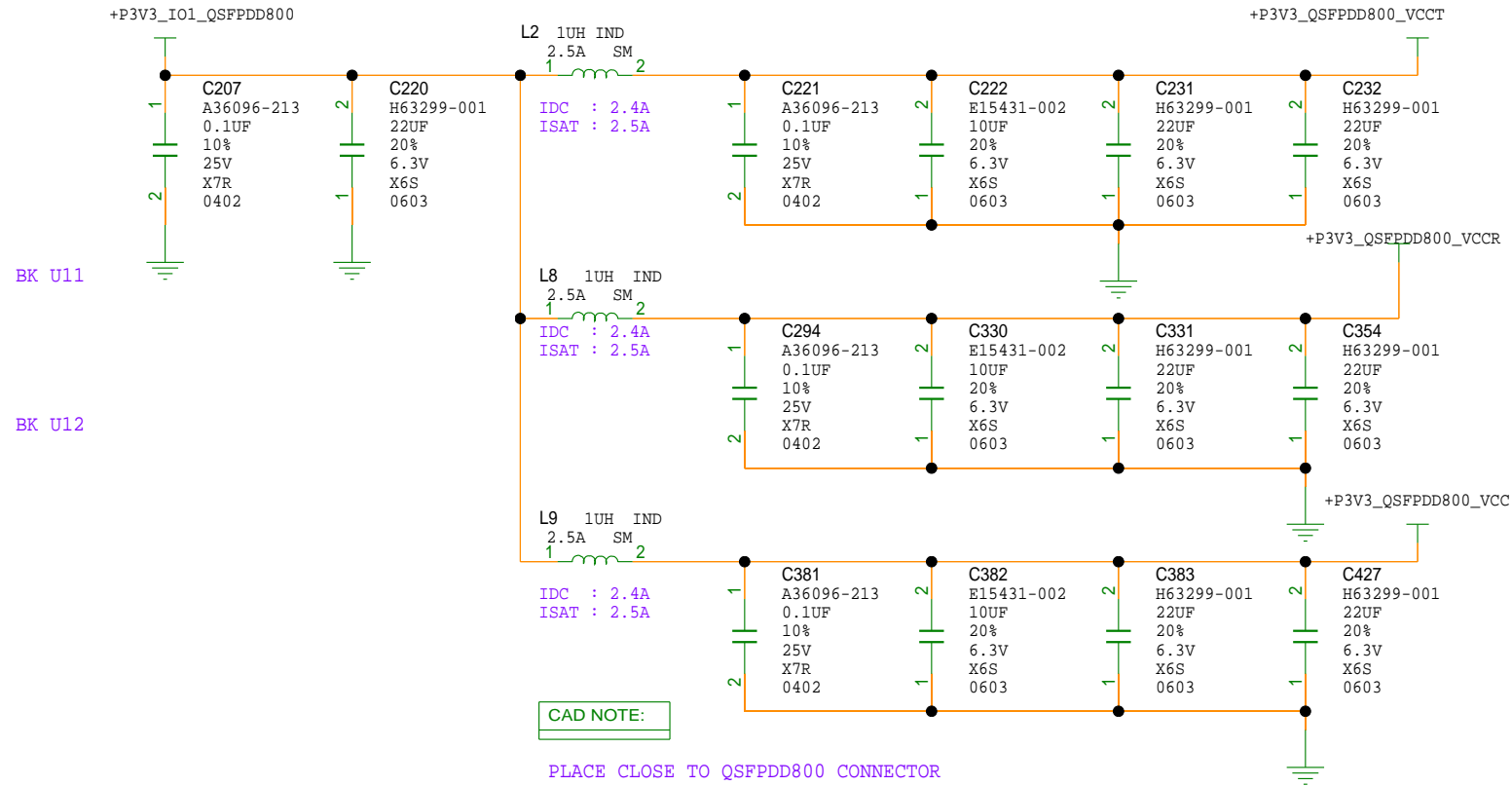
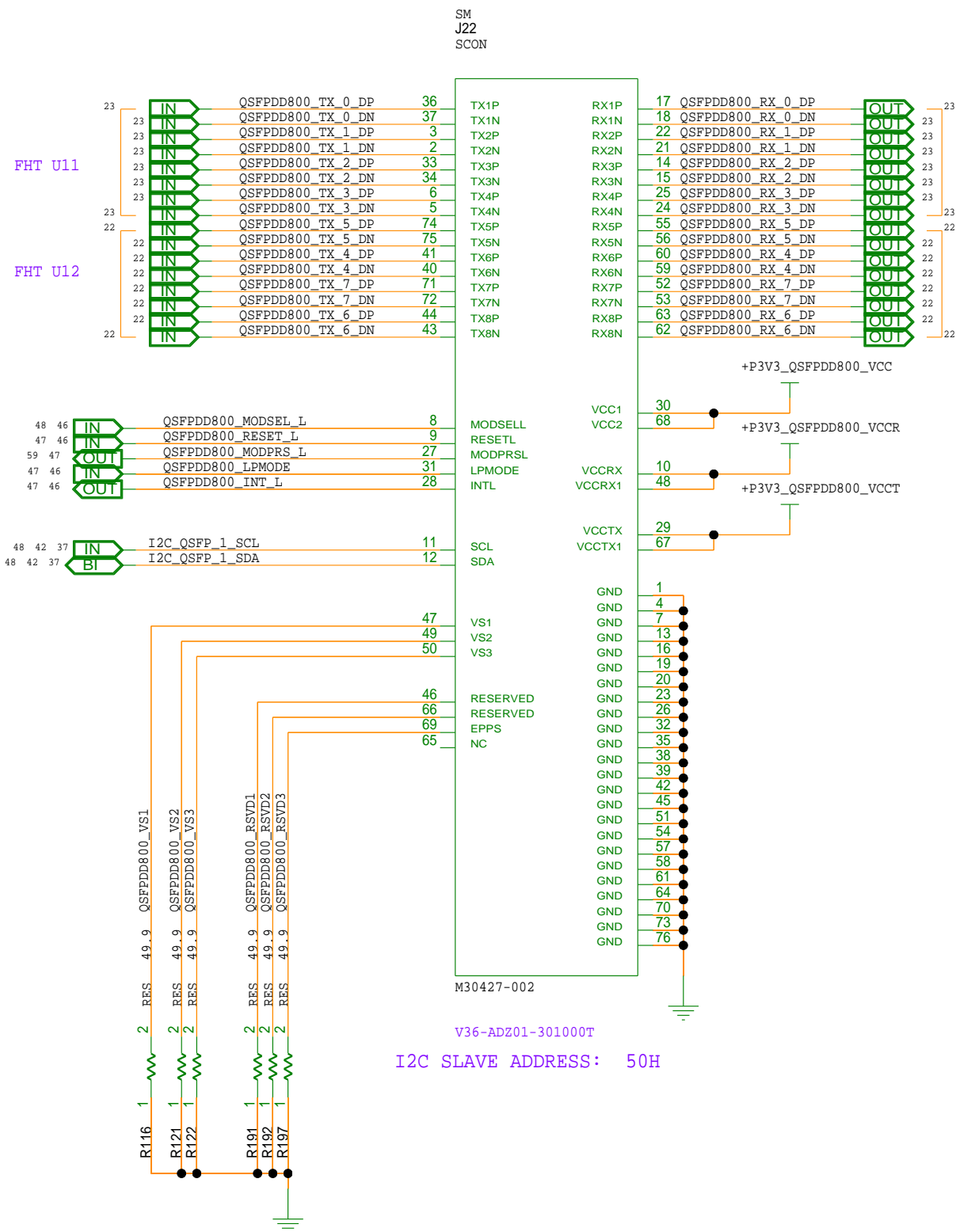
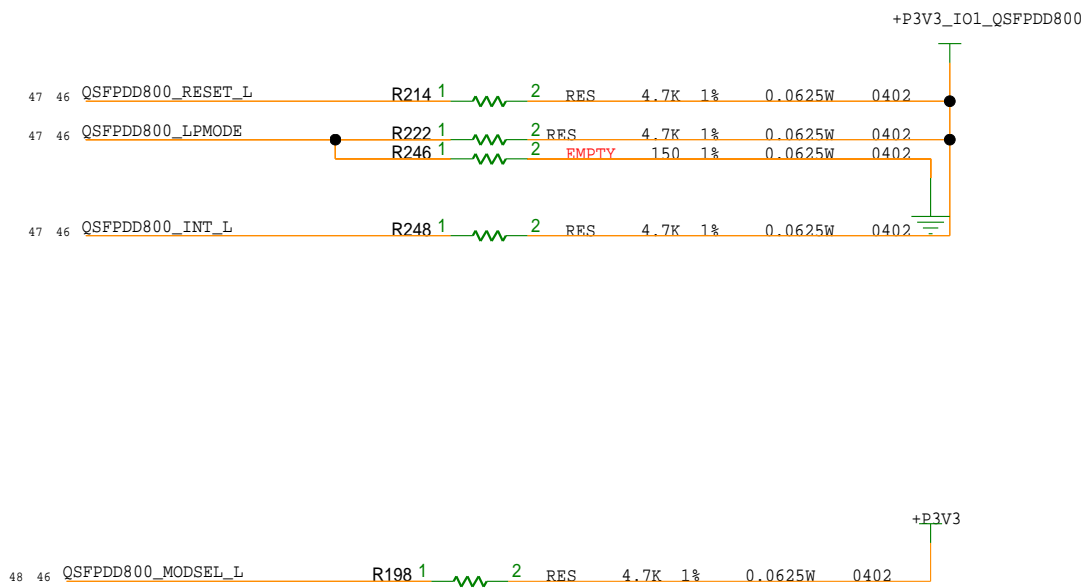
DESIGN NOTE:

CHANNELS MAY BE SWAPPED
WITHIN EACH BK BLOCK TO OPTIMIZE ROUTINGS.
SWAP BOTH TX & RX TOGETHER.

DESIGN NOTE:

NOTE 4: 1UH INDUCTORS SHOULD HAVE A DC RESISTANCE OF LESS THAN 0.1-OHM.
NOTE 2: ZQSFP 100-OHM TERMINATION IS IMPLEMENTED VIA THE FPGA ON-CHIP TERMINATION.
NOTE 1: BYPASS CAPACITORS SHOULD BE PLACED AS CLOSE TO THE ASSOCIATED 20-PIN
CONNECTOR AS POSSIBLE.
NOTE 3: DC BLOCKING CAPACITORS ARE IN THE MODULE FOR RX AND TX.

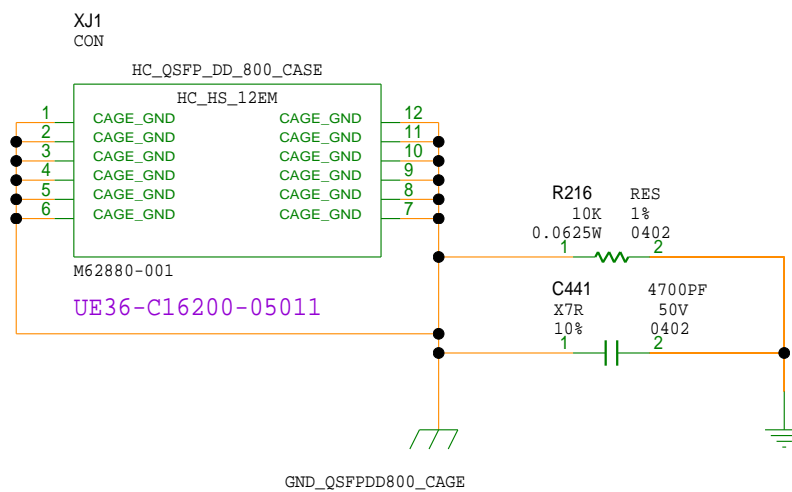
B



CAD NOTE:

PLACE CLOSE TO QSFPDD800 CONNECTOR

1x1 Cage

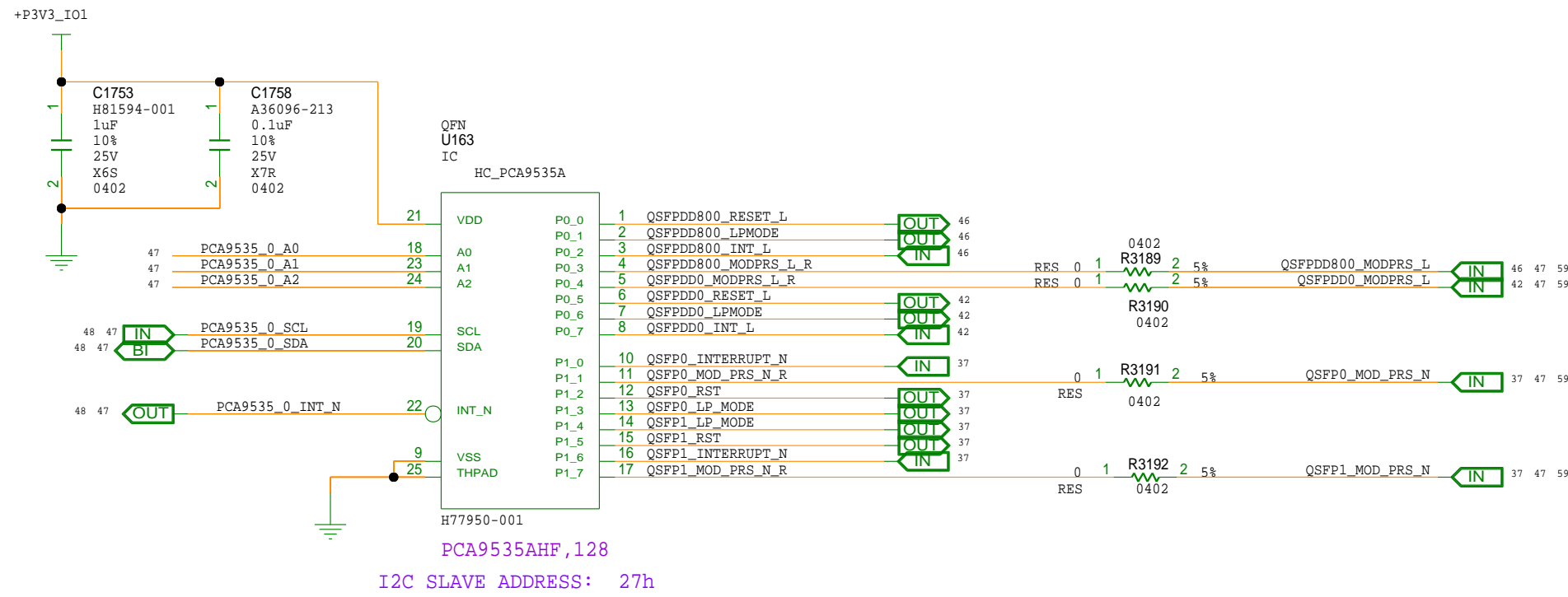


A

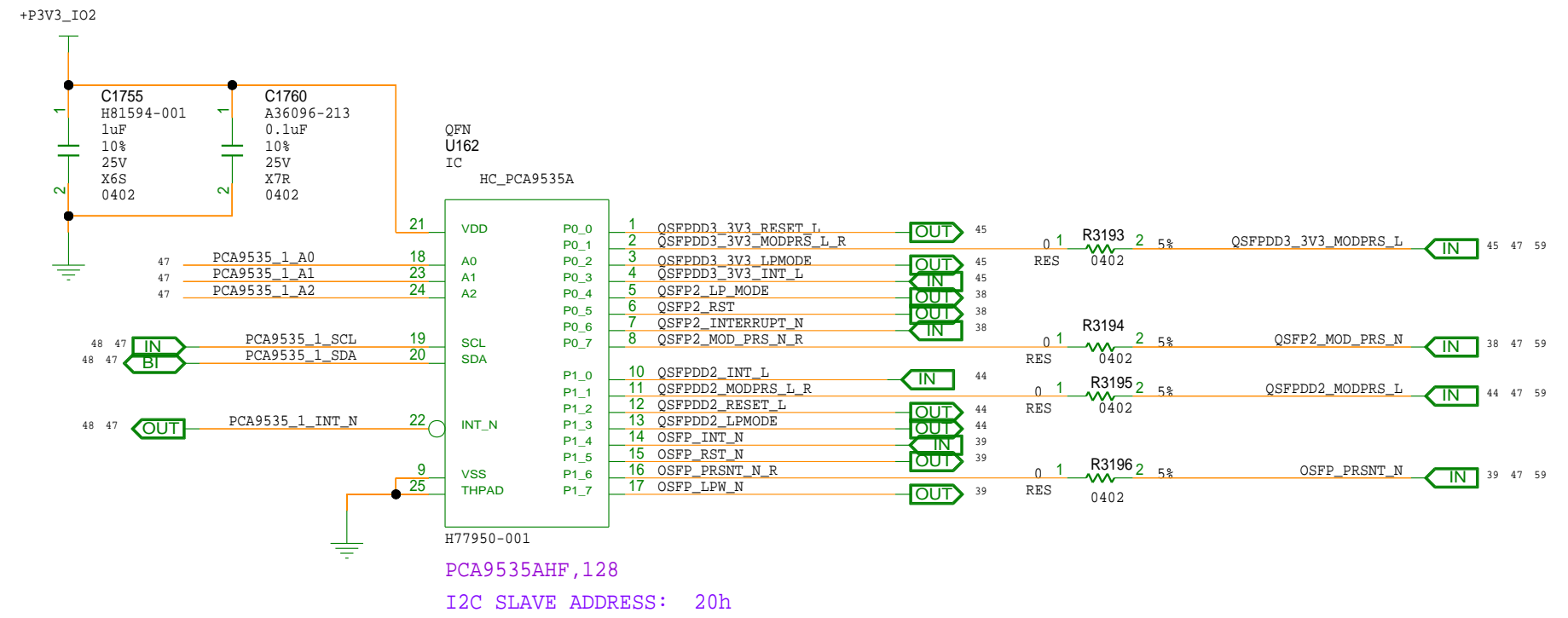
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Wed Mar 6 15:45:35 2024

IO EXPANDER -0



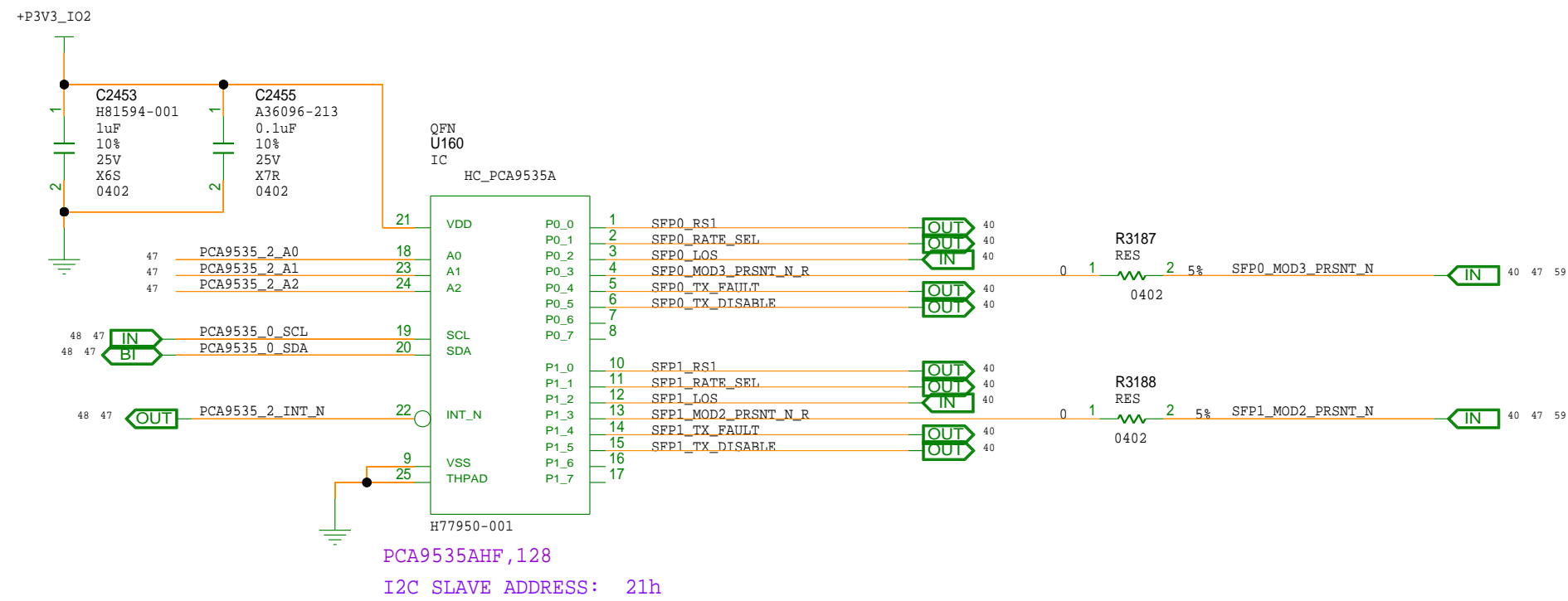
IO EXPANDER -1



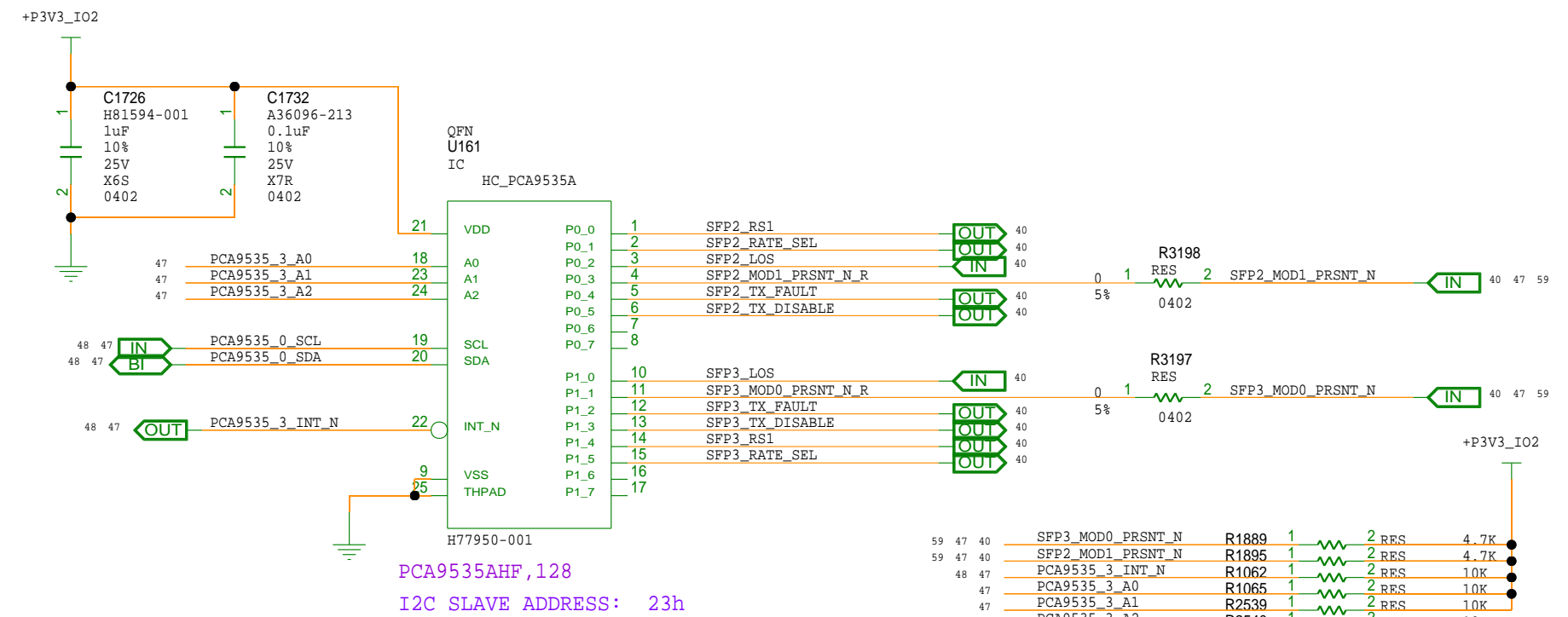
IO EXPANDER CONNECTION AND PLACEMENT DETAILS

CONNECTOR	IO EXPANDER	ADDRESS	I2C BUS	LAYOUT PLACEMENT
QSFDD800	IO EXPANDER 0	0X27H	PCA9535_0	LEFT
QSFP0	IO EXPANDER 0	0X27H	PCA9535_0	LEFT
QSFP1	IO EXPANDER 0	0X27H	PCA9535_0	LEFT
QSFDD0	IO EXPANDER 0	0X27H	PCA9535_0	LEFT
QSFDD3	IO EXPANDER 1	0X20H	PCA9535_1	RIGHT
QSFP2	IO EXPANDER 1	0X20H	PCA9535_1	RIGHT
QSFDD2	IO EXPANDER 1	0X20H	PCA9535_1	RIGHT
QSFP	IO EXPANDER 1	0X20H	PCA9535_1	RIGHT
SFP0	IO EXPANDER 2	0X21H	PCA9535_0	LEFT
SFP1	IO EXPANDER 2	0X21H	PCA9535_0	LEFT
SFP2	IO EXPANDER 3	0X23H	PCA9535_0	LEFT
SFP3	IO EXPANDER 3	0X23H	PCA9535_0	LEFT

IO EXPANDER -2



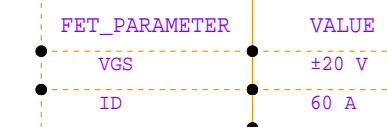
IO EXPANDER-3



Wed Mar 6 15:45:36 2024



SHEET 48 OF 105



49 OF 105

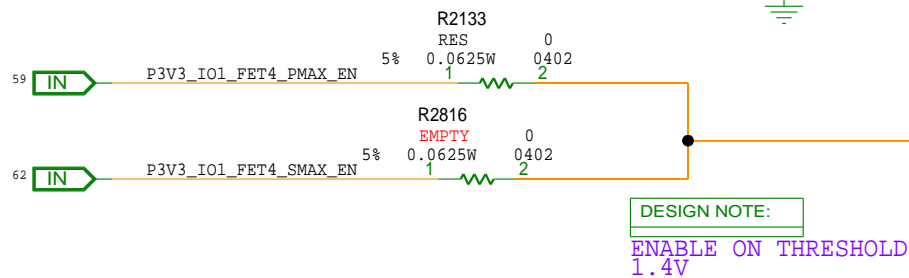
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3

2

1

PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	
LOAD CURRENT	5.6A
FREQUENCY	
RIPPLE _VOLTAGE	



DESIGN NOTE:
Rsense: 7mohm
Itrip(min) : 5.65A
Itrip(Nom) : 7.1A
Pdiss : 360mW

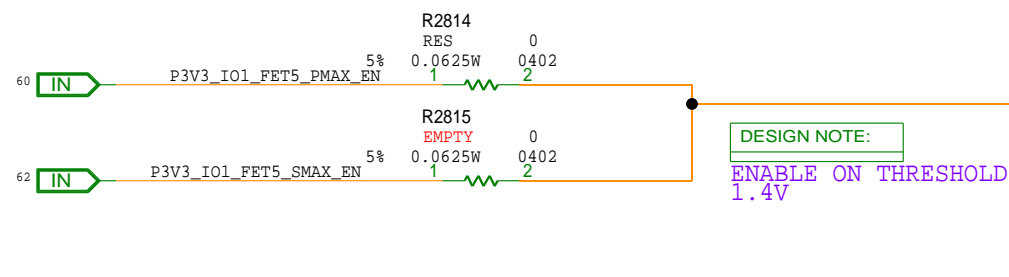
CAD NOTE: PLACE THE SENSE RES NEAR TO LOAD ROUTE AS KELVIN SENSE

CONN POWER LOAD SWITCHES-2

CAD NOTE: PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB. AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

FET_PARAMETER	VALUE
VGS	+20 V
ID	60 A

PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	
LOAD CURRENT	5.6A
FREQUENCY	
RIPPLE _VOLTAGE	



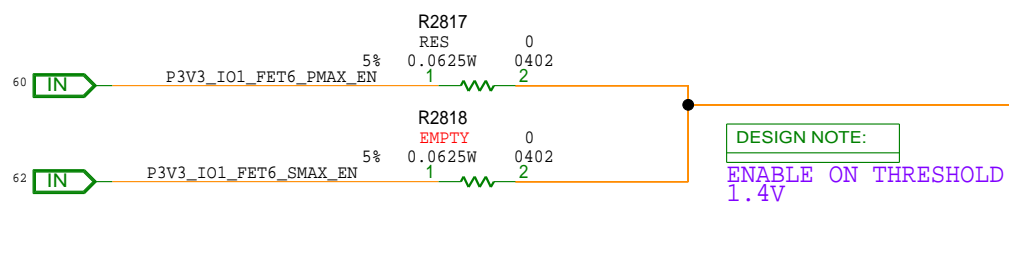
DESIGN NOTE:
Rsense: 7mohm
Itrip(min) : 5.65A
Itrip(Nom) : 7.1A
Pdiss : 360mW

CAD NOTE: PLACE THE SENSE RES NEAR TO LOAD ROUTE AS KELVIN SENSE

CAD NOTE: PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB. AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

FET_PARAMETER	VALUE
VGS	+20 V
ID	60 A

PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	
LOAD CURRENT	5.6A
FREQUENCY	
RIPPLE _VOLTAGE	



DESIGN NOTE:
Rsense: 7mohm
Itrip(min) : 5.65A
Itrip(Nom) : 7.1A
Pdiss : 360mW

CAD NOTE: PLACE THE SENSE RES NEAR TO LOAD ROUTE AS KELVIN SENSE

CAD NOTE: PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB. AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

FET_PARAMETER	VALUE
VGS	+20 V
ID	60 A

Wed Mar 6 15:45:38 2024

4

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1

4

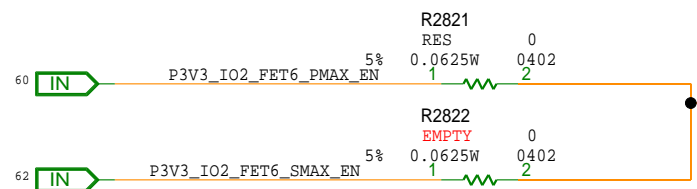
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2

1

CONN POWER LOAD SWITCHES-3

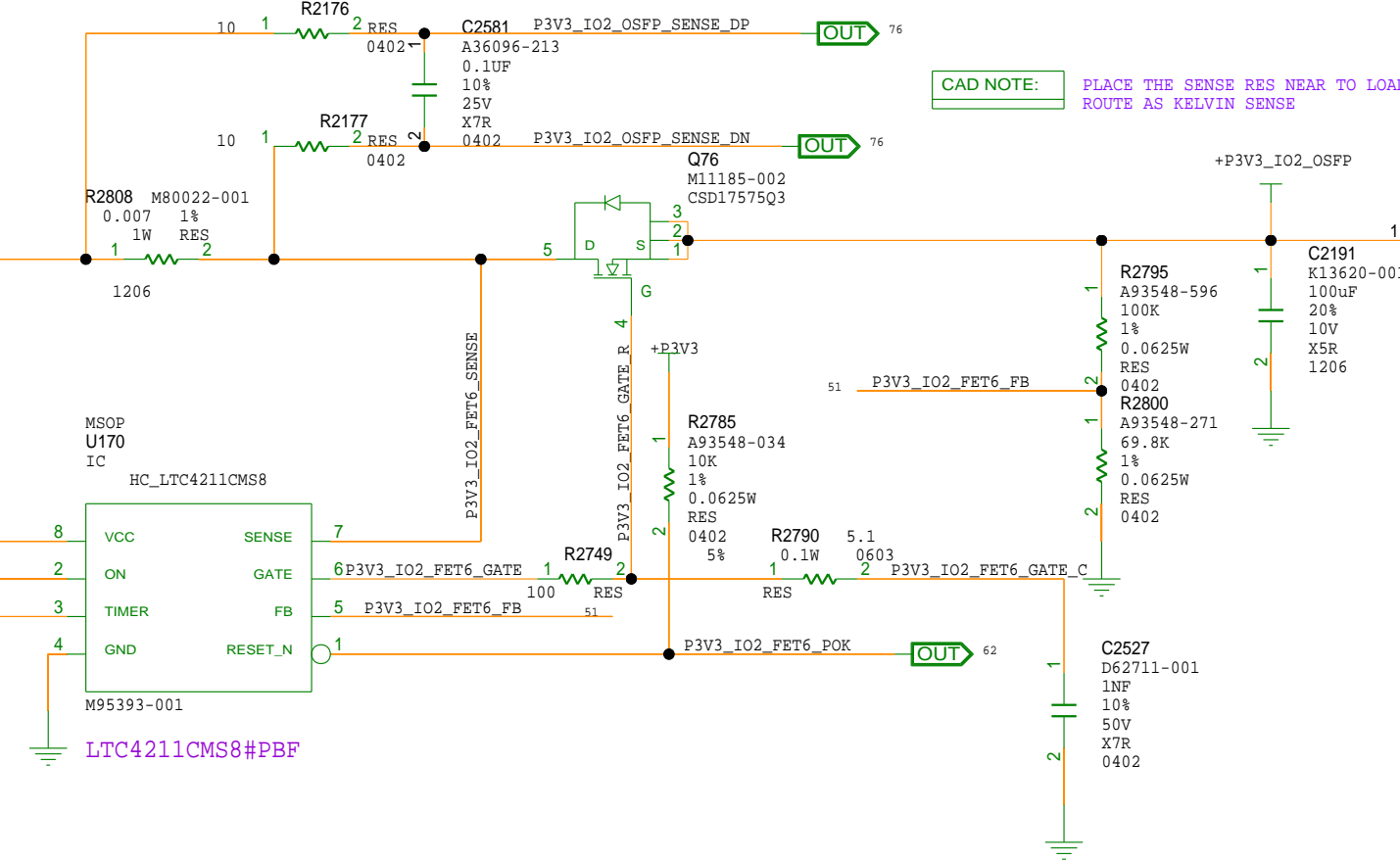
PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	
LOAD CURRENT	5.6A
FREQUENCY	
RIPPLE_VOLTAGE	



DESIGN NOTE:
R_{sense}: 7mohm
I_{trip}(min) : 5.65A
I_{trip}(Nom) : 7.1A
P_{diss} : 360mW

ENABLE ON THRESHOLD
1.4V

DESIGN NOTE:
R_{sense}: 7mohm
I_{trip}(min) : 5.65A
I_{trip}(Nom) : 7.1A
P_{diss} : 360mW

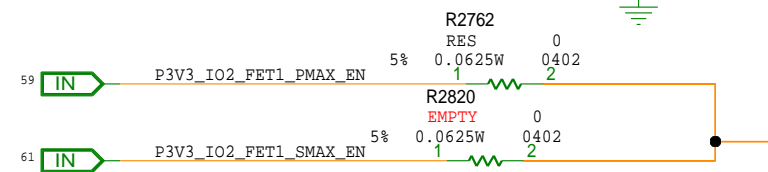


CAD NOTE: PLACE THE SENSE RES NEAR TO LOAD
ROUTE AS KELVIN SENSE

CAD NOTE: PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

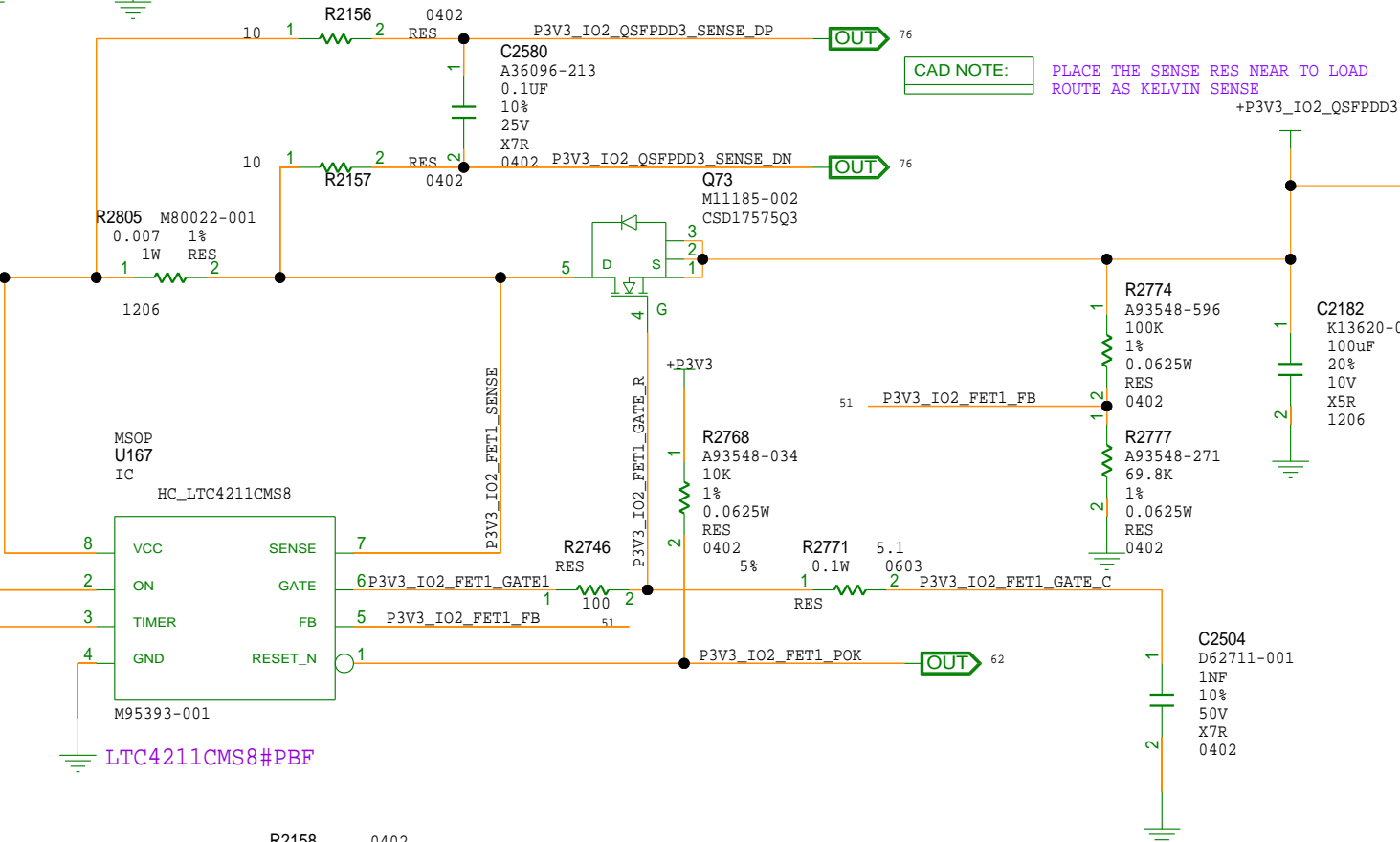
FET_PARAMETER	VALUE
VGS	±20 V
ID	60 A

PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	
LOAD CURRENT	5.6A
FREQUENCY	
RIPPLE_VOLTAGE	



DESIGN NOTE:
R_{sense}: 7mohm
I_{trip}(min) : 5.65A
I_{trip}(Nom) : 7.1A
P_{diss} : 360mW

ENABLE ON THRESHOLD
1.4V

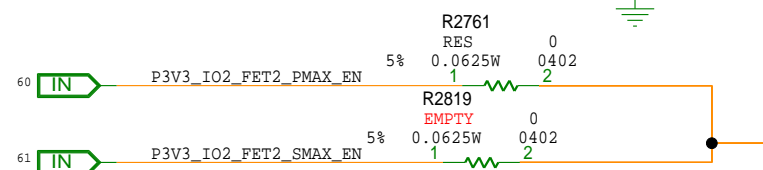


CAD NOTE: PLACE THE SENSE RES NEAR TO LOAD
ROUTE AS KELVIN SENSE

CAD NOTE: PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

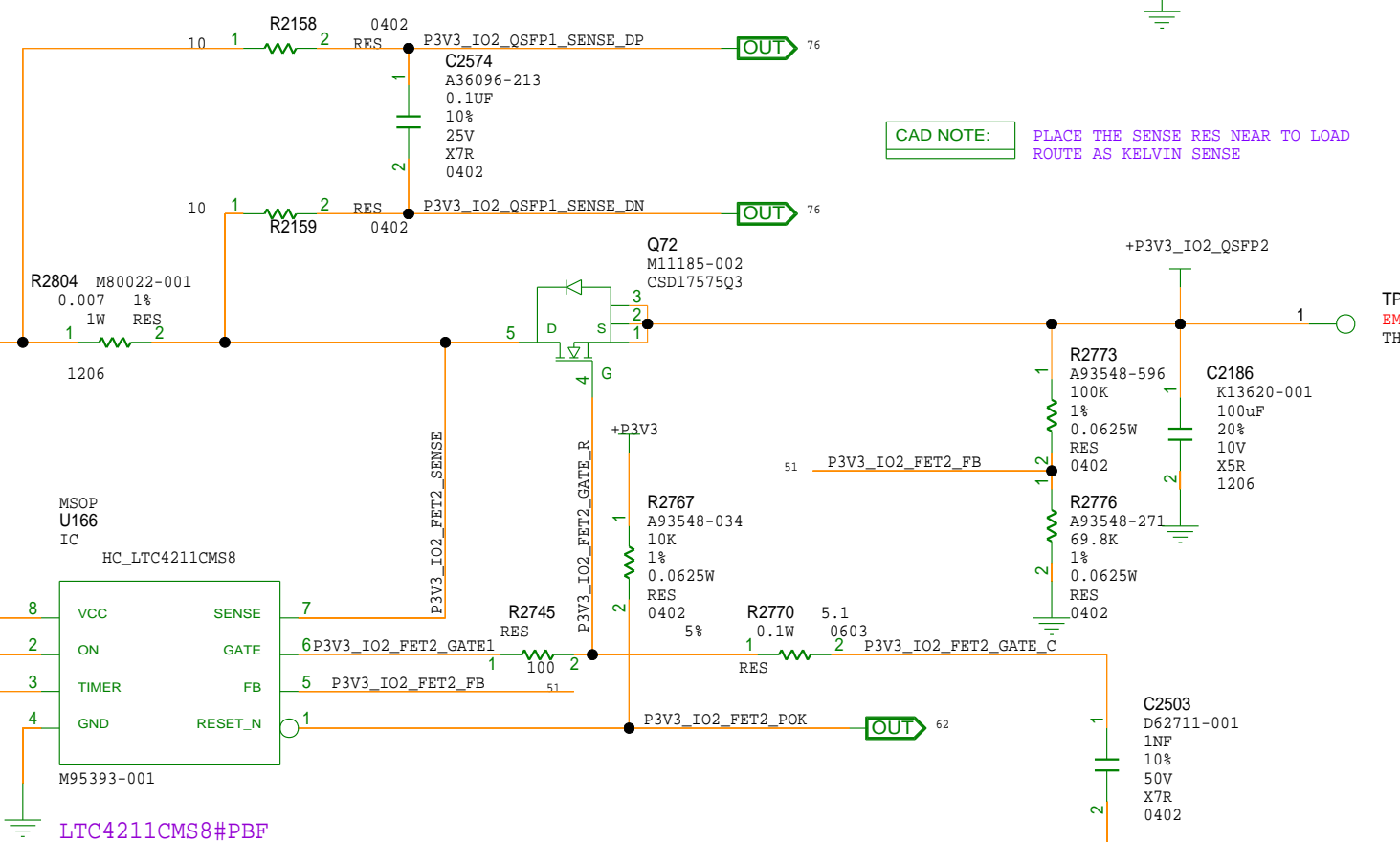
FET_PARAMETER	VALUE
VGS	±20 V
ID	60 A

PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	
LOAD CURRENT	5.6A
FREQUENCY	
RIPPLE_VOLTAGE	



DESIGN NOTE:
R_{sense}: 7mohm
I_{trip}(min) : 5.65A
I_{trip}(Nom) : 7.1A
P_{diss} : 360mW

ENABLE ON THRESHOLD
1.4V



CAD NOTE: PLACE THE SENSE RES NEAR TO LOAD
ROUTE AS KELVIN SENSE

CAD NOTE: PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

FET_PARAMETER	VALUE
VGS	±20 V
ID	60 A

Wed Mar 6 15:45:38 2024

4

3

2

1

DEPARTMENT

UNKNOWN

Intel Corporation

2200 Mission College Blvd.
P.O. BOX 58119
Santa Clara, CA 95052-8119

SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-A2

REV

2.0

SCALE:

DO NOT SCALE DRAWING

SHEET

51 OF 105

4

3

2

1

PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	
LOAD CURRENT	4A
FREQUENCY	
RIPPLE _VOLTAGE	

DESIGN NOTE:

Rsense: 7mohm
Itrip(min) : 5.65A
Itrip(Nom) : 7.1A
Pdiss : 360mW

DESIGN NOTE:

ENABLE ON THRESHOLD
1.4V

PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	
LOAD CURRENT	5.6A
FREQUENCY	
RIPPLE _VOLTAGE	

DESIGN NOTE:

Rsense: 7mohm
Itrip(min) : 5.65A
Itrip(Nom) : 7.1A
Pdiss : 360mW

DESIGN NOTE:

ENABLE ON THRESHOLD
1.4V

PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	
LOAD CURRENT	4A
FREQUENCY	
RIPPLE _VOLTAGE	

DESIGN NOTE:

Rsense: 7mohm
Itrip(min) : 5.65A
Itrip(Nom) : 7.1A
Pdiss : 360mW

DESIGN NOTE:

ENABLE ON THRESHOLD
1.4V

CAD NOTE:

PLACE THE SENSE RES NEAR TO LOAD
ROUTE AS KELVIN SENSE

CAD NOTE:

PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

CONN POWER LOAD SWITCHES-4

FET_PARAMETER	VALUE
VGS	+20 V
ID	60 A

CAD NOTE:

PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

FET_PARAMETER	VALUE
VGS	+20 V
ID	60 A

CAD NOTE:

PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

FET_PARAMETER	VALUE
VGS	+20 V
ID	60 A

Wed Mar 6 15:45:39 2024

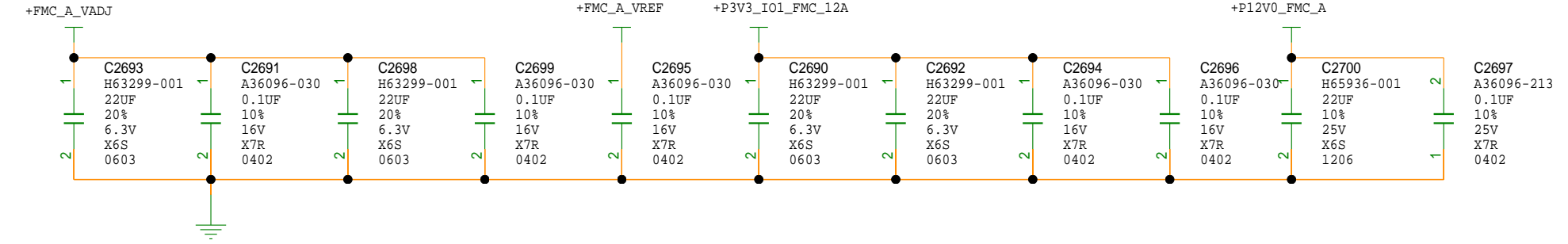
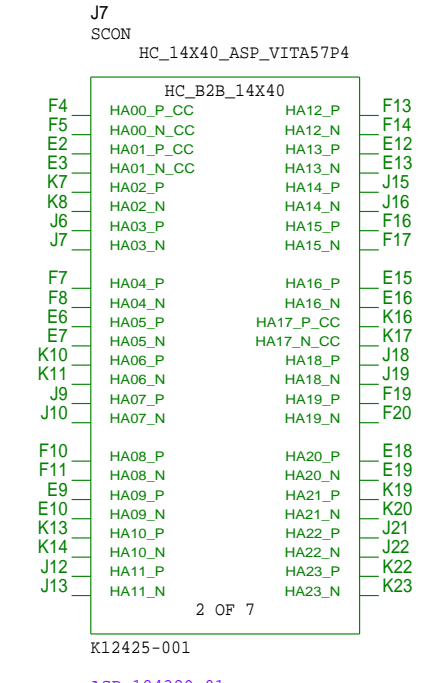
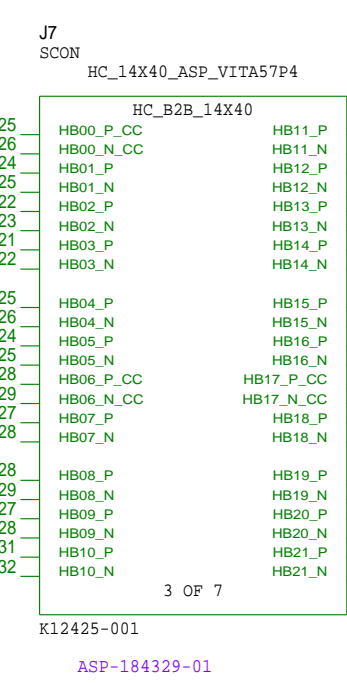
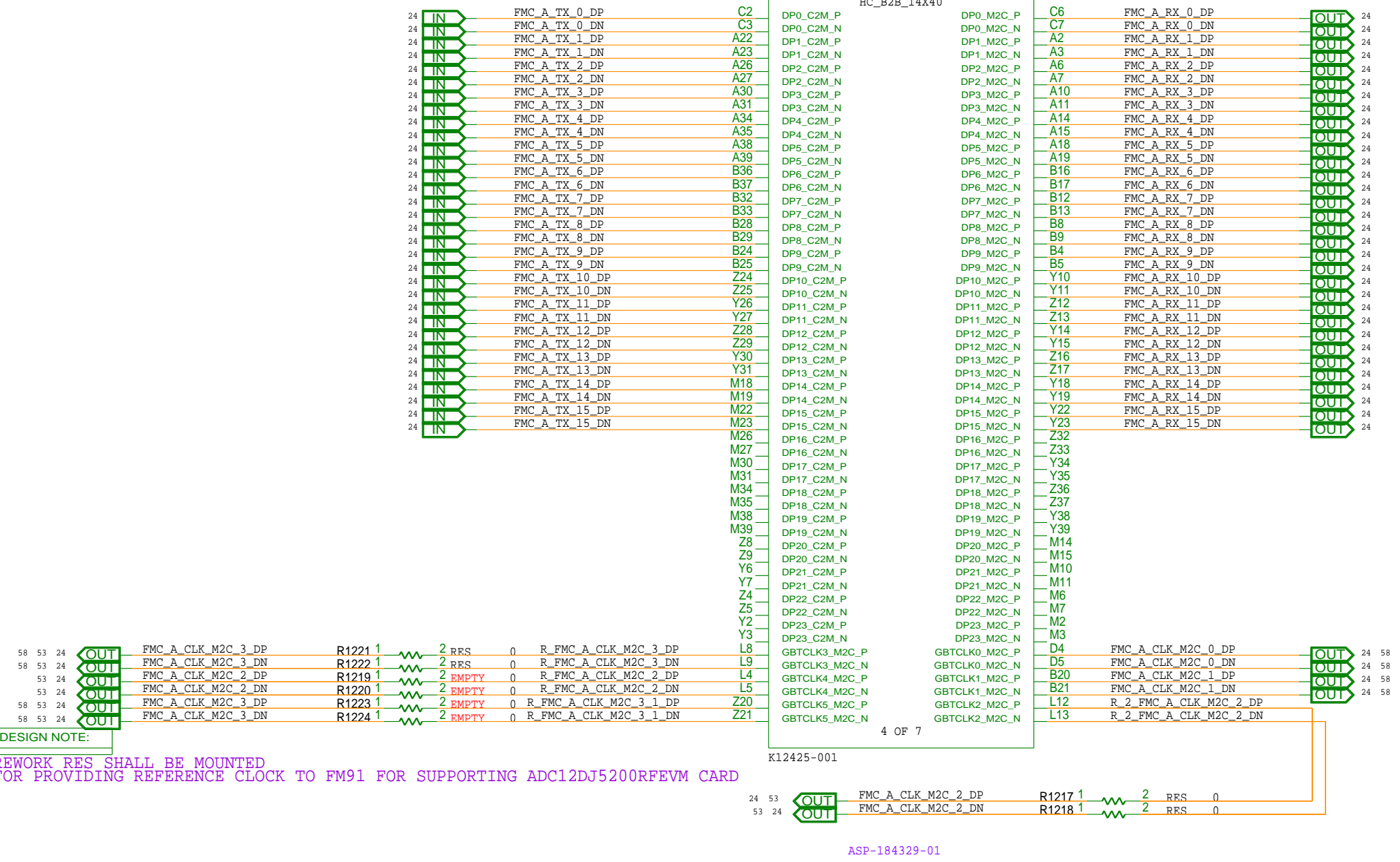
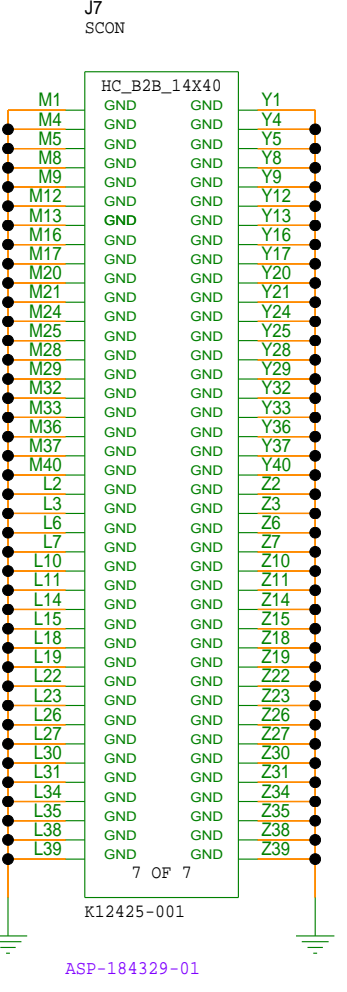
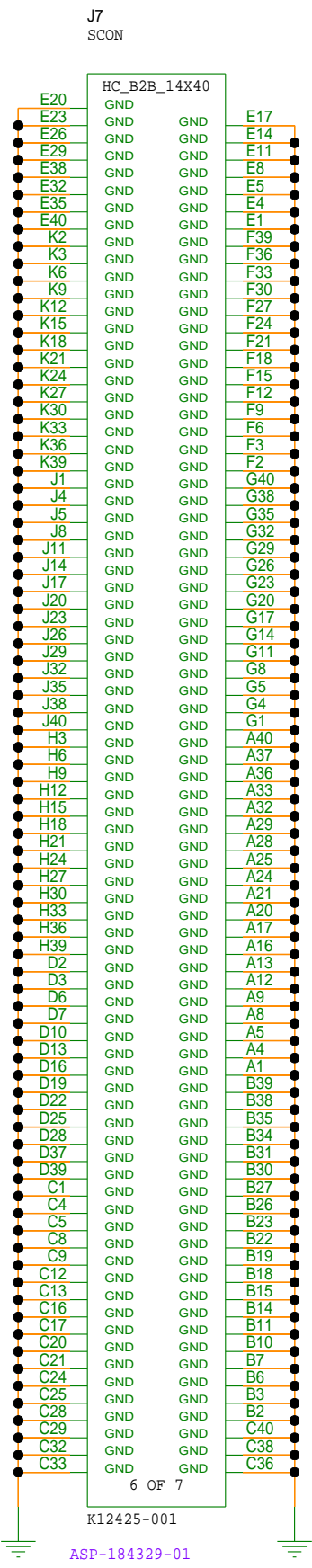
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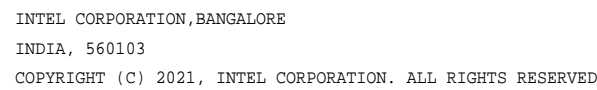
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FMC+ CONNECTOR A (NORTH)



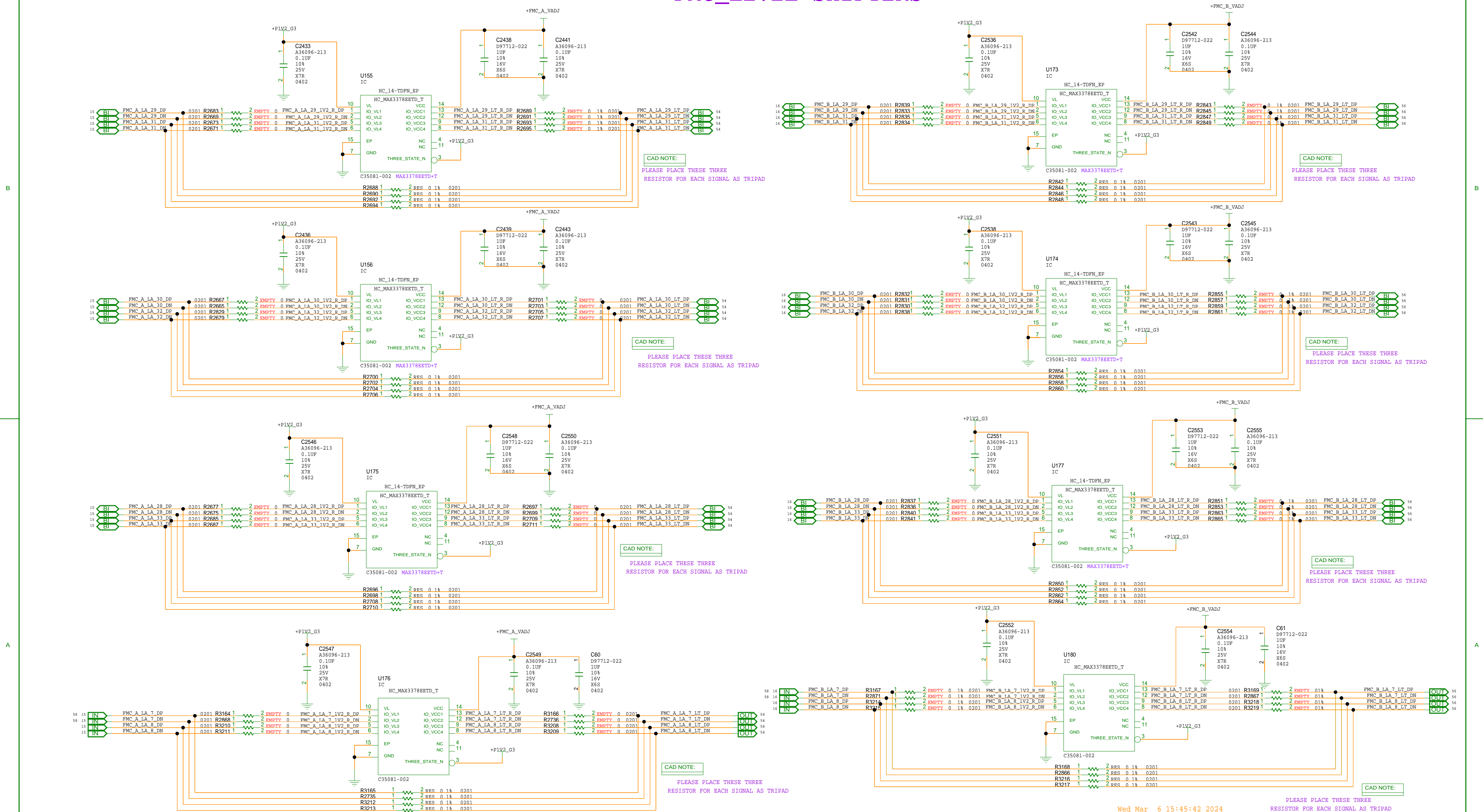
Wed Mar 6 15:45:40 2024

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
P&G	INTEL CORPORATION,BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING			SHEET 53 OF 105



SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330690-A2	REV 2.0
SCALE:		DO NOT SCALE DRAWING	SHEET 54 OF 105

FMC_LEVEL SHIFTERS



Wed Mar 6 15:45:42 2024

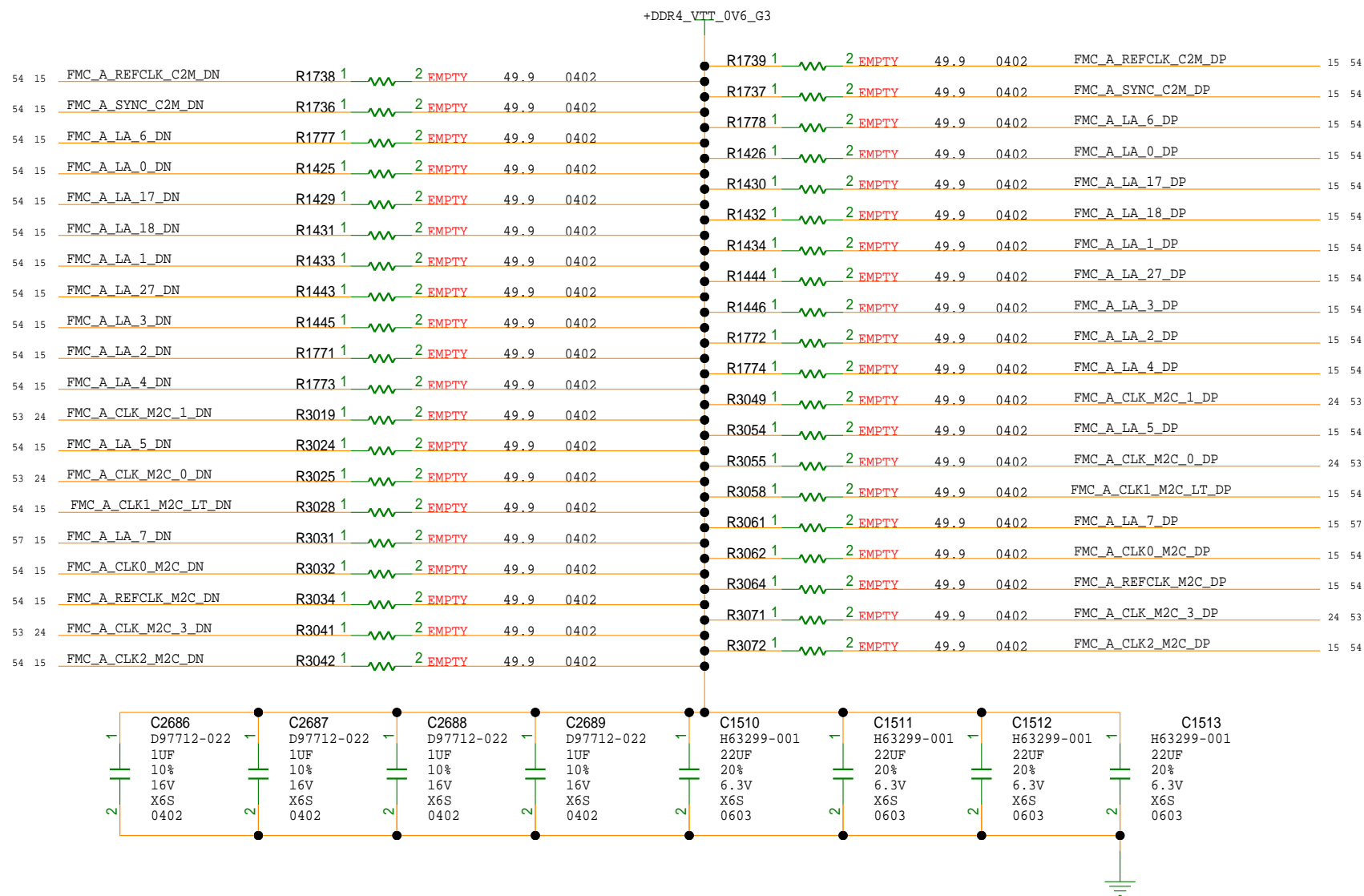
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FMC_TERMINATIONS



Wed Mar 6 15:45:42 2024

4

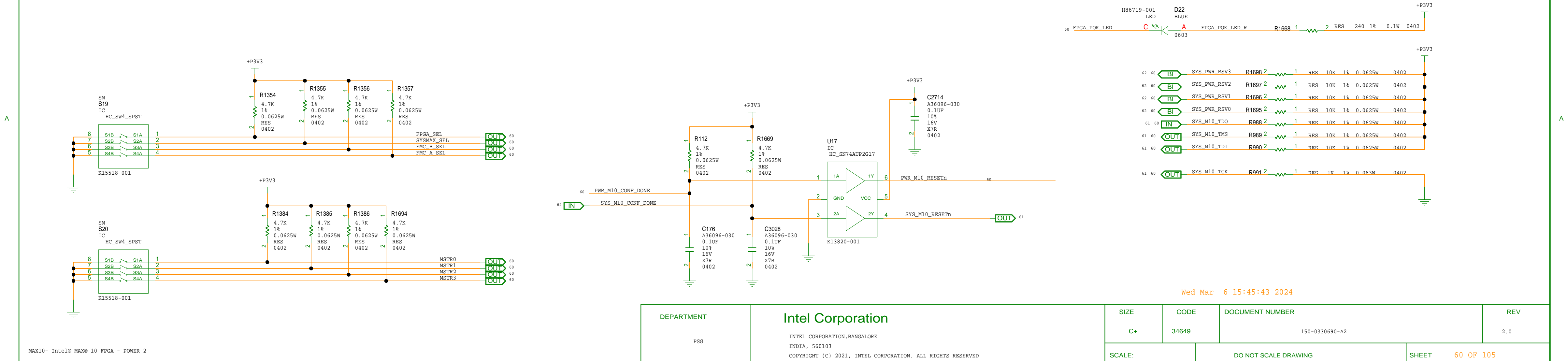
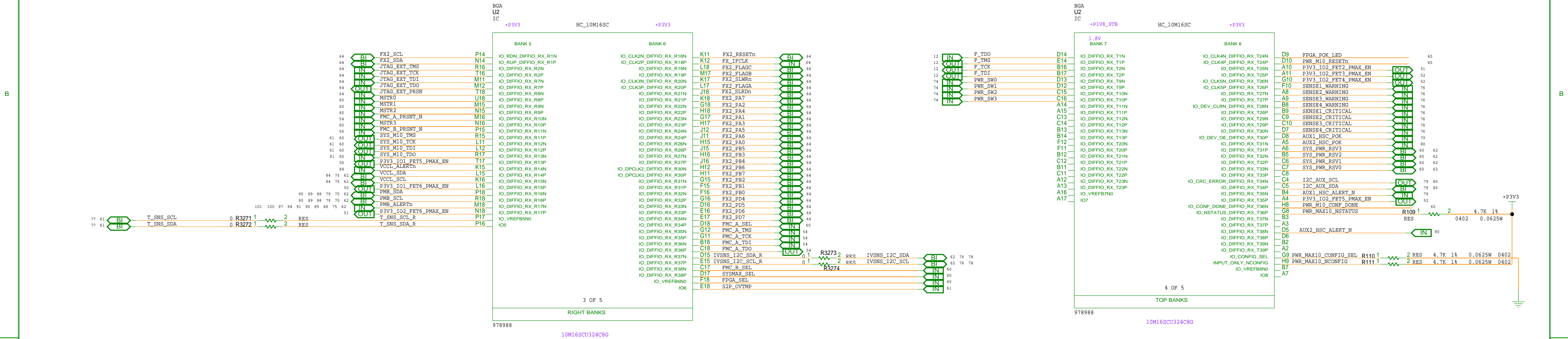
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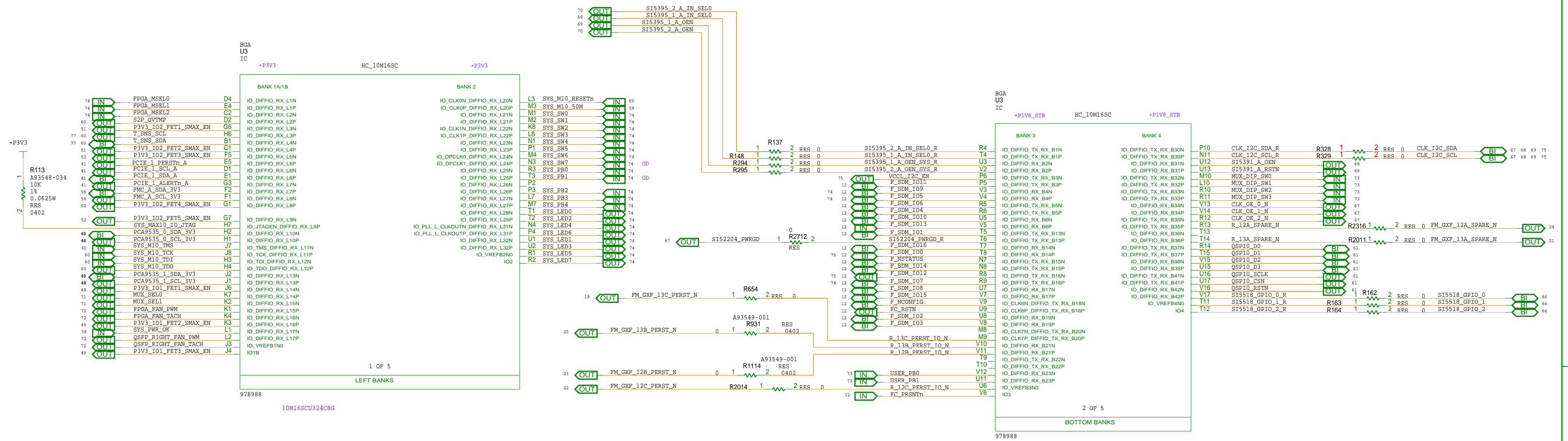
MAX10- Intel® MAX® 10 FPGA

PWR MAX-10- II

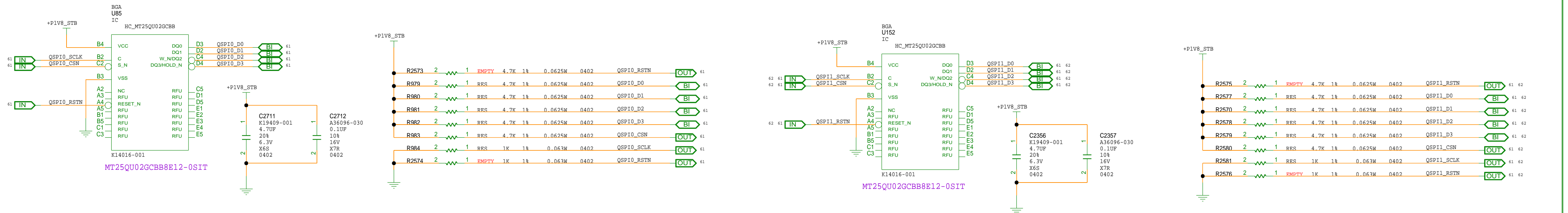


Wed Mar 6 15:45:43 2024

MAX10- Intel® MAX® 10 FPGA
SYS MAX-10- I



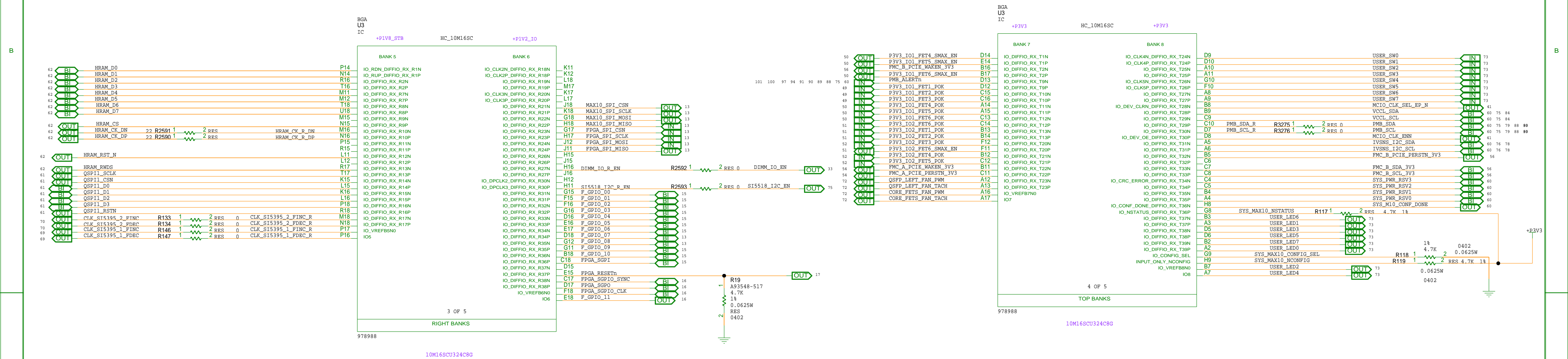
QSPI



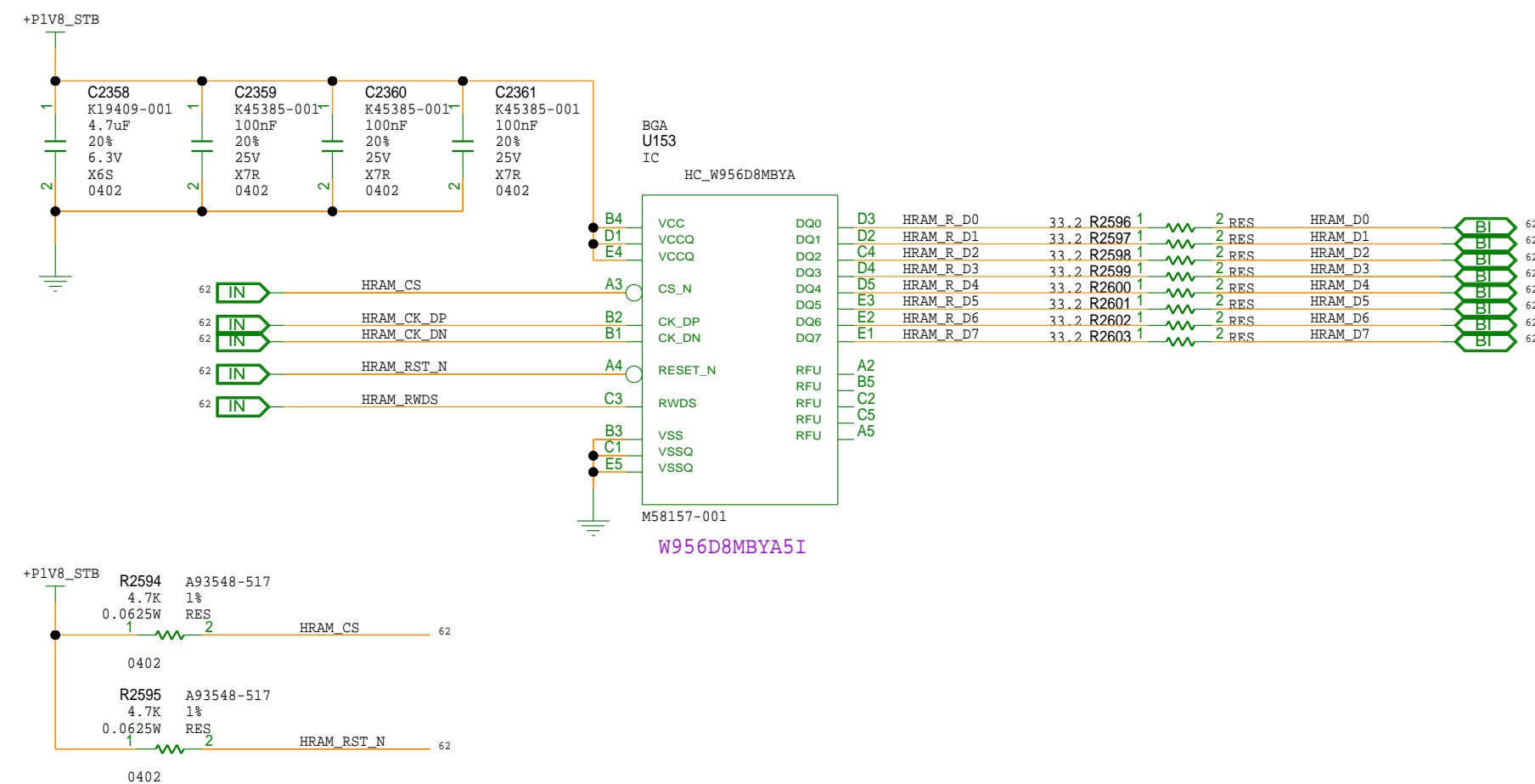
Wed Mar 6 15:45:44 2024

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
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		SCALE:	DO NOT SCALE DRAWING		SHEET 61 OF 105

SYS MAX-10- II



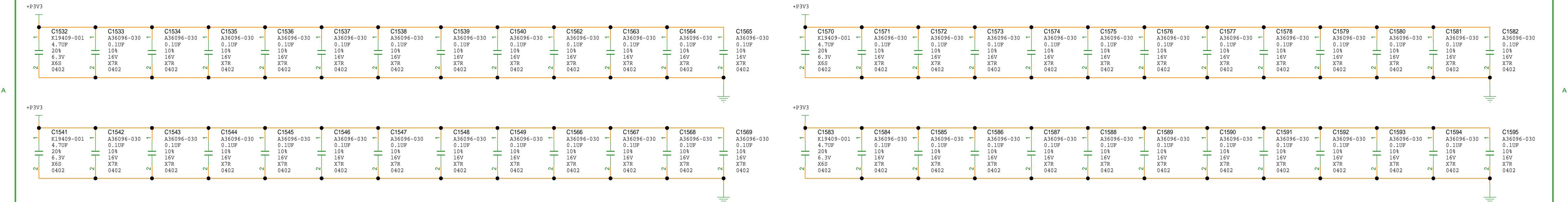
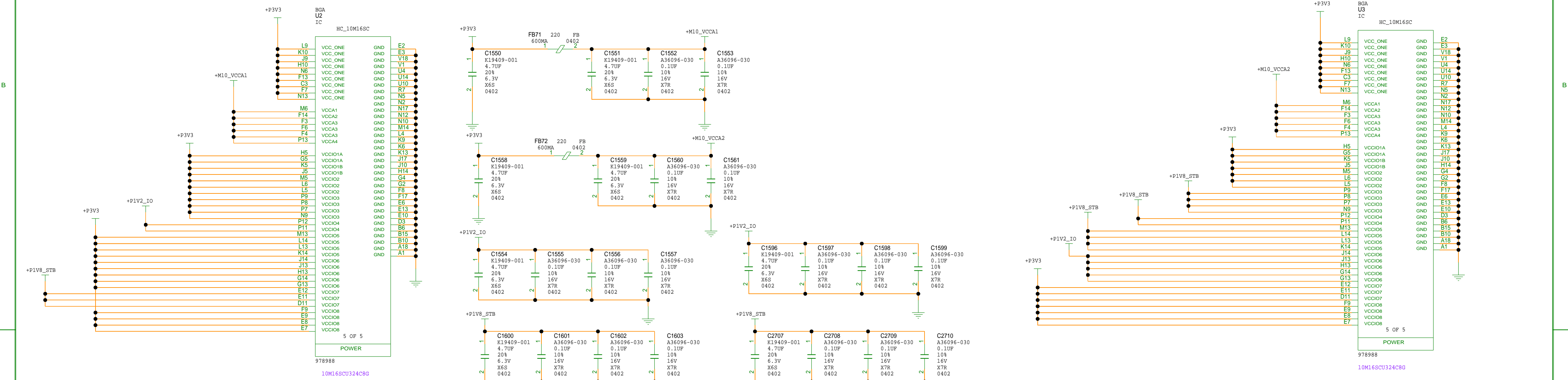
HYPER_RAM



Wed Mar 6 15:45:44 2024

MAX10- Intel® MAX® 10 FPGA

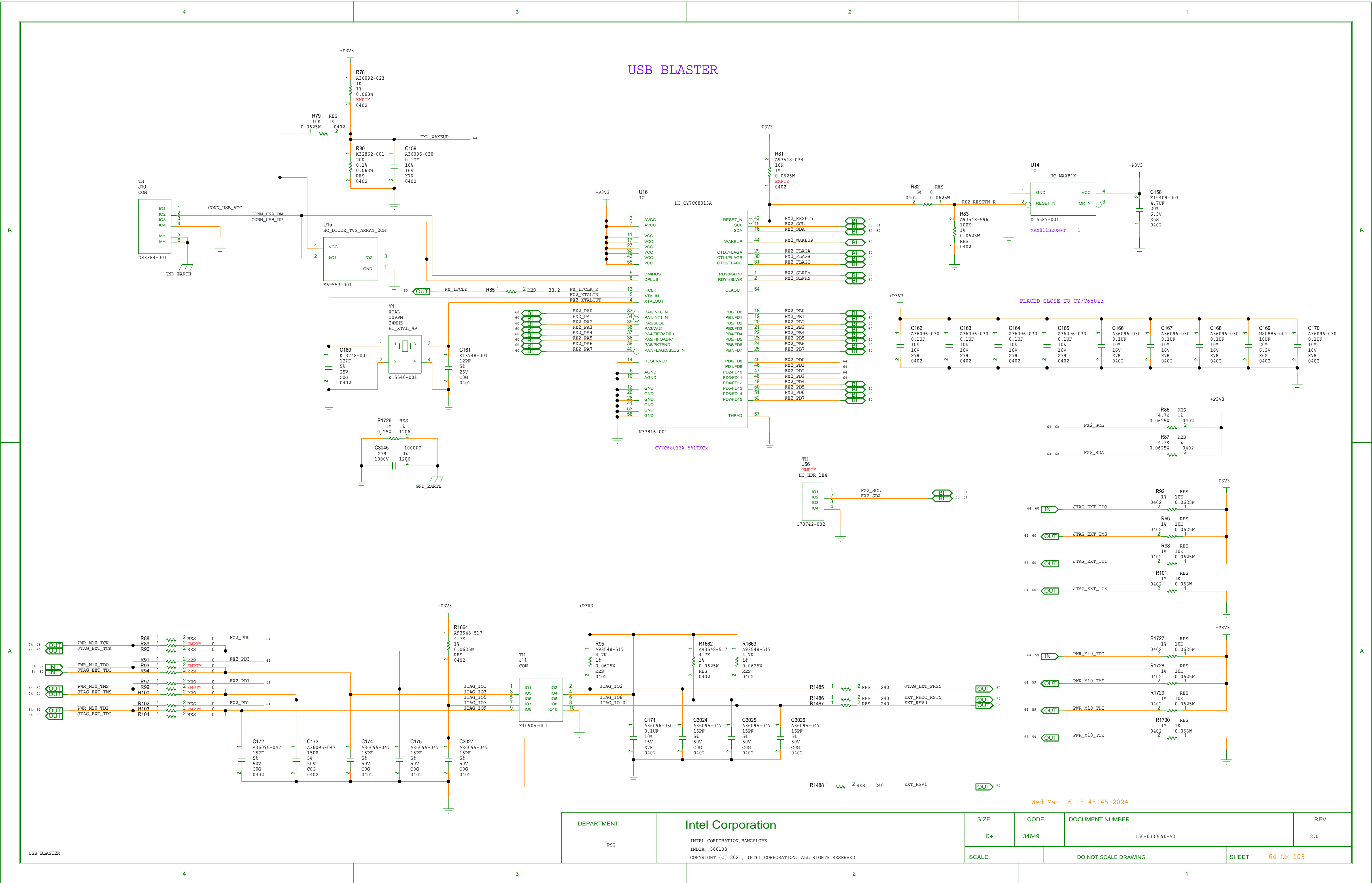
MAX-10 POWER



Wed Mar 6 15:45:45 2024

MAX10- Intel® MAX® 10 FPGA POWER	DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
	PSG	INTEL CORPORATION,BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
			SCALE:	DO NOT SCALE DRAWING		SHEET 63 OF 105

USB BLASTER



Wed Mar 6 15:45:45 2024

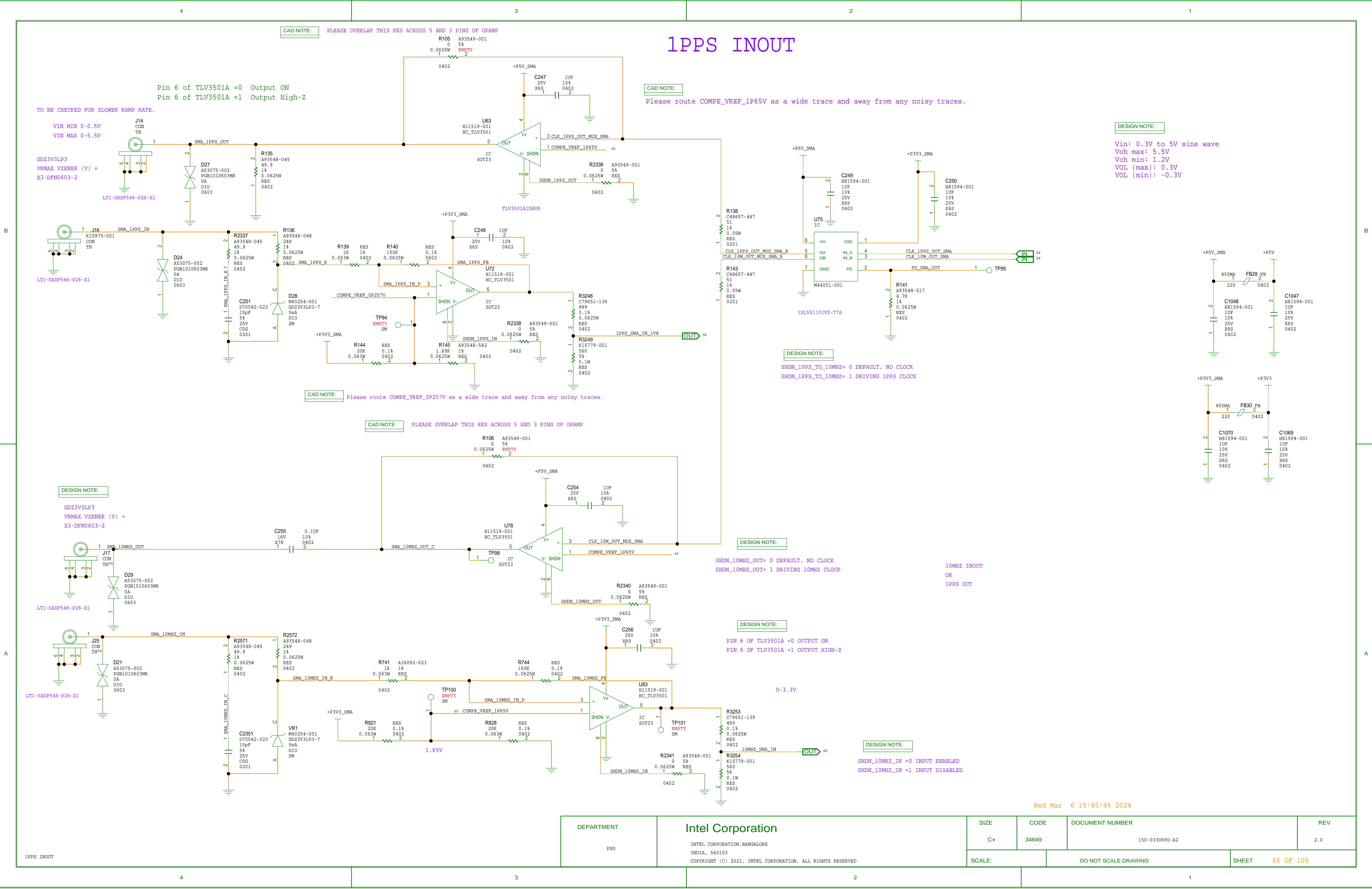
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	INTEL CORPORATION,BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING			SHEET 64 OF 105

4

3

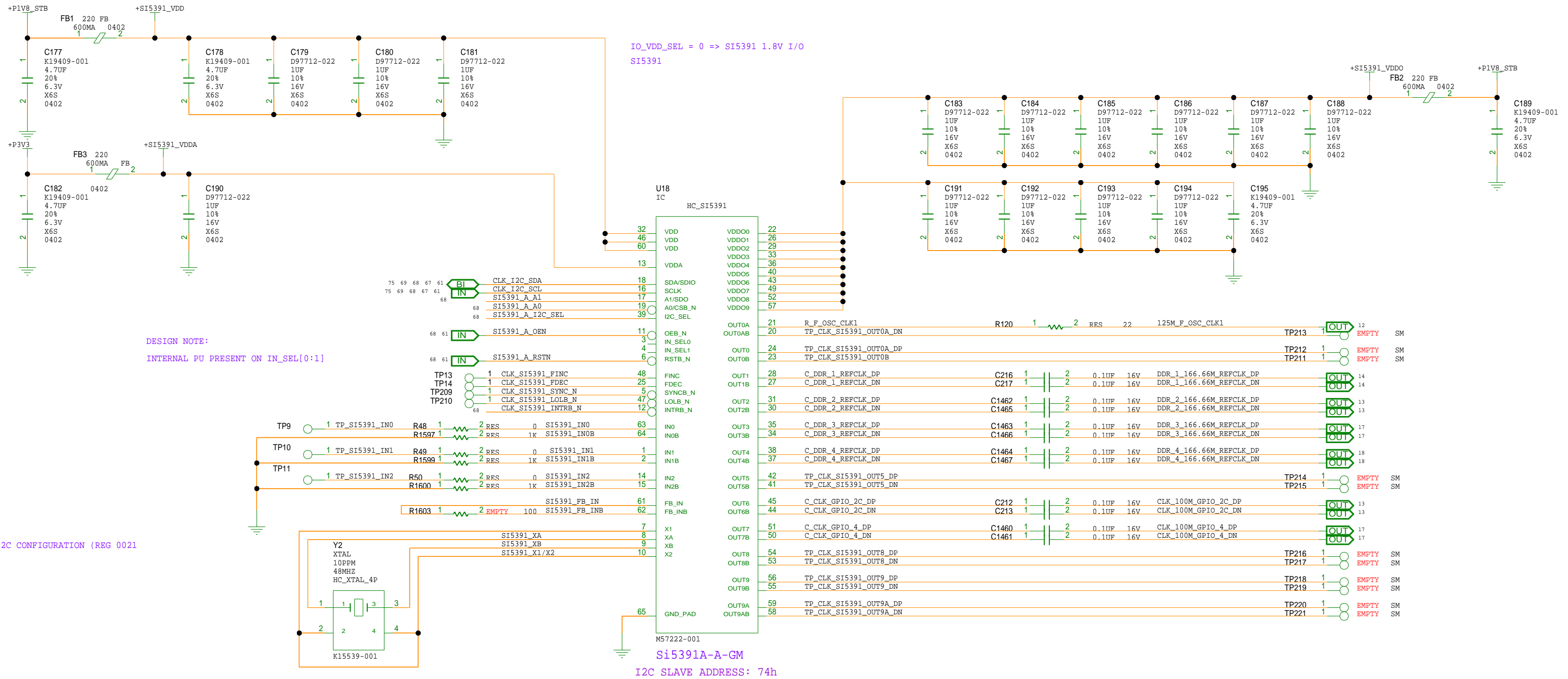
2

1





SI5391 CLOCK GENERATOR



DESIGN NOTE:
INTERNAL PU PRESENT ON IN_SEL[0:1]

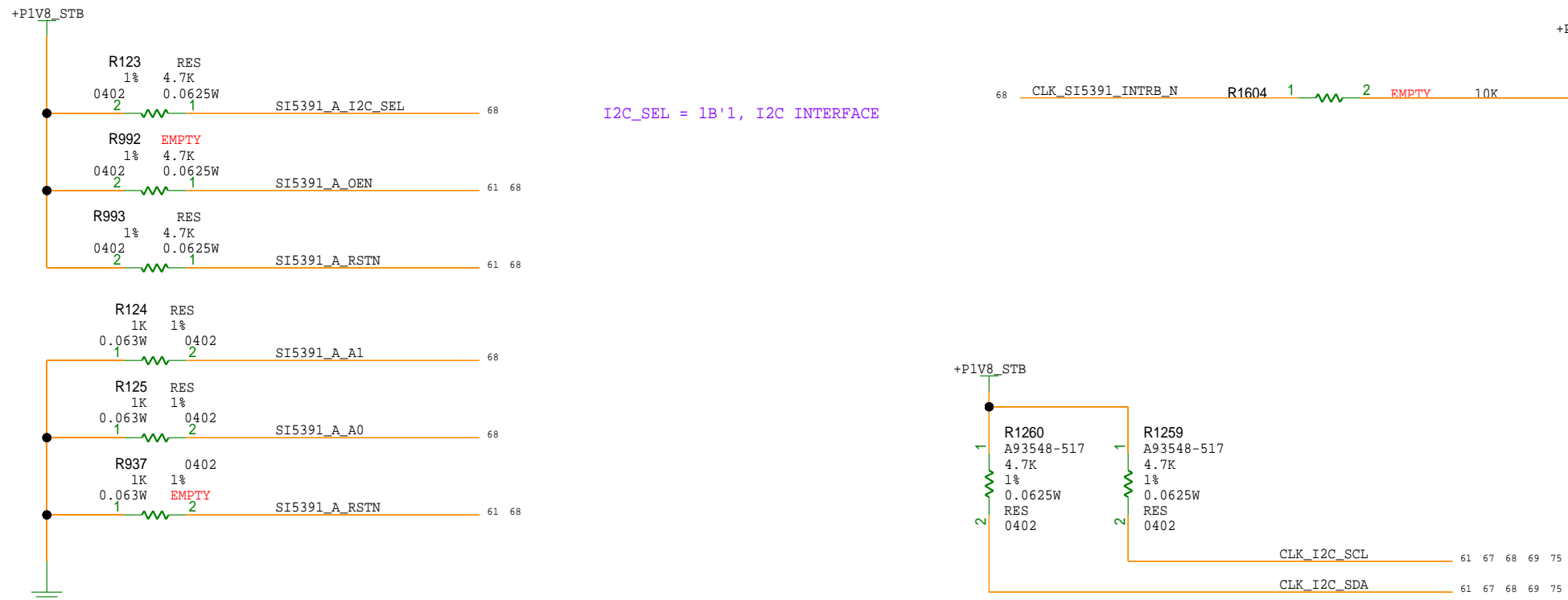
DESIGN NOTE:

INPUT CAN BE SET AS IN0/IN1 THROUGH I2C CONFIGURATION (REG 0021)

INPUT_SOURCE_SELECT		
IN_SEL0	IN_SEL1	DESCRIPTION
0	0	IN0 (NC)
0	1	IN1 (NC)
1	0	IN2 (NC)
1	1	XA/XB (DEFAULT)

PULL-UP/DOWN RESISTORS

```
I2C_SEL = 1B'1, I2C INTERFACE
```



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P&G		C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 68 OF 105

SI5395 CLOCK GENERATOR-1

INPUT SOURCE SELECT

IN_SEL0	IN_SEL1	DESCRIPTION
0	0	IN0 (SI5518 OUTPUT/DEFAULT)
0	1	IN1 (EXTERNAL INPUT)
1	0	IN2 (NC)
1	1	IN3 (LOOPBACK INPUT)

CAD NOTE:

PLACE TERMINATING RES NEAR TO CLOCK

DESIGN NOTE:

IN DESIGN TO CHANGE THE CLOCK AS PER THE INTERFACE NEED THROUGH BTS GUI,
WHICH WILL BE SHARED AS PART OF DESIGN COLLATERALS TO CUSTOMERS

SI5395A-A-GM
I2C SLAVE ADDRESS: 68h

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PSG	INTEL CORPORATION,BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 69 OF 105	

SI5395 CLOCK GENERATOR-2

INPUT SOURCE SELECT

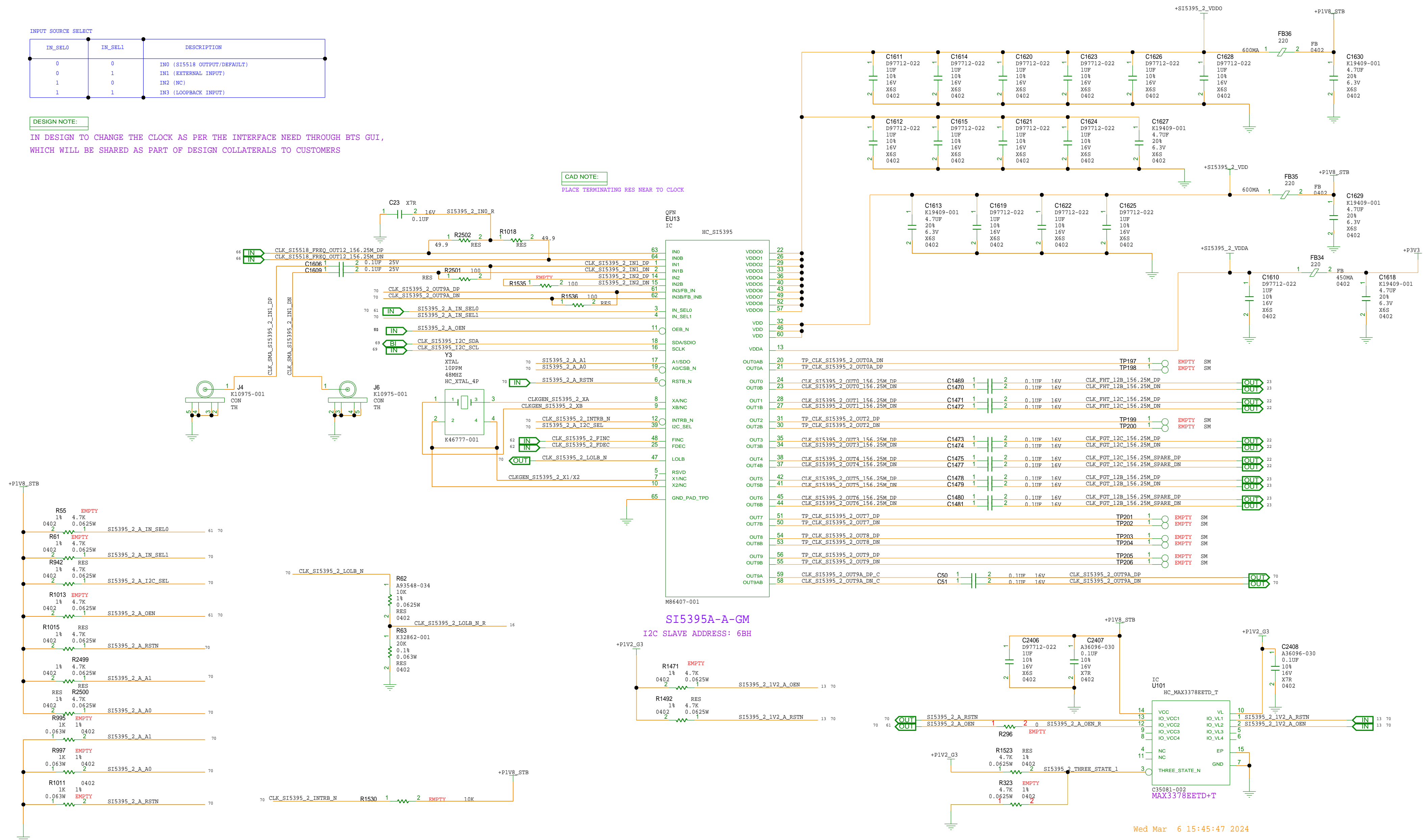
IN_SEL0	IN_SEL1	DESCRIPTION
0	0	IN0 (SI518 OUTPUT/DEFAULT)
0	1	IN1 (EXTERNAL INPUT)
1	0	IN2 (NC)
1	1	IN3 (LOOPBACK INPUT)

DESIGN NOTE:

IN DESIGN TO CHANGE THE CLOCK AS PER THE INTERFACE NEED THROUGH BTS GUI,
WHICH WILL BE SHARED AS PART OF DESIGN COLLATERALS TO CUSTOMERS

CAD NOTE:

PLACE TERMINATING RES NEAR TO CLOCK



Wed Mar 6 15:45:47 2024

DEPARTMENT UNKNOWN	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330690-A2	REV 2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 70 OF 105

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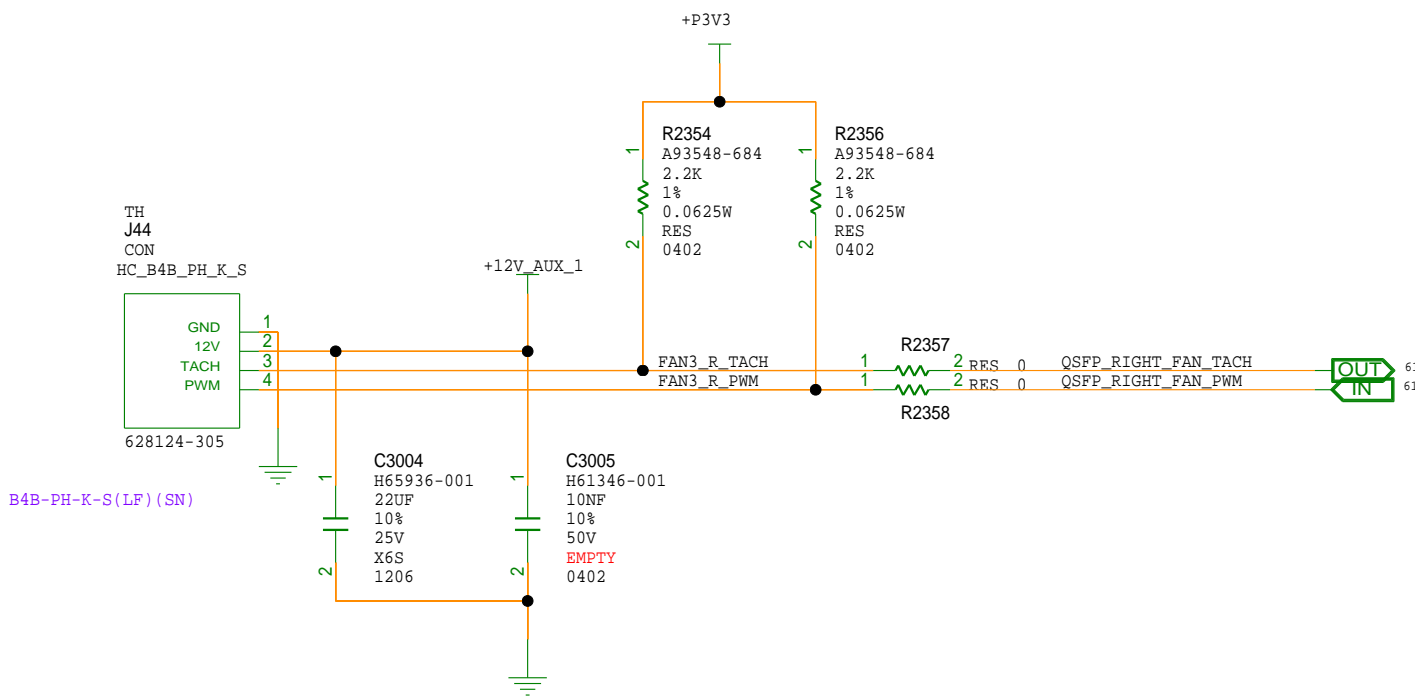
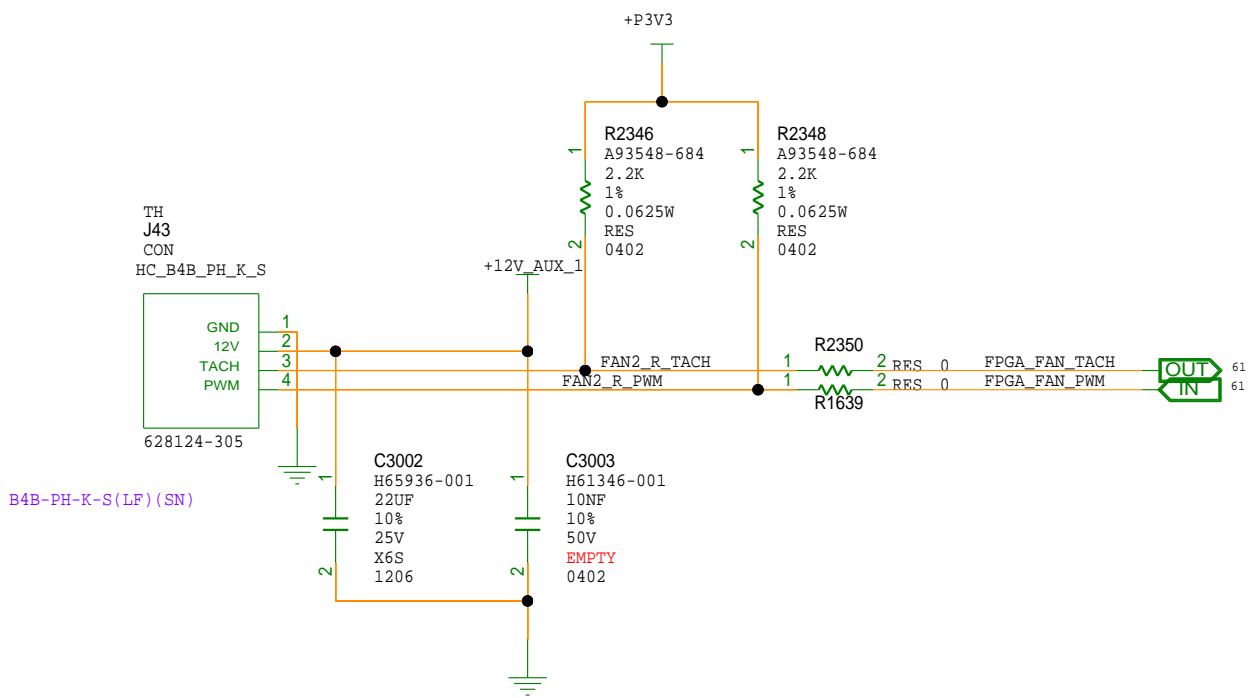
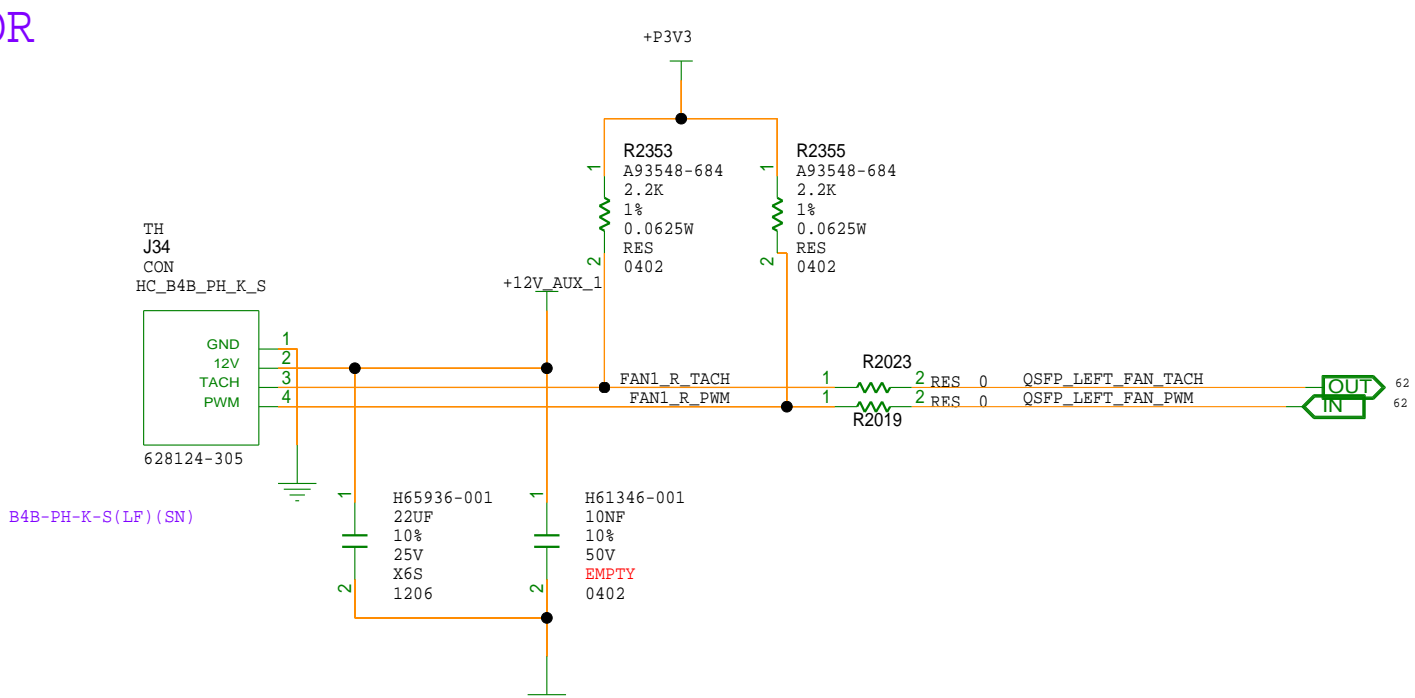
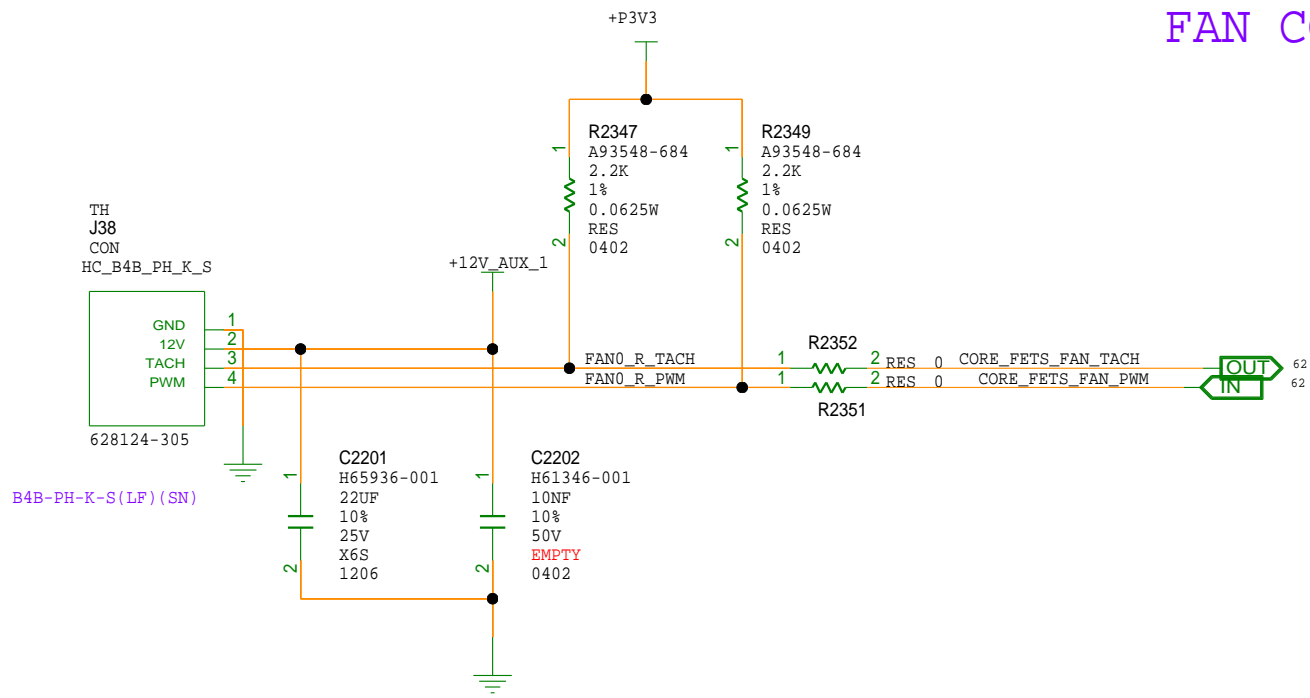
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FAN CONNECTOR



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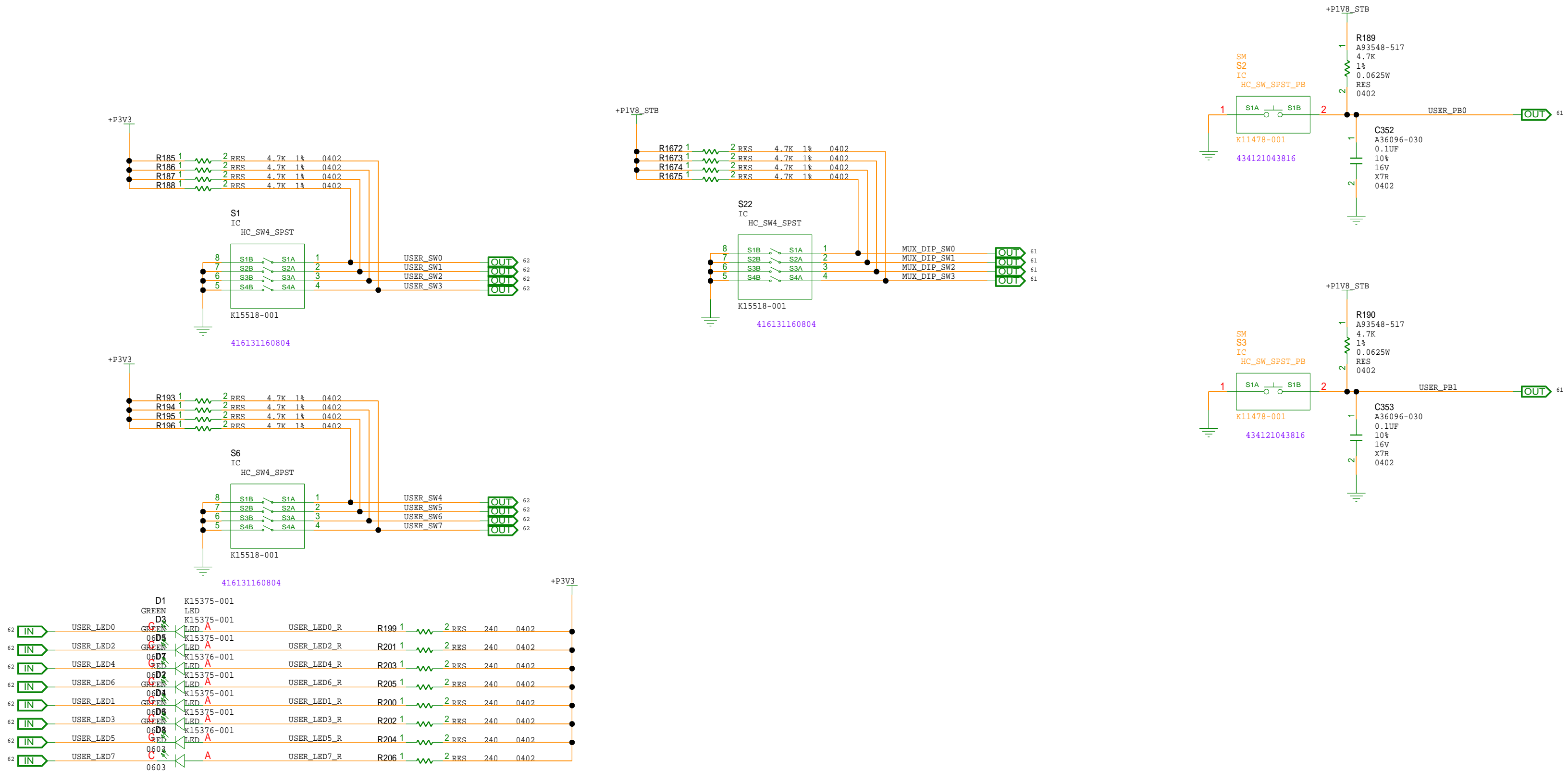
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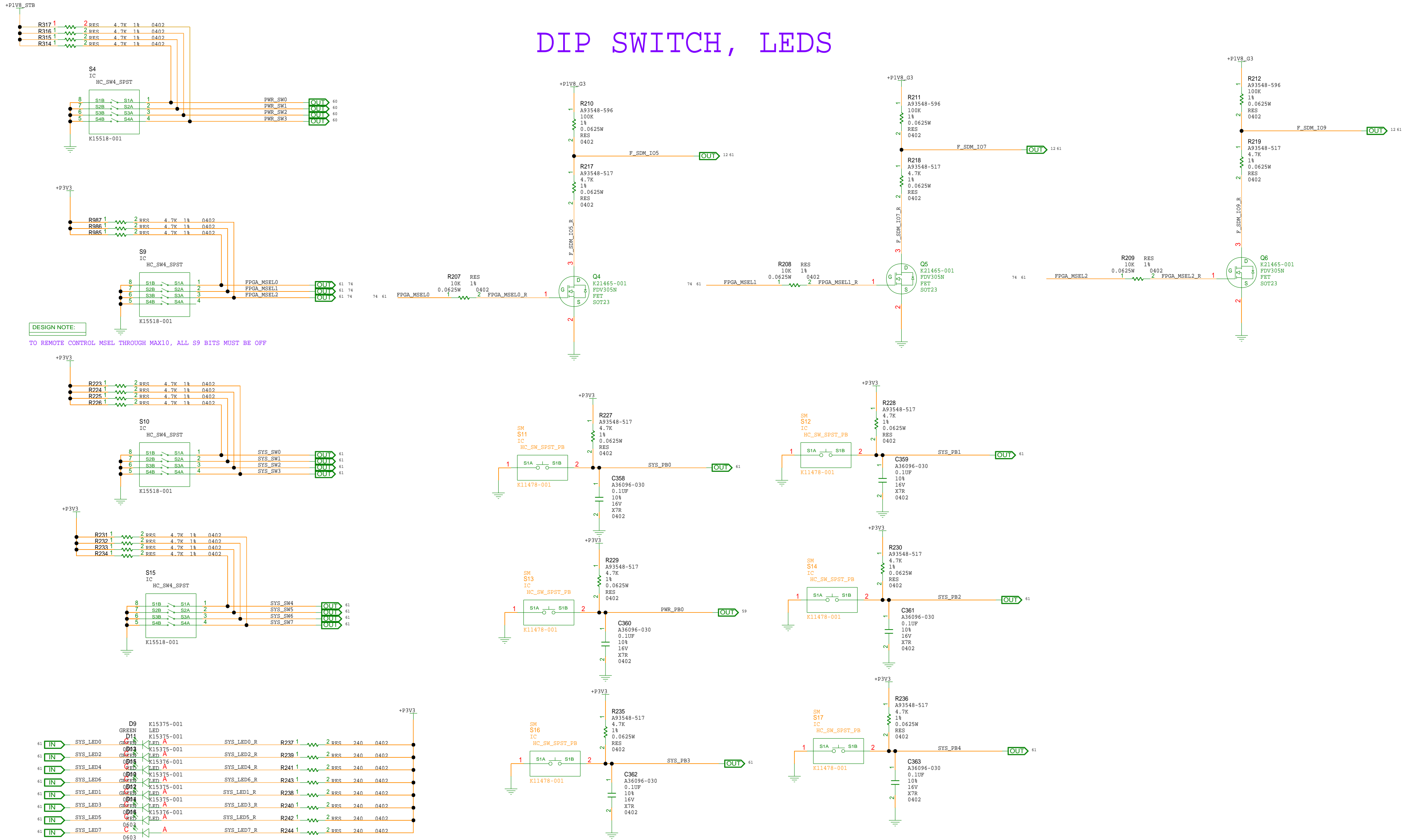
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DIP SWITCH, LEDS



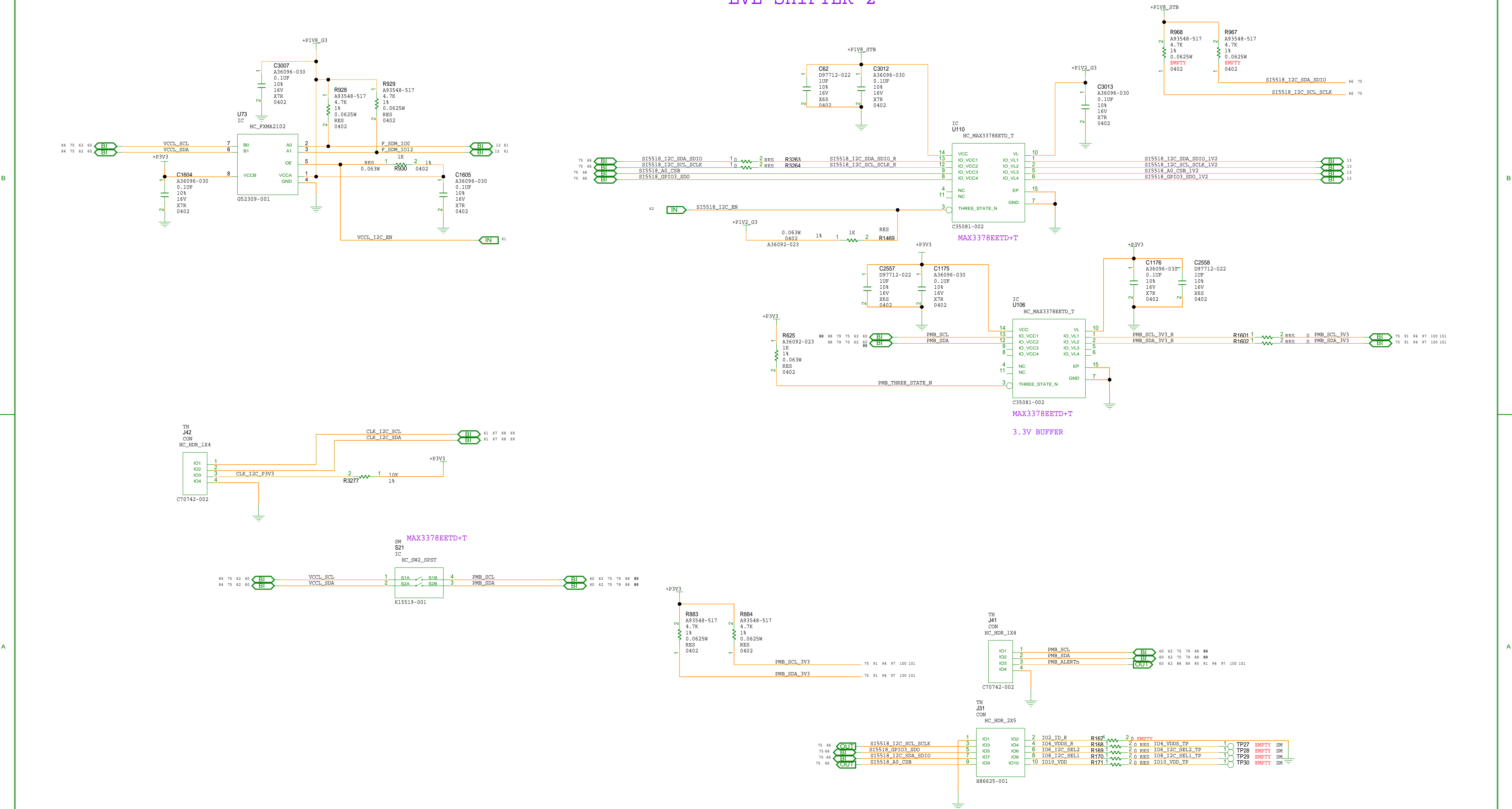
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DIP SWITCH, LEDS

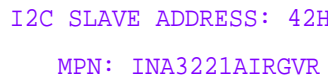
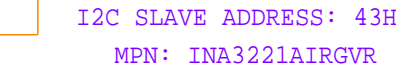
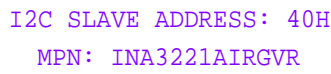


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LVL SHIFTER-2



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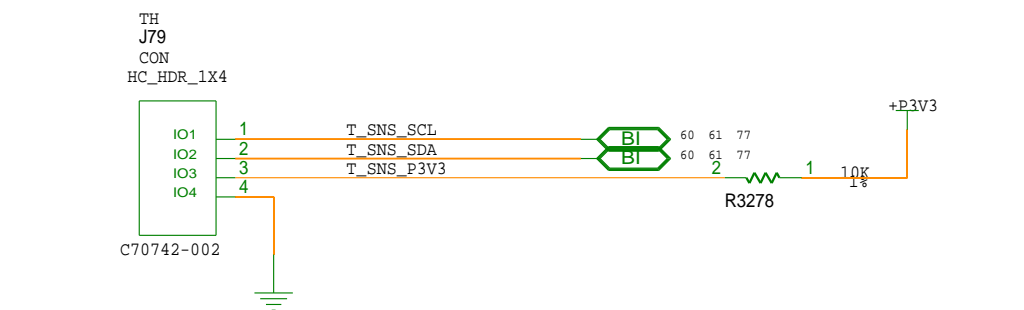
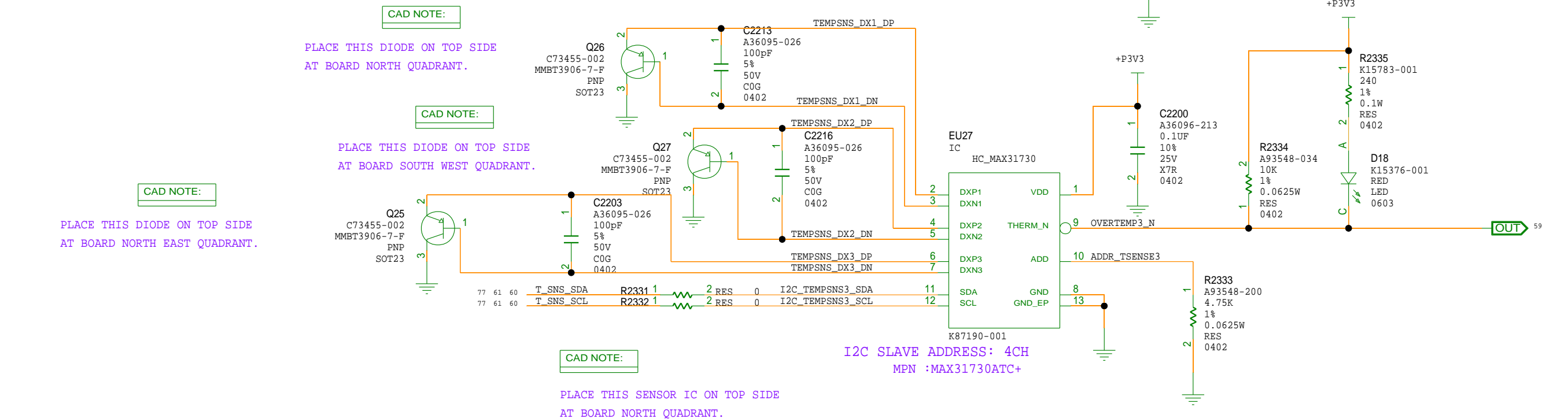
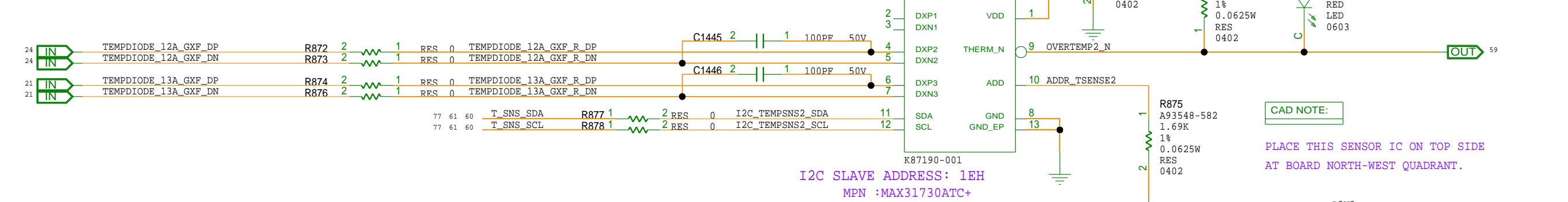
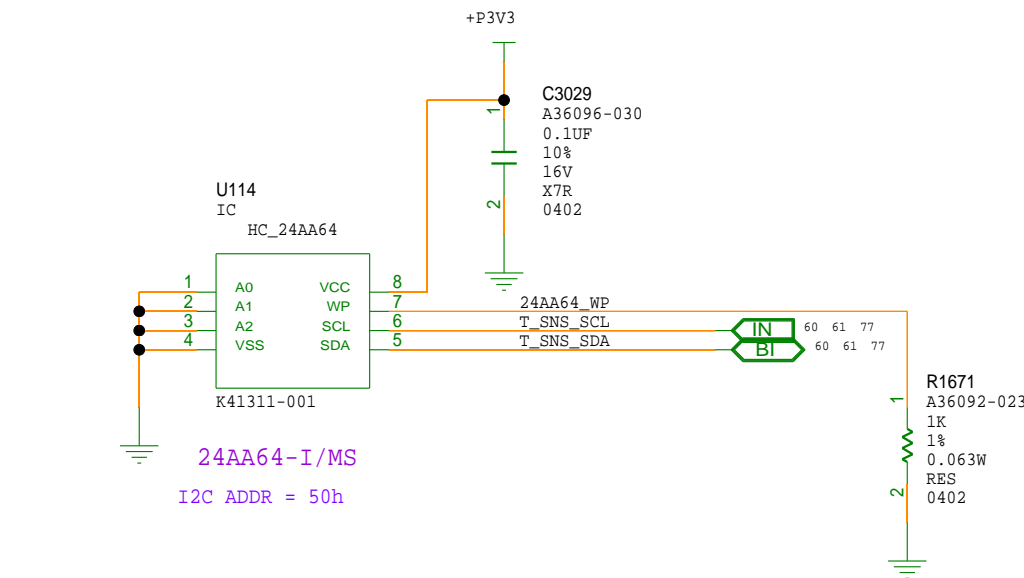
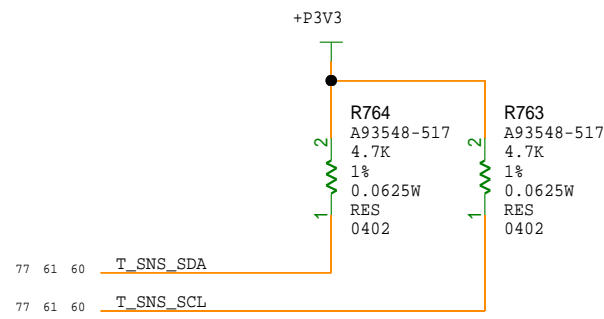
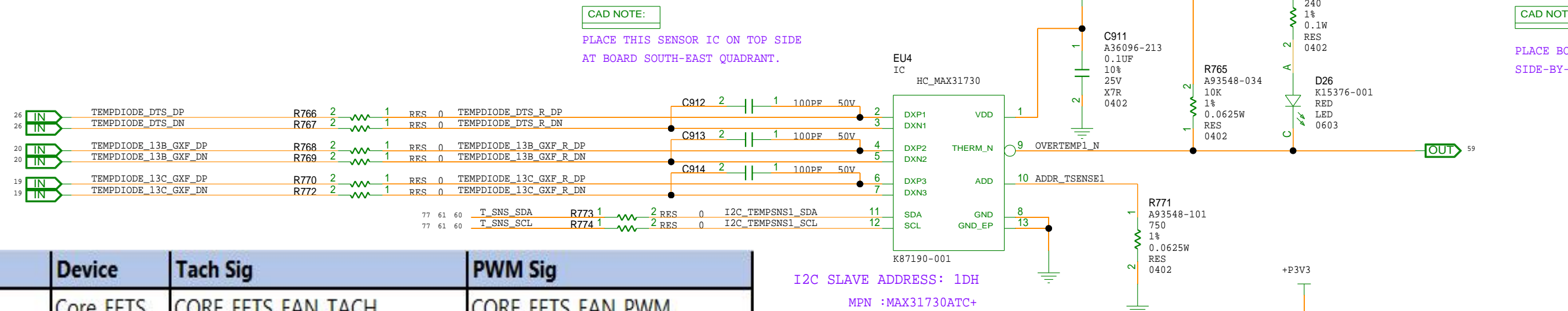
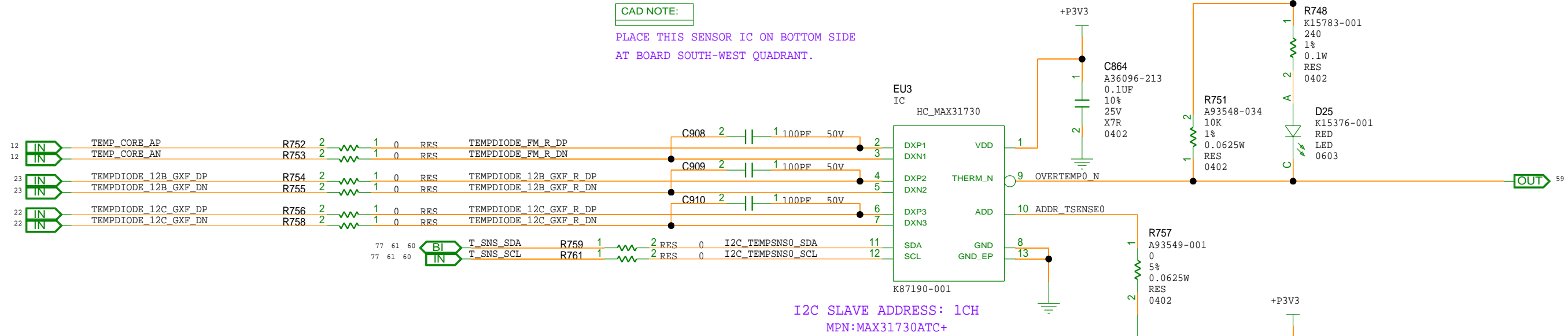
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BOARD TEMP SENSORS



Temp Sensor	Fan Connector	Device	Tach Sig	PWM Sig
Q26/EU27.CH1	J38	Core_FETS	CORE_FETS_FAN_TACH	CORE_FETS_FAN_PWM
EU3/EU4/EU11	J43	FPGA	FPGA_FAN_TACH	FPGA_FAN_PWM
Q27/EU27.CH2	J34	QSFP_LEFT	QSFP_LEFT_FAN_TACH	QSFP_LEFT_FAN_PWM
Q25/EU27.CH3	J44	QSFP_RIGHT	QSFP_RIGHT_FAN_TACH	QSFP_RIGHT_FAN_PWM

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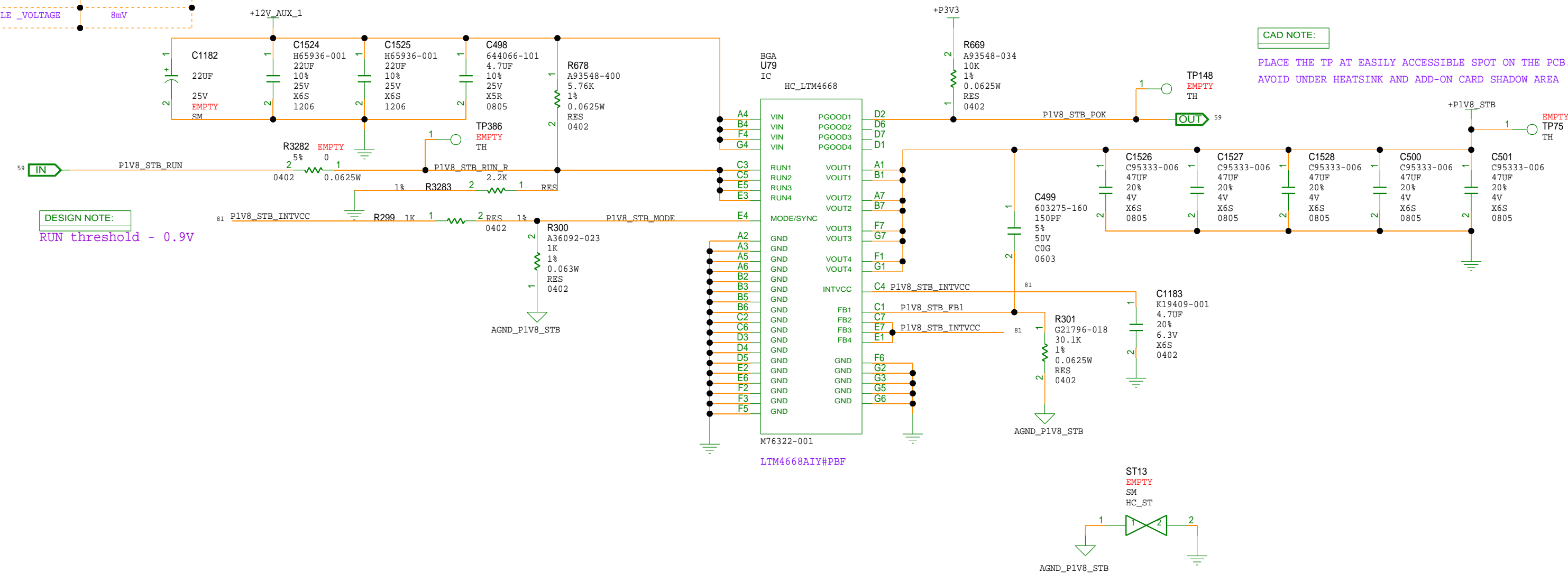
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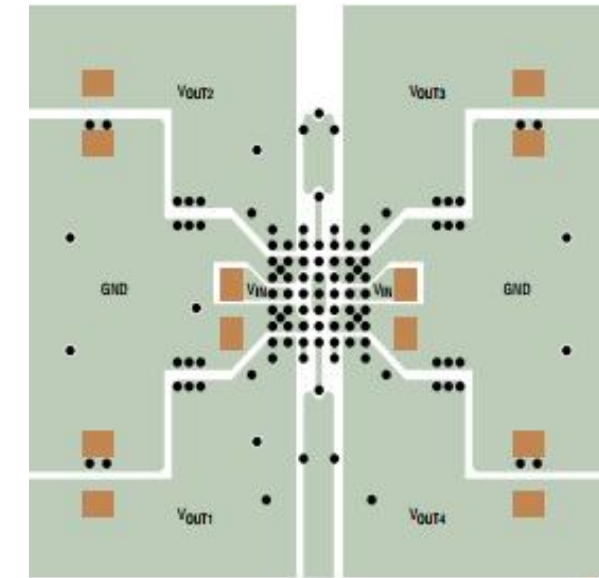
PARAMETER	VALUE
VOUT	1.8V
MAX CURRENT	4.8A
LOAD CURRENT	2.822A
FREQUENCY	
RIPPLE _VOLTAGE	8mV



DESIGN NOTE:
RUN threshold - 0.9V

CAD NOTE:

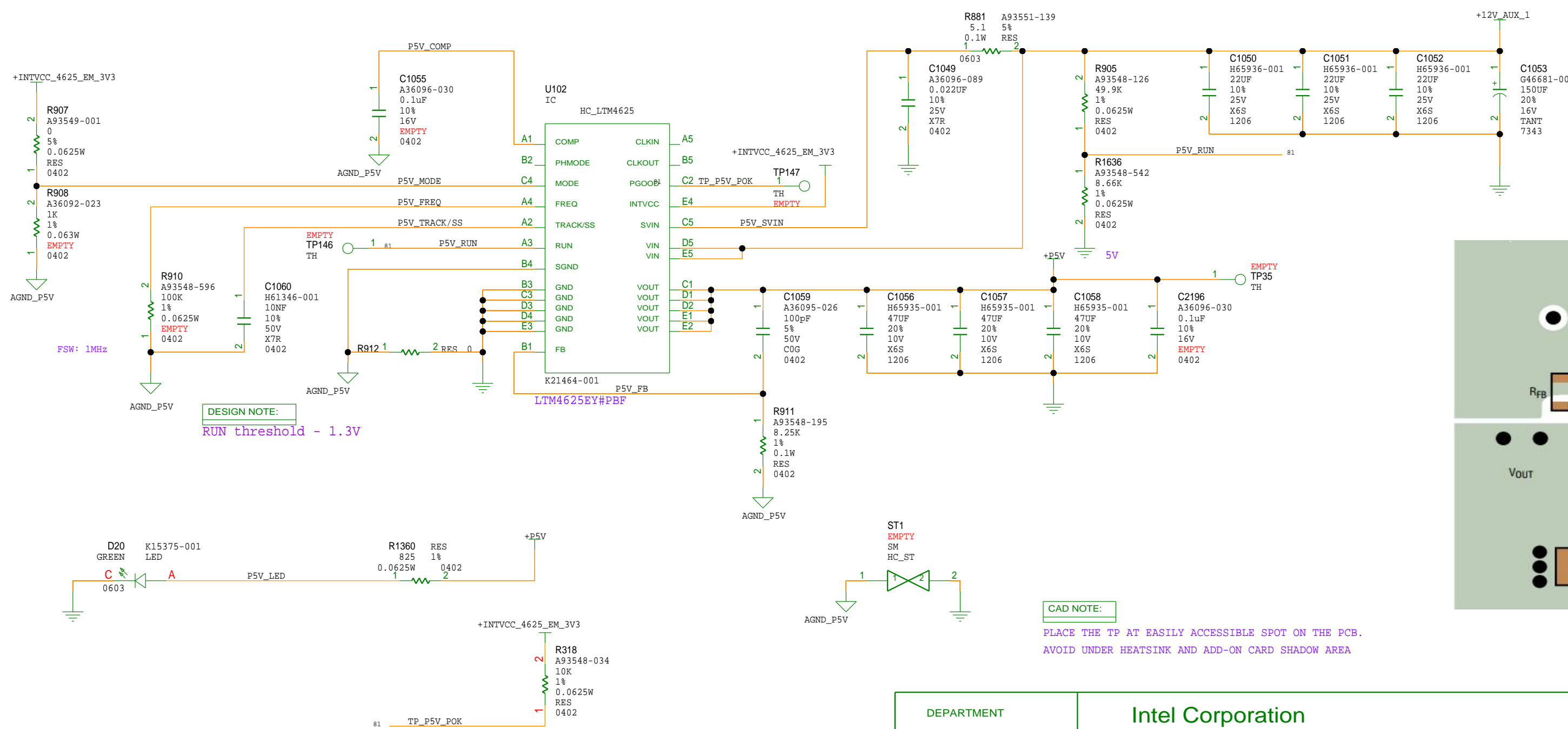
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA.



RECOMMENDED LAYOUT GUIDELINES

- Use large PCB copper areas for high current paths, including V_{IN} , GND, V_{OUT1} and V_{OUT2} . It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN} , PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- For parallel modules, tie the V_{OUT} , V_{FB} and COMP pins together. Use an internal layer to closely connect these pins together. The TRACK pin can be tied a common capacitor for regulator soft-start.
- Bring out test points on the signal pins for monitoring.

PV5

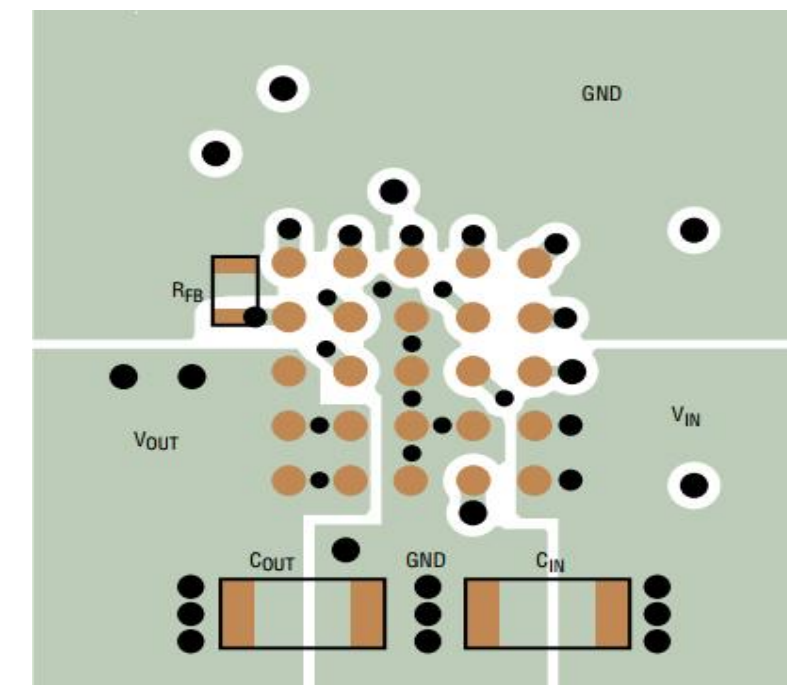


DESIGN NOTE:
RUN threshold - 1.3V

CAD NOTE:

PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

PARAMETER	VALUE
VOUT	5V
MAX CURRENT	5A
LOAD CURRENT	0.05A
FREQUENCY	1MHz
RIPPLE _VOLTAGE	5mV

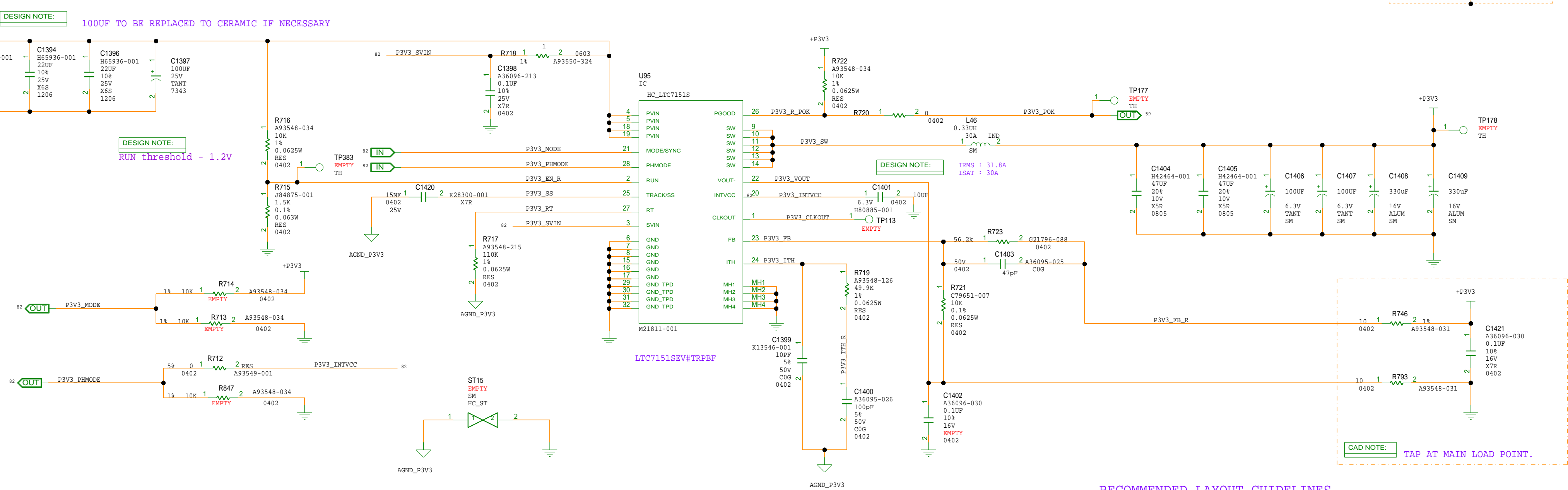


RECOMMENDED LAYOUT GUIDELINES

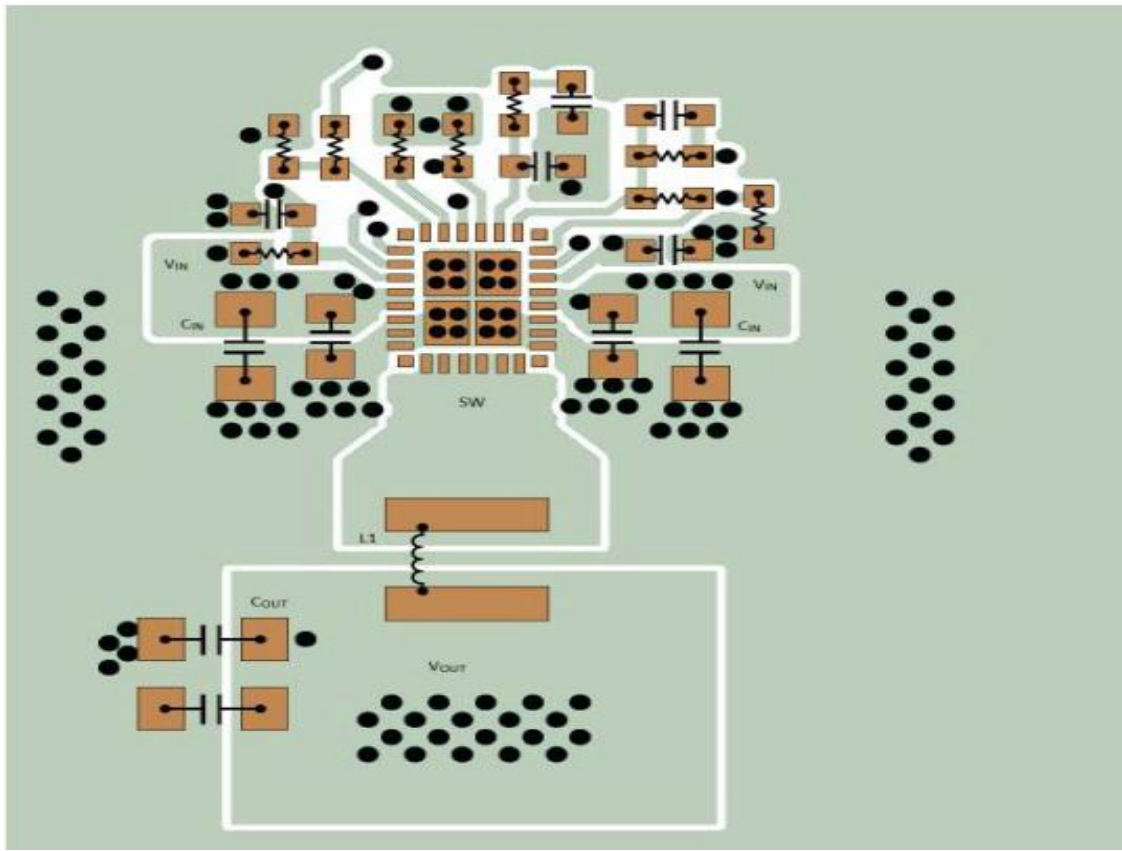
- Use large PCB copper areas for high current paths, including V_{IN} , GND and V_{OUT} . It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN} , PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- Bring out test points on the signal pins for monitoring.
- Keep separation between CLKIN, CLKOUT and FREQ pin traces to minimize possibility of noise due to crosstalk between these signals.

P3V3

PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	15A
LOAD CURRENT	6.189A
FREQUENCY	1.5MHz
RIPPLE_VOLTAGE	



RECOMMENDED LAYOUT GUIDELINES



- Are there pairs of capacitors (C_{IN}) between V_{IN} and GND as close as possible on both sides of the package? These capacitors provide the AC current to the internal power MOSFETs and their drivers as well as minimize EMI/EMC emissions.
- Are C_{OUT} and L closely connected? The (-) plate of C_{OUT} returns current to GND and the (-) plate of C_{IN} .
- Place the FB dividers close to the part with Kelvin connections to V_{OUT} and V_{OUT-} at the point-of-load, for differential V_{OUT} sensing.
- Keep sensitive components away from the SW pin. The FB resistors, R_T resistor, the compensation component, and the $INTV_{CC}$ bypass caps should be routed away from the SW trace and the inductor.

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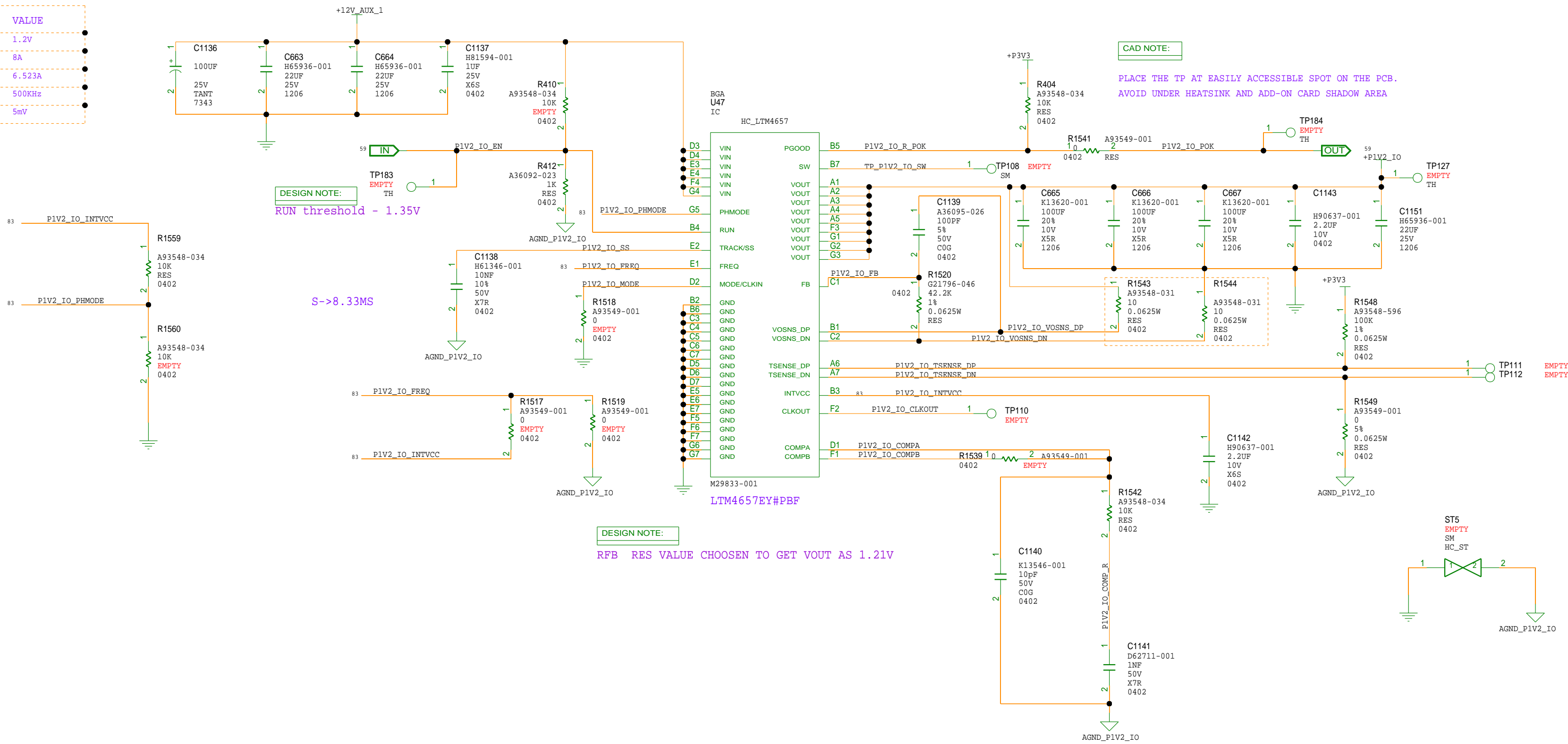
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P1V2_IO

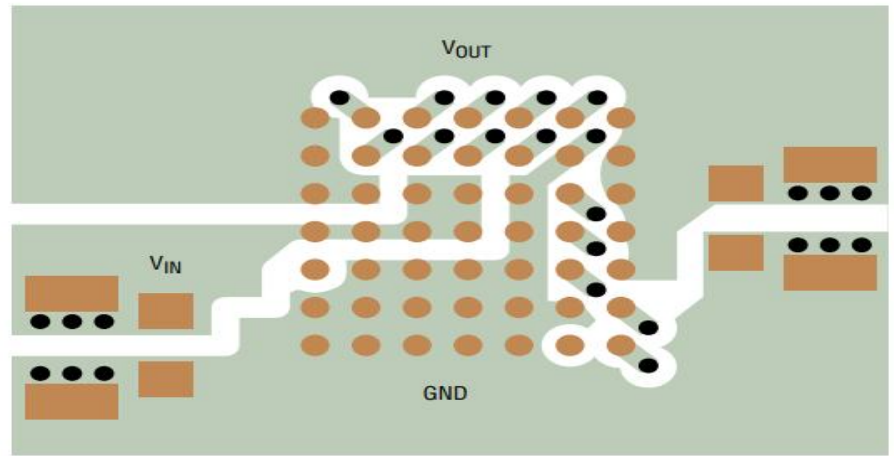
PARAMETER	VALUE
VOUT	1.2V
MAX CURRENT	8A
LOAD CURRENT	6.523A
FREQUENCY	500KHz
RIPPLE _VOLTAGE	5mV



RECOMMENDED LAYOUT GUIDELINES

- Use large PCB copper areas for high current paths, including V_{IN} , GND and V_{OUT} . It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN} , PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Bring out test points on the signal pins for monitoring.
- Keep separation between CLKIN, CLKOUT and FREQ pin traces to minimize possibility of noise due to cross-talk between these signals.

Figure 22 gives a good example of the recommended layout.



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VCCL CONTROLLER

DESIGN NOTE:

This is configured for LTC3888 with option for LTC3888-1 BOM stuffing

LTC3888IUHG#PBF

PMBUS SLAVE ADDRESS : 62H

RECOMMENDED LAYOUT GUIDELINES

- Place a ground or DC voltage layer between a power layer and a small-signal layer. Generally, power planes should be placed on the top layer (4-layer PCB), or top and bottom layer if more than 4 layers are used. Use wide/short copper traces for power components and avoid improper use of thermal relief around power plane vias to minimize resistance and inductance.
- Low ESR input capacitors should be placed as close as possible to the power stage FET supply and ground connections with the shortest copper traces possible. The power stage must be on the same layer of copper as the input capacitors with a common topside power connection at C_{IN} . Do not attempt to split the input decoupling for multiple phases, as a large resonant loop can result. Vias should not be used to make these connections. Avoid blocking forced air flow to the power stages with large size passive components.
- Place the inductor input as close as possible to the power stage. Minimize the surface area of the switch node. Make the trace width the minimum needed to support the maximum output current. Avoid copper fills or pours. Avoid running the connection on multiple copper layers in parallel. Minimize capacitance from the switch node to any other trace or plane.
- PCB traces for remote voltage sense should be run together back to the LTC3888 in pairs with the smallest spacing possible on any given layer on which they are routed. Avoid high frequency switching signals and ideally shield with ground planes. Filter components on these traces should return to GND (IC paddle) and not to a local PGND.
- PCB traces for output current sense (I_{SENSE} , I_{REF}) should avoid high frequency switching signals and ideally be shielded with ground planes. Filter components on these traces should return to GND (IC paddle) and not to a local PGND.
- Place low ESR output capacitors adjacent to the inductor output and ground. Output capacitor ground connections must feed into the same copper that connects to the input capacitor ground before connecting back to system ground.
- Connection of switching ground to system ground, small-signal analog ground or any internal ground plane should be single-point. If the system has an internal system ground plane, a good way to do this is to cluster vias into a single star point to make the connection. This cluster should be located directly beneath the IC GND paddle, which serves as analog signal ground. A useful CAD technique is to make separate ground nets and use a 0 Ω resistor to connect them to system ground.
- Place all small-signal components away from high frequency switching nodes. Place decoupling capacitors for the LTC3888 immediately adjacent to the IC.
- A good rule of thumb for via count in a given high current path is to use 0.5A per via. Be consistent when applying this rule.
- Copper fills or pours are good for all power connections except as noted above in rule 3. Copper planes on multiple layers can also be used in parallel. This helps with thermal management and lowers trace inductance, which further improves EMI performance.

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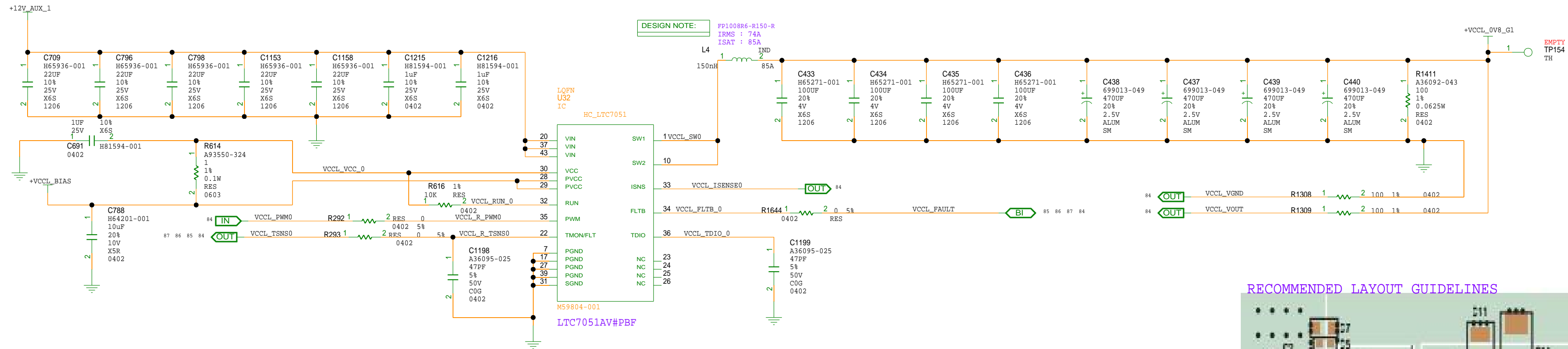
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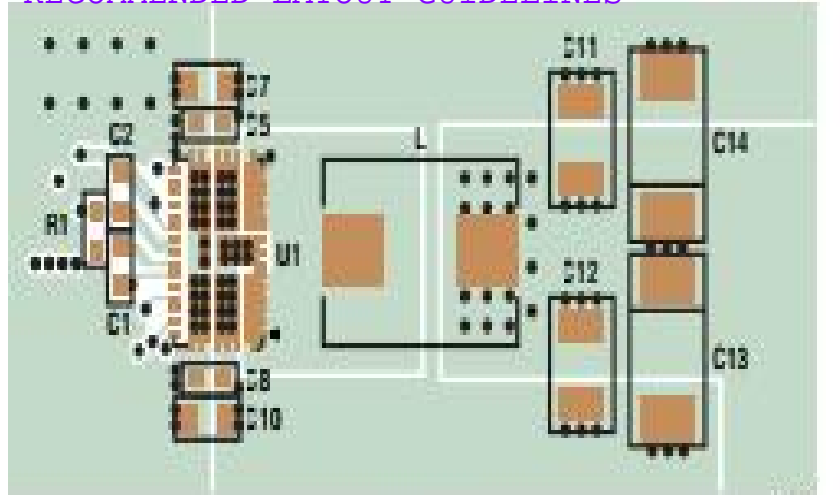
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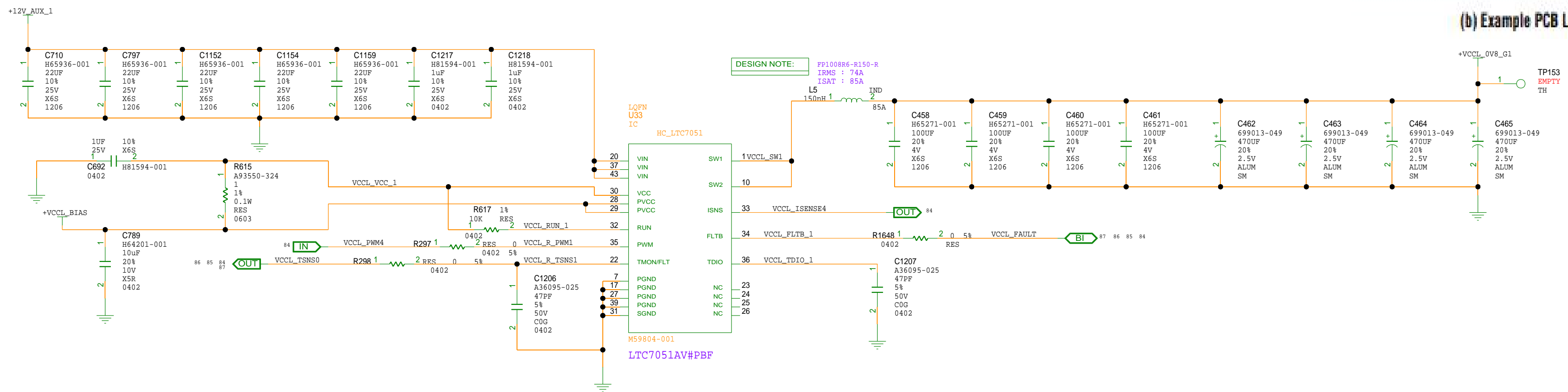
CORE FETS



RECOMMENDED LAYOUT GUIDELINES



(b) Example PCB Layout



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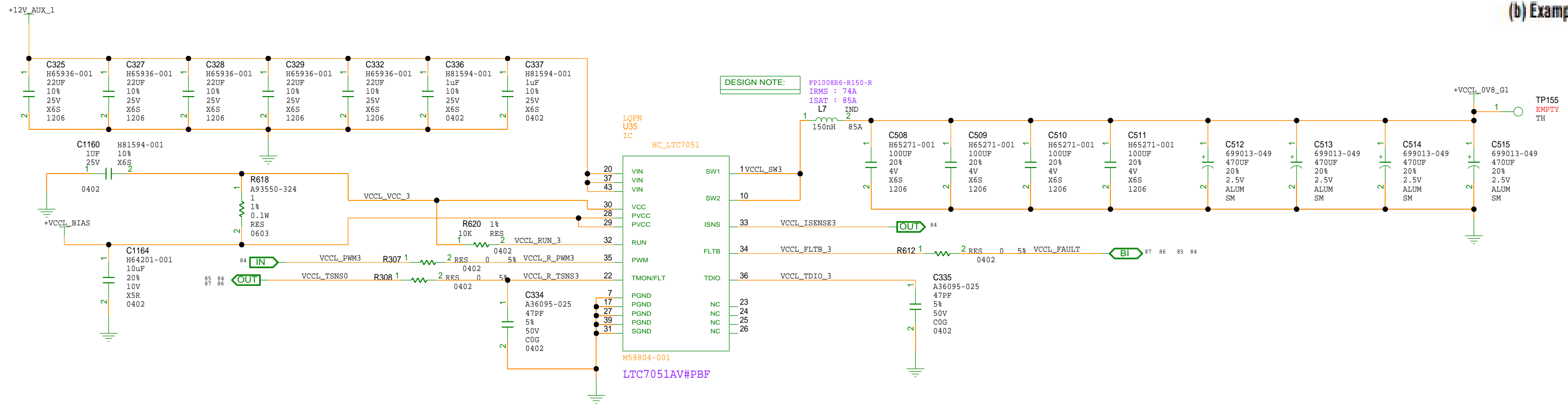
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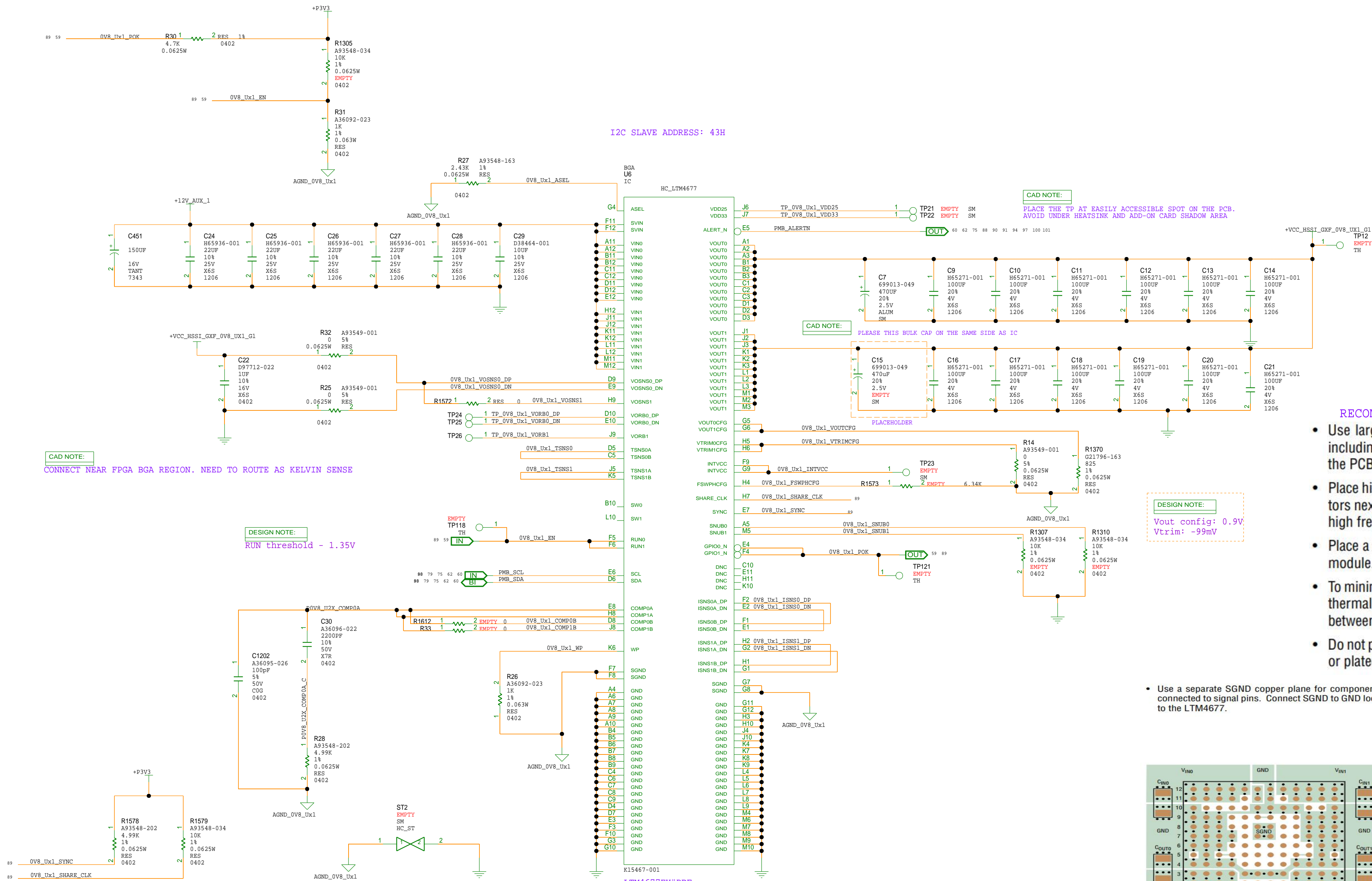
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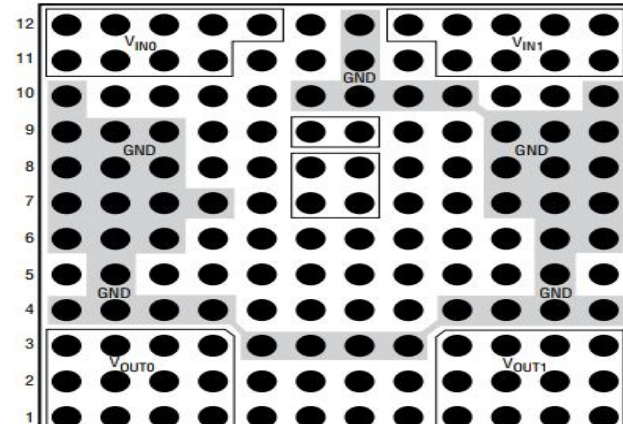
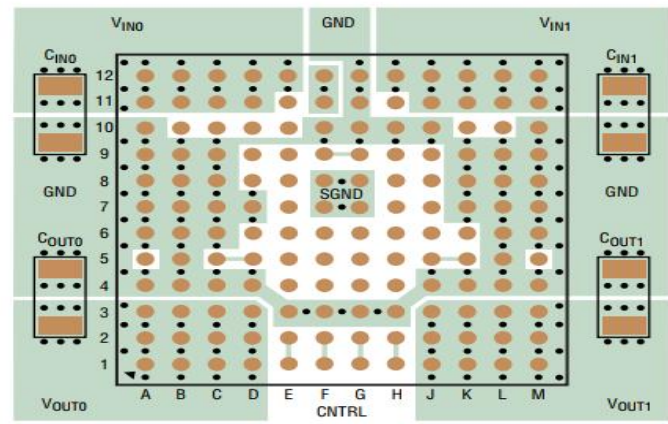
(b) Example PCB Layout

VCC_HSSI_GXF_0V8_UX1_G1



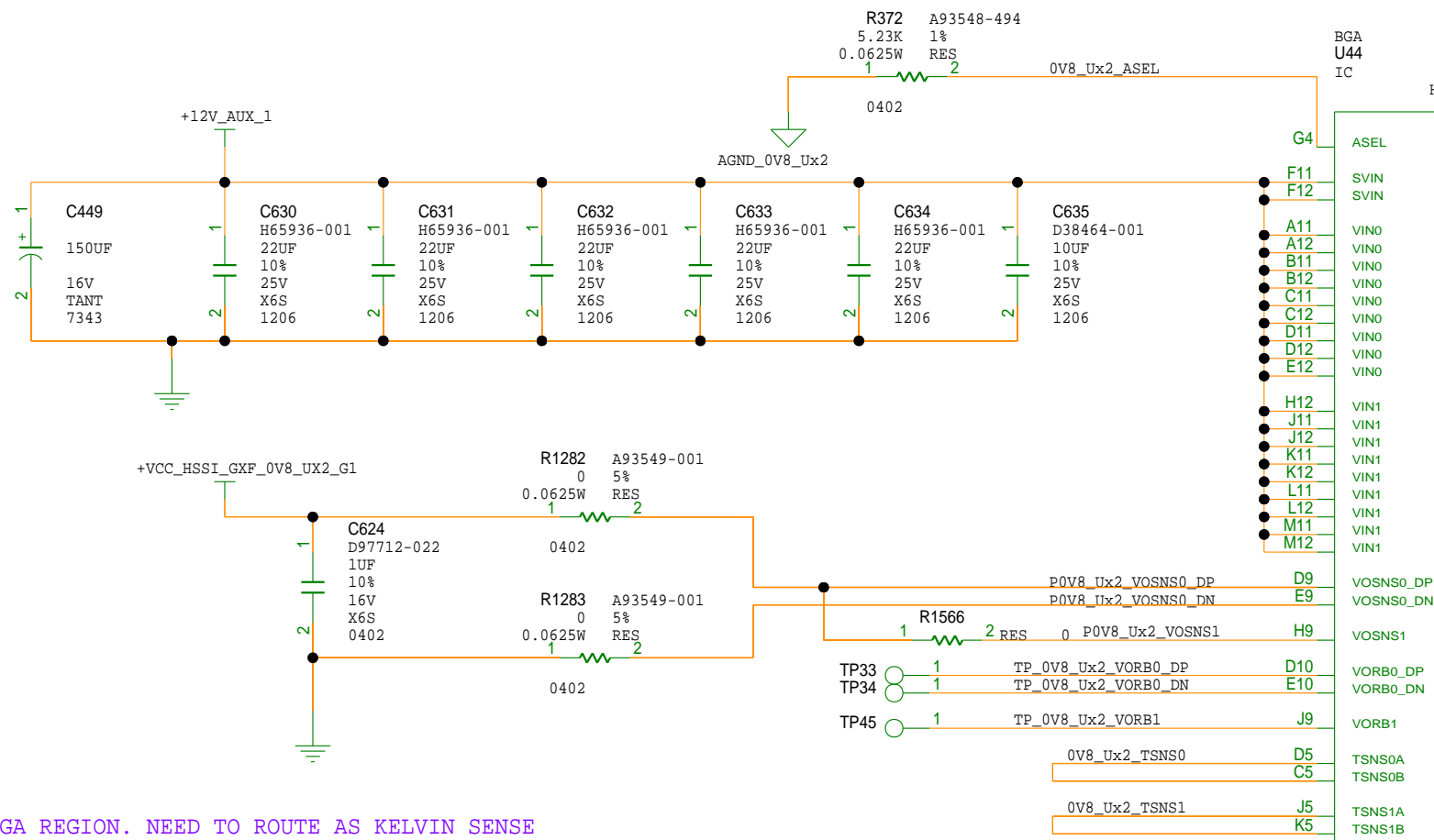
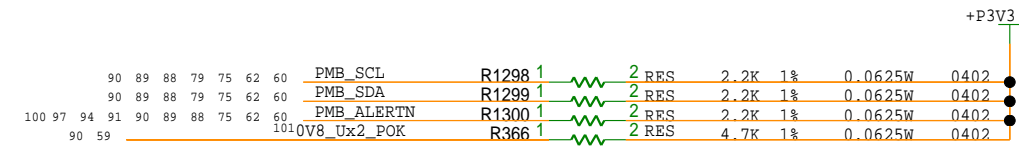
RECOMMENDED LAYOUT GUIDELINES

- Use large PCB copper areas for high current paths, including V_{INn} , GND and V_{OUTn} . It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{INn} , GND and V_{OUTn} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the module.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on pads, unless they are capped or plated over.

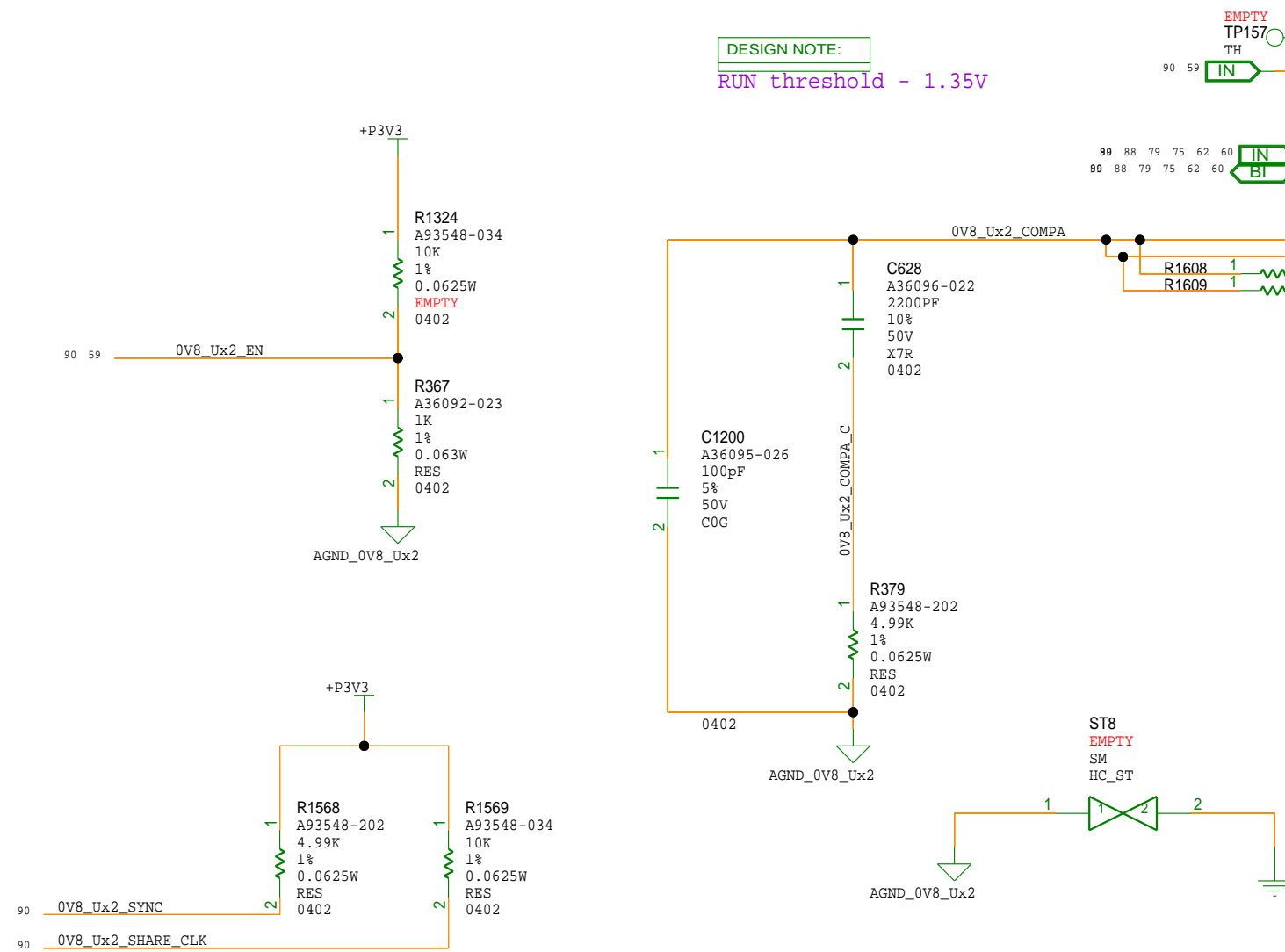


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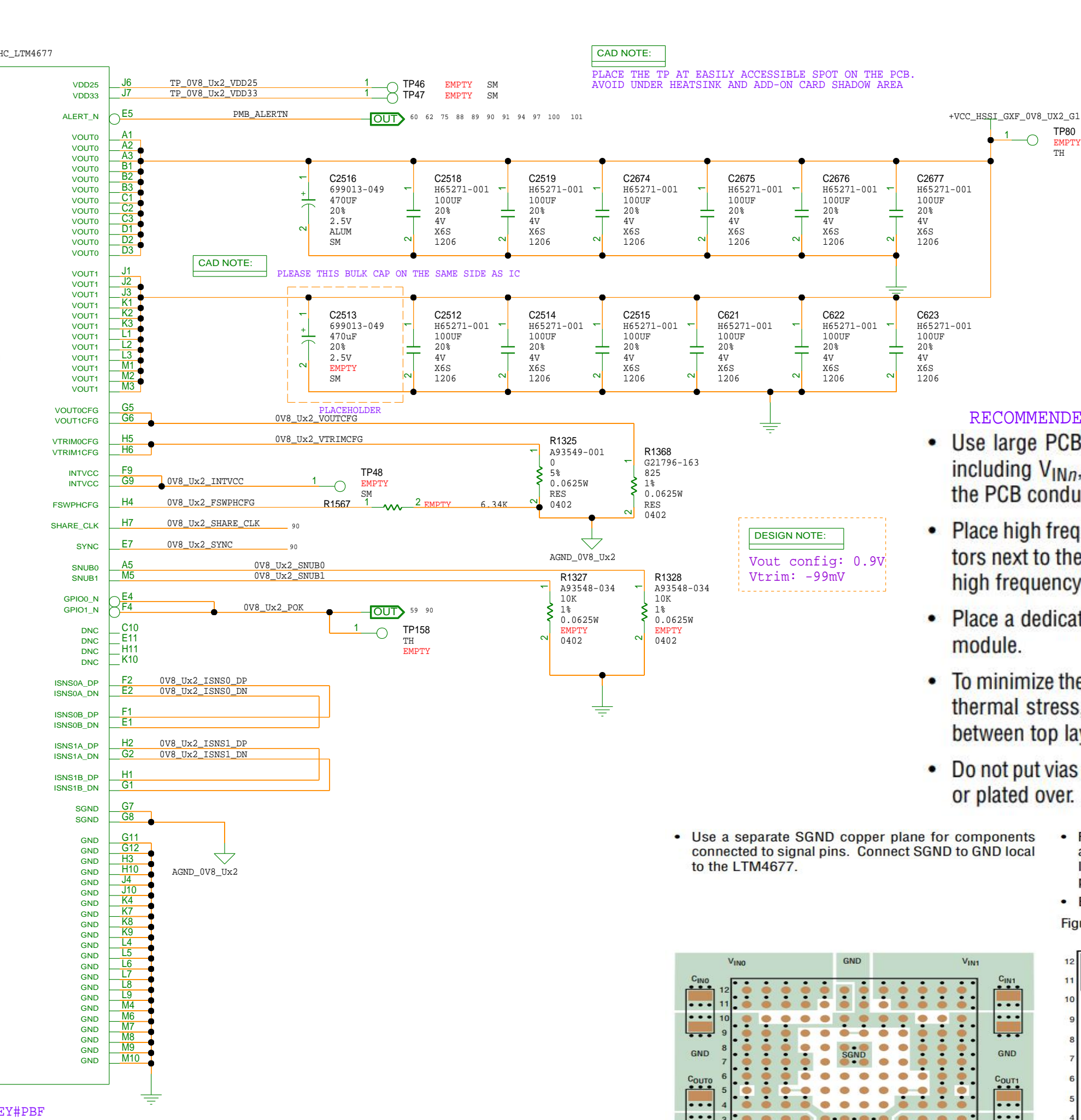
PARAMETER	VALUE
VOUT	0.8V
MAX CURRENT	36A(SINGLE)
LOAD CURRENT	28.787A
FREQUENCY	500KHz
RIPPLE _VOLTAGE	10mV
PM BUS ADDRESS	7 BIT 0X46



CAD NOTE:
CONNECT NEAR FPGA BGA REGION. NEED TO ROUTE AS KELVIN SENSE



DESIGN NOTE:
RUN threshold - 1.35V



CAD NOTE:

PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

CAD NOTE: PLEASE THIS BULK CAP ON THE SAME SIDE AS IC

0V8 11x2 VOUTCEG

DESIGN NOTE:
Vout config: 0.9V
Vtrim: -99mV

RECOMMENDED LAYOUT GUIDELINES

- Use large PCB copper areas for high current paths, including V_{INn} , GND and V_{OUTn} . It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{INn} , GND and V_{OUTn} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the module.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on pads, unless they are capped or plated over.

- Use a separate SGND copper plane for components connected to signal pins. Connect SGND to GND local to the LTM4677.
 - For parallel modules, tie the V_{OUT_n} , V_{OSNSn}^+ / V_{OSNSn}^- and/or V_{OSNSn} /SGND voltage-sense differential pair lines, RUN_n , $GPIO_n$, $COMP_{nA}$, SYNC and SHARE_CLK pins together—as shown in Figure 29.
 - Bring out test points on the signal pins for monitoring.
- Figure 26 gives a good example of the recommended layout.

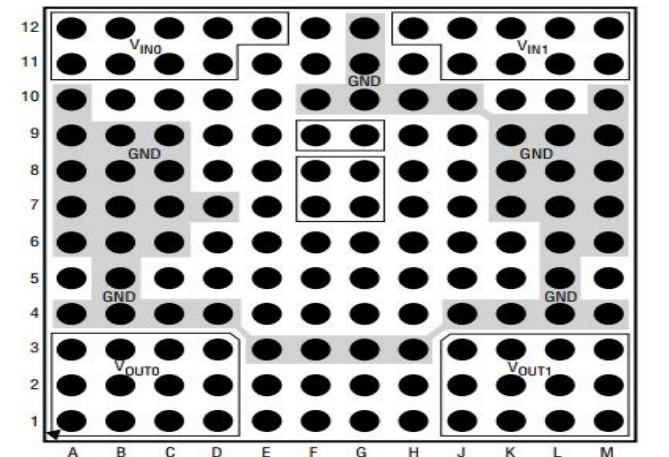
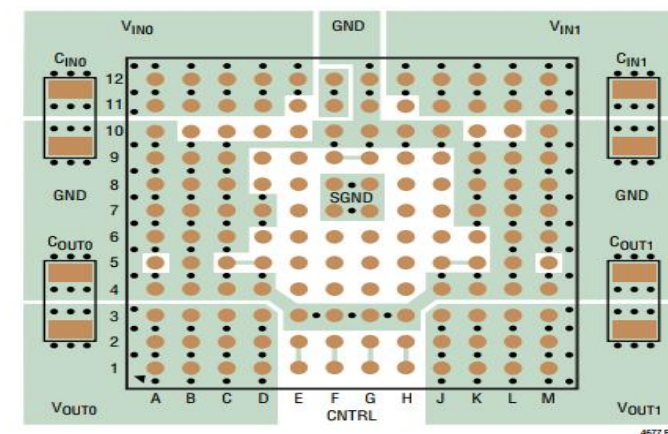
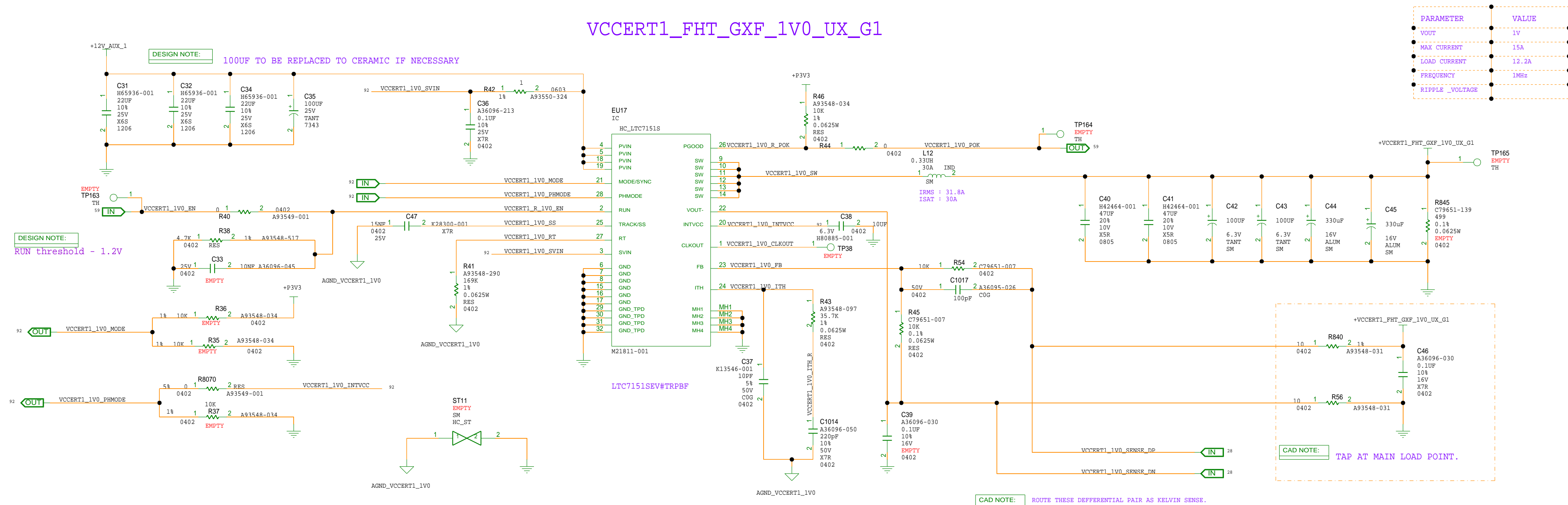


Figure 26 gives a good example of the recommended layout.

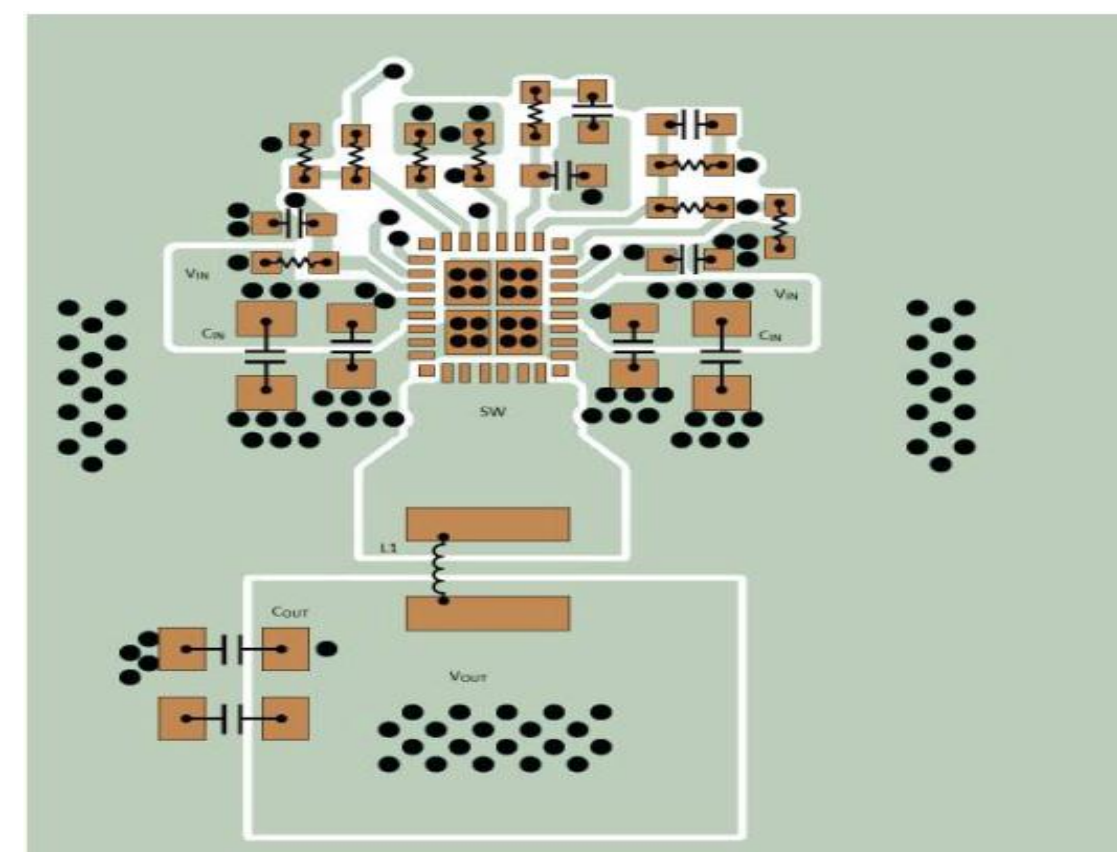
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		C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 90 OF 105





RECOMMENDED LAYOUT GUIDELINES



1. Are there pairs of capacitors (C_{IN}) between V_{IN} and GND as close as possible on both sides of the package? These capacitors provide the AC current to the internal power MOSFETs and their drivers as well as minimize EMI/EMC emissions.
2. Are C_{OUT} and L closely connected? The (-) plate of C_{OUT} returns current to GND and the (-) plate of C_{IN} .
3. Place the FB dividers close to the part with Kelvin connections to V_{OUT} and V_{OUT-} at the point-of-load, for differential V_{OUT} sensing.
4. Keep sensitive components away from the SW pin. The FB resistors, R_T resistor, the compensation component, and the $INTV_{CC}$ bypass caps should be routed away from the SW trace and the inductor.

VCCERT2_FHT_GXF_1V0_UX_G1

PARAMETER	VALUE
VOUT	1V
MAX CURRENT	2A
LOAD CURRENT	1.533A
FREQUENCY	
RIPPLE_VOLTAGE	

RECOMMENDED LAYOUT GUIDELINES

- Place the input capacitor as close as possible to the VIN and GND pins.
- Place the output capacitor as close as possible to the VOUT and GND pins.
- Place the soft start capacitor (C_{SS}) as close as possible to the SS pin.
- Place the reference capacitor (C_{REF}) and regulator capacitor (C_{REG}) as close as possible to the REFCAP pin and the VREG pin, respectively.
- Connect the load as close as possible to the VOUT and SENSE pins.

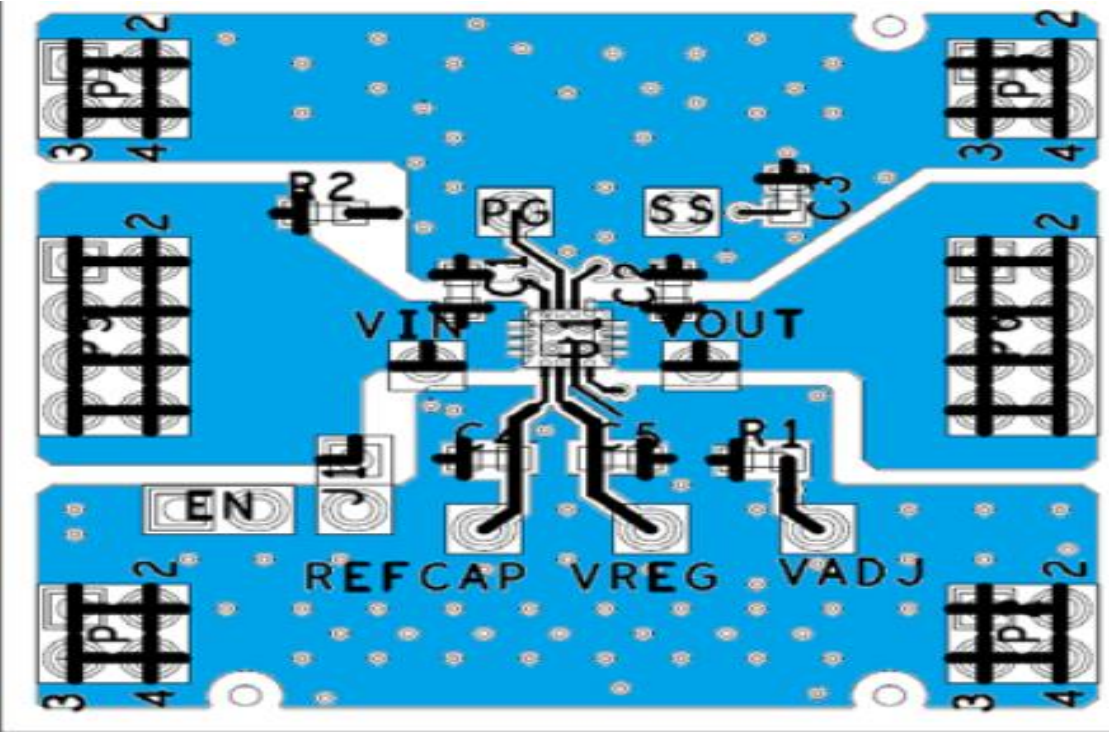


Figure 45. Typical Board Layout, Top Side

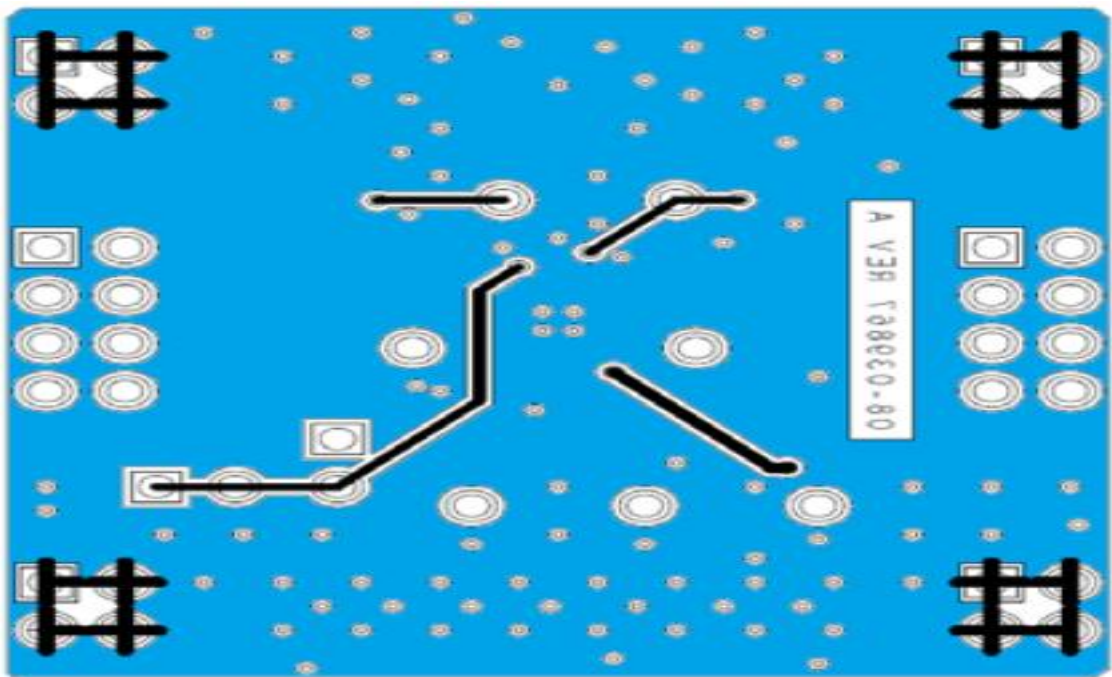


Figure 46. Typical Board Layout, Bottom Side

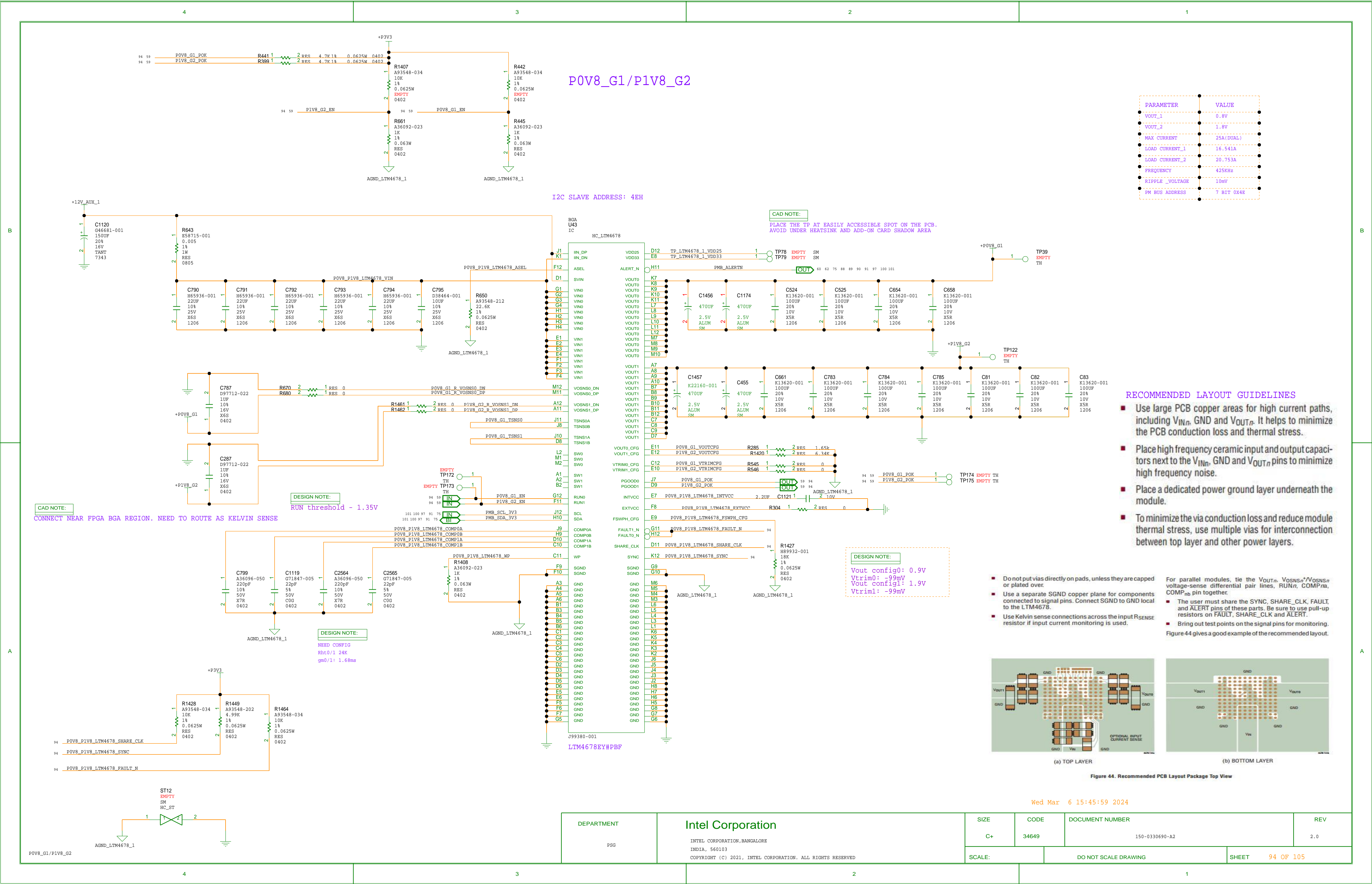
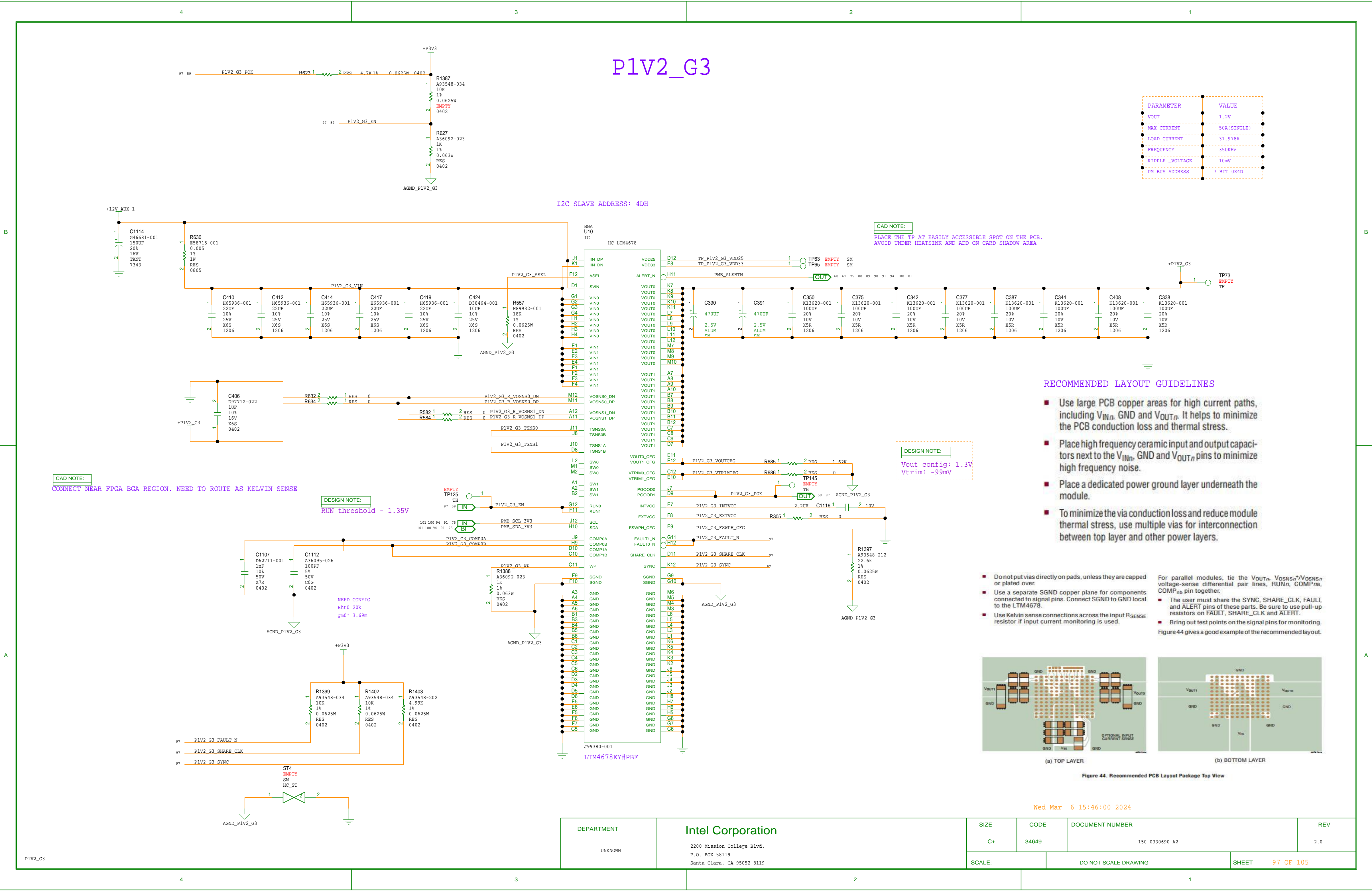




Figure 22 gives a good example of the recommended layout.

VCCEHT_FHT_GXF_1V5_U1X_G2/P2V5_G2







12904-065

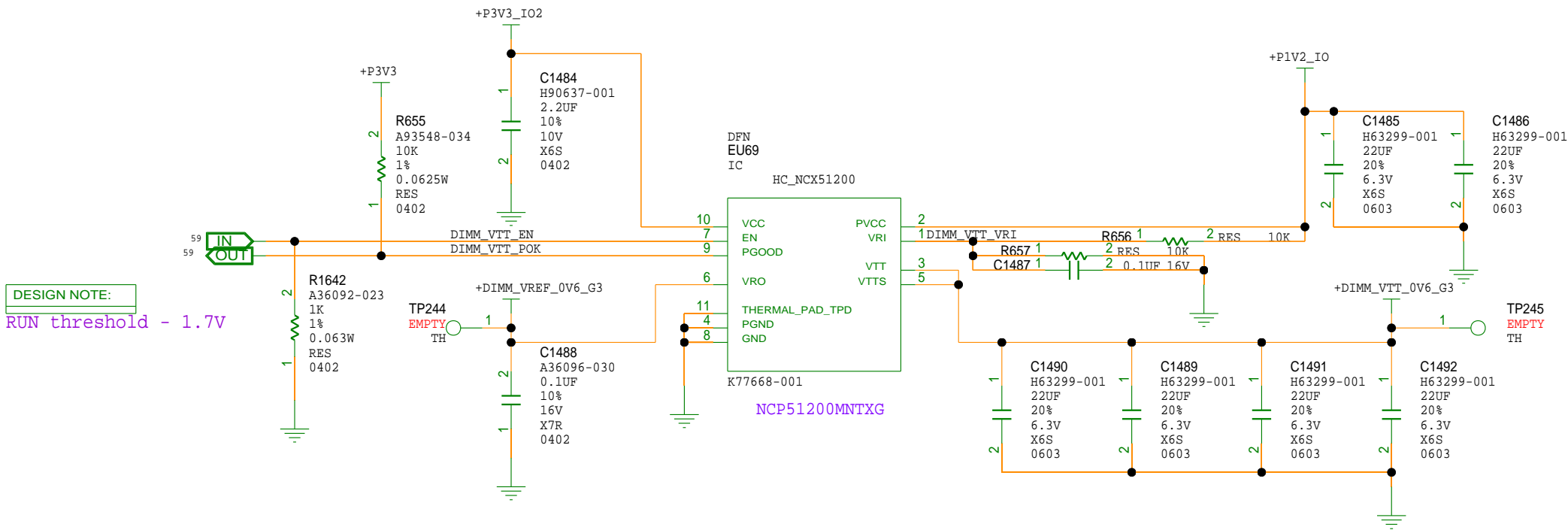
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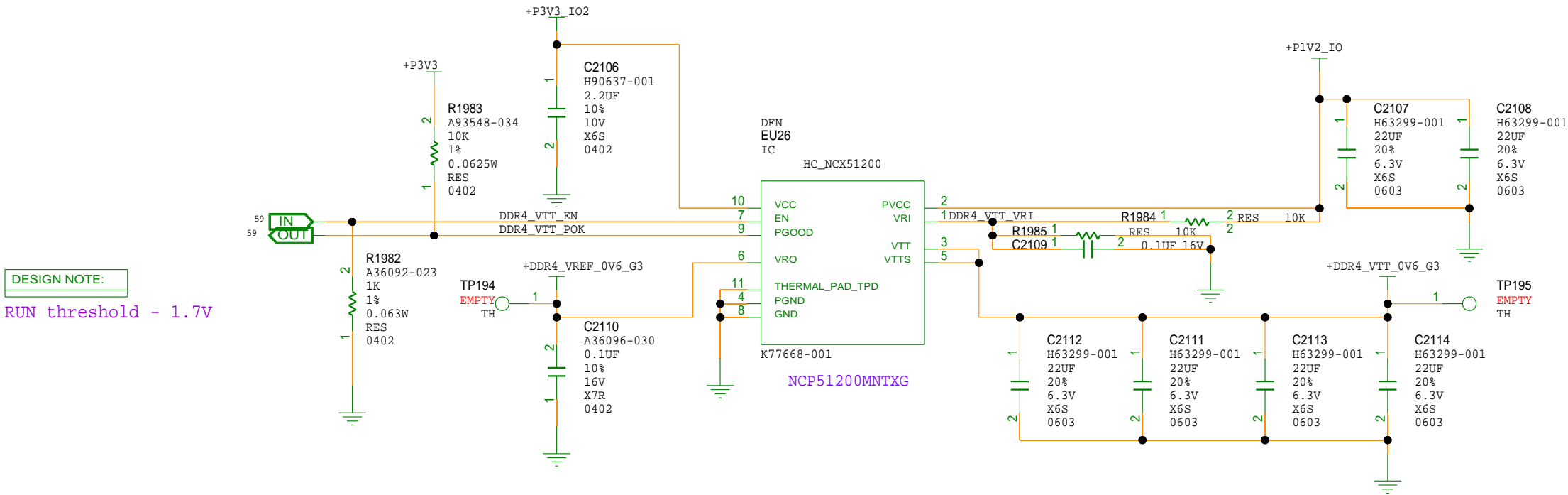
Wed Mar 6 15:46:01 2024

VTT REGULATORS

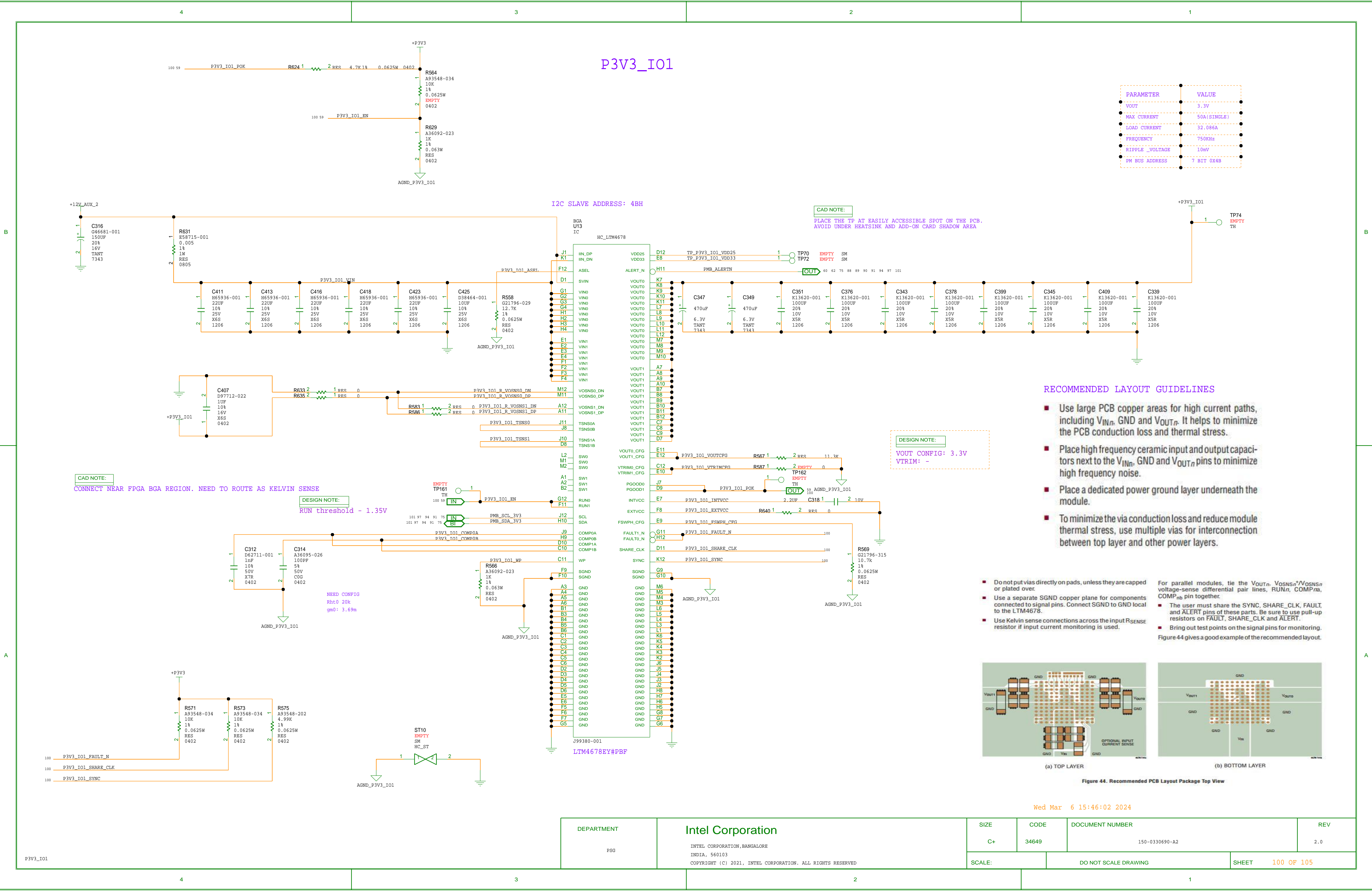
PARAMETER	VALUE
VOUT	0.6V
MAX CURRENT	3A
LOAD CURRENT	1.1A
FREQUENCY	
RIPPLE_VOLTAGE	

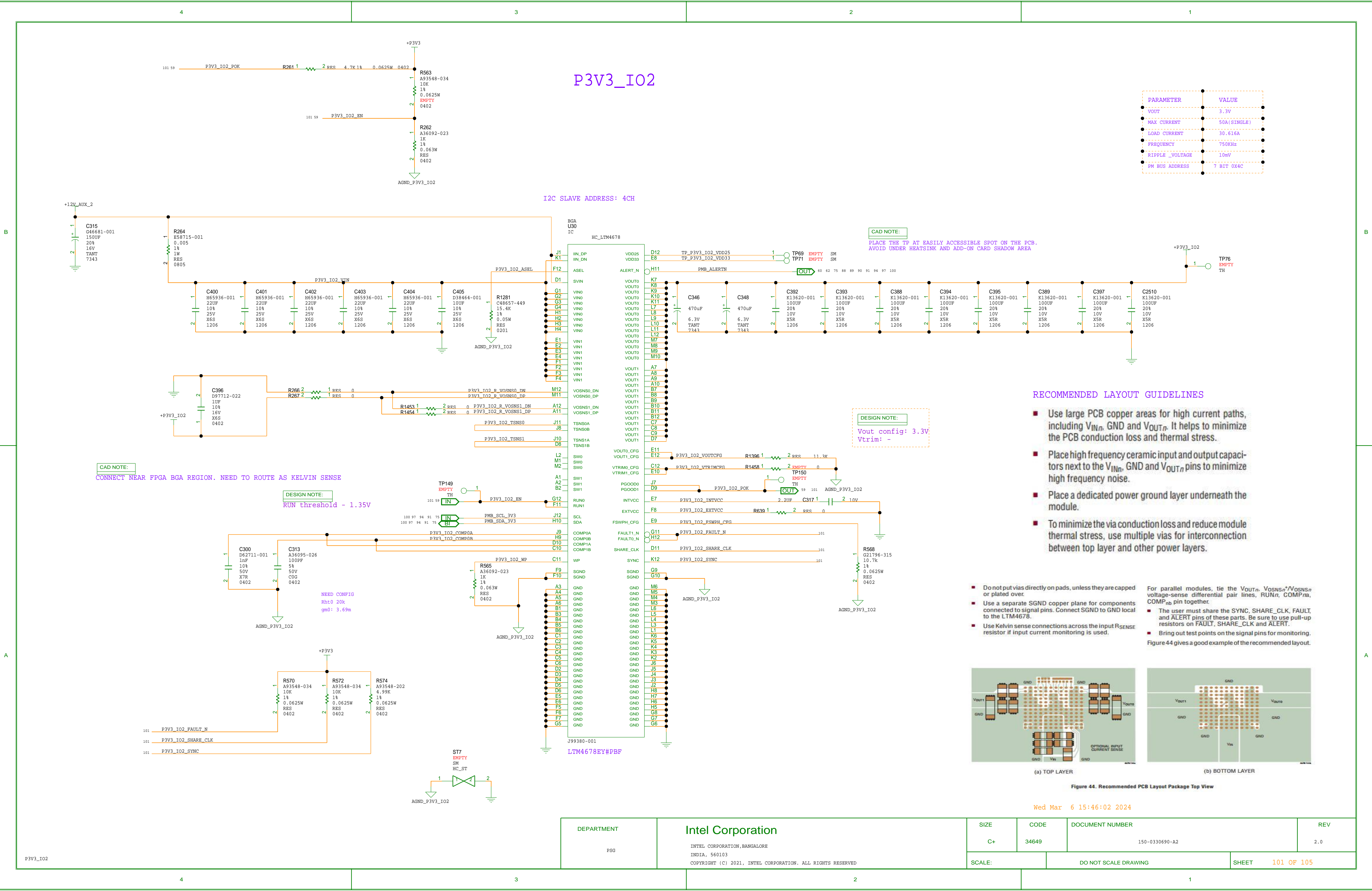


PARAMETER	VALUE
VOUT	0.6V
MAX CURRENT	3A
LOAD CURRENT	1.5A
FREQUENCY	
RIPPLE_VOLTAGE	



Wed Mar 6 15:46:01 2024





FMC PWR LOAD SWITCHES

PARAMETER	VALUE
VOUT	12V
MAX CURRENT	
LOAD CURRENT	1A
FREQUENCY	
RIPPLE_VOLTAGE	

DESIGN NOTE:

ENABLE ON THRESHOLD

1.4V

7A CURRENT LIMIT
0.34W PDISS

LTC4211CMS8#PBF

CAD NOTE:

PLACE CLOSE TO THE RESPECTIVE FMC CONNECTOR

CAD NOTE:

PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

FET_PARAMETER	VALUE
VGS	+20 V
ID	60 A

PARAMETER	VALUE
VOUT	12V
MAX CURRENT	
LOAD CURRENT	1A
FREQUENCY	
RIPPLE_VOLTAGE	

DESIGN NOTE:

ENABLE ON THRESHOLD

1.4V

LTC4211CMS8#PBF

CAD NOTE:

PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

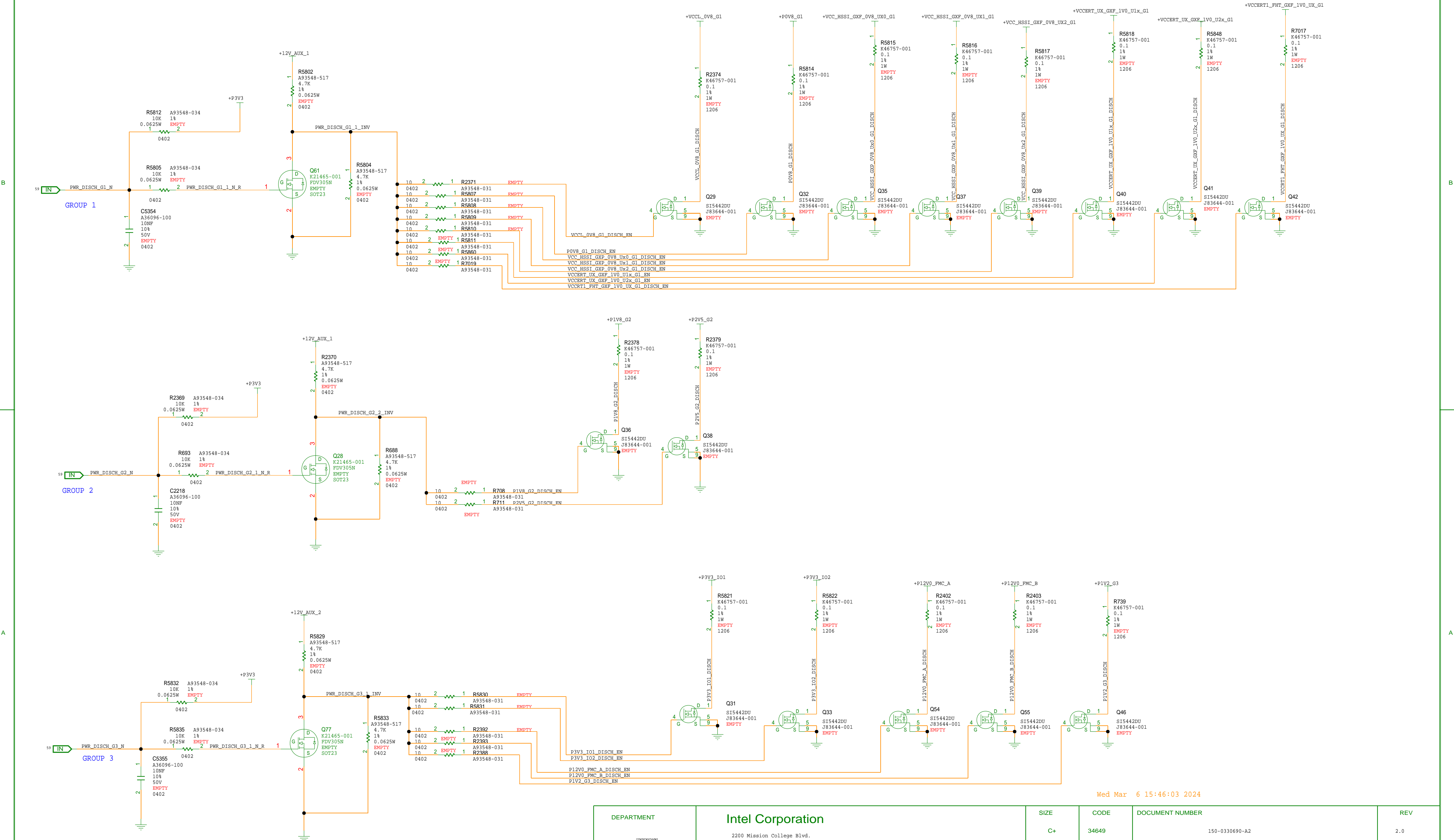
FET_PARAMETER	VALUE
VGS	+20 V
ID	60 A

CAD NOTE:

PLACE CLOSE TO THE RESPECTIVE FMC CONNECTOR

Wed Mar 6 15:46:03 2024

QUICK DISCHARGE 1



Wed Mar 6 15:46:03 2024

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
UNKNOWN	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	C+	34649	150-0330690-A2	2.0
SCALE:		DO NOT SCALE DRAWING			SHEET
					103 OF 105

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REVISION _HISTORY

UPDATED ALL DESIGN CHANGES AS PER THE CHANGE LIST AFTER VALIDATION IS COMPLETED
MAJOR DESIGN CHANGES WERE LISTED BELOW FOR REFERENCE.

- 1) REPLACED OCXO WITH TCXO (7N19471003) AT Y7.
- 2) MOUNTED R1295, R1579, R1569, R1402,R573 WITH 10K RESISTOR.
- 3) CHANGED THE EU13 ADDRESS TO 6BH IN SCHEMATIC TEXTS & POWER TREE DOC.
- 4) USE THE AVAILABLE PB FOR POWER MAX10 RESET CONFIGURATION.
- 5) REMOVE DISCHARGE CIRCUIT FOR ALL THE GROUPS. PAGE 103 & 104 SHOULD BE REMOVED FROM SCHEMATICS.
- 6) REPLACE LTC7151SIV#PBF[-40C TO 125C] WITH LTC7151SEV#PBF[0C TO 85C].
- 7) ADDED PULL-UP TO DDR4_ALERT_N FOR DRR4 MEMORY COMPONENT.
- 8) UPDATED BELOW RESISTORS DNI, SINCE THOSE ARE ADDITIONAL PULL_UPS.
R1906,R1907,R1912,R1913,R1890,R1891,R1896,R1897,R1038,R1049,R1076,R1077,R1845,R1846,R2465,R2466
- 9) ADDED PULL-UP TO TP_5V_POK.
- 10) UPDATED BELOW CAPS DNI AFTER POWER DC SIM RESULTS.
C597,C618,C1360,C1380,C1383,C1333,C1365,C1389,C1367,C1347
- 11) CONNECTED THE DDR4_TEN SIGNAL DIRECTLY TO GND
- 12) ADDED VTT TERMINATION 36 OHM TO DDR4_A3
- 13) UPDTAED QSFP CAGE AND CLIP TO [U95-L111-1001 AND U9011017060BP] FOR QSFP CONNECTORS
- 14) CONNECTED OE PIN OF SI5395, SI5395_1_A_OEN AND SI5395_2_OEN TO SYSTEM MAX10
- 15) UPDATED CLOCK PROGRAMMING DESIN FOR SI5518 AND SI5395 AS BELOW
UPDATED J31 SHOULDE BE USED FOR SI5518 SPI ONLY.
REMOVED R2661,R2662,R3267,R3268 RESISTORS.
CONNECTED R2661.1 TO R3267.2 ON PCB
CONNECTED R2662.1 TO R3268.2 ON PCB
J41 OR J140 SHOULD BE USED FOR CLK_I2C TO PROGRAM SI5391,SI5395_1)EU10),SI5395_2 (EU13).
REMOVED R2015,R3265,R3266.
REMOVED U150, U29 IC'S
- 16) ADDED DIP SWITCH FOR POWER MAX10.
- 17) R2626 RESISTOR IS UPDATED TO DNI.
- 18) R114 AND R55 RESISTORS IS UPDATED TO DNI.

Tue Aug 8 11:18:22 2023

DEPARTMENT

UNKNOWN

Intel Corporation

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P.O. BOX 58119
Santa Clara, CA 95052-8119

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CODE

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DOCUMENT NUMBER

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REV

2.0

SCALE:

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SHEET

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