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Agilex™ 7 FPGA I-Series Transceiver (6 × F-Tile) Development Kit User Guide

Contents

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1. Overview

Agilex™ 7 FPGA I-Series Transceiver (6 × F-Tile) Development Kit is a complete design environment that includes both hardware and software you need to develop Agilex 7 FPGA I-Series designs. The board provides a wide range of peripherals and memory interfaces to facilitate the development of Agilex 7 FPGA I-Series transceiver designs.

Table 1.   Ordering Information

Development Kit Version	Ordering Code	Device Part Number	Serial Number Identifier
Agilex 7 FPGA I-Series Transceiver Development Kit (Production1 6 × F-Tile)	DK-SI-AGI040EA	AGIC040R39A1E1VC	AGI91FT1000000
Agilex 7 FPGA I-Series Transceiver Development Kit (ES1 6 × F-Tile)	DK-SI-AGI040FES	AGIC040R39A2E2VR0	AGI91FT0000001

Figure 1.   Agilex 7 FPGA I-Series Transceiver Development Kit—Top View

Refer to the *Appendix A—Development Kit Components* section for more details about the components on the Agilex 7 FPGA I-Series Transceiver Development Kit.

Related Information

ISO 9001:2015 Registered

1.1. Block Diagram

Figure 2.   Agilex 7 FPGA I-Series Transceiver Development Kit Block Diagram

1.2. Feature Summary

- Agilex 7 I-Series FPGA, 4047 KLE, 3948A package
- F-Tile 1 (12A):
  — 16 FGT transceiver channels fan out to FPGA Mezzanine Card Plus (FMC+) connector
- F-Tile 2 (12B):
  — 4 FHT transceiver channels fan out to Quad Small Form Factor Pluggable Double Density 800 (QSFP-DD800) connector
  — 8 FGT transceiver channels to Quad Small Form Factor Pluggable Double Density (QSFP-DD) connector
  — 4 FGT Transceiver channels to Quad Small Form Factor Pluggable (QSFP) connector
- F-Tile 3 (12C):
  — 4 FHT transceiver channels fan out to QSFP-DD800 connector
  — 8 FGT transceiver channels to QSFP-DD connector
  — 4 FGT Transceiver channel to Small Form Factor (SFF) connector
  — 4 FGT transceiver to channels to QSFP connector
- F-Tile 4 (13A):
  — 4 FGT Transceiver to channels to QSFP connector
  — 8 FGT transceiver channels to QSFP-DD connector

- F-Tile 5 (13B):
  - 4 FGT Transceiver to channels to Mini Cool Edge IO (MCIO)
  - 8 FGT transceiver channels to QSFP-DD connector
  - 4 FHT transceiver channels fan out to Octal Small Form Factor Pluggable (OSFP) connector
- F-Tile 6 (13C):
  - 16 FGT channels to FMC+
  - 4 FHT transceiver channels fan out to OSFP connector
- SR DDR4 2666 MT/s (× 72 w/ECC), 16 GB.
- SR DDR4 2666 MT/s (× 72 w/ECC), 16 GB 1 DPC Dual In-line Memory Modules (DIMM) connector

Note: QSFP-DD400 and OSFP work up to 400 Gbps (50G x 8) PAM4 in DK-SI-AGI040FES. QSFP-DD800 and OSFP work up to 800 Gbps (100G x 8) PAM4 in DK-SI-AGI040EA.

1.3. Box Contents

- Agilex 7 FPGA I-Series Transceiver Development Kit
- Single-rank DDR4 DIMM module
- Quad Serial Peripheral Interface (QSPI) flash daughter card
- USB2.0 Type B cable
- 1 × 240 W power adapter and NA/EU/JP/UK cords

Related Information

Agilex 7 FPGA I-Series Transceiver (6 × F-Tile) Development Kit Website

1.4. Recommended Operating Conditions

Table 2.   Recommended Operating Conditions

Operating Condition	Range of Values
Ambient operating temperature range	0°C to 35 °C
ICC load current	50 A
ICC load transient percentage	269 A/uS
FPGA maximum power supported by active heat sink/fan	300 W

Related Information

Handling the Board on page 7

2. Getting Started

2.1. Before You Begin

You must check the kit contents and inspect the boards to verify that you received all of the items in the box before using the kit of installing the software.

In case any of the items are missing, you must contact Altera before you proceed.

Important: Read the Appendix C.1—Safety and Regulatory Information for safe operation and regulatory adherence.

2.2. Handling the Board

When handling the board, it is important to observe static discharge precautions.

Caution: Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

Caution: This development kit should not be operated in a vibration environment.

2.3. Software and Driver Installation

This section explains how to install the following software and driver:

- Quartus® Prime Pro Edition software
- Intel® SoC FPGA Embedded Development Suite (SoC EDS)
- Agilex 7 FPGA I-Series Transceiver Development Kit software
- Intel FPGA Download Cable II driver

2.3.1. Installing the Quartus Prime Pro Edition Software

1. Download the Quartus Prime Pro Edition software from the FPGA Software Download Center webpage of the Intel website.

2. Follow the on-screen instructions to complete the installation process. Choose an installation directory that is relative to the Quartus Prime Pro Edition software installation directory.

If you have difficulty installing the Quartus Prime software, refer to the *Intel FPGA Software Installation and Licensing*.

Related Information

- Quick-Start for Quartus Prime Pro Edition Software
- Quartus Prime Pro Edition User Guide: Getting Started
- Intel FPGA Software Installation and Licensing

2.3.2. Installing the Intel SoC EDS

The Intel SoC FPGA Embedded Development Suite (SoC EDS) is a comprehensive software tool suite for embedded software development on Altera® system-on-chip (SoC) devices. It contains development tools, utility programs, run-time software, and application examples to expedite firmware and application software of SoC embedded systems.

As a part of the Intel SoC EDS, the Arm* Development Studio 5 (DS-5) Intel SoC FPGA Edition Toolkit provides a comprehensive set of embedded development tools for Altera's SoC FPGAs.

For more information and steps to install the Intel SoC EDS Tool Suite, refer to the links below.

Related Information

- Intel SoC FPGA Embedded Development Suite (SoC EDS) User Guide
- Arm* Development Studio for Intel SoC FPGA

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2.3.3. Installing the Development Kit

1. Download the Agilex 7 FPGA I-Series Transceiver Development Kit installer package from the Agilex 7 FPGA I-Series Transceiver Development Kit webpage on the Intel website.

2. Unzip the Agilex 7 FPGA I-Series Transceiver Development Kit installer package. The package creates the directory structure shown in the figure below.

Figure 3.   Agilex 7 FPGA I-Series Transceiver Development Kit Directory Structure
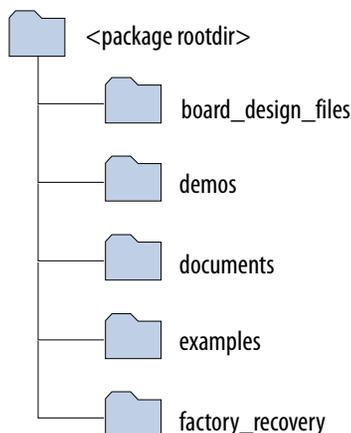
3. For the latest issues and release notes, Altera recommends that you review the `readme.txt` located in the root directory of the kit installation.

Table 3.   Installed Development Kit Directory Description

Lists the file directory names and a description of their contents.

Directory Name	Description of Directory Contents
board_design_files	Contains schematics, layout, assembly, and Bill of Material (BOM) board design files. Use these files as a starting point for a new prototype board design.
documents	Contains the development kit documentation.
examples	Contains the sample design files for the Agilex 7 FPGA I-Series Transceiver Development Kit: • QSPI image, system MAX® 10 image • Board Test System (BTS): BTS GUI, Clock GUI, and Power GUI • Golden Top project for pinout assignments management • Design Examples: Memory, XCVR, GPIO, and PCIe* 4.0
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

2.3.4. Installing the Intel FPGA Download Cable II Driver

The Agilex 7 FPGA I-Series Transceiver Development Kit includes onboard Intel FPGA Download Cable circuits for FPGA and system MAX 10 programming. However, for the host computer and board to communicate, you must install the Intel FPGA Download Cable driver on the host computer.

Installation instructions for the Intel FPGA Download Cable driver for your operating system are available on the Intel website.

On the Intel website, navigate to the *Cable and Adapter Drivers Information* link to locate the table entry for your configuration and click the link to access the instructions.

Related Information

- Cable and Adapter Drivers Information
- Intel FPGA Download Cable II User Guide

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3. Development Kit Setup

The instructions in this chapter explain how to setup the Agilex 7 FPGA I-Series Transceiver Development Kit for specific use cases.

3.1. Default Settings

The Agilex 7 FPGA I-Series Transceiver Development Kit ships with its board switches preconfigured to support the design examples in the kit. If you suspect that your board might not be correctly configured with the default settings, follow the instructions in the *Factory Default Switch Settings* table to return to its factory settings before proceeding ahead.

Note: "X" refers to Don't Care in the table below.

Table 4.   Factory Default Switch Settings

Switch	Default Position	Default Function
S19[1:4]	OFF/OFF/ON/ON	FPGA and system MAX 10 selected in the JTAG chain.
S20[1:4]	ON/ON/ON/ON	Mode 1: On-board Intel download circuit act as the only JTAG Master.
S9[1:4]	ON/OFF/OFF/X AS mode (default setting) OFF/ON/ON/X Avalon® streaming interface x8 mode	Agilex FPGA Mode Select pins. Default—JTAG
S10[1:4]	ON/ON/ON/ON	SYS_SW[0:3] SYS_SW[0]—Factory Load • '0': Load image from Page 0 of the QSPI.
S15[1:4]	ON/ON/ON/OFF	SYS_SW[4:7] • SYS_SW[4]—X • SYS_SW[5]—FMC-A PCIe RP/EP Select. — "0": RP (Default) — "1": EP • SYS_SW[6]—FMC-B PCIex RP/EP Select — "0": RP (Default) — "1": EP • SYS_SW[7]—Not used — "0": RP — "1": EP (Default)
S1[1:4] S6[1:4]	OFF/OFF/OFF/OFF OFF/OFF/OFF/OFF	User Switch [0:3] User Switch [4:7]
S22[1:4]	ON/ON/ON/ON	MUX_DIP_SW[0:3]

continued...

Switch	Default Position	Default Function
		Mapped as follows: • MUX_DIP_SW0 --> MUX_SEL0 • MUX_DIP_SW1 --> MUX_SEL1 • MUX_DIP_SW2 --> MCIO_CLK_SEL_EP_N; RP • MUX_DIP_SW3 --> MCIO_CLK_ENN
S7	OFF	Board power supply
S4	ON/ON/ON/ON	Future development

3.2. Powering Up the Development Kit

1. Use the provided 240 W power adapter to supply power through **J30**.

2. Connect extra 240 W adapter to **J55** only when you require more than 240 W during high use case applications.

3. After power adapter is plugged into **J30**, set the power switch **S7** to the ON position.

When the board powers up, the LED **D22** illuminates, which indicates that the board power up is successful. If the LED **D22** is not turned on, it indicates that one or more power supply is incorrect.

3.3. Performing Board Restore

This development kit ships with GPIO design examples stored in the QSPI flash device and system MAX 10 pre-programmed.

You must perform board restore by using the restore menu under the BTS GUI or using the following instructions through the Quartus Prime Programmer GUI.

3.3.1. Restoring Board System MAX 10 with Default Factory Image

1. Start the Quartus Prime Programmer GUI, and click **Auto Detect** to detect JTAG chain after the system MAX 10 is restored.

2. Attach the system MAX 10 image on the system MAX 10 part.

3. Select programming options and click **Program** button.

Note: Once you plug Intel FPGA Download Cable between **J11** and PC, the on-board Intel FPGA Download Cable circuit is disabled automatically.

3.3.2. Restoring Board QSPI Flash with the Default Factory Image

1. Plug the QSPI flash card into the **J3** slot.

2. Ensure that `MSEL[2:0]` are [ON/ON/OFF] (Avalon streaming interface x8 configuration mode) before powering up the board.

3. Start the Quartus Prime Programmer GUI, and click **Auto Detect** to detect the JTAG chain after the system MAX 10 is restored.

4. Attach the Avalon streaming interface x8 image (BTS/image/ES (PRD)/QSPI folder) on the QSPI flash, which is under the system MAX 10 part.

5. Select programming options and click **Program** button.

Note: The QSPI flash is pre-programmed with GPIO image. It is overwritten by the Avalon streaming interface x8 image after the steps above.
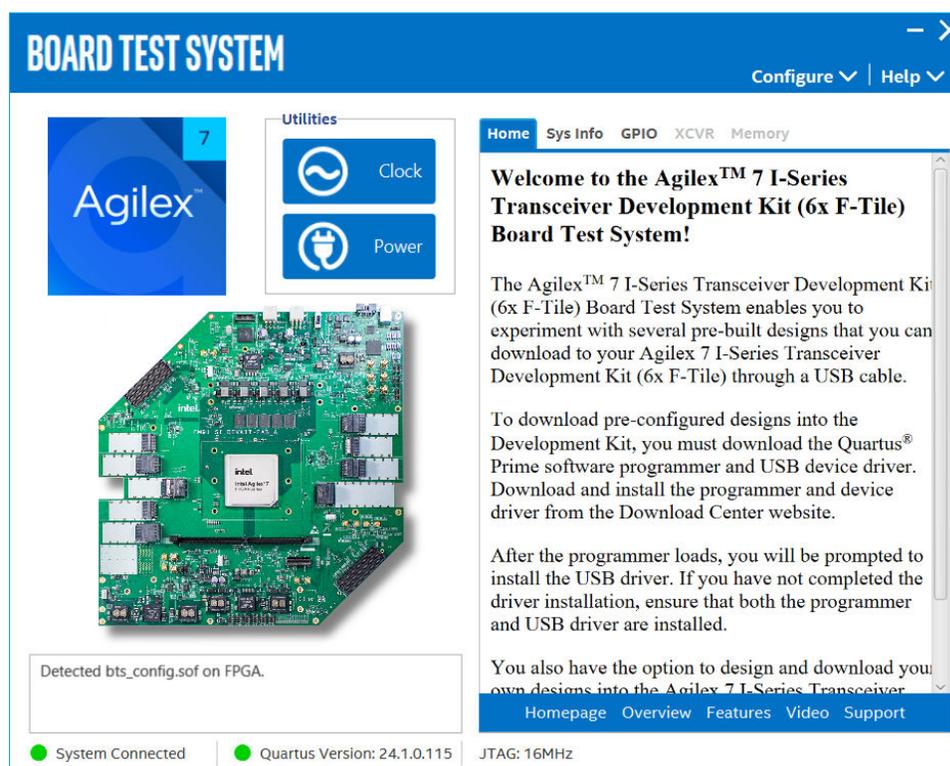
4. Board Test System

The Agilex 7 FPGA I-Series Transceiver (6 × F-Tile) Development Kit includes design examples and the board test system (BTS) GUI to test the functionality of this board. The BTS provides an easy-to-use interface to alter functional settings and observe results. You can use the BTS to test board components, modify functional parameters, observe performance, and measure power usage.

While using the BTS, you reconfigure the FPGA several times with test designs specific to the functionality that you are testing. The BTS is also useful as a reference for designing systems. The BTS communicates over the JTAG bus to a test design running in the Agilex 7 FPGA I-Series Transceiver (6 × F-Tile) device.

The BTS checks for hardware faults before you can use the board. If one or more BTS test items fail, it implies either a wrong hardware setting or hardware fault on specific interface.

The following figure shows the GUI of a board that is in factory configuration.

Figure 4. **BTS GUI**

4.1. Setting Up the BTS GUI Running Environment

To run BTS GUI, including the Power Monitor and Clock Controller GUI, you must download and install Java runtime including OpenJDK and OpenJFX on your systems and set up the running environment. This is a one-time procedure, so if you have already completed it before, you do not need to do it again unless the Java version upgrade is required.

4.1.1. Downloading OpenJDK

1. Download the Temurin* OpenJDK. Refer to the related information for the download link.
2. Select Architecture x64, Package Type JRE, and Version 11.
   a. For the **Windows** system, choose the `JRE.zip` format file.
   b. For the **Linux** system, choose the `JRE.tar.gz` format file.

Related Information

Temurin* OpenJDK

4.1.2. Downloading OpenJFX

1. Download the Gluon* OpenJFX. Refer to the related information for the download link.
2. Select JavaFX version 17.0.2.
   a. For the **Windows** system, download the JavaFX Windows x64 SDK.
   b. For the **Linux** system, download the JavaFX Linux x64 SDK.

Related Information

Gluon* OpenJFX

4.1.3. Installing OpenJDK and OpenJFX

You have two downloaded compressed files. Follow these steps to install them.

1. On **Windows** system, Altera recommends you to unzip the files and put them in the following directory:
   - `C:\Program Files\Java\jre`
   - `C:\Program Files\Java\jfx`

Note: The unzipped folder name of JRE is `jdk-11.0.xx+x-jre` (for example, `jdk-11.0.14+9-jre`), and you must rename it to `jre`. The unzipped folder name of JFX is `javafx-sdk-17.0.2`, and you must rename it to `jfx`.

2. On **Linux** system, Altera recommends you to unzip the files and rename the folders using the following commands:

```
# unzip openjfx-17.0.2_linux-x64_bin-sdk.zip -d /opt/Java/
# tar zxvf OpenJDK11U-jre_x64_linux_hotspot_11.0.14_9.tar.gz -C /opt/Java/
# cd /opt/Java
# mv javafx-sdk-17.0.2 jfx
# mv jdk-11.0.14+9-jre jre
```

You have the following two directories on your **Linux** system:

- `/opt/Java/jre`
- `/opt/Java/jfx`

4.1.4. Setting Up the Quartus Prime Software for BTS Operation

You must install the Quartus Prime software to support the silicon on the development kit. The recommended version is located in the `README.txt` file in the `examples\board_test_system` directory. If you choose to install individual files, you must install Agilex 7 Device Support.

The BTS communicates over JTAG to a test design running in the FPGA. The BTS shares the JTAG with other applications such as the Nios® II JTAG Debug Module and the Signal Tap Logic Analyzer. Altera recommends closing other applications before using BTS, as the GUI is designed based on the Quartus Prime software.

The BTS relies on the Quartus Prime software's specific library. Before running the BTS, open the Quartus Prime software to automatically set the environment variable `QUARTUS_ROOTDIR`. You can also change it through **Environment Variables** in the **System Properties** in Windows*. The BTS uses this environment variable to locate the Quartus Prime library.

Related Information

4.1.5. Running the BTS GUI

With the power to the board off, follow these steps:

1. Connect the USB cable to your PC and the board.
2. Check the development board switches and jumpers are set according to your preferences. Refer to Development Kit Setup. In most cases, BTS requires system MAX 10 and Agilex 7 FPGA on the JTAG chain.
3. Check the external modules status: SFP/QSFP/OSFP/QSFPDD/QSFPDD800/FMC/DIMM.
4. Turn on the board power switch.

Note: To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. You must attach the USB cable and power on the board for BTS to run correctly.

Navigate to the `<packagedir>\examples\board_test_system` directory to run BTS. The BTS release folder always includes the following files.

Figure 5.   BTS Folder
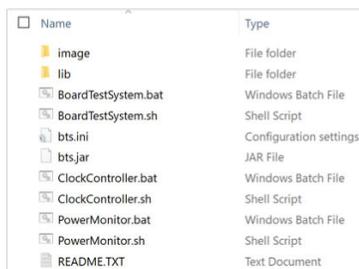
You can run BTS GUI easily with the following scripts.

1. On **Windows** system, double click the `.bat` files to run BTS, Clock Controller, or Power Monitor GUI.

Figure 6.   Windows Console
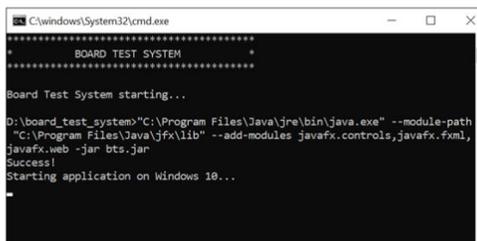
2. On **Linux** system, you need to run the shell script with root privilege.

Figure 7.   Linux Console
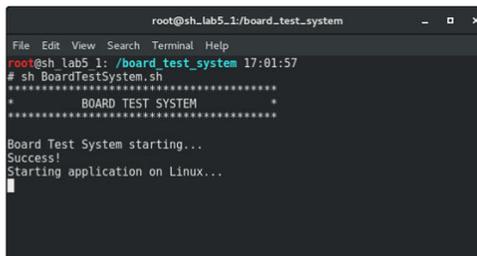
Note: The `.bat` or shell script checks the Java environment settings, copies necessary files, and gives some prompts if the environment is not set up correctly.

The GUI displays the application tab corresponding to the design running in the FPGA. If the design loaded in the FPGA is not supported, it prompts a message to configure your board with a valid BTS design. Refer to The Configure Menu.

4.2. BTS Functionalities

This section describes each control in the BTS.

4.2.1. The Bottom Info Bar

The bottom information bar shows the status of the system connection, the Quartus Prime version and the JTAG clock.

- **System Connected/Disconnected**: Shows if the board is connected to the system. The green sign turns gray if the board becomes disconnected.

- **Quartus Prime Version**: Displays the current Quartus Prime version installed and active on your system. The text turns red if your version is older than the required version. Change the QUARTUS_ROOTDIR environment variable to the required version.

- **JTAG**: Displays the JTAG clock frequency.

4.2.2. The Configure Menu

Use the **Configure** menu to select the design you want to use. Each design example tests different functionality that corresponds to one or more application tabs.

Figure 8.   The Configure Menu

Send Feedback
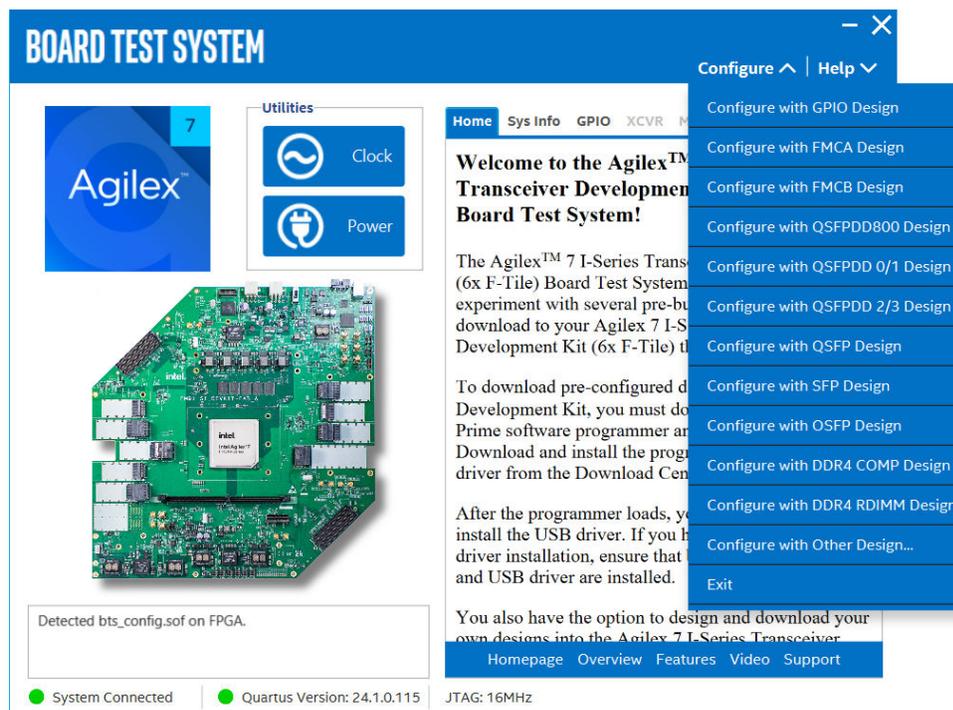
To configure the FPGA with a test system design, follow these steps:

1. On the **Configure** menu, click the **Configure** command that corresponds to the functionality you want to test.

2. In the dialog box that appears, click **Configure** to download the corresponding design's SRAM Object File (`.sof`) to the FPGA. The download process usually takes less than a minute.

When configuration is completed, the design begins running in the FPGA. The corresponding GUI application tabs that interface with the design is now enabled. If you use the Quartus Prime Programmer for configuration, instead of the BTS GUI, you might need to restart the GUI.

4.2.3. The Sys Info Tab

The **Sys Info** tab shows information about the board's current configuration. The tab displays the board information, JTAG Chain devices and other details stored on the board.

Figure 9. **The Sys Info Tab**
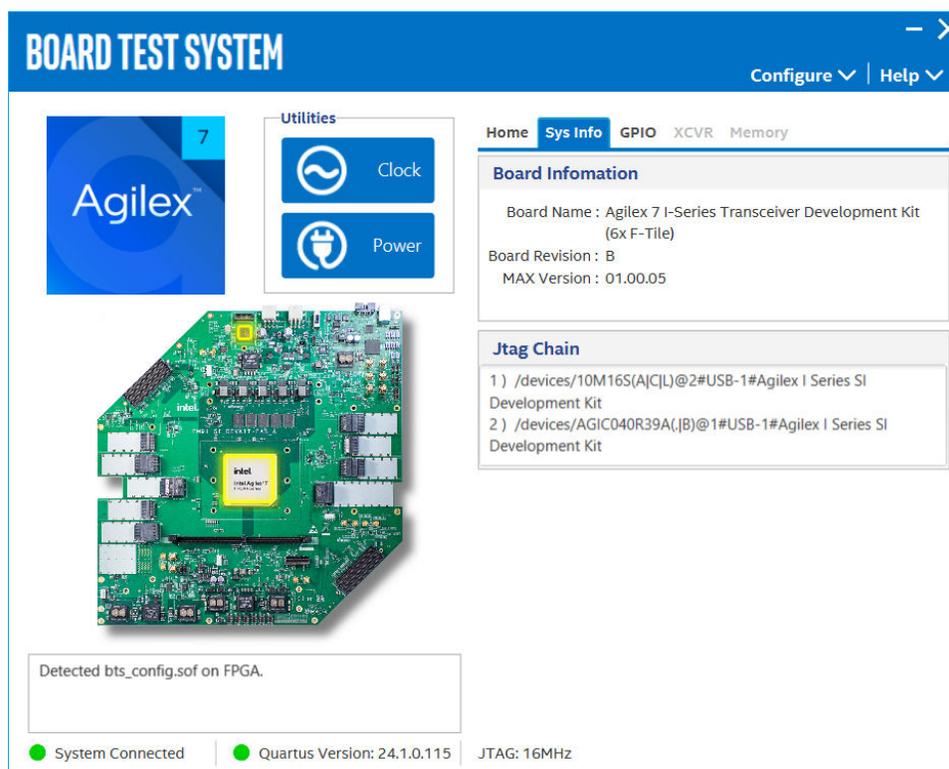
The following sections describe the controls on the **Sys Info** tab.

Board Information

The board information control displays static information about your board.

- **Board Name**: Indicates the official name of the board given by the BTS.
- **Board Revision**: Indicates the revision of the board.
- **MAX Version**: Indicates the version of the system MAX 10.

JTAG Chain

The JTAG chain control shows all the devices currently in the JTAG chain.

Note: You should place the system MAX 10 and FPGA in the JTAG chain when running the BTS GUI.

4.2.4. The GPIO Tab

The **GPIO** tab allows you to interact with all the general-purpose user I/O components on your board. You can turn LEDs on or off and see the status of push buttons and DIP switches.

Figure 10.   The GPIO Tab
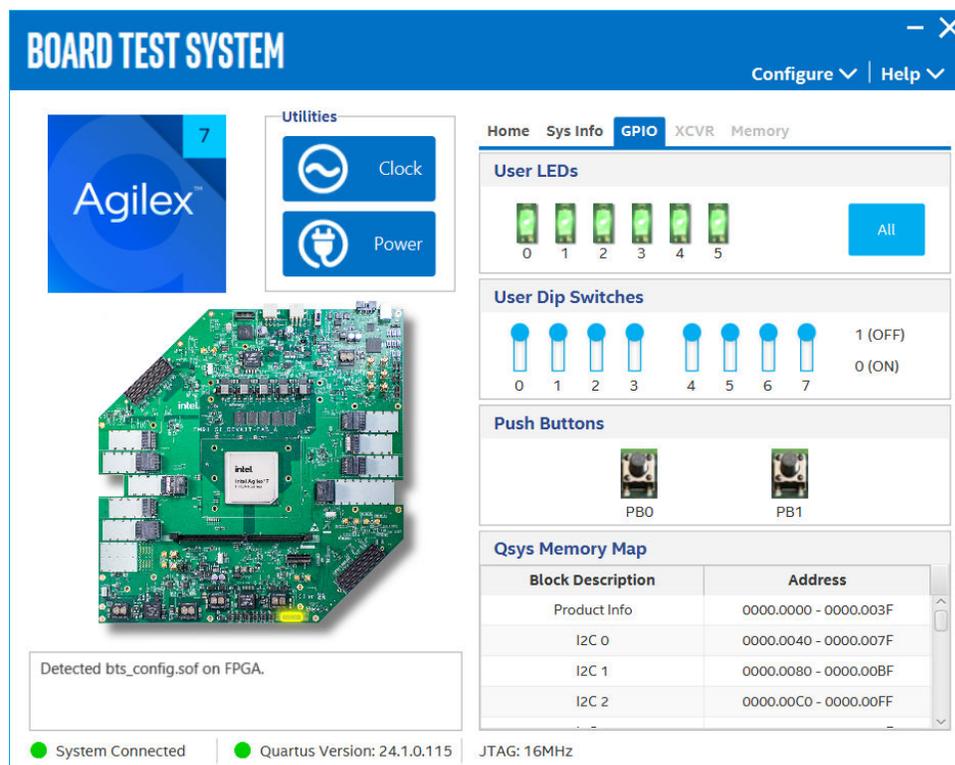
The following sections describe the controls on the **GPIO** tab.

User LEDs

The **User LEDs** control displays the current state of the user LEDs. Toggle the LED buttons to turn the board LEDs on and off. Click the All button to reverse the state of all the LEDs.

User Dip Switches

The **User Dip Switches** control display the status of the USER_SW[0:3] (S1) and USER_SW[4:7] (S6).

Push Buttons

The **Push Buttons** control shows the status of PB0 (S2) and PB1 (S3).

Qsys Memory Map

The **Qsys Memory Map** control shows the memory map of `bts_config.sof` design running on your board.

4.2.5. The XCVR Tab

The **XCVR** tab allows you to run transceiver tests on your board. You can run the test using either electrical loopback modules or optical fiber modules.

4.2.5.1. The QSFPDD NRZ Tab

Figure 11.   The QSFPDD-01 NRZ Tab
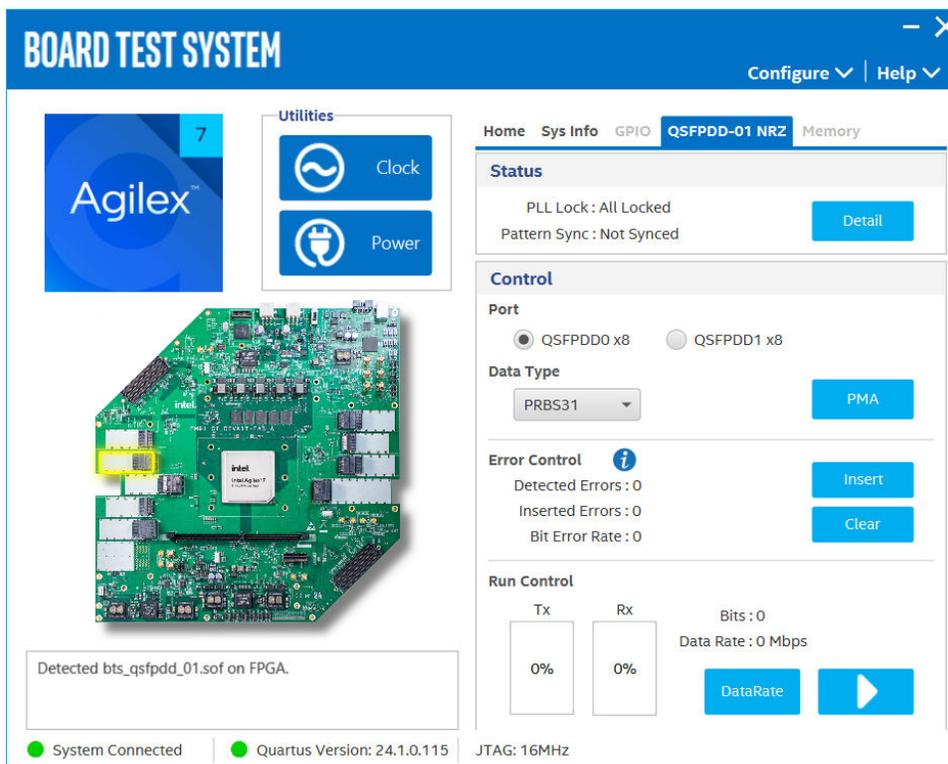
Figure 12. **The QSFPDD-23 NRZ Tab**
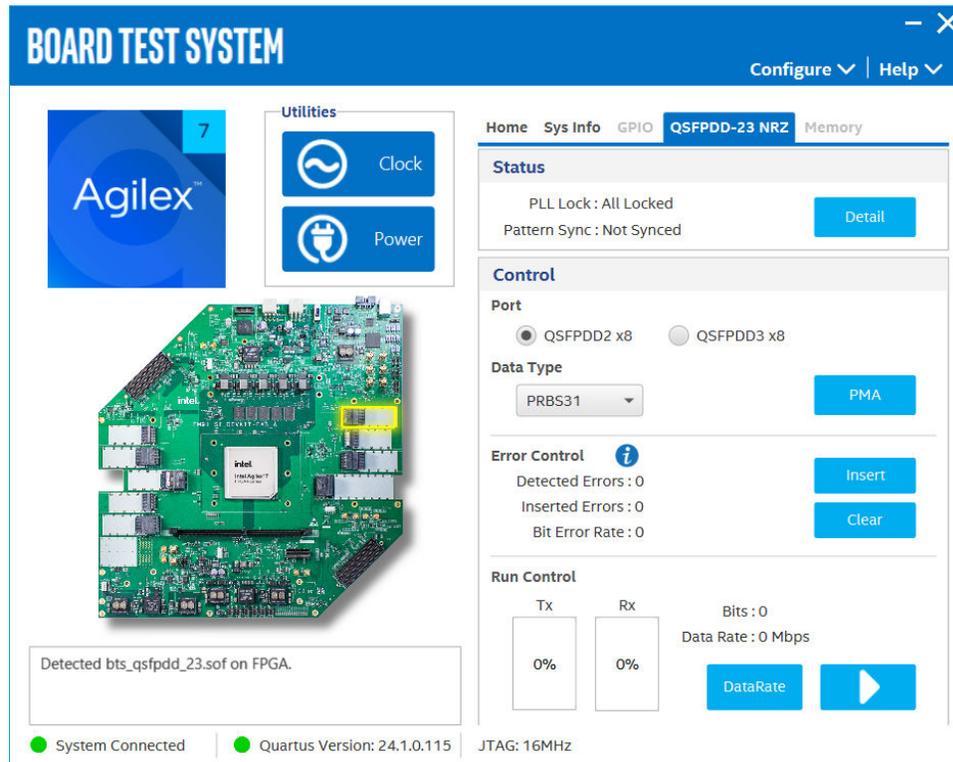
The following sections describe controls in the **QSFPDD NRZ** tab.

Status

The **Status** control displays the following status information during the loopback test:

- **PLL Lock**: Shows the PLL locked or unlocked state.
- **Pattern Sync**: Shows the pattern synced or not state. The pattern is considered synced when the start of the data sequence is detected.
- **Detail**: Shows the PLL lock and pattern sync status of each channel. The number of the error bits of each channel can be found here.

Figure 13. **QSFPDD NRZ—PLL and Pattern Status**

Control

Use the following controls to select an interface to apply PMA settings, data type, and error control:

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- **QSFPDD0 x8**
- **QSFPDD1 x8**
- **QSFPDD2 x8**
- **QSFPDD3 x8**

PMA Setting

The **PMA Setting** control allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback**: Displays the signal status between the transmitter and the receiver.
- **VOD**: Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap**:
  - Pre-tap 1: Specifies the amount of pre-emphasis on the first pre-tap of the transmitter buffer.
  - Pre-tap 2: Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
  - Post-tap 1: Specifies the amount of pre-emphasis on the post-tap of the transmitter buffer.

Figure 14.   QSFPDD NRZ-PMA Setting
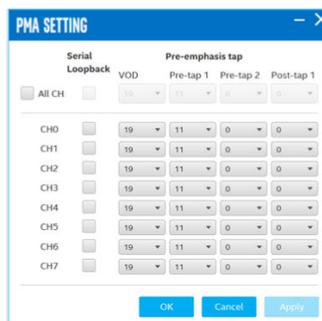
Data Type

The **Data Type** control specifies the type of data pattern contained in the transactions. Select the following available data types for analysis:

- **PRBS7**: Pseudo-random 7-bit binary sequences
- **PRBS15**: Pseudo-random 15-bit binary sequences
- **PRBS23**: Pseudo-random 23-bit binary sequences
- **PRBS31**: Pseudo-random 31-bit binary sequences (default)

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors**: Displays the number of data errors detected in the received bit stream.
- **Inserted Errors**: Displays the number of errors inserted into the transmit data stream.
- **Bit Error Rate**: Calculates the bit error rate of the transmit data stream.
- **Insert**: Insert a one-word error into the transmit data stream each time you click the button. **Insert** is only enabled during transaction performance analysis.
- **Clear**: Resets the **Detected Errors** counter and **Inserted Errors** counter to zeros.

Run Control

- **TX and RX performance bars**: Show the percentage of maximum theoretical data rate that the requested transactions can achieve.
- **Start**: This control initiates the loopback tests.
- **Data Rate**: Displays the XCVR type and data rate of each channel.

Figure 15.   QSFPDD NRZ—Data Rate

Channel	XCVR Type	Frequency
0	F-Tile FGT	22.72211 Gbps
1	F-Tile FGT	22.72205 Gbps
2	F-Tile FGT	22.72211 Gbps
3	F-Tile FGT	22.72211 Gbps
4	F-Tile FGT	22.72205 Gbps
5	F-Tile FGT	22.72211 Gbps
6	F-Tile FGT	22.72211 Gbps
7	F-Tile FGT	22.72205 Gbps

4.2.5.2. The FMCA NRZ Tab

Similar control functions with the **QSFPDD NRZ** tab except for the port selection.

Figure 16.   The FMCA NRZ Tab
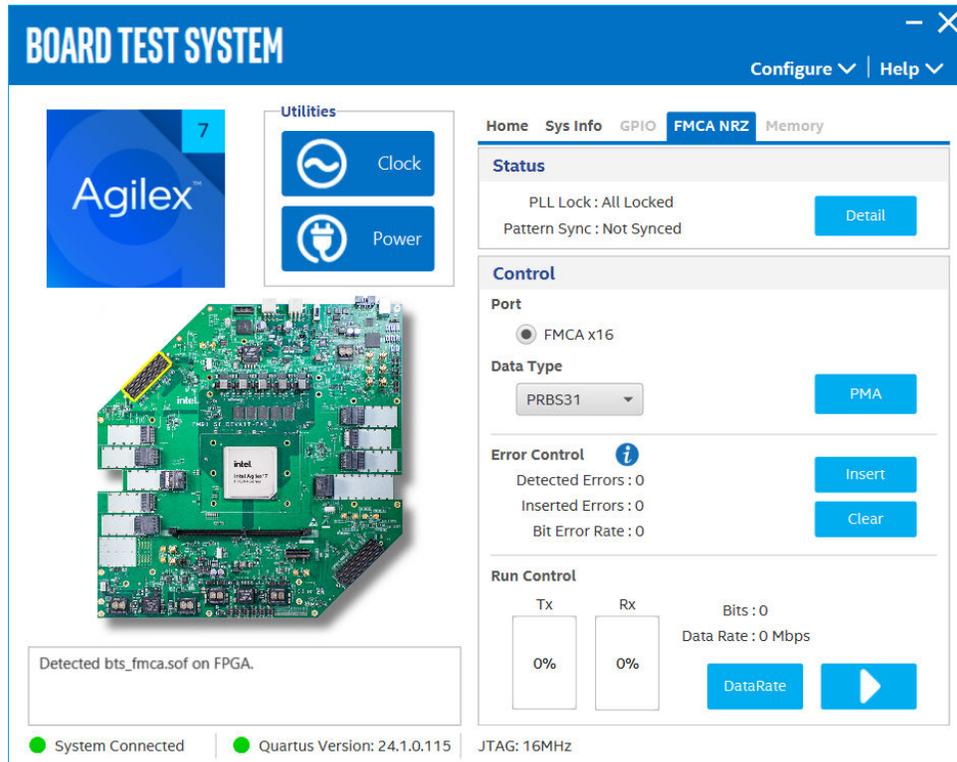
4.2.5.3. The FMCB NRZ Tab

Similar control functions with the **QSFPDD NRZ** tab except for the port selection.

Figure 17.   The FMCB NRZ Tab
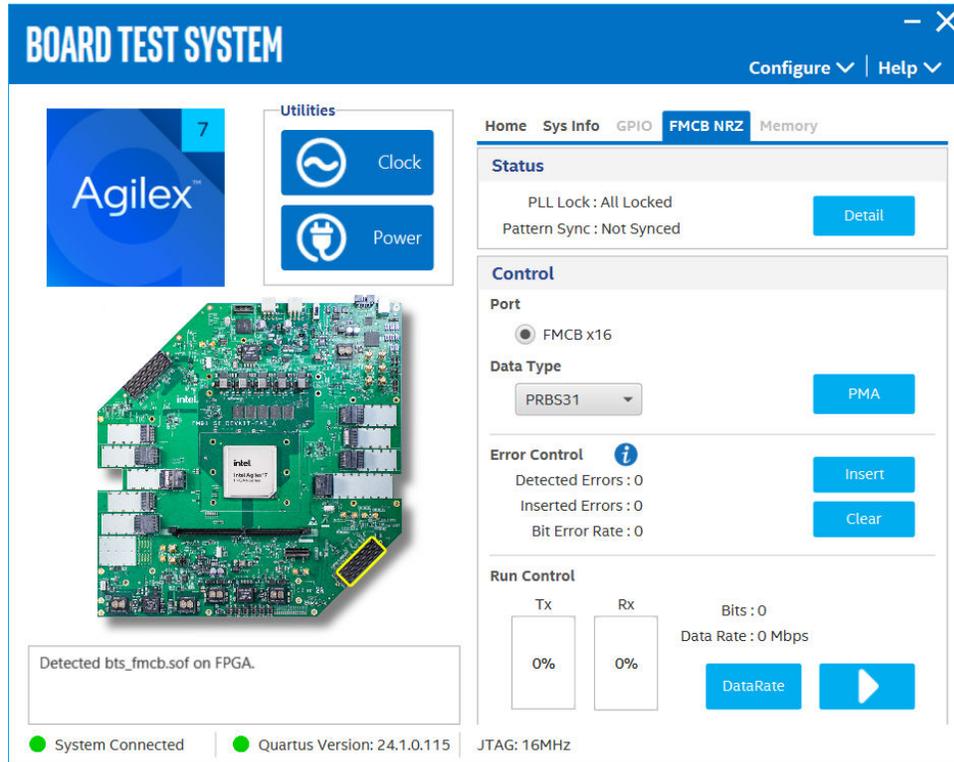
4.2.5.4. The QSFPDD400/QSFPDD800 PAM4 Tab

Similar control functions with the **QSFPDD NRZ** tab except for the port selection. DK-SI-AGI040FES has QSFP-DD400 PAM4, while DK-SI-AGI040EA has QSFP-DD800 PAM4.

Figure 18.   The QSFPDD400/QSFPDD800 PAM4 Tab
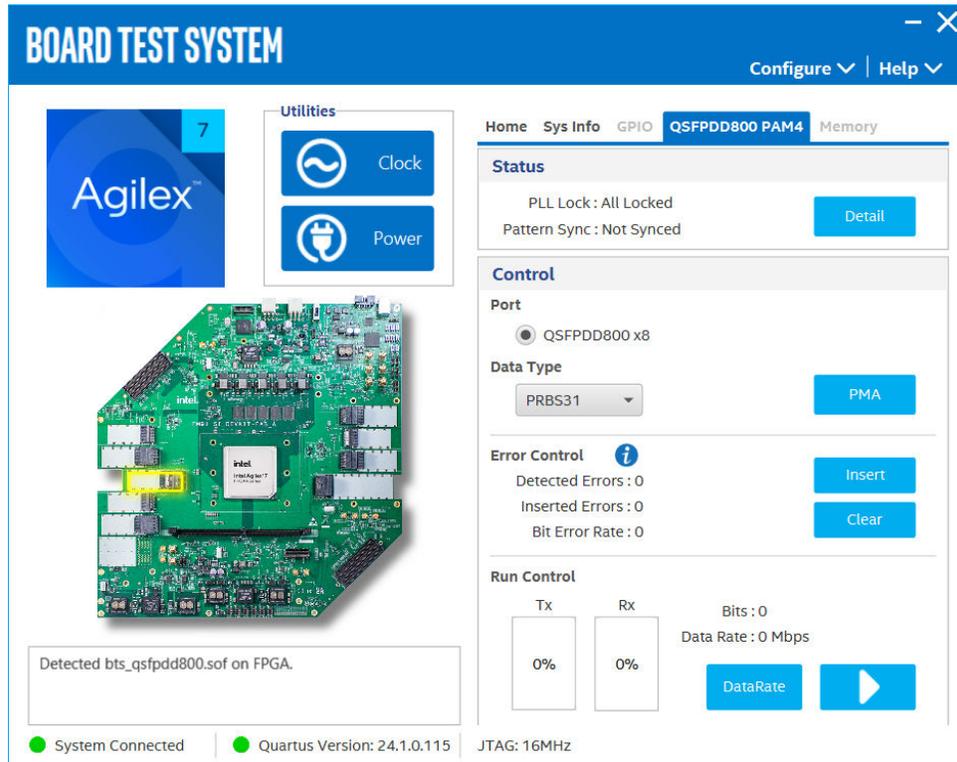
4.2.5.5. The QSFP NRZ Tab

Similar control functions with the **QSFPDD NRZ** tab except for the port selection.

Figure 19.   The QSFP NRZ Tab

Send Feedback
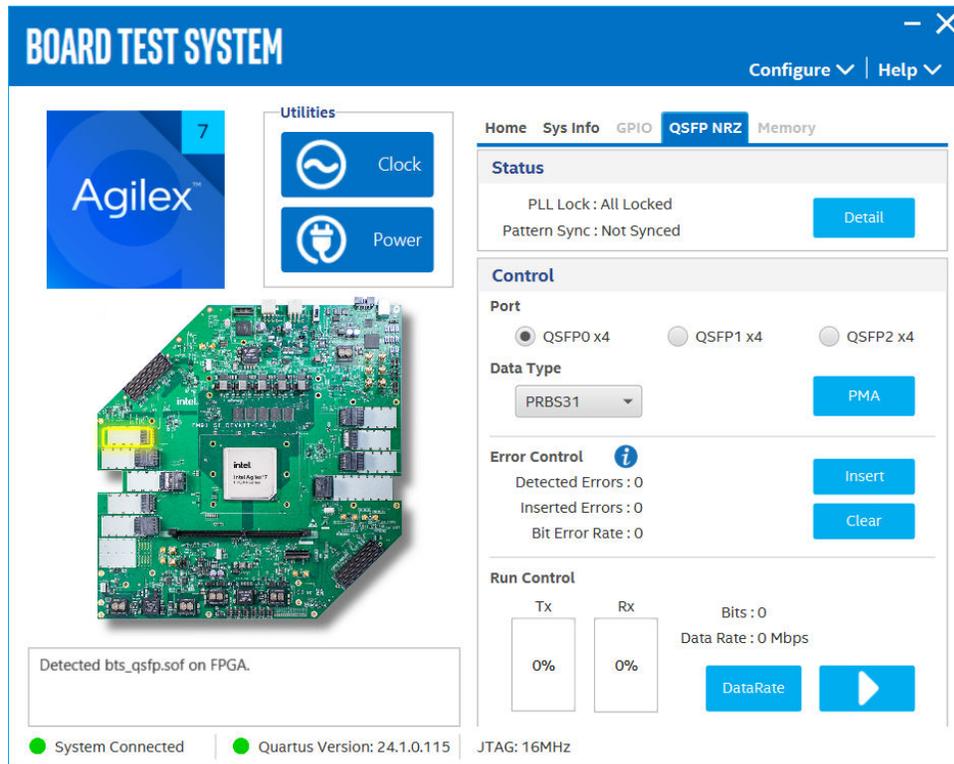
4.2.5.6. The SFP Tab

Similar control functions with the **QSFPDD NRZ** tab.

Figure 20.   The SFP Tab
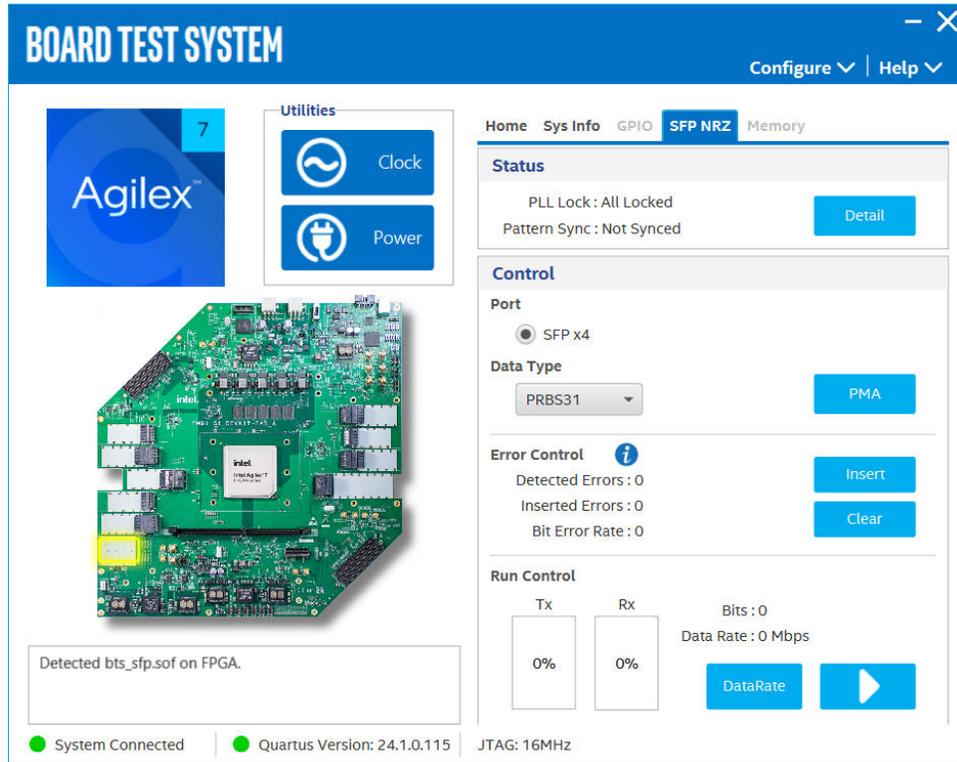
4.2.5.7. The OSFP Tab

Similar control functions with the **QSFPDD NRZ** tab.

Figure 21.   The OSFP Tab
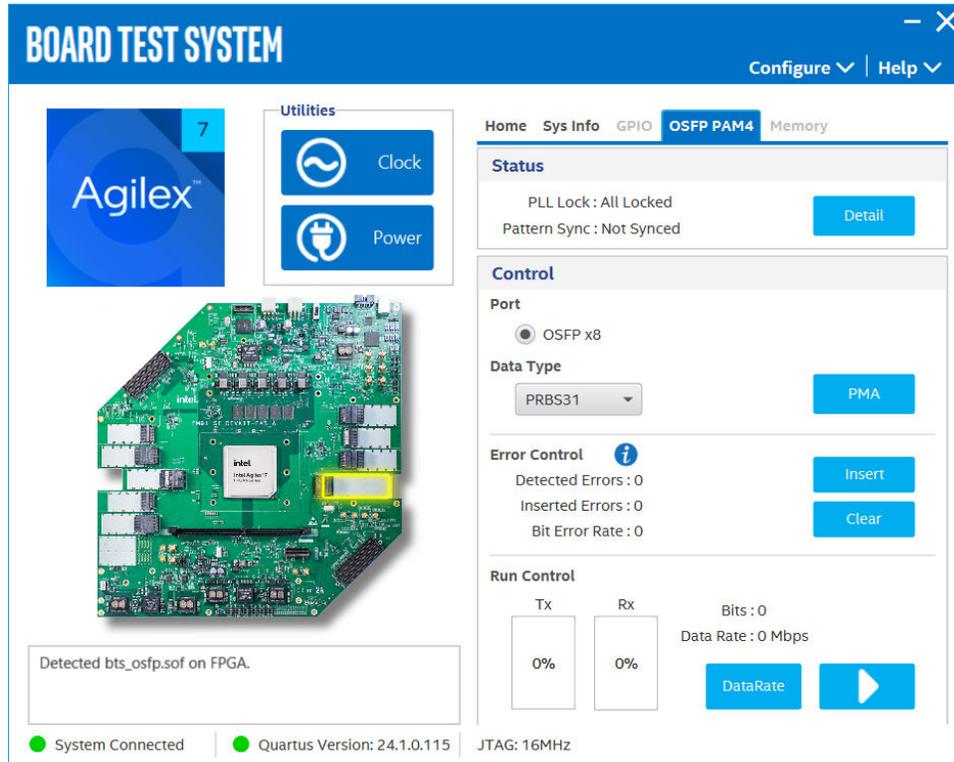
4.2.6. The Memory Tab

This tab allows you to read and write DDR4-COMP and DDR4-RDIMM memory on your board. Download the design through the BTS **Configure** menu.

Figure 22.   The COMP Tab
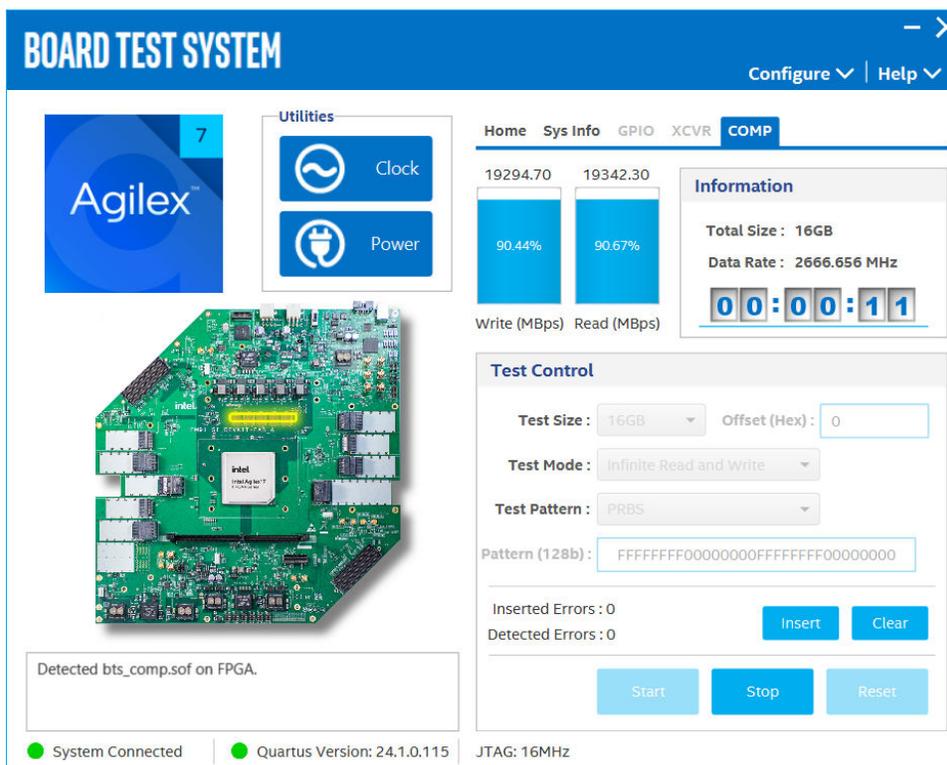
The following sections describe controls on this tab.

Start

Initiates DDR4 memory transaction performance analysis.

Stop

Terminates transaction performance analysis.

Reset

Resets transaction performance analysis.

Performance Indicators

These controls display current transaction performance analysis information collected since you last clicked **Start**:

• **Write and Read performance bars**: Show the percentage of maximum theoretical data rate that the requested transactions can achieve.

• **Write (MBps) and Read (MBps)**: Show the number of bytes analyzed per second.

• **Data Bus**: 72 bits (8 bits ECC) wide, reference clock is 166.666 MHz, and the frequency is 1333.33 MHz double data rate 2666.66 MT/s.

Test Control

• **Test Size**: You can choose the size of the memory to test. The available options are 64 KB, 256 KB, 1 MB, 16 MB, 64 MB, 256 MB, 1 GB, 4 GB, 8 GB, and 16GB (default).

• **Offset (Hex)**: You can define the memory start address to test.

• **Test Mode**: Infinite Read and Write (default), Single Read and Write.

• **Test Pattern**: PRBS (default), User Defined Constant, Walking '0', Walking '1'.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

• **Detected Errors**: Displays the number of data errors detected in the hardware.

• **Inserted Errors**: Displays the number of errors inserted into the transaction stream.

• **Insert**: Insert a one-word error into the transaction stream each time you click the button. Insert error is only enabled during transaction performance analysis.

• **Clear**: Resets the Detected Errors counter and Inserted Errors counter to zeros.

Figure 23.   The RDIMM Tab

Same with DDR4-COMP.
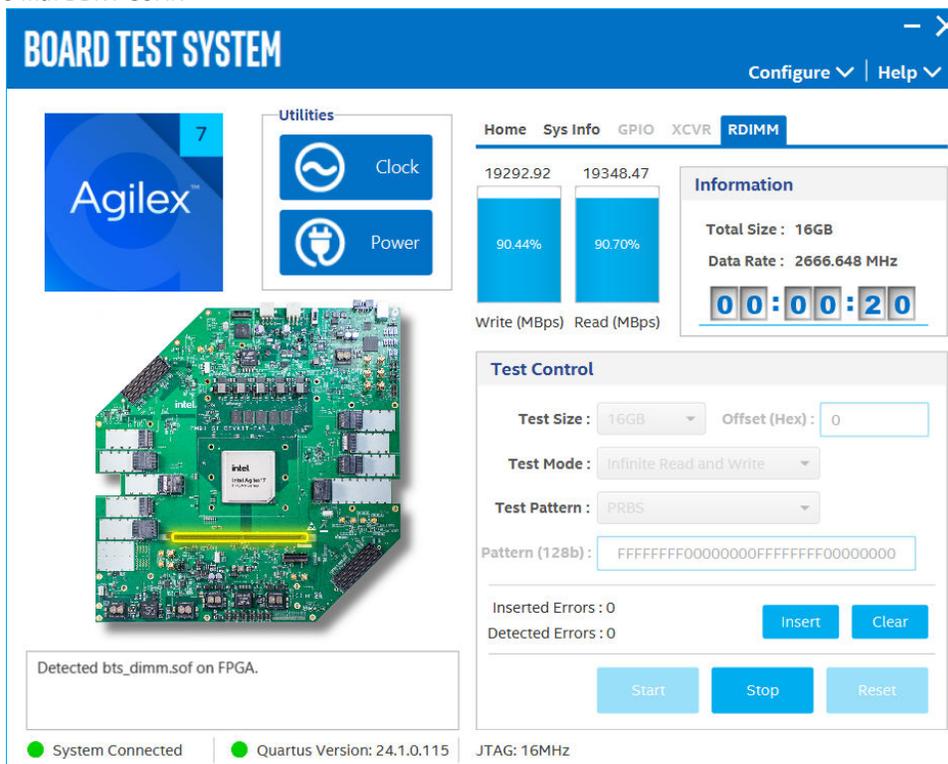
4.3. Control On-Board Clock through Clock Controller GUI

The Clock Controller GUI can change the on-board Si5391/Si5395-1/Si5395-2/Si5518. The instructions to run Clock Controller GUI are stated in the Running the BTS GUI on page 16. Alternatively, you can start using the Clock Controller feature by selecting the **Clock** icon on the BTS GUI.

The Clock Controller communicates with the system MAX 10 device through a 10-pin JTAG header J11 or USB port J10. Then, system MAX 10 controls these programmable clock parts through a 2-wire I^{2}C bus.

Note: You cannot run the stand-alone Clock Controller GUI application when the BTS or Power Monitor GUI is running at the same time. Si5518 can be controlled only when a design in which the SPI interface is instantiated, such as the `bts_config.sof` under the `board_test_system\image\ES folder` has been downloaded to the FPGA.

Figure 24.   Si5391
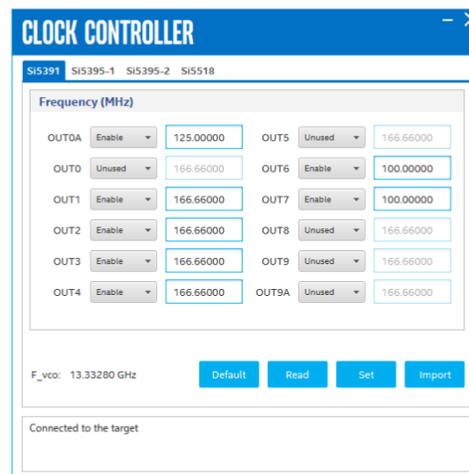
The following sections describe the Clock Controller buttons.

Read

Reads the current frequency setting for the oscillator associated with the active tab.

Default

Sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.

Set

Sets the programmable oscillator frequency for the selected clock to the value in the `OUTx` output controls for Si5391. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Altera recommends resetting the FPGA logic after changing frequencies.

Import

Si5391 has a two-time rewritable non-volatile memory (NVM). You can generate the register list from the Skyworks* ClockBuilder Pro tool and import it into Si5391 to update the settings of the RAM. Register changes are volatile after power cycling.

Figure 25.   Si5395-1

Similar control functions with Si5391.
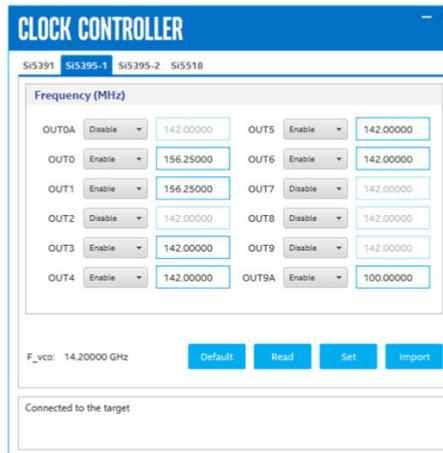
Figure 26.   Si5395-2

Same with Si5395-1.

Figure 27. Si5518
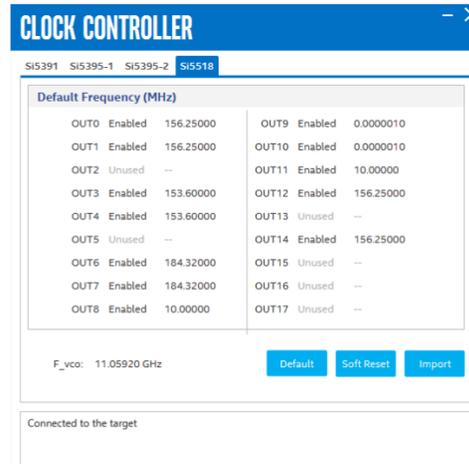
Import

You can generate the register list from the ClockBuilder Pro tool and import it into Si5518 to update the settings of RAM. Register changes are volatile after power cycling.

Default

Sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.

Soft Reset

Initiates a global soft reset. The global soft reset does not download the firmware and frequency plan from NVM. Instead, it restarts the firmware and frequency plan that are currently running on the device. The device acts like it has been rebooted.

Related Information

Skyworks Solution
    More information about the Clockbuilder Pro software.

4.4. Monitor On-Board Power Regulator through Power Monitor GUI

The Power Monitor GUI reports most power rails' voltage, current, and power information on the board. It also collects temperature from FPGA die, power modules, and diodes assembled on PCB.

The Power Monitor GUI communicates with the system MAX 10 through a 10-pin JTAG header (J11) or USB port (J10). System MAX 10 monitors and controls power regulator, temperature/voltage/current sensing chips through a 2-wire I^{2}C bus.

The instructions to run Power Monitor GUI are stated in the Running the BTS GUI on page 16. Alternatively, you can start using the Power Monitor feature by selecting the **Power** icon on the BTS GUI.

Note: You cannot run the stand-alone Power Monitor GUI when the BTS or the Clock Controller GUI is running at the same time.

Figure 28.   Power Monitor GUI—The Power Tab
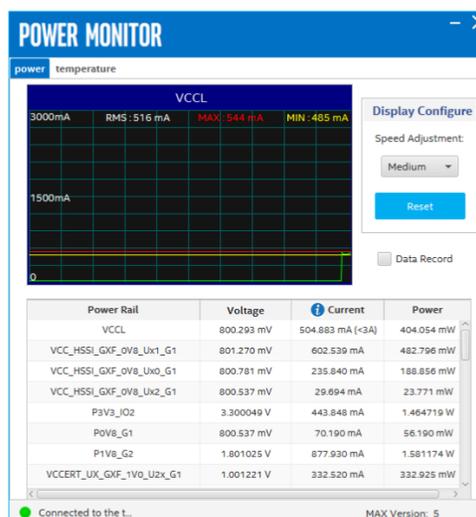
The following sections describe the details of the Power Monitor GUI.

Display Configure

- **Speed Adjustment**: Adjusts the update rate of the current curve.
- **Reset**: Regenerates the graph.

Data Record

When the box is checked, the telemetry data of the selected power rail can be recorded. It saves the data into a `.csv` file in the `log` directory.

Figure 29.   Power Monitor GUI—The Temperature Tab
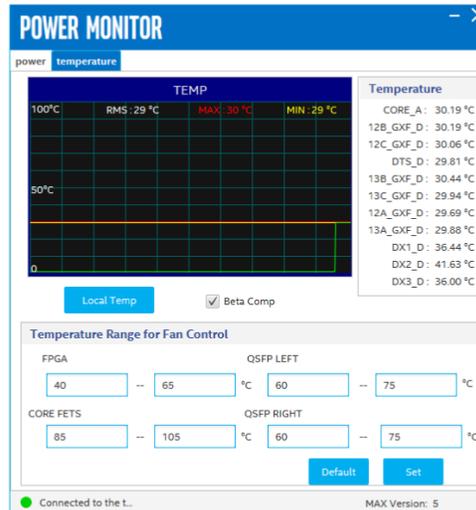
Temperature

Reads the temperature data from temperature sense diodes inside the FPGA die or assembled on PCB.

Local Temp

Shows the temperature comparison of local and remote temperature sensors.

Beta Comp

Enables beta compensation for temperature sensing chips.

Temperature Range for Fan Control

Sets and displays the temperature range for fan control. This part information is store in the first 8 bytes of EEPROM (U114). Pay attention to not overwrite it.

4.5. Identify Test Pass or Fail-based on BTS GUI Test Status

QSFPDD0/QSFPDD1/ QSFPDD2/QSFPDD3

Plug QSFPDD0/QSFPDD1/QSFPDD2/QSFPDD3 loopback module in **J27/J48/J69/J67** before you configure QSFPDD NRZ example build through BTS GUI.

QSFPDD800

Plug QSFPDD800 loopback module in **J22** before you configure QSFPDD800 PAM4 example build through BTS GUI.

FMCA/FMCB

Plug FMCA/FMCB loopback module in **J7/J9** before you configure FMCA/FMCB NRZ example build through BTS GUI.

QSFP

Plug QSFP loopback module in **J57**/**J58**/**J66** before you configure QSFP NRZ example build through BTS GUI.

OSFP

Plug OSFP loopback module in **J45** before you configure OSFP NRZ example build through BTS GUI.

SFP

Plug four SFP loopback modules in **J77** before you configure SFP NRZ example build through BTS GUI.

DDR4 DIMM

Plug the DIMM module which is shipped alone with this development kit in **J5**.

5. Development Kit Hardware and Configuration

The Agilex 7 FPGA I-Series Transceiver (6 × F-Tile) Development Kit can support multiple application scenarios and configuration modes. You need to either change the hardware setting, re-program the system images, or both, for these cases.

Table 5.   Supported Configuration Modes

S9 [1:4]	MSEL [2:0]	Configuration Mode
ON/OFF/OFF/X	001	AS – Fast mode (default setting)
ON/ON/OFF/X	011	AS – Normal mode
ON/ON/ON/X	111	JTAG
OFF/ON/ON/X	110	Avalon streaming x8

5.1. Configuring the FPGA Device by Active Serial (AS) Modes (Default Mode)

Note: The default **S9** and system MAX 10 image support AS configuration only.

1. Plug in the pre-programmed SDM QSPI flash daughter into **J3**.

2. Power on the board.

3. Observe that FPGA User_LED is turned on, and User_LED6 and User_LED7 blinked.

5.2. Configuring the FPGA Device by Avalon Streaming Modes

1. Set S9 to Avalon streaming interface x8 mode.

   Note: The default system MAX 10 image supports Avalon streaming interface x8 configuration only.

2. Restart the board and program the flash device.

3. Observe that User_LED[0:5] are turned on, and User_LED6 and User_LED7 blinked.

6. Custom Projects for the Development Kit

6.1. Add SmartVID Settings in the Quartus Prime QSF File

The Agilex 7 silicon that is assembled on this development kit enables the SmartVID feature by default. To avoid the Quartus Prime software from generating an error due to incomplete SmartVID settings, you must put constraints outlined below into the Quartus Prime project QSF file. These constraints are designed for the LTC3888 PMIC.

Open your Quartus Prime project QSF file, and copy and paste constraint scripts into the file. Ensure that there are no other similar settings with different values.

```
set_global_assignment -name PWRMGT_SLAVE_DEVICE_TYPE LTC3888
set_global_assignment -name PWRMGT_SLAVE_DEVICE0_ADDRESS 62
set_global_assignment -name PWRMGT_SLAVE_DEVICE1_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE2_ADDRESS 00
set_global_assignment -name ACTIVE_SERIAL_CLOCK AS_FREQ_100MHZ
set_global_assignment -name USE_PWRMGT_SCL SDM_IO0
set_global_assignment -name USE_PWRMGT_SDA SDM_IO12
set_global_assignment -name USE_CONF_DONE SDM_IO16
set_global_assignment -name VID_OPERATION_MODE "PMBUS MASTER"

set_global_assignment -name PWRMGT_VOLTAGE_OUTPUT_FORMAT "LINEAR FORMAT"
set_global_assignment -name PWRMGT_LINEAR_FORMAT_N "-12"
set_global_assignment -name PWRMGT_TRANSLATED_VOLTAGE_VALUE_UNIT VOLTS
```

6.2. Golden Top

You can use the Golden Top project as the starting point for your designs. It comes loaded with constraints, pin locations, define I/O standard, direction, and general termination. The DDR4 pin termination settings are not included. Refer to the DDR4 example designs for details.

7. Document Revision History for the Agilex 7 FPGA I-Series Transceiver (6 × F-Tile) Development Kit User Guide

Document Version	Changes

2024.11.21	• Updated the *Overview* chapter:
	— Updated Table: *Ordering Information*:
	  • Replaced the device part number for the Agilex 7 FPGA I-Series Transceiver Development Kit (Production1 6 × F-Tile) in Table: *Ordering Information* from "AGIC040R39A1E1VB" to "AGIC040R39A1E1VC".
	  • Updated the serial number identifiers for the production and ES1 development kits.
	— Added new Figure: *Agilex 7 FPGA I-Series Transceiver Development Kit—Top View*.
	— Updated Figure: *Agilex 7 FPGA I-Series Transceiver Development Kit—Block Diagram*.
	— Updated *Feature Summary*.
	— Updated *Recommended Operating Conditions*.
	• Updated the *Getting Started* chapter:
	— Added new topics:
	  • *Before You Begin*
	  • *Handling the Board*
	  • *Installing the Quartus Prime Pro Edition Software*
	  • *Installing the Intel SoC EDS*
	  • *Installing the Development Kit*
	  • *Installing the Intel FPGA Download Cable II Driver*
	— Removed the following topics:
	  • *Quick Start Guide*
	  • *Design Examples*
	• Updated and retitled chapter *Power Up the Development Kit* to *Development Kit Setup*.
	— Retitled topic *Power Up* to *Powering Up the Development Kit*.
	— Retitled topic *Perform Board Restore* to *Performing Board Restore*.
	— Retitled topic *Restore board System Intel MAX 10 with default factory image* to *Restoring Board System Intel 10 with Default Factory Image*.
	— Retitled topic *Restore Board QSPI Flash with the Default Factory Image* to *Restoring Board QSPI Flash with the Default Factory Image*.
	• Updated the *Board Test System* chapter:
	— Updated and retitled topic *Installing Quartus Prime Software* to *Setting Up the Quartus Prime Software for BTS Operation*.
	— Updated all the figures in the *BTS Functionalities* chapter.
	— Retitled topic *Test the Functionality of the Development Kit* to *BTS Functionalities*.
	— Retitled topic *The QSFPDD400 PAM4 Tab* to *The QSFPDD400/QSFPDD800 PAM4 Tab*.
	• Updated the *Development Kit Hardware and Configuration* chapter:
	— Retitled topic *Configure the FPGA Device by Active Serial (AS) Modes (Default Mode)* to *Configuring the FPGA Device by Active Serial (AS) Modes (Default Mode)*.
	— Retitled topic *Configure the FPGA Device by Avalon-ST (AvST) Modes* to *Configuring the FPGA Device by Avalon Streaming Modes*.
	• Retitled appendix chapter *Additional Information* to *Safety and Regulatory Compliance Information*.
	• Restructured the document to improve clarity and for ease of reference.
	• Updated the document for the latest branding standards.

2023.05.31	Initial release.

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A. Development Kit Components

A.1. Board Overview and Components

This section describes all the components on the development board. A complete set of schematics, a physical layout database, and Gerber files for the development board reside in the development kit documents directory.

A.1.1. Board Overview

Figure 30.   Agilex 7 FPGA I-Series Transceiver (6 × F-Tile) Development Kit (Top View)

ISO 9001:2015 Registered

A.1.2. Board Components

Table 6.   Board Connector/Switch Description

Connector/Switch	Description
J30	12 V AUX1 connector
J55	12 V AUX2 connector
J3	SDM connector
J38	FAN0 connector (Core FET fan)
J7	FMCA connector
J9	FMCB connector
J57	QSFP0 connector
J27	QSFP-DD0 connector
J22	QSFP-DD800 connector
J58	QSFP1 connector
J48	QSFP-DD1 connector
J77	SFP connector
J6	SI5395-2 IN1N connector
J4	SI5395-2 IN1P connector
J34	FAN1 connector (QSFP left fan)
J79	Temperature sensor I^2C connector
J149	Current sensor I^2C connector
J43	FAN2 connector (FPGA fan)
J37	MCIO connector
J5	DIMM connector
J44	FAN3 connector (QSFP right fan)
J45	OSFP connector
J67	QSFP-DD3 connector
J66	QSFP2 connector
J69	QSFP-DD2 connector
J25	10 MHz IN connector
J12	SI5395-1 IN1N connector
J8	SI5395-1 IN1P connector
J17	10 MHz OUT connector
J140	Clock I^2C connector
J41	PMBUS connector
J21	ToD connector
J31	SI5518 SPI connectorconnector
J42	Clock I^2C connector

continued...

Send Feedback

Connector/Switch	Description
J16	1PPS IN connector
J14	1PPS OUT connector
J56	CY7C68013A I^{2}C connector
J11	JTAG connector
J10	USB2.0 connector
J154	12 V hotswap I^{2}C connector
S19	JTAG selection switch
S20	MSTR switch
S21	PMBUS I^{2}C switch
S9	Mode selection switch
S22	MUX_DIP_SW
S10, S15	System switch
S6, S1	User switch
S7	Board power on/off switch

A.2. System Management

Two MAX 10 FPGAs (10M16SCU324C8G) are used for system management. System MAX 10 acts as system controller. It handles FPGA AvST configuration, I2C bus access, fan speed control and system reset functions. The UB2/PWR MAX 10 acts as Power manager and on-board JTAG controller. Refer to below description for each function:

- **Power management:** Control systems and FPGA power up and optional down sequence, supervise power regulators/switches status and manage power faults, supervise temperature sensor interrupt signals and manage temperature faults.

- **JTAG controller:** Manage JTAG chain topology, JTAG master source and JTAG slaves by S19.

Table 7.   JTAG Master Sources

Schematic Signal Name	Description
EXT_JTAG_TCK/TDO/TMS/TDI	JTAG header J11 for Intel FPGA Download Cable
FX2_Dp/n	Input port J10 for on-board Intel download circuit

Mode	S20[4:1]	S19 [4][3] [2] [1] On: bypass from chain Off: enable in chain	Function
000	ON/ON/ON (Default)	S19.1 (SDM+HPS) S19.2 (SysMax) S19.3(FMC_B) S19.4 (FMC_A)	Mode 1: On-board Intel download circuit act as the only JTAG Master. Chained HPS with SDM nodes internally. Mode 3: External Intel FPGA Download Cable act as the only JTAG Master. Chained HPS with SDM nodes internally.
001	ON/ON/OFF	SDM is always enabled in the JTAG chain	Mode 2: On-board Intel download circuit act as the only JTAG Master.

Mode	S20[4:1]	S19 [4][3] [2] [1] On: bypass from chain Off: enable in chain	Function
		S19.1 (HPS) S19.2 (SysMax) S19.3(FMC_B) S19.4 (FMC_A)	Chained HPS with SDM nodes externally. Mode 4: External Intel FPGA Download Cable act as the only JTAG Master. Chained HPS with SDM node externally.
010	ON/OFF/ON	S19.1 (SDM+HPS) S19.2 (SysMax) S19.3 (FMC_B)	Mode 5: FMC_A acts as the only JTAG Master. Chained HPS with SDM nodes internally.
011	ON/OFF/OFF	SDM is always enabled in the JTAG chain S19.1 (HPS) S19.2 (SysMax) S19.3(FMC_B)	Mode 6: FMC_A acts as the only JTAG Master. Chained HPS with SDM nodes externally.
100	OFF/ON/ON	S19.1 (SDM) S19.2 (SysMax) S19.3(FMC_B) S19.4 (FMC_A)	Mode 7: Both On-board Intel download circuit and OOBE act as JTAG Masters. Separated HPS and SDM JTAG chains, OOBE only drive HPS Mode 8: Both External Intel FPGA Download Cable and OOBE JTAG act as JTAG Masters. Separated HPS and SDM JTAG chains, OOBE only drive HPS
101	OFF/ON/OFF	S19.1 (SDM) S19.2 (SysMax) S19.3(FMC_B)	Mode 9: Both On-board Intel download circuit and FMC_A act as JTAG Masters. Separated HPS and SDM JTAG chains, FMC only drive HPS Mode 10: Both External Intel FPGA Download Cable and FMC_A act as JTAG Masters. Separated HPS and SDM JTAG chains, FMC only drive HPS
110	OFF/OFF/ON	N/A	Mode 11: Both On-board Intel download circuit and OOBE act as JTAG Masters. On-board Intel download circuit only drive SDM, OOBE only drive HPS.
111	OFF/OFF/OFF	N/A	Mode 12: Both On-board Intel download circuit and FMC_A act as JTAG Masters. On-board Intel download circuit only drive SDM, FMC only drive HPS.

A.3. Power

Figure 31.   Power Tree

Figure 32.   Power Sequence
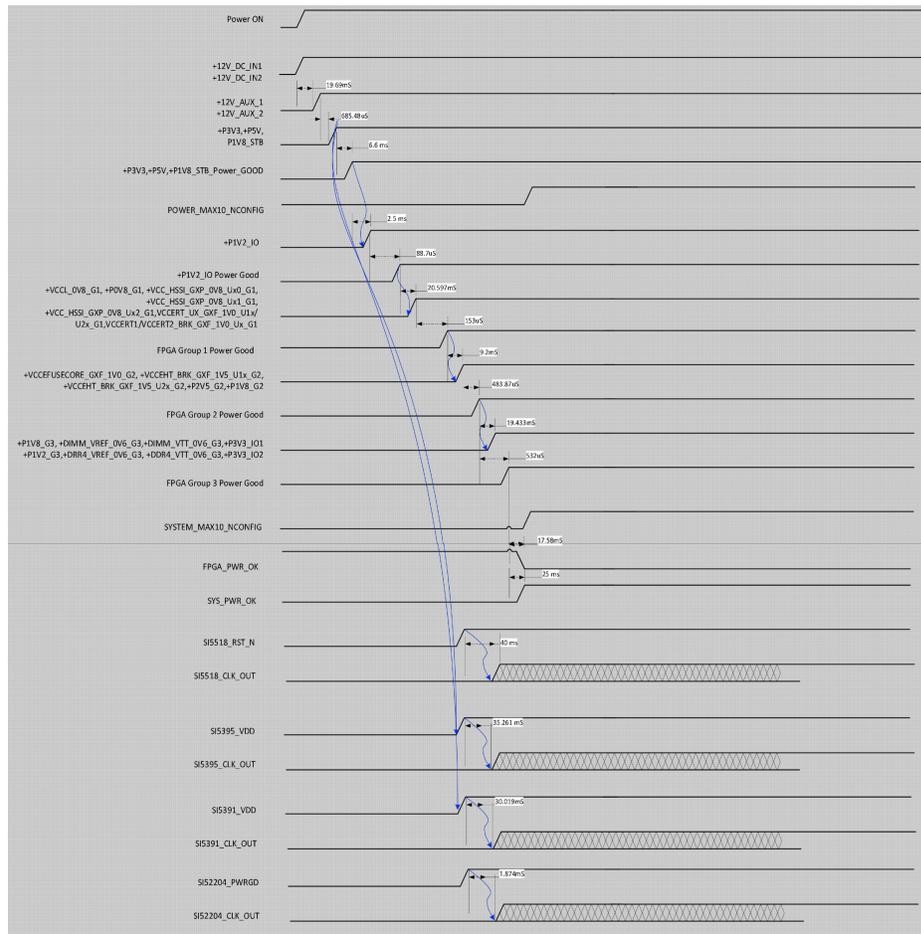
On board hot-plug circuit shuts down all power rails when total power over 360 W (30 A) @ each power port.

UB2/PWR MAX 10 shuts down significant power rails when one or more power good indicators below low due to a power fault.

UB2/PWR MAX10 also shuts down significant power rails when temperature cross the acceptable range.

A.4. Clocks

Table 8.   Default Clock Frequency

Schematic Signal Name	Default Frequency (Hz)
125M_F_OSC_CLK1	125M
CLK_TOD_10M_DN/DP	10M
CLK_1PPS_1V2_FM91	1
	continued...

Schematic Signal Name	Default Frequency (Hz)
DDR_1_166.66M_REFCLK_DN/DP	166.66M
DDR_2_166.66M_REFCLK_DN/DP	166.66M
DDR_3_166.66M_REFCLK_DN/DP	166.66M
DDR_4_166.66M_REFCLK_DN/P	166.66M
CLK_100M_GPIO_2C_DN/DP	100M
1PPS_SMA_OUT_1V2	1
CLK_100M_GPIO_4_DN/DP	100M
CLK_PCIE_EP_MCIO1_DP/DN	100M
CLK_PCIE_RP_MCIO1_DP/DN	100M
PCIE_100M_REF_AP/AN	100M
SYS_M10_50M	50M
PWR_M10_50M	50M
SMA_1PPS_OUT	1
SMA_10MHZ_OUT	10M
REFCLK_FGT_12A_8_DP/DP	Not assigned
REFCLK_FGT_12A_9_DP/DP	Not assigned
FMCA_RECRD_CLK_DP/DN	Not assigned
REFCLK_FGT_13C_8_DP/DN	Not assigned
REFCLK_FGT_13C_9_DP/DN	Not assigned
FMCB_RECRD_CLK_DP/DN	Not assigned
OCXO_19.44MHZ	19.44M
SI5518_REF_IN_R	54M
SI5518_XTAL_XA	54M
FMCA_ETH_REFCLK_156.25M_DP/DN	156.25M
FMCB_ETH_REFCLK_156.25M_DP/DN	156.25M
SI5518_OUT2_1PPS_PLL_FB	1
FMCA_CPRI_REFCLK_153.6M_DP/DN	153.6M
FMCB_CPRI_REFCLK_153.6M_DP/DN	153.6M
FMCA_CPRI_REFCLK_184.32M_DP/DN	184.32M
FMCB_CPRI_REFCLK_184.32M_DP/DN	184.32M
CLK_TOD_10M_DP/DN	156.25M
CLK_1PPS_FM91	1
CLK_1PPS_OUT_SMA	1
CLK_10M_OUT_SMA	10M
CLK_SI5518_FREQ_OUT12_156.25M_DP/DN	156.25M
CLK_SI5518_FREQ_OUT14_156.25M_DP/DN	156.25M

continued...

Schematic Signal Name	Default Frequency (Hz)
REFCLK2_PCIE_100M_DP/DN	100M
REFCLK1_PCIE_100M_DP/N	100M
SI52204_CLKIN	25M
SI5391_XA	48M
CLK_FHT_13B_156.25M_DP/DN	156.25M
CLK_FHT_13C_156.25M_DP/DN	156.25M
CLK_FGT_13B_156.25M_DP/DN	156.25M
CLK_FGT_13B_156.25M_SPARE_DP/DN	156.25M
CLK_FGT_13A_156.25M_DP/DN	156.25M
CLK_FGT_13A_156.25M_SPARE_DP/DN	156.25M
CLK_SI5395_1_OUT9A_DP/DN	100M
CLKGEN_SI5395_2_XA	48M
CLK_FHT_12B_156.25M_DP/DN	156.25M
CLK_FHT_12C_156.25M_DP/DN	156.25M
CLK_FGT_12C_156.25M_DP/DN	156.25M
CLK_FGT_12C_156.25M_SPARE_DP/DN	156.25M
CLK_FGT_12B_156.25M_DP/DN	156.25M
CLK_FGT_12B_156.25M_SPARE_DP/DN	156.25M
CLK_SI5395_2_OUT9A_DP/DN	100M
FX2_XTALIN	24M

Figure 33.   Clock Tree
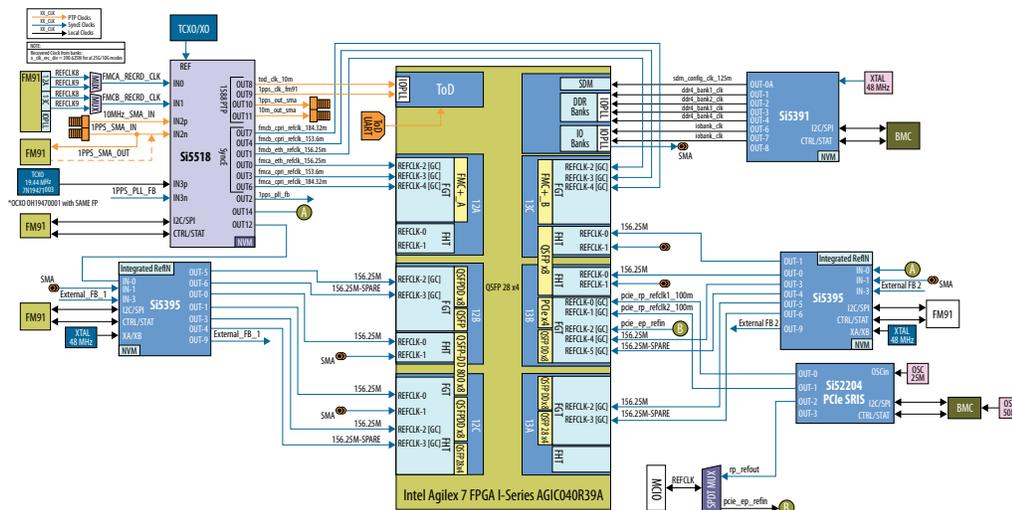
A.5. General Input/Output

Table 9.   MAX 10 and FPGA

Schematic Signal Name	Description
`F_GPIO0`	The value of the filtered `user_pb[0]`.
`F_GPIO1`	The value of the filtered `user_pb[1]`.
`F_GPIO2`	Reserved
`F_GPIO3`	Reserved
`F_GPIO4`	Reserved
`F_GPIO5`	Reserved
`F_GPIO6`	Reserved
`F_GPIO7`	Reserved
`F_GPIO8`	Reserved
`F_GPIO9`	Reserved
`F_GPIO10`	Used for DIP Switch
`F_GPIO11`	Used for Switch Data Transfer

Table 10.   System MAX 10

Schematic Signal Name	Description
`USER_PB0`	User Push Button
`USER_PB1`	User Push Button
`USER_SW0`	User Switch
`USER_SW1`	User Switch
`USER_SW2`	User Switch
`USER_SW3`	User Switch
`USER_SW4`	User Switch
`USER_SW5`	User Switch
`USER_SW6`	User Switch
`USER_SW7`	User Switch
`SYS_PWR_RSV3`	Reserved GPIO between system MAX 10 and Power MAX 10
`SYS_PWR_RSV2`	Reserved GPIO between system MAX 10 and Power MAX 10
`SYS_PWR_RSV1`	Reserved GPIO between system MAX 10 and Power MAX 10
`SYS_PWR_RSV0`	Reserved GPIO between system MAX 10 and Power MAX 10
`USER_LED0`	User LED
`USER_LED1`	User LED
`USER_LED2`	User LED

continued...

Schematic Signal Name	Description
USER_LED3	User LED
USER_LED4	User LED
USER_LED5	User LED
USER_LED6	User LED
USER_LED7	User LED
F_GPIO0	The value of the filtered `user_pb[0]`
F_GPIO1	The value of the filtered `user_pb[1]`
F_GPIO2	MCIO_PERST in RP mode
F_GPIO3	FMC_A_PERST in RP mode
F_GPIO4	FMC_B_PERST in RP mode
F_GPIO5	Reserved
F_GPIO6	Reserved
F_GPIO7	Reserved
F_GPIO8	Reserved
F_GPIO9	Reserved
F_GPIO10	Reserved
F_GPIO11	Reserved
SYS_SW0	Factory load: 0—Load image from Page 0 of the QSPI
SYS_SW1	NU
SYS_SW2	NU
SYS_SW3	NU
SYS_SW4	NU
SYS_SW5	FMC-A PCIe RP/EP Select: "0": RP "1": EP
SYS_SW6	FMC-B PCIe RP/EP Select: "0": RP "1": EP
SYS_SW7	MCIO PCIe RP/EP Select: "0": RP "1": EP
SYS_LED0/D9	PGM_LED0 for Avalon streaming configuration
SYS_LED2/D11	PGM_LED1 for Avalon streaming configuration
SYS_LED4/D13	PGM_LED2 for Avalon streaming configuration
SYS_LED6/D15	MAX_ERROR for Avalon streaming configuration
SYS_LED1/D10	MAX_LOAD for Avalon streaming configuration

continued...

Schematic Signal Name	Description
SYS_LED3/D12	MAX_CONF_DONE for Avalon streaming configuration
SYS_LED5/D14	Reserved
SYS_LED7/D16	Reserved
SYS_PB0/S11	MAX_RESETn
SYS_PB1/S12	FPGA_RESETn
SYS_PB2/S14	Power recycle
SYS_PB3/S16	PGM_SEL for Avalon streaming configuration
SYS_PB4/S17	PGM_CFG for Avalon streaming configuration
FPGA_FAN_PWM	Fan 2 PWM signal
FPGA_FAN_TACH	Fan 2 tachometer signal
QSFP_RIGHT_FAN_PWM	Fan 3 PWM signal
QSFP_RIGHT_FAN_TACH	Fan 3 tachometer signal
QSFP_LEFT_FAN_PWM	Fan 1 PWM signal
QSFP_LEFT_FAN_TACH	Fan 1 tachometer signal
CORE_FETS_FAN_PWM	Fan 0 PWM signal
CORE_FETS_FAN_TACH	Fan 0 tachometer signal
MUX_SEL0	Mux Select for choosing either REFCLK_FGT_12A_8_DP/N (or) REFCLK_FGT_12A_9_DP/N for FMCA_RECRD_CLK 0: FMCA_RECRD_CLK= REFCLK_FGT_12A_8_DP/N 1: FMCA_RECRD_CLK= REFCLK_FGT_12A_9_DP/N
MUX_SEL1	Mux select for choosing either REFCLK_FGT_13C_8_DP/N (or) REFCLK_FGT_13C_9_DP/N for FMCB_RECRD_CLK 0: FMCA_RECRD_CLK= REFCLK_FGT_13C_8_DP/N 1: FMCA_RECRD_CLK= REFCLK_FGT_13C_9_DP/N
MCIO_CLK_SEL_EP_N	Tied to MUX_DIP_SW2
MCIO_CLK_ENN	Tied to MUX_DIP_SW3
MUX_DIP_SW0	DIP switch 0 signal (high by default)—tie this to MUX_SEL0
MUX_DIP_SW1	DIP switch 1 signal (high by default)—tie this to MUX_SEL1
MUX_DIP_SW2	MCIO_CLK_SEL_EP_NN: Low before system power OK High after system power OK
MUX_DIP_SW3	MCIO_CLK_ENN: High before system power OK Low after system power OK
VCCL_I2C_EN	Connect VCCL_SCL/SDA to system MAX 10 (Default: ENABLE-1)
R_13C_PERST_IO_N	Driven low
R_13B_PERST_IO_N	Tied to MCIO PREST internally
R_12B_PERST_IO_N	Driven low

continued...

Schematic Signal Name	Description
R_12C_PERST_IO_N	Driven low
SI5395_1_A_IN_SEL0_R	Do not use (DNU)
SI5395_2_A_OEN_SYS_R	High before system power OK Low after system power OK
SI52204_PWRGD_R	Tied to system power OK
SI5395_2_A_IN_SEL0_R	DNU
SI5395_1_A_OEN_SYS_R	High before system power OK Low after system power OK
SI5391_A_OEN	High before system power OK Low after system power OK
SI5391_A_RSTN	Low until system power OK High after system power OK
SI5518_GPIO_0_R	DNU
CLK_OE_0_N	SI52204 CLK ENABLE0: High before system power OK Low after system power OK
CLK_OE_1_N	SI52204 CLK ENABLE1: High before system power OK Low after system power OK
CLK_OE_2_N	SI52204 CLK ENABLE2: High before system power OK Low after system power OK
SI5518_GPIO_1_R	DNU
SI5518_GPIO_2_R	DNU
CLK_SI5395_2_FINC_R	DNU
CLK_SI5395_2_FDEC_R	DNU
CLK_SI5395_1_FINC_R	DNU
CLK_SI5395_1_FDEC_R	DNU
SI5518_I2C_R_EN	Keep it enabled: Low before system power OK DNU after system power OK
R_12A_SPARE_N	Driven low
R_13A_SPARE_N	Driven low
DIMM_IO_R_EN	Enable always after system power OK Low before system power OK DNU after system power OK
FMC_B_PCIE_PERSTN_3V3	DNU
FMC_B_PCIE_WAKEN_3V3	DNU
FMC_A_PCIE_WAKEN_3V3	DNU
FMC_A_PCIE_PERSTN_3V3	DNU

Table 11.   UB2/PWR MAX 10

Schematic Signal Name	Description
FPGA_POK_LED	FPGA Power Good
SYS_PWR_RSV0	Reserved GPIO between system MAX 10 and power MAX 10
SYS_PWR_RSV1	Reserved GPIO between system MAX 10 and power MAX 10
SYS_PWR_RSV2	Reserved GPIO between system MAX 10 and power MAX 10
SYS_PWR_RSV3	Reserved GPIO between system MAX 10 and ower MAX 10
PWR_PB0	POWER MAX PB0—FU

A.6. Memory Interfaces

FPGA Dedicated External Memory Interface (1DPC DDR4)

Agilex 7 FPGA I-Series Transceiver Development Kit supports 16 GB 1DPC DDR4 with ECC support (x72). Mechanically, the development kit provides 1 Dual In Memory Module slots for the same.

FPGA External Memory Interface (DDR4)

DDR4 component interface is a 72 bit, single rank configuration based on x16 component. It runs at 2666 MT/s. MT40A2G16SKL-062E:B or MT40A2G16TBB-062E:F from Micron is soldered down on the development kit.

A.7. Communication Interfaces

MCIO Port (J37)

The MCIO slot is a PCIe 4.0 x4 port which fans out from Agilex 7 I-Series FPGA F-Tile. This port is designed to meet the standard MCIO pinout.

System MAX 10 acts as the board management controller (BMC) of the development kit. It manages power up reset for both PCIe root port and PCIe end point. PCIE_1_PERSTn_A signal acts as output and input respectively.

Table 12.   MCIO Port

Schematic Signal Name	Description
PCIE_1_PERSTn_A	PCIe endpoint/rootport reset
PCIE_1_ALERTn_A	PCIe Alert
PCIE_100M_REF_AP/AN	PCIe reference clock
PCIE_1_SCL_A/SDA_A	PCIe I^{2}C bus
PCIE_1_TX_[0:3]_DP/DN	Transceiver TX
PCIE_1_RX_[0:3]_DP/DN	Transceiver RX

QSFPDD

Agilex 7 FPGA I-Series Transceiver Development Kit supports 4x QSFPDD ports. The QSFPDD port fans out from the Agilex 7 I-Series FPGA F-Tile (FGT). All 8 channels per QSFPDD can run up to 25 Gbps NRZ and 50 Gbps PAM4.

Table 13.   QSFPDD Connector -0 (12B/J27)

Schematic Signal Names	Description
QSFPDD0_MODPRS_L	Module present
QSFPDD0_RESET_L	Module reset
QSFPDD0_MODSEL_L	Mode select
QSFPDD0_LPMODE	Initial mode
QSFPDD0_INT_L	Interrupt
I2C_QSFP_1_SCL	I^{2}C clock
I2C_QSFP_1_SDA	I^{2}C data
QSFPDD0_TX_[0:7]_DP/DN	Transceiver TX
QSFPDD0_RX_[0:7]_DP/DN	Transceiver RX

Table 14.   QSFPDD Connector 1 (12C/J48)

Schematic Signal Names	Description
QSFPDD1_MODPRS_L	Module present
QSFPDD1_RESET_L	Module reset
QSFPDD1_MODSEL_L	Mode select
QSFPDD1_LPMODE	Initial mode
QSFPDD1_INT_L	Interrupt
I2C_QSFP_3_SCL	I^{2}C clock
I2C_QSFP_3_SDA	I^{2}C data
QSFPDD1_TX_[0:7]_DP/DN	Transceiver TX
QSFPDD1_TX_[0:7]_DP/DN	Transceiver RX

Table 15.   QSFPDD Connector -2 (13A/J69)

Schematic Signal Names	Description
QSFPDD2_MODPRS_L	Module present
QSFPDD2_RESET_L	Module reset
QSFPDD2_MODSEL_L	Mode select
QSFPDD2_LPMODE	Initial mode
QSFPDD2_INT_L	Interrupt
I2C_QSFP_2_SCL	I^{2}C clock

continued...

Schematic Signal Names	Description
I2C_QSFP_2_SDA	I^{2}C data
QSFPDD2_TX_[0:7]_DP/DN	Transceiver TX
QSFPDD2_RX_[0:7]_DP/DN	Transceiver RX

Table 16.   QSFPDD Connector -3 (13B/J67)

Schematic Signal Names	Description
QSFPDD3_3V3_MODPRS_L	Module present
QSFPDD3_3V3_RESET_L	Module reset
QSFPDD3_3V3_MODSEL_L	Mode select
QSFPDD3_3V3_LPMODE	Initial mode
QSFPDD3_3V3_INT_L	Interrupt
I2C_QSFP_2_SCL	I^{2}C clock
I2C_QSFP_2_SDA	I^{2}C data
QSFPDD3_TX_[0:7]_DP/DN	Transceiver TX
QSFPDD3_RX_[0:7]_DP/DN	Transceiver RX

QSFPDD800

Agilex 7 FPGA I-Series Transceiver Development Kit supports 1x QSFPDD800 port. QSFPDD800 port fans out from the Agilex 7 I-Series FPGA F-Tile (FHT). The FHT Tile from bank 12B and 12C can run up to 400 Gbps (50G x 8) PAM4 in DK-SI-AGI040FES. 4 FHT lanes from bank 12B+4 FHT lanes from bank 12C are terminated directly to QSFPDD800 connector lanes [0:7] (J22).

Note: QSFPDD800 works up to 800 Gbps (100 G x 8) PAM4 in DK-SI-AGI040EA.

Table 17.   QSFPDD800 (12B+12C)

Schematic Signal Names	Description
QSFPDD800_MODPRS_L	Module present
QSFPDD800_RESET_L	Module reset
QSFPDD800_MODSEL_L	Mode select
QSFPDD800_LPMODE	Initial mode
QSFPDD800_INT_L	Interrupt
I2C_QSFP_1_SCL	I^{2}C clock
I2C_QSFP_1_SDA	I^{2}C data
QSFPDD800_TX_[0:7]_DP/DN	Transceiver TX
QSFPDD800_RX_[0:7]_DP/DN	Transceiver RX

QSFP

Agilex 7 FPGA I-Series Transceiver Development Kit supports 3x QSFP ports. The QSFP port fans out from the Agilex 7 I-Series FPGA F-Tile (FGT). All 4 channels can run up to 1 Gbps per lane.

Table 18.   QSFP Connector-0 (12B/J57)

Schematic Signal Names	Description
QSFP0_MOD_PRS_N	Module present
QSFP0_RST	Module reset
QSFP0_MOD_SEL_L	Mode select
QSFP0_LP_MODE	Initial mode
QSFP0_INTERRUPT_N	Interrupt
I2C_QSFP_1_SCL	I^{2}C clock
I2C_QSFP_1_SDA	I^{2}C data
QSFP0_TX_[0:3]_DP/DN	Transceiver TX
QSFP0_RX_[0:3]_DP/DN	Transceiver RX

Table 19.   QSFP Connector-1 (12C/J58)

Schematic Signal Names	Description
QSFP1_MOD_PRS_N	Module present
QSFP1_RST	Module reset
QSFP1_MOD_SEL_L	Mode select
QSFP1_LP_MODE	Initial mode
QSFP1_INTERRUPT_N	Interrupt
I2C_QSFP_3_SCL	I^{2}C clock
I2C_QSFP_3_SDA	I^{2}C data
QSFP1_TX_[0:3]_DP/DN	Transceiver TX
QSFP1_RX_[0:3]_DP/DN	Transceiver RX

Table 20.   QSFP Connector-2 (13A/J66)

Schematic Signal Names	Description
QSFP2_MOD_PRS_N	Module present
QSFP2_RST	Module reset
QSFP2_MOD_SEL_L	Mode select
QSFP2_LP_MODE	Initial mode
QSFP2_INTERRUPT_N	Interrupt
I2C_QSFP_2_SCL	I^{2}C clock

continued...

Schematic Signal Names	Description
I2C_QSFP_2_SDA	I^{2}C data
QSFP2_TX_[0:3]_DP/DN	Transceiver TX
QSFP2_RX_[0:3]_DP/DN	Transceiver RX

OSFP

Agilex 7 FPGA I-Series Transceiver Development Kit supports OSFP ports. OSFP port fans out from the Agilex 7 I-Series FPGA F-Tile (FHT). The FHT Tile from bank 13B and 13C can run up to 400 Gbps (50G x 8) PAM4 in DK-SI-AGI040FES. 4 FHT lanes from bank 13B + 4 FHT lanes from bank 13C are terminated directly to OSFP connector lanes [0:7] (J45).

Note: OSFP works up to 800 Gbps (100G x 8) PAM4 in DK-SI-AGI040EA.

Table 21.   OSFP (13B+13C)

Schematic Signal Names	Description
OSFP_LPW_PRSNT_N	Initial mode/Module Present
OSFP_INT_RST_N	Interrupt/Reset
I2C_OSFP_3V3_SCL	I^{2}C clock
I2C_OSFP_3V3_SDA	I^{2}C data
OSFP_TX[0:7]_DP/DN	Transceiver TX
OSFP_RX[0:7]_DP/DN	Transceiver RX

SFP

Agilex 7 FPGA I-Series Transceiver Development Kit supports 4x SFP ports. SFP port fans out from the Agilex 7 I-Series FPGA F-Tile (FGT). All 4 channels can run up to 1 Gbps/each SFP channel.

Table 22.   SFP (12C/J77)

Schematic Signal Names	Description
SFP3_TX_DISABLE	Transmitter Disable
SFP3_RATE_SEL	Module Rate Select 0
SFP3_MOD0_PRSNT_N	Module Present
SFP3_LOS	Loss of Signal
SFP3_TX_FAULT	Transmitter Fault Indication
SFP3_RS1	Module rate select 1
SFP3_MOD0_SCL	I^{2}C clock
SFP3_MOD0_SDA	I^{2}C data
SFP3_TX_DP/DN	Transceiver TX
SFP3_RX_DP/DN	Transceiver RX
SFP2_TX_DISABLE	Transmitter Disable

continued...

Schematic Signal Names	Description
SFP2_RATE_SEL	Module Rate Select 0
SFP2_MOD1_PRSNT_N	Module Present
SFP2_LOS	Loss of Signal
SFP2_TX_FAULT	Transmitter Fault Indication
SFP2_RS1	Module rate select 1
SFP2_MOD1_SCL	I^2C clock
SFP2_MOD1_SDA	I^2C data
SFP2_TX_DP/DN	Transceiver TX
SFP2_RX_DP/DN	Transceiver RX
SFP1_TX_DISABLE	Transmitter Disable
SFP1_RATE_SEL	Module Rate Select 0
SFP1_MOD2_PRSNT_N	Module Present
SFP1_LOS	Loss of Signal
SFP1_TX_FAULT	Transmitter Fault Indication
SFP1_RS1	Module rate select 1
SFP1_MOD2_SCL	I^2C clock
SFP1_MOD2_SDA	I^2C data
SFP1_TX_DP/DN	Transceiver TX
SFP1_RX_DP/DN	Transceiver RX
SFP0_TX_DISABLE	Transmitter Disable
SFP0_RATE_SEL	Module Rate Select 0
SFP0_MOD3_PRSNT_N	Module Present
SFP0_LOS	Loss of Signal
SFP0_TX_FAULT	Transmitter Fault Indication
SFP0_RS1	Module rate select 1
SFP0_MOD3_SCL	I^2C clock
SFP0_MOD3_SDA	I^2C data
SFP0_TX_DP/DN	Transceiver TX
SFP0_RX_DP/DN	Transceiver RX

FMC + Connectors

Agilex 7 FPGA I-Series Transceiver Development Kit supports 2x FMC+ slots for functional expandability. The x16 FGT lanes from bank 13C and 12A are terminated to FMC-A (J7) and FMC-B (J9) connectors respectively. Auxiliary signals are controlled by the System MAX 10.

Serial Buses

SDM I/Os (`SDM_IO0/12`) and MAX 10 I/Os (`VCCL_SDA/SCL`) share the same I^{2}C bus which talks with Agilex 7 FPGA core regulators. By default, SDM acts as SmartVID master and system MAX 10 act as Power GUI master in this chain.

System MAX 10 I/Os (`PMB_SDA/SCL`) manages the second I^{2}C bus which access all I^{2}C slave regulators, except Agilex 7 FPGA core regulators.

System MAX 10 supports I^{2}C master dedicated to clock related devices (`CLK_I2C_SDA/SCL`), which manages 4# clock devices and SPI from Agilex 7 could control SI5518 (clock device).

Agilex 7/System MAX 10 also manages QSFPDD800, 4x QSFPDD, 1DPC DIMM, 3x QSFP, SFP, OSFP, 2x FMC, MCIO I^{2}C buses System MAX 10 supports as a I^{2}C Master for Current (`IVSNS_I2C_SDA /SCL`) and Temperature sensors (`T_SNS_SCL/SDA`).

The SGPI Interface exists between System MAX 10 and Agilex 7 (`FPGA_SGPIO_SYNC/FPGA_SGPO/FPGA_SGPIO_CLK/FPGA_SGPI`).

System MAX 10 as SPI Master to communicate with Agilex 7 (`MAX10_SPI_SCLK/CSN/MOSI/MISO`).

Agilex 7 as SPI Master to communicate with System MAX 10 (`FPGA_SPI_SCLK/CSN/MOSI/MISO`).

Table 23.   I^{2}C Debug Headers

Schematic Signal Name	Description
`PMB_SCL/SDA`	VRs I^{2}C header J41
`CLK_I2C_SDA/SCL_3V3`	System MAX 10 Clock I^{2}C bus header J140 (ES board) or J42 (production board)
`IVSNS_I2C_SDA /SCL`	Current sensor J149
`T_SNS_SCL/SDA`	Temperature sensor I2C J79

Table 24.   SPI Headers

Schematic Signal Name	Description
SI5518_I2C_SCL_SCLK/SI5518_GPIO3_SDO/ SI5518_I2C_SDA_SDIO/SI5518_A0_CSB	SI5518 SPI Header J31

Figure 34. **I²C Serial Bus**
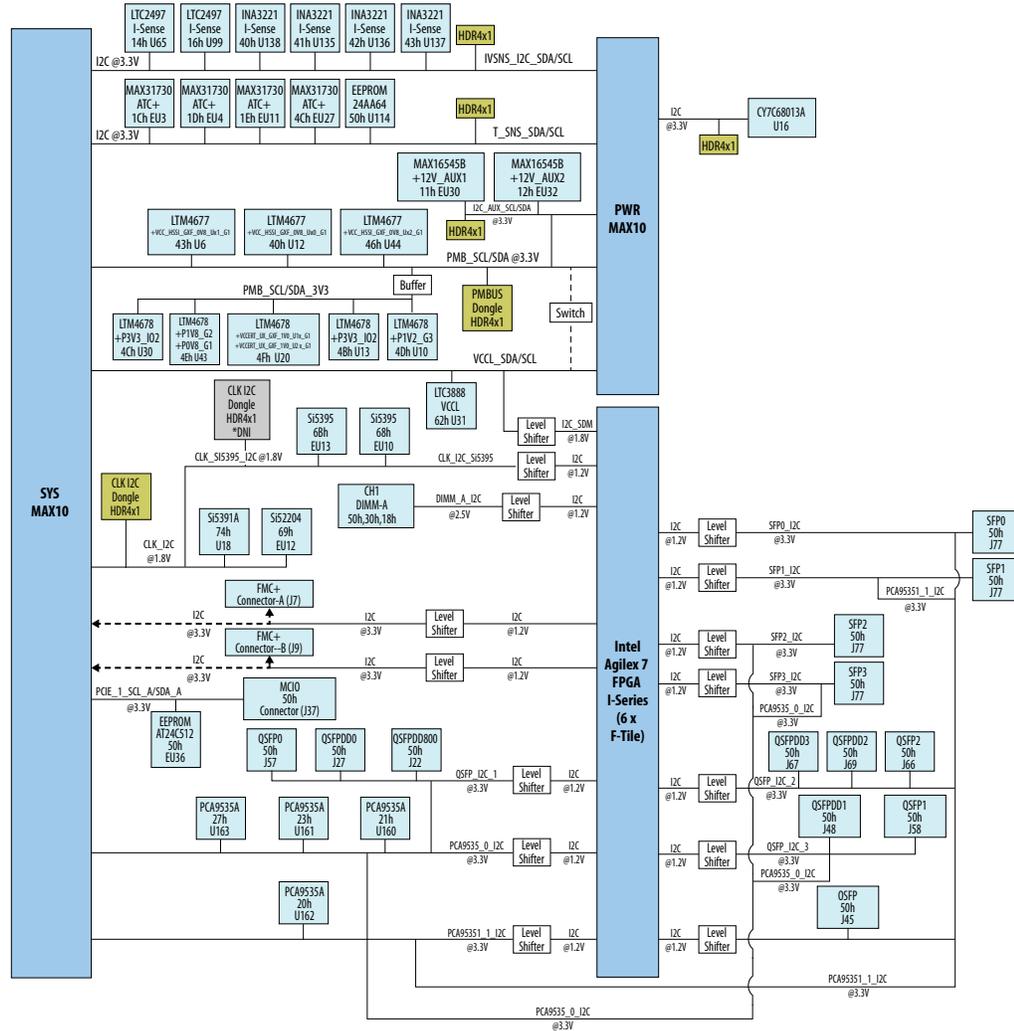
A.8. Daughter Cards

256MB QSPI flash daughter card

This daughter card is pre-programmed with GPIO for AS configuration. It can be re-programmed by customer image. The part number is MT25QU02GCBB8E12-0SIT.

Send Feedback

B. Developer Resources

Use the following links to check the Intel website for other related information.

Table 25.   Agilex 7 FPGA I-Series Transceiver Development Kit References

Reference	Description
Agilex 7 FPGA I-Series Transceiver Development Kit page	Latest board design files, reference designs, and kit installation for Windows* and Linux*.
Rocketboard.org	Open-source community website supporting SoC development including Altera and Partner SoC development kit targets and related designs and documentation.
Intel SoC FPGA Embedded Development Suite (SoC EDS) User Guide	Installing the SoC EDS and ARM DS-5. Preloader user guide. Hard Processor System (HPS) Flash programmer. Bare Metal and Linux* compilers. Debugging.
Agilex 7 FPGA Board Design Guided Journey	The interactive FPGA Board Guided Journey provides step-by-step guidance for developing printed circuit boards (PCBs) using Agilex 7 devices.
Agilex 7 Device Design Guidelines	Guidelines, recommendations, and a list of factors to consider for designs that use the Agilex 7 SoC devices.
AN 958: Board Design Guidelines	Board design-related resources for Altera devices. Its goal is to help you implement successful high-speed PCBs that integrate device(s) and other elements.
Agilex 7 Power Management User Guide	Describes the Agilex 7 devices power-optimization features, power-up and power-down sequences, power distribution network, voltage and temperature monitoring systems with a design example to read the TSDs, and power optimization techniques.
Agilex 7 Power Distribution Network Design Guidelines	Provides information for the Agilex 7 device family power distribution network (PDN) design guidelines.
FPGA SmartVID	SmartVID is a feature on select Altera FPGAs where the device identifies the optimal voltage that it should be operated at, and provides this information to the power regulator via the PMBus. The term represents Smart Voltage IDentification (SmartVID).
SmartVID Debug Checklist and Voltage Regulator Guidelines	Provides the checklist to assist you to rule out the possible causes of configuration failure due to SmartVID.
Agilex 7 Configuration User Guide	Provides the configuration process, the device pins required for configuration, the available configuration schemes, remote system updates, and debugging. This user guide also provides an overview of the secure device manager (SDM) which manages security for the configuration bitstream.
Documentation: Agilex 7	Agilex 7 device documentation.
Cadence* Capture CIS Schematic Symbols	Agilex 7 OrCAD symbols.

C. Safety and Regulatory Compliance Information

C.1. Safety and Regulatory Information

ENGINEERING DEVELOPMENT PRODUCT - NOT FOR RESALE OR LEASE

This development kit is intended for laboratory development and engineering use only.

This development kit is designed to allow:

- Product developers and system engineers to evaluate electronic components, circuits, or software associated with the development kit to determine whether to incorporate such items in a finished product.
- Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required Federal Communications Commission (FCC) equipment authorizations are first obtained.

Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference.

Unless the assembled kit is designed to operate under Part 15, Part 18 or Part 95 of the United States Code of Federal Regulations (CFR) Title 47, the operator of the kit must operate under the authority of an FCC licenseholder or must secure an experimental authorization under Part 5 of the United States CFR Title 47.

Safety Assessment and CE & UKCA mark requirements have been completed, however, other certifications that may be required for installation and operation in your region have not been obtained.

C.1.1. Safety Warnings

Power Supply Hazardous Voltage

AC mains voltages are present within the power supply assembly. No user serviceable parts are present inside the power supply.

Power Connect and Disconnect

The AC power supply cord is the primary disconnect device from mains (AC power) and used to remove all DC power from the board/system. The socket outlet must be installed near the equipment and must be readily accessible.

System Grounding (Earthing)

To avoid shock, you must ensure that the power cord is connected to a properly wired and grounded receptacle. Ensure that any equipment to which this product is attached to is also connected to properly wired and grounded receptacles.
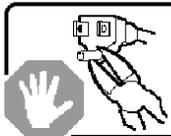
Power Cord Requirements

The plug on the power cord must be a grounding-type male plug designed for use in your region. It must have certification marks showing certification by an agency in your region. The connector that plugs into the appliance inlet of the power supply must be an IEC 320, sheet C13, female connector. If the power cord supplied with the system does not meet requirements for use in your region, discard the cord, and do not use it with adapters. Use only certified power supply cord with appropriate gauge, designed for use in your region.
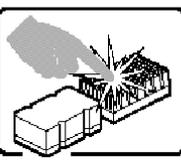

Lightning/Electrical Storm

Do not connect/disconnect any cables or perform installation/maintenance of this product during an electrical storm.

Risk of Fire

To reduce the risk of fire, keep all flammable materials a safe distance away from the boards and power supply. You must configure the development kit on a flame retardant surface.

C.1.2. Safety Cautions

Thermal and Mechanical Injury

Certain components such as heat sinks, power regulators, and processors may be hot. Heatsink fans are not guarded. Power supply fan may be accessible through guard. Care should be taken to avoid contact with these components.

Cooling Requirements

Maintain a minimum clearance area of 5 centimeters (2 inches) around the side, front and back of the board for cooling purposes. Do not block power supply ventilation holes and fan.

Electro-Magnetic Interference (EMI)

This equipment has not been tested for compliance with emission limits of FCC and similar international regulations. Use of this equipment in a residential location is prohibited. This equipment generates, uses and can radiate radio frequency energy which may result in harmful interference to radio communications. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment on and off, you are required to take measures to eliminate this interference.

Telecommunications Port Restrictions

The wireline telecommunications ports (modem, xDSL, T1/E1) on this product must not be connected to the Public Switched Telecommunication Network (PSTN) as it might result in disruption of the network. No formal telecommunication certification to FCC, R&TTE Directive, or other national requirements have been obtained.

Electrostatic Discharge (ESD) Warning

A properly grounded ESD wrist strap must be worn during operation/installation of the boards, connection of cables, or during installation or removal of daughter cards. Failure to use wrist straps can damage components within the system.

Attention: Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of this product in unsorted municipal waste.

Lithium Ion Battery Warnings

Lithium Battery: Risk of explosion if the lithium battery is replaced by an incorrect type. Risk of fire, explosion, or chemical burn if the battery is mistreated (punctured or crushed). Do not attempt to disassemble. Do not incinerate. Observe proper polarity when replacing battery. Do not dispose—the battery is intended to be serviced and disposed by qualified Intel service personnel only.

Perchlorate Material: Special handling may apply. For more details, refer to www.dtsc.ca.gov/hazardouswaste/perchlorate. This notice is required by California Code of Regulations, Title 22, Division 4.5, Chapter 33: Best Management Practices for Perchlorate Materials. This product includes a battery which contains perchlorate material.

Taiwan battery recycling:

廢電池請回收

(Translation - please recycle batteries)

Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of product in unsorted municipal waste.

C.2. Compliance Information

CE EMI Conformity Caution

This development board is delivered conforming to relevant standards mandated by Directive 2014/30/EU. Because of the nature of programmable logic devices, it is possible for the user to modify the development kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as a result of modifications to the delivered material is the responsibility of the user of this development kit.

CE $\quad$ UK CA