5G Application on Sapphire Rapids EE

FEC Acceleration and DFT/iDFT (FFT/iFFT) Offloading with Intel® vRAN Boost

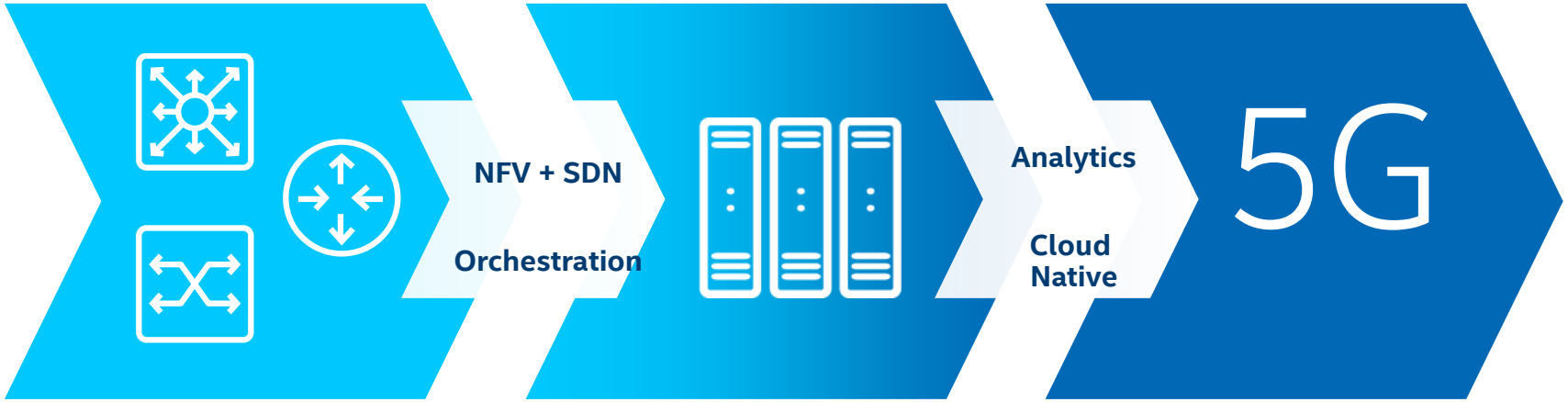
Document Number: 786771

August 2023

Agenda

- Introduction to 5G with vRAN
- vRAN ecosystem enabling with Intel® FlexRAN™ Technology
- Intel® FlexRAN™ Technology Overview
- Intel® vRAN Boost Introduction
- Getting Started
- Setup Guide
- Test Application Demo

NETWORK TRANSFORMATION: FUNDAMENTAL TO 5G



Custom

Proprietary

Hardware Defined

Software Defined

Open Platforms

Virtualized Containers

Network Slicing

Analytics Core to Edge

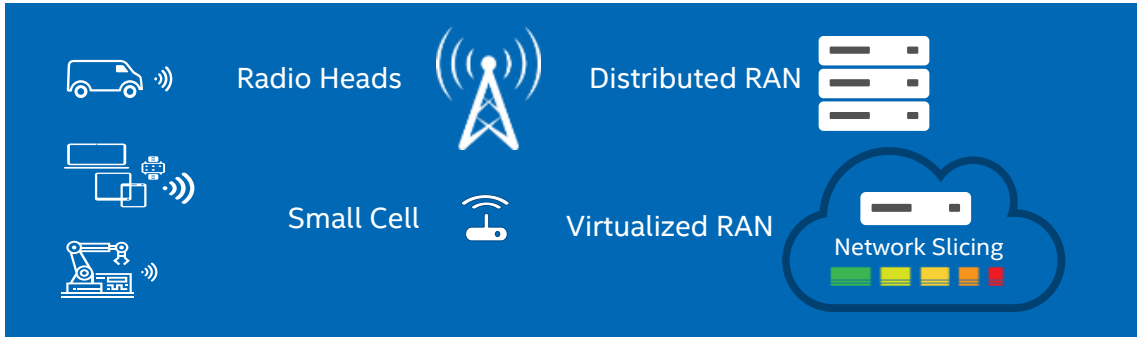
Visual Cloud

Cloudification brings:

- Intelligence where you need it
- Flexibility and agility
- Single scalable architecture
- New services

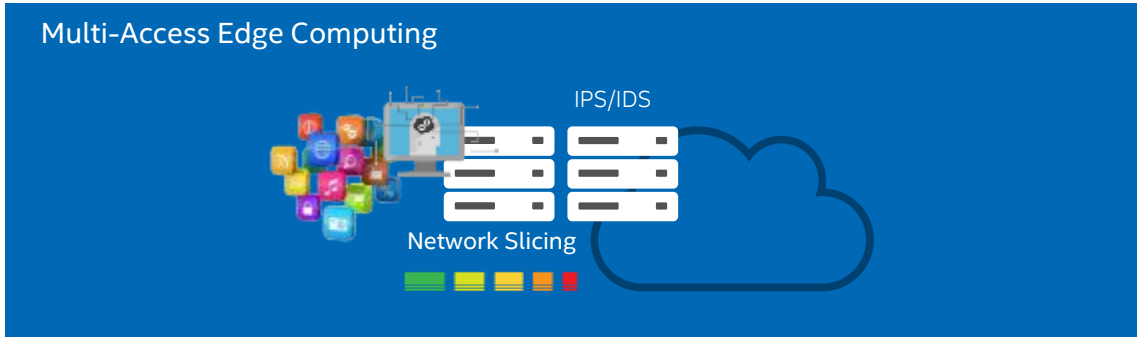
ENABLING ALL RAN DEPLOYMENT MODELS
DISTRIBUTED AND CENTRALIZED, VIRTUALIZED, MACRO & SMALL CELL

ACCESS



DEMAND FOR BROAD RANGE OF DEPLOYMENTS

EDGE



DEMAND FOR CLOUD-LIKE INNOVATION

Future Radio Access Networks will be based on a wide range of solutions deployments - **one size no longer fits all**	Continued 4G & 5G traffic growth require significant increase in RAN capacity – **maximize existing investments**	Evolution to Cloud Platforms provide opportunity for **cloud-like innovation**: flexibility, scale & new revenue models

vRAN AND OPEN RAN

SYSTEM PLATFORM ARCHITECTURE

CUSTOM RAN

- Integration, apps
- Integrated appliances
- Custom ASICs

vRAN

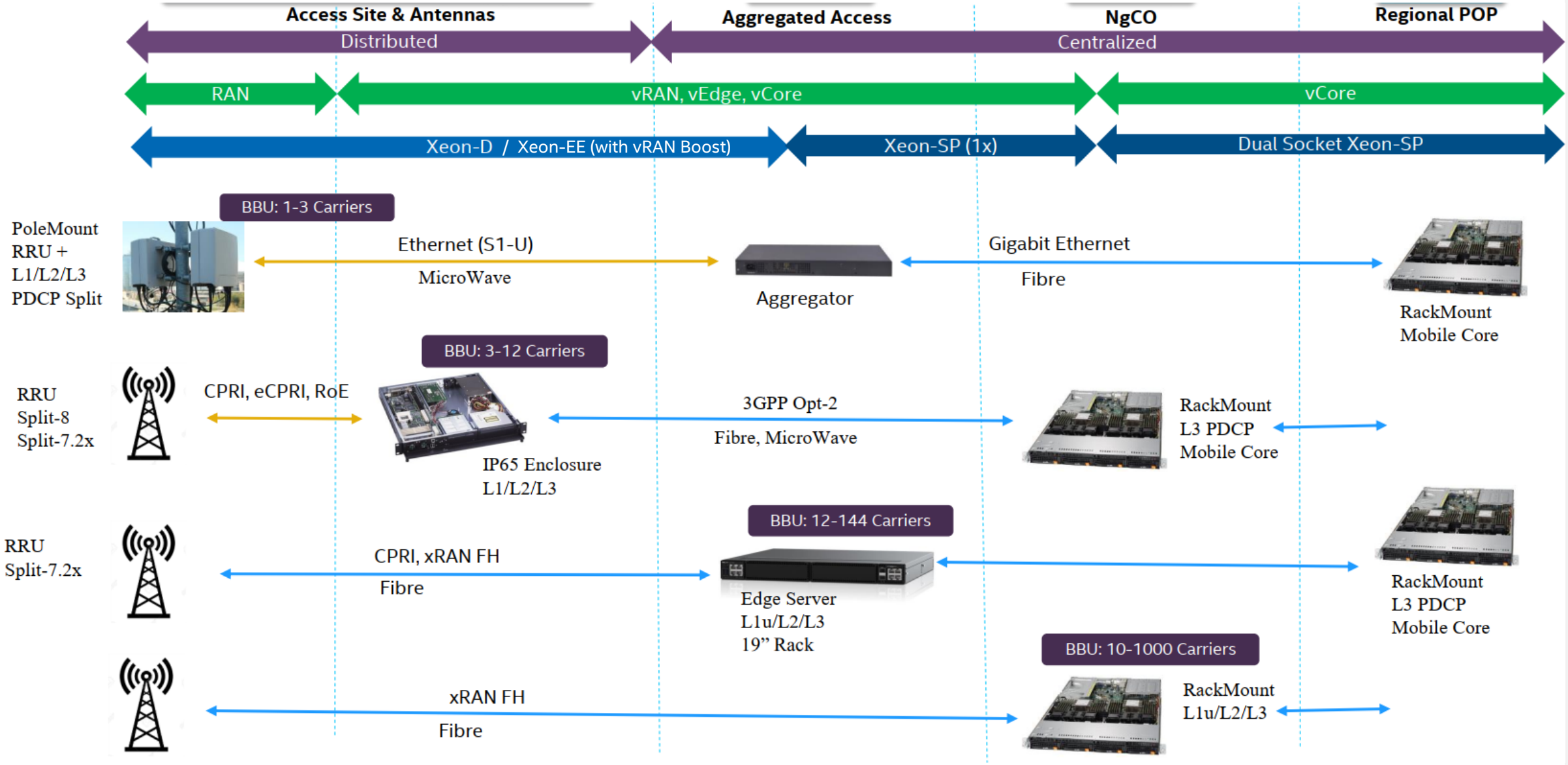
- 5G Services
- Infrastructure Software (orchestration, management)
- VNF software (vRAN, vCore)
- Server with standard Si

OPEN RAN

- Orchestration & Automation
- RAN Intelligent Controller near-RT
- Multi-RAT CU Protocol Stack
- NFVI Platform
- O-DU
- O-RU

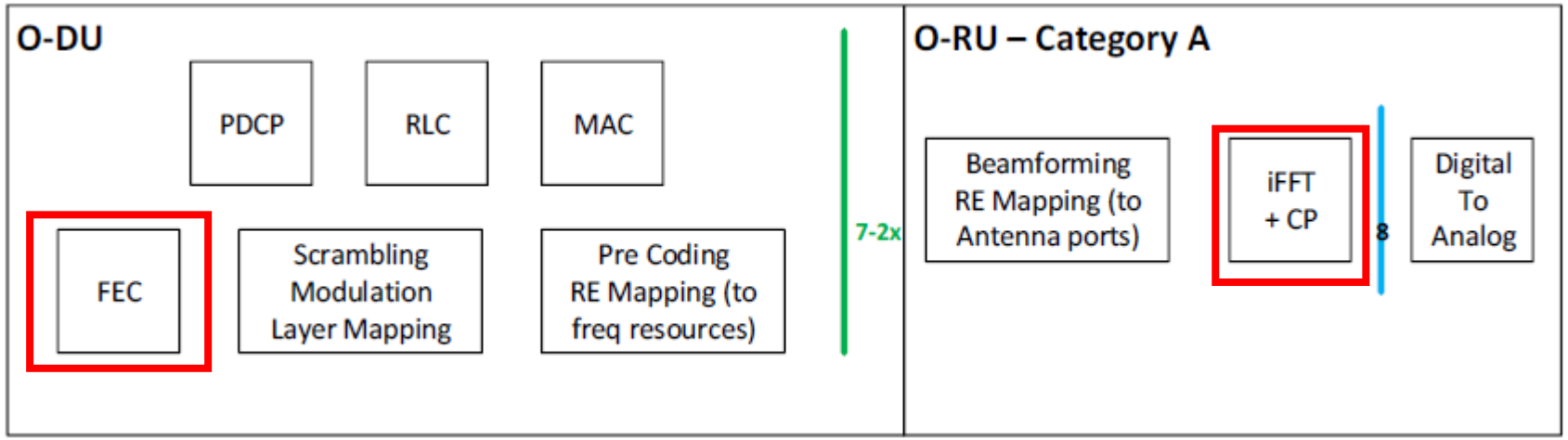
Proprietary and customized solutions by TEMs	Implementation of technologies leveraging **server based architecture** and software to perform traditional RAN function	**Standardized Interfaces** - Set of specifications defining interfaces between radio and base station RAN

Platform/Compute vs Site Example



ORAN FUNCTIONAL SPLIT

Layer 1 functionality between O-DU and O-RU

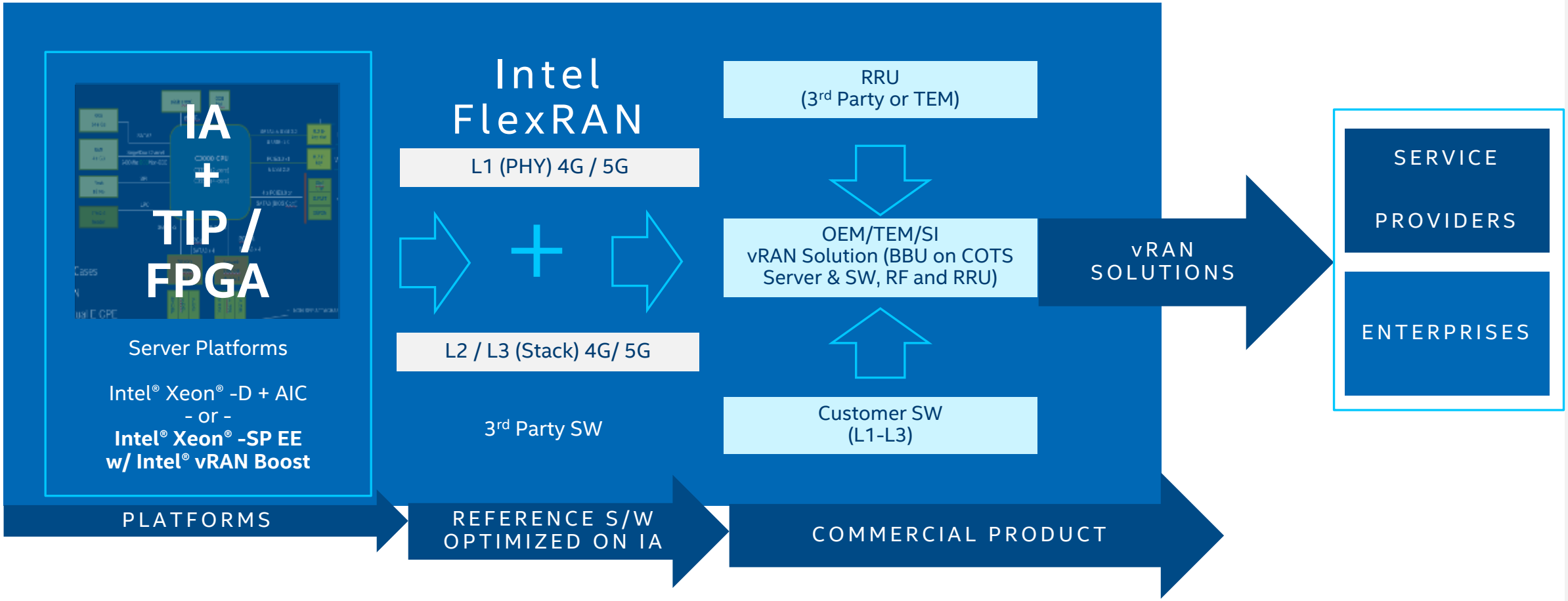


FlexRAN™ OVERVIEW

FlexRAN™ is a software reference architecture that enables customers to build 4G/5G RAN on Intel® architecture, including cloud-native and fully virtualized.

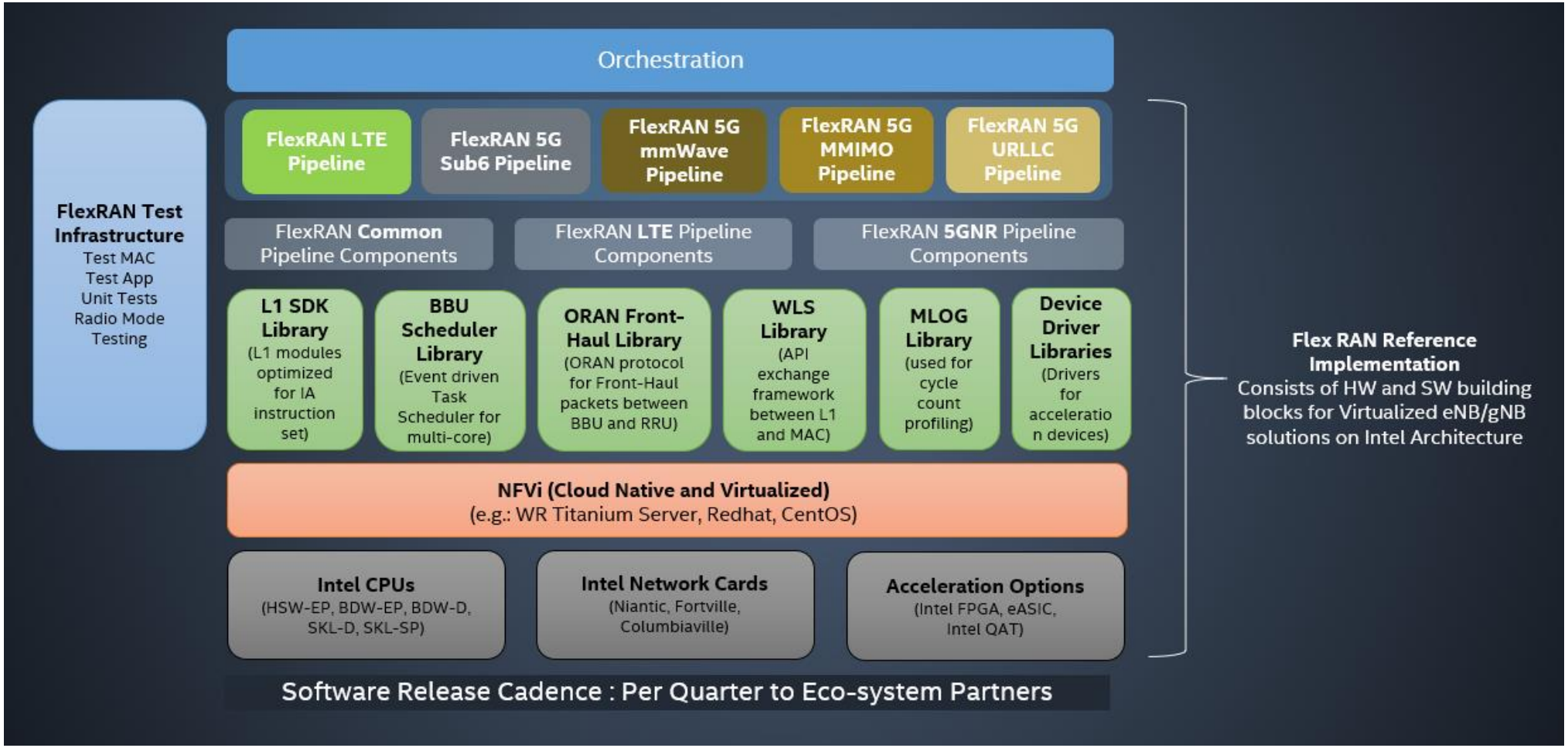
FlexRAN™ Target Segments	Broad RAN use cases: Indoor to Macro, Cloud to Distributed RAN and Rural.
Engagement Model	License agreement for use on Intel Silicon. Customers use the software as BKM and/or in products.
Market Objective	Enable the non-custom RAN ecosystem. Foster new RAN markets.

ECOSYSTEM ENABLING MODEL BASED ON FlexRAN™

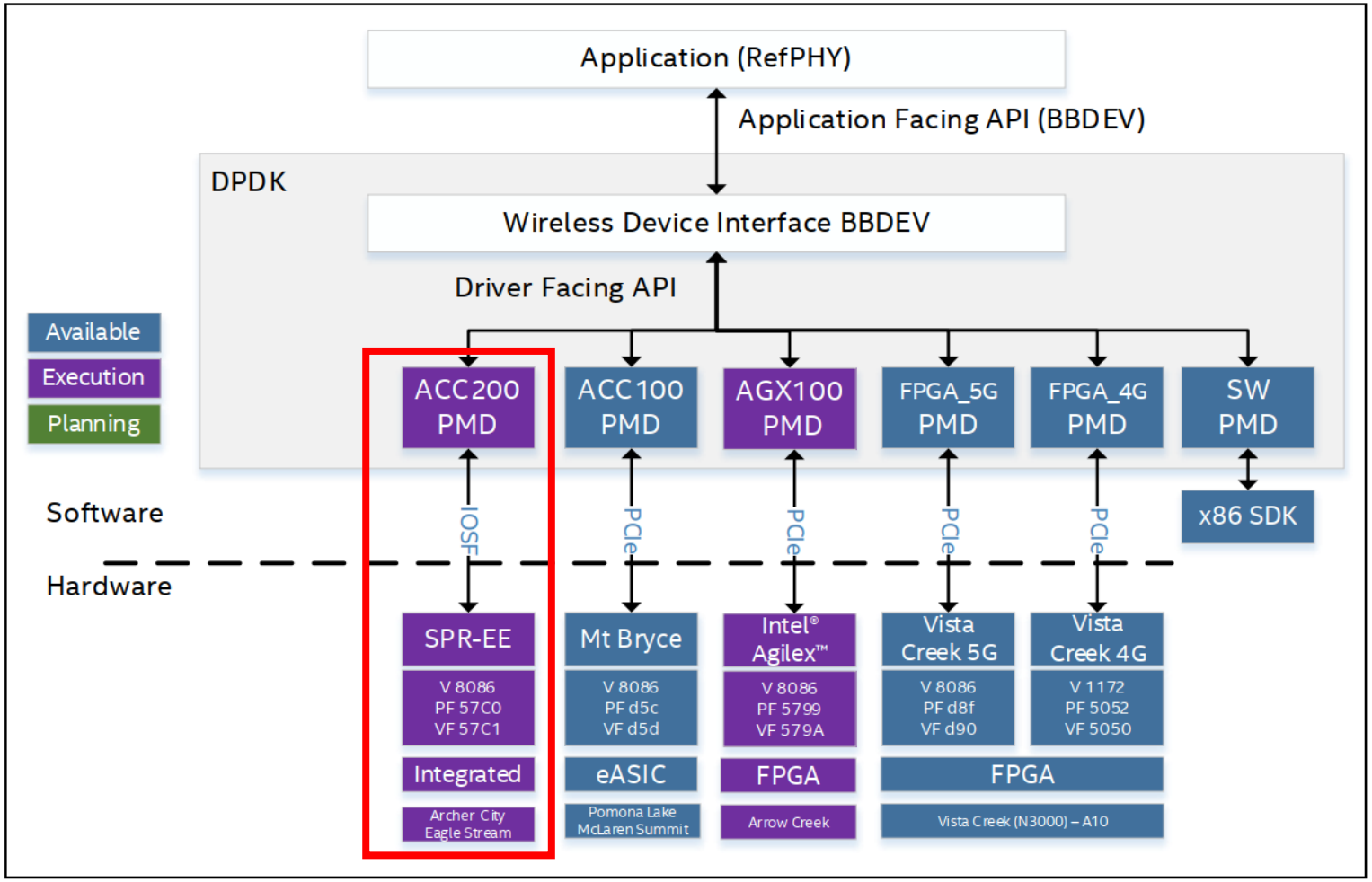


Intel collaborates with and fosters an ecosystem to accelerate the development of vRAN solutions

INTEL® FlexRAN™ ARCHITECTURE



DPDK AND BBDEV POOL MODE DRIVER (PMD)

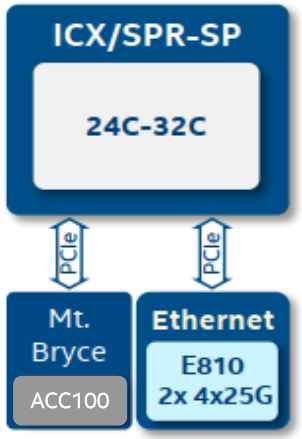
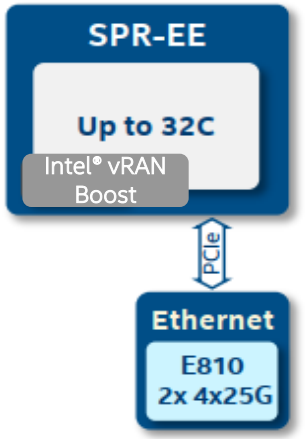


Intel® vRAN Boost

Intel® vRAN Boost (ACC200)

- vs -

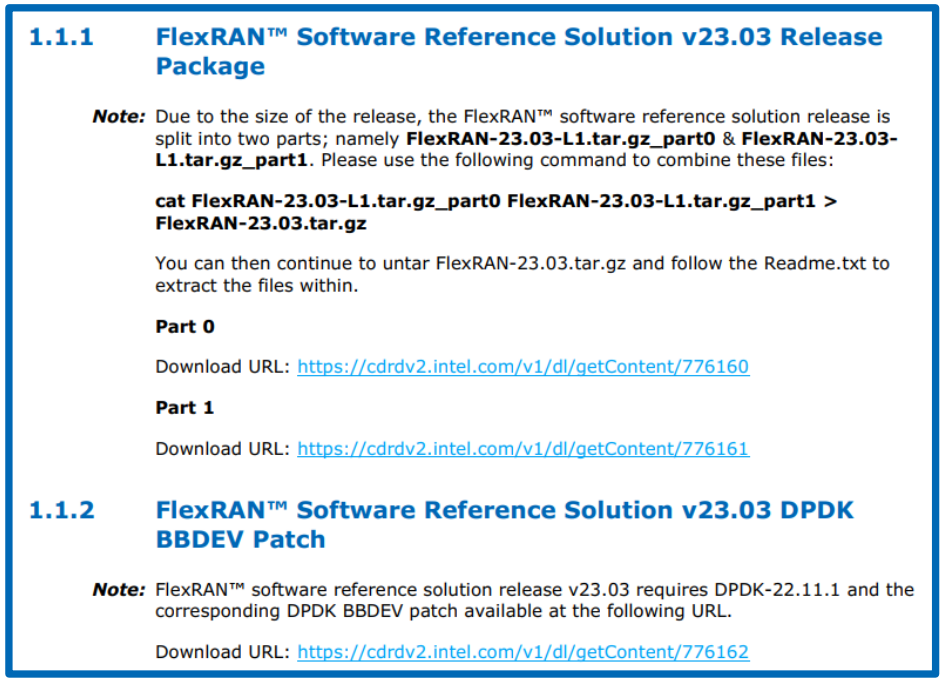
Previous Gen AIC (ACC100)

Platform Configs		
Use case	C-RAN and D-RAN	C-RAN and D-RAN
Baseband Accelerator Config	Discrete Adapter	Integrated, Monolithic CPU
5G FEC (mix of peak/avg, mMIMO**)	Encode = 21 Gbps Decode = 5.5 Gbps	Encode > 40 Gbps Decode > 15 Gbps
5G FEC (4T4R**)	Encode = 21 Gbps Decode = 4 Gbps	Encode > 21 Gbps Decode > 7 Gbps
4G FEC (4T4R**)	Encode = 6 Gbps Decode = 2.2 Gbps	Encode > 14 Gbps Decode > 4 Gbps
FFT Accelerator (SRS Offload)	N/A	SRS processing of 6x100 MHz in 1 TTI***
Accelerator Solution TDP	Up to ~50W	Included in CPU TDP
Memory Used	External DDR4	CPU Cache & DDR5
Process	28nm	Intel 7
Solution Area	35x35mm package	Integrated

Getting Started

Setup Ingredients

- Intel RDC only
- FlexRAN™ Software Release Announcement (Document Number: 645964)
- Main packages needed:
  - FlexRAN™ Software Reference Solution
  - DPDK Patch



1.1.1 FlexRAN™ Software Reference Solution v23.03 Release Package

Note: Due to the size of the release, the FlexRAN™ software reference solution release is split into two parts; namely **FlexRAN-23.03-L1.tar.gz_part0** & **FlexRAN-23.03-L1.tar.gz_part1**. Please use the following command to combine these files:

cat FlexRAN-23.03-L1.tar.gz_part0 FlexRAN-23.03-L1.tar.gz_part1 > FlexRAN-23.03.tar.gz

You can then continue to untar FlexRAN-23.03.tar.gz and follow the Readme.txt to extract the files within.

Part 0

Download URL: https://cdrdv2.intel.com/v1/dl/getContent/776160

Part 1

Download URL: https://cdrdv2.intel.com/v1/dl/getContent/776161

1.1.2 FlexRAN™ Software Reference Solution v23.03 DPDK BBDEV Patch

Note: FlexRAN™ software reference solution release v23.03 requires DPDK-22.11.1 and the corresponding DPDK BBDEV patch available at the following URL.

Download URL: https://cdrdv2.intel.com/v1/dl/getContent/776162

Setup Guide

- Install FlexRAN™ SDK
  - Refer to the *RefPhy Doxygen Documentation* (Document number: 603577)
  - Compilation steps are under **Section 4.1**

    Take note of the dependencies
  - Dependencies:
    - Toolkit - **OneAPI [ICX compiler]** <Based on the FlexRAN version, refer to compilation chapter>
    - Development kit – **DPDK + dpdk-kmods** <Based on the FlexRAN version, refer to compilation chapter>
    - Tools - **pf-bb-config** <latest>

Initialize and Test Intel® vRAN Boost with BBDev (1/4)

1. Get the PCI address of vRAN boost

```
1. Discover vRAN Boost PCI address

> lspci | grep acc
f7:00.0 Processing accelerators: Intel Corporation Device 57c0
```

2. Setup environment

```
2. Configure environment variables

export ACC_PCI_ADDR=0000:f7:00.0

export FLEXRAN_SRC=/home/flexran

export RTE_SDK=/opt/dpdk-stable-22.11.1

export RTE_SDK_KMOD=/opt/dpdk-kmods

export PF_BB_CONFIG=/opt/pf-bb-config

export UUID=00112233-4455-6677-8899-aabbccddeeff
```

Initialize and Test Intel® vRAN Boost with BBDev (2/4)

3. Bind PF device to vfio-pci

```
3. Bind PF device to vfio-pci

Load vfio-pci module:

> modprobe vfio-pci

> echo 1 | tee /sys/module/vfio_pci/parameters/enable_sriov
1

> echo 1 | tee /sys/module/vfio_pci/parameters/disable_idle_d3
1

> /opt/dpdk-stable-22.11.1/usertools/dpdk-devbind.py --bind=vfio-pci 0000:f7:00.0

> /opt/dpdk-stable-22.11.1/usertools/dpdk-devbind.py -s

Network devices using kernel driver
===================================
0000:01:00.0 'Ethernet Controller I225-LM 15f2' if=enp1s0 drv=igc unused=igb_uio,vfio-pci *Active*
0000:04:00.0 'Ethernet Controller X710 for 10GbE SFP+ 1572' if=enp4s0f0 drv=i40e unused=igb_uio,vfio-pci
0000:04:00.1 'Ethernet Controller X710 for 10GbE SFP+ 1572' if=enp4s0f1 drv=i40e unused=igb_uio,vfio-pci
0000:70:00.0 'Ethernet Controller E810-C for QSFP 1592' if=ens11f0 drv=ice unused=igb_uio,vfio-pci
0000:70:00.1 'Ethernet Controller E810-C for QSFP 1592' if=ens11f1 drv=ice unused=igb_uio,vfio-pci

Baseband devices using DPDK-compatible driver
=============================================
0000:f7:00.0 'Device 57c0' drv=vfio-pci unused=igb_uio
```

Initialize and Test Intel® vRAN Boost with BBDev (3/4)

4. Create VF device

```
4. Create VF device

> echo 16 | tee /sys/bus/pci/devices/0000:f7:00.0/sriov_numvfs
16

export ACC_PCI_ADDR_VFS=f7:00.1
f7:00.2
f7:00.3
f7:00.4
f7:00.5
f7:00.6
f7:00.7
f7:01.0
f7:01.1
f7:01.2
f7:01.3
f7:01.4
f7:01.5
f7:01.6
f7:01.7
f7:02.0

> export ACC_PCI_ADDR_VF0=0000:f7:00.1

> export ACC_PCI_ADDR_VF1=0000:f7:00.2
```

Initialize and Test Intel® vRAN Boost with BBDev (4/4)

5. Configure queues for accelerator with VF mode

```
5. Configure queues for accelerator with VF mode

> /opt/pf-bb-config/pf_bb_config ACC200 -v 00112233-4455-6677-8899-aabbccddeeff -c /opt/pf-bb-config/acc200/acc200_config_16vf.cfg
== pf_bb_config Version #VERSION_STRING# ==
Log file = /var/log/pf_bb_cfg_0000:f7:00.0.log
```

Test Applications

Test-BBDev

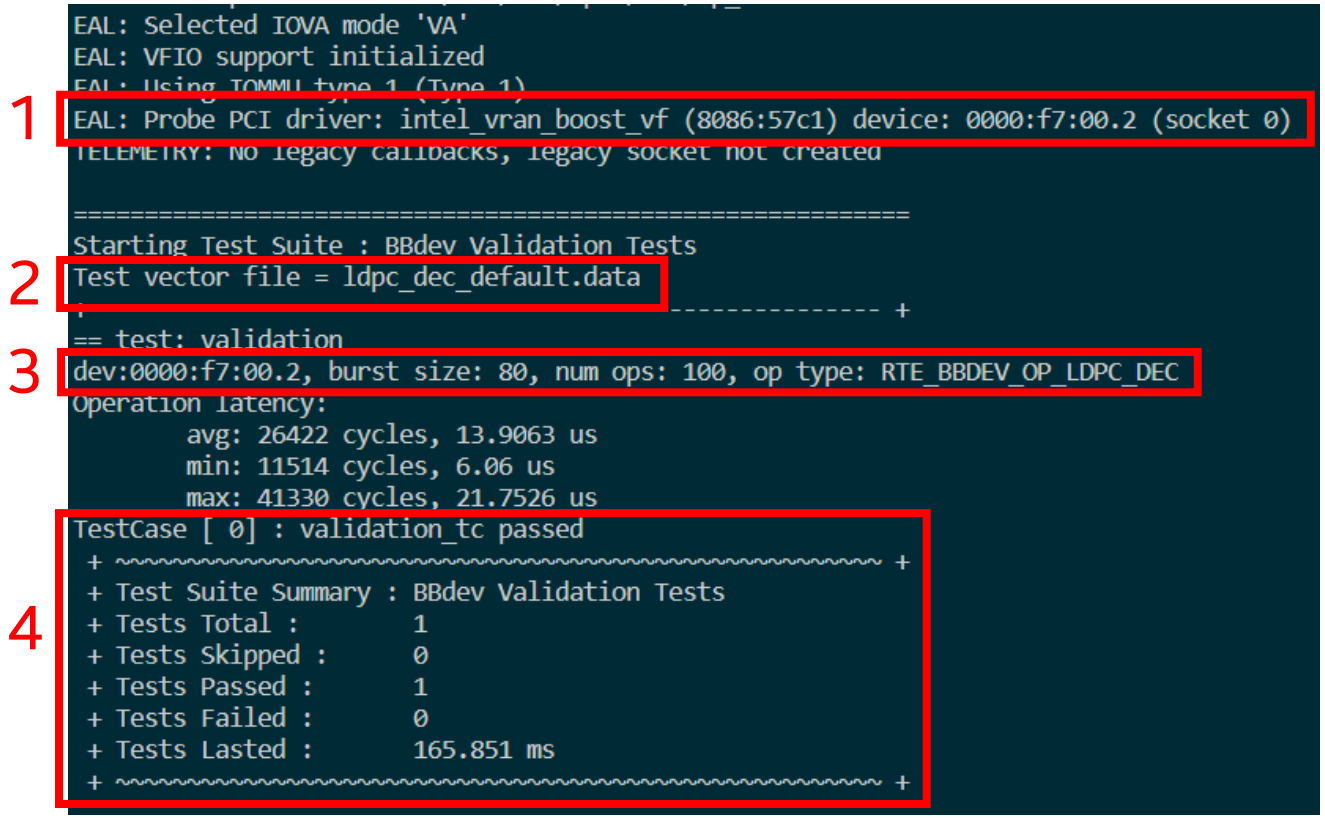
- Running validation for a single code block

```
Run test app: test-bbdev

> source /home/flexran/set_env_var.sh -d -i spr ; icx --version ; cd /opt/dpdk-stable-22.11.1/app/test-bbdev/ ; ./test-bbdev.py -e='-c
0xff0 -a 0000:f7:00.2 --vfio-vf-token=00112233-4455-6677-8899-aabbccddeeff' -t 6 -n 100 -b 80 -l 1 -c validation -v ldpc_dec_default.da
ta
```

https://doc.dpdk.org/guides/tools/testbbdev.html

Test-BBDev



Section 1 - Check for the PCIe address for the FEC accelerator.

Section 2 - Check for the current vector file. This is essential when multiple test vectors are run.

Section 3 - Check that the number of queues mentioned here match with the ones during configuration.

Section 4 - Check for Test Result

BBDevApp

- Run configured 5G workload for performance test

```
$ cd $FLEXRAN_SRC/bin/nr5g/gnb/bbdevapp
$ ./run.sh
```

NOTE: Change `bbdev_cfg.xml` based on test criteria.

- Set DPDK Baseband Device of the HW accelerator with the value of ACC_PCI_ADDR_VF0 or ACC_PCI_ADDR_VF1.
- Set DPDK IOVA Mode based on device type.
- Make sure DPDK BBDev FEC is set to use HW acceleration.

BBDevApp - Performance Measurement

Macro C-RAN - 6 x 100 MHz (6 Average 80% RB 8/4 Layers - 64TR) - FEC 5GUL + FEC 5GDL + FFT

Downlink - Encoder (Peak cell)

%	RBs	Sym	UEs	Layers	Qm	R	MCS	Tp	Spect Eff
100%	272	12	16	16	8	0.93	27	4641	7.4

Downlink - Encoder (Average cell 80%)

%	RBs	Sym	UEs	Layers	Qm	R	MCS	Tp	Spect Eff
20%	44	12	4	16	8	0.93	27	751	7.4
50%	109	12	6	8	6	0.93	28	697	5.6
30%	66	12	6	4	4	0.64	16	98	2.6
Average	219	12	16	8.4	6.5	0.9	26	1546	5.8
Total DL Slot Throughput (6 cells 0P+6A)							**18.6**	**Gbps**	

Measurements			
	FEC DL Total acceleration duration (us)	150	us
	Equivalent HW DL Throughput	62	Gbps

Uplink - Decoder (Peak cell)

%	RBs	Sym	UEs	ReTx	Iters	Layers	Qm	R	MCS	Tp	Spect Eff
100%	272	10	4	10%	15	8	8	0.93	27	1934	7.4

Uplink - Decoder (Average cell 80%)

%	RBs	Sym	UEs	ReTx	Iters	Layers	Qm	R	MCS	Tp	Spect Eff
20%	44	10	4	10%	15	8	8	0.93	27	313	7.4
49%	109	10	6	10%	15	4	6	0.93	28	291	5.6
30%	66	10	6	10%	15	2	4	0.64	16	41	2.6
Average	219	10	16	10%	15	4.2	6.2	0.9	24.5	644	5.5
Total UL Slot Throughput (6 cells 0P+6A)								**7.7**		**Gbps**	

Measurements			
	FEC UL Total acceleration duration (us)	230	us
	Equivalent HW UL Throughput	17	Gbps

```
========== tiapp Time: 2000 TTI 0 0 439347 ==========
-----------------------------------------------------------------
      Cell        DL Tput     UL Tput     FFT Tput    MLD Tput
     0 (Kbptti)  1,546,816     643,216     786,432           0    UEs 16  ReTx 10%
     1 (Kbptti)  1,546,816     643,216     786,432           0    UEs 16  ReTx 10%
     2 (Kbptti)  1,546,816     643,216     786,432           0    UEs 16  ReTx 10%
     3 (Kbptti)  1,546,816     643,216     786,432           0    UEs 16  ReTx 10%
     4 (Kbptti)  1,546,816     643,216     786,432           0    UEs 16  ReTx 10%
     5 (Kbptti)  1,546,816     643,216     786,432           0    UEs 16  ReTx 10%
    Total (Mbps)     18,560       7,718       9,436           0
-----------------------------------------------------------------
      Stats Func:        Count     Min     Avg     Max
         DL PREP (us):    2000   16.00   17.26  162.00
      DL ENQUEUE (us):    2000    6.00    7.09   46.00
         DL POLL (us):    2000   13.00  107.77  124.00
         UL PREP (us):    2000   19.00   20.23  152.00
      UL ENQUEUE (us):    2000   18.00   19.88  121.00
         UL POLL (us):    2000  184.00  230.06  244.00
        SRS PREP (us):    2000    4.00    5.13   51.00
     SRS ENQUEUE (us):    2000    5.00    6.09   32.00
        SRS POLL (us):    2000  404.00  418.32  433.00
-----------------------------------------------------------------
      UL HW LAT  (us):    2000  202.00  236.65  250.00    15.00 Iters
      DL HW LAT  (us):    2000  133.00  137.73  189.00
      FT HW LAT  (us):    2000  405.00  418.41  433.00
      FEC UL Throughput (Gbps):          16.31
      FEC DL Throughput (Gbps):          67.38
         FFT Throughput (GBps):          11.28    (7.5 GCps - 294M FFTps)
-----------------------------------------------------------------
DUL OFFSET (us):    2000   21.00   22.69  142.00
BBDEV Status 876 112
=================================================================
Test Completed after 2001 TTIs 439000 439293
```

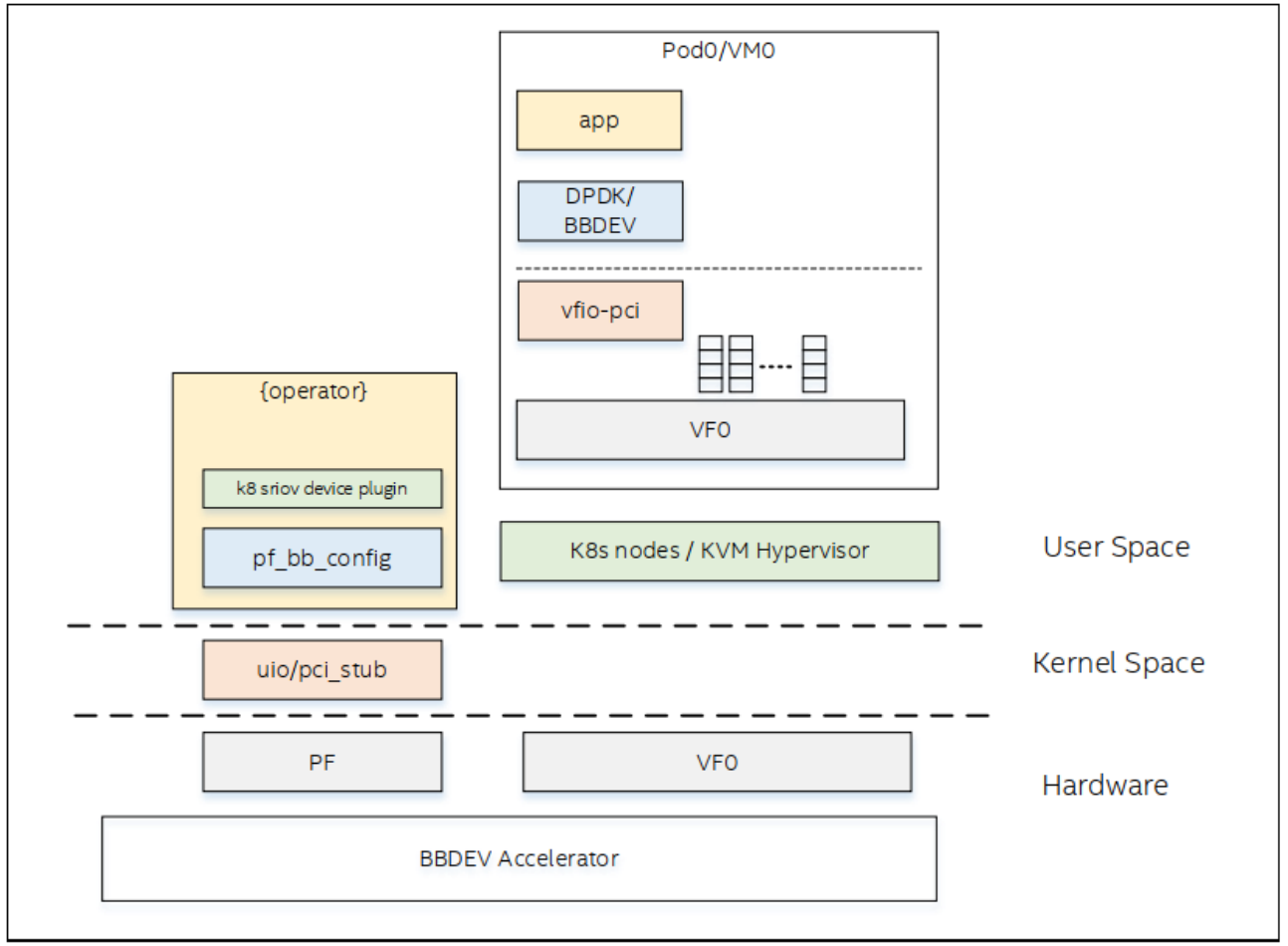
FFT based SRS Processing - cell configuration

Load %	RBs	Comb	RB/UE	CsNum	Ants	Sym	DS	UEs	iFFT Sizes	FFT Num	egress Tp
100%	272	4	272	4	64	1	4	16	1024 256	1280	1671
Total SRS Slot Throughput (6 cells)								**10.0**		**GBps (after depadding)**	

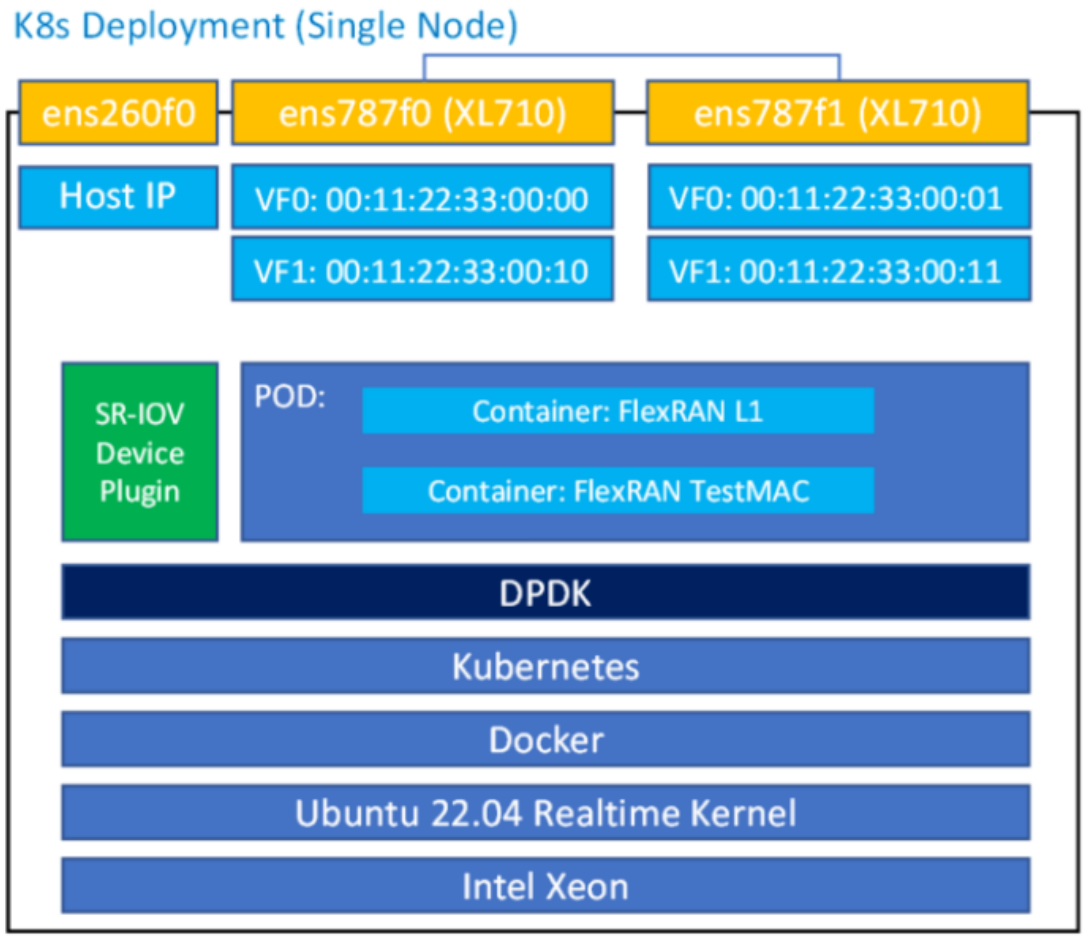
Measurements			
	FFT Total acceleration duration (us)	460	us
	Equivalent HW FFT Throughput	11	GBps (after depadding)
		17	MFFTps
		7	GCps (IQ)

Cloud-Native Use Cases

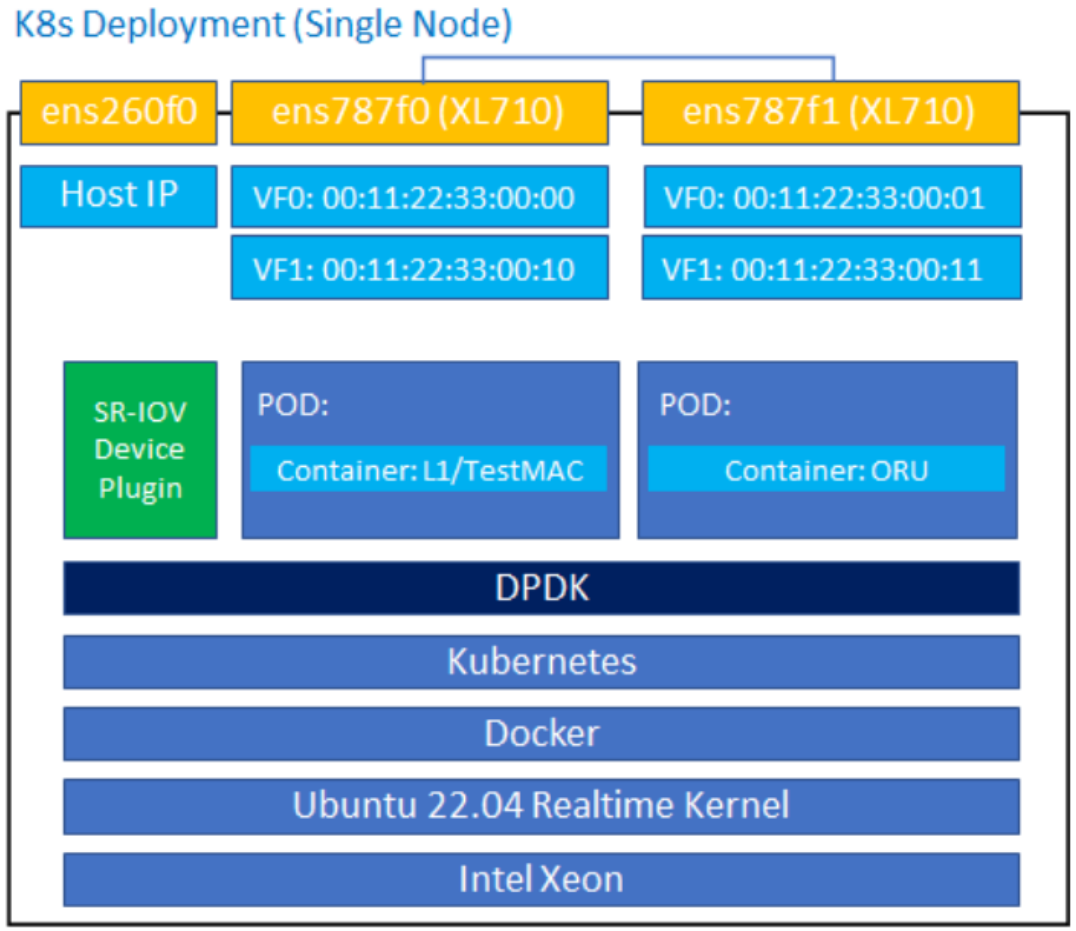
Containerized Environment



Reference Setup - Timer Mode



Reference Setup - xRAN Mode



Reference

- FlexRAN™ Reference Architecture for Wireless Access

  https://www.intel.com/content/www/us/en/developer/topic-technology/edge-5g/tools/flexran.html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