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Hot Chips 2023

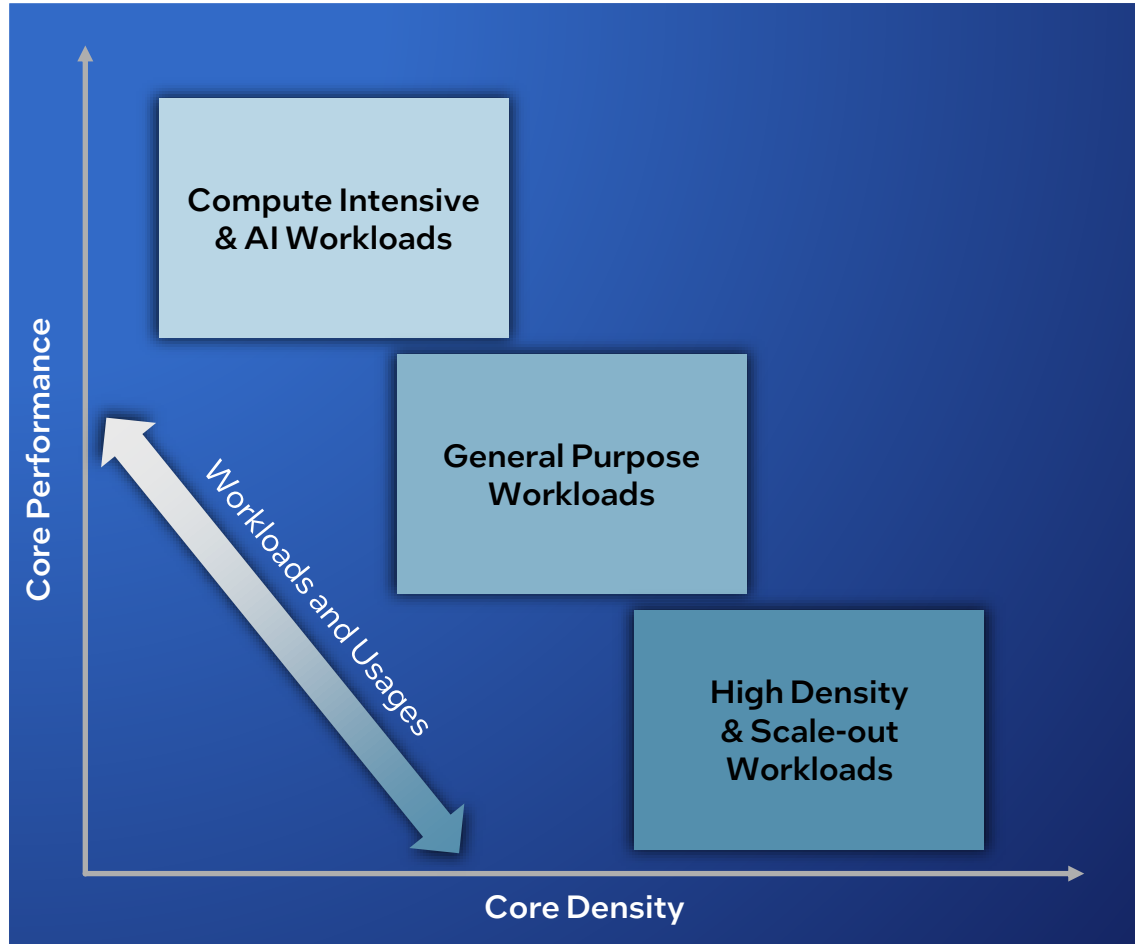
Architecting for Flexibility and Value with Next Gen Intel[®] Xeon[®] Processors

Chris Gianos

Intel Fellow, Datacenter Processor Architecture



Data Center Requirements Are Expanding



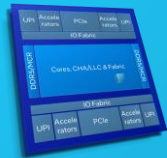
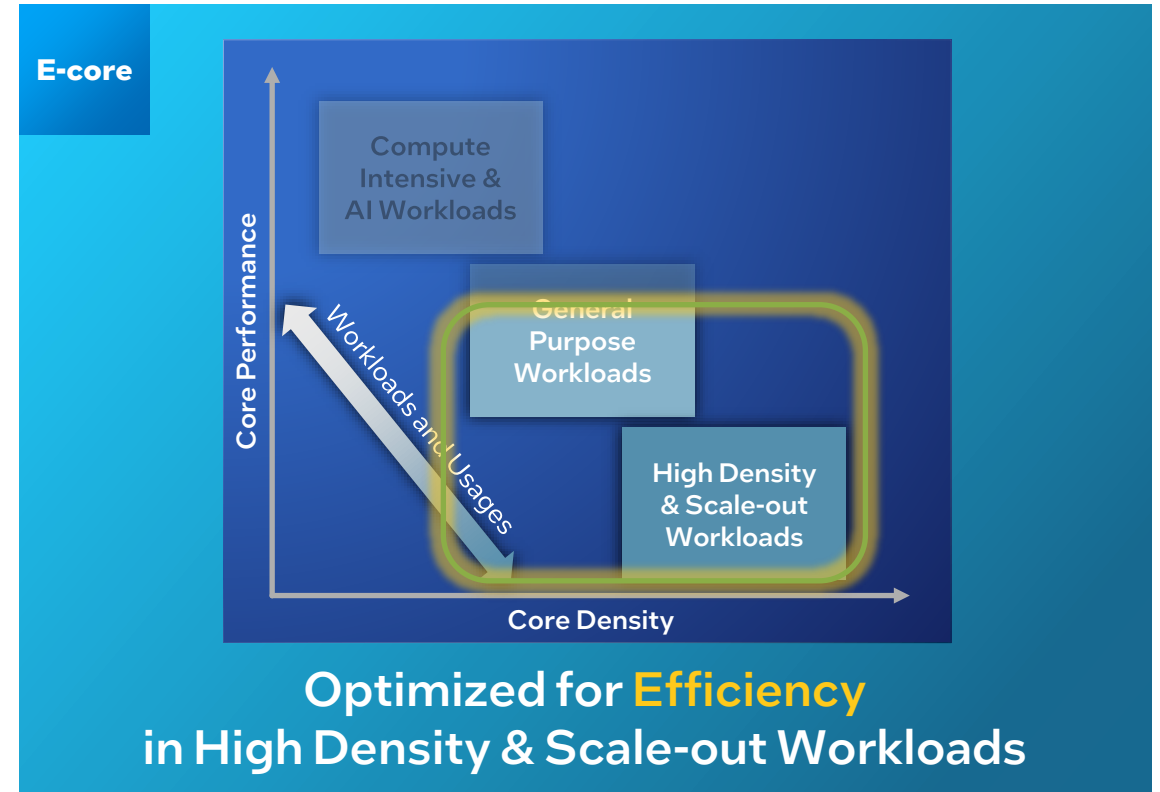
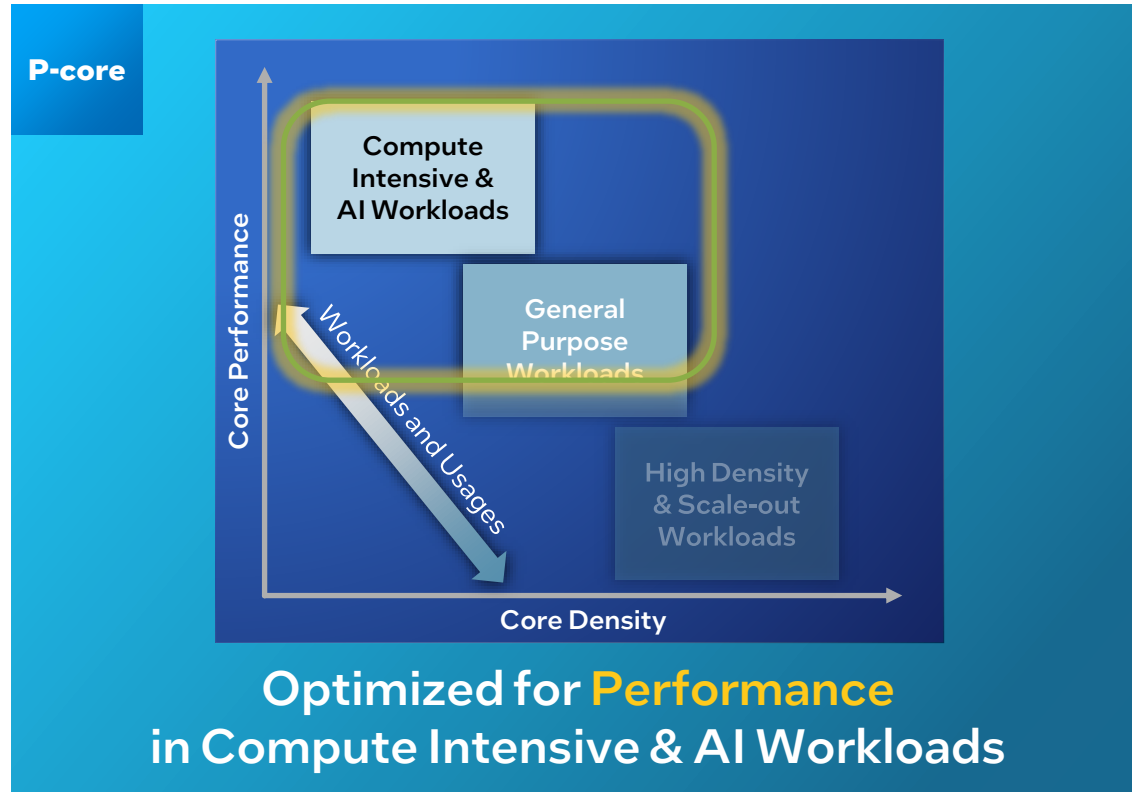
Continuing demand for CPU cores that deliver high performance per core

Growing demand for cores that deliver better density and the best performance per watt at specific performance levels

Optimizing for specific types of workloads requires trade-offs between core performance & core density

Expanding deployment models demanding increased power, IO & memory bandwidth

Expanded Xeon Portfolio with Optimized Processors



Common Platform Foundation
& Shared Software Stack



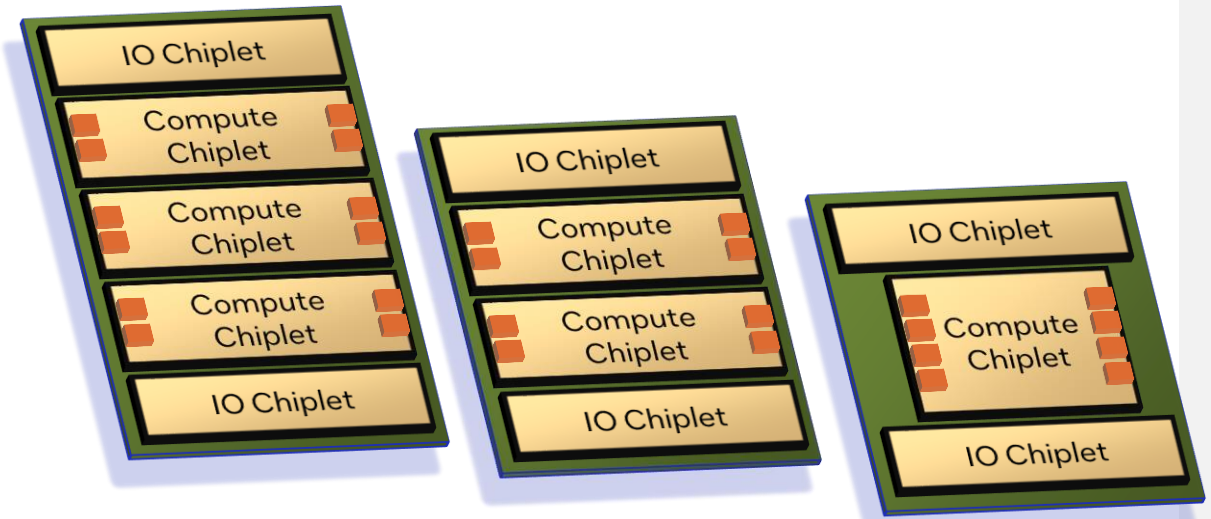
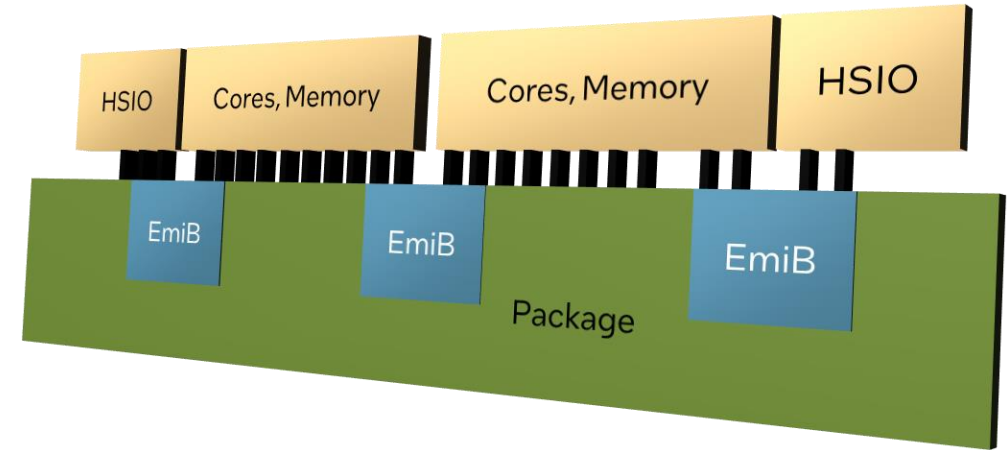
Modular SoC Architecture

Component Details

- Separate Compute and IO silicon chiplets
- EmiB packaging -> high bandwidth / low latency
- Modular die fabric enables flexible construction
- Common IP, Firmware, OS, platform ingredients

Platform Details

- Scalability: 1S-8S (P-core), 1S-2S (E-core)
- Supports range of core counts and thermals
- Memory: up to 12-channels DDR/MCR, 1-2DPC
- Advanced I/O up to 136 lanes PCIe 5.0/CXL 2.0, up to 6 UPI links (144 lanes)
- Self boot

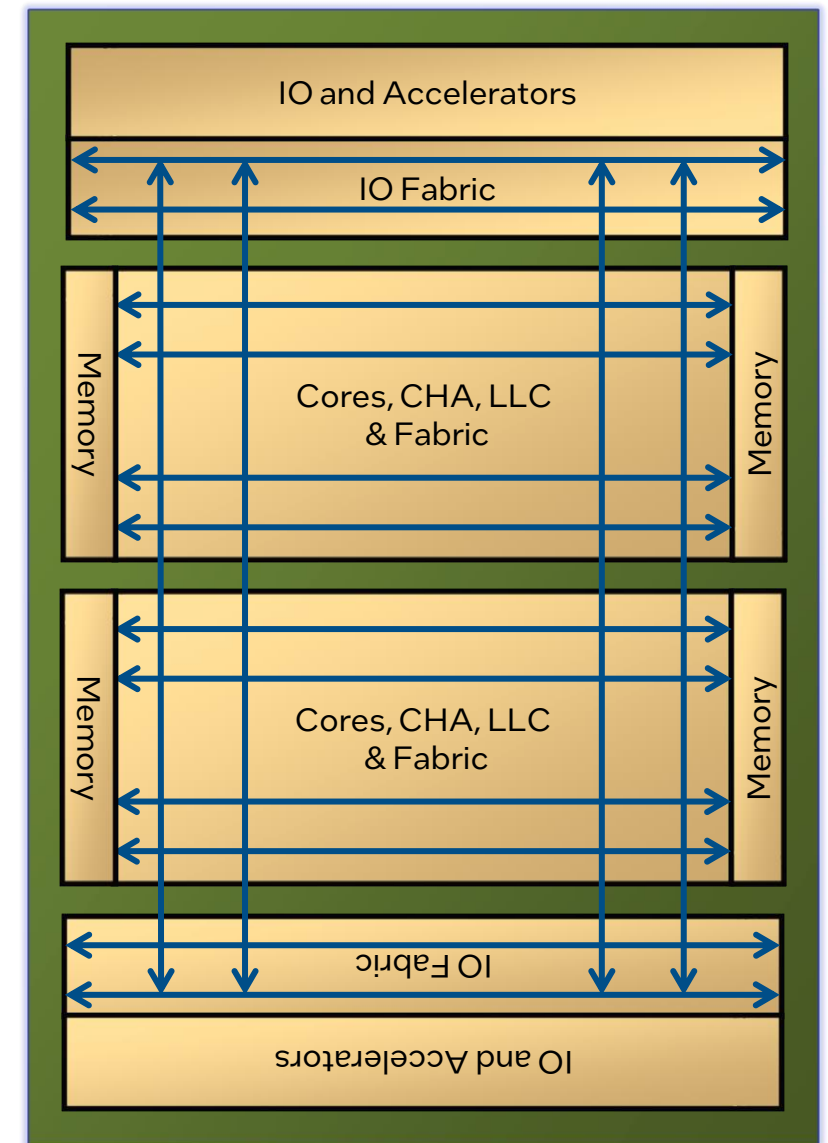


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Scalability and Flexibility to Deliver a Wide Range of Optimized Products

Modular Mesh Fabric

- Logically Monolithic Mesh enables direct access between agents within the socket
- Last level cache is shared amongst all cores and can be partitioned into per-die sub-numa clusters
- EmiB technology extends the high-speed fabric across all die in the package
- Modularity and flexible routing allows per-die definition of rows and columns
- Fabric distributes IO traffic across multiple columns to ease congestion
- Global infrastructure is modular/hierarchical



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Mesh Superhighway scales naturally from small to large configs

Compute Die Architecture

Construction

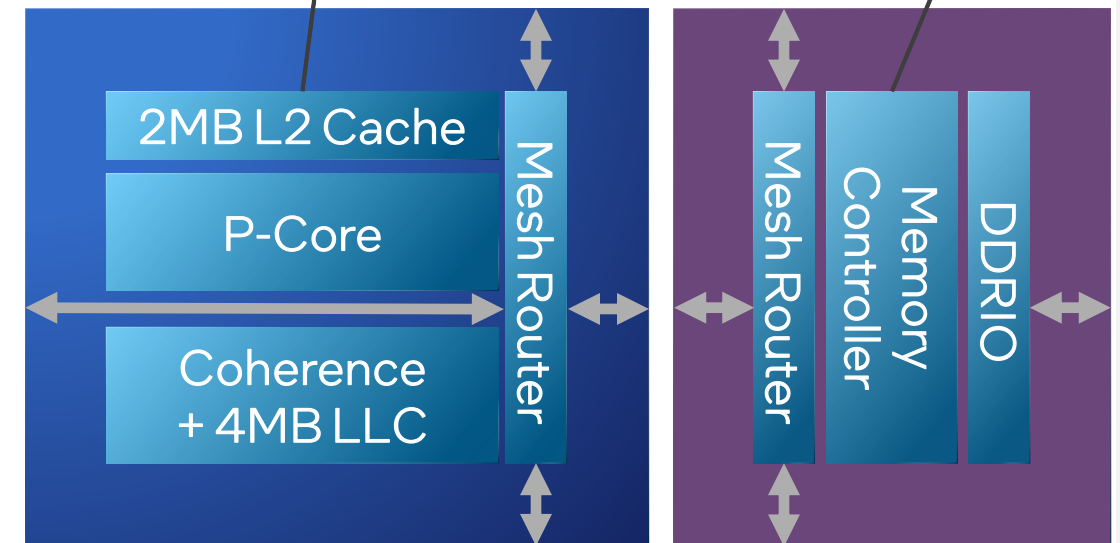
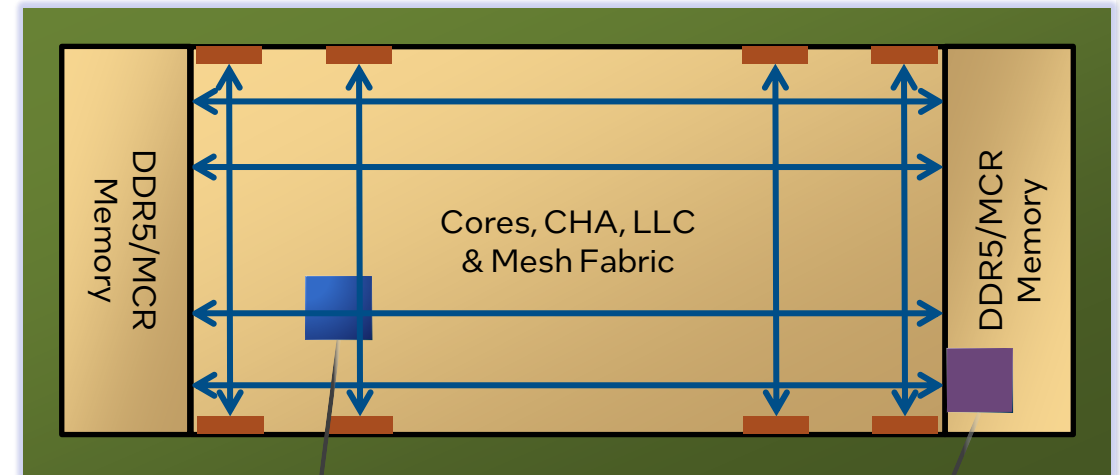
- Higher Performance & Efficiency with Intel 3 process
- Flexible row/column die structure

Core Tile (Mesh building block)

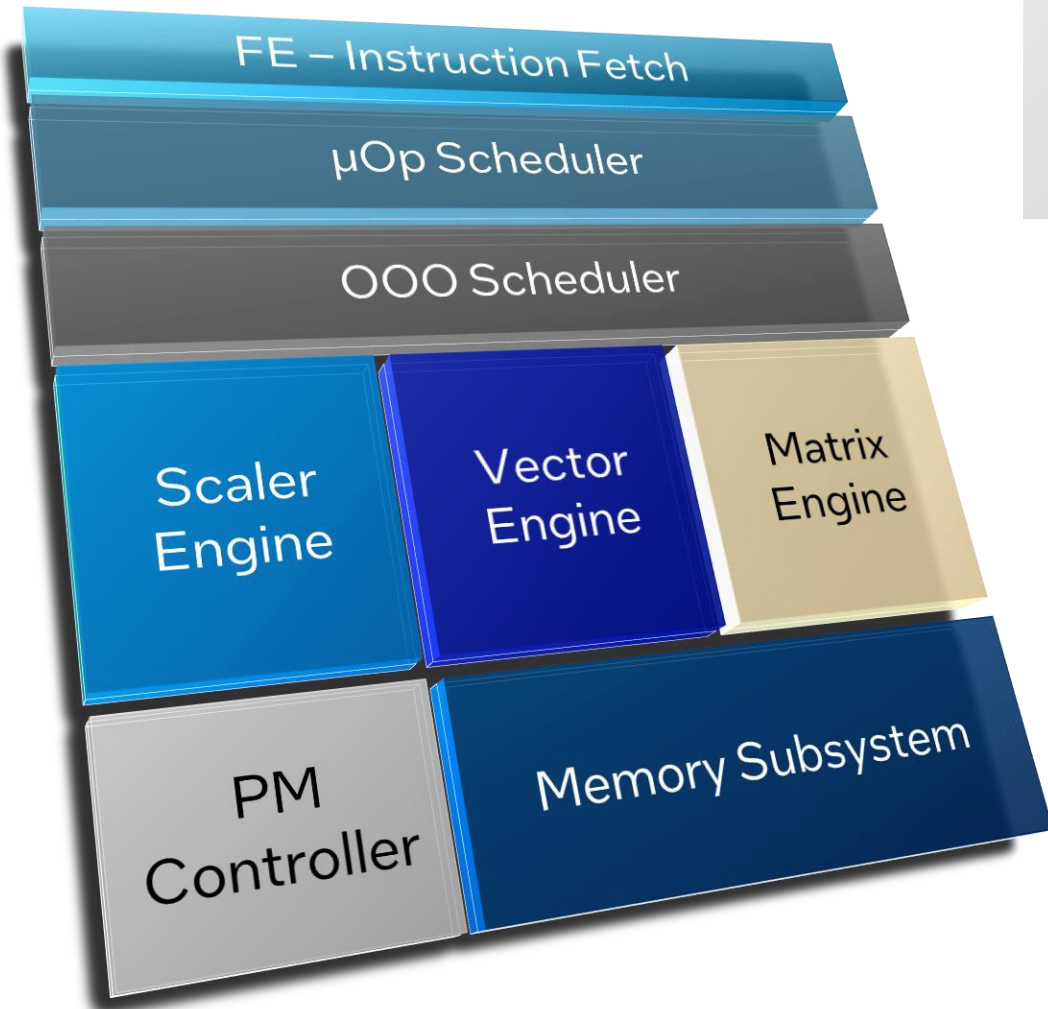
- Contains Core+L2, LLC+SF+CHA slice, mesh fabric interface
- Adaptable to multiple architectures
 - Granite Rapids = P-Core Tiles (RedwoodCove)
 - Sierra Forest = E-Core Tiles (Sierra Glen)

Advanced Memory System

- Common controller/IO supports DDR or MCR memory
- Full support for CXL attached memory



Performance Optimized Core



Proven Intel Xeon Architecture

- Optimized for high performance per core
- Built on the latest Intel 3 process technology
- Improved power efficiency

New Software Capabilities

- Matrix Engine supports FP16 for AI/ML
- More memory encryption keys w/ 256b strength
- Code SW prefetch and taken branch hints
- Per-Thread memory bandwidth allocation
- L2 cache allocation and code/data prioritization

Enhanced µArch

- 64KB, 16-way I-cache
- Improved branch predictor and mis-recovery
- 3-cycle FP multiplication
- More outstanding memory requests and prefetch capabilities

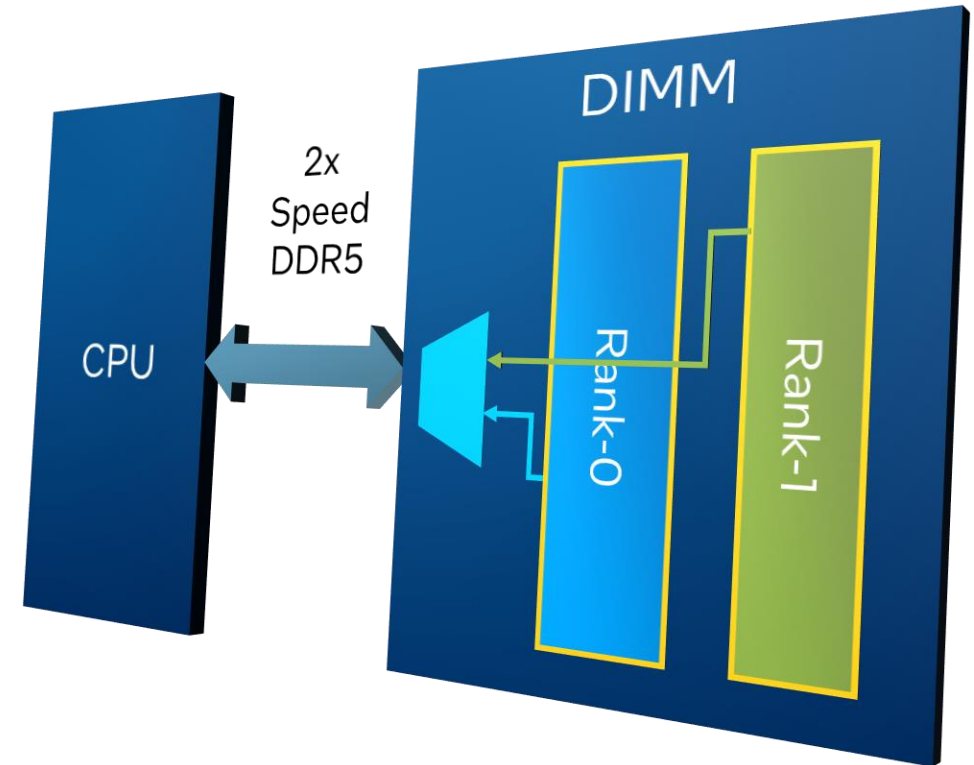
Multiplexed Combined Rank DIMMs

Problem

- New workloads benefiting from more BW/thread
- Adding DIMMs to deliver BW is expensive
- Prefer to increase memory BW @ iso capacity/core

MCR Details

- Fully platform compatible with DDR5 RDIMMs
- Mux merges two ranks at 1x speed into channel running at 2x speed
- Each Rank operates at half the channel speed
- JEDEC standardization in progress today
- Achieving 30-40% more BW than RDIMM



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MCR DIMMs add bandwidth without the cost of excess capacity

CXL Attached Memory

SW tiering with independent regions

- Interleaving within regions

HW tiering through heterogenous interleaving

- Single native DDR + CXL memory region

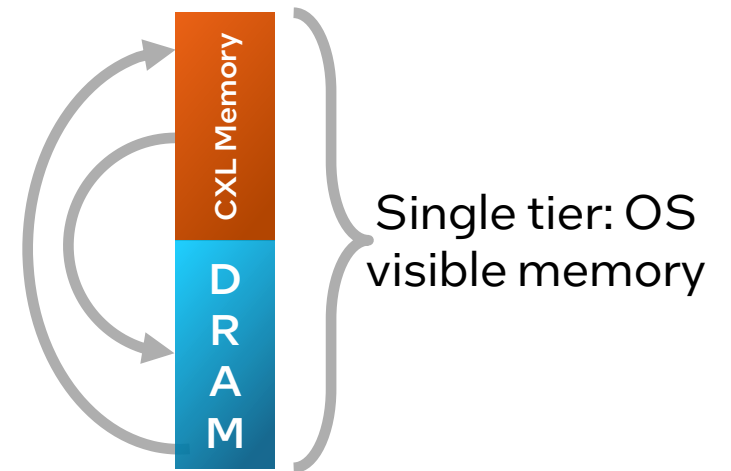
HW tiering with Intel Flat Memory Mode

- Cacheline granular movement
- All memory is addressable (vs. cached)
- Hot lines stay in lower latency memory

HW tiering is fully SW transparent

Flat Memory Mode (1:1 ratio)

50% CXL
memory
+
50% DRAM



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CXL Memory is a cost efficient, flexible, first-class solution

I/O Die Architecture

Universal IO stacks

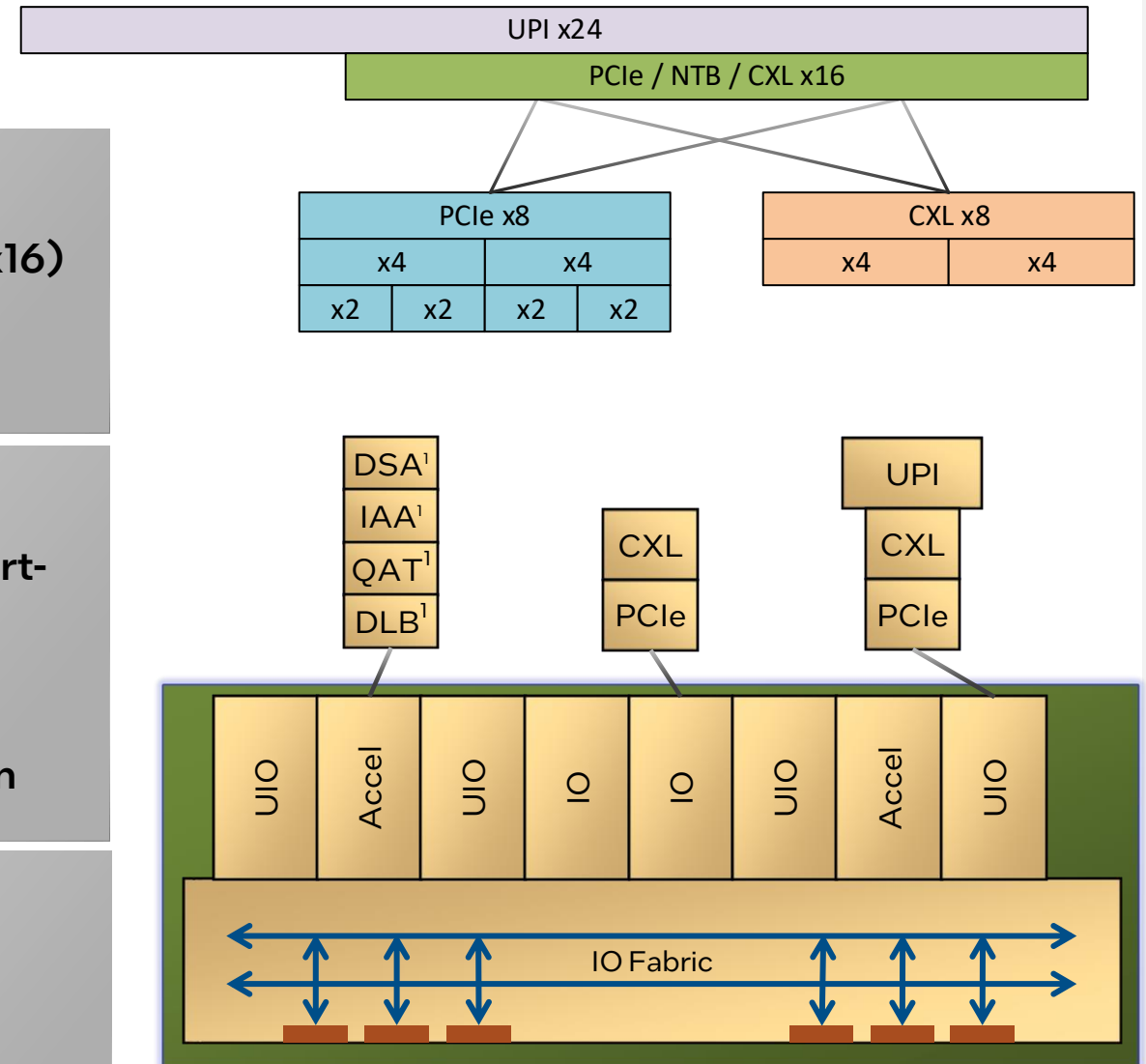
- Each port can operate as UPI (x24), PCIe(x16), CXL(x16)
- PCIe and CXL can be intermixed at x8 granularity
- Integrated workload accelerator engines

New IO Capabilities

- Full CXL 2.0 support - Memory pooling, interleave, port-bifurcation, hot-plug, etc.
- IO RDT – Extends RDT’s resource monitoring and control to I/O devices and channels
- Secure Interconnect – UPI/PCIe/CXL Link Encryption

Enhanced IO performance

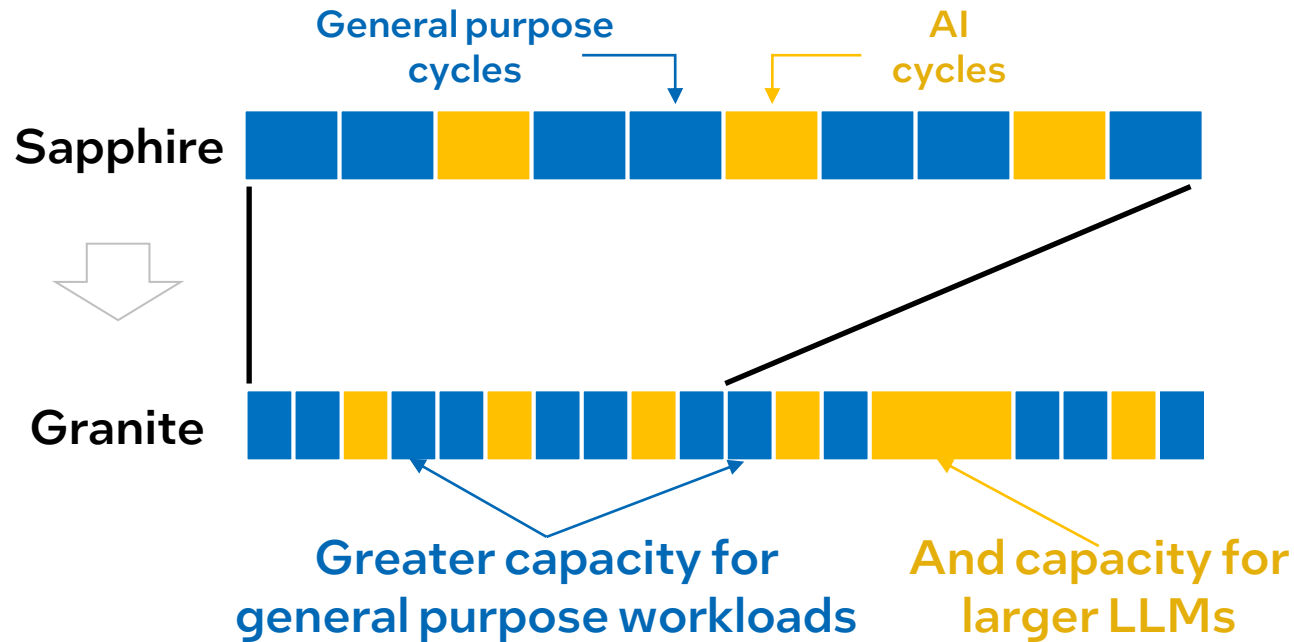
- UPI @ 24GT/s. w/6-links = 1.8x prior gen
- UPI Affinity – keeps traffic closer to the cluster
- Accelerator interface = 64B/cycle = 2x prior gen, 2x DSA
- IO die fabric distributes traffic across all mesh columns



¹Intel® Data Streaming Accelerator (Intel® DSA)
 Intel® In-Memory Analytics Accelerator (Intel® IAA)
 Intel® QuickAssist Technology (Intel® QAT)
 Intel® Dynamic Load Balancer (Intel® DLB)

AI is Everywhere

AI is one of many workloads running on the same infrastructure



Memory Bandwidth

- MCR memory provides 30-40% more BW
- 12 channels provides 1.5x prior gen
- Overall >2.5x prior generation

Socket Scaling

- Higher core count vs prior gen
- ~1/2 GB Last Level Cache for large models

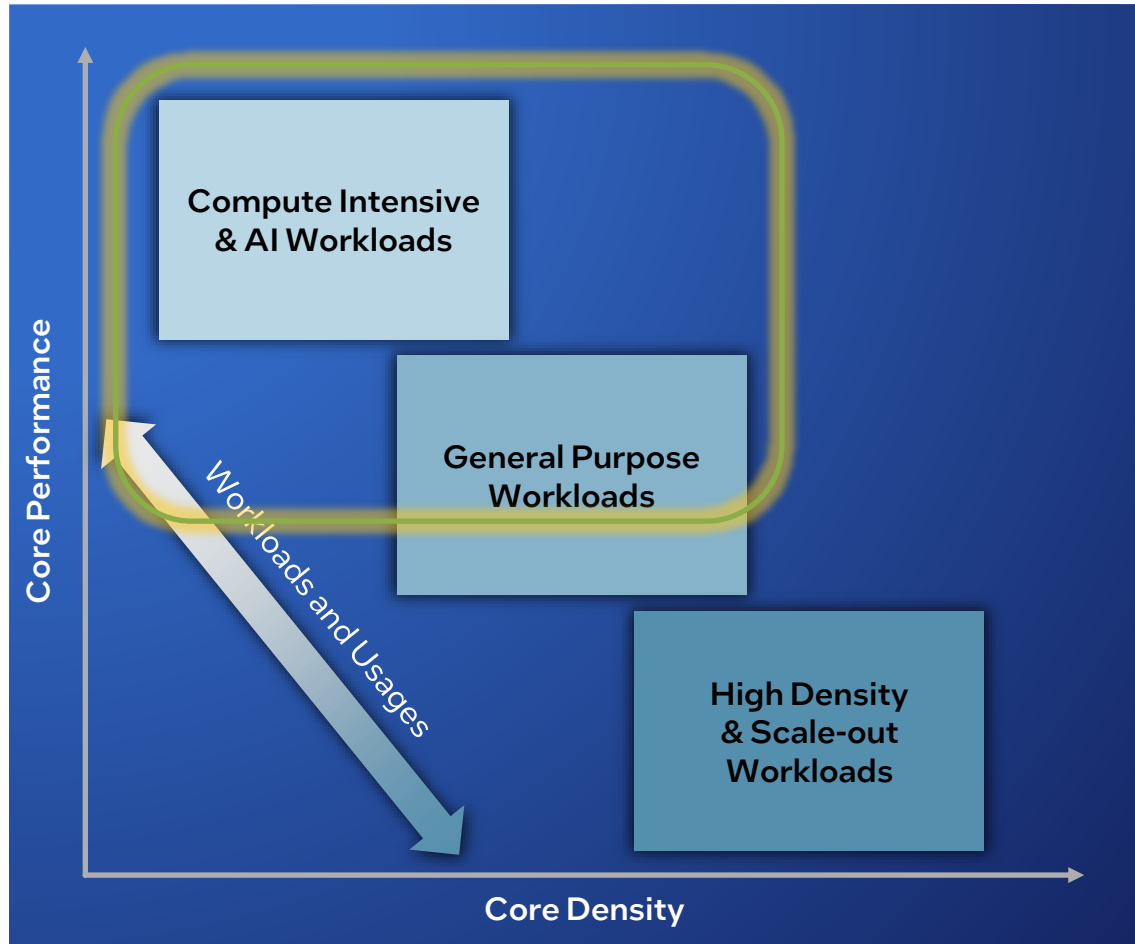
Enhanced P-core

- Intel3 process + power efficiency
- AMX support for FP16
- More inflight memory requests/BW

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2-3x performance / capacity boost for AI and mixed workloads*

Harness the Power of Xeon with P-cores



Optimized to deliver significant per-core performance to meet the growing needs of AI & compute intensive workloads

A common HW, FW and software foundation provides compatibility and consistency across a wide range of products

Platform level (IO, memory and coherent) performance scales to match expanding workload requirements

MCR DIMM and CXL attached memory enable efficient and flexible platform performance options

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Architected for scalability and flexibility for expanding optimization points

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