Applications Spotlight Using Agilex™ 5 FPGAs

Midrange FPGAs offering world-class features and capabilities that address design challenges across various markets.

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An Intel Company

Industrial Spotlight

Start inventing the future

Did you Know?

70% Nearly 70 percent of manufacturers are pursuing smart-factory initiatives‡1

3X Smart factory initiatives will likely triple the labor productivity growth rate during the next decade compared with the last‡2.

75% It's estimated that by 2025, 75 percent of data will be created outside of central data centers, where most processing takes place today. ‡3

30B The total number of IoT connected devices is expected to pass 30B by 2025! ‡4

The Market Landscape Today

New Industrial Trends

Many industrial trends such as Internet of Things (IoT), edge computing, artificial intelligence, 5G, robotics, cybersecurity, virtualization will transform the way industry operates today.

Multi-level Control

Another trend is the use of more solid-state switching converters in energy distribution. This is used to reduce the size and cost of transformers or replace AC transmission using transformers with DC transmission using DC-DC converters. To generate smooth enough output signals, the switching converters may need to be 'multi-level' or 'multi-phase', leading to the use of more switching transistors and a need for synchronized control of many transistors. This kind of control requires the use of multiple parallel digital outputs with a clock frequency of 100+ MHz and control loops with 100+ kHz update rates. FPGAs spatial compute structure allows hardware implementation of parallel synchronized, control loops with higher control bandwidth, and lower jitter than microprocessor alternatives.

New and Faster Drives

New Silicon Carbide (SiC) and Gallium Nitride (GaN) MOSFETs are beginning to replace IGBTs as switching transistors in power electronics. These devices switch faster and dissipate less power, both through the reduced switching time and through lower resistance when switched on. These devices enable the design of smaller, more efficient power converters or motor inverters. Since they switch faster, the switching signals to control them must be delivered with better time resolution and faster switching dynamics to respond quickly to transient source and load behavior. FPGAs can directly process multiple incoming signals and implement hardware-level deterministic, fast -update, parallel control.

Artificial Intelligence

Artificial intelligence is one of the big trends in the industry and it is showing a robust year growth and wide deployment across many market segments. Implementing an AI solution in the FPGA offers several advantages compared to legacy implementations, especially in a continuously changing environment like the one experienced the past few years.

TSN

Time-sensitive networking (TSN) is a set of open standards defined by the IEEE 802.1 working group that will re-shape the industrial communication and allow a real convergence of Information Technology (IT) and Industrial Operations Technology (OT). TSN allows the co-existence of high-priority and non-reserved best effort traffic in the same physical channel and is enabling an interoperability between standard-conformant industrial devices from any vendor. TSN is one of the key features that should be supported by industrial capable devices and FPGA based platforms offer several advantages in this area.

Vision

Industrial cameras, machine vision, artificial intelligence, robotics, or 4K/UHD or even 8K cameras are heavily driving the requirements of the growing vision market today. Some key factors to take into consideration when choosing the right hardware architecture for a vision-based system are higher bandwidth camera I/F, an increasing number of DSP units, format conversion, analytics support, flexibility to interface to several image sensors, and possibility to build custom image sensor pipelines (ISP). FPGA solutions are well positioned to help tackle these applications.

Virtualization or Workload Consolidation

Historically, industrial machines have been built as physically isolated and proprietary system running fix function application (PLC, HMI, etc.) and communicating with each other over proprietary communication link. Such an architecture does often provide the disadvantage of increased complexity, and the difficulty to migrate and scale. Intel is driving the migration of those isolated functions into virtual machines or microservices using more powerful and flexible hardware like FPGA's. Virtualization and containerization are key enabling technologies to allow this migration.

Edge Computing

Industrial companies have been collecting and storing data for years. The trend has been towards moving compute workloads into the cloud, but due to network latency, data security and the cost of transmitting large data, many logical tasks remain on premise or right at the OT/IT edge. Edge analytics in modern factory and process automation environments means increased availability without having to be continually connected to the cloud, increased security, and reduced risk and real-time monitoring and control behavior on the factory floor. FPGAs are expected to play a key role in edge-compute solutions by offering a platform for workload consolidation with acceleration, connectivity, and I/O flexibility.

Notes:

‡1 Capgemini White Paper. Manufacturers investing in the promise of smart factories

‡2 https://deloitte.wsj.com/articles/how-smart-factories-can-ignite-productivity-01580760126

‡3 Rob van der Meulen, "What Edge Computing Means for Infrastructure and Operations Leaders," Smarter with Gartner, October 3, 2018, https://www.gartner.com/smarterwithgartner/what-edge-computing-means-for-infrastructure-and-operations-leaders/.

‡4 https://iot-analytics.com/state-of-the-iot-2020-12-billion-iot-connections-surpassing-non-iot-for-the-first-time/

Flexible, Future-Proof Platform

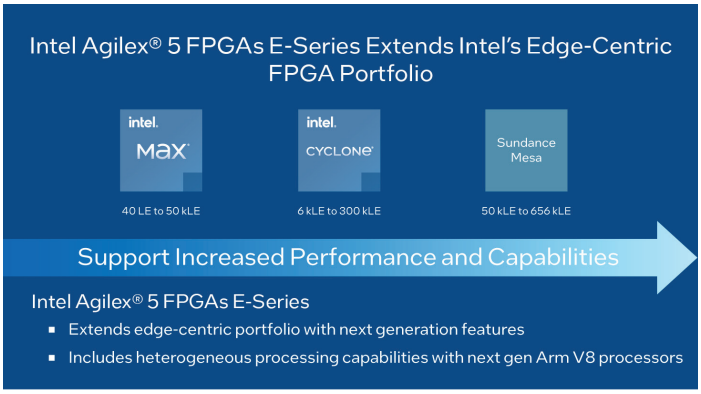
Intel® FPGAs represent a future- proof platform for your next- generation industrial product. Intel FPGAs can be used as stand-alone IoT devices, as companion to an Intel architecture (XPU) device, or even as an accelerator platform to help accelerate your workload in the edge or in the cloud.

Features such as long product lifecycle, industrial use case support, more built-in security, more functional safety support, deterministic low jitter, parallel processing, field upgradability, and the flexibility to support standard and custom specific interfaces makes them a perfect fit for your industrial application.

Why Intel Agilex® 5 FPGAs E-Series?

Intel Agilex® 5 FPGAs E-Series will provide several key additional benefits for industrial applications at the edge such as:

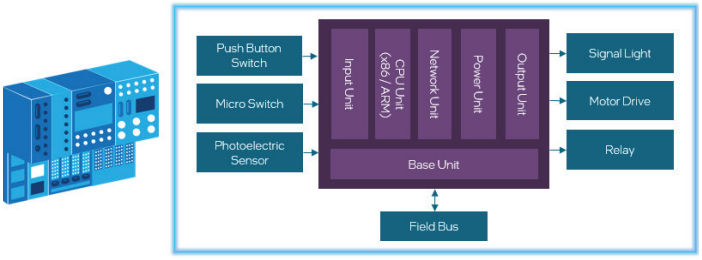
- Low-power Intel-based technology
- Up to 200 high voltage/3.3V I/O
- 2nd generation Hyperflex FPGA architecture
- Density range going tom 50 to 640KLE
- Functional safety support for application up to IEC62558 SIL3
- Hardened TSN endpoint.
- Small package/high compute density
- High- performance Arm based multi core processor
- Comprehensive and very robust security solution
- Hardened floating point DSP blocks
- Hard MIPI D-PHY, PCIe, Ethernet MAC
- Long product lifecycle
- RISC V available as soft processor
- Comprehensive IP ecosystem from Intel and partners



Programmable Logic Controller (PLC)

Why Intel FPGA?

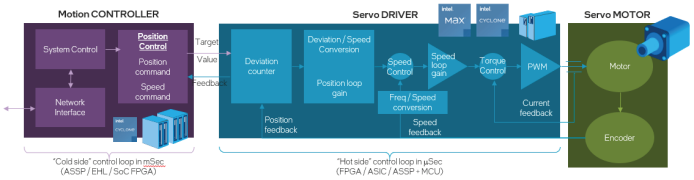
- I/O expansion, industrial Ethernet, and fieldbus protocols
- Deterministic, low-latency, low-jitter truly parallel compute
- Safety-certified SKUs and Functional Safety Data Pack available
- Hardware-based security
- Workload consolidation: Soft PLC + closed-loop control + graphical interface + multiple industrial Ethernet and fieldbus protocol + more safety monitoring … all running in parallel without cross-interference



Motor Drive, Computer Numerical Control (CNC)

Why Intel FPGA?

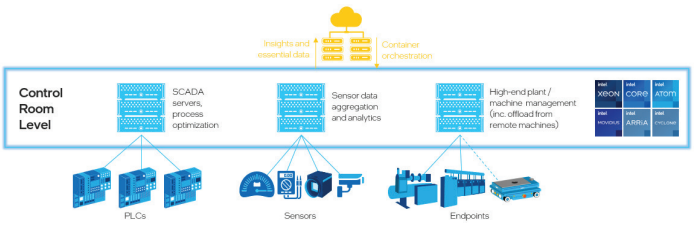
- Deterministic, high-bandwidth multi-axis control
- Industrial network protocols (TSN, industrial Ethernet, field bus, encoders)
- ICE 61508 certifiable SKUs. Functional Safety Data Pack
- Industrial environment; including 3.3V I/O for harsh electromagnetic conditions
- Long product lifecycles and high reliability



Edge Computing

Why Intel FPGA?

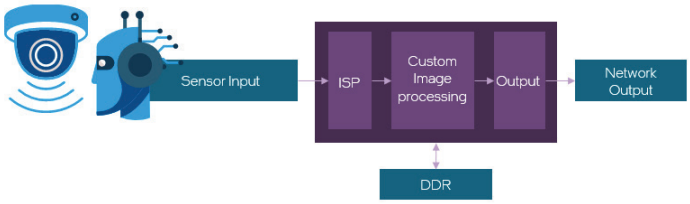
- High-throughput, low-latency network infrastructure acceleration–from Industrial Smart Network Interface Cards to 5G Radio and Distributed Units
- CPU acceleration / offload for AI inference, data preprocessing, and real-time data analytics
- Dedicated hardware-based security functions, such as TLS 1.3, and crypto acceleration



Machine Vision and AI

Why Intel FPGA?

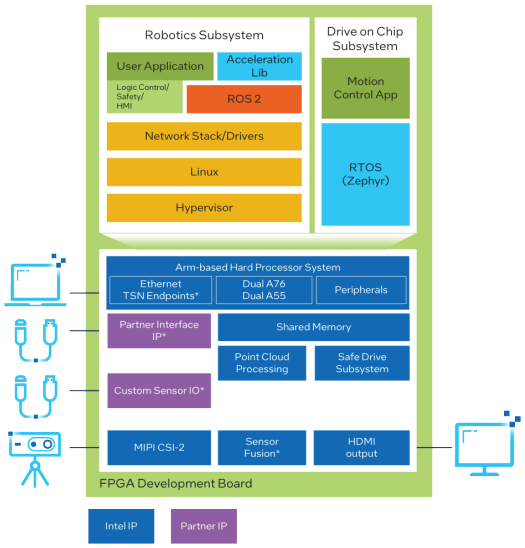
- Flexible architecture as new use cases and topologies emerge
- Direct ingest of data, pipelined straight into ISP or machine learning
- Deterministic, low-latency AI compute, integrated within or alongside other workloads
- Custom image signal processing (filtering, image rotation, 3D vision, photonics imaging, deep learning etc.), and custom images sizes
- Variety of data types supported–custom integer and custom floating point



Robotics

Why Intel FPGA?

- Fast, deterministic closed-loop multi-axis motor control
- Build custom low latency with more high-performance safety functionality on safety-certified SKUs
- Industrial network protocols (TSN, industrial Ethernet, field bus, encoders)
- 3D sensors ingest–Machine vision and AI



IP Cores

Intel offers a comprehensive portfolio of in-house and partner intellectual property (IP) for many applications in categories such as connectivity, video & vision, AI, safety, and security.

Connectivity IP Cores

Time-Sensitive Networking Solution

Intel offers a complete solution that includes hardware and software for customers who would like to design their own TSN solution. This package includes the Cyclone® V SoC FPGA-based TSN switched-end points with TTTech's TSN IP integrated.

Device SKU	Provider
TSN switch IP core (bundled with Cyclone® V SoC FPGA)	Intel and TTTech
TSN System on Module	EXOR
TSN interface card	Kontron

Industrial Ethernet Solutions

FPGAs provide the flexibility that allows customers to overcome the fragmentation of industrial standards while delivering best-in-class performance and determinism.

Intel's connectivity solutions offer:

- Multiple protocol support
- Flexibility for protocol selection and future upgrades

Protocol	Provider
PROFIBUS PROFINET RT / IRT EtherCAT Ethernet POWERLINK EtherNet/IP Soft DLR Modbus TCP / IP	Softing
EtherCAT	Beckhoff
EtherCAT	NDR
Mechatrolink III	Macnica
HSR / PRP	TTTech

Industrial Networking IP–ExpEther

ExpEther enables the extension to PCI Express beyond 1 km with multiple endpoints together on a single network that are connected through the standard Ethernet. Abundant commodities of PCI Express-based software and hardware can be used without any modification.

ExpEther IP enhances an industrial machine by connecting powerful data processing cards and high-speed interface cards to the machine tool. It provides:

- Low latency and high reliability suitable for industrial applications
- Compliant with PCIe and Ethernet standard (PCI-SIG PCI Express certified)
- Can use off-the-shelf L2 Ethernet switch

Video and Vision IP Cores

Video, Imaging, and Vision IP Solutions

Intel offers a variety of video processing solutions such as building block functions, sophisticated video image processing, and interface IP cores. Intel also offers FPGA design services based on a pool of expertise and wealth of IP to solve customer design challenges.

Video and vision processing suite:

- More than 20 IP cores for video processing
- 3D LUT Intel® FPGA IP
- Tone-Mapping Operator Intel® FPGA IP
- Warp Intel® FPGA IP

Machine Vision Interface IP Solutions

Intel FPGAs are ideal for machine vision cameras, frame grabbers, and vision controllers allowing designs to accommodate a wide variety of image sensors as well as specific interfaces.

Protocol	Provider
SLVS-EC CoaXpress GigE Vision USB3 Vision	Macnica
CoaXpress GigE Vision USB3 Vision	Sensor to Image
MIPI-CSI2	Foresys Inc
MIPI (C-PHY, D-PHY, CSI-2)	Arasan Chip Systems Inc

AI

Efficiera - Ultra Low-Power AI Inference Accelerator IP

Low-power CNN IP for object detection and classification by extreme low bit quantization technology. Efficiera enables practical implementation of AI technology using FPGAs on edge devices with compact IP.

- Complete solution contains pre-trained AI models, FPGA IP, and necessary software.
- Integrated design allows edge devices to operate independently in inference node without cloud connectivity.

Safety IP Cores

Functional Safety Data Package (FSDP)

FSDP includes:

- IEC61508 certified device families
- Certified tools and methodologies
- Certified lockstep cores and diagnostic IP
- Safety manuals, device data, reference material, and certificates

Security IP Cores

DOME - Device Ownership Management and Enrollment

DOME (Device Ownership Management and Enrollment) leverages the KMC Commander to help provide lifetime secure device management. For already installed IoT devices, FPGA bump-in-the wire gateways enable cost-effectively retrofitting of powerful security functions.

TLS 1.3 Hardware Security IP Core

Intel FPGAs provide a hardware-based implementation, as mandated by highest government and industry security standards. Isolated from more vulnerable software and OS stacks for critical protection of IIoT devices and the data they produce, process, and transmit.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Drive-On-Chip
Solution
Spotlight

Industry Trend

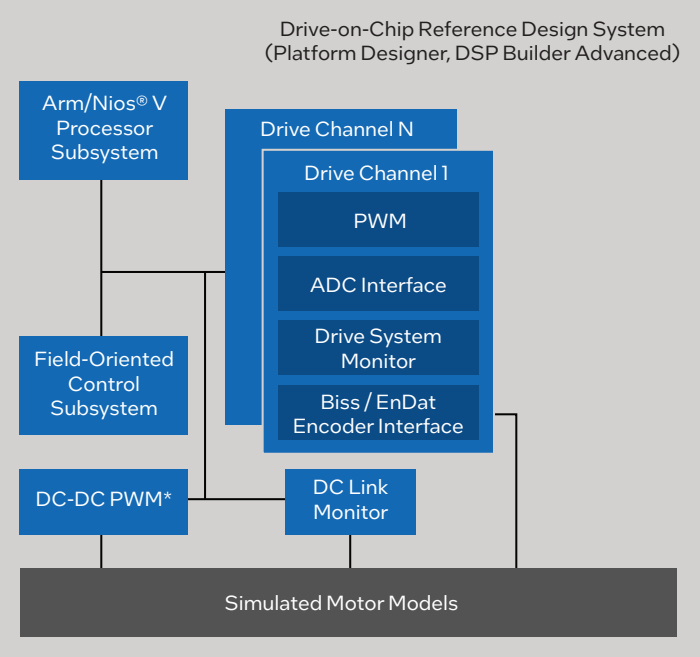
We are living in the era of electrification. New power switches based on Silicon Carbide (SiC) and Gallium Nitride (GaN) MOSFETs are beginning to replace IGBTs and Traditional MOSFETs as switching transistors in power electronics. These devices switch faster and conserve more power through reduced switching time and lower resistance when switched on. These devices enable the design of smaller, more efficient power converters, motor inverters, and other components. Because they switch faster, the switching signals to control them must be delivered with improved time resolution and switching dynamics to respond quickly to transient source and load behavior. Intel Agilex® 5 FPGAs E-Series can directly process multiple incoming signals and implement hardware-level deterministic, fast-update, parallel control. In this paper, we introduce the first building block for a multi-axis Field Oriented Control (FoC) based drive-on-chip.

Key Features

- CPU subsystem configured for multi-axis motor control applications
- Arithmetic IP modules implemented in FPGA resources for algorithm acceleration
- Dedicated FPGA drives control logic that allows interfacing with power electronics
- Performance counters for precise analysis and control of time-sensitive control functions
- Flexible architecture to allow different external interfaces for communications, encoder types, motor types
- Ability to scale the design for single to multiple motor axes
- High performance, low power implementation on E-Series FPGA
- Modular subsystem design approach

Description

This information brief describes a design architecture that integrates many common motor control and associated functions into a single E-Series FPGA. This approach allows a so-called "Drive-on-chip" solution that can address many market needs, for example, Industrial multi-axis control, battery charging, or robotics.



* Not included in initial design release

Benefits of a Scalable Solution

FPGAs are a highly configurable and scalable technology that are well adapted to the needs of a variety of applications. In the case of motor control, developers employing FPGAs enjoy a broad range of connectivity or interface options, a scalable amount of CPU performance, and the potential to accelerate algorithmic functions by using dedicated logic and DSP resources. Additionally, precise timing analysis and control can be implemented with dedicated FPGA logic functions.

Solution Summary

The following sections describe some of the independent subsystems within this design.

CPU scalability

This design architecture includes the option to have application software running either on the high-performance Arm hard processor system (HPS), or to have these functions running on a soft CPU implemented in the FPGA fabric. Use of the soft CPU (e.g., Intel® Nios® V soft processor – RISC-V implementation) frees the Arm HPS for other functions and also allows the design to target the most cost-optimized FPGAs in the E-Series FPGA family.

Position/speed control

This design includes position and speed control implemented in software and executed optionally by either the HPS or by a soft CPU included within the design. This functionality operates at either 16 kHz or 32 kHz using an interrupt service routine synchronized to the pulse-width modulation (PWM) and analog-to-digital (ADC) IP. The software control interfaces to Field Oriented Control (FOC) logic as described below. This function operates in the 10–100 kHz range depending on whether a software- or hardware-based calculation is selected. Finally, the FOC output is transferred to the output interfaces (PWM, ADC, encoder).

FOC

The FOC is a conventional algorithm used for the control of the motor's torque in motion control. Advantages of FOC over other AC motor control techniques include smooth operation combined with fast transient response. This design can optionally include IP to accelerate the mathematical operations such as those used in FOC functions. This design can optionally include fixed-point or floating-point coprocessing units that are implemented in FPGA resources. The E-Series FPGA family includes sophisticated DSP blocks and dedicated tensor processing elements that can be used for these functions.

Parallel processing/multi axis

The parallel processing nature of FPGAs can be leveraged to allow multiple axis motor control applications. This design supports up to six axes running concurrently, however the design can be easily extended to support more axes. The addition of axes consumes more FPGA resources but does not degrade the performance of each axis.

PWM control

This design also incorporates high-performance PWM circuitry with a carrier frequency of over 300 MHz. This allows high resolution control of power transistor switching times.

Drive system monitor

This design includes a drive system monitor state machine that oversees all fault signals from the hardware. The software application makes requests to the state machine when a change of system parameters is desired. The state machine can respond, either accepting or rejecting the request based on the system status and/or fault condition.

Sigma-Delta ADC interface

This design also includes a Sigma-Delta ADC interface for control of the drive axes. The dedicated FPGA IP samples the 20 MHz 1-bit ADC serial input for 3 phase current inputs for each drive axis. The FPGA also implements a sinc3 filter to low pass filter the serial input.

Interfacing and system connectivity

The drive-on-chip architecture integrates many functions, some of which may require external connectivity or interfaces. The flexible I/O capabilities of the E-Series FPGA allow connection of the drive-on-chip functions to external devices supporting the following functions:

- DDR memory
- GPIO/PWM connection to power electronics
- Encoder input interface
- JTAG interface for device/software debug
- UART/SPI for system connectivity
- HMI connections for status and input

Where to Get More Information

Industrial for FPGA
www.intel.com/content/www/us/en/industrial-automation/programmable/applications/overview.html

Drive-on-chip reference design for Intel® Cyclone® families and Intel® MAX® 10 devices
www.intel.com/content/www/us/en/docs/programmable/683466/current/about-the-drive-on-chip-reference-design.html

E-Series FPGA information
www.intel.com/content/www/us/en/products/docs/programmable/agilex-5-e-series-fpga.html

Intel® Nios® V soft CPU
www.intel.com/content/www/us/en/products/details/fpga/nios-processor/v.html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Video and
Vision
Spotlight

Introduction

As innovation continues to democratize the latest technology and the total number of global internet users grows year after year, so too does the amount of video and image data. By the end of 2022, video traffic is predicted to account for over 80% of total internet traffic. With increasing video resolutions, frame rates, and complex streaming demands, significantly more computing resources will be required to meet the rising challenges of this explosion in data volume. Due to the broad variety of video applications, data must be processed in different parts of the network as well, from edge through to the cloud. The wide variety of data-intensive video and image processing workloads necessitates high-performance processing, flexibility, and power economy from computing resources, making FPGAs attractive candidates for these systems.

Built on Intel® 7 process technology, the Intel Agilex® 5 FPGAs E-Series enable up to 2.5X fabric performance and up to 50% lower total power consumption as compared to previous generation Cyclone® V FPGAs. The Intel Agilex® 5 FPGA E-Series is bridging the gap between low-end and mid-range products in our portfolio with:

- 2nd generation FPGA Architecture that delivers on performance while optimizing for low power
- Integrated MIPI D-PHY support enabling MIPI CSI-2 and MIPI DSI-2 in low-power, high-speed (up to 2.5 Gbps) applications
- Support for 12G-SDI
- Wide density range (up to 656 KLEs)
- Higher memory density than previous Cyclone V devices
- Heterogeneous processing capabilities with Arm Cortex-A55 and Arm Cortex-A76 processors within the Hard Processor System (HPS)
- Advanced security features enabled through the Secure Device Manager

For applications requiring higher performance than E-Series FPGAs, we have developed the Intel Agilex® 5 FPGAs D-Series that will extend the Intel Agilex® device family down to 103kLE. It can deliver up to 1.5X fabric performance and up to 40% lower total power consumption compared to previous generation Intel® Stratix® 10 FPGAs.

- 2nd generation Intel Hyperflex FPGA Architecture that delivers on performance while optimizing for low power allows D-Series FPGA to comfortably run video designs at 600 MHz
- 600 MHz clock speeds enable processing of 8K, 60 frames per second (fps) video with 4 pixel-in-parallel (PiP) architecture, enabling a near-halving of resource utilization as compared to other high-performing FPGA families that typically use 8 PiP architectures
- Integrated MIPI D-PHY support enabling MIPI CSI-2 and MIPI DSI-2 in low-power, high-speed (up to 3.5 Gbps) applications
- Advanced security features enabled through the Secure Device Manager
- Supports 8K video at 60 fps with HDMI 2.1 and DisplayPort 2.0 connectivity standards

Integrated MIPI Support

The E-Series FPGAs and D-Series FPGAs offer a new feature for FPGA built-in support for MIPI interfaces that are often used in high-performance, low-power image sensor capture-and-display applications. These FPGAs will natively support MIPI D-PHY v2.5, which is well-suited for applications such as video conferencing cameras and endoscopes.

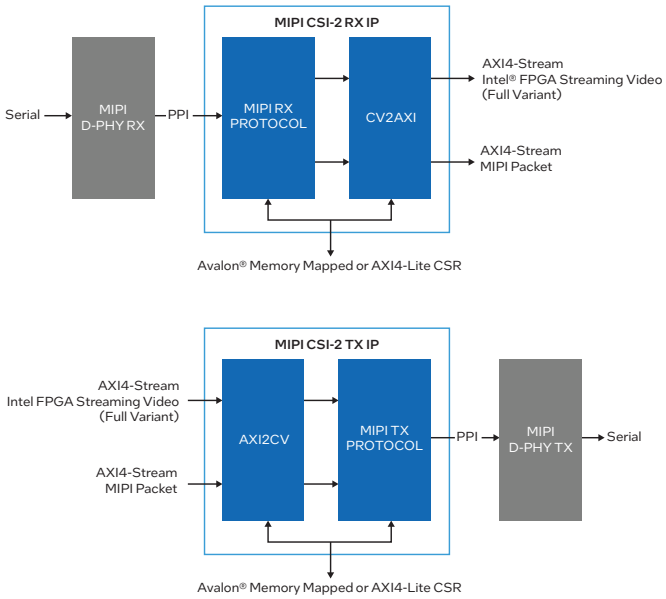
MIPI D-PHY intellectual property (IP) is primarily intended to enable MIPI CSI-2 and DSI-2 interfaces on E-Series FPGAs and D-Series FPGAs. The IP enables unidirectional multi-lane (1, 2, 4, 8 lanes) configuration modes up to 3.5 Gbps per lane on general-purpose input/output (GPIO). The CSI-2 TX and RX IP implement a CSI-2 transmit and receive interface according to the MIPI CSI-2 standard v3.0 with the underlying D-PHY standard. The DSI-2 TX and RX IP implement a DSI-2 transmit and receive interface according to the DSI-2 standard v2.0 with the underlying D-PHY standard.

Supported D-PHY Configurations

- Single 1-8 links per IO96 (4D+1C)
- Supports 4D+1C or 8D+1C
- Standard and short channel support up to 2.5 Gbps
- Uni-directional TX and RX configurations

CSI and DSI Support on D-PHY

- CSI-RX and DSI-TX/RX SIPs
- Pixel interface with AXI4-streaming
  - No pixel encoding or compression
- CCI I3C support maximum 1.2 V



Video and Vision FPGA IP

E-Series FPGAs and D-Series FPGAs are compatible with the Video and Vision Processing Suite, a plug-and-play IP portfolio that presents not only a highly-integrated alternative to video ASSPs, but also the means to develop custom video solutions. Together with easily incorporated connectivity IP blocks, the Video and Vision Processing Suite provides a design philosophy for rapid new design creation and easy integration of custom value-add features. Moving from HD to 4K/UHD processing requires minimal system re-design. The architecture is extensible to 8K, HFR, and HDR requirements. Learn more about Intel's in-house developed and supported video processing and connectivity IP by clicking the following links:

Video Processing IP

- Video and Vision Processing Suite Intel FPGA IP User Guide
- Warp Intel® FPGA IP
- 3D LUT Intel® FPGA IP
- Tone Mapping Operator (TMO) Intel® FPGA IP

Video Connectivity IP

- HDMI Intel FPGA IP User Guide
- DisplayPort Intel FPGA IP User Guide
- SDI II Intel® FPGA IP User Guide
- HDCP Intel® FPGA IP Core

E-Series FPGA and D-Series FPGA Solutions

Simplify your product development with new edge-centric designs. These design examples can jump-start your project development with E-Series FPGAs and D-Series FPGAs.

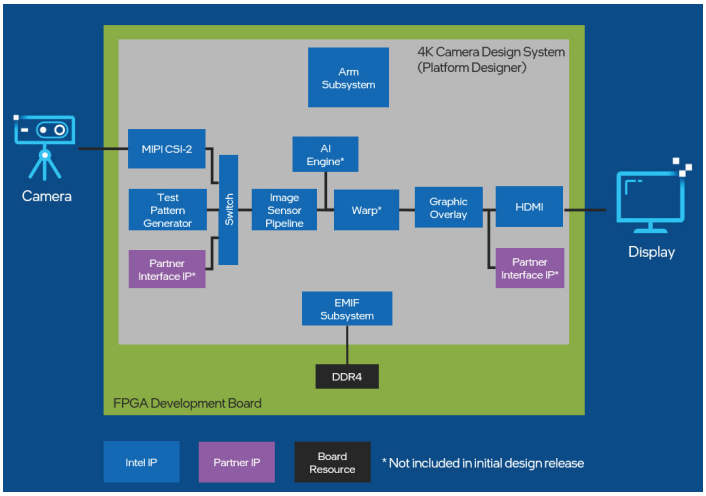
- Committed solutions for 4K cameras, 4K video and vision systems, and 8K video and vision systems are compatible with E-Series FPGA and D-Series FPGA architecture and tools
- Access documented example designs and boards

Leverage existing IP, solutions, and documentation based on current generation Intel FPGA products.

Roadmap Solution: 4K Camera

This design implements an extensible camera pipeline supporting 4K resolution MIPI CSI-2 input and low latency processing at 60 frames per second.

The modular IP-centric methodology and embedded software stack enables extensibility to application specific interfaces, artificial intelligence (AI) inference, and custom processing IP (e.g. geometric correction).



Key Features

- MIPI CSI-2 input and integrated MIPI D-PHY
- Standard AXI-4 interfaces
- Image sensor processing IP subsystem including debayering, pixel defect correction, vignette correction, adaptive noise reduction, and white balance
- HDMI (up to latest version, 2.1) output
- Arm-hosted graphical user interface to control ISP functions
- High-performance embedded direct memory access (DMA)

Development Kit Support

- Power-optimized E-Series FPGA

Solution Type

- Design example and development board

Target Applications

- Industrial cameras
- Consumer and prosumer camera/audio/video
- Medical video (e.g. endoscopy) and monitors
- Security cameras

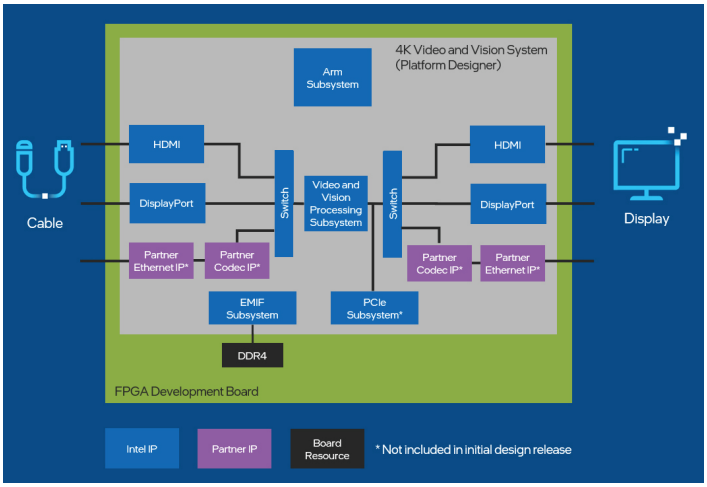
Learn More

- Video and Vision Processing Suite Intel FPGA IP User Guide
- HDMI Intel FPGA IP User Guide

Roadmap Solution: 4K Video and Vision

This flexible design implements a highly optimized, low-latency video and vision processing pipeline, supporting 4K resolution video at 60 frames per second. HDMI and DisplayPort video input and outputs are selectable during development and can be integrated with a Video and Vision Processing Suite. This enables a wide range of video processing operations, including—but not limited to—video format conversion, enhancement, manipulation, and transformation operations.

The modular IP-centric methodology and embedded software stack enables extensibility to Ethernet-based video protocols, mezzanine compression algorithms, application-specific interfaces, and custom processing IP.



Key Features

- HDMI input and output supporting 4K video @ 60 fps
- DisplayPort input and output supporting 4K video @ 60 fps
- Arm-hosted GUI to control video functions
- Video and Vision Processing Suite for low-latency, high-quality video data processing
- High performance DMA IP and efficient DDR access

Development Kit Support

- Power-optimized E-Series FPGA

Solution Type

- Design example and development board

Target Applications

- Video wall, digital signage, projection
- Healthcare
- A/V networking

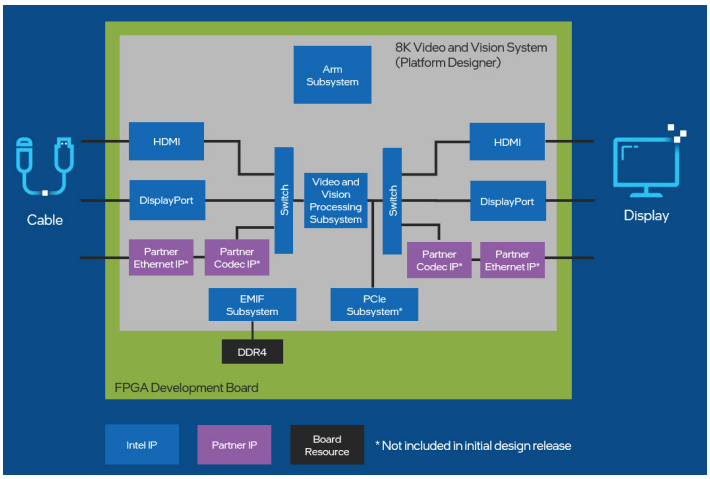
Learn More

- Video and Vision Processing Suite Intel FPGA IP User Guide
- HDMI Intel FPGA IP User Guide
- DisplayPort Intel FPGA IP User Guide

Roadmap Solution: 8K Video and Vision

This flexible, high-performance design implements a highly optimized, low-latency video and vision processing pipeline, supporting 8K resolution video at 60 frames per second. The Video and Vision Processing Suite operates at over 600 MHz, using up to half the logic resources of competing solutions. The pipeline implements a wide range of video format conversation, enhancement, manipulation, and transformation operations.

The modular IP-centric methodology and embedded software stack enables extensibility to Ethernet-based video protocols, mezzanine compression algorithms, application-specific interfaces, and custom processing IP.



Key Features

- HDMI 2.1 input and output supporting 8K video @ 60 fps
- DisplayPort 2.0 input and output supporting 8K video @ 60 fps
- Arm-hosted GUI to control video functions
- Video and Vision Processing Suite for low-latency, high-quality video data processing
- High-performance DMA IP and efficient DDR access

Development Kit Support

- D-Series FPGA

Solution Type

- Design example and development board

Target Applications

- Video wall, digital signage, projection
- Healthcare
- A/V networking

Learn More

- Video and Vision Processing Suite Intel FPGA IP User Guide
- HDMI Intel FPGA IP User Guide
- DisplayPort Intel FPGA IP User Guide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4K Camera Design Solution Spotlight

Introduction

As innovation continues to democratize the latest technology and the total number of global internet users grows year after year, so does the amount of video and image data. By the end of 2022, video traffic is predicted to account for over 80% of total internet traffic[1]. And with increasing video resolutions, frame rates, and complex streaming demands, significantly more computing resources will be required to meet the rising challenges of this explosion in data volume. Due to the broad variety of video applications, data must be processed in different parts of the network as well, from edge through to the cloud. The wide variety of data-intensive video and image processing workloads necessitate high-performance processing, flexibility, and power.

Key Application Markets

- Industrial cameras
- Medical endoscopy
- Surveillance/security
- Robotics/drones

Key Features

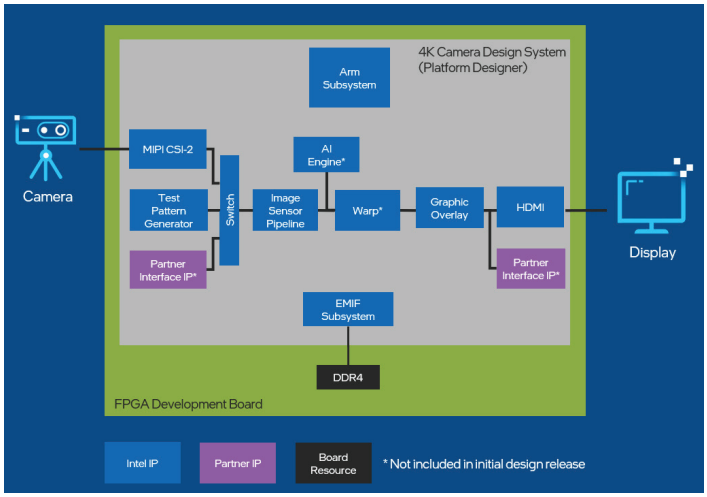
- MIPI CSI-2 input and integrated MIPI D-PHY
- Standard AXI-4 interfaces
- Image sensor processing IP subsystem including debayering, pixel defect correction, vignette correction, adaptive noise reduction, white balance
- Flexible and modular architecture that allows you to modify or extend the design
- HDMI output
- Arm-hosted graphical user interface to control ISP functions
- High-performance embedded direct memory access (DMA)

Description

This information brief describes a design architecture that integrates key image processing intellectual property (IP) into a complete, end-to-end 4K camera solution implemented in an FPGA. This design could be used in a number of application areas such as industrial inspection, medical endoscopy, surveillance, and robotics.

Benefits of a Scalable Solution

FPGAs are a highly configurable and scalable technology that is well adapted to the needs of a variety of applications. In the case of camera and video applications, FPGAs can benefit a developer by allowing a broad range of video connectivity or interface options, a scalable amount of CPU performance, and the potential to accelerate algorithmic functions by using dedicated logic and DSP resources. Additionally, streaming video can be passed directly between pipeline IP blocks allowing high-performance and lower-latency processing.



[1] According to the 2020 Cisco Global Networking Trends Report

Solution Summary

Camera Connectivity

This design example includes camera interface IP that enables an industry standard MIPI CSI-2 interface to be implemented with a MIPI D-PHY. This configuration allows a 4K resolution camera to connect into the FPGA fabric for further processing. The IP converts an AXI streaming output to allow connectivity to other IP cores within Intel's Video and Vision Processing Suite.

Video Output IP

This design example also includes an HDMI output IP core to allow the processed 4K video stream to be output to an external monitor or other HDMI sink. This IP core makes use of the on-chip high speed transceivers and can be configured to support various frame rates vand resolutions. The internal connection of this IP uses a standard AXI streaming protocol that allows it to be used with other IP within Intel's Video and Vision Processing Suite.

Image Sensor Processing IP

This design example includes an Image Sensor Processing subsystem that incorporates a number of common camera processing IP cores. Examples of these functions implemented are pixel defect detection and correction, vignette correction, adaptive noise reduction and white balance correction. This subsystem also implements the conversion of Bayer format images into RGB format (aka Debayering or de-mosaicing). The FPGA fabric and hardened DSP blocks combined with abundant on-chip RAM components allow a designer to implement these functions in a power efficient and low latency manner.

High Performance Warp IP

Future versions of this design example will include a high-performance Warp IP core. The Warp IP core adjusts the geometry of the incoming image and can be used for effects such as fisheye lens correction, keystone correction or other arbitrary warping effects. Intel's Warp IP includes a complex DMA engine that interfaces with external DDR memory to implement these complex warp operations. Control of the Warp IP is done through a GUI using a PC connected to the development kit.

Arm-Hosted GUI for Design Features Control

This design example includes an Arm – hosted GUI to control many features of the design. The Arm core serves a web page that can be accessed via a connected PC. The GUI settings are then translated into specific commands for each IP in the system. The GUI implements many levels of control from simple feature enable/disable, to complex mesh specification for the Warp IP. The GUIs are created using an application toolkit provided with the design example.

Graphic Overlay IP

This design example incorporates a graphic overlay IP that allows user-specified icons to be embedded or overlaid onto the video stream. This IP can be used to display information about the image content, for example it could be used to highlight AI inference results, or information about the resolution of the incoming video stream.

AI Engine

Future versions of this design example will incorporate an AI engine created from the logic elements, DSP, and on-chip RAMs within the FPGA fabric. This compact AI IP core can be used for object detection and/or image classification functions. Control aspects of the inference are provided by the Arm cores on the device. This AI engine is compatible with the OpenVINO™ toolkit AI tool chain.

Interfacing and System Connectivity

The 4K camera design integrates many functions, some of which may require external connectivity or interfaces. The flexible I/O capabilities of the Intel Agilex® 5 FPGAs E-Series allow for connections to many system components:

- DDR memory
- MIPI connection for camera interface
- HDMI connection for video output
- JTAG interface for device or software debug
- Ethernet connection for GUI control

Where to Get More Information

Industrial for FPGA
www.intel.com/content/www/us/en/industrial-automation/programmable/applications/overview.html

Intel Agilex® 5 FPGAs E-Series information
www.intel.com/content/www/us/en/products/docs/programmable/agilex-5-e-series-fpga.html

FPGA products information
www.intel.com/content/www/us/en/products/programmable.html

OpenVINO toolkit information
www.intel.com/content/www/us/en/developer/tools/openvino-toolkit/overview.html

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Healthcare and Medical Systems Spotlight

Introduction

The healthcare industry benefited from technological evolution long before the Covid-19 pandemic struck in 2020; however, the pandemic has served as an accelerant to various forms of innovation, particularly in the following domains.

- Detection and diagnosis (imaging, video)
- Patient care (point-of-care devices, remote capabilities)
- Treatment (ventilators, vaccine, and drug discovery)

In terms of detection and diagnosis, the innovation revolves around improved quality video (for endoscopes, laparoscopes, etc.) and imaging (for ultrasound, CT, PET, MR, and x-ray systems) as well as the addition of artificial intelligence (AI) and mobile, handheld form factors for increased usability.

Patient care is becoming more accessible as more at-home monitoring is being implemented. The incorporation of AI in analysis of patient movement coupled with the improved connectivity to trigger alarms when additional attention is needed is making out-of-hospital patient care more viable for many people in need. Additionally, virtual and augmented reality solutions are enabling new ways for doctor-patient interactions to take place.

In the field of treatment, there has been ongoing improvement in the connectivity and quality of hospital devices such as ventilators, infusion pumps, EKG/ECG, glucose meters, and pulse oximeters. An increasing number of devices (including ventilators) are now being fitted with remote capabilities and being used as point-of-care solutions for mobile treatment as well.

As this innovation continues apace, Intel is developing new lower density FPGAs to enable healthcare companies to build the highest performing products and equipment for this changing world.

Introducing Intel Agilex® 5 FPGAs E-Series and Intel Agilex® 5 FPGAs D-Series

Built on Intel® 7 process technology, Intel Agilex® 5 FPGAs E-Series enable up to **2.5X fabric performance and up to 50% lower total power consumption** as compared to previous generation Cyclone® V FPGAs. The E-Series FPGA is bridging the gap between low- and mid-range products in our portfolio with:

- 2nd generation Intel® Hyperflex® FPGA Architecture that delivers on performance while optimizing for low-power applications
- Integrated MIPI D-PHY support enabling MIPI CSI-2 and MIPI DSI-2 in low-power, high-speed (up to 2.5 Gbps per lane) applications
- Support for high-speed streaming video interfaces, e.g. 12G-SDI, HDMI 2.1, DisplayPort 2.0 with FPGA fabric running at 300 MHz
- Densities up to 656 KLEs
- Higher memory density than previous Cyclone V devices
- Heterogeneous processing capabilities with Arm Cortex-A55 and **Arm Cortex-A76 processors** within the Hard Processor System (HPS)
- Advanced security features enabled through the Secure Device Manager

For applications requiring higher performance than E-Series FPGAs, we have developed the Intel Agilex® 5 FPGAs D-Series that will extend the Intel Agilex® device family down to 103K logic elements (LE). **It can deliver up to 1.5X fabric performance and up to 40% lower total power consumption** compared to previous generation Intel® Stratix® 10 FPGAs.

- 2nd generation Intel Hyperflex FPGA Architecture that delivers on performance while optimizing for low-power applications allows D-Series FPGAs to comfortably run video designs at 600 MHz
- Integrated MIPI D-PHY support enabling MIPI CSI-2 and MIPI DSI-2 in low-power, high-speed (up to 3.5 Gbps per lane) applications
- Advanced security features enabled through the Secure Device Manager
- **Supports 8K video at 60 fps** with HDMI 2.1 and DisplayPort 2.0 connectivity standards

Medical Video and Vision Applications

The medical video application space, including endoscopes and robotic surgery, is growing rapidly with innovation taking place in video quality and display enhancements. Intel FPGAs are ideal for these medical workloads as they can execute custom high-quality HD, 4K, and 8K video pipelines with ultra-low latency, which is critical to success in these procedures.

Why Intel Agilex® 5 FPGAs in medical video:

- The D-Series FPGA offers 600 MHz fabric clock speed processing of 8K, 60 frames per second (fps) video with 4 pixel-in-parallel (PiP) architecture, enabling a near-halving of resource utilization as compared to other high-performing FPGA families that typically use 8 PiP architectures. **This allows for increased return on investment (ROI) for endoscope designs**
- E-Series FPGAs and D-Series FPGAs offer a new feature for FPGAs with built-in support for MIPI interfaces that are often used in high-performance, low-power image sensor capture-and-display applications. These FPGAs will natively support MIPI D-PHY v2.5, which enables thinner, more flexible high-performance optical cables for high-resolution video systems endoscopes
- E-Series FPGAs and D-Series FPGAs also support Video Processing and Connectivity IP out of the box (See "Video Processing, Video Connectivity, and AI Inference IP" section for more information)
- The Intel® FPGA AI Suite works with the OpenVINO™ toolkit and can be used for artificial intelligence modeling in endoscopes (e.g. deep learning inference to aid in diagnosis and surgery)
- With a history of **15+ years of availability** from PRQ, Intel® FPGAs can overcome development cycle investment and **enable higher ROI**

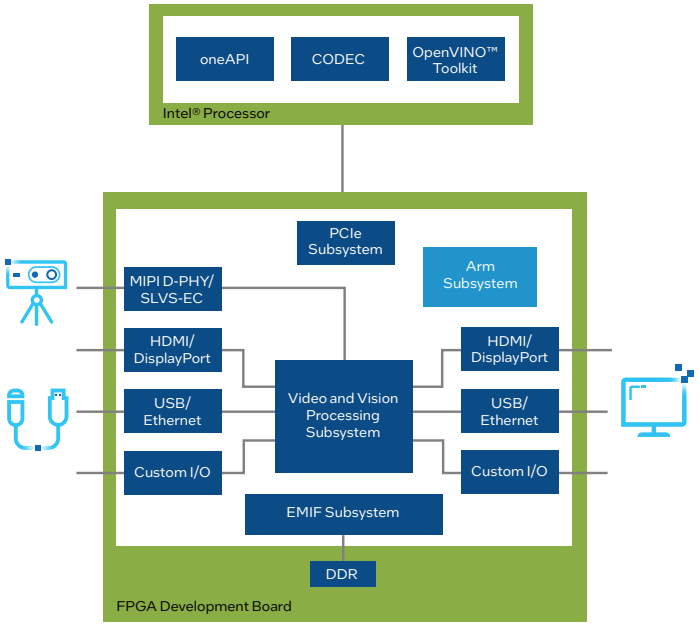


Figure 1. Sample medical video and vision workload block diagram

Medical Imaging Applications

In addition to medical video and vision, medical imaging is undergoing upgrades in both image quality (3D/4D ultrasound, 256+ slice CT machines, 3T+ MRIs, enhanced X-rays) and portability (mobile/handheld ultrasound, CT in a box, and bedside imaging devices). Intel FPGAs are used throughout these devices in various architectures, executing numerous workloads including beamforming, image signal processing, backplane projection, filtering, image reconstruction, and AI.

Why Intel Agilex® 5 FPGAs in medical imaging:

- Small packages and low densities are optimal for handheld and point-of-care application
- Performance optimized for front-end signal processing with PCIe for host connectivity and SLVS, LVDS, and JESD for analog-to-digital converter (ADC)/digital-to-analog converter (DAC) sensor or transmitter connectivity
- High-performance backplane projection and signal processing in chip intensive CT systems optimizing performance and ROI
- With a history of **15+ years of availability** from PRQ, Intel FPGAs can overcome development cycle investment and **enable higher ROI**

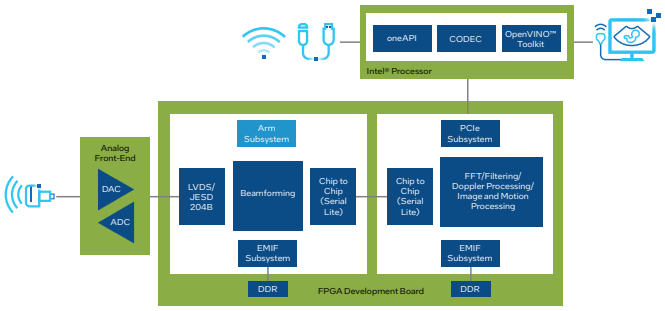


Figure 2. Sample ultrasound workload block diagram

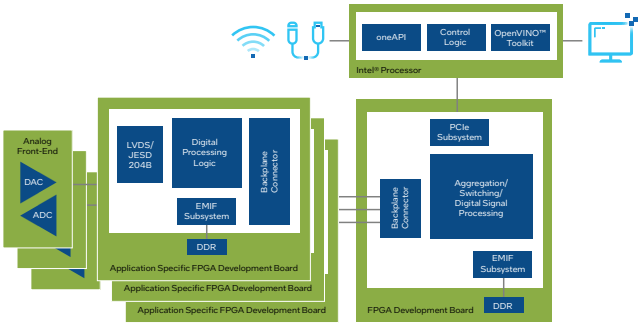


Figure 3. Sample CT/MRI block diagram

Clinical Systems Applications

Clinical systems for the healthcare process are a major part of everyday patient care, critical surgeries, and everything in between. They can range from patient vital sign monitoring to ventilators to lab equipment like mass spectrometers. Innovation in this space is centered around connectivity of devices for holistic patient analysis, all-in-one monitoring devices, AR/VR and data enhancement.

Why Intel Agilex® 5 FPGAs in clinical systems:

- Power-optimized Intel Agilex® 5 FPGAs will provide customers with a new low-density option for use in both plug-in and battery-powered clinical equipment with a long shelf life
- Our new FPGAs will have **dedicated 3.3 V I/Os** for interoperability with legacy systems
- Video processing and connectivity IPs for use in patient camera and display technology as well as AR/VR innovations (See "Video Processing, Video Connectivity, and AI Inference IP Support" section for more information)
- Custom image processing and enhancement techniques for controlling the optics in clinical microscopes
- **Deterministic low latency** and fine grain control for monitoring devices and ventilators
- SoC and non-SoC devices with digital signal processing (DSP) for real-time waveform analysis and graphic controls for Human-Machine Interaction (HMI)

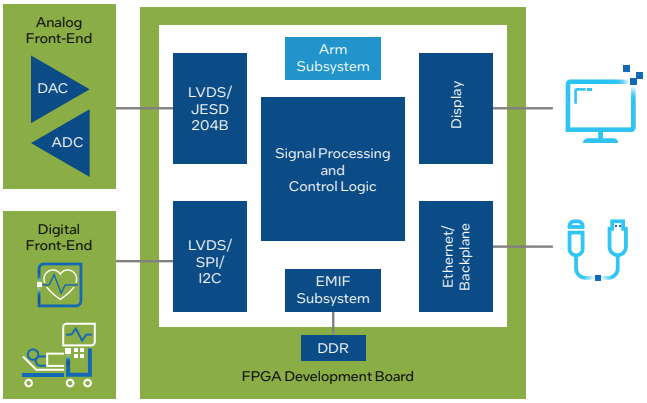


Figure 4. Sample clinical system workload block diagram

Video Processing, Video Connectivity, and AI Inference IP Support

Video Processing IPs available for these devices are:

- Video and Vision Processing Suite Intel FPGA IP User Guide
  - Warp Intel® FPGA IP
  - 3D LUT Intel® FPGA IP
  - Tone Mapping Operator (TMO) Intel® FPGA IP

Video Connectivity IPs available for these devices are:

- HDMI IP User Guide
- DisplayPort IP User Guide
- SDI II Intel® FPGA IP User Guide
- HDCP Intel® FPGA IP Core

The Intel FPGA AI Suite works with the OpenVINO toolkit and can be used for artificial intelligence modeling in endoscopes (e.g. deep learning inference to aid in diagnosis and surgery)

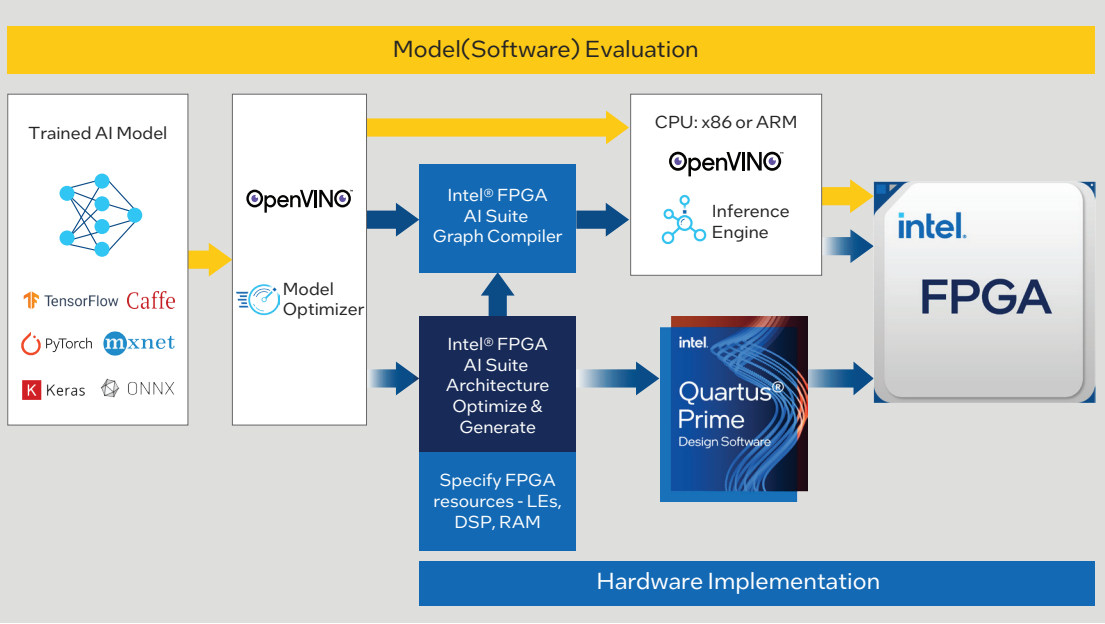
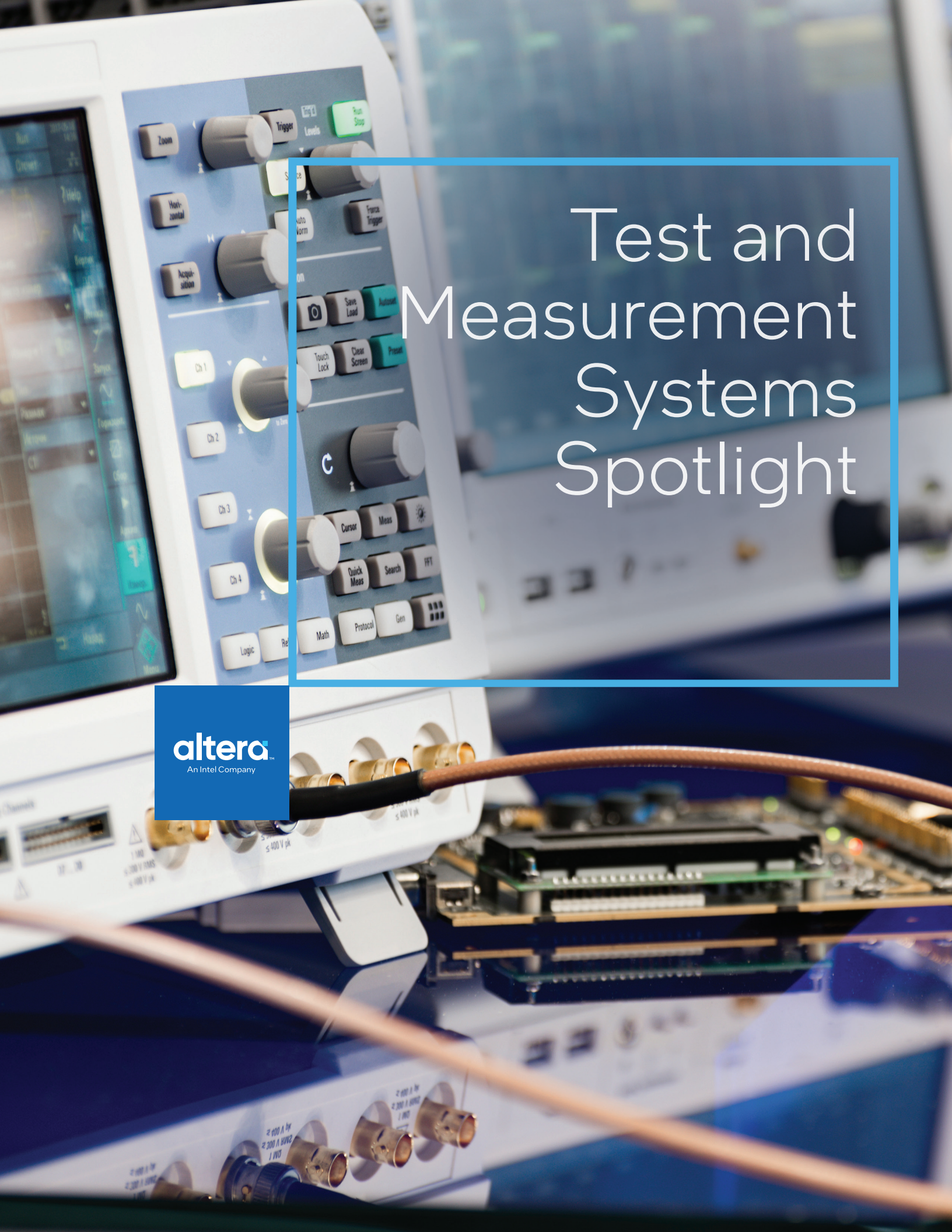


Figure 5. Intel FPGA AI Suite development flow

Conclusion

D-Series FPGAs and E-Series FPGAs possess the capabilities to drive innovation in medical video and vision systems, medical imaging applications, and clinical patient care systems. In addition to delivering on power, performance, IP availability, support and compatibility with the latest connectivity protocols and processor interfaces, and feature robustness, Intel FPGA offers design support from industry veterans from the Intel FPGA Design Services team. To learn more about creating your own medical systems that leverage these new Intel Agilex® 5 FPGAs, reach out to your local Intel sales representative.

Contact Intel



Test and Measurement Systems Spotlight

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Introduction

Testing is a requirement for all market segments–regardless of the end market, all products must be tested before they are shipped to the end user. This necessity for quality assurance drives the pervasiveness of the test and measurement segment, which includes the following sub-segments:

- Automated Test Equipment (ATE) for displays, semiconductors, and system-level test for technologies like solid-state drives (SSD)
- RF Test Instrumentation including various types of oscilloscopes and other high-frequency wideband systems like bit-error rate testers (BERTs)
- Communications Test consists of wired communications (such as Gigabit Ethernet test), wireless (like 5G/6G) test, and other protocol-specific testers

  – Learn more about our Intel Agilex® 7 FPGA I-Series and Intel Agilex® 7 FPGA M-Series which are better targeted for communications test systems

Regardless of the sub-segment, industry-leading test and measurement system designers must overcome several engineering challenges. Testers must be able to:

- Support a variety of the latest high-speed industry standards relative to the device under test (DUT)
- Flexibly upgrade products as new standards emerge to incorporate new features and enable greater functionality to stay competitive in the market
- Meet high compute/memory bandwidth requirements for different data workloads
- Ensure component availability as the global supply chain continues to struggle to meet worldwide demand

Intel® FPGAs provide the capabilities required to meet all four of these difficult design requirements, and with the introduction of Intel Agilex® 5 FPGA E-Series and Intel Agilex® 5 FPGA D-Series, these challenges are now easier to overcome than ever before. These FPGAs are bridging the gap between low-end and mid-range products in our portfolio with the following features:

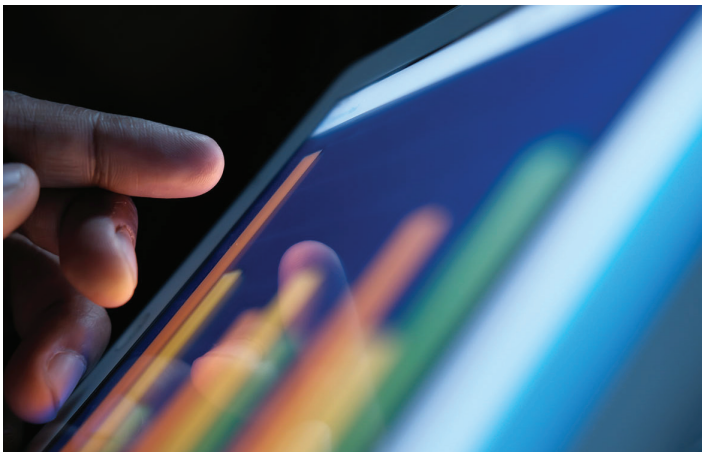
- E-Series FPGAs are performance-optimized FPGAs that delivers up to 1.37X higher fabric performance and up to 39% lower power as compared to Intel® Arria® 10 FPGA
- D-Series FPGA delivers up to 1.5X fabric performance and up to 42% lower total power consumption vs. Intel® Stratix® 10 FPGA
- Support for multiple GPIO standards (1.8 V-3.3 V and LVDS)
- Hardened controllers for DDR4, DDR5, LPDDR4, and LPDDR5 memories
- Hardened PCIe 3.0/4.0 and 10/25Gb Ethernet (MAC+PCS), reducing overall FPGA logic expenditure and mitigating the timing closure risks of soft IP

  – Supports up to six MAC instances

  – Up to 32 transceivers with speeds up to 28 Gbps for D-Series FPGA, and up to 24 transceivers capable of speeds up to 17 Gbps for power-optimized E-Series FPGA (24 transceivers up to 28 Gbps for performance-optimized FPGA)
- Support for multiple high-speed video I/O standards including SDI, DisplayPort, HDMI
- Integrated MIPI D-PHY support enabling MIPI CSI-2 and MIPI DSI-2 in low-power, high-speed (up to 2.5 Gbps for E-Series FPGA and 3.5 Gbps for D-Series FPGA) applications
- Gives designers options with a wide density range of 50 KLE to 656 KLE
- Supports heterogeneous processing capabilities with Arm Cortex-A55 and Arm Cortex-A76 processors within the Hard Processor System (HPS)

Intel Agilex® 5 FPGAs for Automated Test Equipment (ATE)

Display Testers



Display technology is evolving at a rapid pace, and a flexible display testing solution is necessary to keep up with the latest technologies while keeping the cost of innovation low. These display testers must support a large number of I/O connections with varying data rates and interface types. Intel Agilex® 5 FPGAs are ideal candidates for display ATE including display panel (e.g. LCD) testers, camera module testers, tablet and cellphone testers, and scientific display testers. Figures 1 and 2 illustrate a tablet or cellphone display tester block diagram for MIPI D-PHY and DisplayPort displays. These display systems need features like high-speed connection (PCIe, DisplayPort) and host processors for control and video ingest and processing, as well as external memory interfacing (DDR4/5, LPDDR4/5) to store test patterns while they are streamed to the display under test.

Why D-Series FPGAs and E-Series FPGAs for Display Testers:

- Support for multiple video connectivity solutions (both high-speed and low-speed applications)
  - High-speed video I/O standards: MIPI D-PHY up to 2.5G for E-Series FPGAs and up to 3.5G for D-Series FPGAs, up to 12G SDI with multi-rate support, DisplayPort 2.0, HDMI 2.1, and SLVS-EC
  - Low-speed video I/O standards: SLVS, LVDS
- Integrated MIPI D-PHY support enabling MIPI CSI-2 and MIPI DSI-2
- Support for multiple processor interfaces including USB, SPI, PCIe, I2C, Ethernet and customized interfaces that enable communication with host processor systems
- Support for 300 MHz clock frequency on E-Series FPGAs and 600 MHz clock frequency for D-Series FPGA for efficient 4K and 8K video designs
- Easy-to-use Video and Vision Processing Suite IP for streamlined, flexible implementation of different pixel-in-parallel architectures

FPGA supports testing of multiple LCD displays in the same video controller for DUT as shown in the block diagrams in Figure 1 and Figure 2.

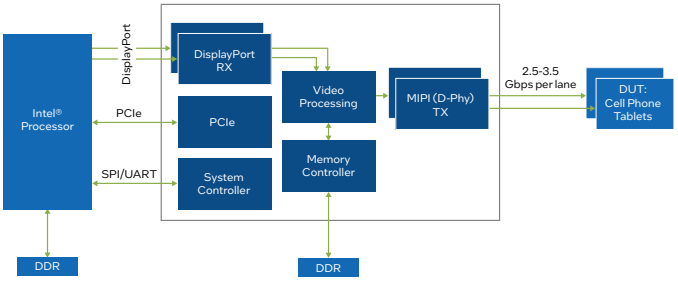


Figure 1. Display ATE with MIPI D-Phy interface to the DUT

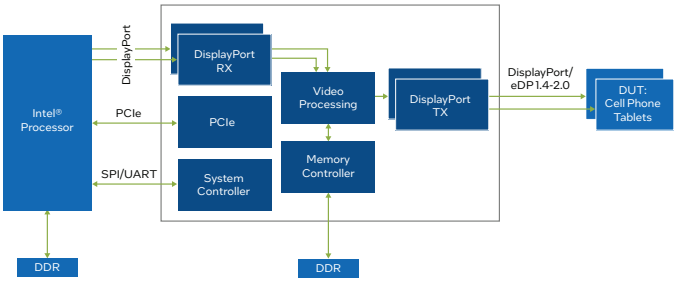
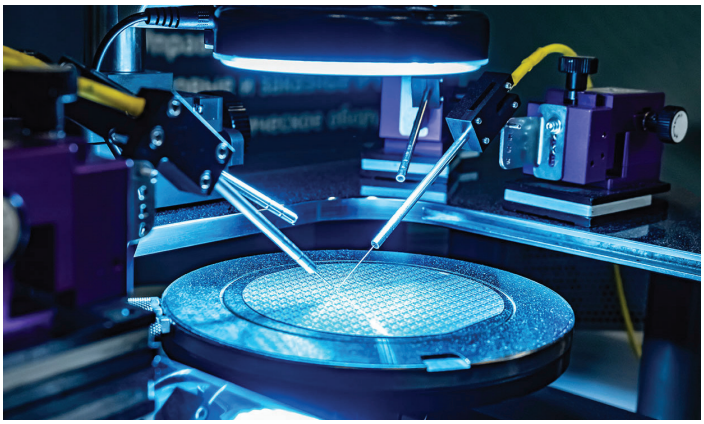


Figure 2. Display ATE with DisplayPort interface to the DUT

Semiconductor Automated Test Equipment



Semiconductor ATE is made up of various instruments or cards that are used to test memory, digital, mixed-signal, and system-on-a-chip (SoC) components at both the wafer and packaged stages. These test systems are evolving in response to consumer, computing, and communication market demand. To keep up with semiconductor industry innovation, today's ATE products must provide more functionality at faster speeds than ever before.

Why D-Series FPGAs and E-Series FPGAs for Semi ATE:

- Built-in I/O delay with picosecond granularity
- Hardened memory controller for external DDR4/5/ LPDDR4/5 memory interfacing
- History of 15+ years of product life cycle support

Figure 3 demonstrates a typical block diagram of semiconductor automated test equipment where FPGA can generate and analyze the test patterns needed for the DUT*.

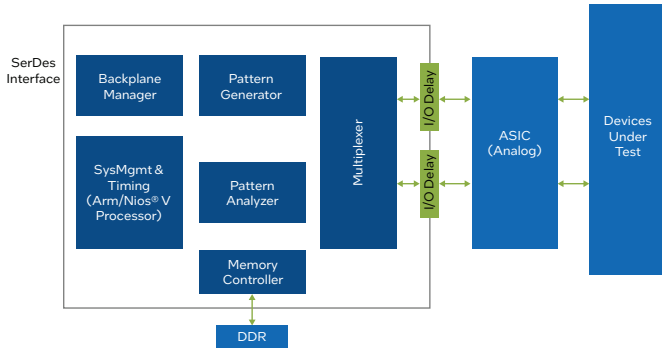
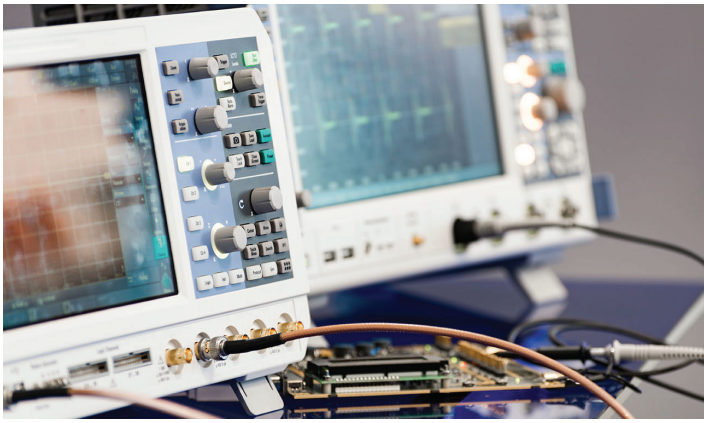


Figure 3. Example system design for semiconductor ATE

RF Test Instrumentation



Due to the widespread adoption of Wi-Fi 6 and 5G, wireless sensors and devices are now present almost everywhere. This rapid adoption has increased the demand for high-efficiency, portable testing equipment. Wideband Spectrum Analyzers, Signal Generators, and Scopes are required to test and maintain the wireless communication equipment required to ensure that RF networks are functional and fully operational. This is crucial because RF networks are often a main part of critical infrastructure, such as the power grid or emergency vehicle communication services. Figure 4 shows a typical RF test instrument block diagram. A variety of analog and digital interfaces are required for test equipment. To efficiently analyze or generate RF signals, signal processing with high efficiency and low latency is required.

Why D-Series FPGAs and E-Series FPGAs for RF Test Instrumentation:

- Wide density range (100K LE to 650K LE) with high-speed on-chip memory and high-performance AI-enabled tensor DSP block to enable custom solution
- Various host processor connections possible ranging from on-chip Arm subsystem to highly efficient and resource-optimized Nios® V processor
- History of 15+ years of product life cycle support
- Hardened memory controller for external DDR4/5/ LPDDR4/5 memory interfacing

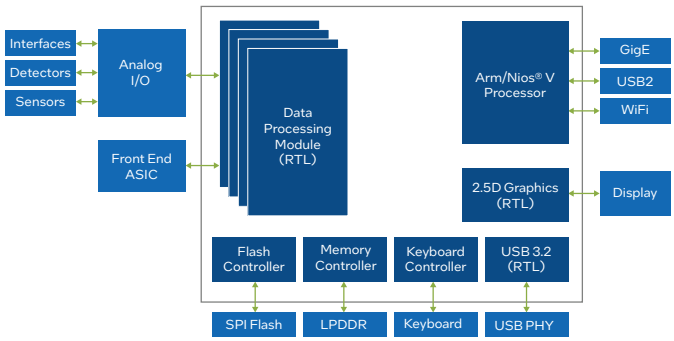


Figure 4. Example system design for low-end oscilloscope for RF testing

Conclusion

There are many reasons to consider using next-generation D-Series FPGAs and E-Series FPGAs for your display testers, semiconductor ATE, and RF test instrumentation needs. In addition to delivering on power, performance, IP availability, support and compatibility with the latest connectivity protocols and processor interfaces, and feature robustness, Intel FPGA offers design support from industry veterans from the Intel FPGA Design Services team. To learn more about creating your own test and measurement systems that leverage these new Intel Agilex® 5 FPGAs, reach out to your local Intel sales representative.

Learn More

Intel Agilex® 5 FPGAs

- Product Information: www.intel.com/content/www/us/en/products/details/fpga/agilex/5.html
- White paper: www.intel.com/content/www/us/en/products/docs/programmable/agilex-5-fpga-whitepaper.html

Intel Agilex® 5 FPGAs E-Series

- Product Information: www.intel.com/content/www/us/en/products/docs/programmable/agilex-5-e-series-fpga.html

Intel Agilex® 5 FPGAs D-Series

- Product Information: www.intel.com/content/www/us/en/products/docs/programmable/agilex-5-d-series-fpga.html

IP and Design Examples

- Video and Vision Processing Suite
- HDMI Intel® FPGA IP User Guide
- DisplayPort Intel® FPGA IP User Guide

Military and Secure Communication Systems

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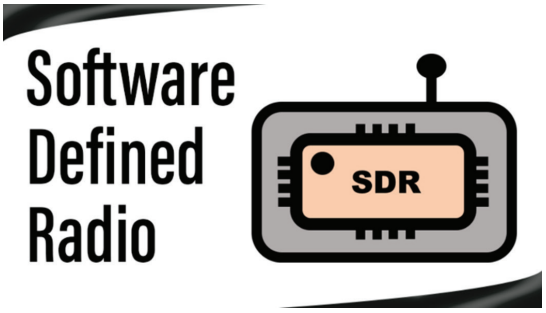
Field Programmable Gate Arrays for Software Defined Waveforms

Modern military communication systems are built around flexible and robust waveforms so that they can be modified and updated with software and firmware upgrades. This is to enable longer field life and utility for soldier, vehicle, and modular communication systems for both voice and data. It also enables radios to switch contexts from waveform to waveform using programmable technologies like FPGAs, reducing size, weight and power when enabling multiple waveforms and channels on a single silicon processing technology.

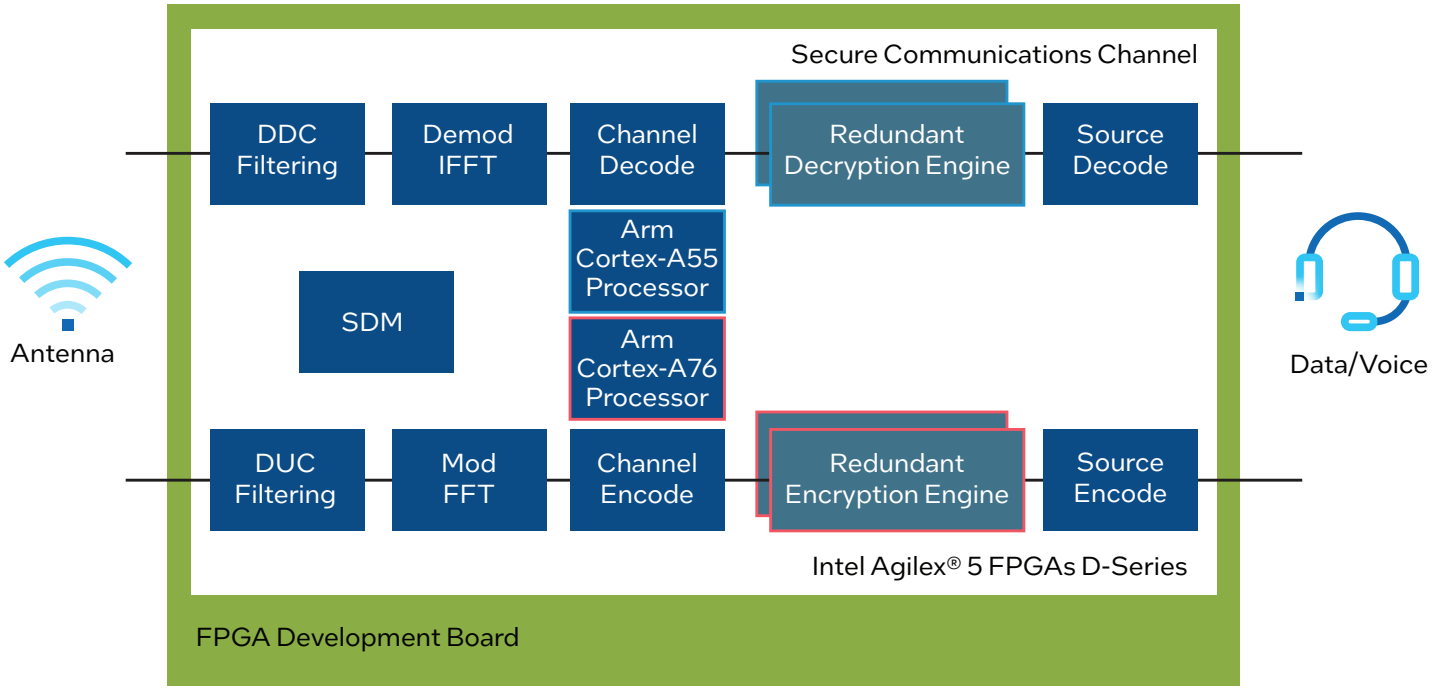


Hardened Cryptographic Services and Custom Logic Cryptography

The primary advantage of using an FPGA for Secure Communication systems is the ability to customize and enable field upgrade to the system. Therefore, utilizing FPGA logic to build customized communication channel encryption and authentication allows for iterative development cycles to meet strict security audit and accreditation. In addition, however, Intel Agilex® 5 FPGAs D-Series and Intel Agilex® 5 FPGAs E-Series also provide 'Cryptographic Services', which enables user access to the FPGA's hardened cryptographic blocks used for bitstream security. These services, including a full hardened key management subsystem, allows designers to have standard cryptographic capabilities in addition to your custom cryptographic design. D-Series and E-Series FPGAs are available with either the Cryptographic Services enabled, or disabled if customers do not plan to use these services to simplify export categorization.

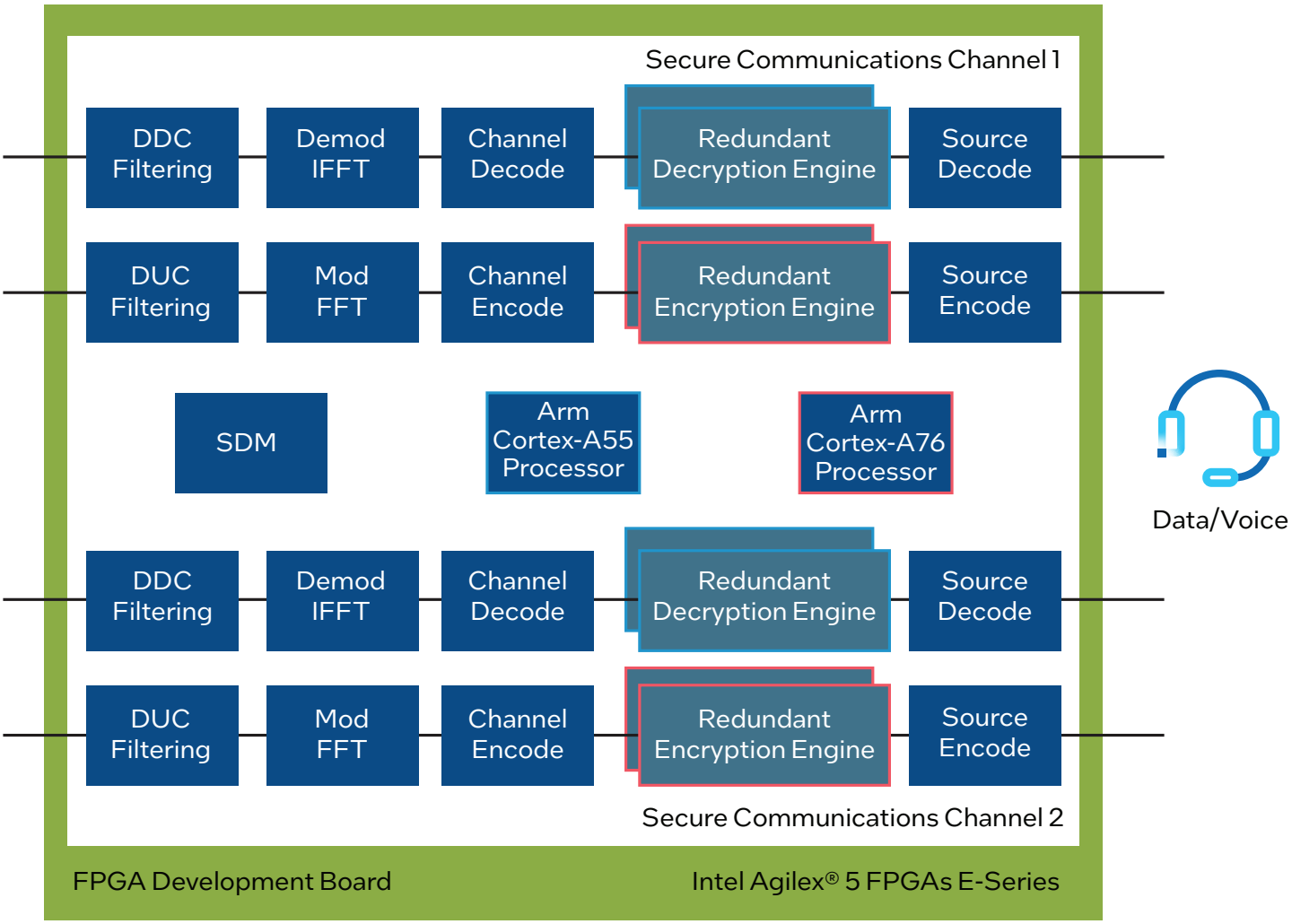
Single Channel Radio Systems with D-Series FPGAs

The D-Series FPGA, with low static power fabric, Secure Device Manager assisted security, and high-speed transceivers provides all the tools needed to develop custom and specialty communication systems for military and federal users.



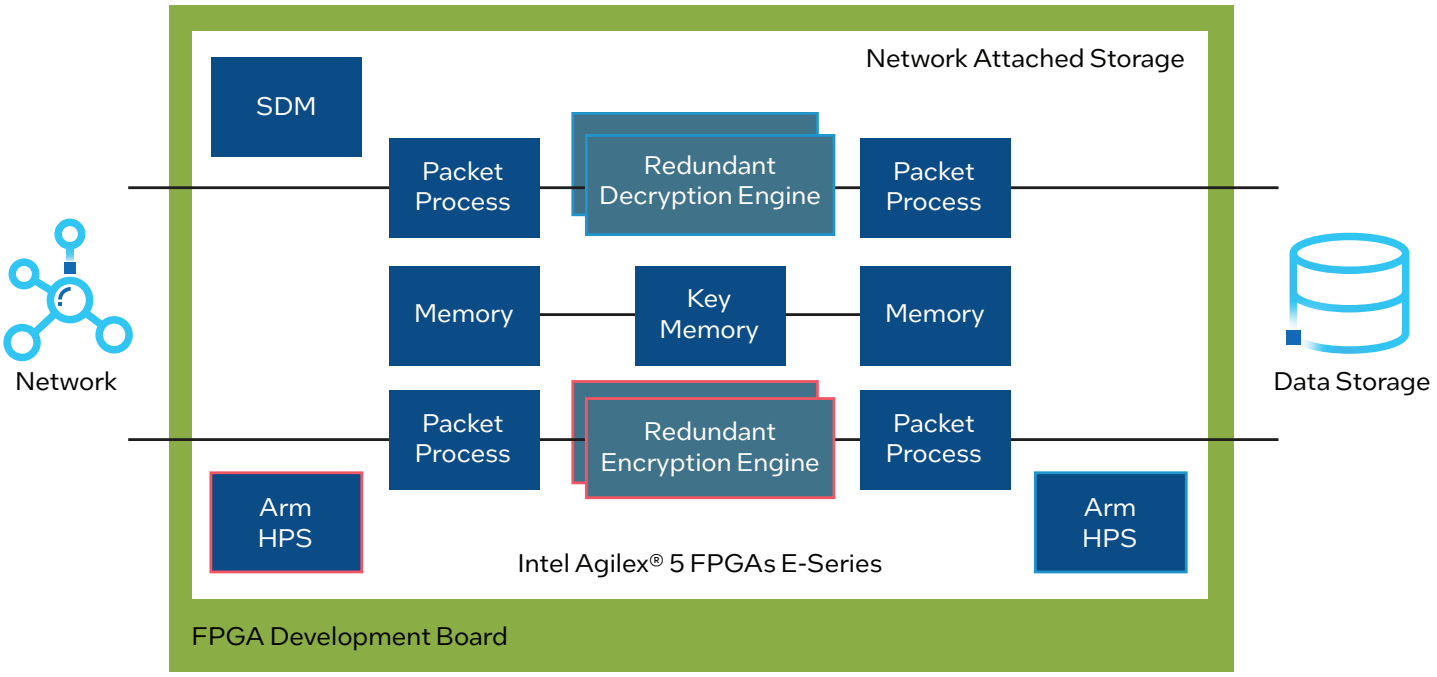
Multi-Channel Radio Systems with E-Series FPGAs

Higher density in E-Series FPGAs and D-Series FPGAs enable the same capabilities with multichannel systems, as well as the ability to enforce the same logic separation boundaries between channels.



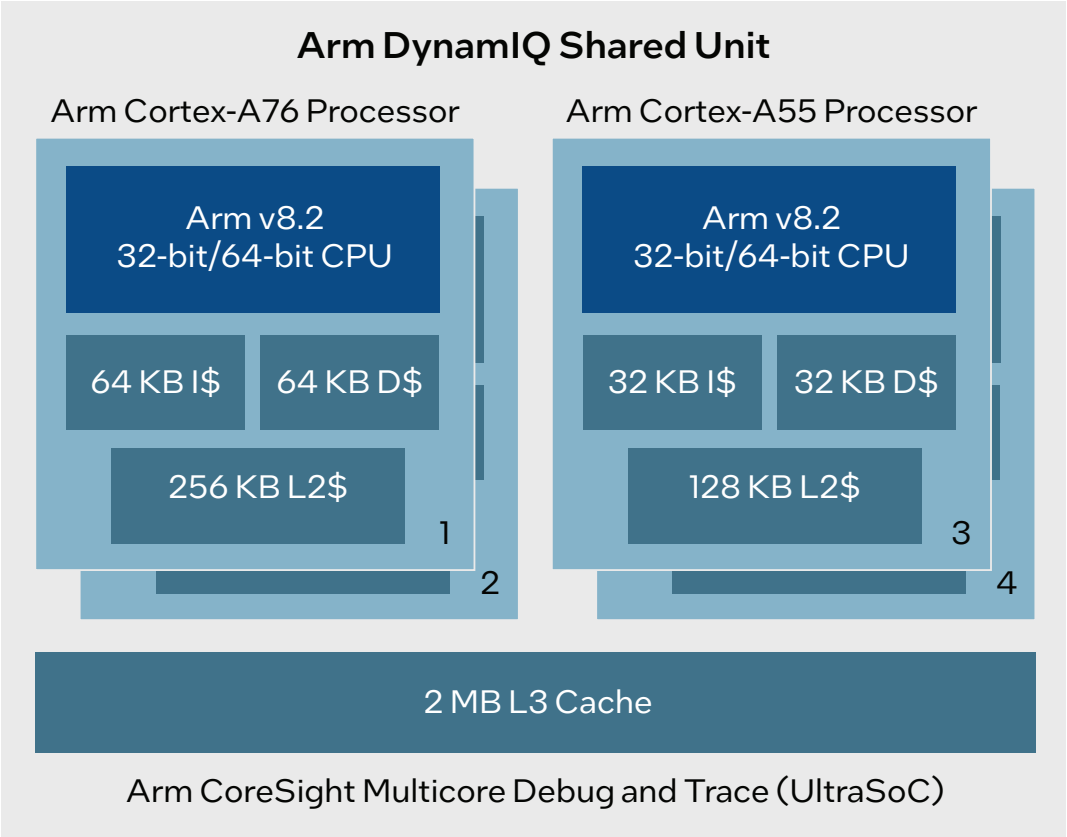
Wideband Data Systems with E-Series FPGAs

High-speed data systems for military and federal use also have similar requirements for separation and redundancy for handling sensitive information, making FPGAs another valuable development technology. Using even higher performance E-Series FPGAs and D-Series FPGAs for these systems provides all the same design separation tools and cryptographic services for high performance data management.



Multiple Hard Processor Subsystems

The E-Series FPGA and D-Series FPGA uses an Arm v8.2 architecture, including a multi-core Arm Cortex processor with dual-core Arm Cortex-A76 processor at 1.8 GHz, and dual-core Arm Cortex-A55 processor at 1.5 GHz. This approach provides limited separability between the subsystem cores and some non-shared cache in each system. Though not architected to provide complete electrical and data separation, each multicore subsystem can be separated virtually for control plane purposes.



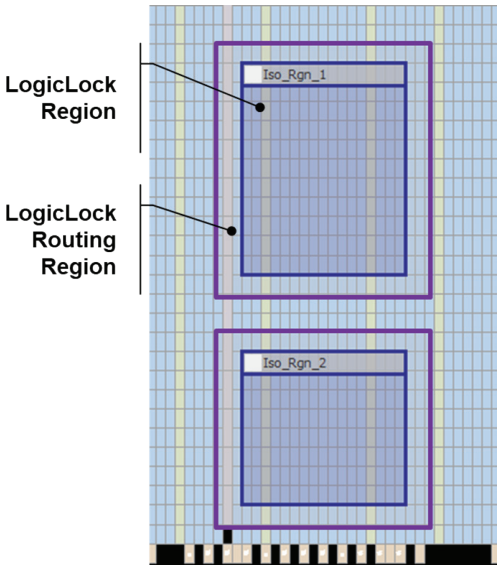
Anti-Tamper Security Features

E-Series FPGAs will be the first low-power and low-density FPGA family to feature the Secure Device Manager as both the secure boot manager of the device (FPGA logic and Arm processor subsystem) and monitoring/ enforcing anti-tamper rules, parameters, and responses of the system.

FPGA Design Separation for Cryptographic System and Channel Separation

Intel® FPGAs have long been used for sensitive cryptographic system designs that require strict hardware separation rules between encrypted data/voice and unencrypted data/voice.

The Intel® Quartus® Prime Software provides several tools, including Logic Lock and Chip Planner, that enable communication system development to enforce both logic and logic routing to be restricted to pre-planned or pre-defined regions.



Wireless Spotlight

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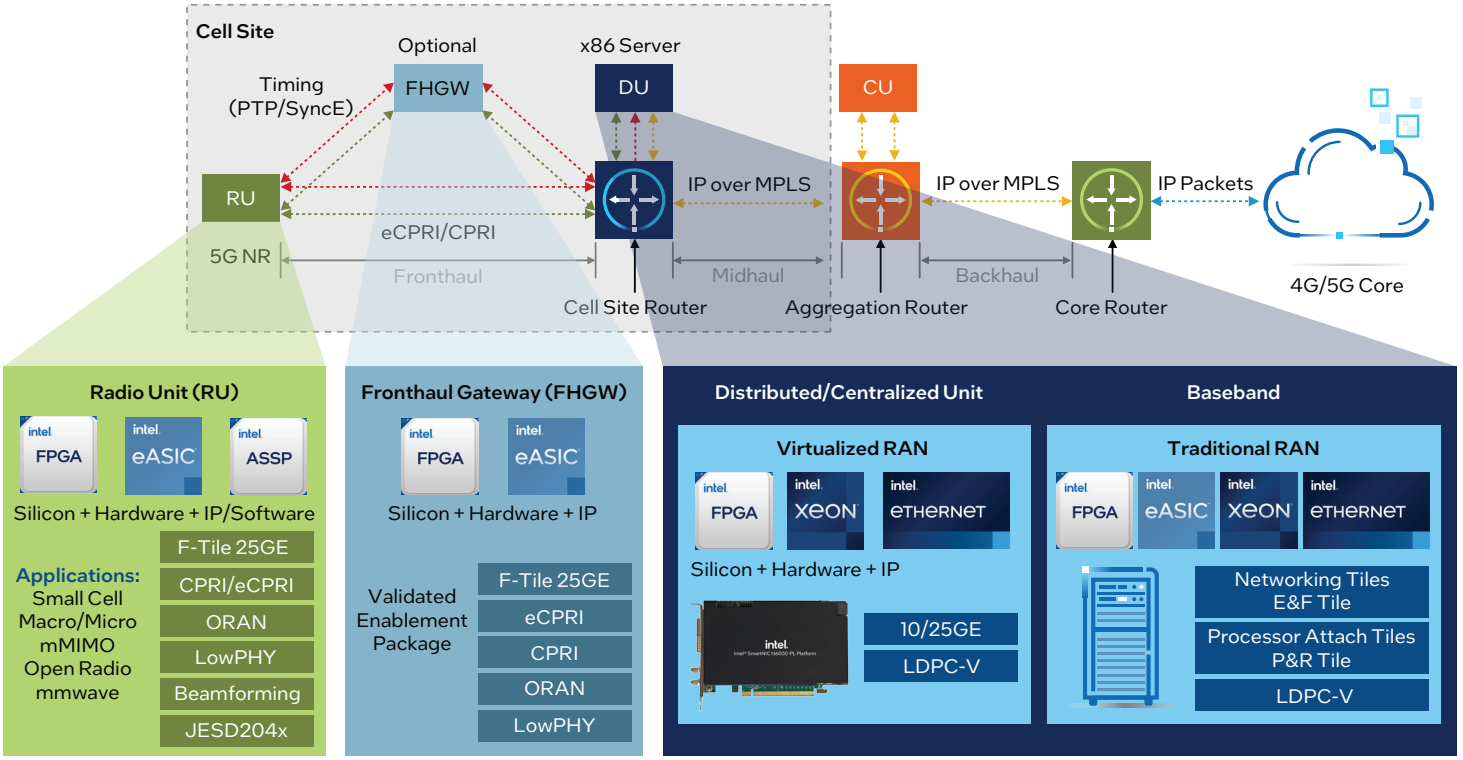
Intel in the RAN

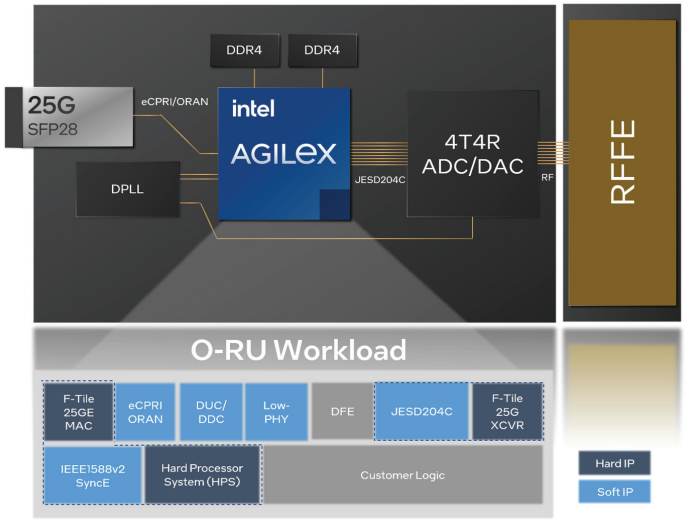


Intel® FPGAs Built for Radio Access Network (RAN)

The race to 5G is on and quickly looking beyond. Intel FPGAs perform with groundbreaking soft logic and integrated chiplet technology, providing performance where it matters and flexibility when you need it.
Be the first to market with Intel's enablement platforms optimized for efficiency and reduced development costs.

Catch the Next Radio Wave

As the demand for wireless connectivity continues to grow, wireless radios are being deployed in increasingly diverse scenarios, whether for macro coverage, user capacity with massive multiple-input multiple-output (mMIMO), or throughput with millimeter wave (mmWave). From commercial mobile networks to private enterprises and manufacturing plants, radios are complex systems that deal with many frequency bands, output power levels, bandwidths, different standards, functional splits, and radio frequency/antenna requirements. Radios must be more flexible and powerful than ever before while operating reliably in tough thermal environments and meeting cost targets. With the recent introduction of Intel Agilex® 5 FPGAs built on the Intel 7 process technology, Intel's broad FPGA portfolio enables up to 2.5X fabric performance and up to 50% lower total power consumption compared to previous generation Cyclone® V FPGAs[1]. Intel's radio enablement silicon, intellectual property (IP) cores, and software adheres to radio platforms of all sizes.



Intel's Open Radio Access Network (ORAN) enablement package model is valuable to customers in their product development as they can reduce design, integration, and verification time by leveraging a fully integrated workload pre-validated on hardware. These designs serve as a blueprint, reducing the time and effort required to design a complex product from scratch. Additionally, Intel's ORAN enablement packages have been thoroughly tested and validated, reducing the risk of design errors and improving the reliability of the final product. By providing a proven and tested design, Intel's enablement packages help customers save time and resources, reducing product development costs and headaches.

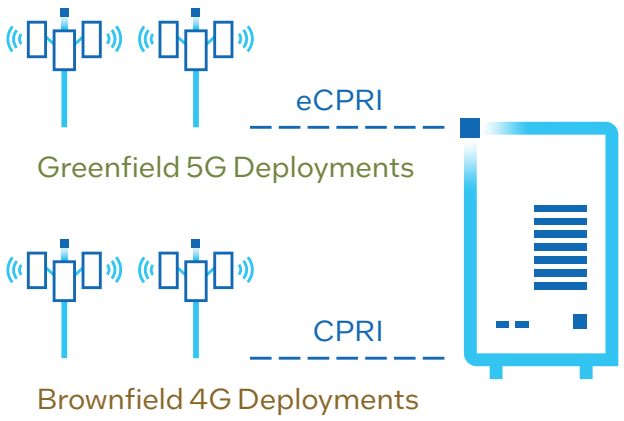
Radio Enablement Package

Macro/Micro | mMIMO | Small Cells | mmWave | RU

[1] Reference: https://edc.intel.com/content/www/us/en/products/performance/benchmarks/agilex-fpga/

Fronthaul Gateway

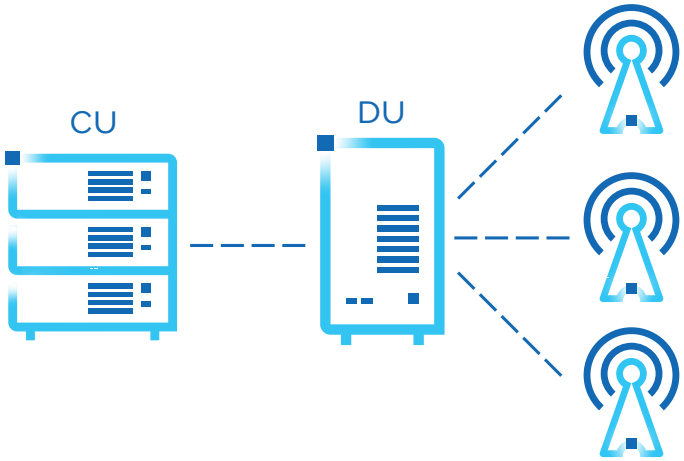
Radio units come in all shapes and sizes with unique bands, antenna configurations, bandwidths, subcarrier spacing, multiplexing, functional splits, and connectivity requirements. The fronthaul gateway aggregates these diverse radio connections, including both legacy 4G (i.e., Split 8) and newer 5G (i.e., Split 7.x), and consolidates them into an ORAN-compliant fronthaul while offering Layer 1 offloading capabilities. Intel provides a comprehensive cell enablement package that accelerates development, minimizes operational and capital costs, and shortens the time required to bring fronthaul appliances to market.



The Distributed Unit, the Heart of the Cell Tower

Distributed units come in all shapes and sizes. Intel FPGAs enable inline and sidecar processing applications with low latency, high bandwidth, and 5G-ready security. Over-the-wire RTL reprogramming allows operators to scale and upgrade hardware like software.

More specifically, the Intel Agilex 5 FPGA was designed to meet the requirements and new technologies enabled within the distributed unit (DU). Artificial intelligence (AI) workloads are coming to the RAN, and the wide density range of Intel Agilex 5 FPGAs – from 100K logic elements (LEs) to 650K LEs – with high-speed on-chip memory and high-performance AI Tensor Blocks enables custom AI workload deployments in the DU.



Intel FPGA SmartNIC N6000-PL Platform

Whether you're supporting brownfield or greenfield deployments, the Intel FPGA SmartNIC N6000-PL Platform enhances your network's overall performance, scalability, and capability to unleash its full potential. Intel and partners offer a turnkey virtualized RAN (vRAN) enablement platform for Virtual Cell Site Router (vCSR), Low-Density Parity Check (LDPC), and fronthaul/security offload leveraging the Intel FPGA SmartNIC N6000-PL Platform. This, in turn, drives fast vRAN adoption and high performance, significantly reducing operational and capital expenses while accelerating time to market.

PTP Synchronization

The demands for Precision Time Protocol (PTP) synchronization scale across multiple verticals and are becoming a network prerequisite, with requirements becoming ever so stringent. All communication networks require an appropriate level of clock synchronization across the different devices that comprise the network. Traditional implementations utilizing PTP employ proprietary or basic open source. These servos are inadequate for many real-world network deployments as they do not allow scaling across products, and even create vendor lock-in with the digital clock synthesizer (DCS) provider.

To address this issue, Intel has developed an advanced PTP servo stack that complies with ORAN standards with partial timing support (PTS) networks that is DCS-agnostic. The Intel Precision Time Protocol Servo (Intel PTP Servo) software can be run on Intel Xeon® CPU-based motherboards, Intel Agilex SoC FPGAs, and network interface cards (NICs) with an external DCS and IEEE 1588 support.

Comparison of 1PPS absolute time error measuremennts between Intel PTP Servo and ptp4l

Test Case	FTS (G.8273.2, Noise Gen)		PTS (G.8271.2)		Without Support (G.8261, TC12)	
	Intel PTP Servo	ptp4l PI Servo	Intel PTP Servo	ptp4l PI Servo	Intel PTP Servo	ptp4l PI Servo
|TE|	<5 ns	<5 ns	1 µs	138 µs	4 µs	85 µs

Experience performance with our Intel PTP Servo-based solution. Achieve a PTS peak-to-peak time error of only 1 µs, significantly outperforming the 138 µs result seen with an open-source ptp4l servo[2]. Our innovative solution is DCS-independent, providing reliable and consistent results. By adhering to the conservative network limits of G.8271.2, considered as a 'worst-case' for 5G network deployments, the Intel PTP Servo can be deployed in legacy networks without full timing support (FTS) and avoid the unnecessary costs and complexities of investing in a new FTS network.

[2] Reference: www.intel.com/content/www/us/en/content-details/784715/intel-precision-time-protocol-servo-intel-ptp-servo-solution-for-time-synchronization-applications.html

Intel Agilex 5 FPGAs in Wireless Applications

Intel Agilex 5 FPGAs E-Series provide several key additional benefits for RAN applications such as:

- Low-power Intel-based technology
- Monolithic chip – low cost and power
- 2nd generation Intel Hyperflex™ FPGA architecture
- Density range from 50 to 640K LEs
- Support for IEEE 1588 PTP
- Hardened Time-Sensitive Networking (TSN) endpoint
- Small package, high compute density
- High-performance Arm-based multicore processor
- Comprehensive and very robust security solution
- Hardened floating-point AI Tensor Blocks
- Hard MIPI D-PHY, PCIe*, and Ethernet MAC
- Long product lifecycle
- RISC-V available as a soft processor
- Comprehensive IP ecosystem from Intel and partners

Learn More

Whitepapers

- mMIMO ORAN Radios with Intel Agilex FPGAs
- Intel's F-Tile Wireless Networking Solutions
- Build More Cost-Effective and More Efficient 5G Radios with Intel Agilex FPGAs
- Flexible Performance for 5G vRAN Deployments
- Enabling 5G Fronthaul
- Intel's Accelerated Virtual Cell Site Router Solution
- Intel PTP Servo Solution for Time Synchronization Applications

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