
Architecting Our Next Gen
Power Efficient Processor
intel

Agenda

- Reconstructing Power Efficiency
- Low Power Island
- Hybrid Architecture Vision
- Primer on 3D Performance Hybrid Architecture
- Unpacking Intel® Thread Director
- OS Optimizations
- Rest of SoC and Platform Technologies

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METEOR LAKE

Tile Architecture

IPs matched to process for performance and energy efficiency

Graphics tile - optimized for 3D performance

SoC tile - optimized for power

Compute tile – optimized for CPU performance

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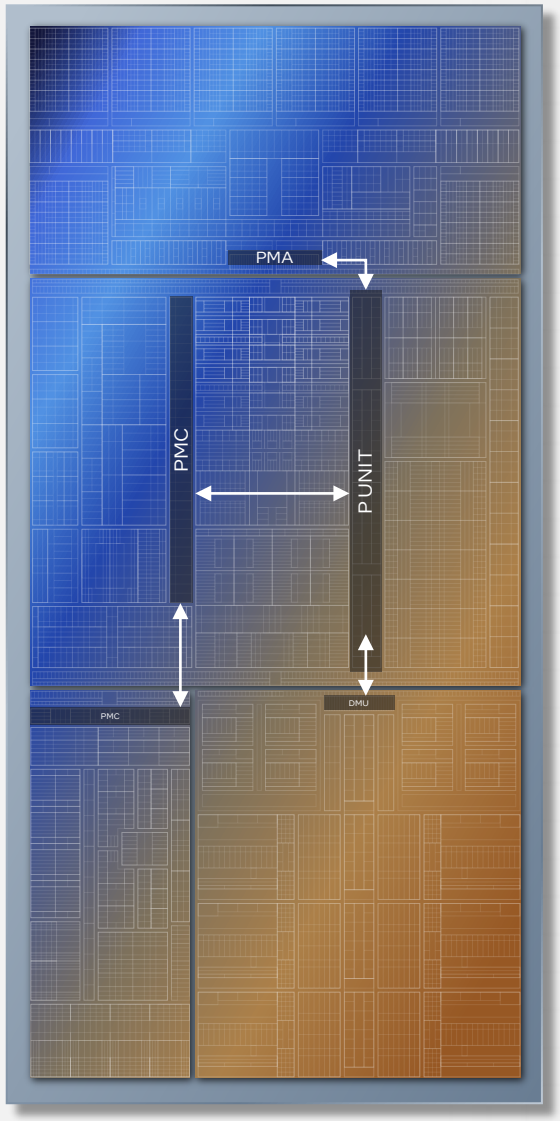

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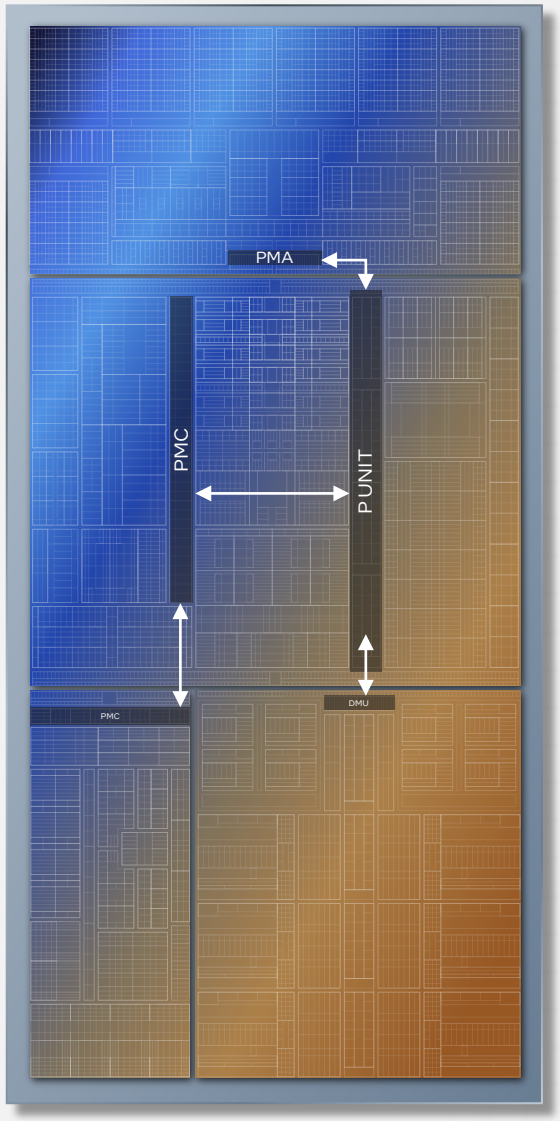
Power Efficiency

New foundations for energy efficiency

- Grounds up **modular and scalable PM** architecture for disaggregation
- New **scalable fabric** for improved bandwidth and energy efficiency
- Coordination between **multiple PM controllers on different tiles**
- Coordination between **SoC PM** controllers and system software



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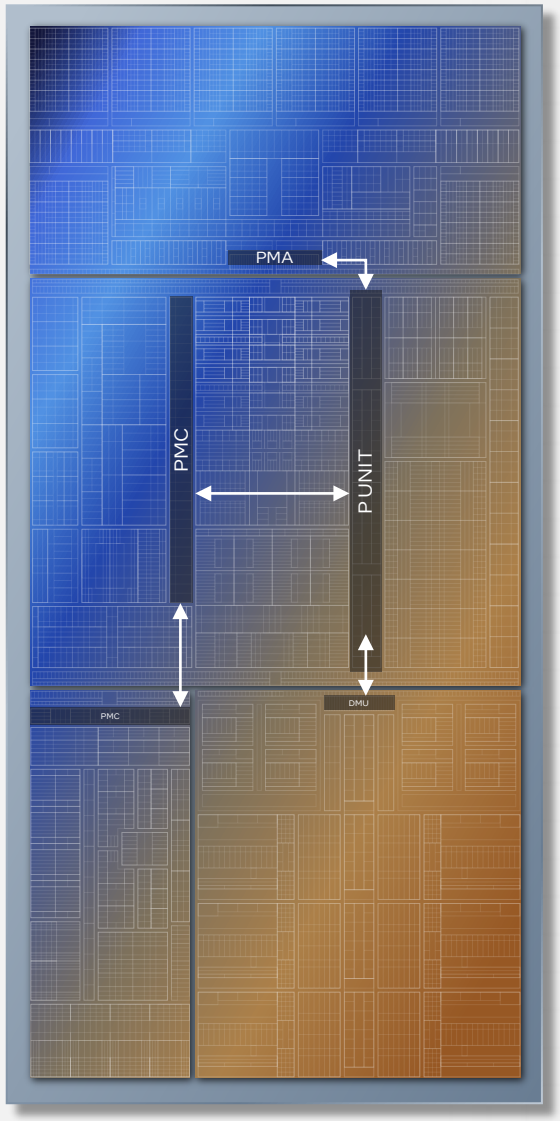

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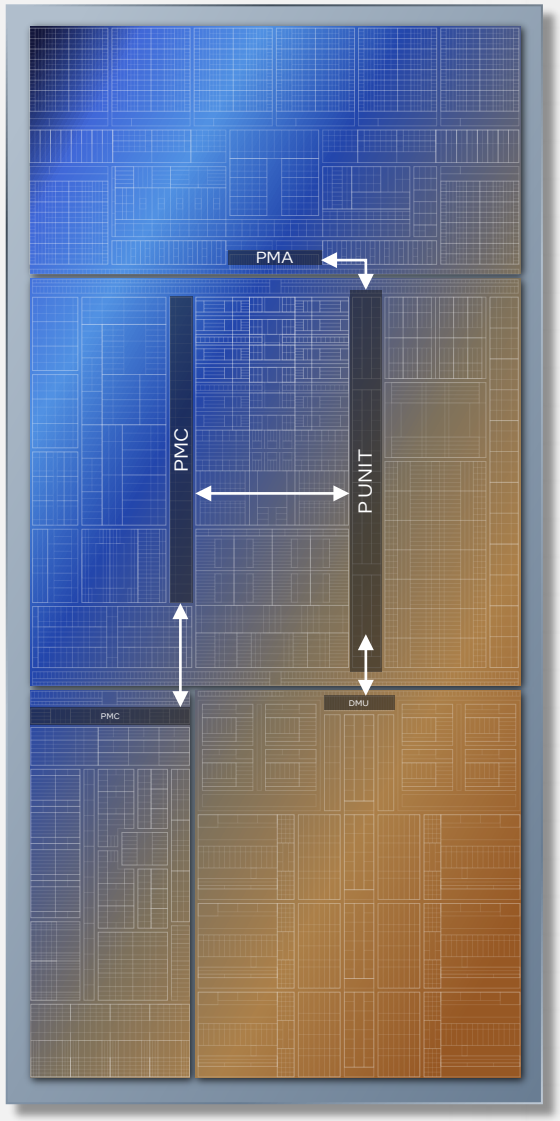

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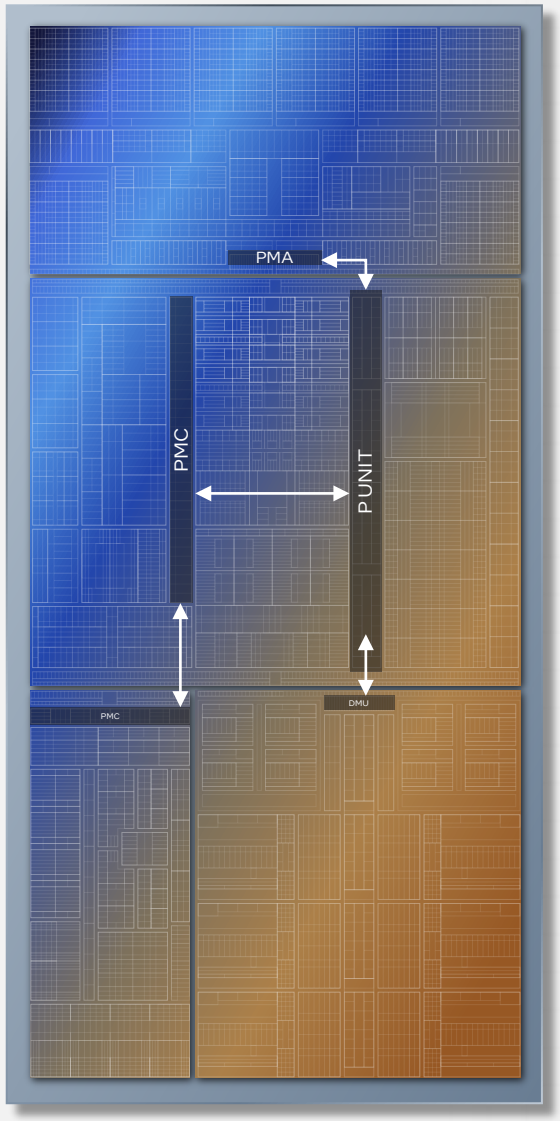

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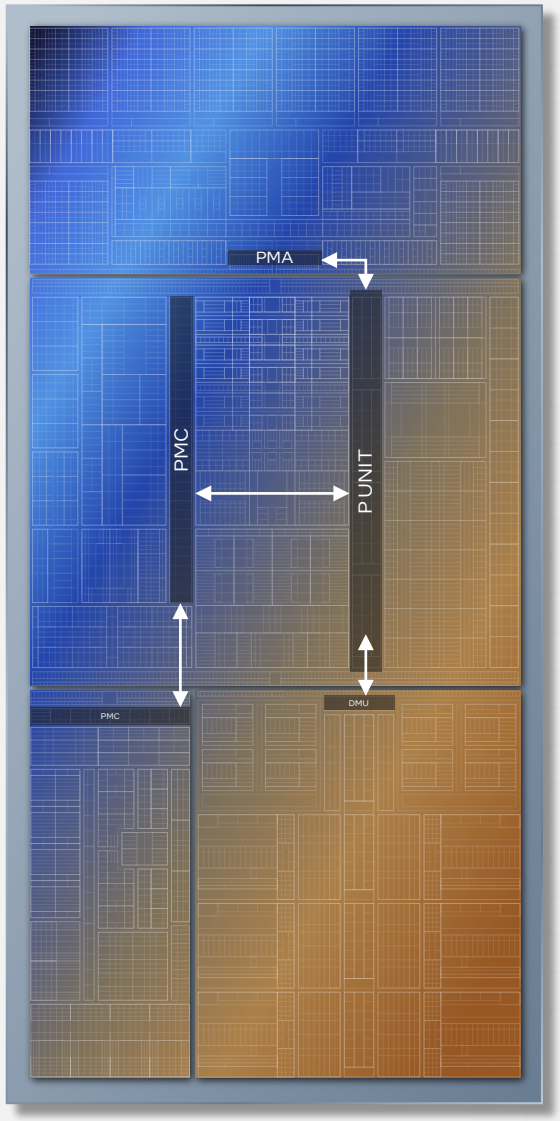

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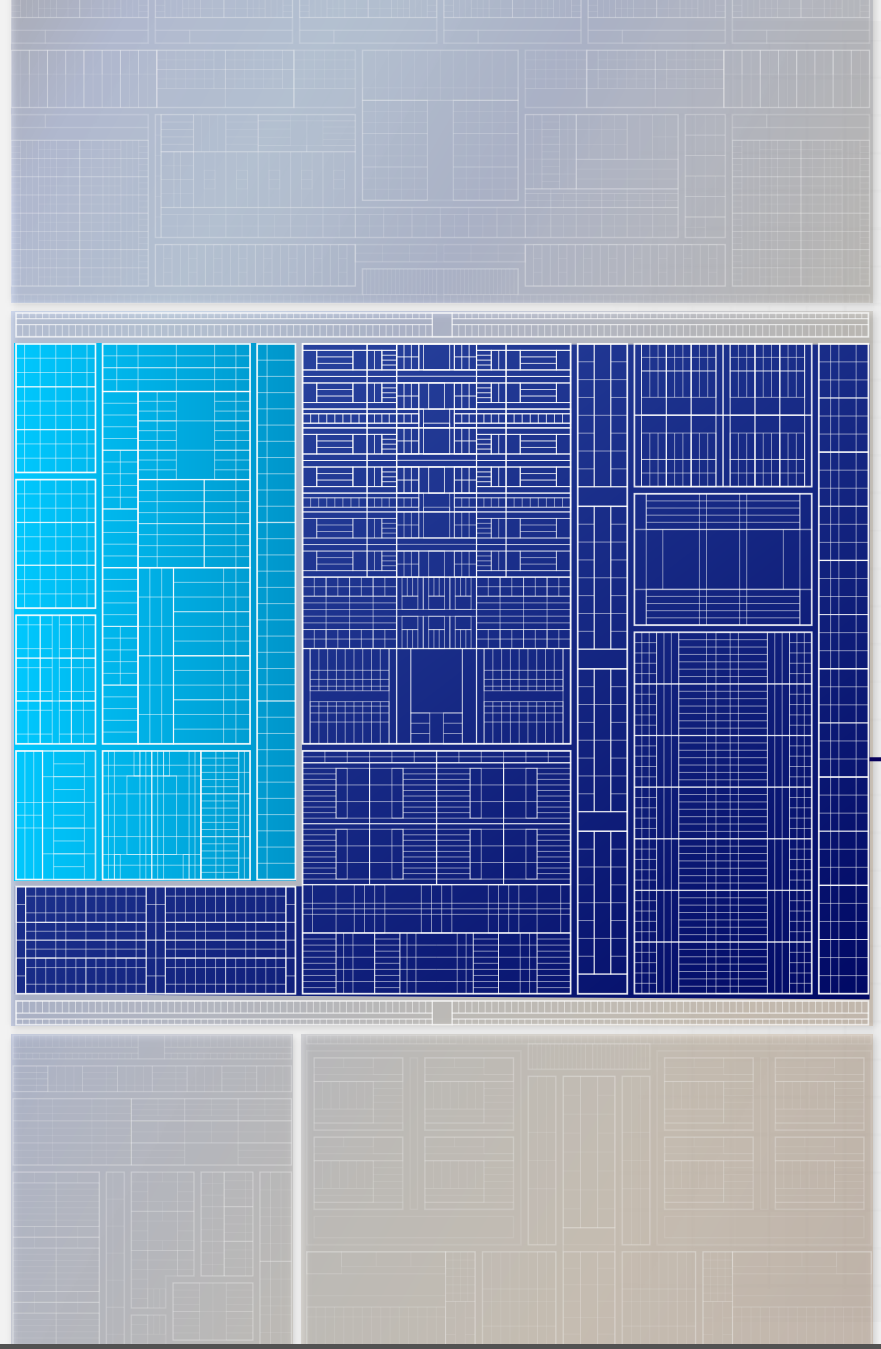

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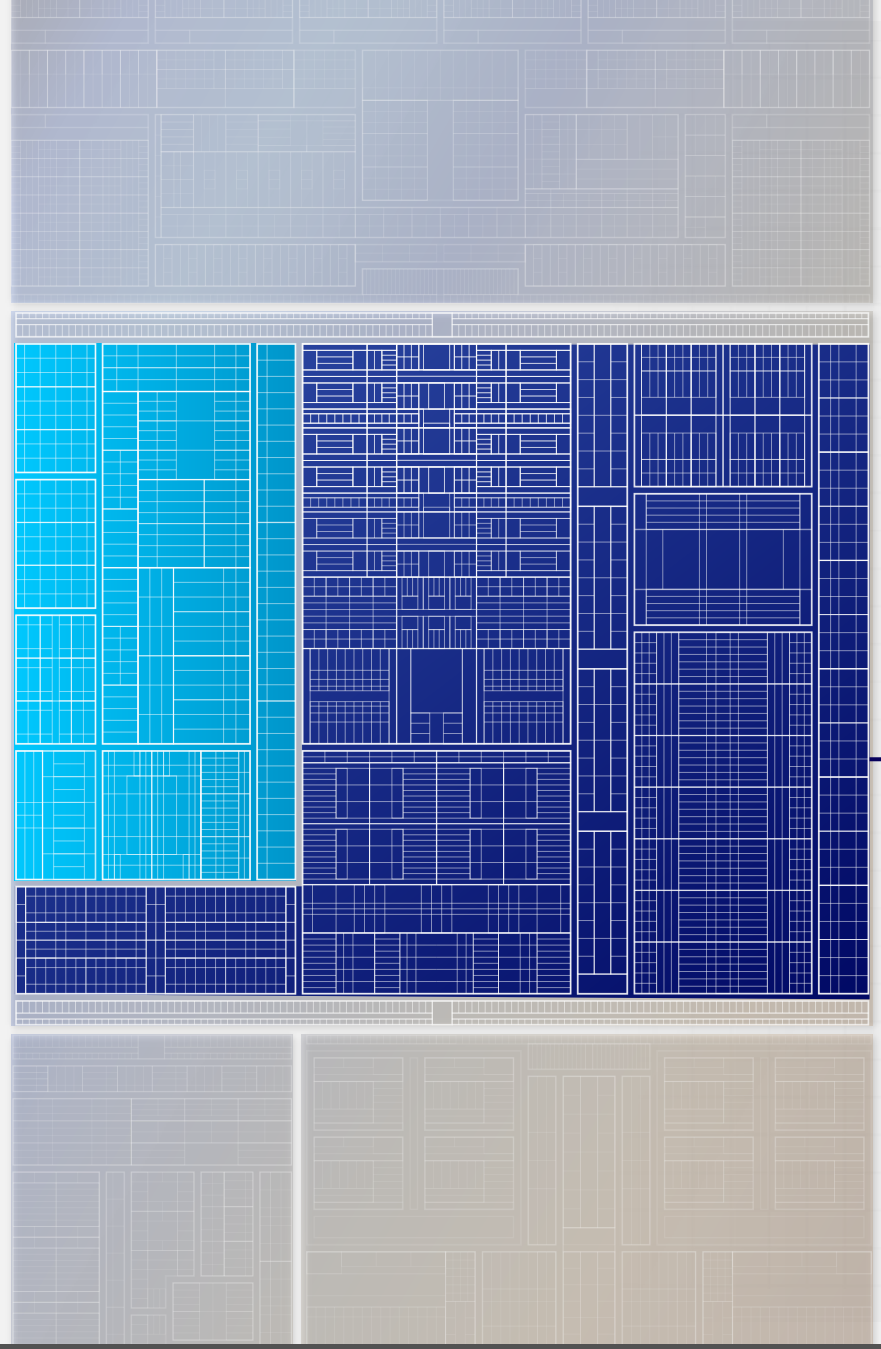
Low Power Island

Built from ground up for efficiency

Components

Memory SS	2x Low Power E-cores	PUNIT	IPU
Media	Display Engine	NPU	Scalable Fabric

- Low Power Island E-cores for light workloads
- Compute die turned on as needed
- Integrated low power AI engine
- IPs to support a wide range of usage



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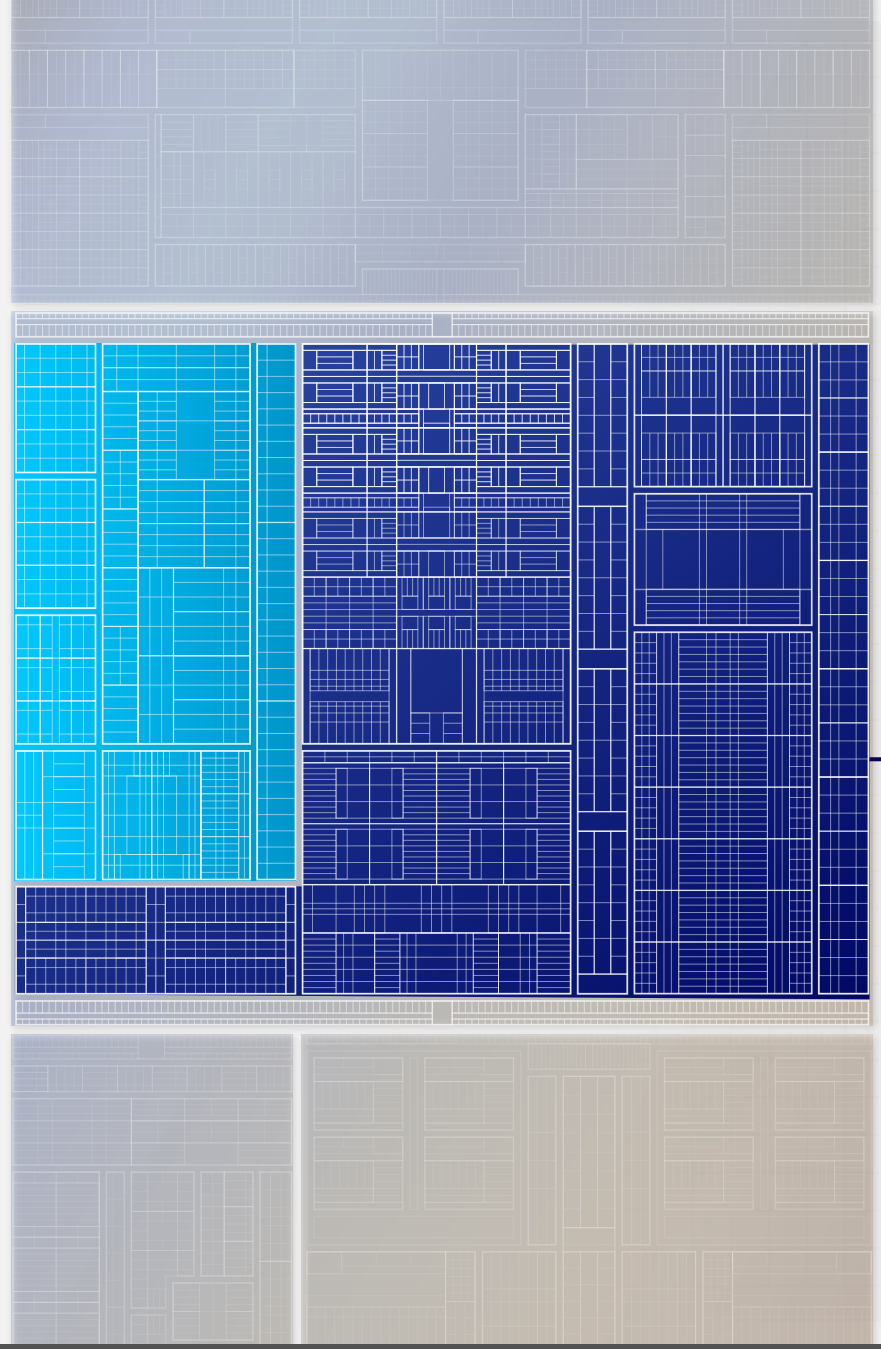

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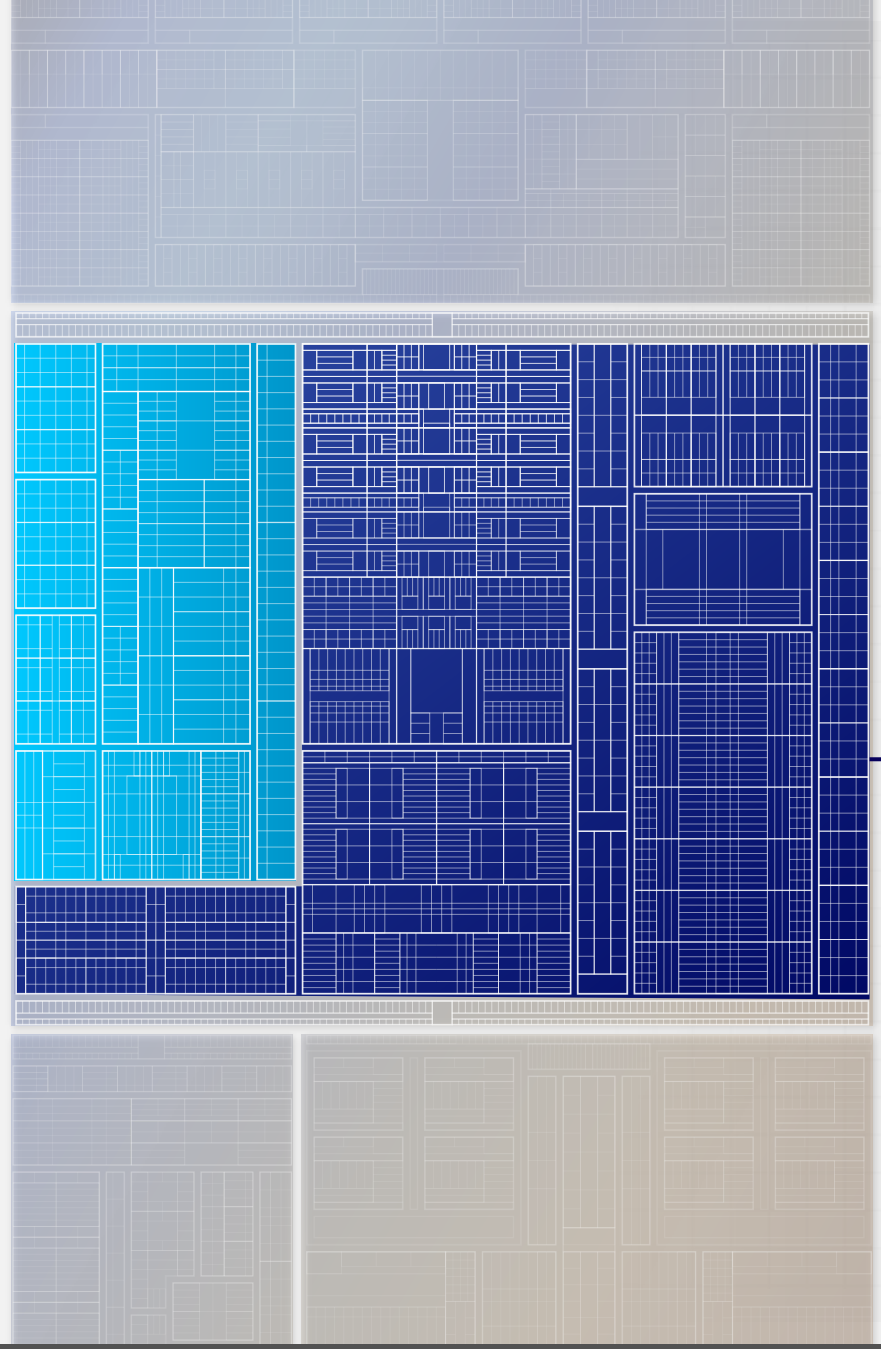

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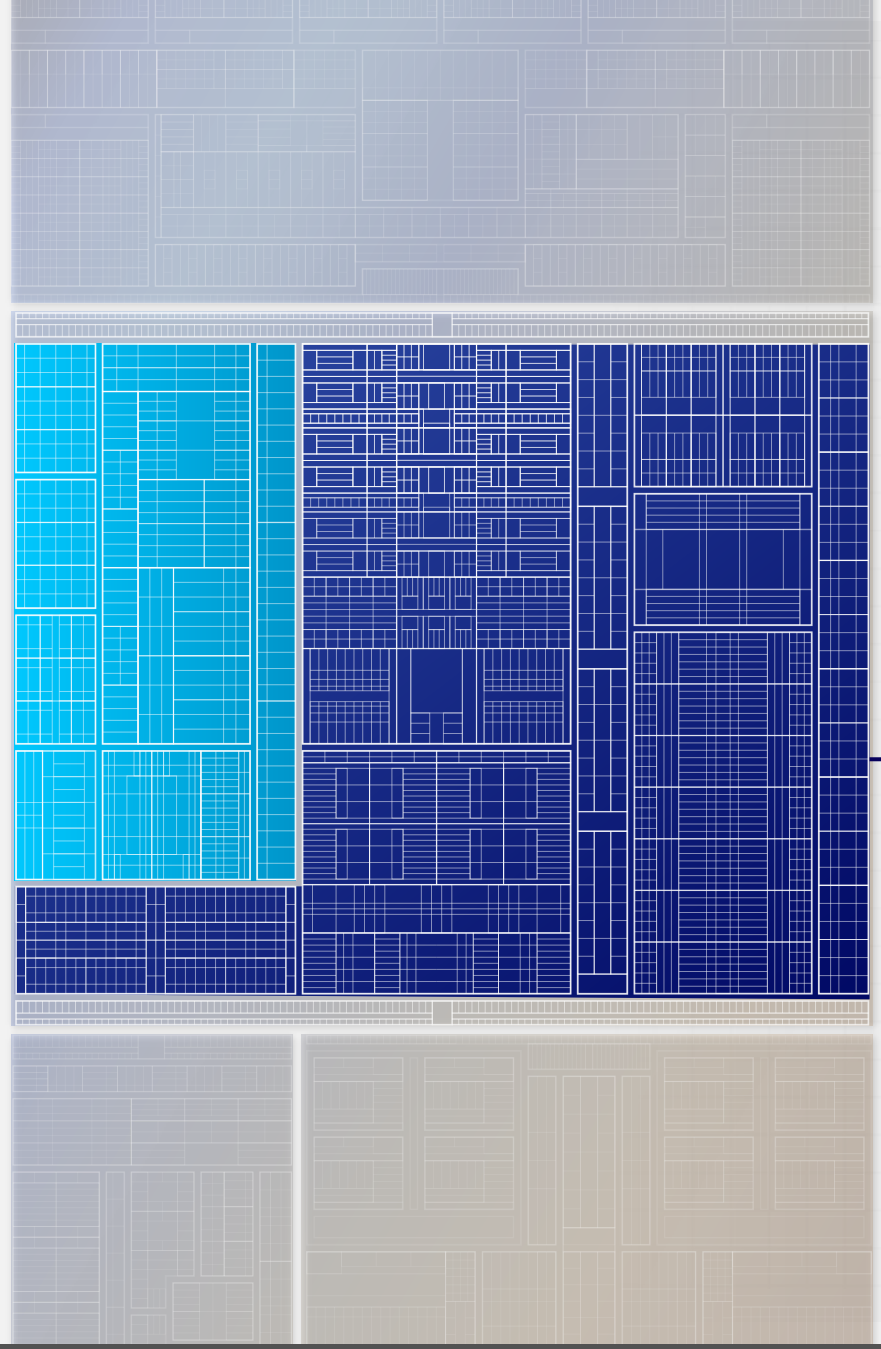

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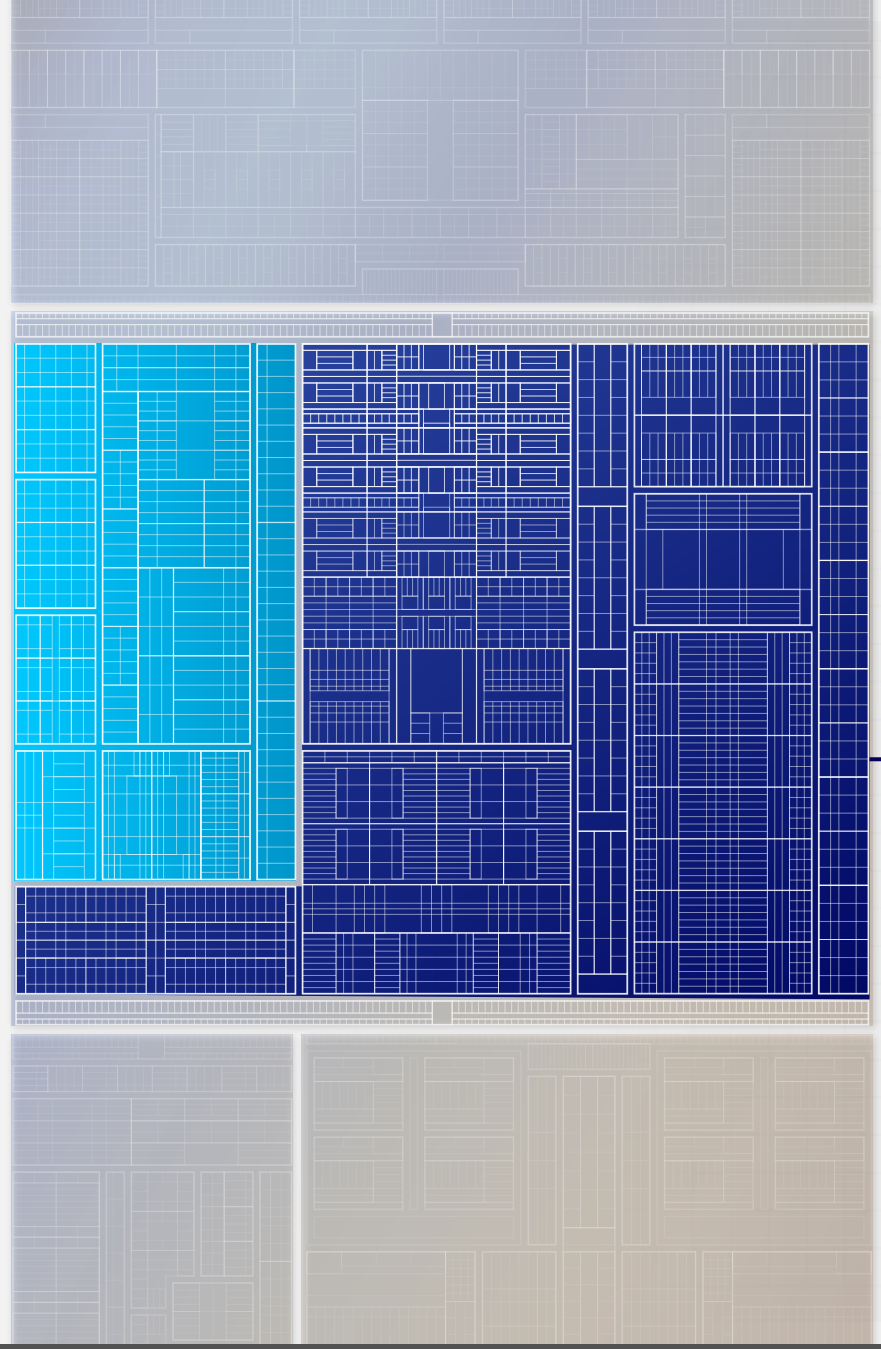

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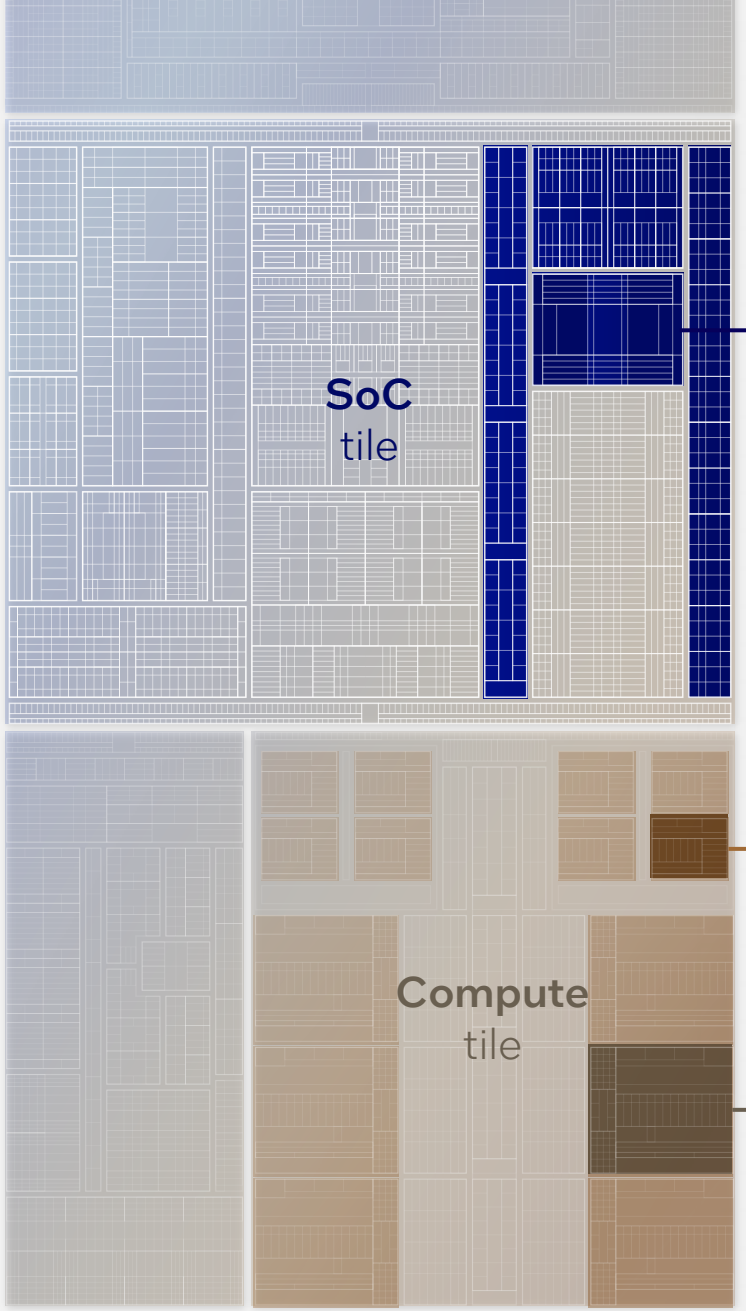
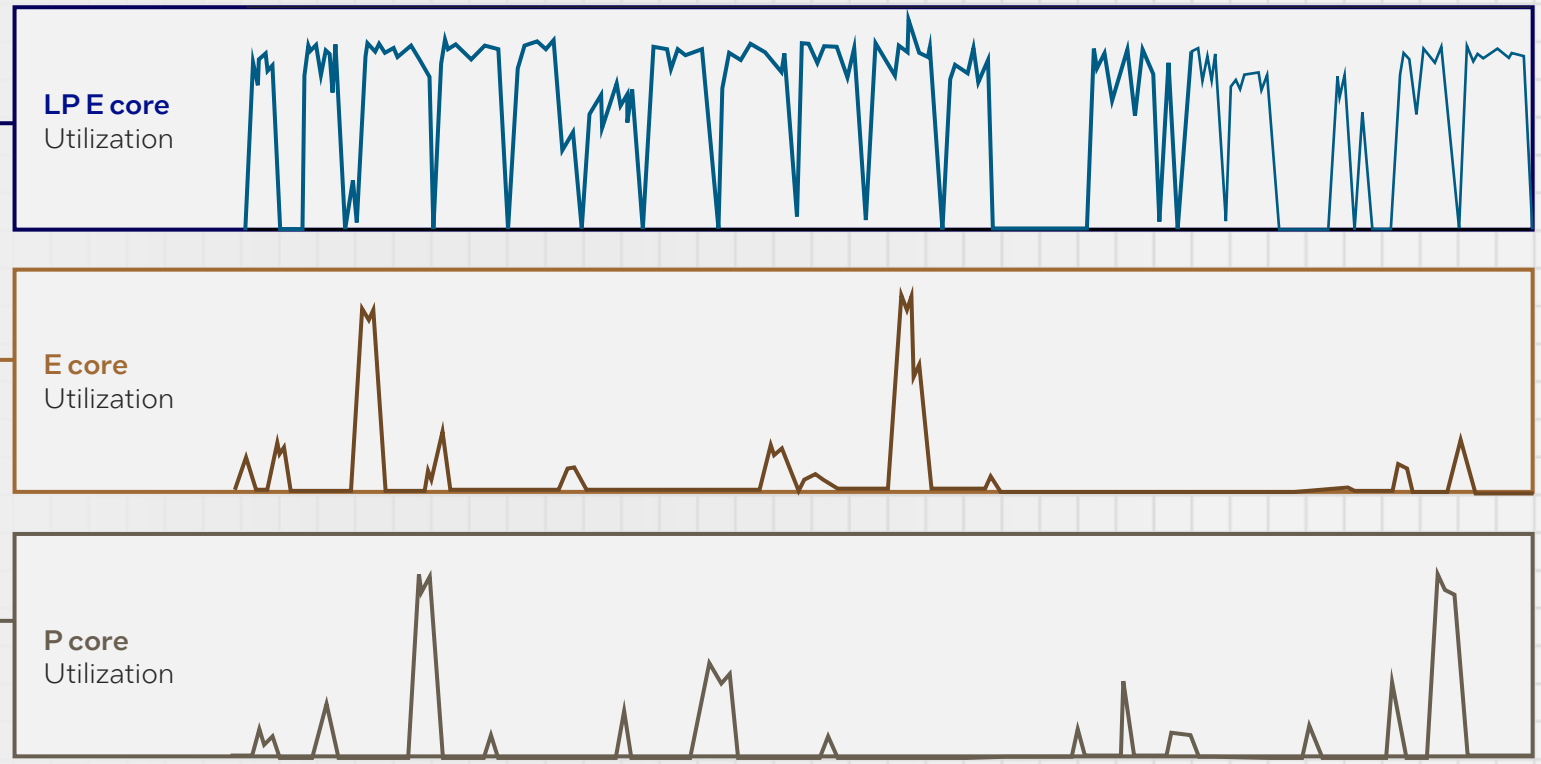
E-cores Usage Example

Most low usage background work (like IT) run on low power E-cores





*Illustrative example of power efficient scheduling

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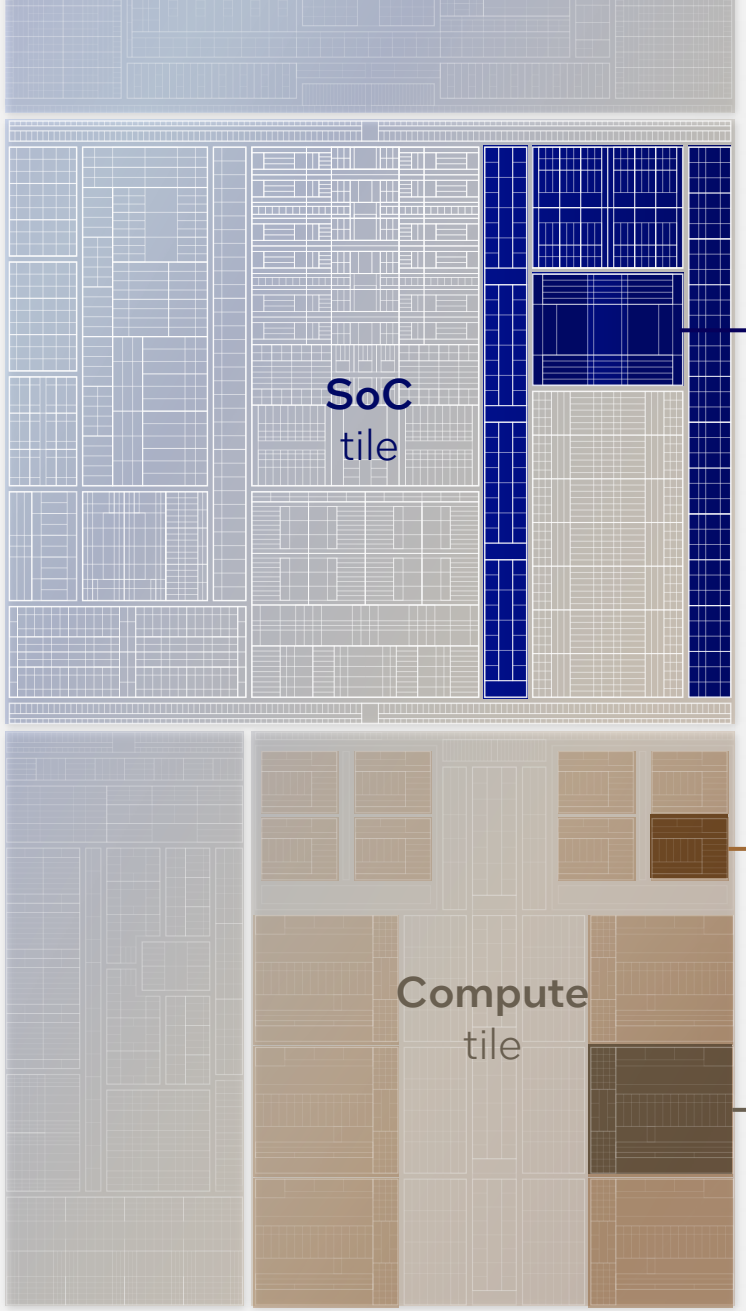

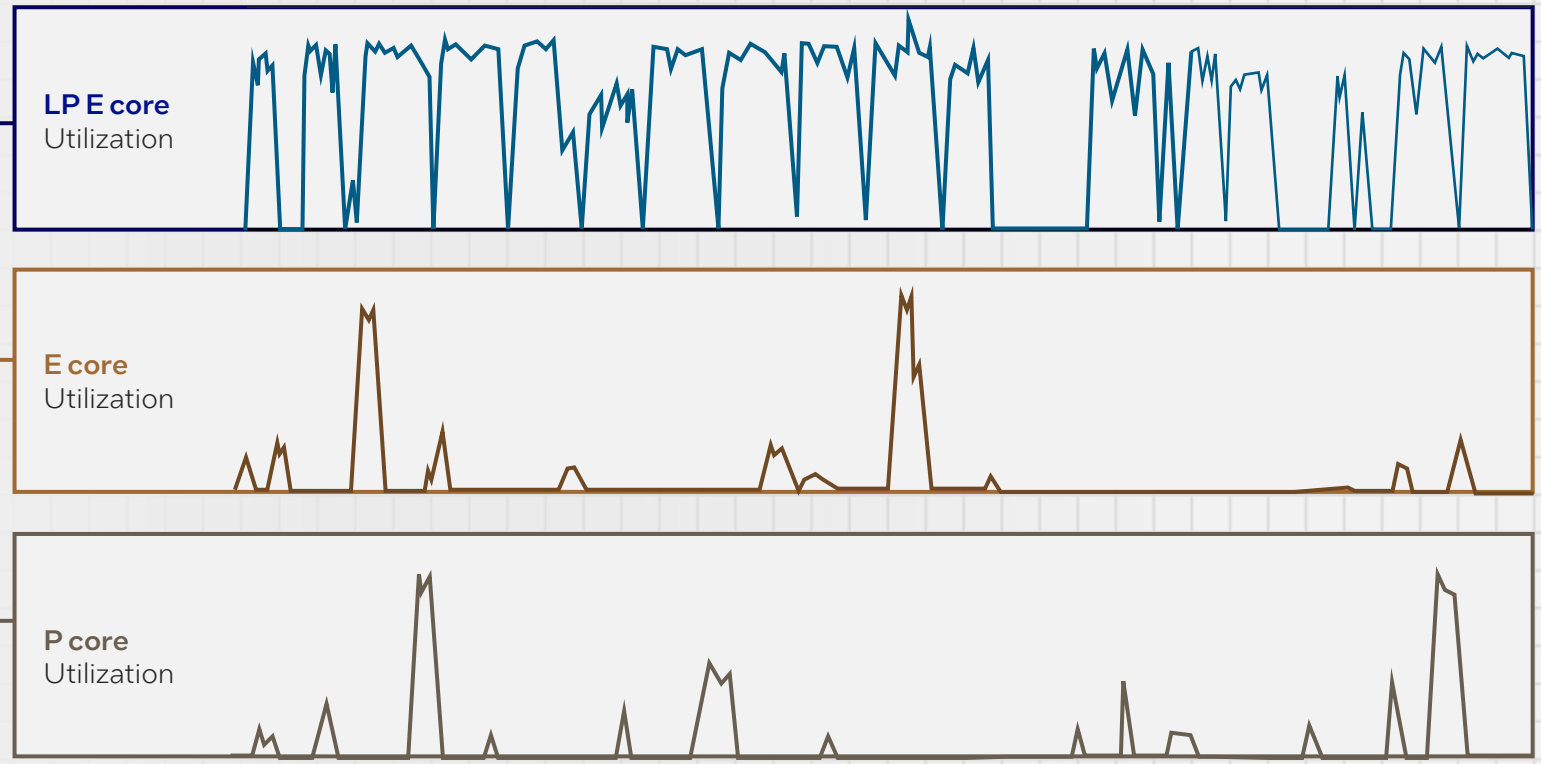

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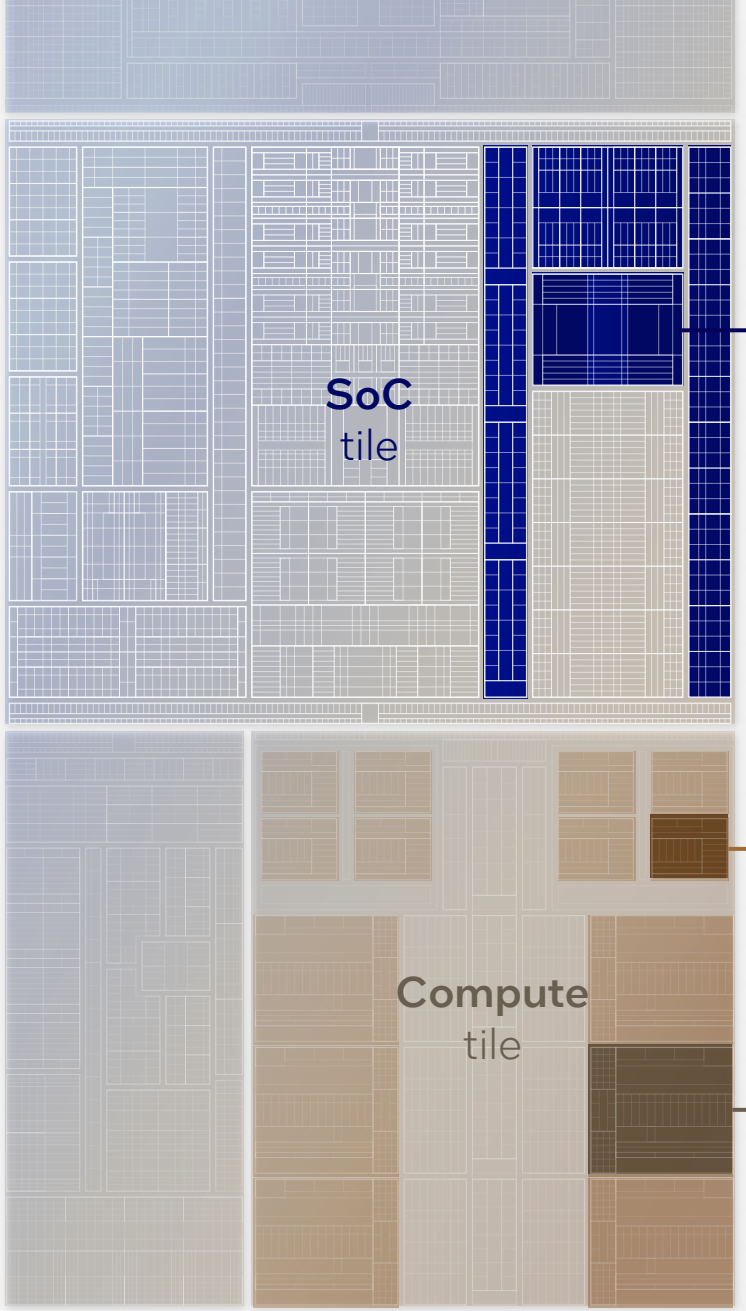

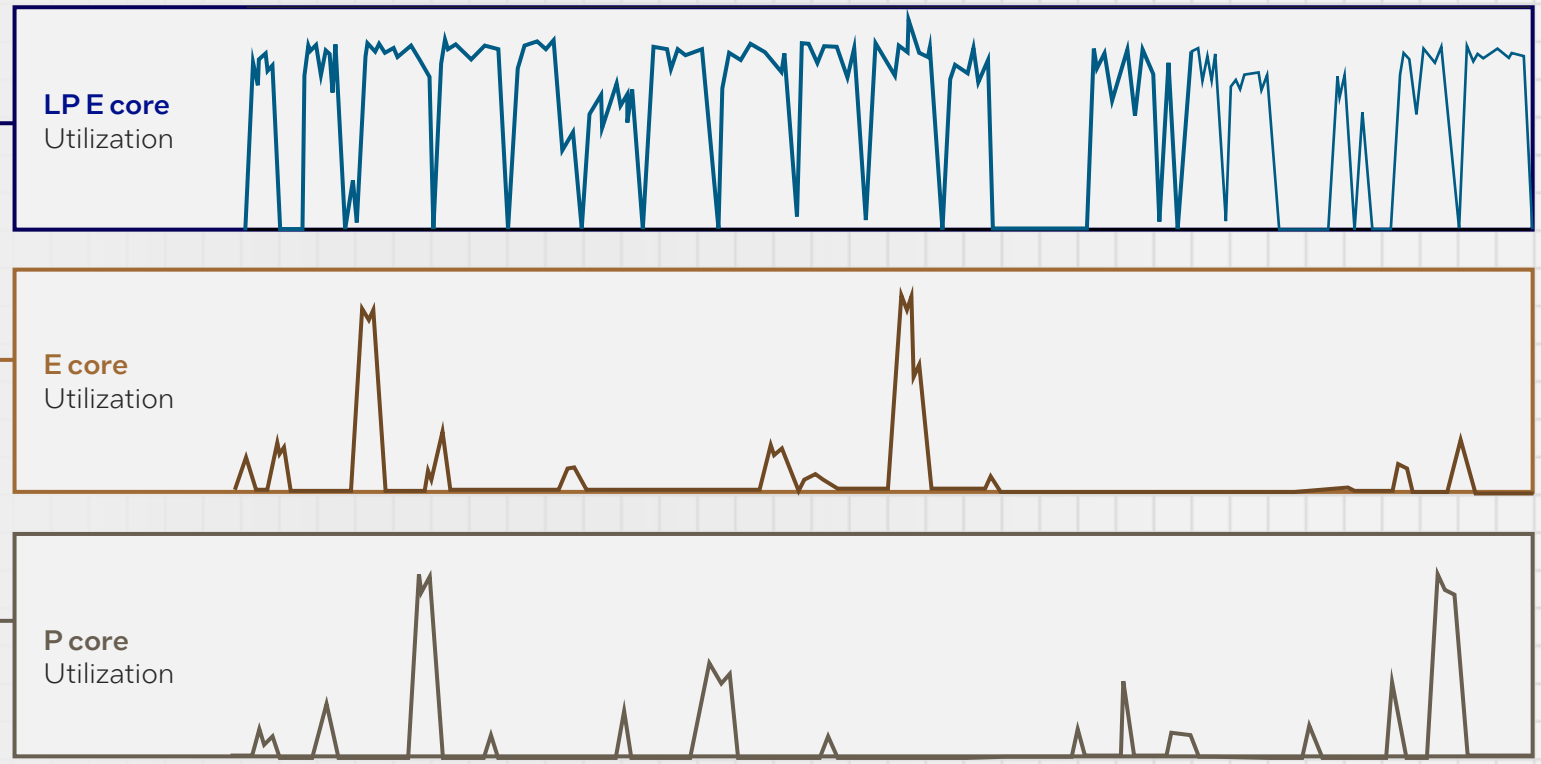

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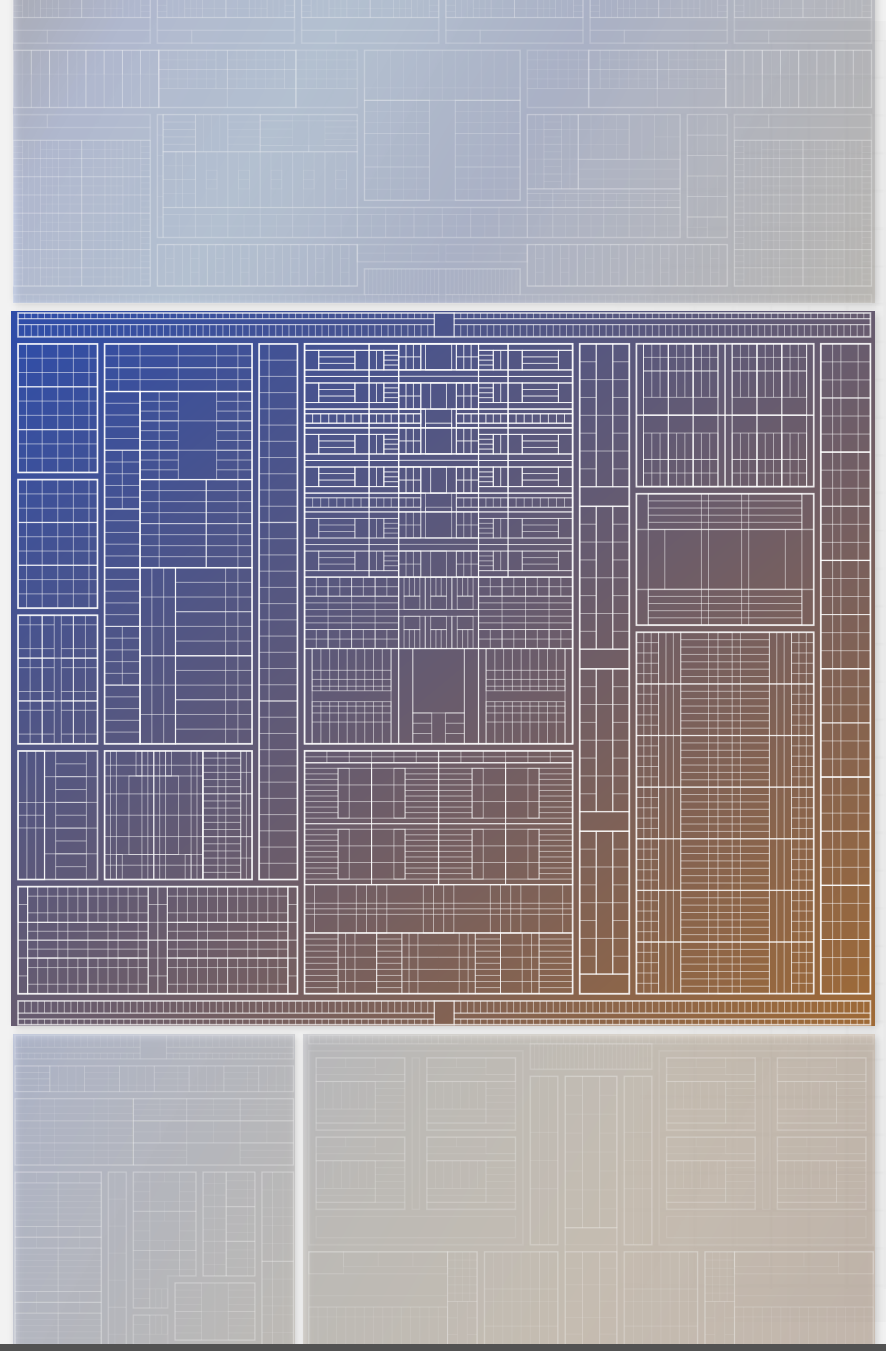

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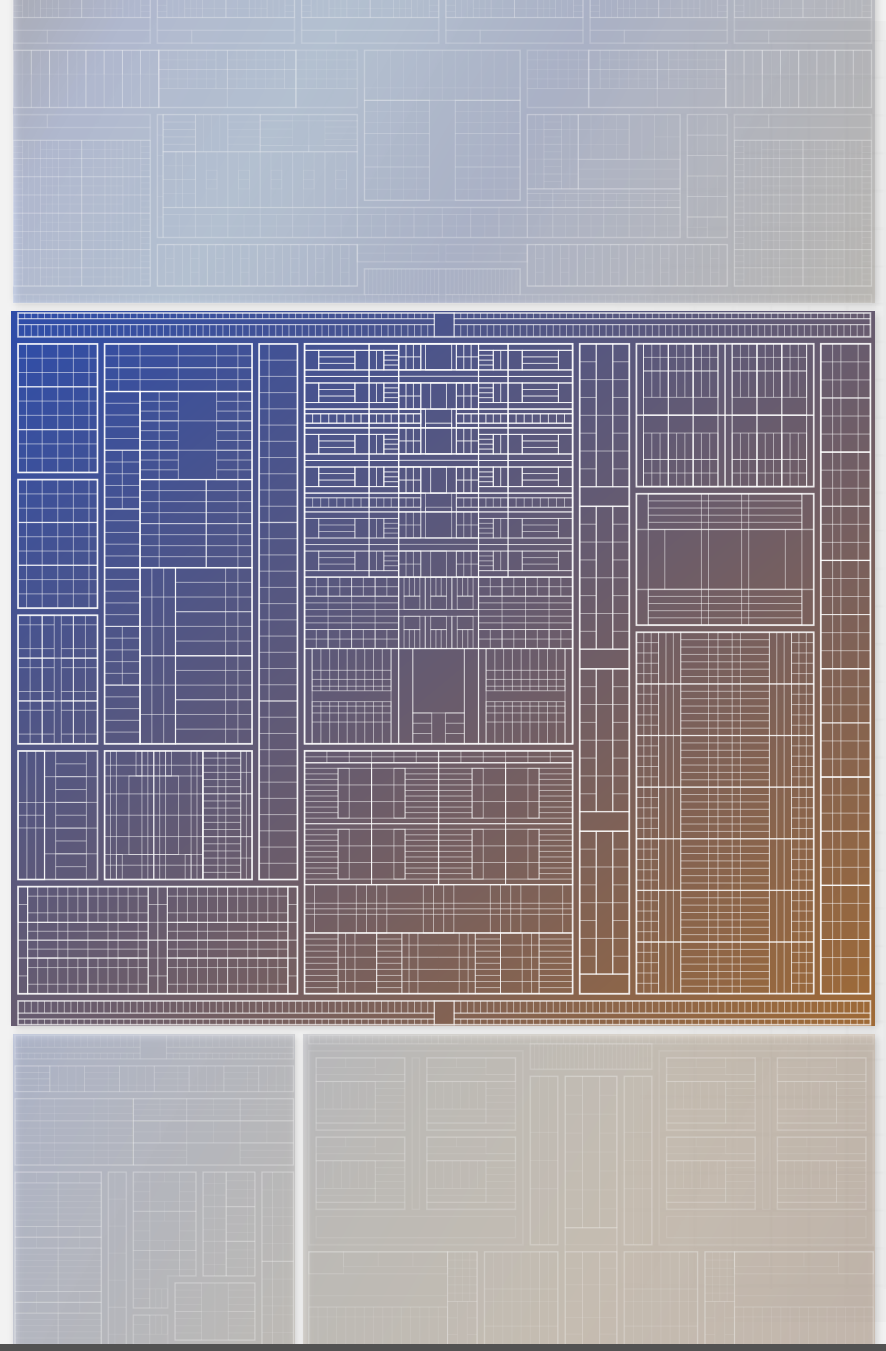
Power Efficiency Features

Integrated DLVRs for fine grained voltage control

Dynamic Fabric Frequency Bandwidth and QoS based

SoC algorithms shaped by Internal WL type inference

Scheduling Enhancements using Intel Thread Director



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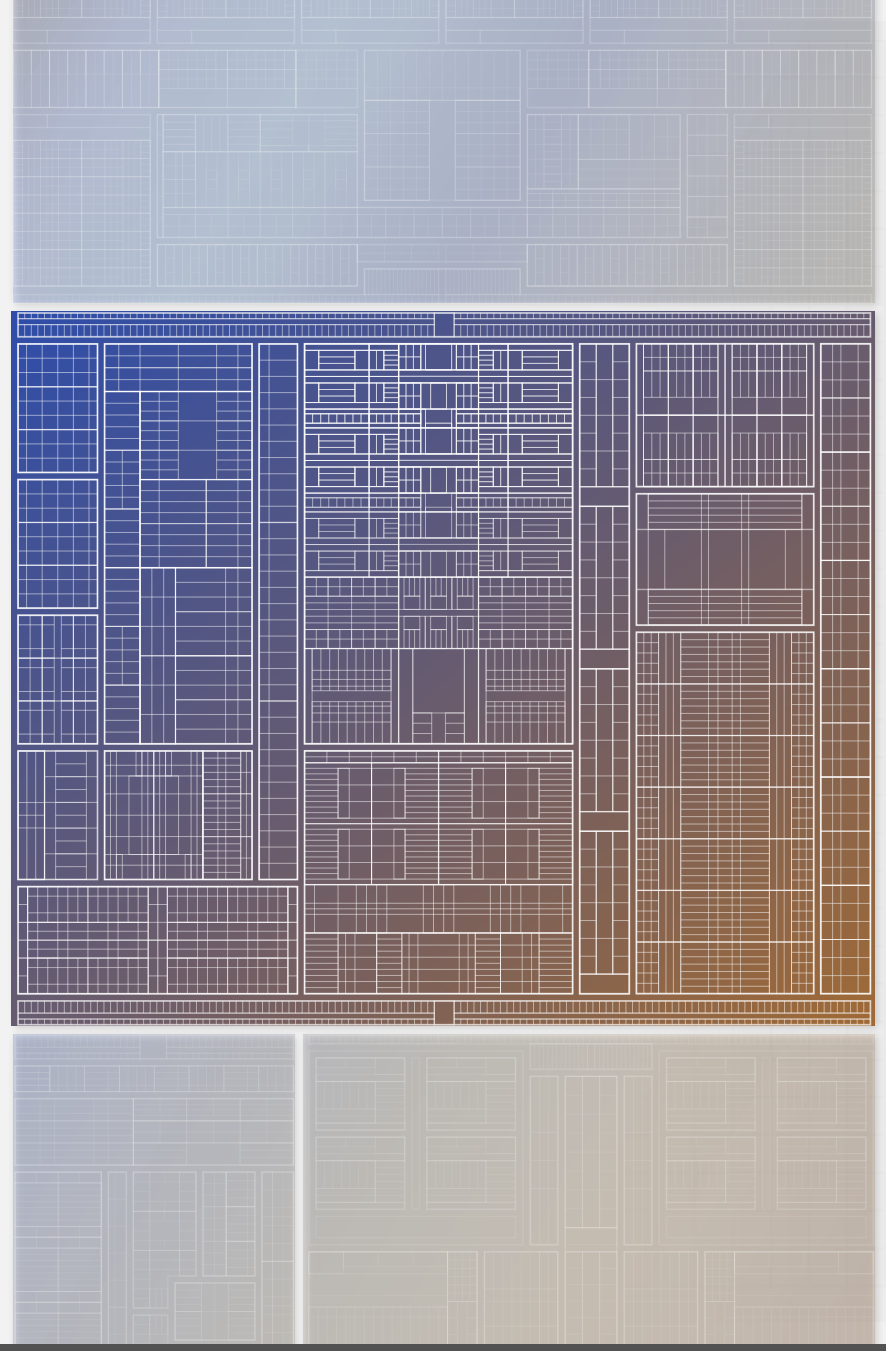

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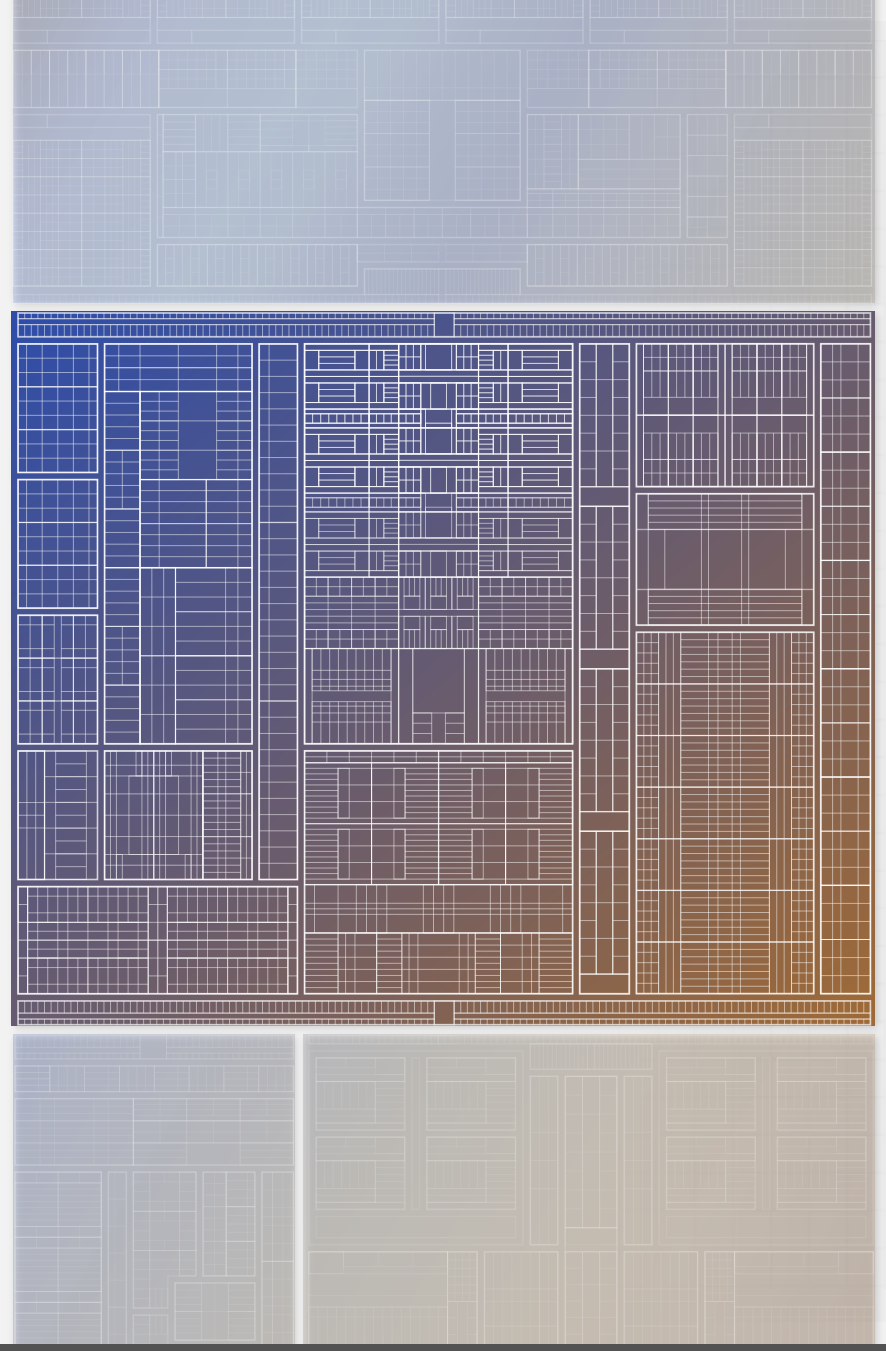

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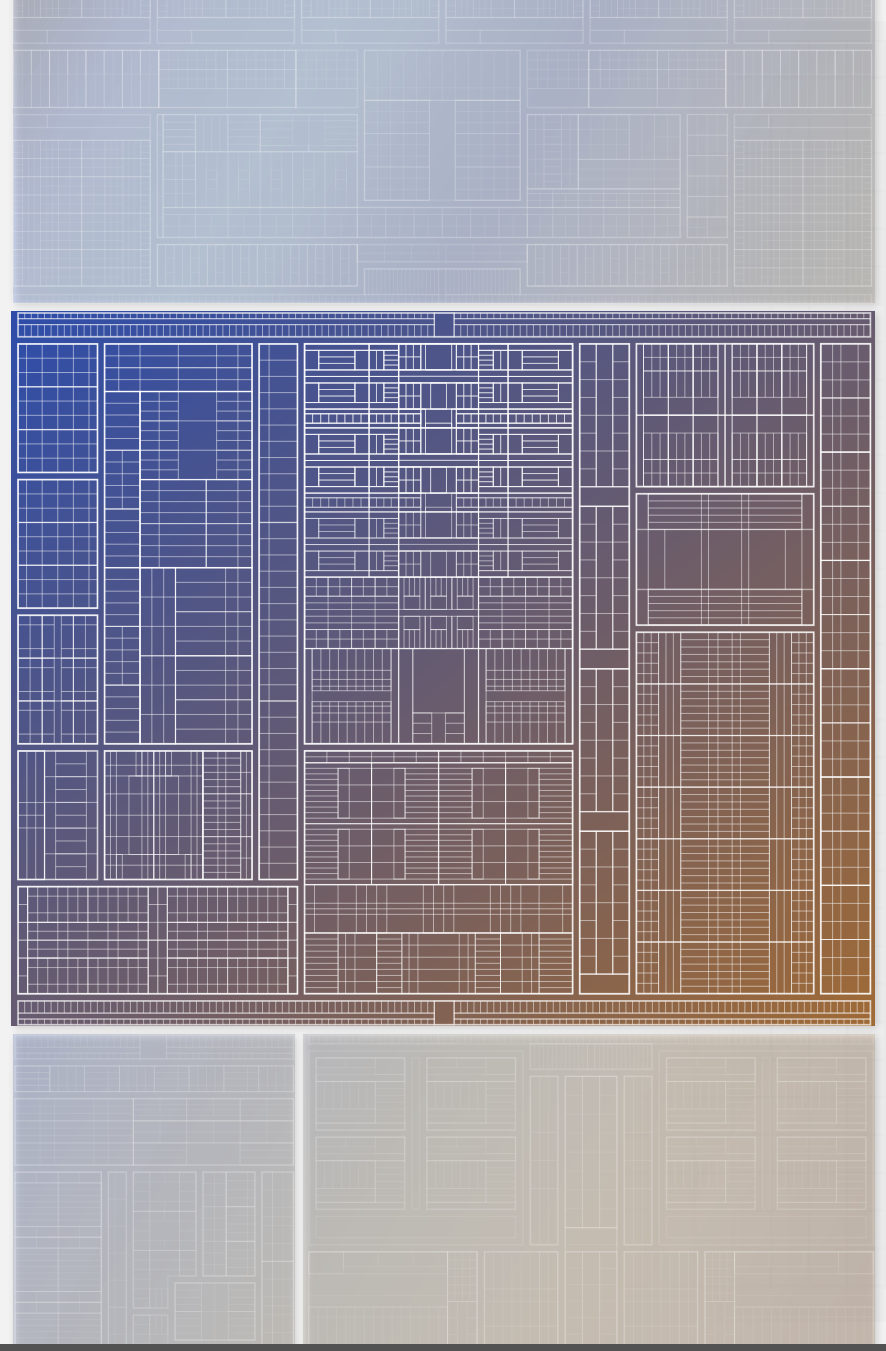

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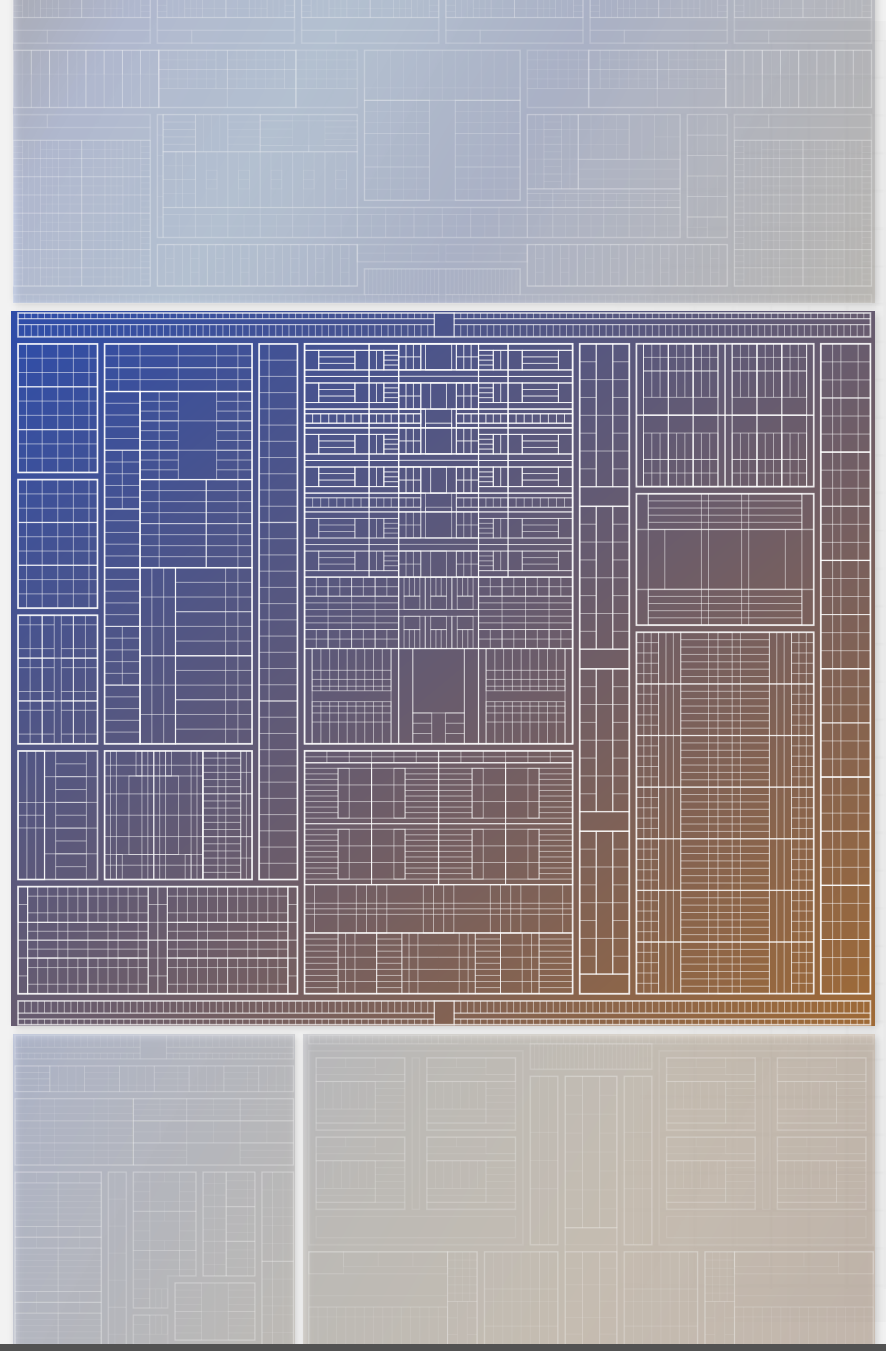

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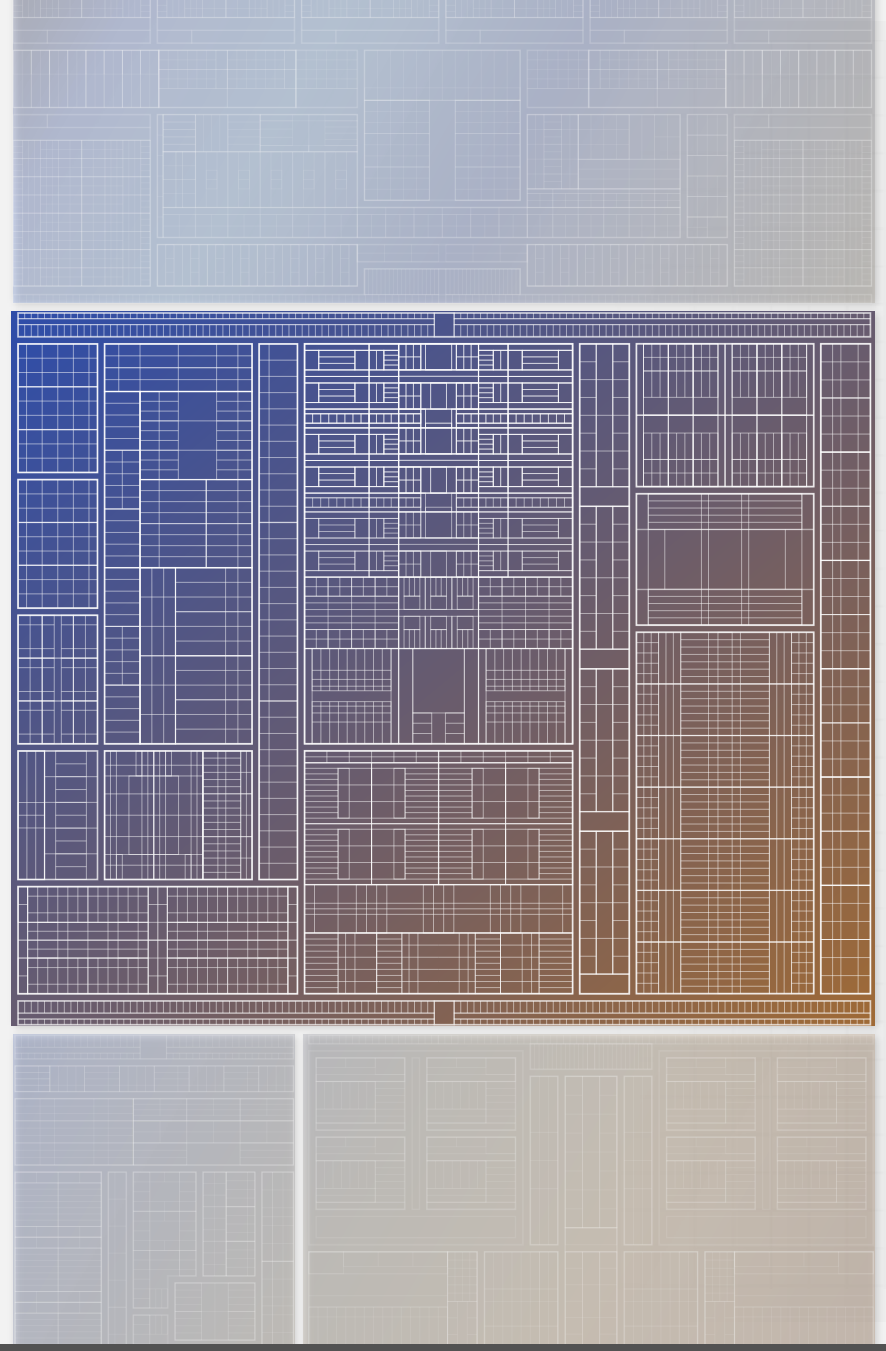

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- Primer on 3D Performance Hybrid Architecture
- Unpacking Intel Thread Director
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3D Performance Hybrid Architecture Vision

Optimize power efficiency while delivering best adaptive performance

Intel Thread Director
hardware that provides feedback to OS for optimal scheduling decisions

Symmetric ISA
exposed to OS as individual logical processors with capabilities enumerated

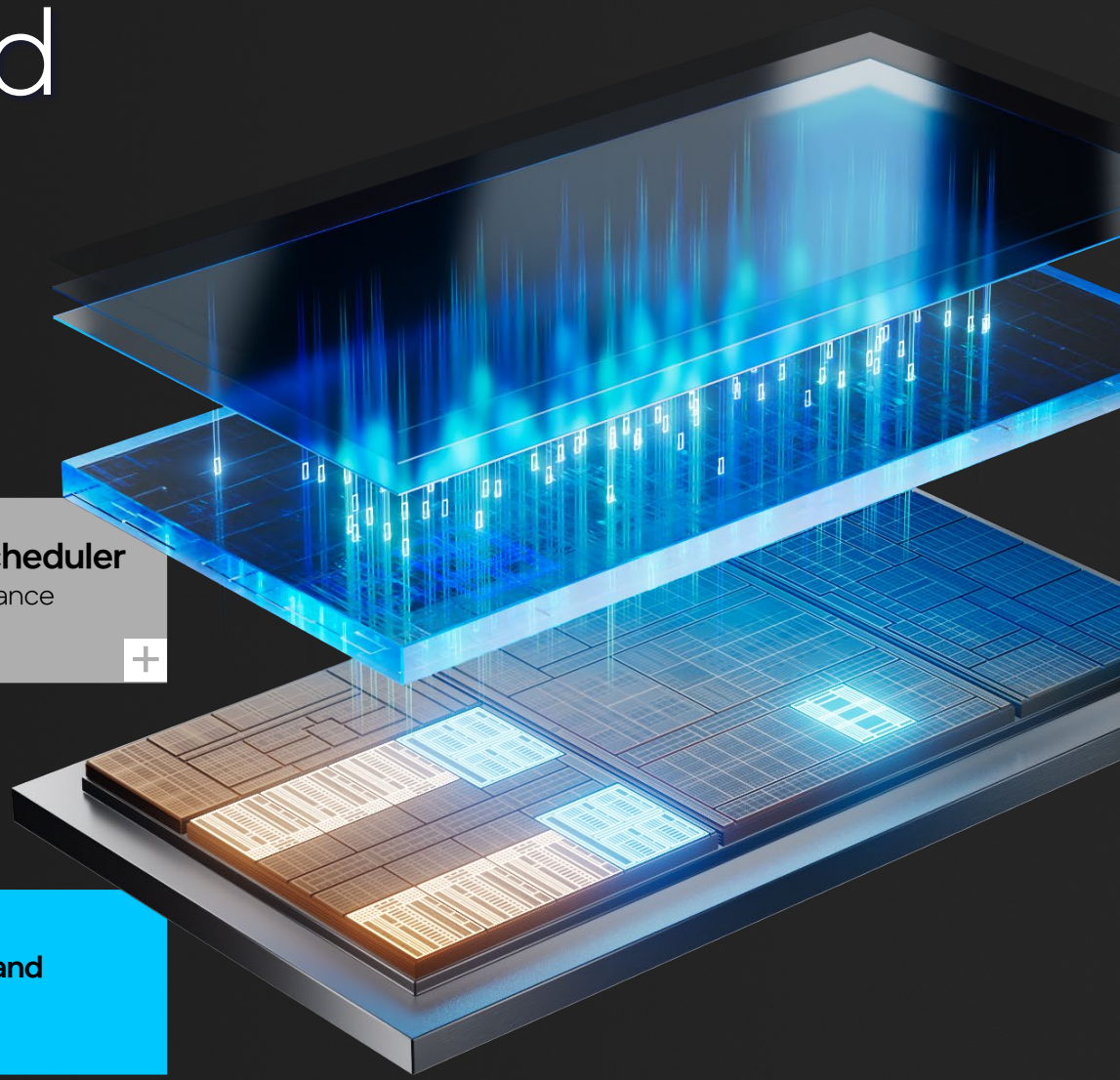
Optimized OS scheduler
unlocks great performance benefits

+

Compute tile P-cores
heavy lifting power for **single & limited threading perf**

Compute tile E-cores
provide **efficient MT throughput**

SoC tile E-cores
provide **low power and energy efficiency**



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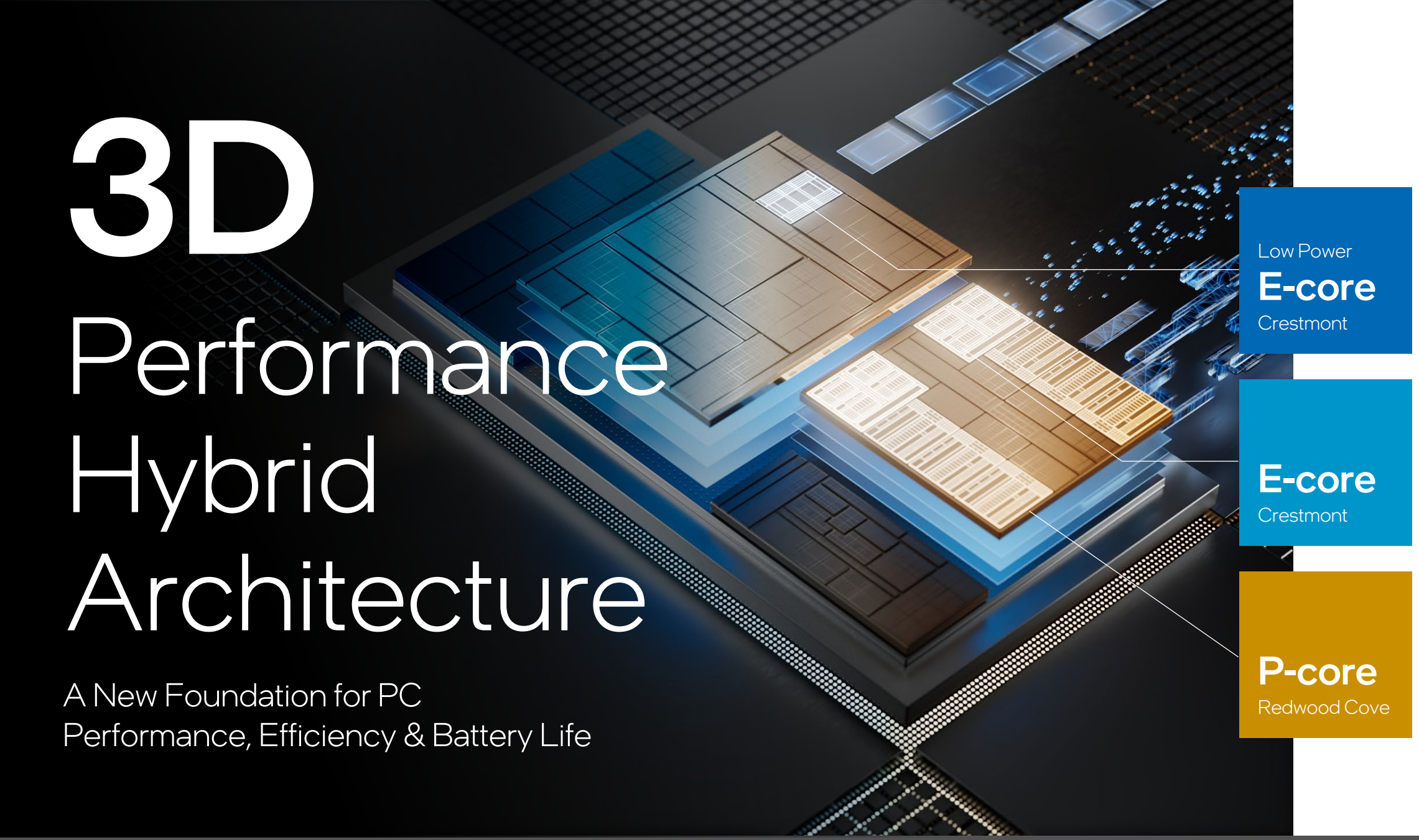
3D Performance Hybrid Architecture

A New Foundation for PC
Performance, Efficiency & Battery Life



REDWOOD COVE

New P-core

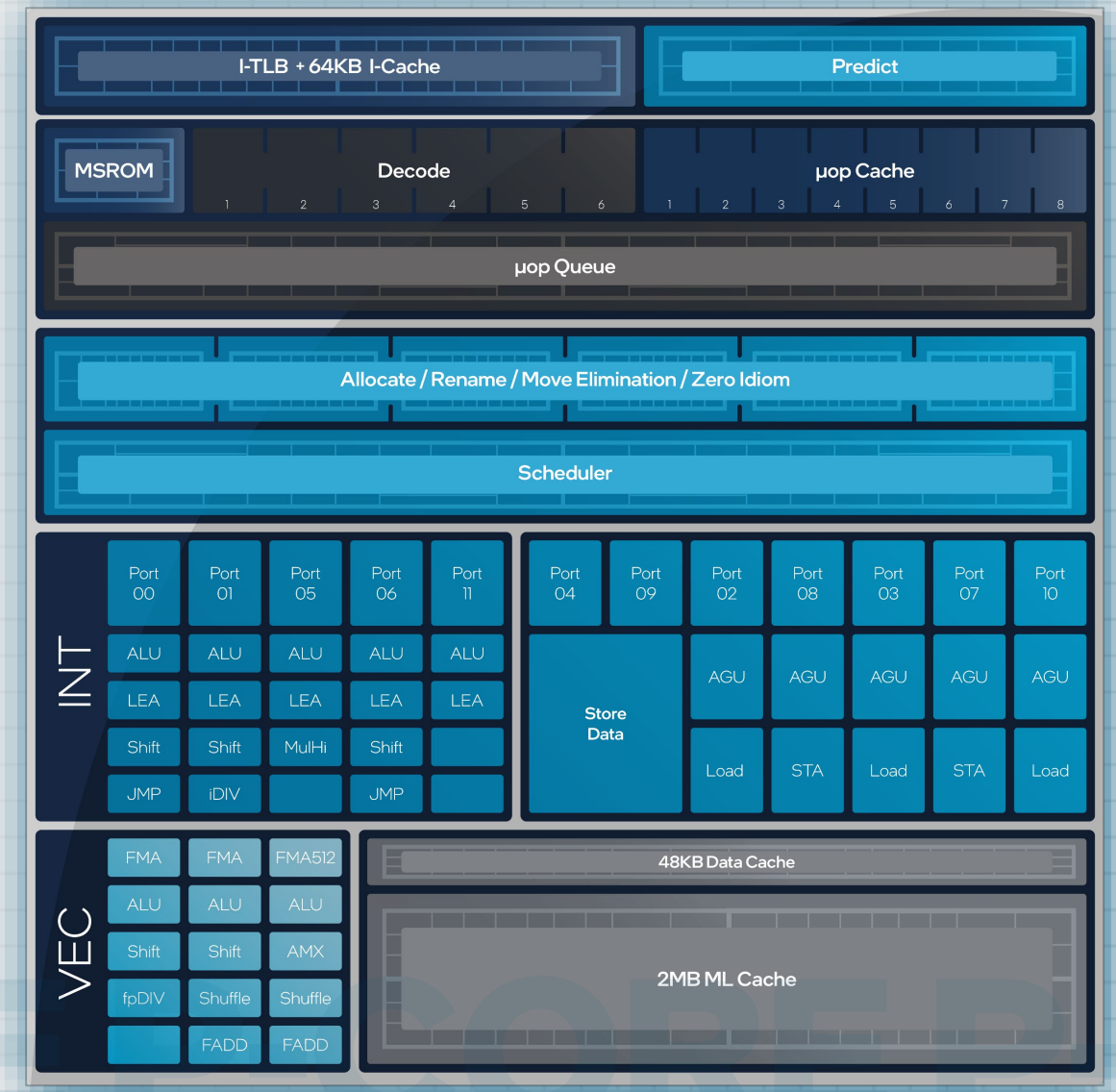
Targeted for efficient performance

Improved performance efficiency*

Increased BW per core package*

Improved Performance Monitoring Unit

Improved feedback Intel Thread Director



*Architectural simulation vs. Golden Cove architecture. Results may vary across workloads.

CRESTMONT

New E-core

Significant improvements over prior E-core

IPC gains over prior E-cores*

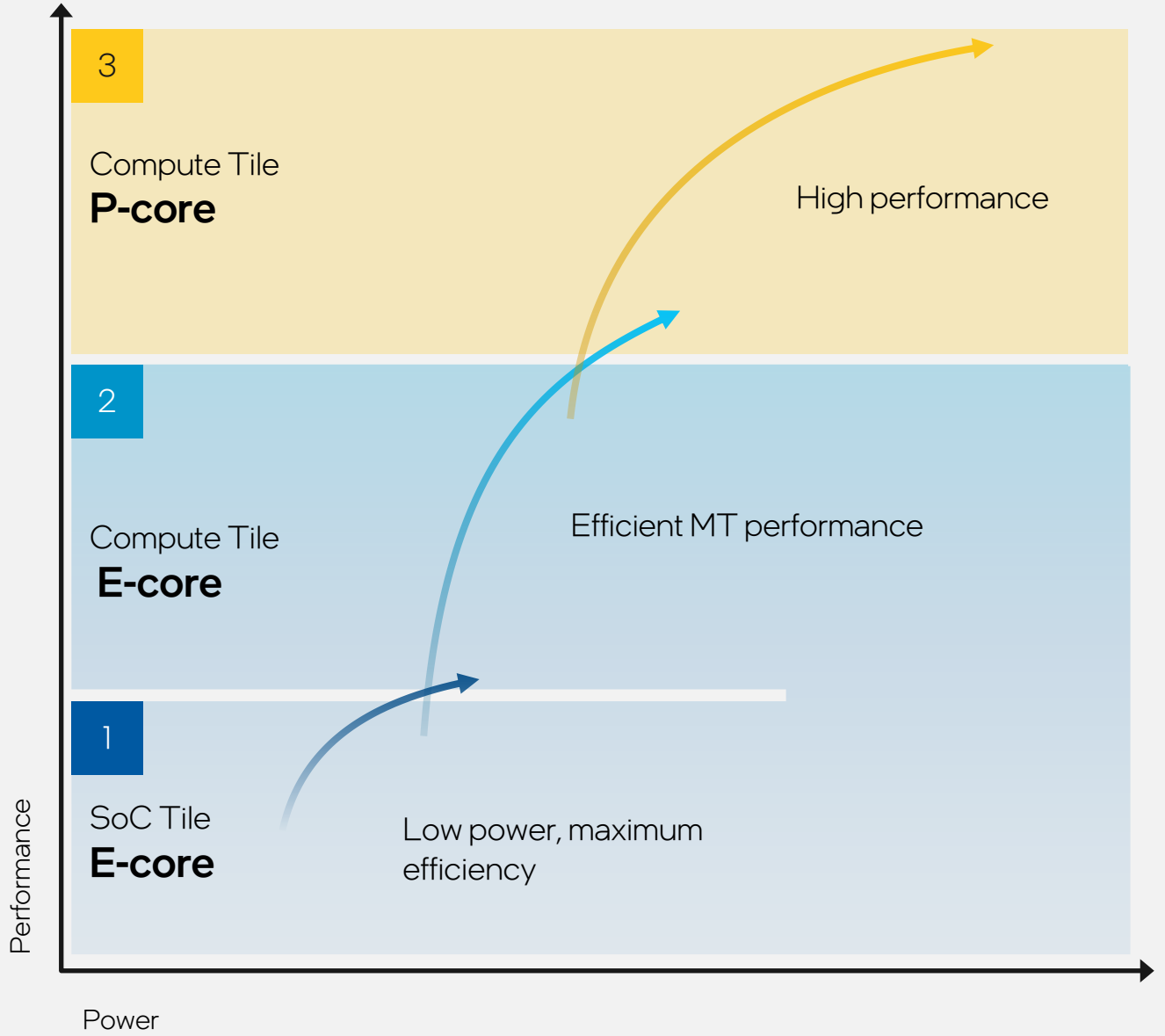
AI acceleration VNNI, ISA improvements*

Enhanced branch prediction

Enhanced Feedback Intel Thread Director

*Architectural simulation vs. Gracemont architecture across a broad set of workloads. VNNI improvements based on doubling the number of VNNI ports. Results may vary.

3D Performance Hybrid Architecture



*Conceptual representation of 3D Perf Hybrid Arch

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INTEL THREAD DIRECTOR

Architecture

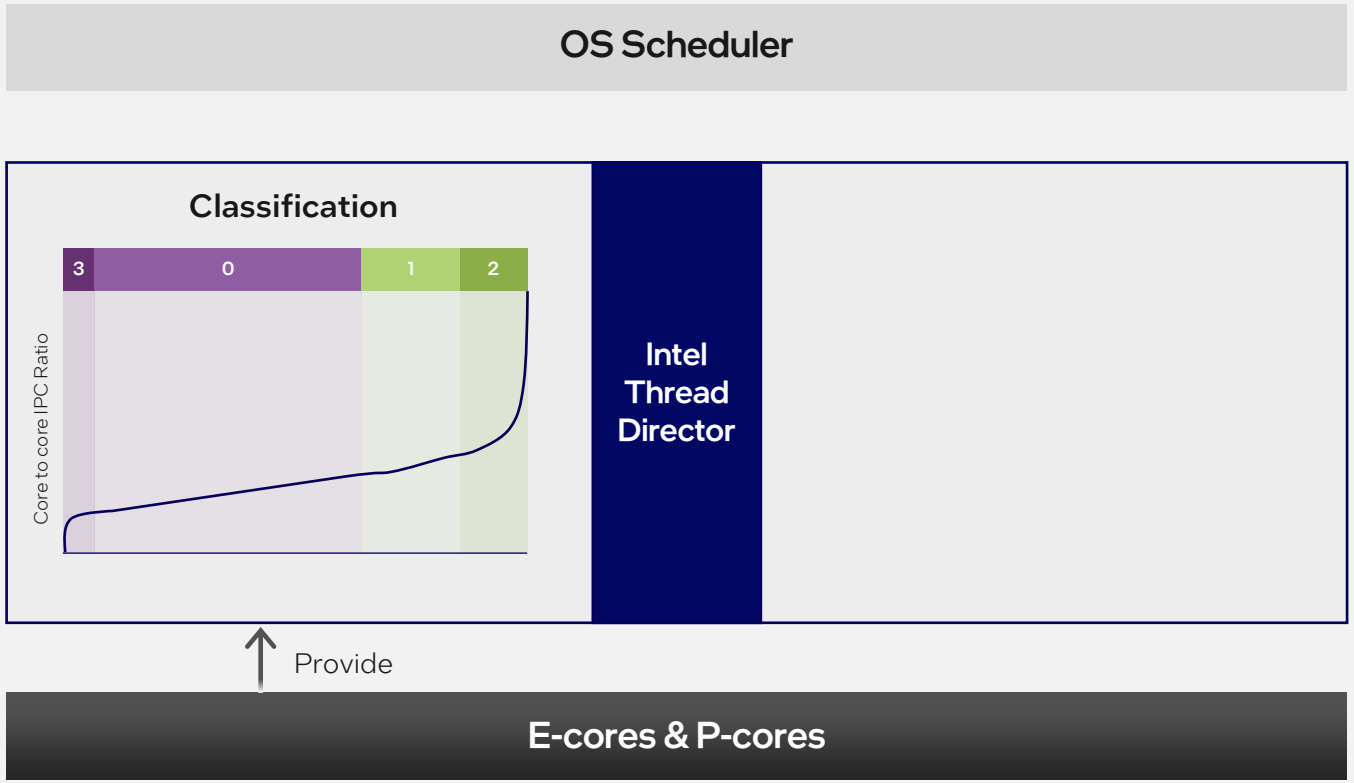
OS Scheduler

Intel Thread Director

E-cores & P-cores

INTEL THREAD DIRECTOR

Architecture



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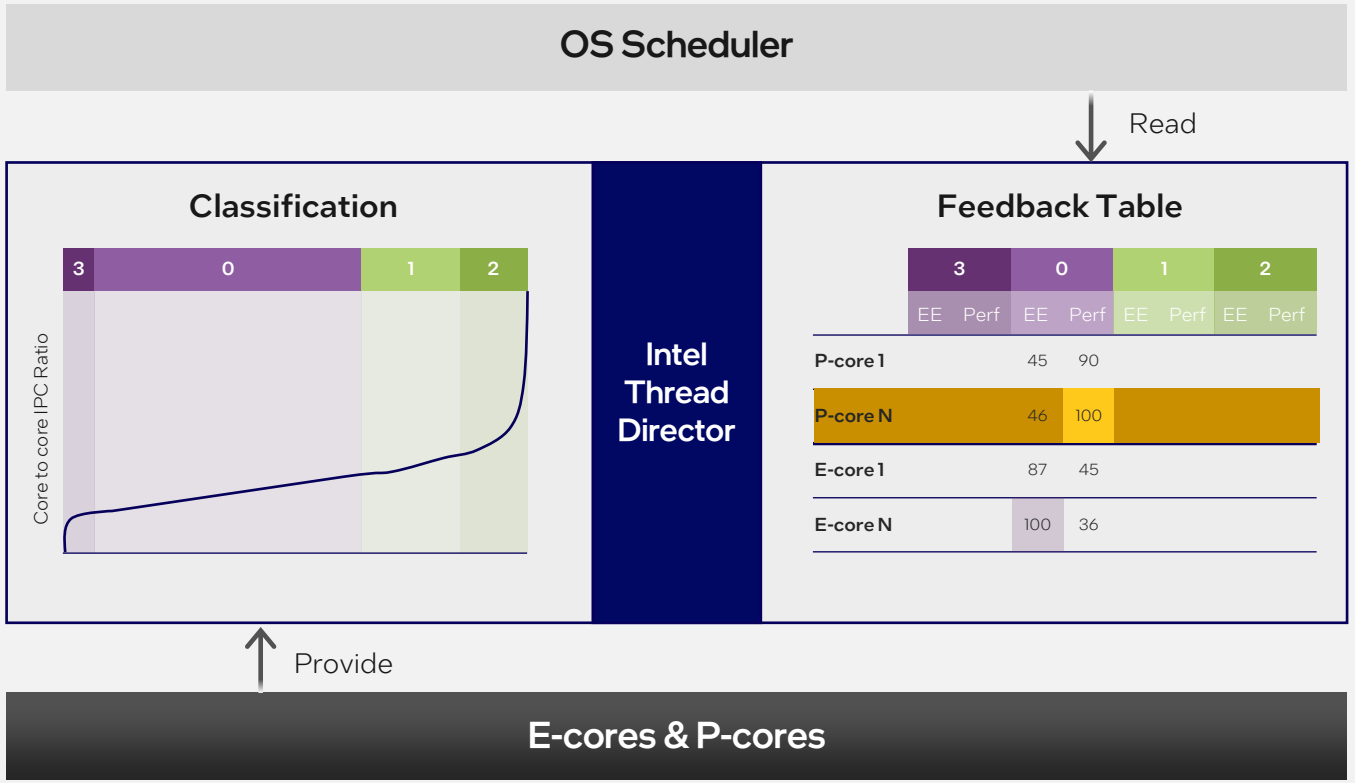

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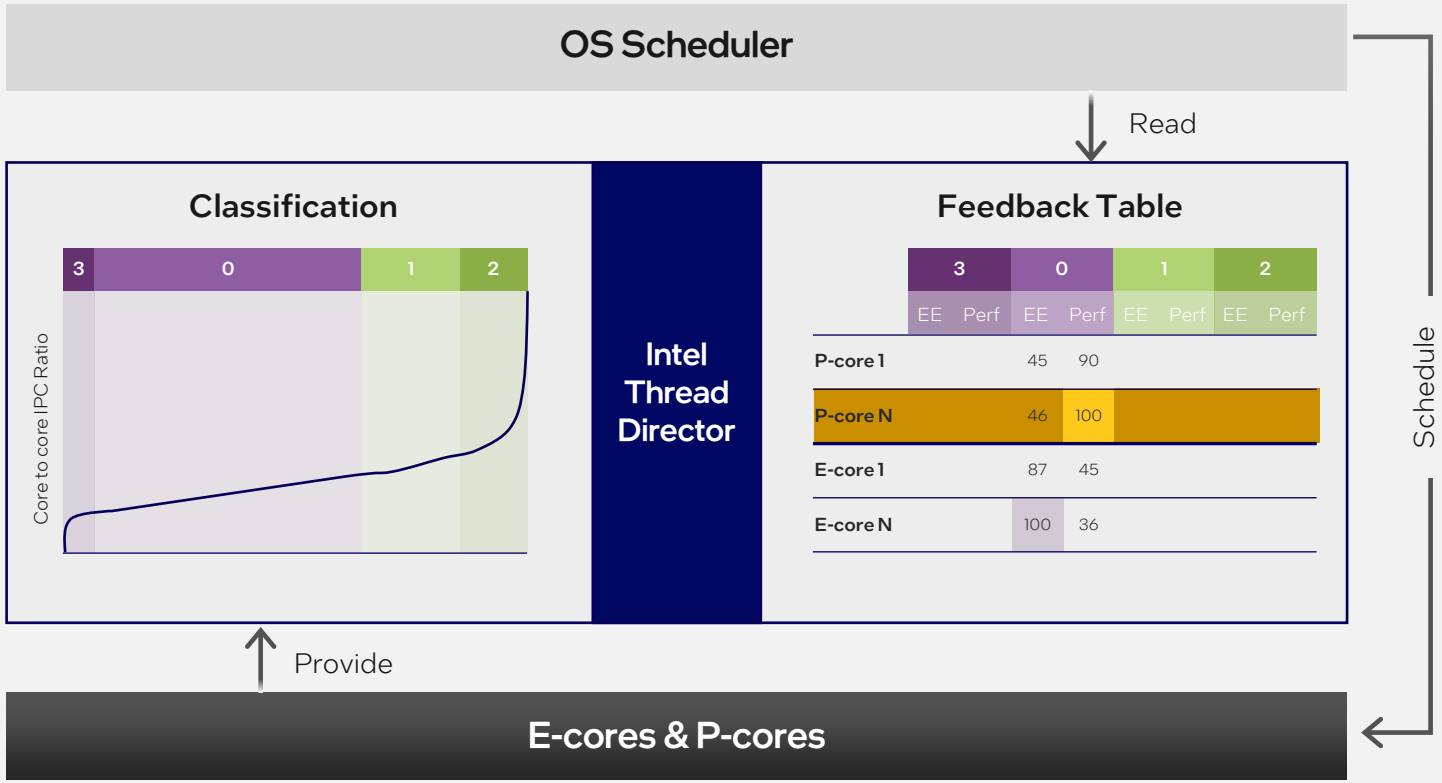

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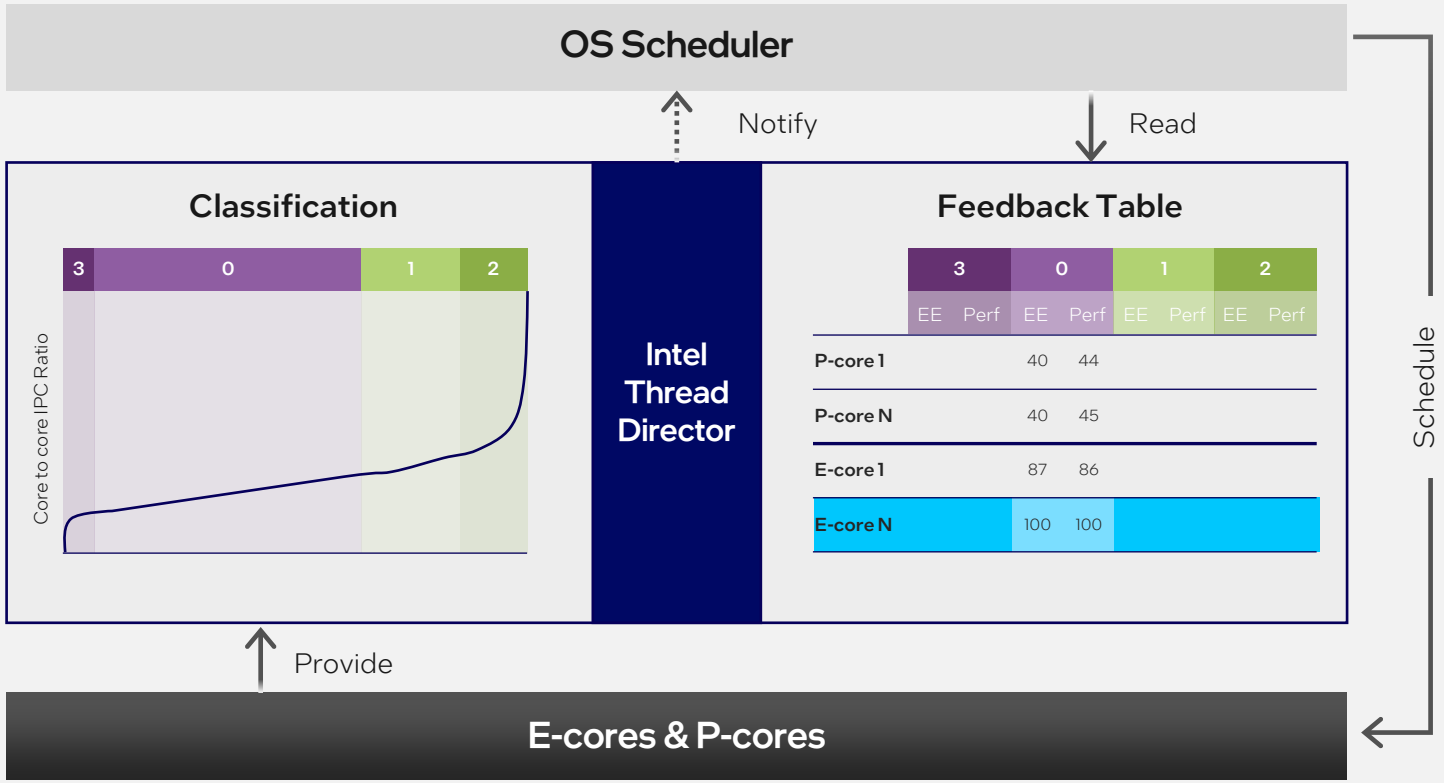


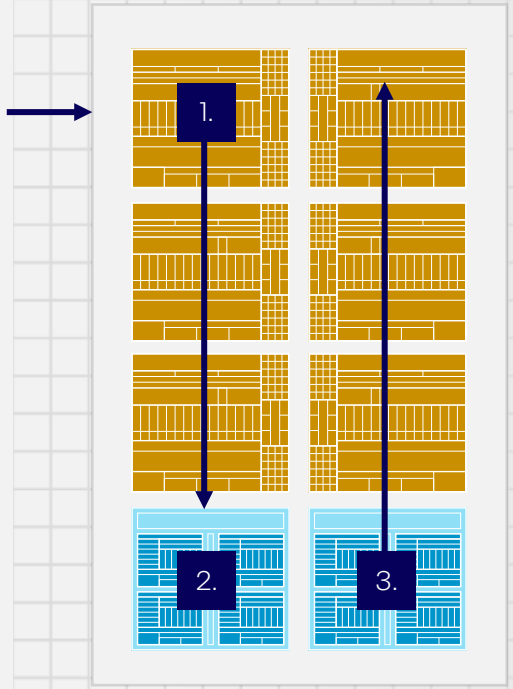
*Conceptual representation of Intel Thread Director technology

What's new in **Intel Thread Director**

- Enhanced feedback / smarter hints
- Dynamic updates when other IPs take power budget
- Updates based on run time capabilities of SoC
- Enhanced tie-in internal power efficiency decisions
- System software hint interface
- Guidance based on system operating mode/ HW characteristics

INTEL THREAD DIRECTOR

Scheduling Improvements



Raptor Lake

1.Higher QoS work moves to **P-cores**

2. Lower QoS work moves to **E-cores**

3. Periodically move **E-core** threads to **P-core** to reclassify and move if necessary

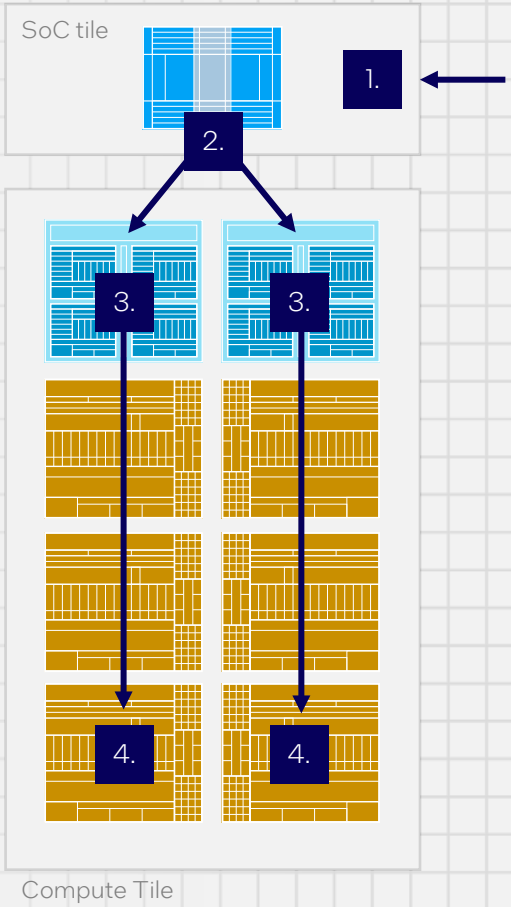
Meteor Lake

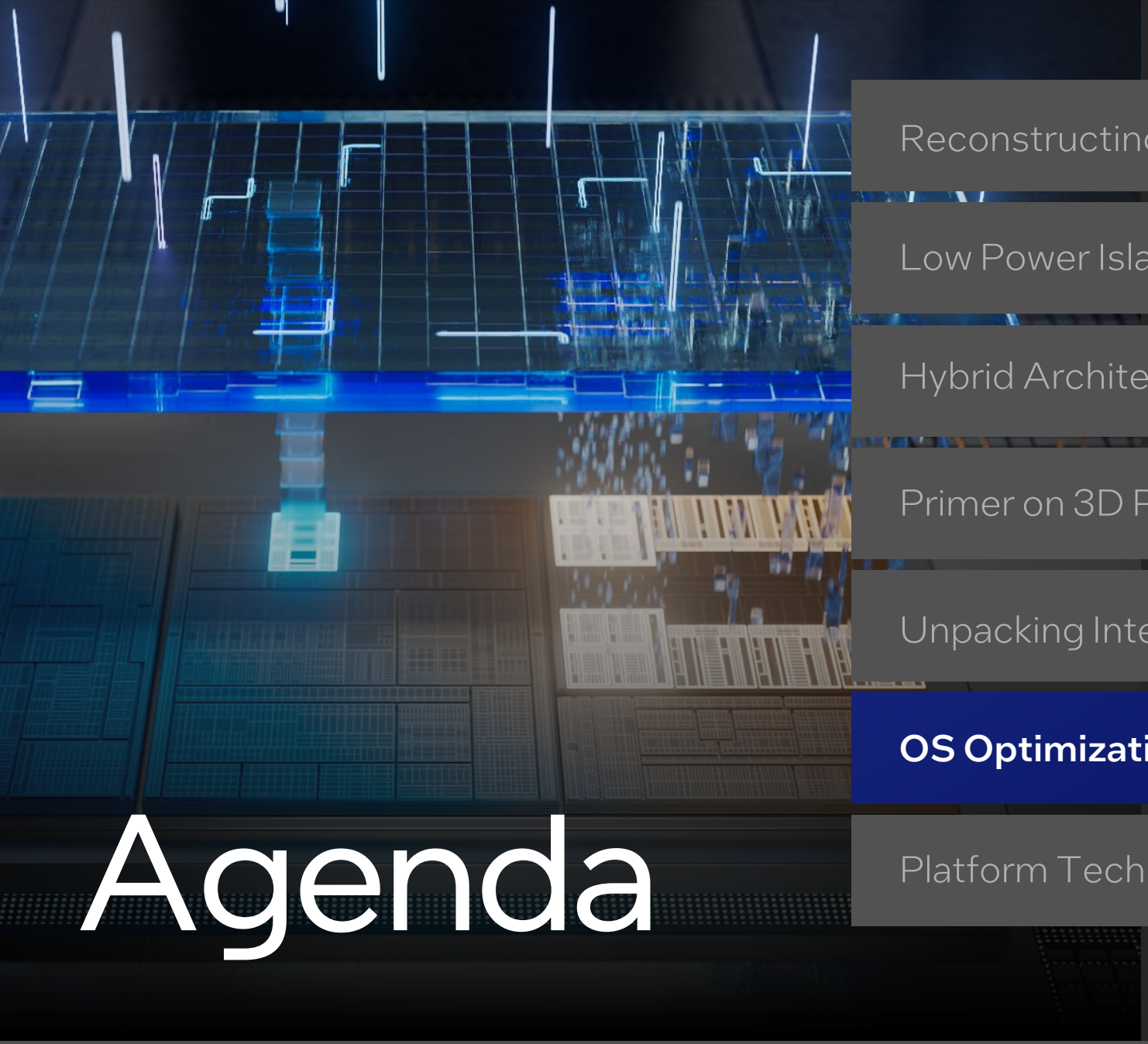
1. Try to contain on SoC **E-cores**

2. When work cannot be contained move to compute tile

3. Use compute tile **E-cores** if the work fits there

4. Higher demand work to **P-cores** that can benefit from those





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co-design with

Windows

Incorporation SoC tile

(low power domain) feedback from Intel Thread Director

Processor power management optimizations

for battery life in DC and perf in AC

Maximizing power and performance

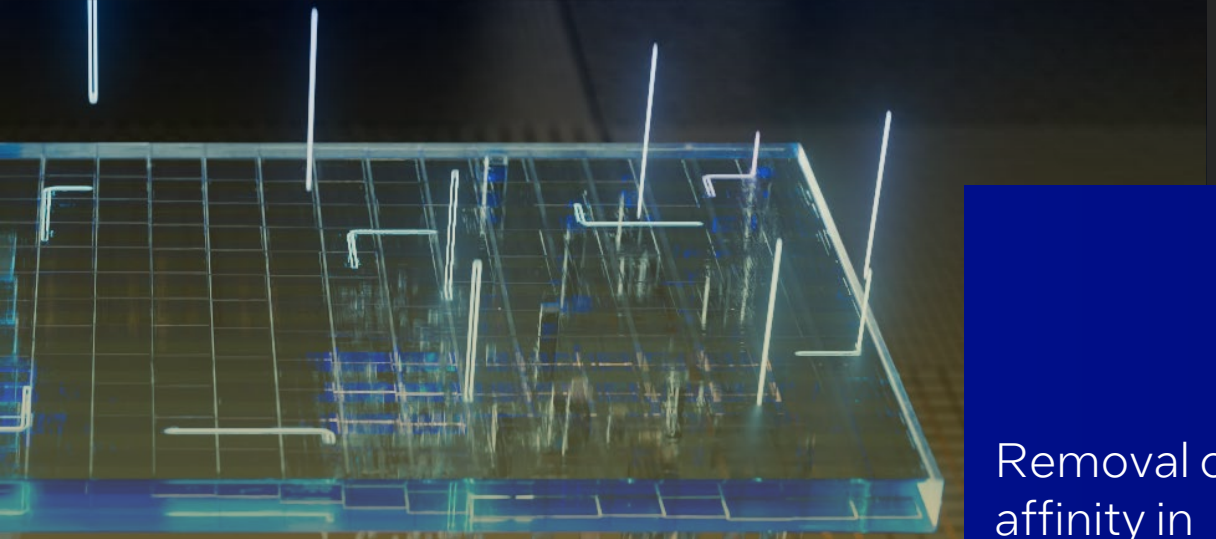
for SoC and compute tile activities

METEOR LAKE

Scheduling Example

Performance

- Low Utilization app (2 Threads on LP E-cores)
- New High Utilization app (4 Threads on P-cores)
- HW updates Intel Thread Director, TD notifies OS



Hybrid Architecture Software Enabling

- Removal of hard affinity in software
- Leverage power throttling (QoS) APIs
- Optimized spin-wait via updated threading libraries
- Integration of optimized SDKs & frameworks in ISV apps
- Detect hybrid architecture through MS API
- AVX-VNNI and new ISA feature

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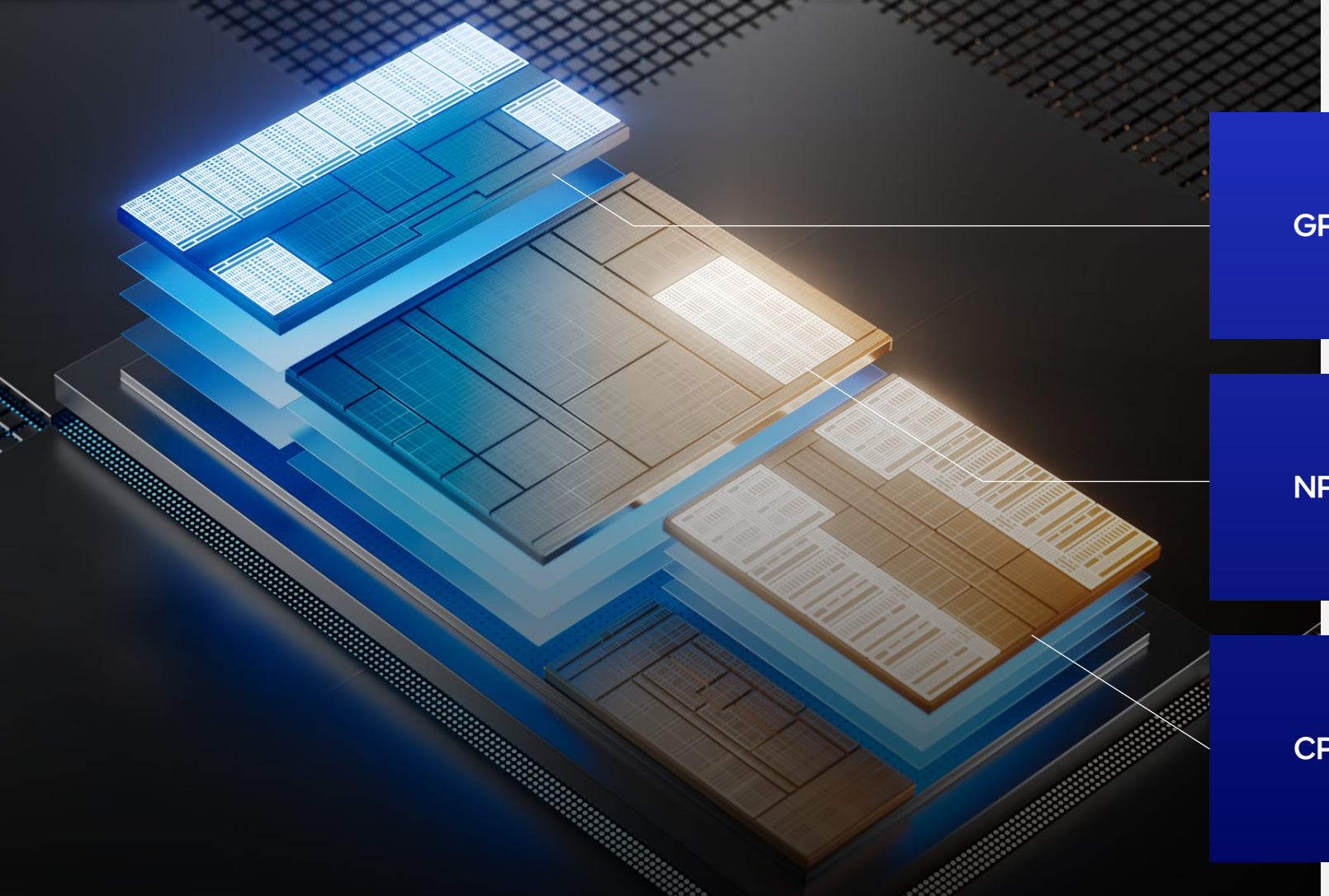


Power Efficient AI

Intel technologies may require enabled hardware, software or service activation.

GPU

Performance Parallelism & Throughput

Ideal for AI infused in Media/3D/render pipeline

NPU

Dedicated Low Power AI Engine

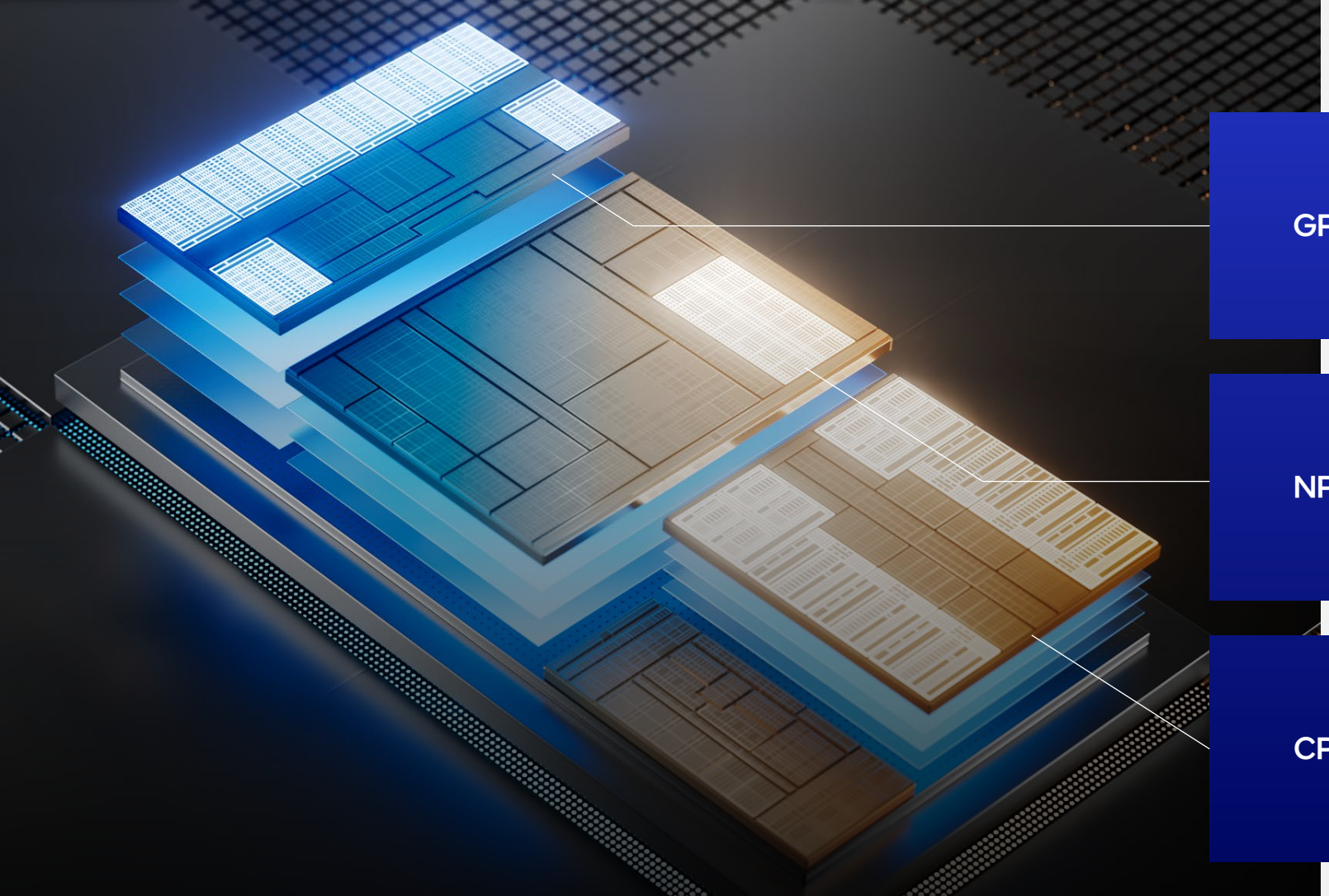
Designed for performance and power efficiency

Ideal for sustained AI and AI offload

CPU

Fast Response

Ideal for light-weight, single inference low-latency AI tasks



Power Efficient AI

Intel technologies may require enabled hardware, software or service activation.

GPU

Performance Parallelism & Throughput

Ideal for AI infused in Media/3D/render pipeline

NPU

Dedicated Low Power AI Engine

Designed for performance and power efficiency

Ideal for sustained AI and AI offload

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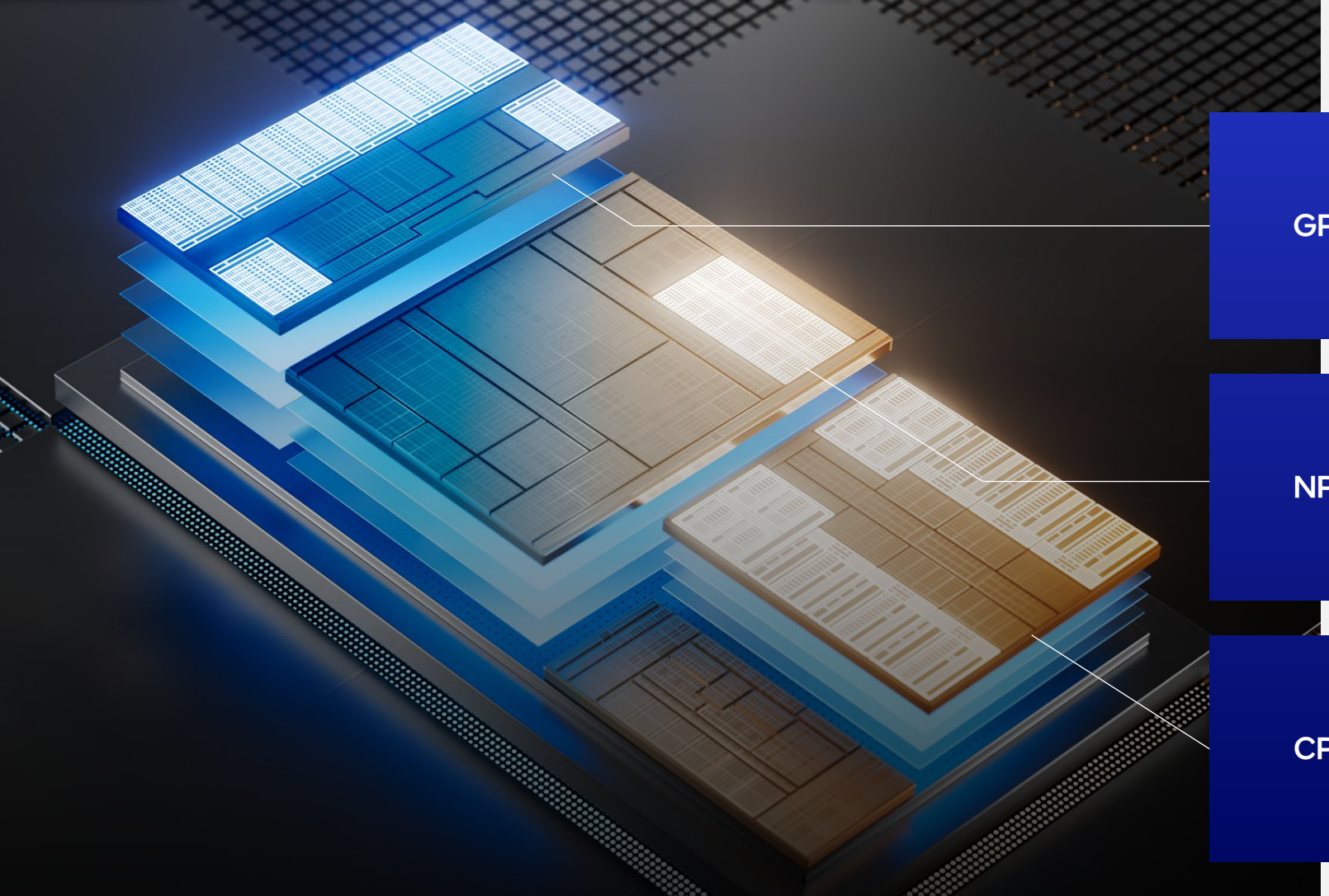

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INTEL

Intelligent Display

Combining ecosystem **display panel innovation** with Intel software to enable

- battery life boost
- enhanced visual experience
- sustainability benefits

Autonomous Low Refresh Rate

Display panel dynamically changes refresh rate based on rendered content

User Based Refresh Rate

Display panel adjusts backlight and refresh rate based on user status and engagement

Dynamic Visual Enhancements

Display panel dynamically adjusts contrast and brightness based on content

*Some Intel Intelligent Display features may require additional panel enhancements.

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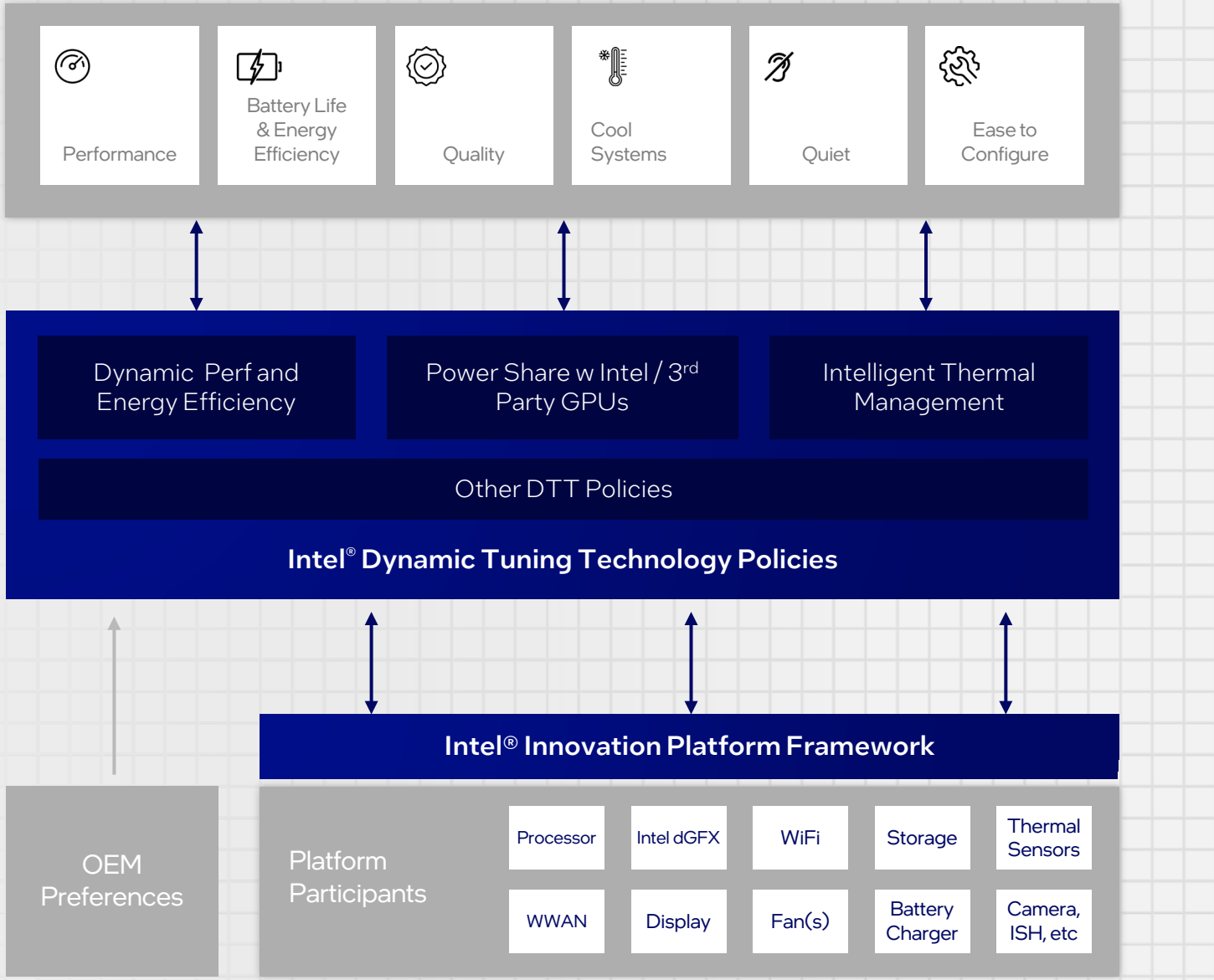
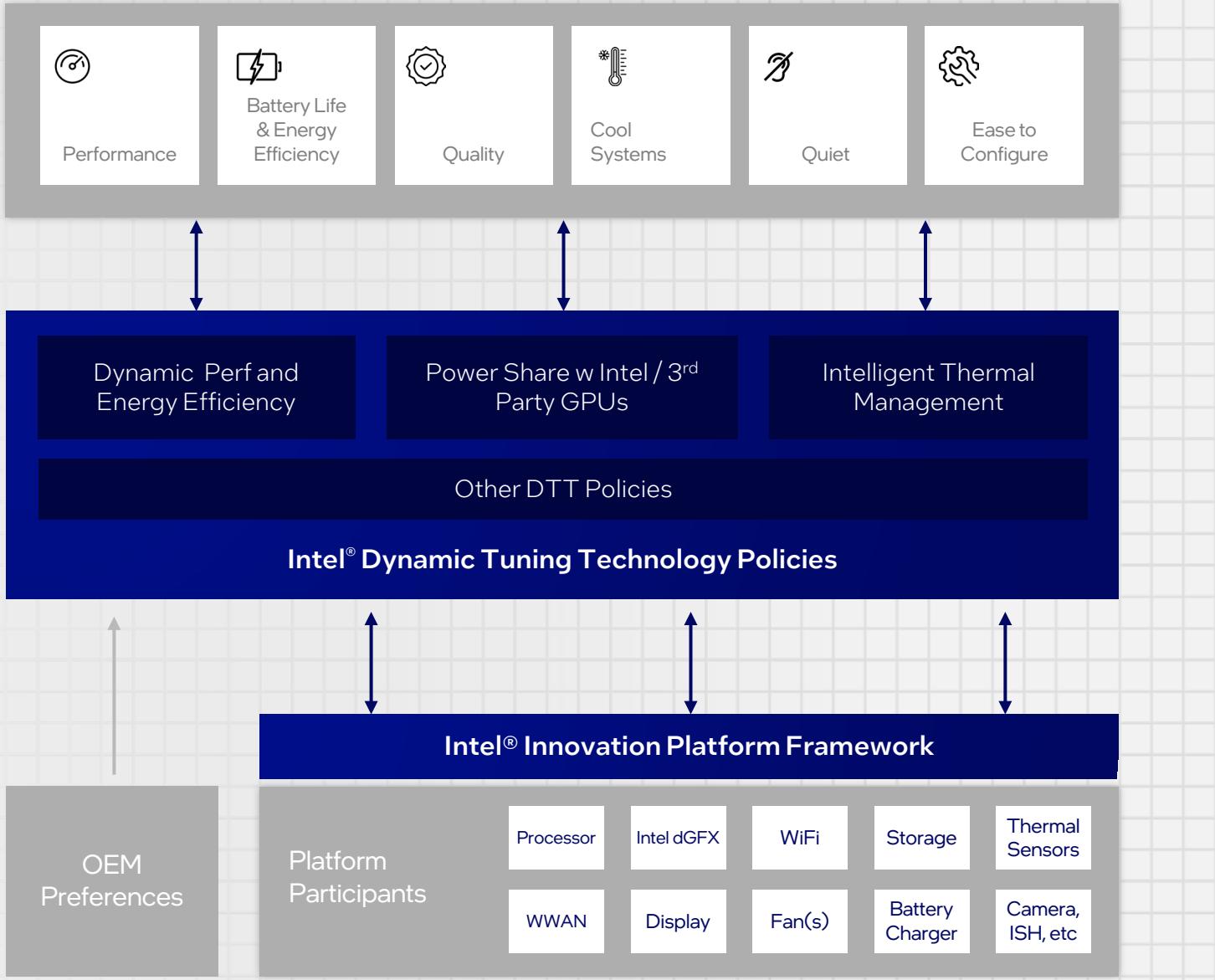
Intel® Dynamic Tuning Technology Software



Intel® Dynamic Tuning Technology Software



Advancing Moore's Law
5 NODES IN 4 YEARS

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Intel Thread Director

Right thread on the right core at the right time

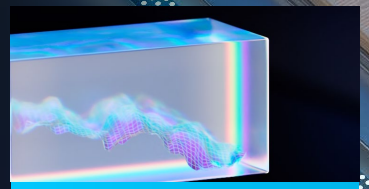
Runtime Instruction Mix Monitoring
nanosecond precision

Runtime Feedback to OS
for optimal scheduling

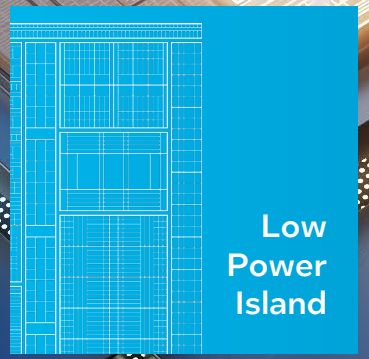
Dynamic intelligent guidance
without user input

Power Efficiency

Our most power-efficient client SoC ever



Reconstructing Power Efficiency



Low Power Island

Rest of SoC and Platform Technologies

3D Performance Hybrid

Right cores for the right work

NEW
P-cores
For high-Performance

NEW
E-cores
Efficient MT performance

SoC TILE
E-cores
Low power, maximum efficiency

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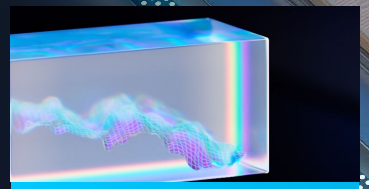

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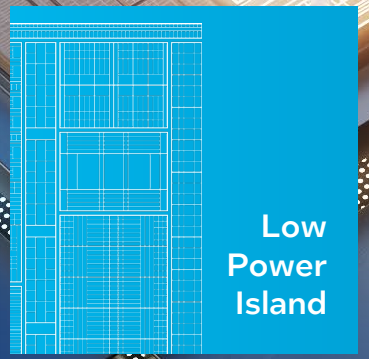

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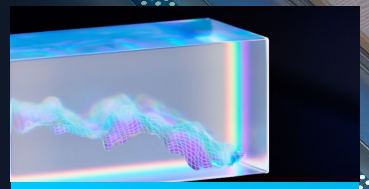

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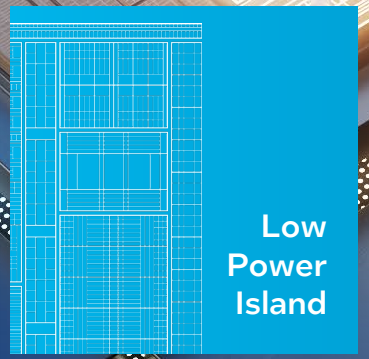

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