NOTES:

1. PROJECT DRAWING NUMBERS:

RAW PCB	100-0330712-A2
GERBER FILES	110-0330712-A2
PCB DESIGN FILES	120-0330712-A2
ASSEMBLY DRAWING	130-0330712-A2
FAB DRAWING	140-0330712-A2
SCHEMATIC DRAWING	150-0330712-A2
PCB FILM	160-0330712-A2
BILL OF MATERIALS	170-0330712-A2
SCHEMATIC DESIGN FILES	180-0330712-A2
FUNCTIONAL SPECIFICATION	210-0330712-A2
PCB LAYOUT GUIDELINES	220-0330712-A2
ASSEMBLY REWORK	320-0330712-A2

INTEL AGILEX® 7 FPGA I-SERIES TRANSCEIVER DEVELOPMENT KIT(6x F-TILE)

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LEVEL	MMID	99C2HX
0	TA	M83887-001
1	ASSY	M77740-100
2	PB	M83888-001

TITLE PAGE

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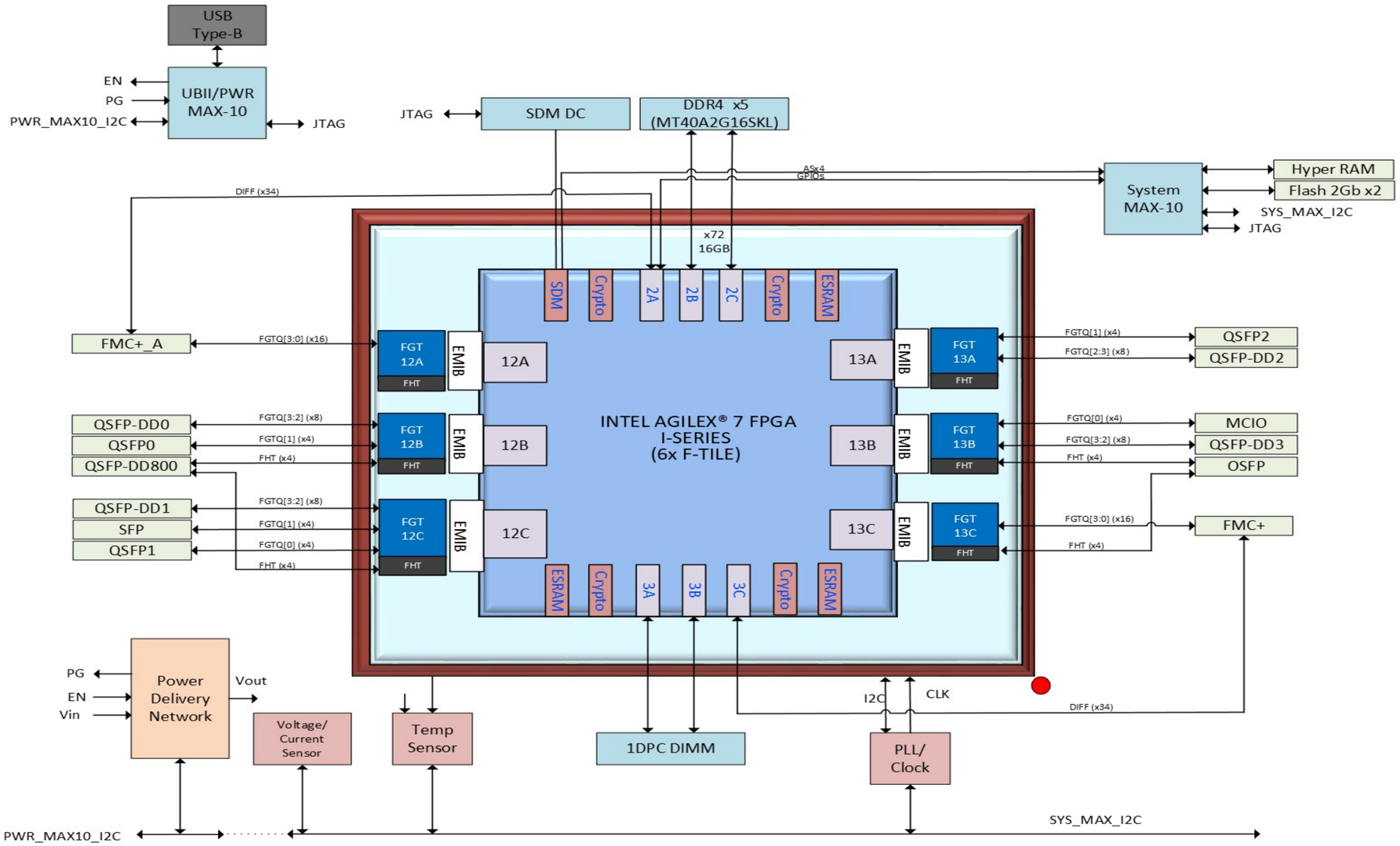
DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	1 OF 105

BLOCK DIAGRAM

INTEL AGILEX® 7 FPGA I-SERIES TRANSCEIVER DEVELOPMENT KIT(6x F-TILE)



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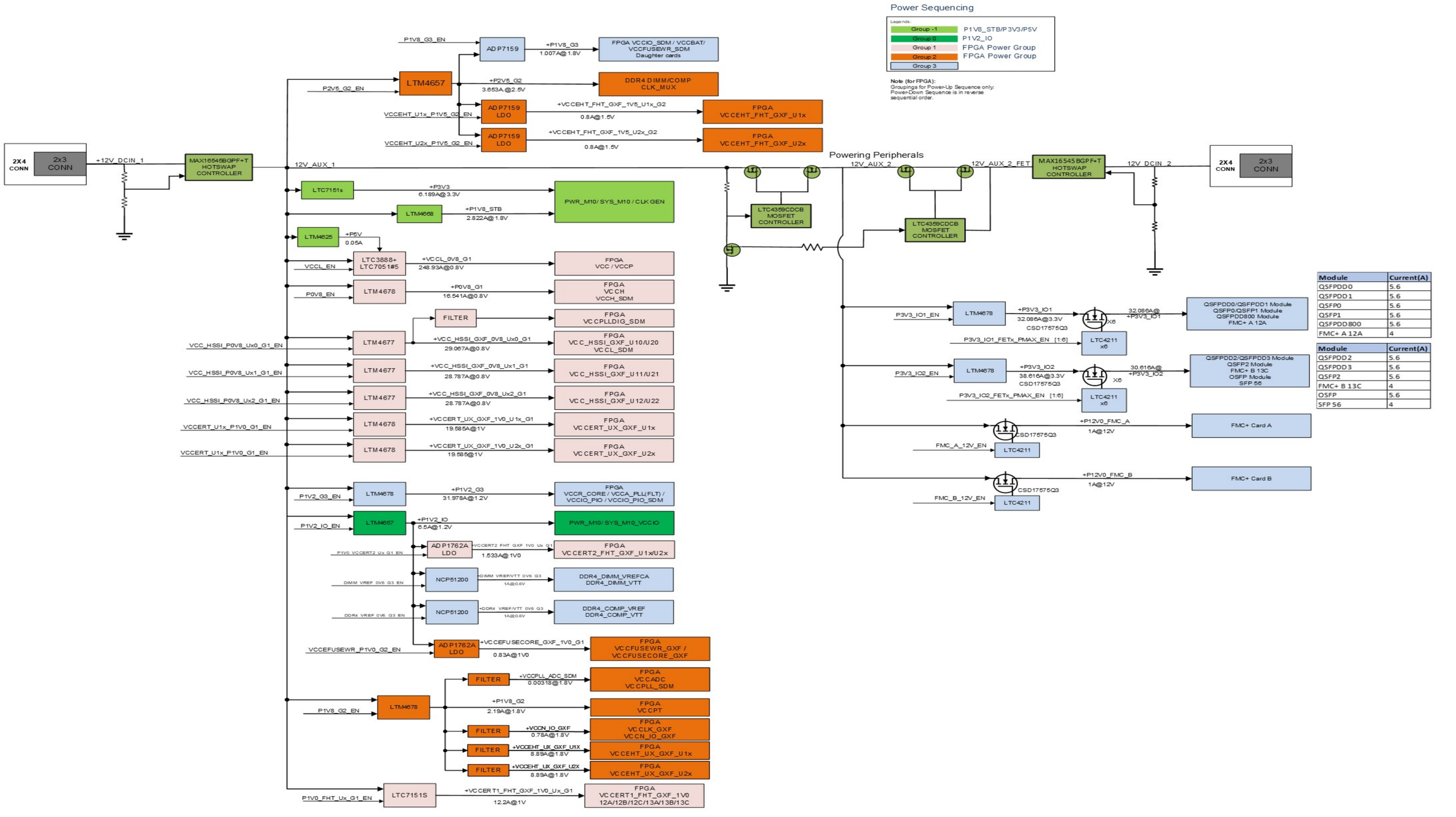
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	2 OF 105

POWER TREE



Module	Current(A)
QSFPDD0	5.6
QSFPDD1	5.6
QSFP0	5.6
QSFP1	5.6
QSFPDD800	5.6
FMC+ A 12A	4

Module	Current(A)
QSFPDD2	5.6
QSFPDD3	5.6
QSFP2	5.6
FMC+ B 13C	4
OSFP	5.6
SFP 56	4

Tue Aug 8 11:15:53 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	3 OF 105

POWER TREE

POWER ESTIMATION

Rail Name	Voltage (V)	Source	Efficiency	Consumption (A)	Power (W)	Voltage Regulator	Current Supported (A)	Group	RefDes
+P3V3	3.3	+12V0_AUX_1	90%	6.189	20.424	LTC7151SEV#PBF	15	Group - (-1)	U95
+P1V8_STB	1.8	+12V0_AUX_1	85%	2.822	5.079	LTM4668AIY#PBF	4.8	Group - (-1)	U79
+P5V	5	+12V0_AUX_1	85%	0.800	4.000	LTM4625EY#PBF	5	Group - (-1)	U102
+P1V2_IO	1.2	+12V0_AUX_1	85%	6.526	7.831	LTM4657EY#PBF	8	Group - 0	U47
+VCCL_0V8_G1	0.8	+12V0_AUX_1	87%	248.930	199.144	LTC3888+LTC7051(5)	300	Group - 1	U31,U32,U33,U34,U35,U181
+VCC_HSSI_GXF_0V8_Ux0_G1	0.8	+12V0_AUX_1	87%	29.067	23.254	LTM4677EY#PBF (Single)	36	Group - 1	U12
+VCC_HSSI_GXF_0V8_Ux1_G1	0.8	+12V0_AUX_1	87%	28.787	23.029	LTM4677EY#PBF (Single)	36	Group - 1	U6
+VCC_HSSI_GXF_0V8_Ux2_G1	0.8	+12V0_AUX_1	87%	28.787	23.029	LTM4677EY#PBF (Single)	36	Group - 1	U44
+VCCERT_UX_GXF_1V0_U1x_G1	1	+12V0_AUX_1	85%	19.585	19.585	LTM4678EY#PBF (Dual)	25	Group - 1	U20
+VCCERT_UX_GXF_1V0_U2x_G1	1	+12V0_AUX_1	85%	19.585	19.585	LTM4678EY#PBF (Dual)	25	Group - 1	U20
+P0V8_G1	0.8	+12V0_AUX_1	87%	16.541	13.233	LTM4678EY#PBF (Dual)	25	Group - 1	U43
+VCCERT1_FHT_GXF_1V0_Ux_G1	1	+12V0_AUX_1	88%	12.200	12.200	LTC7151SEV#PBF	15	Group - 1	EU17
+VCCERT2_FHT_GXF_1V0_Ux_G1	1	+P1V2_IO	83%	1.536	1.536	ADP1762ACPZ-R7	2	Group - 1	U94
+P1V8_G2	1.8	+12V0_AUX_1	90%	20.753	37.356	LTM4678EY#PBF (Dual)	25	Group - 2	U43
+P2V5_G2	2.5	+12V0_AUX_1	85%	3.213	8.032	LTM4657EY#PBF	8	Group - 2	U21
+VCCEHT_FHT_GXF_1V5_U1x_G2	1.5	+P2V5_G2	60%	0.800	1.200	ADP7159ACPZ-01-R7	2	Group - 2	EU8
+VCCEHT_FHT_GXF_1V5_U2x_G2	1.5	+P2V5_G2	60%	0.800	1.200	ADP7159ACPZ-01-R7	2	Group - 2	EU1
+VCCEFUSECORE_GXF_1V0_G2	1	+P1V2_IO	50%	0.830	0.830	ADP1762ACPZ-R7	2	Group - 2	U24
+P3V3_IO1	3.3	+12V0_AUX_2	92%	32.086	105.884	LTM4678EY#PBF (Single)	50	Group - 3	U13
+P3V3_IO2	3.3	+12V0_AUX_2	92%	30.616	101.033	LTM4678EY#PBF (Single)	50	Group - 3	U30
+P1V2_G3	1.2	+12V0_AUX_1	90%	31.978	38.374	LTM4678EY#PBF (Single)	50	Group - 3	U10
+P12V0_FMC_A	12	+12V0_AUX_2	85%	1.000	12.000	FET/LTC4211CMS#PBF	3	Group - 3	U107/Q9
+P12V0_FMC_B	12	+12V0_AUX_2	85%	1.000	12.000	FET/LTC4211CMS#PBF	3	Group - 3	U4/Q10
+P1V8_G3	1.8	+P2V5_G2	85%	1.007	1.812	ADP7159ACPZ-01-R7	2	Group - 3	EU33
+DDR4_VTT_0V6_G3	0.6	+P1V2_IO	50%	1.000	0.600	NCP51200MNTXG	3	Group - 3	EU26
+DIMM_VREF_0V6_G3	0.6	+P1V2_IO	50%	0.100	0.060	NCP51200MNTXG	3	Group - 3	U69
+DIMM_VTT_0V6_G3	0.6	+P1V2_IO	50%	1.000	0.600	NCP51200MNTXG	3	Group - 3	U69
+DRR4_VREF_0V6_G3	0.6	+P1V2_IO	50%	0.500	0.300	NCP51200MNTXG	3	Group - 3	EU26

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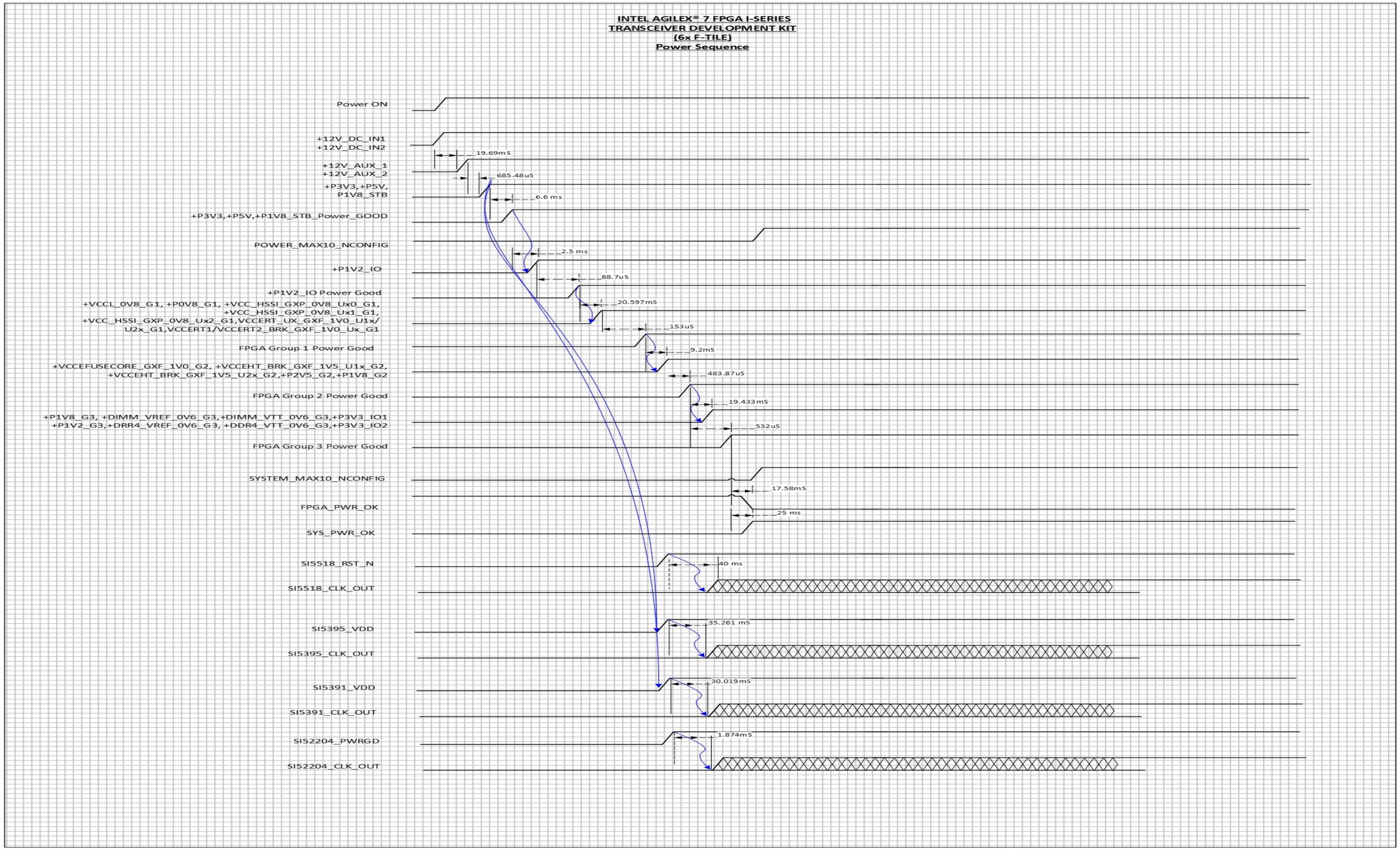
		SCALE:	DO NOT SCALE DRAWING	SHEET 4 OF 105	

POWER SEQUENCE GRAPH



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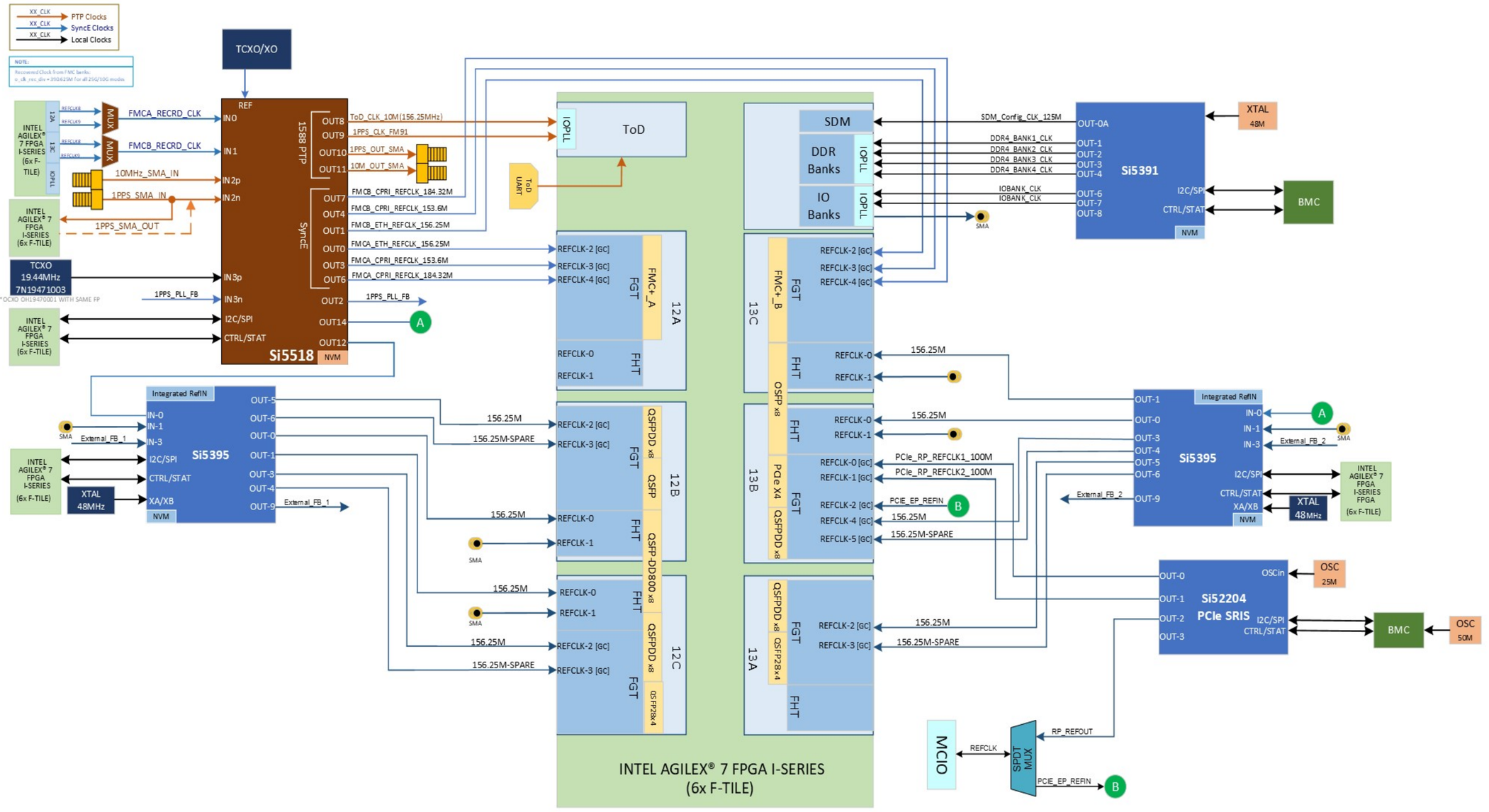
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	5 OF 105

POWER SEQUENCE

CLOCK TREE



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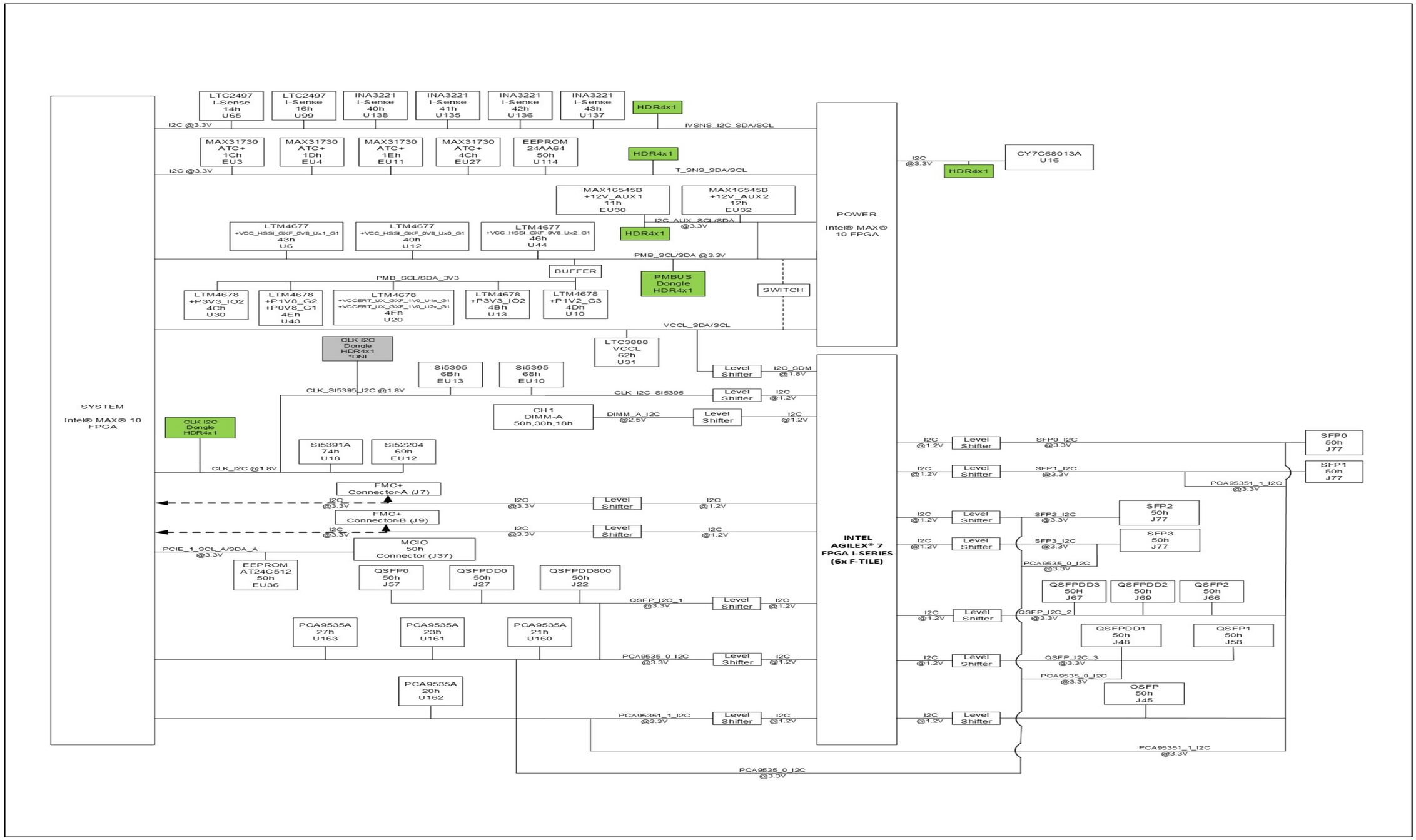
		SCALE:	DO NOT SCALE DRAWING	SHEET 6 OF 105	

CLOCK TREE

I2C TREE



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I2C TREE

I2C TABLE

I2C NETS	MASTER 1	MASTER 2	MASTER 3	SLAVE 1	SLAVE 2	SLAVE 3	SLAVE 4	SLAVE 5	SLAVE 6	SLAVE 7	SLAVE 8	SLAVE 9	INTER I2C CONNECTION
CLK_SI5395_I2C_1V2_SDA CLK_SI5395_I2C_1V2_SCL	U1 FM91	J140 HEADER	------	EU13 SI5395 0x6B	EU10 SI5395 0x68	------	------	------	------	------	------	------	BELOW I2C ARE CONNECTED CLK_SI5395_I2C & CLK_I2C
CLK_I2C_SDA CLK_I2C_SCL	U3 SYSTEM MAX 10	J42 HDR	------	U18 SI5391 0x74	EU12 SI52204_A02BGMR 0x69	------	------	------	------	------	------	------	
PCA9535_0_1V2_SDA PCA9535_0_1V2_SCL	U1 FM91	U3 SYSTEM MAX 10	------	U161 PCA9535A 0x23	U160 PCA9535A 0x21	U163 PCA9535A 0x27	J77 SFP0 MOD3 0xA0	J48 QSFPDD1 0xA0	J58 QSFP1 0xA0	J22 QSFPDD800 0xA0	J27 QSFPDD0 0xA0	J57 QSFP0 0xA0	PCA9535_0_I2C IS CONNECTED TO SFP0_I2C,QSFP3/1_I2C & PROVIDED OPTION FOR **SFP1_I2C MODULES WITH SAME I2C ADDRESS WILL BE CONTROLLED USING MODSEL PIN
SFP0_MOD3_1V2_SDA SFP0_MOD3_1V2_SDA	U1 FM91	U3 SYSTEM MAX 10	------	------	------	------	J77 SFP0 MOD3 0xA0	------	------	------	------	------	
SFP1_MOD2_1V2_SDA SFP1_MOD2_1V2_SCL	U1 FM91	**U3 SYSTEM MAX 10	------	------	------	------	J77 SFP1 MOD2 0xA0	------	------	------	------	------	
I2C_QSFP_3_1V2_SDA I2C_QSFP_3_1V2_SCL	U1 FM91	U3 SYSTEM MAX 10	------	------	------	------	------	J48 QSFPDD1 0xA0	J58 QSFP1 0xA0	------	------	------	
I2C_QSFP_1_1V2_SDA I2C_QSFP_1_1V2_SCL	U1 FM91	U3 SYSTEM MAX 10	------	------	------	------	------	------	------	J22 QSFPDD800 0xA0	J27 QSFPDD0 0xA0	J57 QSFP0 0xA0	
PCA9535_1_1V2_SDA PCA9535_1_1V2_SCL	U1 FM91	U3 SYSTEM MAX 10	------	U162 PCA9535A 0x20	J69 QSFPDD2 0xA0	J67 QSFPDD3 0xA0	J66 QSFP2 0xA0	J77 SFP2 MOD1 0xA0	J45 OSFP 0xA0	------	------	------	PCA9535_1_I2C IS CONNECTED TO QSFP2_I2C & OSFP_I2C. PROVIDED OPTION FOR **SFP2/3_I2C MODULES WITH SAME I2C ADDRESS WILL BE CONTROLLED USING MODSEL PIN
I2C_QSFP_2_1V2_SDA I2C_QSFP_2_1V2_SCL	U1 FM91	U3 SYSTEM MAX 10	------	------	J69 QSFPDD2 0xA0	J67 QSFPDD3 0xA0	J66 QSFP2 0xA0	------	------	------	------	------	
SFP2_MOD1_1V2_SDA SFP2_MOD1_1V2_SCL	U1 FM91	**U3 SYSTEM MAX 10	------	------	------	------	------	J77 SFP2 MOD1 0xA0	------	------	------	------	
SFP3_MOD0_1V2_SDA SFP3_MOD0_1V2_SCL	U1 FM91	**U3 SYSTEM MAX 10	------	------	------	------	------	J77 SFP3 MOD0 0xA0	------	------	------	------	
I2C_OSFP_SDA I2C_OSFP_SCL	U1 FM91	U3 SYSTEM MAX 10	------	------	------	------	------	------	J45 OSFP 0xA0	------	------	------	
FMC_B_SDA_1V2 FMC_B_SCL_1V2	U1 FM91	**U3 SYSTEM MAX 10	------	J9 FMCB	------	------	------	------	------	------	------	------	
FMC_A_SDA_1V2 FMC_A_SCL_1V2	U1 FM91	**U3 SYSTEM MAX 10	------	J7 FMC A	------	------	------	------	------	------	------	------	
DDR4_DIMM_2_SDA_1V2 DDR4_DIMM_2_SCL_1V2	U1 FM91	------	------	J5 DIMM CONN EEPROM Memory- 0x50 WP settind- 0x30 Temp Sensor- 0x18	------	------	------	------	------	------	------	------	
PCIE_1_SCL_A PCIE_1_SDA_A	U3 SYSTEM MAX 10	------	------	J37 MCIO 0x50	EU36 EEPROM 0x50	------	------	------	------	------	------	------	
FX2_SCL FX2_SDA	J56-HDR	U16 CY7C68013A	------	U2 POWER MAX 10	------	------	------	------	------	------	------	------	
VCCL_SDA VCCL_SCL	U2 POWER MAX 10	U3 SYSTEM MAX 10	------	U31 VCCL CONTROLLER 0x62	FM91 SDM	------	------	------	------	------	------	------	VCCL_I2C & PMB_I2C ARE CONNECTED THROUGH A SWITCH S21 **BY DEFAULT- OPEN
PMB_SDA PMB_SCL	U2 POWER MAX 10	U3 SYSTEM MAX 10	J41 HDR	U6 LTM4677 0x43	U44 LTM4677 0x46	U12 LTM4677 0x40	U30 LTM4678 0x4C	U13 LTM4678 0x4B	U10 LTM4678 0x4D	U43 LTM4678 0x4E	U20 LTM4678 0x4F	------	
T_SNS_SCL T_SNS_SDA	**U2 POWER MAX 10	U3 SYSTEM MAX 10	J79 HDR	EU3 MAX31730 0x38	EU4 MAX31730 0x3A	EU11 MAX31730 0x3C	EU27 MAX31730 0x98	U114 EEPROM 24AA64 0x50	------	------	------	------	
IVSNS_I2C_SDA IVSNS_I2C_SCL	**U2 POWER MAX 10	U3 SYSTEM MAX 10	J149-HDR	U138 INA3221 0x40	U135 INA3221 0x41	U136 INA3221 0x42	U137 INA3221 0x43	U99 LTC2497 0x16	U65 LTC2497 0x14	------	------	------	
I2C_AUX_SCL I2C_AUX_SDA	U2 POWER MAX 10	J154 HDR	------	EU30 MAX16545B 0x11	EU32 MAX16545B 0x12	------	------	------	------	------	------	------	

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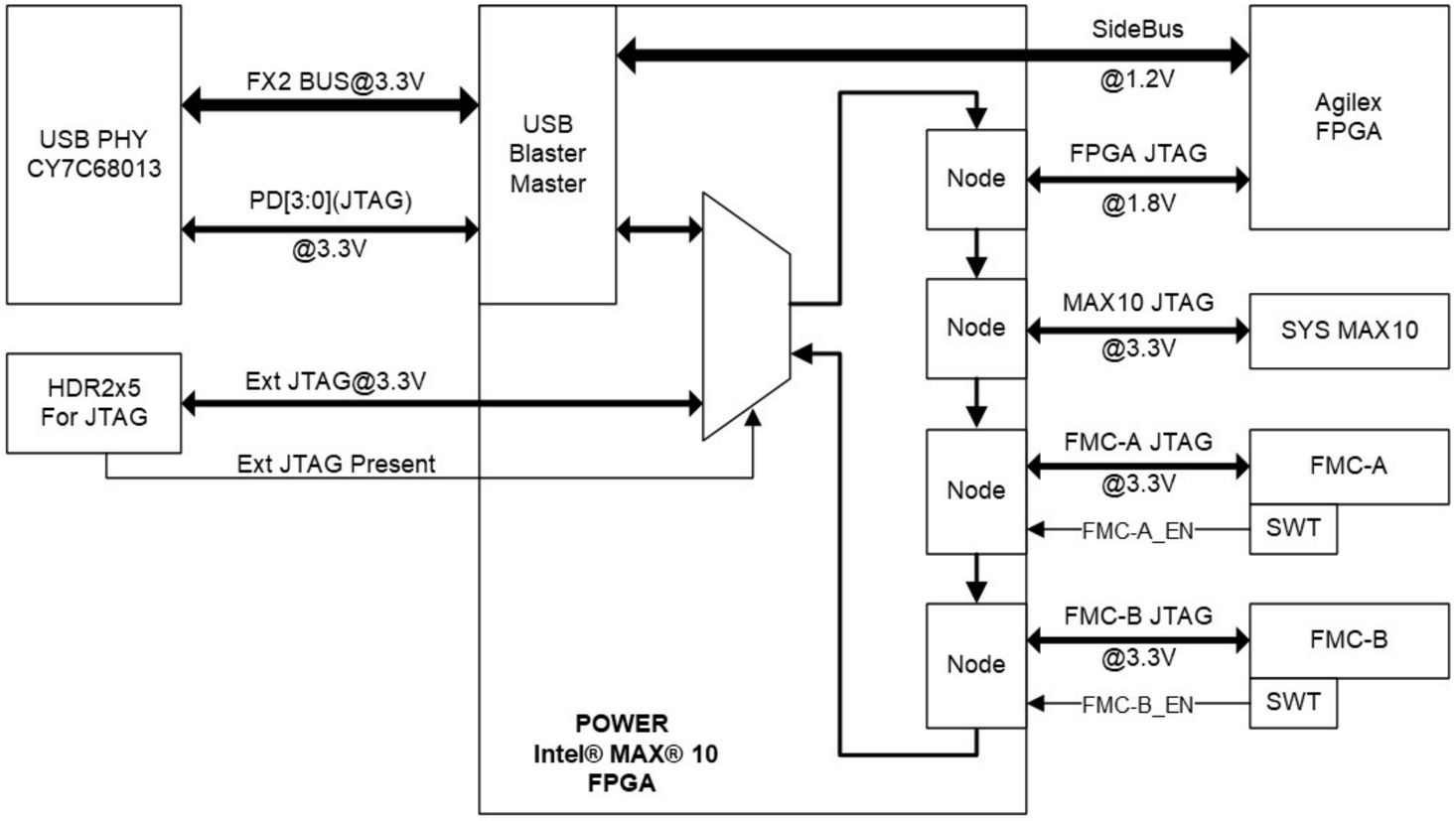
		SCALE:	DO NOT SCALE DRAWING	SHEET 8 OF 105	

I2C_TABLE

JTAG TOPOLOGY



Note:
1. The JTAG of Agilex FPGA can't be added to the chain before fully powered up

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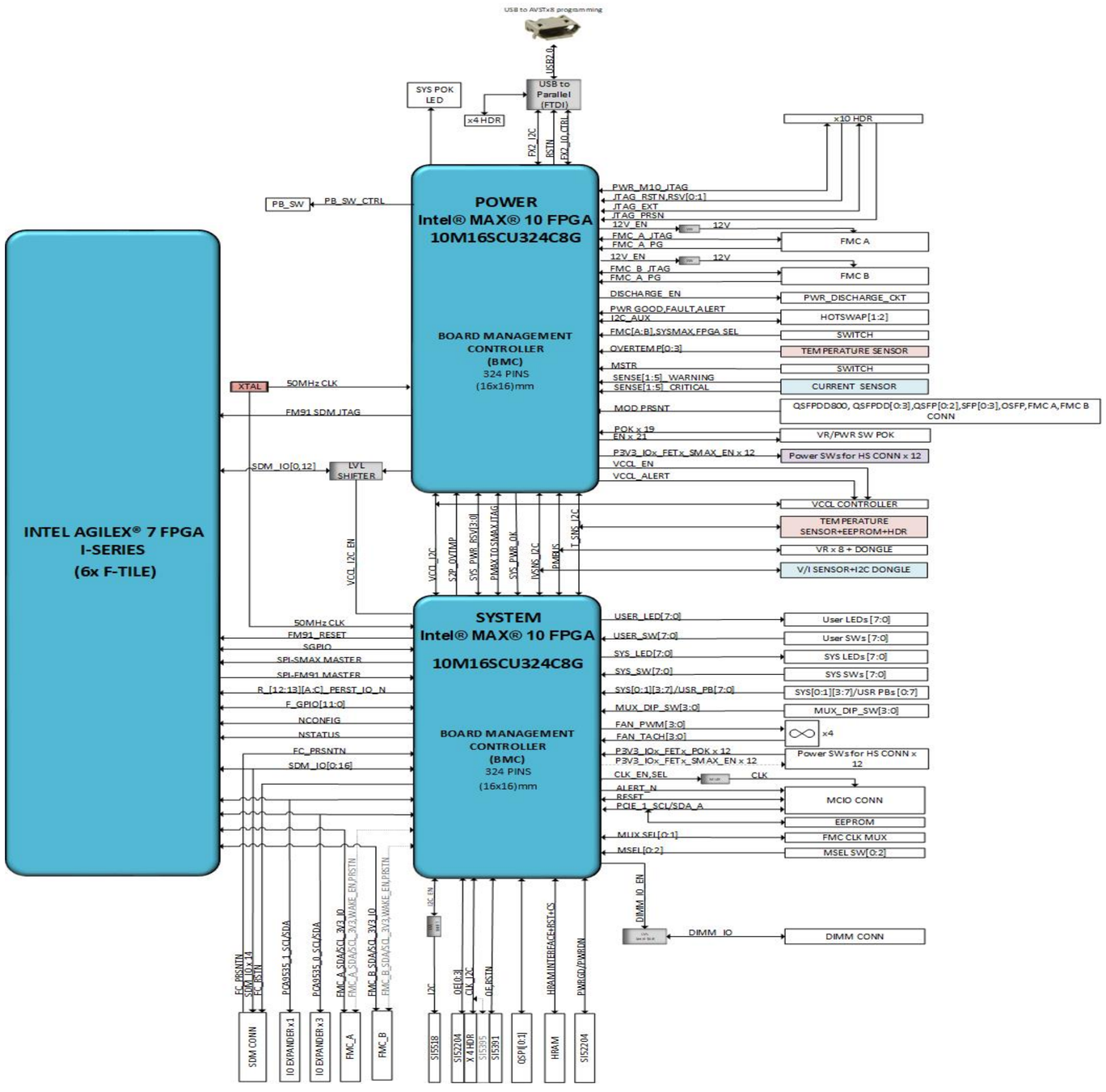
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	9 OF 105

BMC



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		SCALE:	DO NOT SCALE DRAWING	SHEET 10 OF 105	

BMC

SDM IO MAPPING

SDM PINS	MSEL FUNCTIONS	CONFIGURATION SOURCE FUNCTION
		AS
SDM_IO0		PWR_SCL
SDM_IO1		DATA1
SDM_IO2		CLK
SDM_IO3		DATA2
SDM_IO4		DATA0
SDM_IO5	MSEL0	NCSO0
SDM_IO6		DATA3
SDM_IO7	MSEL1	NCSO2
SDM_IO8		NCSO3
SDM_IO9	MSEL2	NCSO1
SDM_IO10		
SDM_IO11		HPS_CRSTN
SDM_IO12		
SDM_IO13		
SDM_IO14		
SDM_IO15		RESETN
SDM_IO16		CFG_DONE

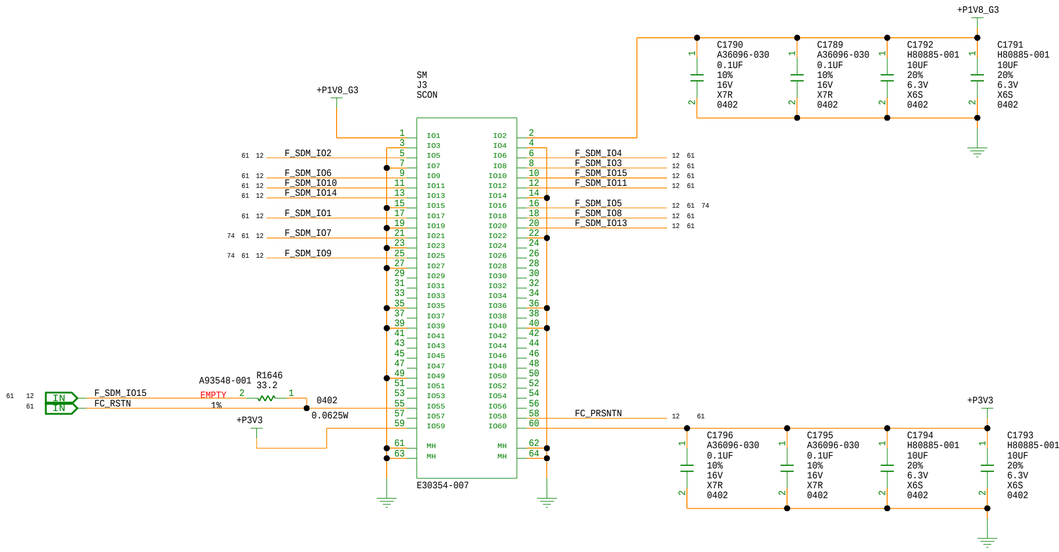
SYSTEM MAX IS THE SOURCE OF HPS_CRSTN FUNCTION

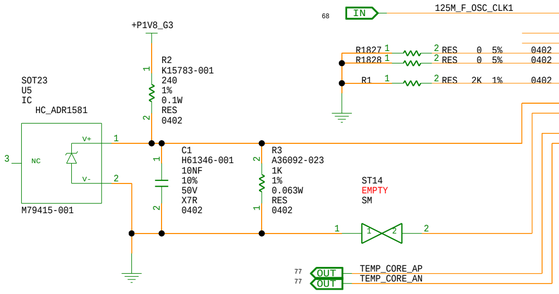
Tue Aug 8 11:15:59 2023

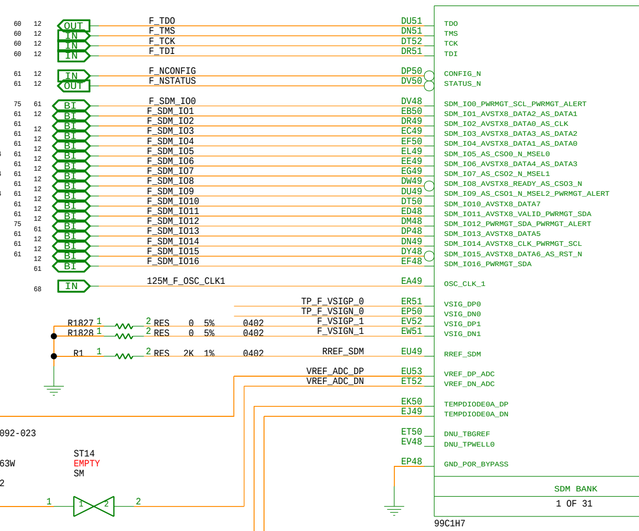
DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	11 OF 105

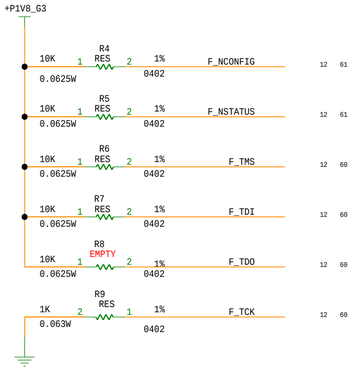
SDM IO MAPPING

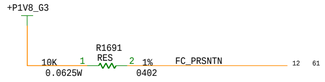
FPGA SDM











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		SCALE:	DO NOT SCALE DRAWING	SHEET	12 OF 105

FPGA BANK 2C

CAD NOTE:

BIT-SWAPPINGS ALLOWED WITHIN A BYTE.
BYTE-SWAPPING IS ALLOWED WITH PRIOR APPROVAL
FROM DESIGN ENGINEER

BGA
U1
EMPTY

HC_FM91_3948BGA

35	BI	DDR4_3_DQ63	ER25	IO_DIFF_RX_2C1_DN_DQ0		IO_CDR_DIFF_RX_2C13_DN_DQ4	CY26	CLK_TOD_10M_DN	IN 13 66
35	BI	DDR4_3_DQ62	ET24	IO_DIFF_RX_2C1_DP_DQ0		IO_CDR_DIFF_RX_2C13_DP_DQ4	DA25	CLK_TOD_10M_DP	IN 13 66
35	BI	DDR4_3_DQ61	EW25	IO_DIFF_TX_2C1_DN_DQ0		IO_DIFF_TX_2C13_DN_DQ4	DB24	QSFP2_MOD_SEL_N_1V2	OUT 48
35	BI	DDR4_3_DQ60	EV24	IO_DIFF_TX_2C1_DP_DQ0		IO_DIFF_TX_2C13_DP_DQ4	DC25	F_GPIO_08	BI 62
			ER27	IO_DIFF_RX_2C2_DN_DQ0		IO_DIFF_RX_2C14_DN_DQ4	CY28	F_GPIO_07	BI 62
35	BI	DDR4_DM7	ET26	IO_DIFF_RX_2C2_DP_DQ0		IO_DIFF_RX_2C14_DP_DQ4	DA27		
35	BI	DDR4_DQS_7_DN	EW27	IO_DIFF_TX_2C2_DN_DQS0_DN		IO_DIFF_TX_2C14_DN_DQS4_DN	DD26	MAX10_SPI_CSN	IN 62
35	BI	DDR4_DQS_7_DP	EV26	IO_DIFF_TX_2C2_DP_DQS0_DP		IO_DIFF_TX_2C14_DP_DQS4_DP	DC27	MAX10_SPI_SCLK	IN 62
35	BI	DDR4_3_DQ59	ER29	IO_CDR_DIFF_RX_2C3_DN_DQ0		IO_CDR_DIFF_RX_2C15_DN_DQ4	CY30	CLK_1PPS_1V2_FM91	IN 66
35	BI	DDR4_3_DQ58	ET28	IO_CDR_DIFF_RX_2C3_DP_DQ0		IO_CDR_DIFF_RX_2C15_DP_DQ4	DA29	MAX10_SPI_MOSI	IN 62
35	BI	DDR4_3_DQ57	EW29	IO_DIFF_TX_2C3_DN_DQ0		IO_DIFF_TX_2C15_DN_DQ4	DD28	MAX10_SPI_MISO	OUT 62
35	BI	DDR4_3_DQ56	EV28	IO_DIFF_TX_2C3_DP_DQ0		IO_DIFF_TX_2C15_DP_DQ4	DC29	PCA9535_1_1V2_INT_N	IN 48
35	BI	DDR4_3_DQ55	EL25	IO_DIFF_RX_2C4_DN_DQ1		IO_CDR_DIFF_RX_2C16_DN_DQ5	DF26	SI5395_1_1V2_A_OEN	OUT 69
35	BI	DDR4_3_DQ54	EK24	IO_DIFF_RX_2C4_DP_DQ1		IO_CDR_DIFF_RX_2C16_DP_DQ5	DE25	SI5395_2_1V2_A_RSTN	OUT 70
35	BI	DDR4_3_DQ53	EN25	IO_DIFF_TX_2C4_DN_DQ1		IO_DIFF_TX_2C16_DN_DQ5	DH26	SI5395_1_1V2_A_RSTN	OUT 69
35	BI	DDR4_3_DQ52	EP24	IO_DIFF_TX_2C4_DP_DQ1		IO_DIFF_TX_2C16_DP_DQ5	DJ25	CLK_SI5395_I2C_1V2_SDA	BI 69
			EL27	IO_DIFF_RX_2C5_DN_DQ1		IO_DIFF_RX_2C17_DN_DQ5	DF28	CLK_SI5395_I2C_1V2_SCL	OUT 69
			EK26	IO_DIFF_RX_2C5_DP_DQ1		IO_DIFF_RX_2C17_DP_DQ5	DE27	SI5395_2_1V2_A_OEN	OUT 70
35	BI	DDR4_DM6	EN27	IO_PLL_2C_T_CLKOUT1_DN_DIFF_TX_2C5_DN_DQS1_DN		IO_PLL_2C_B_CLKOUT1_DN_DIFF_TX_2C17_DN_DQS5_DN	DH28	QSFPDD2_MODSEL_L_1V2	OUT 48
35	BI	DDR4_DQS_6_DN	EP26	IO_PLL_2C_T_CLKOUT1_DP_PLL_2C_T_CLKOUT1_PLL_2C_T_FB1_DIFF_TX_2C5_DP_DQS1_DP		IO_PLL_2C_B_CLKOUT1_DP_PLL_2C_B_CLKOUT1_PLL_2C_B_FB1_DIFF_TX_2C17_DP_DQS5_DP	DJ27	SI5518_I2C_SDA_SDIO_1V2	BI 13 75
35	BI	DDR4_DQS_6_DP	EL29	IO_CDR_DIFF_RX_2C6_DN_DQ1		IO_CDR_DIFF_RX_2C18_DN_DQ5	DF30	SI5518_I2C_SCL_SCLK_1V2	BI 13 75
35	BI	DDR4_3_DQ51	EK28	IO_RZQ_T_2C_CDR_DIFF_RX_2C6_DP_DQ1		IO_RZQ_B_2C_CDR_DIFF_RX_2C18_DP_DQ5	DE29	QSFPDD3_MODSEL_L_1V2	OUT 48
35	BI	DDR4_3_DQ50	EN29	IO_CLK_T_2C_DN1_DIFF_TX_2C6_DN_DQ1		IO_CLK_B_2C_DN1_DIFF_TX_2C18_DN_DQ5	DH30	DDR_2_166.66M_REFCLK_DN	IN 13 68
35	BI	DDR4_3_DQ49	EP28	IO_CLK_T_2C_DP1_DIFF_TX_2C6_DP_DQ1		IO_CLK_B_2C_DP1_DIFF_TX_2C18_DP_DQ5	DJ29	DDR_2_166.66M_REFCLK_DP	IN 13 68
35	BI	DDR4_3_DQ48							
35	BI	DDR4_2_DQ47	EE25	IO_CLK_T_2C_DN0_DIFF_RX_2C7_DN_DQ2		IO_CLK_B_2C_DN0_CDR_DIFF_RX_2C19_DN_DQ6	DN23	CLK_100M_GPIO_2C_DN	IN 13 68
35	BI	DDR4_2_DQ46	EF24	IO_CLK_T_2C_DP0_DIFF_RX_2C7_DP_DQ2		IO_CLK_B_2C_DP0_CDR_DIFF_RX_2C19_DP_DQ6	DM22	CLK_100M_GPIO_2C_DP	IN 13 68
35	BI	DDR4_2_DQ45	EJ25	IO_DIFF_TX_2C7_DN_DQ2		IO_DIFF_TX_2C19_DN_DQ6	DM23		
35	BI	DDR4_2_DQ44	EH24	IO_DIFF_TX_2C7_DP_DQ2		IO_DIFF_TX_2C19_DP_DQ6	DT22	PCA9535_0_1V2_SDA	BI 48
			EE27	IO_PLL_2C_T_CLKOUT0_DN_DIFF_RX_2C8_DN_DQ2		IO_PLL_2C_B_CLKOUT0_DN_DIFF_RX_2C20_DN_DQ6	DL25	PCA9535_0_1V2_SCL	OUT 48
35	BI	DDR4_DM5	EF26	IO_PLL_2C_T_CLKOUT0_DP_PLL_2C_T_CLKOUT0_PLL_2C_T_FB0_DIFF_RX_2C8_DP_DQ2		IO_PLL_2C_B_CLKOUT0_DP_PLL_2C_B_CLKOUT0_PLL_2C_B_FB0_DIFF_RX_2C20_DP_DQ6	DK24	1PPS_SMA_OUT_1V2	OUT 66
35	BI	DDR4_DQS_5_DN	EJ27	IO_DIFF_TX_2C8_DN_DQS2_DN		IO_DIFF_TX_2C20_DN_DQS6_DN	DM25	FPGA_SPI_CSN	OUT 62
35	BI	DDR4_DQS_5_DP	EH26	IO_DIFF_TX_2C8_DP_DQS2_DP		IO_DIFF_TX_2C20_DP_DQS6_DP	DP24	PCA9535_1_1V2_SDA	BI 48
35	BI	DDR4_2_DQ43	EE29	IO_CDR_DIFF_RX_2C9_DN_DQ2		IO_CDR_DIFF_RX_2C21_DN_DQ6	DL27	PCA9535_1_1V2_SCL	OUT 48
35	BI	DDR4_2_DQ42	EF28	IO_CDR_DIFF_RX_2C9_DP_DQ2		IO_CDR_DIFF_RX_2C21_DP_DQ6	DK26	FPGA_SPI_SCLK	OUT 62
35	BI	DDR4_2_DQ41	EJ29	IO_DIFF_TX_2C9_DN_DQ2		IO_DIFF_TX_2C21_DN_DQ6	DN27	FPGA_SPI_MOSI	OUT 62
35	BI	DDR4_2_DQ40	EH28	IO_DIFF_TX_2C9_DP_DQ2		IO_DIFF_TX_2C21_DP_DQ6	DP26	FPGA_SPI_MISO	IN 62
35	BI	DDR4_2_DQ39	ER31	IO_DIFF_RX_2C10_DN_DQ3		IO_CDR_DIFF_RX_2C22_DN_DQ7	DR25	SI5518_RST_N_1V2	OUT 66
35	BI	DDR4_2_DQ38	ET30	IO_DIFF_RX_2C10_DP_DQ3		IO_CDR_DIFF_RX_2C22_DP_DQ7	DT24	SI5518_A0_CSB_1V2	BI 75
35	BI	DDR4_2_DQ37	EW31	IO_DIFF_TX_2C10_DN_DQ3		IO_DIFF_TX_2C22_DN_DQ7	DW25	SI5518_GPIO3_SDO_1V2	BI 75
35	BI	DDR4_2_DQ36	EV30	IO_DIFF_TX_2C10_DP_DQ3		IO_DIFF_TX_2C22_DP_DQ7	DV24	I2C_QSFP_2_1V2_SDA	BI 48
			ER33	IO_DIFF_RX_2C11_DN_DQ3		IO_DIFF_RX_2C23_DN_DQ7	DR27	I2C_QSFP_2_1V2_SCL	OUT 48
35	BI	DDR4_DM4	ET32	IO_DIFF_RX_2C11_DP_DQ3		IO_DIFF_RX_2C23_DP_DQ7	DT26		
35	BI	DDR4_DQS_4_DN	EW33	IO_DIFF_TX_2C11_DN_DQS3_DN		IO_DIFF_TX_2C23_DN_DQS7_DN	DW27		
35	BI	DDR4_DQS_4_DP	EV32	IO_DIFF_TX_2C11_DP_DQS3_DP		IO_DIFF_TX_2C23_DP_DQS7_DP	DV26		
35	BI	DDR4_2_DQ35	ER35	IO_CDR_DIFF_RX_2C12_DN_DQ3		IO_CDR_DIFF_RX_2C24_DN_DQ7	DR29	TOD_UART_TX_1V2	BI 13
35	BI	DDR4_2_DQ34	ET34	IO_CDR_DIFF_RX_2C12_DP_DQ3		IO_CDR_DIFF_RX_2C24_DP_DQ7	DT28	TOD_UART_RX_1V2	BI 13
35	BI	DDR4_2_DQ33	EW35	IO_DIFF_TX_2C12_DN_DQ3		IO_DIFF_TX_2C24_DN_DQ7	DW29		
35	BI	DDR4_2_DQ32	EV34	IO_DIFF_TX_2C12_DP_DQ3		IO_DIFF_TX_2C24_DP_DQ7	DV28		

TOP BOT

IO BANK 2C
2 OF 31

99C1H7

+P1V2_G3

75 13	SI5518_I2C_SDA_SDIO_1V2	R628	1 2	EMPTY	4.7K	1%	0.0625W	0402
75 13	SI5518_I2C_SCL_SCLK_1V2	R747	1 2	EMPTY	4.7K	1%	0.0625W	0402

CAD NOTE:

PLACE THESE TERMINATION RESISTORS UNDER THE FPGA

A36092-043
R165 1% 100 1 2 EMPTY 0.0625W 0402
CLK_100M_GPIO_2C_DP 13 68
CLK_100M_GPIO_2C_DN 13 68

R11 100 1 2 RES
CLK_TOD_10M_DP 13 66
CLK_TOD_10M_DN 13 66

A36092-043
R34 1% 100 1 2 EMPTY 0.0625W 0402
DDR_2_166.66M_REFCLK_DP 13 68
DDR_2_166.66M_REFCLK_DN 13 68

+P1V2_G3

R909 EMPTY 1% 1K 1 2 0.063W 0402
R918 EMPTY 1K 1 2 1% 0.063W 0402
R922 EMPTY 1K 1 2 0.063W 0402 1%
R939 EMPTY 1 2 1K 0.063W 0402 1%

68 13 DDR_2_166.66M_REFCLK_DN
DDR_2_166.66M_REFCLK_DP 13 68

CAD NOTE:

PLACE THESE TERMINATION RESISTORS NEAR TO THE FPGA

TOD HEADER

+P3V3
C65 D97712-022 1UF 10% 16V X6S 0402
C66 A36096-030 0.1UF 10% 16V X7R 0402

+P1V2_G3
C67 A36096-030 0.1UF 10% 16V X7R 0402

+P1V2_G3
R172 A36092-023 1K 1% 0.063W RES 0402

IC U7
HC_MAX3378EETD_T

VCC	14	VL	10
IO_VCC1	13	IO_VL1	1
IO_VCC2	12	IO_VL2	2
IO_VCC3	9	IO_VL3	5
IO_VCC4	8	IO_VL4	6
NC	4	EP	15
NC	11	GND	7
THREE_STATE_N	3		

13 BI TOD_UART_TX_3V3
13 BI TOD_UART_RX_3V3
TOD_UART_TX_1V2 BI 13
TOD_UART_RX_1V2 BI 13
TOD_THREE_STATE_N

C35081-002
MAX3378EETD+T

TH J21 CON HC_HDR_1X4
IO1 1 TOD_UART_TX_3V3 OUT 13
IO2 2 TOD_UART_RX_3V3 IN 13
IO3 3 TOD_P3V3_R 2 1 +P3V3
IO4 4 1% R645 10K
C70742-002

Tue Sep 26 11:47:31 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SCALE:	DO NOT SCALE DRAWING	SHEET	13 OF 105

INTEL AGILEX® 7 FPGA I-SERIES (6x F-TILE) - 2C

FPGA BANK 2B

BGA
U1
EMPTY

HC_FM91_3948BGA

36	BI	DDR4_4_DQ71	EL41	IO_DIFF_RX_2B1_DN_DQ8		IO_CDR_DIFF_RX_2B13_DN_DQ12	EA41	DDR4_1_DQ31	BI 34
36	BI	DDR4_4_DQ70	EK40	IO_DIFF_RX_2B1_DP_DQ8		IO_CDR_DIFF_RX_2B13_DP_DQ12	DY40	DDR4_1_DQ30	BI 34
36	BI	DDR4_4_DQ69	EN41	IO_DIFF_TX_2B1_DN_DQ8		IO_DIFF_TX_2B13_DN_DQ12	EC41	DDR4_1_DQ29	BI 34
36	BI	DDR4_4_DQ68	EP40	IO_DIFF_TX_2B1_DP_DQ8		IO_DIFF_TX_2B13_DP_DQ12	ED40	DDR4_1_DQ28	BI 34
			EL39	IO_DIFF_RX_2B2_DN_DQ8		IO_DIFF_RX_2B14_DN_DQ12	EA39		
36	BI	DDR4_DM8	EK38	IO_DIFF_RX_2B2_DP_DQ8		IO_DIFF_RX_2B14_DP_DQ12	DY38	DDR4_DM3	BI 34
36	BI	DDR4_DQS_8_DN	EN39	IO_DIFF_TX_2B2_DN_DQS8_DN		IO_DIFF_TX_2B14_DN_DQS12_DN	EC39	DDR4_DQS_3_DN	BI 34
36	BI	DDR4_DQS_8_DP	EP38	IO_DIFF_TX_2B2_DP_DQS8_DP		IO_DIFF_TX_2B14_DP_DQS12_DP	ED38	DDR4_DQS_3_DP	BI 34
36	BI	DDR4_4_DQ67	EL37	IO_CDR_DIFF_RX_2B3_DN_DQ8		IO_CDR_DIFF_RX_2B15_DN_DQ12	EA37	DDR4_1_DQ27	BI 34
36	BI	DDR4_4_DQ66	EK36	IO_CDR_DIFF_RX_2B3_DP_DQ8		IO_CDR_DIFF_RX_2B15_DP_DQ12	DY36	DDR4_1_DQ26	BI 34
36	BI	DDR4_4_DQ65	EN37	IO_DIFF_TX_2B3_DN_DQ8		IO_DIFF_TX_2B15_DN_DQ12	EC37	DDR4_1_DQ25	BI 34
36	BI	DDR4_4_DQ64	EP36	IO_DIFF_TX_2B3_DP_DQ8		IO_DIFF_TX_2B15_DP_DQ12	ED36	DDR4_1_DQ24	BI 34
36 35 34	OUT	DDR4_BG0	ER41	IO_DIFF_RX_2B4_DN_DQ9		IO_CDR_DIFF_RX_2B16_DN_DQ13	DR35	DDR4_1_DQ23	BI 34
36 35 34	OUT	DDR4_BA1	ET40	IO_DIFF_RX_2B4_DP_DQ9		IO_CDR_DIFF_RX_2B16_DP_DQ13	DT34	DDR4_1_DQ22	BI 34
36 35 34	OUT	DDR4_BA0	EW41	IO_DIFF_TX_2B4_DN_DQ9		IO_DIFF_TX_2B16_DN_DQ13	DW35	DDR4_1_DQ21	BI 34
36 35 34	IN	DDR4_ALERT_N	EV40	IO_DIFF_TX_2B4_DP_DQ9		IO_DIFF_TX_2B16_DP_DQ13	DV34	DDR4_1_DQ20	BI 34
36 35 34	OUT	DDR4_A16	ER39	IO_DIFF_RX_2B5_DN_DQ9		IO_DIFF_RX_2B17_DN_DQ13	DR33		
36 35 34	OUT	DDR4_A15	ET38	IO_DIFF_RX_2B5_DP_DQ9		IO_DIFF_RX_2B17_DP_DQ13	DT32	DDR4_DM2	BI 34
36 35 34	OUT	DDR4_A14	EW39	IO_PLL_2B_T_CLKOUT1_DN_DIFF_TX_2B5_DN_DQS9_DN		IO_PLL_2B_B_CLKOUT1_DN_DIFF_TX_2B17_DN_DQS13_DN	DW33	DDR4_DQS_2_DN	BI 34
36 35 34	OUT	DDR4_A13	EV38	IO_PLL_2B_T_CLKOUT1_DP_PLL_2B_T_CLKOUT1_PLL_2B_T_FB1_DIFF_TX_2B5_DP_DQS9_DP		IO_PLL_2B_B_CLKOUT1_DP_PLL_2B_B_CLKOUT1_PLL_2B_B_FB1_DIFF_TX_2B17_DP_DQS13_DP	DV32	DDR4_DQS_2_DP	BI 34
36 35 34	OUT	DDR4_A12	ER37	IO_CDR_DIFF_RX_2B6_DN_DQ9		IO_CDR_DIFF_RX_2B18_DN_DQ13	DR31	DDR4_1_DQ19	BI 34
		2B_RZQ	ET36	IO_RZQ_T_2B_CDR_DIFF_RX_2B6_DP_DQ9		IO_RZQ_B_2B_CDR_DIFF_RX_2B18_DP_DQ13	DT30	DDR4_1_DQ18	BI 34
68 14	IN	DDR_1_166.66M_REFCLK_DN	EW37	IO_CLK_T_2B_DN1_DIFF_TX_2B6_DN_DQ9		IO_CLK_B_2B_DN1_DIFF_TX_2B18_DN_DQ13	DW31	DDR4_1_DQ17	BI 34
68 14	IN	DDR_1_166.66M_REFCLK_DP	EV36	IO_CLK_T_2B_DP1_DIFF_TX_2B6_DP_DQ9		IO_CLK_B_2B_DP1_DIFF_TX_2B18_DP_DQ13	DV30	DDR4_1_DQ16	BI 34
36 35 34	OUT	DDR4_A11	EE35	IO_CLK_T_2B_DN0_DIFF_RX_2B7_DN_DQ10		IO_CLK_B_2B_DN0_CDR_DIFF_RX_2B19_DN_DQ14	EA35	DDR4_0_DQ15	BI 34
36 35 34	OUT	DDR4_A10	EF34	IO_CLK_T_2B_DP0_DIFF_RX_2B7_DP_DQ10		IO_CLK_B_2B_DP0_CDR_DIFF_RX_2B19_DP_DQ14	DY34	DDR4_0_DQ14	BI 34
36 35 34	OUT	DDR4_A9	EJ35	IO_DIFF_TX_2B7_DN_DQ10		IO_DIFF_TX_2B19_DN_DQ14	EC35	DDR4_0_DQ13	BI 34
36 35 34	OUT	DDR4_A8	EH34	IO_DIFF_TX_2B7_DP_DQ10		IO_DIFF_TX_2B19_DP_DQ14	ED34	DDR4_0_DQ12	BI 34
36 35 34	OUT	DDR4_A7	EE33	IO_PLL_2B_T_CLKOUT0_DN_DIFF_RX_2B8_DN_DQ10		IO_PLL_2B_B_CLKOUT0_DN_DIFF_RX_2B20_DN_DQ14	EA33		
36 35 34	OUT	DDR4_A6	EF32	IO_PLL_2B_T_CLKOUT0_DP_PLL_2B_T_CLKOUT0_PLL_2B_T_FB0_DIFF_RX_2B8_DP_DQ10		IO_PLL_2B_B_CLKOUT0_DP_PLL_2B_B_CLKOUT0_PLL_2B_B_FB0_DIFF_RX_2B20_DP_DQ14	DY32	DDR4_DM1	BI 34
36 35 34	OUT	DDR4_A5	EJ33	IO_DIFF_TX_2B8_DN_DQS10_DN		IO_DIFF_TX_2B20_DN_DQS14_DN	EC33	DDR4_DQS_1_DN	BI 34
36 35 34	OUT	DDR4_A4	EH32	IO_DIFF_TX_2B8_DP_DQS10_DP		IO_DIFF_TX_2B20_DP_DQS14_DP	ED32	DDR4_DQS_1_DP	BI 34
36 35 34	OUT	DDR4_A3	EE31	IO_CDR_DIFF_RX_2B9_DN_DQ10		IO_CDR_DIFF_RX_2B21_DN_DQ14	EA31	DDR4_0_DQ11	BI 34
36 35 34	OUT	DDR4_A2	EF30	IO_CDR_DIFF_RX_2B9_DP_DQ10		IO_CDR_DIFF_RX_2B21_DP_DQ14	DY30	DDR4_0_DQ10	BI 34
36 35 34	OUT	DDR4_A1	EJ31	IO_DIFF_TX_2B9_DN_DQ10		IO_DIFF_TX_2B21_DN_DQ14	EC31	DDR4_0_DQ9	BI 34
36 35 34	OUT	DDR4_A0	EH30	IO_DIFF_TX_2B9_DP_DQ10		IO_DIFF_TX_2B21_DP_DQ14	ED30	DDR4_0_DQ8	BI 34
36 35 34	OUT	DDR4_PAR	EL35	IO_DIFF_RX_2B10_DN_DQ11		IO_CDR_DIFF_RX_2B22_DN_DQ15	EA29	DDR4_0_DQ7	BI 34
			EK34	IO_DIFF_RX_2B10_DP_DQ11		IO_CDR_DIFF_RX_2B22_DP_DQ15	DY28	DDR4_0_DQ6	BI 34
36 35 34	OUT	DDR4_CK_DN	EN35	IO_DIFF_TX_2B10_DN_DQ11		IO_DIFF_TX_2B22_DN_DQ15	EC29	DDR4_0_DQ5	BI 34
36 35 34	OUT	DDR4_CK_DP	EP34	IO_DIFF_TX_2B10_DP_DQ11		IO_DIFF_TX_2B22_DP_DQ15	ED28	DDR4_0_DQ4	BI 34
			EL33	IO_DIFF_RX_2B11_DN_DQ11		IO_DIFF_RX_2B23_DN_DQ15	EA27		
36 35 34	OUT	DDR4_CKE	EK32	IO_DIFF_RX_2B11_DP_DQ11		IO_DIFF_RX_2B23_DP_DQ15	DY26	DDR4_DM0	BI 34
			EN33	IO_DIFF_TX_2B11_DN_DQS11_DN		IO_DIFF_TX_2B23_DN_DQS15_DN	EC27	DDR4_DQS_0_DN	BI 34
36 35 34	OUT	DDR4_ODT	EP32	IO_DIFF_TX_2B11_DP_DQS11_DP		IO_DIFF_TX_2B23_DP_DQS15_DP	ED26	DDR4_DQS_0_DP	BI 34
36 35 34	OUT	DDR4_ACT_N	EL31	IO_CDR_DIFF_RX_2B12_DN_DQ11		IO_CDR_DIFF_RX_2B24_DN_DQ15	EA25	DDR4_0_DQ3	BI 34
36 35 34	OUT	DDR4_CS_N	EK30	IO_CDR_DIFF_RX_2B12_DP_DQ11		IO_CDR_DIFF_RX_2B24_DP_DQ15	DY24	DDR4_0_DQ2	BI 34
36 35 34	OUT	DDR4_RESET_N	EN31	IO_DIFF_TX_2B12_DN_DQ11		IO_DIFF_TX_2B24_DN_DQ15	EC25	DDR4_0_DQ1	BI 34
36 35 34	OUT	DDR4_BG1	EP30	IO_DIFF_TX_2B12_DP_DQ11	TOP BOT	IO_DIFF_TX_2B24_DP_DQ15	ED24	DDR4_0_DQ0	BI 34

IO BANK 2B
3 OF 31
99C1H7

R2024 240 1% 0.1W RES 0402

+P1V2_G3 +P1V2_G3

R1116 EMPTY 1K 1% 0.063W 0402
R1117 EMPTY 1K 1% 0.063W 0402
R1119 EMPTY 1K 1% 0.063W 0402
R1120 EMPTY 1K 1% 0.063W 0402

68 14 DDR_1_166.66M_REFCLK_DN
DDR_1_166.66M_REFCLK_DP 14 68

R39 A36092-043 100 1% 0.0625W EMPTY 0402

DDR_1_166.66M_REFCLK_DP 14 68
DDR_1_166.66M_REFCLK_DN 14 68

CAD NOTE:

PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA

Tue Sep 26 11:47:31 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation INTEL CORPORATION,BANGALORE INDIA, 560103	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 14 OF 105	

FPGA BANK 2A

BGA
U1
EMPTY

HC_FM91_3948BGA

					IO_DIFF_RX_2A1_DN_DQ16	EE47	FMC_A_LA_22_DN	B1	
					IO_DIFF_RX_2A1_DP_DQ16	EF46	FMC_A_LA_22_DP	B1	
					IO_DIFF_TX_2A1_DN_DQ16	EJ47	FMC_A_LA_19_DN	B1	
					IO_DIFF_TX_2A1_DP_DQ16	EH46	FMC_A_LA_19_DP	B1	
58	54				IO_DIFF_RX_2A2_DN_DQ16	EE45	FMC_A_LA_5_DN	B1	
58	54				IO_DIFF_RX_2A2_DP_DQ16	EF44	FMC_A_LA_5_DP	B1	
					IO_DIFF_TX_2A2_DN_DQS16_DN	EJ45	FMC_A_LA_15_DN	B1	
					IO_DIFF_TX_2A2_DP_DQS16_DP	EH44	FMC_A_LA_15_DP	B1	
58	54				IO_CDR_DIFF_RX_2A3_DN_DQ16	EE43	FMC_A_LA_1_DN	B1	
58	54				IO_CDR_DIFF_RX_2A3_DP_DQ16	EF42	FMC_A_LA_1_DP	B1	
	54				IO_DIFF_TX_2A3_DN_DQ16	EJ43	FMC_A_LA_12_DN	B1	
	54				IO_DIFF_TX_2A3_DP_DQ16	EH42	FMC_A_LA_12_DP	B1	
	54				IO_DIFF_RX_2A4_DN_DQ17	EL47	FMC_A_LA_23_DN	B1	
	54				IO_DIFF_RX_2A4_DP_DQ17	EK46	FMC_A_LA_23_DP	B1	
58	54				IO_DIFF_TX_2A4_DN_DQ17	EN47	FMC_A_LA_18_DN	B1	
58	54				IO_DIFF_TX_2A4_DP_DQ17	EP46	FMC_A_LA_18_DP	B1	
	54				IO_DIFF_RX_2A5_DN_DQ17	EL45	FMC_A_LA_13_DN	B1	
	54				IO_DIFF_RX_2A5_DP_DQ17	EK44	FMC_A_LA_13_DP	B1	
58	54				IO_PLL_2A_T_CLKOUT1_DN_DIFF_TX_2A5_DN_DQS17_DN	EN45	FMC_A_LA_17_DN	B1	
58	54				IO_PLL_2A_T_CLKOUT1_DP_PLL_2A_T_CLKOUT1_PLL_2A_T_FB1_DIFF_TX_2A5_DP_DQS17_DP	EP44	FMC_A_LA_17_DP	B1	
58	54				IO_CDR_DIFF_RX_2A6_DN_DQ17	EL43	FMC_A_LA_4_DN	B1	
58	54				IO_RZQ_T_2A_CDR_DIFF_RX_2A6_DP_DQ17	EK42	FMC_A_LA_4_DP	B1	
58	54				IO_CLK_T_2A_DN1_DIFF_TX_2A6_DN_DQ17	EN43	FMC_A_CLK2_M2C_DN	IN	
58	54				IO_CLK_T_2A_DP1_DIFF_TX_2A6_DP_DQ17	EP42	FMC_A_CLK2_M2C_DP	IN	
	54				IO_CLK_T_2A_DN0_DIFF_RX_2A7_DN_DQ18	ER47	FMC_A_CLK0_M2C_DN	IN	
58	54				IO_CLK_T_2A_DP0_DIFF_RX_2A7_DP_DQ18	ET46	FMC_A_CLK0_M2C_DP	IN	
54	15				IO_DIFF_TX_2A7_DN_DQ18	EW47	FMC_A_SYNC_M2C_DN	IN	
54	15				IO_DIFF_TX_2A7_DP_DQ18	EV46	FMC_A_SYNC_M2C_DP	IN	
58	54				IO_PLL_2A_T_CLKOUT0_DN_DIFF_RX_2A8_DN_DQ18	ER45	FMC_A_REFCLK_C2M_DN	OUT	
58	54				IO_PLL_2A_T_CLKOUT0_DP_PLL_2A_T_CLKOUT0_PLL_2A_T_FB0_DIFF_RX_2A8_DP_DQ18	ET44	FMC_A_REFCLK_C2M_DP	OUT	
58	54				IO_DIFF_TX_2A8_DN_DQS18_DN	EW45	FMC_A_SYNC_C2M_DN	OUT	
58	54				IO_DIFF_TX_2A8_DP_DQS18_DP	EV44	FMC_A_SYNC_C2M_DP	OUT	
	56				IO_CDR_DIFF_RX_2A9_DN_DQ18	ER43	FMC_A_SDA_1V2	B1	
	56				IO_CDR_DIFF_RX_2A9_DP_DQ18	ET42	FMC_A_SCL_1V2	B1	
	54				IO_DIFF_TX_2A9_DN_DQ18	EW43	FMC_A_LA_9_DN	B1	
	54				IO_DIFF_TX_2A9_DP_DQ18	EV42	FMC_A_LA_9_DP	B1	
					IO_DIFF_RX_2A10_DN_DQ19	EE41	FPGA_SGPI	B1	
	62				IO_DIFF_RX_2A10_DP_DQ19	EF40	F_GPIO_10	B1	
	62				IO_DIFF_TX_2A10_DN_DQ19	EJ41	F_GPIO_09	B1	
	48				IO_DIFF_TX_2A10_DP_DQ19	EH40	I2C_QSFP_1_1V2_SDA	B1	
	48				IO_DIFF_RX_2A11_DN_DQ19	EE39	I2C_QSFP_1_1V2_SCL	IN	
	62				IO_DIFF_RX_2A11_DP_DQ19	EF38	F_GPIO_06	B1	
	62				IO_DIFF_TX_2A11_DN_DQS19_DN	EJ39	F_GPIO_05	B1	
	62				IO_DIFF_TX_2A11_DP_DQS19_DP	EH38	F_GPIO_04	B1	
	62				IO_CDR_DIFF_RX_2A12_DN_DQ19	EE37	F_GPIO_03	B1	
	62				IO_CDR_DIFF_RX_2A12_DP_DQ19	EF36	F_GPIO_02	B1	
	62				IO_DIFF_TX_2A12_DN_DQ19	EJ37	F_GPIO_01	B1	
	62				IO_DIFF_TX_2A12_DP_DQ19	EH36	F_GPIO_00	B1	

TOP

					IO_CDR_DIFF_RX_2A13_DN_DQ20	DK46	FMC_A_LA_29_DN	B1	
					IO_CDR_DIFF_RX_2A13_DP_DQ20	DL45	FMC_A_LA_29_DP	B1	
					IO_DIFF_TX_2A13_DN_DQ20	DP46	FMC_A_LA_30_DN	B1	
					IO_DIFF_TX_2A13_DP_DQ20	DN45	FMC_A_LA_30_DP	B1	
					IO_DIFF_RX_2A14_DN_DQ20	DK44	FMC_A_LA_31_DN	B1	
					IO_DIFF_RX_2A14_DP_DQ20	DL43	FMC_A_LA_31_DP	B1	
					IO_DIFF_TX_2A14_DN_DQS20_DN	DP44	FMC_A_LA_33_DN	B1	
					IO_DIFF_TX_2A14_DP_DQS20_DP	DN43	FMC_A_LA_33_DP	B1	
					IO_CDR_DIFF_RX_2A15_DN_DQ20	DK42	FMC_A_LA_32_DN	B1	
					IO_CDR_DIFF_RX_2A15_DP_DQ20	DL41	FMC_A_LA_32_DP	B1	
					IO_DIFF_TX_2A15_DN_DQ20	DP42	FMC_A_LA_10_DN	B1	
					IO_DIFF_TX_2A15_DP_DQ20	DN41	FMC_A_LA_10_DP	B1	
					IO_CDR_DIFF_RX_2A16_DN_DQ21	DR47	FMC_A_LA_24_DN	B1	
					IO_CDR_DIFF_RX_2A16_DP_DQ21	DT46	FMC_A_LA_24_DP	B1	
					IO_DIFF_TX_2A16_DN_DQ21	DW47	FMC_A_LA_21_DN	B1	
					IO_DIFF_TX_2A16_DP_DQ21	DV46	FMC_A_LA_21_DP	B1	
					IO_DIFF_RX_2A17_DN_DQ21	DR45	FMC_A_LA_28_DN	B1	
					IO_DIFF_RX_2A17_DP_DQ21	DT44	FMC_A_LA_28_DP	B1	
				IO_PLL_2A_B_CLKOUT1_DN_DIFF_TX_2A17_DN_DQS21_DN		DW45	FMC_A_LA_25_DN	B1	
				IO_PLL_2A_B_CLKOUT1_DP_PLL_2A_B_CLKOUT1_PLL_2A_B_FB1_DIFF_TX_2A17_DP_DQS21_DP		DV44	FMC_A_LA_25_DP	B1	
				IO_CDR_DIFF_RX_2A18_DN_DQ21		DR43	FMC_A_LA_14_DN	B1	
				IO_RZQ_B_2A_CDR_DIFF_RX_2A18_DP_DQ21		DT42	FMC_A_LA_14_DP	B1	
				IO_CLK_B_2A_DN1_DIFF_TX_2A18_DN_DQ21		DW43	FMC_A_CLK1_M2C_LT_DN	IN	
				IO_CLK_B_2A_DP1_DIFF_TX_2A18_DP_DQ21		DV42	FMC_A_CLK1_M2C_LT_DP	IN	
				IO_CLK_B_2A_DN0_CDR_DIFF_RX_2A19_DN_DQ22		EA47	FMC_A_REFCLK_M2C_DN	IN	
				IO_CLK_B_2A_DP0_CDR_DIFF_RX_2A19_DP_DQ22		DY46	FMC_A_REFCLK_M2C_DP	IN	
				IO_DIFF_TX_2A19_DN_DQ22		EC47	FMC_A_LA_26_DN	B1	
				IO_DIFF_TX_2A19_DP_DQ22		ED46	FMC_A_LA_26_DP	B1	
				IO_PLL_2A_B_CLKOUT0_DN_DIFF_RX_2A20_DN_DQ22		EA45	FMC_A_LA_27_DN	B1	
				IO_PLL_2A_B_CLKOUT0_DP_PLL_2A_B_CLKOUT0_PLL_2A_B_FB0_DIFF_RX_2A20_DP_DQ22		DY44	FMC_A_LA_27_DP	B1	
				IO_DIFF_TX_2A20_DN_DQS22_DN		EC45	FMC_A_LA_0_DN	B1	
				IO_DIFF_TX_2A20_DP_DQS22_DP		ED44	FMC_A_LA_0_DP	B1	
				IO_CDR_DIFF_RX_2A21_DN_DQ22		EA43	FMC_A_LA_3_DN	B1	
				IO_CDR_DIFF_RX_2A21_DP_DQ22		DY42	FMC_A_LA_3_DP	B1	
				IO_DIFF_TX_2A21_DN_DQ22		EC43	FMC_A_LA_11_DN	B1	
				IO_DIFF_TX_2A21_DP_DQ22		ED42	FMC_A_LA_11_DP	B1	
				IO_CDR_DIFF_RX_2A22_DN_DQ23		DR41	FMC_A_LA_16_DN	B1	
				IO_CDR_DIFF_RX_2A22_DP_DQ23		DT40	FMC_A_LA_16_DP	B1	
				IO_DIFF_TX_2A22_DN_DQ23		DW41	FMC_A_LA_2_DN	B1	
				IO_DIFF_TX_2A22_DP_DQ23		DV40	FMC_A_LA_2_DP	B1	
				IO_DIFF_RX_2A23_DN_DQ23		DR39	FMC_A_LA_20_DN	B1	
				IO_DIFF_RX_2A23_DP_DQ23		DT38	FMC_A_LA_20_DP	B1	
				IO_DIFF_TX_2A23_DN_DQS23_DN		DW39	FMC_A_LA_8_DN	B1	
				IO_DIFF_TX_2A23_DP_DQS23_DP		DV38	FMC_A_LA_8_DP	B1	
				IO_CDR_DIFF_RX_2A24_DN_DQ23		DR37	FMC_A_LA_6_DN	B1	
				IO_CDR_DIFF_RX_2A24_DP_DQ23		DT36	FMC_A_LA_6_DP	B1	
				IO_DIFF_TX_2A24_DN_DQ23		DW37	FMC_A_LA_7_DN	B1	
				IO_DIFF_TX_2A24_DP_DQ23		DV36	FMC_A_LA_7_DP	B1	

BOT

IO BANK 2A

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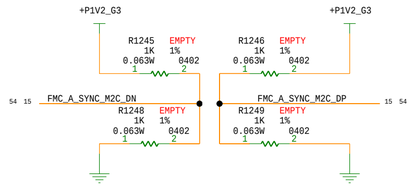

CAD NOTE:

PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA

Tue Sep 26 11:47:32 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SCALE:	DO NOT SCALE DRAWING	SHEET	15 OF 105

INTEL AGILEX® 7 FPGA I-SERIES (6x F-TILE) - 2A

FPGA BANK 3C

BGA
U1
EMPTY

HC_FM91_3948BGA

56	BI	FMC_B_LA_23_DN	P22	IO_DIFF_RX_3C1_DN_DQ24	IO_CDR_DIFF_RX_3C13_DN_DQ28	AP26	FMC_B_LA_28_DN	BI	57
56	BI	FMC_B_LA_23_DP	R21	IO_DIFF_RX_3C1_DP_DQ24	IO_CDR_DIFF_RX_3C13_DP_DQ28	AR25	FMC_B_LA_28_DP	BI	57
56	BI	FMC_B_LA_22_DN	M22	IO_DIFF_TX_3C1_DN_DQ24	IO_DIFF_TX_3C13_DN_DQ28	AM26	FMC_B_LA_31_DN	BI	57
56	BI	FMC_B_LA_22_DP	L21	IO_DIFF_TX_3C1_DP_DQ24	IO_DIFF_TX_3C13_DP_DQ28	AL25	FMC_B_LA_31_DP	BI	57
58 56	BI	FMC_B_LA_4_DN	P24	IO_DIFF_RX_3C2_DN_DQ24	IO_DIFF_RX_3C14_DN_DQ28	AP28	FMC_B_LA_33_DN	BI	57
58 56	BI	FMC_B_LA_4_DP	R23	IO_DIFF_RX_3C2_DP_DQ24	IO_DIFF_RX_3C14_DP_DQ28	AR27	FMC_B_LA_33_DP	BI	57
56	BI	FMC_B_LA_13_DN	M24	IO_DIFF_TX_3C2_DN_DQS24_DN	IO_DIFF_TX_3C14_DN_DQS28_DN	AM28	FMC_B_LA_0_DN	BI	56 58
56	BI	FMC_B_LA_13_DP	L23	IO_DIFF_TX_3C2_DP_DQS24_DP	IO_DIFF_TX_3C14_DP_DQS28_DP	AL27	FMC_B_LA_0_DP	BI	56 58
56	BI	FMC_B_LA_10_DN	P26	IO_CDR_DIFF_RX_3C3_DN_DQ24	IO_CDR_DIFF_RX_3C15_DN_DQ28	AP30	FMC_B_LA_2_DN	BI	56 58
56	BI	FMC_B_LA_10_DP	R25	IO_CDR_DIFF_RX_3C3_DP_DQ24	IO_CDR_DIFF_RX_3C15_DP_DQ28	AR29	FMC_B_LA_2_DP	BI	56 58
56	BI	FMC_B_LA_9_DN	M26	IO_DIFF_TX_3C3_DN_DQ24	IO_DIFF_TX_3C15_DN_DQ28	AM30	FMC_B_LA_3_DN	BI	56 58
56	BI	FMC_B_LA_9_DP	L25	IO_DIFF_TX_3C3_DP_DQ24	IO_DIFF_TX_3C15_DP_DQ28	AL29	FMC_B_LA_3_DP	BI	56 58
56	BI	FMC_B_LA_19_DN	K22	IO_DIFF_RX_3C4_DN_DQ25	IO_CDR_DIFF_RX_3C16_DN_DQ29	AK24	FMC_B_LA_30_DN	BI	57
56	BI	FMC_B_LA_19_DP	J21	IO_DIFF_RX_3C4_DP_DQ25	IO_CDR_DIFF_RX_3C16_DP_DQ29	AJ23	FMC_B_LA_30_DP	BI	57
56	BI	FMC_B_LA_20_DN	F22	IO_DIFF_TX_3C4_DN_DQ25	IO_DIFF_TX_3C16_DN_DQ29	AF24	FMC_B_LA_29_DN	BI	57
56	BI	FMC_B_LA_20_DP	G21	IO_DIFF_TX_3C4_DP_DQ25	IO_DIFF_TX_3C16_DP_DQ29	AG23	FMC_B_LA_29_DP	BI	57
58 56	BI	FMC_B_LA_18_DN	K24	IO_DIFF_RX_3C5_DN_DQ25	IO_DIFF_RX_3C17_DN_DQ29	AK26	FMC_B_LA_32_DN	BI	57
58 56	BI	FMC_B_LA_18_DP	J23	IO_DIFF_RX_3C5_DP_DQ25	IO_DIFF_RX_3C17_DP_DQ29	AJ25	FMC_B_LA_32_DP	BI	57
56	BI	FMC_B_LA_14_DN	F24	IO_PLL_3C_T_CLKOUT1_DN_DIFF_TX_3C5_DN_DQS25_DN	IO_PLL_3C_B_CLKOUT1_DN_DIFF_TX_3C17_DN_DQS29_DN	AF26	FMC_B_LA_1_DN	BI	56 58
56	BI	FMC_B_LA_14_DP	G23	IO_PLL_3C_T_CLKOUT1_DP_PLL_3C_T_CLKOUT1_PLL_3C_T_FB1_DIFF_TX_3C5_DP_DQS25_DP	IO_PLL_3C_B_CLKOUT1_DP_PLL_3C_B_FB1_DIFF_TX_3C17_DP_DQS29_DP	AG25	FMC_B_LA_1_DP	BI	56 58
56	BI	FMC_B_LA_16_DN	K26	IO_CDR_DIFF_RX_3C6_DN_DQ25	IO_CDR_DIFF_RX_3C18_DN_DQ29	AK28	FMC_B_LA_11_DN	BI	56
56	BI	FMC_B_LA_16_DP	J25	IO_RZQ_T_3C_CDR_DIFF_RX_3C6_DP_DQ25	IO_RZQ_B_3C_CDR_DIFF_RX_3C18_DP_DQ29	AJ27	FMC_B_LA_11_DP	BI	56
58 56	IN	FMC_B_CLK2_M2C_DN	F26	IO_CLK_T_3C_DN1_DIFF_TX_3C6_DN_DQ25	IO_CLK_B_3C_DN1_DIFF_TX_3C18_DN_DQ29	AF28	FMC_B_CLK1_M2C_DN	IN	56 58
58 56	IN	FMC_B_CLK2_M2C_DP	G25	IO_CLK_T_3C_DP1_DIFF_TX_3C6_DP_DQ25	IO_CLK_B_3C_DP1_DIFF_TX_3C18_DP_DQ29	AG27	FMC_B_CLK1_M2C_DP	IN	56 58
58 56	IN	FMC_B_CLK0_M2C_DN	D22	IO_CLK_T_3C_DN0_DIFF_RX_3C7_DN_DQ26	IO_CLK_B_3C_DN0_CDR_DIFF_RX_3C19_DN_DQ30	AD22	FMC_B_REFCLK_M2C_DN	IN	56 58
58 56	IN	FMC_B_CLK0_M2C_DP	E21	IO_CLK_T_3C_DP0_DIFF_RX_3C7_DP_DQ26	IO_CLK_B_3C_DP0_CDR_DIFF_RX_3C19_DP_DQ30	AE21	FMC_B_REFCLK_M2C_DP	IN	56 58
56 16	IN	FMC_B_SYNC_M2C_DN	B22	IO_DIFF_TX_3C7_DN_DQ26	IO_DIFF_TX_3C19_DN_DQ30	AB22	FMC_B_LA_25_DN	BI	56
56 16	IN	FMC_B_SYNC_M2C_DP	A21	IO_DIFF_TX_3C7_DP_DQ26	IO_DIFF_TX_3C19_DP_DQ30	AA21	FMC_B_LA_25_DP	BI	56
58 56	OUT	FMC_B_REFCLK_C2M_DN	D24	IO_PLL_3C_T_CLKOUT0_DN_DIFF_RX_3C8_DN_DQ26	IO_PLL_3C_B_CLKOUT0_DN_DIFF_RX_3C20_DN_DQ30	AD24	FMC_B_LA_7_DN	BI	57 58
58 56	OUT	FMC_B_REFCLK_C2M_DP	E23	IO_PLL_3C_T_CLKOUT0_DP_PLL_3C_T_CLKOUT0_PLL_3C_T_FB0_DIFF_RX_3C8_DP_DQ26	IO_PLL_3C_B_CLKOUT0_DP_PLL_3C_B_FB0_DIFF_RX_3C20_DP_DQ30	AE23	FMC_B_LA_7_DP	BI	57 58
58 56	OUT	FMC_B_SYNC_C2M_DN	B24	IO_DIFF_TX_3C8_DN_DQS26_DN	IO_DIFF_TX_3C20_DN_DQS30_DN	AB24	FMC_B_LA_24_DN	BI	56
58 56	OUT	FMC_B_SYNC_C2M_DP	A23	IO_DIFF_TX_3C8_DP_DQS26_DP	IO_DIFF_TX_3C20_DP_DQS30_DP	AA23	FMC_B_LA_24_DP	BI	56
58 56	BI	FMC_B_LA_17_DN	D26	IO_CDR_DIFF_RX_3C9_DN_DQ26	IO_CDR_DIFF_RX_3C21_DN_DQ30	AD26	FMC_B_LA_8_DN	BI	57
58 56	BI	FMC_B_LA_17_DP	E25	IO_CDR_DIFF_RX_3C9_DP_DQ26	IO_CDR_DIFF_RX_3C21_DP_DQ30	AE25	FMC_B_LA_8_DP	BI	57
56	BI	FMC_B_SDA_1V2	B26	IO_DIFF_TX_3C9_DN_DQ26	IO_DIFF_TX_3C21_DN_DQ30	AB26	FMC_B_LA_6_DN	BI	56 58
56	BI	FMC_B_SCL_1V2	A25	IO_DIFF_TX_3C9_DP_DQ26	IO_DIFF_TX_3C21_DP_DQ30	AA25	FMC_B_LA_6_DP	BI	56 58
			P28	IO_DIFF_RX_3C10_DN_DQ27	IO_CDR_DIFF_RX_3C22_DN_DQ31	Y22	FMC_B_LA_26_DN	BI	56
			R27	IO_DIFF_RX_3C10_DP_DQ27	IO_CDR_DIFF_RX_3C22_DP_DQ31	W21	FMC_B_LA_26_DP	BI	56
70	IN	CLK_SI5395_2_LOLB_N_R	M28	IO_DIFF_TX_3C10_DN_DQ27	IO_DIFF_TX_3C22_DN_DQ31	T22	FMC_B_LA_21_DN	BI	56
48	BI	I2C_OSFP_SDA	L27	IO_DIFF_TX_3C10_DP_DQ27	IO_DIFF_TX_3C22_DP_DQ31	U21	FMC_B_LA_21_DP	BI	56
48	OUT	I2C_OSFP_SCL	P30	IO_DIFF_RX_3C11_DN_DQ27	IO_DIFF_RX_3C23_DN_DQ31	Y24	FMC_B_LA_27_DN	BI	56 58
			R29	IO_DIFF_RX_3C11_DP_DQ27	IO_DIFF_RX_3C23_DP_DQ31	W23	FMC_B_LA_27_DP	BI	56 58
			M30	IO_DIFF_TX_3C11_DN_DQS27_DN	IO_DIFF_TX_3C23_DN_DQS31_DN	T24	FMC_B_LA_15_DN	BI	56
69	IN	CLK_SI5395_1_LOLB_N_R	L29	IO_DIFF_TX_3C11_DP_DQS27_DP	IO_DIFF_TX_3C23_DP_DQS31_DP	U23	FMC_B_LA_15_DP	BI	56
62	IN	FPGA_SGPIO_SYNC	P32	IO_CDR_DIFF_RX_3C12_DN_DQ27	IO_CDR_DIFF_RX_3C24_DN_DQ31	Y26	FMC_B_LA_12_DN	BI	56
62	IN	FPGA_SGPIO_CLK	R31	IO_CDR_DIFF_RX_3C12_DP_DQ27	IO_CDR_DIFF_RX_3C24_DP_DQ31	W25	FMC_B_LA_12_DP	BI	56
62	IN	F_GPIO_11	M32	IO_DIFF_TX_3C12_DN_DQ27	IO_DIFF_TX_3C24_DN_DQ31	T26	FMC_B_LA_5_DN	BI	56 58
62	OUT	FPGA_SGPO	L31	IO_DIFF_TX_3C12_DP_DQ27	IO_DIFF_TX_3C24_DP_DQ31	U25	FMC_B_LA_5_DP	BI	56 58
				TOP	BOT				

IO BANK 3C

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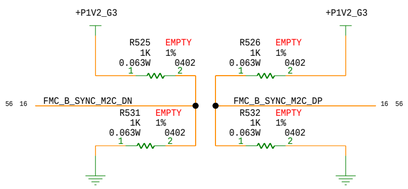

CAD NOTE:

PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA

Tue Sep 26 11:47:32 2023

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER / REV
PSG	INTEL CORPORATION,BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2 / 2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 16 OF 105

INTEL AGILEX® 7 FPGA I-SERIES (6x F-TILE) - 3C

FPGA BANK 3B

BGA
U1
EMPTY

HC_FM91_3948BGA

	IO_DIFF_RX_3B1_DN_DQ32	K38	IO_CDR_DIFF_RX_3B13_DN_DQ36	Y38	DDR4_DIMM_2_DQ47
	IO_DIFF_RX_3B1_DP_DQ32	J37	IO_CDR_DIFF_RX_3B13_DP_DQ36	W37	DDR4_DIMM_2_DQ46
	IO_DIFF_TX_3B1_DN_DQ32	F38	IO_DIFF_TX_3B13_DN_DQ36	T38	DDR4_DIMM_2_DQ44
	IO_DIFF_TX_3B1_DP_DQ32	G37	IO_DIFF_TX_3B13_DP_DQ36	U37	DDR4_DIMM_2_DQ45
	IO_DIFF_RX_3B2_DN_DQ32	K36	IO_DIFF_RX_3B14_DN_DQ36	Y36	DDR4_DIMM_2_DQS14_DN
	IO_DIFF_RX_3B2_DP_DQ32	J35	IO_DIFF_RX_3B14_DP_DQ36	W35	DDR4_DIMM_2_DQS14_DP
	IO_DIFF_TX_3B2_DN_DQS32_DN	F36	IO_DIFF_TX_3B14_DN_DQS36_DN	T36	DDR4_DIMM_2_DQS5_DN
	IO_DIFF_TX_3B2_DP_DQS32_DP	G35	IO_DIFF_TX_3B14_DP_DQS36_DP	U35	DDR4_DIMM_2_DQS5_DP
68 17	IO_CDR_DIFF_RX_3B3_DN_DQ32	K34	IO_CDR_DIFF_RX_3B15_DN_DQ36	Y34	DDR4_DIMM_2_DQ41
68 17	IO_CDR_DIFF_RX_3B3_DP_DQ32	J33	IO_CDR_DIFF_RX_3B15_DP_DQ36	W33	DDR4_DIMM_2_DQ40
	IO_DIFF_TX_3B3_DN_DQ32	F34	IO_DIFF_TX_3B15_DN_DQ36	T34	DDR4_DIMM_2_DQ43
	IO_DIFF_TX_3B3_DP_DQ32	G33	IO_DIFF_TX_3B15_DP_DQ36	U33	DDR4_DIMM_2_DQ42
		P38			
	IO_DIFF_RX_3B4_DN_DQ33	R37	IO_CDR_DIFF_RX_3B16_DN_DQ37	AD38	DDR4_DIMM_2_DQ52
	IO_DIFF_RX_3B4_DP_DQ33	M38	IO_CDR_DIFF_RX_3B16_DP_DQ37	AE37	DDR4_DIMM_2_DQ55
	IO_DIFF_TX_3B4_DN_DQ33	L37	IO_DIFF_TX_3B16_DN_DQ37	AB38	DDR4_DIMM_2_DQ54
	IO_DIFF_TX_3B4_DP_DQ33	P36	IO_DIFF_TX_3B16_DP_DQ37	AA37	DDR4_DIMM_2_DQ53
	IO_DIFF_RX_3B5_DN_DQ33	R35	IO_DIFF_RX_3B17_DN_DQ37	AD36	DDR4_DIMM_2_DQS15_DN
	IO_DIFF_RX_3B5_DP_DQ33	M36	IO_DIFF_RX_3B17_DP_DQ37	AE35	DDR4_DIMM_2_DQS15_DP
	IO_PLL_3B_T_CLKOUT1_DN_DIFF_TX_3B5_DN_DQS33_DN	L35	IO_PLL_3B_B_CLKOUT1_DN_DIFF_TX_3B17_DN_DQS37_DN	AB36	DDR4_DIMM_2_DQS6_DN
	IO_PLL_3B_T_CLKOUT1_DP_PLL_3B_T_CLKOUT1_PLL_3B_T_FB1_DIFF_TX_3B5_DP_DQS33_DP	P34	IO_PLL_3B_B_CLKOUT1_DP_PLL_3B_B_CLKOUT1_PLL_3B_B_FB1_DIFF_TX_3B17_DP_DQS37_DP	AA35	DDR4_DIMM_2_DQS6_DP
	IO_CDR_DIFF_RX_3B6_DN_DQ33	R33	IO_CDR_DIFF_RX_3B18_DN_DQ37	AD34	DDR4_DIMM_2_DQ48
	IO_RZQ_T_3B_CDR_DIFF_RX_3B6_DP_DQ33	M34	IO_RZQ_B_3B_CDR_DIFF_RX_3B18_DP_DQ37	AE33	DDR4_DIMM_2_DQ50
	IO_CLK_T_3B_DN1_DIFF_TX_3B6_DN_DQ33	L33	IO_CLK_B_3B_DN1_DIFF_TX_3B18_DN_DQ37	AB34	DDR4_DIMM_2_DQ51
	IO_CLK_T_3B_DP1_DIFF_TX_3B6_DP_DQ33		IO_CLK_B_3B_DP1_DIFF_TX_3B18_DP_DQ37	AA33	DDR4_DIMM_2_DQ49
		D32			
	IO_CLK_T_3B_DN0_DIFF_RX_3B7_DN_DQ34	E31	IO_CLK_B_3B_DN0_CDR_DIFF_RX_3B19_DN_DQ38	Y32	DDR4_DIMM_2_DQ61
	IO_CLK_T_3B_DP0_DIFF_RX_3B7_DP_DQ34	B32	IO_CLK_B_3B_DP0_CDR_DIFF_RX_3B19_DP_DQ38	W31	DDR4_DIMM_2_DQ63
	IO_DIFF_TX_3B7_DN_DQ34	A31	IO_DIFF_TX_3B19_DN_DQ38	T32	DDR4_DIMM_2_DQ62
	IO_DIFF_TX_3B7_DP_DQ34	D30	IO_DIFF_TX_3B19_DP_DQ38	U31	DDR4_DIMM_2_DQ60
	IO_PLL_3B_T_CLKOUT0_DN_DIFF_RX_3B8_DN_DQ34	E29	IO_PLL_3B_B_CLKOUT0_DN_DIFF_RX_3B20_DN_DQ38	Y30	DDR4_DIMM_2_DQS16_DN
	IO_PLL_3B_T_CLKOUT0_DP_PLL_3B_T_CLKOUT0_PLL_3B_T_FB0_DIFF_RX_3B8_DP_DQ34	B30	IO_PLL_3B_B_CLKOUT0_DP_PLL_3B_B_CLKOUT0_PLL_3B_B_FB0_DIFF_RX_3B20_DP_DQ38	W29	DDR4_DIMM_2_DQS16_DP
	IO_DIFF_TX_3B8_DN_DQS34_DN	A29	IO_DIFF_TX_3B20_DN_DQS38_DN	T30	DDR4_DIMM_2_DQS7_DN
	IO_DIFF_TX_3B8_DP_DQS34_DP	D28	IO_DIFF_TX_3B20_DP_DQS38_DP	U29	DDR4_DIMM_2_DQS7_DP
	IO_CDR_DIFF_RX_3B9_DN_DQ34	E27	IO_CDR_DIFF_RX_3B21_DN_DQ38	Y28	DDR4_DIMM_2_DQ58
	IO_CDR_DIFF_RX_3B9_DP_DQ34	B28	IO_CDR_DIFF_RX_3B21_DP_DQ38	W27	DDR4_DIMM_2_DQ59
	IO_DIFF_TX_3B9_DN_DQ34	A27	IO_DIFF_TX_3B21_DN_DQ38	T28	DDR4_DIMM_2_DQ57
	IO_DIFF_TX_3B9_DP_DQ34		IO_DIFF_TX_3B21_DP_DQ38	U27	DDR4_DIMM_2_DQ56
		K32			
	IO_DIFF_RX_3B10_DN_DQ35	J31	IO_CDR_DIFF_RX_3B22_DN_DQ39	AD32	DDR4_DIMM_2_DQ36
	IO_DIFF_RX_3B10_DP_DQ35	F32	IO_CDR_DIFF_RX_3B22_DP_DQ39	AE31	DDR4_DIMM_2_DQ39
	IO_DIFF_TX_3B10_DN_DQ35	G31	IO_DIFF_TX_3B22_DN_DQ39	AB32	DDR4_DIMM_2_DQ38
	IO_DIFF_TX_3B10_DP_DQ35	K30	IO_DIFF_TX_3B22_DP_DQ39	AA31	DDR4_DIMM_2_DQ37
	IO_DIFF_RX_3B11_DN_DQ35	J29	IO_DIFF_RX_3B23_DN_DQ39	AD30	DDR4_DIMM_2_DQS13_DN
	IO_DIFF_RX_3B11_DP_DQ35	F30	IO_DIFF_RX_3B23_DP_DQ39	AE29	DDR4_DIMM_2_DQS13_DP
	IO_DIFF_TX_3B11_DN_DQS35_DN	G29	IO_DIFF_TX_3B23_DN_DQS39_DN	AB30	DDR4_DIMM_2_DQS4_DN
	IO_DIFF_TX_3B11_DP_DQS35_DP	K28	IO_DIFF_TX_3B23_DP_DQS39_DP	AA29	DDR4_DIMM_2_DQS4_DP
	IO_CDR_DIFF_RX_3B12_DN_DQ35	J27	IO_CDR_DIFF_RX_3B24_DN_DQ39	AD28	DDR4_DIMM_2_DQ33
	IO_CDR_DIFF_RX_3B12_DP_DQ35	F28	IO_CDR_DIFF_RX_3B24_DP_DQ39	AE27	DDR4_DIMM_2_DQ34
	IO_DIFF_TX_3B12_DN_DQ35	G27	IO_DIFF_TX_3B24_DN_DQ39	AB28	DDR4_DIMM_2_DQ35
	IO_DIFF_TX_3B12_DP_DQ35		IO_DIFF_TX_3B24_DP_DQ39	AA27	DDR4_DIMM_2_DQ32

TOP BOT

IO BANK 3B
6 OF 31
99C1H7

48 IN PCA9535_0_1V2_INT_N
48 IN PCA9535_2_1V2_INT_N
40 BI SFP0_MOD3_1V2_SDA
40 OUT SFP0_MOD3_1V2_SCL
48 BI SFP1_MOD2_1V2_SDA
48 OUT SFP1_MOD2_1V2_SCL
68 17 IN CLK_100M_GPIO_4_DN
68 17 IN CLK_100M_GPIO_4_DP
62 IN FPGA_RESETn

40 BI SFP2_MOD1_1V2_SDA
40 OUT SFP2_MOD1_1V2_SCL
33 IN DDR4_DIMM_2_EVENTn_1V2
33 OUT DDR4_DIMM_2_SAVEn_1V2
40 BI SFP3_MOD0_1V2_SDA
40 OUT SFP3_MOD0_1V2_SCL

68 17 IN DDR_3_166.66M_REFCLK_DN
68 17 IN DDR_3_166.66M_REFCLK_DP

J33
SM
SCON
J85530-001

CLK_3B_DIFF_DN_SMA
CLK_3B_DIFF_DP_SMA

25V
0.1UF 1 2 C1223
0.1UF 1 2 C1224
25V

CLK_3B_DIFF_DN
CLK_3B_DIFF_DP

J32
SM
SCON
J85530-001

48 BI I2C_QSFP_3_1V2_SDA
48 IN I2C_QSFP_3_1V2_SCL
48 IN PCA9535_3_1V2_INT_N
48 43 IN QSFPDD1_RESET_L_1V2
33 IN DDR4_DIMM_2_SDA_1V2
33 BI DDR4_DIMM_2_SCL_1V2
48 43 OUT QSFPDD1_MODPRS_L_1V2
48 43 OUT QSFPDD1_LPMODE_1V2
48 43 IN QSFPDD1_INT_L_1V2

32 BI DDR4_DIMM_2_DQ68
32 BI DDR4_DIMM_2_DQ69
32 BI DDR4_DIMM_2_DQ70
32 BI DDR4_DIMM_2_DQ71
32 BI DDR4_DIMM_2_DQS17_DN
32 BI DDR4_DIMM_2_DQS17_DP
32 BI DDR4_DIMM_2_DQS8_DN
32 BI DDR4_DIMM_2_DQS8_DP
32 BI DDR4_DIMM_2_DQ65
32 BI DDR4_DIMM_2_DQ64
32 BI DDR4_DIMM_2_DQ66
32 BI DDR4_DIMM_2_DQ67

+P1V2_G3

R913 EMPTY 1K 1% 0.063W 0402
R923 EMPTY 1K 1% 0.063W 0402

68 17 DDR_3_166.66M_REFCLK_DN

CAD NOTE:
PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA

+P1V2_G3

R920 EMPTY 1K 1% 0.063W 0402
R940 EMPTY 1K 1% 0.063W 0402

DDR_3_166.66M_REFCLK_DP 17 68

CAD NOTE:
PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA

R166 A36092-043 100 1% 0.0625W EMPTY 0402

CLK_100M_GPIO_4_DP 17 68
CLK_100M_GPIO_4_DN 17 68

R999 A36092-043 100 1% 0.0625W EMPTY 0402

DDR_3_166.66M_REFCLK_DP 17 68
DDR_3_166.66M_REFCLK_DN 17 68

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DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation INTEL CORPORATION,BANGALORE INDIA, 560103	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET	17 OF 105

FPGA BANK 3A

BGA
U1
EMPTY

HC_FM91_3948BGA

32	OUT	DDR4_DIMM_2_CK1_DN	P46	IO_DIFF_RX_3A1_DN_DQ40			
32	OUT	DDR4_DIMM_2_CK1_DP	R45	IO_DIFF_RX_3A1_DP_DQ40			
48	OUT	QSFPDD800_MODSEL_L_1V2	M46	IO_DIFF_TX_3A1_DN_DQ40			
32	IN	DDR4_DIMM_2_ALERTN	L45	IO_DIFF_TX_3A1_DP_DQ40			
48	OUT	QSFP0_MOD_SEL_N_1V2	K46	IO_DIFF_RX_3A2_DN_DQ40			
48	OUT	QSFP1_MOD_SEL_N_1V2	J45	IO_DIFF_RX_3A2_DP_DQ40_AVST_READY			
48	OUT	QSFPDD0_MODSEL_L_1V2	F46	IO_DIFF_TX_3A2_DN_DQS40_DN_AVST_DATA31			
			G45	IO_DIFF_TX_3A2_DP_DQS40_DP_AVST_DATA30			
		1PPS_SMA_IN_FPGA_R	D46	IO_CDR_DIFF_RX_3A3_DN_DQ40_AVST_DATA29			
48	OUT	QSFPDD1_MODSEL_L_1V2	E45	IO_CDR_DIFF_RX_3A3_DP_DQ40_AVST_DATA28			
32	OUT	DDR4_DIMM_2_C1	B46	IO_DIFF_TX_3A3_DN_DQ40_AVST_DATA27			
32	OUT	DDR4_DIMM_2_C0	A45	IO_DIFF_TX_3A3_DP_DQ40_AVST_DATA26			
32	OUT	DDR4_DIMM_2_BG0	D44	IO_DIFF_RX_3A4_DN_DQ41_AVST_DATA25			
32	OUT	DDR4_DIMM_2_BA1	E43	IO_DIFF_RX_3A4_DP_DQ41_AVST_DATA24			
32	OUT	DDR4_DIMM_2_BA0	B44	IO_DIFF_TX_3A4_DN_DQ41_AVST_DATA23			
32	OUT	DDR4_DIMM_2_A17	A43	IO_DIFF_TX_3A4_DP_DQ41_AVST_DATA22			
32	OUT	DDR4_DIMM_2_A16	D42	IO_DIFF_RX_3A5_DN_DQ41_AVST_DATA21			
32	OUT	DDR4_DIMM_2_A15	E41	IO_DIFF_RX_3A5_DP_DQ41_AVST_DATA20			
32	OUT	DDR4_DIMM_2_A14	B42	IO_PLL_3A_T_CLKOUT1_DN_DIFF_TX_3A5_DN_DQS41_DN_AVST_DATA19			
32	OUT	DDR4_DIMM_2_A13	A41	IO_PLL_3A_T_CLKOUT1_DP_PLL_3A_T_CLKOUT1_PLL_3A_T_FB1_DIFF_TX_3A5_DP_DQS41_DP_AVST_DATA18			
32	OUT	DDR4_DIMM_2_A12	D40	IO_CDR_DIFF_RX_3A6_DN_DQ41_AVST_DATA17			
32	OUT	3A_RZQ	E39	IO_RZQ_T_3A_CDR_DIFF_RX_3A6_DP_DQ41_AVST_DATA16			
68 18	IN	DDR_4_166.66M_REFCLK_DN	B40	IO_CLK_T_3A_DN1_DIFF_TX_3A6_DN_DQ41			
68 18	IN	DDR_4_166.66M_REFCLK_DP	A39	IO_CLK_T_3A_DP1_DIFF_TX_3A6_DP_DQ41			
32	OUT	DDR4_DIMM_2_A11	K44	IO_CLK_T_3A_DN0_DIFF_RX_3A7_DN_DQ42			
32	OUT	DDR4_DIMM_2_A10	J43	IO_CLK_T_3A_DP0_DIFF_RX_3A7_DP_DQ42			
32	OUT	DDR4_DIMM_2_A9	F44	IO_DIFF_TX_3A7_DN_DQ42			
32	OUT	DDR4_DIMM_2_A8	G43	IO_DIFF_TX_3A7_DP_DQ42			
32	OUT	DDR4_DIMM_2_A7	K42	IO_PLL_3A_T_CLKOUT0_DN_DIFF_RX_3A8_DN_DQ42			
32	OUT	DDR4_DIMM_2_A6	J41	IO_PLL_3A_T_CLKOUT0_DP_PLL_3A_T_CLKOUT0_PLL_3A_T_FB0_DIFF_RX_3A8_DP_DQ42			
32	OUT	DDR4_DIMM_2_A5	F42	IO_DIFF_TX_3A8_DN_DQS42_DN_AVST_CLK			
32	OUT	DDR4_DIMM_2_A4	G41	IO_DIFF_TX_3A8_DP_DQS42_DP_AVST_DATA15			
32	OUT	DDR4_DIMM_2_A3	K40	IO_CDR_DIFF_RX_3A9_DN_DQ42_AVST_DATA14			
32	OUT	DDR4_DIMM_2_A2	J39	IO_CDR_DIFF_RX_3A9_DP_DQ42_AVST_DATA13			
32	OUT	DDR4_DIMM_2_A1	F40	IO_DIFF_TX_3A9_DN_DQ42_AVST_DATA12			
32	OUT	DDR4_DIMM_2_A0	G39	IO_DIFF_TX_3A9_DP_DQ42_AVST_DATA11			
32	OUT	DDR4_DIMM_2_PAR	D38	IO_DIFF_RX_3A10_DN_DQ43_AVST_DATA10			
32	OUT	DDR4_DIMM_2_CSN_B	E37	IO_DIFF_RX_3A10_DP_DQ43_AVST_DATA9			
32	OUT	DDR4_DIMM_2_CK0_DN	B38	IO_DIFF_TX_3A10_DN_DQ43_AVST_DATA8			
32	OUT	DDR4_DIMM_2_CK0_DP	A37	IO_DIFF_TX_3A10_DP_DQ43_AVST_VALID			
32	OUT	DDR4_DIMM_2_CKE_B	D36	IO_DIFF_RX_3A11_DN_DQ43_AVST_DATA7			
32	OUT	DDR4_DIMM_2_CKE0	E35	IO_DIFF_RX_3A11_DP_DQ43_AVST_DATA6			
32	OUT	DDR4_DIMM_2_ODT_B	B36	IO_DIFF_TX_3A11_DN_DQS43_DN_AVST_DATA5			
32	OUT	DDR4_DIMM_2_ODT0	A35	IO_DIFF_TX_3A11_DP_DQS43_DP_AVST_DATA4			
32	OUT	DDR4_DIMM_2_ACTN	D34	IO_CDR_DIFF_RX_3A12_DN_DQ43_AVST_DATA3			
32	OUT	DDR4_DIMM_2_CSN0	E33	IO_CDR_DIFF_RX_3A12_DP_DQ43_AVST_DATA2			
32	OUT	DDR4_DIMM_2_RSTN	B34	IO_DIFF_TX_3A12_DN_DQ43_AVST_DATA1			
32	OUT	DDR4_DIMM_2_BG1	A33	IO_DIFF_TX_3A12_DP_DQ43_AVST_DATA0			
				TOP	BOT		
				IO_CDR_DIFF_RX_3A13_DN_DQ44		AK46	DDR4_DIMM_2_DQ30 B1 32
				IO_CDR_DIFF_RX_3A13_DP_DQ44		AJ45	DDR4_DIMM_2_DQ31 B1 32
				IO_DIFF_TX_3A13_DN_DQ44		AF46	DDR4_DIMM_2_DQ29 B1 32
				IO_DIFF_TX_3A13_DP_DQ44		AG45	DDR4_DIMM_2_DQ28 B1 32
				IO_DIFF_RX_3A14_DN_DQ44		AD46	DDR4_DIMM_2_DQS12_DN B1 32
				IO_DIFF_RX_3A14_DP_DQ44		AE45	DDR4_DIMM_2_DQS12_DP B1 32
				IO_DIFF_TX_3A14_DN_DQS44_DN		AB46	DDR4_DIMM_2_DQS3_DN B1 32
				IO_DIFF_TX_3A14_DP_DQS44_DP		AA45	DDR4_DIMM_2_DQS3_DP B1 32
				IO_CDR_DIFF_RX_3A15_DN_DQ44		Y46	DDR4_DIMM_2_DQ27 B1 32
				IO_CDR_DIFF_RX_3A15_DP_DQ44		W45	DDR4_DIMM_2_DQ26 B1 32
				IO_DIFF_TX_3A15_DN_DQ44		T46	DDR4_DIMM_2_DQ25 B1 32
				IO_DIFF_TX_3A15_DP_DQ44		U45	DDR4_DIMM_2_DQ24 B1 32
				IO_CDR_DIFF_RX_3A16_DN_DQ45		AD44	DDR4_DIMM_2_DQ5 B1 32
				IO_CDR_DIFF_RX_3A16_DP_DQ45		AE43	DDR4_DIMM_2_DQ4 B1 32
				IO_DIFF_TX_3A16_DN_DQ45		AB44	DDR4_DIMM_2_DQ6 B1 32
				IO_DIFF_TX_3A16_DP_DQ45		AA43	DDR4_DIMM_2_DQ7 B1 32
				IO_DIFF_RX_3A17_DN_DQ45		AD42	DDR4_DIMM_2_DQS9_DN B1 32
				IO_DIFF_RX_3A17_DP_DQ45		AE41	DDR4_DIMM_2_DQS9_DP B1 32
				IO_PLL_3A_B_CLKOUT1_DN_DIFF_TX_3A17_DN_DQS45_DN		AB42	DDR4_DIMM_2_DQS0_DN B1 32
				IO_PLL_3A_B_CLKOUT1_DP_PLL_3A_B_CLKOUT1_PLL_3A_B_FB1_DIFF_TX_3A17_DP_DQS45_DP		AA41	DDR4_DIMM_2_DQS0_DP B1 32
				IO_CDR_DIFF_RX_3A18_DN_DQ45		AD40	DDR4_DIMM_2_DQ1 B1 32
				IO_RZQ_B_3A_CDR_DIFF_RX_3A18_DP_DQ45		AE39	DDR4_DIMM_2_DQ0 B1 32
				IO_CLK_B_3A_DN1_DIFF_TX_3A18_DN_DQ45		AB40	DDR4_DIMM_2_DQ3 B1 32
				IO_CLK_B_3A_DP1_DIFF_TX_3A18_DP_DQ45		AA39	DDR4_DIMM_2_DQ2 B1 32
				IO_CLK_B_3A_DN0_CDR_DIFF_RX_3A19_DN_DQ46		Y44	DDR4_DIMM_2_DQ15 B1 32
				IO_CLK_B_3A_DP0_CDR_DIFF_RX_3A19_DP_DQ46		W43	DDR4_DIMM_2_DQ14 B1 32
				IO_DIFF_TX_3A19_DN_DQ46		T44	DDR4_DIMM_2_DQ12 B1 32
				IO_DIFF_TX_3A19_DP_DQ46		U43	DDR4_DIMM_2_DQ13 B1 32
				IO_PLL_3A_B_CLKOUT0_DN_DIFF_RX_3A20_DN_DQ46		Y42	DDR4_DIMM_2_DQS10_DN B1 32
				IO_PLL_3A_B_CLKOUT0_DP_PLL_3A_B_CLKOUT0_PLL_3A_B_FB0_DIFF_RX_3A20_DP_DQ46		W41	DDR4_DIMM_2_DQS10_DP B1 32
				IO_DIFF_TX_3A20_DN_DQS46_DN		T42	DDR4_DIMM_2_DQS1_DN B1 32
				IO_DIFF_TX_3A20_DP_DQS46_DP		U41	DDR4_DIMM_2_DQS1_DP B1 32
				IO_CDR_DIFF_RX_3A21_DN_DQ46		Y40	DDR4_DIMM_2_DQ8 B1 32
				IO_CDR_DIFF_RX_3A21_DP_DQ46		W39	DDR4_DIMM_2_DQ9 B1 32
				IO_DIFF_TX_3A21_DN_DQ46		T40	DDR4_DIMM_2_DQ11 B1 32
				IO_DIFF_TX_3A21_DP_DQ46		U39	DDR4_DIMM_2_DQ10 B1 32
				IO_CDR_DIFF_RX_3A22_DN_DQ47		P44	DDR4_DIMM_2_DQ22 B1 32
				IO_CDR_DIFF_RX_3A22_DP_DQ47		R43	DDR4_DIMM_2_DQ23 B1 32
				IO_DIFF_TX_3A22_DN_DQ47		M44	DDR4_DIMM_2_DQ20 B1 32
				IO_DIFF_TX_3A22_DP_DQ47		L43	DDR4_DIMM_2_DQ21 B1 32
				IO_DIFF_RX_3A23_DN_DQ47		P42	DDR4_DIMM_2_DQS11_DN B1 32
				IO_DIFF_RX_3A23_DP_DQ47		R41	DDR4_DIMM_2_DQS11_DP B1 32
				IO_DIFF_TX_3A23_DN_DQS47_DN		M42	DDR4_DIMM_2_DQS2_DN B1 32
				IO_DIFF_TX_3A23_DP_DQS47_DP		L41	DDR4_DIMM_2_DQS2_DP B1 32
				IO_CDR_DIFF_RX_3A24_DN_DQ47		P40	DDR4_DIMM_2_DQ18 B1 32
				IO_CDR_DIFF_RX_3A24_DP_DQ47		R39	DDR4_DIMM_2_DQ17 B1 32
				IO_DIFF_TX_3A24_DN_DQ47		M40	DDR4_DIMM_2_DQ19 B1 32
				IO_DIFF_TX_3A24_DP_DQ47		L39	DDR4_DIMM_2_DQ16 B1 32

IO BANK 3A
7 OF 31
99C1H7

66 IN 1PPS_SMA_IN_FPGA_1V2 — R3258 0 1 2 RES — 1PPS_SMA_IN_FPGA_R

R2336 240 RES 1% 0.1W 0402 1 2 — 3A_RZQ

+P1V2_G3 — R914 EMPTY 1K 1% 0.063W 0402 1 2 — DDR_4_166.66M_REFCLK_DN 68 18
+P1V2_G3 — R921 EMPTY 1K 1% 0.063W 0402 1 2 — DDR_4_166.66M_REFCLK_DP 18 68
R934 EMPTY 1K 1% 0.063W 0402 1 2 — DDR_4_166.66M_REFCLK_DN
R941 EMPTY 1K 1% 0.063W 0402 1 2 — DDR_4_166.66M_REFCLK_DP

CAD NOTE:
PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA

R47 A36092-043 100 1% 0.0625W EMPTY 0402 1 2
DDR_4_166.66M_REFCLK_DP 18 68
DDR_4_166.66M_REFCLK_DN 18 68

Tue Sep 26 11:47:33 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	18 OF 105

FPGA BANK 13C

CAD NOTE:

PLACE THESE 100-OHM RES RIGHT BELOW FPGA BALLS ON THE BREAKOUT VIAS.

R1380 A36092-043 100 1% 0.0625W EMPTY 0402 — CLK_FHT_13C_156.25M_DP — CLK_FHT_13C_156.25M_DN
R1381 A36092-043 100 1% 0.0625W EMPTY 0402 — CLK_13C_FHT_DP — CLK_13C_FHT_DN
R1389 A36092-043 100 1% 0.0625W EMPTY 0402 — FMCB_ETH_REFCLK_156.25M_DP — FMCB_ETH_REFCLK_156.25M_DN
R1398 A36092-043 100 1% 0.0625W EMPTY 0402 — FMCB_CPRI_REFCLK_153.6M_DP — FMCB_CPRI_REFCLK_153.6M_DN
R1404 A36092-043 100 1% 0.0625W EMPTY 0402 — FMCB_CPRI_REFCLK_184.32M_DP — FMCB_CPRI_REFCLK_184.32M_DN
R2582 A36092-043 100 1% 0.0625W EMPTY 0402 — FMC_B_CLK_M2C_0_DP — FMC_B_CLK_M2C_0_DN
R2583 A36092-043 100 1% 0.0625W EMPTY 0402 — FMC_B_CLK_M2C_1_DP — FMC_B_CLK_M2C_1_DN
R2584 A36092-043 100 1% 0.0625W EMPTY 0402 — FMC_B_CLK_M2C_2_DP — FMC_B_CLK_M2C_2_DN
R2585 A36092-043 100 1% 0.0625W EMPTY 0402 — FMC_B_CLK_M2C_3_DP — FMC_B_CLK_M2C_3_DN
R1457 A36092-043 100 1% 0.0625W EMPTY 0402 — REFCLK_FGT_13C_8_DP — REFCLK_FGT_13C_8_DN
R1459 A36092-043 100 1% 0.0625W EMPTY 0402 — REFCLK_FGT_13C_9_DP — REFCLK_FGT_13C_9_DN

CAD NOTE:

PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS.
FMC_B_RX*

BGA
U1
EMPTY

HC_FM91_3948BGA

C1384 C1385 0.1UF 25V

CLK_SMP_13C_DN
CLK_SMP_13C_DP

J73 J85530-001 SCON SM
J74 J85530-001 SCON SM

SM EMPTY TP303

R1782 R263 RES 0.5% 0.0625W 0402

F-TILE BANK 13C
13 OF 31
99C1H7

CAD NOTE:

PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS

CAD NOTE:

Place RCOMP res right below FPGA balls on the breakout vias.

DESIGN NOTE:

Indicates BARAK_IS_USED

+P1V8_G2

R325 RES 499 0.1% 0.0625W 0402
R2197 RES 1.5K 0.1% 0.063W 0402
R2213 RES
R326 A93549-001 0 5% 0.0625W RES 0402
R330 A93549-034 10K 1% 0.0625W EMPTY 0402
R2008 A93549-034 10K 1% 0.0625W RES 0402
C2118 H61346-001 10NF 10% 50V EMPTY 0402

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DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	19 OF 105

FPGA BANK 13B

CAD NOTE:

PLACE THESE 100-OHM RES RIGHT BELOW FPGA BALLS ON THE BREAKOUT VIAS.

R1885 A36092-043 100 1% 0.0625W EMPTY 0402
CLK_FHT_13B_156.25M_DP
CLK_FHT_13B_156.25M_DN

R1813 A36092-043 100 1% 0.0625W EMPTY 0402
CLK_13B_FHT_DP
CLK_13B_FHT_DN

R1814 A36092-043 100 1% 0.0625W EMPTY 0402
REFCLK1_PCIE_100M_DP
REFCLK1_PCIE_100M_DN

R1815 A36092-043 100 1% 0.0625W EMPTY 0402
REFCLK2_PCIE_100M_DP
REFCLK2_PCIE_100M_DN

R1450 A36092-043 100 1% 0.0625W EMPTY 0402
CLK_PCIE_EP_MCIO1_DP
CLK_PCIE_EP_MCIO1_DN

R1451 A36092-043 100 1% 0.0625W EMPTY 0402
CLK_FGT_13B_156.25M_DP
CLK_FGT_13B_156.25M_DN

R1452 A36092-043 100 1% 0.0625W EMPTY 0402
CLK_FGT_13B_156.25M_SPARE_DP
CLK_FGT_13B_156.25M_SPARE_DN

C1306 0.1UF 25V CLK_13B_FHT_DN
C1307 0.1UF 25V CLK_13B_FHT_DP
156.25M
156.25M
CLK_SHP_13B_DN
CLK_SHP_13B_DP

J75 J85530-001 SCON SM
J76 J85530-001 SCON SM

BGA
U1
EMPTY
HC_FM91_3948BGA

OSFP_RX3_DN CL5
OSFP_RX3_DP CM6
OSFP_RX2_DN CR5
OSFP_RX2_DP CT6
OSFP_RX1_DN CY6
OSFP_RX1_DP CW5
OSFP_RX0_DN DD6
OSFP_RX0_DP DC5
CLK_FHT_13B_156.25M_DN CM10
CLK_FHT_13B_156.25M_DP CN9
CT10
CU9

PCIE_1_RX_0_DN AY6
PCIE_1_RX_0_DP AW5
PCIE_1_RX_1_DN BA3
PCIE_1_RX_1_DP BB2
PCIE_1_RX_2_DN BD6
PCIE_1_RX_2_DP BC5
PCIE_1_RX_3_DN BE3
PCIE_1_RX_3_DP BF2
REFCLK1_PCIE_100M_DN BL15
REFCLK1_PCIE_100M_DP BK16
REFCLK2_PCIE_100M_DN BM14
REFCLK2_PCIE_100M_DP BK14

R2267 0 RES FGT_13B_RX_CH0_DN BH6
R2268 0 RES FGT_13B_RX_CH0_DP BG5
R2269 0 RES FGT_13B_RX_CH1_DN BJ3
R2270 0 RES FGT_13B_RX_CH1_DP BK2
R2271 0 RES FGT_13B_RX_CH2_DN BM6
R2272 0 RES FGT_13B_RX_CH2_DP BL5
R2273 0 RES FGT_13B_RX_CH3_DN BN3
R2274 0 RES FGT_13B_RX_CH3_DP BP2

CLK_PCIE_EP_MCIO1_DN BP16
CLK_PCIE_EP_MCIO1_DP BT16
R2275 0 RES REFCLK_FGT_13B_CH3_DN BR15
R2276 0 RES REFCLK_FGT_13B_CH3_DP BT14

QSFPDD3_RX_7_DN BT6
QSFPDD3_RX_7_DP BR6
QSFPDD3_RX_6_DN BU3
QSFPDD3_RX_6_DP BV2
QSFPDD3_RX_5_DN BY6
QSFPDD3_RX_5_DP BW5
QSFPDD3_RX_4_DN CA3
QSFPDD3_RX_4_DP CB2
CLK_FGT_13B_156.25M_DN BU15
CLK_FGT_13B_156.25M_DP BV16
CLK_FGT_13B_156.25M_SPARE_DN CB14
CLK_FGT_13B_156.25M_SPARE_DP BY14
CB16
CA15

QSFPDD3_RX_3_DN CD6
QSFPDD3_RX_3_DP CC5
QSFPDD3_RX_2_DN CE3
QSFPDD3_RX_2_DP CF2
QSFPDD3_RX_1_DN CH6
QSFPDD3_RX_1_DP CG5
QSFPDD3_RX_0_DN CJ3
QSFPDD3_RX_0_DP CK2

R2277 0 RES REFCLK_FGT_13B_CH6_DN CC15
R2278 0 RES REFCLK_FGT_13B_CH6_DP CD14
R2279 0 RES REFCLK_FGT_13B_CH7_DN CF16
R2280 0 RES REFCLK_FGT_13B_CH7_DP CH16
CH14
CG15

FM_GXF_13B_PERST_N R1784 0 RES FM_GXF_13B_PERST_N_R AH18
SM EMPTY TP87 FM_GXF_13B_IO_PLL R1232 0 RES FM_GXF_13B_IO_PLL_R AB20

TP_13B_GDR_IO_JTAG_TDO_DFX AG19
TP_13B_GDR_I_JTAG_TDI_DFX AJ19
TP_13B_GDR_APROBE_0_ATB AH20
TP_13B_GDR_APROBE_1_ATB AG21
TP_13B_GXF_APROBE1 CW11
TP_13B_GXF_APROBE2 CY10
TP_13B_GXF_APROBE_Q0_CH3_FGT BN15
TP_13B_GXF_APROBE_Q2_CH3_FGT BP14
TP_13B_GXF_APROBE_Q3_CH3_FGT CF14
TP_13B_GXF_APROBE2_Q3_CH3_FGT CE15

TEMPDIODE_13B_GXF_DN CP12
TEMPDIODE_13B_GXF_DP CM12
V20

F-TILE BANK 13B
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99C1H7

FHTR13B_RX_CH0_DN
FHTR13B_RX_CH0_DP
FHTR13B_RX_CH1_DN
FHTR13B_RX_CH1_DP
FHTR13B_RX_CH2_DN
FHTR13B_RX_CH2_DP
FHTR13B_RX_CH3_DN
FHTR13B_RX_CH3_DP
REFCLK_FHTR13B_CH0_DN
REFCLK_FHTR13B_CH0_DP
REFCLK_FHTR13B_CH1_DN
REFCLK_FHTR13B_CH1_DP

FGTR13B_RX_Q0_CH0_DN
FGTR13B_RX_Q0_CH0_DP
FGTR13B_RX_Q0_CH1_DN
FGTR13B_RX_Q0_CH1_DP
FGTR13B_RX_Q0_CH2_DN
FGTR13B_RX_Q0_CH2_DP
FGTR13B_RX_Q0_CH3_DN
FGTR13B_RX_Q0_CH3_DP
REFCLK_FGTR13B_Q0_RX_CH0_DN
REFCLK_FGTR13B_Q0_RX_CH0_DP
REFCLK_FGTR13B_Q0_RX_CH1_DN
REFCLK_FGTR13B_Q0_RX_CH1_DP

FGTR13B_RX_Q1_CH0_DN
FGTR13B_RX_Q1_CH0_DP
FGTR13B_RX_Q1_CH1_DN
FGTR13B_RX_Q1_CH1_DP
FGTR13B_RX_Q1_CH2_DN
FGTR13B_RX_Q1_CH2_DP
FGTR13B_RX_Q1_CH3_DN
FGTR13B_RX_Q1_CH3_DP
REFCLK_FGTR13B_Q1_RX_CH2_DN
REFCLK_FGTR13B_Q1_RX_CH2_DP
REFCLK_FGTR13B_Q1_RX_CH3_DN
REFCLK_FGTR13B_Q1_RX_CH3_DP

FGTR13B_RX_Q2_CH0_DN
FGTR13B_RX_Q2_CH0_DP
FGTR13B_RX_Q2_CH1_DN
FGTR13B_RX_Q2_CH1_DP
FGTR13B_RX_Q2_CH2_DN
FGTR13B_RX_Q2_CH2_DP
FGTR13B_RX_Q2_CH3_DN
FGTR13B_RX_Q2_CH3_DP
REFCLK_FGTR13B_Q2_RX_CH4_DN
REFCLK_FGTR13B_Q2_RX_CH4_DP
REFCLK_FGTR13B_Q2_RX_CH5_DN
REFCLK_FGTR13B_Q2_RX_CH5_DP
REFCLK_FGTR13B_Q2_CH8_DN
REFCLK_FGTR13B_Q2_CH8_DP

FGTR13B_RX_Q3_CH0_DN
FGTR13B_RX_Q3_CH0_DP
FGTR13B_RX_Q3_CH1_DN
FGTR13B_RX_Q3_CH1_DP
FGTR13B_RX_Q3_CH2_DN
FGTR13B_RX_Q3_CH2_DP
FGTR13B_RX_Q3_CH3_DN
FGTR13B_RX_Q3_CH3_DP
REFCLK_FGTR13B_Q3_RX_CH6_DN
REFCLK_FGTR13B_Q3_RX_CH6_DP
REFCLK_FGTR13B_Q3_RX_CH7_DN
REFCLK_FGTR13B_Q3_RX_CH7_DP
REFCLK_FGTR13B_Q3_CH9_DN
REFCLK_FGTR13B_Q3_CH9_DP

I_PIN_PERST_N_13B_GXF
U21_GDR_IO_PLL_REFCLK_DNU
DNU_U21_GDR_O_JTAG_TDO_DFX
DNU_U21_GDR_I_JTAG_TDI_DFX
DNU_U21_GDR_APROBE_0_ATB
DNU_U21_GDR_APROBE_1_ATB
APROBE1_GXF_FHT13B
APROBE2_GXF_FHT13B
APROBE_GXF_FGT13B_Q0_CH3
APROBE_GXF_FGT13B_Q2_CH3
APROBE_GXF_FGT13B_Q3_CH3
APROBE2_GXF_FGT13B_Q3_CH3
TEMPDIODE5_DN_U21_GDR_O_SENS_THERM
TEMPDIODE5_DP_U21_GDR_I_SENS_THERM
GND_U21_GDR_I_EDM_IN

RCOMP_DN_Q2_CH1_FGT_13B_GXF
RCOMP_DP_Q2_CH1_FGT_13B_GXF
RCOMP_DN_FHT_13B_GXF
RCOMP_DP_FHT_13B_GXF
ENB_GXF_FHT13B

FGTR13B_TX_Q0_CH0_DN
FGTR13B_TX_Q0_CH0_DP
FGTR13B_TX_Q0_CH1_DN
FGTR13B_TX_Q0_CH1_DP
FGTR13B_TX_Q0_CH2_DN
FGTR13B_TX_Q0_CH2_DP
FGTR13B_TX_Q0_CH3_DN
FGTR13B_TX_Q0_CH3_DP

FGTR13B_TX_Q1_CH0_DN
FGTR13B_TX_Q1_CH0_DP
FGTR13B_TX_Q1_CH1_DN
FGTR13B_TX_Q1_CH1_DP
FGTR13B_TX_Q1_CH2_DN
FGTR13B_TX_Q1_CH2_DP
FGTR13B_TX_Q1_CH3_DN
FGTR13B_TX_Q1_CH3_DP

FGTR13B_TX_Q2_CH0_DN
FGTR13B_TX_Q2_CH0_DP
FGTR13B_TX_Q2_CH1_DN
FGTR13B_TX_Q2_CH1_DP
FGTR13B_TX_Q2_CH2_DN
FGTR13B_TX_Q2_CH2_DP
FGTR13B_TX_Q2_CH3_DN
FGTR13B_TX_Q2_CH3_DP

FGTR13B_TX_Q3_CH0_DN
FGTR13B_TX_Q3_CH0_DP
FGTR13B_TX_Q3_CH1_DN
FGTR13B_TX_Q3_CH1_DP
FGTR13B_TX_Q3_CH2_DN
FGTR13B_TX_Q3_CH2_DP
FGTR13B_TX_Q3_CH3_DN
FGTR13B_TX_Q3_CH3_DP

CP2 OSFP_TX3_DN
CN3 OSFP_TX3_DP
CV2 OSFP_TX2_DN
CU3 OSFP_TX2_DP
DA3 OSFP_TX1_DN
DB2 OSFP_TX1_DP
DE3 OSFP_TX0_DN
DF2 OSFP_TX0_DP

AY12 PCIE_1_TX_0_DN
AW11 PCIE_1_TX_0_DP
BA9 PCIE_1_TX_1_DN
BB8 PCIE_1_TX_1_DP
BD12 PCIE_1_TX_2_DN
BC11 PCIE_1_TX_2_DP
BE9 PCIE_1_TX_3_DN
BF8 PCIE_1_TX_3_DP

BH12
BG11
BJ9
BK8
BM12
BL11
BN9
BP8

BT12 QSFPDD3_TX_7_DN
BR11 QSFPDD3_TX_7_DP
BU9 QSFPDD3_TX_6_DN
BV8 QSFPDD3_TX_6_DP
BY12 QSFPDD3_TX_5_DN
BW11 QSFPDD3_TX_5_DP
CA9 QSFPDD3_TX_4_DN
CB8 QSFPDD3_TX_4_DP

CD12 QSFPDD3_TX_3_DN
CC11 QSFPDD3_TX_3_DP
CE9 QSFPDD3_TX_2_DN
CF8 QSFPDD3_TX_2_DP
CH12 QSFPDD3_TX_1_DN
CG11 QSFPDD3_TX_1_DP
CJ9 QSFPDD3_TX_0_DN
CK8 QSFPDD3_TX_0_DP

BW15 GXF_13B_FGT_RCOMP_0_DN
BY16 GXF_13B_FGT_RCOMP_0_DP
DB10 GXF_13B_FHT_RCOMP_0_DN
DA9 GXF_13B_FHT_RCOMP_0_DP
AE19 U21_GXF_IO_DFX_0

R2191 RES 499 0.1% 0.0625W 0402
R2200 RES 1.5K 0.1% 0.063W 0402

CAD NOTE:
Place RCOMP res right below FPGA balls on the breakout vias.

CAD NOTE:
PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS

DESIGN NOTE:
Indicates BARAK_IS_USED

+P1V8_G2
R2194 A93549-001 0 5% 0.0625W RES 0402
R2195 A93548-034 10K 1% 0.0625W EMPTY 0402

+P1V8_G2
R1788 A93548-034 10K 1% 0.0625W RES 0402
FM_GXF_13B_PERST_N
C3052 H61346-001 10NF 10% 50V EMPTY 0402

Tue Sep 26 11:47:35 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SCALE:	DO NOT SCALE DRAWING	SHEET	20 OF 105

INTEL AGILEX® 7 FPGA I-SERIES (6x F-TILE) - F-TILE 13B/U21

FPGA BANK 13A

CAD NOTE:

PLACE THESE 100-OHM RES RIGHT BELOW FPGA BALLS
ON THE BREAKOUT VIAS.

R311 A36092-043 100 1% 0.0625W EMPTY 0402
CLK_FGT_13A_156.25M_DP — 21 69
CLK_FGT_13A_156.25M_DN — 21 69

R312 A36092-043 100 1% 0.0625W EMPTY 0402
CLK_FGT_13A_156.25M_SPARE_DP — 21 69
CLK_FGT_13A_156.25M_SPARE_DN — 21 69

BGA
U1
EMPTY
HC_FM91_3948BGA

0	R2214	RES	FHT_13A_RX_CH0_DN	EG15	FHTR13A_RX_CH0_DN	FHTR13A_TX_CH0_DN	EN15
0	R2215	RES	FHT_13A_RX_CH0_DP	EE15	FHTR13A_RX_CH0_DP	FHTR13A_TX_CH0_DP	EL15
0	R2216	RES	FHT_13A_RX_CH1_DN	EJ17	FHTR13A_RX_CH1_DN	FHTR13A_TX_CH1_DN	ER17
0	R2217	RES	FHT_13A_RX_CH1_DP	EG17	FHTR13A_RX_CH1_DP	FHTR13A_TX_CH1_DP	EN17
0	R2218	RES	FHT_13A_RX_CH2_DN	EE19	FHTR13A_RX_CH2_DN	FHTR13A_TX_CH2_DN	EL19
0	R2219	RES	FHT_13A_RX_CH2_DP	EG19	FHTR13A_RX_CH2_DP	FHTR13A_TX_CH2_DP	EN19
0	R2220	RES	FHT_13A_RX_CH3_DN	EG21	FHTR13A_RX_CH3_DN	FHTR13A_TX_CH3_DN	EN21
0	R2221	RES	FHT_13A_RX_CH3_DP	EJ21	FHTR13A_RX_CH3_DP	FHTR13A_TX_CH3_DP	ER21
0	R2222	RES	REFCLK_FHT_13A_CH0_DN	EA21	REFCLK_FHTR13A_CH0_DN		
0	R2223	RES	REFCLK_FHT_13A_CH0_DP	EC21	REFCLK_FHTR13A_CH0_DP		
0	R2224	RES	REFCLK_FHT_13A_CH1_DN	EA17	REFCLK_FHTR13A_CH1_DN		
0	R2225	RES	REFCLK_FHT_13A_CH1_DP	EC17	REFCLK_FHTR13A_CH1_DP		
0	R2230	RES	FGT_13A_RX_CH0_DN	DH6	FGTR13A_RX_Q0_CH0_DN	FGTR13A_TX_Q0_CH0_DN	DE9
0	R2231	RES	FGT_13A_RX_CH0_DP	DG5	FGTR13A_RX_Q0_CH0_DP	FGTR13A_TX_Q0_CH0_DP	DF8
0	R2232	RES	FGT_13A_RX_CH1_DN	DJ3	FGTR13A_RX_Q0_CH1_DN	FGTR13A_TX_Q0_CH1_DN	DH12
0	R2233	RES	FGT_13A_RX_CH1_DP	DK2	FGTR13A_RX_Q0_CH1_DP	FGTR13A_TX_Q0_CH1_DP	DG11
0	R2234	RES	FGT_13A_RX_CH2_DN	DM6	FGTR13A_RX_Q0_CH2_DN	FGTR13A_TX_Q0_CH2_DN	DJ9
0	R2235	RES	FGT_13A_RX_CH2_DP	DL5	FGTR13A_RX_Q0_CH2_DP	FGTR13A_TX_Q0_CH2_DP	DK8
0	R2236	RES	FGT_13A_RX_CH3_DN	DN3	FGTR13A_RX_Q0_CH3_DN	FGTR13A_TX_Q0_CH3_DN	DM12
0	R2237	RES	FGT_13A_RX_CH3_DP	DP2	FGTR13A_RX_Q0_CH3_DP	FGTR13A_TX_Q0_CH3_DP	DL11
0	R2226	RES	REFCLK_FGT_13A_CH0_DN	CJ15	REFCLK_FGTR13A_Q0_RX_CH0_DN		
0	R2227	RES	REFCLK_FGT_13A_CH0_DP	CK16	REFCLK_FGTR13A_Q0_RX_CH0_DP		
0	R2228	RES	REFCLK_FGT_13A_CH1_DN	CP14	REFCLK_FGTR13A_Q0_RX_CH1_DN		
0	R2229	RES	REFCLK_FGT_13A_CH1_DP	CM14	REFCLK_FGTR13A_Q0_RX_CH1_DP		

38 IN	QSFP2_RX_3_DN	DT6	FGTR13A_RX_Q1_CH0_DN				
38 IN	QSFP2_RX_3_DP	DR5	FGTR13A_RX_Q1_CH0_DP				
38 IN	QSFP2_RX_2_DN	DU3	FGTR13A_RX_Q1_CH1_DN	FGTR13A_TX_Q1_CH0_DN	DN9	QSFP2_TX_3_DN	OUT 38
38 IN	QSFP2_RX_2_DP	DV2	FGTR13A_RX_Q1_CH1_DP	FGTR13A_TX_Q1_CH0_DP	DP8	QSFP2_TX_3_DP	OUT 38
38 IN	QSFP2_RX_1_DN	DY6	FGTR13A_RX_Q1_CH2_DN	FGTR13A_TX_Q1_CH1_DN	DT12	QSFP2_TX_2_DN	OUT 38
38 IN	QSFP2_RX_1_DP	DW5	FGTR13A_RX_Q1_CH2_DP	FGTR13A_TX_Q1_CH1_DP	DR11	QSFP2_TX_2_DP	OUT 38
38 IN	QSFP2_RX_0_DN	EA3	FGTR13A_RX_Q1_CH3_DN	FGTR13A_TX_Q1_CH2_DN	DU9	QSFP2_TX_1_DN	OUT 38
38 IN	QSFP2_RX_0_DP	EB2	FGTR13A_RX_Q1_CH3_DP	FGTR13A_TX_Q1_CH2_DP	DV8	QSFP2_TX_1_DP	OUT 38
				FGTR13A_TX_Q1_CH3_DN	DY12	QSFP2_TX_0_DN	OUT 38
69 21 IN	CLK_FGT_13A_156.25M_DN	CN15	REFCLK_FGTR13A_Q1_RX_CH2_DN	FGTR13A_TX_Q1_CH3_DP	DW11	QSFP2_TX_0_DP	OUT 38
69 21 IN	CLK_FGT_13A_156.25M_DP	CP16	REFCLK_FGTR13A_Q1_RX_CH2_DP				
69 21 IN	CLK_FGT_13A_156.25M_SPARE_DN	CT14	REFCLK_FGTR13A_Q1_RX_CH3_DN				
69 21 IN	CLK_FGT_13A_156.25M_SPARE_DP	CR15	REFCLK_FGTR13A_Q1_RX_CH3_DP				

44 IN	QSFPDD2_RX_7_DN	ED6	FGTR13A_RX_Q2_CH0_DN				
44 IN	QSFPDD2_RX_7_DP	EC5	FGTR13A_RX_Q2_CH0_DP				
44 IN	QSFPDD2_RX_6_DN	EE3	FGTR13A_RX_Q2_CH1_DN				
44 IN	QSFPDD2_RX_6_DP	EF2	FGTR13A_RX_Q2_CH1_DP	FGTR13A_TX_Q2_CH0_DN	EA9	QSFPDD2_TX_7_DN	OUT 44
44 IN	QSFPDD2_RX_5_DN	EH6	FGTR13A_RX_Q2_CH2_DN	FGTR13A_TX_Q2_CH0_DP	EB8	QSFPDD2_TX_7_DP	OUT 44
44 IN	QSFPDD2_RX_5_DP	EG5	FGTR13A_RX_Q2_CH2_DP	FGTR13A_TX_Q2_CH1_DN	ED12	QSFPDD2_TX_6_DN	OUT 44
44 IN	QSFPDD2_RX_4_DN	EJ3	FGTR13A_RX_Q2_CH3_DN	FGTR13A_TX_Q2_CH1_DP	EC11	QSFPDD2_TX_6_DP	OUT 44
44 IN	QSFPDD2_RX_4_DP	EK2	FGTR13A_RX_Q2_CH3_DP	FGTR13A_TX_Q2_CH2_DN	EE9	QSFPDD2_TX_5_DN	OUT 44
				FGTR13A_TX_Q2_CH2_DP	EF8	QSFPDD2_TX_5_DP	OUT 44
0 R2238	RES REFCLK_FGT_13A_CH4_DN	CY14	REFCLK_FGTR13A_Q2_RX_CH4_DN	FGTR13A_TX_Q2_CH3_DN	EH12	QSFPDD2_TX_4_DN	OUT 44
0 R2239	RES REFCLK_FGT_13A_CH4_DP	CW15	REFCLK_FGTR13A_Q2_RX_CH4_DP	FGTR13A_TX_Q2_CH3_DP	EG11	QSFPDD2_TX_4_DP	OUT 44
0 R2240	RES REFCLK_FGT_13A_CH5_DN	CY16	REFCLK_FGTR13A_Q2_RX_CH5_DN				
0 R2241	RES REFCLK_FGT_13A_CH5_DP	CV16	REFCLK_FGTR13A_Q2_RX_CH5_DP				
0 R12	RES REFCLK_FGT_13A_CH8_DN	DB16	REFCLK_FGTR13A_Q2_CH8_DN				
0 R152	RES REFCLK_FGT_13A_CH8_DP	DA15	REFCLK_FGTR13A_Q2_CH8_DP				

44 IN	QSFPDD2_RX_3_DN	EM6	FGTR13A_RX_Q3_CH0_DN				
44 IN	QSFPDD2_RX_3_DP	EL5	FGTR13A_RX_Q3_CH0_DP				
44 IN	QSFPDD2_RX_2_DN	EN3	FGTR13A_RX_Q3_CH1_DN				
44 IN	QSFPDD2_RX_2_DP	EP2	FGTR13A_RX_Q3_CH1_DP				
44 IN	QSFPDD2_RX_1_DN	ET6	FGTR13A_RX_Q3_CH2_DN	FGTR13A_TX_Q3_CH0_DN	EJ9	QSFPDD2_TX_3_DN	OUT 44
44 IN	QSFPDD2_RX_1_DP	ER5	FGTR13A_RX_Q3_CH2_DP	FGTR13A_TX_Q3_CH0_DP	EK8	QSFPDD2_TX_3_DP	OUT 44
44 IN	QSFPDD2_RX_0_DN	EU9	FGTR13A_RX_Q3_CH3_DN	FGTR13A_TX_Q3_CH1_DN	EM12	QSFPDD2_TX_2_DN	OUT 44
44 IN	QSFPDD2_RX_0_DP	EV8	FGTR13A_RX_Q3_CH3_DP	FGTR13A_TX_Q3_CH1_DP	EL11	QSFPDD2_TX_2_DP	OUT 44
				FGTR13A_TX_Q3_CH2_DN	EN9	QSFPDD2_TX_1_DN	OUT 44
0 R2242	RES REFCLK_FGT_13A_CH6_DN	DD14	REFCLK_FGTR13A_Q3_RX_CH6_DN	FGTR13A_TX_Q3_CH2_DP	EP8	QSFPDD2_TX_1_DP	OUT 44
0 R2243	RES REFCLK_FGT_13A_CH6_DP	DF14	REFCLK_FGTR13A_Q3_RX_CH6_DP	FGTR13A_TX_Q3_CH3_DN	ET12	QSFPDD2_TX_0_DN	OUT 44
0 R2244	RES REFCLK_FGT_13A_CH7_DN	DF16	REFCLK_FGTR13A_Q3_RX_CH7_DN	FGTR13A_TX_Q3_CH3_DP	ER11	QSFPDD2_TX_0_DP	OUT 44
0 R2245	RES REFCLK_FGT_13A_CH7_DP	DE15	REFCLK_FGTR13A_Q3_RX_CH7_DP				
0 R151	RES REFCLK_FGT_13A_CH9_DN	DG15	REFCLK_FGTR13A_Q3_CH9_DN				
0 R153	RES REFCLK_FGT_13A_CH9_DP	DH14	REFCLK_FGTR13A_Q3_CH9_DP				

61 21 IN FM_GXF_13A_SPARE_N R1705 1 2 RES 0.5% 0.0625W 0402 FM_GXF_13A_SPARE_N_R — DP16
SM EMPTY 1 TP304 CLK_13A_IO_PLL R1706 1 2 RES 0.5% 0.0625W 0402 CLK_13A_IO_PLL_R — DP14

I_PIN_PERST_N_13A_GXF
U20_GDR_IO_PLL_REFCLK_DNU
DNU_U20_GDR_I_JTAG_TDI_DFX
DNU_U20_GDR_O_JTAG_TDO_DFX
DNU_U20_GDR_APROBE_0_ATB
DNU_U20_GDR_APROBE_1_ATB
APROBE1_GXF_FHT13A
APROBE2_GXF_FHT13A
APROBE_GXF_FGT13A_Q0_CH3
APROBE_GXF_FGT13A_Q2_CH3
APROBE_GXF_FGT13A_Q3_CH3
APROBE2_GXF_FGT13A_Q3_CH3
TEMPDIODE4_DN_U20_GDR_O_SENS_THERM
TEMPDIODE4_DP_U20_GDR_I_SENS_THERM
GND_U20_GDR_I_EDM_IN

RCOMP_DN_Q2_CH1_FGT_13A_GXF
RCOMP_DP_Q2_CH1_FGT_13A_GXF
RCOMP_DN_FHT_13A_GXF
RCOMP_DP_FHT_13A_GXF
ENB_GXF_FHT13A

DB14	GXF_13A_FGT_RCOMP_0_DN	R2189 RES 499 0.1% 0.0625W 0402	
DC15	GXF_13A_FGT_RCOMP_0_DP		
DR19	GXF_13A_FHT_RCOMP_0_DN	R2198 RES 1.5K 0.1% 0.063W 0402	
DT18	GXF_13A_FHT_RCOMP_0_DP		
DU15	ENB_GXF_FHT_13A	0 R2246 RES	

CAD NOTE:
Place RCOMP res right below FPGA balls on the breakout vias.

F-TILE BANK 13A
11 OF 31
99C1H7

CAD NOTE:
PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS

+P1V8_G2
R2099 A93548-034 10K 1% 0.0625W RES 0402
61 21 IN FM_GXF_13A_SPARE_N
C2119 H61346-001 10NF 10% 50V EMPTY 0402

Tue Sep 26 11:47:35 2023

INTEL AGILEX® 7 FPGA I-SERIES (6x F-TILE) - F-TILE 13A/U20

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	21 OF 105

FPGA BANK 12C

BGA
U1
EMPTY

HC_FM91_3948BGA

46 IN	QSFPDD800_RX_7_DN	N55	FHTL12C_RX_CH0_DN	FHTL12C_TX_CH0_DN	G55 QSFPDD800_TX_7_DN OUT 46
46 IN	QSFPDD800_RX_7_DP	R55	FHTL12C_RX_CH0_DP	FHTL12C_TX_CH0_DP	J55 QSFPDD800_TX_7_DP OUT 46
46 IN	QSFPDD800_RX_6_DN	L53	FHTL12C_RX_CH1_DN	FHTL12C_TX_CH1_DN	E53 QSFPDD800_TX_6_DN OUT 46
46 IN	QSFPDD800_RX_6_DP	N53	FHTL12C_RX_CH1_DP	FHTL12C_TX_CH1_DP	G53 QSFPDD800_TX_6_DP OUT 46
46 IN	QSFPDD800_RX_5_DN	R51	FHTL12C_RX_CH2_DN	FHTL12C_TX_CH2_DN	J51 QSFPDD800_TX_5_DN OUT 46
46 IN	QSFPDD800_RX_5_DP	N51	FHTL12C_RX_CH2_DP	FHTL12C_TX_CH2_DP	G51 QSFPDD800_TX_5_DP OUT 46
46 IN	QSFPDD800_RX_4_DN	N49	FHTL12C_RX_CH3_DN	FHTL12C_TX_CH3_DN	G49 QSFPDD800_TX_4_DN OUT 46
46 IN	QSFPDD800_RX_4_DP	L49	FHTL12C_RX_CH3_DP	FHTL12C_TX_CH3_DP	E49 QSFPDD800_TX_4_DP OUT 46

CAD NOTE:
PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS

C471 1 2 0.1UF 25V 22 CLK_12C_FHT_DN
C477 1 2 0.1UF 25V 22 CLK_12C_FHT_DP

70 22 IN	CLK_FHT_12C_156.25M_DN	W49	REFCLK_FHTL12C_CH0_DN	
70 22 IN	CLK_FHT_12C_156.25M_DP	U49	REFCLK_FHTL12C_CH0_DP	
		W53	REFCLK_FHTL12C_CH1_DN	
		U53	REFCLK_FHTL12C_CH1_DP	

37 IN	QSFP1_RX_3_DN	AM64	FGTL12C_RX_Q0_CH0_DN	FGTL12C_TX_Q0_CH0_DN	AR61 QSFP1_TX_3_DN OUT 37
37 IN	QSFP1_RX_3_DP	AN65	FGTL12C_RX_Q0_CH0_DP	FGTL12C_TX_Q0_CH0_DP	AP62 QSFP1_TX_3_DP OUT 37
37 IN	QSFP1_RX_2_DN	AL67	FGTL12C_RX_Q0_CH1_DN	FGTL12C_TX_Q0_CH1_DN	AM58 QSFP1_TX_2_DN OUT 37
37 IN	QSFP1_RX_2_DP	AK68	FGTL12C_RX_Q0_CH1_DP	FGTL12C_TX_Q0_CH1_DP	AN59 QSFP1_TX_2_DP OUT 37
37 IN	QSFP1_RX_1_DN	AH64	FGTL12C_RX_Q0_CH2_DN	FGTL12C_TX_Q0_CH2_DN	AL61 QSFP1_TX_1_DN OUT 37
37 IN	QSFP1_RX_1_DP	AJ65	FGTL12C_RX_Q0_CH2_DP	FGTL12C_TX_Q0_CH2_DP	AK62 QSFP1_TX_1_DP OUT 37
37 IN	QSFP1_RX_0_DN	AG67	FGTL12C_RX_Q0_CH3_DN	FGTL12C_TX_Q0_CH3_DN	AH58 QSFP1_TX_0_DN OUT 37
37 IN	QSFP1_RX_0_DP	AF68	FGTL12C_RX_Q0_CH3_DP	FGTL12C_TX_Q0_CH3_DP	AJ59 QSFP1_TX_0_DP OUT 37

0 R2281 1 2 RES	REFCLK_FGT_12C_CH0_DN	BL55	REFCLK_FGTL12C_Q0_RX_CH0_DN	
0 R2282 1 2 RES	REFCLK_FGT_12C_CH0_DP	BK54	REFCLK_FGTL12C_Q0_RX_CH0_DP	
0 R2283 1 2 RES	REFCLK_FGT_12C_CH1_DN	BF56	REFCLK_FGTL12C_Q0_RX_CH1_DN	
0 R2284 1 2 RES	REFCLK_FGT_12C_CH1_DP	BH56	REFCLK_FGTL12C_Q0_RX_CH1_DP	

40 IN	SFP3_RX_DN	AD64	FGTL12C_RX_Q1_CH0_DN	FGTL12C_TX_Q1_CH0_DN	AG61 SFP3_TX_DN OUT 40
40 IN	SFP3_RX_DP	AE65	FGTL12C_RX_Q1_CH0_DP	FGTL12C_TX_Q1_CH0_DP	AF62 SFP3_TX_DP OUT 40
40 IN	SFP2_RX_DP	AC67	FGTL12C_RX_Q1_CH1_DN	FGTL12C_TX_Q1_CH1_DN	AD58 SFP2_TX_DP OUT 40
40 IN	SFP2_RX_DN	AB68	FGTL12C_RX_Q1_CH1_DP	FGTL12C_TX_Q1_CH1_DP	AE59 SFP2_TX_DN OUT 40
40 IN	SFP1_RX_DN	Y64	FGTL12C_RX_Q1_CH2_DN	FGTL12C_TX_Q1_CH2_DN	AC61 SFP1_TX_DN OUT 40
40 IN	SFP1_RX_DP	AA65	FGTL12C_RX_Q1_CH2_DP	FGTL12C_TX_Q1_CH2_DP	AB62 SFP1_TX_DP OUT 40
40 IN	SFP0_RX_DN	W67	FGTL12C_RX_Q1_CH3_DN	FGTL12C_TX_Q1_CH3_DN	Y58 SFP0_TX_DN OUT 40
40 IN	SFP0_RX_DP	V68	FGTL12C_RX_Q1_CH3_DP	FGTL12C_TX_Q1_CH3_DP	AA59 SFP0_TX_DP OUT 40

DESIGN NOTE:
SFP2_TX/RX_DN/DP SIGNALS SWAPPED AS PER SI FEEDBACK FOR LAYOUT FESIBILITY.
NEED TO BE TAKEN CARE DURING VALIDATION.

CAD NOTE:
TRANSCEIVER PAIRS MAY BE SWAPPED
TO OPTIMIZE LAYOUT (EXCEPT UX CH0).

70 22 IN	CLK_FGT_12C_156.25M_DN	BG55	REFCLK_FGTL12C_Q1_RX_CH2_DN	
70 22 IN	CLK_FGT_12C_156.25M_DP	BF54	REFCLK_FGTL12C_Q1_RX_CH2_DP	
70 22 IN	CLK_FGT_12C_156.25M_SPARE_DN	BD56	REFCLK_FGTL12C_Q1_RX_CH3_DN	
70 22 IN	CLK_FGT_12C_156.25M_SPARE_DP	BE55	REFCLK_FGTL12C_Q1_RX_CH3_DP	

43 IN	QSFPDD1_RX_7_DN	T64	FGTL12C_RX_Q2_CH0_DN	FGTL12C_TX_Q2_CH0_DN	W61 QSFPDD1_TX_7_DN OUT 43
43 IN	QSFPDD1_RX_7_DP	U65	FGTL12C_RX_Q2_CH0_DP	FGTL12C_TX_Q2_CH0_DP	V62 QSFPDD1_TX_7_DP OUT 43
43 IN	QSFPDD1_RX_6_DN	R67	FGTL12C_RX_Q2_CH1_DN	FGTL12C_TX_Q2_CH1_DN	T58 QSFPDD1_TX_6_DN OUT 43
43 IN	QSFPDD1_RX_6_DP	P68	FGTL12C_RX_Q2_CH1_DP	FGTL12C_TX_Q2_CH1_DP	U59 QSFPDD1_TX_6_DP OUT 43
43 IN	QSFPDD1_RX_5_DN	M64	FGTL12C_RX_Q2_CH2_DN	FGTL12C_TX_Q2_CH2_DN	R61 QSFPDD1_TX_5_DN OUT 43
43 IN	QSFPDD1_RX_5_DP	N65	FGTL12C_RX_Q2_CH2_DP	FGTL12C_TX_Q2_CH2_DP	P62 QSFPDD1_TX_5_DP OUT 43
43 IN	QSFPDD1_RX_4_DN	L67	FGTL12C_RX_Q2_CH3_DN	FGTL12C_TX_Q2_CH3_DN	M58 QSFPDD1_TX_4_DN OUT 43
43 IN	QSFPDD1_RX_4_DP	K68	FGTL12C_RX_Q2_CH3_DP	FGTL12C_TX_Q2_CH3_DP	N59 QSFPDD1_TX_4_DP OUT 43

0 R2285 1 2 RES	REFCLK_FGT_12C_CH4_DN	AY56	REFCLK_FGTL12C_Q2_RX_CH4_DN	
0 R2286 1 2 RES	REFCLK_FGT_12C_CH4_DP	BA55	REFCLK_FGTL12C_Q2_RX_CH4_DP	
0 R2287 1 2 RES	REFCLK_FGT_12C_CH5_DN	AY54	REFCLK_FGTL12C_Q2_RX_CH5_DN	
0 R2288 1 2 RES	REFCLK_FGT_12C_CH5_DP	BB54	REFCLK_FGTL12C_Q2_RX_CH5_DP	
		AV54	REFCLK_FGTL12C_Q2_CH8_DN	
		AW55	REFCLK_FGTL12C_Q2_CH8_DP	

43 IN	QSFPDD1_RX_3_DN	H64	FGTL12C_RX_Q3_CH0_DN	FGTL12C_TX_Q3_CH0_DN	L61 QSFPDD1_TX_3_DN OUT 43
43 IN	QSFPDD1_RX_3_DP	J65	FGTL12C_RX_Q3_CH0_DP	FGTL12C_TX_Q3_CH0_DP	K62 QSFPDD1_TX_3_DP OUT 43
43 IN	QSFPDD1_RX_2_DN	G67	FGTL12C_RX_Q3_CH1_DN	FGTL12C_TX_Q3_CH1_DN	H58 QSFPDD1_TX_2_DN OUT 43
43 IN	QSFPDD1_RX_2_DP	F68	FGTL12C_RX_Q3_CH1_DP	FGTL12C_TX_Q3_CH1_DP	J59 QSFPDD1_TX_2_DP OUT 43
43 IN	QSFPDD1_RX_1_DN	D64	FGTL12C_RX_Q3_CH2_DN	FGTL12C_TX_Q3_CH2_DN	G61 QSFPDD1_TX_1_DN OUT 43
43 IN	QSFPDD1_RX_1_DP	E65	FGTL12C_RX_Q3_CH2_DP	FGTL12C_TX_Q3_CH2_DP	F62 QSFPDD1_TX_1_DP OUT 43
43 IN	QSFPDD1_RX_0_DN	C61	FGTL12C_RX_Q3_CH3_DN	FGTL12C_TX_Q3_CH3_DN	D58 QSFPDD1_TX_0_DN OUT 43
43 IN	QSFPDD1_RX_0_DP	B62	FGTL12C_RX_Q3_CH3_DP	FGTL12C_TX_Q3_CH3_DP	E59 QSFPDD1_TX_0_DP OUT 43

CAD NOTE:
Place RCOMP res right below FPGA balls on the breakout vias.

0 R2289 1 2 RES	REFCLK_FGT_12C_CH6_DN	AT56	REFCLK_FGTL12C_Q3_RX_CH6_DN	
0 R2290 1 2 RES	REFCLK_FGT_12C_CH6_DP	AP56	REFCLK_FGTL12C_Q3_RX_CH6_DP	
0 R2291 1 2 RES	REFCLK_FGT_12C_CH7_DN	AP54	REFCLK_FGTL12C_Q3_RX_CH7_DN	
0 R2292 1 2 RES	REFCLK_FGT_12C_CH7_DP	AR55	REFCLK_FGTL12C_Q3_RX_CH7_DP	
		AN55	REFCLK_FGTL12C_Q3_CH9_DN	
		AM56	REFCLK_FGTL12C_Q3_CH9_DP	

			I_PIN_PERST_N_12C_GXF		
			U12_GDR_IO_PLL_REFCLK_DNU	RCOMP_DN_Q2_CH1_FGT_12C_GXF	AV56 GXF_12C_FGT_RCOMP_0_DN
				RCOMP_DP_Q2_CH1_FGT_12C_GXF	AU55 GXF_12C_FGT_RCOMP_0_DP
			DNU_U12_GDR_I_JTAG_TDI_DFX		R2201 RES 1.5K 1 2 0.1% 0.063W 0402
			DNU_U12_GDR_O_JTAG_TDO_DFX	RCOMP_DN_FHT_12C_GXF	AC51 GXF_12C_FHT_RCOMP_0_DN
				RCOMP_DP_FHT_12C_GXF	AB52 GXF_12C_FHT_RCOMP_0_DP
			DNU_U12_GDR_APROBE_0_ATB		
			DNU_U12_GDR_APROBE_1_ATB	ENB_GXF_FHT12C	AF52 U12_GXF_IO_DFX_0
			APROBE1_GXF_FHT12C		
			APROBE2_GXF_FHT12C		
			APROBE_GXF_FGT12C_Q0_CH3		
			APROBE_GXF_FGT12C_Q2_CH3		
			APROBE_GXF_FGT12C_Q3_CH3		
			APROBE2_GXF_FGT12C_Q3_CH3		
			TEMPDIODE3_DN_U12_GDR_0_SENS_THERM		
			TEMPDIODE3_DP_U12_GDR_1_SENS_THERM		
			GND_U12_GDR_I_EDM_IN		

R2192 RES 499 0.1% 0.0625W 0402 1 2

+P1V8_G2

R59 A93549-001 0 5% 0.0625W RES 0402

R60 A93548-034 10K 1% 0.0625W EMPTY 0402

DESIGN NOTE:
Indicates BARAK_IS_USED

61 22 IN FM_GXF_12C_PERST_N

+P1V8_G2

R2010 A93548-034 10K 1% 0.0625W RES 0402

C2120 H61346-001 10NF 10% 50V EMPTY 0402

CAD NOTE:
PLACE THESE 100-OHM RES RIGHT BELOW FPGA BALLS
ON THE BREAKOUT VIAS.

R1808	A36092-043	100 1% 0.0625W EMPTY 0402	CLK_FHT_12C_156.25M_DP 22 70 / CLK_FHT_12C_156.25M_DN 22 70
R1809	A36092-043	100 1% 0.0625W EMPTY 0402	CLK_12C_FHT_DP 22 / CLK_12C_FHT_DN 22
R1810	A36092-043	100 1% 0.0625W EMPTY 0402	CLK_FGT_12C_156.25M_DP 22 70 / CLK_FGT_12C_156.25M_DN 22 70
R998	A36092-043	100 1% 0.0625W EMPTY 0402	CLK_FGT_12C_156.25M_SPARE_DP 22 70 / CLK_FGT_12C_156.25M_SPARE_DN 22 70

CLK_SHP_12C_DN
CLK_SHP_12C_DP

J23 J85530-001 SCON SM
J24 J85530-001 SCON SM

61 22 IN FM_GXF_12C_PERST_N R1781 1 2 RES 5% 0 0.0625W 0402 FM_GXF_12C_PERST_N_R AH54
SM EMPTY 1 TP306 CLK_12C_IO_PLL R57 1 2 RES 5% 0 0.0625W 0402 CLK_12C_IO_PLL_R AD54

	TP_12C_GDR_I_JTAG_TDI_DFX	AF54
	TP_12C_GDR_IO_JTAG_TDO_DFX	AD56
	TP_12C_GDR_APROBE_0_ATB	AG55
	TP_12C_GDR_APROBE_1_ATB	AF56
	TP_12C_GXF_APROBE1_COM_FHT	AF50
	TP_12C_GXF_APROBE2_COM_FHT	AD50
	TP_12C_GXF_APROBE_Q0_CH3_FGT	BD54
	TP_12C_GXF_APROBE_Q2_CH3_FGT	BC55
	TP_12C_GXF_APROBE_Q3_CH3_FGT	AL55
	TP_12C_GXF_APROBE2_Q3_CH3_FGT	AM54

CAD NOTE:
BREAK-OUT EVERY TP* NETS TO AN
EXPOSED PAD ON THE BOTTOM SIDE.

77 OUT	TEMPDIODE_12C_GXF_DN	AJ55	
77 OUT	TEMPDIODE_12C_GXF_DP	AH56	
		AG53	

F-TILE BANK 12C
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DEPARTMENT: PSG	Intel Corporation INTEL CORPORATION,BANGALORE INDIA, 560103	SIZE: C+	CODE: 34649	DOCUMENT NUMBER: 150-0330690-A2 REV: 2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 22 OF 105

INTEL AGILEX® 7 FPGA I-SERIES (6x F-TILE) - F-TILE 12C/U12

FPGA BANK 12B

CAD NOTE:

PLACE THESE 100-OHM RES RIGHT BELOW FPGA BALLS ON THE BREAKOUT VIAS.

R1819 A36092-043 100 1% 0.0625W EMPTY 0402 — CLK_FHT_12B_156.25M_DP / CLK_FHT_12B_156.25M_DN

R1821 A36092-043 100 1% 0.0625W EMPTY 0402 — CLK_12B_FHT_DP / CLK_12B_FHT_DN

R1822 A36092-043 100 1% 0.0625W EMPTY 0402 — CLK_FGT_12B_156.25M_DP / CLK_FGT_12B_156.25M_DN

R1823 A36092-043 100 1% 0.0625W EMPTY 0402 — CLK_FGT_12B_156.25M_SPARE_DP / CLK_FGT_12B_156.25M_SPARE_DN

156.25M 156.25M

C1225 0.1UF 25V — CLK_12B_FHT_DN

C1226 0.1UF 25V — CLK_12B_FHT_DP

CLK_SMP_12B_DN / CLK_SMP_12B_DP

J61 J85530-001 SCON SM

J62 J85530-001 SCON SM

SM EMPTY TP385 — FM_GXF_12B_PERST_N / CLK_12B_IO_PLL

R1783 RES 5% 0 0.0625W 0402 — FM_GXF_12B_PERST_N_R

R2524 RES 5% 0 0.0625W 0402 — CLK_12B_IO_PLL_R

BGA
U1
EMPTY

HC_FM91_3948BGA

QSFPDD800_RX_3_DN	BJ65	FHTL12B_RX_CH0_DN	FHTL12B_TX_CH0_DN / BF68 QSFPDD800_TX_3_DN
QSFPDD800_RX_3_DP	BH64	FHTL12B_RX_CH0_DP	FHTL12B_TX_CH0_DP / BG67 QSFPDD800_TX_3_DP
QSFPDD800_RX_2_DN	BE65	FHTL12B_RX_CH1_DN	FHTL12B_TX_CH1_DN / BB68 QSFPDD800_TX_2_DN
QSFPDD800_RX_2_DP	BD64	FHTL12B_RX_CH1_DP	FHTL12B_TX_CH1_DP / BC67 QSFPDD800_TX_2_DP
QSFPDD800_RX_1_DN	AY64	FHTL12B_RX_CH2_DN	FHTL12B_TX_CH2_DN / AW67 QSFPDD800_TX_1_DN
QSFPDD800_RX_1_DP	BA65	FHTL12B_RX_CH2_DP	FHTL12B_TX_CH2_DP / AV68 QSFPDD800_TX_1_DP
QSFPDD800_RX_0_DN	AT64	FHTL12B_RX_CH3_DN	FHTL12B_TX_CH3_DN / AR67 QSFPDD800_TX_0_DN
QSFPDD800_RX_0_DP	AU65	FHTL12B_RX_CH3_DP	FHTL12B_TX_CH3_DP / AP68 QSFPDD800_TX_0_DP
CLK_FHT_12B_156.25M_DN	BH60	REFCLK_FHTL12B_CH0_DN	
CLK_FHT_12B_156.25M_DP	BG61	REFCLK_FHTL12B_CH0_DP	
CLK_12B_FHT_DN	BD60	REFCLK_FHTL12B_CH1_DN	
CLK_12B_FHT_DP	BC61	REFCLK_FHTL12B_CH1_DP	
R2251 RES FGT_12B_RX_CH0_DN	CY64	FGTL12B_RX_Q0_CH0_DN	FGTL12B_TX_Q0_CH0_DN / CY58
R2252 RES FGT_12B_RX_CH0_DP	DA65	FGTL12B_RX_Q0_CH0_DP	FGTL12B_TX_Q0_CH0_DP / DA59
R2253 RES FGT_12B_RX_CH1_DN	CW67	FGTL12B_RX_Q0_CH1_DN	FGTL12B_TX_Q0_CH1_DN / CW61
R2254 RES FGT_12B_RX_CH1_DP	CV68	FGTL12B_RX_Q0_CH1_DP	FGTL12B_TX_Q0_CH1_DP / CV62
R2255 RES FGT_12B_RX_CH2_DN	CT64	FGTL12B_RX_Q0_CH2_DN	FGTL12B_TX_Q0_CH2_DN / CT58
R2256 RES FGT_12B_RX_CH2_DP	CU65	FGTL12B_RX_Q0_CH2_DP	FGTL12B_TX_Q0_CH2_DP / CU59
R2257 RES FGT_12B_RX_CH3_DN	CR67	FGTL12B_RX_Q0_CH3_DN	FGTL12B_TX_Q0_CH3_DN / CR61
R2258 RES FGT_12B_RX_CH3_DP	CP68	FGTL12B_RX_Q0_CH3_DP	FGTL12B_TX_Q0_CH3_DP / CP62
R2247 RES REFCLK_FGT_12B_CH0_DN	CJ55	REFCLK_FGTL12B_Q0_RX_CH0_DN	
R2248 RES REFCLK_FGT_12B_CH0_DP	CK54	REFCLK_FGTL12B_Q0_RX_CH0_DP	
R2249 RES REFCLK_FGT_12B_CH1_DN	CH56	REFCLK_FGTL12B_Q0_RX_CH1_DN	
R2250 RES REFCLK_FGT_12B_CH1_DP	CK56	REFCLK_FGTL12B_Q0_RX_CH1_DP	
QSFP0_RX_3_DN	CM64	FGTL12B_RX_Q1_CH0_DN	FGTL12B_TX_Q1_CH0_DN / CM58 QSFP0_TX_3_DN
QSFP0_RX_3_DP	CN65	FGTL12B_RX_Q1_CH0_DP	FGTL12B_TX_Q1_CH0_DP / CN59 QSFP0_TX_3_DP
QSFP0_RX_2_DN	CL67	FGTL12B_RX_Q1_CH1_DN	FGTL12B_TX_Q1_CH1_DN / CL61 QSFP0_TX_2_DN
QSFP0_RX_2_DP	CK68	FGTL12B_RX_Q1_CH1_DP	FGTL12B_TX_Q1_CH1_DP / CK62 QSFP0_TX_2_DP
QSFP0_RX_1_DN	CH64	FGTL12B_RX_Q1_CH2_DN	FGTL12B_TX_Q1_CH2_DN / CH58 QSFP0_TX_1_DN
QSFP0_RX_1_DP	CJ65	FGTL12B_RX_Q1_CH2_DP	FGTL12B_TX_Q1_CH2_DP / CJ59 QSFP0_TX_1_DP
QSFP0_RX_0_DN	CG67	FGTL12B_RX_Q1_CH3_DN	FGTL12B_TX_Q1_CH3_DN / CG61 QSFP0_TX_0_DN
QSFP0_RX_0_DP	CF68	FGTL12B_RX_Q1_CH3_DP	FGTL12B_TX_Q1_CH3_DP / CF62 QSFP0_TX_0_DP
CLK_FGT_12B_156.25M_DN	CF54	REFCLK_FGTL12B_Q1_RX_CH2_DN	
CLK_FGT_12B_156.25M_DP	CD54	REFCLK_FGTL12B_Q1_RX_CH2_DP	
CLK_FGT_12B_156.25M_SPARE_DN	CE55	REFCLK_FGTL12B_Q1_RX_CH3_DN	
CLK_FGT_12B_156.25M_SPARE_DP	CD56	REFCLK_FGTL12B_Q1_RX_CH3_DP	
QSFPDD0_RX_7_DN	CD64	FGTL12B_RX_Q2_CH0_DN	FGTL12B_TX_Q2_CH0_DN / CD58 QSFPDD0_TX_7_DN
QSFPDD0_RX_7_DP	CE65	FGTL12B_RX_Q2_CH0_DP	FGTL12B_TX_Q2_CH0_DP / CE59 QSFPDD0_TX_7_DP
QSFPDD0_RX_6_DN	CC67	FGTL12B_RX_Q2_CH1_DN	FGTL12B_TX_Q2_CH1_DN / CC61 QSFPDD0_TX_6_DN
QSFPDD0_RX_6_DP	CB68	FGTL12B_RX_Q2_CH1_DP	FGTL12B_TX_Q2_CH1_DP / CB62 QSFPDD0_TX_6_DP
QSFPDD0_RX_5_DN	BY64	FGTL12B_RX_Q2_CH2_DN	FGTL12B_TX_Q2_CH2_DN / BY58 QSFPDD0_TX_5_DN
QSFPDD0_RX_5_DP	CA65	FGTL12B_RX_Q2_CH2_DP	FGTL12B_TX_Q2_CH2_DP / CA59 QSFPDD0_TX_5_DP
QSFPDD0_RX_4_DN	BW67	FGTL12B_RX_Q2_CH3_DN	FGTL12B_TX_Q2_CH3_DN / BW61 QSFPDD0_TX_4_DN
QSFPDD0_RX_4_DP	BV68	FGTL12B_RX_Q2_CH3_DP	FGTL12B_TX_Q2_CH3_DP / BV62 QSFPDD0_TX_4_DP
R2259 RES REFCLK_FGT_12B_CH4_DN	CC55	REFCLK_FGTL12B_Q2_RX_CH4_DN	
R2260 RES REFCLK_FGT_12B_CH4_DP	CB54	REFCLK_FGTL12B_Q2_RX_CH4_DP	
R2261 RES REFCLK_FGT_12B_CH5_DN	BV56	REFCLK_FGTL12B_Q2_RX_CH5_DN	
R2262 RES REFCLK_FGT_12B_CH5_DP	BY56	REFCLK_FGTL12B_Q2_RX_CH5_DP	
	BV54	REFCLK_FGTL12B_Q2_CH0_DN	
	BW55	REFCLK_FGTL12B_Q2_CH0_DP	
QSFPDD0_RX_3_DN	BT64	FGTL12B_RX_Q3_CH0_DN	FGTL12B_TX_Q3_CH0_DN / BT58 QSFPDD0_TX_3_DN
QSFPDD0_RX_3_DP	BU65	FGTL12B_RX_Q3_CH0_DP	FGTL12B_TX_Q3_CH0_DP / BU59 QSFPDD0_TX_3_DP
QSFPDD0_RX_2_DN	BR67	FGTL12B_RX_Q3_CH1_DN	FGTL12B_TX_Q3_CH1_DN / BR61 QSFPDD0_TX_2_DN
QSFPDD0_RX_2_DP	BP68	FGTL12B_RX_Q3_CH1_DP	FGTL12B_TX_Q3_CH1_DP / BP62 QSFPDD0_TX_2_DP
QSFPDD0_RX_1_DN	BM64	FGTL12B_RX_Q3_CH2_DN	FGTL12B_TX_Q3_CH2_DN / BM58 QSFPDD0_TX_1_DN
QSFPDD0_RX_1_DP	BN65	FGTL12B_RX_Q3_CH2_DP	FGTL12B_TX_Q3_CH2_DP / BN59 QSFPDD0_TX_1_DP
QSFPDD0_RX_0_DN	BL67	FGTL12B_RX_Q3_CH3_DN	FGTL12B_TX_Q3_CH3_DN / BL61 QSFPDD0_TX_0_DN
QSFPDD0_RX_0_DP	BK68	FGTL12B_RX_Q3_CH3_DP	FGTL12B_TX_Q3_CH3_DP / BK62 QSFPDD0_TX_0_DP
R2263 RES REFCLK_FGT_12B_CH6_DN	BU55	REFCLK_FGTL12B_Q3_RX_CH6_DN	
R2264 RES REFCLK_FGT_12B_CH6_DP	BT56	REFCLK_FGTL12B_Q3_RX_CH6_DP	
R2265 RES REFCLK_FGT_12B_CH7_DN	BP54	REFCLK_FGTL12B_Q3_RX_CH7_DN	
R2266 RES REFCLK_FGT_12B_CH7_DP	BM54	REFCLK_FGTL12B_Q3_RX_CH7_DP	
	BM56	REFCLK_FGTL12B_Q3_CH9_DN	
	BN55	REFCLK_FGTL12B_Q3_CH9_DP	
	DP54	I_PIN_PERST_N_12B_GXF	
	DK48	U11_GDR_IO_PLL_REFCLK_DNU	RCOMP_DN_Q2_CH1_FGT_12B_GXF / RCOMP_DP_Q2_CH1_FGT_12B_GXF
TP_12B_GDR_I_JTAG_TDI_DFX	DN55	DNU_U11_GDR_I_JTAG_TDI_DFX	
TP_12B_GDR_IO_JTAG_TDO_DFX	DR53	DNU_U11_GDR_O_JTAG_TDO_DFX	
TP_12B_GDR_APROBE_0_ATB	DK52	DNU_U11_GDR_APROBE_0_ATB	RCOMP_DN_FHT_12B_GXF / RCOMP_DP_FHT_12B_GXF
TP_12B_GDR_APROBE_1_ATB	DL51	DNU_U11_GDR_APROBE_1_ATB	
TP_12B_GXF_APROBE1	BA59	APROBE1_GXF_FHT12B	ENB_GXF_FHT12B
TP_12B_GXF_APROBE2	AY60	APROBE2_GXF_FHT12B	
TP_12B_GXF_APROBE_Q0_CH3_FGT	CG55	APROBE_GXF_FGT12B_Q0_CH3	
TP_12B_GXF_APROBE_Q2_CH3_FGT	CF56	APROBE_GXF_FGT12B_Q2_CH3	
TP_12B_GXF_APROBE_Q3_CH3_FGT	BP56	APROBE_GXF_FGT12B_Q3_CH3	
TP_12B_GXF_APROBE2_Q3_CH3_FGT	BR55	APROBE2_GXF_FGT12B_Q3_CH3	
TEMPDIODE_12B_GXF_DN	BF58	TEMPDIODE2_DN_U11_GDR_O_SENS_THERM	
TEMPDIODE_12B_GXF_DP	BH58	TEMPDIODE2_DP_U11_GDR_I_SENS_THERM	
	DM52	GND_U11_GDR_I_EDM_IN	

F-TILE BANK 12B

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CAD NOTE:

PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS.

CAD NOTE:

Place RCOMP res right below FPGA balls on the breakout vias.

R2190 RES 499 0.1% 0.0625W 0402 — CA55 GXF_12B_FGT_RCOMP_0_DN / BY54 GXF_12B_FGT_RCOMP_0_DP

R2199 RES 1.5K 0.1% 0.063W 0402 — AV60 GXF_12B_FHT_RCOMP_0_DN / AW61 GXF_12B_FHT_RCOMP_0_DP

DN53 U11_GXF_IO_DFX_0

+P1V8_G2

R2196 A93549-001 0 5% 0.0625W RES 0402

R2186 A93548-034 10K 1% 0.0625W EMPTY 0402

DESIGN NOTE:

Indicates BARAK_IS_USED

+P1V8_G2

R1003 A93548-034 10K 1% 0.0625W RES 0402

61 23 IN FM_GXF_12B_PERST_N

C696 H61346-001 10NF 10% 50V EMPTY 0402

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DEPARTMENT: PSG	Intel Corporation INTEL CORPORATION,BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SIZE: C+	CODE: 34649	DOCUMENT NUMBER: 150-0330690-A2 / REV: 2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET: 23 OF 105

INTEL AGILEX® 7 FPGA I-SERIES (6x F-TILE) - F-TILE 12B/U11

FPGA BANK 12A

CAD NOTE:

PLACE THESE 100-OHM RES RIGHT BELOW FPGA BALLS
ON THE BREAKOUT VIAS.

R1364 A36092-043 100 1% 0.0625W EMPTY 0402 — FMCA_ETH_REFCLK_156.25M_DP / FMCA_ETH_REFCLK_156.25M_DN (24 66)

R1365 A36092-043 100 1% 0.0625W EMPTY 0402 — FMCA_CPRI_REFCLK_153.6M_DP / FMCA_CPRI_REFCLK_153.6M_DN (24 66)

R1460 A36092-043 100 1% 0.0625W EMPTY 0402 — FMCA_CPRI_REFCLK_184.32M_DP / FMCA_CPRI_REFCLK_184.32M_DN (24 66)

R2586 A36092-043 100 1% 0.0625W EMPTY 0402 — FMC_A_CLK_M2C_0_DP / FMC_A_CLK_M2C_0_DN (58 24 53)

R2587 A36092-043 100 1% 0.0625W EMPTY 0402 — FMC_A_CLK_M2C_1_DP / FMC_A_CLK_M2C_1_DN (58 24 53)

R2588 A36092-043 100 1% 0.0625W EMPTY 0402 — FMC_A_CLK_M2C_2_DP / FMC_A_CLK_M2C_2_DN (24 53)

R2589 A36092-043 100 1% 0.0625W EMPTY 0402 — FMC_A_CLK_M2C_3_DP / FMC_A_CLK_M2C_3_DN (58 24 53)

R1405 A36092-043 100 1% 0.0625W EMPTY 0402 — REFCLK_FGT_12A_8_DP / REFCLK_FGT_12A_8_DN (24 71)

R1409 A36092-043 100 1% 0.0625W EMPTY 0402 — REFCLK_FGT_12A_9_DP / REFCLK_FGT_12A_9_DN (24 71)

BGA
U1
EMPTY

HC_FM91_3948BGA

0 R2293	FHT_12A_RX_CH0_DN	DU65	FHTL12A_RX_CH0_DN	FHTL12A_TX_CH0_DN	DR67		
0 R2294	FHT_12A_RX_CH0_DP	DT64	FHTL12A_RX_CH0_DP	FHTL12A_TX_CH0_DP	DP68		
0 R2295	FHT_12A_RX_CH1_DN	DN65	FHTL12A_RX_CH1_DN	FHTL12A_TX_CH1_DN	DL67		
0 R2296	FHT_12A_RX_CH1_DP	DM64	FHTL12A_RX_CH1_DP	FHTL12A_TX_CH1_DP	DK68		
0 R2297	FHT_12A_RX_CH2_DN	DH64	FHTL12A_RX_CH2_DN	FHTL12A_TX_CH2_DN	DF68		
0 R2298	FHT_12A_RX_CH2_DP	DJ65	FHTL12A_RX_CH2_DP	FHTL12A_TX_CH2_DP	DG67		
0 R2299	FHT_12A_RX_CH3_DN	DD64	FHTL12A_RX_CH3_DN	FHTL12A_TX_CH3_DN	DB68		
0 R2300	FHT_12A_RX_CH3_DP	DE65	FHTL12A_RX_CH3_DP	FHTL12A_TX_CH3_DP	DC67		
0 R2301	REFCLK_FHT_12A_CH0_DN	DP62	REFCLK_FHTL12A_CH0_DN				
0 R2302	REFCLK_FHT_12A_CH0_DP	DR61	REFCLK_FHTL12A_CH0_DP				
0 R2303	REFCLK_FHT_12A_CH1_DN	DK62	REFCLK_FHTL12A_CH1_DN				
0 R2304	REFCLK_FHT_12A_CH1_DP	DJ61	REFCLK_FHTL12A_CH1_DP				
IN	FMC_A_RX_15_DN	EH52	FGTL12A_RX_Q0_CH0_DN				
IN	FMC_A_RX_15_DP	EJ53	FGTL12A_RX_Q0_CH0_DP	FGTL12A_TX_Q0_CH0_DN	DY52	FMC_A_TX_15_DN	OUT 53
IN	FMC_A_RX_14_DN	EM52	FGTL12A_RX_Q0_CH1_DN	FGTL12A_TX_Q0_CH0_DP	EA53	FMC_A_TX_15_DP	OUT 53
IN	FMC_A_RX_14_DP	EN53	FGTL12A_RX_Q0_CH1_DP	FGTL12A_TX_Q0_CH1_DN	ED52	FMC_A_TX_14_DN	OUT 53
IN	FMC_A_RX_13_DN	ER55	FGTL12A_RX_Q0_CH2_DN	FGTL12A_TX_Q0_CH1_DP	EE53	FMC_A_TX_14_DP	OUT 53
IN	FMC_A_RX_13_DP	EP56	FGTL12A_RX_Q0_CH2_DP	FGTL12A_TX_Q0_CH2_DN	EG55	FMC_A_TX_13_DN	OUT 53
IN	FMC_A_RX_12_DN	EW55	FGTL12A_RX_Q0_CH3_DN	FGTL12A_TX_Q0_CH2_DP	EF56	FMC_A_TX_13_DP	OUT 53
IN	FMC_A_RX_12_DP	EV56	FGTL12A_RX_Q0_CH3_DP	FGTL12A_TX_Q0_CH3_DN	EL55	FMC_A_TX_12_DN	OUT 53
				FGTL12A_TX_Q0_CH3_DP	EK56	FMC_A_TX_12_DP	OUT 53
58 53 24 IN	FMC_A_CLK_M2C_0_DN	DH56	REFCLK_FGTL12A_Q0_RX_CH0_DN				
58 53 24 IN	FMC_A_CLK_M2C_0_DP	DJ55	REFCLK_FGTL12A_Q0_RX_CH0_DP				
58 53 24 IN	FMC_A_CLK_M2C_1_DN	DH54	REFCLK_FGTL12A_Q0_RX_CH1_DN				
58 53 24 IN	FMC_A_CLK_M2C_1_DP	DK54	REFCLK_FGTL12A_Q0_RX_CH1_DP				
IN	FMC_A_RX_11_DN	ET58	FGTL12A_RX_Q1_CH0_DN				
IN	FMC_A_RX_11_DP	EU59	FGTL12A_RX_Q1_CH0_DP	FGTL12A_TX_Q1_CH0_DN	EC55	FMC_A_TX_11_DN	OUT 53
IN	FMC_A_RX_10_DN	EW61	FGTL12A_RX_Q1_CH1_DN	FGTL12A_TX_Q1_CH0_DP	EB56	FMC_A_TX_11_DP	OUT 53
IN	FMC_A_RX_10_DP	EV62	FGTL12A_RX_Q1_CH1_DP	FGTL12A_TX_Q1_CH1_DN	DW55	FMC_A_TX_10_DN	OUT 53
IN	FMC_A_RX_9_DN	ET64	FGTL12A_RX_Q1_CH2_DN	FGTL12A_TX_Q1_CH1_DP	DV56	FMC_A_TX_10_DP	OUT 53
IN	FMC_A_RX_9_DP	EU65	FGTL12A_RX_Q1_CH2_DP	FGTL12A_TX_Q1_CH2_DN	EM58	FMC_A_TX_9_DN	OUT 53
IN	FMC_A_RX_8_DN	ER67	FGTL12A_RX_Q1_CH3_DN	FGTL12A_TX_Q1_CH2_DP	EN59	FMC_A_TX_9_DP	OUT 53
IN	FMC_A_RX_8_DP	EP68	FGTL12A_RX_Q1_CH3_DP	FGTL12A_TX_Q1_CH3_DN	ER61	FMC_A_TX_8_DN	OUT 53
				FGTL12A_TX_Q1_CH3_DP	EP62	FMC_A_TX_8_DP	OUT 53
156.25M 66 24 IN	FMCA_ETH_REFCLK_156.25M_DN	DG55	REFCLK_FGTL12A_Q1_RX_CH2_DN				
156.25M 66 24 IN	FMCA_ETH_REFCLK_156.25M_DP	DF54	REFCLK_FGTL12A_Q1_RX_CH2_DP				
153.6M 66 24 IN	FMCA_CPRI_REFCLK_153.6M_DN	DB56	REFCLK_FGTL12A_Q1_RX_CH3_DN				
153.6M 66 24 IN	FMCA_CPRI_REFCLK_153.6M_DP	DD56	REFCLK_FGTL12A_Q1_RX_CH3_DP				
IN	FMC_A_RX_7_DN	EM64	FGTL12A_RX_Q2_CH0_DN				
IN	FMC_A_RX_7_DP	EN65	FGTL12A_RX_Q2_CH0_DP	FGTL12A_TX_Q2_CH0_DN	EH58	FMC_A_TX_7_DN	OUT 53
IN	FMC_A_RX_6_DN	EL67	FGTL12A_RX_Q2_CH1_DN	FGTL12A_TX_Q2_CH0_DP	EJ59	FMC_A_TX_7_DP	OUT 53
IN	FMC_A_RX_6_DP	EK68	FGTL12A_RX_Q2_CH1_DP	FGTL12A_TX_Q2_CH1_DN	EL61	FMC_A_TX_6_DN	OUT 53
IN	FMC_A_RX_5_DN	EH64	FGTL12A_RX_Q2_CH2_DN	FGTL12A_TX_Q2_CH1_DP	EK62	FMC_A_TX_6_DP	OUT 53
IN	FMC_A_RX_5_DP	EJ65	FGTL12A_RX_Q2_CH2_DP	FGTL12A_TX_Q2_CH2_DN	ED58	FMC_A_TX_5_DN	OUT 53
IN	FMC_A_RX_4_DN	EG67	FGTL12A_RX_Q2_CH3_DN	FGTL12A_TX_Q2_CH2_DP	EE59	FMC_A_TX_5_DP	OUT 53
IN	FMC_A_RX_4_DP	EF68	FGTL12A_RX_Q2_CH3_DP	FGTL12A_TX_Q2_CH3_DN	EG61	FMC_A_TX_4_DN	OUT 53
				FGTL12A_TX_Q2_CH3_DP	EF62	FMC_A_TX_4_DP	OUT 53
184.32M 66 24 IN	FMCA_CPRI_REFCLK_184.32M_DN	DC55	REFCLK_FGTL12A_Q2_RX_CH4_DN				
184.32M 66 24 IN	FMCA_CPRI_REFCLK_184.32M_DP	DB54	REFCLK_FGTL12A_Q2_RX_CH4_DP				
R2309 0	REFCLK_FGT_12A_CH5_DN	CY56	REFCLK_FGTL12A_Q2_RX_CH5_DN				
0 R2310	REFCLK_FGT_12A_CH5_DP	DA55	REFCLK_FGTL12A_Q2_RX_CH5_DP				
71 24 OUT	REFCLK_FGT_12A_8_DN	CU55	REFCLK_FGTL12A_Q2_CH8_DN				
71 24 OUT	REFCLK_FGT_12A_8_DP	CT56	REFCLK_FGTL12A_Q2_CH8_DP				
IN	FMC_A_RX_3_DN	ED64	FGTL12A_RX_Q3_CH0_DN				
IN	FMC_A_RX_3_DP	EE65	FGTL12A_RX_Q3_CH0_DP				
IN	FMC_A_RX_2_DN	EC67	FGTL12A_RX_Q3_CH1_DN	FGTL12A_TX_Q3_CH0_DN	DY58	FMC_A_TX_3_DN	OUT 53
IN	FMC_A_RX_2_DP	EB68	FGTL12A_RX_Q3_CH1_DP	FGTL12A_TX_Q3_CH0_DP	EA59	FMC_A_TX_3_DP	OUT 53
IN	FMC_A_RX_1_DN	DY64	FGTL12A_RX_Q3_CH2_DN	FGTL12A_TX_Q3_CH1_DN	EC61	FMC_A_TX_2_DN	OUT 53
IN	FMC_A_RX_1_DP	EA65	FGTL12A_RX_Q3_CH2_DP	FGTL12A_TX_Q3_CH1_DP	EB62	FMC_A_TX_2_DP	OUT 53
IN	FMC_A_RX_0_DN	DW67	FGTL12A_RX_Q3_CH3_DN	FGTL12A_TX_Q3_CH2_DN	DT58	FMC_A_TX_1_DN	OUT 53
IN	FMC_A_RX_0_DP	DV68	FGTL12A_RX_Q3_CH3_DP	FGTL12A_TX_Q3_CH2_DP	DU59	FMC_A_TX_1_DP	OUT 53
				FGTL12A_TX_Q3_CH3_DN	DW61	FMC_A_TX_0_DN	OUT 53
				FGTL12A_TX_Q3_CH3_DP	DV62	FMC_A_TX_0_DP	OUT 53
53 24 IN	FMC_A_CLK_M2C_2_DN	CV54	REFCLK_FGTL12A_Q3_RX_CH6_DN				
53 24 IN	FMC_A_CLK_M2C_2_DP	CT54	REFCLK_FGTL12A_Q3_RX_CH6_DP				
58 53 24 IN	FMC_A_CLK_M2C_3_DN	CP54	REFCLK_FGTL12A_Q3_RX_CH7_DN				
58 53 24 IN	FMC_A_CLK_M2C_3_DP	CR55	REFCLK_FGTL12A_Q3_RX_CH7_DP				
71 24 OUT	REFCLK_FGT_12A_9_DN	CL55	REFCLK_FGTL12A_Q3_CH9_DN				
71 24 OUT	REFCLK_FGT_12A_9_DP	CM56	REFCLK_FGTL12A_Q3_CH9_DP				
61 24 IN FM_GXF_12A_SPARE_N	R1680 1 2 RES 0.5% 0.0625W 0402	FM_GXF_12A_SPARE_N_R	DL59				
SM EMPTY 1 TP307 CLK_12A_IO_PLL	R1681 1 2 RES 0.5% 0.0625W 0402	CLK_12A_IO_PLL_R	DU53				
	TP_12A_GXF_I_JTAG_TDI_DFX		DL57				
	TP_12A_GXF_IO_JTAG_TDO_DFX		DT54				
	TP_12A_GXF_APROBE_0_ATB		DN59				
	TP_12A_GXF_APROBE_1_ATB		DM60				
	TP_12A_GXF_APROBE1_COM_FHT		DD60				
	TP_12A_GXF_APROBE2_COM_FHT		DE61				
	TP_12A_GXF_APROBE_Q0_CH3_FGT		DE55				
	TP_12A_GXF_APROBE_Q2_CH3_FGT		DD54				
	TP_12A_GXF_APROBE_Q3_CH3_FGT		CN55				
	TP_12A_GXF_APROBE2_Q3_CH3_FGT		CM54				
77 OUT	TEMPDIODE_12A_GXF_DN		DM56				
77 OUT	TEMPDIODE_12A_GXF_DP		DN57				
			DM58				

I_PIN_PERST_N_12A_GXF	
U10_GDR_IO_PLL_REFCLK_DNU	
DNU_U10_GDR_I_JTAG_TDI_DFX	
DNU_U10_GDR_O_JTAG_TDO_DFX	
DNU_U10_GDR_APROBE_0_ATB	
DNU_U10_GDR_APROBE_1_ATB	
APROBE1_GXF_FHT12A	
APROBE2_GXF_FHT12A	
APROBE_GXF_FGT12A_Q0_CH3	
APROBE_GXF_FGT12A_Q2_CH3	
APROBE_GXF_FGT12A_Q3_CH3	
APROBE2_GXF_FGT12A_Q3_CH3	
TEMPDIODE1_DN_U10_GDR_O_SENS_THERM	
TEMPDIODE1_DP_U10_GDR_I_SENS_THERM	
GND_U10_GDR_I_EDM_IN	

RCOMP_DN_Q2_CH1_FGT_12A_GXF
RCOMP_DP_Q2_CH1_FGT_12A_GXF
RCOMP_DN_FHT_12A_GXF
RCOMP_DP_FHT_12A_GXF
ENB_GXF_FHT12A

CV56 GXF_12A_FGT_RCOMP_0_DN
CW55 GXF_12A_FGT_RCOMP_0_DP
DB62 GXF_12A_FHT_RCOMP_0_DN
DC61 GXF_12A_FHT_RCOMP_0_DP
DR55 ENB_GXF_FHT_12A — 0 R2315 — RES

R2193 RES 499 0.1% 0.0625W 0402
R2202 RES 1.5K 0.1% 0.063W 0402

CAD NOTE:
Place RCOMP res right below FPGA balls on the breakout vias.

CAD NOTE:
PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS.

F-TILE BANK 12A
8 OF 31
99C1H7

+P1V8_G2
R1787 A93548-034 10K 1% 0.0625W RES 0402
61 24 IN FM_GXF_12A_SPARE_N
C3051 H61346-001 10NF 10% 50V EMPTY 0402

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DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	24 OF 105

INTEL AGILEX® 7 FPGA I-SERIES (6x F-TILE) - F-TILE 12A/U10

FPGA GND- I

BGA
U1
EMPTY
HC_FM91_3948BGA

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16 OF 31
17 OF 31
18 OF 31
19 OF 31
20 OF 31
21 OF 31
22 OF 31
99C1H7

MTH1 MTH2 MTH3 MTH4 MTH5 MTH6 MTH7 MTH16 MTH17
MTH8 MTH9 MTH10 MTH11 MTH12 MTH13 MTH14 MTH15 MTH18
EMPTY
HC_MTG_HOLE
GND

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INTEL AGILEX® 7 FPGA I-SERIES (6x F-TILE) - GND 1

DEPARTMENT: PSG

Intel Corporation
INTEL CORPORATION,BANGALORE
INDIA, 560103

SIZE	CODE	DOCUMENT NUMBER	REV
C+	34649	150-0330690-A2	2.0

SCALE: | DO NOT SCALE DRAWING | SHEET 25 OF 105

FPGA GND- II

BGA
U1
EMPTY
HC_FM91_3948BGA

23 OF 31
99C1H7

BGA
U1
EMPTY
HC_FM91_3948BGA

14 OF 31
99C1H7

BGA
U1
EMPTY
HC_FM91_3948BGA

30 OF 31
99C1H7

MTH19
EMPTY
HC_MTG_HOLE

MTH21
EMPTY
HC_MTG_HOLE

MTH20
EMPTY
HC_MTG_HOLE

MTH22
EMPTY
HC_MTG_HOLE

HC_TP
A69956-001
TP392
EMPTY
TH

HC_TP
A69956-001
TP393
EMPTY
TH

HC_TP
A69956-001
TP394
EMPTY
TH

HC_TP
A69956-001
TP395
EMPTY
TH

HC_TP
A69956-001
TP396
EMPTY
TH

HC_TP
A69956-001
TP397
EMPTY
TH

HC_TP
A69956-001
TP398
EMPTY
TH

HC_TP
A69956-001
TP399
EMPTY
TH

HC_TP
A69956-001
TP400
EMPTY
TH

CAD NOTE:
Place these TP 's near to VR's Enable/PG/Vout TP's.

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DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SCALE:	DO NOT SCALE DRAWING	SHEET	26 OF 105

INTEL AGILEX® 7 FPGA I-SERIES (6x F-TILE) - GND 2

POWER-1

BGA U1 EMPTY HC_FM91_3948BGA

25 OF 31

99C1H7

+VCCL_0V8_G1 — 0.8V (Group 1)

C3 A36096-213 0.1UF 10% 25V X7R 0402

VCCL_SENSE_R_P — R66 RES 0 5% 0.0625W 0402 — VCCL_SENSE_P

VCCL_SENSE_R_N — R107 RES 0 5% 0.0625W 0402 — VCCL_SENSE_N

Place C434 right below FPGA balls

R10 A93548-031 10 1% 0.0625W RES 0402

R265 A93548-031 10 1% 0.0625W RES 0402

VCCL_SENSE_P / VCCL_SENSE_N → OUT 84 / OUT 84

+P1V8_G2 — 1.8V (Group 2)

BGA U1 EMPTY HC_FM91_3948BGA

24 OF 31

99C1H7

+VCCL_0V8_G1 — 0.8V (Group 1)

BGA U1 EMPTY HC_FM91_3948BGA

VCCP

[VCCA_PLL] — DP40 DP36 DP28 DP32 — DE43 DE41 DC43 DC41

[VCCA_PLL] — AF38 AF42 AF34 AF32

[VCCH] — DB46 CV46 CT46 CM46

[VCCH] — CD46 BY46 BT46 BM46

[VCCH] — BF46 BB46 AV46 AP46

[VCCH] — DF24 CV24 CP24

[VCCH] — CF24 CB24 BV24 BP24

[VCCH] — BH24 BD24 AY24 AT24

[VCCPT] — DJ39 DJ37 DJ35 DJ33 DJ31

[VCCPT] — AL39 AL37 AL35 AL33 AL31

[VCCRCORE] — DD38 DD36 DD34 DD32 DD30 AT38 AT36 AT34 AT32 AT40

[VCCIO_SDM] — DG43

[VCCIO_PIO_SDM] — DE45

[VCCADC] — DH44

[VCCBAT] — DG45

VCCFUSEWR_SDM — DC45

29 OF 31

99C1H7

+VCCL_0V8_G1 — 0.8V (Group 1)

+VCCA_PLL — 1.2V (Group 3)

+P0V8_G1 — 0.8V (Group 1)

+VCC_HSSI_GXF_0V8_UX0_G1 — 0.8V (Group 1)

+VCCPLLDIG_SDM — 0.8V (Group 1)

DESIGN NOTE: 0.8V (Group 1) Voltage rail sense: Connect to VCCH

+P0V8_G1 — +VCCPLL_ADC_SDM — 1.8V (Group 2)

+P1V8_G3 — 1.8V (Group 3)

+P1V2_G3 — 1.2V (Group 3)

+VCCPLL_ADC_SDM — 1.8V (Group 2)

+P1V8_VCCBAT — 1.8V (Group 3)

+P1V8_G3 — 1.8V (Group 3)

+DIMM_VREF_0V6_G3 — R1000 RES 0 5% 0.0625W 0402 — +FMC_B_VREF

+DDR4_VREF_0V6_G3 — R1002 RES 0 5% 0.0625W 0402 — +FMC_A_VREF

BGA U1 EMPTY HC_FM91_3948BGA

VCCIO_PIO_2A DN39 DN37 DL39 DL37

VCCIO_PIO_2B DN35 DN33 DL35 DL33

VCCIO_PIO_2C DN31 DN29 DL31 DL29

VCCIO_PIO_3A AJ39 AJ37 AG39 AG37

VCCIO_PIO_3B AJ35 AJ33 AG35 AG33

VCCIO_PIO_3C AJ31 AJ29 AG31 AG29

VREFB2AN0 DM38 VREFB2BN0 DM34 VREFB2CN0 DM30

VREFB3AN0 AH40 VREFB3BN0 AH36 VREFB3CN0 AH30

26 OF 31

99C1H7

+P1V2_G3 — 1.2V (Group 3)

+P1V2_G3 — 1.2V (Group 3)

+FMC_A_VREF — 0.6V (Group 3)

+DDR4_VREF_0V6_G3 — 0.6V (Group 3)

+DIMM_VREF_0V6_G3 — 0.6V (Group 3)

+FMC_B_VREF

+P1V8_G3 — R375 RES 0 5% 0.0625W 0402 — +P1V8_VCCBAT

+VCCBAT — R2640 EMPTY 0 5% 0.0625W 0402

HC_BT1 BT1 K12163-001 HC_BATTERY IC SM

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PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
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INTEL AGILEX® 7 FPGA I-SERIES (6x F-TILE) - POWER 1

POWER-2

BGA
U1
EMPTY

HC_FM91_3948BGA

DESIGN NOTE: UNUSED FHT TILES

DESIGN NOTE: UNUSED FHT TILES

R64 0 RES — VCCERT1_FHT_GDR_U10 — CV50 CT50 CR49 CP50 CM50 CL49

1.0V (Group 1) +VCCERT1_FHT_GXF_1V0_UX_G1

BT50 BR49 BP50 BM50 BL49 BK50

R240R 0 RES — VCC_SENSE_FHT_12A — DF58
R240S 0 RES — VSS_SENSE_FHT_12A — DH58

VCC_SENSE_FHT_12B — AT58
VSS_SENSE_FHT_12B — AV58

R65 0 RES — VCCERT2_FHT_GDR_U10 — CM52 CK52

1.0V (Group 1) +VCCERT2_FHT_GXF_1V0_UX_G1

BM52 BK52

DESIGN NOTE: UNUSED FHT TILES

R129 0 RES — VCCEHT_FHT_GDR_U10 — CU51 CT52 CP52 CN51 CL51

1.5V (Group 2) +VCCEHT_FHT_GXF_1V5_U1X_G2

BU51 BT52 BP52 BN51 BL51

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99C1H7

DK20 DJ21 DH20 DF20 DE21 DD20 — VCCERT1_FHT_GDR_U20 — R132 1 0 RES

1.0V (Group 1) +VCCERT1_FHT_GXF_1V0_UX_G1

CK20 CJ21 CH20 CF20 CE21 CD20

EA19 VCC_SENSE_FHT_13A
DW19 VSS_SENSE_FHT_13A
R176 0 RES
R177 0 RES

DD12 DB12

DK18 DH18 — VCCERT2_FHT_GDR_U20 — R130 1 0 RES

1.0V (Group 1) +VCCERT2_FHT_GXF_1V0_UX_G1

CK18 CH18

DESIGN NOTE: UNUSED FHT TILES

R131 1 0 RES — VCCEHT_FHT_GDR_U20

1.5V (Group 2) +VCCEHT_FHT_GXF_1V5_U2X_G2

DJ19 DG19 DF18 DD18 DC19

CJ19 CG19 CF18 CD18 CC19

+P1V8_G2

R173 0 RES 0805
R174 0 RES 0805
R281 0 RES 0805

+VCCEHT_UX_GXF_U1X

C59 H94455-002 100UF 20% 4V X6S 0805

C69 H94455-002 100UF 20% 4V X6S 0805

+P1V8_G2

R175 0 RES 0805
R253 0 RES 0805
R282 0 RES 0805

+VCCEHT_UX_GXF_U2X

C70 H94455-002 100UF 20% 4V X6S 0805

C80 H94455-002 100UF 20% 4V X6S 0805

+VCCERT1_FHT_GXF_1V0_UX_G1

R2486 100 1% 0.0625W RES 0402 A36092-043

VCCERT1_1V0_SENSE_DP — R2410 0 RES — VCC_SENSE_FHT_12B

R2482 100 1% 0.0625W RES 0402 A36092-043

C2328 A36096-213 0.1UF 10% 25V X7R 0402

VCCERT1_1V0_SENSE_DN — R2411 0 RES — VSS_SENSE_FHT_12B

+VCCERT1_FHT_GXF_1V0_UX_G1

R2484 100 1% 0.0625W RES 0402 A36092-043

TP282 — VCC_SENSE_FHT_R_12C — R2412 0 RES — VCC_SENSE_FHT_12C

R2481 100 1% 0.0625W RES 0402 A36092-043

C2329 A36096-213 0.1UF 10% 25V X7R 0402

TP283 — VSS_SENSE_FHT_R_12C — R2413 0 RES — VSS_SENSE_FHT_12C

BGA
U1
EMPTY

HC_FM91_3948BGA

0.8V (Group 1) +VCC_HSSI_GXF_0V8_UX0_G1

DH48 DG47 DF48 DE47 DD48 DC47 DB48 DA47 CY48 CW47 CV48 CU47 CT48 CR47 CP48 CN47 CM48 CL47

0.8V (Group 1) +VCC_HSSI_GXF_0V8_UX2_G1

CH48 CG47 CF48 CE47 CD48 CC47 CB48 CA47 BY48 BW47 BV48 BU47 BT48 BR47 BP48 BN47 BM48 BL47

1.0V (Group 1) +VCCERT_UX_GXF_1V0_U1x_G1

DH50 DG49 DF50 DD50 DC49 DB50 CY50 CW49

1.0V (Group 1) +VCCERT_UX_GXF_1V0_U1x_G1

CG49 CF50 CD50 CC49 CB50 BY50 BW49 BV50

1.8V (Group 2) +VCCEHT_UX_GXF_U1X

DG51 DF52 DD52 DC51 DB52 CY52 CW51 CV52

1.8V (Group 2) +VCCEHT_UX_GXF_U1X

CG51 CF52 CD52 CC51 CB52 BY52 BW51 BV52

1.8V (Group 2) +VCCN_IO_GDR

DJ51 DH52

1.8V (Group 2) +VCCN_IO_GDR

CJ51 CH52

1.5V (Group 2) +VCCEFUSECORE_GXF_1V0_G2

DJ49 CJ49 CK22 BL21

[VCC_HSSI_GXFL_12A] [VCC_HSSI_GXFL_13A]
VCC_HSSI_GDR_U10 … VCC_HSSI_GDR_U20

[VCC_HSSI_GXFL_12B] [VCC_HSSI_GXFL_13B]
VCC_HSSI_GDR_U11 … VCC_HSSI_GDR_U21

[VCCERT_FGT_GXFL_12A] [VCCERT_FGT_GXFL_13A]
VCCERT_UX_GDR_U10 … VCCERT_UX_GDR_U20

[VCCERT_FGT_GXFL_12B] [VCCERT_FGT_GXFL_13B]
VCCERT_UX_GDR_U11 … VCCERT_UX_GDR_U21

[VCCH_FGT_GXFL_12A] [VCCH_FGT_GXFL_13A]
VCCEHT_UX_GDR_U10 … VCCEHT_UX_GDR_U20

[VCCH_FGT_GXFL_12B] [VCCH_FGT_GXFL_13B]
VCCEHT_UX_GDR_U11 … VCCEHT_UX_GDR_U21

[VCCCLK_GXFL_12A] [VCCCLK_GXFL_13A]
VCCN_IO_GDR_U10 … VCCN_IO_GDR_U20

[VCCCLK_GXFL_12B] [VCCCLK_GXFL_13B]
VCCN_IO_GDR_U11 … VCCN_IO_GDR_U21

[VCCFUSEWR_GXFL_***] [VCCFUSECORE_GXFL_***]
VCCFUSEWR_GDR_U10 … VCCFUSECORE_GDR_U10
VCCFUSEWR_GDR_U11 … VCCFUSECORE_GDR_U11
VCCFUSEWR_GDR_U20 … VCCFUSECORE_GDR_U20
VCCFUSEWR_GDR_U21 … VCCFUSECORE_GDR_U21

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99C1H7

0.8V (Group 1) +VCC_HSSI_GXF_0V8_UX0_G1

DJ23 DH22 DG23 DF22 DE23 DD22 DC23 DB22 DA23 CY22 CW23 CV22 CU23 CT22 CR23 CP22 CN23 CM22

0.8V (Group 1) +VCC_HSSI_GXF_0V8_UX1_G1

CJ23 CH22 CG23 CF22 CE23 CD22 CC23 CB22 CA23 BY22 BW23 BV22 BU23 BT22 BR23 BP22 BN23 BM22

1.0V (Group 1) +VCCERT_UX_GXF_1V0_U2x_G1

DB20 DA21 CY20 CV20 CU21 CT20 CP20 CN21

1.0V (Group 1) +VCCERT_UX_GXF_1V0_U2x_G1

CB20 CA21 BY20 BV20 BU21 BT20 BP20 BN21

1.8V (Group 2) +VCCEHT_UX_GXF_U2X

DB18 DA19 CW18 CV18 CU19 CR19 CP18 CN19

1.8V (Group 2) +VCCEHT_UX_GXF_U2X

CB18 CA19 BY18 BV18 BU19 BT18 BP18 BN19

1.8V (Group 2) +VCCN_IO_GDR

CM18 CL19

1.8V (Group 2) +VCCN_IO_GDR

BM18 BL19

1.8V (Group 2) +VCCEFUSECORE_GXF_1V0_G2

DK50 CK48 CL21 BK22

BGA
U1
EMPTY

HC_FM91_3948BGA

0.8V (Group 1) +VCC_HSSI_GXF_0V8_UX2_G1

BH48 BG47 BF48 BE47 BD48 BC47 BB48 BA47 AY48 AW47 AV48 AU47 AT48 AR47 AP48 AN47 AM48 AL47

1.0V (Group 1) +VCCERT_UX_GXF_1V0_U1x_G1

BG49 BF50 BD50 BC49 BB50 AY50 AW49 AV50

1.8V (Group 2) +VCCEHT_UX_GXF_U1X

BG51 BF52 BE51 BC51 BB52 BA51 AW51 AV52

1.8V (Group 2) +VCCN_IO_GDR

BJ51 BH52

1.8V (Group 2) +VCCEFUSECORE_GXF_1V0_G2

BK48 AK20

1.0V (Group 1) +VCCERT1_FHT_GXF_1V0_UX_G1

AT50 AR49 AP50 AM50 AL49 AK50

VCC_SENSE_FHT_12C — W51
VSS_SENSE_FHT_12C — AA51

1.0V (Group 1) +VCCERT2_FHT_GXF_1V0_UX_G1

AM52 AK52

1.5V (Group 2) +VCCEHT_FHT_GXF_1V5_U1X_G2

AU51 AT52 AP52 AN51 AL51

[VCC_HSSI_GXFL_12C] [VCC_HSSI_GXFL_13C]
VCC_HSSI_GDR_U12 … VCC_HSSI_GDR_U22

[VCCERT_FGT_GXFL_12C] [VCCERT_FGT_GXFL_13C]
VCCERT_UX_GDR_U12 … VCCERT_UX_GDR_U22

[VCCH_FGT_GXFL_12C] [VCCH_FGT_GXFL_13C]
VCCEHT_UX_GDR_U12 … VCCEHT_UX_GDR_U22

[VCCCLK_GXFL_12C] [VCCCLK_GXFL_13C]
VCCN_IO_GDR_U12 … VCCN_IO_GDR_U22

[VCCFUSEWR_GXFL_***] [VCCFUSECORE_GXFL_***]
VCCFUSEWR_GDR_U12 … VCCFUSECORE_GDR_U12
VCCFUSEWR_GDR_U22 … VCCFUSECORE_GDR_U22

[VCCERT1_FHT_GXFL_12C] [VCCERT1_FHT_GXFL_13C]
VCCERT1_BRK_GDR_U12 … VCCERT1_BRK_GDR_U22

[VCCERT2_FHT_GXFL_12C] [VCCERT2_FHT_GXFL_13C]
VCCERT2_BRK_GDR_U12 … VCCERT2_BRK_GDR_U22

[VCCEHT_FHT_GXFL_12C] [VCCEHT_FHT_GXFL_13C]
VCCEHT_BRK_GDR_U12 … VCCEHT_BRK_GDR_U22

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99C1H7

0.8V (Group 1) +VCC_HSSI_GXF_0V8_UX1_G1

BJ23 BH22 BG23 BF22 BE23 BD22 BC23 BB22 BA23 AY22 AW23 AV22 AU23 AT22 AR23 AP22 AN23 AM22

1.0V (Group 1) +VCCERT_UX_GXF_1V0_U2x_G1

BA21 AY20 AV20 AU21 AT20 AP20 AN21 AM20

1.8V (Group 2) +VCCEHT_UX_GXF_U2X

BB18 BA19 AY18 AV19 AU19 AT18 AP18 AN19

1.8V (Group 2) +VCCN_IO_GDR

AM18 AL19

1.0V (Group 1) +VCCEFUSECORE_GXF_1V0_G2

BJ49 AK22

1.0V (Group 1) +VCCERT1_FHT_GXF_1V0_UX_G1

BJ21 BH20 BF20 BE21 BD20 BB20

AP12 AM12

1.0V (Group 1) +VCCERT2_FHT_GXF_1V0_UX_G1

BK18 BH18

1.5V (Group 2) +VCCEHT_FHT_GXF_1V5_U2X_G2

BJ19 BG19 BF18 BD18 BC19

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DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation INTEL CORPORATION,BANGALORE INDIA, 560103	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET	28 OF 105

FPGA DECOUPLING - I

+VCCL_0V8_G1

VCCL

C2247 H94455-003 100UF 20% 2.5V X6S 0805
C2244 H94455-003 100UF 20% 2.5V X6S 0805
C2245 H94455-003 100UF 20% 2.5V X6S 0805
C2246 H94455-003 100UF 20% 2.5V X6S 0805
C2249 H94455-003 100UF 20% 2.5V X6S 0805
C2250 H94455-003 100UF 20% 2.5V X6S 0805
C2370 H94455-003 100UF 20% 2.5V X6S 0805
C2353 H94455-003 100UF 20% 2.5V X6S 0805
C2251 H94455-003 100UF 20% 2.5V X6S 0805
C2252 H94455-003 100UF 20% 2.5V X6S 0805
C781 H94455-003 100UF 20% 2.5V X6S 0805
C803 H94455-003 100UF 20% 2.5V X6S 0805
C805 H94455-003 100UF 20% 2.5V X6S 0805
C808 H94455-003 100UF 20% 2.5V X6S 0805

BOTTOM SIDE CAPS

C2267 H80885-001 10uF 20% 6.3V EMPTY 0402
C2268 H80885-001 10uF 20% 6.3V EMPTY 0402
C2269 H80885-001 10uF 20% 6.3V EMPTY 0402
C2270 H80885-001 10uF 20% 6.3V EMPTY 0402
C2271 H80885-001 10uF 20% 6.3V EMPTY 0402
C2272 H80885-001 10uF 20% 6.3V EMPTY 0402
C2273 H80885-001 10uF 20% 6.3V EMPTY 0402
C2274 H80885-001 10uF 20% 6.3V EMPTY 0402
C2275 H80885-001 10uF 20% 6.3V EMPTY 0402
C2276 H80885-001 10uF 20% 6.3V EMPTY 0402
C2277 H80885-001 10uF 20% 6.3V EMPTY 0402
C2278 H80885-001 10uF 20% 6.3V EMPTY 0402
C2279 H80885-001 10uF 20% 6.3V EMPTY 0402
C2280 H80885-001 10uF 20% 6.3V EMPTY 0402
C2281 H80885-001 10uF 20% 6.3V EMPTY 0402
C2282 H80885-001 10uF 20% 6.3V EMPTY 0402
C2283 H80885-001 10uF 20% 6.3V EMPTY 0402
C2284 H80885-001 10uF 20% 6.3V EMPTY 0402
C2285 H80885-001 10uF 20% 6.3V EMPTY 0402
C2286 H80885-001 10uF 20% 6.3V EMPTY 0402

C2287 H80885-001 10uF 20% 6.3V EMPTY 0402
C2288 H80885-001 10uF 20% 6.3V EMPTY 0402
C2289 H80885-001 10uF 20% 6.3V EMPTY 0402
C2290 H80885-001 10uF 20% 6.3V EMPTY 0402
C2291 H80885-001 10uF 20% 6.3V EMPTY 0402
C2292 H80885-001 10uF 20% 6.3V EMPTY 0402
C2293 H80885-001 10uF 20% 6.3V EMPTY 0402
C2294 H80885-001 10uF 20% 6.3V EMPTY 0402
C2295 H80885-001 10uF 20% 6.3V EMPTY 0402
C2296 H80885-001 10uF 20% 6.3V EMPTY 0402
C2297 H80885-001 10uF 20% 6.3V EMPTY 0402
C2298 H80885-001 10uF 20% 6.3V EMPTY 0402
C2299 H80885-001 10uF 20% 6.3V EMPTY 0402
C2300 H80885-001 10uF 20% 6.3V EMPTY 0402
C2301 H80885-001 10uF 20% 6.3V EMPTY 0402
C2302 H80885-001 10uF 20% 6.3V EMPTY 0402
C2303 H80885-001 10uF 20% 6.3V EMPTY 0402
C2304 H80885-001 10uF 20% 6.3V EMPTY 0402
C2305 H80885-001 10uF 20% 6.3V EMPTY 0402
C2306 H80885-001 10uF 20% 6.3V EMPTY 0402

C603 H80885-001 10uF 20% 6.3V EMPTY 0402
C625 H80885-001 10uF 20% 6.3V EMPTY 0402
C636 H80885-001 10uF 20% 6.3V EMPTY 0402
C648 H80885-001 10uF 20% 6.3V EMPTY 0402
C689 H80885-001 10uF 20% 6.3V EMPTY 0402
C700 H80885-001 10uF 20% 6.3V EMPTY 0402
C766 H80885-001 10uF 20% 6.3V EMPTY 0402
C769 H80885-001 10uF 20% 6.3V EMPTY 0402
C772 H80885-001 10uF 20% 6.3V EMPTY 0402
C776 H80885-001 10uF 20% 6.3V EMPTY 0402

BOTTOM SIDE CAPS

C2307 H94455-003 100UF 20% 2.5V X6S 0805
C2308 H94455-003 100UF 20% 2.5V X6S 0805
C2309 H94455-003 100UF 20% 2.5V X6S 0805
C2310 H94455-003 100UF 20% 2.5V X6S 0805
C2311 H94455-003 100UF 20% 2.5V X6S 0805
C2337 H94455-003 100UF 20% 2.5V X6S 0805
C2243 H94455-003 100UF 20% 2.5V X6S 0805
C2248 H94455-003 100UF 20% 2.5V X6S 0805
C774 H94455-003 100UF 20% 2.5V X6S 0805
C779 H94455-003 100UF 20% 2.5V X6S 0805
C801 H94455-003 100UF 20% 2.5V X6S 0805
C806 H94455-003 100UF 20% 2.5V X6S 0805

C604 H94455-003 100UF 20% 2.5V X6S 0805
C619 H94455-003 100UF 20% 2.5V X6S 0805
C629 H94455-003 100UF 20% 2.5V X6S 0805
C656 H94455-003 100UF 20% 2.5V X6S 0805
C698 H94455-003 100UF 20% 2.5V X6S 0805
C708 H94455-003 100UF 20% 2.5V X6S 0805
C767 H94455-003 100UF 20% 2.5V X6S 0805
C770 H94455-003 100UF 20% 2.5V X6S 0805
C775 H94455-003 100UF 20% 2.5V X6S 0805
C780 H94455-003 100UF 20% 2.5V X6S 0805
C802 H94455-003 100UF 20% 2.5V X6S 0805
C807 H94455-003 100UF 20% 2.5V X6S 0805

PERIPHERAL SURROUNDING FPGA

+P0V8_G1

VCCH

C2392 H63299-001 22UF 20% 6.3V X6S 0603
C2393 H63299-001 22UF 20% 6.3V X6S 0603
C2394 H63299-001 22UF 20% 6.3V X6S 0603
C2395 H63299-001 22UF 20% 6.3V X6S 0603
C2427 C95333-006 47UF 20% 4V X6S 0805
C2426 C95333-006 47UF 20% 4V X6S 0805

BOTTOM SIDE CAPS

PERIPHERAL SURROUNDING FPGA

+P1V8_G2

VCCPT

C773 J33429-001 4.7uF 20% 6.3V X5R 0201
C777 J33429-001 4.7uF 20% 6.3V X5R 0201
C782 H80885-001 10uF 20% 6.3V X6S 0402

BOTTOM SIDE CAPS

PERIPHERAL SURROUNDING FPGA

VCCR_CORE

+P1V2_G3

C810 C83410-015 1uF 10% 6.3V X5R 0201

BOTTOM SIDE CAPS

+P1V2_G3

L22 IND 19A 0.1UH SM

IRMS : 19A
ISAT : 29A

VCCA_PLL

+VCCA_PLL

C814 H80883-001 22uF 20% 16V X6S 0805
C816 C95333-006 47UF 20% 4V X6S 0805
C818 H94455-003 100UF 20% 2.5V X6S 0805
C820 H80885-001 10UF 20% 6.3V X6S 0402
C821 H80885-001 10UF 20% 6.3V X6S 0402

PERIPHERAL SURROUNDING FPGA

BOTTOM SIDE CAPS

+P1V2_G3

VCCIO_PIO PER CHANNEL

C596 J33429-001 4.7uF 20% 6.3V X5R 0201
C616 J33429-001 4.7uF 20% 6.3V X5R 0201
C639 H80885-001 10uF 20% 6.3V X6S 0402
C674 J33429-001 4.7uF 20% 6.3V X5R 0201
C699 J33429-001 4.7uF 20% 6.3V X5R 0201
C765 H80885-001 10uF 20% 6.3V X6S 0402
C768 J33429-001 4.7uF 20% 6.3V X5R 0201
C771 J33429-001 4.7uF 20% 6.3V X5R 0201
C778 H80885-001 10uF 20% 6.3V X6S 0402
C800 J33429-001 4.7uF 20% 6.3V X5R 0201
C804 J33429-001 4.7uF 20% 6.3V X5R 0201
C809 H80885-001 10uF 20% 6.3V X6S 0402
C811 J33429-001 4.7uF 20% 6.3V X5R 0201
C812 J33429-001 4.7uF 20% 6.3V X5R 0201
C813 H80885-001 10uF 20% 6.3V X6S 0402
C815 J33429-001 4.7uF 20% 6.3V X5R 0201
C817 J33429-001 4.7uF 20% 6.3V X5R 0201
C819 H80885-001 10uF 20% 6.3V X6S 0402

BOTTOM SIDE CAPS

PERIPHERAL SURROUNDING FPGA

C597 J33429-001 4.7uF 20% 6.3V EMPTY 0201
C618 J33429-001 4.7uF 20% 6.3V EMPTY 0201
C644 H80885-001 10uF 20% 6.3V EMPTY 0402

BOTTOM SIDE CAPS

PERIPHERAL SURROUNDING FPGA

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DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	29 OF 105

INTEL AGILEX® 7 FPGA I-SERIES (6x F-TILE) DECOUPLING 1

FPGA DECOUPLING - II

VCCH_SDM

+P0V8_G1

C822 C83410-015 1uF 10% 6.3V X5R 0201

BOTTOM SIDE CAPS

VCCL_SDM

+VCC_HSSI_GXF_0V8_UX0_G1

C833 C83410-015 1uF 10% 6.3V X5R 0201

C839 C83410-015 1uF 10% 6.3V X5R 0201

BOTTOM SIDE CAPS

VCCIO_PIO_SDM

+P1V2_G3

C848 C83410-015 1uF 10% 6.3V X5R 0201

BOTTOM SIDE CAPS

VCCPLLDIG_SDM

+VCC_HSSI_GXF_0V8_UX0_G1

FB11 22 8A FB 0603

+VCCPLLDIG_SDM

C867 C95333-006 47UF 20% 4V X6S 0805

C870 C95333-006 47UF 20% 4V X6S 0805

BOTTOM SIDE CAPS

C874 C83410-015 1uF 10% 6.3V X5R 0201

PERIPHERAL SURROUNDING FPGA

VCCPLL_ADC_SDM

+P1V8_G2

FB12 22 8A FB 0603

+VCCPLL_ADC_SDM

C894 C95333-006 47UF 20% 4V X6S 0805

C896 H80883-001 22uF 20% 16V X6S 0805

C901 H80883-001 22uF 20% 16V X6S 0805

BOTTOM SIDE CAPS

C933 C83410-015 1uF 10% 6.3V X5R 0201

C849 C83410-015 1uF 10% 6.3V X5R 0201

PERIPHERAL SURROUNDING FPGA

VCCN_IO_GDR

+P1V8_G2

FB10 22 8A FB 0603

+VCCN_IO_GDR

C834 C95333-006 47UF 20% 4V X6S 0805

C840 H80883-001 22uF 20% 16V X6S 0805

C845 H80883-001 22uF 20% 16V X6S 0805

PERIPHERAL SURROUNDING FPGA

VCCIO_SDM

+P1V8_G3

C857 C83410-015 1uF 10% 6.3V X5R 0201

C861 H80885-001 10uF 20% 6.3V X6S 0402

PERIPHERAL SURROUNDING FPGA

BOTTOM SIDE CAPS

VCCBAT_SDM

+P1V8_VCCBAT

C871 C83410-015 1uF 10% 6.3V X5R 0201

C876 H80885-001 10uF 20% 6.3V X6S 0402

PERIPHERAL SURROUNDING FPGA

BOTTOM SIDE CAPS

VCCFUSEWR_SDM

+P1V8_G3

C883 C83410-015 1uF 10% 6.3V X5R 0201

C892 J33429-001 4.7uF 20% 6.3V X5R 0201

PERIPHERAL SURROUNDING FPGA

BOTTOM SIDE CAPS

VCC_HSSI_GDR

+VCC_HSSI_GXF_0V8_UX0_G1

C899 H80885-001 10uF 20% 6.3V X6S 0402

C904 H80885-001 10uF 20% 6.3V X6S 0402

C934 C95333-006 47UF 20% 4V X6S 0805

C995 C95333-006 47UF 20% 4V X6S 0805

PERIPHERAL SURROUNDING FPGA

BOTTOM SIDE CAPS

NOTE: PLACE NEAR VCC_HSSI_GDR_U10 PINS

VCC_HSSI_GDR

+VCC_HSSI_GXF_0V8_UX0_G1

C825 H80885-001 10uF 20% 6.3V X6S 0402

C829 H80885-001 10uF 20% 6.3V X6S 0402

C835 C95333-006 47UF 20% 4V X6S 0805

C841 C95333-006 47UF 20% 4V X6S 0805

PERIPHERAL SURROUNDING FPGA

BOTTOM SIDE CAPS

NOTE: PLACE NEAR VCC_HSSI_GDR_U20 PINS

VCC_HSSI_GDR

+VCC_HSSI_GXF_0V8_UX1_G1

C852 H80885-001 10uF 20% 6.3V X6S 0402

C855 H80885-001 10uF 20% 6.3V X6S 0402

C859 C95333-006 47UF 20% 4V X6S 0805

C863 C95333-006 47UF 20% 4V X6S 0805

PERIPHERAL SURROUNDING FPGA

BOTTOM SIDE CAPS

NOTE: PLACE NEAR VCC_HSSI_GDR_U11 PINS

VCC_HSSI_GDR

+VCC_HSSI_GXF_0V8_UX1_G1

C875 H80885-001 10uF 20% 6.3V X6S 0402

C878 H80885-001 10uF 20% 6.3V X6S 0402

C885 C95333-006 47UF 20% 4V X6S 0805

C891 C95333-006 47UF 20% 4V X6S 0805

PERIPHERAL SURROUNDING FPGA

BOTTOM SIDE CAPS

NOTE: PLACE NEAR VCC_HSSI_GDR_U21 PINS

VCC_HSSI_GDR

+VCC_HSSI_GXF_0V8_UX2_G1

C900 H80885-001 10uF 20% 6.3V X6S 0402

C905 H80885-001 10uF 20% 6.3V X6S 0402

C935 C95333-006 47UF 20% 4V X6S 0805

C996 C95333-006 47UF 20% 4V X6S 0805

PERIPHERAL SURROUNDING FPGA

BOTTOM SIDE CAPS

NOTE: PLACE NEAR VCC_HSSI_GDR_U12 PINS

VCC_HSSI_GDR

+VCC_HSSI_GXF_0V8_UX2_G1

C826 H80885-001 10uF 20% 6.3V X6S 0402

C830 H80885-001 10uF 20% 6.3V X6S 0402

C836 C95333-006 47UF 20% 4V X6S 0805

C842 C95333-006 47UF 20% 4V X6S 0805

PERIPHERAL SURROUNDING FPGA

BOTTOM SIDE CAPS

NOTE: PLACE NEAR VCC_HSSI_GDR_U22 PINS

VCCERT_UX_GDR

+VCCERT_UX_GXF_1V0_U1x_G1

C853 H80885-001 10uF 20% 6.3V X6S 0402

C856 H80885-001 10uF 20% 6.3V X6S 0402

C860 C95333-006 47UF 20% 4V X6S 0805

C866 C95333-006 47UF 20% 4V X6S 0805

C868 C95333-006 47UF 20% 4V X6S 0805

C872 C95333-006 47UF 20% 4V X6S 0805

PERIPHERAL SURROUNDING FPGA

BOTTOM SIDE CAPS

NOTE: PLACE NEAR VCCERT_UX_GDR_U10 PINS

VCCERT_UX_GDR

+VCCERT_UX_GXF_1V0_U1x_G1

C884 H80885-001 10uF 20% 6.3V X6S 0402

C886 H80885-001 10uF 20% 6.3V X6S 0402

C895 C95333-006 47UF 20% 4V X6S 0805

C898 C95333-006 47UF 20% 4V X6S 0805

C902 C95333-006 47UF 20% 4V X6S 0805

C915 C95333-006 47UF 20% 4V X6S 0805

PERIPHERAL SURROUNDING FPGA

BOTTOM SIDE CAPS

NOTE: PLACE NEAR VCCERT_UX_GDR_U11 PINS

VCCERT_UX_GDR

+VCCERT_UX_GXF_1V0_U1x_G1

C827 H80885-001 10uF 20% 6.3V X6S 0402

C831 H80885-001 10uF 20% 6.3V X6S 0402

C837 C95333-006 47UF 20% 4V X6S 0805

C843 C95333-006 47UF 20% 4V X6S 0805

C846 C95333-006 47UF 20% 4V X6S 0805

C850 C95333-006 47UF 20% 4V X6S 0805

PERIPHERAL SURROUNDING FPGA

BOTTOM SIDE CAPS

NOTE: PLACE NEAR VCCERT_UX_GDR_U12 PINS

VCCERT_UX_GDR

+VCCERT_UX_GXF_1V0_U2x_G1

C858 H80885-001 10uF 20% 6.3V X6S 0402

C862 H80885-001 10uF 20% 6.3V X6S 0402

C869 C95333-006 47UF 20% 4V X6S 0805

C873 C95333-006 47UF 20% 4V X6S 0805

C877 C95333-006 47UF 20% 4V X6S 0805

C879 C95333-006 47UF 20% 4V X6S 0805

PERIPHERAL SURROUNDING FPGA

BOTTOM SIDE CAPS

NOTE: PLACE NEAR VCCERT_UX_GDR_U20 PINS

VCCERT_UX_GDR

+VCCERT_UX_GXF_1V0_U2x_G1

C893 H80885-001 10uF 20% 6.3V X6S 0402

C897 H80885-001 10uF 20% 6.3V X6S 0402

C903 C95333-006 47UF 20% 4V X6S 0805

C919 C95333-006 47UF 20% 4V X6S 0805

C937 C95333-006 47UF 20% 4V X6S 0805

C997 C95333-006 47UF 20% 4V X6S 0805

PERIPHERAL SURROUNDING FPGA

BOTTOM SIDE CAPS

NOTE: PLACE NEAR VCCERT_UX_GDR_U21 PINS

VCCERT_UX_GDR

+VCCERT_UX_GXF_1V0_U2x_G1

C828 H80885-001 10uF 20% 6.3V X6S 0402

C832 H80885-001 10uF 20% 6.3V X6S 0402

C838 C95333-006 47UF 20% 4V X6S 0805

C844 C95333-006 47UF 20% 4V X6S 0805

C847 C95333-006 47UF 20% 4V X6S 0805

C851 C95333-006 47UF 20% 4V X6S 0805

PERIPHERAL SURROUNDING FPGA

BOTTOM SIDE CAPS

NOTE: PLACE NEAR VCCERT_UX_GDR_U22 PINS

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PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	30 OF 105

INTEL AGILEX® 7 FPGA I-SERIES (6x F-TILE) DECOUPIING 2

FPGA DECOUPLING - III

VCCERT2_FHT_GDR — BOTTOM SIDE CAPS

+VCCERT2_FHT_GXF_1V0_UX_G1	+VCCERT2_FHT_GXF_1V0_UX_G1	+VCCERT2_FHT_GXF_1V0_UX_G1	+VCCERT2_FHT_GXF_1V0_UX_G1	+VCCERT2_FHT_GXF_1V0_UX_G1	+VCCERT2_FHT_GXF_1V0_UX_G1
C1062 H80885-001 10uF 20% 6.3V X6S 0402	C1115 H80885-001 10uF 20% 6.3V X6S 0402	C1127 H80885-001 10uF 20% 6.3V X6S 0402	C1330 H80885-001 10uF 20% 6.3V X6S 0402	C1336 H80885-001 10uF 20% 6.3V X6S 0402	C1351 H80885-001 10uF 20% 6.3V X6S 0402
NOTE: PLACE NEAR VCCERT2_FHT_GDR_U10	NOTE: PLACE NEAR VCCERT2_FHT_GDR_U11	NOTE: PLACE NEAR VCCERT2_FHT_GDR_U12	NOTE: PLACE NEAR VCCERT2_FHT_GDR_U20	NOTE: PLACE NEAR VCCERT2_FHT_GDR_U21	NOTE: PLACE NEAR VCCERT2_FHT_GDR_U22

VCCERT1_FHT_GDR

+VCCERT1_FHT_GXF_1V0_UX_G1

C1359 H80885-001 10uF 20% 6.3V X6S 0402
C1364 H80885-001 10uF 20% 6.3V X6S 0402
C1367 C95333-006 47UF 20% 4V EMPTY 0805
C1372 C95333-006 47UF 20% 4V X6S 0805

PERIPHERAL SURROUNDING FPGA

BOTTOM SIDE CAPS

NOTE: PLACE NEAR VCCERT1_FHT_GDR_U10 PINS

VCCERT1_FHT_GDR

+VCCERT1_FHT_GXF_1V0_UX_G1

C1380 H80885-001 10UF 20% 6.3V EMPTY 0402
C1383 H80885-001 10UF 20% 6.3V EMPTY 0402
C1388 C95333-006 47UF 20% 4V X6S 0805
C1392 C95333-006 47UF 20% 4V X6S 0805

PERIPHERAL SURROUNDING FPGA

BOTTOM SIDE CAPS

NOTE: PLACE NEAR VCCERT1_FHT_GDR_U11 PINS

VCCERT1_FHT_GDR

+VCCERT1_FHT_GXF_1V0_UX_G1

C1064 H80885-001 10uF 20% 6.3V X6S 0402
C1113 H80885-001 10uF 20% 6.3V X6S 0402
C1123 C95333-006 47UF 20% 4V X6S 0805
C1126 C95333-006 47UF 20% 4V X6S 0805

PERIPHERAL SURROUNDING FPGA

BOTTOM SIDE CAPS

NOTE: PLACE NEAR VCCERT1_FHT_GDR_U12 PINS

VCCERT1_FHT_GDR

+VCCERT1_FHT_GXF_1V0_UX_G1

C1332 H80885-001 10uF 20% 6.3V X6S 0402
C1333 H80885-001 10UF 20% 6.3V EMPTY 0402
C1347 C95333-006 47UF 20% 4V EMPTY 0805
C1349 C95333-006 47UF 20% 4V X6S 0805

PERIPHERAL SURROUNDING FPGA

BOTTOM SIDE CAPS

NOTE: PLACE NEAR VCCERT1_FHT_GDR_U20 PINS

VCCERT1_FHT_GDR

+VCCERT1_FHT_GXF_1V0_UX_G1

C1356 H80885-001 10uF 20% 6.3V X6S 0402
C1360 H80885-001 10UF 20% 6.3V EMPTY 0402
C1365 C95333-006 47UF 20% 4V EMPTY 0805
C1368 C95333-006 47UF 20% 4V X6S 0805

PERIPHERAL SURROUNDING FPGA

BOTTOM SIDE CAPS

NOTE: PLACE NEAR VCCERT1_FHT_GDR_U21 PINS

VCCERT1_FHT_GDR

+VCCERT1_FHT_GXF_1V0_UX_G1

C1376 H80885-001 10uF 20% 6.3V X6S 0402
C1381 H80885-001 10UF 20% 6.3V X6S 0402
C1384 C95333-006 47UF 20% 4V X6S 0805
C1389 C95333-006 47UF 20% 4V EMPTY 0805

PERIPHERAL SURROUNDING FPGA

BOTTOM SIDE CAPS

NOTE: PLACE NEAR VCCERT1_FHT_GDR_U22 PINS

VCCEHT_UX_GXF

+VCCEHT_UX_GXF_U1X	+VCCEHT_UX_GXF_U1X	+VCCEHT_UX_GXF_U1X	+VCCEHT_UX_GXF_U2X	+VCCEHT_UX_GXF_U2X	+VCCEHT_UX_GXF_U2X		
C1054 H80885-001 10uF 20% 6.3V X6S 0402 / C1065 H80885-001 10uF 20% 6.3V X6S 0402	C1118 H80885-001 10uF 20% 6.3V X6S 0402 / C1124 H80885-001 10UF 20% 6.3V X6S 0402	C1187 H80885-001 10uF 20% 6.3V X6S 0402 / C1190 H80885-001 10uF 20% 6.3V X6S 0402	C1334 H80885-001 10uF 20% 6.3V X6S 0402 / C1348 H80885-001 10uF 20% 6.3V X6S 0402	C1353 H80885-001 10uF 20% 6.3V X6S 0402 / C1354 H80885-001 10UF 20% 6.3V X6S 0402	C1358 H80885-001 10uF 20% 6.3V X6S 0402 / C1362 H80885-001 10UF 20% 6.3V X6S 0402		
BOTTOM SIDE CAPS	BOTTOM SIDE CAPS	BOTTOM SIDE CAPS	BOTTOM SIDE CAPS	BOTTOM SIDE CAPS	BOTTOM SIDE CAPS		
NOTE: PLACE NEAR VCCEHT_UX_GXF_U10	NOTE: PLACE NEAR VCCEHT_UX_GXF_U11	NOTE: PLACE NEAR VCCEHT_UX_GXF_U12	NOTE: PLACE NEAR VCCEHT_UX_GXF_U20	NOTE: PLACE NEAR VCCEHT_UX_GXF_U21	NOTE: PLACE NEAR VCCEHT_UX_GXF_U22		

VCCEHT_FHT_GDR

+VCCEHT_FHT_GXF_1V5_U1X_G2	+VCCEHT_FHT_GXF_1V5_U1X_G2	+VCCEHT_FHT_GXF_1V5_U1X_G2		
C1369 H80885-001 10UF 20% 6.3V EMPTY 0402 / C1373 H80885-001 10UF 20% 6.3V EMPTY 0402	C1377 H80885-001 10uF 20% 6.3V X6S 0402 / C1379 H80885-001 10UF 20% 6.3V X6S 0402	C1386 H80885-001 10uF 20% 6.3V X6S 0402 / C1391 H80885-001 10UF 20% 6.3V X6S 0402		
BOTTOM SIDE CAPS	BOTTOM SIDE CAPS	BOTTOM SIDE CAPS		
NOTE: PLACE NEAR VCCEHT_FHT_GDR_U10	NOTE: PLACE NEAR VCCEHT_FHT_GDR_U12	NOTE: PLACE NEAR VCCEHT_FHT_GDR_U11		

VCCEHT_FHT_GDR

+VCCEHT_FHT_GXF_1V5_U2X_G2	+VCCEHT_FHT_GXF_1V5_U2X_G2	+VCCEHT_FHT_GXF_1V5_U2X_G2
C1061 H80885-001 10UF 20% 6.3V EMPTY 0402 / C1100 H80885-001 10UF 20% 6.3V EMPTY 0402	C1122 H80885-001 10uF 20% 6.3V X6S 0402 / C1125 H80885-001 10uF 20% 6.3V X6S 0402	C1189 H80885-001 10uF 20% 6.3V X6S 0402 / C1329 H80885-001 10uF 20% 6.3V X6S 0402
BOTTOM SIDE CAPS	BOTTOM SIDE CAPS	BOTTOM SIDE CAPS
NOTE: PLACE NEAR VCCEHT_FHT_GDR_U20	NOTE: PLACE NEAR VCCEHT_FHT_GDR_U21	NOTE: PLACE NEAR VCCEHT_FHT_GDR_U22

VCCFUSECORE_GDR — BOTTOM SIDE CAPS

+VCCEFUSECORE_GXF_1V0_G2	+VCCEFUSECORE_GXF_1V0_G2	+VCCEFUSECORE_GXF_1V0_G2	+VCCEFUSECORE_GXF_1V0_G2	+VCCEFUSECORE_GXF_1V0_G2	+VCCEFUSECORE_GXF_1V0_G2
C1335 J33429-001 4.7uF 20% 6.3V X5R 0201	C1350 J33429-001 4.7uF 20% 6.3V X5R 0201	C1355 J33429-001 4.7uF 20% 6.3V X5R 0201	C1363 J33429-001 4.7uF 20% 6.3V X5R 0201	C1370 J33429-001 4.7uF 20% 6.3V X5R 0201	C1375 J33429-001 4.7uF 20% 6.3V X5R 0201
NOTE: PLACE NEAR VCCFUSECORE_GDR_U10	NOTE: PLACE NEAR VCCFUSECORE_GDR_U11	NOTE: PLACE NEAR VCCFUSECORE_GDR_U12	NOTE: PLACE NEAR VCCFUSECORE_GDR_U20	NOTE: PLACE NEAR VCCFUSECORE_GDR_U21	NOTE: PLACE NEAR VCCFUSECORE_GDR_U22

VCCN_IO_GDR

+VCCN_IO_GDR

C1382 H80885-001 10uF 20% 6.3V X6S 0402
C1387 H80885-001 10uF 20% 6.3V X6S 0402

BOTTOM SIDE CAPS

NOTE: PLACE NEAR VCCN_IO_GDR_U10

VCCFUSEWR_GDR — BOTTOM SIDE CAPS

+VCCEFUSECORE_GXF_1V0_G2	+VCCEFUSECORE_GXF_1V0_G2	+VCCEFUSECORE_GXF_1V0_G2	+VCCEFUSECORE_GXF_1V0_G2	+VCCEFUSECORE_GXF_1V0_G2	+VCCEFUSECORE_GXF_1V0_G2
C1063 C83410-015 1uF 10% 6.3V X5R 0201	C1117 C83410-015 1uF 10% 6.3V X5R 0201	C1149 C83410-015 1uF 10% 6.3V X5R 0201	C1331 C83410-015 1uF 10% 6.3V X5R 0201	C1346 C83410-015 1uF 10% 6.3V X5R 0201	C1352 C83410-015 1uF 10% 6.3V X5R 0201
NOTE: PLACE NEAR VCCFUSEWR_GDR_U10	NOTE: PLACE NEAR VCCFUSEWR_GDR_U11	NOTE: PLACE NEAR VCCFUSEWR_GDR_U12	NOTE: PLACE NEAR VCCFUSEWR_GDR_U20	NOTE: PLACE NEAR VCCFUSEWR_GDR_U21	NOTE: PLACE NEAR VCCFUSEWR_GDR_U22

VCCN_IO_GDR

+VCCN_IO_GDR	+VCCN_IO_GDR	+VCCN_IO_GDR	+VCCN_IO_GDR	+VCCN_IO_GDR
C1357 H80885-001 10uF 20% 6.3V X6S 0402 / C1361 H80885-001 10uF 20% 6.3V X6S 0402	C1366 H80885-001 10uF 20% 6.3V X6S 0402 / C1371 H80885-001 10uF 20% 6.3V X6S 0402	C1374 H80885-001 10uF 20% 6.3V X6S 0402 / C1378 H80885-001 10uF 20% 6.3V X6S 0402	C1385 H80885-001 10uF 20% 6.3V X6S 0402 / C1390 H80885-001 10uF 20% 6.3V X6S 0402	
BOTTOM SIDE CAPS	BOTTOM SIDE CAPS	BOTTOM SIDE CAPS	BOTTOM SIDE CAPS	
NOTE: PLACE NEAR VCCN_IO_GDR_U11	NOTE: PLACE NEAR VCCN_IO_GDR_U12	NOTE: PLACE NEAR VCCN_IO_GDR_U20	NOTE: PLACE NEAR VCCN_IO_GDR_U21	

VCCN_IO_GDR

+VCCN_IO_GDR

C2139 H80885-001 10uF 20% 6.3V X6S 0402
C2137 H80885-001 10uF 20% 6.3V X6S 0402

BOTTOM SIDE CAPS

NOTE: PLACE NEAR VCCN_IO_GDR_U22

INTEL AGILEX® 7 FPGA I-SERIES (6x F-TILE) DECOUPLING 3

Tue Sep 26 11:47:41 2023

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER / REV
PSG	INTEL CORPORATION,BANGALORE INDIA, 560103	C+	34649	150-0330690-A2 / 2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 31 OF 105

1DPC DIMM

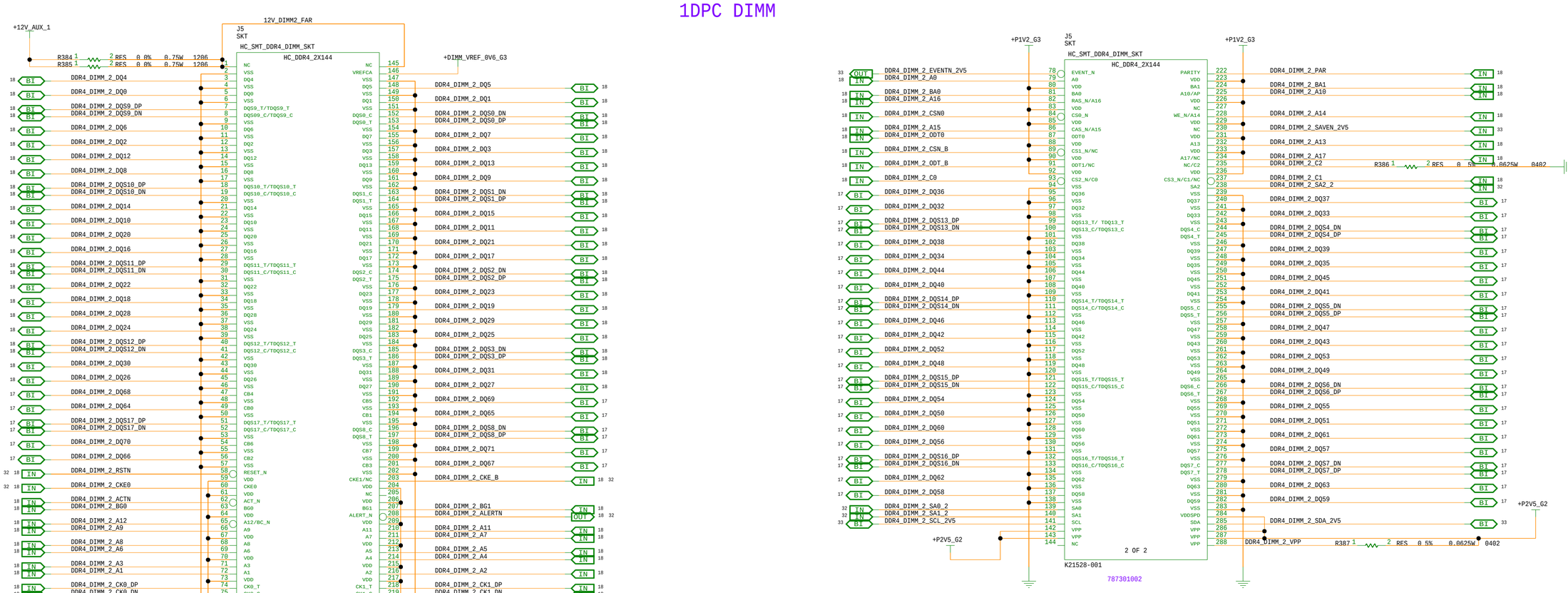

Figure 55. Signal connections for DDR4 1DPC DIMM configuration using SMT DIMM connector

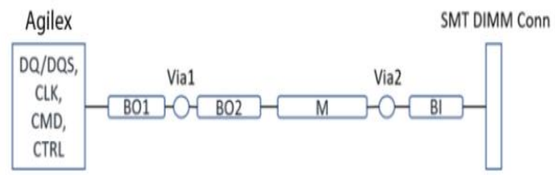

Table 94. Specific DDR4 1DPC routing guidelines for UDIMM, RDIMM, LRDIMM, and SODIMM configurations

Signal Group	Segment	Routing Layer	Max Length (mil)		Target Zse (ohms)	Target Width, W (mil)	Trace Spacing, S1 (mil): Within Group	Trace Spacing, S2 (mil): CMD/CTRL/CLK to DQ/DQS	Trace Spacing, S3 (mil):DQ Nibble to Nibble	Trace Spacing (mil), Within DIFF pair	Trace Spacing (mil), DQS pair to DQ	Trace Spacing (mil), CLK pair to CMD/CTRL/CKE	Channel to Channel Spacing (DQ to DQ, between two channels)
			Segment	Total MS									
CLK	BO1	US	50	4500		4	5, 17	5, 17		4		17	
	BO2	SL	1000			4	5, 17	5, 17		4		17	
	M	SL			45	4.5		12 (3h)		4		12 (3)	
	BI	US	50			4		12 (3h)		4		12 (3h)	
CMD, CTRL, ALERT	BO1	US	50	4500		4	5, 17	5, 17					
	BO2	SL	1000			4	5, 17	5, 17					
	M	SL			45	4.5		8 (2h)	12 (3h)				
	BI	US	100			4		8 (2h)	12 (3h)				
DQ	BO1	US	50	4500		3	5, 17		17				17
	BO2	SL	1000			3	5, 17		17				17
	M	SL			50	3.5		8 (2h)	12 (3h)				16 (4h)
	BI	US	50			3.5		8 (2h)	12 (3h)				16 (4h)
DQS	BO1	US	50	4500		3	5, 17			4	17		
	BO2	SL	1000			3	5, 17			4	17		
	M	SL			50	3.5				4	12 (3h)		
	BI	US	50			3.5							

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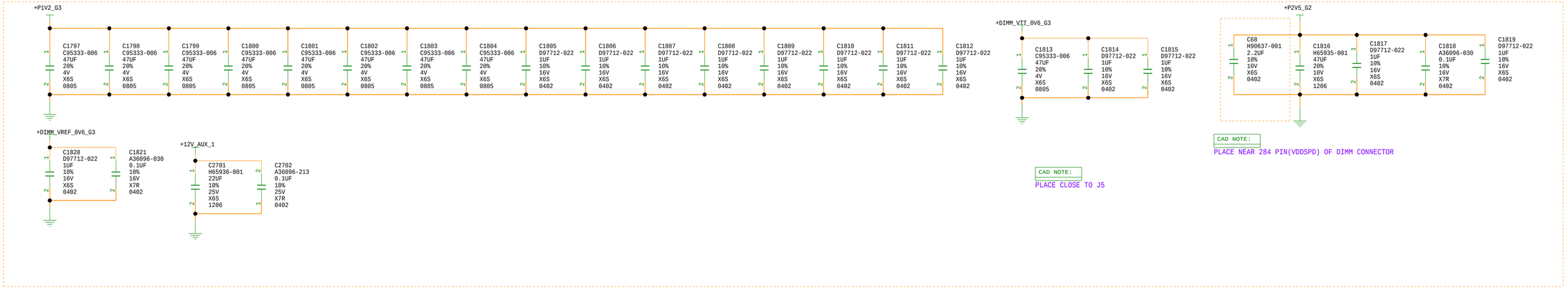
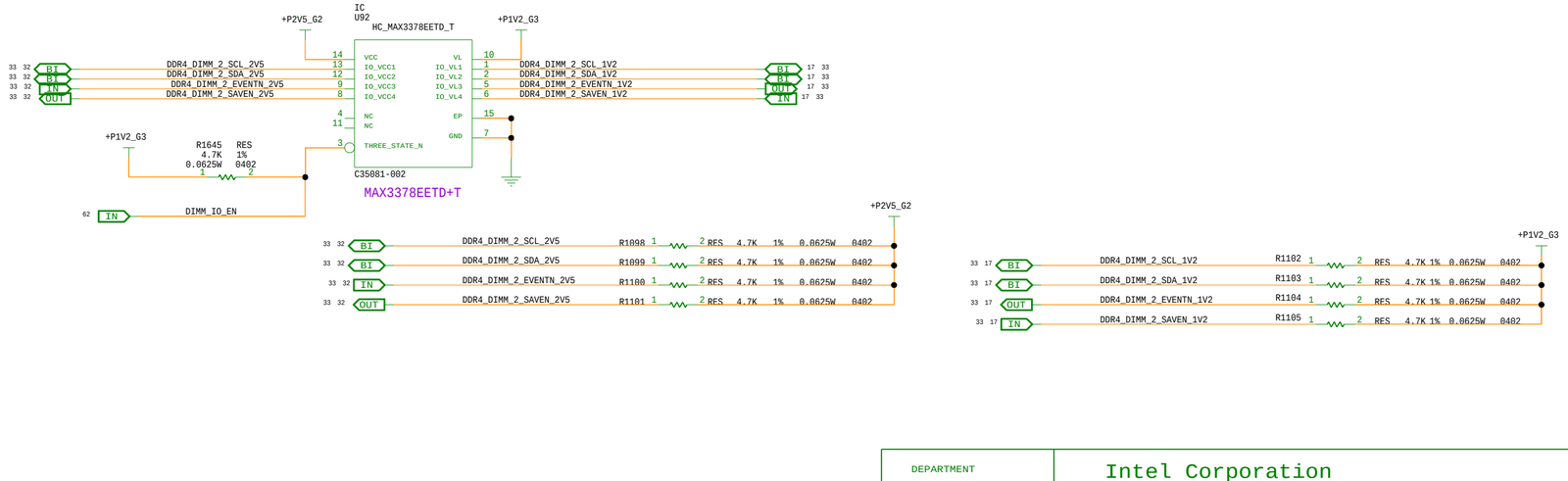
DDR4 DIMM

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE	SCALE:	DO NOT SCALE DRAWING	SHEET	32 OF 105
	INDIA, 560103				

1DPC DIMM-FILTER AND LVL SHIFTER





Tue Sep 26 11:47:43 2023

DIMM FILTER & LEVEL SHIFTETR

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE	SCALE:	DO NOT SCALE DRAWING	SHEET	33 OF 105
	INDIA, 560103				

DDR4-I

BGA
U109
IC
HC_MT40A2G16SKL

DDR4_A0 DDR4_A1 DDR4_A2 DDR4_A3 DDR4_A4 DDR4_A5 DDR4_A6 DDR4_A7 DDR4_A8 DDR4_A9 DDR4_A10 DDR4_A11 DDR4_A12 DDR4_A13 DDR4_A14 DDR4_A15 DDR4_A16
DDR4_BG0 DDR4_BG1 DDR4_BA0 DDR4_BA1
DDR4_CS_N DDR4_ODT DDR4_ACT_N DDR4_PAR DDR4_CKE
DDR4_RESET_N
DDR4_CK_DP DDR4_CK_DN

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10_AP A11 A12_BC_N A13 WE_N_A14 CAS_N_A15 RAS_N_A16
BG0 BG1 BA0 BA1
CS_N ODT ACT_N PAR CKE
RESET_N
CK_T CK_C
VREFCA

VDD0 VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9
VDDQ0 VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9
VSS0 VSS1 VSS2 VSS3 VSS4 VSS7 VSS8 NF
VSSQ0 VSSQ1 VSSQ2 VSSQ3 VSSQ4 VSSQ5 VSSQ6 VSSQ7 VSSQ8 VSSQ9
VPP0 VPP1
TEN

LDQ0 LDQ1 LDQ2 LDQ3 LDQ4 LDQ5 LDQ6 LDQ7 UDQ0 UDQ1 UDQ2 UDQ3 UDQ4 UDQ5 UDQ6 UDQ7
DDR4_0_DQ0 DDR4_0_DQ1 DDR4_0_DQ2 DDR4_0_DQ3 DDR4_0_DQ4 DDR4_0_DQ5 DDR4_0_DQ6 DDR4_0_DQ7 DDR4_0_DQ8 DDR4_0_DQ9 DDR4_0_DQ10 DDR4_0_DQ11 DDR4_0_DQ12 DDR4_0_DQ13 DDR4_0_DQ14 DDR4_0_DQ15
NF_UDM_N_UDBI_N NF_LDM_N_LDBI_N
DDR4_DM1 DDR4_DM0
UDQS_T UDQS_C LDQS_T LDQS_C
DDR4_DQS_1_DP DDR4_DQS_1_DN DDR4_DQS_0_DP DDR4_DQS_0_DN
ALERT_N
DDR4_ALERT_N
LZQ
UZQ
TP_LZQ0
TP_UZQ0

K41096-002
MT40A2G16SKL-062E:B

+DDR4_VREF_0V6_G3
C2019 H87607-002 0.1UF 10% 6.3V X7R 0201

+P1V2_G3
+P2V5_G2

C2020 C83410-015 1UF 10% 6.3V X5R 0201
C2021 C83410-015 1UF 10% 6.3V X5R 0201
R2075 K15783-001 240 1% 0.1W RES 0402
R1976 K15783-001 240 1% 0.1W RES 0402

BGA
U113
IC
HC_MT40A2G16SKL

DDR4_A0 DDR4_A1 DDR4_A2 DDR4_A3 DDR4_A4 DDR4_A5 DDR4_A6 DDR4_A7 DDR4_A8 DDR4_A9 DDR4_A10 DDR4_A11 DDR4_A12 DDR4_A13 DDR4_A14 DDR4_A15 DDR4_A16
DDR4_BG0 DDR4_BG1 DDR4_BA0 DDR4_BA1
DDR4_CS_N DDR4_ODT DDR4_ACT_N DDR4_PAR DDR4_CKE
DDR4_RESET_N
DDR4_CK_DP DDR4_CK_DN

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10_AP A11 A12_BC_N A13 WE_N_A14 CAS_N_A15 RAS_N_A16
BG0 BG1 BA0 BA1
CS_N ODT ACT_N PAR CKE
RESET_N
CK_T CK_C
VREFCA

VDD0 VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9
VDDQ0 VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9
VSS0 VSS1 VSS2 VSS3 VSS4 VSS7 VSS8 NF
VSSQ0 VSSQ1 VSSQ2 VSSQ3 VSSQ4 VSSQ5 VSSQ6 VSSQ7 VSSQ8 VSSQ9
VPP0 VPP1
TEN

LDQ0 LDQ1 LDQ2 LDQ3 LDQ4 LDQ5 LDQ6 LDQ7 UDQ0 UDQ1 UDQ2 UDQ3 UDQ4 UDQ5 UDQ6 UDQ7
DDR4_1_DQ16 DDR4_1_DQ17 DDR4_1_DQ18 DDR4_1_DQ19 DDR4_1_DQ20 DDR4_1_DQ21 DDR4_1_DQ22 DDR4_1_DQ23 DDR4_1_DQ24 DDR4_1_DQ25 DDR4_1_DQ26 DDR4_1_DQ27 DDR4_1_DQ28 DDR4_1_DQ29 DDR4_1_DQ30 DDR4_1_DQ31
NF_UDM_N_UDBI_N NF_LDM_N_LDBI_N
DDR4_DM3 DDR4_DM2
UDQS_T UDQS_C LDQS_T LDQS_C
DDR4_DQS_3_DP DDR4_DQS_3_DN DDR4_DQS_2_DP DDR4_DQS_2_DN
ALERT_N
DDR4_ALERT_N
LZQ
UZQ
TP_LZQ1
TP_UZQ1

K41096-002
MT40A2G16SKL-062E:B

+DDR4_VREF_0V6_G3
C2022 H87607-002 0.1UF 10% 6.3V X7R 0201

+P1V2_G3
+P2V5_G2

C2023 C83410-015 1UF 10% 6.3V X5R 0201
C2024 C83410-015 1UF 10% 6.3V X5R 0201
R2076 K15783-001 240 1% 0.1W RES 0402
R1977 K15783-001 240 1% 0.1W RES 0402

+P1V2_G3

C2035 A36096-027 1UF 10% 6.3V X5R 0402
C2059 A36096-027 1UF 10% 6.3V X5R 0402
C2043 A36096-027 1UF 10% 6.3V X5R 0402
C2027 A36096-027 1UF 10% 6.3V X5R 0402
C2031 H87607-002 0.1UF 10% 6.3V X7R 0201
C2087 H87607-002 0.1UF 10% 6.3V X7R 0201
C2067 H87607-002 0.1UF 10% 6.3V X7R 0201
C2047 H87607-002 0.1UF 10% 6.3V X7R 0201
C2063 H87607-002 0.1UF 10% 6.3V X7R 0201
C2051 K31665-001 1UF 20% 6.3V X6S 0201
C2055 K31665-001 1UF 20% 6.3V X6S 0201
C2075 D70538-004 1NF 10% 25V X7R 0201

CAD NOTE:
PLACE THE CAPACITORS NEAR PINS OF COMPONENT

+P1V2_G3

C2036 A36096-027 1UF 10% 6.3V X5R 0402
C2060 A36096-027 1UF 10% 6.3V X5R 0402
C2044 A36096-027 1UF 10% 6.3V X5R 0402
C2028 A36096-027 1UF 10% 6.3V X5R 0402
C2032 H87607-002 0.1UF 10% 6.3V X7R 0201
C2090 H87607-002 0.1UF 10% 6.3V X7R 0201
C2068 H87607-002 0.1UF 10% 6.3V X7R 0201
C2048 H87607-002 0.1UF 10% 6.3V X7R 0201
C2064 H87607-002 0.1UF 10% 6.3V X7R 0201
C2052 K31665-001 1UF 20% 6.3V X6S 0201
C2056 K31665-001 1UF 20% 6.3V X6S 0201
C2076 D70538-004 1NF 10% 25V X7R 0201

CAD NOTE:
PLACE THE CAPACITORS NEAR PINS OF COMPONENT

+P1V2_G3

C2086 H80885-001 10UF 20% 6.3V X6S 0402
C2039 H80885-001 10UF 20% 6.3V X6S 0402

+P2V5_G2

C2104 A36096-134 4.7UF 20% 10V X5R 0402
C2071 J33429-001 4.7UF 20% 6.3V X5R 0201
C2088 J33429-001 4.7UF 20% 6.3V X5R 0201

+P1V2_G3

C2089 H80885-001 10UF 20% 6.3V X6S 0402
C2040 H80885-001 10UF 20% 6.3V X6S 0402

+P2V5_G2

C2105 A36096-134 4.7UF 20% 10V X5R 0402
C2072 J33429-001 4.7UF 20% 6.3V X5R 0201
C2091 J33429-001 4.7UF 20% 6.3V X5R 0201

Tue Sep 26 11:47:43 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	34 OF 105

DDR4-II

BGA
U115
IC
HC_MT40A2G16SKL

DDR4_A0 DDR4_A1 DDR4_A2 DDR4_A3 DDR4_A4 DDR4_A5 DDR4_A6 DDR4_A7 DDR4_A8 DDR4_A9 DDR4_A10 DDR4_A11 DDR4_A12 DDR4_A13 DDR4_A14 DDR4_A15 DDR4_A16
DDR4_BG0 DDR4_BG1 DDR4_BA0 DDR4_BA1
DDR4_CS_N DDR4_ODT DDR4_ACT_N DDR4_PAR DDR4_CKE
DDR4_RESET_N
DDR4_CK_DP DDR4_CK_DN

+DDR4_VREF_0V6_G3
+P1V2_G3
+P2V5_G2

C2010 H87607-002 0.1UF 10% 6.3V X7R 0201
C2011 C83410-015 1UF 10% 6.3V X5R 0201
C2012 C83410-015 1UF 10% 6.3V X5R 0201
R2043 K15783-001 240 1% 0.1W RES 0402
R1960 K15783-001 240 1% 0.1W RES 0402

DDR4_2_DQ32 DDR4_2_DQ33 DDR4_2_DQ34 DDR4_2_DQ35 DDR4_2_DQ36 DDR4_2_DQ37 DDR4_2_DQ38 DDR4_2_DQ39 DDR4_2_DQ40 DDR4_2_DQ41 DDR4_2_DQ42 DDR4_2_DQ43 DDR4_2_DQ44 DDR4_2_DQ45 DDR4_2_DQ46 DDR4_2_DQ47
DDR4_DM5 DDR4_DM4
DDR4_DQS_5_DP DDR4_DQS_5_DN DDR4_DQS_4_DP DDR4_DQS_4_DN
DDR4_ALERT_N
TP_LZQ2 TP_UZQ2

K41096-002
MT40A2G16SKL-062E:B

+P1V2_G3

C585 A36096-027 1UF 10% 6.3V X5R 0402
C612 A36096-027 1UF 10% 6.3V X5R 0402
C605 A36096-027 1UF 10% 6.3V X5R 0402
C579 A36096-027 1UF 10% 6.3V X5R 0402
C580 H87607-002 0.1UF 10% 6.3V X7R 0201
C2078 H87607-002 0.1UF 10% 6.3V X7R 0201
C615 H87607-002 0.1UF 10% 6.3V X7R 0201
C606 H87607-002 0.1UF 10% 6.3V X7R 0201
C613 H87607-002 0.1UF 10% 6.3V X7R 0201
C610 K31665-001 1UF 20% 6.3V X6S 0201
C611 K31665-001 1UF 20% 6.3V X6S 0201
C733 D70538-004 1NF 10% 25V X7R 0201

CAD NOTE:
PLACE THE CAPACITORS NEAR PINS OF COMPONENT

+P1V2_G3

C2077 H80885-001 10UF 20% 6.3V X6S 0402
C587 H80885-001 10UF 20% 6.3V X6S 0402

+P2V5_G2

C2101 A36096-134 4.7UF 20% 10V X5R 0402
C695 J33429-001 4.7UF 20% 6.3V X5R 0201
C2079 J33429-001 4.7UF 20% 6.3V X5R 0201

BGA
U119
IC
HC_MT40A2G16SKL

DDR4_A0 DDR4_A1 DDR4_A2 DDR4_A3 DDR4_A4 DDR4_A5 DDR4_A6 DDR4_A7 DDR4_A8 DDR4_A9 DDR4_A10 DDR4_A11 DDR4_A12 DDR4_A13 DDR4_A14 DDR4_A15 DDR4_A16
DDR4_BG0 DDR4_BG1 DDR4_BA0 DDR4_BA1
DDR4_CS_N DDR4_ODT DDR4_ACT_N DDR4_PAR DDR4_CKE
DDR4_RESET_N
DDR4_CK_DP DDR4_CK_DN

+DDR4_VREF_0V6_G3
+P1V2_G3
+P2V5_G2

C2013 H87607-002 0.1UF 10% 6.3V X7R 0201
C2014 C83410-015 1UF 10% 6.3V X5R 0201
C2015 C83410-015 1UF 10% 6.3V X5R 0201
R2044 K15783-001 240 1% 0.1W RES 0402
R1961 K15783-001 240 1% 0.1W RES 0402

DDR4_3_DQ48 DDR4_3_DQ49 DDR4_3_DQ50 DDR4_3_DQ51 DDR4_3_DQ52 DDR4_3_DQ53 DDR4_3_DQ54 DDR4_3_DQ55 DDR4_3_DQ56 DDR4_3_DQ57 DDR4_3_DQ58 DDR4_3_DQ59 DDR4_3_DQ60 DDR4_3_DQ61 DDR4_3_DQ62 DDR4_3_DQ63
DDR4_DM7 DDR4_DM6
DDR4_DQS_7_DP DDR4_DQS_7_DN DDR4_DQS_6_DP DDR4_DQS_6_DN
DDR4_ALERT_N
TP_LZQ3 TP_UZQ3

K41096-002
MT40A2G16SKL-062E:B

+P1V2_G3

C2033 A36096-027 1UF 10% 6.3V X5R 0402
C2057 A36096-027 1UF 10% 6.3V X5R 0402
C2041 A36096-027 1UF 10% 6.3V X5R 0402
C2025 A36096-027 1UF 10% 6.3V X5R 0402
C2029 H87607-002 0.1UF 10% 6.3V X7R 0201
C2081 H87607-002 0.1UF 10% 6.3V X7R 0201
C2065 H87607-002 0.1UF 10% 6.3V X7R 0201
C2045 H87607-002 0.1UF 10% 6.3V X7R 0201
C2061 H87607-002 0.1UF 10% 6.3V X7R 0201
C2049 K31665-001 1UF 20% 6.3V X6S 0201
C2053 K31665-001 1UF 20% 6.3V X6S 0201
C2073 D70538-004 1NF 10% 25V X7R 0201

CAD NOTE:
PLACE THE CAPACITORS NEAR PINS OF COMPONENT

+P1V2_G3

C2080 H80885-001 10UF 20% 6.3V X6S 0402
C2037 H80885-001 10UF 20% 6.3V X6S 0402

+P2V5_G2

C2102 A36096-134 4.7UF 20% 10V X5R 0402
C2069 J33429-001 4.7UF 20% 6.3V X5R 0201
C2082 J33429-001 4.7UF 20% 6.3V X5R 0201

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DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
UNKNOWN	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET	35 OF 105

DDR4-II

DDR4-III

BGA
U120
1C

HC_MT40A2G16SKL

DDR4_A0	P3	A0	LDQ0	G2	DDR4_4_DQ64	BI	14
DDR4_A1	P7	A1	LDQ1	F7	DDR4_4_DQ65	BI	14
DDR4_A2	R3	A2	LDQ2	H3	DDR4_4_DQ66	BI	14
DDR4_A3	N7	A3	LDQ3	H7	DDR4_4_DQ67	BI	14
DDR4_A4	N3	A4	LDQ4	H2	DDR4_4_DQ68	BI	14
DDR4_A5	P8	A5	LDQ5	H8	DDR4_4_DQ69	BI	14
DDR4_A6	P2	A6	LDQ6	J3	DDR4_4_DQ70	BI	14
DDR4_A7	R8	A7	LDQ7	J7	DDR4_4_DQ71	BI	14
DDR4_A8	R2	A8	UDQ0	A3			
DDR4_A9	R7	A9	UDQ1	B8			
DDR4_A10	M3	A10_AP	UDQ2	C3			
DDR4_A11	T2	A11	UDQ3	C7			
DDR4_A12	M7	A12_BC_N	UDQ4	C2			
DDR4_A13	T8	A13	UDQ5	C8			
DDR4_A14	L2	WE_N_A14	UDQ6	D3			
DDR4_A15	M8	CAS_N_A15	UDQ7	D7			
DDR4_A16	L8	RAS_N_A16	NF_UDM_N_UDBI_N	E2			
			NF_LDM_N_LDBI_N	E7	DDR4_DM8	BI	14
DDR4_BG0	M2	BG0	UDQS_T	B7			
DDR4_BG1	M9	BG1	UDQS_C	A7			
DDR4_BA0	N2	BA0	LDQS_T	G3	DDR4_DQS_8_DP	BI	14
DDR4_BA1	N8	BA1	LDQS_C	F3	DDR4_DQS_8_DN	BI	14
DDR4_CS_N	L7	CS_N	ALERT_N	P9	DDR4_ALERT_N	OUT	14 34 35
DDR4_ODT	K3	ODT	LZQ	F9	TP_LZQ4		
DDR4_ACT_N	L3	ACT_N	UZQ	E9	TP_UZQ4		
DDR4_PAR	T3	PAR	VPP0	R9			
DDR4_CKE	K2	CKE	VPP1	B1			
DDR4_RESET_N	P1	RESET_N	VSS0	B2			
DDR4_CK_DP	K7	CK_T	VSS1	E1			
DDR4_CK_DN	K8	CK_C	VSS2	G8			
	M1	VREFCA	VSS3	K1			
	B3	VDD0	VSS4	K9			
	B9	VDD1	VSS7	N1			
	D1	VDD2	VSS8	T1			
	G7	VDD3	NF	T7			
	J1	VDD4	VSSQ0	A2			
	J9	VDD5	VSSQ1	A8			
	L1	VDD6	VSSQ2	C9			
	L9	VDD7	VSSQ3	D2			
	R1	VDD8	VSSQ4	D8			
	T9	VDD9	VSSQ5	E3			
	A1	VDDQ0	VSSQ6	E8			
	A9	VDDQ1	VSSQ7	F1			
	C1	VDDQ2	VSSQ8	H1			
	D9	VDDQ3	VSSQ9	H9			
	F2	VDDQ4	TEN	N9			
	F8	VDDQ5					
	G1	VDDQ6					
	G9	VDDQ7					
	J2	VDDQ8					
	J8	VDDQ9					

K41096-002

MT40A2G16SKL-062E:B

+DDR4_VREF_0V6_G3

C2016
H87607-002
0.1UF
10%
6.3V
X7R
0201

+P1V2_G3

+P2V5_G2

C2017
C83410-015
1UF
10%
6.3V
X5R
0201

C2018
C83410-015
1UF
10%
6.3V
X5R
0201

R2045
K15783-001
240
1%
0.1W
RES
0402

R1962
K15783-001
240
1%
0.1W
RES
0402

+P1V2_G3

C2034 A36096-027 1UF 10% 6.3V X5R 0402
C2058 A36096-027 1UF 10% 6.3V X5R 0402
C2042 A36096-027 1UF 10% 6.3V X5R 0402
C2026 H87607-002 0.1UF 10% 6.3V X7R 0201
C2030 H87607-002 0.1UF 10% 6.3V X7R 0201
C2084 H87607-002 0.1UF 10% 6.3V X7R 0201
C2066 H87607-002 0.1UF 10% 6.3V X7R 0201
C2046 H87607-002 0.1UF 10% 6.3V X7R 0201
C2062 H87607-002 0.1UF 10% 6.3V X7R 0201
C2050 K31665-001 1UF 20% 6.3V X6S 0201
C2054 K31665-001 1UF 20% 6.3V X6S 0201
C2074 D70538-004 1NF 10% 25V X7R 0201

CAD NOTE:

PLACE THE CAPACITORS NEAR PINS OF COMPONENT

+P1V2_G3

C2083 H80885-001 10UF 20% 6.3V X6S 0402
C2038 H80885-001 10UF 20% 6.3V X6S 0402

+P2V5_G2

C2103 A36096-134 4.7UF 20% 10V X5R 0402
C2070 J33429-001 4.7UF 20% 6.3V X5R 0201
C2085 J33429-001 4.7UF 20% 6.3V X5R 0201

+DDR4_VTT_0V6_G3

C1714 D97712-022 1uF 10% 16V X6S 0402
C1715 D97712-022 1uF 10% 16V X6S 0402
C1716 D97712-022 1uF 10% 16V X6S 0402
C1717 D97712-022 1uF 10% 16V X6S 0402
C1718 H80885-001 10uF 20% 6.3V X6S 0402
C1719 H80885-001 10uF 20% 6.3V X6S 0402
C1720 H80885-001 10uF 20% 6.3V X6S 0402

+DDR4_VTT_0V6_G3

C2128 602433-109 47uF 20% 6.3V X5R 0603
C2132 A36096-134 4.7uF 20% 10V X5R 0402

R2050	RES	1%	C48657-238	0201	DDR4_A0	OUT	14 34 35 36
R2051	RES	1%	C48657-238	0201	DDR4_A1	OUT	14 34 35 36
R2052	RES	1%	C48657-238	0201	DDR4_A2	OUT	14 34 35 36
R 2290	RES	1%	C48657-238	0201	DDR4_A3	OUT	14 34 35 36
R2053	RES	1%	C48657-238	0201	DDR4_A4	OUT	14 34 35 36
R2054	RES	1%	C48657-238	0201	DDR4_A5	OUT	14 34 35 36
R2055	RES	1%	C48657-238	0201	DDR4_A6	OUT	14 34 35 36
R2056	RES	1%	C48657-238	0201	DDR4_A7	OUT	14 34 35 36
R2057	RES	1%	C48657-238	0201	DDR4_A8	OUT	14 34 35 36
R2058	RES	1%	C48657-238	0201	DDR4_A9	OUT	14 34 35 36
R2059	RES	1%	C48657-238	0201	DDR4_A10	OUT	14 34 35 36
R2060	RES	1%	C48657-238	0201	DDR4_A11	OUT	14 34 35 36
R2061	RES	1%	C48657-238	0201	DDR4_A12	OUT	14 34 35 36
R2062	RES	1%	C48657-238	0201	DDR4_A13	OUT	14 34 35 36
R2063	RES	1%	C48657-238	0201	DDR4_A14	OUT	14 34 35 36
R2064	RES	1%	C48657-238	0201	DDR4_A15	OUT	14 34 35 36
R2065	RES	1%	C48657-238	0201	DDR4_A16	OUT	14 34 35 36
R2066	RES	1%	C48657-238	0201	DDR4_BG0	OUT	14 34 35 36
R2067	RES	1%	C48657-238	0201	DDR4_BG1	OUT	14 34 35 36
R2068	RES	1%	C48657-238	0201	DDR4_BA0	OUT	14 34 35 36
R2069	RES	1%	C48657-238	0201	DDR4_BA1	OUT	14 34 35 36
R2070	RES	1%	C48657-238	0201	DDR4_CS_N	OUT	14 34 35 36
R2071	RES	1%	C48657-238	0201	DDR4_ODT	OUT	14 34 35 36
R2072	RES	1%	C48657-238	0201	DDR4_ACT_N	OUT	14 34 35 36
R2073	RES	1%	C48657-238	0201	DDR4_PAR	OUT	14 34 35 36
R2074	RES	1%	C48657-238	0201	DDR4_CKE	OUT	14 34 35 36

+P1V2_G3

C2129
H61346-001
10nF
10%
50V
X7R
0402

DDR4_CK

C2131
H61346-001
10nF
10%
50V
EMPTY
0402

R2046	RES	1%	C48657-238	0201	DDR4_CK_DP	OUT	14 34 35 36
R2047	RES	1%	C48657-238	0201	DDR4_CK_DN	OUT	14 34 35 36

R2048 4.75K RES 1% A93548-200 0402 DDR4_RESET_N OUT 14 34 35 36

+P1V2_G3

DDR4_ALERT_N R291 RES 4.7K

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DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER / REV
UNKNOWN	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	C+	34649	150-0330690-A2 / 2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 36 OF 105

DDR4-III

QSFP-0

12B-BANK

+P3V3_IO1_QSFP0

IDC : 2.4A
ISAT : 2.5A

L23 1UH 2.5A IND SM

C1227 A36096-030 0.1uF 10% 16V X7R 0402
C1229 K46765-001 22UF 20% 6.3V X5R 0402
C1231 A36096-030 0.1uF 10% 16V X7R 0402
C1233 K46765-001 22UF 20% 6.3V X5R 0402

+P3V3_QSFP0_VCCT

L25 1UH 2.5A IND SM

IDC : 2.4A
ISAT : 2.5A

C1234 A36096-030 0.1uF 10% 16V X7R 0402
C1239 K46765-001 22UF 20% 6.3V X5R 0402

+P3V3_QSFP0_VCCR

L26 1UH 2.5A IND SM

IDC : 2.4A
ISAT : 2.5A

C1235 A36096-030 0.1uF 10% 16V X7R 0402
C1240 K46765-001 22UF 20% 6.3V X5R 0402

+P3V3_QSFP0_VCC

+P3V3_QSFP0_VCC
+P3V3_QSFP0_VCCR
+P3V3_QSFP0_VCCT

SM
J57
SCON
HC_QSFP_1704320001

VCC 30
VCCR 10
VCCT 29

23 IN 23 IN	QSFP0_TX_0_DP / QSFP0_TX_0_DN	36 / 37	TD1_DP / TD1_DN	RD1_DP / RD1_DN	17 / 18	QSFP0_RX_0_DP / QSFP0_RX_0_DN	OUT 23 OUT 23
23 IN 23 IN	QSFP0_TX_1_DP / QSFP0_TX_1_DN	3 / 2	TD2_DP / TD2_DN	RD2_DP / RD2_DN	22 / 21	QSFP0_RX_1_DP / QSFP0_RX_1_DN	OUT 23 OUT 23
23 IN 23 IN	QSFP0_TX_2_DP / QSFP0_TX_2_DN	33 / 34	TD3_DP / TD3_DN	RD3_DP / RD3_DN	14 / 15	QSFP0_RX_2_DP / QSFP0_RX_2_DN	OUT 23 OUT 23
23 IN 23 IN	QSFP0_TX_3_DP / QSFP0_TX_3_DN	6 / 5	TD4_DP / TD4_DN	RD4_DP / RD4_DN	25 / 24	QSFP0_RX_3_DP / QSFP0_RX_3_DN	OUT 23 OUT 23
				INT_N / MOD_PRS_N	28 / 27	QSFP0_INTERRUPT_N / QSFP0_MOD_PRS_N	OUT 37 47 OUT 47 59
48 37 IN	QSFP0_MOD_SEL_N	8	MOD_SEL_N				
47 37 IN	QSFP0_LP_MODE	31	LP_MODE				
47 37 IN	QSFP0_RST	9	RST_N				
48 46 42 IN / 48 46 42 BI	I2C_QSFP_1_SCL / I2C_QSFP_1_SDA	11 / 12	SCL / SDA				

GND 1, 4, 7, 13, 16, 19, 20, 23, 26, 32, 35, 38

K11736-001

1704320001

I2C SLAVE ADDRESS: 50H

+P3V3_IO1_QSFP0

47 37	QSFP0_RST	R1686	1 2 RES	4.7K
47 37	QSFP0_LP_MODE	R1689	1 2 RES	4.7K
47 37	QSFP0_INTERRUPT_N	R1690	1 2 RES	4.7K

+P3V3

48 37	QSFP0_MOD_SEL_N	R1685	1 2 RES	4.7K

TH
XJ15
CON
HC_HS_10EM

CAGE_GND 1, 2, 3, 4, 5, 6, 7, 8, 9, 10

N17779-001
U95L1111001

R1010 RES 10K 1% 0.0625W 0402
C1468 X7R 4700PF 10% 50V 0402

GND_QSFP0_CAGE

QSFP-1

12C-BANK

+P3V3_IO1_QSFP1

IDC : 2.4A
ISAT : 2.5A

L24 1UH 2.5A IND SM

C1228 A36096-030 0.1uF 10% 16V X7R 0402
C1230 K46765-001 22UF 20% 6.3V X5R 0402
C1232 A36096-030 0.1uF 10% 16V X7R 0402
C1236 K46765-001 22UF 20% 6.3V X5R 0402

+P3V3_QSFP1_VCCT

L27 1UH 2.5A IND SM

IDC : 2.4A
ISAT : 2.5A

C1237 A36096-030 0.1uF 10% 16V X7R 0402
C1241 K46765-001 22UF 20% 6.3V X5R 0402

+P3V3_QSFP1_VCCR

L28 1UH 2.5A IND SM

IDC : 2.4A
ISAT : 2.5A

C1238 A36096-030 0.1uF 10% 16V X7R 0402
C1242 K46765-001 22UF 20% 6.3V X5R 0402

+P3V3_QSFP1_VCC

+P3V3_QSFP1_VCC
+P3V3_QSFP1_VCCR
+P3V3_QSFP1_VCCT

SM
J58
SCON
HC_QSFP_1704320001

VCC 30
VCCR 10
VCCT 29

22 IN 22 IN	QSFP1_TX_0_DP / QSFP1_TX_0_DN	36 / 37	TD1_DP / TD1_DN	RD1_DP / RD1_DN	17 / 18	QSFP1_RX_0_DP / QSFP1_RX_0_DN	OUT 22 OUT 22
22 IN 22 IN	QSFP1_TX_1_DP / QSFP1_TX_1_DN	3 / 2	TD2_DP / TD2_DN	RD2_DP / RD2_DN	22 / 21	QSFP1_RX_1_DP / QSFP1_RX_1_DN	OUT 22 OUT 22
22 IN 22 IN	QSFP1_TX_2_DP / QSFP1_TX_2_DN	33 / 34	TD3_DP / TD3_DN	RD3_DP / RD3_DN	14 / 15	QSFP1_RX_2_DP / QSFP1_RX_2_DN	OUT 22 OUT 22
22 IN 22 IN	QSFP1_TX_3_DP / QSFP1_TX_3_DN	6 / 5	TD4_DP / TD4_DN	RD4_DP / RD4_DN	25 / 24	QSFP1_RX_3_DP / QSFP1_RX_3_DN	OUT 22 OUT 22
				INT_N / MOD_PRS_N	28 / 27	QSFP1_INTERRUPT_N / QSFP1_MOD_PRS_N	OUT 37 47 OUT 47 59
48 37 IN	QSFP1_MOD_SEL_N	8	MOD_SEL_N				
47 37 IN	QSFP1_LP_MODE	31	LP_MODE				
47 37 IN	QSFP1_RST	9	RST_N				
48 43 IN / 48 43 BI	I2C_QSFP_3_SCL / I2C_QSFP_3_SDA	11 / 12	SCL / SDA				

GND 1, 4, 7, 13, 16, 19, 20, 23, 26, 32, 35, 38

K11736-001

1704320001

I2C SLAVE ADDRESS: 50H

+P3V3

48 37	QSFP1_MOD_SEL_N	R879	1 2 RES	4.7K

+P3V3_IO1_QSFP1

47 37	QSFP1_RST	R882	1 2 RES	4.7K
47 37	QSFP1_LP_MODE	R881	1 2 RES	4.7K
47 37	QSFP1_INTERRUPT_N	R900	1 2 RES	4.7K

TH
XJ16
CON
HC_HS_10EM

CAGE_GND 1, 2, 3, 4, 5, 6, 7, 8, 9, 10

N17779-001
U95L1111001

R1017 RES 10K 1% 0.0625W 0402
C1531 X7R 4700PF 10% 50V 0402

GND_QSFP1_CAGE

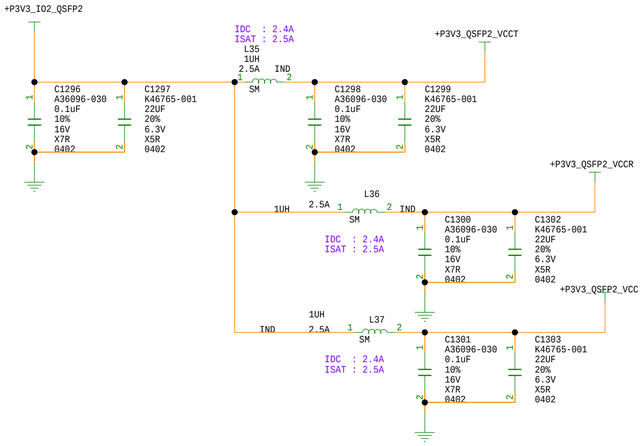
Tue Sep 26 11:47:45 2023

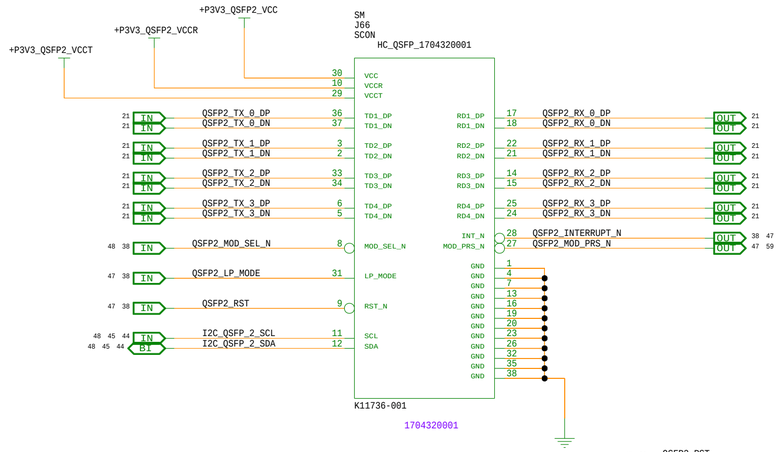
QSFP-0,1

DEPARTMENT		SIZE	C+
PSG		CODE	34649
		DOCUMENT NUMBER	150-0330690-A2
		REV	2.0
SCALE:	DO NOT SCALE DRAWING	SHEET	37 OF 105

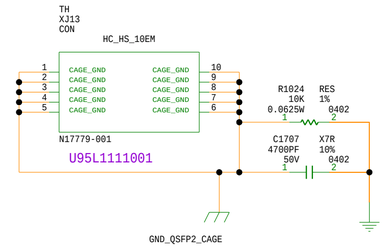
QSFP-2

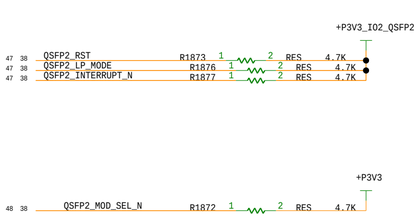
13A-BANK





I2C SLAVE ADDRESS: 50H





Tue Sep 26 11:47:45 2023

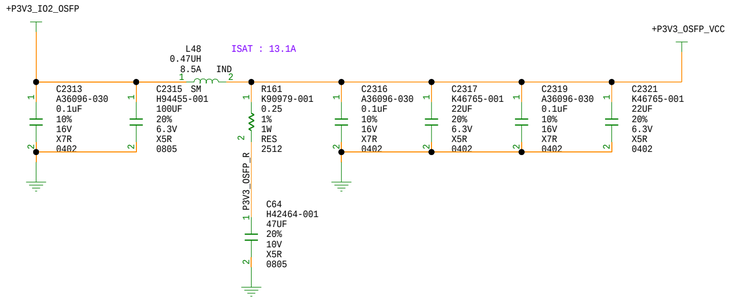
DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	38 OF 105

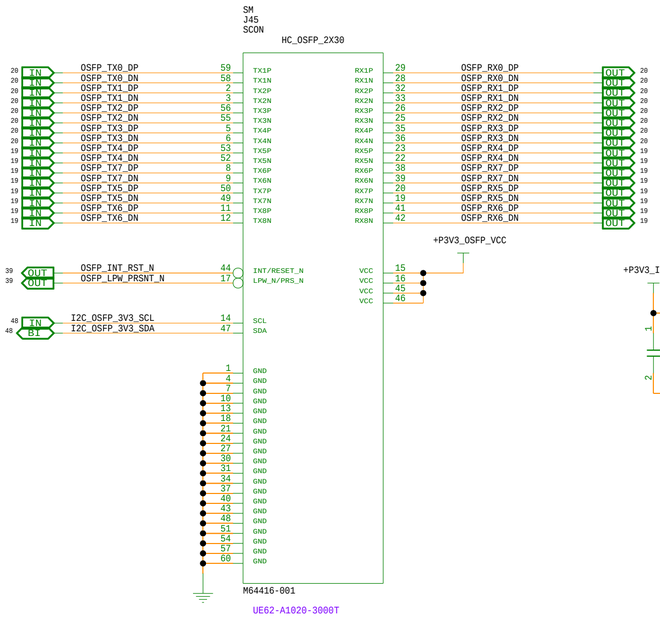
QSFP-2

OSFP

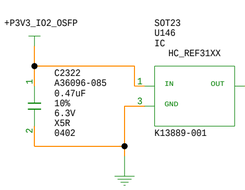
MODE	LPW_N	PRSNT_N
LOW POWER	LOW	LOW
HIGH POWER	HIGH	LOW
MODULE NOT PRESENT	-	HIGH

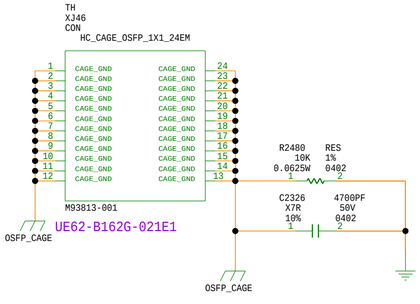
OPERATION ZONE	RST_N	INT_N
RESET	LOW	HIGH
NORMAL	HIGH	HIGH
INTERRUPT	HIGH	LOW





I2C SLAVE ADDRESS: 50H



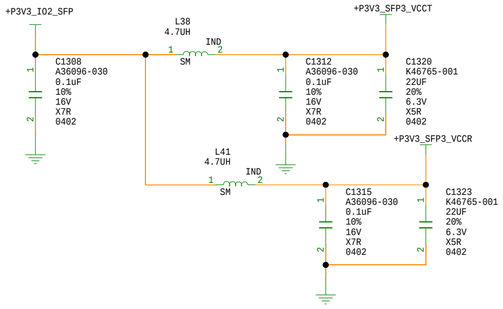


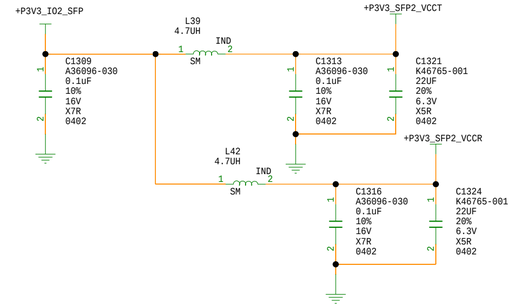
Tue Sep 26 11:47:46 2023

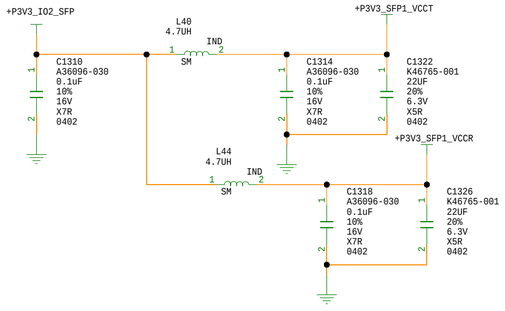
DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
UNKNOWN	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET	39 OF 105

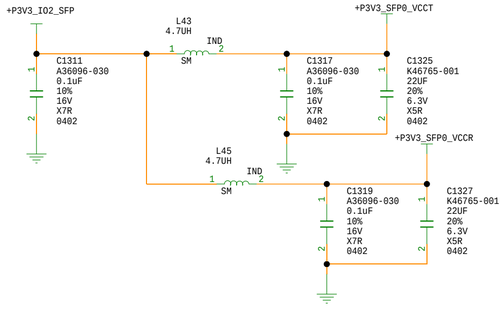
OSFP

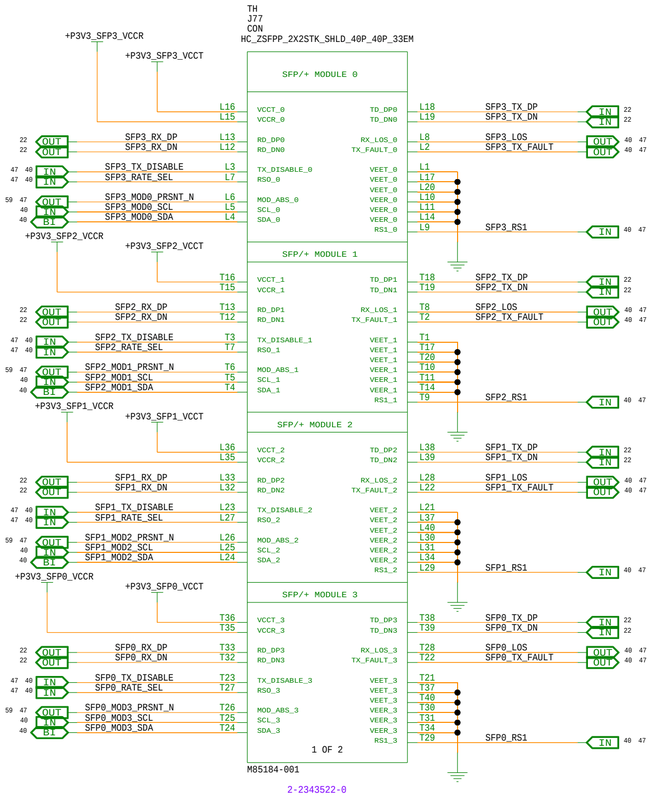
SFP CONNETCOR



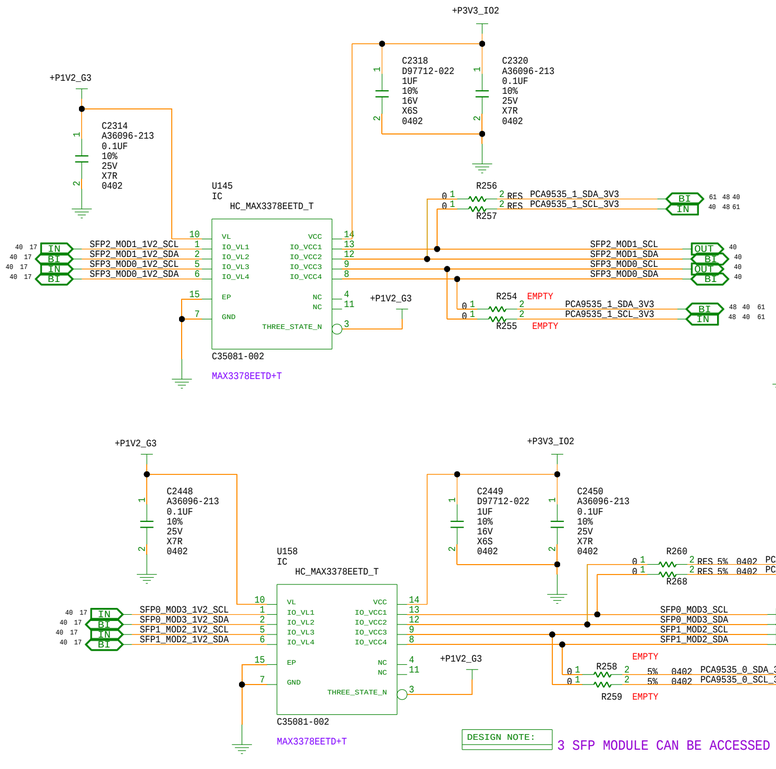


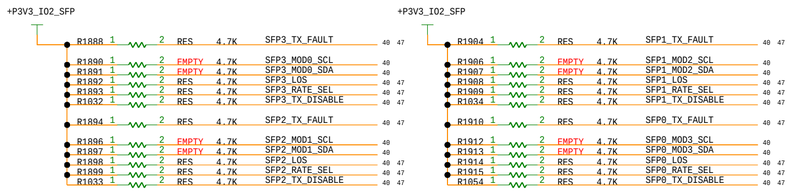


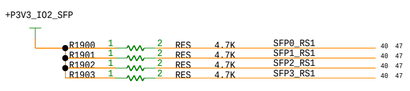


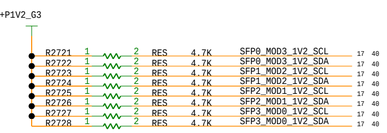


I2C SLAVE ADDRESS: 50H









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SFP CONNECTOR

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	40 OF 105

MCIO

SM
J37
SCON

K64129-002

G97V22312HR

PCIE_1_PERSTN_A
PCIE_1_RX_0_DP
PCIE_1_RX_0_DN
PCIE_1_RX_1_DP
PCIE_1_RX_1_DN
PCIE_1_SCL_A
PCIE_1_SDA_A
PCIE_1_RX_2_DP
PCIE_1_RX_2_DN
PCIE_1_RX_3_DP
PCIE_1_RX_3_DN

R51 RES 33.2 PCIE_1_PERSTN_A_R
R1093 EMPTY 0 PCIE_1_IO_A12
R1455 RES 33.2 PCIE_1_IO_A29
R1456 EMPTY 0 PCIE_1_IO_A30

PCIE_1_R_TX_0_DP / PCIE_1_R_TX_0_DN → C118 / C119 220NF 6.3V → PCIE_1_TX_0_DP / PCIE_1_TX_0_DN
PCIE_1_R_TX_1_DP / PCIE_1_R_TX_1_DN → C120 / C121 220NF 6.3V → PCIE_1_TX_1_DP / PCIE_1_TX_1_DN
PCIE_1_ALERTN_A
PCIE_100M_R_REF_AP / PCIE_100M_R_REF_AN → R52 / R53 RES 0 → PCIE_100M_REF_AP / PCIE_100M_REF_AN
PCIE_1_R_TX_2_DP / PCIE_1_R_TX_2_DN → C122 / C123 220NF 6.3V → PCIE_1_TX_2_DP / PCIE_1_TX_2_DN
PCIE_1_R_TX_3_DP / PCIE_1_R_TX_3_DN → C124 / C125 220NF 6.3V → PCIE_1_TX_3_DP / PCIE_1_TX_3_DN

R18 A36092-043 100 1% 0.0625W EMPTY 0402
PCIE_100M_REF_AP
PCIE_100M_REF_AN

+P3V3

R949 A93548-517 4.7K 1% 0.0625W RES 0402 — PCIE_1_SCL_A
R950 A93548-517 4.7K 1% 0.0625W RES 0402 — PCIE_1_SDA_A
R951 A93548-517 4.7K 1% 0.0625W RES 0402 — PCIE_1_ALERTn_A

I2C SLAVE ADDRESS: 50H

DESIGN NOTE: WHEN MCIO IS MASTER, ADDRESS CONFLICT MAY occur

SUPPORT MCIO 8X LS * 2 TO PCIE GOLD FINGER CARD ASSEMBLY

+P3V3

C1833 H80885-001 10uF 20% 6.3V X6S 0402

R1465 A93549-001 0 5% 0.0625W RES 0402 — CLK_PCIE_EP_MCIO1_DP
R1466 A93549-001 0 5% 0.0625W RES 0402 — CLK_PCIE_EP_MCIO1_DN

CLK_PCIE_EP_MCIO1_R_DP
CLK_PCIE_EP_MCIO1_R_DN
CLK_PCIE_RP_MCIO1_DP
CLK_PCIE_RP_MCIO1_DN
MCIO_CLK_ENN
MCIO_CLK_SEL_EP_N

R1467 A36092-023 1K 1% 0.063W RES 0402
R1468 A36092-023 1K 1% 0.063W RES 0402

U93
IC
HC_TMUX154E
D37827-007
TMUX154EDGSR

VCC, A0, B0, A1, B1, EN_N, SEL, GND
A: PCIE_100M_REF_AP
B: PCIE_100M_REF_AN

RP:
MCIO_CLK_SEL_EPN = 1
EP:
MCIO_CLK_SEL_EPN = 0
SET PCIE_PERSTN_A AND PCIE_ALERTN AS INPUT TO MAX-10

+P3V3

C2568 H80885-001 10uF 20% 6.3V X6S 0402

R3200 R3201 R3202 R3203 R3204 R3205 C48657-004 10K 1% 0.05W EMPTY/RES 0201

UDFN
EU36
IC
HC_AT24C512C
H95972-001
AT24C512C-MAHM-T

VCC, WP, A0, A1, A2, SDA, SCL, GND, THPAD
AT24C512C_A0
AT24C512C_A1
AT24C512C_A2
AT24C512C_WP
PCIE_1_SDA_A
PCIE_1_SCL_A

+P3V3

R3206 C48657-004 10K 1% 0.05W EMPTY R3207C48657-004 0201 10K 1% 0.05W RES

I2C SLAVE ADDRESS: 50h

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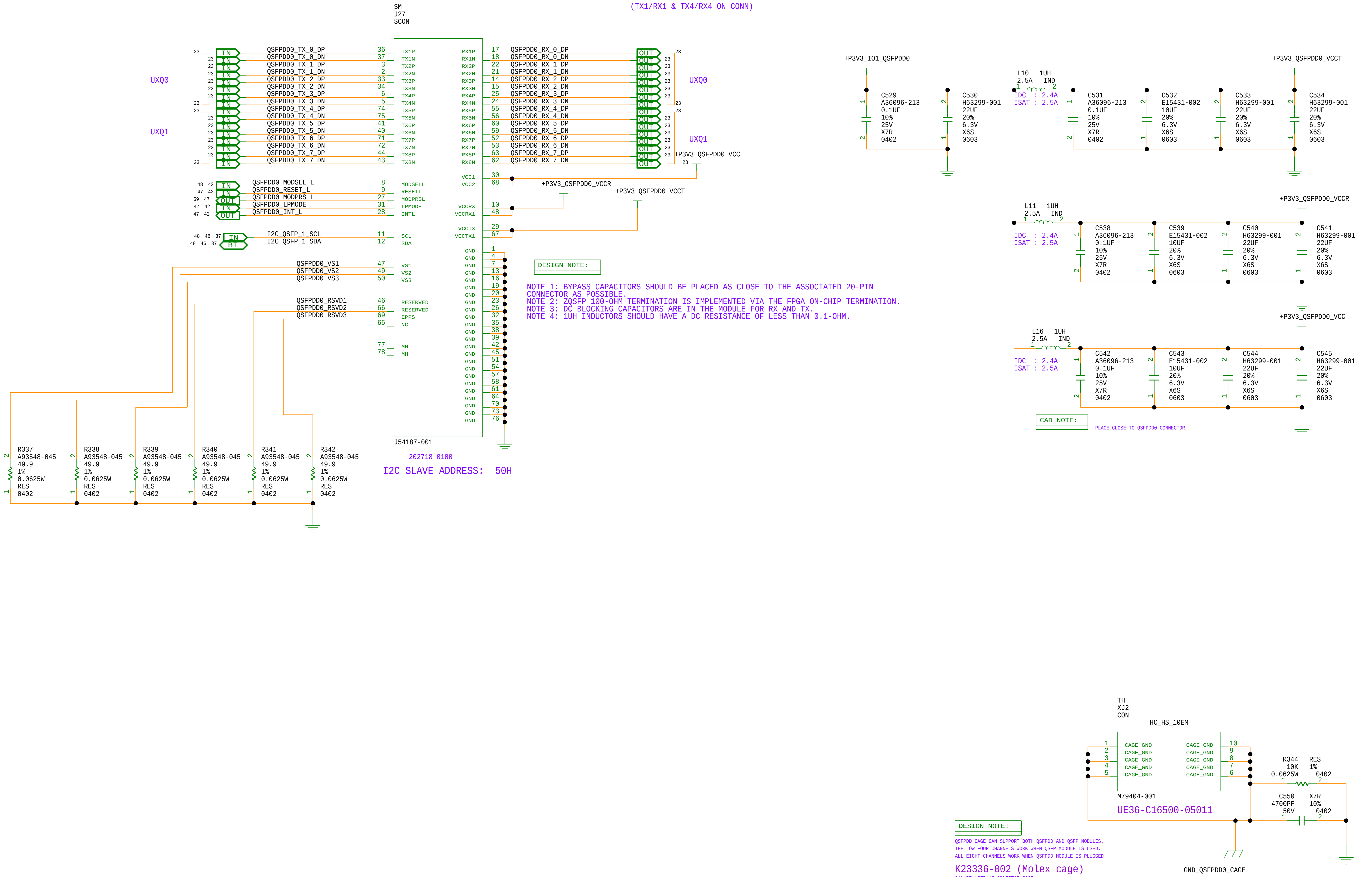
DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation INTEL CORPORATION,BANGALORE INDIA, 560103	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET	41 OF 105

MCIO

QSFP-DD CONN #0 (56G ETHERNET)

DESIGN NOTE: CHANNELS MAY BE SWAPPED WITHIN EACH UX BLOCK TO OPTIMIZE ROUTINGS. LANE 0 & 4 MAY NOT BE SWAPPED. (TX1/RX1 & TX4/RX4 ON CONN)



SM
J27
SCON
UXQ0
UXQ1
QSFPDD0_TX_0_DP
QSFPDD0_TX_0_DN
QSFPDD0_TX_1_DP
QSFPDD0_TX_1_DN
QSFPDD0_TX_2_DP
QSFPDD0_TX_2_DN
QSFPDD0_TX_3_DP
QSFPDD0_TX_3_DN
QSFPDD0_TX_4_DP
QSFPDD0_TX_4_DN
QSFPDD0_TX_5_DP
QSFPDD0_TX_5_DN
QSFPDD0_TX_6_DP
QSFPDD0_TX_6_DN
QSFPDD0_TX_7_DP
QSFPDD0_TX_7_DN
QSFPDD0_RX_0_DP
QSFPDD0_RX_0_DN
QSFPDD0_RX_1_DP
QSFPDD0_RX_1_DN
QSFPDD0_RX_2_DP
QSFPDD0_RX_2_DN
QSFPDD0_RX_3_DP
QSFPDD0_RX_3_DN
QSFPDD0_RX_4_DP
QSFPDD0_RX_4_DN
QSFPDD0_RX_5_DP
QSFPDD0_RX_5_DN
QSFPDD0_RX_6_DP
QSFPDD0_RX_6_DN
QSFPDD0_RX_7_DP
QSFPDD0_RX_7_DN
QSFPDD0_MODSEL_L
QSFPDD0_RESET_L
QSFPDD0_MODPRS_L
QSFPDD0_LPMODE
QSFPDD0_INT_L
I2C_QSFP_1_SCL
I2C_QSFP_1_SDA
QSFPDD0_VS1
QSFPDD0_VS2
QSFPDD0_VS3
QSFPDD0_RSVD1
QSFPDD0_RSVD2
QSFPDD0_RSVD3
+P3V3_IO1_QSFPDD0
+P3V3_QSFPDD0_VCC
+P3V3_QSFPDD0_VCCR
+P3V3_QSFPDD0_VCCT
+P3V3
R347 RES 4.7K 1% 0.0625W 0402
R351 RES 4.7K 1% 0.0625W 0402
R359 EMPTY 150 1% 0.0625W 0402
R361 RES 4.7K 1% 0.0625W 0402
R345 RES 4.7K 1% 0.0625W 0402
R337 A93548-045 49.9 1% 0.0625W RES 0402
R338 A93548-045 49.9 1% 0.0625W RES 0402
R339 A93548-045 49.9 1% 0.0625W RES 0402
R340 A93548-045 49.9 1% 0.0625W RES 0402
R341 A93548-045 49.9 1% 0.0625W RES 0402
R342 A93548-045 49.9 1% 0.0625W RES 0402
J54187-001
202718-0100
I2C SLAVE ADDRESS: 50H
L10 2.5A 1UH IND
L11 2.5A 1UH IND
L16 2.5A 1UH IND
IDC : 2.4A
ISAT : 2.5A
C529 A36096-213 0.1UF 10% 25V X7R 0402
C530 H63299-001 22UF 20% 6.3V X6S 0603
C531 A36096-213 0.1UF 10% 25V X7R 0402
C532 E15431-002 10UF 20% 6.3V X6S 0603
C533 H63299-001 22UF 20% 6.3V X6S 0603
C534 H63299-001 22UF 20% 6.3V X6S 0603
C538 A36096-213 0.1UF 10% 25V X7R 0402
C539 E15431-002 10UF 20% 6.3V X6S 0603
C540 H63299-001 22UF 20% 6.3V X6S 0603
C541 H63299-001 22UF 20% 6.3V X6S 0603
C542 A36096-213 0.1UF 10% 25V X7R 0402
C543 E15431-002 10UF 20% 6.3V X6S 0603
C544 H63299-001 22UF 20% 6.3V X6S 0603
C545 H63299-001 22UF 20% 6.3V X6S 0603
CAD NOTE: PLACE CLOSE TO QSFPDD0 CONNECTOR
TH
XJ2
CON
HC_HS_10EM
CAGE_GND
M79404-001
UE36-C16500-05011
R344 RES 10K 1% 0.0625W 0402
C550 4700PF 50V X7R 10% 0402
GND_QSFPDD0_CAGE

DESIGN NOTE:

NOTE 1: BYPASS CAPACITORS SHOULD BE PLACED AS CLOSE TO THE ASSOCIATED 20-PIN CONNECTOR AS POSSIBLE.
NOTE 2: ZQSFP 100-OHM TERMINATION IS IMPLEMENTED VIA THE FPGA ON-CHIP TERMINATION.
NOTE 3: DC BLOCKING CAPACITORS ARE IN THE MODULE FOR RX AND TX.
NOTE 4: 1UH INDUCTORS SHOULD HAVE A DC RESISTANCE OF LESS THAN 0.1-OHM.

DESIGN NOTE: QSFPDD CAGE CAN SUPPORT BOTH QSFPDD AND QSFP MODULES. THE LOW FOUR CHANNELS WORK WHEN QSFP MODULE IS USED. ALL EIGHT CHANNELS WORK WHEN QSFPDD MODULE IS PLUGGED.

K23336-002 (Molex cage)
CAN BE USED AS ASLERTAE CAGE.

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DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	INTEL CORPORATION,BANGALORE INDIA, 560103	C+	34649	150-0330690-A2	2.0
		SCALE:		DO NOT SCALE DRAWING	SHEET 42 OF 105

QSFP-DD CONN #1 (56G ETHERNET)

J48
SCON

UXQ0 / UXQ1

DESIGN NOTE:
CHANNELS MAY BE SWAPPED WITHIN EACH UX BLOCK TO OPTIMIZE ROUTINGS.
LANE 0 & 4 MAY NOT BE SWAPPED.
(TX1/RX1 & TX4/RX4 ON CONN)

J54187-001
202718-0100

I2C SLAVE ADDRESS: 50H

DESIGN NOTE:
NOTE 1: BYPASS CAPACITORS SHOULD BE PLACED AS CLOSE TO THE ASSOCIATED 20-PIN CONNECTOR AS POSSIBLE.
NOTE 2: ZQSFP 100-OHM TERMINATION IS IMPLEMENTED VIA THE FPGA ON-CHIP TERMINATION.
NOTE 3: DC BLOCKING CAPACITORS ARE IN THE MODULE FOR RX AND TX.
NOTE 4: 1UH INDUCTORS SHOULD HAVE A DC RESISTANCE OF LESS THAN 0.1-OHM.

+P3V3_IO1_QSFPDD1
R1041 RES 4.7K 1% 0.0625W 0402 — QSFPDD1_RESET_L
R1045 RES 4.7K 1% 0.0625W 0402 — QSFPDD1_MODPRS_L
R1047 RES 4.7K 1% 0.0625W 0402 — QSFPDD1_LPMODE
R1050 EMPTY 150 1% 0.0625W 0402
R1052 RES 4.7K 1% 0.0625W 0402 — QSFPDD1_INT_L

R1004 / R1005 / R1006 / R1007 / R1008 / R1035
A93548-045 49.9 1% 0.0625W RES 0402

+P3V3_IO1_QSFPDD1
C697 A36096-213 0.1UF 10% 25V X7R 0402
C761 H63299-001 22UF 20% 6.3V X6S 0603

+P3V3_QSFPDD1_VCCT
L3 1UH 2.5A IND — IDC : 2.4A, ISAT : 2.5A
C1073 A36096-213 0.1UF 10% 25V X7R 0402
C1074 E15431-002 10UF 20% 6.3V X6S 0603
C1075 H63299-001 22UF 20% 6.3V X6S 0603
C1076 H63299-001 22UF 20% 6.3V X6S 0603

+P3V3_QSFPDD1_VCCR
L15 1UH 2.5A IND — IDC : 2.4A, ISAT : 2.5A
C1080 A36096-213 0.1UF 10% 25V X7R 0402
C1081 E15431-002 10UF 20% 6.3V X6S 0603
C1082 H63299-001 22UF 20% 6.3V X6S 0603
C1083 H63299-001 22UF 20% 6.3V X6S 0603

+P3V3_QSFPDD1_VCC
L20 1UH 2.5A IND — IDC : 2.4A, ISAT : 2.5A
C1084 A36096-213 0.1UF 10% 25V X7R 0402
C1085 E15431-002 10UF 20% 6.3V X6S 0603
C1086 H63299-001 22UF 20% 6.3V X6S 0603
C1087 H63299-001 22UF 20% 6.3V X6S 0603

CAD NOTE: PLACE CLOSE TO QSFPDD-1 CONNECTOR

+P1V2_G3
C2125 A36096-213 0.1UF 10% 25V X7R 0402

+P3V3_IO1
C2126 D97712-022 1UF 10% 16V X6S 0402
C2127 A36096-213 0.1UF 10% 25V X7R 0402

U130
IC
HC_MAX3378EETD_T
C35081-002
MAX3378EETD+T

QSFPDD1_RESET_L_1V2
QSFPDD1_MODPRS_L_1V2
QSFPDD1_LPMODE_1V2
QSFPDD1_INT_L_1V2

R3199 2 RES 5% 0402 — QSFPDD1_MODPRS_L

+P3V3
R1039 RES 4.7K 1% 0.0625W 0402 — QSFPDD1_MODSEL_L

TH
XJ3
CON
HC_HS_10EM
M79404-001
UE36-C16500-05011
R1037 RES 10K 1% 0.0625W 0402
C1092 4700PF 10% 50V 0402
GND_QSFPDD1_CAGE

DESIGN NOTE:
QSFPDD CAGE CAN SUPPORT BOTH QSFPDD AND QSFP MODULES.
THE LOW FOUR CHANNELS WORK WHEN QSFP MODULE IS USED.
ALL EIGHT CHANNELS WORK WHEN QSFPDD MODULE IS PLUGGED.

Tue Sep 26 11:47:48 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	43 OF 105

QSFPDD CONNECTOR-1

QSFP-DD CONN #2 (56G ETHERNET)

DESIGN NOTE: CHANNELS MAY BE SWAPPED WITHIN EACH UX BLOCK TO OPTIMIZE ROUTINGS. LANE 0 & 4 MAY NOT BE SWAPPED. (TX1/RX1 & TX4/RX4 ON CONN)

J69
SCON

IN	QSFPDD2_TX_0_DP	36	TX1P	RX1P	17	QSFPDD2_RX_0_DP	OUT
IN	QSFPDD2_TX_0_DN	37	TX1N	RX1N	18	QSFPDD2_RX_0_DN	OUT
IN	QSFPDD2_TX_1_DP	3	TX2P	RX2P	22	QSFPDD2_RX_1_DP	OUT
IN	QSFPDD2_TX_1_DN	2	TX2N	RX2N	21	QSFPDD2_RX_1_DN	OUT
IN	QSFPDD2_TX_2_DP	33	TX3P	RX3P	14	QSFPDD2_RX_2_DP	OUT
IN	QSFPDD2_TX_2_DN	34	TX3N	RX3N	15	QSFPDD2_RX_2_DN	OUT
IN	QSFPDD2_TX_3_DP	6	TX4P	RX4P	25	QSFPDD2_RX_3_DP	OUT
IN	QSFPDD2_TX_3_DN	5	TX4N	RX4N	24	QSFPDD2_RX_3_DN	OUT
IN	QSFPDD2_TX_4_DP	74	TX5P	RX5P	55	QSFPDD2_RX_4_DP	OUT
IN	QSFPDD2_TX_4_DN	75	TX5N	RX5N	56	QSFPDD2_RX_4_DN	OUT
IN	QSFPDD2_TX_5_DP	41	TX6P	RX6P	60	QSFPDD2_RX_5_DP	OUT
IN	QSFPDD2_TX_5_DN	40	TX6N	RX6N	59	QSFPDD2_RX_5_DN	OUT
IN	QSFPDD2_TX_6_DP	71	TX7P	RX7P	52	QSFPDD2_RX_6_DP	OUT
IN	QSFPDD2_TX_6_DN	72	TX7N	RX7N	53	QSFPDD2_RX_6_DN	OUT
IN	QSFPDD2_TX_7_DP	44	TX8P	RX8P	63	QSFPDD2_RX_7_DP	OUT
IN	QSFPDD2_TX_7_DN	43	TX8N	RX8N	62	QSFPDD2_RX_7_DN	OUT
				VCC1	30	+P3V3_QSFPDD2_VCC	
				VCC2	68	+P3V3_QSFPDD2_VCCR	
				VCCRX	10		
				VCCRX1	48	+P3V3_QSFPDD2_VCCT	
				VCCTX	29		
				VCCTX1	67		
				GND	1		
				GND	4		
				GND	7		
				GND	13		
				GND	16		
				GND	19		
				GND	20		
				GND	23		
				GND	26		
				GND	32		
				GND	35		
				GND	38		
				GND	39		
				GND	42		
				GND	45		
				GND	51		
				GND	54		
				GND	57		
				GND	58		
				GND	61		
				GND	64		
				GND	70		
				GND	73		
				GND	76		
IN	QSFPDD2_MODSEL_L	8	MODSELL				
IN	QSFPDD2_RESET_L	9	RESETL				
OUT	QSFPDD2_MODPRS_L	27	MODPRSL				
IN	QSFPDD2_LPMODE	31	LPMODE				
OUT	QSFPDD2_INT_L	28	INTL				
IN	I2C_QSFP_2_SCL	11	SCL				
B1	I2C_QSFP_2_SDA	12	SDA				
	QSFPDD2_VS1	47	VS1				
	QSFPDD2_VS2	49	VS2				
	QSFPDD2_VS3	50	VS3				
	QSFPDD2_RSVD1	46	RESERVED				
	QSFPDD2_RSVD2	66	RESERVED				
	QSFPDD2_RSVD3	69	EPPS				
		65	NC				
		77	MH				
		78	MH				

J54187-001

202718-0100

I2C SLAVE ADDRESS: 50H

DESIGN NOTE:

NOTE 1: BYPASS CAPACITORS SHOULD BE PLACED AS CLOSE TO THE ASSOCIATED 20-PIN CONNECTOR AS POSSIBLE.
NOTE 2: ZQSFP 100-OHM TERMINATION IS IMPLEMENTED VIA THE FPGA ON-CHIP TERMINATION.
NOTE 3: DC BLOCKING CAPACITORS ARE IN THE MODULE FOR RX AND TX.
NOTE 4: 1UH INDUCTORS SHOULD HAVE A DC RESISTANCE OF LESS THAN 0.1-OHM.

+P3V3_IO2_QSFPDD2

R1840	RES	4.7K	1% 0.0625W 0402
R1842	RES	4.7K	1% 0.0625W 0402
R1843	EMPTY	150	1% 0.0625W 0402
R1844	RES	4.7K	1% 0.0625W 0402

47 44 QSFPDD2_RESET_L
47 44 QSFPDD2_LPMODE
47 44 QSFPDD2_INT_L

R1858	A93548-045	49.9	1%	0.0625W RES 0402
R1859	A93548-045	49.9	1%	0.0625W RES 0402
R1861	A93548-045	49.9	1%	0.0625W RES 0402
R1864	A93548-045	49.9	1%	0.0625W RES 0402
R1865	A93548-045	49.9	1%	0.0625W RES 0402
R1866	A93548-045	49.9	1%	0.0625W RES 0402

DESIGN NOTE:

QSFPDD CAGE CAN SUPPORT BOTH QSFPDD AND QSFP MODULES.
THE LOW FOUR CHANNELS WORK WHEN QSFP MODULE IS USED.
ALL EIGHT CHANNELS WORK WHEN QSFPDD MODULE IS PLUGGED.

+P3V3

R1839 RES 4.7K 1% 0.0625W 0402

48 44 QSFPDD2_MODSEL_L

+P3V3_IO2_QSFPDD2

C1281	A36096-213	0.1UF	10% 25V	X7R 0402
C1282	H63299-001	22UF	20% 6.3V	X6S 0603

L32 1UH 2.5A IND
IDC : 2.4A
ISAT : 2.5A

+P3V3_QSFPDD2_VCCT

C1283	A36096-213	0.1UF	10% 25V	X7R 0402
C1286	E15431-002	10UF	20% 6.3V	X6S 0603
C1289	H63299-001	22UF	20% 6.3V	X6S 0603
C1293	H63299-001	22UF	20% 6.3V	X6S 0603

L33 1UH 2.5A IND
IDC : 2.4A
ISAT : 2.5A

+P3V3_QSFPDD2_VCCR

C1284	A36096-213	0.1UF	10% 25V	X7R 0402
C1287	E15431-002	10UF	20% 6.3V	X6S 0603
C1290	H63299-001	22UF	20% 6.3V	X6S 0603
C1294	H63299-001	22UF	20% 6.3V	X6S 0603

L34 1UH 2.5A IND
IDC : 2.4A
ISAT : 2.5A

+P3V3_QSFPDD2_VCC

C1285	A36096-213	0.1UF	10% 25V	X7R 0402
C1288	E15431-002	10UF	20% 6.3V	X6S 0603
C1291	H63299-001	22UF	20% 6.3V	X6S 0603
C1295	H63299-001	22UF	20% 6.3V	X6S 0603

CAD NOTE:
PLACE CLOSE TO QSFPDD-2 CONNECTOR

TH
XJ70
CON
HC_HS_10EM

1	CAGE_GND	CAGE_GND	10
2	CAGE_GND	CAGE_GND	9
3	CAGE_GND	CAGE_GND	8
4	CAGE_GND	CAGE_GND	7
5	CAGE_GND	CAGE_GND	6

M79404-001
UE36-C16500-05011

R1867 RES 10K 1% 0.0625W 0402

C1292 4700PF X7R 10% 50V 0402

GND_QSFPDD2_CAGE

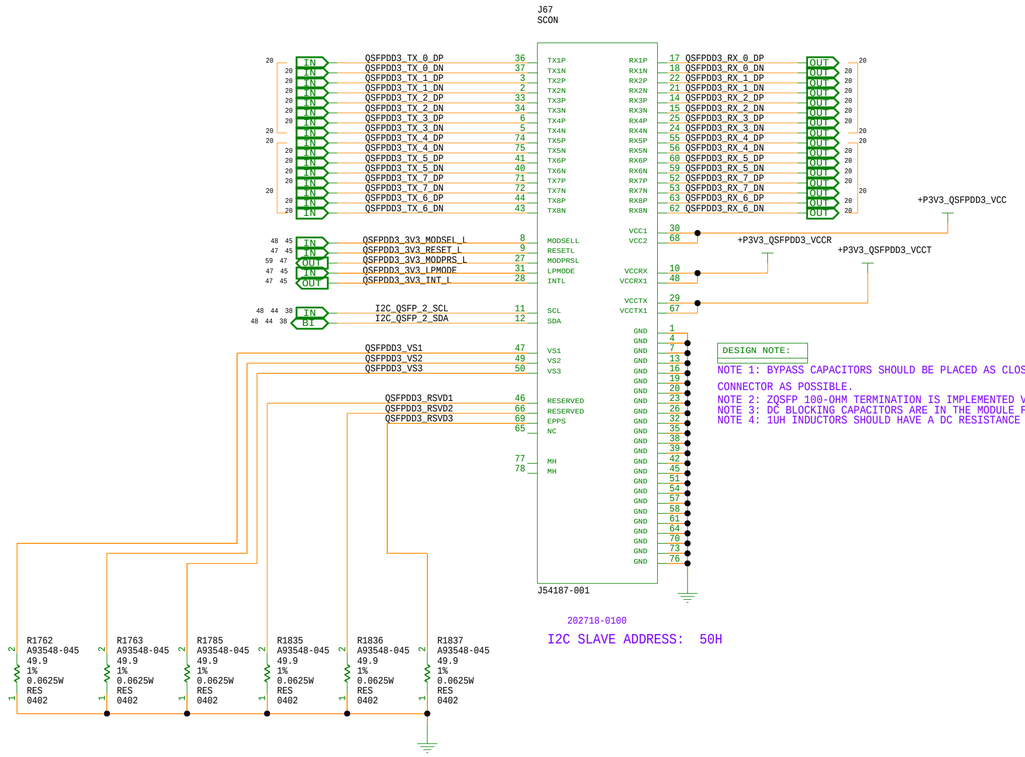
Tue Sep 26 11:47:48 2023

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER / REV
PSG	INTEL CORPORATION,BANGALORE INDIA, 560103	C+	34649	150-0330690-A2 / 2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 44 OF 105

QSFPDD CONNECTOR-2

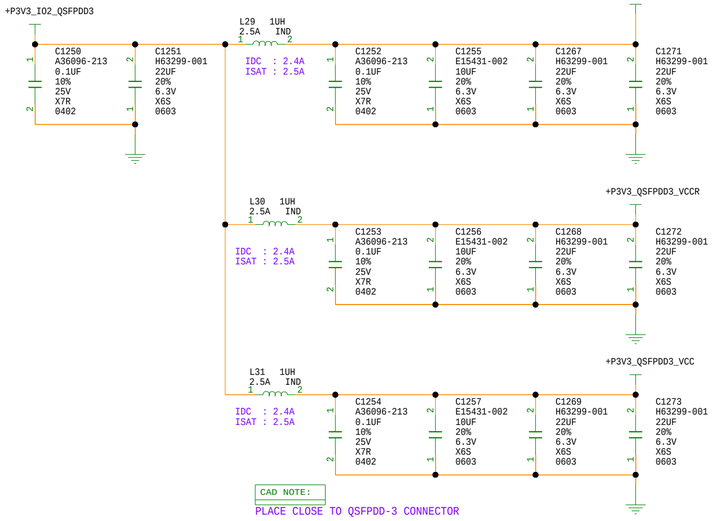
QSFP-DD CONN #3 (56G ETHERNET)

DESIGN NOTE:
CHANNELS MAY BE SWAPPED
WITHIN EACH UX BLOCK TO OPTIMIZE ROUTINGS.
LANE 0 & 4 MAY NOT BE SWAPPED.
(TX1/RX1 & TX4/RX4 ON CONN)

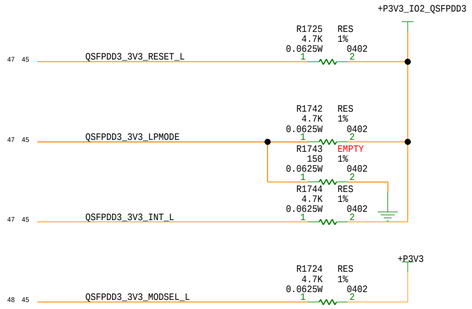


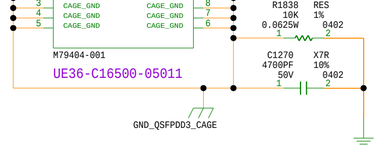
I2C SLAVE ADDRESS: 50H

DESIGN NOTE:
NOTE 1: BYPASS CAPACITORS SHOULD BE PLACED AS CLOSE TO THE ASSOCIATED 20-PIN
CONNECTOR AS POSSIBLE.
NOTE 2: ZQSFP 100-OHM TERMINATION IS IMPLEMENTED VIA THE FPGA ON-CHIP TERMINATION.
NOTE 3: DC BLOCKING CAPACITORS ARE IN THE MODULE FOR RX AND TX.
NOTE 4: 1UH INDUCTORS SHOULD HAVE A DC RESISTANCE OF LESS THAN 0.1-OHM.



CAD NOTE:
PLACE CLOSE TO QSFPDD-3 CONNECTOR





DESIGN NOTE:
QSFPDD CAGE CAN SUPPORT BOTH QSFPDD AND QSFP MODULES.
THE LOW FOUR CHANNELS WORK WHEN QSFP MODULE IS USED.
ALL EIGHT CHANNELS WORK WHEN QSFPDD MODULE IS PLUGGED.

Tue Sep 26 11:47:49 2023

QSFPDD CONNECTOR-3

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE	SCALE:	DO NOT SCALE DRAWING	SHEET	45 OF 105
	INDIA, 560103				

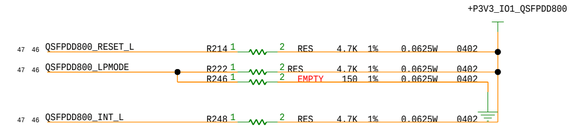
QSFP-DD-800 CONN (112G ETHERNET)

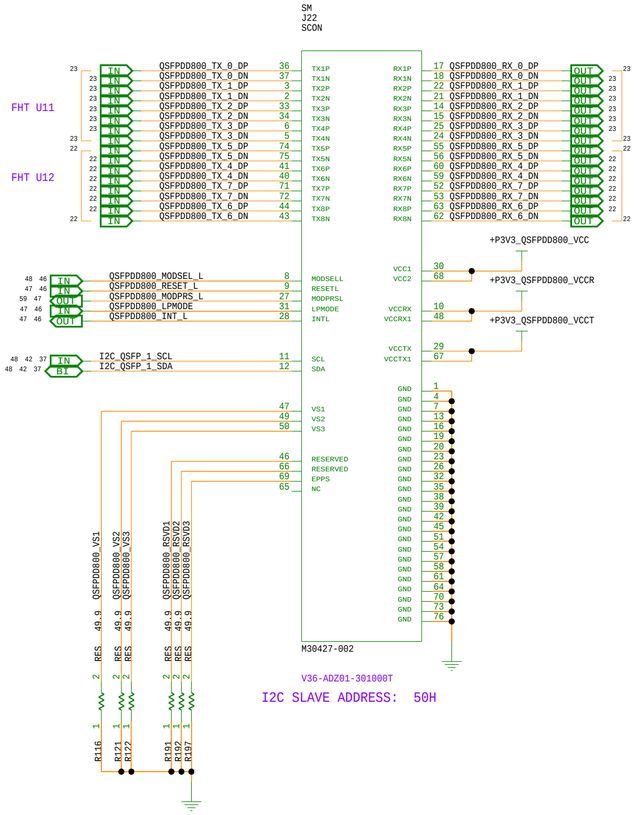
DESIGN NOTE:

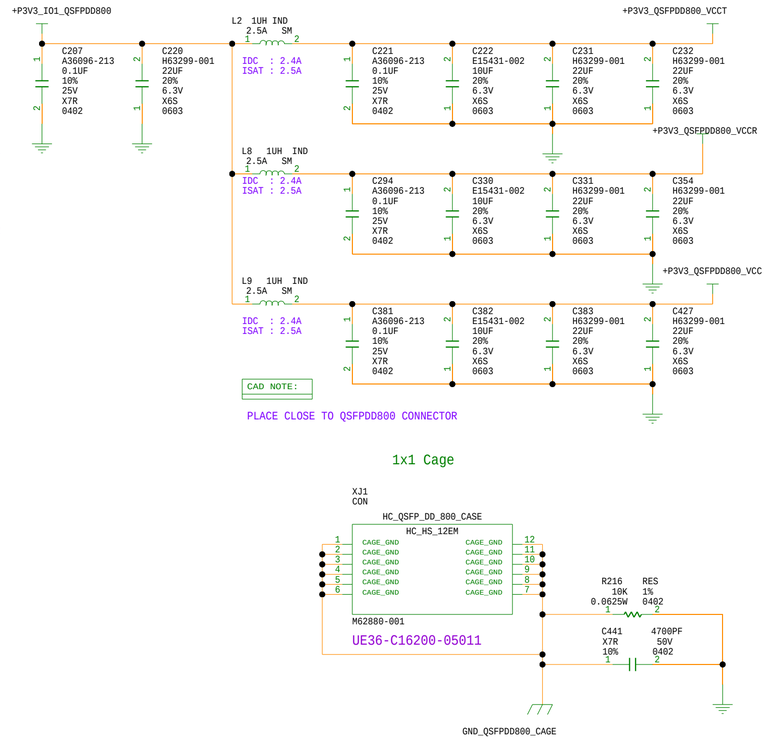
CHANNELS MAY BE SWAPPED
WITHIN EACH BK BLOCK TO OPTIMIZE ROUTINGS.
SWAP BOTH TX & RX TOGETHER.

DESIGN NOTE:

NOTE 4: 1UH INDUCTORS SHOULD HAVE A DC RESISTANCE OF LESS THAN 0.1-OHM.
NOTE 2: ZQSFP 100-OHM TERMINATION IS IMPLEMENTED VIA THE FPGA ON-CHIP TERMINATION.
NOTE 1: BYPASS CAPACITORS SHOULD BE PLACED AS CLOSE TO THE ASSOCIATED 20-PIN CONNECTOR AS POSSIBLE.
NOTE 3: DC BLOCKING CAPACITORS ARE IN THE MODULE FOR RX AND TX.







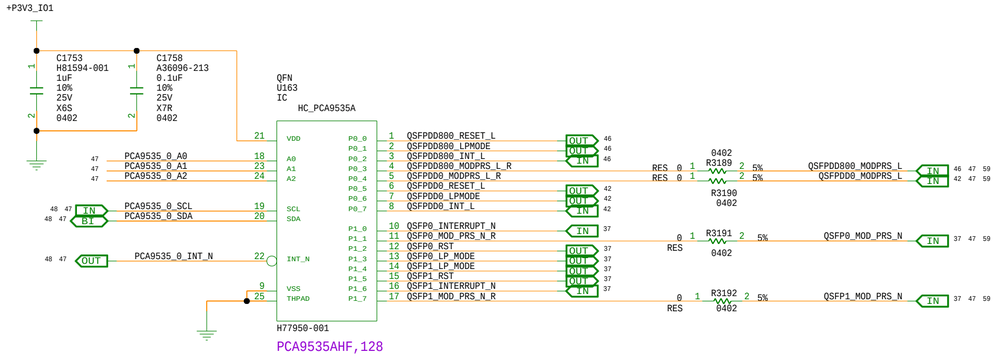
1x1 Cage

Tue Sep 26 11:47:49 2023

QSFPDD800 CONNECTOR

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SCALE:	DO NOT SCALE DRAWING	SHEET	46 OF 105

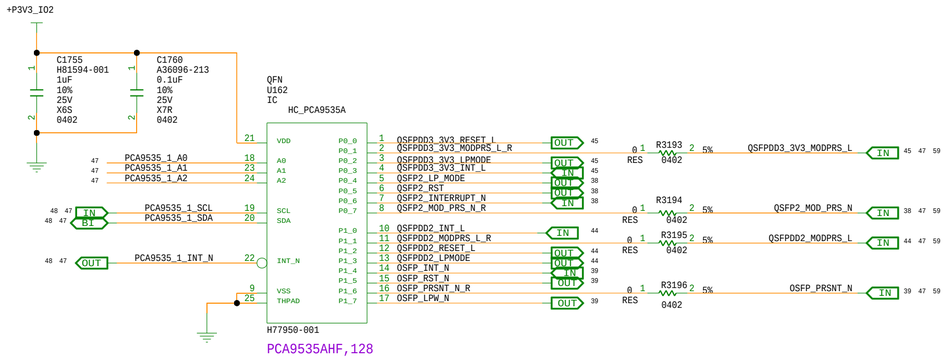
IO EXPANDER -0



PCA9535AHF,128

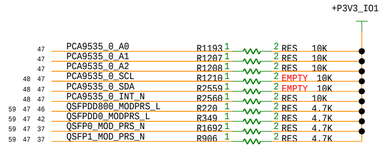
I2C SLAVE ADDRESS: 27h

IO EXPANDER -1



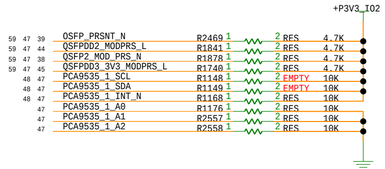
PCA9535AHF,128

I2C SLAVE ADDRESS: 20h

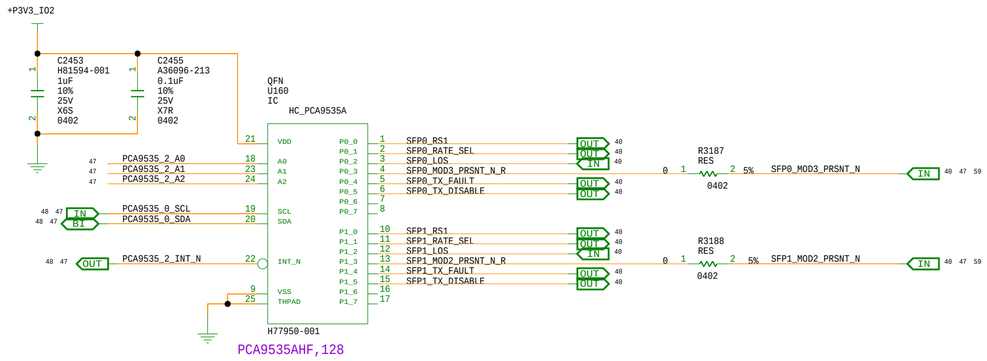


IO EXPANDER CONNECTION AND PLACEMENT DETAILS

CONNECTOR	IO EXPANDER	ADDRESS	I2C BUS	LAYOUT PLACEMENT
QSFPDD800	IO EXPANDER 0	0X27H	PCA9535_0	LEFT
QSFP0	IO EXPANDER 0	0X27H	PCA9535_0	LEFT
QSFP1	IO EXPANDER 0	0X27H	PCA9535_0	LEFT
QSFPDD0	IO EXPANDER 0	0X27H	PCA9535_0	LEFT
QSFPDD3	IO EXPANDER 1	0X20H	PCA9535_1	RIGHT
QSFP2	IO EXPANDER 1	0X20H	PCA9535_1	RIGHT
QSFPDD2	IO EXPANDER 1	0X20H	PCA9535_1	RIGHT
0SFP	IO EXPANDER 1	0X20H	PCA9535_1	RIGHT
SFP0	IO EXPANDER 2	0X21H	PCA9535_0	LEFT
SFP1	IO EXPANDER 2	0X21H	PCA9535_0	LEFT
SFP2	IO EXPANDER 3	0X23H	PCA9535_0	LEFT
SFP3	IO EXPANDER 3	0X23H	PCA9535_0	LEFT

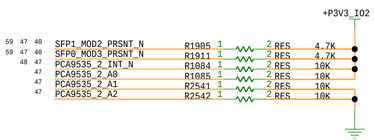


IO EXPANDER -2

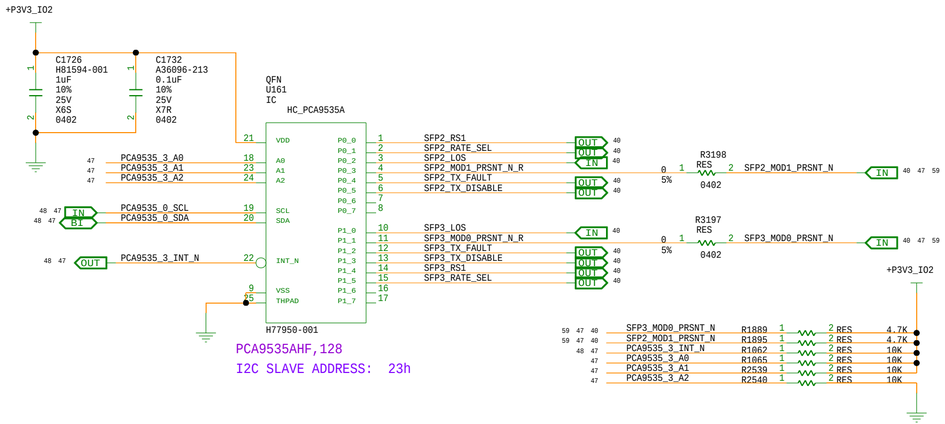


PCA9535AHF,128

I2C SLAVE ADDRESS: 21h



IO EXPANDER-3



PCA9535AHF,128

I2C SLAVE ADDRESS: 23h

Tue Sep 26 11:47:49 2023

IO EXPANDER

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	47 OF 105

LEVEL_SHIFTERS_1

U71 — C35081-002 (MAX3378EETD+T)

+P1V2_G3 → C128 A36096-213 0.1UF 10% 25V X7R 0402

+P3V3_IO1 → C126 D97712-022 1UF 10% 16V X6S 0402; C127 A36096-213 0.1UF 10% 25V X7R 0402

48 13	IN	PCA9535_0_1V2_SCL	
48 13	BI	PCA9535_0_1V2_SDA	
48 17	OUT	PCA9535_0_1V2_INT_N	
		PCA9535_0_SCL_R	R3156 0
		PCA9535_0_SDA_R	R3157 0
		PCA9535_0_INT_N	R3160 0
		PCA9535_0_SDA_3V3	R3161 0
		PCA9535_0_SCL_3V3	

RES 5% 0402

PCA9535_0_SCL → OUT 47 48 17
PCA9535_0_SDA → BI 47 48 13
PCA9535_0_INT_N → IN 47 48 17
PCA9535_0_SDA_3V3 → BI 40 48 61
PCA9535_0_SCL_3V3 → IN 40 48 61

+P1V2_G3

U117 — C35081-002 (MAX3378EETD+T)

+P1V2_G3 → C1244 A36096-213 0.1UF 10% 25V X7R 0402

48 17	IN	I2C_QSFP_3_1V2_SCL
48 17	BI	I2C_QSFP_3_1V2_SDA
48 15	IN	I2C_QSFP_1_1V2_SCL
48 15	BI	I2C_QSFP_1_1V2_SDA

+P3V3_IO1 → C1246 D97712-022 1UF 10% 16V X6S 0402; C1248 A36096-213 0.1UF 10% 25V X7R 0402

R275 0, R276 0 — RES 5% 0402

I2C_QSFP_3_SCL → OUT 37 43 48
I2C_QSFP_3_SDA → BI 37 43 48
I2C_QSFP_1_SCL → OUT 37 42 46 48
I2C_QSFP_1_SDA → BI 37 42 46 48

PCA9535_0_SDA_3V3 → BI 61 40 48
PCA9535_0_SCL_3V3 → IN 61 40 48

R273 0, R274 0 — RES 5% 0402

PCA9535_1_SDA_3V3 → BI 40 48 61
PCA9535_1_SCL_3V3 → IN 40 48 61

+P1V2_G3

U48 — C35081-002 (MAX3378EETD+T)

+P1V2_G3 → C1448 A36096-213 0.1UF 10% 25V X7R 0402

48 18	IN	QSFPDD800_MODSEL_L_1V2
48 18	IN	QSFP0_MOD_SEL_N_1V2
48 18	IN	QSFP1_MOD_SEL_N_1V2
48 18	IN	QSFPDD0_MODSEL_L_1V2

+P3V3 → C1450 D97712-022 1UF 10% 16V X6S 0402; C1452 A36096-213 0.1UF 10% 25V X7R 0402

QSFPDD800_MODSEL_L → OUT 46
QSFP0_MOD_SEL_N → OUT 37
QSFP1_MOD_SEL_N → OUT 37
QSFPDD0_MODSEL_L → OUT 42

+P1V2_G3

U61 — C35081-002 (MAX3378EETD+T)

+P1V2_G3 → C1722 A36096-213 0.1UF 10% 25V X7R 0402

48 17	OUT	PCA9535_2_1V2_INT_N
48 17	OUT	PCA9535_3_1V2_INT_N

+P3V3_IO2 → C1727 D97712-022 1UF 10% 16V X6S 0402; C1733 A36096-213 0.1UF 10% 25V X7R 0402

PCA9535_2_INT_N → IN 47
PCA9535_3_INT_N → IN 47

+P1V2_G3

U122 — C35081-002 (MAX3378EETD+T)

+P1V2_G3 → C1245 A36096-213 0.1UF 10% 25V X7R 0402

48 13	IN	I2C_QSFP_2_1V2_SCL
48 13	BI	I2C_QSFP_2_1V2_SDA
48 16	IN	I2C_QSFP_SCL
48 16	BI	I2C_QSFP_SDA

+P3V3_IO2 → C1247 D97712-022 1UF 10% 16V X6S 0402; C1249 A36096-213 0.1UF 10% 25V X7R 0402

R271 0, R272 0 — RES 5% 0402

PCA9535_1_SDA_3V3 → BI 61 40 48
PCA9535_1_SCL_3V3 → IN 61 40 48

I2C_QSFP_2_SCL → OUT 38 44 45 48
I2C_QSFP_2_SDA → BI 38 44 45 48
I2C_QSFP_3V3_SCL → OUT 39 48
I2C_QSFP_3V3_SDA → BI 39 48

R269 0, R270 0 — RES 5% 0402

PCA9535_1_SDA_3V3 → BI 40 48 61
PCA9535_1_SCL_3V3 → IN 40 48 61

+P1V2_G3

U91 — C35081-002 (MAX3378EETD+T)

+P1V2_G3 → C1785 A36096-213 0.1UF 10% 25V X7R 0402

48 18	IN	QSFPDD1_MODSEL_L_1V2
48 18	IN	QSFPDD2_MODSEL_L_1V2
48 13	IN	QSFPDD3_MODSEL_L_1V2
48 13	IN	QSFP2_MOD_SEL_N_1V2

+P3V3 → C1822 D97712-022 1UF 10% 16V X6S 0402; C1825 A36096-213 0.1UF 10% 25V X7R 0402

QSFPDD1_MODSEL_L → OUT 43
QSFPDD2_MODSEL_L → OUT 44
QSFPDD3_3V3_MODSEL_L → OUT 45
QSFP2_MOD_SEL_N → OUT 38

+P1V2_G3

U88 — C35081-002 (MAX3378EETD+T)

+P1V2_G3 → C1750 A36096-213 0.1UF 10% 25V X7R 0402

48 13	OUT	PCA9535_1_1V2_INT_N
48 13	IN	PCA9535_1_1V2_SCL
48 13	BI	PCA9535_1_1V2_SDA

+P3V3_IO2 → C1754 D97712-022 1UF 10% 16V X6S 0402; C1759 A36096-213 0.1UF 10% 25V X7R 0402

PCA9535_1_INT_N → R3158 0 — RES 5% 0402 → PCA9535_1_SCL → IN 47
PCA9535_1_SCL_R → R3159 0 — RES 5% 0402 → PCA9535_1_SDA → BI 47

R3162 0, R3163 0 — RES 5% 0402

PCA9535_1_SDA_3V3 → BI 40 48 61
PCA9535_1_SCL_3V3 → IN 40 48 61

+P1V2_G3

SM EMPTY TP345–TP348 (test points)

SM EMPTY TP345	1	PCA9535_0_1V2_SCL	13 48
SM EMPTY TP346	1	PCA9535_0_1V2_SDA	13 48
SM EMPTY TP343	1	PCA9535_1_1V2_SCL	13 48
SM EMPTY TP344	1	PCA9535_1_1V2_SDA	13 48

+P1V2_G3

48 13	PCA9535_0_1V2_SCL	R1272	1–2	RES	10K
48 13	PCA9535_0_1V2_SDA	R1278	1–2	RES	10K
48 17	PCA9535_0_1V2_INT_N	R1279	1–2	RES	10K
48 17	PCA9535_2_1V2_INT_N	R1134	1–2	RES	10K
48 17	PCA9535_3_1V2_INT_N	R1111	1–2	RES	10K
48 13	PCA9535_1_1V2_SCL	R1211	1–2	RES	10K
48 13	PCA9535_1_1V2_SDA	R1247	1–2	RES	10K
48 13	PCA9535_1_1V2_INT_N	R1261	1–2	RES	10K

SM EMPTY TP378–TP381 (test points)

+P3V3_IO1

SM EMPTY TP378	48 43 37	I2C_QSFP_3_SCL	R1038	1–2	EMPTY	2.2K 1%	0.0625W 0402
SM EMPTY TP379	48 43 37	I2C_QSFP_3_SDA	R1040	1–2	EMPTY	2.2K 1%	0.0625W 0402
SM EMPTY TP380	42 37 48 46	I2C_QSFP_1_SCL	R1076	1–2	EMPTY	2.2K 1%	0.0625W 0402
SM EMPTY TP381	42 37 48 46	I2C_QSFP_1_SDA	R1077	1–2	EMPTY	2.2K 1%	0.0625W 0402

SM EMPTY TP335–TP342 (test points)

+P3V3_IO2

SM EMPTY TP335	48 45 44 38	I2C_QSFP_2_SCL	R1845	1–2	EMPTY	2.2K	
SM EMPTY TP336	48 45 44 38	I2C_QSFP_2_SDA	R1846	1–2	EMPTY	2.2K	
SM EMPTY TP341	48 39	I2C_QSFP_3V3_SCL	R2465	1–2	EMPTY	4.7K	
SM EMPTY TP342	48 39	I2C_QSFP_3V3_SDA	R2466	1–2	EMPTY	4.7K	

+P1V2_G3

48 15	I2C_QSFP_1_1V2_SCL	R2733	1–2	RES	2.2K	1%	0.0625W 0402
48 15	I2C_QSFP_1_1V2_SDA	R2734	1–2	RES	2.2K	1%	0.0625W 0402
48 18	QSFPDD800_MODSEL_L_1V2	R1720	1–2	RES	2.2K	1%	0.0625W 0402

+P3V3 pull-ups

61 48 40	PCA9535_1_SDA_3V3	R280	4.7K	1%	0.0625W 0402
61 48 40	PCA9535_1_SCL_3V3	R277	4.7K	1%	0.0625W 0402
61 48 40	PCA9535_0_SDA_3V3	R278	4.7K	1%	0.0625W 0402
61 48 40	PCA9535_0_SCL_3V3	R279	4.7K	1%	0.0625W 0402

+P1V2_G3

48 17	I2C_QSFP_3_1V2_SCL	R2731	2.2K	1%	0.0625W 0402
48 17	I2C_QSFP_3_1V2_SDA	R2732	2.2K	1%	0.0625W 0402
48 18	QSFPDD1_MODSEL_L_1V2	R2738	2.2K	1%	0.0625W 0402
43 17	QSFPDD1_RESET_L_1V2	R363	2.2K	1%	0.0625W 0402
43 17	QSFPDD1_MODPRS_L_1V2	R365	2.2K	1%	0.0625W 0402
43 17	QSFPDD1_LPMODE_1V2	R1745	2.2K	1%	0.0625W 0402
43 17	QSFPDD1_INT_L_1V2	R1746	2.2K	1%	0.0625W 0402
48 18	QSFP0_MOD_SEL_N_1V2	R2719	4.7K	1%	0.0625W 0402
48 18	QSFP1_MOD_SEL_N_1V2	R2492	4.7K	1%	0.0625W 0402
48 18	QSFPDD0_MODSEL_L_1V2	R2729	2.2K	1%	0.0625W 0402
48 13	QSFPDD2_MODSEL_L_1V2	R3173	2.2K	1%	0.0625W 0402
48 13	QSFPDD3_MODSEL_L_1V2	R1719	2.2K	1%	0.0625W 0402
48 13	QSFP2_MOD_SEL_N_1V2	R2741	4.7K	1%	0.0625W 0402
48 13	I2C_QSFP_2_1V2_SDA	R2739	2.2K	1%	0.0625W 0402
48 13	I2C_QSFP_2_1V2_SCL	R2740	2.2K	1%	0.0625W 0402
48 16	I2C_OSFP_SCL	R2459	4.7K	1%	0.0625W 0402
48 16	I2C_OSFP_SDA	R2460	4.7K	1%	0.0625W 0402

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LEVEL_SHIFTERS_1

DEPARTMENT		SIZE	C+
PSG		CODE	34649
		DOCUMENT NUMBER	150-0330690-A2
		REV	2.0
SCALE:	DO NOT SCALE DRAWING	SHEET	48 OF 105

Intel Corporation
INTEL CORPORATION,BANGALORE
INDIA, 560103

CONN POWER LOAD SWITCHES-1

PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	
LOAD CURRENT	5.6A
FREQUENCY	
RIPPLE _VOLTAGE	

DESIGN NOTE:
Rsense: 7mohm
Itrip(min) : 5.65A
Itrip(Nom) : 7.1A
Pdiss : 360mW

+P3V3_IO1
C2149 H81594-001 1UF 10% 25V X6S 0402
R2138 M80022-001 0.007 1% 1W RES 1206
R2178 0402 RES
C2582 A36096-213 0.1UF 10% 25V X7R 0402
R2179 0402 RES
P3V3_IO1_QSFPDD0_SENSE_DP
P3V3_IO1_QSFPDD0_SENSE_DN
OUT 76
Q24 M11185-002 CSD17575Q3
P3V3_IO1_FET1_SENSE
P3V3_IO1_FET1_GATE_R
+P3V3
R2140 A93548-034 10K 1% 0.0625W RES 0402
R2145 A93548-596 100K 1% 0.0625W RES 0402
R2146 A93548-271 69.8K 1% 0.0625W RES 0402
P3V3_IO1_FET1_FB
+P3V3_IO1_QSFPDD0
TP259 EMPTY TH
C2184 K13620-001 100uF 20% 10V X5R 1206

CAD NOTE:
PLACE THE SENSE RES NEAR TO LOAD
ROUTE AS KELVIN SENSE

CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

FET_PARAMETER	VALUE
VGS	±20 V
ID	60 A

U134 MSOP IC HC_LTC4211CMS8
VCC SENSE ON GATE TIMER FB GND RESET_N
M95393-001
LTC4211CMS8#PBF

IN P3V3_IO1_FET1_PMAX_EN
IN P3V3_IO1_FET1_SMAX_EN
R2823 RES 0 5% 0.0625W 0402
R2824 EMPTY 0 5% 0.0625W 0402
P3V3_IO1_FET1_EN_R
P3V3_IO1_FET1_TIMER
R2084 A36092-023 1K 1% 0.063W RES 0402
C2136 A36096-089 0.022UF 10% 25V X7R 0402
R2080 100 RES
R2142 5.1 0.1W 0603 RES
P3V3_IO1_FET1_GATE_C
P3V3_IO1_FET1_POK
C2180 D62711-001 1NF 10% 50V X7R 0402

DESIGN NOTE:
ENABLE ON THRESHOLD
1.4V

PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	
LOAD CURRENT	5.6A
FREQUENCY	
RIPPLE _VOLTAGE	

DESIGN NOTE:
Rsense: 7mohm
Itrip(min) : 5.65A
Itrip(Nom) : 7.1A
Pdiss : 360mW

+P3V3_IO1
C2498 H81594-001 1UF 10% 25V X6S 0402
R2810 M80022-001 0.007 1% 1W RES 1206
R2180 0402 RES
C2583 A36096-213 0.1UF 10% 25V X7R 0402
R2181 0402 RES
P3V3_IO1_QSFP0_SENSE_DP
P3V3_IO1_QSFP0_SENSE_DN
OUT 76
Q79 M11185-002 CSD17575Q3
P3V3_IO1_FET2_SENSE
P3V3_IO1_FET2_GATE_R
+P3V3
R2787 A93548-034 10K 1% 0.0625W RES 0402
R2797 A93548-596 100K 1% 0.0625W RES 0402
R2802 A93548-271 69.8K 1% 0.0625W RES 0402
P3V3_IO1_FET2_FB
+P3V3_IO1_QSFP0
TP274 EMPTY TH
C2559 K13620-001 100uF 20% 10V X5R 1206

CAD NOTE:
PLACE THE SENSE RES NEAR TO LOAD
ROUTE AS KELVIN SENSE

CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

FET_PARAMETER	VALUE
VGS	±20 V
ID	60 A

MSOP U172 IC HC_LTC4211CMS8
VCC SENSE ON GATE TIMER FB GND RESET_N
M95393-001
LTC4211CMS8#PBF

IN P3V3_IO1_FET2_PMAX_EN
IN P3V3_IO1_FET2_SMAX_EN
R2827 RES 0 5% 0.0625W 0402
R2828 EMPTY 0 5% 0.0625W 0402
P3V3_IO1_FET2_EN_R
P3V3_IO1_FET2_TIMER
R2759 A36092-023 1K 1% 0.063W RES 0402
C2482 A36096-089 0.022UF 10% 25V X7R 0402
R2751 100 RES
R2792 5.1 0.1W 0603 RES
P3V3_IO1_FET2_GATE_C
P3V3_IO1_FET2_POK
C2534 D62711-001 1NF 10% 50V X7R 0402

DESIGN NOTE:
ENABLE ON THRESHOLD
1.4V

PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	
LOAD CURRENT	4A
FREQUENCY	
RIPPLE _VOLTAGE	

DESIGN NOTE:
Rsense: 7mohm
Itrip(min) : 5.65A
Itrip(Nom) : 7.1A
Pdiss : 360mW

+P3V3_IO1
C2493 H81594-001 1UF 10% 25V X6S 0402
R2809 M80022-001 0.007 1% 1W RES 1206
R2182 0402 RES
C2584 A36096-213 0.1UF 10% 25V X7R 0402
R2183 0402 RES
P3V3_IO1_FMC_12A_SENSE_DP
P3V3_IO1_FMC_12A_SENSE_DN
OUT 76
Q78 M11185-002 CSD17575Q3
P3V3_IO1_FET3_SENSE
P3V3_IO1_FET3_GATE_R
+P3V3
R2786 A93548-034 10K 1% 0.0625W RES 0402
R2796 A93548-596 100K 1% 0.0625W RES 0402
R2801 A93548-271 69.8K 1% 0.0625W RES 0402
P3V3_IO1_FET3_FB
+P3V3_IO1_FMC_12A
TP355 EMPTY TH
C2535 K13620-001 100uF 20% 10V X5R 1206

CAD NOTE:
PLACE THE SENSE RES NEAR TO LOAD
ROUTE AS KELVIN SENSE

CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

FET_PARAMETER	VALUE
VGS	±20 V
ID	60 A

MSOP U171 IC HC_LTC4211CMS8
VCC SENSE ON GATE TIMER FB GND RESET_N
M95393-001
LTC4211CMS8#PBF

IN P3V3_IO1_FET3_PMAX_EN
IN P3V3_IO1_FET3_SMAX_EN
R2825 RES 0 5% 0.0625W 0402
R2826 EMPTY 0 5% 0.0625W 0402
P3V3_IO1_FET3_EN_R
P3V3_IO1_FET3_TIMER
R2758 A36092-023 1K 1% 0.063W RES 0402
C2481 A36096-089 0.022UF 10% 25V X7R 0402
R2750 100 RES
R2791 5.1 0.1W 0603 RES
P3V3_IO1_FET3_GATE_C
P3V3_IO1_FET3_POK
C2533 D62711-001 1NF 10% 50V X7R 0402

DESIGN NOTE:
ENABLE ON THRESHOLD
1.4V

Tue Sep 26 11:47:51 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
UNKNOWN	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET	49 OF 105

CONNECTOR POWER LOAD SWITCHES

CONN POWER LOAD SWITCHES-2

PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	
LOAD CURRENT	5.6A
FREQUENCY	
RIPPLE _VOLTAGE	

DESIGN NOTE:
Rsense: 7mohm
Itrip(min) : 5.65A
Itrip(Nom) : 7.1A
Pdiss : 360mW

DESIGN NOTE:
ENABLE ON THRESHOLD 1.4V

CAD NOTE: PLACE THE SENSE RES NEAR TO LOAD ROUTE AS KELVIN SENSE

CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

FET_PARAMETER	VALUE
VGS	±20 V
ID	60 A

LTC4211CMS8#PBF

CONNECTOR POWER LOAD SWITCHES

Tue Sep 26 11:47:51 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
UNKNOWN	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET	50 OF 105

CONN POWER LOAD SWITCHES-3

PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	
LOAD CURRENT	5.6A
FREQUENCY	
RIPPLE _VOLTAGE	

DESIGN NOTE:
Rsense: 7mohm
Itrip(min) : 5.65A
Itrip(Nom) : 7.1A
Pdiss : 360mW

DESIGN NOTE:
ENABLE ON THRESHOLD
1.4V

CAD NOTE: PLACE THE SENSE RES NEAR TO LOAD ROUTE AS KELVIN SENSE

CAD NOTE: PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB. AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

FET_PARAMETER	VALUE
VGS	±20 V
ID	60 A

LTC4211CMS8#PBF

CONNECTOR POWER LOAD SWITCHES

Tue Sep 26 11:47:51 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
UNKNOWN	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET	51 OF 105

CONN POWER LOAD SWITCHES-4

PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	
LOAD CURRENT	4A
FREQUENCY	
RIPPLE _VOLTAGE	

DESIGN NOTE:
Rsense: 7mohm
Itrip(min) : 5.65A
Itrip(Nom) : 7.1A
Pdiss : 360mw

DESIGN NOTE:
ENABLE ON THRESHOLD
1.4V

CAD NOTE: PLACE THE SENSE RES NEAR TO LOAD
ROUTE AS KELVIN SENSE

CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

FET_PARAMETER	VALUE
VGS	±20 V
ID	60 A

LTC4211CMS8#PBF

PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	
LOAD CURRENT	5.6A
FREQUENCY	
RIPPLE _VOLTAGE	

PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	
LOAD CURRENT	4A
FREQUENCY	
RIPPLE _VOLTAGE	

Tue Sep 26 11:47:52 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
UNKNOWN	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET	52 OF 105

CONNECTOR POWER LOAD SWITCHES

FMC+ CONNECTOR A (NORTH)

J7
SCON
HC_B2B_14X40
6 OF 7
K12425-001
ASP-184329-01

J7
SCON
HC_B2B_14X40
7 OF 7
K12425-001
ASP-184329-01

J7
SCON
HC_14X40_ASP_VITA57P4
HC_B2B_14X40
3 OF 7
K12425-001
ASP-184329-01

J7
SCON
HC_14X40_ASP_VITA57P4
HC_B2B_14X40
2 OF 7
K12425-001
ASP-184329-01

J7
SCON
HC_B2B_14X40
4 OF 7
K12425-001
ASP-184329-01

DESIGN NOTE:
REWORK RES SHALL BE MOUNTED
FOR PROVIDING REFERENCE CLOCK TO FM91 FOR SUPPORTING ADC12DJ5200RFEVM CARD

+FMC_A_VADJ
+FMC_A_VREF
+P3V3_IO1_FMC_12A
+P12V0_FMC_A

Tue Sep 26 11:47:53 2023

DEPARTMENT: PSG	Intel Corporation INTEL CORPORATION,BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SIZE: C+	CODE: 34649	DOCUMENT NUMBER: 150-0330690-A2 / REV: 2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET: 53 OF 105

FMC A CONNECTOR-1

FMC+ CONNECTOR A (NORTH)

J7
SCON
HC_B2B_14X40
1 OF 7
K12425-001
ASP-184329-01

5 OF 7

DESIGN NOTE:
5: SUPPORT ONLY FOR SPECIFIC 1.8V IO STANDARD FMC+ CARDS.

U74
IC
HC_14-TDFN_EP
HC_MAX3378EETD_T
C35081-002
MAX3378EETD+T

U89
IC

U80
IC

CAD NOTE:
PLEASE PLACE THESE THREE
RESISTOR FOR EACH SIGNAL AS TRIPAD.

FMC A CONNECTOR-2

Tue Sep 26 11:47:54 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	54 OF 105

FMC+ CONNECTOR B (EAST)

SM
J9
SCON
HC_B2B_14X40

6 OF 7

K12425-001

ASP-184329-01

SM
J9
SCON
HC_B2B_14X40

7 OF 7

K12425-001

ASP-184329-01

SM
J9
SCON
HC_B2B_14X40

4 OF 7

K12425-001

ASP-184329-01

58 55 19	OUT	FMC_B_CLK_M2C_3_DP	R58	1	2	RES 0	R_FMC_B_CLK_M2C_3_DP	L8	
58 55 19	OUT	FMC_B_CLK_M2C_3_DN	R352	1	2	RES 0	R_FMC_B_CLK_M2C_3_DN	L9	
55 19	OUT	FMC_B_CLK_M2C_2_DP	R353	1	2	EMPTY 0	R_FMC_B_CLK_M2C_2_DP	L4	
55 19	OUT	FMC_B_CLK_M2C_2_DN	R354	1	2	EMPTY 0	R_FMC_B_CLK_M2C_2_DN	L5	
58 55 19	OUT	FMC_B_CLK_M2C_3_DP	R355	1	2	EMPTY 0	R_FMC_B_CLK_M2C_3_1_DP	Z20	
58 55 19	OUT	FMC_B_CLK_M2C_3_DN	R356	1	2	EMPTY 0	R_FMC_B_CLK_M2C_3_1_DN	Z21	

								OUT	19 58
								OUT	19 58
								OUT	19 58
								OUT	19 58
R357	2	1	RES 0	FMC_B_CLK_M2C_2_DP				OUT	19 55
R401	2	1	RES 0	FMC_B_CLK_M2C_2_DN				OUT	19 55

DESIGN NOTE:

REWORK RES SHALL BE MOUNTED
FOR PROVIDING REFERENCE CLOCK TO FM91 FOR SUPPORTING ADC12DJ5200RFEVM CARD

SM
J9
SCON
HC_B2B_14X40

3 OF 7

K12425-001

ASP-184329-01

SM
J9
SCON
HC_B2B_14X40

2 OF 7

K12425-001

ASP-184329-01

+FMC_B_VADJ

C357	H63299-001	22UF	20%	6.3V X6S 0603
C364	A36096-030	0.1UF	10%	16V X7R 0402
C365	H63299-001	22UF	20%	6.3V X6S 0603
C366	A36096-030	0.1UF	10%	16V X7R 0402

+FMC_B_VREF

C367	A36096-030	0.1UF	10%	16V X7R 0402

+P3V3_IO2_FMC_13C

C368	H63299-001	22UF	20%	6.3V X6S 0603
C369	H63299-001	22UF	20%	6.3V X6S 0603
C370	A36096-030	0.1UF	10%	16V X7R 0402
C371	A36096-030	0.1UF	10%	16V X7R 0402

+P12V0_FMC_B

C372	H65936-001	22UF	10%	25V X6S 1206
C373	A36096-213	0.1UF	10%	25V X7R 0402

FMC B CONNECTOR-1

Tue Sep 26 11:47:54 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	55 OF 105

FMC+ CONNECTOR B (EAST)

J9
SCON
HC_14X40_ASP_VITA57P4
HC_B2B_14X40

K12425-001
ASP-184329-01
1 OF 7

		FMC_B_LA_0_DP	R2942		RES 0 1% 0201	FMC_B_LA_0_R_DP	G6	G18	FMC_B_LA_16_R_DP	R2974		RES 01% 0201	FMC_B_LA_16_DP						
		FMC_B_LA_0_DN	R2943		RES 0 1% 0201	FMC_B_LA_0_R_DN	G7	G19	FMC_B_LA_16_R_DN	R2975		RES 01% 0201	FMC_B_LA_16_DN						
		FMC_B_LA_1_DP	R2944		RES 0 1% 0201	FMC_B_LA_1_R_DP	D8	D20	FMC_B_LA_17_R_DP	R415		RES 01% 0201	FMC_B_LA_17_DP						
		FMC_B_LA_1_DN	R2945		RES 0 1% 0201	FMC_B_LA_1_R_DN	D9	D21	FMC_B_LA_17_R_DN	R2976		RES 01% 0201	FMC_B_LA_17_DN						
		FMC_B_LA_2_DP	R2946		RES 0 1% 0201	FMC_B_LA_2_R_DP	H7	C22	FMC_B_LA_18_R_DP	R2977		RES 01% 0201	FMC_B_LA_18_DP						
		FMC_B_LA_2_DN	R2947		RES 0 1% 0201	FMC_B_LA_2_R_DN	H8	C23	FMC_B_LA_18_R_DN	R2978		RES 01% 0201	FMC_B_LA_18_DN						
		FMC_B_LA_3_DP	R2948		RES 0 1% 0201	FMC_B_LA_3_R_DP	G9	H22	FMC_B_LA_19_R_DP	R2979		RES 01% 0201	FMC_B_LA_19_DP						
		FMC_B_LA_3_DN	R2949		RES 0 1% 0201	FMC_B_LA_3_R_DN	G10	H23	FMC_B_LA_19_R_DN	R2980		RES 01% 0201	FMC_B_LA_19_DN						
		FMC_B_LA_4_DP	R2950		RES 0 1% 0201	FMC_B_LA_4_R_DP	H10	G21	FMC_B_LA_20_R_DP	R2981		RES 01% 0201	FMC_B_LA_20_DP						
		FMC_B_LA_4_DN	R2951		RES 0 1% 0201	FMC_B_LA_4_R_DN	H11	G22	FMC_B_LA_20_R_DN	R2982		RES 01% 0201	FMC_B_LA_20_DN						
		FMC_B_LA_5_DP	R2952		RES 0 1% 0201	FMC_B_LA_5_R_DP	D11	H25	FMC_B_LA_21_R_DP	R2983		RES 01% 0201	FMC_B_LA_21_DP						
		FMC_B_LA_5_DN	R2953		RES 0 1% 0201	FMC_B_LA_5_R_DN	D12	H26	FMC_B_LA_21_R_DN	R2984		RES 01% 0201	FMC_B_LA_21_DN						
		FMC_B_LA_6_DP	R2954		RES 0 1% 0201	FMC_B_LA_6_R_DP	C10	G24	FMC_B_LA_22_R_DP	R2985		RES 01% 0201	FMC_B_LA_22_DP						
		FMC_B_LA_6_DN	R2955		RES 0 1% 0201	FMC_B_LA_6_R_DN	C11	G25	FMC_B_LA_22_R_DN	R2986		RES 01% 0201	FMC_B_LA_22_DN						
		FMC_B_LA_7_LT_DP	R2956		RES 0 1% 0201	FMC_B_LA_7_R_DP	H13	D23	FMC_B_LA_23_R_DP	R2987		RES 01% 0201	FMC_B_LA_23_DP						
		FMC_B_LA_7_LT_DN	R2957		RES 0 1% 0201	FMC_B_LA_7_R_DN	H14	D24	FMC_B_LA_23_R_DN	R2988		RES 01% 0201	FMC_B_LA_23_DN						
		FMC_B_LA_8_LT_DP	R2958		RES 0 1% 0201	FMC_B_LA_8_R_DP	G12	H28	FMC_B_LA_24_R_DP	R2989		RES 01% 0201	FMC_B_LA_24_DP						
		FMC_B_LA_8_LT_DN	R2959		RES 0 1% 0201	FMC_B_LA_8_R_DN	G13	H29	FMC_B_LA_24_R_DN	R2990		RES 01% 0201	FMC_B_LA_24_DN						
		FMC_B_LA_9_DP	R2960		RES 0 1% 0201	FMC_B_LA_9_R_DP	D14	G27	FMC_B_LA_25_R_DP	R2991		RES 01% 0201	FMC_B_LA_25_DP						
		FMC_B_LA_9_DN	R2961		RES 0 1% 0201	FMC_B_LA_9_R_DN	D15	G28	FMC_B_LA_25_R_DN	R2992		RES 01% 0201	FMC_B_LA_25_DN						
		FMC_B_LA_10_DP	R2962		RES 0 1% 0201	FMC_B_LA_10_R_DP	C14	D26	FMC_B_LA_26_R_DP	R2993		RES 01% 0201	FMC_B_LA_26_DP						
		FMC_B_LA_10_DN	R2963		RES 0 1% 0201	FMC_B_LA_10_R_DN	C15	D27	FMC_B_LA_26_R_DN	R2994		RES 01% 0201	FMC_B_LA_26_DN						
		FMC_B_LA_11_DP	R2964		RES 0 1% 0201	FMC_B_LA_11_R_DP	H16	C26	FMC_B_LA_27_R_DP	R2995		RES 01% 0201	FMC_B_LA_27_DP						
		FMC_B_LA_11_DN	R2965		RES 0 1% 0201	FMC_B_LA_11_R_DN	H17	C27	FMC_B_LA_27_R_DN	R2996		RES 01% 0201	FMC_B_LA_27_DN						
		FMC_B_LA_12_DP	R2966		RES 0 1% 0201	FMC_B_LA_12_R_DP	G15	H31	FMC_B_LA_28_R_DP	R2997		RES 01% 0201	FMC_B_LA_28_LT_DP						
		FMC_B_LA_12_DN	R2967		RES 0 1% 0201	FMC_B_LA_12_R_DN	G16	H32	FMC_B_LA_28_R_DN	R2998		RES 01% 0201	FMC_B_LA_28_LT_DN						
		FMC_B_LA_13_DP	R2968		RES 0 1% 0201	FMC_B_LA_13_R_DP	D17	G30	FMC_B_LA_29_R_DP	R2999		RES 01% 0201	FMC_B_LA_29_LT_DP						
		FMC_B_LA_13_DN	R2969		RES 0 1% 0201	FMC_B_LA_13_R_DN	D18	G31	FMC_B_LA_29_R_DN	R3000		RES 01% 0201	FMC_B_LA_29_LT_DN						
		FMC_B_LA_14_DP	R2970		RES 0 1% 0201	FMC_B_LA_14_R_DP	C18	H34	FMC_B_LA_30_R_DP	R3001		RES 01% 0201	FMC_B_LA_30_LT_DP						
		FMC_B_LA_14_DN	R2971		RES 0 1% 0201	FMC_B_LA_14_R_DN	C19	H35	FMC_B_LA_30_R_DN	R3002		RES 01% 0201	FMC_B_LA_30_LT_DN						
		FMC_B_LA_15_DP	R2972		RES 0 1% 0201	FMC_B_LA_15_R_DP	H19	G33	FMC_B_LA_31_R_DP	R3003		RES 01% 0201	FMC_B_LA_31_LT_DP						
		FMC_B_LA_15_DN	R2973		RES 0 1% 0201	FMC_B_LA_15_R_DN	H20	G34	FMC_B_LA_31_R_DN	R3004		RES 01% 0201	FMC_B_LA_31_LT_DN						
								H37	FMC_B_LA_32_R_DP	R3005		RES 01% 0201	FMC_B_LA_32_CON_DP						
								H38	FMC_B_LA_32_R_DN	R3006		RES 01% 0201	FMC_B_LA_32_CON_DN						
								G36	FMC_B_LA_33_R_DP	R3007		RES 01% 0201	FMC_B_LA_33_CON_DP						
								G37	FMC_B_LA_33_R_DN	R3008		RES 01% 0201	FMC_B_LA_33_CON_DN						

+FMC_B_VADJ
+P1V2_G3
+P1V8_G2

R1180 RES 0 0% 0.75W 1206
R1181 EMPTY 0 0% 0.75W 1206

DESIGN NOTE:
0 OHM OPTION PROVIDED ONLY TO ISOLATE VADJ FROM THE FMC CONNECTOR

+P12V0_FMC_B
+P3V3_IO2_FMC_13C

J9
SCON
HC_14X40_ASP_VITA57P4
HC_B2B_14X40

								D32	3P3VAUX										
														VADJ	E39				
														VADJ	F40				
														VADJ	G39				
								D40	3P3V					VADJ	H40				
								C39	3P3V										
								D36	3P3V										
								D38	3P3V										
								Z40	3P3V										
														VIO_B_M2C	K40	FMC_B_VIO_B_0_M2C	1	TP4	EMPTY SM
														VIO_B_M2C	J39	FMC_B_VIO_B_1_M2C	1	TP5	EMPTY SM
								C35	12P0V										
								C37	12P0V					VREF_B_M2C	K1	FMC_B_VREF_B_M2C	1	TP6	EMPTY SM
								L36	12P0V					VREF_A_M2C	H1	FMC_B_VREF_A_M2C			
								L37	12P0V										
								L40	12P0V										
59 56	IN	FMC_B_POK_C2M						D1	PG_C2M					PG_M2C	F1	FMC_B_PG_M2C	56		
60 56	OUT	FMC_B_PRSNT_N						H2	PRSNT_M2C_L					RES2	L32				
								Z1	HSPC_PRSNT_M2C_L					RES3	L33				
56	BI	FMC_B_SDA_3V3_CON						C31	SDA					TRST_L	D34	FMC_B_TRST_L	R457 1	2 RES 10K 1% 0.0625W 0402	
56	BI	FMC_B_SCL_3V3_CON						C30	SCL					TMS	D33			FMC_B_TMS	IN 56 59
														TDO	D31			FMC_B_TDO	OUT 56 59
														TDI	D30			FMC_B_TDI	IN 56 59
58 16	OUT	FMC_B_CLK2_M2C_DP	C151	1	2	0.22UF 16V	C_FMC_B_CLK2_M2C_DP	K4	CLK2_BIDIR_P					TCK	D29			FMC_B_TCK	IN 56 59
58 16	OUT	FMC_B_CLK2_M2C_DN	C152	1	2	0.22UF 16V	C_FMC_B_CLK2_M2C_DN	K5	CLK2_BIDIR_N										
								J2	CLK3_BIDIR_P					CLK0_M2C_P	H4	C_FMC_B_CLK0_DP	C153 1	2 0.22UF 16V	FMC_B_CLK0_M2C_DP OUT 16 58
								J3	CLK3_BIDIR_N					CLK0_M2C_N	H5	C_FMC_B_CLK0_DN	C154 1	2 0.22UF 16V	FMC_B_CLK0_M2C_DN OUT 16 58
								B1	CLK_DIR					CLK1_M2C_P	G2	C_FMC_B_CLK1_DP	C155 1	2 0.22UF 16V	FMC_B_CLK1_M2C_DP OUT 16 58
														CLK1_M2C_N	G3	C_FMC_B_CLK1_DN	C156 1	2 0.22UF 16V	FMC_B_CLK1_M2C_DN OUT 16 58
+P3V3_IO2_FMC_13C																			
								C34	GA0										
56		FMC_B_CLK_DIR						D35	GA1										
								B40	RES0										
								L1	RES1										
58 16	IN	FMC_B_REFCLK_C2M_DP	R468	1	2 RES 0 0402	R_FMC_B_REFCLK_C2M_DP		L20	REFCLK_C2M_P					SYNC_C2M_P	L16	R_FMC_B_SYNC_C2M_DP	R469 1	2 RES 0 0402	FMC_B_SYNC_C2M_DP IN 16 58
58 16	IN	FMC_B_REFCLK_C2M_DN	R473	1	2 RES 0 0402	R_FMC_B_REFCLK_C2M_DN		L21	REFCLK_C2M_N					SYNC_C2M_N	L17	R_FMC_B_SYNC_C2M_DN	R474 1	2 RES 0 0402	FMC_B_SYNC_C2M_DN IN 16 58
58 16	OUT	FMC_B_REFCLK_M2C_DP	C157	1	2 0.22UF 16V	C_FMC_B_REFCLK_M2C_DP		L24	REFCLK_M2C_P					SYNC_M2C_P	L28	R_FMC_B_SYNC_M2C_DP	R477 1	2 RES 0 0402	FMC_B_SYNC_M2C_DP OUT 16
58 16	OUT	FMC_B_REFCLK_M2C_DN	C446	1	2 0.22UF 16V	C_FMC_B_REFCLK_M2C_DN		L25	REFCLK_M2C_N					SYNC_M2C_N	L29	R_FMC_B_SYNC_M2C_DN	R481 1	2 RES 0 0402	FMC_B_SYNC_M2C_DN OUT 16

5 OF 7

K12425-001
ASP-184329-01

+FMC_B_VADJ
+FMC_B_VREF
+P3V3_IO2_FMC_13C

+P1V2_G3
+P3V3_IO2_FMC_13C

C503 A36096-213 0.1UF 10% 25V X7R 0402
C504 D97712-022 1UF 10% 16V X6S 0402
C505 A36096-213 0.1UF 10% 25V X7R 0402

U62
IC
HC_MAX3378EETD_T

			10	VL	VCC	14													
56 15	BI	FMC_A_SDA_1V2	1	IO_VL1	IO_VCC1	13	FMC_A_SDA_3V3_IO	BI	56										
56 15	BI	FMC_A_SCL_1V2	2	IO_VL2	IO_VCC2	12	FMC_A_SCL_3V3_IO	BI	56										
56 16	BI	FMC_B_SDA_1V2	5	IO_VL3	IO_VCC3	9	FMC_B_SDA_3V3_IO	BI	56										
56 16	BI	FMC_B_SCL_1V2	6	IO_VL4	IO_VCC4	8	FMC_B_SCL_3V3_IO	BI	56										
			15	EP	NC	4													
					NC	11													
			7	GND															
					THREE_STATE_N	3													

+P1V2_G3

C35081-002
MAX3378EETD+T

+P3V3_IO2_FMC_13C

R520 1 2 RES 10K 1% 0.0625W 0402 FMC_B_CLK_DIR 56
R521 1 2 EMPTY 10K 1% 0.0625W 0402

56	BI	FMC_B_LA_33_CON_DP	R482	1	2	RES 0 5% 0.0625W 0402	FMC_B_LA_33_LT_DP	BI	57										
56	BI	FMC_B_LA_33_CON_DN	R483	1	2	RES 0 5% 0.0625W 0402	FMC_B_LA_33_LT_DN	BI	57										
			R484	1	2	EMPTY 0 0402	FMC_B_PCIE_PERSTN_3V3	BI	62										
			R485	1	2	EMPTY 0 0402	FMC_B_PCIE_WAKEN_3V3	BI	62										
56	BI	FMC_B_LA_32_CON_DP	R486	1	2	RES 0 5% 0.0625W 0402	FMC_B_LA_32_LT_DP	BI	57										
56	BI	FMC_B_LA_32_CON_DN	R487	1	2	RES 0 5% 0.0625W 0402	FMC_B_LA_32_LT_DN	BI	57										

R488 EMPTY 100 1% 0.0625W 0402

+P3V3_IO2_FMC_13C

59 56		FMC_B_TMS	R511	1	2	RES 10K 1% 0.0625W 0402													
59 56		FMC_B_TDI	R512	1	2	RES 10K 1% 0.0625W 0402													
59 56		FMC_B_TDO	R513	1	2	RES 10K 1% 0.0625W 0402													
60 56		FMC_B_PRSNT_N	R514	1	2	RES 10K 1% 0.0625W 0402													
56		FMC_B_PG_M2C	R515	1	2	RES 10K 1% 0.0625W 0402													
56	BI	FMC_B_SDA_3V3_CON	R516	1	2	RES 4.7K 1% 0.0625W 0402													
56	BI	FMC_B_SCL_3V3_CON	R517	1	2	RES 4.7K 1% 0.0625W 0402													

+P1V2_G3

56 16	BI	FMC_B_SDA_1V2	R1302	1	2	RES 4.7K 1% 0.0625W 0402													
56 16	BI	FMC_B_SCL_1V2	R1371	1	2	RES 4.7K 1% 0.0625W 0402													
56 15	BI	FMC_A_SDA_1V2	R1562	1	2	RES 4.7K 1% 0.0625W 0402													
56 15	BI	FMC_A_SCL_1V2	R1563	1	2	RES 4.7K 1% 0.0625W 0402													

R518 A36092-023 1K 1% 0.063W RES 0402 FMC_B_TCK 56 59
R519 A36092-023 1K 1% 0.063W RES 0402 FMC_B_POK_C2M 56 59

54	BI	FMC_A_SDA_3V3_CON	R1182	1	2	EMPTY 0 5% 0.0625W 0402	FMC_A_SDA_3V3	BI	61										
54	BI	FMC_A_SCL_3V3_CON	R1183	1	2	EMPTY 0 5% 0.0625W 0402	FMC_A_SCL_3V3	BI	61										
			R673	1	2	RES 0 0402	FMC_A_SDA_3V3_IO	BI	56										
			R674	1	2	RES 0 0402	FMC_A_SCL_3V3_IO	BI	56										

CAD NOTE: PLEASE CONNECT THESE AS TRIPAD.

56	BI	FMC_B_SDA_3V3_CON	R1184	1	2	EMPTY 0 5% 0.0625W 0402	FMC_B_SDA_3V3	BI	62										
56	BI	FMC_B_SCL_3V3_CON	R1185	1	2	EMPTY 0 5% 0.0625W 0402	FMC_B_SCL_3V3	BI	62										
			R677	1	2	RES 0 0402	FMC_B_SDA_3V3_IO	BI	56										
			R681	1	2	RES 0 0402	FMC_B_SCL_3V3_IO	BI	56										

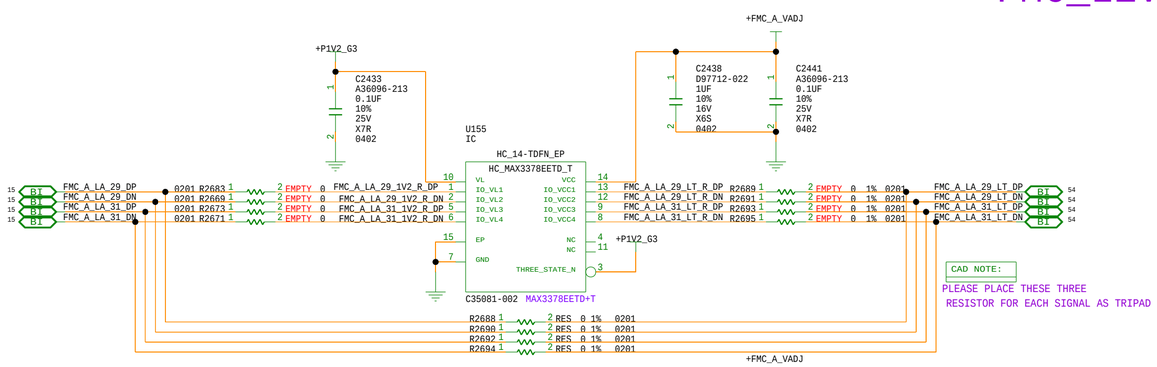
CAD NOTE: PLEASE CONNECT THESE AS TRIPAD.

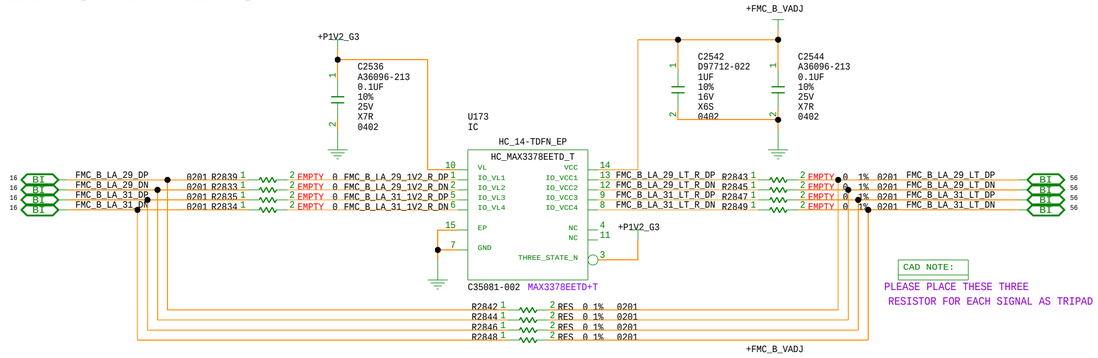
Tue Sep 26 11:47:55 2023

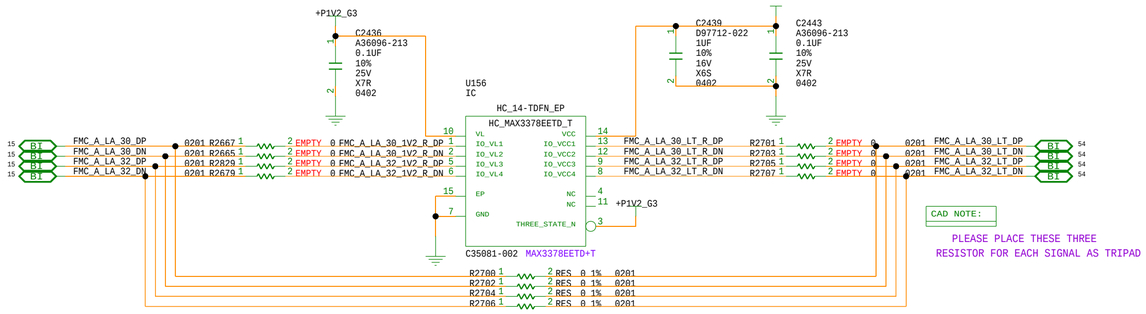
DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	56 OF 105

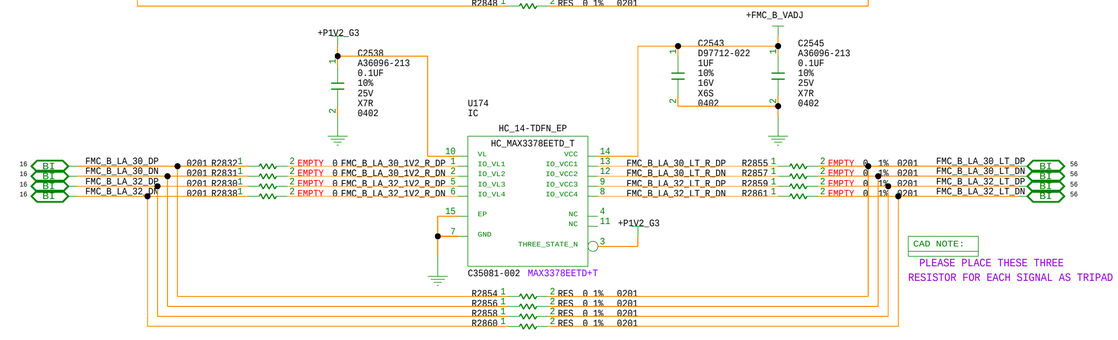
FMC B CONNECTOR-2

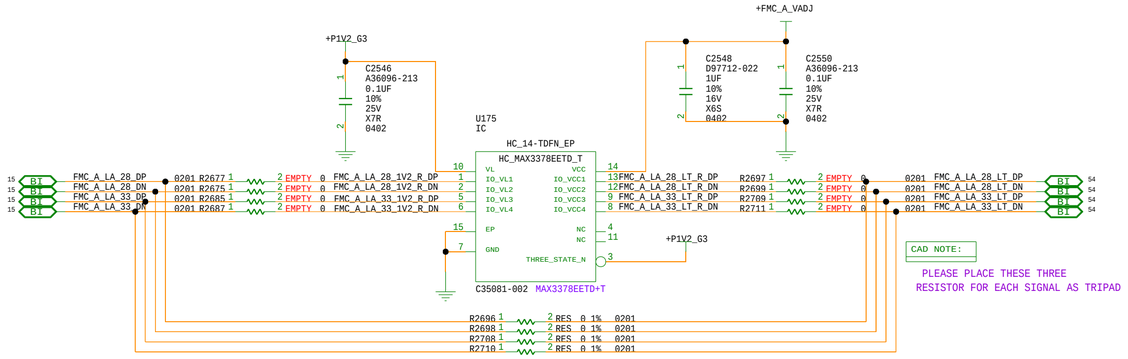
FMC_LEVEL SHIFTERS

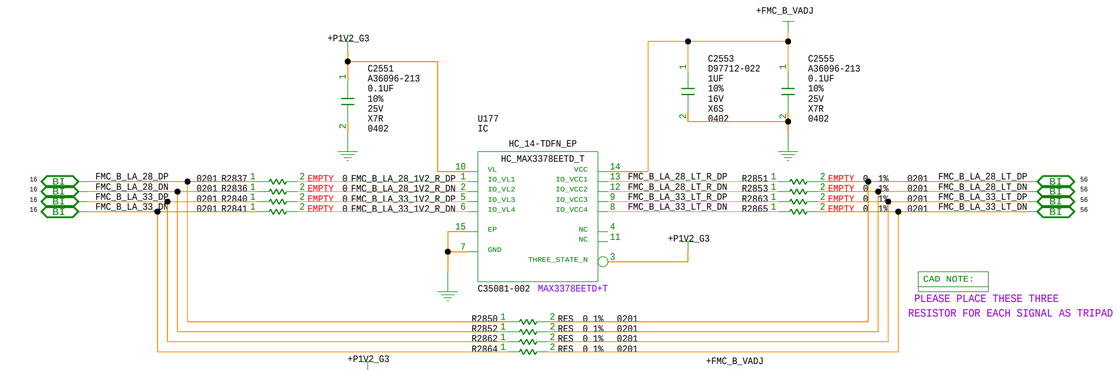


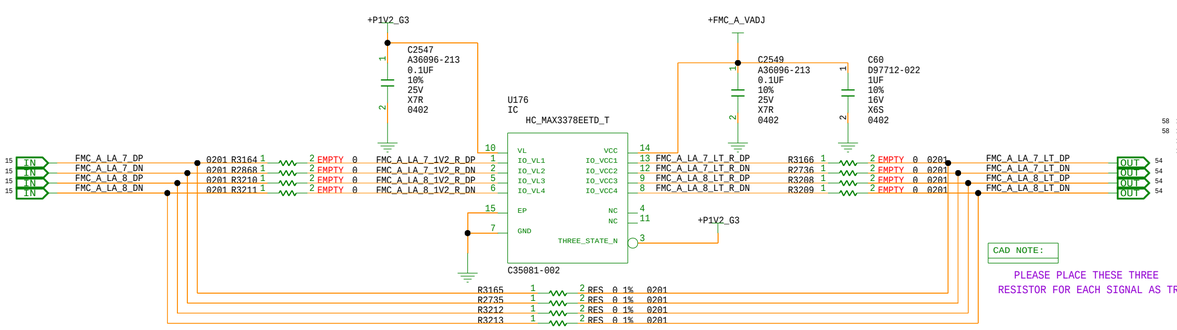


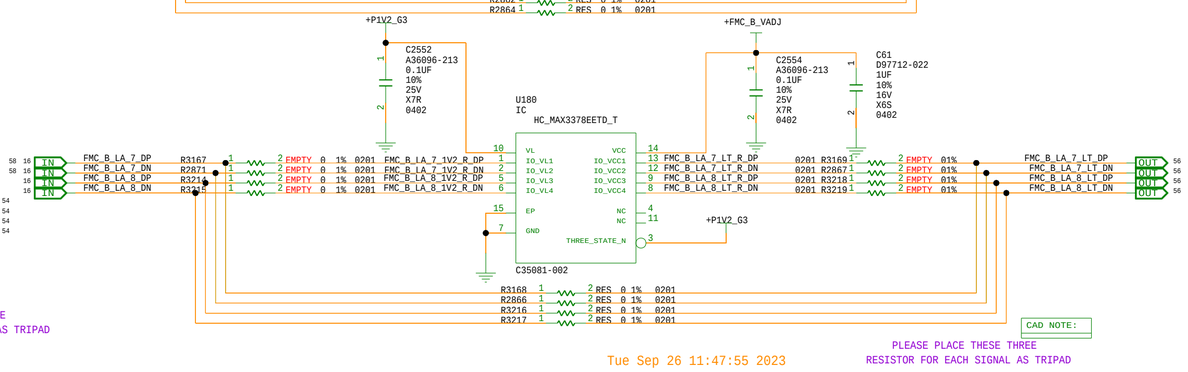










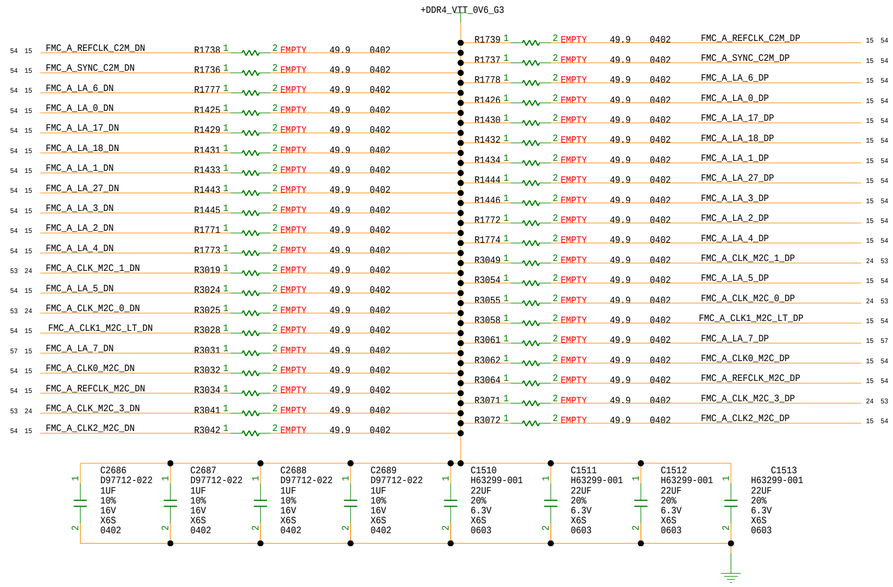


Tue Sep 26 11:47:55 2023

DEPARTMENT: UNKNOWN	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	SIZE: C+	CODE: 34649	DOCUMENT NUMBER: 150-0330690-A2 REV: 2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET: 57 OF 105

FMC_LEVEL SHIFTERS

FMC_TERMINATIONS



Tue Sep 26 11:47:56 2023

DEPARTMENT: UNKNOWN	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	SIZE: C+	CODE: 34649	DOCUMENT NUMBER: 150-0330690-A2 REV: 2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 58 OF 105

FMC_TERMINATIONS

MAX10- Intel® MAX® 10 FPGA
PWR MAX-10- I

BGA
U2
IC

+P3V3 — HC_10M16SC — +P3V3

BANK 1A/1B

83	IN	P1V2_IO_POK					D4
83	OUT	P1V2_IO_EN	R1621	1	2 RES 0	P1V2_IO_R_EN	E4
92	IN	VCCERT1_1V0_POK					C2
92	OUT	VCCERT1_1V0_EN					D2
97	OUT	P1V2_G3_EN	R1622	1	2 RES 0	P1V2_G3_R_EN	G6
97	IN	P1V2_G3_POK	R3220	1	2 RES 0	P1V2_G3_R_POK	H6
94	IN	P1V8_G2_POK	R3221	1	2 RES 0	P1V8_G2_R_POK	B1
94	IN	P1V8_G2_EN	R1626	1	2 RES 0	P1V8_G2_R_EN	C1
102	IN	FMC_A_12V_POK	R3222	1	2 RES 0	FMC_A_12V_R_POK	F5
102	OUT	FMC_A_12V_EN					E5
95	IN	VCCEHT_U1X_POK	R178	1	2 RES 0	VCCEHT_U1X_POK_R	D1
98	OUT	P1V8_G3_EN					E1
82	IN	P3V3_POK					G3
81	IN	P1V8_STB_RUN					F2
99	OUT	DIMM_VTT_POK	R3223	1	2 RES 0	DIMM_VTT_R_POK	F1
99	OUT	DIMM_VTT_EN	R2419	1	2 RES 0	DIMM_VTT_R_EN	G1
99	IN	DDR4_VTT_POK	R3242	1	2 RES 0	DDR4_VTT_R_POK	G7
			R106	1	2 RES 10K	PWR_M10_JTAGEN	H7
99	OUT	DDR4_VTT_EN	R2420	1	2 RES 0	DDR4_VTT_R_EN	H2
81	IN	P1V8_STB_POK	R3224	1	2 RES 0	P1V8_STB_R_POK	H1
64	IN	PWR_M10_TMS					J7
64	IN	PWR_M10_TCK					J8
64	IN	PWR_M10_TDI					H3
64	IN	PWR_M10_TDO					H4
100	OUT	P3V3_IO1_EN	R798	1	2 RES 0	P3V3_IO1_R_EN	J2
95	OUT	P2V5_G2_EN	R1618	1	2 RES 0	P2V5_G2_R_EN	J1
95	IN	P2V5_G2_POK	R3225	1	2 RES 0	P2V5_G2_R_POK	J6
100	IN	P3V3_IO1_POK	R3226	1	2 RES 0	P3V3_IO1_R_POK	K7
101	IN	P3V3_IO2_POK	R3227	1	2 RES 0	P3V3_IO2_R_POK	K2
101	OUT	P3V3_IO2_EN	R1619	1	2 RES 0	P3V3_IO2_R_EN	K1
84	OUT	VCCL_EN	R1620	1	2 RES 0	VCCL_R_EN	K4
84	IN	VCCL_POK	R3228	1	2 RES 0	VCCL_POK_R	K3
93	OUT	VCCERT2_1V0_Ux_EN	R3229	1	2 RES 0	VCCERT2_1V0_Ux_R_EN	L1
98	IN	P1V8_G3_POK	R179	1	2 RES 0	P1V8_G3_POK_R	L2
96	OUT	VCCEHT_U2X_POK	R180	1	2 RES 0	VCCEHT_U2X_POK_R	J3
51	OUT	P3V3_IO2_FET1_PMAX_EN					J4

BANK 2

IO_DIFFIO_RX_L1N							L3
IO_DIFFIO_RX_L1P	0V8_Ux1_R_EN	R1633	1	2 RES 0	0V8_Ux1_EN	OUT	89
IO_DIFFIO_RX_L2N	QSFPDD800_MODPRS_L_PWR_MAX10	R3174	1	2 RES 0	QSFPDD800_MODPRS_L	IN	46 47
IO_DIFFIO_RX_L2P	QSFPDD8_MODPRS_L_PWR_MAX10	R3175	1	2 RES 0	QSFPDD8_MODPRS_L	IN	42 47
IO_DIFFIO_RX_L3N	0V8_Ux1_R_POK	R3211	1	2 RES 0	0V8_Ux1_POK	OUT	89
IO_DIFFIO_RX_L3P	QSFP0_MOD_PRS_N_PWR_MAX10	R3176	1	2 RES 0	QSFP0_MOD_PRS_N	IN	37 47
IO_DIFFIO_RX_L4N	VCCERT2_1V0_Ux_R_POK	R3221	1	2 RES 0	VCCERT2_1V0_Ux_POK	IN	93
IO_DIFFIO_RX_L4P	QSFP1_MOD_PRS_N_PWR_MAX10	R3177	1	2 RES 0	QSFP1_MOD_PRS_N	IN	37 47
IO_DIFFIO_RX_L5N	SFP0_MOD3_PRSNT_N_PWR_MAX10	R3178	1	2 RES 0	SFP0_MOD3_PRSNT_N	IN	40 47
IO_DIFFIO_RX_L5P	FMC_B_12V_R_POK	R331	1	2 RES 0	FMC_B_12V_POK	IN	102
IO_DPCLK0_DIFFIO_RX_L24N					FMC_B_12V_EN	OUT	102
IO_DPCLK1_DIFFIO_RX_L24P	0V8_Ux0_R_POK	R332	1	2 RES 0	0V8_Ux0_POK	IN	88
IO_DIFFIO_RX_L25N	0V8_Ux0_R_EN	R1631	1	2 RES 0	0V8_Ux0_EN	OUT	88
IO_DIFFIO_RX_L25P	SFP1_MOD2_PRSNT_N_PWR_MAX10	R3179	1	2 RES 0	SFP1_MOD2_PRSNT_N	IN	40 47
IO_DIFFIO_RX_L26N	P0V8_G1_R_POK	R333	1	2 RES 0	P0V8_G1_POK	IN	94
IO_DIFFIO_RX_L26P	P0V8_G1_R_EN	R839	1	2 RES 0	P0V8_G1_EN	OUT	94
IO_DIFFIO_RX_L27N	SFP2_MOD1_PRSNT_N_PWR_MAX10	R3180	1	2 RES 0	SFP2_MOD1_PRSNT_N	IN	40 47
IO_DIFFIO_RX_L27P	SFP3_MOD0_PRSNT_N_PWR_MAX10	R3181	1	2 RES 0	SFP3_MOD0_PRSNT_N	IN	40 47
IO_DIFFIO_RX_L28N	QSFPDD3_3V3_MODPRS_L_PWR_MAX10	R3182	1	2 RES 0	QSFPDD3_3V3_MODPRS_L	IN	45 47
IO_DIFFIO_RX_L28P	QSFP2_MOD_PRS_N_PWR_MAX10	R3183	1	2 RES 0	QSFP2_MOD_PRS_N	IN	38 47
IO_PLL_L_CLKOUTN_DIFFIO_RX_L31N	QSFPDD2_MODPRS_L_PWR_MAX10	R3184	1	2 RES 0	QSFPDD2_MODPRS_L	IN	44 47
IO_PLL_L_CLKOUTP_DIFFIO_RX_L31P	QSFP_PRSNT_N_PWR_MAX10	R3185	1	2 RES 0	QSFP_PRSNT_N	IN	39 47
IO_DIFFIO_RX_L32N	QSFPDD1_MODPRS_L_PWR_MAX10	R3186	1	2 RES 0	QSFPDD1_MODPRS_L	IN	43
IO_DIFFIO_RX_L32P							R1
IO_VREFB2N0							R2
IO2							

1 OF 5

LEFT BANKS

978988

10M16SCU324C8G

R1665 A36092-023 1K 1% 0.063W RES 0402

61 59 SYS_PWR_OK — 2 — R1665 — 1

BGA
U2
IC

+P3V3 — HC_10M16SC — +P1V2_IO

BANK 3

64	IN	EXT_PROC_RSTN					R4
49	OUT	P3V3_IO1_FET2_PMAX_EN					T4
64	IN	EXT_RSV0					U3
64	IN	EXT_RSV1					V2
103	OUT	PWR_DISCH_G1_N					P6
91	IN	VCCERT_U2X_POK	R3235	1	2 RES 0	VCCERT_U2X_R_POK	P5
103	OUT	PWR_DISCH_G2_N					V3
49	OUT	P3V3_IO1_FET3_PMAX_EN					V4
50	OUT	P3V3_IO1_FET4_PMAX_EN					R5
56	OUT	FMC_B_POK_C2M					R6
103	IN	PWR_DISCH_G3_N					U5
54	OUT	FMC_A_POK_C2M					V5
91	IN	VCCERT_U1X_POK	R3236	1	2 RES 0	VCCERT_U1X_R_POK	T5
91	OUT	VCCERT_U1X_EN	R846	1	2 RES 0	VCCERT_U1X_R_EN	T6
77	IN	OVERTEMP0_N					T7
77	IN	OVERTEMP1_N					T8
98	IN	VCCEFUSECORE_POK	R3237	1	2 RES 0	VCCEFUSECORE_R_POK	N7
90	OUT	0V8_Ux2_EN	R1634	1	2 RES 0	0V8_Ux2_R_EN	N8
90	IN	0V8_Ux2_POK	R3238	1	2 RES 0	0V8_Ux2_R_POK	R8
91	OUT	VCCERT_U2X_EN	R1635	1	2 RES 0	VCCERT_U2X_R_EN	R9
96	OUT	VCCEHT_U2x_EN	R3239	1	2 RES 0	VCCEHT_U2x_R_EN	U7
98	OUT	VCCEFUSECORE_EN	R3240	1	2 RES 0	VCCEFUSECORE_R_EN	V7
104	OUT	PWR_DISCH_G_N					V9
77	IN	OVERTEMP3_N					U9
77	IN	OVERTEMP2_N					U8
95	IN	VCCEHT_U1X_EN	R3241	1	2 RES 0	VCCEHT_U1X_R_EN	V8
104	OUT	PWR_DISCH_G0_N					M8
59	IN	PWR_M10_50M					M9
74	IN	PWR_PB0	R306	1	2 RES 0	PWR_PB0_R	V10
56	IN	FMC_B_TDI					V11
56	OUT	FMC_B_TDO					T9
61 59	OUT	SYS_PWR_OK					T10
56	IN	FMC_B_TMS					V12
56	IN	FMC_B_TCK					U11
							U6
49	OUT	P3V3_IO1_FET1_PMAX_EN					V6

BANK 4

IO_DIFFIO_TX_RX_B1N							P10
IO_DIFFIO_TX_RX_B1P	IO_DIFFIO_TX_RX_B30N						N11
IO_DIFFIO_RX_B2N	IO_DIFFIO_TX_RX_B30P						U12
IO_DIFFIO_RX_B2P	IO_DIFFIO_RX_B31N						U13
IO_DIFFIO_TX_RX_B3N	IO_DIFFIO_RX_B31P						M10
IO_DIFFIO_TX_RX_B3P	IO_DIFFIO_TX_RX_B32N						L10
IO_DIFFIO_RX_B4N	IO_DIFFIO_TX_RX_B32P						R10
IO_DIFFIO_RX_B4P	IO_DIFFIO_TX_RX_B33N						R11
IO_DIFFIO_TX_RX_B5N	IO_DIFFIO_TX_RX_B33P						V13
IO_DIFFIO_TX_RX_B5P	IO_DIFFIO_RX_B34N						V14
IO_DIFFIO_RX_B6N	IO_DIFFIO_RX_B34P						R12
IO_DIFFIO_RX_B6P	IO_DIFFIO_TX_RX_B35N						R13
IO_DIFFIO_TX_RX_B13N	IO_DIFFIO_RX_B35P						T13
IO_DIFFIO_TX_RX_B13P	IO_DIFFIO_RX_B36N						T14
IO_DIFFIO_RX_B14N	IO_DIFFIO_RX_B36P						R14
IO_DIFFIO_RX_B14P	IO_DIFFIO_TX_RX_B37N						T15
IO_DIFFIO_TX_RX_B15N	IO_DIFFIO_TX_RX_B37P						V15
IO_DIFFIO_TX_RX_B15P	IO_DIFFIO_RX_B38N						U15
IO_DIFFIO_TX_RX_B16N	IO_DIFFIO_RX_B38P						U16
IO_DIFFIO_TX_RX_B16P	IO_DIFFIO_TX_RX_B41N						U17
IO_DIFFIO_RX_B17N	IO_DIFFIO_TX_RX_B41P						V16
IO_DIFFIO_RX_B17P	IO_DIFFIO_RX_B42N						V17
IO_CLK6N_DIFFIO_TX_RX_B18N	IO_DIFFIO_RX_B42P						T11
IO_CLK6P_DIFFIO_TX_RX_B18P	IO_VREFB4N0						T12
IO_DIFFIO_RX_B19N	IO4						
IO_DIFFIO_RX_B19P							
IO_CLK7N_DIFFIO_TX_RX_B20N							
IO_CLK7P_DIFFIO_TX_RX_B20P							
IO_DIFFIO_RX_B21N							
IO_DIFFIO_RX_B21P							
IO_DIFFIO_TX_RX_B22N							
IO_DIFFIO_TX_RX_B22P							
IO_DIFFIO_RX_B23N							
IO_DIFFIO_RX_B23P							
IO_VREFB3N0							
IO3							

2 OF 5

BOTTOM BANKS

978988

10M16SCU324C8G

+P3V3

U84
XTAL
30PPM
50MHZ
HC_SI510

R976 1 — 2 — 4.7K RES 0402 — SI510_OE

C2715
A36096-030
0.1UF
10%
16V
X7R
0402

VDD 6 · OE 2 · GND 3 · CLK+ 4 · CLK- 5 · NC 1

K14787-001

SYS_M10_50M_R — R977 1 — 2 RES 33.2 0402 — SYS_M10_50M — OUT 61
PWR_M10_50M_R — R978 1 — 2 RES 33.2 0402 — PWR_M10_50M — OUT 59

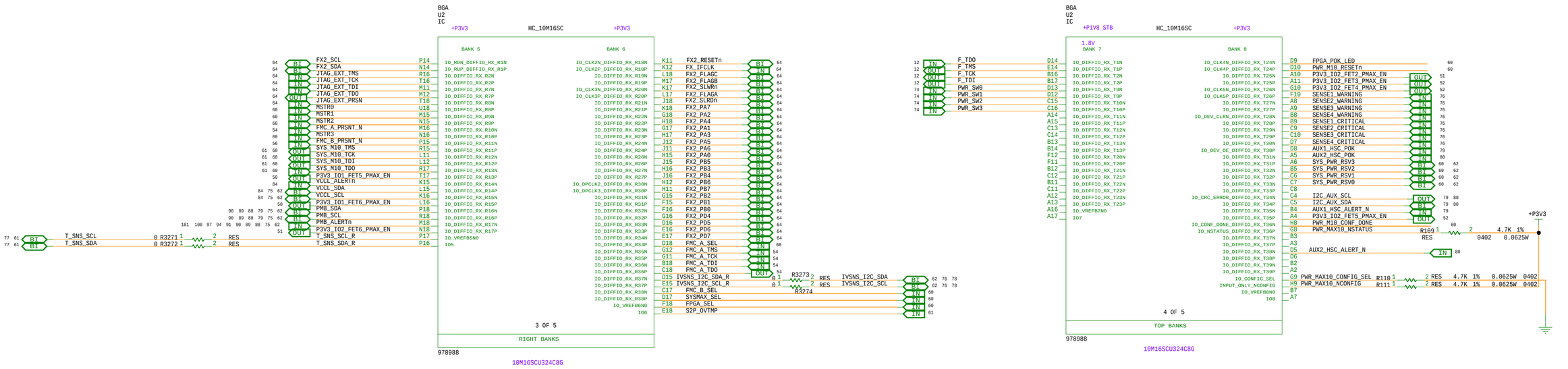
DESIGN NOTE: OPERATING IN DUAL CMOS BUFFER OPTION

Tue Sep 26 11:47:57 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE	SCALE:	DO NOT SCALE DRAWING	SHEET	59 OF 105
	INDIA, 560103				

MAX10- Intel® MAX® 10 FPGA

PWR MAX-10- II



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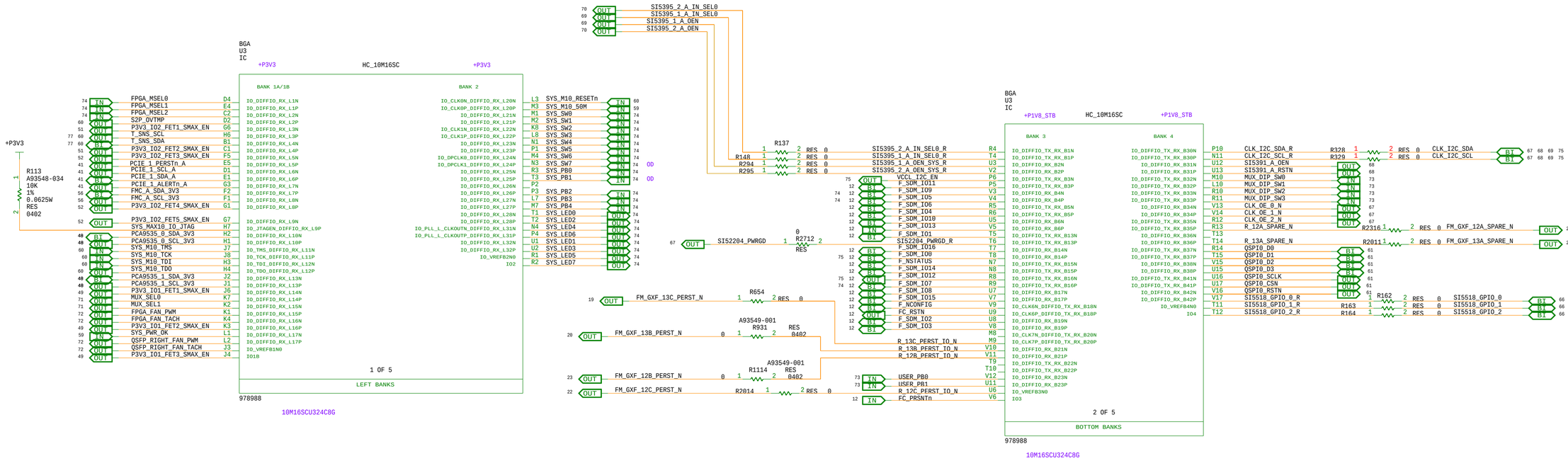
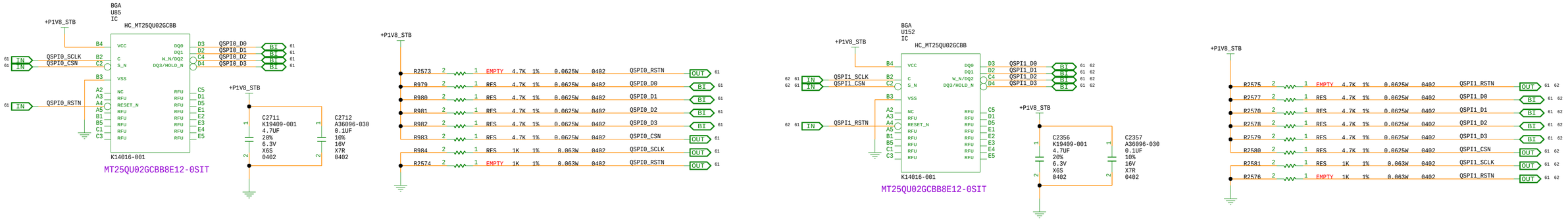
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER / REV
PSG	INTEL CORPORATION,BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2 / 2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 60 OF 105

MAX10- Intel® MAX® 10 FPGA
SYS MAX-10- I



QSPI



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DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SCALE:	DO NOT SCALE DRAWING	SHEET	61 OF 105

MAX10- Intel® MAX® 10 FPGA

SYS MAX-10- II

BGA
U3
IC

+P1V8_STB

HC_10M16SC

+P1V2_IO

BANK 5

IO_RDN_DIFFIO_RX_R1N		P14
IO_RUP_DIFFIO_RX_R1P		N14
IO_DIFFIO_RX_R2N		R16
IO_DIFFIO_RX_R2P		T16
IO_DIFFIO_RX_R7N		M11
IO_DIFFIO_RX_R7P		M12
IO_DIFFIO_RX_R8N		T18
IO_DIFFIO_RX_R8P		U18
IO_DIFFIO_RX_R9N		M15
IO_DIFFIO_RX_R9P		N15
IO_DIFFIO_RX_R10N		M16
IO_DIFFIO_RX_R10P		N16
IO_DIFFIO_RX_R11N		P15
IO_DIFFIO_RX_R11P		R15
IO_DIFFIO_RX_R12N		L11
IO_DIFFIO_RX_R12P		L12
IO_DIFFIO_RX_R13N		R17
IO_DIFFIO_RX_R13P		T17
IO_DIFFIO_RX_R14N		K15
IO_DIFFIO_RX_R14P		L15
IO_DIFFIO_RX_R15N		K16
IO_DIFFIO_RX_R15P		L16
IO_DIFFIO_RX_R16N		P18
IO_DIFFIO_RX_R16P		R18
IO_DIFFIO_RX_R17N		M18
IO_DIFFIO_RX_R17P		N18
IO_VREFB5N0		P17
IO5		P16

BANK 6

IO_CLK2N_DIFFIO_RX_R18N		K11
IO_CLK2P_DIFFIO_RX_R18P		K12
IO_DIFFIO_RX_R19N		L18
IO_DIFFIO_RX_R19P		M17
IO_CLK3N_DIFFIO_RX_R20N		K17
IO_CLK3P_DIFFIO_RX_R20P		L17
IO_DIFFIO_RX_R21N		J18
IO_DIFFIO_RX_R21P		K18
IO_DIFFIO_RX_R22N		G18
IO_DIFFIO_RX_R22P		H18
IO_DIFFIO_RX_R23N		G17
IO_DIFFIO_RX_R23P		H17
IO_DIFFIO_RX_R24N		J12
IO_DIFFIO_RX_R24P		J11
IO_DIFFIO_RX_R26N		H15
IO_DIFFIO_RX_R26P		J15
IO_DIFFIO_RX_R27N		H16
IO_DIFFIO_RX_R27P		J16
IO_DPCLK2_DIFFIO_RX_R30N		H12
IO_DPCLK3_DIFFIO_RX_R30P		H11
IO_DIFFIO_RX_R31N		G15
IO_DIFFIO_RX_R31P		F15
IO_DIFFIO_RX_R32N		F16
IO_DIFFIO_RX_R32P		G16
IO_DIFFIO_RX_R33N		D16
IO_DIFFIO_RX_R33P		E16
IO_DIFFIO_RX_R34N		E17
IO_DIFFIO_RX_R34P		D18
IO_DIFFIO_RX_R35N		G12
IO_DIFFIO_RX_R35P		G11
IO_DIFFIO_RX_R36N		B18
IO_DIFFIO_RX_R36P		C18
IO_DIFFIO_RX_R37N		D15
IO_DIFFIO_RX_R37P		E15
IO_DIFFIO_RX_R38N		C17
IO_DIFFIO_RX_R38P		D17
IO_VREFB6N0		F18
IO6		E18

3 OF 5

RIGHT BANKS

978988

10M16SCU324C8G

BGA
U3
IC

+P3V3

HC_10M16SC

+P3V3

BANK 7

IO_DIFFIO_RX_T1N		D14
IO_DIFFIO_RX_T1P		E14
IO_DIFFIO_RX_T2N		B16
IO_DIFFIO_RX_T2P		B17
IO_DIFFIO_RX_T9N		D13
IO_DIFFIO_RX_T9P		D12
IO_DIFFIO_RX_T10N		C15
IO_DIFFIO_RX_T10P		C16
IO_DIFFIO_RX_T11N		A14
IO_DIFFIO_RX_T11P		A15
IO_DIFFIO_RX_T12N		C13
IO_DIFFIO_RX_T12P		C14
IO_DIFFIO_RX_T13N		B13
IO_DIFFIO_RX_T13P		B14
IO_DIFFIO_RX_T20N		F12
IO_DIFFIO_RX_T20P		F11
IO_DIFFIO_RX_T21N		B12
IO_DIFFIO_RX_T21P		C12
IO_DIFFIO_RX_T22N		B11
IO_DIFFIO_RX_T22P		C11
IO_DIFFIO_RX_T23N		A12
IO_DIFFIO_RX_T23P		A13
IO_VREFB7N0		A16
IO7		A17

BANK 8

IO_CLK4N_DIFFIO_RX_T24N		D9
IO_CLK4P_DIFFIO_RX_T24P		D10
IO_DIFFIO_RX_T25N		A10
IO_DIFFIO_RX_T25P		A11
IO_CLK5N_DIFFIO_RX_T26N		G10
IO_CLK5P_DIFFIO_RX_T26P		F10
IO_DIFFIO_RX_T27N		A8
IO_DIFFIO_RX_T27P		A9
IO_DEV_CLRN_DIFFIO_RX_T28N		B8
IO_DIFFIO_RX_T28P		B9
IO_DIFFIO_RX_T29N		C9
IO_DIFFIO_RX_T29P		C10
IO_DIFFIO_RX_T30N		D7
IO_DEV_OE_DIFFIO_RX_T30P		D8
IO_DIFFIO_RX_T31N		A5
IO_DIFFIO_RX_T31P		A6
IO_DIFFIO_RX_T32N		B5
IO_DIFFIO_RX_T32P		C6
IO_DIFFIO_RX_T33N		C7
IO_DIFFIO_RX_T33P		C8
IO_CRC_ERROR_DIFFIO_RX_T34N		C4
IO_DIFFIO_RX_T34P		C5
IO_DIFFIO_RX_T35N		B4
IO_DIFFIO_RX_T35P		A4
IO_CONF_DONE_DIFFIO_RX_T36N		H8
IO_NSTATUS_DIFFIO_RX_T36P		G8
IO_DIFFIO_RX_T37N		B3
IO_DIFFIO_RX_T37P		A3
IO_DIFFIO_RX_T38N		D5
IO_DIFFIO_RX_T38P		D6
IO_DIFFIO_RX_T39N		B2
IO_DIFFIO_RX_T39P		A2
IO_CONFIG_SEL		G9
INPUT_ONLY_NCONFIG		H9
IO_VREFB8N0		B7
IO8		A7

4 OF 5

TOP BANKS

978988

10M16SCU324C8G

HYPER_RAM

+P1V8_STB

C2358 K19409-001 4.7uF 20% 6.3V X6S 0402

C2359 K45385-001 100nF 20% 25V X7R 0402

C2360 K45385-001 100nF 20% 25V X7R 0402

C2361 K45385-001 100nF 20% 25V X7R 0402

BGA
U153
IC

HC_W956D8MBYA

VCC	B4		DQ0	D3	HRAM_R_D0
VCCQ	D1		DQ1	D2	HRAM_R_D1
VCCQ	E4		DQ2	C4	HRAM_R_D2
			DQ3	D4	HRAM_R_D3
			DQ4	D5	HRAM_R_D4
			DQ5	E3	HRAM_R_D5
			DQ6	E2	HRAM_R_D6
			DQ7	E1	HRAM_R_D7
CS_N	A3	HRAM_CS			
CK_DP	B2	HRAM_CK_DP			
CK_DN	B1	HRAM_CK_DN			
RESET_N	A4	HRAM_RST_N			
RWDS	C3	HRAM_RWDS			
VSS	B3		RFU	A2	
VSSQ	C1		RFU	B5	
VSSQ	E5		RFU	C2	
			RFU	C5	
			RFU	A5	

M58157-001

W956D8MBYA5I

+P1V8_STB

R2594 4.7K 0.0625W RES 0402 A93548-517 1% — HRAM_CS

R2595 4.7K 0.0625W RES 0402 A93548-517 1% — HRAM_RST_N

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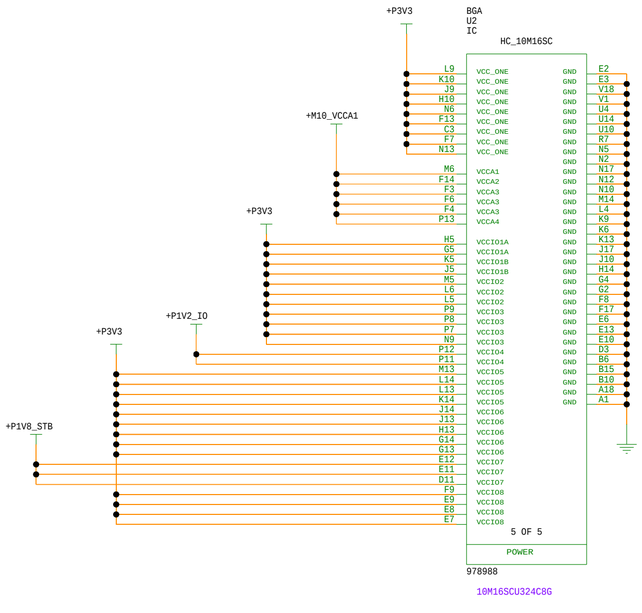
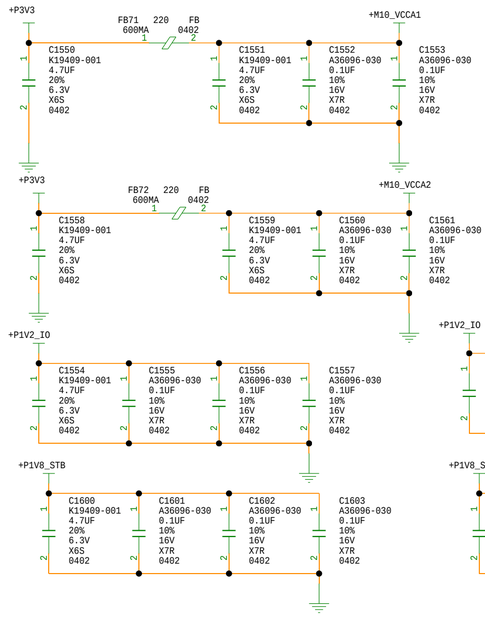
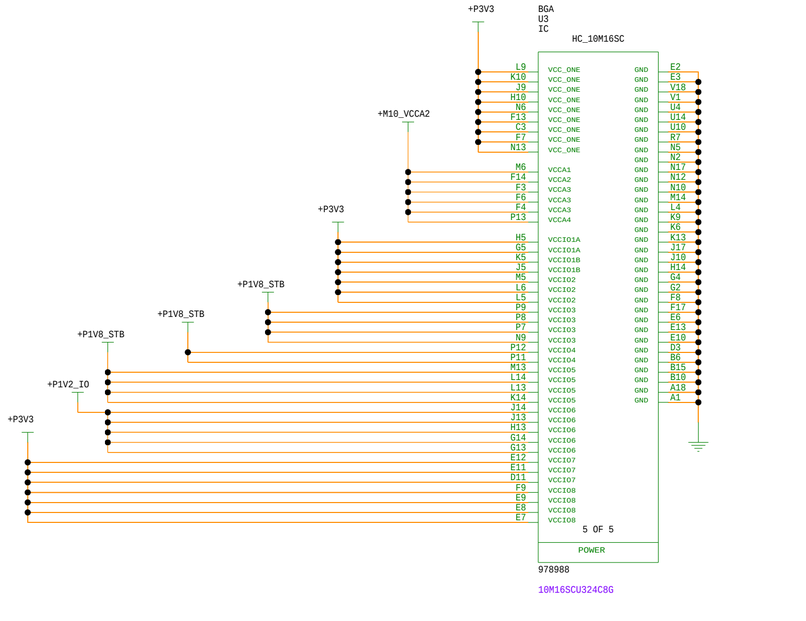
DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	62 OF 105

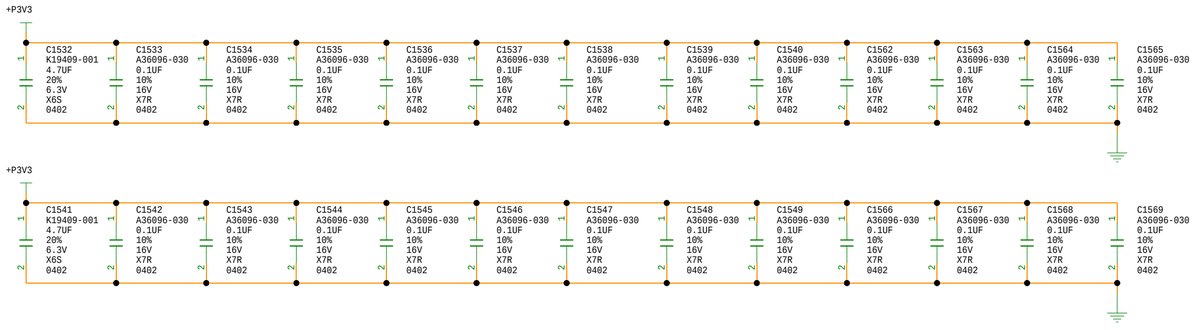
MAX10- Intel® MAX® 10 FPGA

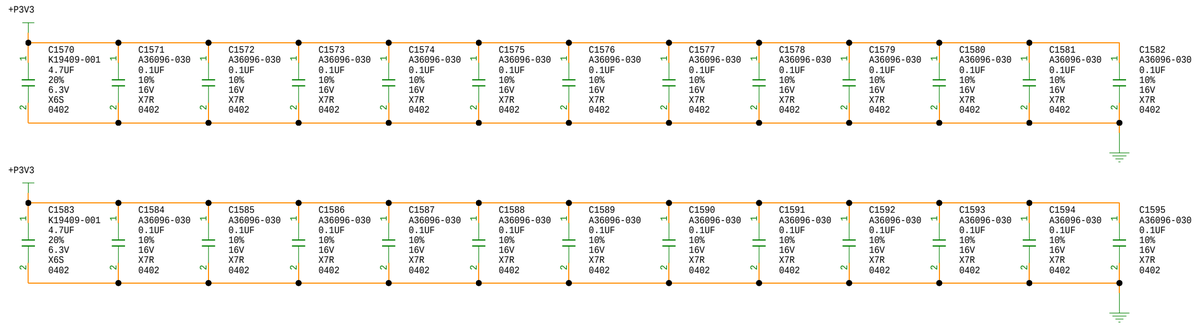
MAX-10 POWER











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DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
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	INTEL CORPORATION,BANGALORE	SCALE:	DO NOT SCALE DRAWING	SHEET	63 OF 105
	INDIA, 560103				

USB BLASTER

+P3V3
R78
A36092-023
1K
1%
0.063W
EMPTY
0402
R79 RES
10K 1%
0.0625W 0402
FX2_WAKEUP 64
R80
K32862-001
20K
0.1%
0.063W
RES
0402
C159
A36096-030
0.1UF
10%
16V
X7R
0402
TH
J10
CON
IO1 IO2 IO3 IO4 MH MH
CONN_USB_VCC
CONN_USB_DM
CONN_USB_DP
D83384-001
GND_EARTH
U15
HC_DIODE_TVS_ARRAY_2CH
VCC I/O1 I/O2 GND
K69553-001
60 OUT FX_IFCLK
R85 RES 33.2
FX_IFCLK_R
FX2_XTALIN
FX2_XTALOUT
Y1
XTAL
10PPM
24MHZ
HC_XTAL_4P
K15540-001
C160
K13748-001
12PF
5%
25V
C0G
0402
C161
K13748-001
12PF
5%
25V
C0G
0402
R1726 RES
1M 1%
0.25W 1206
C3045 1000PF
X7R 10%
1000V 1206
GND_EARTH
+P3V3
U16
IC
HC_CY7C68013A
AVCC AVCC VCC VCC VCC VCC VCC VCC
DMINUS DPLUS
IFCLK XTALIN XTALOUT
RESET_N SCL SDA
WAKEUP
CTL0/FLAGA CTL1/FLAGB CTL2/FLAGC
RDY0/SLRD RDY1/SLWR
CLKOUT
PA0/INT0_N PA1/INT1_N PA2/SLOE PA3/WU2 PA4/FIFOADR0 PA5/FIFOADR1 PA6/PKTEND PA7/FLAGD/SLCS_N
PB0/FD0 PB1/FD1 PB2/FD2 PB3/FD3 PB4/FD4 PB5/FD5 PB6/FD6 PB7/FD7
PD0/FD8 PD1/FD9 PD2/FD10 PD3/FD11 PD4/FD12 PD5/FD13 PD6/FD14 PD7/FD15
RESERVED
AGND AGND
GND GND GND GND GND GND GND
THPAD
FX2_PA0 FX2_PA1 FX2_PA2 FX2_PA3 FX2_PA4 FX2_PA5 FX2_PA6 FX2_PA7
FX2_RESETn FX2_SCL FX2_SDA
FX2_WAKEUP
FX2_FLAGA FX2_FLAGB FX2_FLAGC
FX2_SLRDn FX2_SLWRN
FX2_PB0 FX2_PB1 FX2_PB2 FX2_PB3 FX2_PB4 FX2_PB5 FX2_PB6 FX2_PB7
FX2_PD0 FX2_PD1 FX2_PD2 FX2_PD3 FX2_PD4 FX2_PD5 FX2_PD6 FX2_PD7
K33816-001
CY7C68013A-56LTXCx
+P3V3
R81
A93548-034
10K
1%
0.0625W
EMPTY
0402
R82 RES
5% 0
0402 0.0625W
FX2_RESETN_R
R83
A93548-596
100K
1%
0.0625W
RES
0402
U14
IC
HC_MAX81X
GND VCC RESET_N MR_N
D16587-001
MAX811SEUS+T 1
+P3V3
C158
K19409-001
4.7UF
20%
6.3V
X6S
0402
PLACED CLOSE TO CY7C68013
+P3V3
C162 C163 C164 C165 C166 C167 C168 C169 C170
A36096-030 0.1UF 10% 16V X7R 0402
H80885-001 10UF 20% 6.3V X6S 0402
TH
J56
EMPTY
HC_HDR_1X4
IO1 IO2 IO3 IO4
FX2_SCL
FX2_SDA
C70742-002
+P3V3
R86 RES
4.7K 1%
0.0625W 0402
FX2_SCL
R87 RES
4.7K 1%
0.0625W 0402
FX2_SDA
+P3V3
R92 RES
1% 10K
0402 0.0625W
JTAG_EXT_TDO
R96 RES
1% 10K
0402 0.0625W
JTAG_EXT_TMS
R98 RES
1% 10K
0402 0.0625W
JTAG_EXT_TDI
R101 RES
1% 1K
0402 0.063W
JTAG_EXT_TCK
+P3V3
R1727 RES
1% 10K
0402 0.0625W
PWR_M10_TDO
R1728 RES
1% 10K
0402 0.0625W
PWR_M10_TMS
R1729 RES
1% 10K
0402 0.0625W
PWR_M10_TDI
R1730 RES
1% 1K
0402 0.063W
PWR_M10_TCK
+P3V3
R1664
A93548-517
4.7K
1%
0.0625W
RES
0402
R88 R89 R90 R91 R93 R94 R97 R99 R100 R102 R103 R104
RES 0 EMPTY 0
PWR_M10_TCK JTAG_EXT_TCK
PWR_M10_TDO JTAG_EXT_TDO
PWR_M10_TMS JTAG_EXT_TMS
PWR_M10_TDI JTAG_EXT_TDI
FX2_PD0 FX2_PD3 FX2_PD1 FX2_PD2
TH
J11
CON
IO1 IO2 IO3 IO4 IO5 IO6 IO7 IO8 IO9 IO10
K10905-001
JTAG_IO1 JTAG_IO3 JTAG_IO5 JTAG_IO7 JTAG_IO9
+P3V3
R95
A93548-517
4.7K
1%
0.0625W
RES
0402
JTAG_IO2
JTAG_IO8 JTAG_IO10
R1662 R1663
A93548-517 4.7K 1% 0.0625W RES 0402
C171
A36096-030
0.1UF
10%
16V
X7R
0402
C172 C173 C174 C175 C3027
A36095-047
15PF
5%
50V
C0G
0402
C3024 C3025 C3026
A36095-047
15PF
5%
50V
C0G
0402
R1485 R1486 R1487 R1488
RES 240
JTAG_EXT_PRSN
EXT_PROC_RSTN
EXT_RSV0
EXT_RSV1

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DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
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USB BLASTER

1PPS INOUT

CAD NOTE: PLEASE OVERLAP THIS RES ACROSS 5 AND 3 PINS OF OPAMP

R105 A93549-001 0 5% 0.0625W EMPTY 0402

+P5V_SMA

C247 1UF 25V X6S 0402

U63 H11519-001 HC_TLV3501 IC SOT23

TLV3501AIDBVR

Pin 6 of TLV3501A =0 Output ON
Pin 6 of TLV3501A =1 Output High-Z

TO BE CHECKED FOR SLOWER RAMP RATE.

VIN MIN 0-0.5V
VIN MAX 0-5.5V

GDZ3V3LP3
VRMAX VZENER (V) =
X3-DFN0603-2

J14 CON TH — SMA_1PPS_OUT

D27 A53075-002 PGB1010603MR 0A DIO 0603

LTI-SASF546-P26-X1

R135 A93548-045 49.9 1% 0.0625W RES 0402

CLK_1PPS_OUT_MUX_SMA

COMPE_VREF_1P65V 65

R2339 A93549-001 0 5% 0.0625W RES 0402 — SHDN_1PPS_OUT

CAD NOTE: Please route COMPE_VREF_1P65V as a wide trace and away from any noisy traces.

J16 K10975-001 CON TH — SMA_1PPS_IN

D24 A53075-002 PGB1010603MR 0A DIO 0603

LTI-SASF546-P26-X1

R2337 A93548-045 49.9 1% 0.0625W RES 0402 — SMA_1PPS_IN_R

R136 A93548-048 249 1% 0.0625W RES 0402 — SMA_1PPS_R

C251 D70542-023 15pF 5% 25V C0G 0201

D28 M48254-001 GDZ3V3LP3-7 5mA DIO SM

+P3V3_SMA

C248 1UF 25V X6S 0402

R139 1K 0.063W RES 1% 0402

R140 150K 0.0625W RES 0.1% 0402

SMA_1PPS_FB

SMA_1PPS_IN_P

COMPE_VREF_0P257V

U72 H11519-001 HC_TLV3501 IC SOT23

TP94 EMPTY SM

R144 20K 0.063W RES 0.1% 0402

R145 1.69K 0.0625W A93548-582 1% RES 0402

SHDN_1PPS_IN

R2338 A93549-001 0 5% 0.0625W RES 0402

R3248 C79651-139 499 0.1% 0.0625W RES 0402

R3249 K15779-001 560 5% 0.1W RES 0402

1PPS_SMA_IN_1V8 — OUT 66

CAD NOTE: Please route COMPE_VREF_0P257V as a wide trace and away from any noisy traces.

CAD NOTE: PLEASE OVERLAP THIS RES ACROSS 5 AND 3 PINS OF OPAMP

R108 A93549-001 0 5% 0.0625W EMPTY 0402

+P5V_SMA

C254 1UF 25V X6S 0402

U78 H11519-001 HC_TLV3501 IC SOT23

TP98

CLK_10M_OUT_MUX_SMA

COMPE_VREF_1P65V 65

R2340 A93549-001 0 5% 0.0625W RES 0402 — SHDN_10MHZ_OUT

DESIGN NOTE:

GDZ3V3LP3
VRMAX VZENER (V) =
X3-DFN0603-2

J17 CON TH — SMA_10MHZ_OUT

D29 A53075-002 PGB1010603MR 0A DIO 0603

LTI-SASF546-P26-X1

C255 16V X7R 0.1UF 10% 0402

SMA_10MHZ_OUT_C

DESIGN NOTE:

SHDN_10MHZ_OUT= 0 DEFAULT, NO CLOCK
SHDN_10MHZ_OUT= 1 DRIVING 10MHZ CLOCK

10MHZ INOUT
OR
1PPS OUT

DESIGN NOTE:

PIN 6 OF TLV3501A =0 OUTPUT ON
PIN 6 OF TLV3501A =1 OUTPUT HIGH-Z

J25 CON TH — SMA_10MHZ_IN

D21 A53075-002 PGB1010603MR 0A DIO 0603

LTI-SASF546-P26-X1

R2571 A93548-045 49.9 1% 0.0625W RES 0402 — SMA_10MHZ_IN_C

R2572 A93548-048 249 1% 0.0625W RES 0402 — SMA_10MHZ_IN_R

C2351 D70542-023 15pF 5% 25V C0G 0201

VR1 M48254-001 GDZ3V3LP3-7 5mA DIO SM

+P3V3_SMA

C256 25V X6S 1UF 10% 0402

R741 A36092-023 1K 0.063W 1% RES 0402

R744 150K 0.0625W RES 0.1% 0402 — SMA_10MHZ_FB

TP100 EMPTY SM

SMA_10MHZ_IN_P

COMPE_VREF_1P65V 65

U83 H11519-001 HC_TLV3501 IC SOT23

TP101 EMPTY SM

R821 20K 0.063W RES 0.1% 0402

R828 20K 0.063W RES 0.1% 0402

1.65V

0-3.3V

R3253 C79651-139 499 0.1% 0.0625W RES 0402

10MHZ_SMA_IN — OUT 66

R3254 K15779-001 560 5% 0.1W RES 0402

R2341 A93549-001 0 5% 0.0625W RES 0402 — SHDN_10MHZ_IN

DESIGN NOTE:

SHDN_10MHZ_IN =0 INPUT ENABLED
SHDN_10MHZ_IN =1 INPUT DISABLED

DESIGN NOTE:

SHDN_1PPS_TO_10MHZ= 0 DEFAULT, NO CLOCK
SHDN_1PPS_TO_10MHZ= 1 DRIVING 1PPS CLOCK

+P5V_SMA — C249 H81594-001 1UF 10% 25V X6S 0402

+P3V3_SMA — C250 H81594-001 1UF 10% 25V X6S 0402

U75 IC — VH, VDD, OA, IN_A, IN_B, GND, PD

M44051-001

ISL55110IVZ-T7A

R138 C48657-447 51 1% 0.05W RES 0201 — CLK_1PPS_OUT_MUX_SMA_R

R143 C48657-447 51 1% 0.05W RES 0201 — CLK_10M_OUT_MUX_SMA_R

CLK_1PPS_OUT_SMA — IN 66

CLK_10M_OUT_SMA — IN 66

PD_SMA_OUT — TP95

R141 A93548-517 4.7K 1% 0.0625W RES 0402

DESIGN NOTE:

Vin: 0.3V to 5V sine wave
Voh max: 5.5V
Voh min: 1.2V
VOL (max): 0.3V
VOL (min): -0.3V

+P5V_SMA — 450MA FB29 FB 220 0402 — +P5V

C1048 H81594-001 1UF 10% 25V X6S 0402

C1047 H81594-001 1UF 10% 25V X6S 0402

+P3V3_SMA — 450MA FB30 FB 220 0402 — +P3V3

C1070 H81594-001 1UF 10% 25V X6S 0402

C1069 H81594-001 1UF 10% 25V X6S 0402

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DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	65 OF 105

SI5518 CLOCK GENERATOR

Intel Corporation

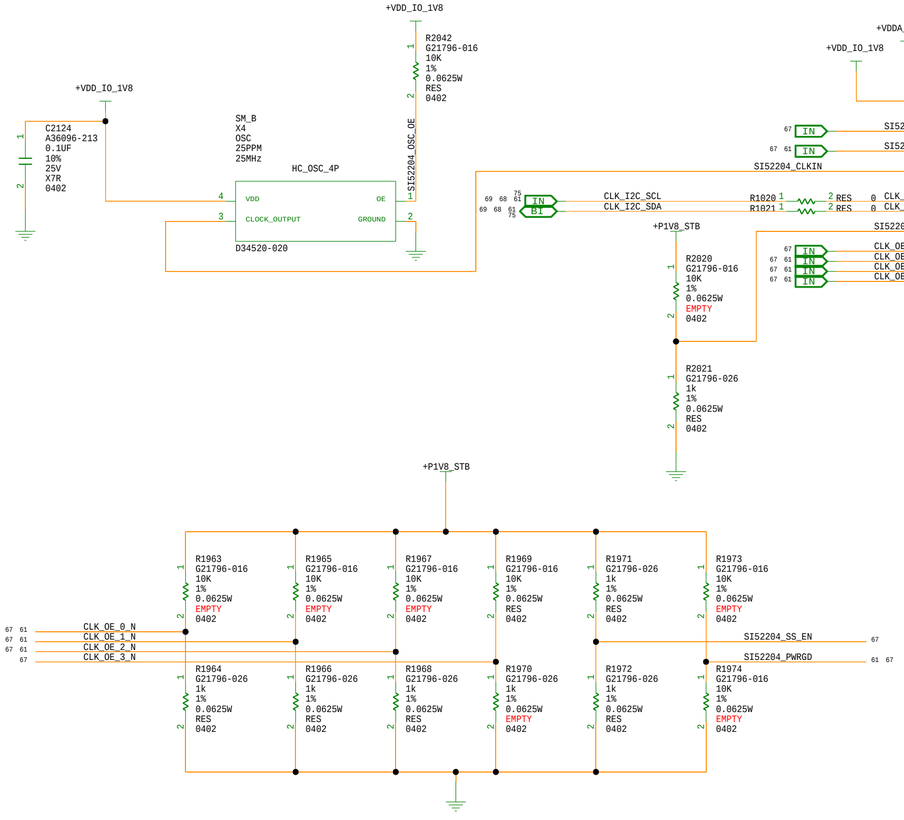
INTEL CORPORATION,BANGALORE
INDIA, 560103

DEPARTMENT	SIZE	CODE	DOCUMENT NUMBER	REV
PSG	C+	34649	150-0330690-A2	2.0
	SCALE:	DO NOT SCALE DRAWING	SHEET	66 OF 105

SI5518 CLK

Tue Sep 26 11:48:02 2023

SI52204 PCIE CLOCK GENERATOR



SI5391 CLOCK GENERATOR

+P1V8_STB
FB1 220 FB 600MA 0402
+SI5391_VDD
C177 K19409-001 4.7UF 20% 6.3V X6S 0402
C178 K19409-001 4.7UF 20% 6.3V X6S 0402
C179 D97712-022 1UF 10% 16V X6S 0402
C180 D97712-022 1UF 10% 16V X6S 0402
C181 D97712-022 1UF 10% 16V X6S 0402

+P3V3
FB3 220 600MA FB 0402
+SI5391_VDDA
C182 K19409-001 1UF 10% 16V X6S 0402
C190 D97712-022 1UF 10% 16V X6S 0402

IO_VDD_SEL = 0 => SI5391 1.8V I/O
SI5391

+SI5391_VDDO
FB2 220 FB 600MA 0402
+P1V8_STB
C183 D97712-022 1UF 10% 16V X6S 0402
C184 D97712-022 1UF 10% 16V X6S 0402
C185 D97712-022 1UF 10% 16V X6S 0402
C186 D97712-022 1UF 10% 16V X6S 0402
C187 D97712-022 1UF 10% 16V X6S 0402
C188 D97712-022 1UF 10% 16V X6S 0402
C189 K19409-001 4.7UF 20% 6.3V X6S 0402
C191 D97712-022 1UF 10% 16V X6S 0402
C192 D97712-022 1UF 10% 16V X6S 0402
C193 D97712-022 1UF 10% 16V X6S 0402
C194 D97712-022 1UF 10% 16V X6S 0402
C195 K19409-001 4.7UF 20% 6.3V X6S 0402

U18
IC
HC_SI5391

32	VDD	VDDO0	22
46	VDD	VDDO1	26
60	VDD	VDDO2	29
		VDDO3	33
13	VDDA	VDDO4	36
		VDDO5	40
		VDDO6	43
		VDDO7	49
		VDDO8	52
		VDDO9	57
18	SDA/SDIO	OUT0A	21
16	SCLK	OUT0AB	20
17	A1/SDO		
19	A0/CSB_N	OUT9	24
39	I2C_SEL	OUT9B	23
11	OEB_N	OUT1	28
3	IN_SEL0	OUT1B	27
4	IN_SEL1	OUT2	31
6	RSTB_N	OUT2B	30
48	FINC	OUT3	35
25	FDEC	OUT3B	34
5	SYNCB_N	OUT4	38
47	LOLB_N	OUT4B	37
12	INTRB_N	OUT5	42
63	IN0	OUT5B	41
64	IN0B	OUT6	45
1	IN1	OUT6B	44
2	IN1B	OUT7	51
14	IN2	OUT7B	50
15	IN2B	OUT8	54
61	FB_IN	OUT8B	53
62	FB_INB	OUT9	56
7	X1	OUT9B	55
8	XA	OUT9A	59
9	XB	OUT9AB	58
10	X2		
65	GND_PAD		

M57222-001

CLK_I2C_SDA 75 69 68 67 61 BI
CLK_I2C_SCL 75 69 68 67 61 IN
SI5391_A_A1 68
SI5391_A_A0 68
SI5391_A_I2C_SEL 68
SI5391_A_OEN 68 61 IN
SI5391_A_RSTN 68 61 IN
TP13 CLK_SI5391_FINC
TP14 CLK_SI5391_FDEC
TP209 CLK_SI5391_SYNC_N
TP210 CLK_SI5391_LOLB_N
CLK_SI5391_INTRB_N 68

TP9 TP_SI5391_IN0 R48 0 SI5391_IN0 / R1597 0 SI5391_IN0B
TP10 TP_SI5391_IN1 R49 0 SI5391_IN1 / R1599 0 SI5391_IN1B
TP11 TP_SI5391_IN2 R50 0 SI5391_IN2 / R1600 0 SI5391_IN2B
R1603 EMPTY 100 SI5391_FB_IN SI5391_FB_INB

Y2 XTAL 10PPM 48MHZ HC_XTAL_4P
K15539-001
SI5391_XA
SI5391_XB
SI5391_X1/X2

R120 RES 22 125M_F_OSC_CLK1
TP_CLK_SI5391_OUT0A_DN TP213 EMPTY SM
TP_CLK_SI5391_OUT0A_DP TP212 EMPTY SM
TP_CLK_SI5391_OUT0B TP211 EMPTY SM
C_DDR_1_REFCLK_DP C216 0.1UF 16V DDR_1_166.66M_REFCLK_DP
C_DDR_1_REFCLK_DN C217 0.1UF 16V DDR_1_166.66M_REFCLK_DN
C_DDR_2_REFCLK_DP C1462 0.1UF 16V DDR_2_166.66M_REFCLK_DP
C_DDR_2_REFCLK_DN C1465 0.1UF 16V DDR_2_166.66M_REFCLK_DN
C_DDR_3_REFCLK_DP C1463 0.1UF 16V DDR_3_166.66M_REFCLK_DP
C_DDR_3_REFCLK_DN C1466 0.1UF 16V DDR_3_166.66M_REFCLK_DN
C_DDR_4_REFCLK_DP C1464 0.1UF 16V DDR_4_166.66M_REFCLK_DP
C_DDR_4_REFCLK_DN C1467 0.1UF 16V DDR_4_166.66M_REFCLK_DN
TP_CLK_SI5391_OUT5_DP TP214 EMPTY SM
TP_CLK_SI5391_OUT5_DN TP215 EMPTY SM
C_CLK_GPIO_2C_DP C212 0.1UF 16V CLK_100M_GPIO_2C_DP
C_CLK_GPIO_2C_DN C213 0.1UF 16V CLK_100M_GPIO_2C_DN
C_CLK_GPIO_4_DP C1460 0.1UF 16V CLK_100M_GPIO_4_DP
C_CLK_GPIO_4_DN C1461 0.1UF 16V CLK_100M_GPIO_4_DN
TP_CLK_SI5391_OUT8_DP TP216 EMPTY SM
TP_CLK_SI5391_OUT8_DN TP217 EMPTY SM
TP_CLK_SI5391_OUT9_DP TP218 EMPTY SM
TP_CLK_SI5391_OUT9_DN TP219 EMPTY SM
TP_CLK_SI5391_OUT9A_DP TP220 EMPTY SM
TP_CLK_SI5391_OUT9A_DN TP221 EMPTY SM

DESIGN NOTE:
INTERNAL PU PRESENT ON IN_SEL[0:1]

DESIGN NOTE:
INPUT CAN BE SET AS IN0/IN1 THROUGH I2C CONFIGURATION (REG 0021

Si5391A-A-GM
I2C SLAVE ADDRESS: 74h

INPUT SOURCE SELECT

IN_SEL0	IN_SEL1	DESCRIPTION
0	0	IN0 (NC)
0	1	IN1 (NC)
1	0	IN2 (NC)
1	1	XA/XB (DEFAULT)

PULL-UP/DOWN RESISTORS

+P1V8_STB
R123 RES 1% 4.7K 0402 0.0625W SI5391_A_I2C_SEL 68
R992 EMPTY 1% 4.7K 0402 0.0625W SI5391_A_OEN 61 68
R993 RES 1% 4.7K 0402 0.0625W SI5391_A_RSTN 61 68
R124 RES 1K 1% 0.063W 0402 SI5391_A_A1 68
R125 RES 1K 1% 0.063W 0402 SI5391_A_A0 68
R937 0402 1K 1% 0.063W EMPTY SI5391_A_RSTN 61 68

I2C_SEL = 1B'1, I2C INTERFACE

+P1V8_STB
CLK_SI5391_INTRB_N 68 R1604 EMPTY 10K

+P1V8_STB
R1260 A93548-517 4.7K 1% 0.0625W RES 0402
R1259 A93548-517 4.7K 1% 0.0625W RES 0402
CLK_I2C_SCL 61 67 68 69 75
CLK_I2C_SDA 61 67 68 69 75

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DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	68 OF 105

SI5391

SI5395 CLOCK GENERATOR-1

INPUT SOURCE SELECT

IN_SEL0	IN_SEL1	DESCRIPTION
0	0	IN0 (SI5518 OUTPUT/DEFAULT)
0	1	IN1 (EXTERNAL INPUT)
1	0	IN2 (NC)
1	1	IN3 (LOOPBACK INPUT)

CAD NOTE:

PLACE TERMINATING RES NEAR TO CLOCK

DESIGN NOTE:

IN DESIGN TO CHANGE THE CLOCK AS PER THE INTERFACE NEED THROUGH BTS GUI,

WHICH WILL BE SHARED AS PART OF DESIGN COLLATERALS TO CUSTOMERS

SI5395A-A-GM

I2C SLAVE ADDRESS: 68h

MAX3378EETD+T

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DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	69 OF 105

SI5395 CLK-1

SI5395 CLOCK GENERATOR-2

INPUT SOURCE SELECT

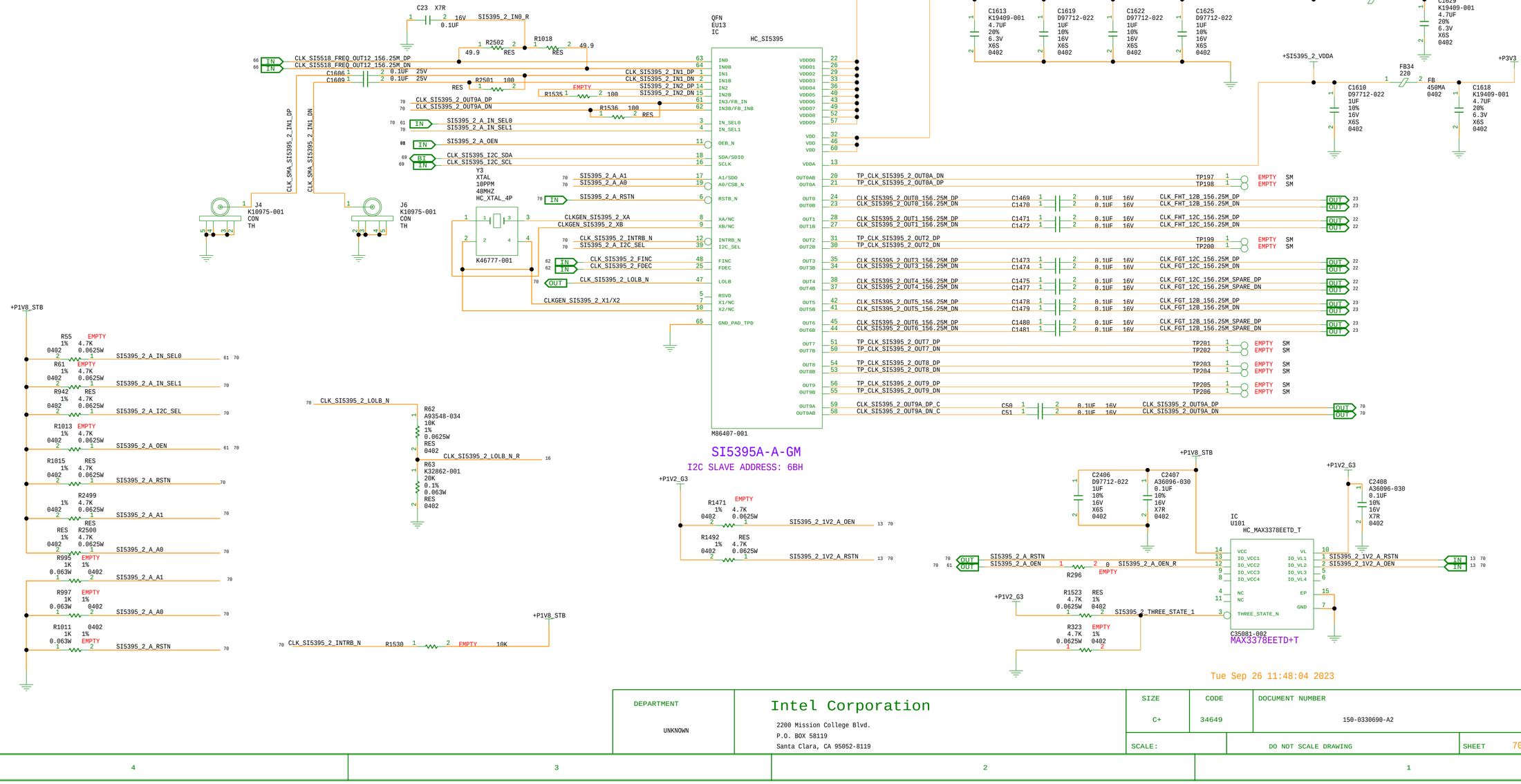
IN_SEL0	IN_SEL1	DESCRIPTION
0	0	IN0 (SI5518 OUTPUT/DEFAULT)
0	1	IN1 (EXTERNAL INPUT)
1	0	IN2 (NC)
1	1	IN3 (LOOPBACK INPUT)

DESIGN NOTE:

IN DESIGN TO CHANGE THE CLOCK AS PER THE INTERFACE NEED THROUGH BTS GUI,
WHICH WILL BE SHARED AS PART OF DESIGN COLLATERALS TO CUSTOMERS

CAD NOTE:

PLACE TERMINATING RES NEAR TO CLOCK



SI5395 CLK-2

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
UNKNOWN	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET	70 OF 105

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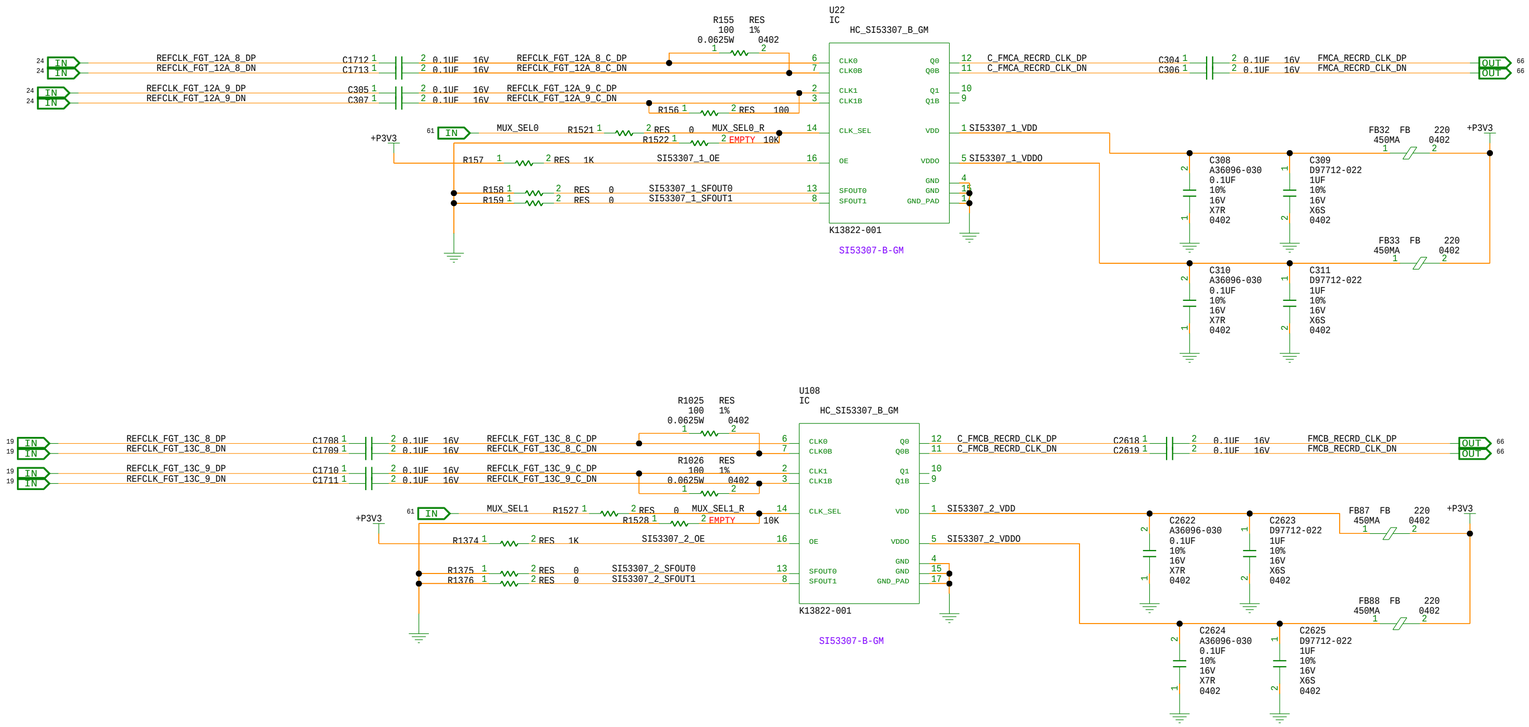
CLOCK MUX-I



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DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
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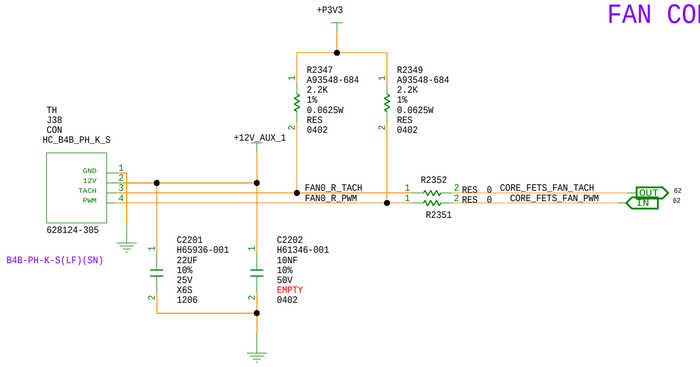
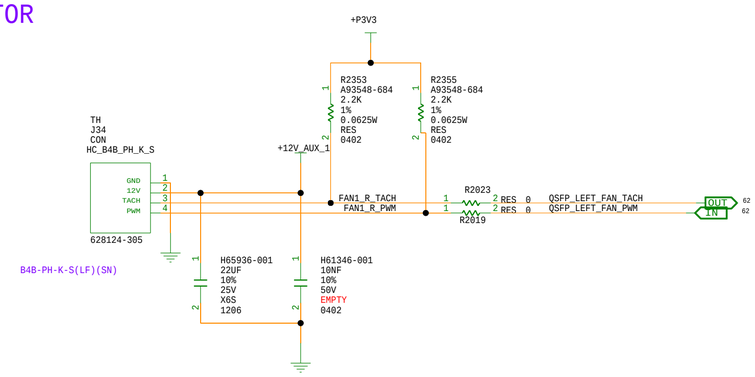
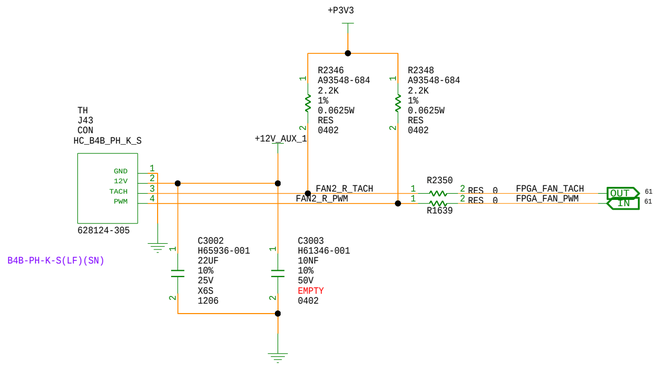
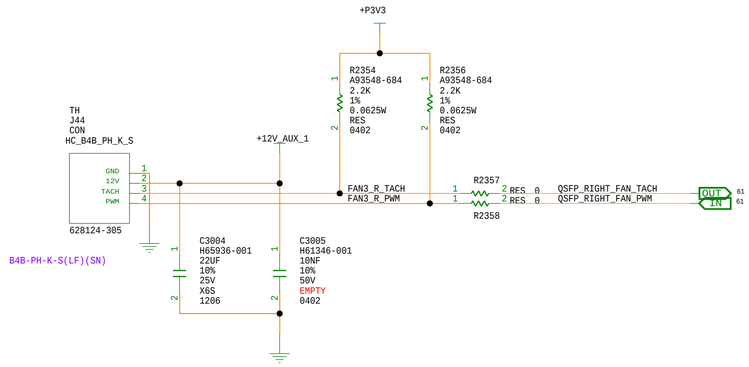
CLOCK MUX-1

FAN CONNECTOR







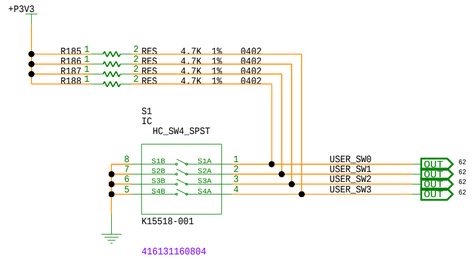


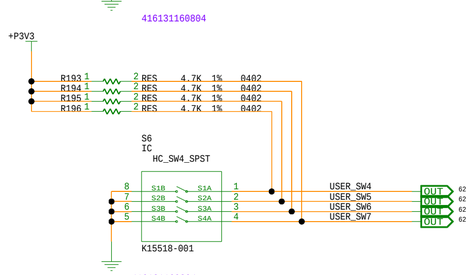
Tue Sep 26 11:48:05 2023

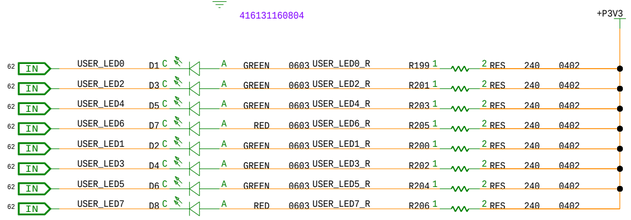
DEPARTMENT: PSG	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	SIZE: C+	CODE: 34649	DOCUMENT NUMBER: 150-0330690-A2 REV: 2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 72 OF 105

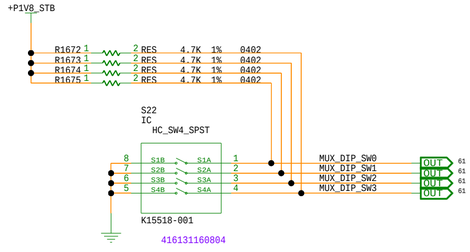
FAN CONNECTOR

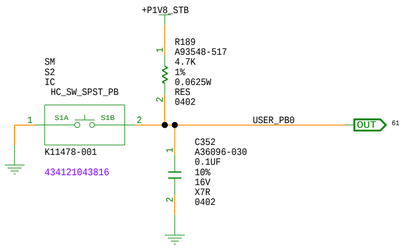
DIP SWITCH, LEDS

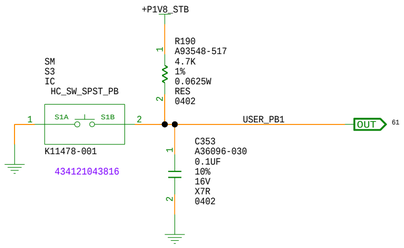












Tue Sep 26 11:48:05 2023

DIP SWITCH LEDS

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	73 OF 105

DIP SWITCH, LEDS

+P1V8_STB

R317 1 2 RES 4.7K 1% 0402
R316 1 2 RES 4.7K 1% 0402
R315 1 2 RES 4.7K 1% 0402
R314 1 2 RES 4.7K 1% 0402

S4
IC
HC_SW4_SPST
K15518-001

S1B S1A 1 PWR_SW0 OUT 60
S2B S2A 2 PWR_SW1 OUT 60
S3B S3A 3 PWR_SW2 OUT 60
S4B S4A 4 PWR_SW3 OUT 60

+P3V3

R987 1 2 RES 4.7K 1% 0402
R986 1 2 RES 4.7K 1% 0402
R985 1 2 RES 4.7K 1% 0402

S9
IC
HC_SW4_SPST
K15518-001

S1B S1A 1 FPGA_MSEL0 OUT 61 74
S2B S2A 2 FPGA_MSEL1 OUT 61 74
S3B S3A 3 FPGA_MSEL2 OUT 61 74
S4B S4A 4

DESIGN NOTE:

TO REMOTE CONTROL MSEL THROUGH MAX10, ALL S9 BITS MUST BE OFF

+P3V3

R223 1 2 RES 4.7K 1% 0402
R224 1 2 RES 4.7K 1% 0402
R225 1 2 RES 4.7K 1% 0402
R226 1 2 RES 4.7K 1% 0402

S10
IC
HC_SW4_SPST
K15518-001

S1B S1A 1 SYS_SW0 OUT 61
S2B S2A 2 SYS_SW1 OUT 61
S3B S3A 3 SYS_SW2 OUT 61
S4B S4A 4 SYS_SW3 OUT 61

+P3V3

R231 1 2 RES 4.7K 1% 0402
R232 1 2 RES 4.7K 1% 0402
R233 1 2 RES 4.7K 1% 0402
R234 1 2 RES 4.7K 1% 0402

S15
IC
HC_SW4_SPST
K15518-001

S1B S1A 1 SYS_SW4 OUT 61
S2B S2A 2 SYS_SW5 OUT 61
S3B S3A 3 SYS_SW6 OUT 61
S4B S4A 4 SYS_SW7 OUT 61

+P3V3

IN SYS_LED0 D9 C A GREEN 0603 SYS_LED0_R R237 1 2 RES 240 0402
IN SYS_LED2 D11 C A GREEN 0603 SYS_LED2_R R239 1 2 RES 240 0402
IN SYS_LED4 D13 C A GREEN 0603 SYS_LED4_R R241 1 2 RES 240 0402
IN SYS_LED6 D15 C A RED 0603 SYS_LED6_R R243 1 2 RES 240 0402
IN SYS_LED1 D10 C A GREEN 0603 SYS_LED1_R R238 1 2 RES 240 0402
IN SYS_LED3 D12 C A GREEN 0603 SYS_LED3_R R240 1 2 RES 240 0402
IN SYS_LED5 D14 C A GREEN 0603 SYS_LED5_R R242 1 2 RES 240 0402
IN SYS_LED7 D16 C A RED 0603 SYS_LED7_R R244 1 2 RES 240 0402

+P1V8_G3

R210
A93548-596
100K
1%
0.0625W
RES
0402

F_SDM_IO5 OUT 12 61

R217
A93548-517
4.7K
1%
0.0625W
RES
0402

F_SDM_IO5_R

R207 RES 10K 1% 0.0625W 0402
FPGA_MSEL0 1 2 FPGA_MSEL0_R

Q4
K21465-001
FDV305N
FET
SOT23

+P1V8_G3

R211
A93548-596
100K
1%
0.0625W
RES
0402

F_SDM_IO7 OUT 12 61

R218
A93548-517
4.7K
1%
0.0625W
RES
0402

F_SDM_IO7_R

R208 RES 10K 1% 0.0625W 0402
FPGA_MSEL1 1 2 FPGA_MSEL1_R

Q5
K21465-001
FDV305N
FET
SOT23

+P1V8_G3

R212
A93548-596
100K
1%
0.0625W
RES
0402

F_SDM_IO9 OUT 12 61

R219
A93548-517
4.7K
1%
0.0625W
RES
0402

F_SDM_IO9_R

R209 RES 10K 1% 0.0625W 0402
FPGA_MSEL2 1 2 FPGA_MSEL2_R

Q6
K21465-001
FDV305N
FET
SOT23

+P3V3

SM
S11
IC
HC_SW_SPST_PB
K11478-001

R227
A93548-517
4.7K
1%
0.0625W
RES
0402

SYS_PB0 OUT 61

C358
A36096-030
0.1UF
10%
16V
X7R
0402

+P3V3

SM
S13
IC
HC_SW_SPST_PB
K11478-001

R229
A93548-517
4.7K
1%
0.0625W
RES
0402

PWR_PB0 OUT 59

C360
A36096-030
0.1UF
10%
16V
X7R
0402

+P3V3

SM
S16
IC
HC_SW_SPST_PB
K11478-001

R235
A93548-517
4.7K
1%
0.0625W
RES
0402

SYS_PB3 OUT 61

C362
A36096-030
0.1UF
10%
16V
X7R
0402

+P3V3

SM
S12
IC
HC_SW_SPST_PB
K11478-001

R228
A93548-517
4.7K
1%
0.0625W
RES
0402

SYS_PB1 OUT 61

C359
A36096-030
0.1UF
10%
16V
X7R
0402

+P3V3

SM
S14
IC
HC_SW_SPST_PB
K11478-001

R230
A93548-517
4.7K
1%
0.0625W
RES
0402

SYS_PB2 OUT 61

C361
A36096-030
0.1UF
10%
16V
X7R
0402

+P3V3

SM
S17
IC
HC_SW_SPST_PB
K11478-001

R236
A93548-517
4.7K
1%
0.0625W
RES
0402

SYS_PB4 OUT 61

C363
A36096-030
0.1UF
10%
16V
X7R
0402

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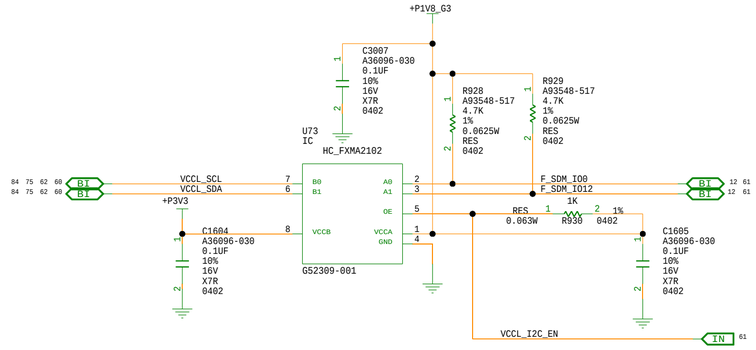
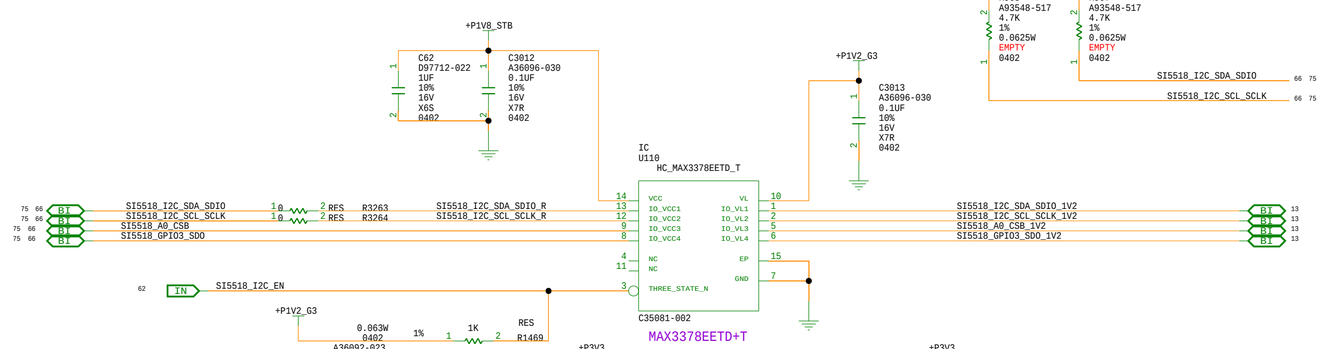
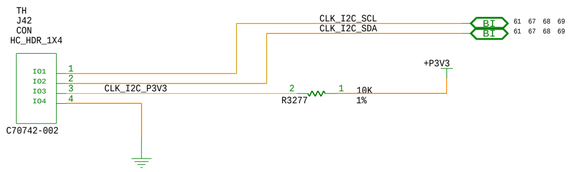
DIP SWITCH LEDS

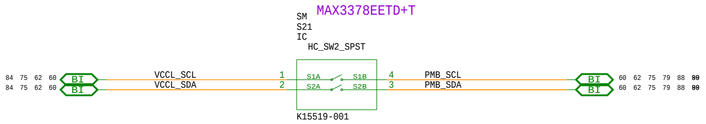
DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	74 OF 105

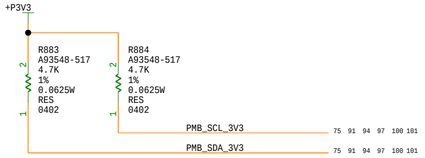
LVL SHIFTER-2

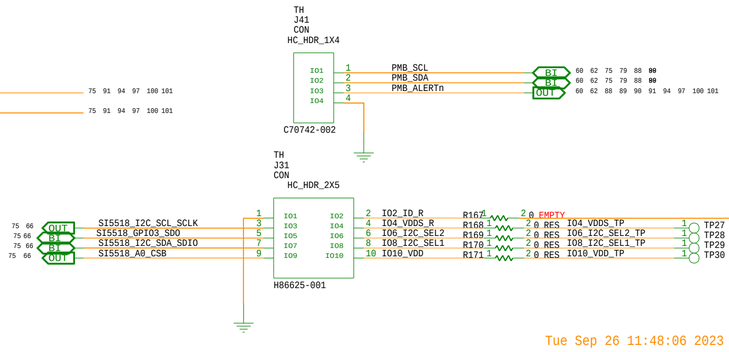












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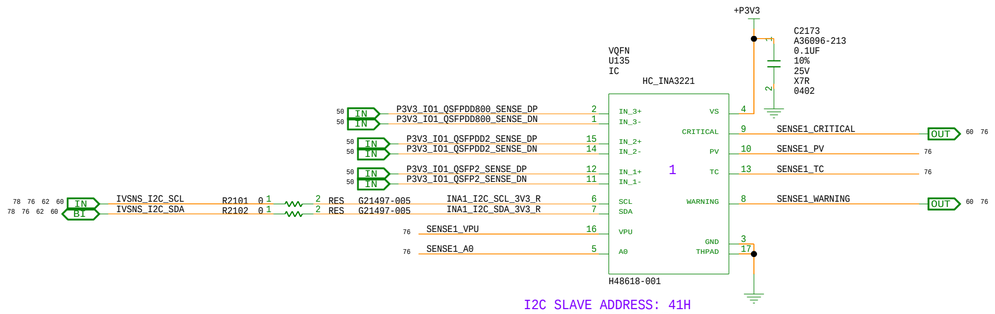
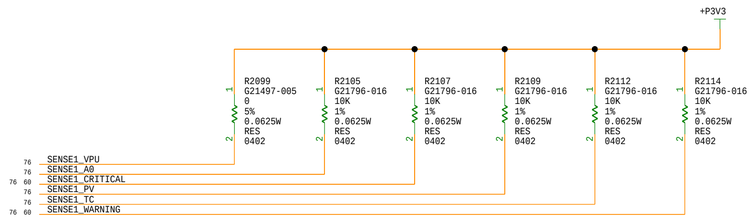
LEVEL SHIFTER 2

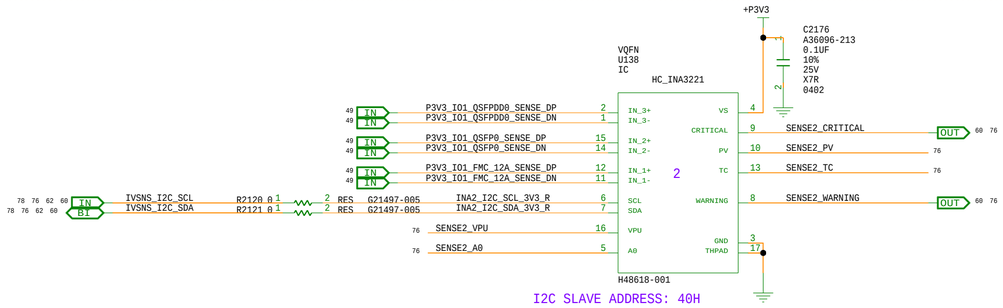
DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation INTEL CORPORATION,BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET	75 OF 105

INA3221

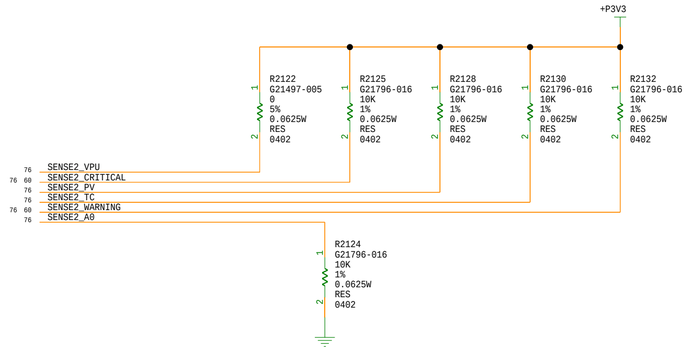


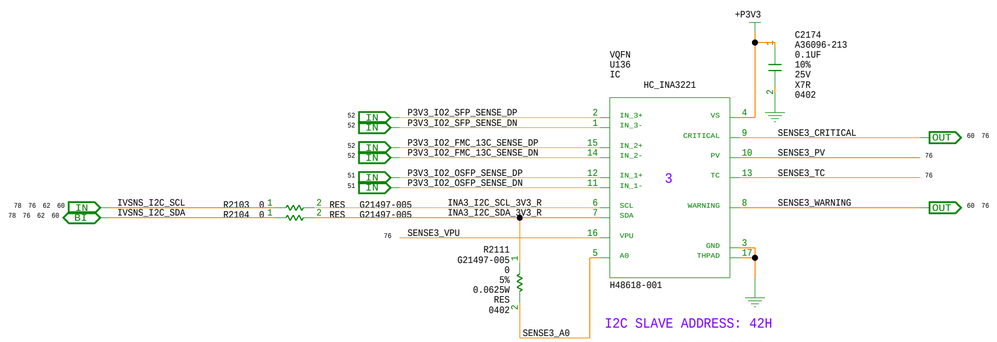
I2C SLAVE ADDRESS: 41H
MPN: INA3221AIRGVR



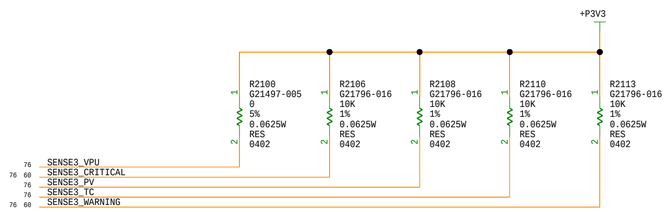


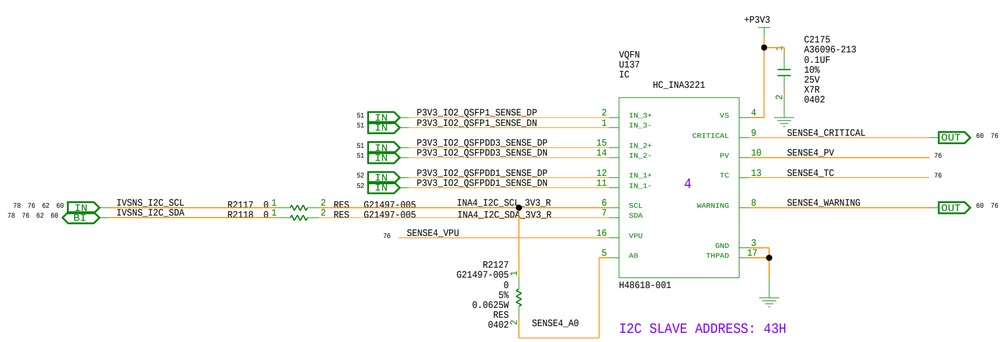
I2C SLAVE ADDRESS: 40H
MPN: INA3221AIRGVR



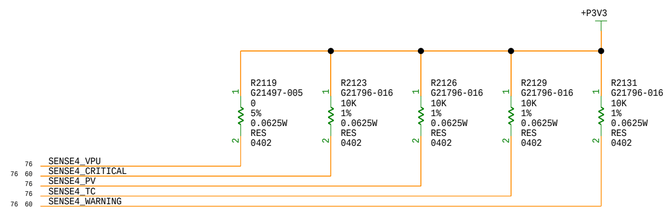


I2C SLAVE ADDRESS: 42H
MPN: INA3221AIRGVR





I2C SLAVE ADDRESS: 43H
MPN: INA3221AIRGVR



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CURRENT SENSE - INA3221

DEPARTMENT: PSG	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	SIZE: C+	CODE: 34649	DOCUMENT NUMBER: 150-0330690-A2 — REV: 2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET: 76 OF 105

BOARD TEMP SENSORS

Temp Sensor	Fan Connector	Device	Tach Sig	PWM Sig
Q26/EU27.CH1	J38	Core_FETS	CORE_FETS_FAN_TACH	CORE_FETS_FAN_PWM
EU3/EU4/EU11	J43	FPGA	FPGA_FAN_TACH	FPGA_FAN_PWM
Q27/EU27.CH2	J34	QSFP_LEFT	QSFP_LEFT_FAN_TACH	QSFP_LEFT_FAN_PWM
Q25/EU27.CH3	J44	QSFP_RIGHT	QSFP_RIGHT_FAN_TACH	QSFP_RIGHT_FAN_PWM

CAD NOTE:
PLACE THIS SENSOR IC ON BOTTOM SIDE
AT BOARD SOUTH-WEST QUADRANT.

EU3 IC HC_MAX31730 — K87190-001
I2C SLAVE ADDRESS: 1CH
MPN:MAX31730ATC+

CAD NOTE:
PLACE THIS SENSOR IC ON TOP SIDE
AT BOARD SOUTH-EAST QUADRANT.

EU4 IC HC_MAX31730 — K87190-001
I2C SLAVE ADDRESS: 1DH
MPN :MAX31730ATC+

CAD NOTE:
PLACE THIS SENSOR IC ON TOP SIDE
AT BOARD NORTH-WEST QUADRANT.

EU11 IC HC_MAX31730 — K87190-001
I2C SLAVE ADDRESS: 1EH
MPN :MAX31730ATC+

CAD NOTE:
PLACE THIS SENSOR IC ON TOP SIDE
AT BOARD NORTH QUADRANT.

EU27 IC HC_MAX31730 — K87190-001
I2C SLAVE ADDRESS: 4CH
MPN :MAX31730ATC+

CAD NOTE:
PLACE BOTH OVERTEMP LEDS
SIDE-BY-SIDE.

CAD NOTE:
PLACE THIS DIODE ON TOP SIDE
AT BOARD NORTH QUADRANT.

CAD NOTE:
PLACE THIS DIODE ON TOP SIDE
AT BOARD SOUTH WEST QUADRANT.

CAD NOTE:
PLACE THIS DIODE ON TOP SIDE
AT BOARD NORTH EAST QUADRANT.

U114 IC HC_24AA64 — K41311-001
24AA64-I/MS
I2C ADDR = 50h

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DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	77 OF 105

BOARD TEMP SENSORS

CURRENT/VOLTAGE MONITOR

DESIGN NOTE:
ADDED THESE RESISTOR AS PLACEHOLDER.
FOR 1.25V VREF PLEASE UNMOUNT BOTTOM RES AND REPLACE TOP RES WITH 0OHM

+P1V8_STB
R644 K15783-001 240 1% 0.1W RES 0402
C2615 D97712-022 1UF 10% 16V X6S 0402
SOT23 U67 IC HC_ADR1581
M79415-001
C1476 H61346-001 10NF 10% 50V X7R 0402
LTC2497_1_REF
R1326 A36092-023 1K 1% 0.063W RES 0402
VREF = 0.625V
R478 A36092-023 1K 1% 0.063W RES 0402
C1108 A36096-003 470PF 10% 50V X7R 0402
LTC2497_1_REF_R
U65 IC HC_LTC2497
LTC2497_1_ADCIN_DN
LTC2497_1_ADCIN_DP
IVSNS_I2C_SDA
IVSNS_I2C_SCL
+P3V3
FB64 220 450MA FB 0402
C1109 K19409-001 4.7UF 20% 6.3V X6S 0402
C1110 K19409-001 4.7UF 20% 6.3V X6S 0402
C1111 A36096-030 0.1UF 10% 16V X7R 0402
LTC2497_1_VCC
K13870-001
LTC2497CUHF#PBF
I2C SLAVE ADDRESS: 14h
LTC2497_1_COM
LTC2497_1_REF
R3245 A36092-023 1K 1% 0.063W EMPTY 0402
R3246 RES 1K 1% 0402
A36092-023 0.063W
LTC2497_1_CH14
LTC2497_1_CH15
R3142 C48657-027 0 1% 0.05W EMPTY 0201
R3143 C48657-027 0 1% 0.05W EMPTY 0201
C2562 A36096-030 0.1UF 10% 16V X7R 0402
C2563 A36096-030 0.1UF 10% 16V X7R 0402
C2636 A36096-030 0.1UF 10% 16V X7R 0402
C2637 A36096-030 0.1UF 10% 16V X7R 0402
C2638 A36096-030 0.1UF 10% 16V X7R 0402
C2639 A36096-030 0.1UF 10% 16V X7R 0402
C2640 A36096-030 0.1UF 10% 16V X7R 0402
C2641 A36096-030 0.1UF 10% 16V X7R 0402
C2642 A36096-030 0.1UF 10% 16V X7R 0402
C2643 A36096-030 0.1UF 10% 16V X7R 0402
C2644 A36096-030 0.1UF 10% 16V X7R 0402
C2645 A36096-030 0.1UF 10% 16V X7R 0402
C2646 A36096-030 0.1UF 10% 16V X7R 0402
C2647 A36096-030 0.1UF 10% 16V X7R 0402
LTC2497_1_CH10
LTC2497_1_CH11
LTC2497_1_CH12
LTC2497_1_CH13
P1V8_G3_SENSE_R_DP
P1V8_G3_SENSE_R_DN
VCCERT2_1V0_SENSE_R_DP
VCCERT2_1V0_SENSE_R_DN
VCCEHT_1V5_U2x_SENSE_R_DP
VCCEHT_1V5_U2x_SENSE_R_DN
VCCEHT_1V5_U1x_SENSE_R_DP
VCCEHT_1V5_U1x_SENSE_R_DN
VCCFUSECORE_GXF_1V0_G2_SENSE_R_DP
VCCFUSECORE_GXF_1V0_G2_SENSE_R_DN
R3144 R3145 R3390 R3391 R3392 R3393 R3394 R3395 R2317 R2318 RES 100
P1V8_G3_SENSE_DP
P1V8_G3_SENSE_DN
VCCERT2_1V0_SENSE_DP
VCCERT2_1V0_SENSE_DN
VCCEHT_1V5_U2x_SENSE_DP
VCCEHT_1V5_U2x_SENSE_DN
VCCEHT_1V5_U1x_SENSE_DP
VCCEHT_1V5_U1x_SENSE_DN
VCCFUSECORE_GXF_1V0_G2_SENSE_DP
VCCFUSECORE_GXF_1V0_G2_SENSE_DN

+P3V3
R479 A93548-517 4.7K 1% 0.0625W RES 0402
R480 A93548-517 4.7K 1% 0.0625W RES 0402
IVSNS_I2C_SDA
IVSNS_I2C_SCL
C1937 A36096-003 470PF 10% 50V X7R 0402
U99 IC HC_LTC2497
+VCCERT1_FHT_GXF_1V0_UX_G1
+VCCERT2_FHT_GXF_1V0_UX_G1
+VCCEHT_FHT_GXF_1V5_U2X_G2
+VCCEHT_FHT_GXF_1V5_U1X_G2
LTC2497_2_ADCIN_DN
LTC2497_2_ADCIN_DP
P2V5_G2_VSNS
P3V3_VSNS
P1V2_IO
P1V8_G3_VSNS
+VCCEFUSECORE_GXF_1V0_G2
P5V_VSNS
P1V8_STB_VSNS
P12V0_FMC_A_VSNS
P12V0_FMC_B_VSNS
C1939 K19409-001 4.7UF 20% 6.3V X6S 0402
C1940 K19409-001 4.7UF 20% 6.3V X6S 0402
C1941 A36096-030 0.1UF 10% 16V X7R 0402
LTC2497_2_VCC
K13870-001
LTC2497CUHF#PBF
I2C SLAVE ADDRESS: 16h
LTC2497_2_COM
R3141 C48657-027 0 1% 0.05W EMPTY 0201
R3146 C48657-027 0 1% 0.05W EMPTY 0201
R3147 C48657-027 0 1% 0.05W EMPTY 0201
R3243 A36092-023 1K 1% 0.063W EMPTY 0402
R3244 RES 1K 1% 0402
A36092-023 0.063W
R1756 RES 1K 1% 0.063W 0402
R1757 RES 1K 1% 0.063W 0402
R2187 RES 1K 1% 0.063W 0402
R2188 RES 1K 1% 0.063W 0402
R1760 RES 10K 1% 0.0625W 0402
R1761 RES 4.99K 1% 0.0625W 0402
R13 RES 1K 1% 0.063W 0402
R15 RES 1K 1% 0.063W 0402
R16 RES 1K 1% 0.063W 0402
R17 RES 1K 1% 0.063W 0402
TH J149 CON HC_HDR_1X4
C70742-002
R3281 10K 1%
R3298 A93548-400 5.76K 1% RES 0.0625W 0402
R3299 RES 1K 1% 0.063W 0402
R3300 A93548-400 5.76K 1% RES 0.0625W 0402
R3301 RES 1K 1% 0.063W 0402

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DEPARTMENT: PSG	Intel Corporation INTEL CORPORATION,BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SIZE: C+	CODE: 34649	DOCUMENT NUMBER: 150-0330690-A2 REV: 2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET: 78 OF 105

CURRENT/VOLATGE MONITOR

POWER In- 12V_AUX1 Hotswap

TH
J47
EMPTY
HC_01_0004_26

+12V_DCIN_1

M44881-001

150W 2x4 ATX AUX
INPUT POWER
CONNECTOR

DESIGN NOTE:

When 16V, EN = 1.96V
When 15V, EN = 1.84V
When 14V, EN = 1.72V
When 13V, EN = 1.59V
When 12V, EN = 1.47V
When 11V, EN = 1.35V
When 10V, EN = 1.23V

12V DCIN
2X3 ATX

SM
J30
SCON
HC_01_0004_36

+12V_DCIN_1

K12408-001

01-0004-36

DESIGN NOTE:

Power input support is 300W

CAD NOTE:

Place close to
MAX16545B VIN

+12V_DCIN_1

VR2
J31279-001
5.0SMDJ12A
252A
DIO
SM

C2362 560uF 16V ALUM SM
C2363 H65936-001 22UF 10% 25V X6S 1206
C2364 H65936-001 22UF 10% 25V X6S 1206
C2365 H65936-001 22UF 10% 25V X6S 1206
C2366 H65936-001 22UF 10% 25V X6S 1206

+AUX1_VDD_1V8

R2616 A93548-034 10K 1% 0.0625W RES 0402

TP7 EMPTY TH

TP387 EMPTY TH

+12V_DCIN_1

C2367 A36096-213 0.1uF 10% 25V X7R 0402
R2617 A93548-129 41.2K 1% 0.0625W EMPTY 0402
C2368 A36096-045 10nF 10% 25V X7R 0402
R2618 A93548-400 5.76K 1% 0.0625W RES 0402
C2372 H81594-001 1uF 10% 25V X6S 0402
C2373 A36096-213 0.1uF 10% 25V X7R 0402

+AUX1_VDD_1V8

QFN
IC
EU30 HC_MAX16545B

22	VDD	PWRGD	17
9	VIN	VOUT	5
10	VIN	VOUT	6
11	VIN	VOUT	7
12	VIN	VOUT	8
14	EN/UVLO		
16	FAULT_N	ILOAD_IN	21
1	SMBUS_CLK	VBST	4
19	SMBUS_DATA		
15	SMBUS_ALERT_N		
20	SMBUS_ID	ILOAD	2
18	ROCP		
3	SS	GND	13

K21748-001

AUX1_HSC_EN
AUX1_HSC_FAULT_R_N
I2C_AUX1_R_SCL
I2C_AUX1_R_SDA
AUX1_HSC_ALERT_N
AUX1_HSC_SMB_ID_R
AUX1_HSC_ROCP
AUX1_HSC_SS

R2604 23.2k RES
R2605 210K RES A93548-399
C2369 0.1uF 25V A36096-213 10% X7R 0402
C2374 K28300-001 15nF 10% 25V X7R 0402

MAX16545BGPF+T

I2C SLAVE ADDRESS: 11H

p: 30A, 360W

+P3V3

R2622 A93548-034 10K 1% 0.0625W RES 0402

AUX1_HSC_POK

TP384 EMPTY TH

C2376 K13747-001 0.22UF 10% 16V X7R 0402

R2624 A93548-034 10K 1% 0.0625W RES 0402

AUX1_HSC_NC
AUX1_HSC_BST

C2375 A36096-045 10nF 10% 25V X7R 0402
R2627 A93548-195 8.25K 1% 0.1W RES 0402

AUX1_HSC_ILOAD

I_LOAD:48.863A

TH
J154
EMPTY
HC_HDR_1X4

C70742-002

I2C_AUX_SCL
I2C_AUX_SDA
I2C_AUX_P3V3

BI BI

R3279 0 RES 0402

+P3V3

+12V_AUX_1

TP385 EMPTY TH

C2377 A36096-213 0.1uF 10% 25V X7R 0402

CR1 M92377-001 30A DIO

LCC

+12V_AUX_1

C2379 560uF 16V ALUM SM
C2380 560uF 16V ALUM SM

FET_PARAMETER	VALUE
VGS	±20 V
ID	300 A

+12V_AUX_1

Q66
K21466-001
PSMN1R0-30YLD
FET
SM

Q67
K21466-001
PSMN1R0-30YLD
FET
SM

+12V_AUX_2

TP388 EMPTY TH

AUX1_GATE2_R
R20 A93548-031 10 1% 0.0625W RES 0402
AUX1_GATE1_R
R21 A93548-031 10 1% 0.0625W RES 0402

R2628 10K 1% 0.0625W RES 0402 A93548-034

AUX1_HSC_R_GATE

R2626 A93548-596 100K 1% 0.0625W EMPTY 0402

C2378 A36096-045 10nF 10% 25V X7R 0402

AUX1_HSC_SOURCE

DFN
EU31
IC
HC_LTC4359

4	IN	OUT	1
3	SOURCE	GATE	2 AUX1_HSC_GATE
5	SHDN_N	VSS	6 AUX1_HSC_VSS
	EXPOSED_PAD_TPD		7

J69312-001

LTC4359HDCB#TRPBF

AUX1_HSC_SHDN_N

C2 K19472-001 1.5UF 10% 50V X6S 1206

R2629 A36092-023 1K 1% 0.063W RES 0402

Switch Position S7	+12V_DCIN_1	+12V_DCIN_2	+12V_AUX_1	+12V_AUX_2_FET	EU35	EU31	+12V_AUX_1 Shorts with +12V_AUX_2	+12V_AUX_2_FET Shorts with +12V_AUX_2	Power Up Case
2-1 (ON) & 5-4 (ON)	Present	Present	ON	ON	ON	OFF	No	Yes	High Power Case
2-1 (ON) & 5-4 (ON)	Present	Not Present	ON	OFF	OFF	ON	Yes	No	Low Power Case
2-3 & 5-6 (OFF)	Present	Present	OFF	OFF	OFF	OFF	No	No	OFF Case

BI PMB_SDA R319 RES 0
BI PMB_SCL R320 RES 0

IN I2C_AUX_SCL
BI I2C_AUX_SDA

R2606 RES 0 I2C_AUX1_R_SCL
R2607 RES 0 I2C_AUX1_R_SDA

+P3V3

R2612 A93548-034 10K 1% 0.0625W EMPTY 0402
R2613 A93548-034 10K 1% 0.0625W EMPTY 0402
R2614 A93548-034 10K 1% 0.0625W RES 0402

I2C_AUX_SCL
I2C_AUX_SDA
AUX1_HSC_ALERT_N

+12V_DCIN_1

R2619 A93548-129 41.2K 1% 0.0625W RES 0402

TH
S7
IC
K15516-001

SW_AUX1
SW_AUX2
SW_FET

AUX1_HSC_EN

+12V_DCIN_2

R2620 A93550-165 60.4k 1% 0.1W RES 0603

R2623 K32862-001 20K 0.1% 0.063W EMPTY 0402

R2621 0 5% 0.0625W RES A93549-001 0402

R2625 A93550-165 60.4K 1% 0.1W RES 0603

Q68 K21465-001 FDV305N FET SOT23

AUX2_HSC_EN

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UNKNOWN	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET	79 OF 105

POWER INPUT-1

POWER In- 12V_AUX2 Hotswap

TH
J51
EMPTY
HC_01_0004_26
+12V_DCIN_2
GND SENSE0 GND GND
12V 12V 12V 12V
M44881-001

150W 2x4 ATX AUX
INPUT POWER
CONNECTOR

DESIGN NOTE:
When 16V, EN = 1.96V
When 15V, EN = 1.84V
When 14V, EN = 1.72V
When 13V, EN = 1.59V
When 12V, EN = 1.47V
When 11V, EN = 1.35V
When 10V, EN = 1.23V

CAD NOTE:
Place close to
MAX16545B VIN

+12V_DCIN_2
+AUX2_VDD_1V8
C2387 A36096-213 0.1uF 10% 25V X7R 0402
C2388 A36096-045 10nF 10% 25V X7R 0402
C2390 H81594-001 1uF 10% 25V X6S 0402
C2391 A36096-213 0.1uF 10% 25V X7R 0402
R2633 A93548-129 41.2K 1% 0.0625W RES 0402
R2634 A93548-400 5.76K 1% 0.0625W RES 0402
R2632 A93548-034 10K 1% 0.0625W RES 0402
TP389 EMPTY TH
AUX2_EN

QFN
EU32
IC HC_MAX16545B
K21748-001

VDD PWRGD
VIN VOUT
VIN VOUT
VIN VOUT
VIN VOUT
EN/UVLO
FAULT_N ILOAD_IN
SMBUS_CLK VBST
SMBUS_DATA
SMBUS_ALERT_N
SMBUS_ID ILOAD
ROCP
SS GND

EMPTY TP8 TH
IN I2C_AUX_SCL R2610 RES 0 I2C_AUX2_R_SCL
BI I2C_AUX_SDA R2611 RES 0 I2C_AUX2_R_SDA
OUT
AUX2_HSC_FAULT_R_N
AUX2_HSC_ALERT_N
R2608 0402 30.9K RES A93548-382 AUX2_HSC_SMB_ID_R
R2609 0402 210K RES A93548-399 AUX2_HSC_ROCP
+P3V3 R2631 10K 0.0625W 1% RES 0402 A93548-034
AUX2_HSC_SS
C2398 K28300-001 15nF 10% 25V X7R 0402
+12V_AUX_2_FET
C2389 0.1uF 10% 25V 0402 A36096-213 X7R

+P3V3
R2635 A93548-034 10K 1% 0.0625W RES 0402
AUX2_HSC_POK
TP390 EMPTY TH
AUX2_HSC_NC
AUX2_HSC_BST
AUX2_HSC_ILOAD
C2399 A36096-045 10nF 10% 25V X7R 0402
R2637 A93548-195 8.25K 1% 0.1W RES 0402
R2636 10K 0.0625W A93548-034 1% RES 0402
C2400 K13747-001 0.22UF 10% 16V X7R 0402
C2401 A36096-213 0.1uF 10% 25V X7R 0402

I_LOAD:21.095A

+12V_AUX_2_FET
TP391 EMPTY TH
CR2 M92377-001 30A DIO LCC
C2402 560uF 16V ALUM SM
C2403 560uF 16V ALUM SM

+12V_DCIN_2
VR3 J31279-001 5.0SMDJ12A 252A DIO SM
C2382 560uF 16V ALUM SM
C2383 H65936-001 22UF 10% 25V X6S 1206
C2384 H65936-001 22UF 10% 25V X6S 1206
C2385 H65936-001 22UF 10% 25V X6S 1206
C2386 H65936-001 22UF 10% 25V X6S 1206

p: 30A, 360W

MAX16545BGPF+T
I2C SLAVE ADDRESS: 12H

FET_PARAMETER	VALUE
VGS	+/- 20V
ID	60 A

+12V_AUX_2_FET
Q69 K21466-001 PSMN1R0-30YLD FET SM
Q70 K21466-001 PSMN1R0-30YLD FET SM
+12V_AUX_2
AUX2_GATE2_R
AUX2_GATE1_R
R22 A93548-031 10 1% 0.0625W RES 0402
R23 A93548-031 10 1% 0.0625W RES 0402
R2638 10K 0.0625W 1% RES 0402 A93548-034
R2743 A93548-596 100K 1% 0.0625W EMPTY 0402
C2405 A36096-045 10nF 10% 25V X7R 0402
AUX2_HSC_R_GATE
AUX2_HSC_SOURCE
DFN
EU35
IC HC_LTC4359
IN OUT
SOURCE GATE
SHDN_N VSS
EXPOSED_PAD_TPD
J69312-001
AUX2_HSC_GATE
AUX2_HSC_VSS
C6 1.5UF 50V 10% X6S 1206 K19472-001
R2639 A36092-023 1K 1% 0.063W RES 0402
IN AUX2_HSC_EN

LTC4359HDCB#TRPBF

12V DCIN
2X3 ATX
SM
J55
SCON
HC_01_0004_36
+12V_DCIN_2
GND0 GND1 GND2
12V0 12V1 12V2
K12408-001
01-0004-36

DESIGN NOTE:
Power input support is 300W

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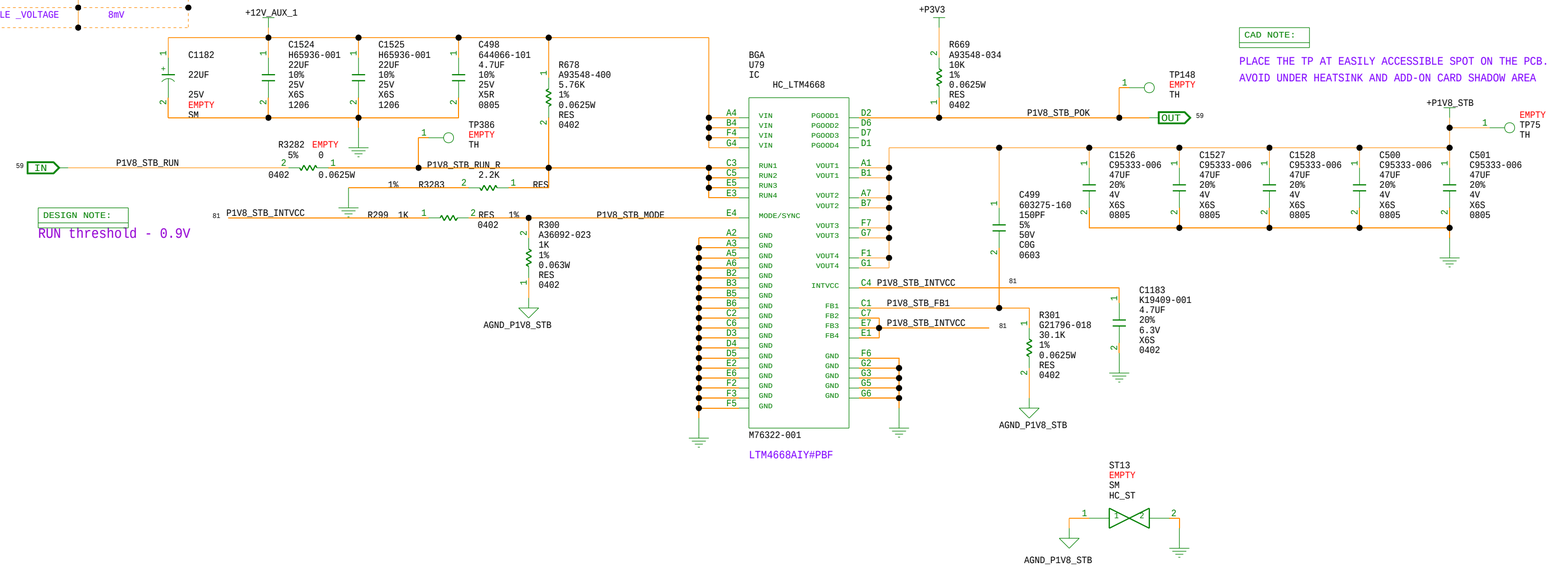
UNKNOWN	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET	80 OF 105

POWER INPUT-2

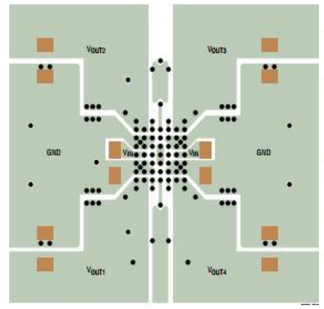
P1V8_STB

PARAMETER	VALUE
VOUT	1.8V
MAX CURRENT	4.8A
LOAD CURRENT	2.822A
FREQUENCY	
RIPPLE _VOLTAGE	8mV

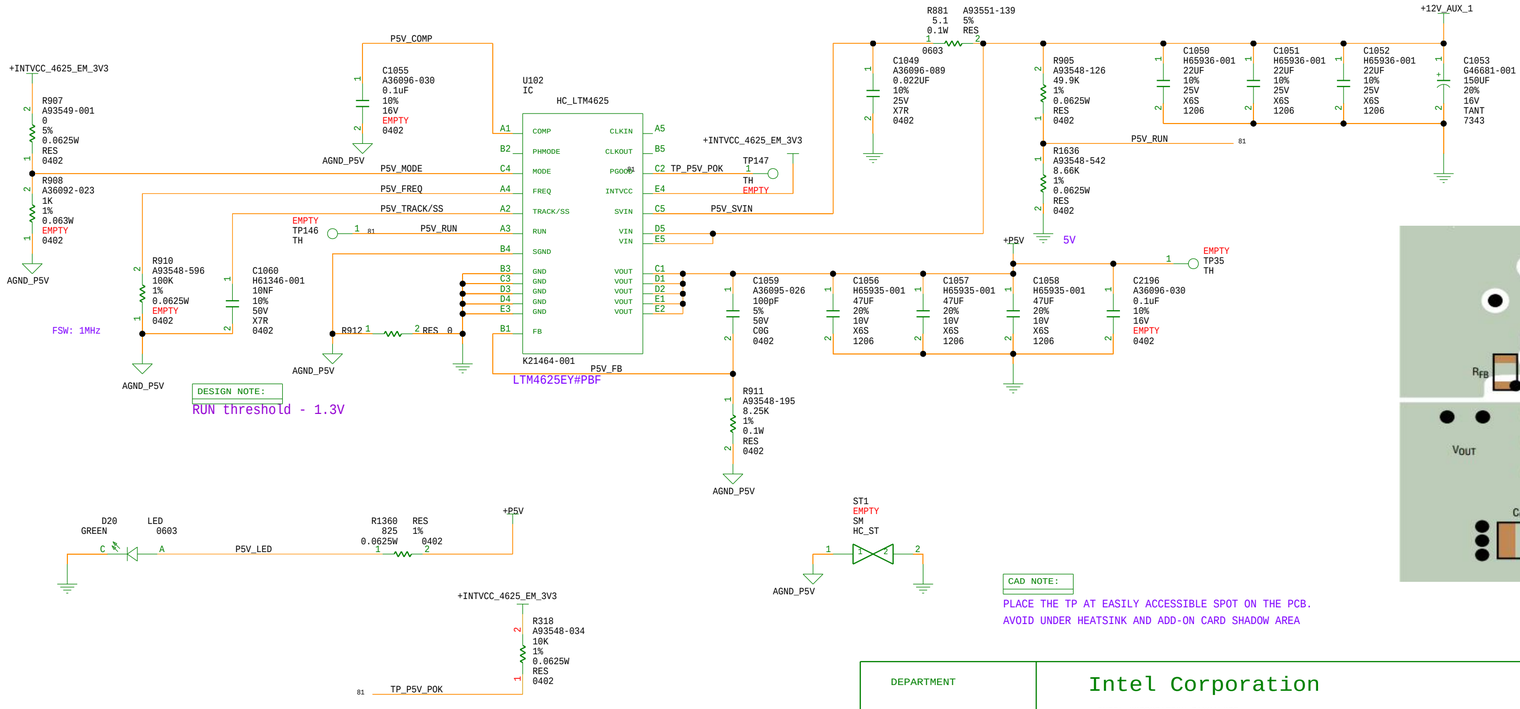


RECOMMENDED LAYOUT GUIDELINES

- Use large PCB copper areas for high current paths, including V_{IN}, GND, V_{OUT1} and V_{OUT2}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- For parallel modules, tie the V_{OUT}, V_{FB} and COMP pins together. Use an internal layer to closely connect these pins together. The TRACK pin can be tied a common capacitor for regulator soft-start.
- Bring out test points on the signal pins for monitoring.



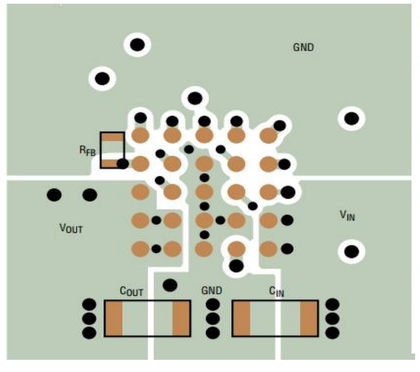
PV5



PARAMETER	VALUE
VOUT	5V
MAX CURRENT	5A
LOAD CURRENT	0.05A
FREQUENCY	1MHz
RIPPLE _VOLTAGE	5mV

RECOMMENDED LAYOUT GUIDELINES

- Use large PCB copper areas for high current paths, including V_{IN}, GND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- Bring out test points on the signal pins for monitoring.
- Keep separation between CLKIN, CLKOUT and FREQ pin traces to minimize possibility of noise due to crosstalk between these signals.



CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

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PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	81 OF 105

P3V3

PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	15A
LOAD CURRENT	6.189A
FREQUENCY	1.5MHz
RIPPLE _VOLTAGE	

+12V_AUX_1

DESIGN NOTE: 100UF TO BE REPLACED TO CERAMIC IF NECESSARY

C1393 H65936-001 22UF 10% 25V X6S 1206
C1394 H65936-001 22UF 10% 25V X6S 1206
C1396 H65936-001 22UF 10% 25V X6S 1206
C1397 100UF 25V TANT 7343

DESIGN NOTE: RUN threshold - 1.2V

R716 A93548-034 10K 1% 0.0625W RES 0402
R715 J84875-001 1.5K 0.1% 0.063W RES 0402
TP383 EMPTY TH

82 P3V3_SVIN
R718 1 1% 2 0603 A93550-324
C1398 A36096-213 0.1UF 10% 25V X7R 0402

U95 IC HC_LTC7151S

PVIN	4,5,18,19	PGOOD	26
MODE/SYNC	21	SW	9,10,11,12,13,14
PHMODE	28	VOUT-	22
RUN	2	INTVCC	20
TRACK/SS	25	CLKOUT	1
RT	27	FB	23
SVIN	3	ITH	24
GND	6,7,8,15,16,17	MH1	MH1
GND_TPD	29,30,31,32	MH2	MH2
		MH3	MH3
		MH4	MH4

M21811-001

82 IN P3V3_MODE
82 IN P3V3_PHMODE
P3V3_EN_R
P3V3_SS
P3V3_RT
82 P3V3_SVIN

15NF 0402 25V
C1420 K28300-001 X7R
AGND_P3V3

R717 A93548-215 110K 1% 0.0625W RES 0402
AGND_P3V3

+P3V3
R722 A93548-034 10K 1% 0.0625W RES 0402
P3V3_R_POK
R720 0 0402
TP177 EMPTY TH
P3V3_POK

L46 0.33UH 30A IND SM
P3V3_SW

DESIGN NOTE: IRMS : 31.8A ISAT : 30A

C1401 6.3V 0402 H80885-001 10UF
TP113 EMPTY
P3V3_VOUT
P3V3_INTVCC
P3V3_CLKOUT

C1404 H42464-001 47UF 20% 10V X5R 0805
C1405 H42464-001 47UF 20% 10V X5R 0805
C1406 100UF 6.3V TANT SM
C1407 100UF 6.3V TANT SM
C1408 330uF 16V ALUM SM
C1409 330uF 16V ALUM SM
+P3V3
TP178 EMPTY TH

P3V3_FB
R723 56.2k 1 2 G21796-088 0402
C1403 50V 0402 1 2 A36095-025 C0G 47pF

R719 A93548-126 49.9K 1% 0.0625W RES 0402
P3V3_ITH
P3V3_ITH_R
C1399 K13546-001 10PF 5% 50V C0G 0402
C1400 A36095-026 100pF 5% 50V C0G 0402
AGND_P3V3

R721 C79651-007 10K 0.1% 0.0625W RES 0402
C1402 A36096-030 0.1UF 10% 16V EMPTY 0402

P3V3_FB_R
+P3V3
R746 10 1 2 1% 0402 A93548-031
C1421 A36096-030 0.1UF 10% 16V X7R 0402
R793 10 1 2 A93548-031

CAD NOTE: TAP AT MAIN LOAD POINT.

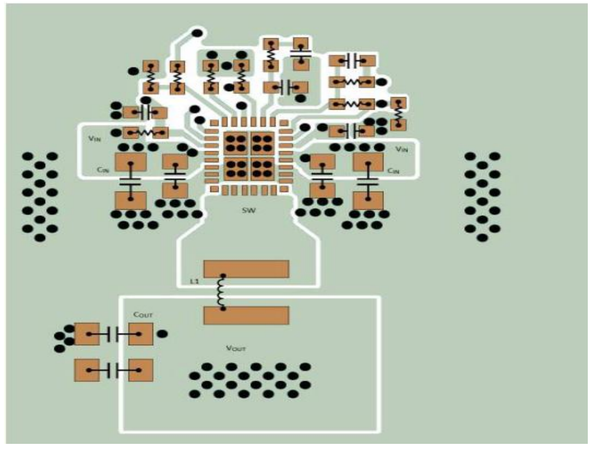
+P3V3
R714 1% 10K 1 2 A93548-034 0402 EMPTY
R713 1% 10K 1 2 A93548-034 0402 EMPTY
82 OUT P3V3_MODE

R712 5% 0 1 2 RES 0402 A93549-001 P3V3_INTVCC 82
R847 1% 10K 1 2 A93548-034 0402 EMPTY
82 OUT P3V3_PHMODE

ST15 EMPTY SM HC_ST
AGND_P3V3

LTC7151SEV#TRPBF

RECOMMENDED LAYOUT GUIDELINES



1. Are there pairs of capacitors (C_{IN}) between V_{IN} and GND as close as possible on both sides of the package? These capacitors provide the AC current to the internal power MOSFETs and their drivers as well as minimize EUI/EMC emissions.
2. Are C_{OUT} and L closely connected? The (–) plate of C_{OUT} returns current to GND and the (–) plate of C_{IN}.
3. Place the FB dividers close to the part with Kelvin connections to V_{OUT} and V_{OUT}– at the point-of-load, for differential V_{OUT} sensing.
4. Keep sensitive components away from the SW pin. The FB resistors, R_T resistor, the compensation component, and the $INTV_{CC}$ bypass caps should be routed away from the SW trace and the inductor.

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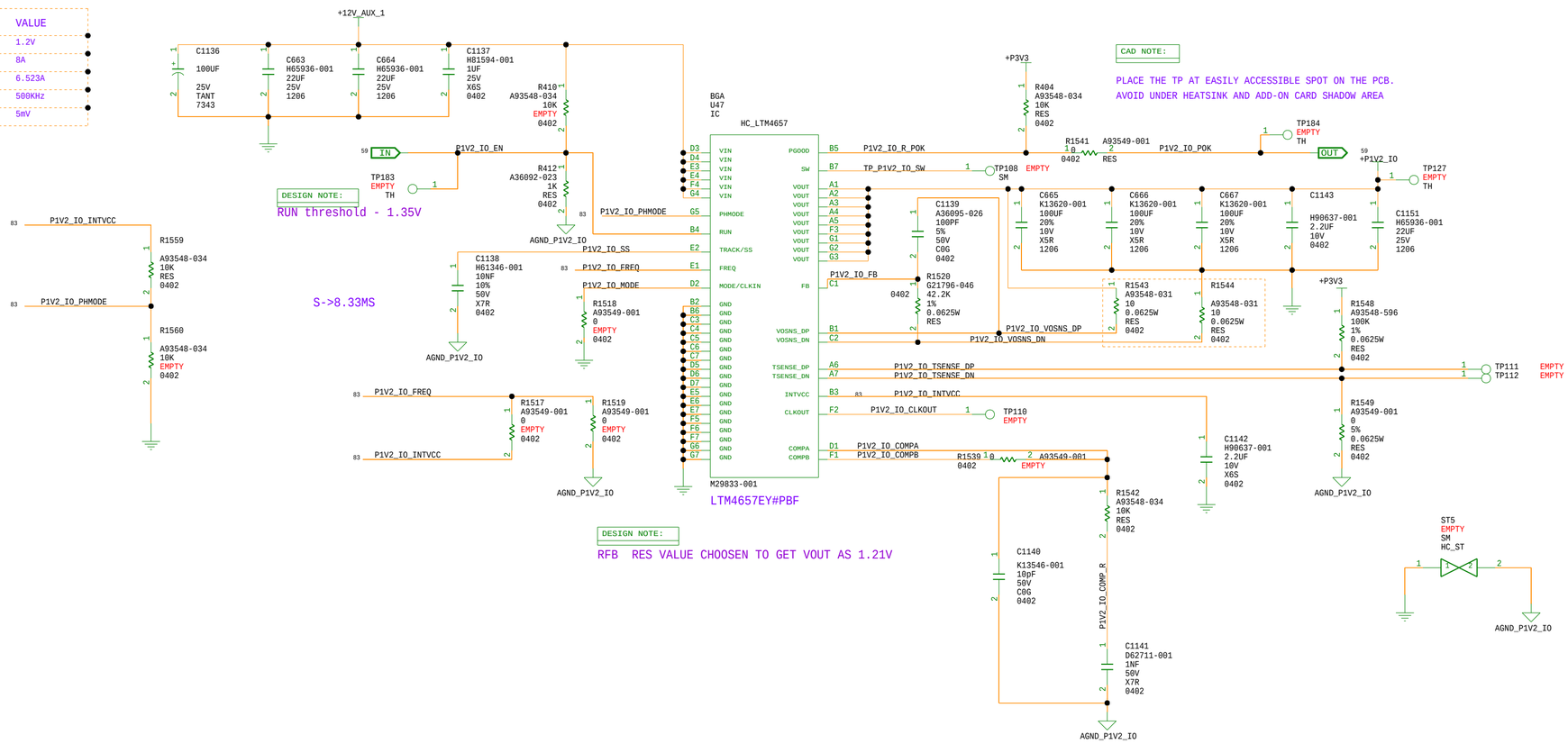
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	82 OF 105

P3V3

P1V2_IO

PARAMETER	VALUE
VOUT	1.2V
MAX CURRENT	8A
LOAD CURRENT	6.523A
FREQUENCY	500KHz
RIPPLE _VOLTAGE	5mV



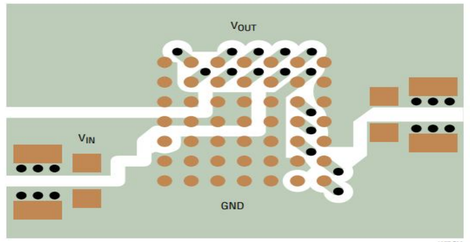
DESIGN NOTE:

RFB RES VALUE CHOOSEN TO GET VOUT AS 1.21V

RECOMMENDED LAYOUT GUIDELINES

- Use large PCB copper areas for high current paths, including V_{IN}, GND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
  - Do not put via directly on the pad, unless they are capped or plated over.
  - Bring out test points on the signal pins for monitoring.
  - Keep separation between CLKIN, CLKOUT and FREQ pin traces to minimize possibility of noise due to cross-talk between these signals.

Figure 22 gives a good example of the recommended layout.



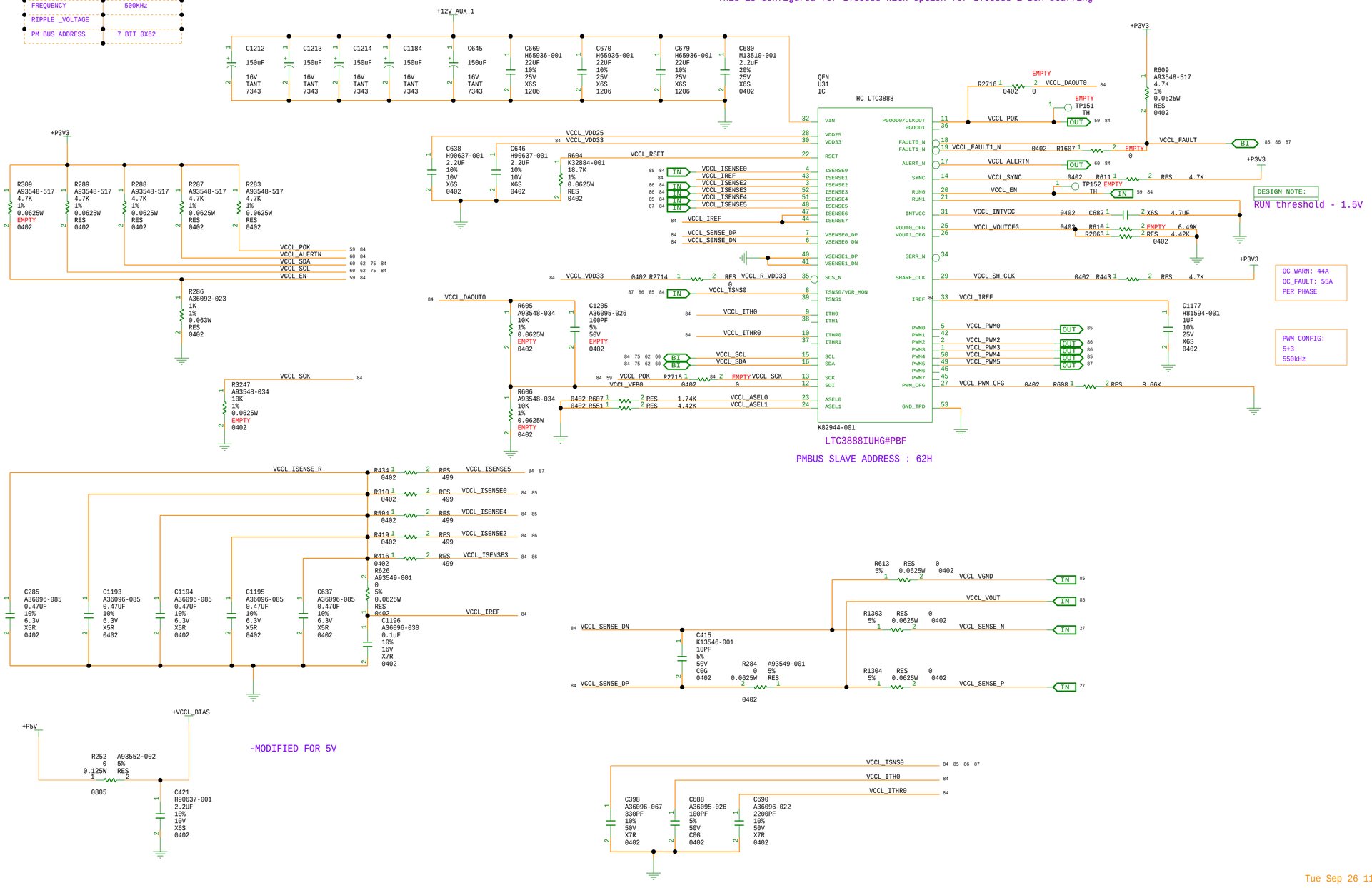
Tue Sep 26 11:48:11 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	83 OF 105

VCCL CONTROLLER

PARAMETER	VALUE
VOUT	0.8V
MAX CURRENT	300A
LOAD CURRENT	248.93A
FREQUENCY	500KHz
RIPPLE _VOLTAGE	
PM BUS ADDRESS	7 BIT 0X62

DESIGN NOTE:
This is configured for LTC3888 with option for LTC3888-1 BOM stuffing



RECOMMENDED LAYOUT GUIDELINES

1. Place a ground or DC voltage layer between a power layer and a small-signal layer. Generally, power planes should be placed on the top layer (4-layer PCB), or top and bottom layer if more than 4 layers are used. Use wide/short copper traces for power components and avoid improper use of thermal relief around power plane vias to minimize resistance and inductance.
2. Low ESR input capacitors should be placed as close as possible to the power stage FET supply and ground connections with the shortest copper traces possible. The power stage must be on the same layer of copper as the input capacitors with a common topside power connection at C_{IN}. Do not attempt to split the input decoupling for multiple phases, as a large resonant loop can result. Vias should not be used to make these connections. Avoid blocking forced air flow to the power stages with large size passive components.
3. Place the inductor input as close as possible to the power stage. Minimize the surface area of the switch node. Make the trace width the minimum needed to support the maximum output current. Avoid copper fills or pours. Avoid running the connection on multiple copper layers in parallel. Minimize capacitance from the switch node to any other trace or plane.
4. PCB traces for remote voltage sense should be run together back to the LTC3888 in pairs with the smallest spacing possible on any given layer on which they are routed. Avoid high frequency switching signals and ideally be shielded with ground planes. Locate any filter component on these traces next to the LTC3888, and not at the Kelvin sense location.
5. PCB traces for output current sense (I_{SENSE}, IREF) should avoid high frequency switching signals and ideally be shielded with ground planes. Filter components on these traces should return to GND (IC paddle) and not to a local PGND.
6. Place low ESR output capacitors adjacent to the inductor output and ground. Output capacitor ground connections must feed into the same copper that connects to the input capacitor ground before connecting back to system ground.
7. Connection of switching ground to system ground, small-signal analog ground or any internal ground plane should be single-point. If the system has an internal system ground plane, a good way to do this is to cluster vias into a single star point to make the connection. This cluster should be located directly beneath the IC GND paddle, which serves as analog signal ground. A useful CAD technique is to make separate ground nets and use a 0Ω resistor to connect them to system ground.
8. Place all small-signal components away from high frequency switching nodes. Place decoupling capacitors for the LTC3888 immediately adjacent to the IC.
9. A good rule of thumb for via count in a given high current path is to use 0.5A per via. Be consistent when applying this rule.
10. Copper fills or pours are good for all power connections except as noted above in rule 3. Copper planes on multiple layers can also be used in parallel. This helps with thermal management and lowers trace inductance, which further improves EMI performance.

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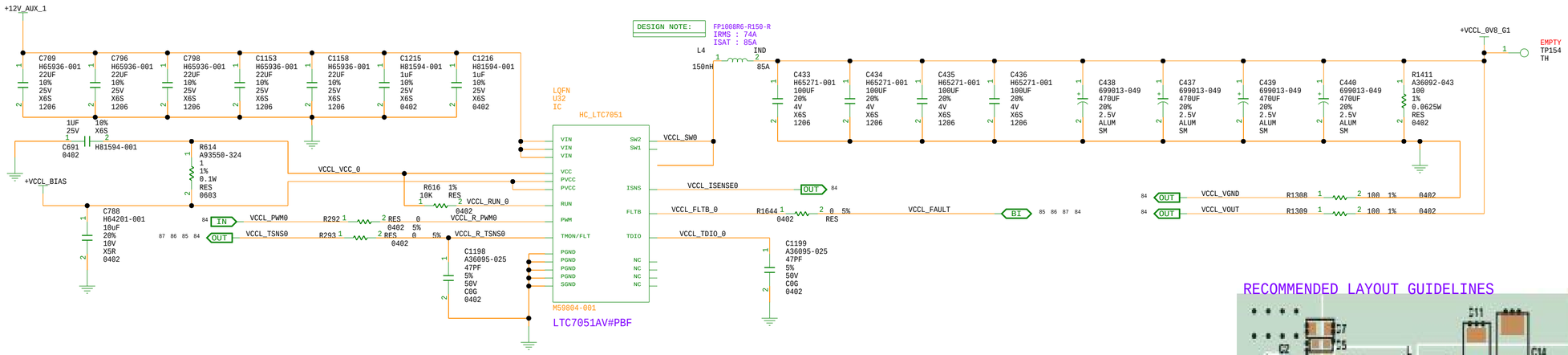
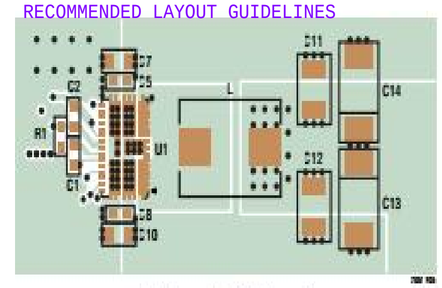
DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	84 OF 105

VCCL CONTROLLER

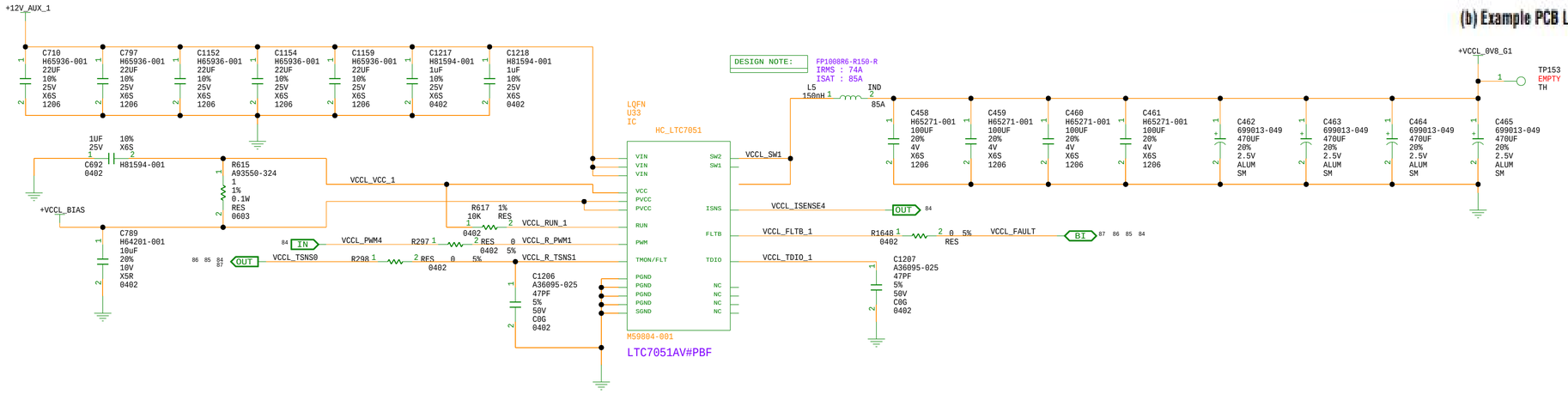
CORE FETS



RECOMMENDED LAYOUT GUIDELINES



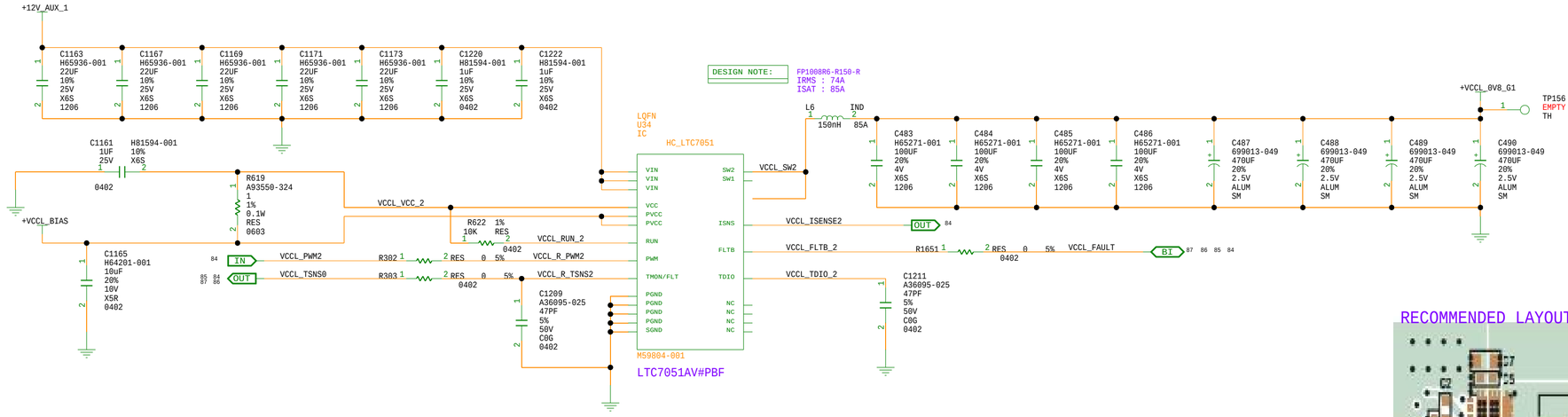
(b) Example PCB Layout



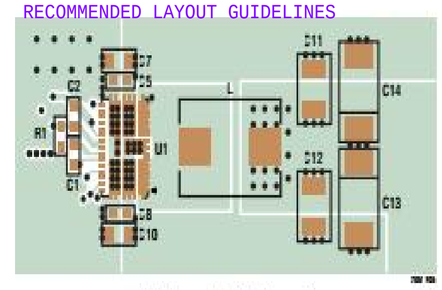
Tue Sep 26 11:48:12 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	85 OF 105

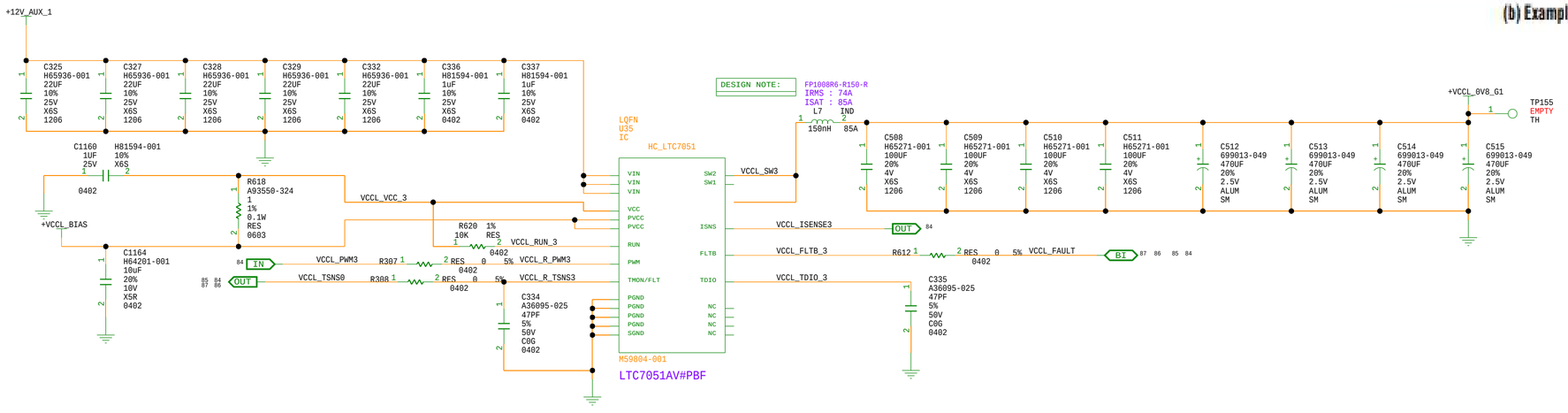
CORE FETS



RECOMMENDED LAYOUT GUIDELINES



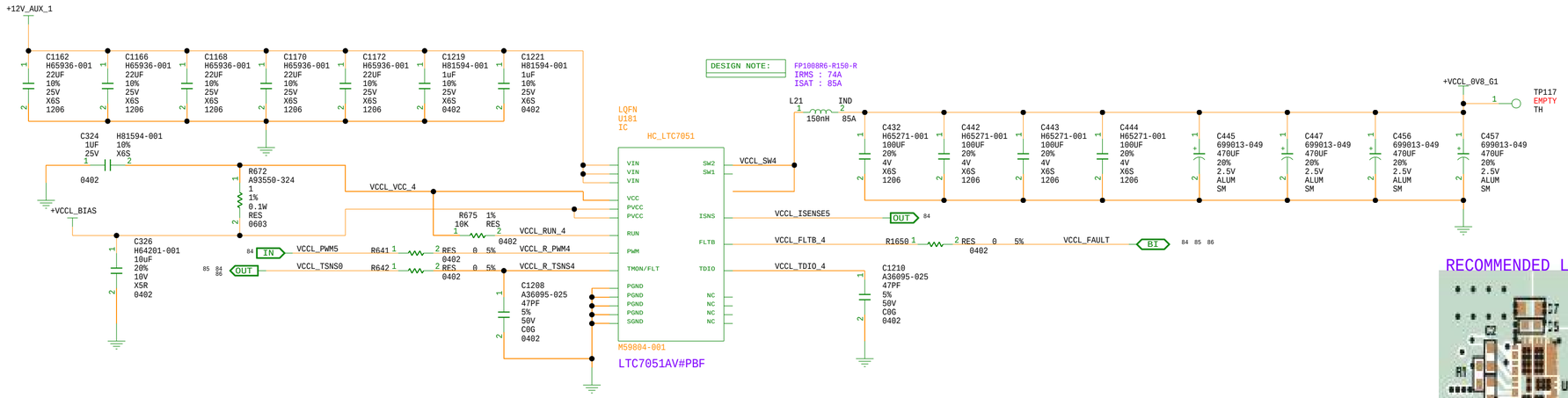
(b) Example PCB Layout



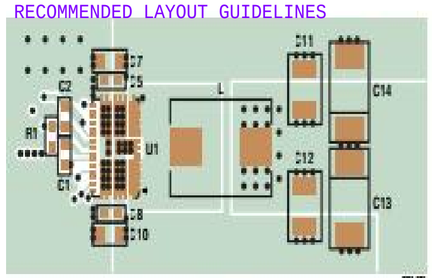
Tue Sep 26 11:48:13 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	86 OF 105

CORE FETS



RECOMMENDED LAYOUT GUIDELINES



(b) Example PCB Layout

Tue Sep 26 11:48:13 2023

DEPARTMENT: UNKNOWN	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	SIZE: C+	CODE: 34649	DOCUMENT NUMBER: 150-0330690-A2 REV: 2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 87 OF 105

CORE FETS

VCC_HSSI_GXF_0V8_UX0_G1

PARAMETER	VALUE
VOUT	0.8V
MAX CURRENT	36A(SINGLE)
LOAD CURRENT	29.067A
FREQUENCY	500KHz
RIPPLE _VOLTAGE	10mV
PM BUS ADDRESS	7 BIT 0X40

I2C SLAVE ADDRESS: 40H

CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

CAD NOTE:
CONNECT NEAR FPGA BGA REGION. NEED TO ROUTE AS KELVIN SENSE

DESIGN NOTE:
RUN threshold - 1.35V

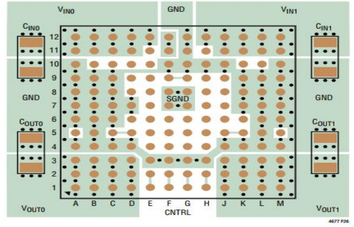
DESIGN NOTE:
Vout config: 0.9V
Vtrim: -99mV

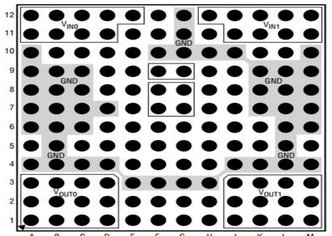
CAD NOTE:
PLEASE THIS BULK CAP ON THE SAME SIDE AS IC

RECOMMENDED LAYOUT GUIDELINES

- Use large PCB copper areas for high current paths, including $V_{IN}n$, GND and $V_{OUT}n$. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the $V_{IN}n$, GND and $V_{OUT}n$ pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the module.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on pads, unless they are capped or plated over.
- Use a separate SGND copper plane for components connected to signal pins. Connect SGND to GND local to the LTM4677.
- For parallel modules, tie the $V_{OUT}n$, V_{OSNS0}^+/V_{OSNS}^- and/or $V_{OSNS1}/SGND$ voltage-sense differential pair lines, RUN_n, $\overline{GPIO}_n$, $COMP_{na}$, SYNC and SHARE_CLK pins together—as shown in Figure 29.
- Bring out test points on the signal pins for monitoring.

Figure 26 gives a good example of the recommended layout.





Tue Sep 26 11:48:14 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation INTEL CORPORATION,BANGALORE INDIA, 560103	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET	88 OF 105

VCC_HSSI_GXF_0V8_UX1_G1

PARAMETER	VALUE
VOUT	0.8V
MAX CURRENT	36A(SINGLE)
LOAD CURRENT	28.787A
FREQUENCY	500KHz
RIPPLE _VOLTAGE	10mV
PM BUS ADDRESS	7 BIT 0X43

I2C SLAVE ADDRESS: 43H

+P3V3

89 59 0V8_Ux1_POK — R30 4.7K 0.0625W RES 0402 1%

R1305 A93548-034 10K 1% 0.0625W EMPTY 0402

89 59 0V8_Ux1_EN

R31 A36092-023 1K 1% 0.063W RES 0402

AGND_0V8_Ux1

R27 A93548-163 2.43K 0.0625W 1% RES 0402 — 0V8_Ux1_ASEL

+12V_AUX_1

C451 150UF 16V TANT 7343

C24 H65936-001 22UF 10% 25V X6S 1206

C25 H65936-001 22UF 10% 25V X6S 1206

C26 H65936-001 22UF 10% 25V X6S 1206

C27 H65936-001 22UF 10% 25V X6S 1206

C28 H65936-001 22UF 10% 25V X6S 1206

C29 D38464-001 10UF 10% 25V X6S 1206

+VCC_HSSI_GXF_0V8_UX1_G1

C22 D97712-022 1UF 10% 16V X6S 0402

R32 A93549-001 0 5% 0.0625W RES 0402

R25 A93549-001 0 5% 0.0625W RES 0402

R1572 RES 0 0V8_Ux1_VOSNS1

TP24 TP_0V8_Ux1_VORB0_DP

TP25 TP_0V8_Ux1_VORB0_DN

TP26 TP_0V8_Ux1_VORB1

0V8_Ux1_TSNS0

0V8_Ux1_TSNS1

CAD NOTE:

CONNECT NEAR FPGA BGA REGION. NEED TO ROUTE AS KELVIN SENSE

DESIGN NOTE:

RUN threshold - 1.35V

EMPTY TP118 TH — 89 59 IN — 0V8_Ux1_EN

80 79 75 62 60 IN PMB_SCL

80 79 75 62 60 B1 PMB_SDA

0V8_U2X_COMP0A

C30 A36096-022 2200PF 10% 50V X7R 0402

C1202 A36095-026 100pF 5% 50V C0G 0402

R1612 EMPTY 0 0V8_Ux1_COMP0B

R33 EMPTY 0 0V8_Ux1_COMP1B

R28 A93548-202 4.99K 1% 0.0625W RES 0402

0V8_Ux1_WP

R26 A36092-023 1K 1% 0.063W RES 0402

AGND_0V8_Ux1

+P3V3

R1578 A93548-202 4.99K 1% 0.0625W RES 0402

R1579 A93548-034 10K 1% 0.0625W RES 0402

89 0V8_Ux1_SYNC

89 0V8_Ux1_SHARE_CLK

ST2 EMPTY SM HC_ST

AGND_0V8_Ux1

BGA U6 IC HC_LTM4677

ASEL, SVIN, VIN0, VIN1, VOSNS0_DP, VOSNS0_DN, VOSNS1, VORB0_DP, VORB0_DN, VORB1, TSNS0A, TSNS0B, TSNS1A, TSNS1B, SW0, SW1, RUN0, RUN1, SCL, SDA, COMP0A, COMP1A, COMP0B, COMP1B, WP, SGND, GND

K15467-001

LTM4677EY#PBF

VDD25 J6 TP_0V8_Ux1_VDD25 — TP21 EMPTY SM

VDD33 J7 TP_0V8_Ux1_VDD33 — TP22 EMPTY SM

ALERT_N E5 PMB_ALERTN — OUT 60 62 75 88 90 91 94 97 100 101

VOUT0 A1 A2 A3 B1 B2 B3 C1 C2 C3 D1 D2 D3

VOUT1 J1 J2 J3 K1 K2 K3 L1 L2 L3 M1 M2 M3

CAD NOTE:

PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB. AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

+VCC_HSSI_GXF_0V8_UX1_G1 — TP12 EMPTY TH

C7 699013-049 470UF 20% 2.5V ALUM SM

C9 H65271-001 100UF 20% 4V X6S 1206

C10 H65271-001 100UF 20% 4V X6S 1206

C11 H65271-001 100UF 20% 4V X6S 1206

C12 H65271-001 100UF 20% 4V X6S 1206

C13 H65271-001 100UF 20% 4V X6S 1206

C14 H65271-001 100UF 20% 4V X6S 1206

CAD NOTE:

PLEASE THIS BULK CAP ON THE SAME SIDE AS IC

C15 699013-049 470UF 20% 2.5V EMPTY SM

C16 H65271-001 100UF 20% 4V X6S 1206

C17 H65271-001 100UF 20% 4V X6S 1206

C18 H65271-001 100UF 20% 4V X6S 1206

C19 H65271-001 100UF 20% 4V X6S 1206

C20 H65271-001 100UF 20% 4V X6S 1206

C21 H65271-001 100UF 20% 4V X6S 1206

PLACEHOLDER

VOUTOCFG G5, VOUT1CFG G6 — 0V8_Ux1_VOUTCFG

VTRIM0CFG H5, VTRIM1CFG H6 — 0V8_Ux1_VTRIMCFG

R14 A93549-001 0 5% 0.0625W RES 0402

R1370 G21796-163 825 1% 0.0625W RES 0402

INTVCC F9, INTVCC G9 — 0V8_Ux1_INTVCC — TP23 EMPTY SM

FSWPHCFG H4 — 0V8_Ux1_FSWPHCFG — R1573 6.34K

SHARE_CLK H7 — 0V8_Ux1_SHARE_CLK — 89

SYNC E7 — 0V8_Ux1_SYNC — 89

AGND_0V8_Ux1

SNUB0 A5, SNUB1 M5 — 0V8_Ux1_SNUB0, 0V8_Ux1_SNUB1

R1307 A93548-034 10K 1% 0.0625W EMPTY 0402

R1310 A93548-034 10K 1% 0.0625W EMPTY 0402

GPIO0_N E4, GPIO1_N F4 — 0V8_Ux1_POK — OUT 59 89 — TP121 EMPTY TH

DNC C10, E11, H11, K10

ISNS0A_DP F2 0V8_Ux1_ISNS0_DP, ISNS0A_DN E2 0V8_Ux1_ISNS0_DN

ISNS0B_DP F1, ISNS0B_DN E1

ISNS1A_DP H2 0V8_Ux1_ISNS1_DP, ISNS1A_DN G2 0V8_Ux1_ISNS1_DN

ISNS1B_DP H1, ISNS1B_DN G1

SGND G7, G8 — AGND_0V8_Ux1

DESIGN NOTE:

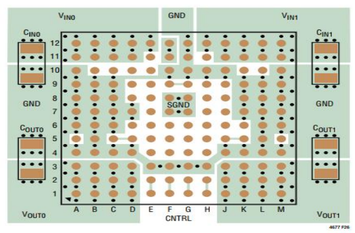
Vout config: 0.9V
Vtrim: -99mV

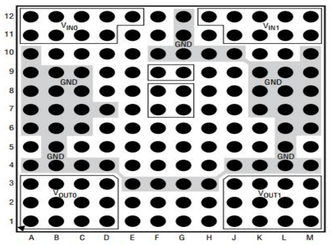
RECOMMENDED LAYOUT GUIDELINES

- Use large PCB copper areas for high current paths, including $V_{IN}n$, GND and $V_{OUT}n$. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the $V_{IN}n$, GND and $V_{OUT}n$ pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the module.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on pads, unless they are capped or plated over.

- Use a separate SGND copper plane for components connected to signal pins. Connect SGND to GND local to the LTM4677.
- For parallel modules, tie the $V_{OUT}n$, V_{OSNS0}^+/V_{OSNS0}^- and/or V_{OSNS1}/SGND voltage-sense differential pair lines, RUN_n, $GPIO_n$, $COMP_{na}$, SYNC and SHARE_CLK pins together—as shown in Figure 29.
- Bring out test points on the signal pins for monitoring.

Figure 26 gives a good example of the recommended layout.





Tue Sep 26 11:48:14 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE	SCALE:	DO NOT SCALE DRAWING	SHEET	89 OF 105
	INDIA, 560103				

VCC_HSSI_GXF_0V8_UX1_G1

VCC_HSSI_GXF_0V8_UX2_G1

PARAMETER	VALUE
VOUT	0.8V
MAX CURRENT	36A(SINGLE)
LOAD CURRENT	28.787A
FREQUENCY	500KHz
RIPPLE _VOLTAGE	10mV
PM BUS ADDRESS	7 BIT 0X46

I2C SLAVE ADDRESS: 46H

+P3V3
PMB_SCL R1298 2.2K 1% 0.0625W 0402
PMB_SDA R1299 2.2K 1% 0.0625W 0402
PMB_ALERTN R1300 2.2K 1% 0.0625W 0402
0V8_Ux2_POK R366 4.7K 1% 0.0625W 0402

+12V_AUX_1
C449 150UF 16V TANT 7343
C630 H65936-001 22UF 10% 25V X6S 1206
C631 H65936-001 22UF 10% 25V X6S 1206
C632 H65936-001 22UF 10% 25V X6S 1206
C633 H65936-001 22UF 10% 25V X6S 1206
C634 H65936-001 22UF 10% 25V X6S 1206
C635 D38464-001 10UF 10% 25V X6S 1206
AGND_0V8_Ux2

R372 A93548-494 5.23K 1% 0.0625W RES 0402
0V8_Ux2_ASEL

BGA U44 IC
HC_LTM4677

+VCC_HSSI_GXF_0V8_UX2_G1
C624 D97712-022 1UF 10% 16V X6S 0402
R1282 A93549-001 0 5% 0.0625W RES 0402
R1283 A93549-001 0 5% 0.0625W RES 0402
R1566 0 RES
P0V8_Ux2_VOSNS0_DP
P0V8_Ux2_VOSNS0_DN
P0V8_Ux2_VOSNS1

TP33 TP_0V8_Ux2_VORB0_DP
TP34 TP_0V8_Ux2_VORB0_DN
TP45 TP_0V8_Ux2_VORB1
0V8_Ux2_TSNS0
0V8_Ux2_TSNS1

CAD NOTE:
CONNECT NEAR FPGA BGA REGION. NEED TO ROUTE AS KELVIN SENSE

DESIGN NOTE:
RUN threshold - 1.35V

EMPTY TP157 TH
0V8_Ux2_EN

PMB_SCL
PMB_SDA

+P3V3
R1324 A93548-034 10K 1% 0.0625W EMPTY 0402
0V8_Ux2_EN
R367 A36092-023 1K 1% 0.063W RES 0402
AGND_0V8_Ux2

0V8_Ux2_COMPA
R1608 2 EMPTY 0 0V8_Ux2_COMP0B
R1609 2 EMPTY 0 0V8_Ux2_COMP1B
C628 A36096-022 2200PF 10% 50V X7R 0402
C1209 A36095-026 100pF 5% 50V C0G
0V8_Ux2_COMPA_C
R379 A93548-202 4.99K 1% 0.0625W RES 0402
AGND_0V8_Ux2

0V8_Ux2_WP
R378 A36092-023 1K 1% 0.063W RES 0402
AGND_0V8_Ux2

+P3V3
R1568 A93548-202 4.99K 1% 0.0625W RES 0402
R1569 A93548-034 10K 1% 0.0625W RES 0402
0V8_Ux2_SYNC
0V8_Ux2_SHARE_CLK

ST8 EMPTY SM HC_ST
AGND_0V8_Ux2

K15467-001
LTM4677EY#PBF

TP_0V8_Ux2_VDD25 TP46 EMPTY SM
TP_0V8_Ux2_VDD33 TP47 EMPTY SM
PMB_ALERTN

CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

+VCC_HSSI_GXF_0V8_UX2_G1
TP80 EMPTY TH

C2516 699013-049 470UF 20% 2.5V ALUM SM
C2518 H65271-001 100UF 20% 4V X6S 1206
C2519 H65271-001 100UF 20% 4V X6S 1206
C2674 H65271-001 100UF 20% 4V X6S 1206
C2675 H65271-001 100UF 20% 4V X6S 1206
C2676 H65271-001 100UF 20% 4V X6S 1206
C2677 H65271-001 100UF 20% 4V X6S 1206

CAD NOTE:
PLEASE THIS BULK CAP ON THE SAME SIDE AS IC

C2513 699013-049 470UF 20% 2.5V EMPTY SM
C2512 H65271-001 100UF 20% 4V X6S 1206
C2514 H65271-001 100UF 20% 4V X6S 1206
C2515 H65271-001 100UF 20% 4V X6S 1206
C621 H65271-001 100UF 20% 4V X6S 1206
C622 H65271-001 100UF 20% 4V X6S 1206
C623 H65271-001 100UF 20% 4V X6S 1206
PLACEHOLDER

0V8_Ux2_VOUTCFG
0V8_Ux2_VTRIMCFG
R1325 A93549-001 0 5% 0.0625W RES 0402
R1368 G21796-163 825 1% 0.0625W RES 0402
AGND_0V8_Ux2

TP48 EMPTY SM
0V8_Ux2_INTVCC
0V8_Ux2_FSWPHCFG
R1567 6.34K EMPTY
0V8_Ux2_SHARE_CLK
0V8_Ux2_SYNC

0V8_Ux2_SNUB0
0V8_Ux2_SNUB1
R1327 A93548-034 10K 1% 0.0625W EMPTY 0402
R1328 A93548-034 10K 1% 0.0625W EMPTY 0402
0V8_Ux2_POK
TP158 TH EMPTY

0V8_Ux2_ISNS0_DP
0V8_Ux2_ISNS0_DN
0V8_Ux2_ISNS1_DP
0V8_Ux2_ISNS1_DN
AGND_0V8_Ux2

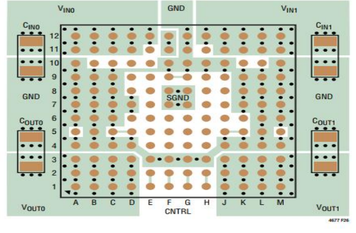
DESIGN NOTE:
Vout config: 0.9V
Vtrim: -99mV

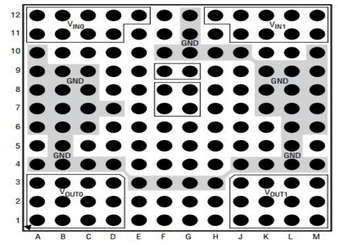
RECOMMENDED LAYOUT GUIDELINES

- Use large PCB copper areas for high current paths, including $V_{IN}n$, GND and $V_{OUT}n$. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the $V_{IN}n$, GND and $V_{OUT}n$ pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the module.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on pads, unless they are capped or plated over.

- Use a separate SGND copper plane for components connected to signal pins. Connect SGND to GND local to the LTM4677.
- For parallel modules, tie the $V_{OUT}n$, V_{OSNS0}^+/V_{OSNS}^- and/or V_{OSNS1}/SGND voltage-sense differential pair lines, RUN_n, $GPIO_n$, $COMP_{na}$, SYNC and SHARE_CLK pins together—as shown in Figure 29.
- Bring out test points on the signal pins for monitoring.

Figure 26 gives a good example of the recommended layout.





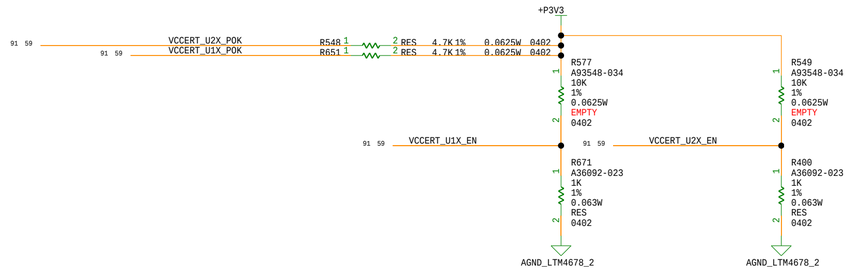
Tue Sep 26 11:48:15 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation INTEL CORPORATION,BANGALORE INDIA, 560103	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET	90 OF 105

VCC_HSSI_GXP_0V8_Ux2_G1

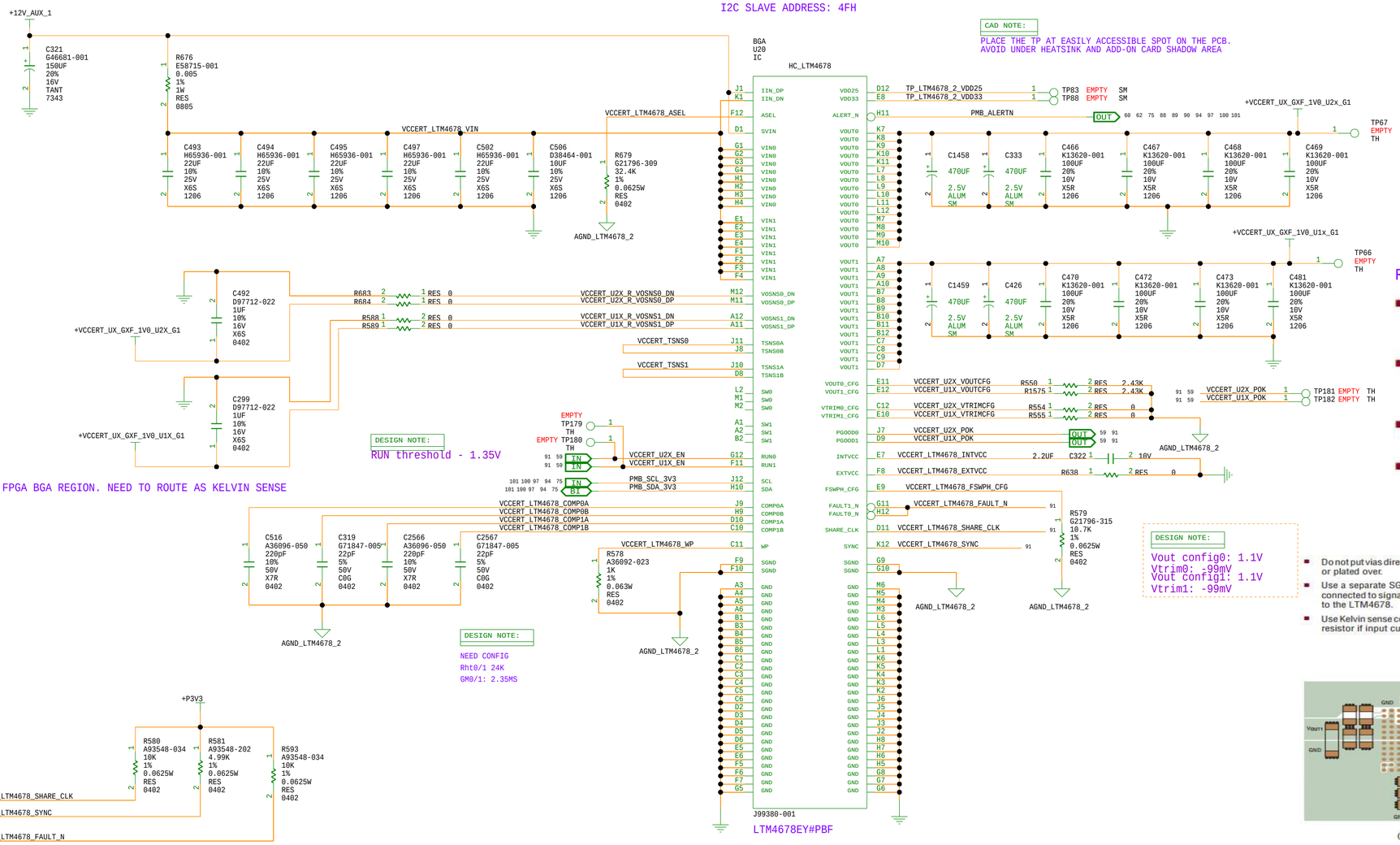
VCCERT_U1x/VCCERT_U2x

PARAMETER	VALUE
VOUT_1	1V
VOUT_2	1V
MAX CURRENT	25A(DUAL)
LOAD CURRENT_1	19.585A
LOAD CURRENT_2	19.585A
FREQUENCY	750KHZ
RIPPLE _VOLTAGE	10mV
PM BUS ADDRESS	7 BIT 0X4F



I2C SLAVE ADDRESS: 4FH

CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA



RECOMMENDED LAYOUT GUIDELINES

- Use large PCB copper areas for high current paths, including V_{INn}, GND and V_{OUTn}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{INn}, GND and V_{OUTn} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the module.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.

- Do not put vias directly on pads, unless they are capped or plated over.
- Use a separate SGND copper plane for components connected to signal pins. Connect SGND to GND local to the LTM4678.
- Use Kelvin sense connections across the input R_{SENSE} resistor if input current monitoring is used.

For parallel modules, tie the V_{OUTn}, V_{OSNSn}+/V_{OSNSn}- voltage-sense differential pair lines, RUNn, COMPna, COMPnb pin together.

- The user must share the SYNC, SHARE_CLK, FAULT, and ALERT pins of these parts. Be sure to use pull-up resistors on FAULT, SHARE_CLK and ALERT.
- Bring out test points on the signal pins for monitoring.

Figure 44 gives a good example of the recommended layout.

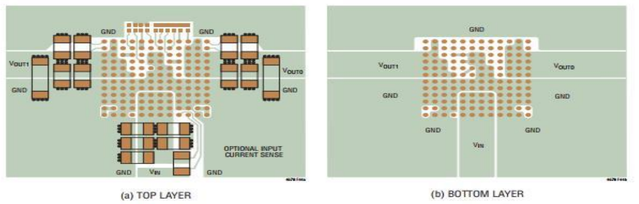


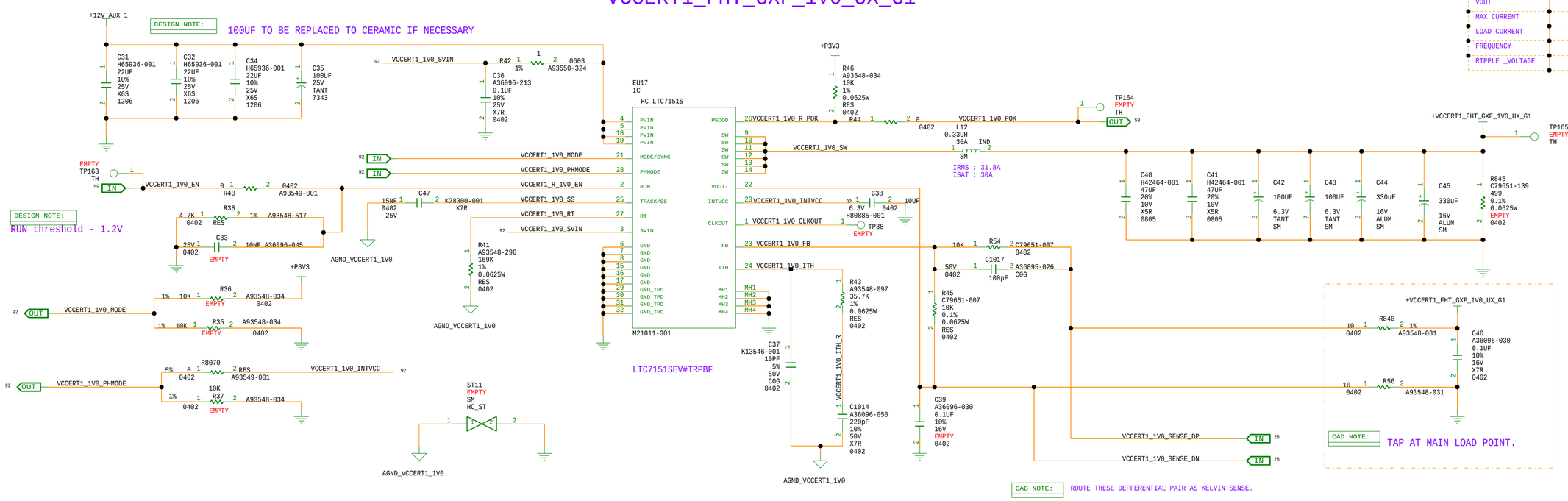
Figure 44. Recommended PCB Layout Package Top View

Tue Sep 26 11:48:16 2023

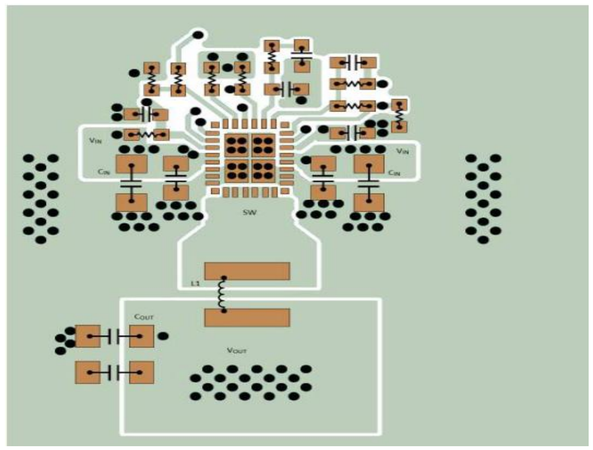
DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	91 OF 105

VCCERT1_FHT_GXF_1V0_UX_G1

PARAMETER	VALUE
VOUT	1V
MAX CURRENT	15A
LOAD CURRENT	12.2A
FREQUENCY	1MHz
RIPPLE _VOLTAGE	



RECOMMENDED LAYOUT GUIDELINES



1. Are there pairs of capacitors (C_{IN}) between V_{IN} and GND as close as possible on both sides of the package? These capacitors provide the AC current to the internal power MOSFETs and their drivers as well as minimize EUI/EMC emissions.
2. Are C_{OUT} and L closely connected? The (–) plate of C_{OUT} returns current to GND and the (–) plate of C_{IN}.
3. Place the FB dividers close to the part with Kelvin connections to V_{OUT} and V_{OUT}– at the point-of-load, for differential V_{OUT} sensing.
4. Keep sensitive components away from the SW pin. The FB resistors, R_T resistor, the compensation component, and the $INTV_{CC}$ bypass caps should be routed away from the SW trace and the inductor.

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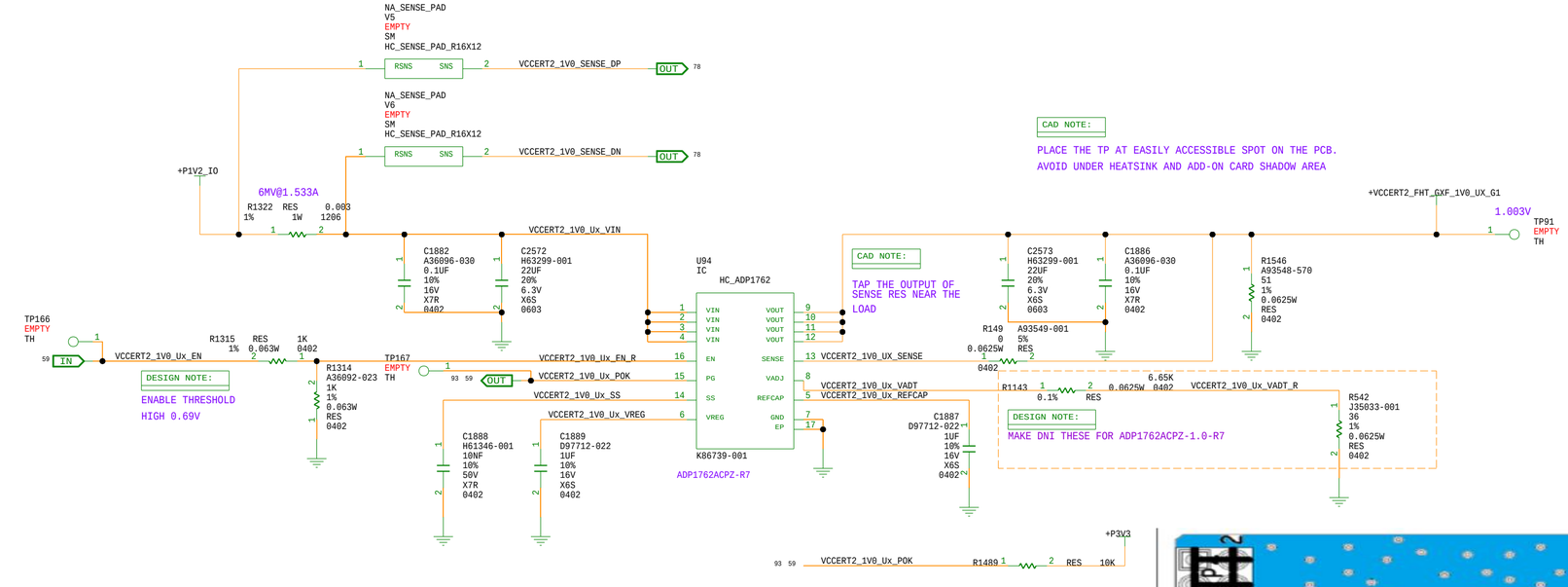
DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	92 OF 105

VCCERT2_FHT_GXF_1V0_UX_G1



PARAMETER	VALUE
VOUT	1V
MAX CURRENT	2A
LOAD CURRENT	1.533A
FREQUENCY	
RIPPLE _VOLTAGE	

RECOMMENDED LAYOUT GUIDELINES

- Place the input capacitor as close as possible to the VIN and GND pins.
- Place the output capacitor as close as possible to the VOUT and GND pins.
- Place the soft start capacitor (C_{SS}) as close as possible to the SS pin.
- Place the reference capacitor (C_{REF}) and regulator capacitor (C_{REG}) as close as possible to the REFCAP pin and the VREG pin, respectively.
- Connect the load as close as possible to the VOUT and SENSE pins.

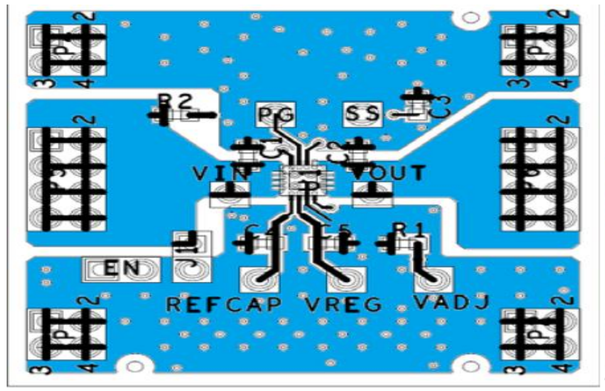


Figure 45. Typical Board Layout, Top Side

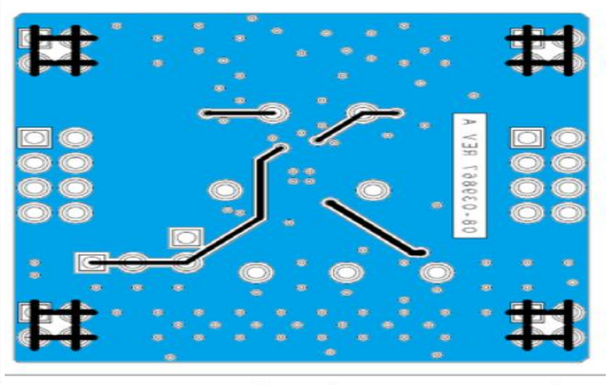


Figure 46. Typical Board Layout, Bottom Side

Tue Sep 26 11:48:16 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103 COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SCALE:	DO NOT SCALE DRAWING	SHEET	93 OF 105

VCCERT2_FHT_GXF_1V0_UX_G1

P0V8_G1/P1V8_G2

PARAMETER	VALUE
VOUT_1	0.8V
VOUT_2	1.8V
MAX CURRENT	25A(DUAL)
LOAD CURRENT_1	16.541A
LOAD CURRENT_2	20.753A
FREQUENCY	425KHz
RIPPLE _VOLTAGE	10mV
PM BUS ADDRESS	7 BIT 0X4E

I2C SLAVE ADDRESS: 4EH

CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

DESIGN NOTE:
RUN threshold - 1.35V

CAD NOTE:
CONNECT NEAR FPGA BGA REGION. NEED TO ROUTE AS KELVIN SENSE

DESIGN NOTE:
NEED CONFIG
Rht0/1 24K
gm0/1: 1.68ms

DESIGN NOTE:
Vout config0: 0.9V
Vtrim0: -99mV
Vout config1: 1.9V
Vtrim1: -99mV

RECOMMENDED LAYOUT GUIDELINES

- Use large PCB copper areas for high current paths, including V_{INn}, GND and V_{OUTn}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{INn}, GND and V_{OUTn} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the module.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.

- Do not put vias directly on pads, unless they are capped or plated over.
- Use a separate SGND copper plane for components connected to signal pins. Connect SGND to GND local to the LTM4678.
- Use Kelvin sense connections across the input R_{SENSE} resistor if input current monitoring is used.

For parallel modules, tie the V_{OUTn}, V_{OSNSn}+/V_{OSNSn}- voltage-sense differential pair lines, RUN*n*, COMP*na*, $COMP_{nb}$ pin together.

- The user must share the SYNC, SHARE_CLK, FAULT, and ALERT pins of these parts. Be sure to use pull-up resistors on FAULT, SHARE_CLK and ALERT.
- Bring out test points on the signal pins for monitoring.

Figure 44 gives a good example of the recommended layout.

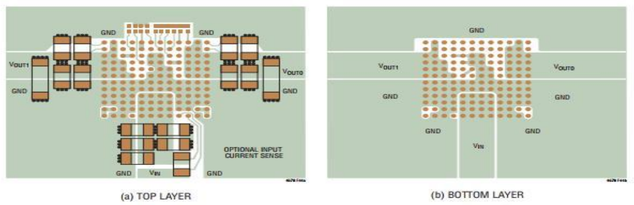


Figure 44. Recommended PCB Layout Package Top View

Tue Sep 26 11:48:17 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	94 OF 105

VCCEHT_FHT_GXF_1V5_U1X_G2

PARAMETER	VALUE
VOUT	1.5V
MAX CURRENT	2A
LOAD CURRENT	1.18A
FREQUENCY	
RIPPLE _VOLTAGE	

17.7MV@1.18A

CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

DESIGN NOTE:
ENABLE THRESHOLD
HIGH 1.31V

CAD NOTE:
PLACE THESE NEAR TO VR

P2V5_G2

PARAMETER	VALUE
VOUT	2.5V
MAX CURRENT	8A
LOAD CURRENT	4.413A
FREQUENCY	1MHZ
RIPPLE _VOLTAGE	5mV

DESIGN NOTE:
RUN threshold - 1.35V

S->0.833MS

CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

LTM4657EY#PBF

RECOMMENDED LAYOUT GUIDELINES

Place the input capacitor as close as possible between the VIN pin and ground. Place the output capacitor as close as possible between the VOUT pin and ground. Place the bypass capacitors (C_{REG}, C_{REF}, and C_{BYP}) for V_{REG}, V_{REF}, and V_{BYP} close to the respective pins (VREG, REF, and BYP) and ground. The use of a 0805, a 0603, or a 0402 size capacitor achieves the smallest possible footprint solution on boards where area is limited. Maximize the amount of ground metal for the exposed pad, and use as many vias as possible on the component side to improve thermal dissipation.

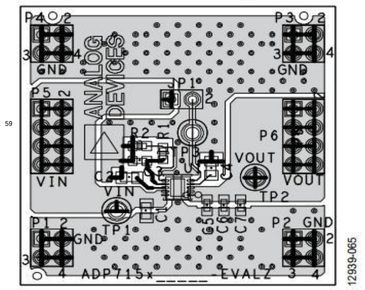
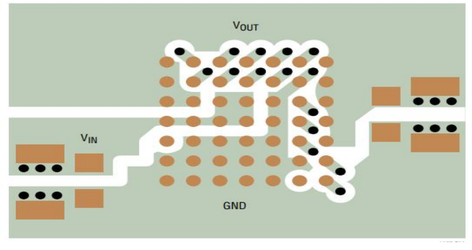


Figure 63. Sample 10-Lead LFCSP PCB Layout

RECOMMENDED LAYOUT GUIDELINES

- Use large PCB copper areas for high current paths, including V_{IN}, GND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
  - Do not put via directly on the pad, unless they are capped or plated over.
  - Bring out test points on the signal pins for monitoring.
  - Keep separation between CLKIN, CLKOUT and FREQ pin traces to minimize possibility of noise due to cross-talk between these signals.

Figure 22 gives a good example of the recommended layout.



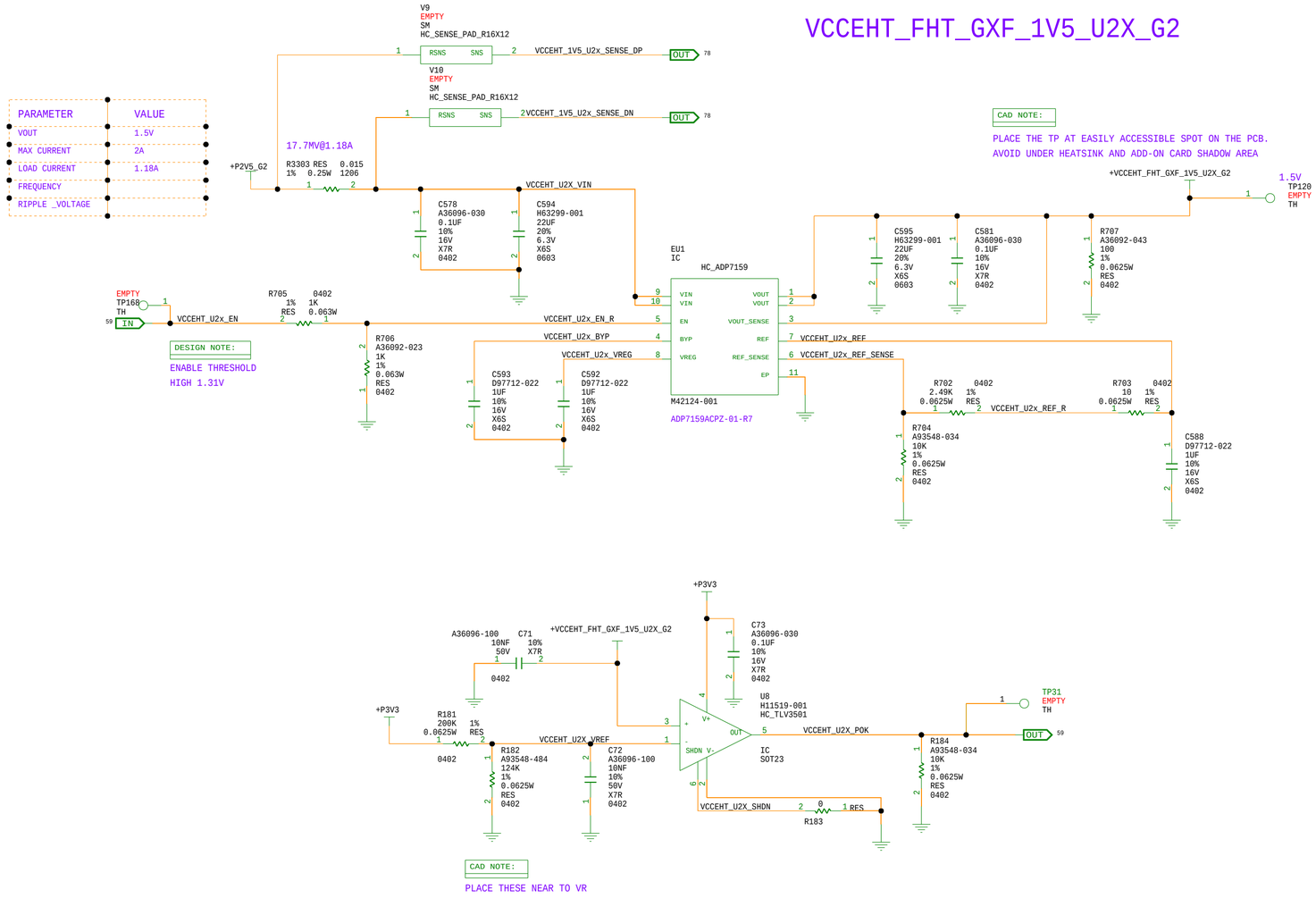
Tue Sep 26 11:48:18 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation INTEL CORPORATION,BANGALORE INDIA, 560103	C+	34649	150-0330690-A2	2.0
	COPYRIGHT (C) 2021, INTEL CORPORATION. ALL RIGHTS RESERVED	SCALE:	DO NOT SCALE DRAWING	SHEET	95 OF 105

VCCEHT_FHT_GXF_1V5_U1X_G2/P2V5_G2

VCCEHT_FHT_GXF_1V5_U2X_G2

PARAMETER	VALUE
VOUT	1.5V
MAX CURRENT	2A
LOAD CURRENT	1.18A
FREQUENCY	
RIPPLE _VOLTAGE	



RECOMMENDED LAYOUT GUIDELINES

Place the input capacitor as close as possible between the VIN pin and ground. Place the output capacitor as close as possible between the VOUT pin and ground. Place the bypass capacitors (C_{REG}, C_{REF}, and C_{BYP}) for V_{REG}, V_{REF}, and V_{BYP} close to the respective pins (VREG, REF, and BYP) and ground. The use of a 0805, a 0603, or a 0402 size capacitor achieves the smallest possible footprint solution on boards where area is limited. Maximize the amount of ground metal for the exposed pad, and use as many vias as possible on the component side to improve thermal dissipation.

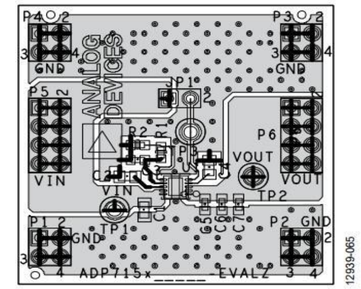


Figure 63. Sample 10-Lead LFCSP PCB Layout

Tue Sep 26 11:48:18 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	96 OF 105

P1V2_G3

PARAMETER	VALUE
VOUT	1.2V
MAX CURRENT	50A(SINGLE)
LOAD CURRENT	31.978A
FREQUENCY	350KHz
RIPPLE _VOLTAGE	10mV
PM BUS ADDRESS	7 BIT 0X4D

I2C SLAVE ADDRESS: 4DH

+P3V3

97 59 P1V2_G3_POK — R623 RES 4.7K 1% 0.0625W 0402 — R1387 A93548-034 10K 1% 0.0625W EMPTY 0402

97 59 P1V2_G3_EN — R627 A36092-023 1K 1% 0.063W RES 0402

AGND_P1V2_G3

+12V_AUX_1

C1114 G46681-001 150UF 20% 16V TANT 7343

R630 E58715-001 0.005 1% 1W RES 0805

P1V2_G3_VIN

C410 H65936-001 22UF 10% 25V X6S 1206
C412 H65936-001 22UF 10% 25V X6S 1206
C414 H65936-001 22UF 10% 25V X6S 1206
C417 H65936-001 22UF 10% 25V X6S 1206
C419 H65936-001 22UF 10% 25V X6S 1206
C424 D38464-001 10UF 10% 25V X6S 1206

P1V2_G3_ASEL — R557 H89932-001 18K 1% 0.0625W RES 0402 — AGND_P1V2_G3

BGA
U10
IC

HC_LTM4678

J1	IIN_DP	VDD25	D12
K1	IIN_DN	VDD33	E8
F12	ASEL	ALERT_N	H11
D1	SVIN	VOUT0	K7
G1	VIN0	VOUT0	K8
G2	VIN0	VOUT0	K9
G3	VIN0	VOUT0	K10
G4	VIN0	VOUT0	K11
H1	VIN0	VOUT0	L7
H2	VIN0	VOUT0	L8
H3	VIN0	VOUT0	L9
H4	VIN0	VOUT0	L10
		VOUT0	L11
		VOUT0	L12
		VOUT0	M7
		VOUT0	M8
		VOUT0	M9
		VOUT0	M10
E1	VIN1	VOUT1	A7
E2	VIN1	VOUT1	A8
E3	VIN1	VOUT1	A9
E4	VIN1	VOUT1	A10
F1	VIN1	VOUT1	B7
F2	VIN1	VOUT1	B8
F3	VIN1	VOUT1	B9
F4	VIN1	VOUT1	B10
		VOUT1	B11
		VOUT1	B12
		VOUT1	C7
		VOUT1	C8
		VOUT1	C9
		VOUT1	D7
M12	VOSNS0_DN		
M11	VOSNS0_DP		
A12	VOSNS1_DN		
A11	VOSNS1_DP		
J11	TSNS0A		
J8	TSNS0B		
J10	TSNS1A		
D8	TSNS1B		
L2	SW0		
M1	SW0		
M2	SW0		
A1	SW1		
A2	SW1		
B2	SW1		
G12	RUN0		
F11	RUN1		
J12	SCL		
H10	SDA		
J9	COMP0A		
H9	COMP0B		
D10	COMP1A		
C10	COMP1B		
C11	WP		
F9	SGND		
F10	SGND		
A3	GND		
A4	GND		
A5	GND		
A6	GND		
B1	GND		
B3	GND		
B4	GND		
B5	GND		
B6	GND		
C1	GND		
C2	GND		
C3	GND		
C4	GND		
C5	GND		
C6	GND		
D2	GND		
D3	GND		
D4	GND		
D5	GND		
D6	GND		
E5	GND		
E6	GND		
F5	GND		
F6	GND		
F7	GND		
G5	GND		
		GND	M6
		GND	M5
		GND	M4
		GND	M3
		GND	L6
		GND	L5
		GND	L4
		GND	L3
		GND	L1
		GND	K6
		GND	K5
		GND	K4
		GND	K3
		GND	K2
		GND	J6
		GND	J5
		GND	J4
		GND	J3
		GND	J2
		GND	H8
		GND	H7
		GND	H6
		GND	H5
		GND	G8
		GND	G7
		GND	G6

J99380-001
LTM4678EY#PBF

TP_P1V2_G3_VDD25 — 1 TP63 EMPTY SM
TP_P1V2_G3_VDD33 — 1 TP65 EMPTY SM

PMB_ALERTN — OUT — 60 62 75 88 89 90 91 94 100 101

+P1V2_G3 — 1 TP73 EMPTY TH

C390 470UF 2.5V ALUM SM
C391 470UF 2.5V ALUM SM
C350 K13620-001 100UF 20% 10V X5R 1206
C375 K13620-001 100UF 20% 10V X5R 1206
C342 K13620-001 100UF 20% 10V X5R 1206
C377 K13620-001 100UF 20% 10V X5R 1206
C387 K13620-001 100UF 20% 10V X5R 1206
C344 K13620-001 100UF 20% 10V X5R 1206
C408 K13620-001 100UF 20% 10V X5R 1206
C338 K13620-001 100UF 20% 10V X5R 1206

CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

RECOMMENDED LAYOUT GUIDELINES

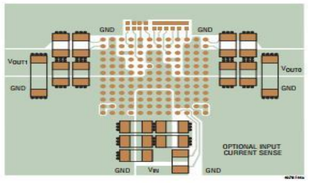
- Use large PCB copper areas for high current paths, including V_{INn}, GND and V_{OUTn}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{INn}, GND and V_{OUTn} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the module.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.

- Do not put vias directly on pads, unless they are capped or plated over.
- Use a separate SGND copper plane for components connected to signal pins. Connect SGND to GND local to the LTM4678.
- Use Kelvin sense connections across the input R_{SENSE} resistor if input current monitoring is used.

For parallel modules, tie the V_{OUTn}, V_{OSNSn}^+/V_{OSNSn}^- voltage-sense differential pair lines, RUN_n, $COMP_{na}$, $COMP_{nb}$ pin together.

- The user must share the SYNC, SHARE_CLK, FAULT, and ALERT pins of these parts. Be sure to use pull-up resistors on FAULT, SHARE_CLK and ALERT.
- Bring out test points on the signal pins for monitoring.

Figure 44 gives a good example of the recommended layout.



(a) TOP LAYER (b) BOTTOM LAYER

Figure 44. Recommended PCB Layout Package Top View

DESIGN NOTE:
Vout config: 1.3V
Vtrim: -99mV

CAD NOTE:
CONNECT NEAR FPGA BGA REGION. NEED TO ROUTE AS KELVIN SENSE

DESIGN NOTE:
RUN threshold - 1.35V

EMPTY TP125 TH — 97 59 IN — P1V2_G3_EN

101 100 94 91 75 IN — PMB_SCL_3V3
101 100 94 91 75 B1 — PMB_SDA_3V3

C1107 D62711-001 1nF 10% 50V X7R 0402
C1112 A36095-026 100PF 5% 50V C0G 0402

P1V2_G3_COMP0A
P1V2_G3_COMP0B

NEED CONFIG
Rht0 20k
gm0: 3.69m

AGND_P1V2_G3

+P1V2_G3 — C406 D97712-022 1UF 10% 16V X6S 0402

R632 2 — 1 RES 0
R634 2 — 1 RES 0

P1V2_G3_R_VOSNS0_DN
P1V2_G3_R_VOSNS0_DP

R582 1 — 2 RES 0 P1V2_G3_R_VOSNS1_DN
R584 1 — 2 RES 0 P1V2_G3_R_VOSNS1_DP

P1V2_G3_TSNS0
P1V2_G3_TSNS1

P1V2_G3_WP — R1388 A36092-023 1K 1% 0.063W RES 0402 — AGND_P1V2_G3

P1V2_G3_VOUTCFG — R685 1 — 2 RES 1.62K
P1V2_G3_VTRIMCFG — R686 1 — 2 RES 0 — TP145 EMPTY TH

P1V2_G3_POK — OUT — 59 97 AGND_P1V2_G3

P1V2_G3_INTVCC — 2.2UF C1116 1 — 2 10V
P1V2_G3_EXTVCC — R305 1 — 2 RES 0
P1V2_G3_FSWPH_CFG
P1V2_G3_FAULT_N — 97
P1V2_G3_SHARE_CLK — 97
P1V2_G3_SYNC — 97

AGND_P1V2_G3

R1397 A93548-212 22.6k 1% 0.0625W RES 0402 — AGND_P1V2_G3

+P3V3

R1399 A93548-034 10K 1% 0.0625W RES 0402
R1402 A93548-034 10K 1% 0.0625W RES 0402
R1403 A93548-202 4.99K 1% 0.0625W RES 0402

97 P1V2_G3_FAULT_N
97 P1V2_G3_SHARE_CLK
97 P1V2_G3_SYNC

ST4 EMPTY SM HC_ST — 1 2

AGND_P1V2_G3

P1V2_G3

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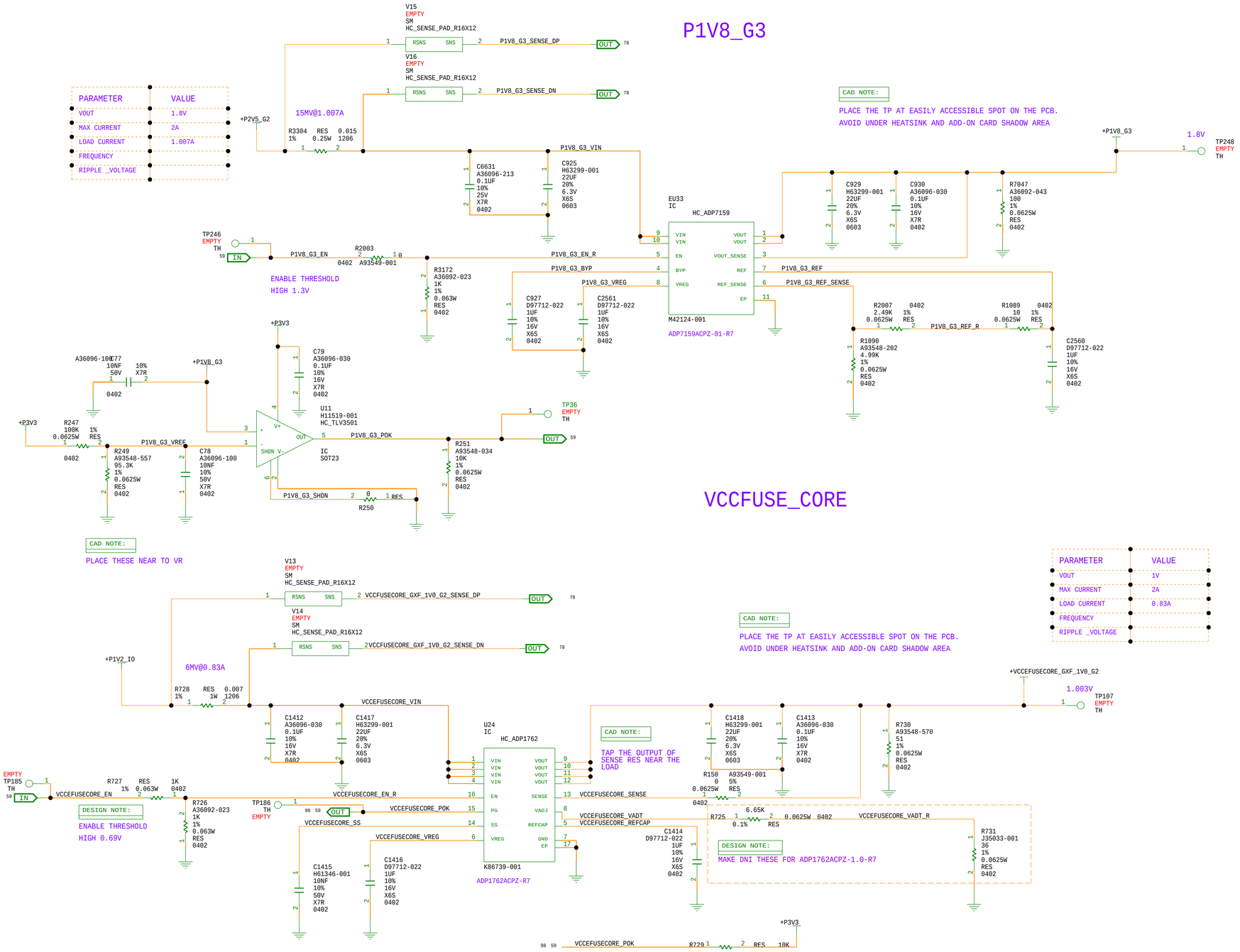
DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
UNKNOWN	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET	97 OF 105



RECOMMENDED LAYOUT GUIDELINES

Place the input capacitor as close as possible between the VIN pin and ground. Place the output capacitor as close as possible between the VOUT pin and ground. Place the bypass capacitors (C_{REG}, C_{REF}, and C_{BYP}) for V_{REG}, V_{REF}, and V_{BYP} close to the respective pins (VREG, REF, and BYP) and ground. The use of a 0805, a 0603, or a 0402 size capacitor achieves the smallest possible footprint solution on boards where area is limited. Maximize the amount of ground metal for the exposed pad, and use as many vias as possible on the component side to improve thermal dissipation.

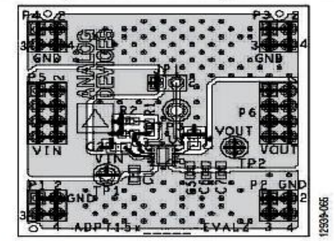


Figure 63. Sample 10-Lead LFCSP PCB Layout

RECOMMENDED LAYOUT GUIDELINES

- Place the input capacitor as close as possible to the VIN and GND pins.
- Place the output capacitor as close as possible to the VOUT and GND pins.
- Place the soft start capacitor (C_{SS}) as close as possible to the SS pin.
- Place the reference capacitor (C_{REF}) and regulator capacitor (C_{REG}) as close as possible to the REFCAP pin and the VREG pin, respectively.
- Connect the load as close as possible to the VOUT and SENSE pins.

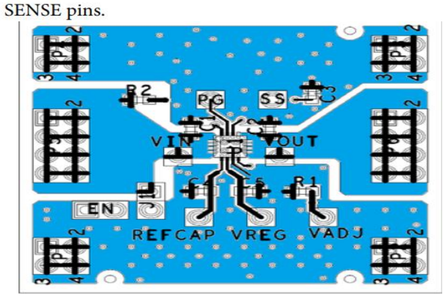


Figure 45. Typical Board Layout, Top Side

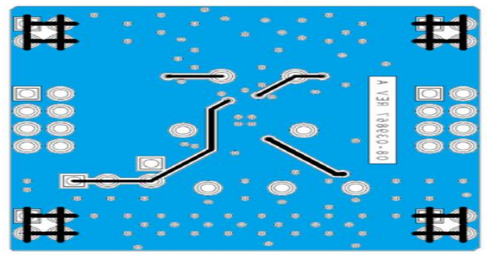


Figure 46. Typical Board Layout, Bottom Side

Tue Sep 26 11:48:19 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
UNKNOWN	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	C+	34649	150-0330690-A2	2.0
		SCALE:	DO NOT SCALE DRAWING	SHEET	98 OF 105

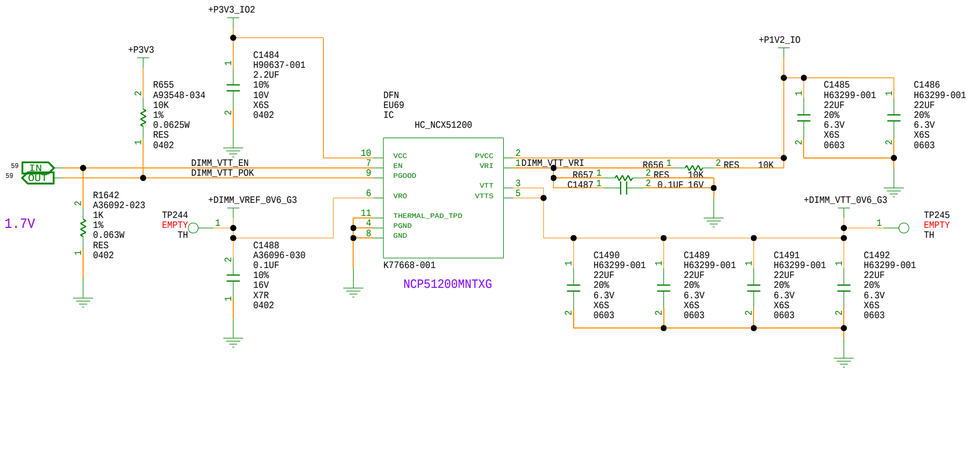
VCCFUSECORE/ P1V8_G3

VTT REGULATORS

PARAMETER	VALUE
VOUT	0.6V
MAX CURRENT	3A
LOAD CURRENT	1.1A
FREQUENCY	
RIPPLE _VOLTAGE	

DESIGN NOTE:

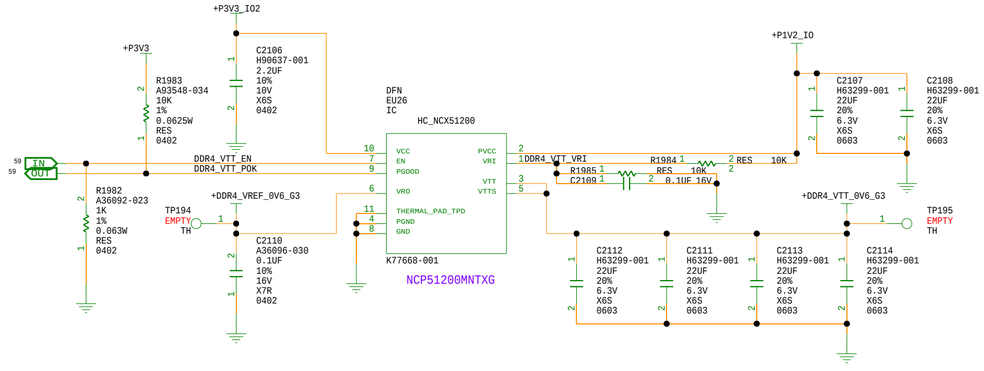
RUN threshold - 1.7V



PARAMETER	VALUE
VOUT	0.6V
MAX CURRENT	3A
LOAD CURRENT	1.5A
FREQUENCY	
RIPPLE _VOLTAGE	

DESIGN NOTE:

RUN threshold - 1.7V



Tue Sep 26 11:48:20 2023

VTT REGULATORS

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE	SCALE:	DO NOT SCALE DRAWING	SHEET	99 OF 105
	INDIA, 560103				

P3V3_IO1

PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	50A(SINGLE)
LOAD CURRENT	32.086A
FREQUENCY	750KHz
RIPPLE _VOLTAGE	10mV
PM BUS ADDRESS	7 BIT 0X4B

I2C SLAVE ADDRESS: 4BH

CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

CAD NOTE:
CONNECT NEAR FPGA BGA REGION. NEED TO ROUTE AS KELVIN SENSE

DESIGN NOTE:
RUN threshold - 1.35V

DESIGN NOTE:
VOUT CONFIG: 3.3V
VTRIM: -

NEED CONFIG
Rht0 20k
gm0: 3.69m

RECOMMENDED LAYOUT GUIDELINES

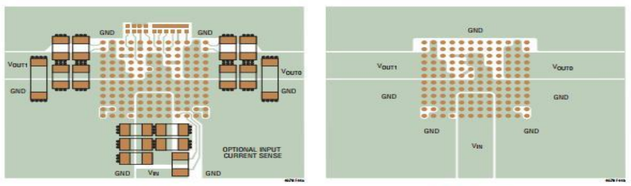
- Use large PCB copper areas for high current paths, including V_{INn}, GND and V_{OUTn}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{INn}, GND and V_{OUTn} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the module.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.

- Do not put vias directly on pads, unless they are capped or plated over.
- Use a separate SGND copper plane for components connected to signal pins. Connect SGND to GND local to the LTM4678.
- Use Kelvin sense connections across the input R_{SENSE} resistor if input current monitoring is used.

For parallel modules, tie the V_{OUTn}, V_{OSNSn}^{+}/V_{OSNSn}^{-} voltage-sense differential pair lines, RUN*n*, COMP*na*, $COMP_{nb}$ pin together.

- The user must share the SYNC, SHARE_CLK, FAULT, and $\overline{ALERT}$ pins of these parts. Be sure to use pull-up resistors on $\overline{FAULT}$, SHARE_CLK and $\overline{ALERT}$.
- Bring out test points on the signal pins for monitoring.

Figure 44 gives a good example of the recommended layout.



(a) TOP LAYER (b) BOTTOM LAYER

Figure 44. Recommended PCB Layout Package Top View

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DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	100 OF 105

P3V3_IO1

P3V3_IO2

PARAMETER	VALUE
VOUT	3.3V
MAX CURRENT	50A(SINGLE)
LOAD CURRENT	30.616A
FREQUENCY	750KHz
RIPPLE _VOLTAGE	10mV
PM BUS ADDRESS	7 BIT 0X4C

I2C SLAVE ADDRESS: 4CH

CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

CAD NOTE:
CONNECT NEAR FPGA BGA REGION. NEED TO ROUTE AS KELVIN SENSE

DESIGN NOTE:
RUN threshold - 1.35V

DESIGN NOTE:
Vout config: 3.3V
Vtrim: -

NEED CONFIG
Rht0 20k
gm0: 3.69m

RECOMMENDED LAYOUT GUIDELINES

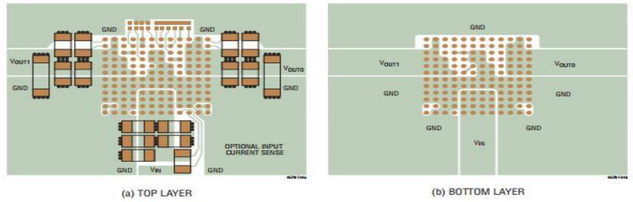
- Use large PCB copper areas for high current paths, including $V_{IN}n$, GND and $V_{OUT}n$. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the $V_{IN}n$, GND and $V_{OUT}n$ pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the module.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.

- Do not put vias directly on pads, unless they are capped or plated over.
- Use a separate SGND copper plane for components connected to signal pins. Connect SGND to GND local to the LTM4678.
- Use Kelvin sense connections across the input R_{SENSE} resistor if input current monitoring is used.

For parallel modules, tie the $V_{OUT}n$, $V_{OSNS}n^+/V_{OSNS}n^-$ voltage-sense differential pair lines, RUNn, COMPna, COMP$_{nb}$ pin together.

- The user must share the SYNC, SHARE_CLK, FAULT, and ALERT pins of these parts. Be sure to use pull-up resistors on FAULT, SHARE_CLK and ALERT.
- Bring out test points on the signal pins for monitoring.

Figure 44 gives a good example of the recommended layout.



(a) TOP LAYER (b) BOTTOM LAYER

Figure 44. Recommended PCB Layout Package Top View

Tue Sep 26 11:48:21 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	101 OF 105

P3V3_IO2

FMC PWR LOAD SWITCHES

PARAMETER	VALUE
VOUT	12V
MAX CURRENT	
LOAD CURRENT	1A
FREQUENCY	
RIPPLE _VOLTAGE	

7A CURRENT LIMIT
0.34W PDISS

+12V_AUX_2
C2605 H81594-001 1UF 10% 25V X6S 0402
R1166 RES 1% 1W 0.007 1206
Q9 M11185-002 CSD17575Q3
SM FET
~10V PGOOD THRESHOLD
+P12V0_FMC_A
TP128 EMPTY TH
C2609 G46681-001 150uF 20% 16V TANT 7343
R1284 G64084-195 93.1K 1% 0.0625W RES 0402
R1290 G21796-270 12.4K 1% 0.0625W RES 0402
102 FMC_A_FB
+P3V3
R1175 A93548-034 10K 1% 0.0625W RES 0402
FMC_A_GATE
FMC_A_SENSE
MSOP U107 IC
HC_LTC4211CMS8
VCC SENSE ON GATE TIMER FB GND RESET_N
M95393-001
TP190 EMPTY TH
59 IN
FMC_A_12V_EN
R736 RES 5% 0.0625W 0 0402
FMC_A_12V_EN_R
FMC_A_12V_TIMER
R1367 A36092-023 1K 1% 0.063W RES 0402
C2607 A36096-089 0.022UF 10% 25V X7R 0402
FMC_A_GATE_R
R1363 100 RES
FMC_A_FB
RES 0.1W 5% 5.1 0603 R1362
FMC_A_GATE_C
FMC_A_12V_POK
OUT 59
TP192 EMPTY TH
C2608 D62711-001 1NF 10% 50V X7R 0402
LTC4211CMS8#PBF

CAD NOTE:
PLACE CLOSE TO THE RESPECTIVE FMC CONNECTOR

CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

FET_PARAMETER	VALUE
VGS	±20 V
ID	60 A

DESIGN NOTE: ENABLE ON THRESHOLD 1.4V

PARAMETER	VALUE
VOUT	12V
MAX CURRENT	
LOAD CURRENT	1A
FREQUENCY	
RIPPLE _VOLTAGE	

+12V_AUX_2
C5 H81594-001 1UF 10% 25V X6S 0402
R1412 RES 1% 1W 0.007 1206
Q10 M11185-002 CSD17575Q3
FET SM
+P12V0_FMC_B
TP129 EMPTY TH
C4 G46681-001 150uF 20% 16V TANT 7343
R1296 G64084-195 93.1K 1% 0.0625W RES 0402
R1301 G21796-270 12.4K 1% 0.0625W RES 0402
102 FMC_B_FB
+P3V3
R1276 A93548-034 10K 1% 0.0625W RES 0402
FMC_B_GATE
FMC_B_SENSE
MSOP U4 IC
HC_LTC4211CMS8
VCC SENSE ON GATE TIMER FB GND RESET_N
M95393-001
TP191 EMPTY TH
59 IN
FMC_B_12V_EN
R1082 RES 5% 0.0625W 0 0402
FMC_B_12V_EN_R
FMC_B_12V_TIMER
R84 A36092-023 1K 1% 0.063W RES 0402
C206 A36096-089 0.022UF 10% 25V X7R 0402
FMC_B_GATE_R
R1170 100 RES
FMC_B_FB
R1280 0.1W 5% 5.1 0603 RES
FMC_B_GATE_C
FMC_B_12V_POK
OUT 59
TP193 EMPTY TH
C1181 D62711-001 1NF 10% 50V X7R 0402
LTC4211CMS8#PBF

CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

FET_PARAMETER	VALUE
VGS	±20 V
ID	60 A

DESIGN NOTE: ENABLE ON THRESHOLD 1.4V

CAD NOTE:
PLACE CLOSE TO THE RESPECTIVE FMC CONNECTOR

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DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
PSG	Intel Corporation	C+	34649	150-0330690-A2	2.0
	INTEL CORPORATION,BANGALORE INDIA, 560103	SCALE:	DO NOT SCALE DRAWING	SHEET	102 OF 105

QUICK DISCHARGE 1

GROUP 1

59 IN — PWR_DISCH_G1_N

R5812 10K 0.0625W 1% EMPTY 0402 — +P3V3

R5805 10K 0.0625W 1% EMPTY 0402 — PWR_DISCH_G1_N_R

C5354 A36096-100 10NF 10% 50V EMPTY 0402

+12V_AUX_1

R5802 A93548-517 4.7K 1% 0.0625W EMPTY 0402

PWR_DISCH_G1_1_INV

Q61 K21465-001 FDV305N EMPTY SOT23

R5804 A93548-517 4.7K 1% 0.0625W EMPTY 0402

R2371	A93548-031	EMPTY	VCCL_0V8_G1_DISCH_EN	
R5807	A93548-031	EMPTY	P0V8_G1_DISCH_EN	
R5808	A93548-031	EMPTY	VCC_HSSI_GXP_0V8_UX0_G1_DISCH_EN	
R5809	A93548-031	EMPTY	VCC_HSSI_GXP_0V8_UX1_G1_DISCH_EN	
R5810	A93548-031	EMPTY	VCC_HSSI_GXP_0V8_UX2_G1_DISCH_EN	
R5811	A93548-031	EMPTY	VCCERT_UX_GXF_1V0_U1x_G1_EN	
R5860	A93548-031	EMPTY	VCCERT_UX_GXF_1V0_U2x_G1_EN	
R7019	A93548-031	EMPTY	VCCRT1_FHT_GXF_1V0_UX_G1_DISCH_EN	

+VCCL_0V8_G1 — R2374 K46757-001 0.1 1% 1W EMPTY 1206 — VCCL_0V8_G1_DISCH — Q29 SI5442DU J83644-001 EMPTY

+P0V8_G1 — R5814 K46757-001 0.1 1% 1W EMPTY 1206 — P0V8_G1_DISCH — Q32 SI5442DU J83644-001 EMPTY

+VCC_HSSI_GXF_0V8_UX0_G1 — R5815 K46757-001 0.1 1% 1W EMPTY 1206 — VCC_HSSI_GXP_0V8_UX0_G1_DISCH — Q35 SI5442DU J83644-001 EMPTY

+VCC_HSSI_GXF_0V8_UX1_G1 — R5816 K46757-001 0.1 1% 1W EMPTY 1206 — VCC_HSSI_GXP_0V8_UX1_G1_DISCH — Q37 SI5442DU J83644-001 EMPTY

+VCC_HSSI_GXF_0V8_UX2_G1 — R5817 K46757-001 0.1 1% 1W EMPTY 1206 — VCC_HSSI_GXP_0V8_UX2_G1_DISCH — Q39 SI5442DU J83644-001 EMPTY

+VCCERT_UX_GXF_1V0_U1x_G1 — R5818 K46757-001 0.1 1% 1W EMPTY 1206 — VCCERT_UX_GXF_1V0_U1x_G1_DISCH — Q40 SI5442DU J83644-001 EMPTY

+VCCERT_UX_GXE_1V0_U2x_G1 — R5848 K46757-001 0.1 1% 1W EMPTY 1206 — VCCERT_UX_GXF_1V0_U2x_G1_DISCH — Q41 SI5442DU J83644-001 EMPTY

+VCCERT1_FHT_GXF_1V0_UX_G1 — R7017 K46757-001 0.1 1% 1W EMPTY 1206 — VCCRT1_FHT_GXF_1V0_UX_G1_DISCH — Q42 SI5442DU J83644-001 EMPTY

GROUP 2

59 IN — PWR_DISCH_G2_N

R2369 A93548-034 10K 0.0625W 1% EMPTY 0402 — +P3V3

R693 A93548-034 10K 0.0625W 1% EMPTY 0402 — PWR_DISCH_G2_1_N_R

C2218 A36096-100 10NF 10% 50V EMPTY 0402

+12V_AUX_1

R2370 A93548-517 4.7K 1% 0.0625W EMPTY 0402

PWR_DISCH_G2_2_INV

Q28 K21465-001 FDV305N EMPTY SOT23

R688 A93548-517 4.7K 1% 0.0625W EMPTY 0402

R708	A93548-031	EMPTY	P1V8_G2_DISCH_EN	
R711	A93548-031	EMPTY	P2V5_G2_DISCH_EN	

+P1V8_G2 — R2378 K46757-001 0.1 1% 1W EMPTY 1206 — P1V8_G2_DISCH — Q36 SI5442DU J83644-001 EMPTY

+P2V5_G2 — R2379 K46757-001 0.1 1% 1W EMPTY 1206 — P2V5_G2_DISCH — Q38 SI5442DU J83644-001 EMPTY

GROUP 3

59 IN — PWR_DISCH_G3_N

R5832 A93548-034 10K 0.0625W 1% EMPTY 0402 — +P3V3

R5835 A93548-034 10K 0.0625W 1% EMPTY 0402 — PWR_DISCH_G3_1_N_R

C5355 A36096-100 10NF 10% 50V EMPTY 0402

+12V_AUX_2

R5829 A93548-517 4.7K 1% 0.0625W EMPTY 0402

PWR_DISCH_G3_1_INV

Q77 K21465-001 FDV305N EMPTY SOT23

R5833 A93548-517 4.7K 1% 0.0625W EMPTY 0402

R5830	A93548-031	EMPTY	P3V3_IO1_DISCH_EN	
R5831	A93548-031	EMPTY	P3V3_IO2_DISCH_EN	
R2392	A93548-031	EMPTY	P12V0_FMC_A_DISCH_EN	
R2393	A93548-031	EMPTY	P12V0_FMC_B_DISCH_EN	
R2388	A93548-031	EMPTY	P1V2_G3_DISCH_EN	

+P3V3_IO1 — R5821 K46757-001 0.1 1% 1W EMPTY 1206 — P3V3_IO1_DISCH — Q31 SI5442DU J83644-001 EMPTY

+P3V3_IO2 — R5822 K46757-001 0.1 1% 1W EMPTY 1206 — P3V3_IO2_DISCH — Q33 SI5442DU J83644-001 EMPTY

+P12V0_FMC_A — R2402 K46757-001 0.1 1% 1W EMPTY 1206 — P12V0_FMC_A_DISCH — Q54 SI5442DU J83644-001 EMPTY

+P12V0_FMC_B — R2403 K46757-001 0.1 1% 1W EMPTY 1206 — P12V0_FMC_B_DISCH — Q55 SI5442DU J83644-001 EMPTY

+P1V2_G3 — R739 K46757-001 0.1 1% 1W EMPTY 1206 — P1V2_G3_DISCH — Q46 SI5442DU J83644-001 EMPTY

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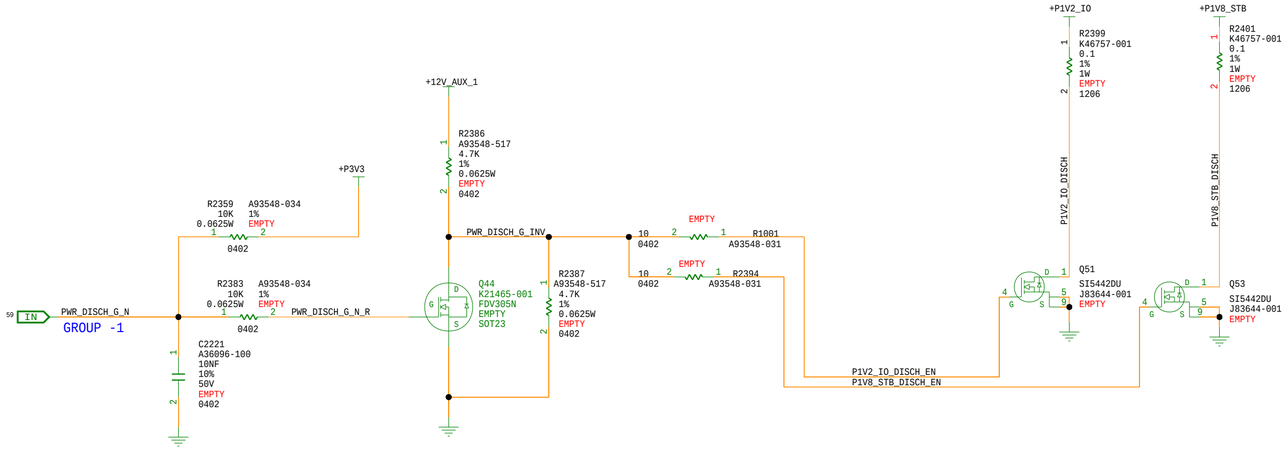
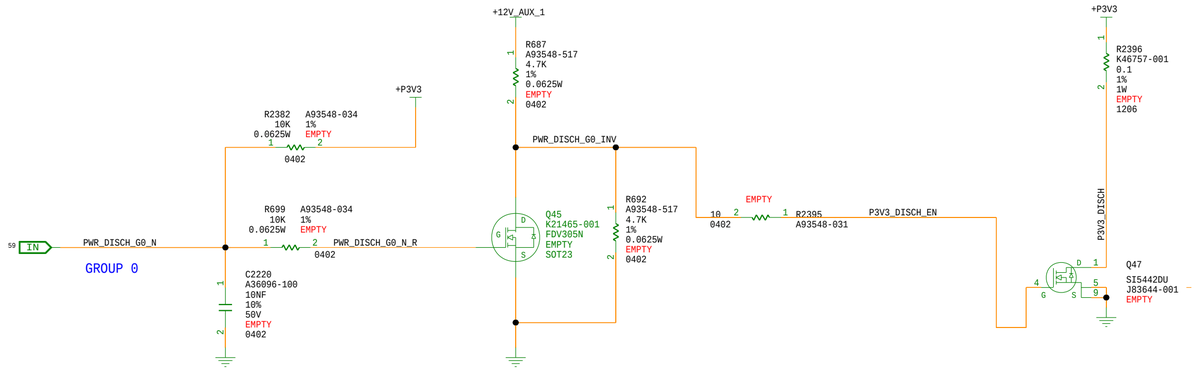
DEPARTMENT	UNKNOWN	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	
SIZE	C+	CODE	34649
DOCUMENT NUMBER	150-0330690-A2	REV	2.0
SCALE:		DO NOT SCALE DRAWING	
SHEET	103 OF 105		

QUICK DISCHARGE 1

QUICK DISCHARGE 2





Tue Sep 26 11:48:23 2023

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
UNKNOWN	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	C+	34649	150-0330690-A2	2.0
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QUICK DISCHARGE 2

REVISION _HISTORY

UPDATED ALL DESIGN CHANGES AS PER THE CHANGE LIST AFTER VALIDATION IS COMPLETED

MAJOR DESIGN CHANGES WERE LISTED BELOW FOR REFERENCE.

1) REPLACED OCXO WITH TCXO (7N19471003) AT Y7.

2) MOUNTED R1295, R1579, R1569, R1402,R573 WITH 10K RESISTOR.

3) CHANGED THE EU13 ADDRESS TO 6BH IN SCHEMATIC TEXTS & POWER TREE DOC.

4) USE THE AVAILABLE PB FOR POWER MAX10 RESET CONFIGURATION.

5) REMOVE DISCHARGE CIRCUIT FOR ALL THE GROUPS. PAGE 103 & 104 SHOULD BE REMOVED FROM SCHEMATICS.

6) REPLACE LTC7151SIV#PBF[-40C TO 125C] WITH LTC7151SEV#PBF[0C TO 85C].

7) ADDED PULL-UP TO DDR4_ALERT_N FOR DRR4 MEMORY COMPONENT.

8) UPDATED BELOW RESISTORS DNI, SINCE THOSE ARE ADDITIONAL PULL_UPS.
   R1906,R1907,R1912,R1913,R1890,R1891,R1896,R1897,R1038,R1049,R1076,R1077,R1845,R1846,R2465,R2466

9) ADDED PULL-UP TO TP_5V_POK.

10) UPDATED BELOW CAPS DNI AFTER POWER DC SIM RESULTS.
    C597,C618,C1360,C1380,C1383,C1333,C1365,C1389,C1367,C1347

11) CONNECTED THE DDR4_TEN SIGNAL DIRECTLY TO GND

12) ADDED VTT TERMINATION 36 OHM TO DDR4_A3

13) UPDTAED QSFP CAGE AND CLIP TO [U95-L111-1001 AND U9011017060BP] FOR QSFP CONNECTORS

14) CONNECTED OE PIN OF SI5395, SI5395_1_A_OEN AND SI5395_2_OEN TO SYSTEM MAX10

15) UPDATED CLOCK PROGRAMMING DESIN FOR SI5518 AND SI5395 AS BELOW
    UPDATED J31 SHOULDE BE USED FOR SI5518 SPI ONLY.
    REMOVED R2661,R2662,R3267,R3268 RESISTORS.
    CONNECTED R2661.1 TO R3267.2 ON PCB
    CONNECTED R2662.1 TO R3268.2 ON PCB
    J41 OR J140 SHOULD BE USED FOR CLK_I2C TO PROGRAM SI5391,SI5395_1)EU10),SI5395_2 (EU13).
    REMOVED R2015,R3265,R3266.
    REMOVED U150, U29 IC'S

16) ADDED DIP SWITCH FOR POWER MAX10.

17) R2626 RESISTOR IS UPDATED TO DNI.

18) R114 AND R55 RESISTORS IS UPDATED TO DNI.

Tue Aug 8 11:18:22 2023

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REVISION HISTORY