



Intel® Core™ Ultra Processor

Specification Update

*Supporting Intel® Core™ Ultra Processors for H, U, and U
Type4 Series Platforms, formerly known as Meteor Lake*

Revision 012

February 2025



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Revision History

Document Number	Revision Number	Description	Revision Date
792254	001	• Initial Revision – Includes Errata MTL001-MTL011	December 2023
	002	• Added U Type4 Series • Added Errata: MTL012 , MTL013	January 2024
	003	• Added Errata: MTL014 , MTL015 , MTL016 , MTL017 , MTL018 , MTL019	February 2024
	004	• Added Errata: MTL020 , MTL021 , MTL022 , MTL023 , MTL024 , MTL025 , MTL026 , MTL027	March 2024
	005	• Added Errata: MTL028 , MTL029 , MTL030 , MTL031	April 2024
	006	• Added Errata: MTL032 , MTL033 , MTL034 , MTL035 , MTL036	May 2024
	007	• Added Errata: MTL037 , MTL038 , MTL039 , MTL040 , MTL041 , MTL042	July 2024
	008	• Added Errata: MTL043 , MTL044 , MTL045 , MTL046 , MTL047 , MTL048 , MTL049 , MTL050	August 2024
	009	• Added Errata: MTL051 , MTL052 , MTL053 , MTL054 , MTL055 , MTL056	October 2024
	010	• Added Errata: MTL058 , MTL059	November 2024
	011	• Added Errata: MTL060 , MTL061 , MTL062	December 2024
	012	• Added Erratum: MTL063	February 2025

1 Preface

This document is an update to the specifications contained in the documents listed in the following [Affected Documents/Related Documents](#) table. It is a compilation of device and document errata and specification clarifications and changes and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this updated document and are no longer published in other documents. This document may also contain information that has not been previously published.

1.1 Affected Documents

Document Title	Document Number
Intel® Core™ Ultra Processor Datasheet, Volume 1 of 2	792044
Intel® Core™ Ultra Processors Datasheet, Volume 2 of 2	795249

1.2 Related Documents

Document Title	Document Number/Location
AP-485, Intel® Processor Identification and the CPUID Instruction	http://www.intel.com/design/processor/applnots/241618.htm
Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1: Basic Architecture Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2A: Instruction Set Reference Manual A-M Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2B: Instruction Set Reference Manual N-Z Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A: System Programming Guide Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B: System Programming Guide Intel® 64 and IA-32 Intel® Architecture Optimization Reference Manual	http://www.intel.com/products/processor/manuals/index.htm
Intel® 64 and IA-32 Architectures Software Developer's Manual Documentation Changes	http://www.intel.com/content/www/us/en/processors/architectures-software-developer-manuals.html
Intel® Virtualization Technology Specification for Directed I/O Architecture Specification	D51397-001
ACPI Specifications	www.acpi.info

1.3 Nomenclature

Errata – These are design defects or errors. Errata may cause the processor’s behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes – These are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications – These describe a specification in greater detail or further highlight a specification’s impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes – These include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Note: Errata remain in the specification update throughout the product’s lifecycle or until a stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications, and documentation changes are removed from the specification update, when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).



2 Identification Information

2.1 Component Identification via Programming Interface

The processor stepping is identified by the following register contents:

Table 2-1. Component Identification

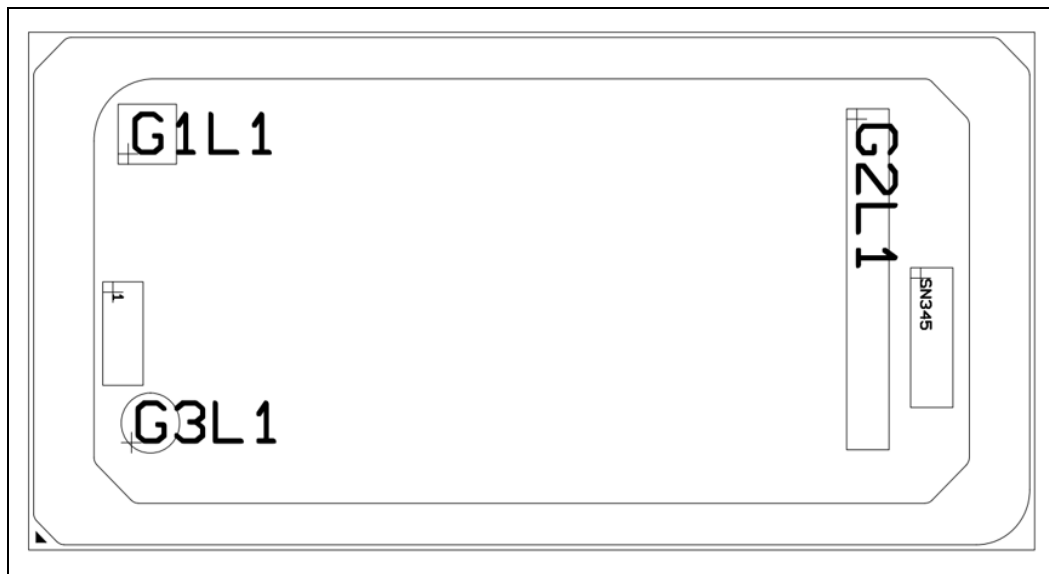
Samples	Stepping	CPUID	Reserved [31:28]	Extended Family [27:20]	Extended Model [19:16]	Reserved [15:14]	Processor Type [13:12]	Family Code [11:8]	Model Number [7:4]	Stepping ID [3:0]
MTL-H 6P+8E	C0	0xA06A4	Reserved	0000000b	1010b	Reserved	00b	0110b	1010b	0100b
MTL-U 2P+8E	C0	0xA06A4	Reserved	0000000b	1010b	Reserved	00b	0110b	1010b	0100b
MTL-U Type4 2P+8E	C0	0xA06A4	Reserved	0000000b	1010b	Reserved	00b	0110b	1010b	0100b

1. The Extended Family, Bits [27:20] are used in conjunction with the Family Code, specified in Bits[11:8], to indicate whether the processor belongs to the Celeron®, Pentium®, or Intel® Core™ processor family.
2. The Extended Model, Bits [19:16] in conjunction with the Model Number, specified in Bits [7:4], are used to identify the model of the processor within the processor’s family.
3. The Family Code corresponds to Bits [11:8] of the EDX register after RESET, Bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register accessible through Boundary Scan.
4. The Model Number corresponds to Bits [7:4] of the EDX register after RESET, Bits [7:4] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the model field of the Device ID register accessible through Boundary Scan.
5. The Stepping ID in Bits [3:0] indicates the revision number of that model. Refer table above for the processor stepping ID number in the CPUID information.
6. Refer to Processor BIOS Specification for additional information. When EAX is initialized to a value of '1', the CPUID instruction returns the Extended Family, Extended Model, Processor Type, Family Code, Model Number and Stepping ID value in the EAX register. The EDX processor signature value after reset is equivalent to the processor signature output value in the EAX register.

Cache and TLB descriptor parameters are provided in the EAX, EBX, ECX and EDX registers after the CPUID instruction is executed with a 2 in the EAX register.

2.2 Component Marking Information

Figure 2-1. H/U-Series Chip Package BGA Top-Side Markings



Pin Count: 2049

Package Size (width x height): 50 mm x 25 mm

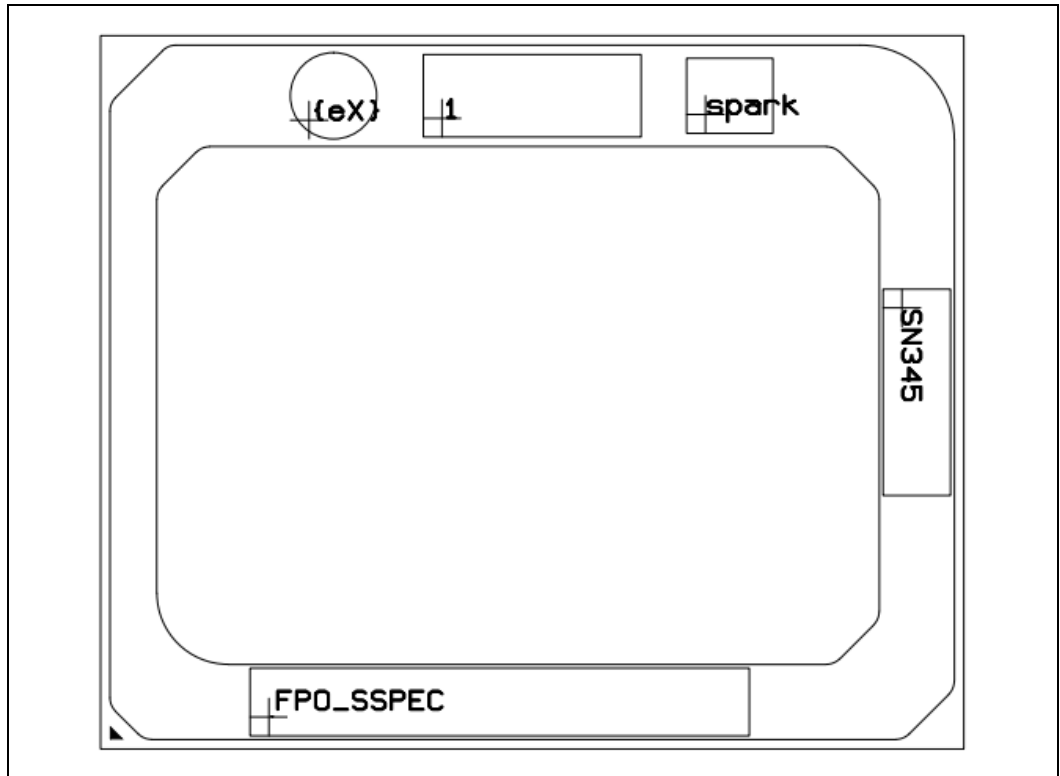
Production (SSPEC):

- SN345
- G1L1: SPARK
- G2L1: FPO_SSPEC
- G3L1: {ex}

Note: "1" is used to extract the unit visual ID (2D ID).

Identification Information

Figure 2-2. U Type4 Series Chip Package BGA Top-Side Markings



Pin Count: 2551

Package Size (width x height): 23 mm x 19 mm

Production (SSPEC):

- SN345
- SPARK
- {ex}
- FPO_SSPEC

Note: "1" is used to extract the unit visual ID (2D ID).

Note: Processor list can be found at:

<https://ark.intel.com/content/www/us/en/ark/products/series/236803/intel-core-ultra-processors-series-1.html>

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3 Summary Tables of Changes

The following tables indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes which apply to the listed processor stepping. Intel may intend to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. These tables use the following notations:

3.1 Codes Used in Summary Table

Stepping	Description
(No mark) or (Blank box)	This erratum is fixed or does not apply to the listed stepping or specification change does not apply to the listed stepping.

Status	Description
Plan Fix	This erratum may be fixed in a future hardware stepping, firmware, or software update.
Fixed	This erratum has been previously fixed in Intel hardware, firmware, or software.
No Fix	There are no plans to fix this erratum.

3.2 Errata Summary Table

Erratum ID	Processor Line			Title
	H 6P+8E	U 2P+8E	U Type4 2P+8E	
MTL001	No Fix	No Fix	No Fix	USB DbC or Device Mode Port When Resuming From S4, S5, or G3 State
MTL002	No Fix	No Fix	No Fix	xHCI USB 2.0 ISOCH Device Missed Service Interval
MTL003	No Fix	No Fix	No Fix	Intel® VT-d Remapping Hardware Does Not Perform Reserved(0) Check on PGSNP Field of Scalable-mode PASID Table Entry
MTL004	Fixed	Fixed	Fixed	HDMI Analyzer Color Corruption in HDMI2.1 YUV420
MTL005	No Fix	No Fix	No Fix	Processor C-States With USB Full-Speed or Low-Speed Device Hotplug
MTL006	No Fix	No Fix	No Fix	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
MTL007	No Fix	No Fix	No Fix	xHCI Controller Reset Due to Missing Link Credit From Device

Summary Tables of Changes

Erratum ID	Processor Line			Title
	H 6P+8E	U 2P+8E	U Type4 2P+8E	
MTL008	No Fix	No Fix	No Fix	xHCI Controller Hang With Zero-Length Data Packet
MTL009	No Fix	No Fix	No Fix	PCIe Root Port Lane Error Status Register May Not be Cleared
MTL010	No Fix	No Fix	No Fix	Type-C Display May be Blank Following S3/S4/S5 Resume
MTL011	No Fix	No Fix	No Fix	Precision Time Measurement (PTM) Interpretation Capability Bit Incorrect Register Offset
MTL012	No Fix	No Fix	No Fix	Performance Monitoring Event Branch Instruction Retired May Not Count CALLs to Next Sequential Instruction
MTL013	No Fix	No Fix	No Fix	Performance Monitoring Event Branch Instruction Retired May Overcount on Certain Types of Branch and Complex Instructions
MTL014	No Fix	N/A	N/A	PCIe Gen5 Root Ports Link Equalization Unexpected Behavior at High Temperature
MTL015	Fixed	Fixed	Fixed	Unpredictable System Behavior When SAGV is Enabled
MTL016	No Fix	No Fix	No Fix	MSI From VMD-Owned Device May Pass Memory Write
MTL017	No Fix	No Fix	No Fix	IA32_MC2_ADDR And IA32_MC2_MISC MSRs May be Cleared on Warm Reset
MTL018	No Fix	No Fix	No Fix	Performance Monitoring Events TOPDOWN.BACKEND_BOUND_SLOTS and IDQ_BUBBLES May be Inaccurate
MTL019	No Fix	No Fix	No Fix	Performance Monitoring Event IDQ.MS_UOPS May Undercount
MTL020	No Fix	No Fix	No Fix	HDMI2.1 FRL Audio Distortion With 144Hz Display With Reduced Blanking Interval
MTL021	Fixed	Fixed	Fixed	P-core Not Exiting LFM
MTL022	No Fix	No Fix	No Fix	I2S Audio Channels Swapped With High Frame Polarity in Device Mode
MTL023	No Fix	No Fix	No Fix	System May Hang When Operating at Maximum Turbo Frequency
MTL024	Fixed	Fixed	Fixed	System May Signal MCE When Operating at Maximum Single Core Turbo Frequency
MTL025	Fixed	Fixed	Fixed	Processor May Hang When Intel® HD Graphics is Disabled
MTL026	Fixed	Fixed	Fixed	Processor Power Sharing May Not Perform as Expected

Erratum ID	Processor Line			Title
	H 6P+8E	U 2P+8E	U Type4 2P+8E	
MTL027	No Fix	No Fix	No Fix	Unexpected System Behavior When Re-Enabling Intel® HT
MTL028	No Fix	No Fix	No Fix	A Write to The TSC Deadline MSR May Cause an Unexpected Timer Interrupt
MTL029	No Fix	No Fix	No Fix	Processor Trace May Generate PSB Packets Too Infrequently
MTL030	No Fix	No Fix	No Fix	Processor Trace May Not Generate a CYC Packet Before MODE.EXEC Packets
MTL031	No Fix	No Fix	No Fix	Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results
MTL032	No Fix	No Fix	No Fix	Platform May Perform a Cold Reset Rather Than a Warm Reset
MTL033	No Fix	No Fix	No Fix	Disabling The APIC While an Interrupt is Being Delivered May Cause a System Hang
MTL034	No Fix	No Fix	No Fix	Guaranteed Bandwidth Requirement For Isochronous I/O Devices May be Violated
MTL035	Fixed	Fixed	Fixed	Split Load May Return Incorrect Data
MTL036	Fixed	Fixed	Fixed	Locked Operations May Hang
MTL037	Fixed	Fixed	Fixed	RC6 Exit May Cause a System Hang
MTL038	Fixed	Fixed	Fixed	E-core May Generate Speculative Requests Beyond 4k Boundary During Short String Operations
MTL039	No Fix	No Fix	No Fix	Processor May Provide Insufficient System Agent Voltage
MTL040	Fixed	Fixed	Fixed	Lower Than Expected VCCSA and VCCGT Voltage
MTL041	Fixed	Fixed	Fixed	Audio Distortions May Occur When Using Audio APOs
MTL042	Fixed	Fixed	Fixed	RC6 Exit May Cause Machine Check Exception System Hang
MTL043	No Fix	No Fix	No Fix	Debug Exceptions May Be Lost or Misreported When MOV SS or POP SS Instruction is Not Followed By a Write to SP
MTL044	No Fix	No Fix	No Fix	Processor May Generate Malformed TLP
MTL045	No Fix	No Fix	No Fix	Intel PT Trace May Contain Incorrect Data When Configured With Single Range Output Larger Than 4KB
MTL046	No Fix	No Fix	No Fix	Setting MISC_FEATURE_CONTROL.DISABLE_THREE_STRIKE_CNT Does Not Prevent The Three-strike Counter From Incrementing

Summary Tables of Changes

Erratum ID	Processor Line			Title
	H 6P+8E	U 2P+8E	U Type4 2P+8E	
MTL047	No Fix	No Fix	No Fix	VM Exit Qualification May Not be Correctly Set on APIC Access While Serving a User Interrupt
MTL048	No Fix	No Fix	No Fix	Processor May Encrypt TME Exclude Range if Mapped to Remap Range
MTL049	No Fix	No Fix	No Fix	WRMSR to a Few Core MSRs Might be Overwritten
MTL050	No Fix	No Fix	No Fix	Single Step on Branches Might be Missed When VMM Enables Notification On VM Exit
MTL051	No Fix	No Fix	No Fix	USB 3.2 Device May Not Function as Expected With TC10 Enabled
MTL052	No Fix	No Fix	No Fix	PCONFIG Error Reporting May be Incorrect
MTL053	No Fix	No Fix	No Fix	DP Monitor May Not Operate After S4/S5 Resume
MTL054	No Fix	No Fix	No Fix	Remapping Hardware May Abort ZLR to Second-Stage Write Only Pages
MTL055	No Fix	No Fix	No Fix	xHCI Out of Order ACK Due to LCRD1
MTL056	No Fix	No Fix	No Fix	Non-Responsive USB Port After Disconnecting Full-speed Device
MTL057	N/A	N/A	N/A	N/A. Erratum has been removed.
MTL058	No Fix	No Fix	No Fix	Display Artifacts With YUV420 Format
MTL059	No Fix	No Fix	No Fix	SPI0 Dual IO Mode With SPI0 IO2 And SPI0 IO3 Connected to SPI Device
MTL060	No Fix	No Fix	No Fix	Locked Page Split Access May Not be Detected by UC-lock Disable if Split-lock Disable is Not Used
MTL061	No Fix	No Fix	No Fix	Non Canonical Fault May be Signaled on Access That Wraps Address Space When LAM is Enabled
MTL062	Fixed	Fixed	Fixed	VM Exit Following MOV to CR8 Instruction May Lead to Unexpected IDT Vectoring-Information
MTL063	No Fix	No Fix	No Fix	Cache Level Wrongly Reported in Machine Check Banks

3.3 Specification Changes

No.	Specification Changes
	None for this revision of this specification update.

3.4 Specification Clarifications

No.	Specification Clarifications
	None for this revision of this specification update.

3.5 Documentation Changes

No.	Documentation Changes
	None for this revision of this specification update.

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4 Errata Details

MTL001	USB DbC or Device Mode Port When Resuming From S4, S5, or G3 State
Problem	<p>If a processor USB Type-C* port is configured in Device Mode (or in DbC mode) and connected to an external USB 3.2 host controller, it may cause the USB port to go into a non-functional state in the following scenarios:</p> <ol style="list-style-type: none"> 1. The processor resumes from S4 or S5, the port may remain in U2. 2. The port is connected to a USB 3.2 Gen 1x1 host controller when resuming from S4, S5, or G3, the port may enter into Compliance Mode or an inactive state if Compliance Mode is disabled. 3. The port is connected to a USB 3.2 Gen 2x1 host controller when resuming from S4, S5, or G3, the port may enter an inactive state.
Implication	Due to this erratum, the processor USB Type-C port configured in Device Mode (or in DbC mode) may fail to enumerate or become unavailable.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL002	xHCI USB 2.0 ISOCH Device Missed Service Interval
Problem	When the xHCI controller is stressed with concurrent traffic across multiple USB ports, the xHCI controller may fail to service USB 2.0 Isochronous IN endpoints within the required service interval.
Implication	<p>Due to this erratum, USB 2.0 isochronous devices connected to the xHCI controller may experience dropped packets.</p> <p>NOTE: This issue has only been observed in a synthetic environment.</p>
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL003	Intel® VT-d Remapping Hardware Does Not Perform Reserved(0) Check on PGSNP Field of Scalable-mode PASID Table Entry
Problem	Intel® VT-d remapping hardware does perform Reserved(0) check on Page Snoop (PGSNP) field in scalable-mode Process Address ID (PASID) table entry when Snoop Control capability is defined as not available in the Extended Capability Register Offset 10h bit 7 (ECAP.SC=0)
Implication	There are no known functional implications due to this erratum. Intel has not observed this erratum with any commercially available software.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL004	HDMI Analyzer Color Corruption in HDMI2.1 YUV420
Problem	When in HDMI2.1 FRL YUV420 mode, and the previous frame ended with an unexpected odd line, green image corruption may occur.
Implication	Due to this erratum, when using HDMI analyzer, corruption may be observed as green color data, contained within a vertical bar on right side of the analyzer monitor. Intel has not observed and functional issue due to the Erratum.
Workaround	A workaround for this erratum is available in iGFX Driver revision 101.5005 or later.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL005	Processor C-States With USB Full-Speed or Low-Speed Device Hotplug
Problem	When doing a hotplug on a USB hub with two or more USB Full-speed or Low-speed devices each with a 1 ms service interval interrupt endpoint, a race condition may occur between the PMC and the xHCI controller.
Implication	Due to this erratum, the processor may fail to enter C3 or deeper package C-States. NOTE: This erratum has only been observed in a synthetic environment.
Workaround	None identified. This condition is recovered after the xHCI controller has successfully entered D3.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL006	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
Problem	On USB 3.2 Gen 1x1 only capable ports, including ports configured as USB 3.2 Gen 1x1 by soft strap, the xHCI controller may send only 15 LFPS signals instead of a burst of 16 LFPS signals as specified by the USB 3.2 specification.
Implication	There are no known functional implications due to this erratum. LFPS handshake requires the receiver link partner to only detect 2 LFPS signals. This issue may impact the SuperSpeed compliance test case which checks for the 16 LFPS burst requirements: TD6.4, TD6.5, and TD7.31.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL007	xHCI Controller Reset Due to Missing Link Credit From Device
Problem	The xHCI controller may not send LCRD (Link Credit) to the device after the link U0 state recovery is completed if a USB 3.2 device incorrectly stops sending LCRD.
Implication	When this erratum occurs, subsequence transfers from the device may not be completed and the xHCI host controller driver may initiate a host controller reset.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

Errata Details

MTL008	xHCI Controller Hang With Zero-Length Data Packet
Problem	The xHCI controller may fail to handle a zero-length data packet when doing concurrent traffic with the following devices connected on three separate root ports: <ul style="list-style-type: none"> • USB 3.2 Gen 2x1 (or 2x2) hub with at least two USB 3.2 bulk devices. • USB 3.2 Gen 2x1 (or 2x2) hub with at least two USB 3.2 bulk devices. • USB isochronous device that sends zero-length data packets.
Implication	Due to this erratum, the xHCI controller may hang. Intel has only observed this behavior with USB audio offload enabled and USB 2.0 audio devices that send zero-length data packets.
Workaround	None identified. A mitigation for USB 2.0 audio devices using USB audio offload is available in Intel® Smart Sound Technology driver version 20.40.9509.0 or later.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL009	PCIe Root Port Lane Error Status Register May Not be Cleared
Problem	Re-enabling a port following a link disable or hot reset the PCIe Lane Error Status register (Offset 0xA38) may not be cleared.
Implication	Due to this erratum, the Lane Error Status register may indicate lane errors on some of the Root Ports. Intel has not observed any functional issues due this erratum.
Workaround	None identified. Software should ignore the lane error status register to mitigate this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL010	Type-C Display May be Blank Following S3/S4/S5 Resume
Problem	When switching between Type-C Display Alt Mode and an Multi-Function Device (MFD) while the system is in S3/S4/S5, the Display may not enumerate.
Implication	When this erratum occurs the Display may be blank. A device unplug and re-plug may be necessary to recover the display.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL011	Precision Time Measurement (PTM) Interpretation Capability Bit Incorrect Register Offset
Problem	The PTM Propagation Delay Adaptation Interpretation B (PTMPDAIB) Bit is implemented at Configuration Space (CFG) Offset 158h instead of at 50h as documented in the PCI-SIG PTM Byte Ordering Adaptation Engineering Change Notice (ECN).
Implication	Due to this erratum, End Point Device (EPD) software that implements the PTM Byte Ordering Adaptation ECN may not be able to program their PTMPDAIB Bit correctly since it is located at a different register offset.
Workaround	None identified. To mitigate this issue, EPD software that implements the PTM Byte Ordering Adaptation ECN must access PTMPDAIB at CFG Offset 158h.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL012	Performance Monitoring Event Branch Instruction Retired May Not Count CALLs to Next Sequential Instruction
Problem	A CALL instruction whose target is the next sequential instruction (the same address pushed onto the stack) may not increment the performance monitoring event BR_INST_RETIRED (Event: C4H, UMask: 00H, F9H).
Implication	Due to this erratum, software monitoring Branch Instruction Retired events may undercount. Since the CALL is to the next instruction, control flow tracing with the Last Branch Retired (LBR) records should not be affected.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL013	Performance Monitoring Event Branch Instruction Retired May Overcount on Certain Types of Branch and Complex Instructions
Problem	On certain types of branch and complex instructions the performance monitoring event BR_INST_RETIRED (Event: C4H, UMask: 00H / 7EH / BFH / C0H / DFH / EBH / FBH / F9H) may overcount by 1. Affected instructions include FAR CALL/JMP, RETF, IRET, VMENTRY/VMEXIT/VMPTRLD and complex SGX/SMX/CSTATE instructions/flows.
Implication	Due to this erratum, software monitoring Branch Instruction Retired events may overcount.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL014	PCIe Gen5 Root Ports Link Equalization Unexpected Behavior at High Temperature
Problem	PCIe Lanes 21 through 28 may fail Gen5 link equalization at high temperatures due to complex lane microarchitectural conditions.
Implication	Due to this erratum, the associated PCIe Gen5 link may exhibit link errors, hang, or fail compliance tests. No issues have been observed when the PCIe link attempts Gen4 or lower.
Workaround	It is possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL015	Unpredictable System Behavior When SAGV is Enabled
Problem	On platforms that enable System Agent Geyserville (SAGV), a technology that allows load-specific memory speeds, the processor may exhibit unpredictable system behavior.
Implication	When this erratum occurs, the processor exhibits unpredictable system behavior.
Workaround	It is possible for BIOS to work around this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

Errata Details

MTL016	MSI From VMD-Owned Device May Pass Memory Write
Problem	When the storage subsystem is configured to operate in RAID 0 or 1 mode, a Message Signaled Interrupt (MSI) from an Intel® Volume Management Device (Intel® VMD) owned device may interrupt a core before a previous write from the device is completed.
Implication	Due to this erratum, the platform may experience unpredictable system behavior.
Workaround	None identified. The VMD MSI interrupt-handler should initially perform a dummy register read to the MSI initiator device prior to any writes to ensure proper PCIe ordering.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL017	IA32_MC2_ADDR And IA32_MC2_MISC MSRs May be Cleared on Warm Reset
Problem	A non-zero value written to IA32_MC2_ADDR (40Ah) and IA32_MC2_MISC(40Bh) MSRs may be incorrectly cleared following a warm reset.
Implication	Due to this erratum, software that relies on the IA32_MC2_ADDR and IA32_MC2_MISC MSR values may not function correctly after a warm reset. Intel has not observed this erratum with any commercially available software.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL018	Performance Monitoring Events TOPDOWN.BACKEND_BOUND_SLOTS and IDQ_BUBBLES May be Inaccurate
Problem	The performance monitoring events TOPDOWN.BACKEND_BOUND_SLOTS (Event A4h, UMask 02h) and IDQ_BUBBLES.* (Event 9Ch, UMask 01h) may not count when the processor is in the C0.2 power sub-state, which is entered via the TPAUSE or UWAIT instructions. This erratum also impacts the accuracy of MSR_PERF_METRICS fields Frontend Bound, Backend Bound, and Fetch Latency (MSR 329h, Bits [23:16], [31:24] and [55:48]).
Implication	Due to this erratum, these performance monitoring events and the fields in MSR_PERF_METRICS may be inaccurate.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL019	Performance Monitoring Event IDQ.MS_UOPS May Undercount
Problem	The performance monitoring events IDQ.MS_UOPS, IDQ.MS_SWITCHES, and IDQ.MS_CYCLES_ANY (Event 79h, UMask 30h) may undercount MS_UOPS that come from the Decode Stream Buffer (DSB).
Implication	Due to this erratum, performance monitoring counters may report counts lower than expected.
Workaround	None identified. Performance monitoring event UOPS_RETIRED.MS may be used instead.

MTL019	Performance Monitoring Event IDQ.MS_UOPS May Undercount
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL020	HDMI2.1 FRL Audio Distortion With 144Hz Display With Reduced Blanking Interval
Problem	The processor may not have sufficient display bandwidth to support display audio when using HDMI2.1 FRL (Fixed Rate Link) with a 144Hz display with reduced blanking interval.
Implication	Due to this erratum, intermittent or complete loss of audio may occur.
Workaround	A mitigation has been identified for this erratum and may be available in a software update.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL021	P-core Not Exiting LFM
Problem	P-core frequency may not be updated after resuming from PKG C6.
Implication	Due to this erratum, P-core may unexpectedly remain in Low Frequency Mode (LFM).
Workaround	A BIOS code change has been identified and may be implemented as a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL022	I2S Audio Channels Swapped With High Frame Polarity in Device Mode
Problem	When the I2S interface is in device mode, the audio controller may not be correctly configured if the audio codec requires high frame polarity.
Implication	Due to this erratum, the left and right audio channels may swap when frame polarity is set to high.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL023	System May Hang When Operating at Maximum Turbo Frequency
Problem	The processor may fail to correctly thermally throttle when running at maximum turbo frequency.
Implication	Due to this erratum, the system may hang with an Internal Timeout Error Machine Check (IA32_MCI_STATUS.MSCOD=080h and IA32_MCI_STATUS.MCACOD=0400h) or unpredictable system behavior may occur.
Workaround	None identified. It may be possible for BIOS to contain a mitigation for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

Errata Details

MTL024	System May Signal MCE When Operating at Maximum Single Core Turbo Frequency
Problem	DCU DCACHEL0_EVICT_ERR (MSCOD=0100h and MCACOD=0174h) may be observed when the core frequency is operating at Maximum Single Core Turbo Frequency.
Implication	Due to this erratum, the system may signal a fatal DCACHEL0_EVICT_ERR machine check exception.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL025	Processor May Hang When Intel® HD Graphics is Disabled
Problem	If internal graphics is disabled (Bus 0, Device 2, Function 0) when using a discrete graphics solution, the processor may fail to exit Package C6 state and report a machine check exception with an MCACOD=0402H and MSCOD=0823H.
Implication	Due to this erratum, the processor may hang with a machine check exception.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL026	Processor Power Sharing May Not Perform as Expected
Problem	The processor exposes certain power sharing capabilities via the Intel Performance Framework. However, the processor may not honor power sharing requests made via SET_PERF_PREFERENCE_MIN and SET_PERF_PREFERENCE_MAX.
Implication	Due to this erratum, software may not achieve its expected processor power allocation.
Workaround	It is possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL027	Unexpected System Behavior When Re-Enabling Intel® HT
Problem	When performing a warm reset as part of enabling of Intel® Hyper-Threading, machine check banks may not be initialized correctly.
Implication	Due to this erratum, software that relies on initialized values in machine check banks may not behave as expected.
Workaround	None identified. Software or BIOS can avoid this erratum by performing cold reset when re-enabling Intel® HT.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL028	A Write to The TSC_Deadline MSR May Cause an Unexpected Timer Interrupt
Problem	Under complex micro-architectural conditions, writing a non-zero value to the Time-Stamp Counter (TSC) Deadline counter, IA32-TSC_DEADLINE MSR (6E0h), may cause timer interrupt following the write.
Implication	Due to this erratum, a unexpected timer interrupt may be signaled.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL029	Processor Trace May Generate PSB Packets Too Infrequently
Problem	A Packet Stream Boundary (PSB) packet should be generated for every PSBFreq number of trace output bytes. Due to this erratum, PSB packets may be generated only after as many as four times that number of output bytes have been generated.
Implication	Due to this erratum, trace decoder software may see fewer PSB packets than expected. This may lead to the trace decoder software needing to search further to find a starting point to decode or, when used in circular mode, being unable to decode the trace due to lacking any PSB packets.
Workaround	None identified. Software can request more frequent PSB packets by programming PSBFreq (bits[27:24]) of IA32_RTIT_CTL MSR (570H) to a value 1/4 of the desired value.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL030	Processor Trace May Not Generate a CYC Packet Before MODE.EXEC Packets
Problem	When a Processor Trace MODE.EXEC packet is generated due to a change in RFLAGS.IF (interrupt flag) or the CS.L or CS.D bits, the processor may not generate a CYC packet before generating the MODE.EXEC packet.
Implication	Due to this erratum, trace decoder software may not be able to precisely determine when mode changes that involve changing the interrupt flag or the application's default operand size happened.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL031	Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results
Problem	The act of one processor or system bus master writing data into a currently executing code segment of a second processor with the intent of having the second processor execute that data as code is called cross-modifying code (XMC). XMC that does not force the second processor to execute a synchronizing instruction prior to execution of the new code is called unsynchronized XMC. Software using unsynchronized XMC to modify the instruction byte stream of a processor can see unexpected or unpredictable execution behavior from the processor that is executing the modified code.

MTL031	Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results
Implication	In this case the phrase "unexpected or unpredictable execution behavior" encompasses the generation of most of the exceptions listed in the Intel Architecture Software Developer's Manual Volume 3: System Programming Guide including a General Protection Fault (GPF) or other unexpected behaviors. In the event that unpredictable execution causes a GPF the application executing the unsynchronized XMC operation would be terminated by the operating system.
Workaround	In order to avoid this erratum programmers should use the XMC synchronization algorithm as detailed in the Intel Architecture Software Developer's Manual Volume 3: System Programming Guide Section: Handling Self- and Cross-Modifying Code.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL032	Platform May Perform a Cold Reset Rather Than a Warm Reset
Problem	Under complex microarchitectural conditions, if a warm reset event occurs when an Address Translation invalidation transaction is in progress, the processor may perform a cold reset.
Implication	Due to this erratum, the platform may perform a cold reset, rather than a warm reset. Intel has only observed this behavior in a synthetic test environment.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL033	Disabling The APIC While an Interrupt is Being Delivered May Cause a System Hang
Problem	If software disables the APIC by clearing APIC global enable flag (bit 11) in IA32_APIC_BASE (MSR 1Bh) while an interrupt is being delivered, the system may hang with a machine check exception reported in IA32_MCi_STATUS, with MCACOD (bits [15:0]) value of 0400H, and MSCOD (bits [31:16]) value of 0080H.
Implication	Due to this erratum, the system may hang. Intel has not observed this erratum in any commercial available software.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL034	Guaranteed Bandwidth Requirement For Isochronous I/O Devices May be Violated
Problem	Longer exit C-State latency associated with SVID slew rate Fast/8 is not accounted for when handling Latency Tolerance Reporting (LTR) thresholds for processor Die/Pkg C-States.
Implication	Due to this erratum, the guaranteed bandwidth requirement for isochronous I/O devices may be violated.
Workaround	It may be possible for the BIOS to contain a mitigation for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL035	Split Load May Return Incorrect Data
Problem	Under complex microarchitectural conditions, a cache line split load may return incorrect data.
Implication	Due to this erratum, split loads may return incorrect data, which may lead to unpredictable system behavior. Intel has only observed this erratum in a synthetic test environment.
Workaround	It may be possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL036	Locked Operations May Hang
Problem	Under complex microarchitectural conditions, a locked operation, including instructions that use the LOCK prefix, may hang the system.
Implication	The processor may hang with a Internal Timeout Error Machine Check exception (IA32_MCi_STATUS.MCACOD = 0400h). Intel has only observed this erratum in a synthetic test environment.
Workaround	It may be possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL037	RC6 Exit May Cause a System Hang
Problem	During boot, the initial RC6 exit may cause a system hang.
Implication	Due to this erratum, the processor may hang with a machine check exception with IA32_MCi_STATUS.MSCOD=0x0096 and IA32_MCi_STATUS.MCACOD=0402h.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL038	E-core May Generate Speculative Requests Beyond 4k Boundary During Short String Operations
Problem	During short string operations, it is possible for the E-core to speculatively access addresses beyond the current 4K page boundary, including pages that may be mapped as UnCachable (UC).
Implication	Due to this erratum, it is possible to speculatively access MMIO space, which may lead to unpredictable system behavior, including IO device malfunction.
Workaround	It is possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

Errata Details

MTL039	Processor May Provide Insufficient System Agent Voltage
Problem	When operating at maximum bandwidth and lowest latency memory conditions (e.g., when SAGV is configured in a Gear 2 mode), the processor may not provide the necessary voltage to the System Agent devices supplied by the VccSA voltage rail.
Implication	Due to this erratum, System Agent devices supplied by the VccSA rail may be operate at insufficient voltage, which may lead to unpredictable system behavior.
Workaround	None identified. It is possible for BIOS to contain a mitigation for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL040	Lower Than Expected VCCSA and VCCGT Voltage
Problem	The processor may incorrectly limit the VCCSA and VCCGT rail voltage.
Implication	Due to this erratum, the system may exhibit unpredictable behavior.
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL041	Audio Distortions May Occur When Using Audio APOs
Problem	The processor may not meet package Cstate exit latency requirements when processing offline Audio Processing Objects (APOs).
Implication	Due to this erratum, intermediate audio distortions may occur.
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL042	RC6 Exit May Cause Machine Check Exception System Hang
Problem	RC6 exit request may not complete when processor is in Package C-state C0.
Implication	Due to this erratum, the processor may hang with a GPSB_MESSAGE_CHANNEL_TIMEOUT machine check exception (MCACOD=0414h, MSCOD=0080h).
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL043	Debug Exceptions May Be Lost or Misreported When MOV SS or POP SS Instruction is Not Followed By a Write to SP
Problem	If a MOV SS or POP SS instruction generated a debug exception, and is not followed by an explicit write to the stack pointer (SP), the processor may fail to deliver the debug exception or, if it does, the DR6 register contents may not correctly reflect the causes of the debug exception.

MTL043	Debug Exceptions May Be Lost or Misreported When MOV SS or POP SS Instruction is Not Followed By a Write to SP
Implication	Debugging software may fail to operate properly if a debug exception is lost or does not report complete information. Intel has not observed this erratum with any commercially available software.
Workaround	Software should explicitly write to the stack pointer immediately after executing MOV SS or POP SS.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL044	Processor May Generate Malformed TLP
Problem	If the processor root port receives an FetchAdd, Swap, or CAS TLP (an atomic operation) that is erroneous, it should generate a UR completion to the downstream requestor. If the TLP has an operand size greater than 4 bytes, the generated UR completion will report an operand size of 4 bytes, which will be interpreted as a malformed transaction.
Implication	When this erratum occurs, the processor may respond with a malformed transaction.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL045	Intel PT Trace May Contain Incorrect Data When Configured With Single Range Output Larger Than 4KB
Problem	Under complex micro-architectural conditions, when using Intel(r) Processor Trace (PT) with single range output larger than 4KB, disabling PT and then enabling PT using the TraceEn bit in IA32_RTIT_CTL MSR (MSR 570h, bit 0) may cause incorrect output values to be recorded.
Implication	Due to this erratum, a PT trace may contain incorrect values.
Workaround	None identified. Software should avoid using PT with single range output larger than 4KB.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL046	Setting MISC_FEATURE_CONTROL.DISABLE_THREE_STRIKE_CNT Does Not Prevent The Three-strike Counter From Incrementing
Problem	Setting MISC_FEATURE_CONTROL.DISABLE_THREE_STRIKE_CNT (bit 11 in MSR 1A4h) does not prevent the three-strike counter from incrementing as documented; instead, it only prevents the signaling of the three-strike event once the counter has expired.
Implication	Due to this erratum, software may be able to see the three-strike logged in the MC3_STATUS (MSR 40Dh, MCACOD = 400h [bits 15:0]) even when MISC_FEATURE_CONTROL.DISABLE_THREE_STRIKE_CNT is set.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL047	VM Exit Qualification May Not be Correctly Set on APIC Access While Serving a User Interrupt
Problem	A VM Exit that occurs while the processor is serving a user interrupt in non-root mode should set the “asynchronous to instruction execution” bit in the Exit Qualification field in the Virtual Machine Control Structure (bit 16). However, if a VM Exit occurs during processing a user interrupt due to an APIC access, the bit will not be set.
Implication	Due to this erratum, the “asynchronous to instruction execution” bit will not be set if an APIC Access VM Exit occurs while the processor is serving a user interrupt. Intel has not observed this erratum with any commercially available software.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL048	Processor May Encrypt TME Exclude Range if Mapped to Remap Range
Problem	The processor accesses to TME exclude range may be encrypted but not decrypted if mapped to remap range.
Implication	Due to this erratum, the processor exclude range it will be encrypted but will but not decrypted if mapped to remap range.
Workaround	It may be possible for BIOS to workaround this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL049	WRMSR to a Few Core MSRs Might be Overwritten
Problem	If any thread is in thread C6 while another thread is updating one of the following MSRs, a subsequent transition from single thread operation to multi-thread operation or vice versa might cause that MSR to revert to its previous value. The affected MSRs are: MEMORY_CONTROL (MSR 33h bit 28), QUIESCE_CTL1 (MSR 50h) and QUIESCE_CTL2 (MSR 51h).
Implication	Due to this erratum, the values of the above MSRs may be incorrect. Intel has not observed any functional impact due to this erratum.
Workaround	None identified. Software must ensure that the other thread is not in TC6 when writing this MSR.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL050	Single Step on Branches Might be Missed When VMM Enables Notification On VM Exit
Problem	Under complex micro-architectural conditions, single step on branches (IA32_DEBUGGTLMSR (Offset 1D9h, bit [1]) and also TF flag in EFLAGS register is set) in guest might be missed when VMM enables notification on VM Exit (IA32_VMX_PROCBASED_CTL2 MSR, Offset 48Bh, bit [31]) while the dirty access bit is not set for the code page (bit [6] in paging-structure entry).
Implication	When single step is enabled under the above condition, some single step branches will be missed. Intel has only observed this erratum in a synthetic test environment.

MTL050	Single Step on Branches Might be Missed When VMM Enables Notification On VM Exit
Workaround	When enabling single step on branches for debugging, software should first set the dirty bit of the code page.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL051	USB 3.2 Device May Not Function as Expected With TC10 Enabled
Problem	When TC10 is enabled, a USB 3.2 device connected to USB Type-C port directly without retimer may not function as expected.
Implication	Due to this erratum, a USB 3.2 device may not function as expected.
Workaround	None identified. It may be possible for the BIOS to contain a mitigation for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL052	PCONFIG Error Reporting May be Incorrect
Problem	If invalid parameters are provided, the PCONFIG instruction should generate a #GP exception. Due to this erratum, the processor may instead set a ZF flag, with EAX reporting failure reasons.
Implication	Due to this erratum, incorrectly configured PCONFIG usage may lead to unexpected error reporting.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL053	DP Monitor May Not Operate After S4/S5 Resume
Problem	When switching a USB Type-C Display Port (DP) monitor connection between Alt Mode and MFD in S4/S5, the monitor may not be enumerated when resuming from S4/S5.
Implication	Due to this erratum, a DP Monitor may not operate when resuming from S4/S5 and may require a hot plug to recover.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL054	Remapping Hardware May Abort ZLR to Second-Stage Write Only Pages
Problem	Remapping hardware will report non-recoverable VT-d fault and cause the Zero-Length-Read (ZLR) to be aborted, if a ZLR encounters read-only page in first-stage tables and write-only page in second-stage tables.
Implication	Due to this erratum, device may observe an unexpected abort on a ZLR and a VT-d fault may be indicated. Intel has not observed this erratum with any commercially available software.

Errata Details

MTL054	Remapping Hardware May Abort ZLR to Second-Stage Write Only Pages
Workaround	None identified. System software should not create write only pages in second-stage page tables.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL055	xHCI Out of Order ACK Due to LCRD1
Problem	A delay in the availability of LCRD1 (Link Credit 1) from a USB 3.2 hub, with two or more downstream USB 3.2 bulk endpoint devices engaged in SuperSpeedPlus concurrent transfers, may lead to the connected xHCI controller sending the ACK and Status of a transfer packet out of order.
Implication	Due to this erratum, a USB 3.2 bulk endpoint device may not respond to subsequent transfers. It may be possible for a device driver to recover the USB 3.2 device.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL056	Non-Responsive USB Port After Disconnecting Full-speed Device
Problem	Disconnecting a USB full-speed device from the USB port while the xHCI controller is in the process of sending the Start of Frame may cause the USB 2.0 functionality to become unresponsive for that specific port.
Implication	Due to this erratum, USB 2.0 devices may not be recognized on the USB port until a host controller reset occurs. Intel has only observed this behavior in a synthetic test environment.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL057	N/A. Erratum has been removed.
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MTL058	Display Artifacts With YUV420 Format
Problem	While in DP2.1 UHBR mode and using the YUV420 format with scaling, displays with a resolution higher than 5K @ 60Hz may show display artifacts.
Implication	Due to this erratum, display artifacts may be seen.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL059	SPI0 Dual IO Mode With SPI0_IO2 And SPI0_IO3 Connected to SPI Device
Problem	On systems with dual IO mode enabled, SPI0_IO2 and SPI0_IO3 may momentarily drive low before these signals are pulled high by internal resistors during boot from the G3 state.
Implication	Due to this erratum, unexpected system behavior may occur on systems when SPI0_IO2 and SPI0_IO3 signals are connected to an SPI device.
Workaround	None identified. To mitigate this erratum, do not connect SPI0_IO2 and SPI0_IO3 to an SPI device in SPI0 dual IO mode enabled systems.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL060	Locked Page Split Access May Not be Detected by UC-lock Disable if Split-lock Disable is Not Used
Problem	The UC-lock disable feature (MSR_MEMORY_CTRL bit [28] (MSR 33h)) may not cause a fault (#AC(4)) for a page split lock that accesses a page with non-WB memory type if the split lock disable (MSR_MEMORY_CTRL bit [29]) is not set.
Implication	Due to this erratum, system software may not be able to fully prevent bus locks due to locks to non-WB memory unless they use the split-lock disable feature to prevent bus locks due to splits. Intel has not observed this erratum with any commercially available software.
Workaround	None identified. Software using the UC-lock disable feature should also enable the split lock disable feature.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL061	Non Canonical Fault May be Signaled on Access That Wraps Address Space When LAM is Enabled
Problem	When Linear Address Masking (LAM) is enabled, a non-canonical fault may be signaled if there is an access which splits the 64-bit linear address space (and thus touches both linear address FFFF_FFFF_FFFF_FFFFh and 0h).
Implication	Due to this erratum, software may receive an unexpected exception on such accesses. Intel has not observed this erratum with any commercially available software.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL062	VM Exit Following MOV to CR8 Instruction May Lead to Unexpected IDT Vectoring-Information
Problem	Under certain conditions, a VM exit following execution of the MOV to CR8 instruction may unexpectedly result in setting the Valid bit (bit 31) of the IDT-Vectoring Information Field in the Virtual Machine Control Structure (VMCS).
Implication	Depending on the operation of the virtual-machine monitor (VMM), this may result in unexpected VM behavior.
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.

Errata Details

MTL062	VM Exit Following MOV to CR8 Instruction May Lead to Unexpected IDT Vectoring-Information
Status	For the steppings affected, refer to the Summary Table of Changes .

MTL063	Cache Level Wrongly Reported in Machine Check Banks
Problem	When reporting a machine check in the module level caches (IA32_MC1_STATUS, MSR 405H), a Compound Error Code of type Cache Hierarchy Error will be reported with a Level (LL) Sub-field of 0b10[L2] instead of 0b01[L1].
Implication	Due to this erratum, system software relying on this data, may wrongly categorize the cache level in which the error was reported. The severity of the error will be reported accurately.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

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5 Specification Changes

None.

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6 ***Specification Clarification***

None.

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7 Document Change

None.

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