Intel® Core™ Ultra Processor

Specification Update

Supporting Intel® Core™ Ultra Processors for H, U, and U Type4 Series Platforms, formerly known as Meteor Lake

Revision 005

April 2024

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Revision History

Revision Number	Description	Revision Date
001	• Initial Revision – Includes Errata MTL001-MTL011	December 2023
002	• Added U Type4 Series • Added Errata: MTL012, MTL013	January 2024
003	• Added Errata: MTL014, MTL015, MTL016, MTL017, MTL018, MTL019	February 2024
004	• Added Errata: MTL020, MTL021, MTL022, MTL023, MTL024, MTL025, MTL026, MTL027	March 2024
005	• Added Errata: MTL028, MTL029, MTL030, MTL031	April 2024

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1 Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this updated document and are no longer published in other documents. This document may also contain information that has not been previously published.

1.1 Affected Documents

Document Title	Document Number
Intel® Core™ Ultra Processor Datasheet, Volume 1 of 2	792044
Intel® Core™ Ultra Processors Datasheet, Volume 2 of 2	795249

1.2 Related Documents

Document Title	Document Number/Location
AP-485, Intel® Processor Identification and the CPUID Instruction	http://www.intel.com/design/processor/applnots/241618.htm
Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1: Basic Architecture Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2A: Instruction Set Reference Manual A-M Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2B: Instruction Set Reference Manual N-Z Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A: System Programming Guide Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B: System Programming Guide Intel® 64 and IA-32 Intel® Architecture Optimization Reference Manual	http://www.intel.com/products/processor/manuals/index.htm
Intel® 64 and IA-32 Architectures Software Developer's Manual Documentation Changes	http://www.intel.com/content/www/us/en/processors/architectures-software-developer-manuals.html
Intel® Virtualization Technology Specification for Directed I/O Architecture Specification	D51397-001
ACPI Specifications	www.acpi.info

1.3 Nomenclature

Errata – These are design defects or errors. Errata may cause the processor's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes – These are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications – These describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes – These include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Note: Errata remain in the specification update throughout the product's lifecycle or until a stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications, and documentation changes are removed from the specification update, when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

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2 Identification Information

2.1 Component Identification via Programming Interface

The processor stepping is identified by the following register contents:

Table 1. Component Identification

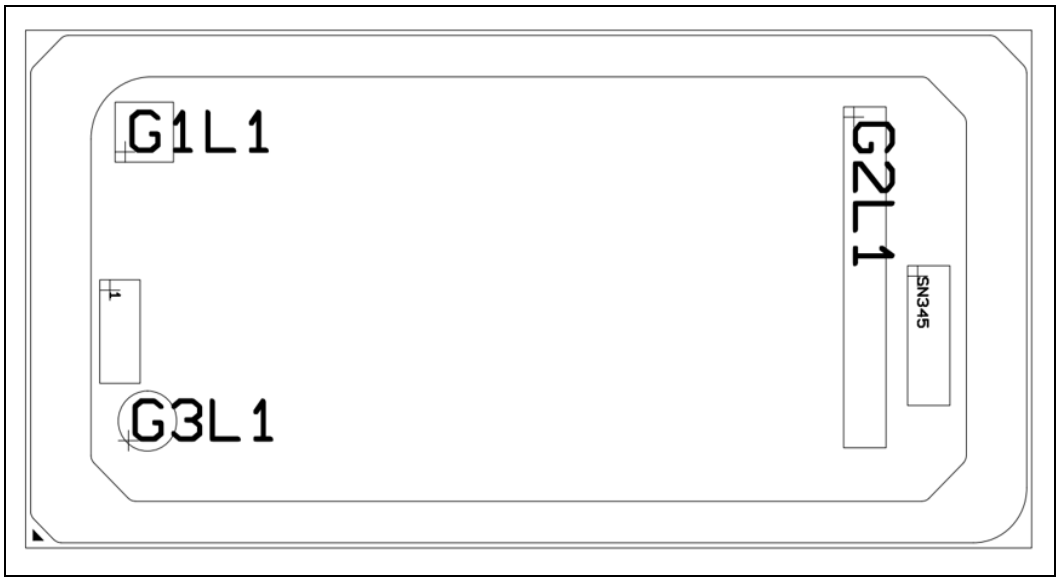
Samples	Stepping	CPUID	Reserved [31:28]	Extended Family [27:20]	Extended Model [19:16]	Reserved [15:14]	Processor Type [13:12]	Family Code [11:8]	Model Number [7:4]	Stepping ID [3:0]
MTL-H 6P+8E	C0	0xA06A4	Reserved	0000000b	1010b	Reserved	00b	0110b	1010b	0100b
MTL-U 2P+8E	C0	0xA06A4	Reserved	0000000b	1010b	Reserved	00b	0110b	1010b	0100b
MTL-U Type4 2P+8E	C0	0xA06A4	Reserved	0000000b	1010b	Reserved	00b	0110b	1010b	0100b

1. The Extended Family, Bits [27:20] are used in conjunction with the Family Code, specified in Bits[11:8], to indicate whether the processor belongs to the Celeron®, Pentium®, or Intel® Core™ processor family.
2. The Extended Model, Bits [19:16] in conjunction with the Model Number, specified in Bits [7:4], are used to identify the model of the processor within the processor's family.
3. The Family Code corresponds to Bits [11:8] of the EDX register after RESET, Bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register accessible through Boundary Scan.
4. The Model Number corresponds to Bits [7:4] of the EDX register after RESET, Bits [7:4] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the model field of the Device ID register accessible through Boundary Scan.
5. The Stepping ID in Bits [3:0] indicates the revision number of that model. Refer table above for the processor stepping ID number in the CPUID information.
6. Refer to Processor BIOS Specification for additional information. When EAX is initialized to a value of '1', the CPUID instruction returns the Extended Family, Extended Model, Processor Type, Family Code, Model Number and Stepping ID value in the EAX register. The EDX processor signature value after reset is equivalent to the processor signature output value in the EAX register.

Cache and TLB descriptor parameters are provided in the EAX, EBX, ECX and EDX registers after the CPUID instruction is executed with a 2 in the EAX register.

2.2 Component Marking Information

Figure 1. H/U-Series Chip Package BGA Top-Side Markings



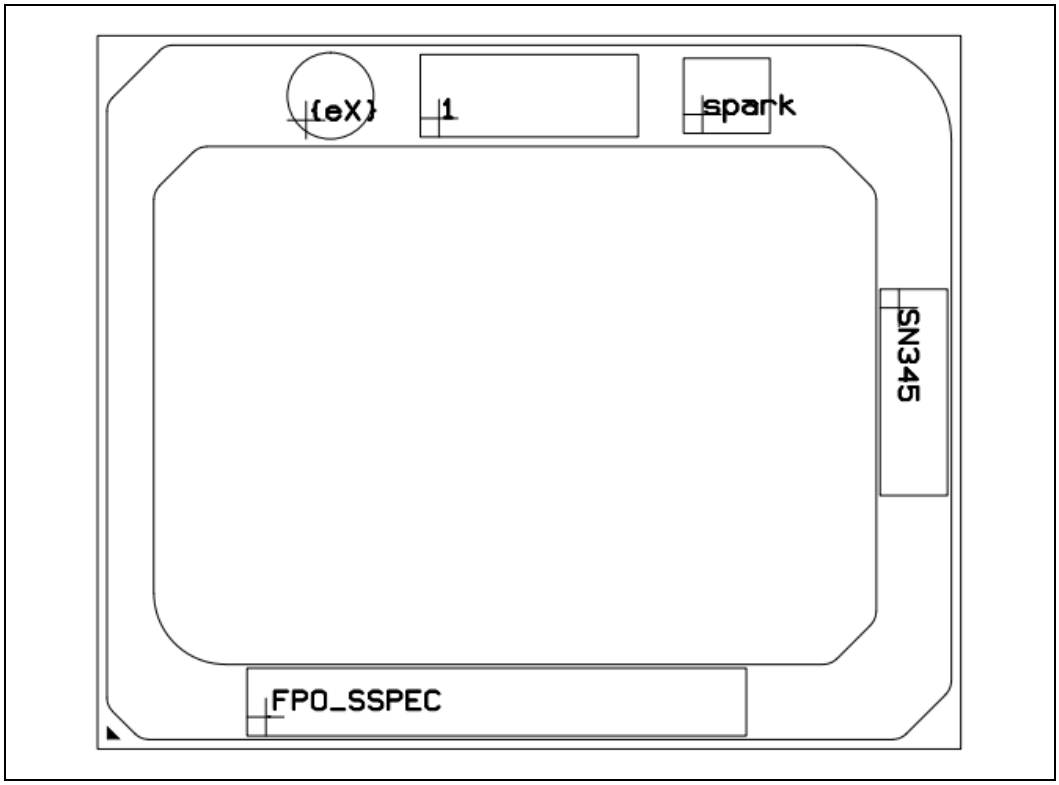
Pin Count: 2049 Package Size (width x height): 50 mm x 25 mm

Production (SSPEC):

- SN345
- G1L1: SPARK
- G2L1: FPO_SSPEC
- G3L1: {ex}

Note: "1" is used to extract the unit visual ID (2D ID).

Figure 2. U Type4 Series Chip Package BGA Top-Side Markings



Pin Count: 2551 Package Size (width x height): 23 mm x 19 mm

Production (SSPEC):

- SN345
- SPARK
- {ex}
- FPO_SSPEC

Note: "1" is used to extract the unit visual ID (2D ID).

Note: Processor list can be found at:
https://ark.intel.com/content/www/us/en/ark/products/series/236803/intel-core-ultra-processors-series-1.html

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3 Summary Tables of Changes

The following tables indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes which apply to the listed processor stepping. Intel may intend to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. These tables use the following notations:

3.1 Codes Used in Summary Table

Stepping	Description
(No mark) or (Blank box)	This erratum is fixed or does not apply to the listed stepping or specification change does not apply to the listed stepping.

Status	Description
Plan Fix	This erratum may be fixed in a future hardware stepping, firmware, or software update.
Fixed	This erratum has been previously fixed in Intel hardware, firmware, or software.
No Fix	There are no plans to fix this erratum.

3.2 Errata Summary Table

Erratum ID	Processor Line			Title
	H 6P+8E	U 2P+8E	U Type4 2P+8E	
MTL001	No Fix	No Fix	No Fix	USB DbC or Device Mode Port When Resuming From S4, S5, or G3 State
MTL002	No Fix	No Fix	No Fix	xHCI USB 2.0 ISOCH Device Missed Service Interval
MTL003	No Fix	No Fix	No Fix	Intel® VT-d Remapping Hardware Does Not Perform Reserved(0) Check on PGSNP Field of Scalable-mode PASID Table Entry
MTL004	Fixed	Fixed	Fixed	HDMI Analyzer Color Corruption in HDMI2.1 YUV420
MTL005	No Fix	No Fix	No Fix	Processor C-States With USB Full-Speed or Low-Speed Device Hotplug
MTL006	No Fix	No Fix	No Fix	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
MTL007	No Fix	No Fix	No Fix	xHCI Controller Reset Due to Missing Link Credit From Device

Erratum ID	Processor Line			Title
	H 6P+8E	U 2P+8E	U Type4 2P+8E	
MTL008	No Fix	No Fix	No Fix	xHCI Controller Hang With Zero-Length Data Packet
MTL009	No Fix	No Fix	No Fix	PCIe Root Port Lane Error Status Register May Not be Cleared
MTL010	No Fix	No Fix	No Fix	Type-C Display May be Blank Following S3/S4/S5 Resume
MTL011	No Fix	No Fix	No Fix	Precision Time Measurement (PTM) Interpretation Capability Bit Incorrect Register Offset
MTL012	No Fix	No Fix	No Fix	Performance Monitoring Event Branch Instruction Retired Will Not Count CALLs to Next Sequential Instruction
MTL013	No Fix	No Fix	No Fix	Performance Monitoring Event Branch Instruction Retired Will Overcount on Certain Types of Branch and Complex Instructions
MTL014	No Fix	N/A	N/A	PCIe Gen5 Root Ports Link Equalization Unexpected Behavior at High Temperature
MTL015	Fixed	Fixed	Fixed	Unpredictable System Behavior When SAGV is Enabled
MTL016	No Fix	No Fix	No Fix	MSI From VMD-Owned Device May Pass Memory Write
MTL017	No Fix	No Fix	No Fix	IA32_MC2_ADDR And IA32_MC2_MISC MSRs Will be Cleared on Warm Reset
MTL018	No Fix	No Fix	No Fix	Performance Monitoring Events TOPDOWN.BACKEND_BOUND_SLOTS and IDQ_BUBBLES May be Inaccurate
MTL019	No Fix	No Fix	No Fix	Performance Monitoring Event IDQ.MS_UOPS May Undercount
MTL020	No Fix	No Fix	No Fix	HDMI2.1 FRL Audio Distortion With 144Hz Display With Reduced Blanking Interval
MTL021	Fixed	Fixed	Fixed	P-core Not Exiting LFM
MTL022	No Fix	No Fix	No Fix	I2S Audio Channels Swapped With High Frame Polarity in Device Mode
MTL023	No Fix	No Fix	No Fix	System May Hang When Operating at Maximum Turbo Frequency
MTL024	Fixed	Fixed	Fixed	System May Signal MCE When Operating at Maximum Single Core Turbo Frequency
MTL025	Fixed	Fixed	Fixed	Processor May Hang When Intel® HD Graphics is Disabled
MTL026	Fixed	Fixed	Fixed	Processor Power Sharing May Not Perform as Expected

Erratum ID	Processor Line			Title
	H 6P+8E	U 2P+8E	U Type4 2P+8E	
MTL027	No Fix	No Fix	No Fix	Unexpected System Behavior When Re-Enabling Intel® HT
MTL028	No Fix	No Fix	No Fix	A Write to The TSC_Deadline MSR May Cause an Unexpected Timer Interrupt
MTL029	No Fix	No Fix	No Fix	Processor Trace May Generate PSB Packets Too Infrequently
MTL030	No Fix	No Fix	No Fix	Processor Trace May Not Generate a CYC Packet Before MODE.EXEC Packets
MTL031	No Fix	No Fix	No Fix	Unsynchronized Cross-Modifying Code Operations Can Cause an Unexpected Instruction Execution Results

3.3 Specification Changes

No.	Specification Changes
	None for this revision of this specification update.

3.4 Specification Clarifications

No.	Specification Clarifications
	None for this revision of this specification update.

3.5 Documentation Changes

No.	Documentation Changes
	None for this revision of this specification update.

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4 Errata Details

MTL001	USB DbC or Device Mode Port When Resuming From S4, S5, or G3 State
Problem	If a processor USB Type-C* port is configured in Device Mode (or in DbC mode) and connected to an external USB 3.2 host controller, it may cause the USB port to go into a non-functional state in the following scenarios: 1. The processor resumes from S4 or S5, the port may remain in U2. 2. The port is connected to a USB 3.2 Gen 1x1 host controller when resuming from S4, S5, or G3, the port may enter into Compliance Mode or an inactive state if Compliance Mode is disabled. 3. The port is connected to a USB 3.2 Gen 2x1 host controller when resuming from S4, S5, or G3, the port may enter an inactive state.
Implication	Due to this erratum, the processor USB Type-C port configured in Device Mode (or in DbC mode) may fail to enumerate or become unavailable.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL002	xHCI USB 2.0 ISOCH Device Missed Service Interval
Problem	When the xHCI controller is stressed with concurrent traffic across multiple USB ports, the xHCI controller may fail to service USB 2.0 Isochronous IN endpoints within the required service interval.
Implication	Due to this erratum, USB 2.0 isochronous devices connected to the xHCI controller may experience dropped packets. **NOTE:** This issue has only been observed in a synthetic environment.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL003	Intel® VT-d Remapping Hardware Does Not Perform Reserved(0) Check on PGSNP Field of Scalable-mode PASID Table Entry
Problem	Intel® VT-d remapping hardware does perform Reserved(0) check on Page Snoop (PGSNP) field in scalable-mode Process Address ID (PASID) table entry when Snoop Control capability is defined as not available in the Extended Capability Register Offset 10h bit 7 (ECAP.SC=0)
Implication	There are no known functional implications due to this erratum. Intel has not observed this erratum with any commercially available software.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL004	HDMI Analyzer Color Corruption in HDMI2.1 YUV420
Problem	When in HDMI2.1 FRL YUV420 mode, and the previous frame ended with an unexpected odd line, green image corruption may occur.
Implication	Due to this erratum, when using HDMI analyzer, corruption may be observed as green color data, contained within a vertical bar on right side of the analyzer monitor. Intel has not observed and functional issue due to the Erratum.
Workaround	A workaround for this erratum is available in iGFX Driver revision 101.5005 or later.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL005	Processor C-States With USB Full-Speed or Low-Speed Device Hotplug
Problem	When doing a hotplug on a USB hub with two or more USB Full-speed or Low-speed devices each with a 1 ms service interval interrupt endpoint, a race condition may occur between the PMC and the xHCI controller.
Implication	Due to this erratum, the processor may fail to enter C3 or deeper package C-States. **NOTE:** This erratum has only been observed in a synthetic environment.
Workaround	None identified. This condition is recovered after the xHCI controller has successfully entered D3.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL006	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
Problem	On USB 3.2 Gen 1x1 only capable ports, including ports configured as USB 3.2 Gen 1x1 by soft strap, the xHCI controller may send only 15 LFPS signals instead of a burst of 16 LFPS signals as specified by the USB 3.2 specification.
Implication	There are no known functional implications due to this erratum. LFPS handshake requires the receiver link partner to only detect 2 LFPS signals. This issue may impact the SuperSpeed compliance test case which checks for the 16 LFPS burst requirements: TD6.4, TD6.5, and TD7.31.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL007	xHCI Controller Reset Due to Missing Link Credit From Device
Problem	The xHCI controller may not send LCRD (Link Credit) to the device after the link U0 state recovery is completed if a USB 3.2 device incorrectly stops sending LCRD.
Implication	When this erratum occurs, subsequence transfers from the device may not be completed and the xHCI host controller driver may initiate a host controller reset.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL008	xHCI Controller Hang With Zero-Length Data Packet
Problem	The xHCI controller may fail to handle a zero-length data packet when doing concurrent traffic with the following devices connected on three separate root ports: • USB 3.2 Gen 2x1 (or 2x2) hub with at least two USB 3.2 bulk devices. • USB 3.2 Gen 2x1 (or 2x2) hub with at least two USB 3.2 bulk devices. • USB isochronous device that sends zero-length data packets.
Implication	Due to this erratum, the xHCI controller may hang. Intel has only observed this behavior with USB audio offload enabled and USB 2.0 audio devices that send zero-length data packets.
Workaround	None identified. A mitigation for USB 2.0 audio devices using USB audio offload is available in Intel® Smart Sound Technology driver version 20.40.9509.0 or later.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL009	PCIe Root Port Lane Error Status Register May Not be Cleared
Problem	Re-enabling a port following a link disable or hot reset the PCIe Lane Error Status register (Offset 0xA38) may not be cleared.
Implication	Due to this erratum, the Lane Error Status register may indicate lane errors on some of the Root Ports. Intel has not observed any functional issues due this erratum.
Workaround	None identified. Software should ignore the lane error status register to mitigate this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL010	Type-C Display May be Blank Following S3/S4/S5 Resume
Problem	When switching between Type-C Display Alt Mode and an Multi-Function Device (MFD) while the system is in S3/S4/S5, the Display may not enumerate.
Implication	When this erratum occurs the Display may be blank. A device unplug and re-plug may be necessary to recover the display.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL011	Precision Time Measurement (PTM) Interpretation Capability Bit Incorrect Register Offset
Problem	The PTM Propagation Delay Adaptation Interpretation B (PTMPDAIB) Bit is implemented at Configuration Space (CFG) Offset 158h instead of at 50h as documented in the PCI-SIG PTM Byte Ordering Adaptation Engineering Change Notice (ECN).
Implication	Due to this erratum, End Point Device (EPD) software that implements the PTM Byte Ordering Adaptation ECN will not be able to program their PTMPDAIB Bit correctly since it is located at a different register offset.
Workaround	None identified. To mitigate this issue, EPD software that implements the PTM Byte Ordering Adaptation ECN must access PTMPDAIB at CFG Offset 158h.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL012	Performance Monitoring Event Branch Instruction Retired Will Not Count CALLs to Next Sequential Instruction
Problem	A CALL instruction whose target is the next sequential instruction (the same address pushed onto the stack) will not increment the performance monitoring event BR_INST_RETIRED (Event: C4H, UMask: 00H, F9H).
Implication	Due to this erratum, software monitoring Branch Instruction Retired events may undercount. Since the CALL is to the next instruction, control flow tracing with the Last Branch Retired (LBR) records should not be affected.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL013	Performance Monitoring Event Branch Instruction Retired Will Overcount on Certain Types of Branch and Complex Instructions
Problem	On certain types of branch and complex instructions the performance monitoring event BR_INST_RETIRED (Event: C4H, UMask: 00H / 7EH / BFH / C0H / DFH / EBH / FBH / F9H) will overcount by 1. Affected instructions include FAR CALL/JMP, RETF, IRET, VMENTRY/VMEXIT/VMPTRLD and complex SGX/SMX/CSTATE instructions/flows.
Implication	Due to this erratum, software monitoring Branch Instruction Retired events may overcount.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL014	PCIe Gen5 Root Ports Link Equalization Unexpected Behavior at High Temperature
Problem	PCIe Lanes 21 through 28 may fail Gen5 link equalization at high temperatures due to complex lane microarchitectural conditions.
Implication	Due to this erratum, the associated PCIe Gen5 link may exhibit link errors, hang, or fail compliance tests. No issues have been observed when the PCIe link attempts Gen4 or lower.

Workaround	It is possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL015	Unpredictable System Behavior When SAGV is Enabled
Problem	On platforms that enable System Agent Geyserville (SAGV), a technology that allows load-specific memory speeds, the processor may exhibit unpredictable system behavior.
Implication	When this erratum occurs, the processor exhibits unpredictable system behavior.
Workaround	It is possible for BIOS to work around this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL016	MSI From VMD-Owned Device May Pass Memory Write
Problem	When the storage subsystem is configured to operate in RAID 0 or 1 mode, a Message Signaled Interrupt (MSI) from an Intel® Volume Management Device (Intel® VMD) owned device may interrupt a core before a previous write from the device is completed.
Implication	Due to this erratum, the platform may experience unpredictable system behavior.
Workaround	None Identified. The VMD MSI interrupt-handler should initially perform a dummy register read to the MSI initiator device prior to any writes to ensure proper PCIe ordering.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL017	IA32_MC2_ADDR And IA32_MC2_MISC MSRs Will be Cleared on Warm Reset
Problem	A non-zero value written to IA32_MC2_ADDR (40Ah) and IA32_MC2_MISC(40Bh) MSRs will be incorrectly cleared following a warm reset.
Implication	Due to this erratum, software that relies on the IA32_MC2_ADDR and IA32_MC2_MISC MSR values may not function correctly after a warm reset. Intel has not observed this erratum with any commercially available software.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL018	Performance Monitoring Events TOPDOWN.BACKEND_BOUND_SLOTS and IDQ_BUBBLES May be Inaccurate
Problem	The performance monitoring events TOPDOWN.BACKEND_BOUND_SLOTS (Event A4h, UMask 02h) and IDQ_BUBBLES.* (Event 9Ch, UMask 01h) may not count when the processor is in the C0.2 power sub-state, which is entered via the TPAUSE or UWAIT instructions. This erratum also impacts the accuracy of MSR_PERF_METRICS fields Frontend Bound, Backend Bound, and Fetch Latency (MSR 329h, Bits [23:16], [31:24] and [55:48]).

Implication	Due to this erratum, these performance monitoring events and the fields in MSR_PERF_METRICS may be inaccurate.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL019	**Performance Monitoring Event IDQ.MS_UOPS May Undercount**
Problem	The performance monitoring events IDQ.MS_UOPS, IDQ.MS_SWITCHES, and IDQ.MS_CYCLES_ANY (Event 79h, UMask 30h) may undercount MS_UOPS that come from the Decode Stream Buffer (DSB).
Implication	Due to this erratum, performance monitoring counters may report counts lower than expected.
Workaround	None identified. Performance monitoring event UOPS_RETIRED.MS may be used instead.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL020	**HDMI2.1 FRL Audio Distortion With 144Hz Display With Reduced Blanking Interval**
Problem	The processor may not have sufficient display bandwidth to support display audio when using HDMI2.1 FRL (Fixed Rate Link) with a 144Hz display with reduced blanking interval.
Implication	Due to this erratum, intermittent or complete loss of audio may occur.
Workaround	A mitigation has been identified for this erratum and may be available in a software update.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL021	**P-core Not Exiting LFM**
Problem	P-core frequency may not be updated after resuming from PKG C6.
Implication	Due to this erratum, P-core may unexpectedly remain in Low Frequency Mode (LFM).
Workaround	A BIOS code change has been identified and may be implemented as a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL022	**I2S Audio Channels Swapped With High Frame Polarity in Device Mode**
Problem	When the I2S interface is in device mode, the audio controller may not be correctly configured if the audio codec requires high frame polarity.
Implication	Due to this erratum, the left and right audio channels may swap when frame polarity is set to high.
Workaround	None identified.

Status	For the steppings affected, refer to the Summary Table of Changes.

MTL023	**System May Hang When Operating at Maximum Turbo Frequency**
Problem	The processor may fail to correctly thermally throttle when running at maximum turbo frequency.
Implication	Due to this erratum, the system may hang with an Internal Timeout Error Machine Check (IA32_MCi_STATUS.MSCOD=080h and IA32_MCi_STATUS.MCACOD=0400h) or unpredictable system behavior may occur.
Workaround	None identified. It may be possible for BIOS to contain a mitigation for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL024	**System May Signal MCE When Operating at Maximum Single Core Turbo Frequency**
Problem	DCU DCACHEL0_EVICT_ERR (MSCOD=0100h and MCACOD=0174h) may be observed when the core frequency is operating at Maximum Single Core Turbo Frequency.
Implication	Due to this erratum, the system may signal a fatal DCACHEL0_EVICT_ERR machine check exception.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL025	**Processor May Hang When Intel® HD Graphics is Disabled**
Problem	If internal graphics is disabled (Bus 0, Device 2, Function 0) when using a discrete graphics solution, the processor may fail to exit Package C6 state and report a machine check exception with an MCACOD=0402H and MSCOD=0823H.
Implication	Due to this erratum, the processor may hang with a machine check exception.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL026	**Processor Power Sharing May Not Perform as Expected**
Problem	The processor exposes certain power sharing capabilities via the Intel Performance Framework. However, the processor may not honor power sharing requests made via SET_PERF_PREFERENCE_MIN and SET_PERF_PREFERENCE_MAX.
Implication	Due to this erratum, software may not achieve its expected processor power allocation.
Workaround	It it possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL027	Unexpected System Behavior When Re-Enabling Intel® HT
Problem	When performing a warm reset as part of enabling of Intel® Hyper-Threading, machine check banks may not be initialized correctly.
Implication	Due to this erratum, software that relies on initialized values in machine check banks may not behave as expected.
Workaround	None identified. Software or BIOS can avoid this erratum by performing cold reset when re-enabling Intel® HT.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL028	A Write to The TSC_Deadline MSR May Cause an Unexpected Timer Interrupt
Problem	Under complex micro-architectural conditions, writing a non-zero value to the Time-Stamp Counter (TSC) Deadline counter, IA32-TSC_DEADLINE MSR (6E0h), may cause timer interrupt following the write.
Implication	Due to this erratum, a unexpected timer interrupt may be signaled.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL029	Processor Trace May Generate PSB Packets Too Infrequently
Problem	A Packet Stream Boundary (PSB) packet should be generated for every PSBFreq number of trace output bytes. Due to this erratum, PSB packets may be generated only after as many as four times that number of output bytes have been generated.
Implication	Due to this erratum, trace decoder software may see fewer PSB packets than expected. This may lead to the trace decoder software needing to search further to find a starting point to decode or, when used in circular mode, being unable to decode the trace due to lacking any PSB packets.
Workaround	None identified. Software can request more frequent PSB packets by programming PSBFreq (bits[27:24]) of IA32_RTIT_CTL MSR (570H) to a value 1/4 of the desired value.
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL030	Processor Trace May Not Generate a CYC Packet Before MODE.EXEC Packets
Problem	When a Processor Trace MODE.EXEC packet is generated due to a change in RFLAGS.IF (interrupt flag) or the CS.L or CS.D bits, the processor may not generate a CYC packet before generating the MODE.EXEC packet.
Implication	Due to this erratum, trace decoder software will not be able to precisely determine when mode changes that involve changing the interrupt flag or the application's default operand size happened.
Workaround	None identified
Status	For the steppings affected, refer to the Summary Table of Changes.

MTL031	Unsynchronized Cross-Modifying Code Operations Can Cause an Unexpected Instruction Execution Results
Problem	The act of one processor or system bus master writing data into a currently executing code segment of a second processor with the intent of having the second processor execute that data as code is called cross-modifying code (XMC). XMC that does not force the second processor to execute a synchronizing instruction prior to execution of the new code is called unsynchronized XMC. Software using unsynchronized XMC to modify the instruction byte stream of a processor can see unexpected or unpredictable execution behavior from the processor that is executing the modified code.
Implication	In this case the phrase "unexpected or unpredictable execution behavior" encompasses the generation of most of the exceptions listed in the Intel Architecture Software Developer's Manual Volume 3: System Programming Guide including a General Protection Fault (GPF) or other unexpected behaviors. In the event that unpredictable execution causes a GPF the application executing the unsynchronized XMC operation would be terminated by the operating system.
Workaround	In order to avoid this erratum programmers should use the XMC synchronization algorithm as detailed in the Intel Architecture Software Developer's Manual Volume 3: System Programming Guide Section: Handling Self- and Cross-Modifying Code.
Status	For the steppings affected, refer to the Summary Table of Changes.

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5 Specification Changes

None.

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6 Specification Clarification

None.

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7 Document Change

None.

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