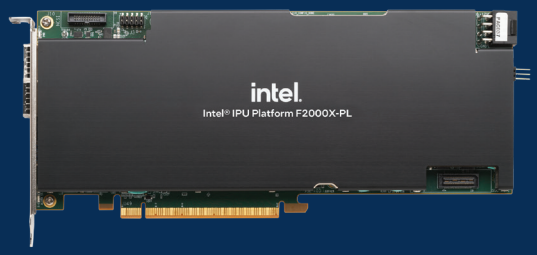
Product Brief

Intel® Infrastructure Processing Unit (Intel IPU) Platform F2000X-PL

High-Performance FPGA-based Platform for Accelerating Cloud Infrastructure Workloads



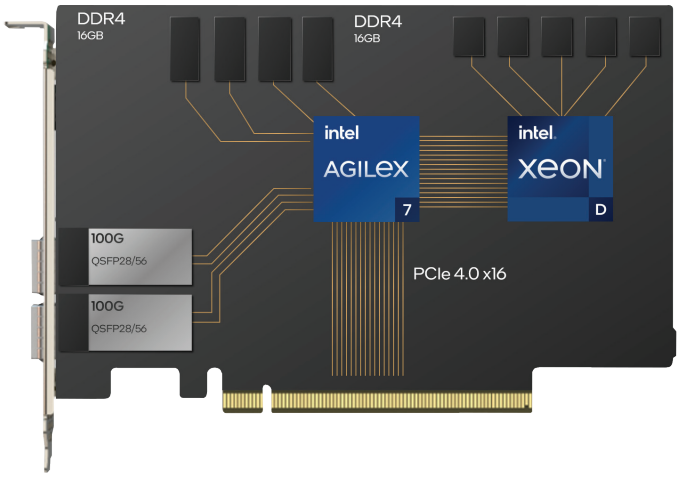
2x100 Gb
Ethernet Connectivity

Intel Agilex® 7 FPGA F-Series
FPGA

Intel® Xeon® D CPU
Processor

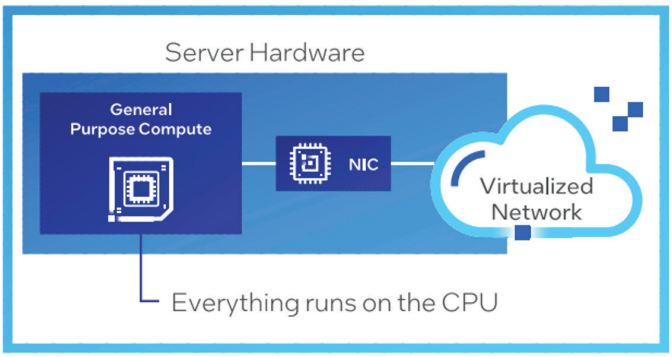
PCIe* Form Factor
¾ Length, Full Height

The Intel® Infrastructure Processing Unit (Intel IPU) Platform F2000X-PL is a high-performance Intel Agliex® 7 FPGA and Intel® Xeon® based Cloud and Enterprise Infrastructure acceleration platform with 2 x 100 Gb Ethernet network interfaces.

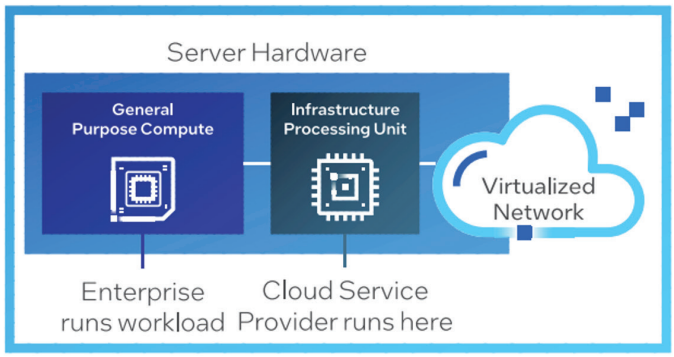


It is designed to support the offload and acceleration of compute-intensive cloud infrastructure workloads such as networking (for example, Open vSwitch), storage (for example, NVMe*/TCP), and security (for example, TLS and TCP). The built-in hardware crypto block enables security at line rate and helps provide tenant isolation.

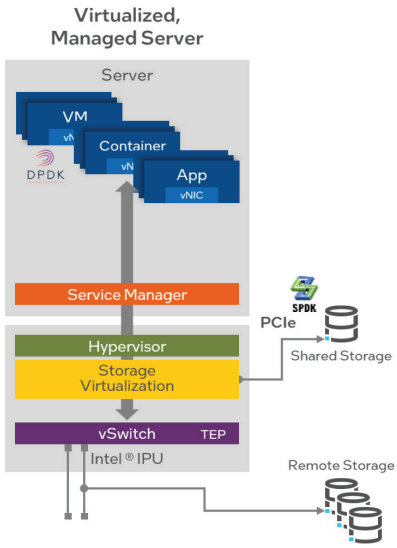
'Classic' Enterprise Data Center Approach



IPU Data Center Approach for CSP



Intel IPU Use Cases



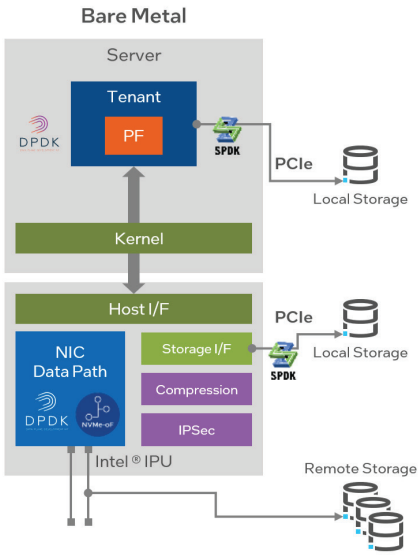
Virtualized Public Cloud

Intel® IPU Features

- Programmable NIC Pipeline
- vSwitch Control and Management
- Tunnel Endpoint (TEP)
- Data Encryption (IPsec)

Intel IPU Benefits

- Lower Host Overhead →Improved TCO
- Keep Up with Higher Link Speeds
- Transparent to VM or Containers
- Secure Traffic in Data Center



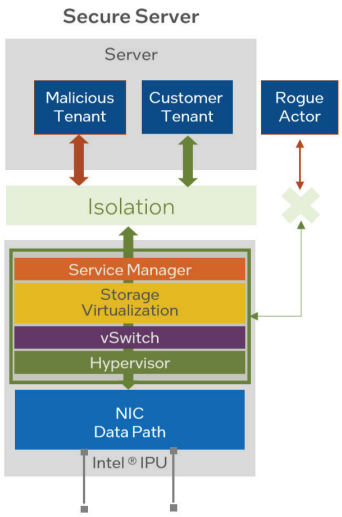
Cloud – Bare Metal

Intel® IPU Features

- Security Isolation
- In-Band Management
- Root of Trust for Server
- Accelerated Networking, Remote Storage
- Encrypted Physical or Virtual Links

Intel IPU Benefits

- Infrastructure Isolation
- Cloud Service Provider (CSP) Monitors and Manage Resources
- Monitor and Manage Resources
- Accelerated Remote Storage Access



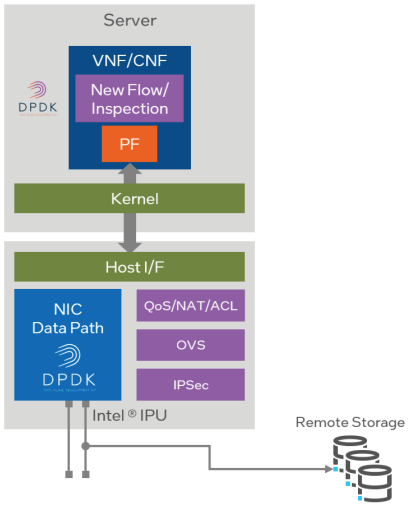
Security Air-Gap

Intel® IPU Features

- Security Isolation
- IPU is the Root of Trust for Server
- Integrated Management Complex Manages Secure Resources

Intel IPU Benefits

- Infrastructure Isolation
- CSP Monitors and Manage Resources
- IPU Secure Boot and Configuration of SoC Infrastructure



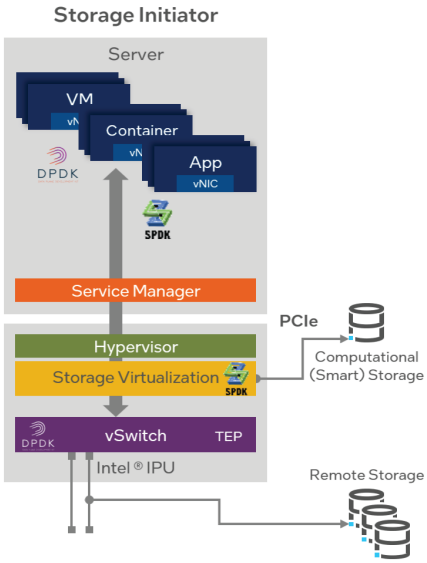
5G Telco NFV Infrastructure

Intel® IPU Features

- NFV Infrastructure Acceleration
- Virtual Switching (Contrail / OVS)
- Segment Routing IPV6
- Load Balancing

Intel IPU Benefits

- Routing Offloaded to IPU
- Infrastructure Switching
- Improved Throughput Possible



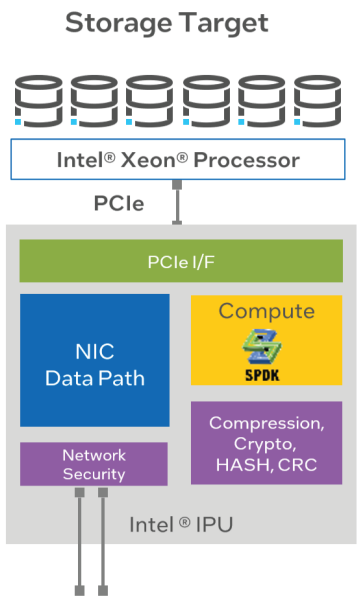
Storage Initiator

Intel® IPU Features

- Support local NVMe*, NVMe-oF, and VirtIO Protocols
- Standard Storage Stacks such as SPDK
- Proprietary Storage Stacks
- Compression, Encryption Services

Intel IPU Benefits

- Transparent to VM or Containers
- Less Host Overhead →Lower TCO
- Keep up with Higher Link Speeds
- Secure Storage Traffic in the Data Center
- Increases Storage Efficiency in Hyper-converged Environment



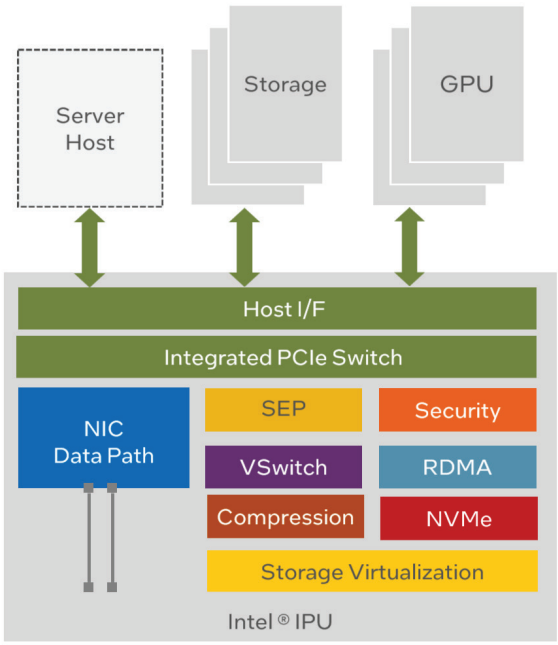
Storage Target Node

Intel® IPU Features

- High-Speed Network Pipeline
- RDMA and Reliable Transport
- Compute Subsystem for SPDK and Storage Applications
- Compression, Crypto, HASH/CRC Offload Engine
- Integration PCIe* Switch for Fanout

Intel IPU Benefits

- Storage Data Path Acceleration
- Add-on PCIe Switch for Fanout
- Power-Efficient System Design
- Low-Cost JBOF(Just Bunch of Flash) Solutions



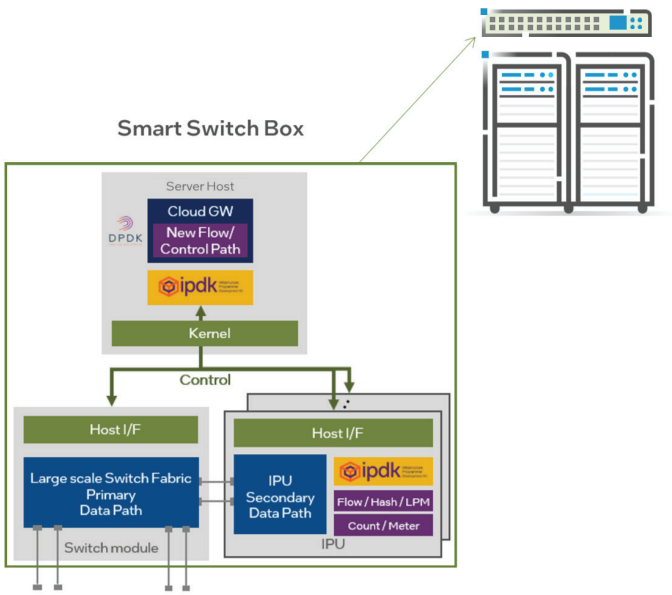
Artificial Intelligence

Intel® IPU Features

- vSwitch Offload
- Integrated PCIe Switch for Fanout
- Support Local NVMe, NVMe-oF, and VirtIO Protocols
- Standard Storage Stacks like SPDK
- Proprietary Storage Stacks
- Compression, Encryption Services
- RDMA and Reliable Transport

Intel IPU Benefits

- Reduce Latency
- Reduced Total Cost of Ownership (TCO)
- Improved Performance
- Increased Security



Smart Switch

Intel® IPU Features

- P4 Programmable Pipeline
- Stateful Flow Processing, LPM, ACL, Hash
- QoS, Count, Meter
- Encryption (IPSec/TLS)

Intel IPU Benefits

- Unified Platform for Cloud Gateways
- Much Greater Throughput Possible
- Host (Cloud Gateway) for Control Path Processing
- Datapath Offloaded to Switch and IPU
- IPU for More Sophistic, Flow-based Processing
- IPU for Customized Pipelines to Serve Different Cloud Gateway Apps

Platform Specifications

Hardware	
FPGA	Intel Agilex® FPGA F-Series AGFC023 ▪ 2.3M LEs, 782.4K ALMs ▪ 246 Mb on-chip memory ▪ 1,640 digital signal processing (DSP) blocks ▪ Hardened crypto ▪ 4x4 GB FPGA memory (error correcting code (ECC), 40 bit, 2,666 MTps)
CPU	Intel® Xeon® D-1736 SoC ▪ 8 cores, 16 threads ▪ 2.3 GHz, 3.4 GHz turbo frequency ▪ 15 MB cache ▪ 2x8 GB DDR4 Intel Xeon SoC memory (ECC, 72 bit, 2,900 MTps) ▪ 64 GB NVMe* in the M.2 slot on the IPU for the SoC operating system
PCI Express Interfaces	▪ PCIe* 4.0 x16 (16 GTps) between the CPU and host ▪ PCIe 4.0 x16 (16 GTps) between the FPGA and CPU
Front Panel Network Interface	▪ 2-port QSFP28/56 ▪ 2x100GBASE-LR4/SR4/CR4 ▪ 2x10/25GBASE-LR/SR/CR (QSFP/SFP adapter) ▪ 8x10/25GBASE-SR/CR (breakout cable) ▪ Dedicated 1G management port (RJ45)
Mechanical, Thermal, and Power	▪ Full-height, ¾ length, single-slot PCIe form factor (note: partners may develop versions with different form factors) ▪ Maximum power consumption for standard hardware configuration: 150 W
Board Management Controller (BMC)	▪ Ethernet, USB (front panel), UART (internal) connectivity ▪ Secure FPGA image update ▪ Wake-on-LAN ▪ MCTP over SMBus ▪ MCTP over PCIe VDM ▪ Dedicated NC-SI RBT internal port ▪ PLDM for monitor and control (DSP0248) ▪ PLDM for FRU (DSP0257)
SoC Operating System	▪ Fedora Linux* ▪ UEFI basic input/output system (BIOS) ▪ PXE boot support ▪ Full shell access via SSH and UART
Tool Support	▪ Intel Acceleration Stack for Intel Xeon CPU with FPGAs ▪ Intel Quartus® Prime Design Software ▪ Data Plane Development Kit (DPDK) ▪ Storage Performance Development Kit (SPDK) ▪ Infrastructure Programmer Development Kit (IPDK)
Environment and Approvals	▪ EU, US, and APCJ regulatory approvals ▪ Thermal, shock, and vibration tested ▪ UL marked, RoHS, and REACH compliant ▪ Temperature range: -5°C to +45°C ▪ ASHRAE class A2
Application Stack Acceleration Framework	▪ Framework for embedding customer Accelerator Functional Units (AFU) implementing workload acceleration/offload in FPGA ▪ Six AFUs supported ▪ Throughput up to 200 Gbps ▪ Look-aside and inline AFU configurations ▪ Pre-integrated AFUs for host VirtIO-net direct memory access (DMA), SoC VirtIO-net DMA, and packet processor with foundational network interface card (NIC) functions.

Development Tools

IPDK is an open-source, vendor-agnostic framework of drivers and APIs for infrastructure offload and management that runs on a CPU, IPU, DPU, or switch. IPDK runs in Linux and uses a set of well-established tools such as SPDK, DPDK, and P4 to enable network virtualization, storage virtualization, workload provisioning, root-of-trust, and offload capabilities found in the platform. IPDK provides a common platform for increasing performance, optimizing resources, and securing the infrastructure as a sub-project of Open Programmable Infrastructure, a Linux Foundation Project.

SPDK provides a set of tools and libraries for writing high-performance, scalable, user-mode storage applications.

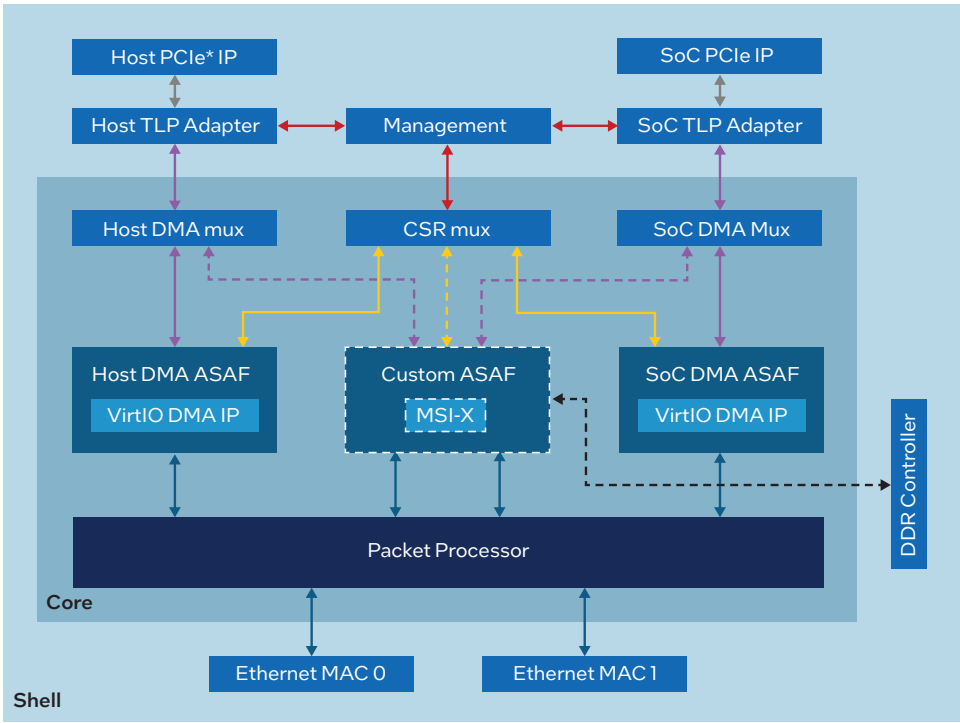
- Leverage the latest NVMe features
- User-mode drivers with minimal Linux version dependencies
- Poll-mode and event-loop design for maximum performance
- Lockless, thread-per-core design

DPDK is an open-source software project managed by the Linux Foundation. It provides a set of data plane libraries and network interface controller polling-mode drivers for offloading TCP packet processing from the operating system kernel to processes running in user space. This offloading achieves higher computing efficiency and higher packet throughput than is possible using the interrupt-driven processing provided in the kernel.

Application Packages

Application	Details	Provider
Networking	▪ Supports packet processor with the basic NIC functionality ▪ Supports packet processor implementing Open vSwitch (OvS) hardware offload of the data plane ▪ OvS hardware offload at the megaflows layer (wildcard matches) ▪ 1024 megaflow cache supporting millions of exact flows ▪ Supports VLAN, QinQ, and VxLAN encapsulation/decapsulation in hardware ▪ OvS control plane on the host or on the SoC ▪ Exposes VirtIO-net virtual interfaces as physical functions (PFs) or virtual functions (VFs) (SR-IOV)	Napatech
Storage	▪ NVMe/TCP offload ▪ Presents 16 block devices to the host (VirtIO block) ▪ Compatible with the VirtIO block drivers present in the latest RHEL and Ubuntu Linux distributions ▪ No proprietary software or drivers are required in the host ▪ No network interfaces exposed to the host ▪ NVMe/TCP initiator running on the SoC ▪ Offloads all NVMe/TCP operations from the host CPU to the IPU ▪ No access to the SoC from the host (air gap) ▪ Storage configuration over the SPDK remote procedure call (RPC) interface ▪ NVMe/TCP multipath support ▪ 2x100G connectivity to the storage network	Napatech
Security	▪ TCP offload + TLS acceleration ▪ Present up to 16 network devices to the host (VirtIO-net) ▪ 2x100G Ethernet front-port connectivity ▪ TLS 1.2/1.3 encryption offload ▪ OpenSSL support ▪ Nginx-based HTTP(s) reverse proxy with caching ▪ WebSockets support ▪ Load balancing to host ▪ Web server acceleration (reduced page load time) with static file caching and image optimization	Napatech

Application Stack Acceleration Framework (ASAF)



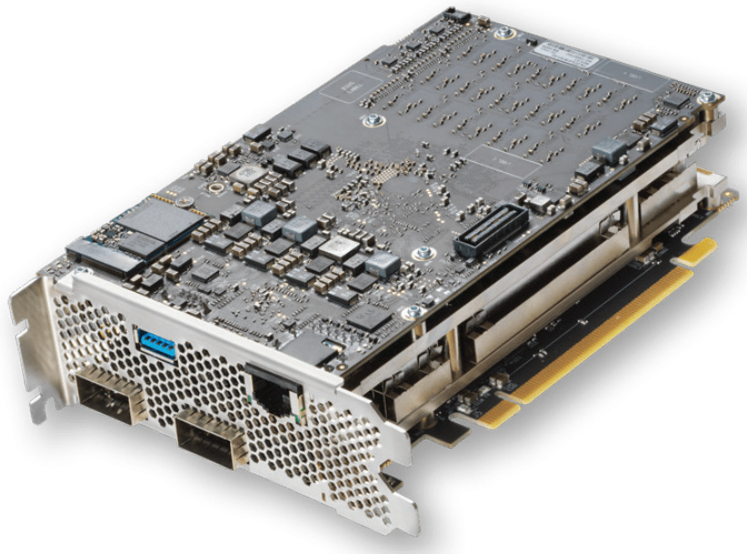
- TLP Interface (proprietary)
- DMA Interface (Avalon® Streaming[1])
- PP Interface (Avalon® Streaming[1])
- Ctrl and Status Interface (Avalon Memory Mapped[1])
- PCI Driver BAR Access (Avalon Memory Mapped[1])
- DDR Interface (Avalon Memory Mapped[1])

[1] N.B. Includes some ASAF specific extensions over the Avalon standards

Ordering Information

Napatech

F2070X Infrastructure Processing Unit (IPU)



Learn More

- F2070X Product Page
- Link-Virtualization Software
- Link-Storage Software
- Link-Security Software

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