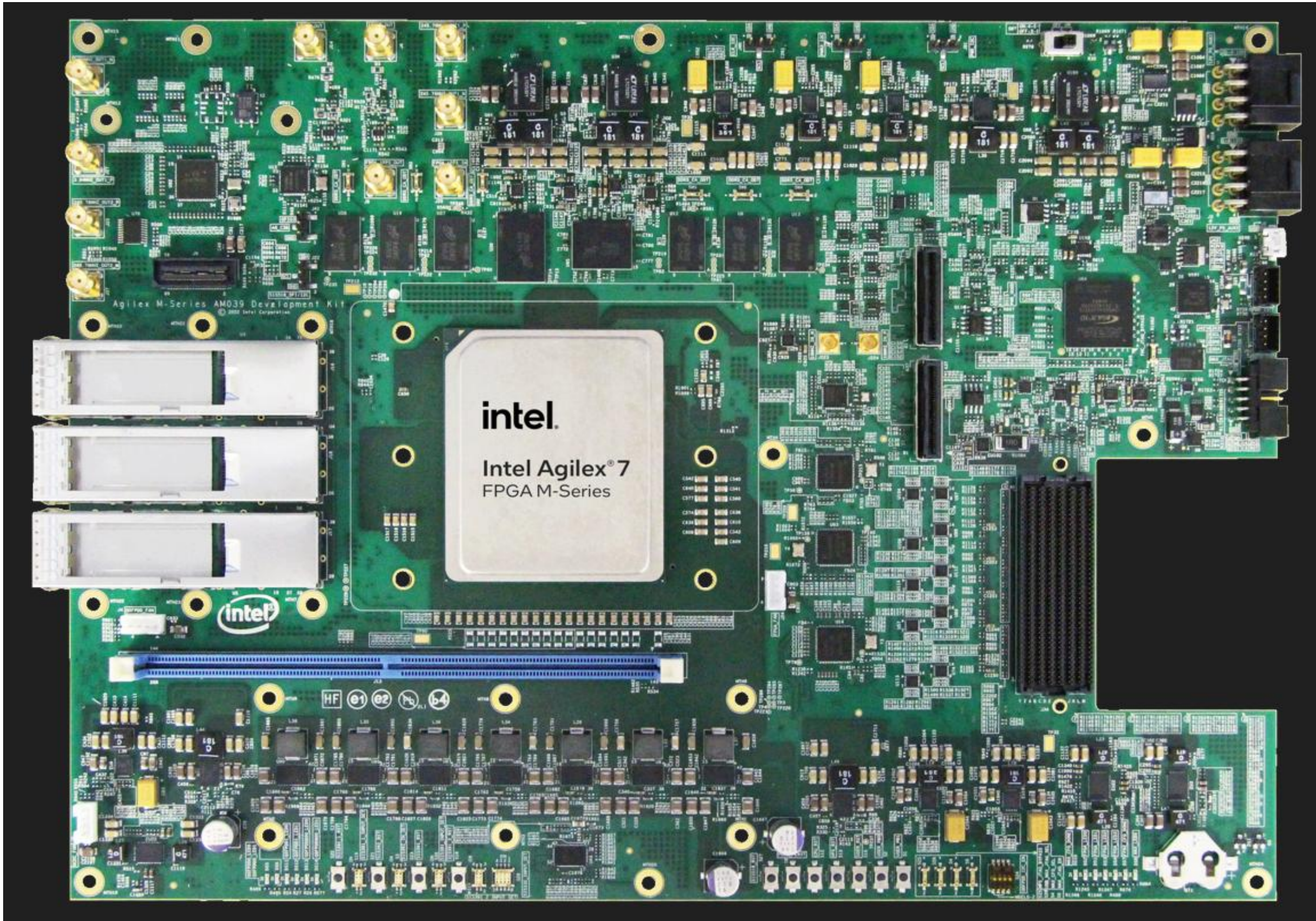


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TOP ASSEMBLY (TA)# M85147-001  
PRINTED BOARD ASSEMBLY (PBA)# M68999-100  
SCHEMATIC DRAWING #  
ASSEMBLY FILES #  
RAW PRINTED BOARD (PB)#  
GERBER FILES #

# FP82 DEV KIT



SPEED TOP NUMBER 99C25M  
TOP ASSEMBLY - M85147-001  
PCB ASSEMBLY - M69899-100  
FP8 SCHEMATIC - 180-0330697-B1  
FP82DK RAW PCB - 100-0330697-B1  
GERBERS - 110-0330697-B1  
FALCON PARK (PRO) MMID: 99AZCT

PAGE	DESCRIPTION	PAGE	DESCRIPTION
1	TITLE PAGE	57	LPDDR5
2	FP82DK PLACEMENT	58	LPDDR5 POWER
3	POWER SEQUENCE DIAGRAM	59	LPDDR5 DECOUPLING CAP
4	RESERVED	60	DDR5 COMPM16_0 ECC
5	MAX10 AND FPGA I2C DIAGRAM	61	DDR5 COMPM16 1
6	CLOCK DIAGRAM	62	HPS DDR5X16 0 ECC
7	BLOCK DIAGRAM	63	HPS DDR5X16 1
8	12V AUX1 CONNECTOR / 12V INRUSH CURRENT	64	RESERVED
9	12V AUX2 CONNECTOR / 12V INRUSH CURRENT	65	MOUTING HOLES
10	FP82 BANK -SDM2	66	QSFDD0-1 QSFDD800 LED /USER LEDS
11	FP82 BANK - 2A-FMC IO	67	TEMP SENSOR FAN
12	FP82 BANK - 2B	68	LEVEL XTLR IO EXP1
13	FP82 BANK - 2C RDIMM BK-A	69	LEVEL XTLR IO EXP2
14	FP82 BANK - 2D RDIMM BK-B	70	LEVEL XTRL IO EXP3
15	FP82 BANK -3A-DDR5X16	71	TEST POINT 2
16	FP82 BANK -3B -LPDDR5	72	VCC HSSI RNR /VCCBAT_SDM
17	FP82 BANK -3C-GPIO-NAND	73	FMC VIDEO CLOCK
18	FP82 BANK -3D-HPS-DDR5X16	74	RESERVED
19	FP82 BANK - NC	75	VCCERT1_2 BRK GDR U20 U22
20	FP82 BANK - DNU	76	VCCE PLL REF RNR/P3V3 CLK
21	FP82 BANK - DNU & REFCLK	77	DDR5 COMPM16 1V1/1V8
22	FP82 BANK - HPS	78	RESERVED
23	FP82 BANK - F TILE -12A	79	HBM1 HBM2 2.5V
24	FP82 BANK - F TILE -13A	80	VCCERT RNR /VCCEHT BRK GXF U20 U22
25	FP82 BANK - F TILE -13C	81	VCCERT UX GDR U10/1V8 FPGA
26	FP82 BANK - R TILE -14C	82	RESERVED
27	FP82 BANK - GND 1	83	RESERVED
28	FP82 BANK - GND 2	84	P1V2 INPUT FOR ALL LDO
29	FP82 BANK - POWER 1 FPGA VCC	85	LPDDR5 OV9 & 1V8
30	FP82 BANK - POWER 2	86	LPDDR5 1V05 & OV5
31	FP82 BANK - POWER 3	87	VCCEHT UX GDR U10 U20 U22
32	FP82 BANK - POWER 4	88	1V1 DDR5 SYS
33	FP82 BANK - DECOUPLING CAPACITORS 1	89	POWER MISC 1
34	FP82 BANK - DECOUPLING CAPACITORS 1	90	POWER MISC 2
35	BUFFER AND VOLTAGE TRANSLATOR	91	FPGA VCC CONTROLLER
36	MCIO CONNECTORS	92	VCC PHASE 1
37	VOLTAGE TRANSLATOR FOR 1588 CLOCK	93	VCC PHASE 2
38	SMA FOR 1588 FEATURE	94	VCC PHASE 3
39	10MHZ SMA FOR 1588	95	VCC PHASE 4
40	1588 CLOCK	96	VCC PHASE 5
41	SI5391 FAN OUT FOR 1588 SYNC FEATURE	97	VCC PHASE 6
42	1588 FEATURE	98	VCCIO UIB PHASE 7
43	UIB CLOCK	99	VCC HSSI GXF U20 U22
44	PCIE CLOCK	100	VCCERT UX GDR U20 U22/VCCN PIO
45	SYSTEM CLOCK FOR DDR AND IO BANK	101	VCC HSSI GDR U10 /VCCH AIB/VCCCL HPS
46	MAX10 POWER	102	3V3 STBY
47	MAX10 IO	103	P5V0/P1V8_IN
48	MAX10 DECOUPLING CAPS	104	RESET BUTTON
49	MAX10 FLASH USB PHY	105	FMC+ IO CONNECTOR
50	FPGA DECOUPLING CAPS 3	106	FMC+ TRANSCEIVER CONNECTOR
51	FPGA DECOUPLING CAPS 4	107	FMC+ VTT COMP
52	QSFDD CONN 0	108	TERMINATION FOR ALL FMC SIGNALS
53	QSFDD CONN1	109	FMC+ VOLTAGE TRANSLATOR
54	QSFDD800 CONN	110	VOLTAGE TRANSLATOR FOR FMC
55	NAND FLASH	111	REVISION HISTORY
56	DDR5 RDIM		

Fri Oct 6 12:36:45 2023

TITLE PAGE

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DOCUMENT NUMBER

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REV

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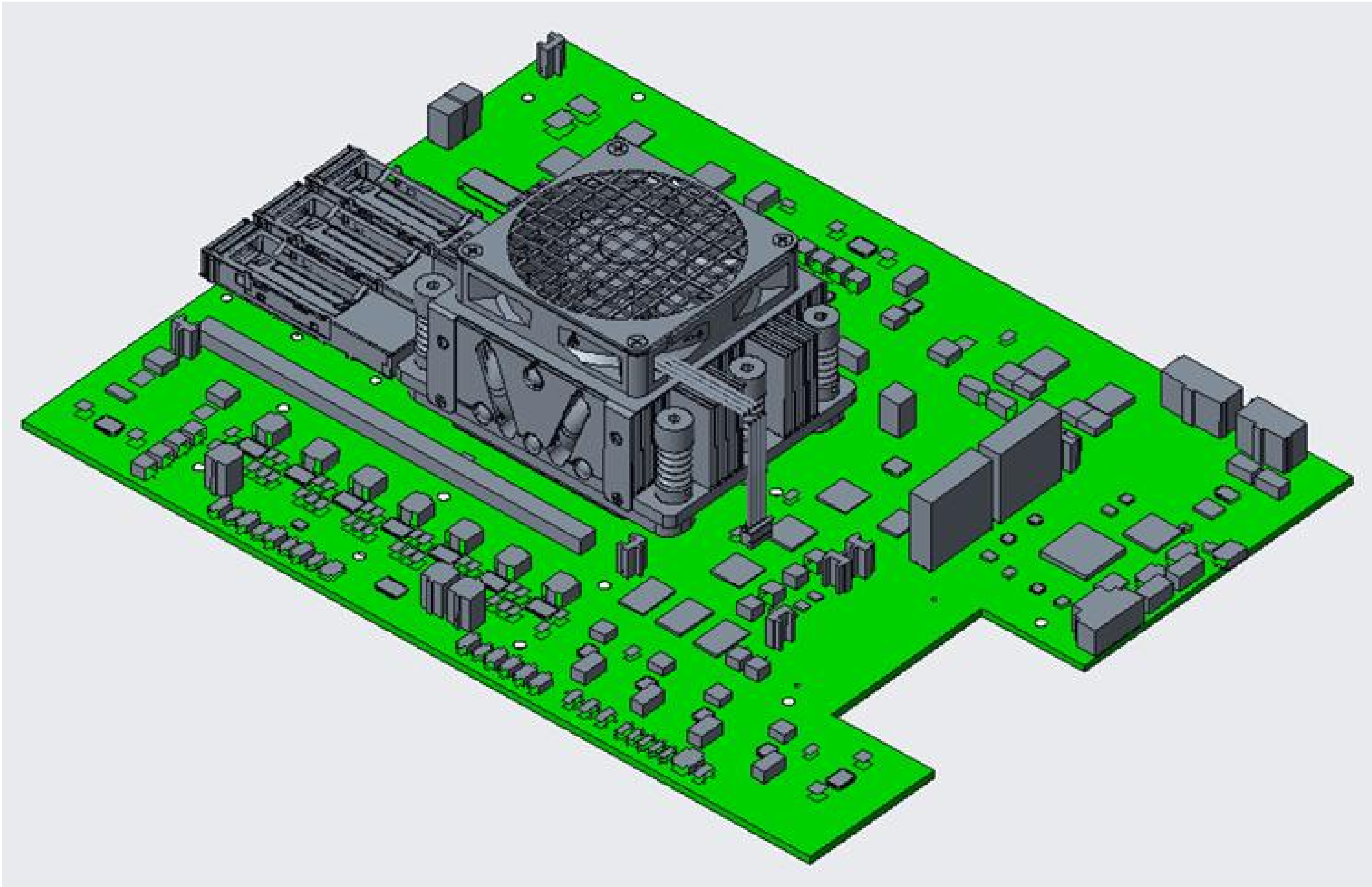
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DIAGRAM POWER TREE



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DIAGRAM: POWER TREE

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## Power Tree



DIAGRAM: POWER SEQUENCE

4

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DIAGRAM BMC/JTAG

B

B

A

A

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DIAGRAM: BMC/JTAG

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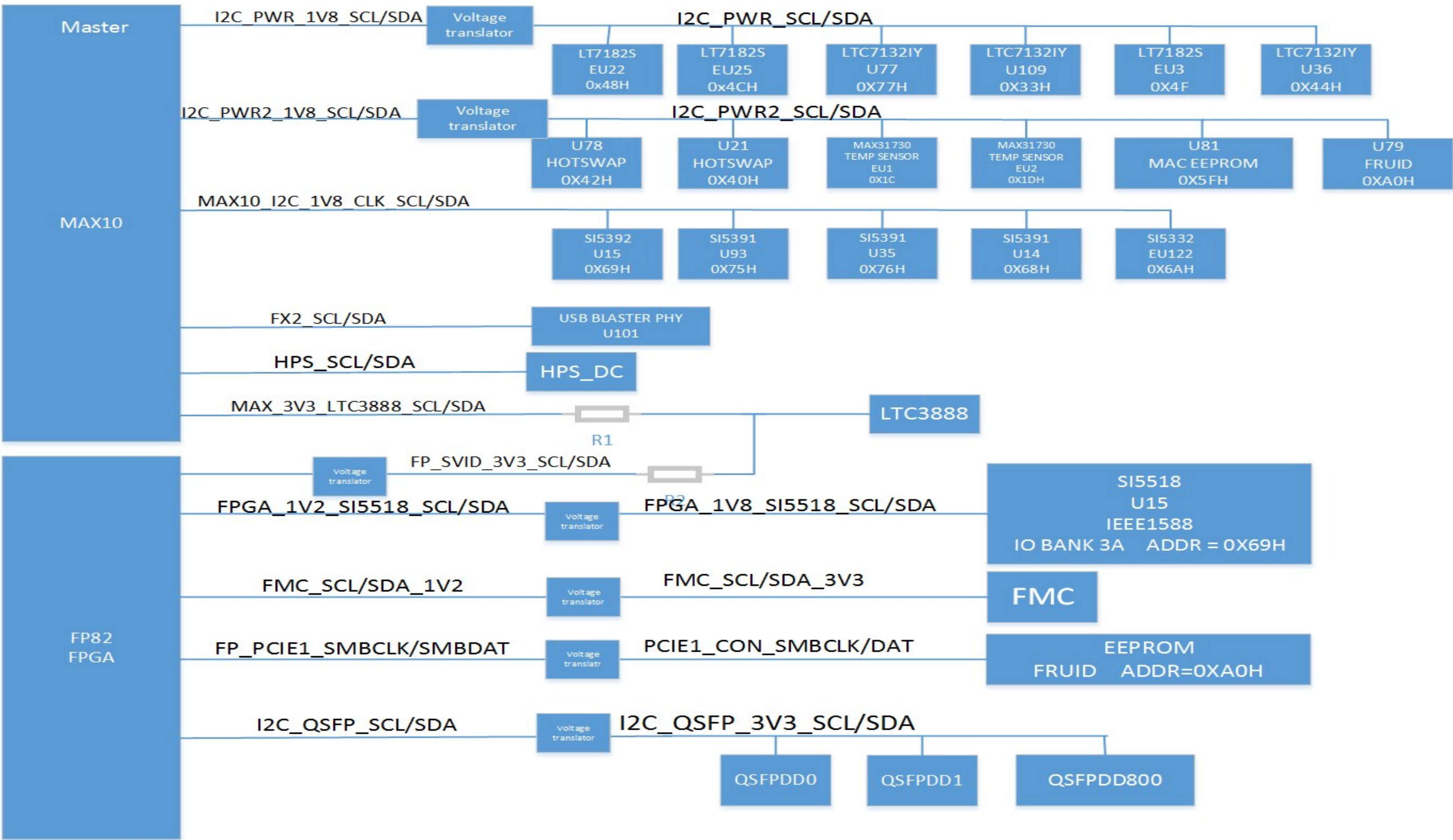
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DIAGRAM BMC/I2C

FP82DK I2C BLOCK DIAGRAM

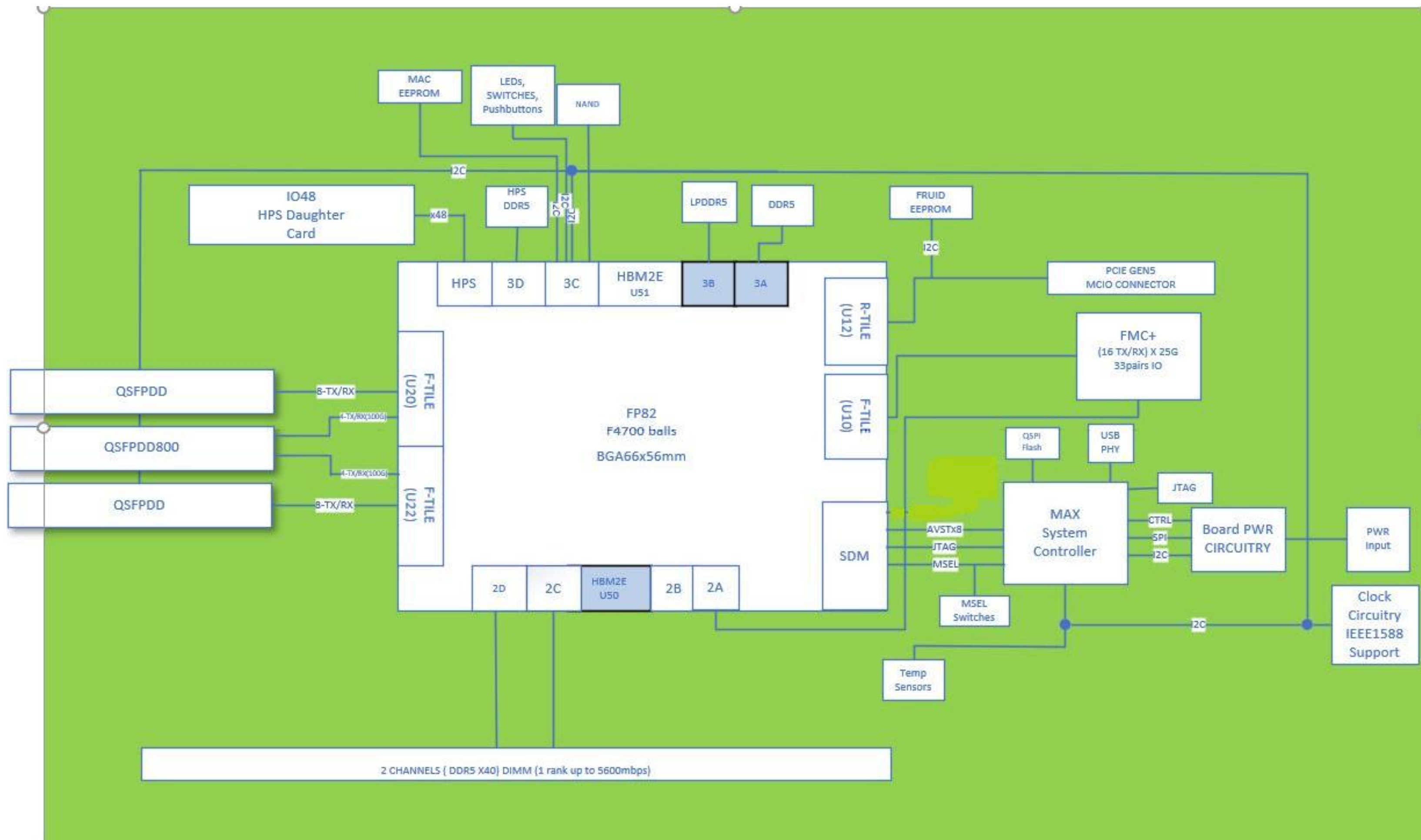


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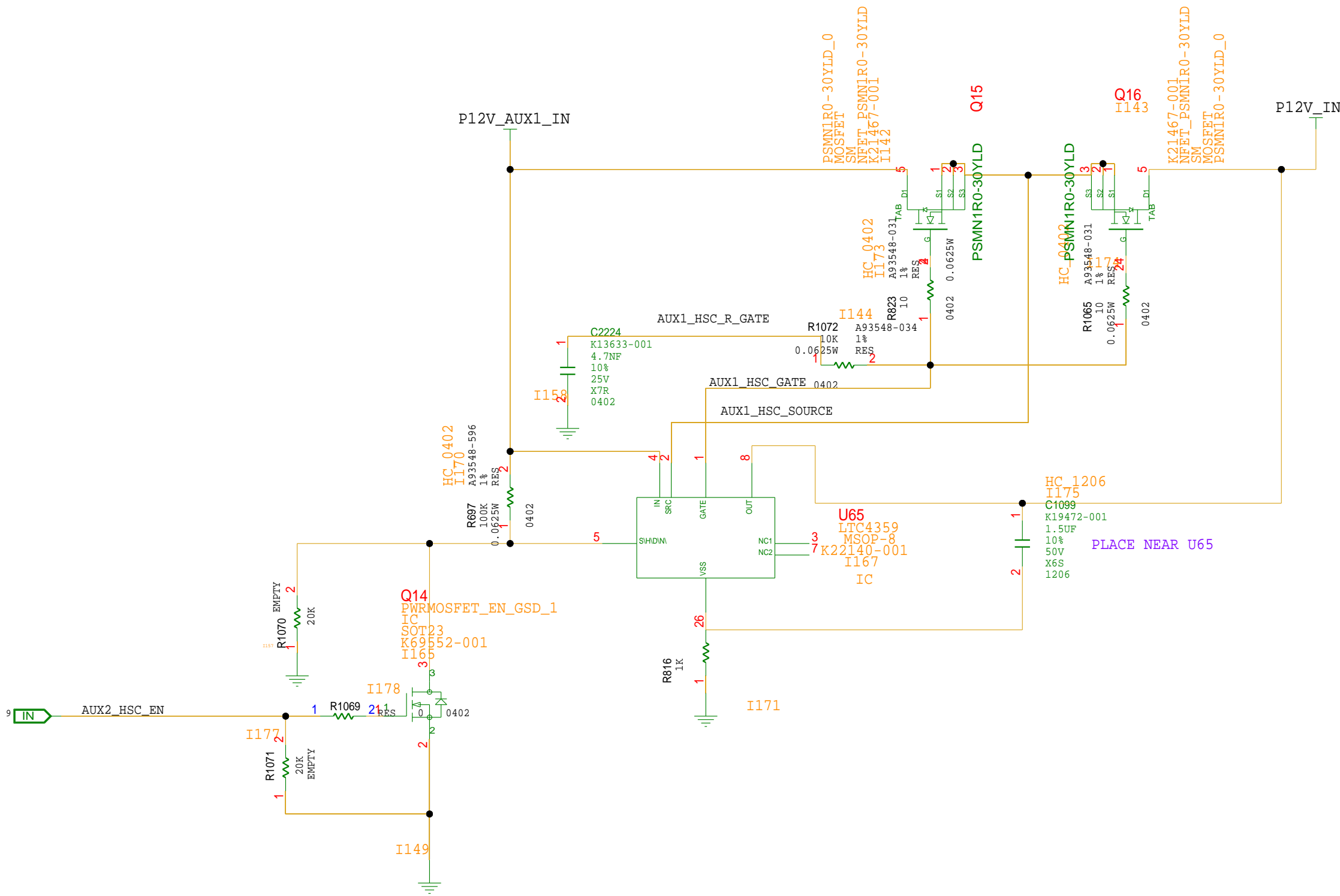
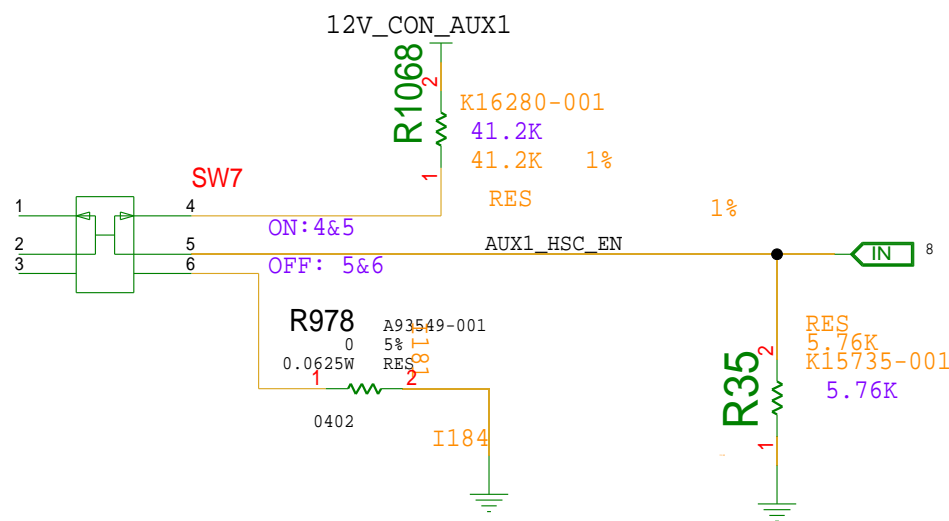
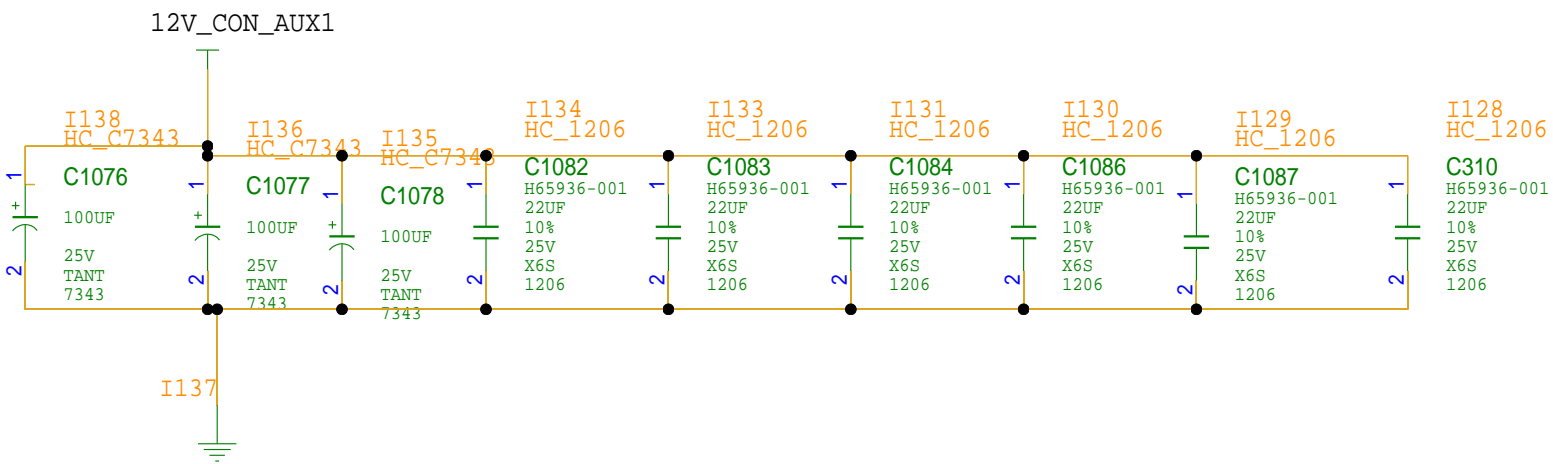
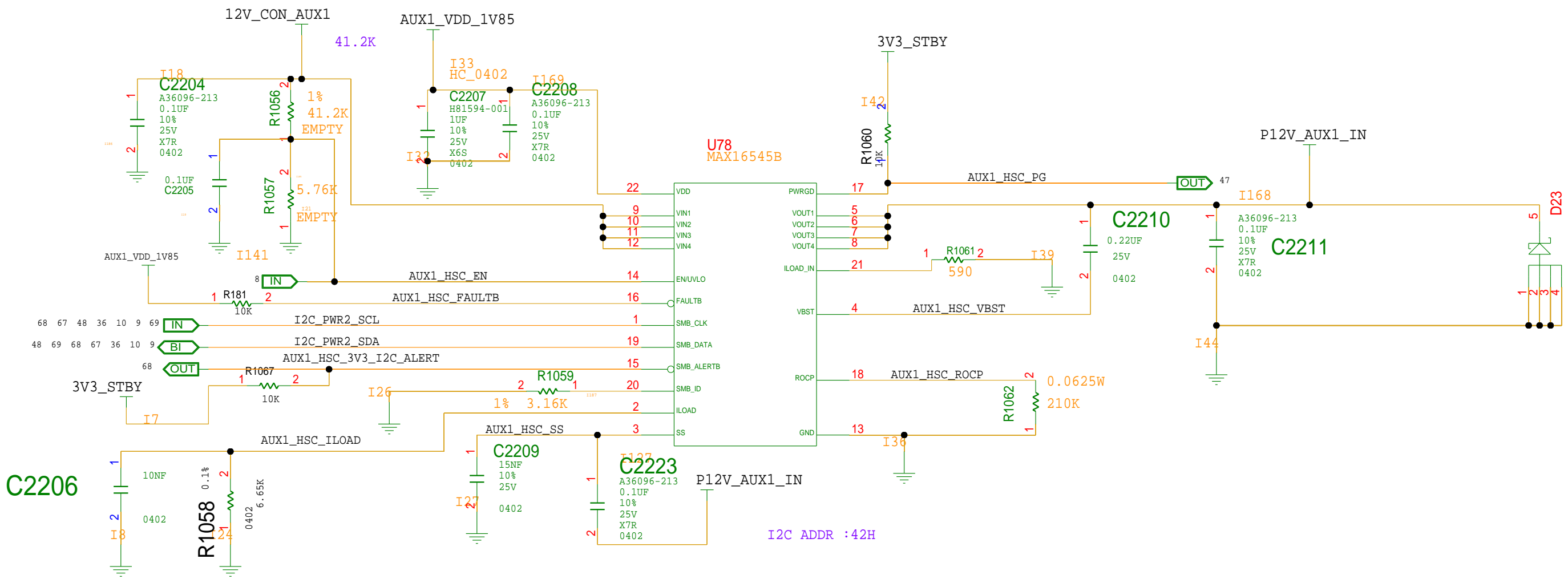
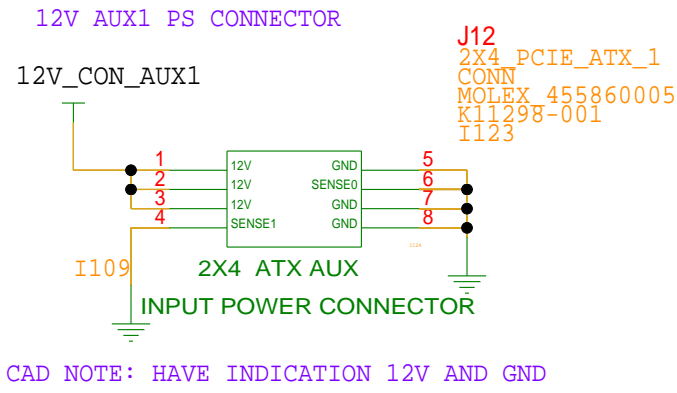
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POWER SUPPLY CONNECTOR



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HOTSWAP

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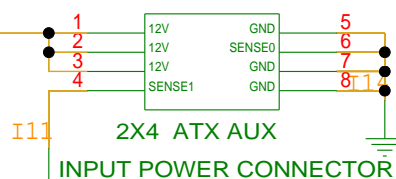
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12V AUX2 PS CONNECTOR

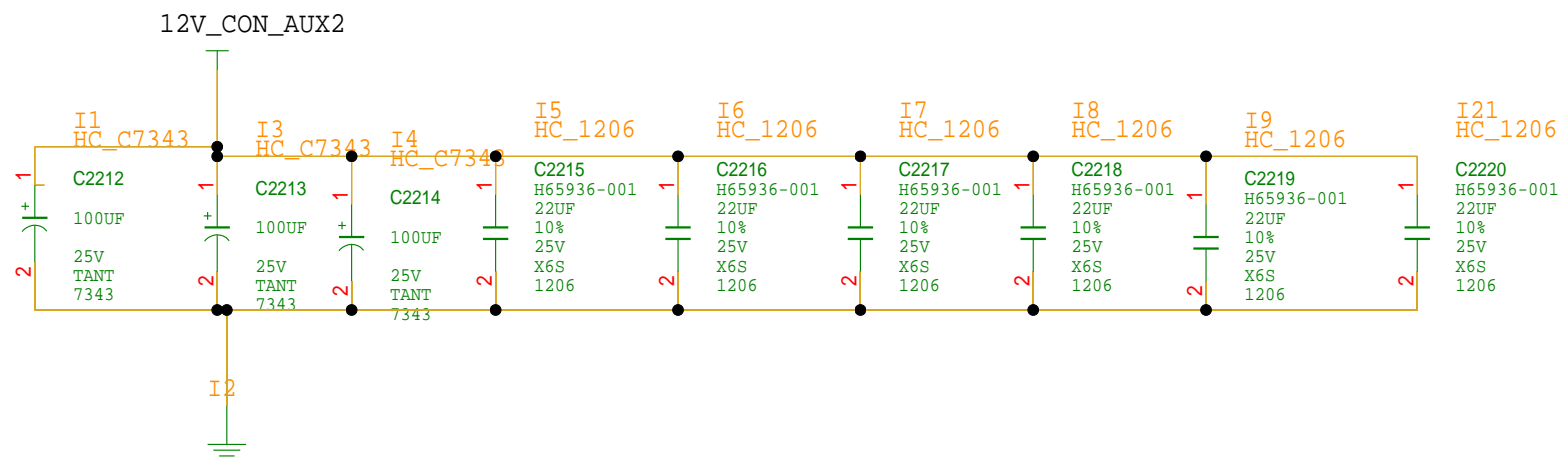
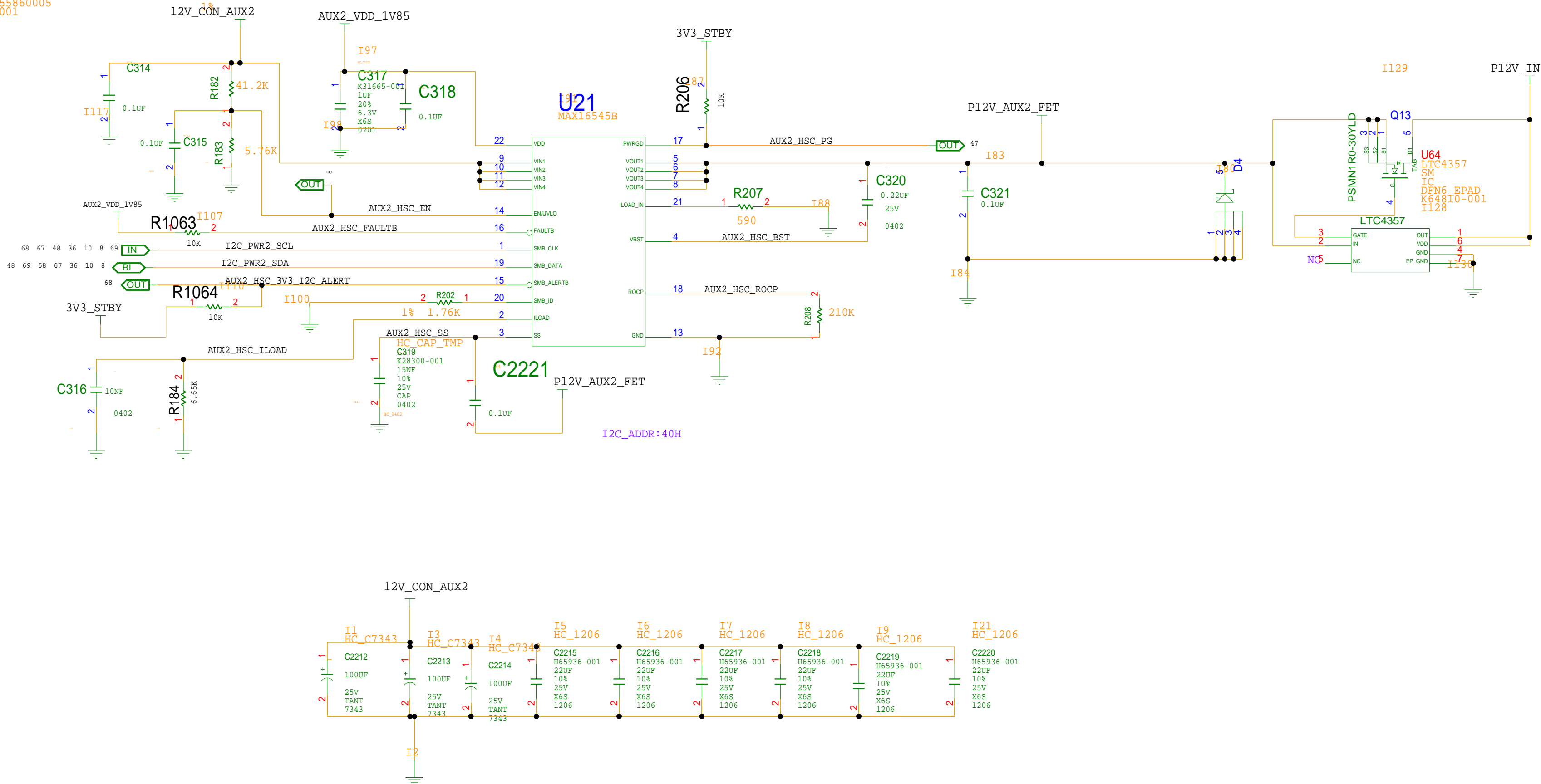
12V\_CON\_AUX2



CAD NOTE: HAVE INDICATION 12V AND GND

J3  
12V  
2X4 PCIE\_ATX\_1  
CONN  
MOLEX\_455860005  
R11298-001

## POWER SUPPLY CONNECTOR



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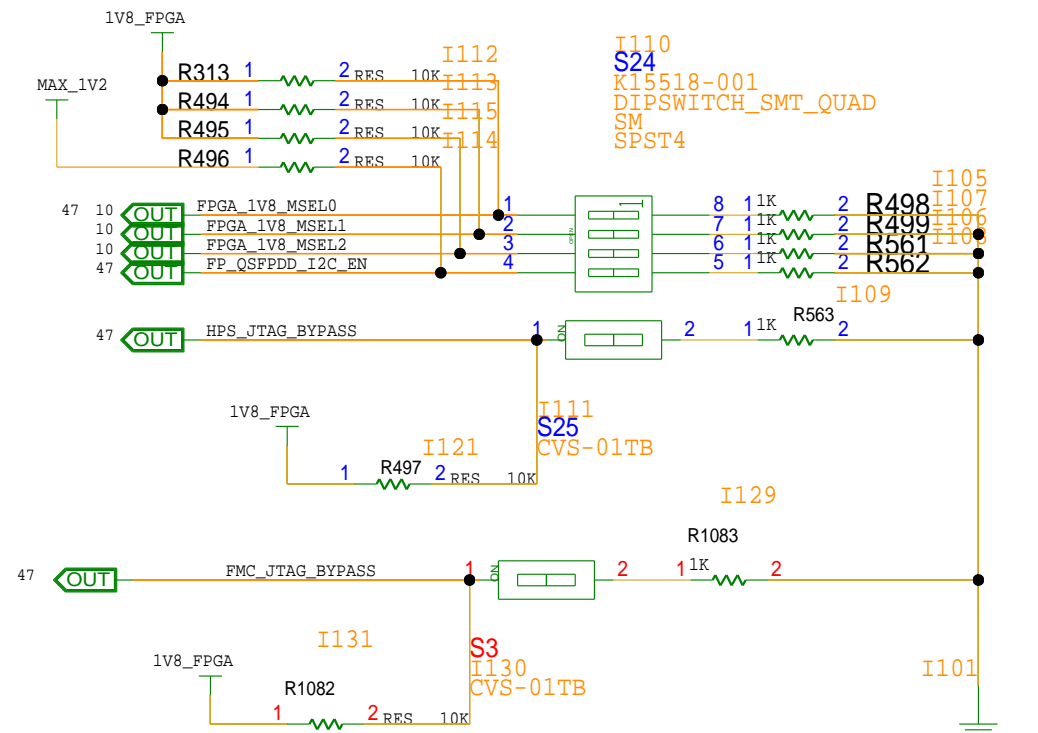
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CAD NOTE:  
RESISTORS PADSHARE





IN SAME ONE GROUP



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## FP82 BANK - 2B

I185  
BGA  
U1  
IC  
HC\_FP8\_4700A

1.2V

FV41	0B, DIFF, I0_2B, T1N, DQ48
FU42	0B, DIFF, I0_2B, T1P, DQ48
FV41	0B, DIFF, I0_2B, T2N, DQ48
G442	0B, DIFF, I0_2B, T2P, DQ48
FU44	0B, DIFF, I0_2B, T3N, DQ48
FV43	0B, DIFF, I0_2B, T3P, DQ48
G444	0B, DIFF, I0_2B, T4N, DQSGN48
FY43	0B, DIFF, I0_2B, T4P, DQSGN48
FV45	0B, CDR, DIFF, I0_2B, T5N, DQ48
FU46	0B, CDR, DIFF, I0_2B, T5P, DQ48
G446	0B, DIFF, I0_2B, T6N, DQ48
FY46	0B, DIFF, I0_2B, T6P, DQ48
FM39	0B, DIFF, I0_2B, T7N, DQ49
FL40	0B, DIFF, I0_2B, T7P, DQ49
FP39	0B, DIFF, I0_2B, T8N, DQ49
FR40	0B, DIFF, I0_2B, T8P, DQ49
FL42	0B, DIFF, I0_2B, T9N, DQ49
FM41	0B, DIFF, I0_2B, T9P, DQ49
FR42	0B, DIFF, I0_2B, T10N, DQSGN49
FP41	0B, DIFF, I0_2B, T10P, DQSGN49
FM43	0B, CDR, DIFF, I0_2B, T11N, DQ49
FL44	0B, CDR, DIFF, I0_2B, T11P, DQ49
FR44	0B, CDR, DIFF, I0_2B, T12N, DQ49
FP43	0B, DIFF, I0_2B, T12P, DQ49
FE40	0B, DIFF, I0_2B, T13N, DQ50
FF39	0B, DIFF, I0_2B, T13P, DQ50
FM39	0B, DIFF, I0_2B, T14N, DQ50
FU40	0B, DIFF, I0_2B, T14P, DQ50
FE42	0B, DIFF, I0_2B, T15N, DQ50
FU41	0B, DIFF, I0_2B, T15P, DQ50
FJ42	0B, PLL, ZB, T, CLKOUTIN, DIFF, I0_2B, T16N, DQSGN50
FM43	0B, PLL, ZB, T, CLKOUTPI, PLL, ZB, T, CLKOUTPI, PLL, ZB, T, FB1, DIFF, I0_2B, T16P, DQSGN50
FE43	0B, CDR, DIFF, I0_2B, T17N, DQ50
FE44	0B, RQZ, T, ZB, CDR, DIFF, I0_2B, T17P, DQ50
FJ44	0B, CLK, T, ZB, 1N, DIFF, I0_2B, T18N, DQ50
FM45	0B, CLK, T, ZB, 1P, DIFF, I0_2B, T18P, DQ50
EW40	0B, CLK, T, ZB, 0N, DIFF, I0_2B, T19N, DQ51
EY39	0B, CLK, T, ZB, 0P, DIFF, I0_2B, T19P, DQ51
FC40	0B, DIFF, I0_2B, T20N, DQ51
FB39	0B, DIFF, I0_2B, T20P, DQ51
EW42	0B, PLL, ZB, T, CLKOUTIN, DIFF, I0_2B, T21N, DQ51
FM43	0B, PLL, ZB, T, CLKOUTPI, PLL, ZB, T, CLKOUTPI, PLL, ZB, T, FB0, DIFF, I0_2B, T21P, DQ51
FC42	0B, DIFF, I0_2B, T22N, DQSGN51
FB41	0B, DIFF, I0_2B, T22P, DQSGN51
EW44	0B, CDR, DIFF, I0_2B, T23N, DQ51
EY43	0B, CDR, DIFF, I0_2B, T23P, DQ51
FC44	0B, DIFF, I0_2B, T24N, DQ51
FB43	0B, DIFF, I0_2B, T24P, DQ51

	IOB, CDR, DIFF_10_2B_B1N, DQ52	EY45
	IOB, CDR, DIFF_10_2B_B1P, DQ52	EV46
	IOB, DIFF_10_2B_B2N, DQ52	FC46
	IOB, DIFF_10_2B_B2P, DQ52	FB45
	IOB, DIFF_10_2B_B3N, DQ52	EV47
	IOB, DIFF_10_2B_B3P, DQ52	EV48
	IOB, PLL_2B_B_CLKOUT1P, DIFF_10_2B_B4N, DQ52	FB47
IOB, PLL_2B_B_CLKOUT1P, PLL_2B_B_CLKOUT1P, PLL_2B_B_CLKOUT1P, DIFF_10_2B_B4P, DQ52	IOB, DIFF_10_2B_B5N, DQ52	EV50
	IOB, R2Q_2, CDR, DIFF_10_2B_B5P, DQ52	EV51
	IOB, CLK_B_2B_1N, DIFF_10_2B_B6N, DQ52	FC50
	IOB, CLK_B_2B_1P, DIFF_10_2B_B6P, DQ52	FC51
	IOB, CLK_B_2B_0N, CDR, DIFF_10_2B_B7N, DQ53	FF45
	IOB, CLK_B_2B_0P, CDR, DIFF_10_2B_B7P, DQ53	FE46
	IOB, DIFF_10_2B_B8N, DQ53	FC46
	IOB, DIFF_10_2B_B8P, DQ53	FE48
	IOB, PLL_2B_B_CLKOUT1N, DIFF_10_2B_B9N, DQ53	FJ46
IOB, PLL_2B_B_CLKOUT1N, PLL_2B_B_CLKOUT1P, PLL_2B_B_CLKOUT1P, PLL_2B_B_CLKOUT1P, DIFF_10_2B_B9P, DQ53	IOB, DIFF_10_2B_B10N, DQ53	FJ47
	IOB, DIFF_10_2B_B10P, DQ53	FH48
	IOB, CDR, DIFF_10_2B_B11N, DQ53	FF48
	IOB, CDR, DIFF_10_2B_B11P, DQ53	FE50
	IOB, DIFF_10_2B_B12N, DQ53	FJ50
	IOB, DIFF_10_2B_B12P, DQ53	FH49
	IOB, CDR, DIFF_10_2B_B13N, DQ54	FL46
	IOB, CDR, DIFF_10_2B_B13P, DQ54	FM45
	IOB, DIFF_10_2B_B14N, DQ54	FP45
	IOB, DIFF_10_2B_B14P, DQ54	FR46
	IOB, DIFF_10_2B_B15N, DQ54	FL48
	IOB, DIFF_10_2B_B15P, DQ54	FM47
	IOB, DIFF_10_2B_B16N, DQ54	FR48
	IOB, DIFF_10_2B_B16P, DQ54	FP47
	IOB, CDR, DIFF_10_2B_B17N, DQ54	FL50
	IOB, CDR, DIFF_10_2B_B17P, DQ54	FM49
	IOB, DIFF_10_2B_B18N, DQ54	FR49
	IOB, DIFF_10_2B_B18P, DQ54	FR50
	IOB, CDR, DIFF_10_2B_B19N, DQ55	FU48
	IOB, CDR, DIFF_10_2B_B19P, DQ55	FV47
	IOB, DIFF_10_2B_B20N, DQ55	FY47
	IOB, DIFF_10_2B_B20P, DQ55	G448
	IOB, DIFF_10_2B_B21N, DQ55	FU50
	IOB, DIFF_10_2B_B21P, DQ55	FV49
	IOB, CDR, DIFF_10_2B_B22N, DQ55	FY49
	IOB, CDR, DIFF_10_2B_B22P, DQ55	FU52
	IOB, DIFF_10_2B_B24N, DQ55	FY51
	IOB, DIFF_10_2B_B24P, DQ55	G452

	EY45
	EW46
	FC46
	FB45
	EW48
	EY47
	FC48
	FB47
	EW50
	EY49
	FB49
	FC50
	FF45
	FE46
	FH45
	FJ46
	FE48
	FF47
	FJ48
	FH47
	FF49
	FE50
	FJ50
	FH49
	FL46
	FM45
	FP45
	FR46
	FL48
	FM47
	FR48
	FP47
	FL50
	FM49
	FP49
	FR50
	FU48
	FV47
	FY47
	GA48
	FU50
	FV49
	GA50
	FY49
	FV51
	FU52
	FY51
	GA52

IO BANK 2B  
8 OF 39

TBD\_FP8

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FP82 BANK - 2C

CAD NOTE:  
PLACE RESISTOR NEAR TO FP82

R1145  
240 RES 0402  
A93548-504

NO NEED TO CONNECT TO TP

R1357 A93548-043  
100 1% 0402

CAD NOTE:  
PLACE RESISTOR NEAR TO FP82  
FPGA BALLS ON THE BREAKOUT VIAS

I359

BGA  
U1

1C

HC\_FP8\_4700A

1.1V

LEFT RIGHT

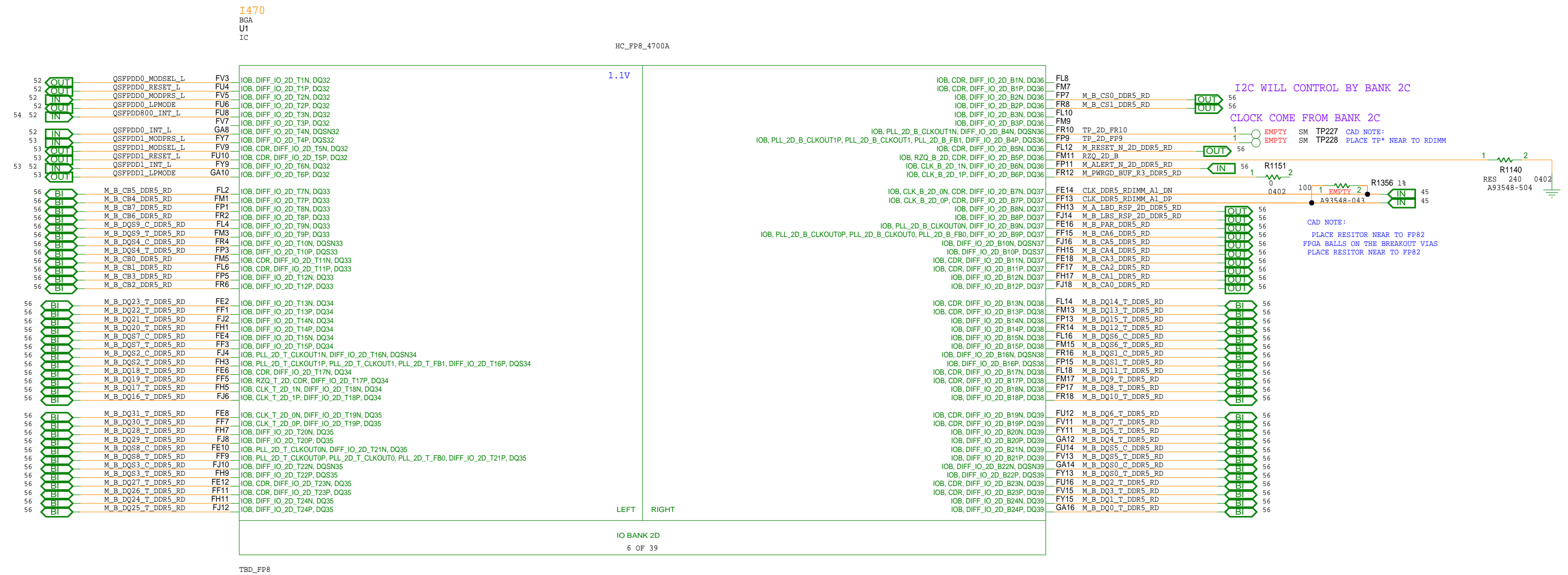
IO BANK 2C  
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TBD\_FP8

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## FP82 BANK - 2D



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B



A

A

FP82 BANK - 3A

4

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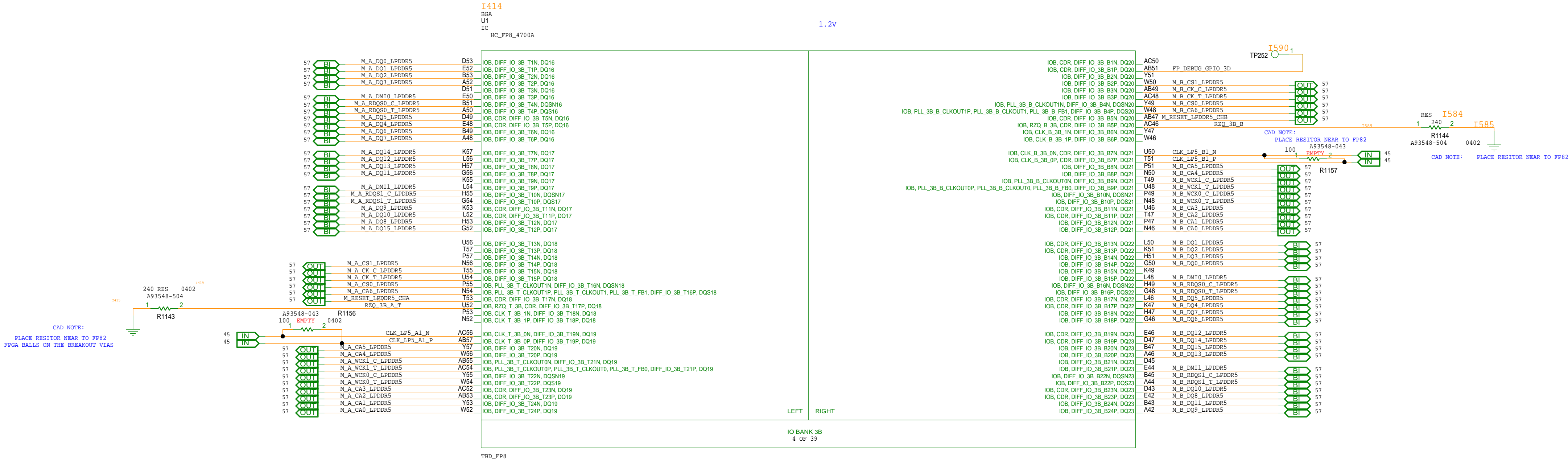
FP82 BANK - 3B

B

B

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A



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DOCUMENT NUMBER

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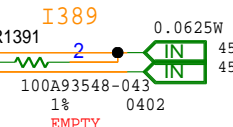


FP82 BANK - 3C

0.7

SHEET 17 OF 111

FP82 BANK - 3D





4

3

2

1

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FP82 BANK - NC  
FP82 BANK - SDM2

Configuration Mode		MSEL[2:0]
Passive	AVSTx32	000
	AVSTx16	101
	AVSTx8	110
	JTAG	111
Active	CvP	001
	SD MMC	100
	AS - Fast	001
	AS - Normal	011

BGA U1 IC HC_FP8_4700A		
Y9	NC	FC4
Y5	NC	FC26
Y45	NC	FC2
Y33	NC	FC18
Y3	NC	FC16
Y19	NC	FC14
Y17	NC	FC12
Y15	NC	FC10
Y11	NC	FB9
Y1	NC	FB7
W8	NC	FB5
W6	NC	FB3
W4	NC	FB25
W2	NC	FB17
W18	NC	FB15
W16	NC	FB13
W14	NC	FB11
W12	NC	FB1
W10	NC	FA8
V33	NC	FA6
U44	NC	FA4
U32	NC	FA26
T45	NC	FA2
T33	NC	FA16
R44	NC	FA14
R34	NC	FA12
R32	NC	FA10
R45	NC	EY9
N44	NC	EY7
N42	NC	EY5
N40	NC	EY3
N38	NC	EY25
N36	NC	EY17
N34	NC	EY15
N32	NC	EY13
L44	NC	EY11
K45	NC	EY1
H45	NC	EW8
G44	NC	EW6
FR38	NC	EW4
FR36	NC	EW26
FR34	NC	EW2
FR32	NC	EW18
FR30	NC	EW16
FP35	NC	EW14
FP33	NC	EW12
FP31	NC	EW10
FN36	NC	EV9
FN34	NC	EV7
FN37	NC	EV5
FN35	NC	EV3
FM33	NC	EV27
FM31	NC	EV17
FL36	NC	EV15
FL34	NC	EV13
FL32	NC	EV11
FJ32	NC	EV1
FJ30	NC	EU68
FJ28	NC	EU66
FJ26	NC	EU64
FH29	NC	EU62
FH27	NC	EU60
FH25	NC	EU58
FG30	NC	EU56
FG28	NC	EU54
FG26	NC	EU52
FF29	NC	EU50
FF27	NC	EU48
FF25	NC	EU46
FE28	NC	EU44
FE26	NC	EU42
FD27	NC	EU40
FC9	NC	EU26
FC6	NC	

26 OF 39

TBD\_FP8

BGA U1 IC HC_FP8_4700A		
EU24	NC	EN26
EU22	NC	EN26
EU20	NC	EM57
EU18	NC	EM55
EU16	NC	EM53
EU14	NC	EM51
ET69	NC	EM49
ET67	NC	EM47
ET65	NC	EM45
ET63	NC	EM43
ET61	NC	EM41
ET59	NC	EL56
ET57	NC	EL54
ET55	NC	EL52
ET53	NC	EL50
ET51	NC	EL48
ET49	NC	EL46
ET47	NC	EL44
ET45	NC	EL42
ET43	NC	EL40
ET41	NC	EL26
ET39	NC	EK55
ET37	NC	EK53
ET35	NC	EK51
ET33	NC	EK49
ET31	NC	EK47
ER88	NC	EK45
ER86	NC	EK43
ER84	NC	EK41
ER82	NC	EK25
ER80	NC	EJ66
ER58	NC	EJ64
ER56	NC	EJ42
ER54	NC	EJ40
ER52	NC	EJ26
ER50	NC	EH57
ER48	NC	EG42
ER46	NC	AR46
ER44	NC	AR28
ER42	NC	AR24
ER40	NC	AR22
ER38	NC	AR20
ER16	NC	AP23
EP69	NC	AP21
EP67	NC	AN48
EP65	NC	AN46
EP63	NC	AN44
EP61	NC	AN30
EP59	NC	AN28
EP57	NC	AN26
EP55	NC	AN24
EP53	NC	AN22
EP51	NC	AN20
EP49	NC	AM69
EP47	NC	AM63
EP45	NC	AM57
EP43	NC	AM49
EP41	NC	AM47
EP25	NC	AM45
EP17	NC	AM29
EN68	NC	AM27
EN66	NC	AM25
EN64	NC	AM23
EN62	NC	AM21
EN60	NC	AM19
EN58	NC	AL68
EN56	NC	AL64
EN54	NC	AL62
EN52	NC	AL58
EN50	NC	AL56
EN48	NC	AL54
EN46	NC	AL52
EN44	NC	AL50
EN42	NC	AL48
EN40	NC	

27 OF 39

TBD\_FP8

BGA U1 IC HC_FP8_4700A		
AL46	NC	AG60
AL44	NC	AG58
AL30	NC	AG56
AL28	NC	AG54
AL26	NC	AG52
AL24	NC	AG50
AL22	NC	AG48
AL20	NC	AG46
AL18	NC	AG44
AK69	NC	AG30
AK67	NC	AG28
AK65	NC	AG26
AK63	NC	AG24
AK61	NC	AG22
AK59	NC	AG20
AK57	NC	AG18
AK55	NC	AF69
AK53	NC	AF67
AK51	NC	AF65
AK49	NC	AF61
AK47	NC	AF59
AK45	NC	AF57
AK29	NC	AF55
AK27	NC	AF53
AK25	NC	AF51
AK23	NC	AF49
AK21	NC	AF47
AK19	NC	AF45
AK17	NC	AF29
AJ68	NC	AF27
AJ66	NC	AF25
AJ64	NC	AF23
AJ62	NC	AF21
AJ60	NC	AF19
AJ58	NC	AF17
AJ56	NC	AE68
AJ54	NC	AE66
AJ52	NC	AE64
AJ50	NC	AE62
AJ48	NC	AE60
AJ46	NC	AE58
AJ44	NC	AE56
AJ30	NC	AE54
AJ28	NC	AE52
AJ26	NC	AE50
AJ24	NC	AE48
AJ22	NC	AE46
AJ20	NC	AE30
AJ18	NC	AE28
AJ16	NC	AE26
AH69	NC	AE24
AH67	NC	AE22
AH65	NC	AE20
AH63	NC	AE18
AH61	NC	AE16
AH59	NC	AD19
AH57	NC	AD17
AH55	NC	AC2
AH53	NC	AC18
AB45	NC	AB45
AB3	NC	AB3
AB19	NC	AB19
AB17	NC	AB17
AB1	NC	AB1
AA4	NC	AA4
AA2	NC	AA2
AA18	NC	AA18
AA16	NC	AA16
AA10	NC	AA10
FN32	NC	FN32
P33	NC	P33
FK35	NC	FK35
T39	NC	T39

28 OF 39

TBD\_FP8

Pins	MSEL Function	Configuration Source Function			
		SDM_DC_EN=0	SDM_DC_EN=1		
		Avalon-ST x8	Avalon-ST x16/x32	AS (normal/ fast mode - CVP)	SD/MMC
SDM_IO0	—	PWRMGT_SCL	INIT_DONE	INIT_DONE	INIT_DONE
SDM_IO1	—	AVSTx8_DATA2	—	AS_DATA1	SDMMC_CFG_DATA1
SDM_IO2	—	AVSTx8_DATA0	—	AS_CLK	SDMMC_CFG_DATA0
SDM_IO3	—	AVSTx8_DATA3	—	AS_DATA2	SDMMC_CFG_DATA2
SDM_IO4	—	AVSTx8_DATA1	—	AS_DATA0	SDMMC_CFG_CMD
SDM_IO5	MSEL0	INIT_DONE/CONF_DONE	—	AS_nCS00	SDMMC_CFG_CCLK
SDM_IO6	—	AVSTx8_DATA4	—	AS_DATA3	SDMMC_CFG_DATA3
SDM_IO7	MSEL1	—	—	AS_nCS02	—
SDM_IO8	—	AVST_READY	—	AS_nCS03	SDMMC_CFG_DATA4
SDM_IO9	MSEL2	—	—	AS_nCS01	—
SDM_IO10	—	AVSTx8_DATA7	—	—	SDMMC_CFG_DATA7
SDM_IO11	—	AVSTx8_VALID	PWRMGT_SDA	PWRMGT_SDA	PWRMGT_SDA
SDM_IO12	—	PWRMGT_ALERT	PWRMGT_ALERT	PWRMGT_ALERT	PWRMGT_ALERT
SDM_IO13	—	AVSTx8_DATA5	—	—	SDMMC_CFG_DATA5
SDM_IO14	—	AVSTx8_CLK	PWRMGT_SCL	PWRMGT_SCL	PWRMGT_SCL
SDM_IO15	—	AVSTx8_DATA6	—	CvP_CONFDONE	SDMMC_CFG_DATA6
SDM_IO16	—	PWRMGT_SDA	CONF_DONE	CONF_DONE	CONF_DONE

Mon Jun 27 16:50:43 2022

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SIZE

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CODE

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DOCUMENT NUMBER

M60500

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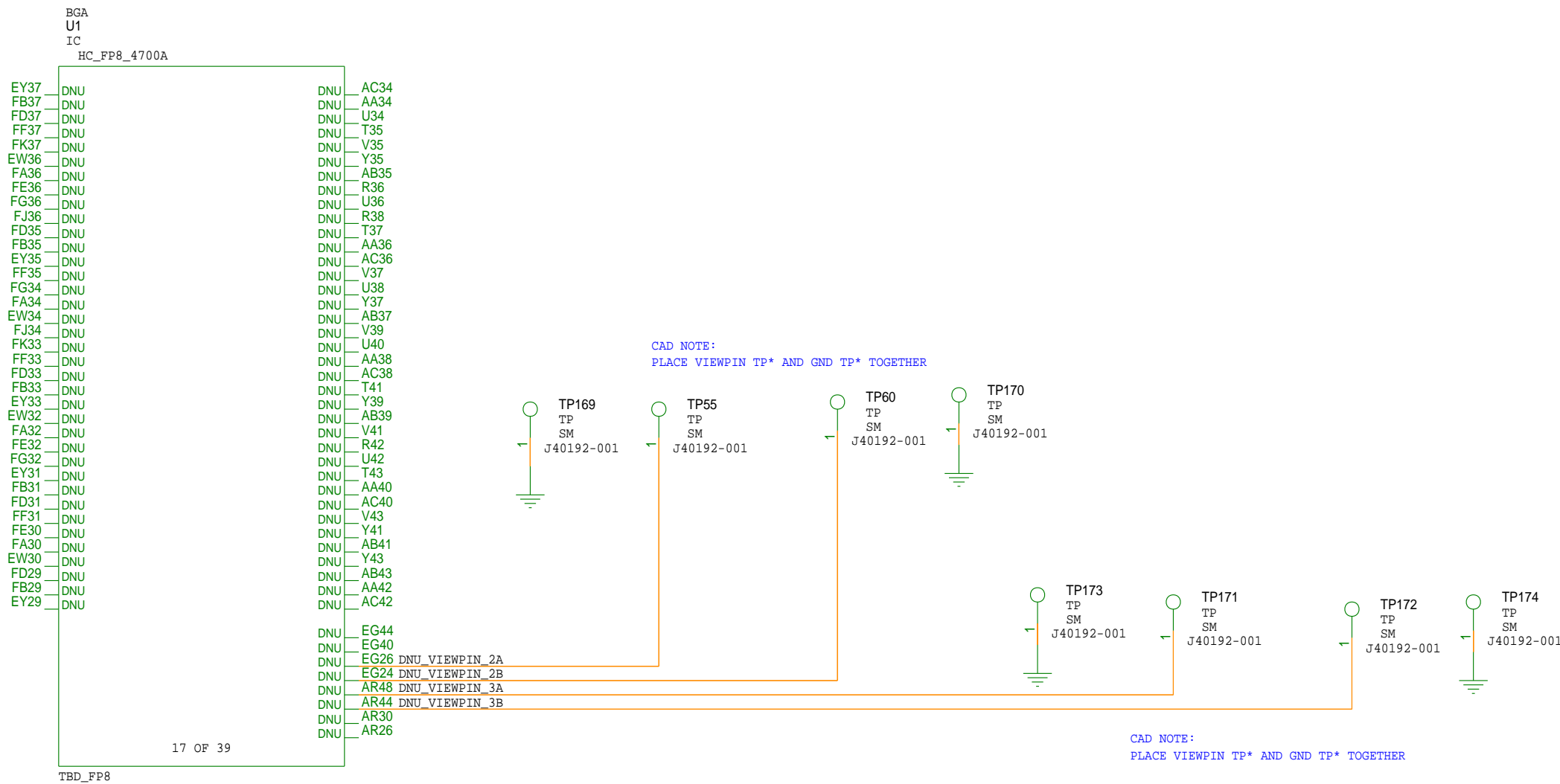
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SHEET

19 OF 111

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FP82 BANK - DNU

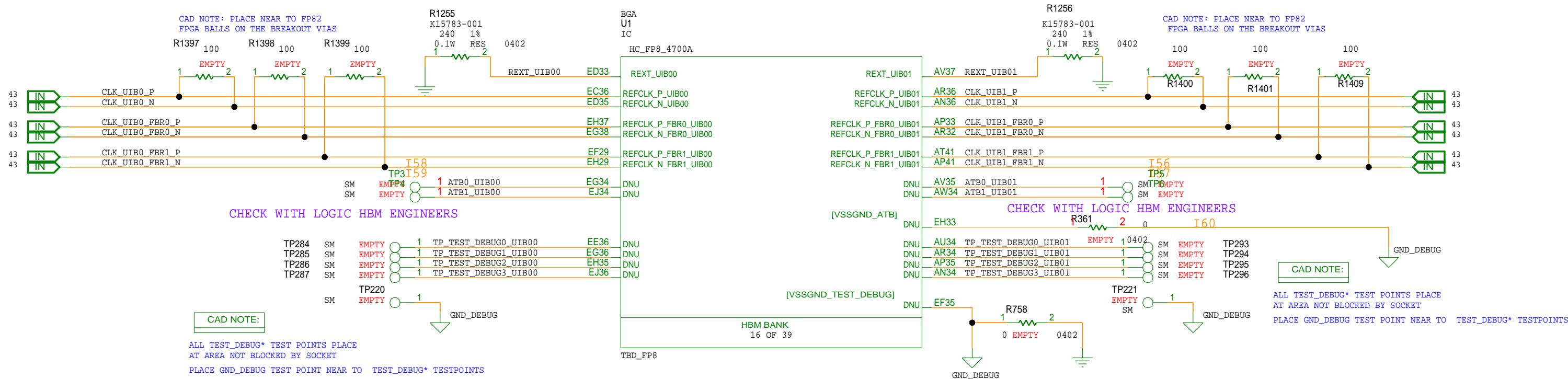


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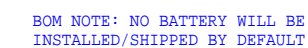
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FP82 BANK - DNU & REFCLK



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FP82 BANK - HPS



1



TRY TO ROUTE FMC\_RX/TX\_P(N)[0:7] AS SHORT AS POSSIBLE WITHIN 4.5 IN

FP82 BANK - F TILE - 12A

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TIM WILL CHECK Q1 CLOCK INPUT CAN BE USED FOR ALL Q  
MARY WILL CHECK AND EXCHANGE THE RESPONSE

FROM SI5395  
FROM FMC CONNECTOR

FROM FMC CONNECTOR  
FROM SI5518

GO TO 5392 INPUT

GO TO 5392 INPUT

DESIGN NOTE:

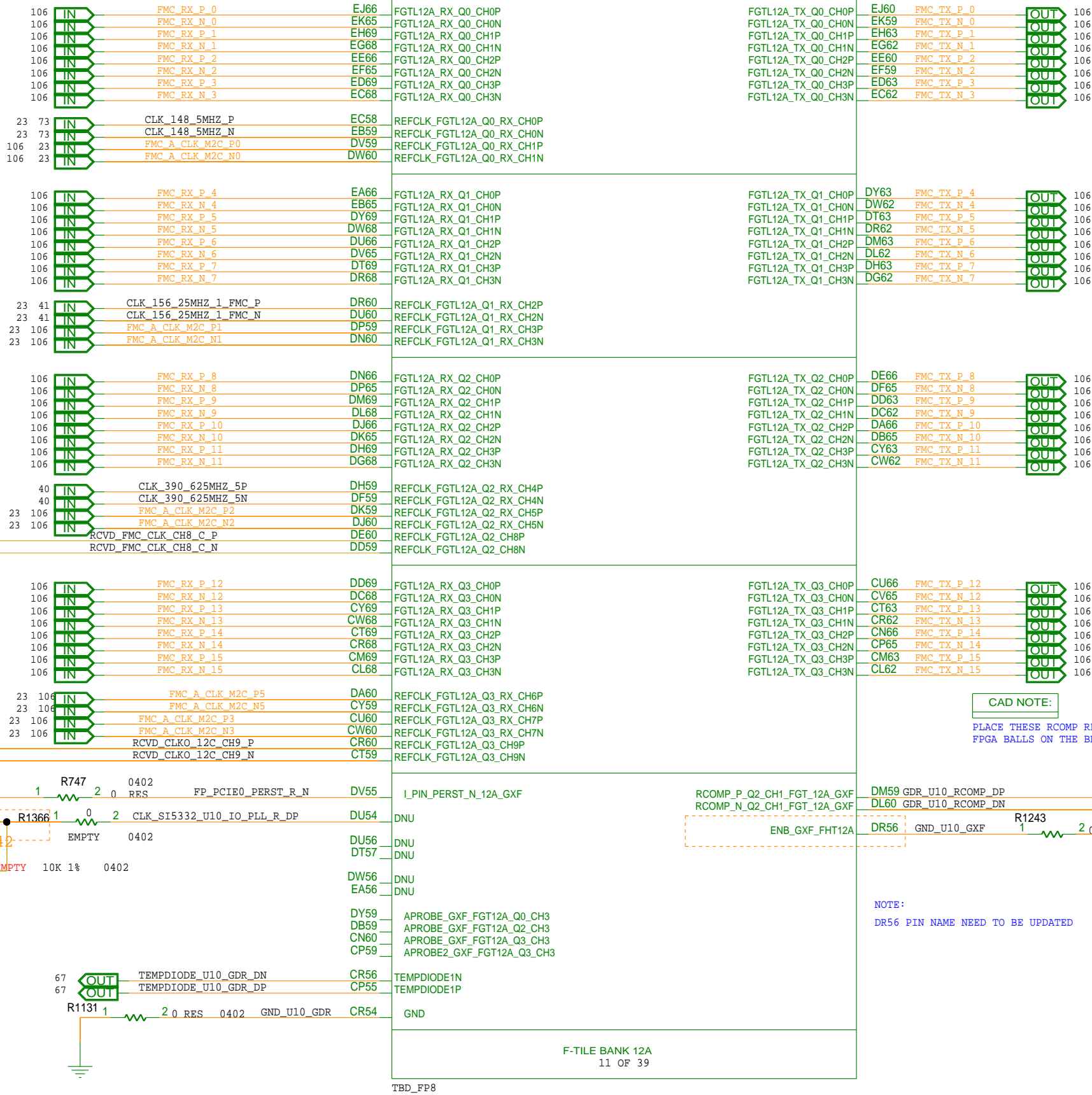
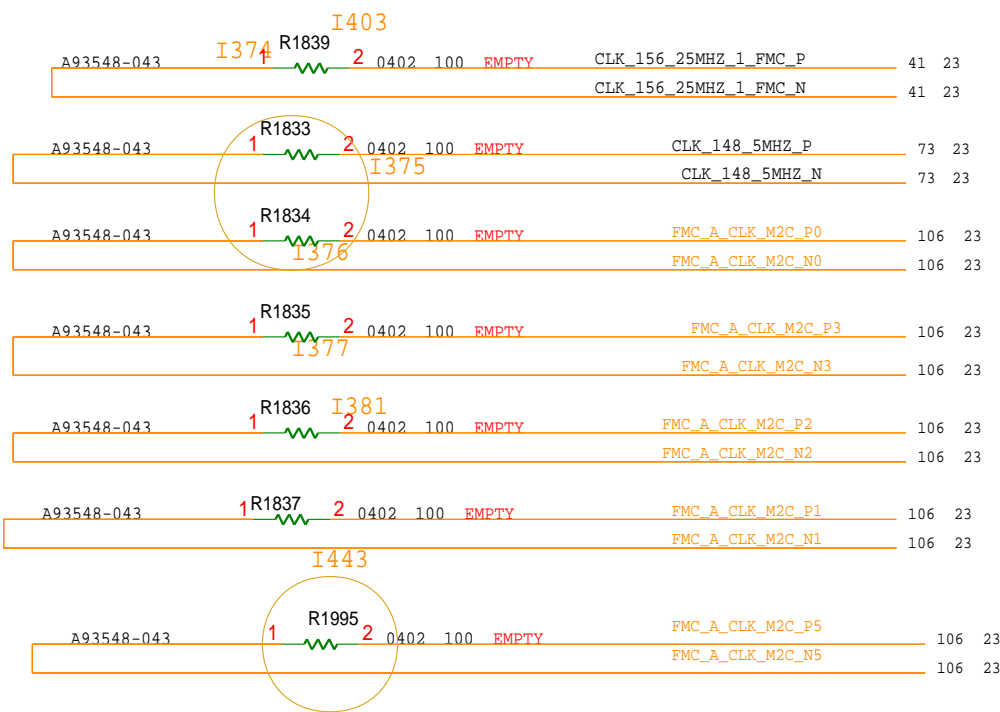
CAD NOTE:

CAD NOTE:

CAD NOTE:  
PAD SHARE

BREAKOUT EVERY TP\* NETS TO AN  
EXPOSED PAD ON BOTTOM SIDE  
ALL APROBE TEST POINTS PLACE  
TOP AREA NOT BLOCKED BY SOCKET

PUT 100 OHM TERMINATION CLOSE TO DESTINATION U1



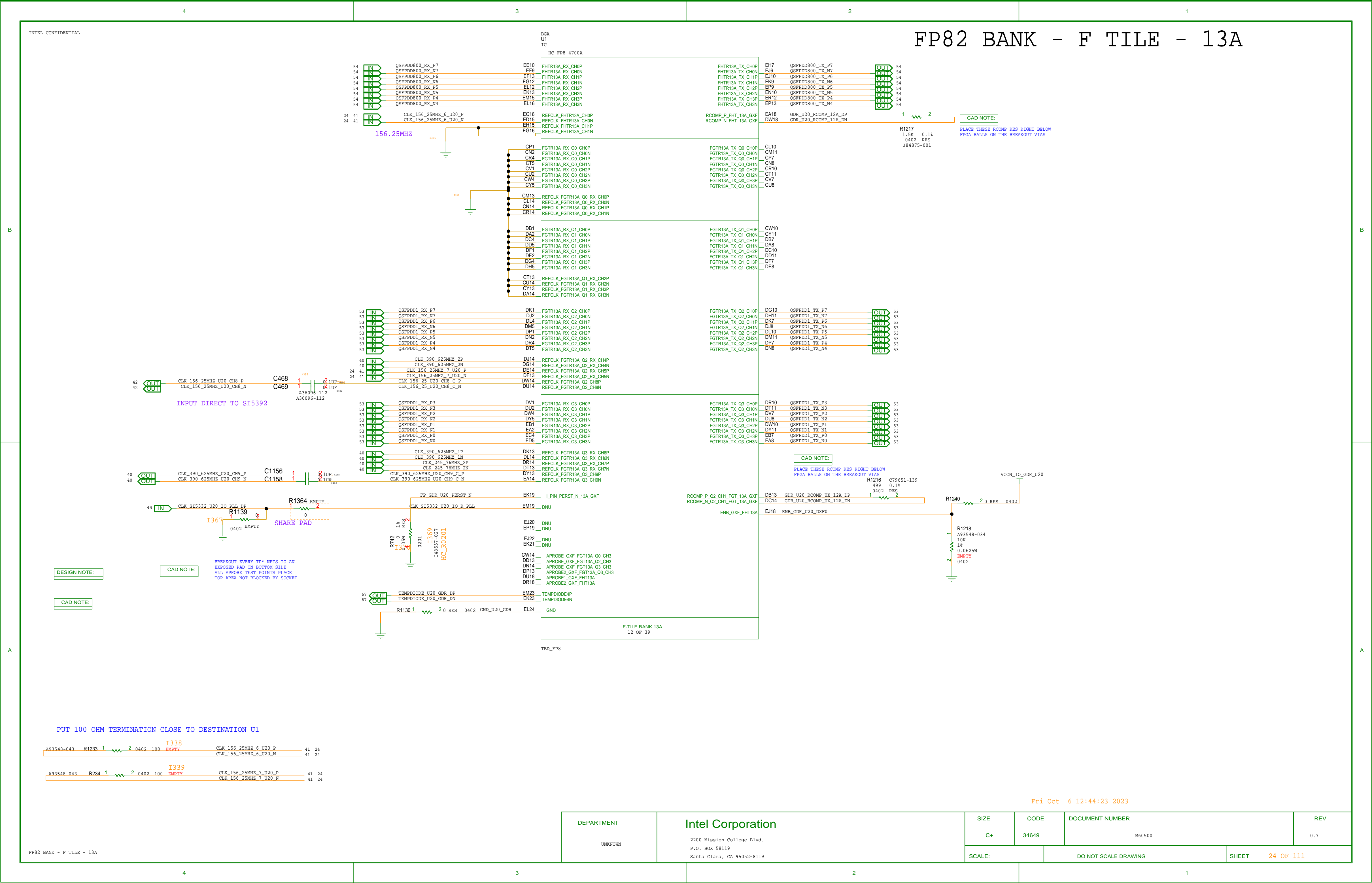
CAD NOTE:

PLACE THESE RCOMP RES RIGHT BELOW  
FPGA BALLS ON THE BREAKOUT VIAS

NOTE:  
DR56 PIN NAME NEED TO BE UPDATED

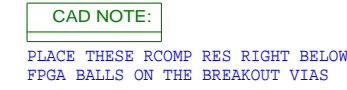
Fri Oct 6 12:44:23 2023

FP82 BANK - F TILE - 13A



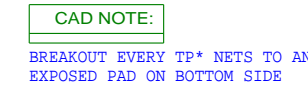


FP82 BANK - F TILE - 13C

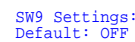


SHEET 25 OF 111

FP82 BANK - R TILE - 14C







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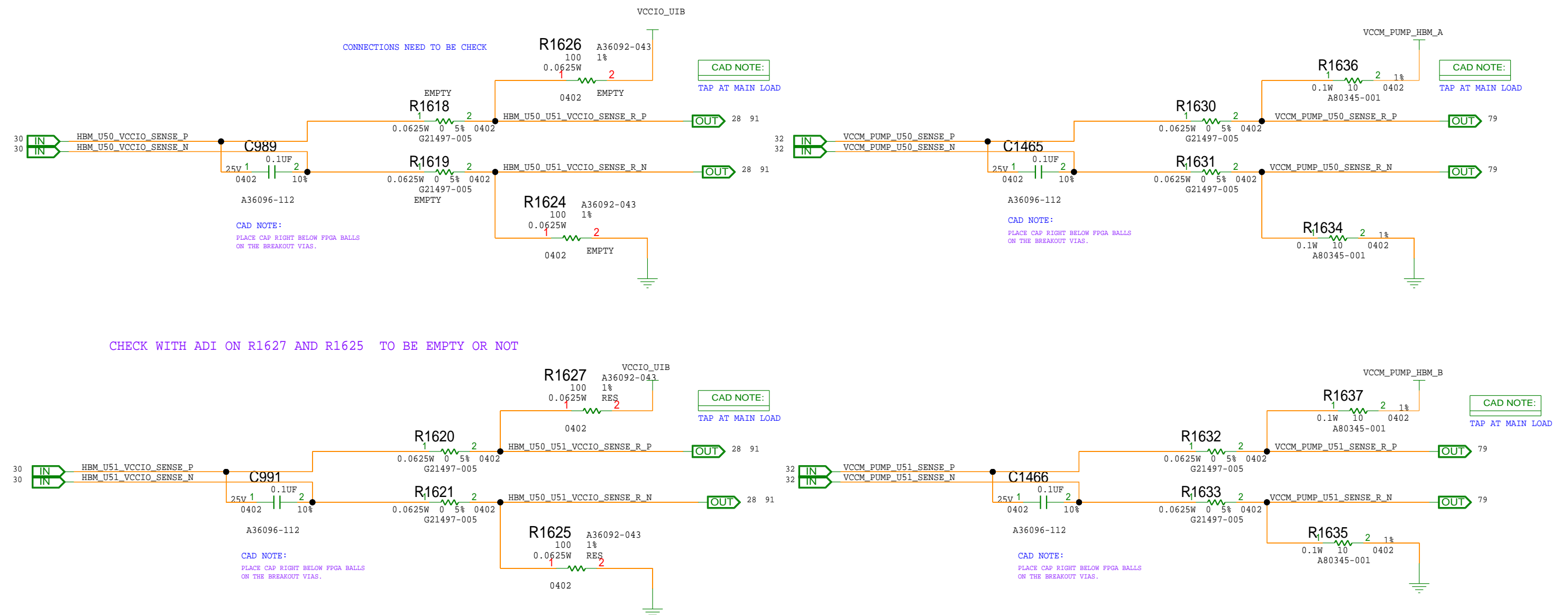
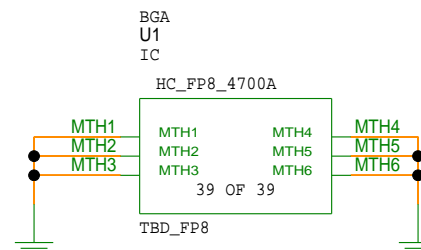
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7 OF 111



FP82 BANK - GND 2



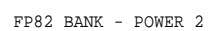
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UNKNOWN	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	SCALE:	DO NOT SCALE DRAWING		SHEET 28 OF 111

FP82 BANK - POWER 1



SHEET 29 OF 111

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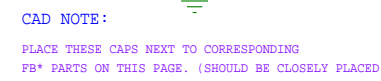


FP82 BANK - POWER 3



FP82 BANK - POWER 3

FP82 BANK - POWER 4



SHEET 32 OF 111

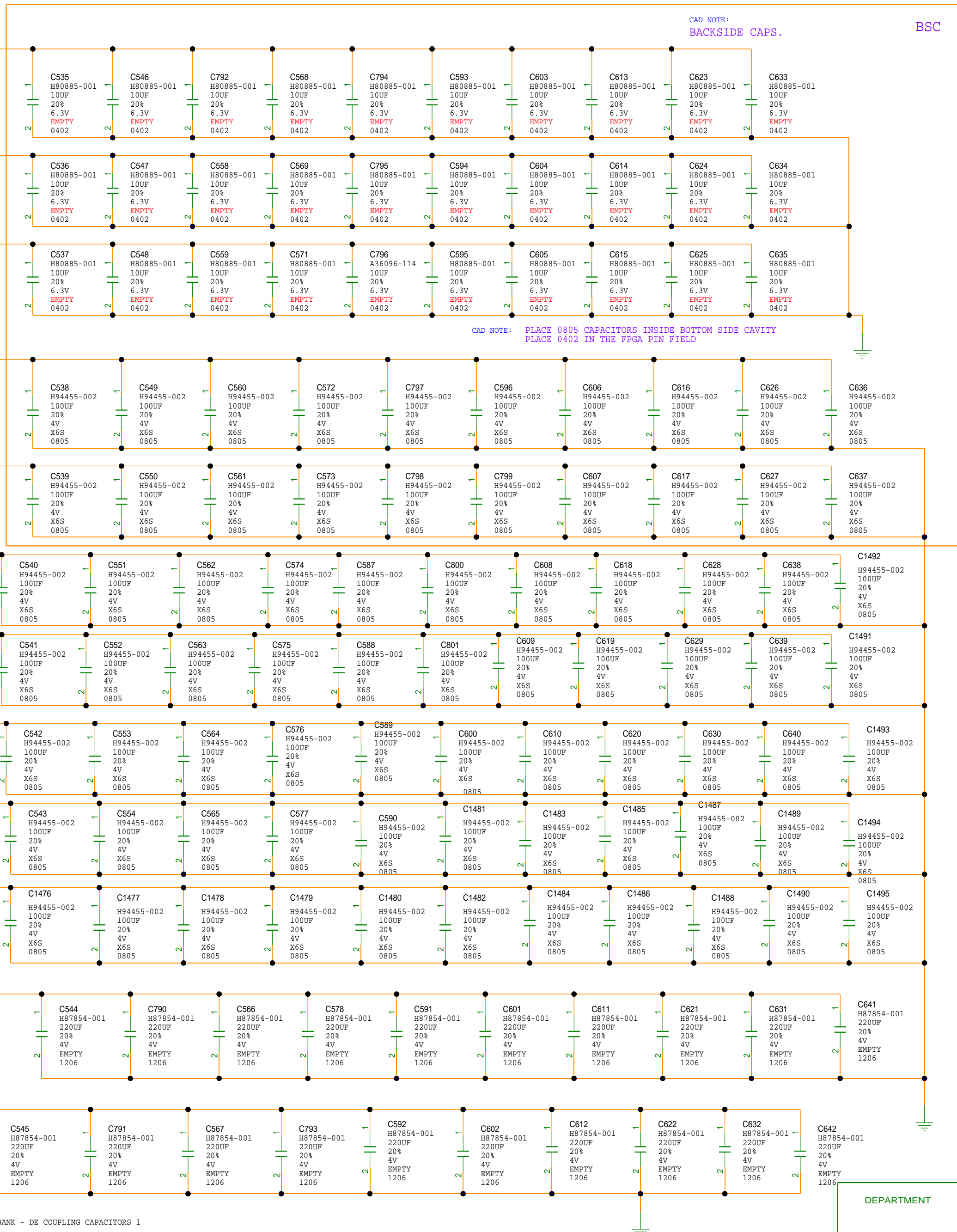
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## FPGA\_VCC

CAD NOTE:  
PERIPHERY CAPS.  
PLACE ON TOP SIDE SURROUNDING FPGA

AD NOTE:  
BACKSIDE CAPS.

BSC



FP82 BANK - DE COUPLING CAPACITORS 1

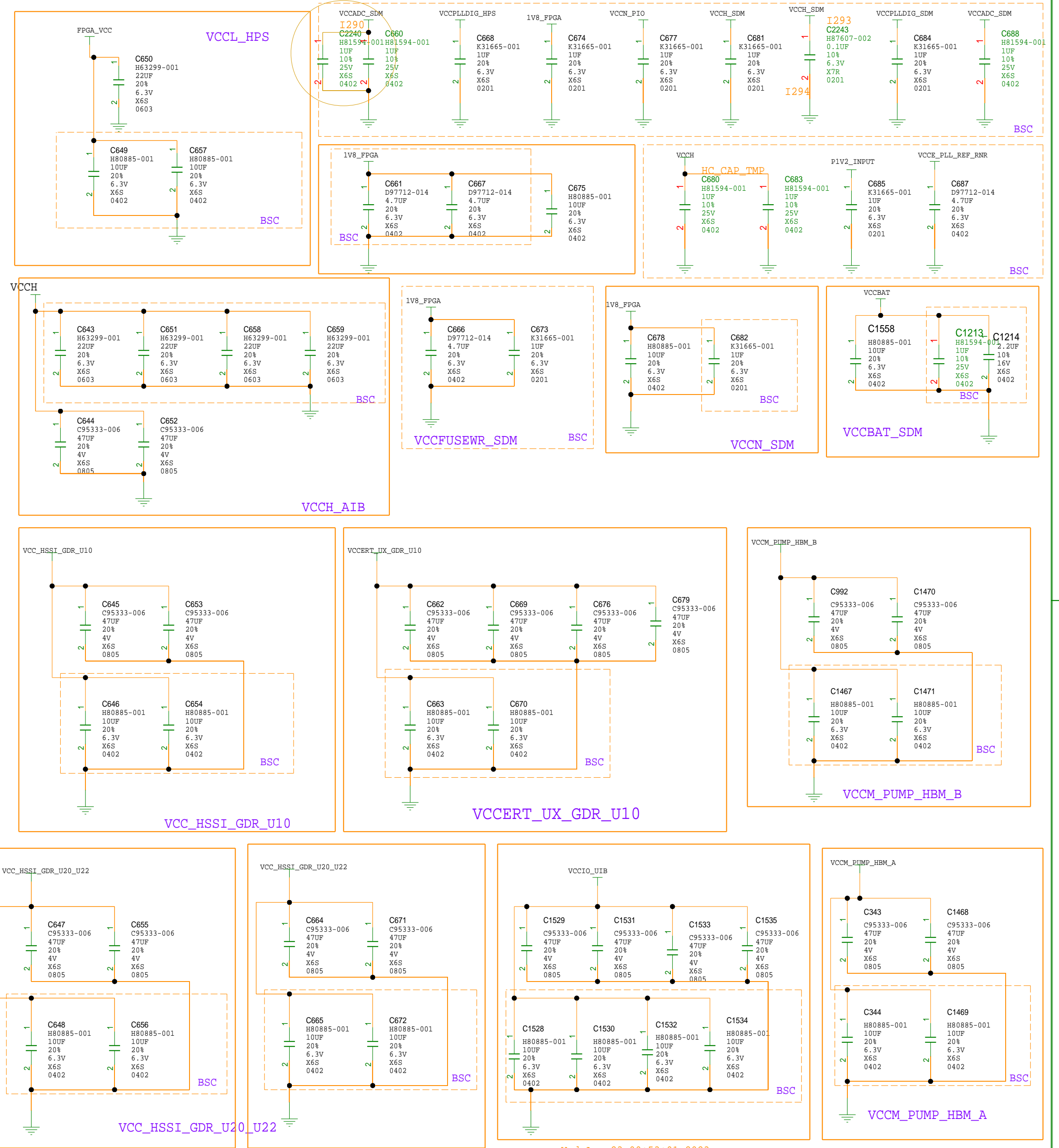
DEPARTMENT

UNKNOWN

# Intel Corporation

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## FP82 BANK - DECOUPLING CAPACITORS 1

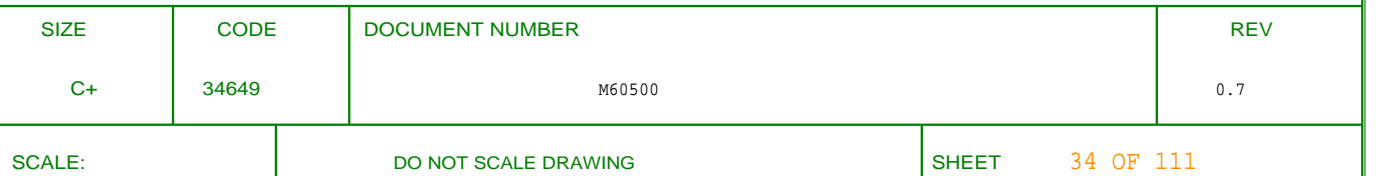


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SCALE:		DO NOT SCALE DRAWING	SHEET 33 OF 111	



B



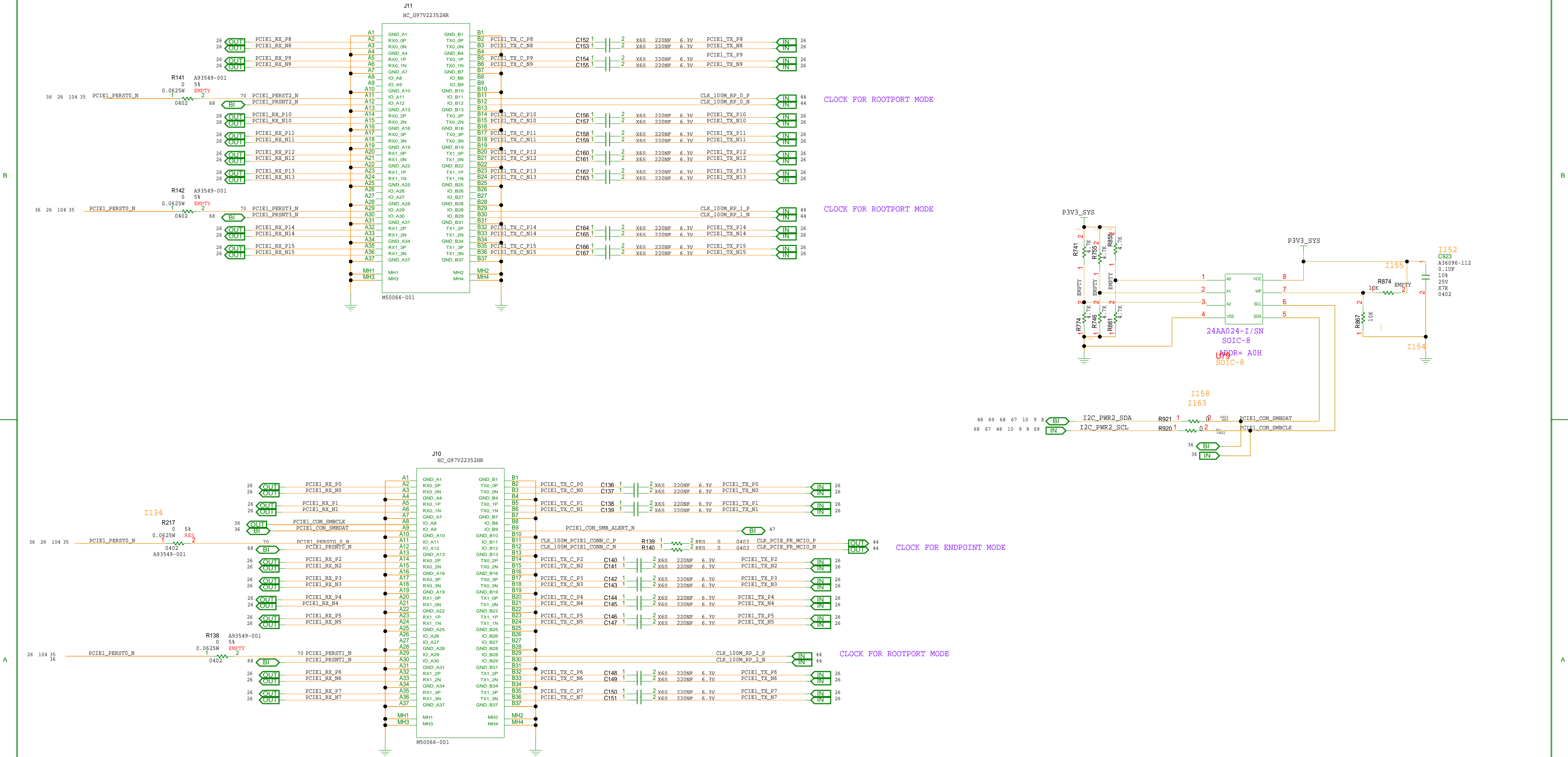
PCIE EDGE GOLD FINGER



35 OF 111

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# MCIO CONNECTORS



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MCIO CONNECTORS

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DOCUMENT NUMBER

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REV

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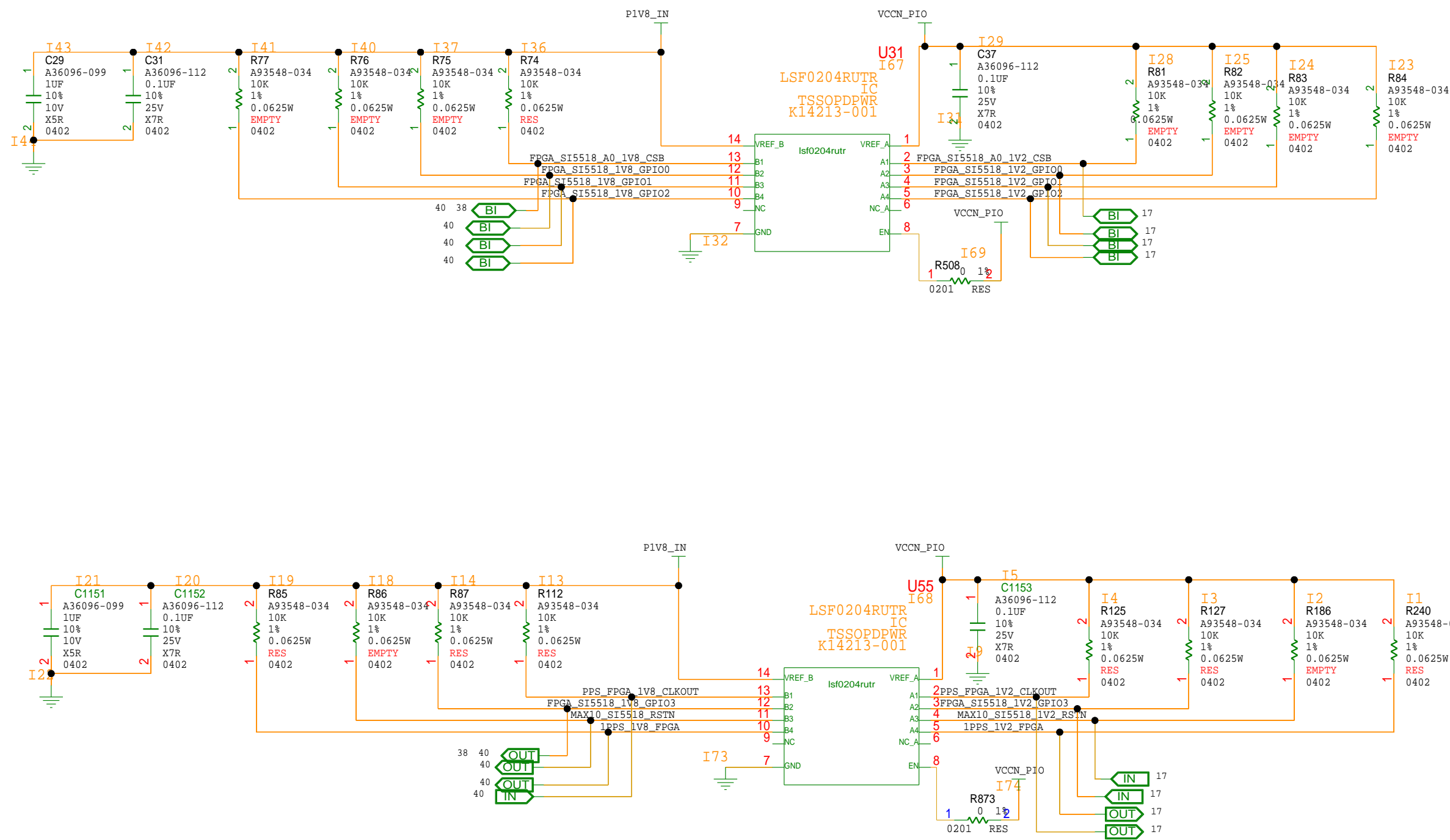
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36 OF 111



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DOCUMENT NUMBER

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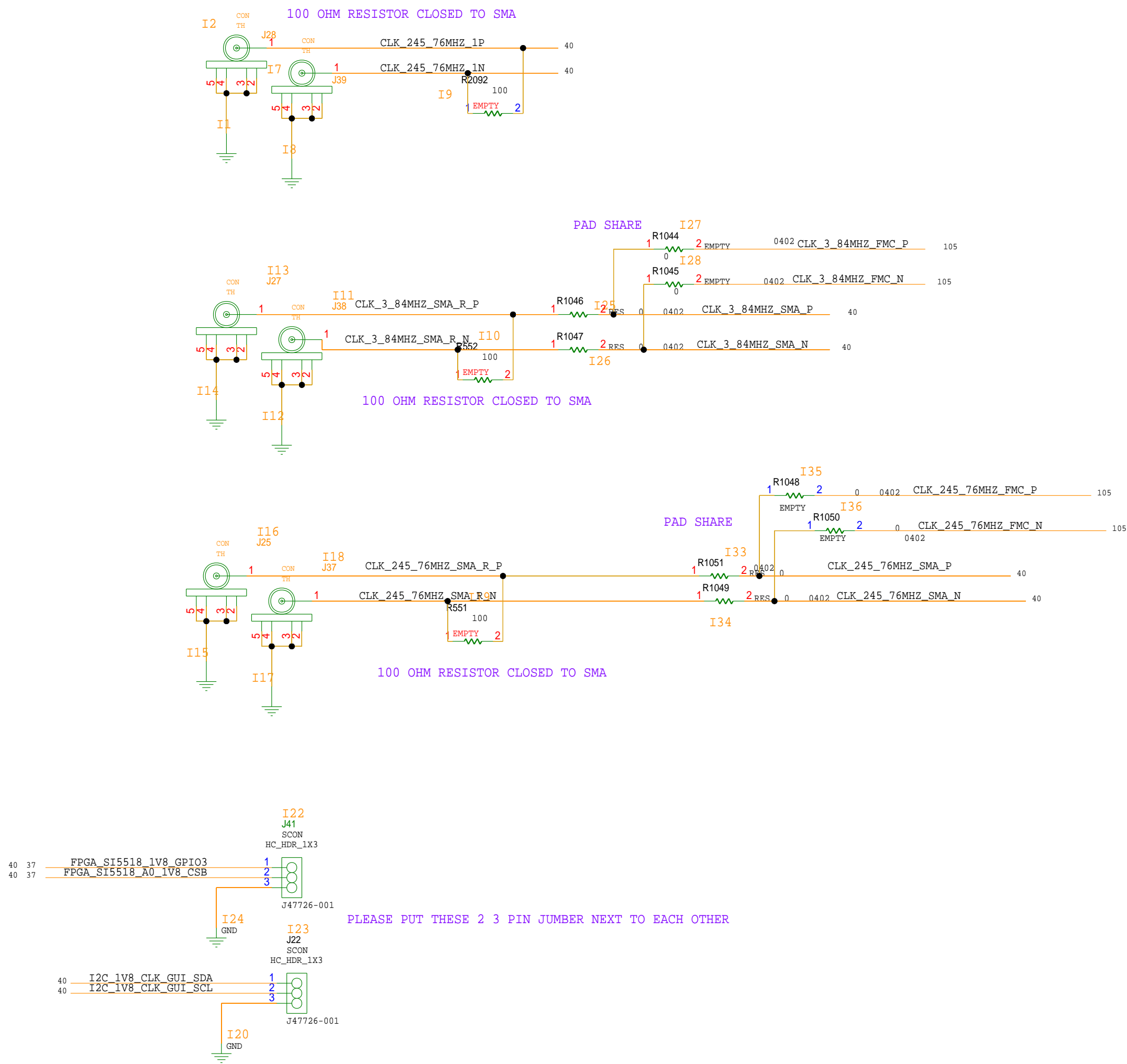
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DOCUMENT NUMBER

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38 OF 111

B



A



B



1

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		SCALE:		DO NOT SCALE DRAWING	SHEET 40 OF 111	

B



A

SIZE	CODE	DOCUMENT NUMBER	REV
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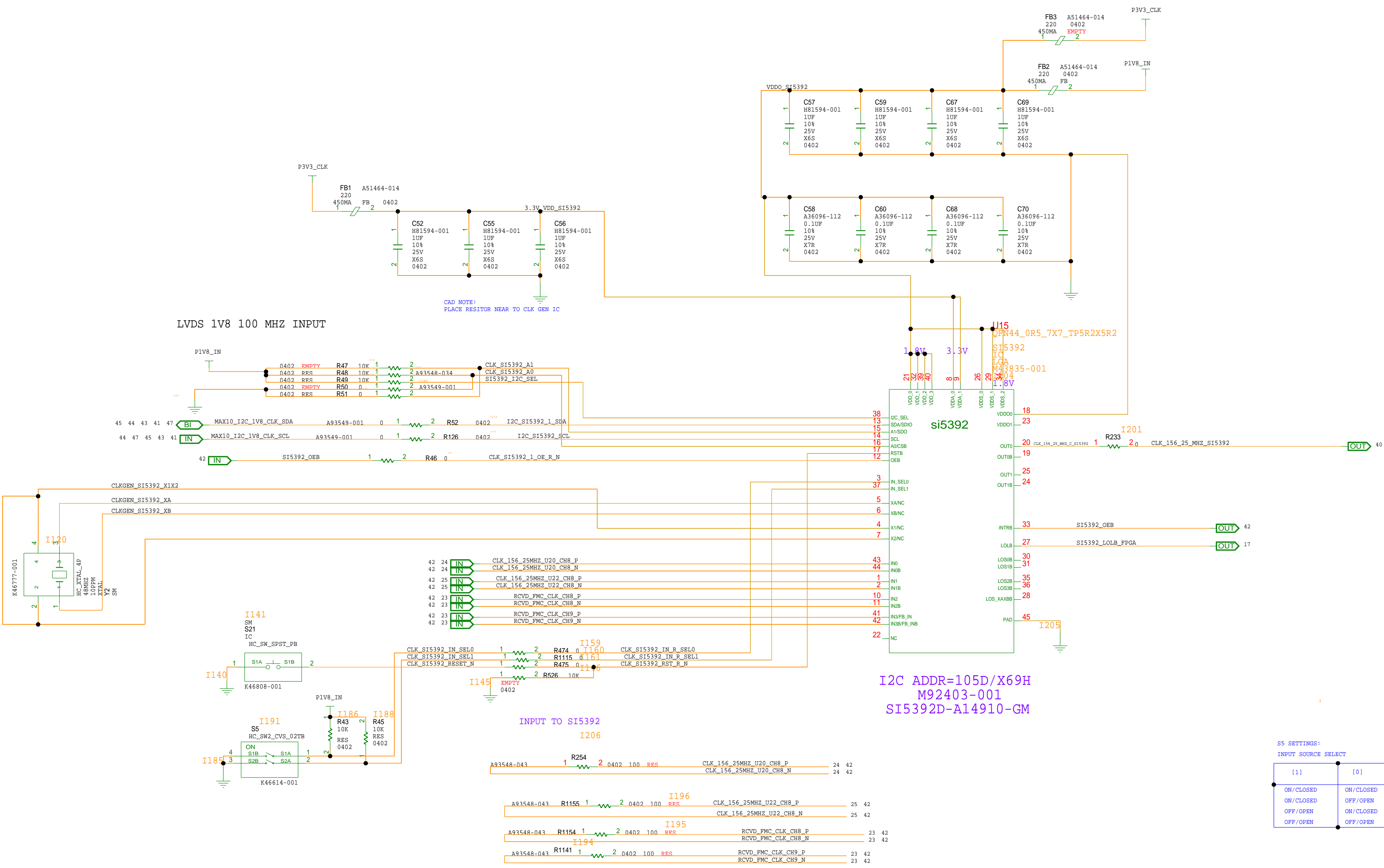
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REV  
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UNTITLED

SYSTEM CLOCKS 1



S16 SETTINGS:

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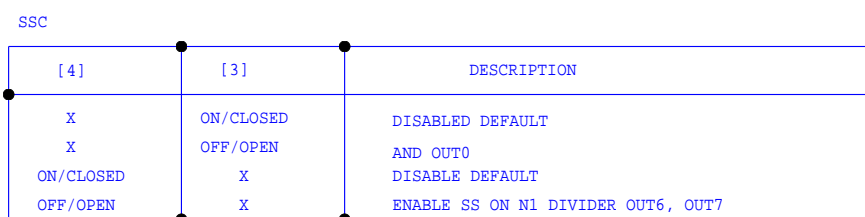


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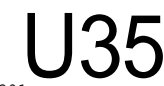
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SYSTEM CLOCKS 1



44 OF 111

SYSTEM CLOCKS 3

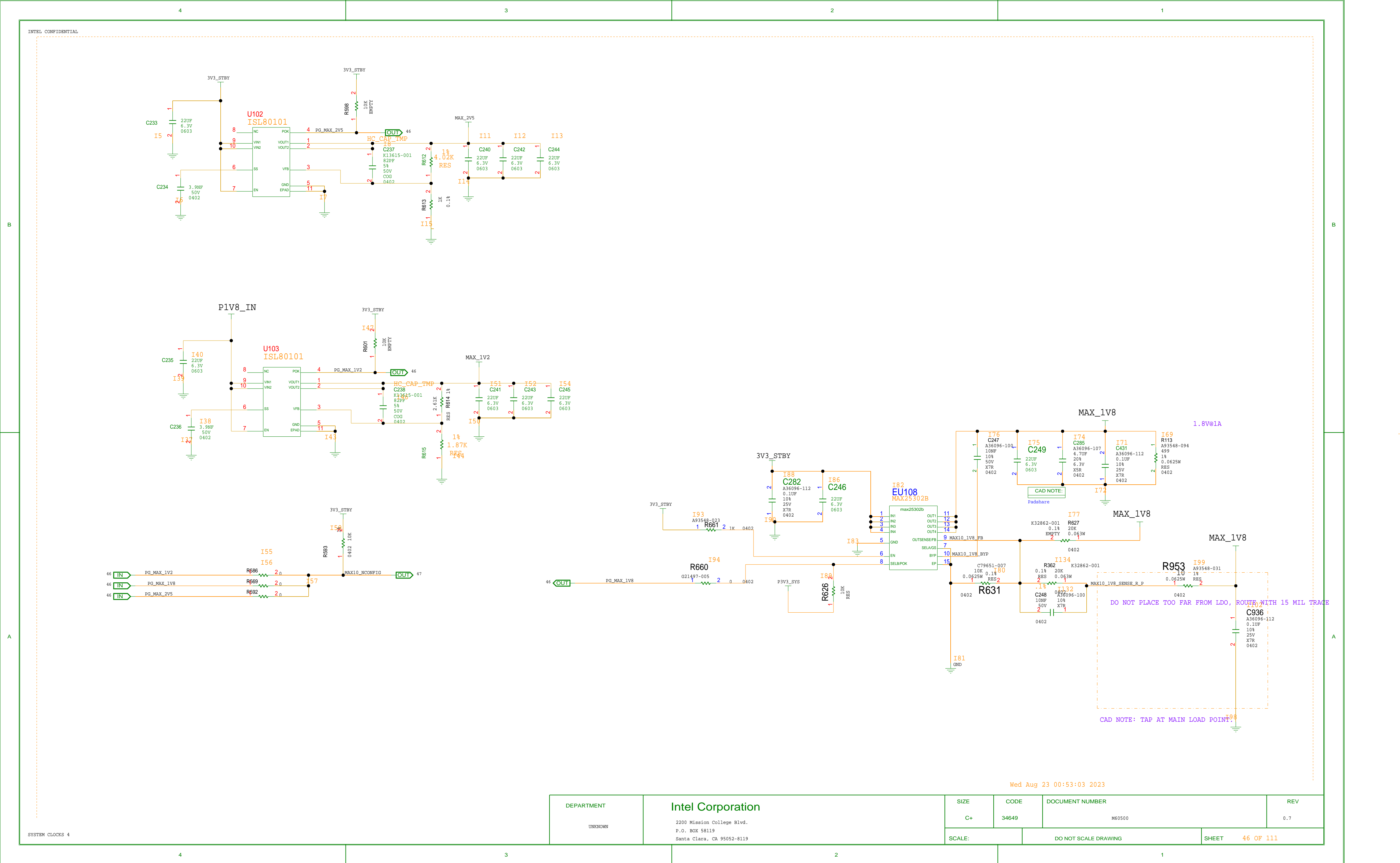


N33424-001  
I2C ADDRESS 0X76  
SI5391B-A15531-GM

SHEET 45 OF 111



CR-46 : @FP82\_MIDV\_L1B.FP8DK(SCH\_1):PAGE46



Wed Aug 23 00:53:03 2023

4

3

2

1

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10M50DAF256I7G  
U84

U84

10M50DAF256I7G

10M50DAF256I7G  
U84

10M50DAF256I7G  
U84

I1269  
10M50DAF256I7G  
U84

U84

10M50DAF256I7G  
U84

10M50DAF256I7G  
U84

10M50DAF256I7G  
U84

PLACE R1055 CLOSED TO U84

CHECK TO SEE IF WE NEED THE SECOND FLASH

U84

U84

respective primary load points.

Fri Oct 6 12:44:23 2023

BOARD B2B CONN - POWER

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47 OF 111

E



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B

B

A

A

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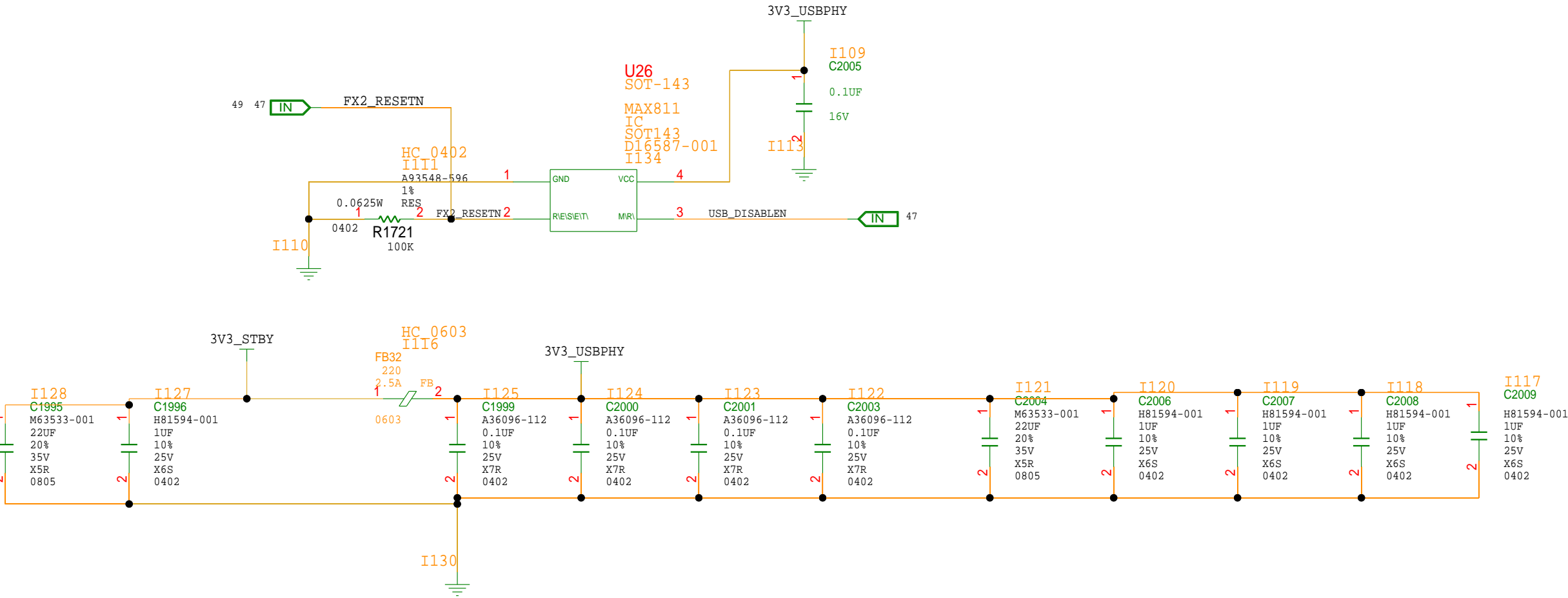
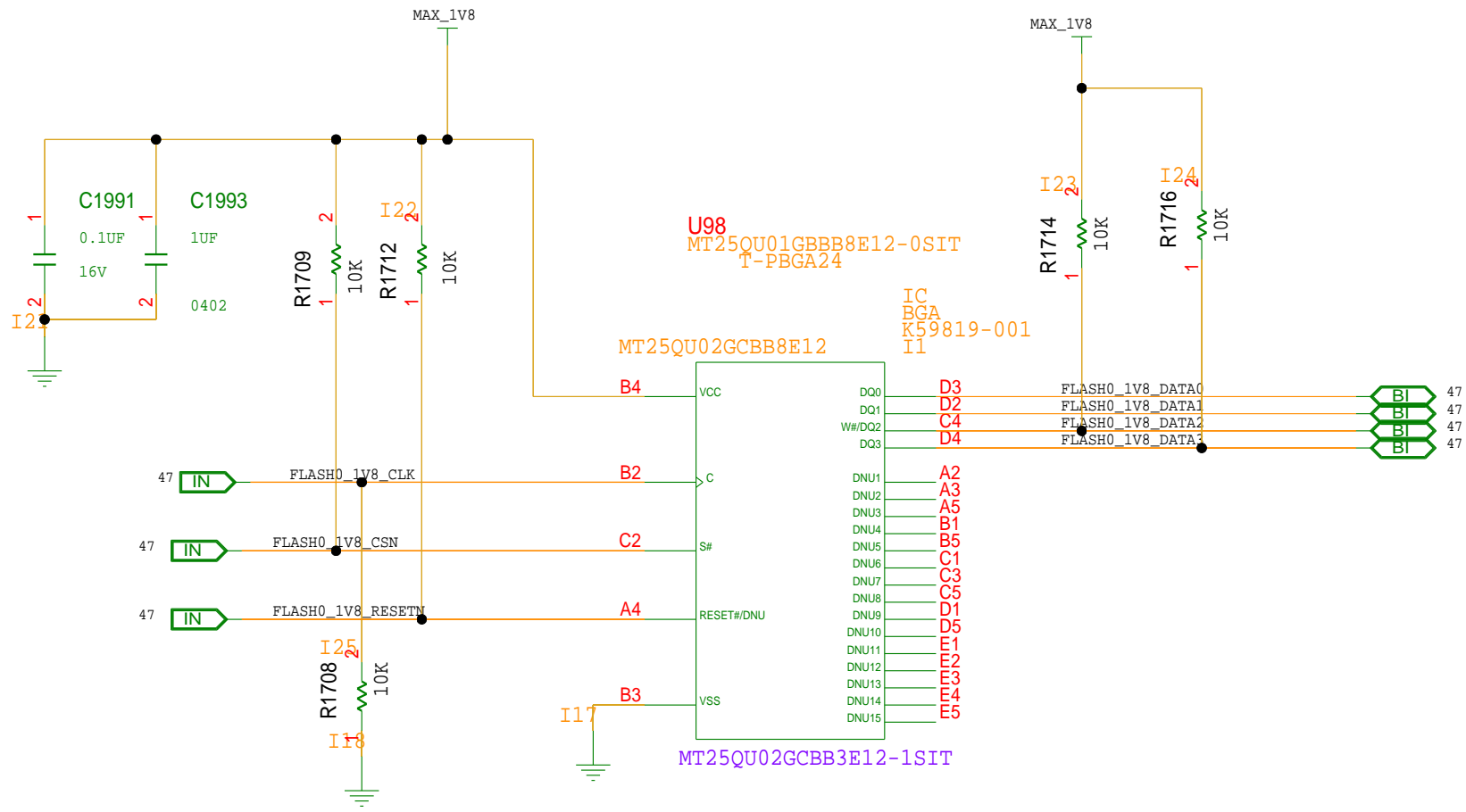
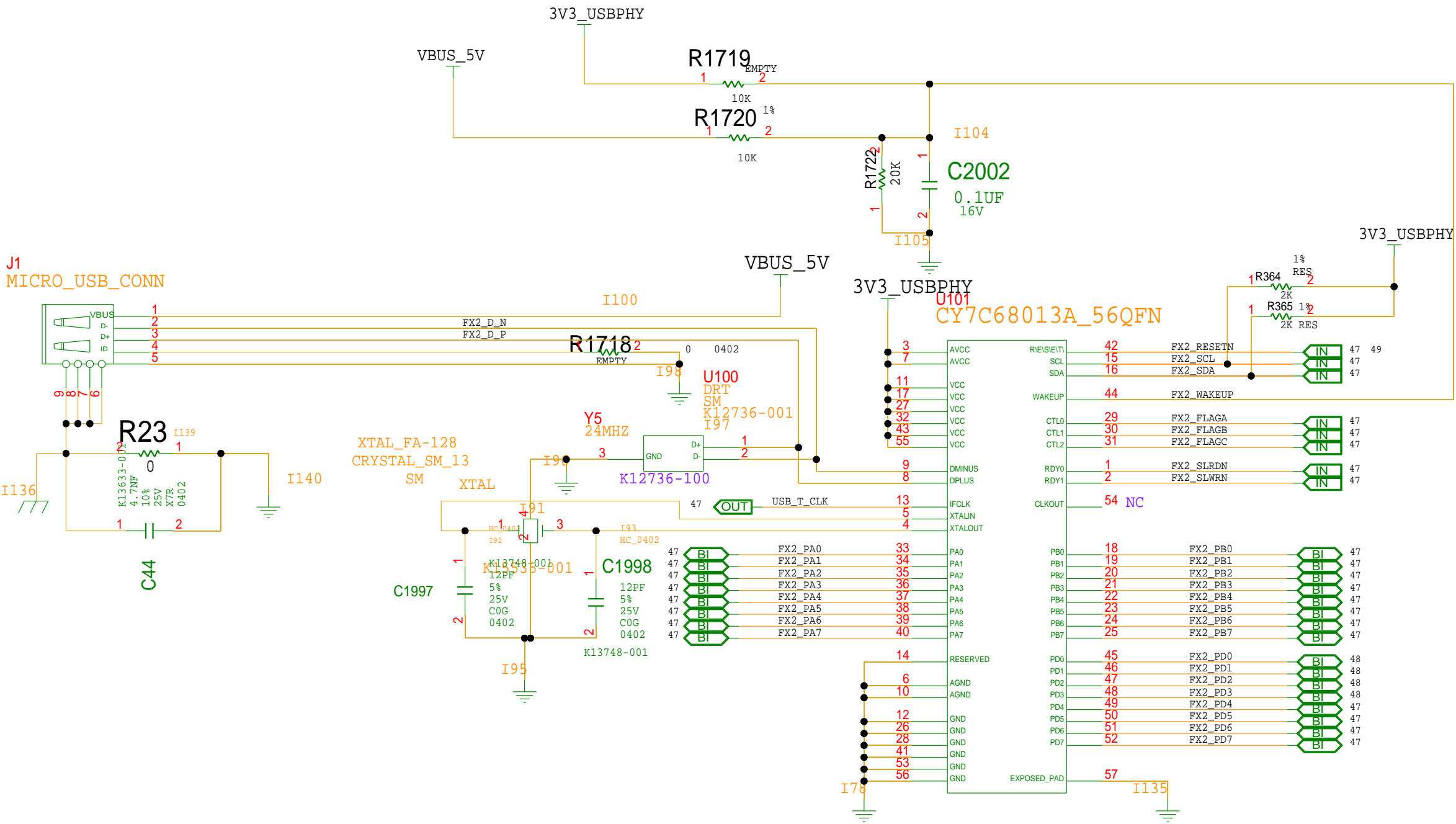
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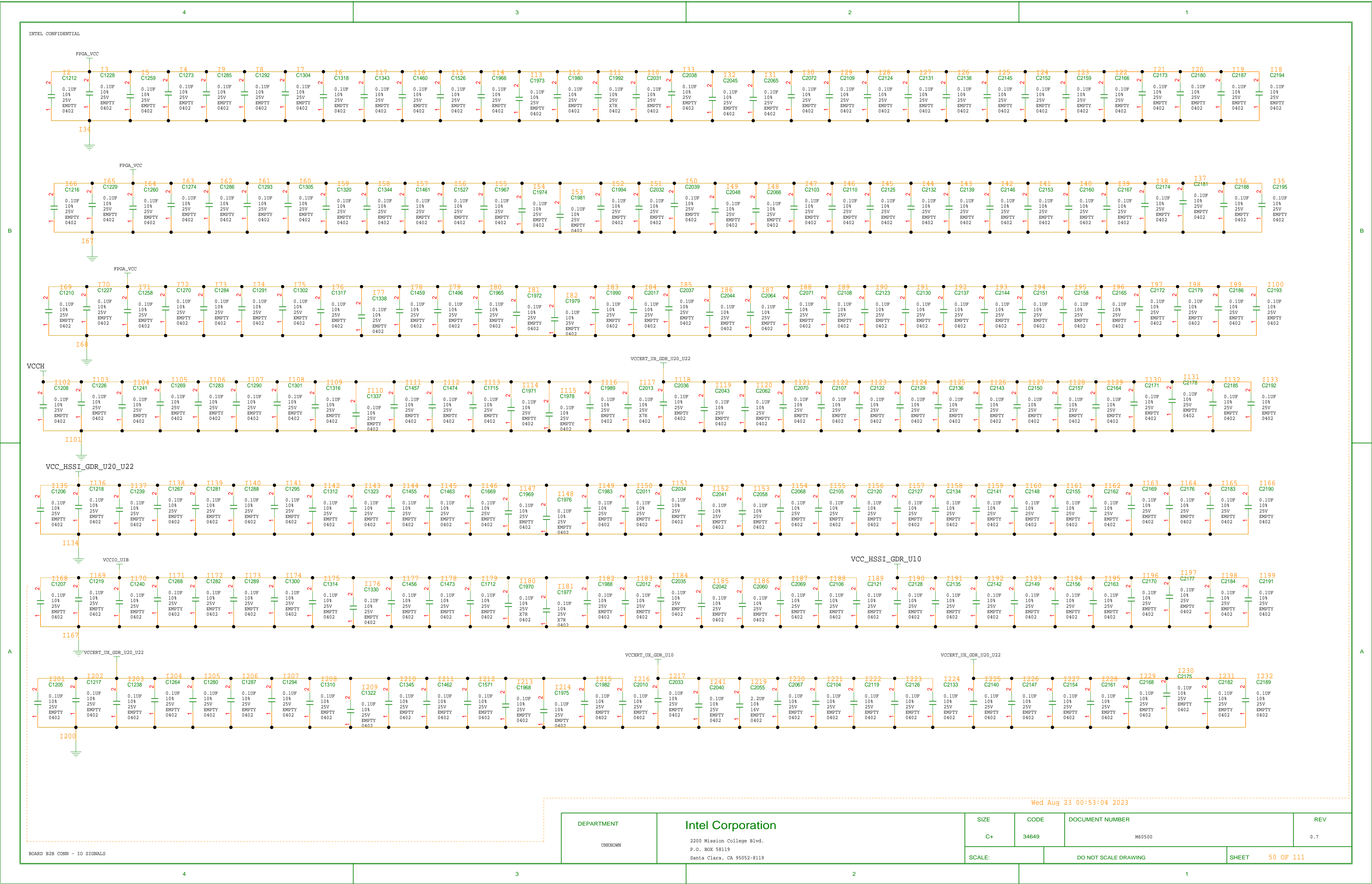
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3

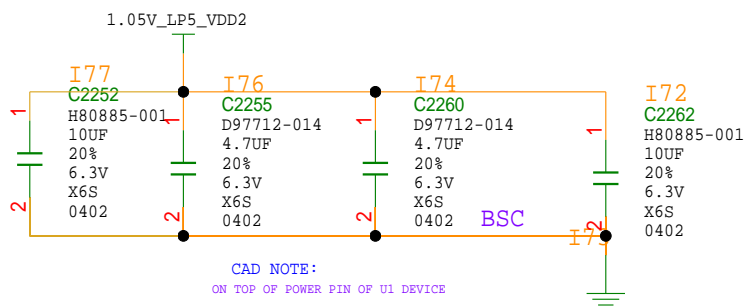
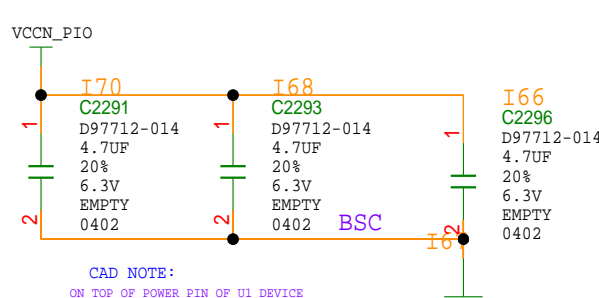
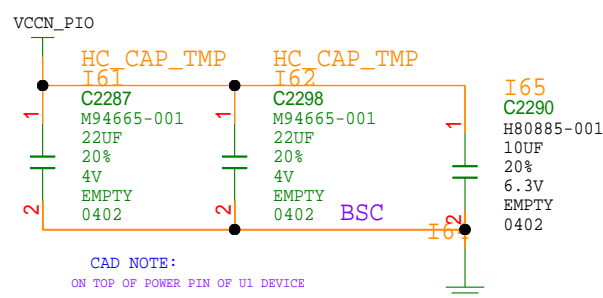
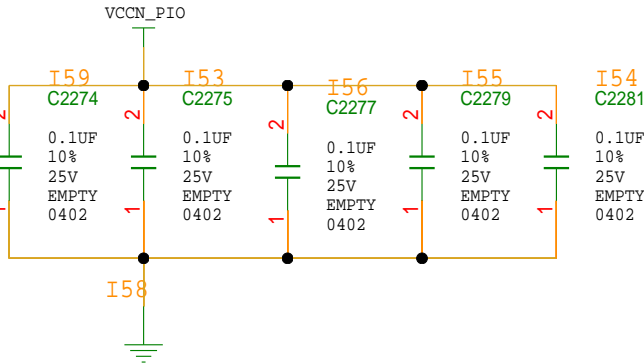
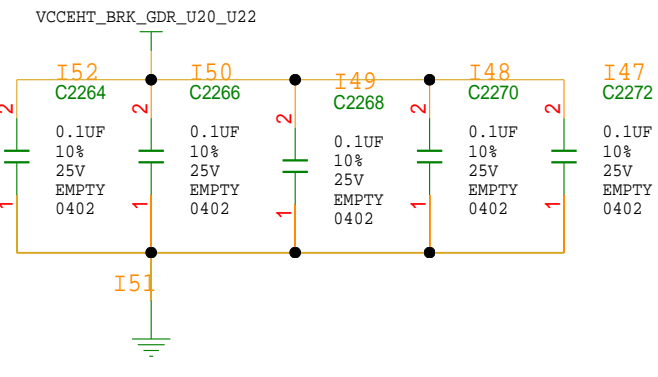
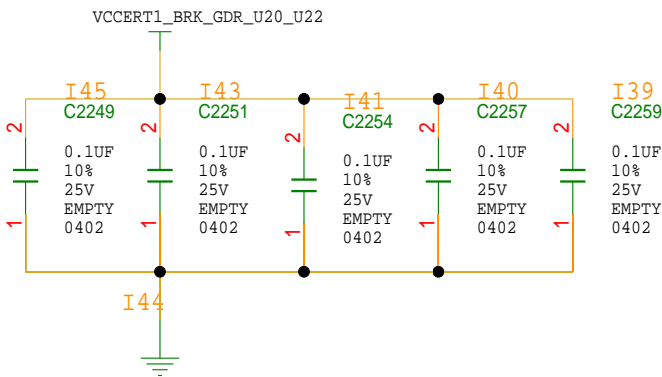
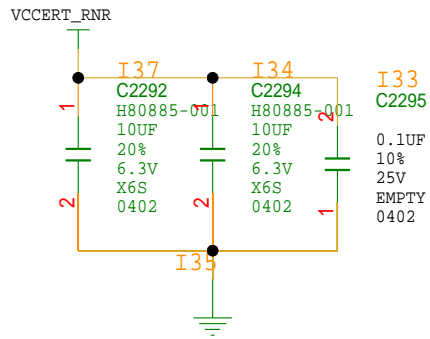
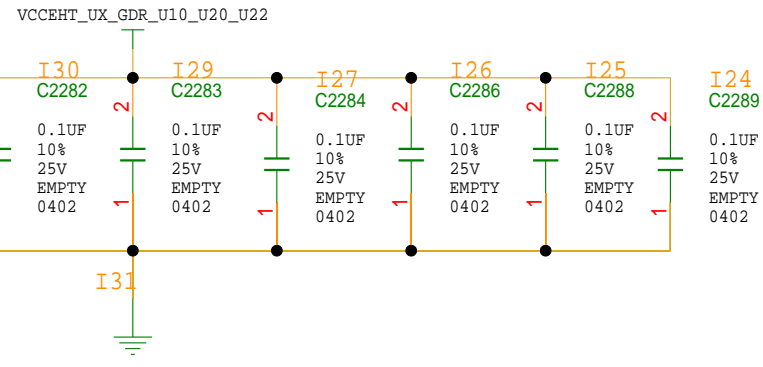
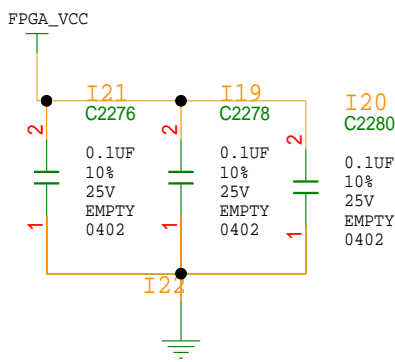
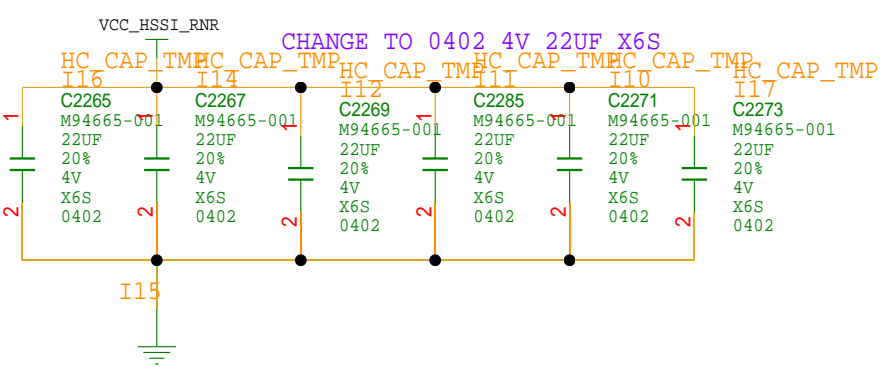
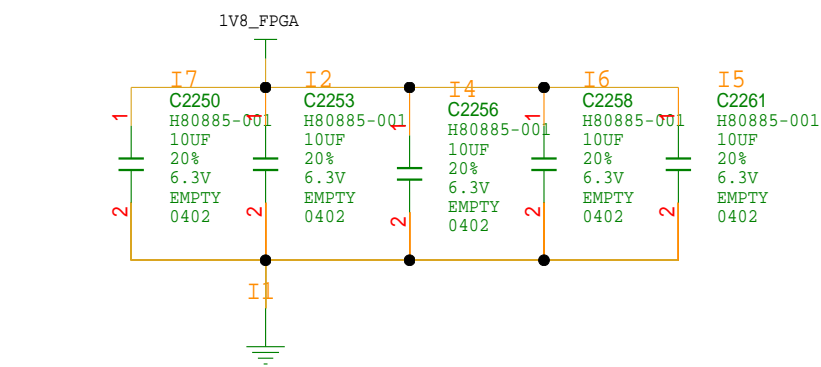
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1

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SIMULATION REQUESTED TO HAVE THESE IN

CHANGE TO 0402 4V 22UF X6S



CAD NOTE:  
ON TOP OF POWER PIN OF UI DEVICE

CAD NOTE:  
ON TOP OF POWER PIN OF UI DEVICE

CAD NOTE:  
ON TOP OF POWER PIN OF UI DEVICE

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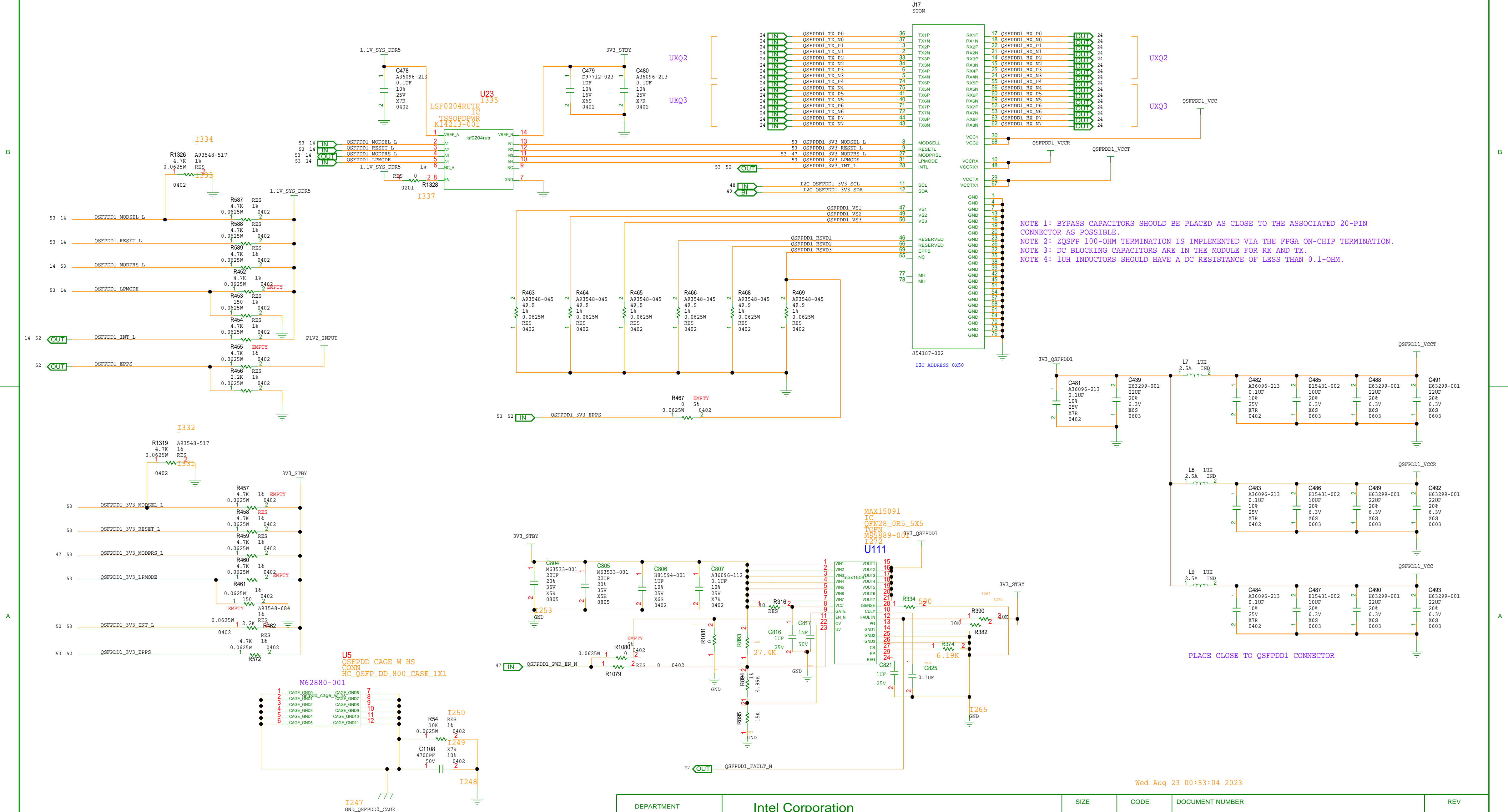


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QSFP-DD CONN #1 (56G ETHERNET)

QSFP - DD CONN1

DESIGN NOTE: CHANNELS MAY BE SWAPPED  
WITHIN EACH UX BLOCK TO OPTIMIZE ROUTINGS.  
LANE 0 & 4 MAY NOT BE SWAPPED.  
(TX1/RX1 & TX4/RX4 ON CONN)



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## QSFP - DD-800 CONN



QSFP-DD-800 CONN

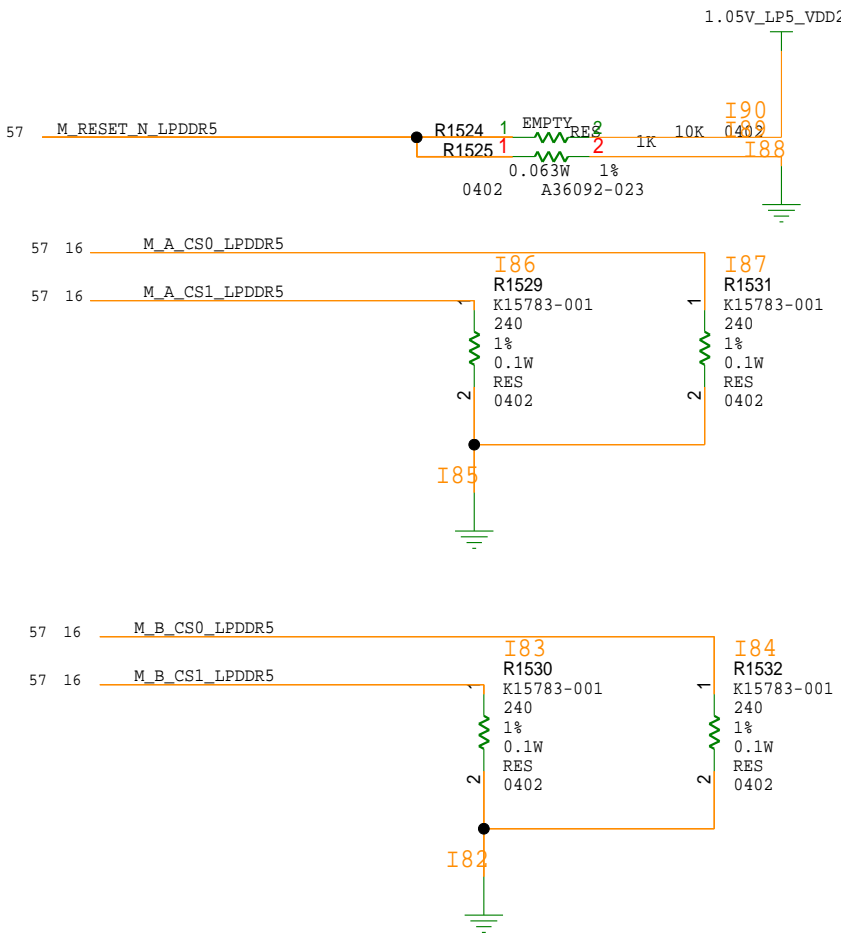
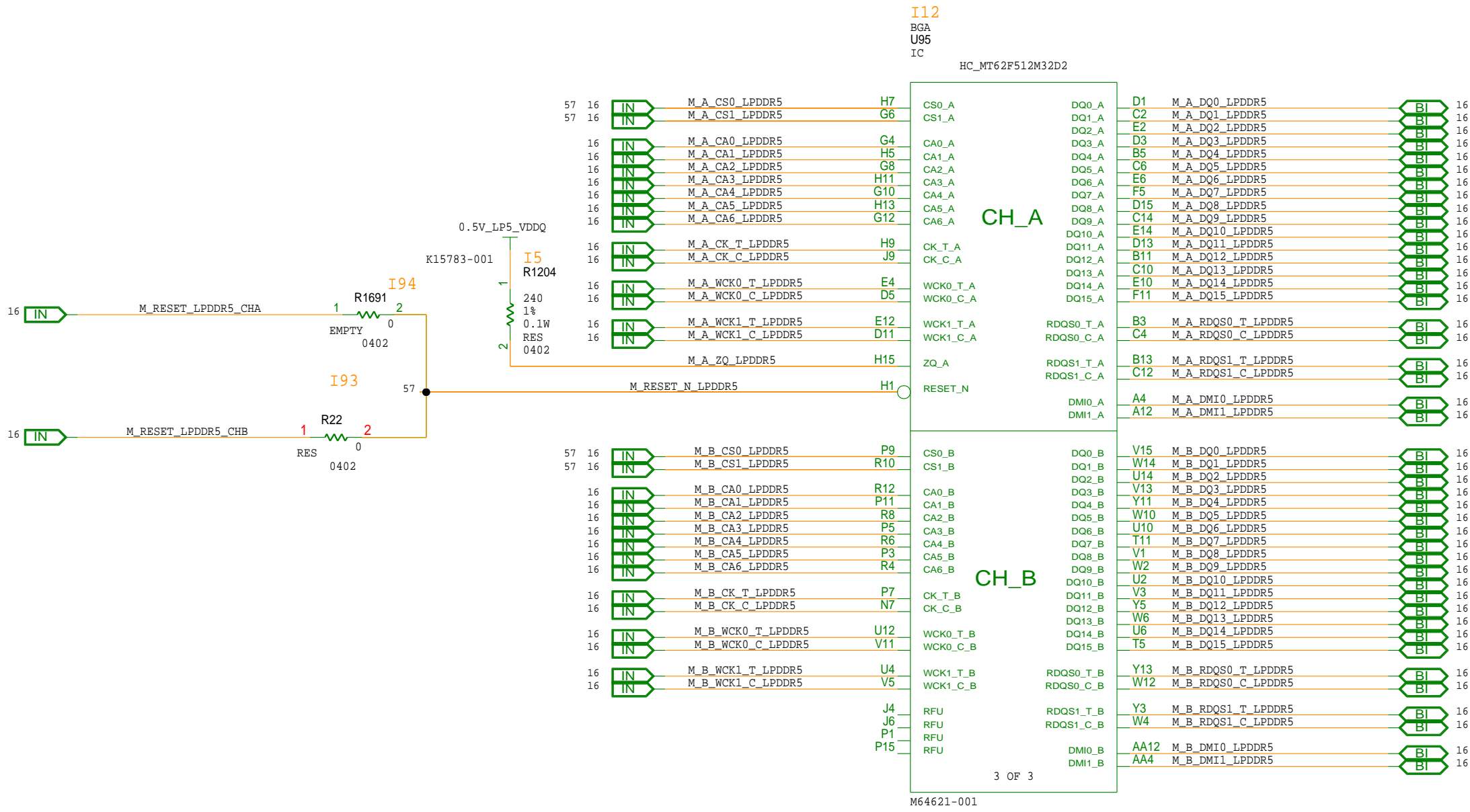




J13  
SCON  
HC\_DDR504426008J

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# LPDDR5 IO



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DOCUMENT NUMBER

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57 OF 111



4

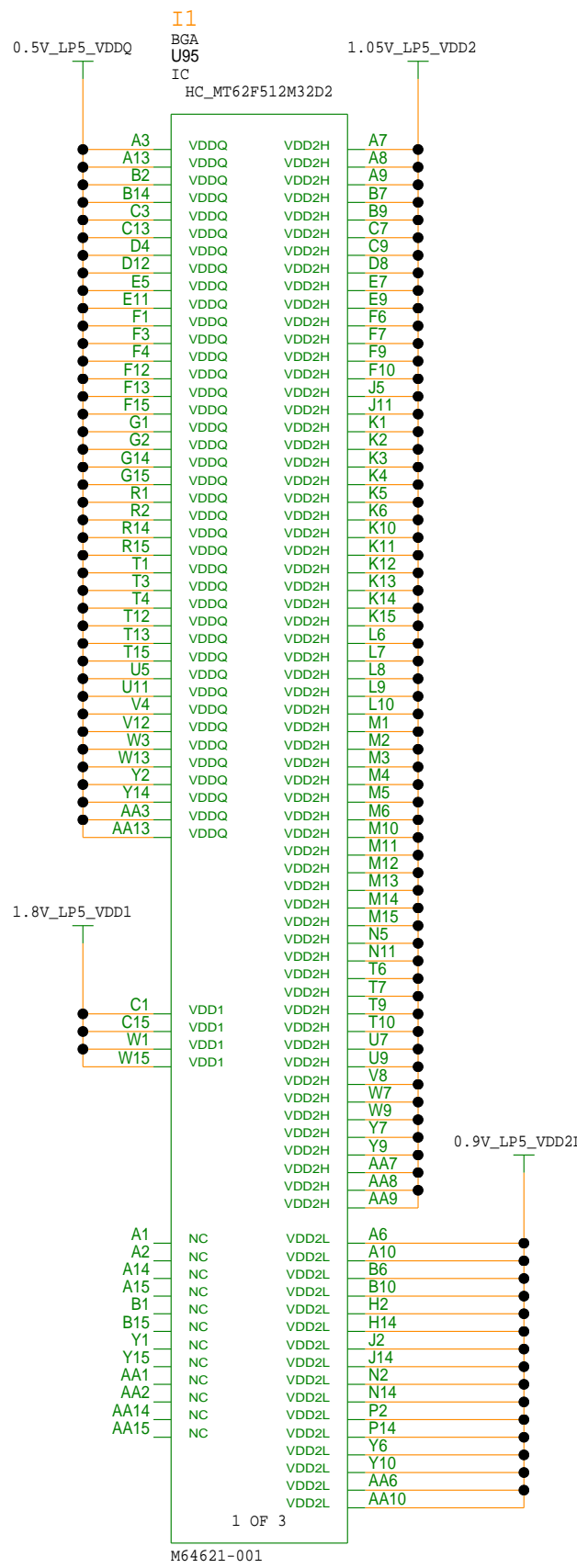
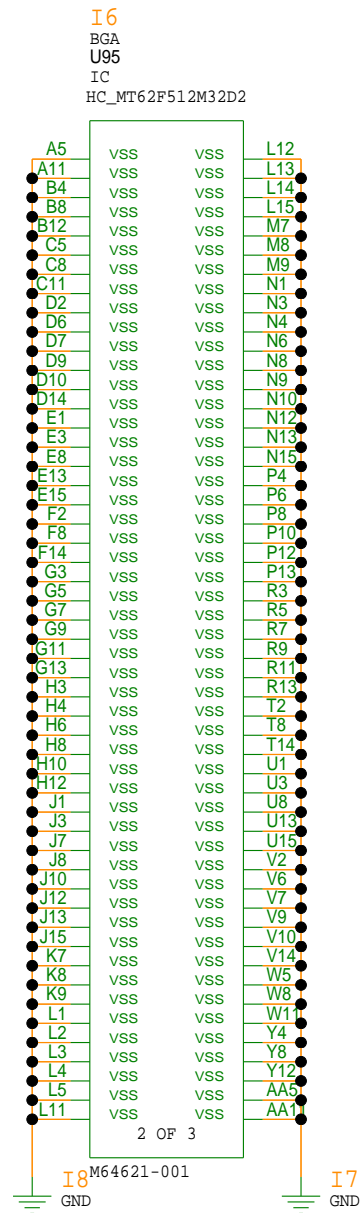
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INTEL CONFIDENTIAL

# LPDDR5 POWER



Wed Aug 23 00:53:05 2023

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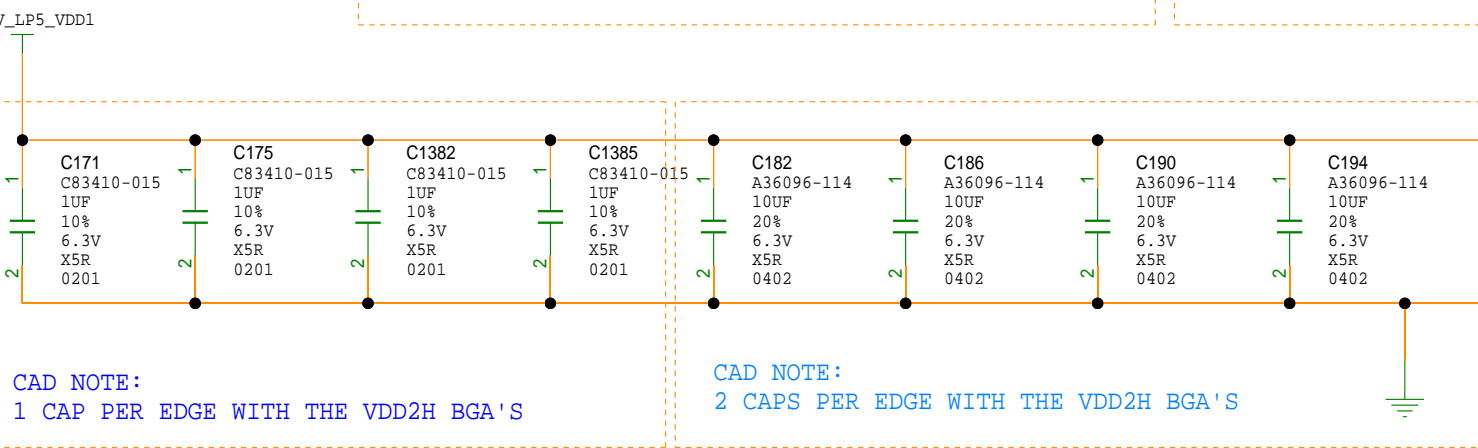
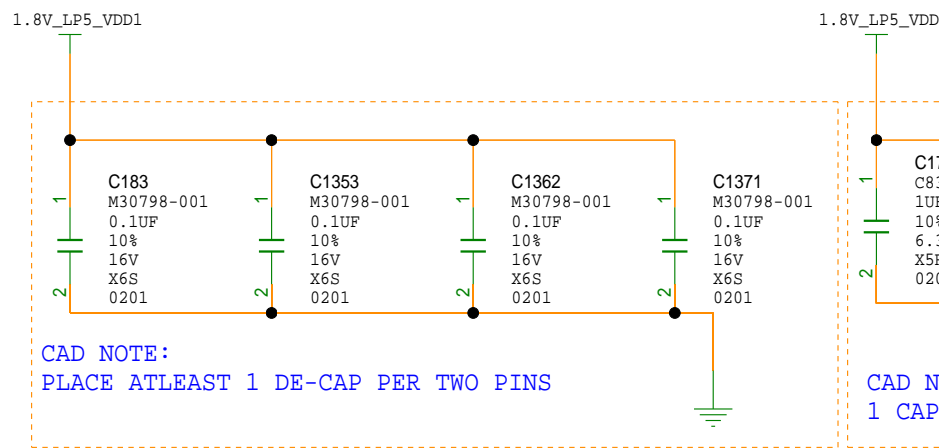
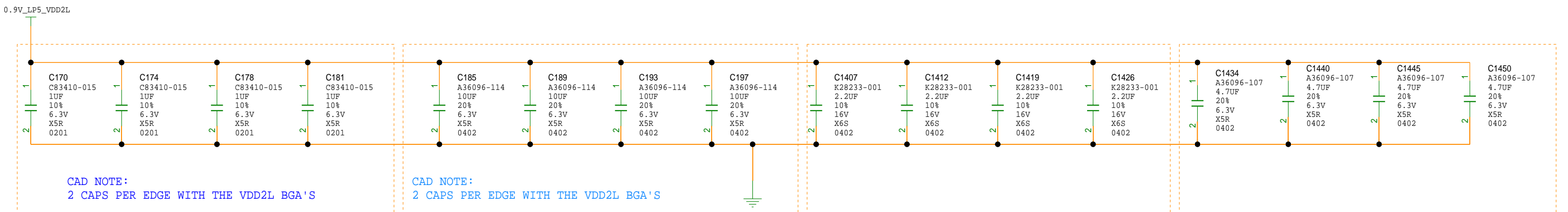
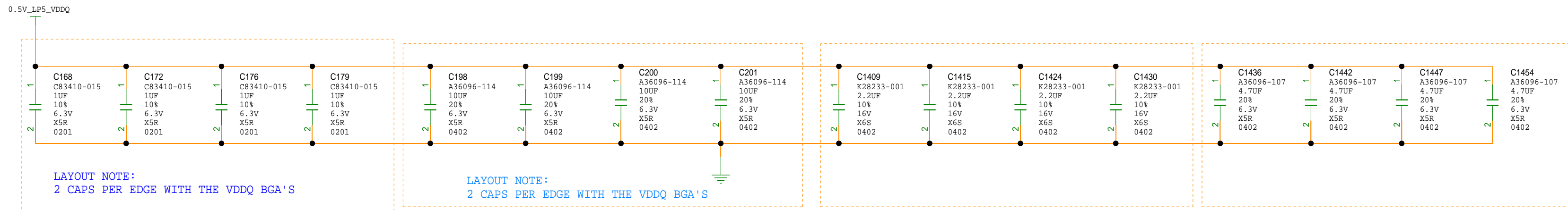
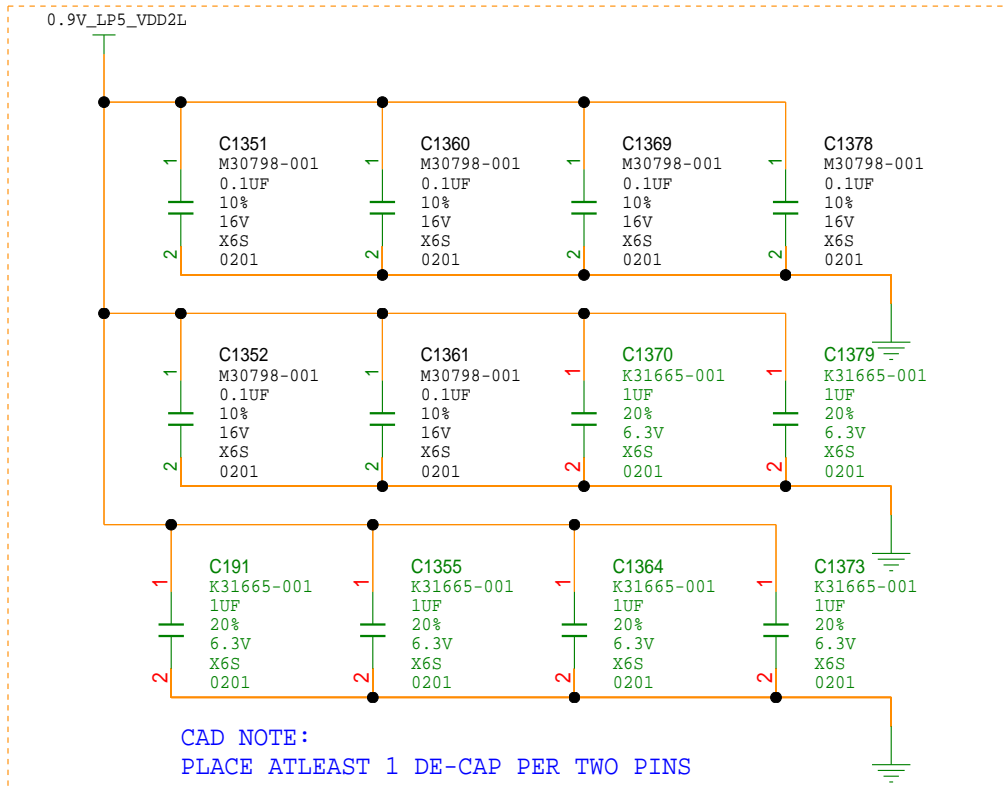
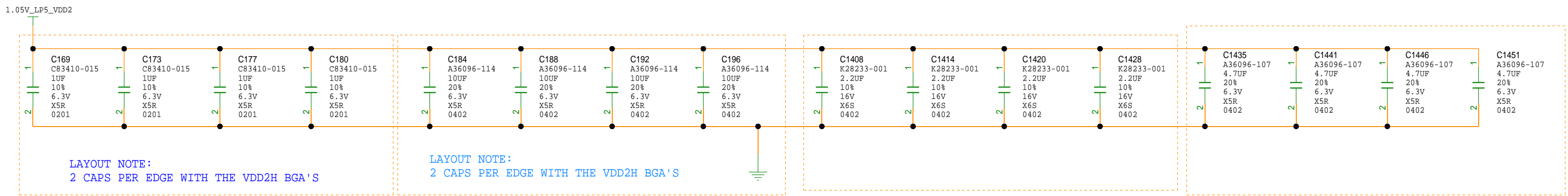
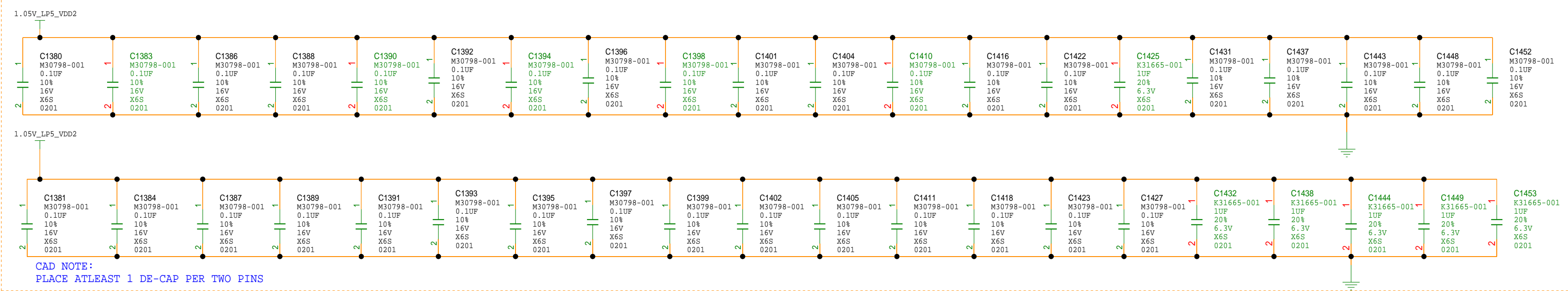
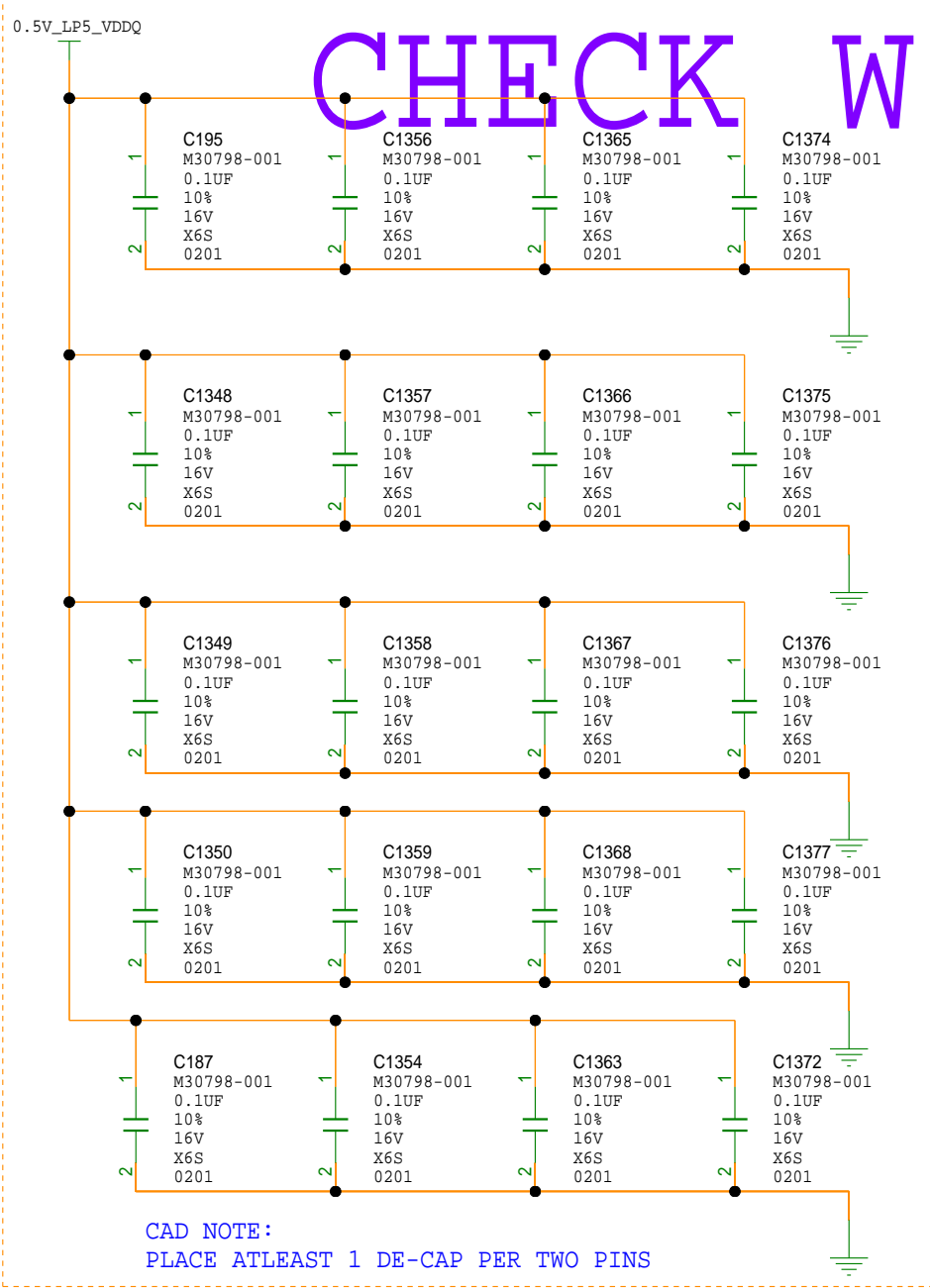
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# CHECK WITH LATEST WOODPECK RIDGE

## LPDDR5 DECOUPLING CAPACITORS



Wed Aug 23 00:53:05 2023

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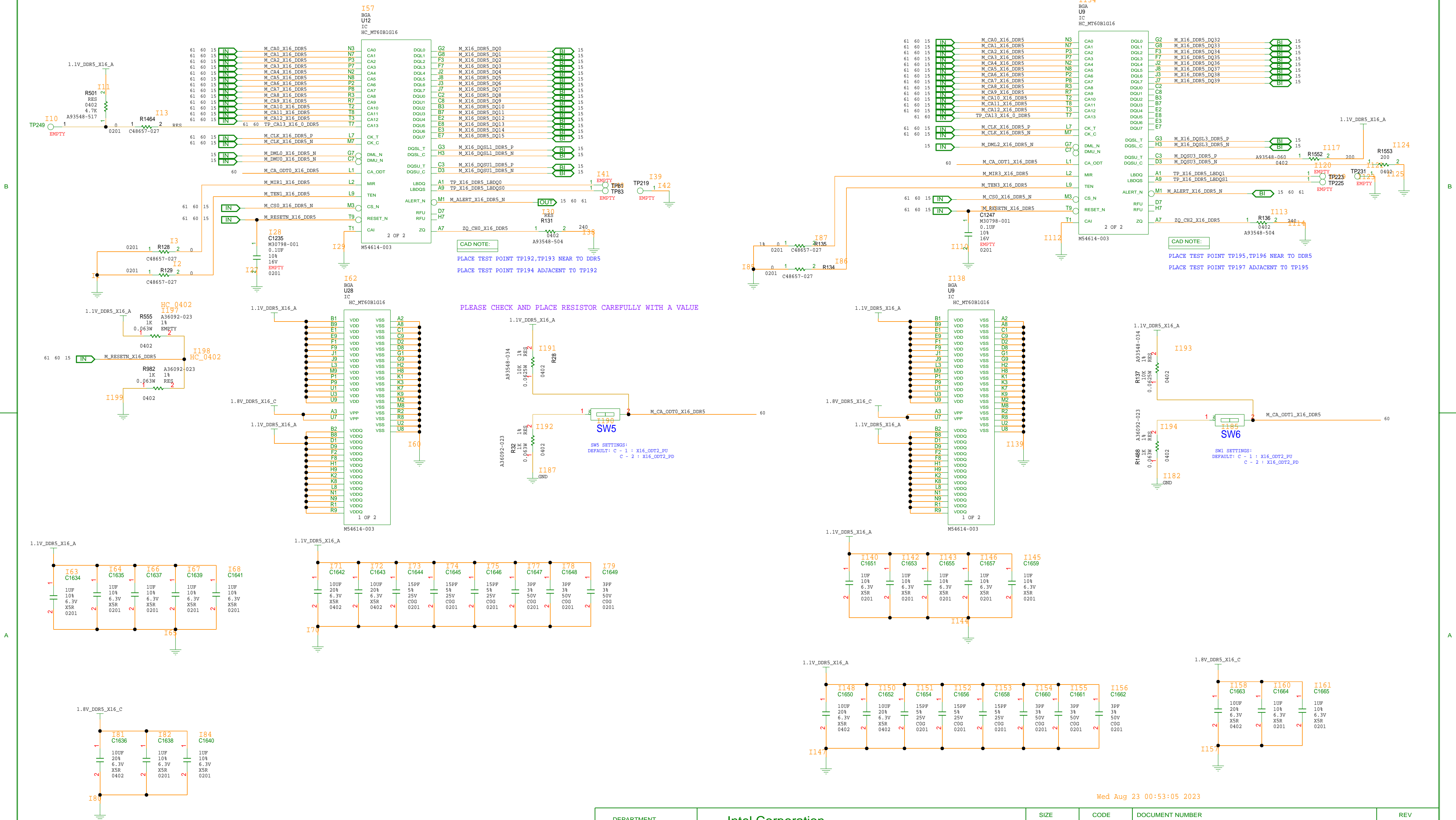
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## DDR5 X40 COMP-0

## TOP

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M60500

REV

0.7

SCALE:

DO NOT SCALE DRAWING

SHEET

60 OF 111



B

## A



RESERVED

DDR5 X40 COMP-0

TOP

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B

B

A

A

I55  
BGA  
U27  
IC  
HC\_M760B1G16

I148  
BGA  
U19  
IC  
HC\_M760B1G16

I18  
BGA  
U13  
IC  
HC\_M760B1G16

I74  
BGA  
U19  
IC  
HC\_M760B1G16

CAD NOTE:

PLACE TEST POINT TP192,TP193 NEAR TO DDR5  
PLACE TEST POINT TP194 ADJACENT TO TP192

CAD NOTE:

PLACE TEST POINT TP195,TP196 NEAR TO DDR5  
PLACE TEST POINT TP197 ADJACENT TO TP195

SW4 SETTINGS:  
DEFAULT: C - 1 : X16\_ODT2\_PU  
C - 2 : X16\_ODT2\_PD

SW4 SETTINGS:  
DEFAULT: C - 1 : X16\_ODT2\_PU  
C - 2 : X16\_ODT2\_PD

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DOCUMENT NUMBER

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REV

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62 OF 111

RESERVED

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SDM DAUGHTER CARD

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Tue May 16 20:53:11 2023

SDM DAUGHTER CARD

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CODE

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DOCUMENT NUMBER

M60500

REV

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64 OF 111

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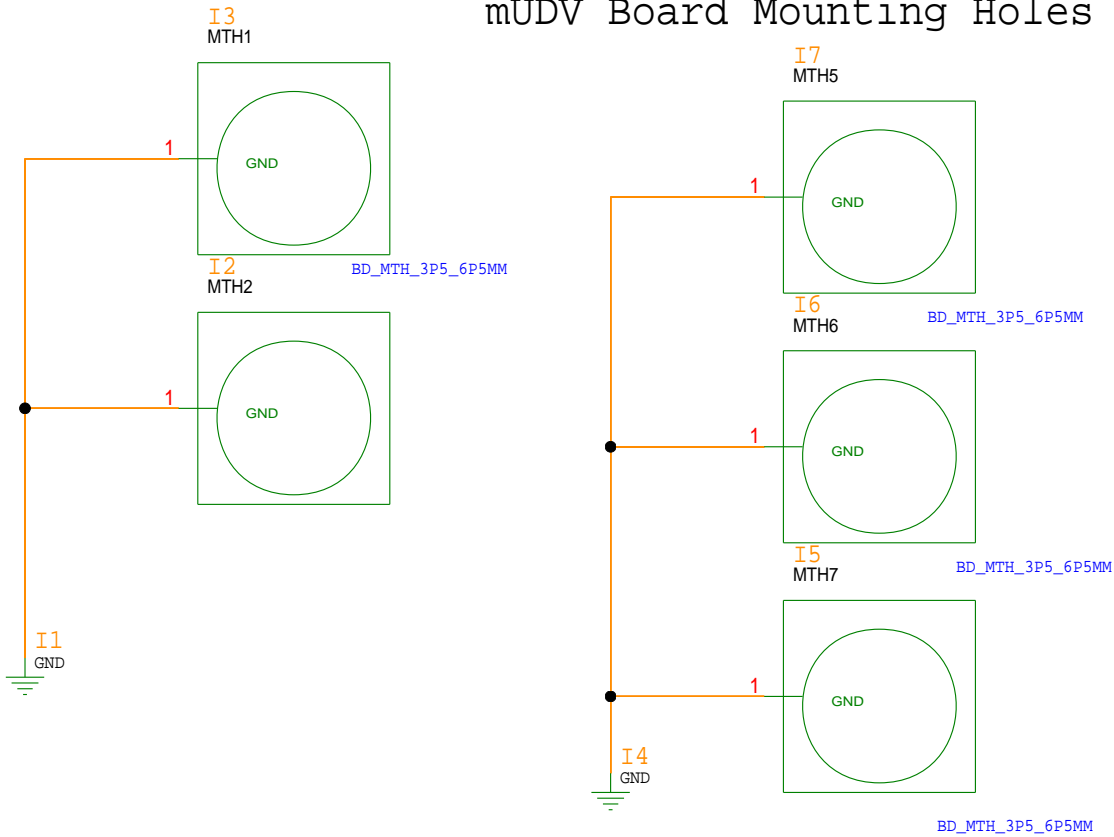
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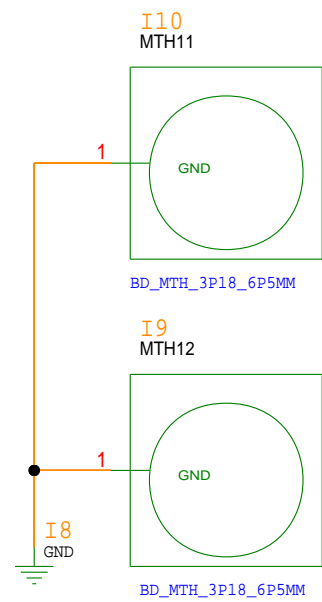
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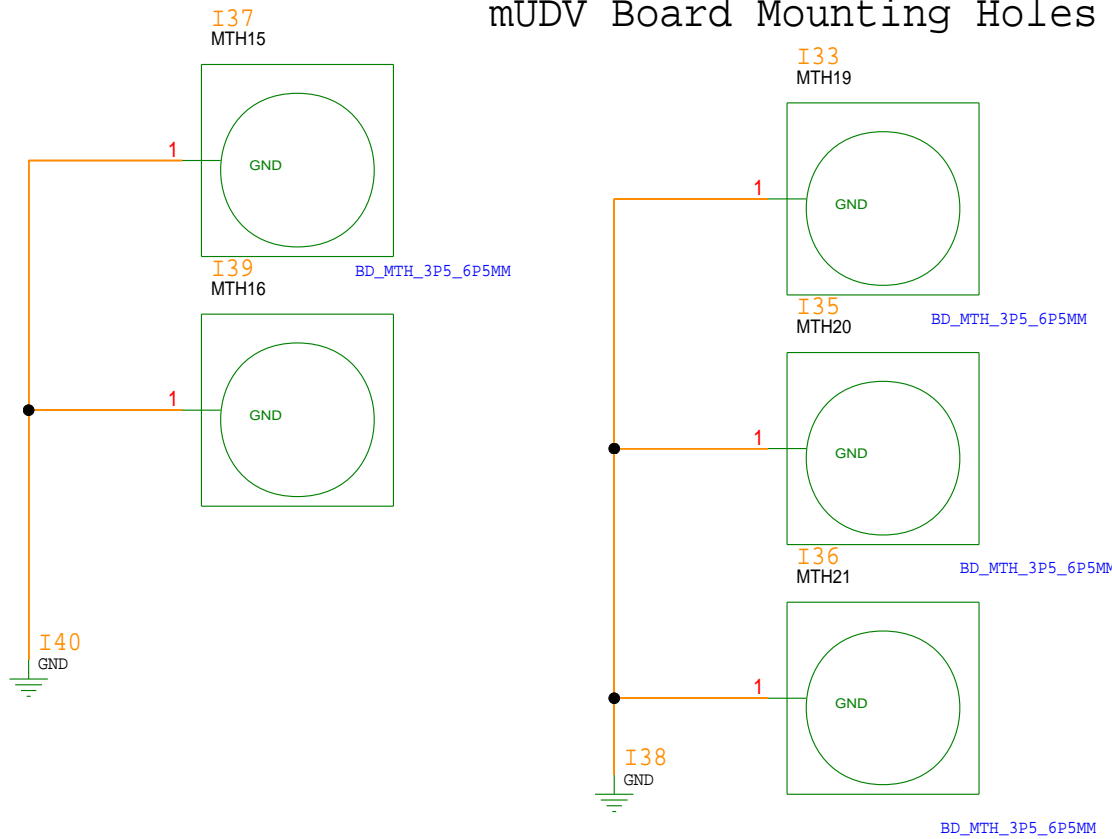
mUDV Board Mounting Holes



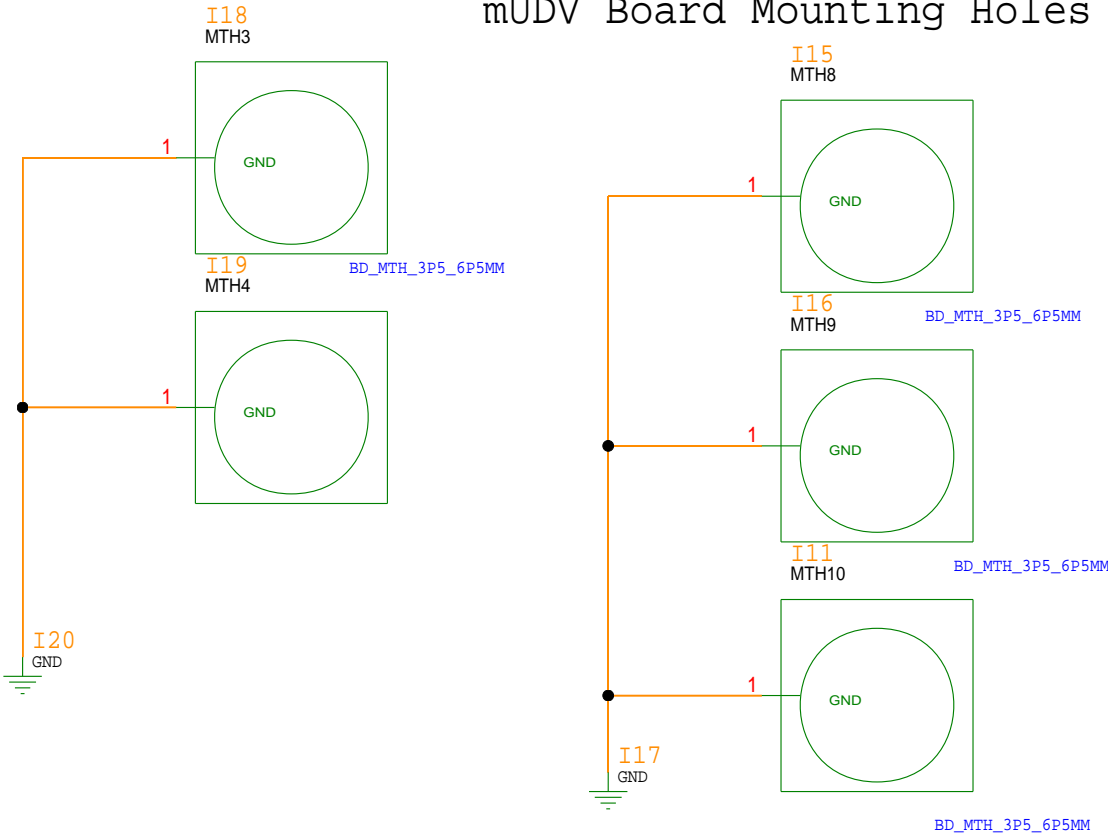
PCIe Bracket



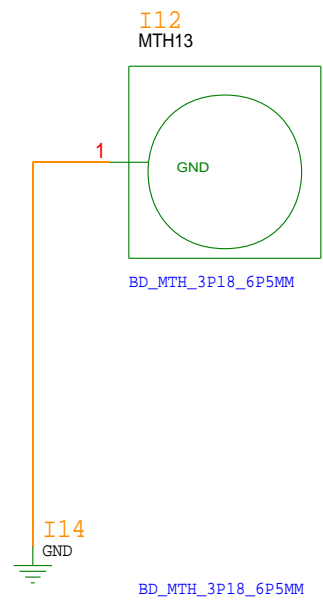
mUDV Board Mounting Holes



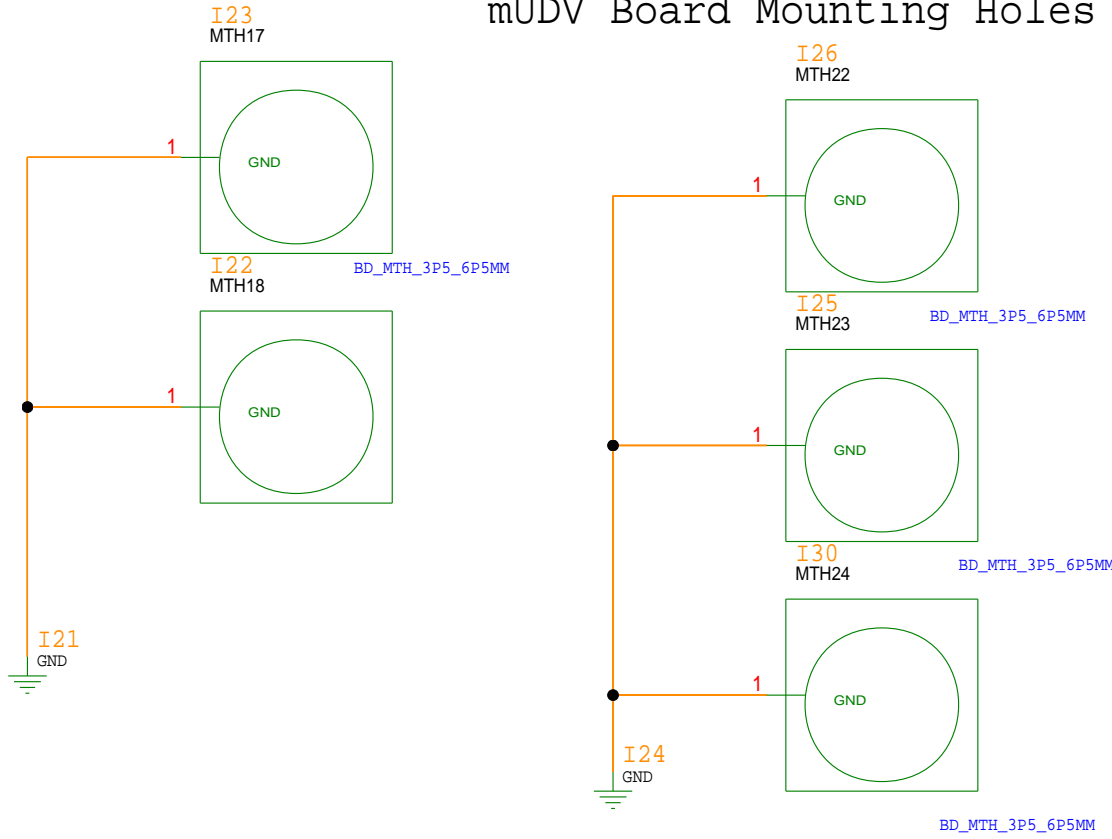
mUDV Board Mounting Holes



PCIe Bracket



mUDV Board Mounting Holes



Wed Aug 23 00:53:06 2023

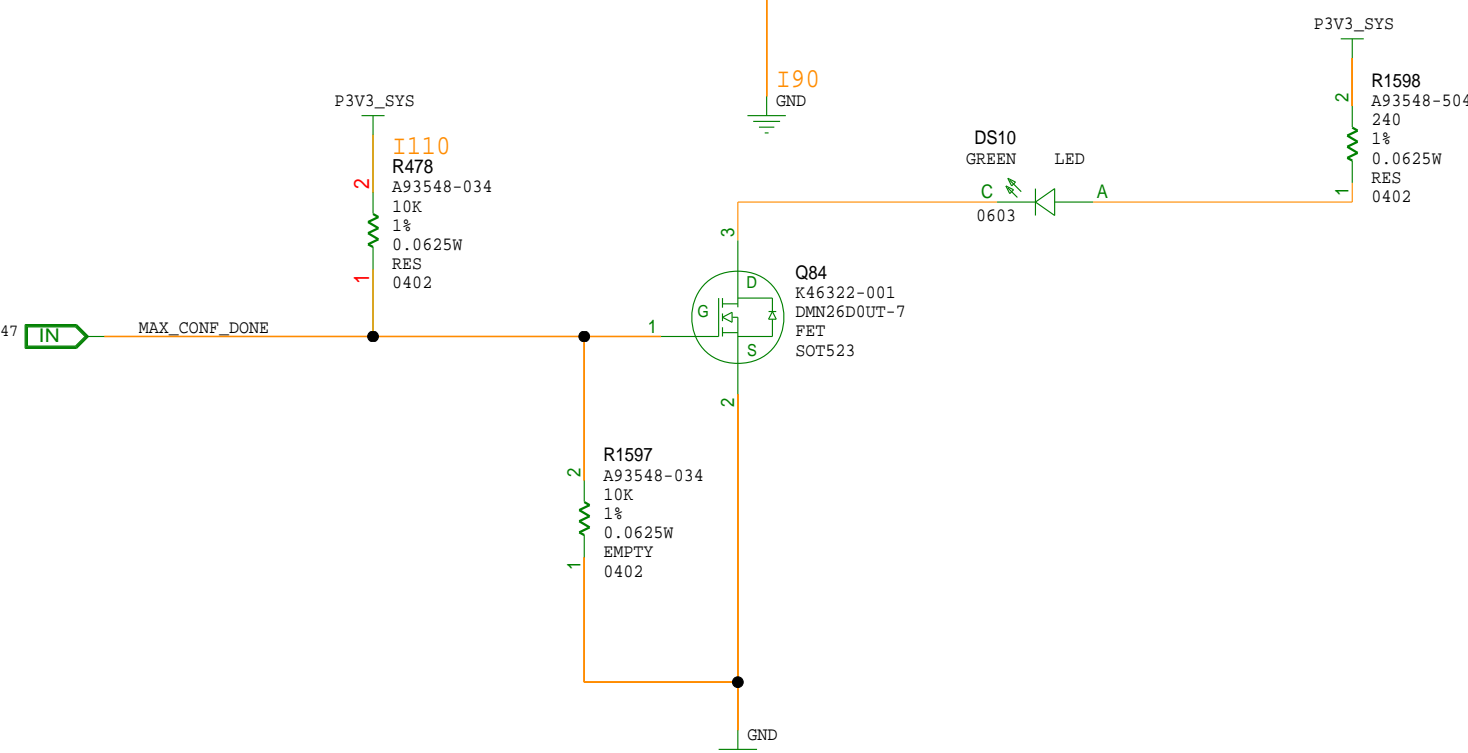
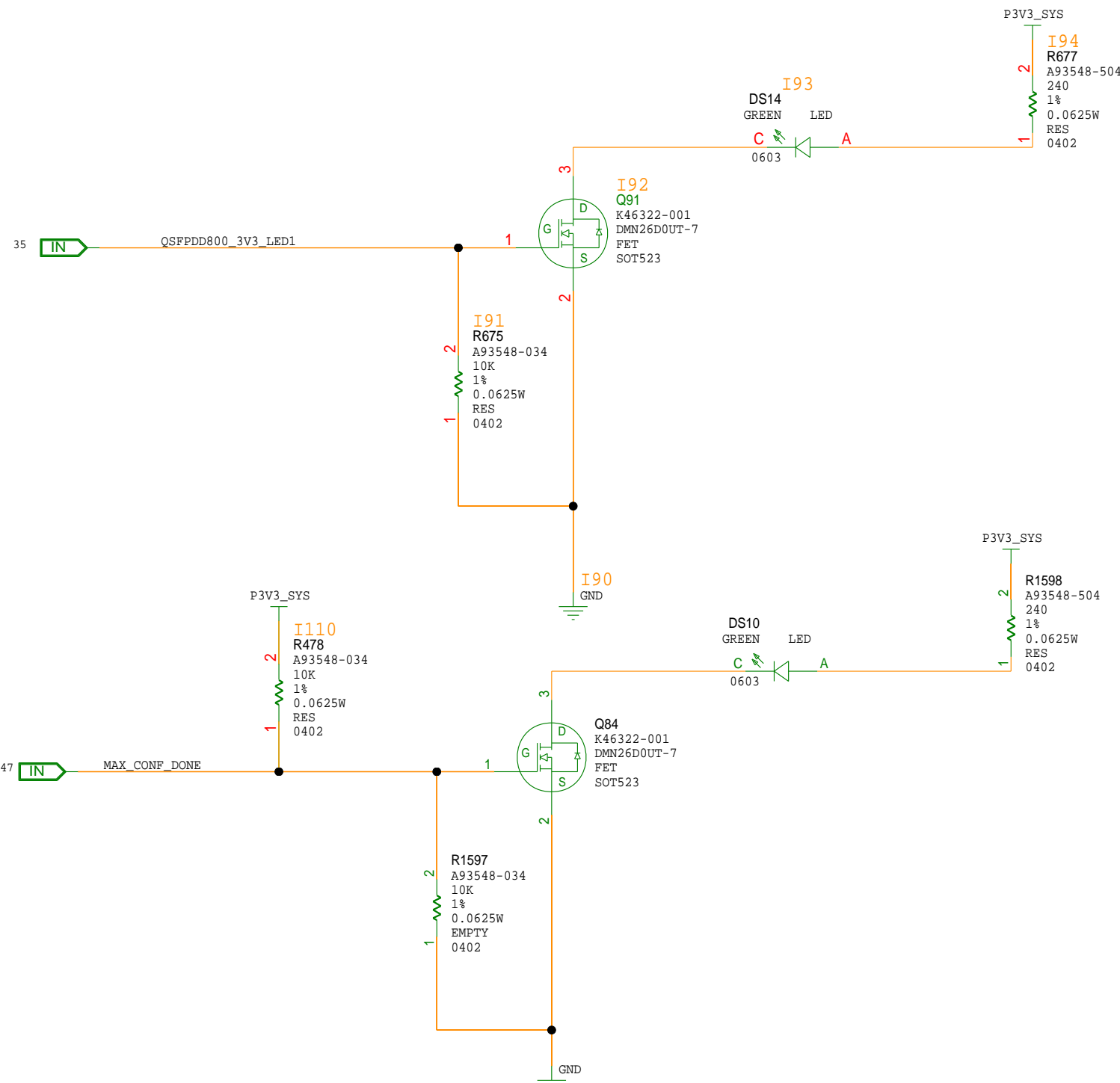
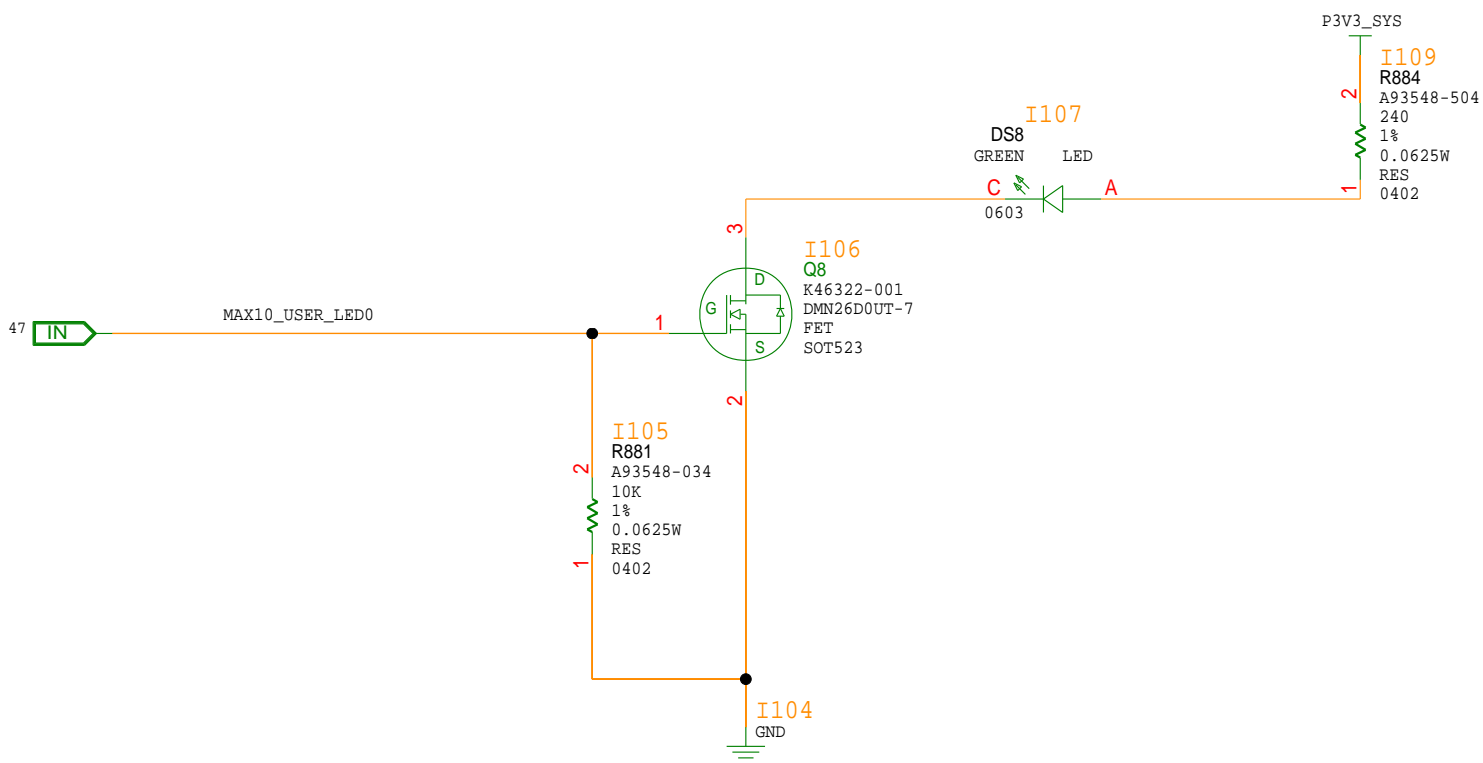
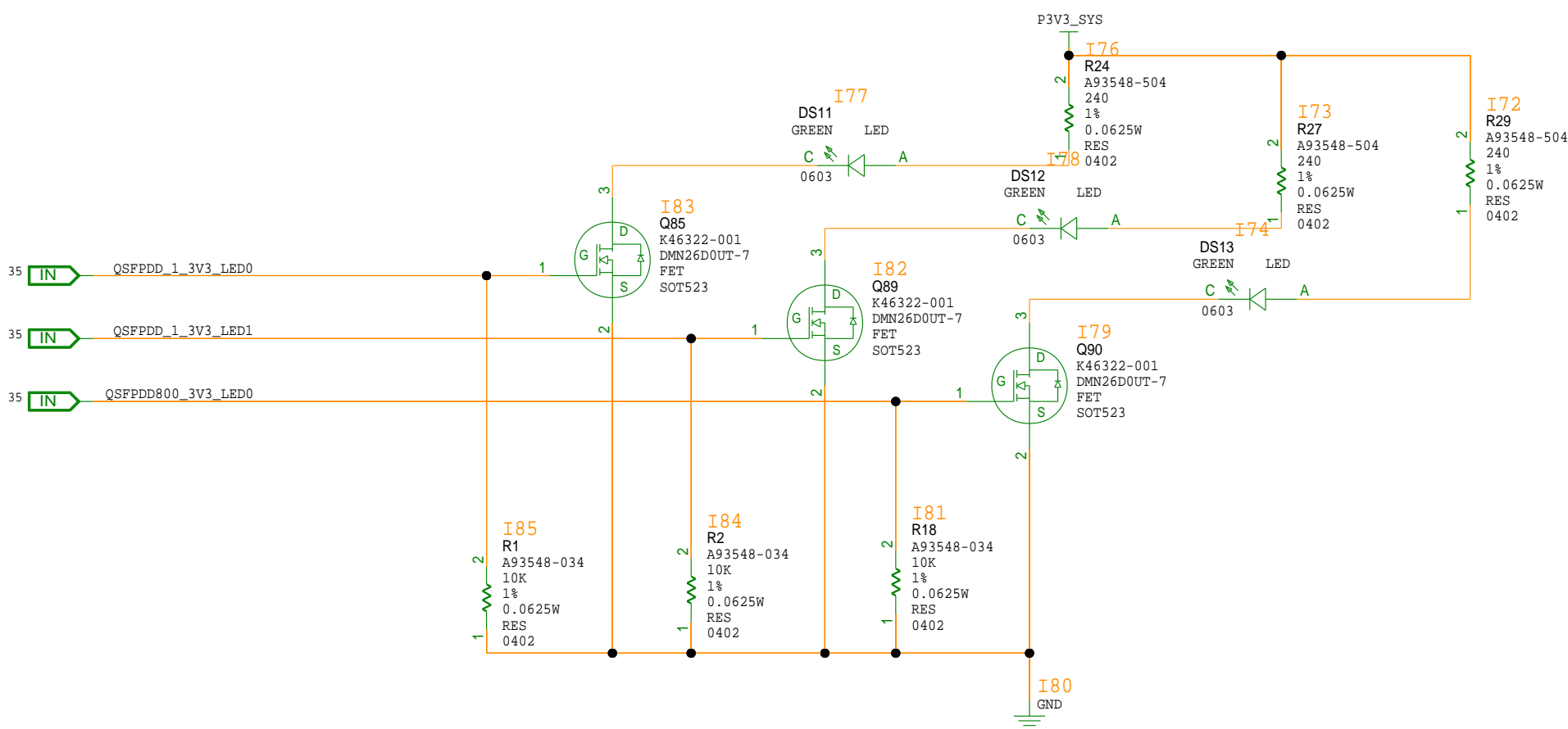
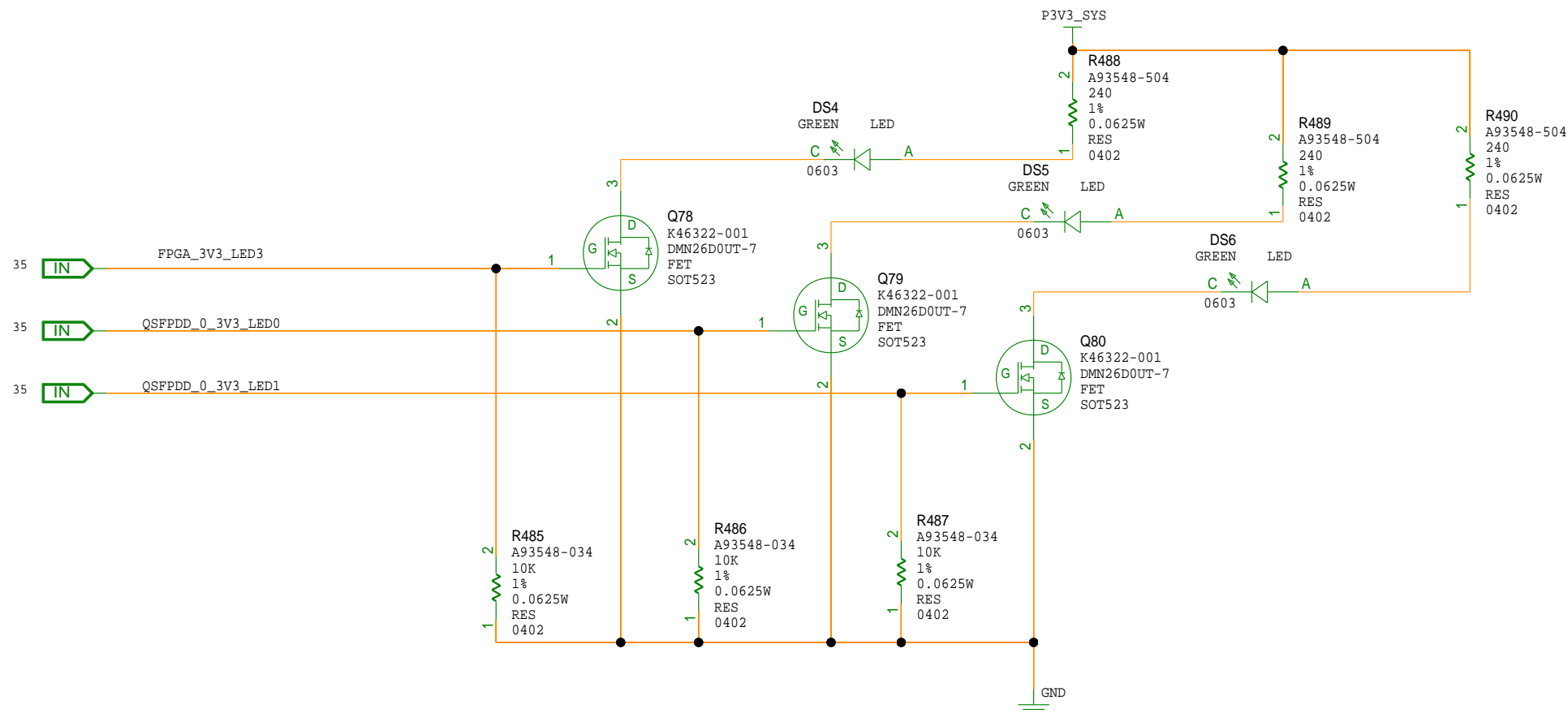
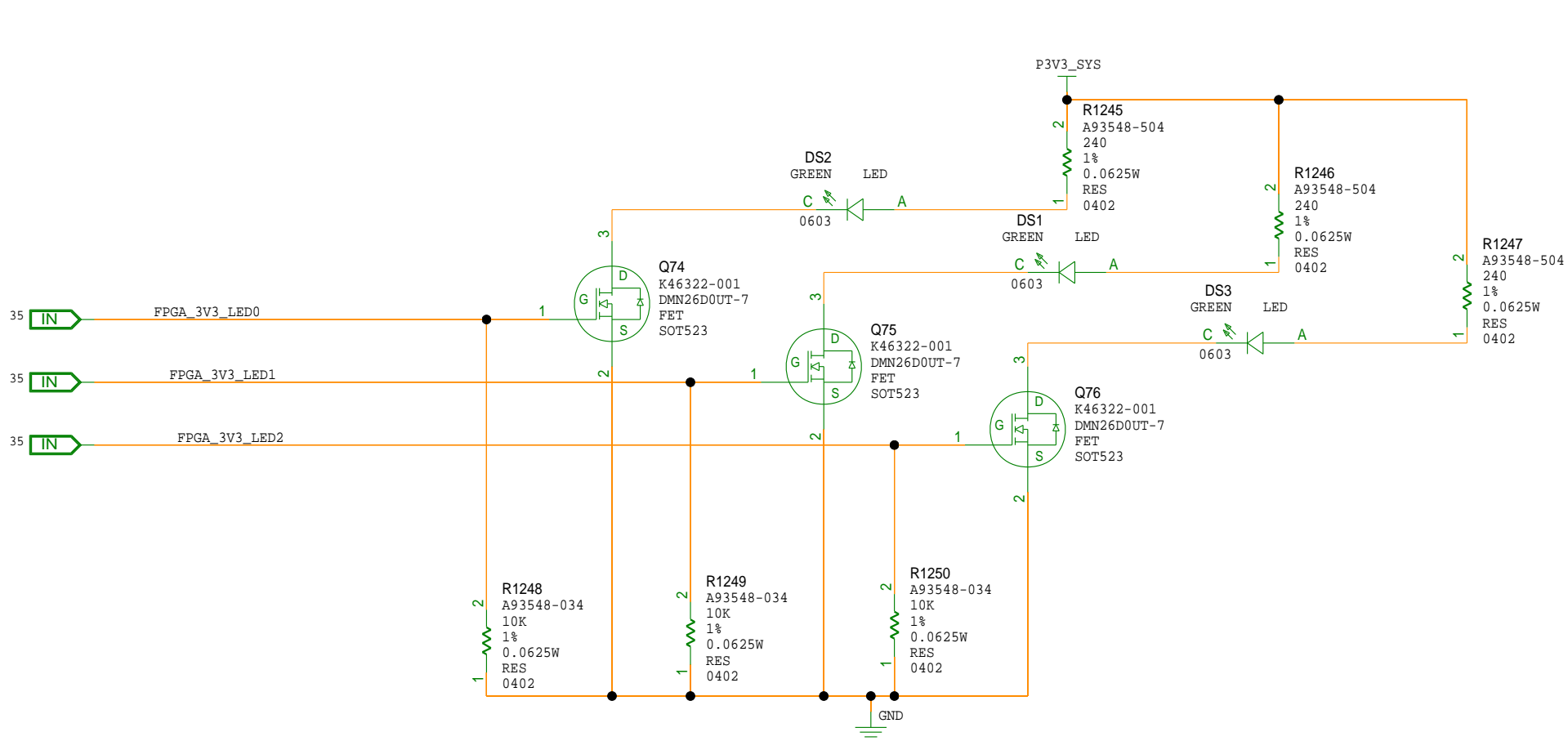
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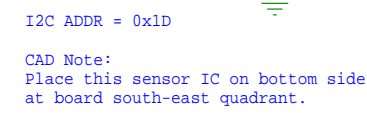
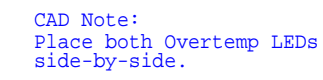
# USER LED 2



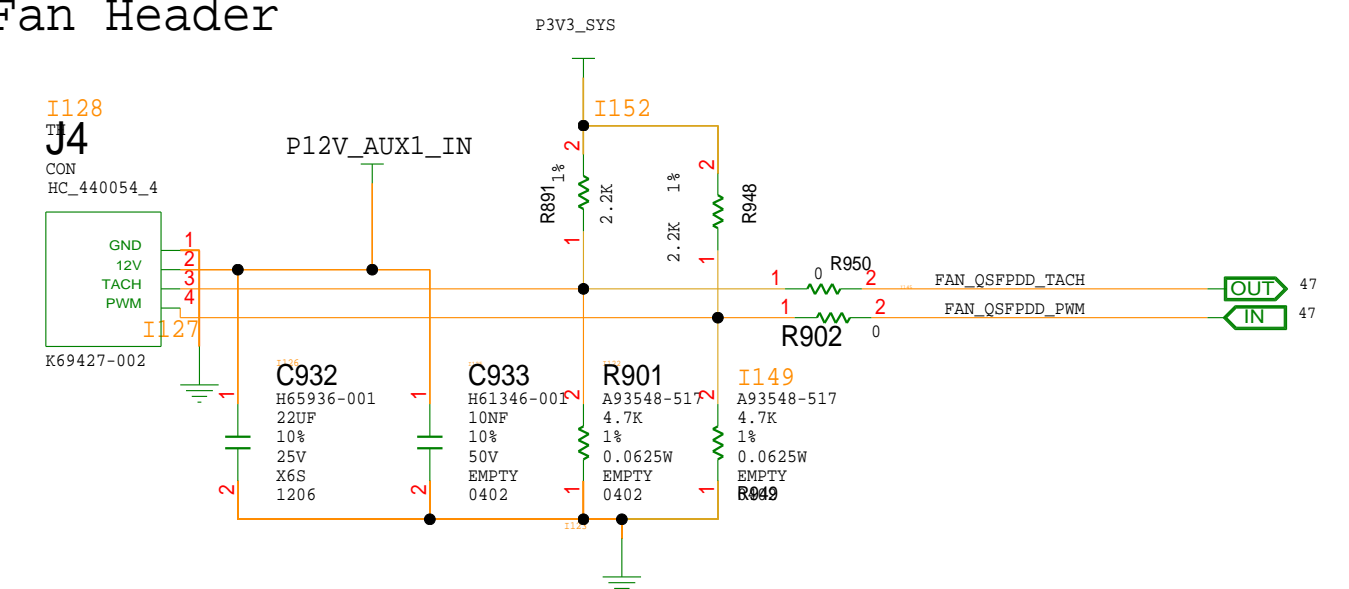
Fri Oct 6 12:44:25 2023



TEMP SENSOR FAN



Fan Header

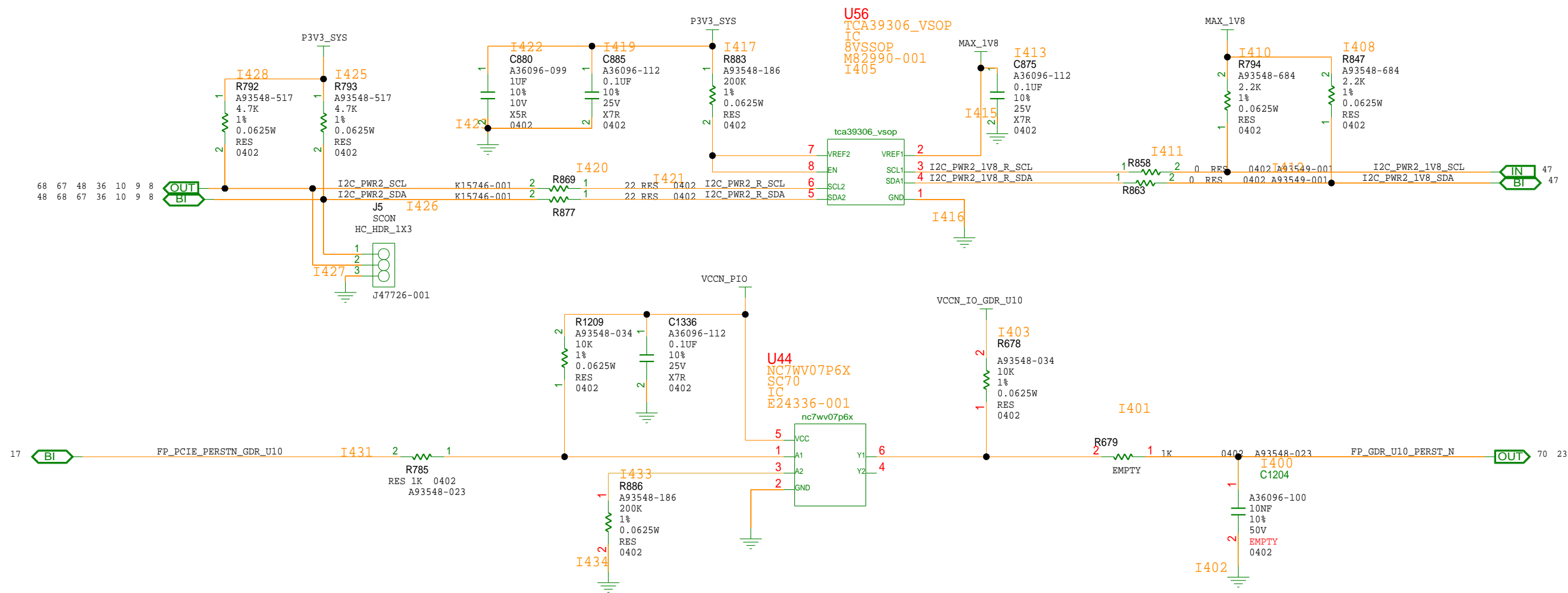


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LEVEL XTLR, IO EXP 2



S11 SETTINGS:  
[1-4]-OFF/OPEN, [2-3]-ON/CLOSED: END POINT ( DEFAULT )

Wed Aug 23 00:53:07 2023

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UNKNOWN	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	C+	34649	M60500	0.7
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TEST POINTS 1

4

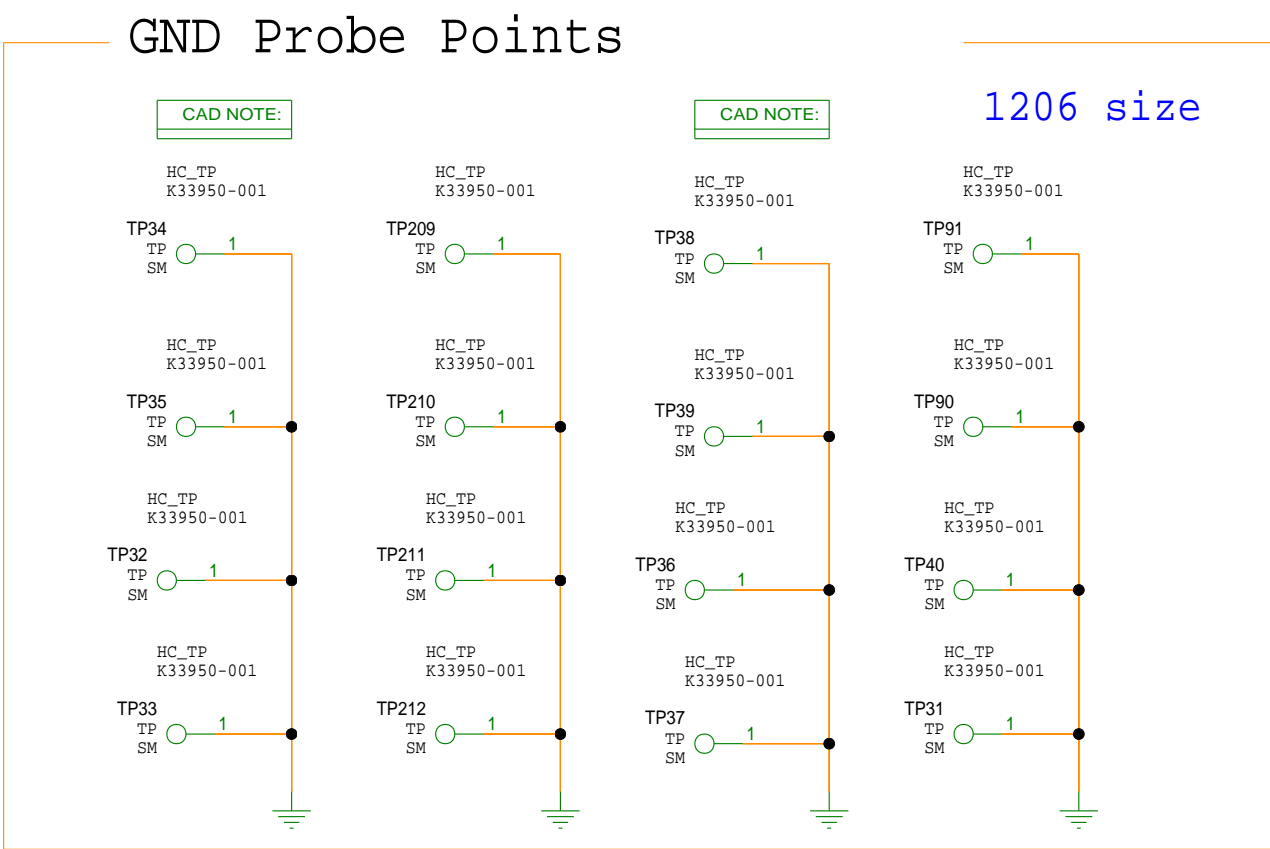
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TEST POINTS 2



Wed Aug 23 00:53:07 2023

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71 OF 111

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VCC\_HSSI\_RNR VCCN\_HPS VCCBAT\_SDM



SHEET 72 OF 111



POWER MISC 1

POWER MISC 1

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POWER MISC 2

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Sun Oct 09 09:45:36 2022

POWER MISC 2

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74 OF 111

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POWER MISC 3

VCCERT\_RNR

VCCERT1\_2\_BRK\_GDR\_U20\_U22  
1.0V @10A

VCCERT1\_BRK\_GDR\_U20\_U22

FREQUENCY: 1MHZ

CHECK WITH ADI ABOUT R716, R935 NEED TO BE EMPTY??

CAD NOTE: TAP AT MAIN LOAD POINT.

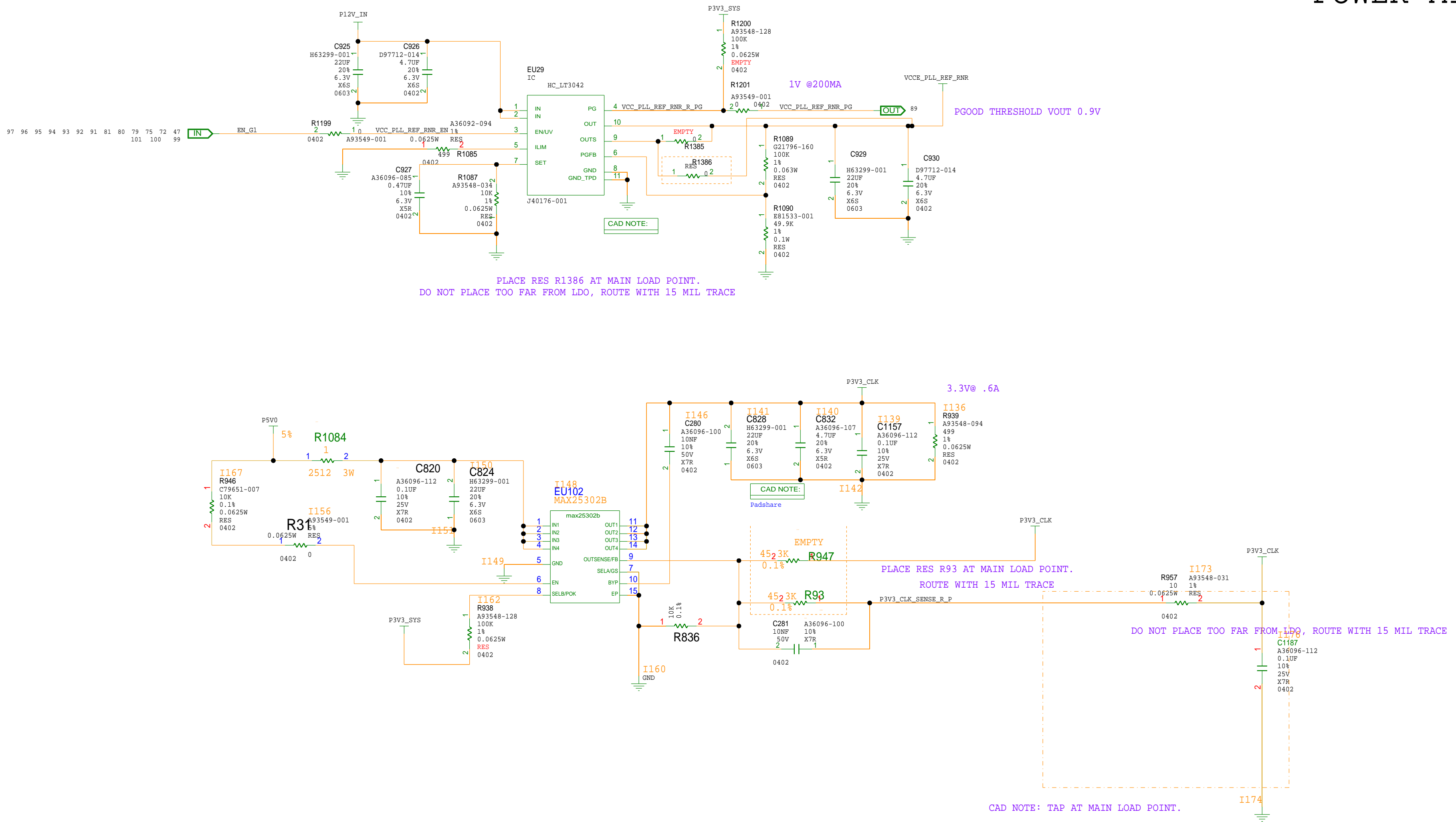
ROUTE AS DIFF PAIR 15 MIL TRACES

Wed Aug 23 00:53:07 2023



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# POWER MISC 4



Wed Aug 23 00:53:07 2023

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CODE

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DOCUMENT NUMBER

M60500

REV

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SCALE:

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76 OF 111



1.1V @10.2A

1.1V\_DDR5\_X16\_A

ROUTE AS DIFF PARI 15 MIL TRACES

CAD NOTE: TAP AT MAIN LOAD POINT.

FREQUENCY: 1MHZ



1.8V@0.5A

1.8V\_DDR5\_X16\_C

1.8V\_DDR5\_X16\_C

DO NOT PLACE TOO FAR FROM LDO, ROUTE WITH 15 MIL TRACE

CAD NOTE: TAP AT MAIN LOAD POINT.

Wed Aug 23 00:53:08 2023

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		SCALE:  		DO NOT SCALE DRAWING	SHEET 77 OF 111

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Tue Sep 20 14:29:59 2022

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		SCALE:	DO NOT SCALE DRAWING		SHEET 78 OF 111

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## POWER MISC 7

VCCERT\_RNR

VCCERT\_RNR 1V@12A

FREQUENCY: 1MHZ

CAD NOTE: TAP AT MAIN LOAD POINT.

VCCEHT\_BRK\_GXF\_U20\_U22

1.5V @ 7.6A

FREQUENCY: 1MHZ

CAD NOTE: TAP AT MAIN LOAD POINT.

Wed Aug 23 00:53:08 2023

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CODE

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DOCUMENT NUMBER

M60500

REV

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80 OF 111

POWER MISC 8

VCCERT\_UX\_GDR\_U10  
1V @10A

VCCERT\_UX\_GDR\_U10

FREQUENCY: 1MHZ

1V8\_FPGA

1.8V @10A

FREQUENCY: 1MHZ

CAD NOTE: TAP AT MAIN LOAD POINT.

Wed Aug 23 00:53:08 2023

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REV

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M60500

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81 OF 111

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Thu Jul 27 00:35:56 2023

POWER MISC 9

DEPARTMENT

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CODE

34649

DOCUMENT NUMBER

M60500

REV

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SCALE:

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82 OF 111

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Sun May 29 16:08:34 2022

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POWER MISC 10



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UNKNOWN	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	SCALE:	DO NOT SCALE DRAWING		SHEET 84 OF 111



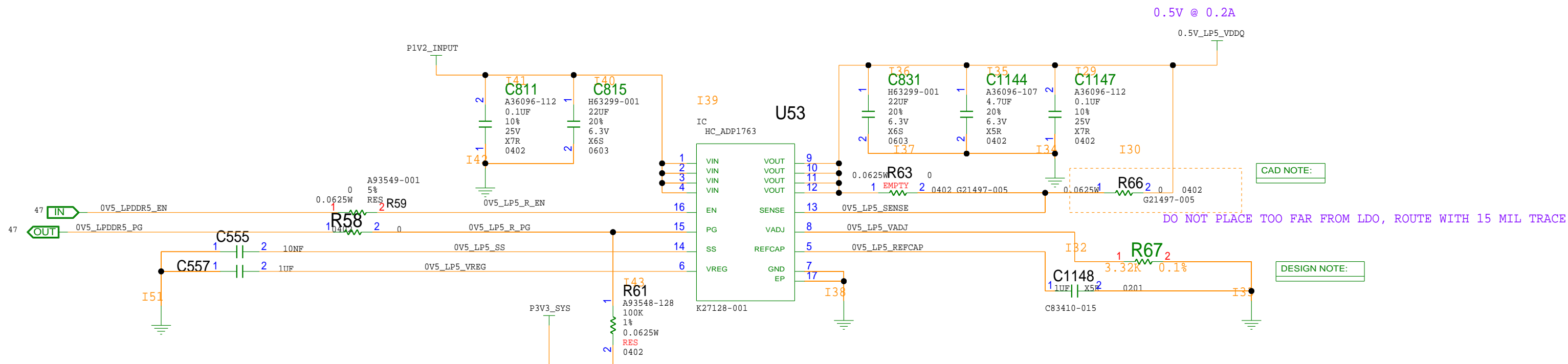
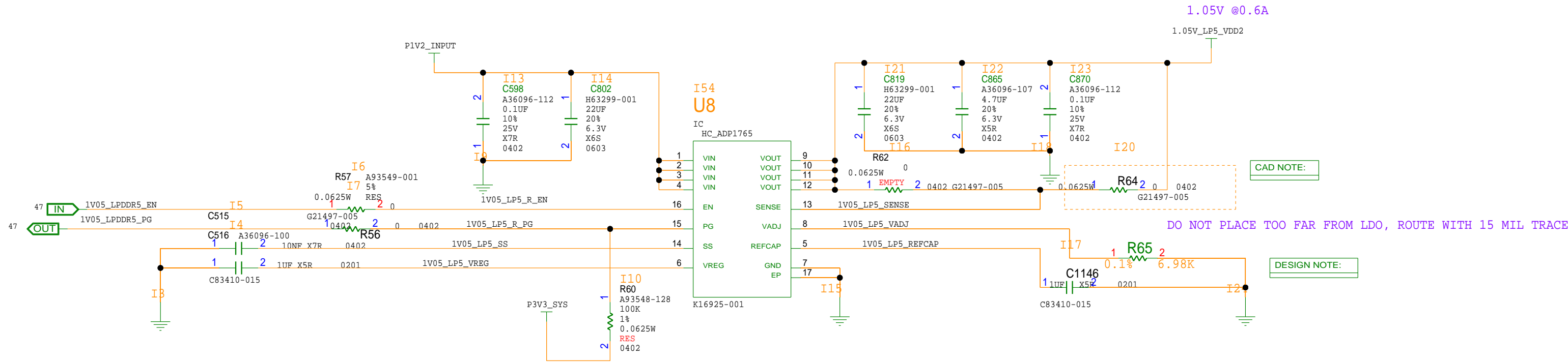
LPDDR5 0V9 0V5 1V05 1V8



POWER MISC 11

1

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DOCUMENT NUMBER

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86 OF 111

## VCCEHT\_UX\_GDR\_U20 &amp; VCCEHT\_UX\_GDR\_U22

POWER MISC 13

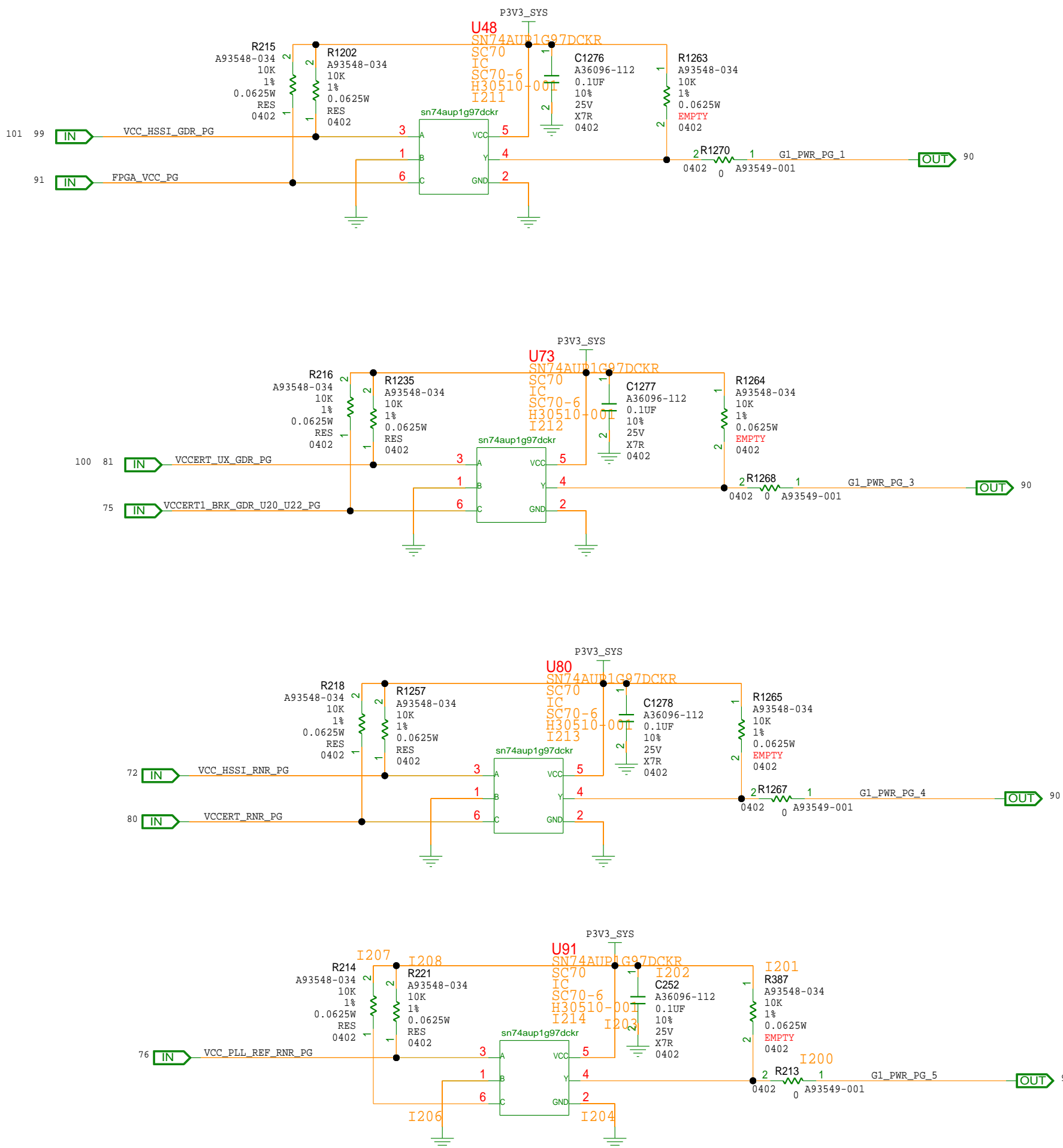


POWER MISC 14

Wed Aug 23 00:53:09 2023

POWER MISC 15

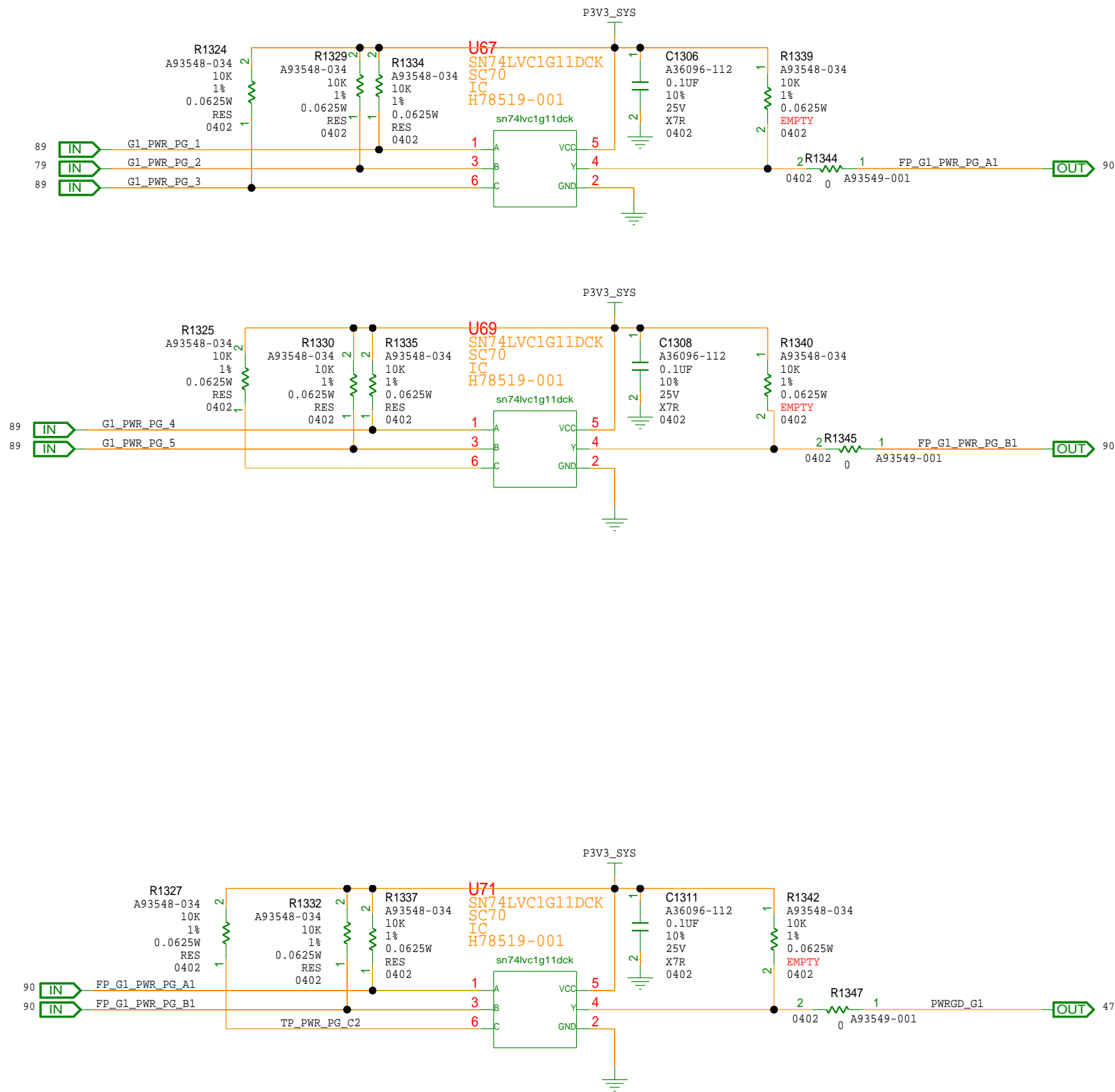
COPY FROM EIGHTMILE RIDGE



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POWER MISC 16



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90 OF 111



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91 OF 111

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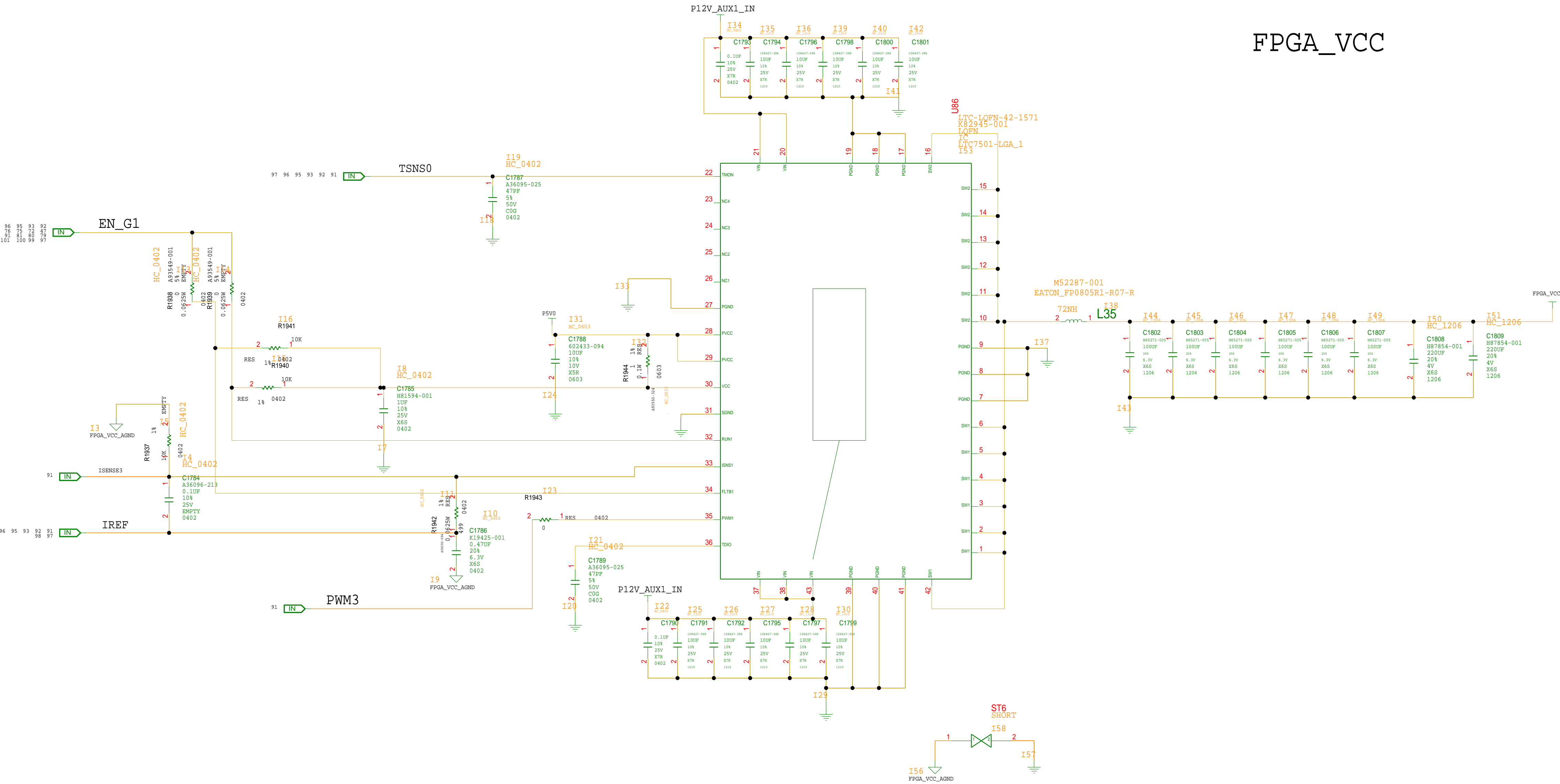
FPGA\_VCC

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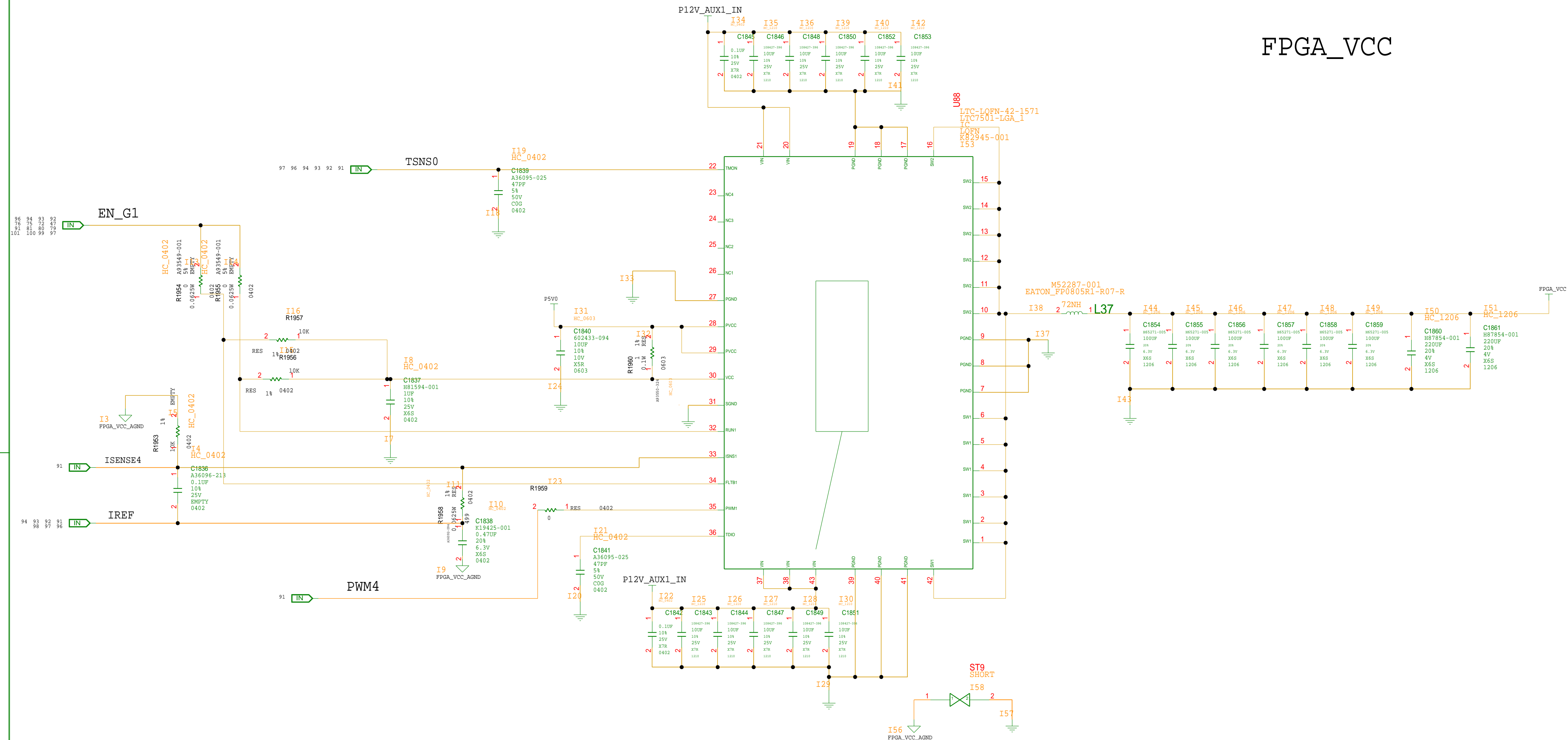
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94 OF 111



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CODE
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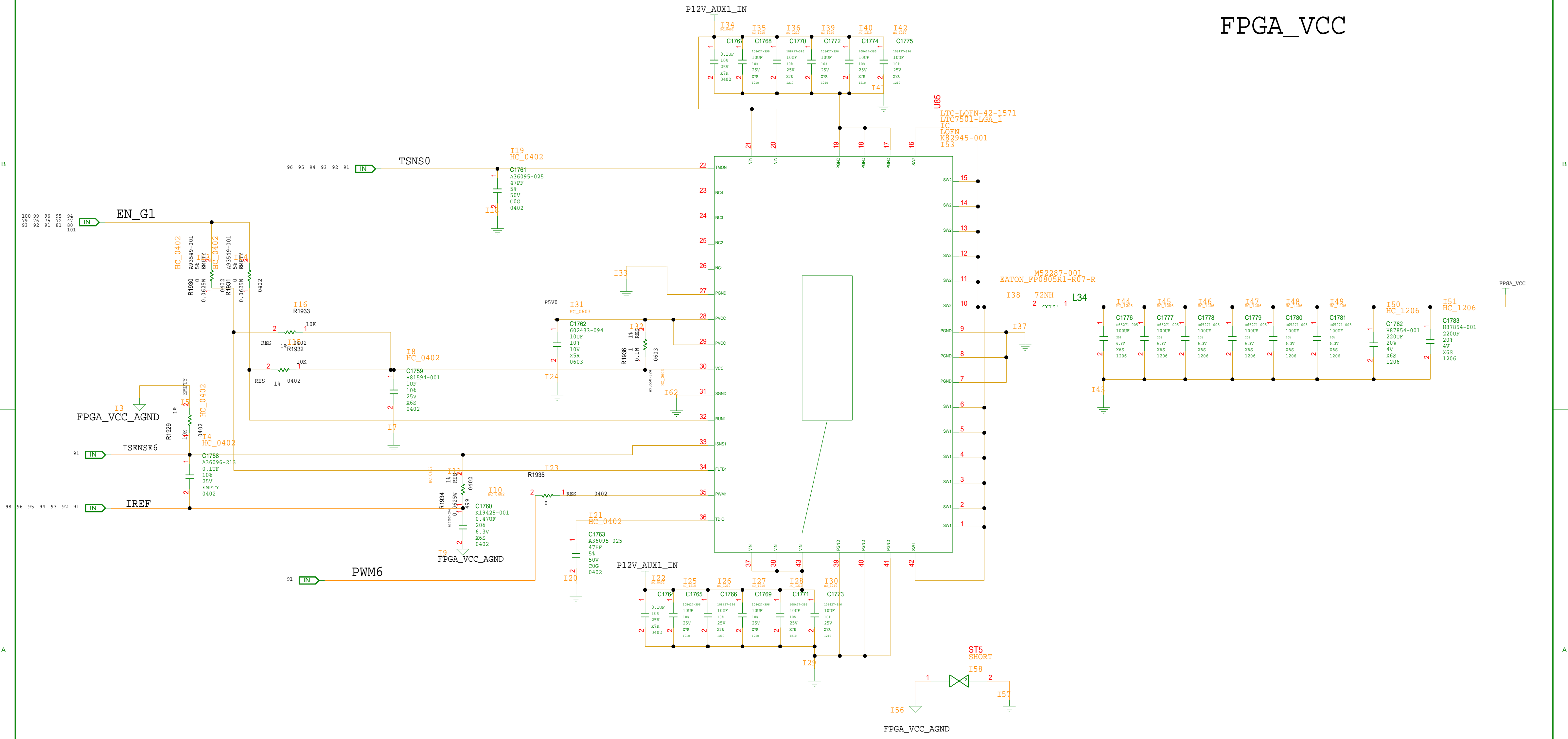
SCALE:

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FPGA\_VCC

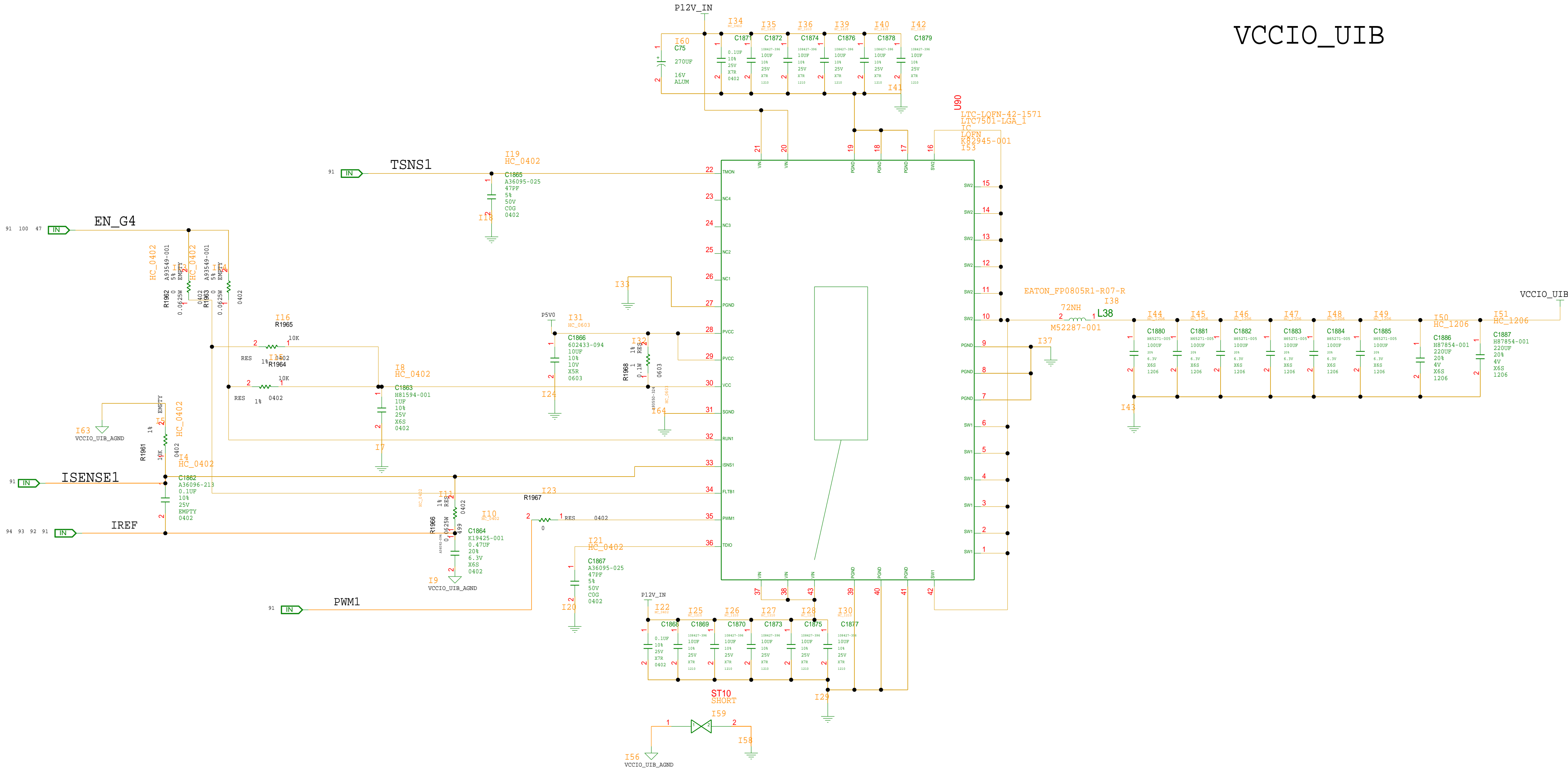


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REV

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SCALE:

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98 OF 111



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0.8V@40A

VCC\_HSSI\_GDR\_U20\_U22

ADDRESS : 0X77H

PLACE TEMP SENSE NEAR L14

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DOCUMENT NUMBER

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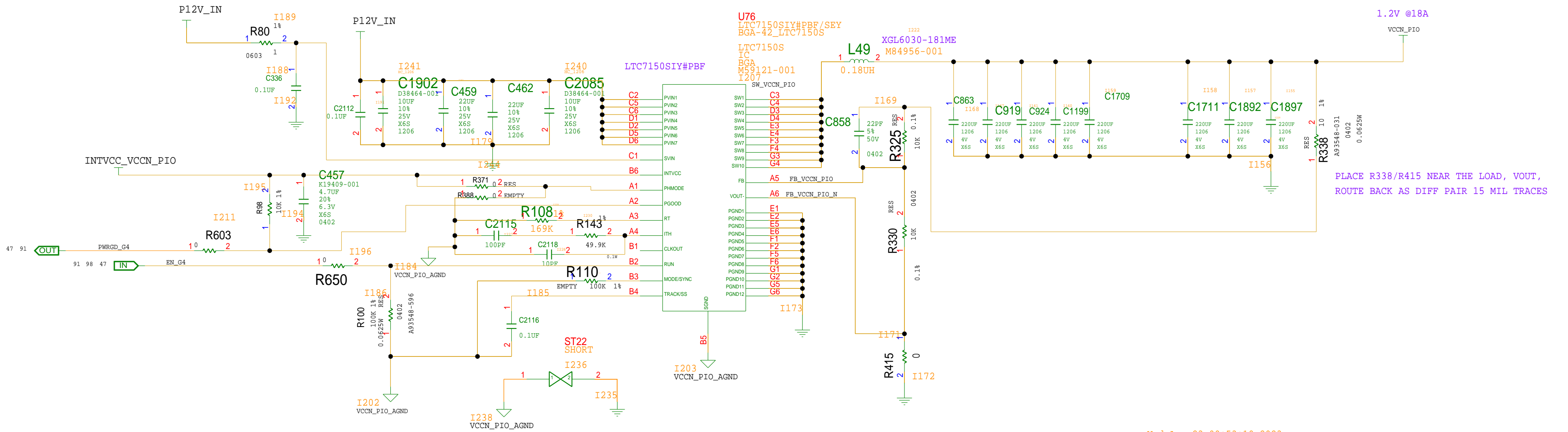
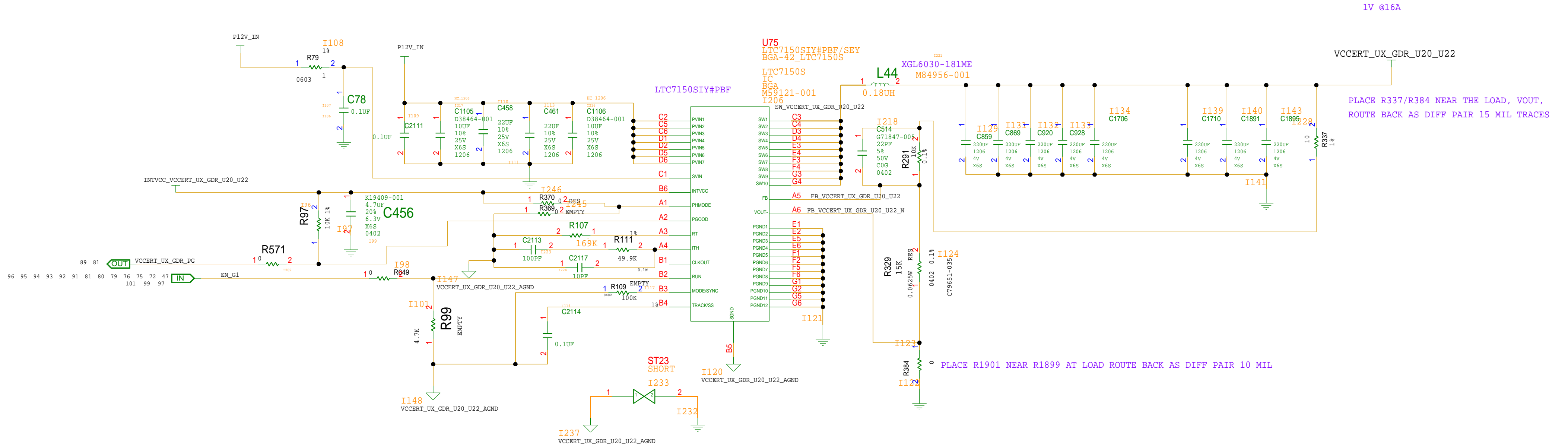
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99 OF 111

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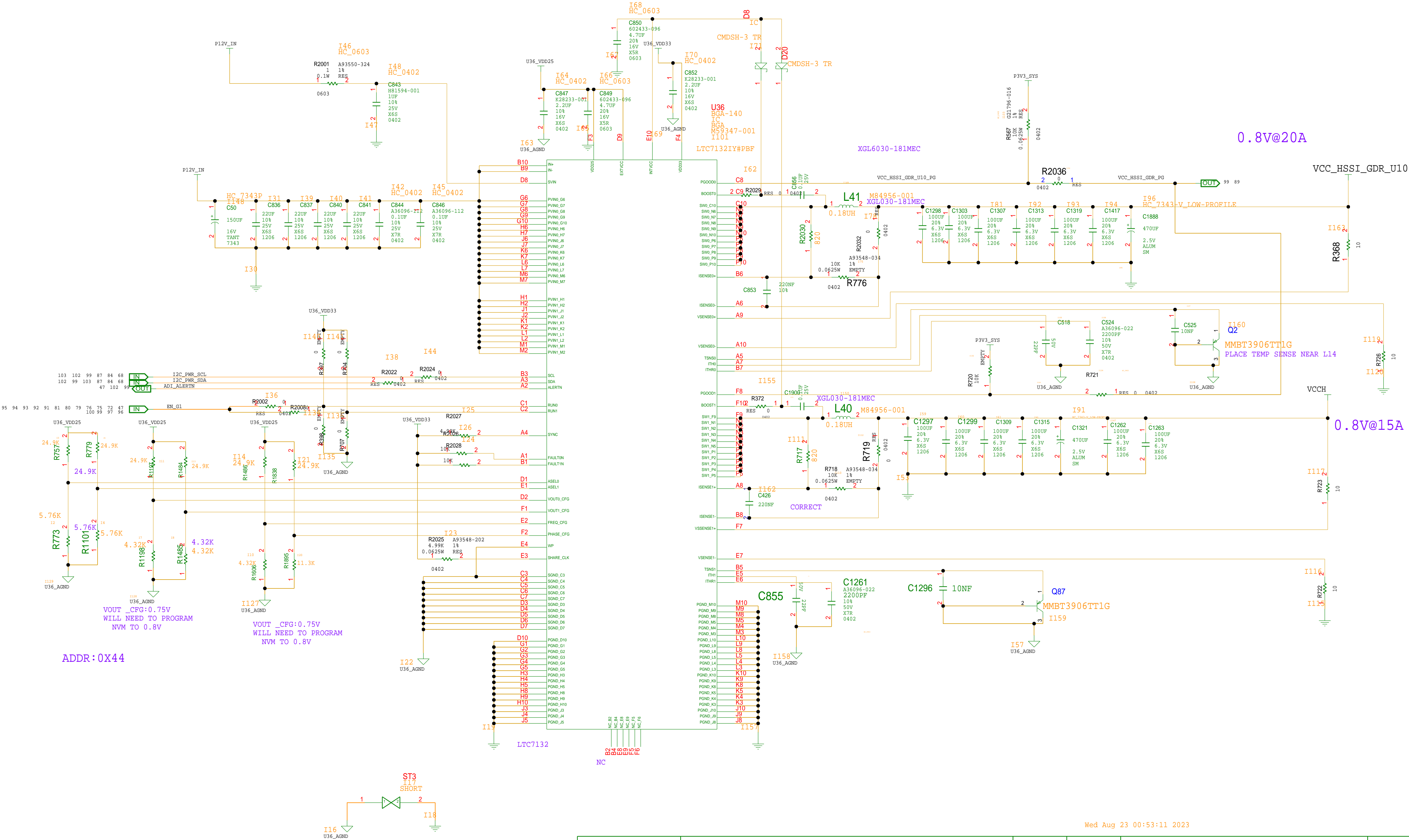
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100 OF 111

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101 OF 111



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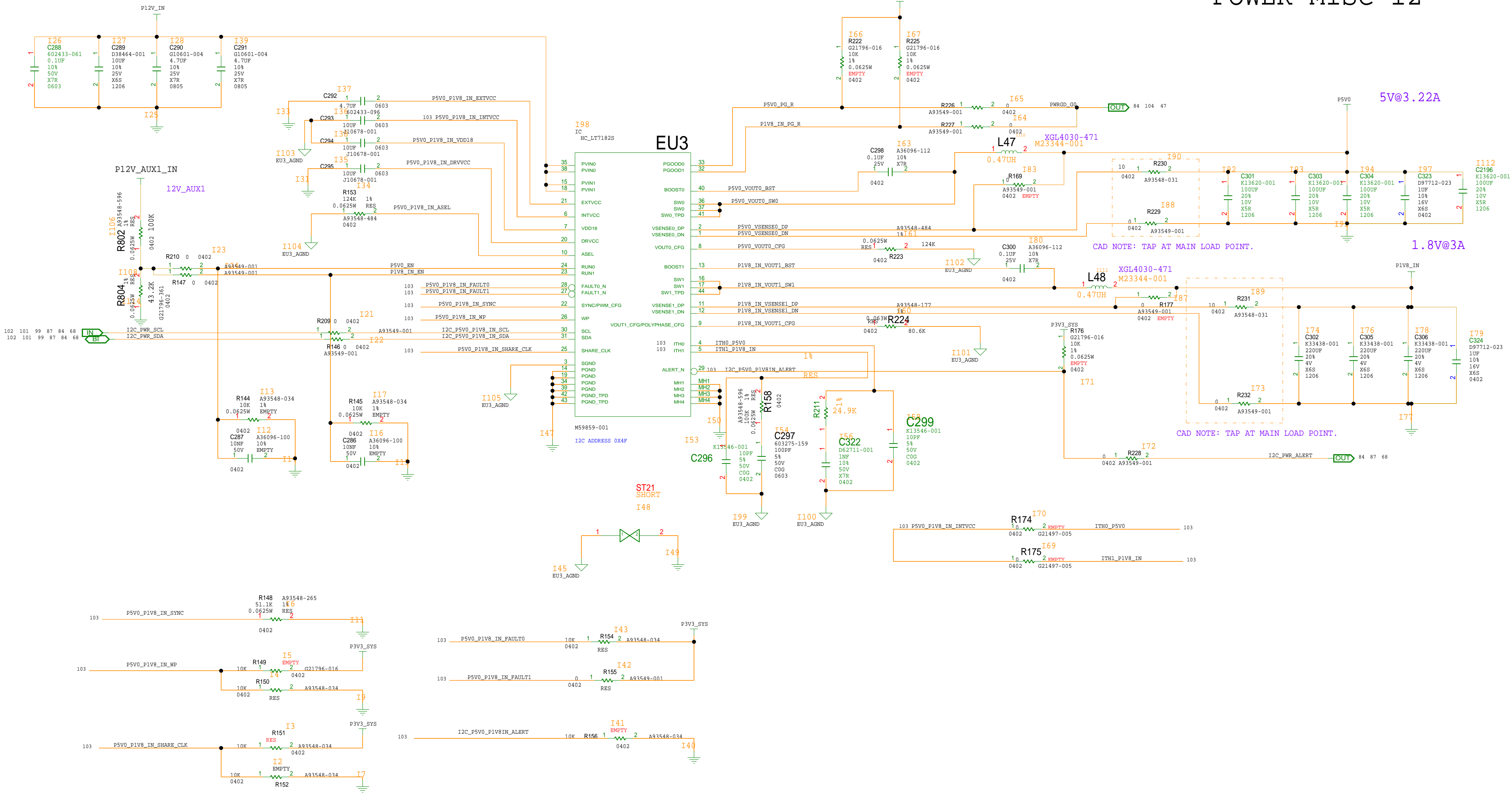
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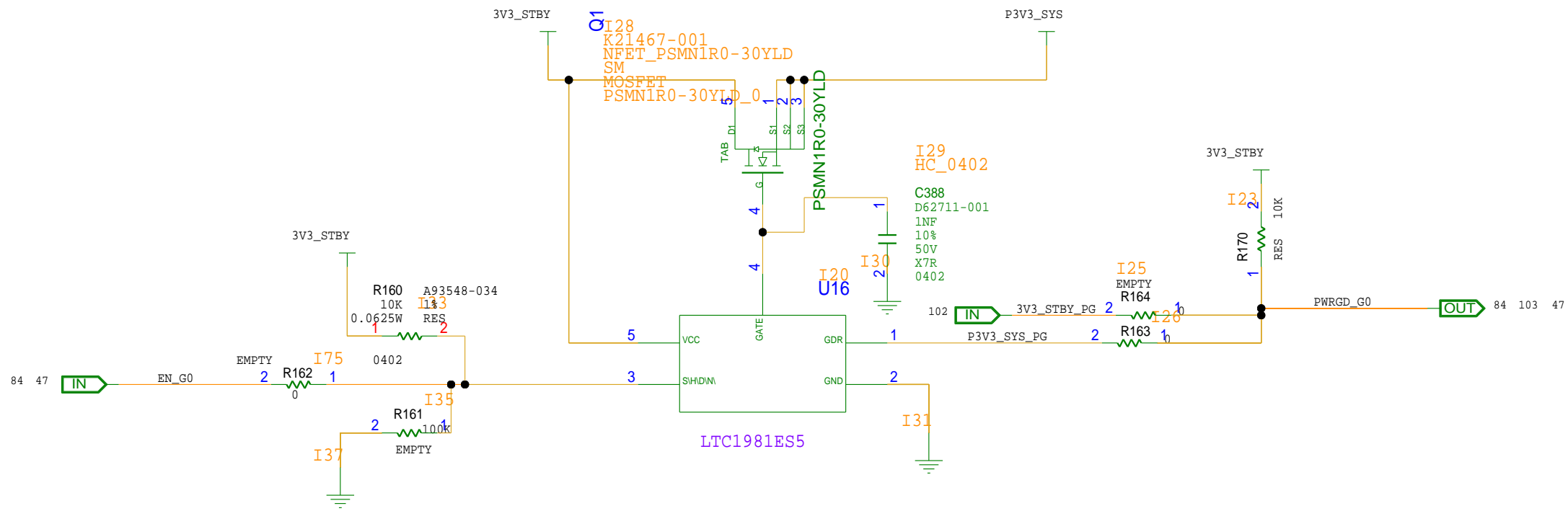
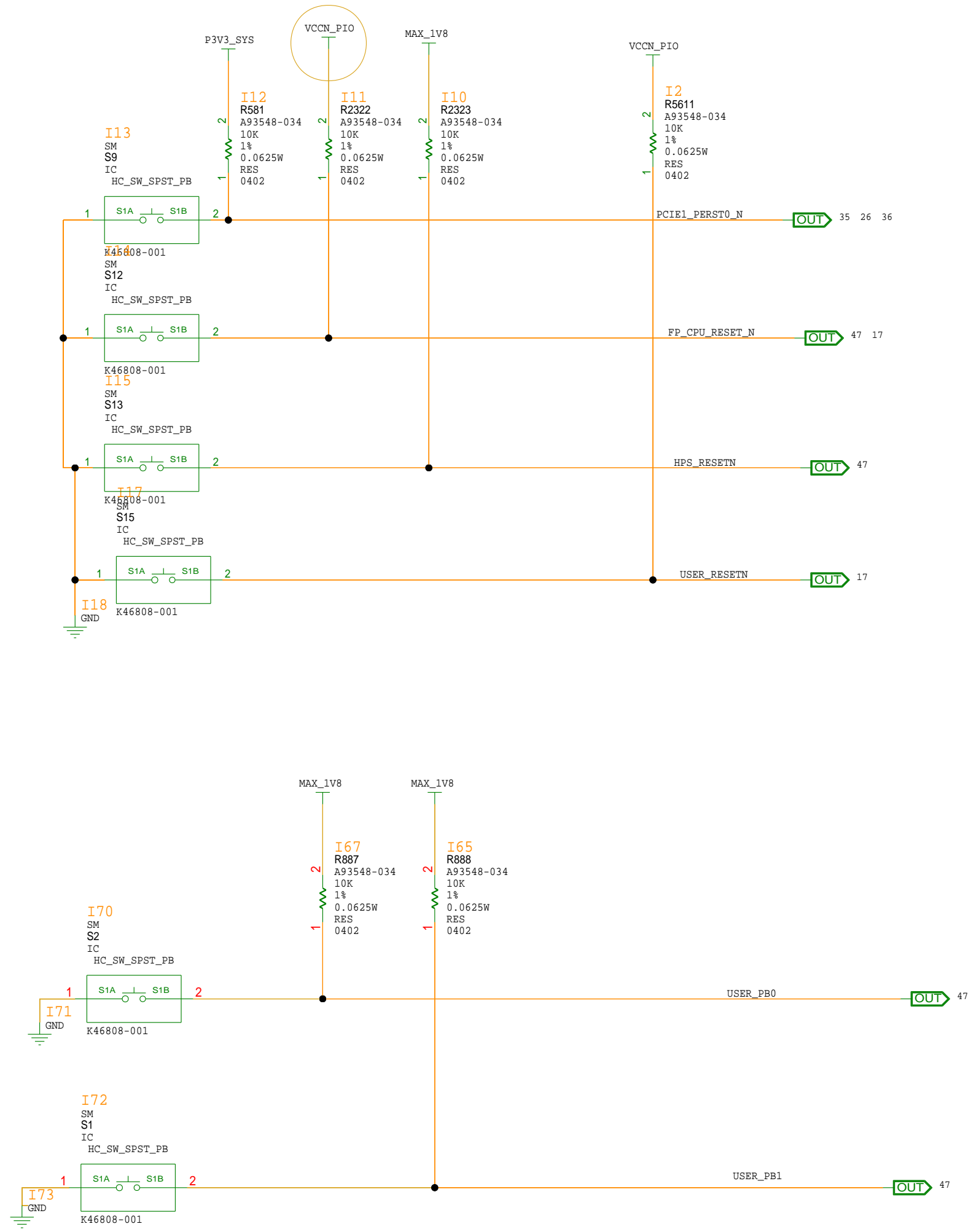


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# POWER MISC 12



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Fri Oct 6 12:44:26 2023

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SIZE  
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CODE  
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DOCUMENT NUMBER

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REV  
0.1

SCALE:

DO NOT SCALE DRAWING

SHEET

104 OF 111

```

3: CHANGE RESISTOR OPTIONS AND ROUTE LA_P/N/32/33 TO SYSTEM
   MAX10 WHEN THESE PINS RUN 3.3V SIGNALS
   [ INTEL BUILT FMC+ TO PCIE GOLD FINGER CABLE, SAMTEC]

4: NOT GUARANTEE SUPPORT OTHER FMC CARDS IF:
   FMC DAUGHTER CARD'S ON-BOARD LEVEL SHIFTER DOESN'T SUPPORT
   THE REQUIREMENT OF FMC DIFFERENTIAL SIGNAL IS NOT COMPLIANT
   WITH A6LXEX 1.2V IO

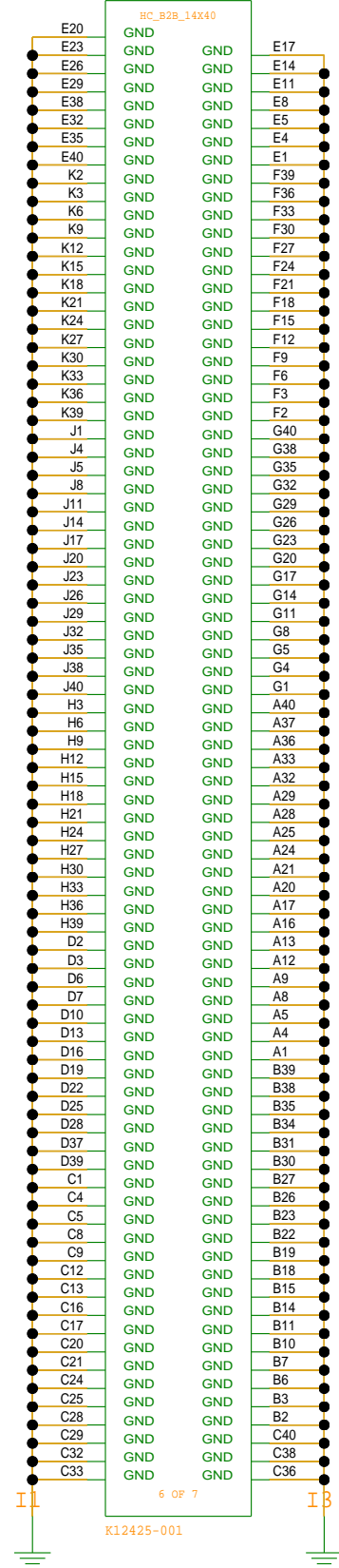
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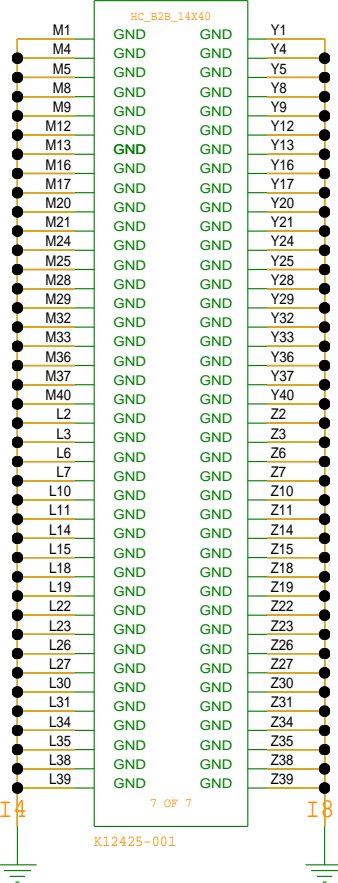


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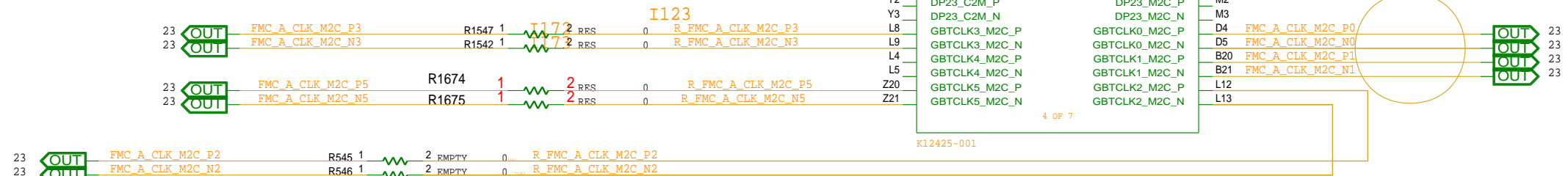
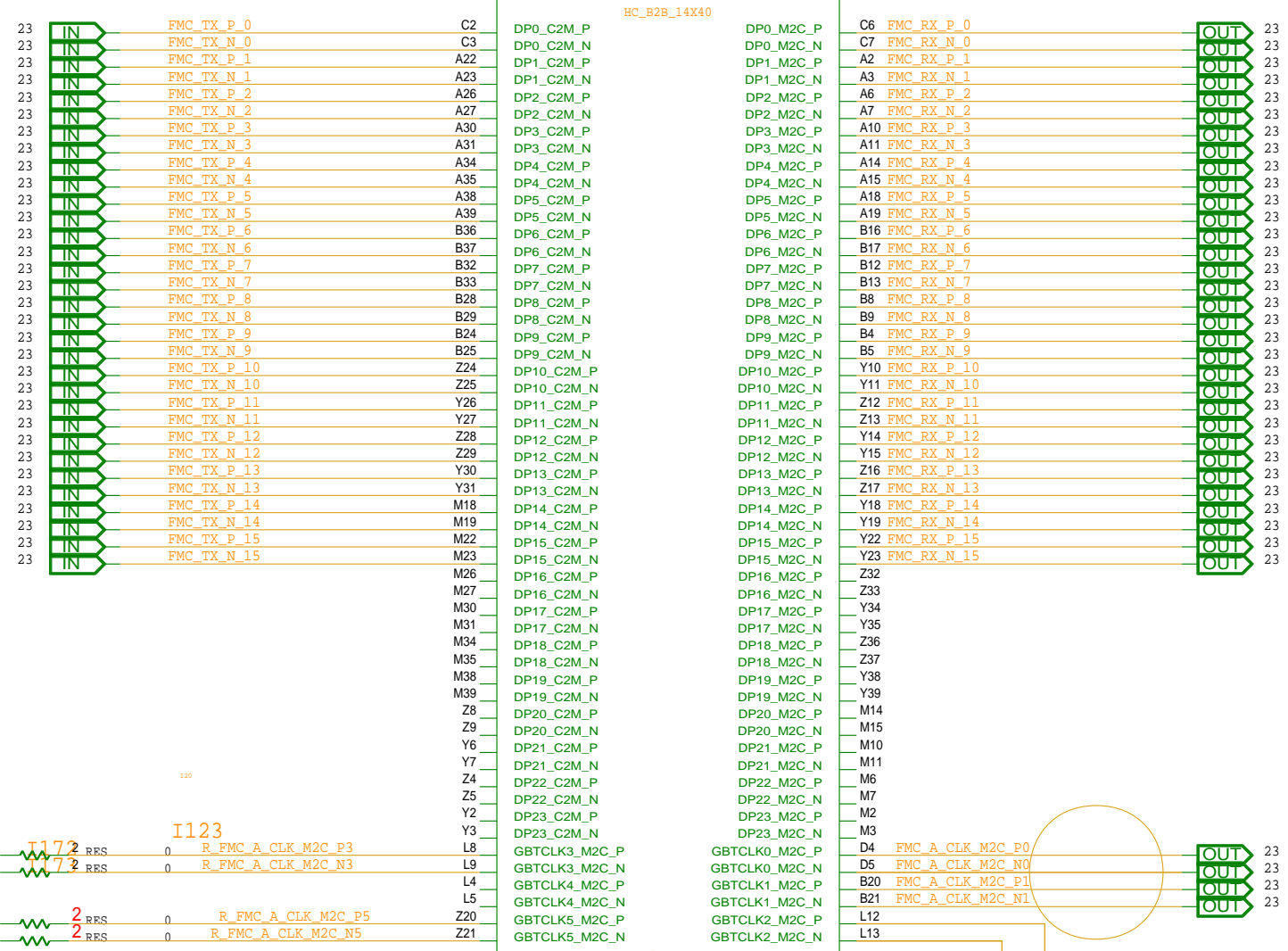
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J34  
SCOR



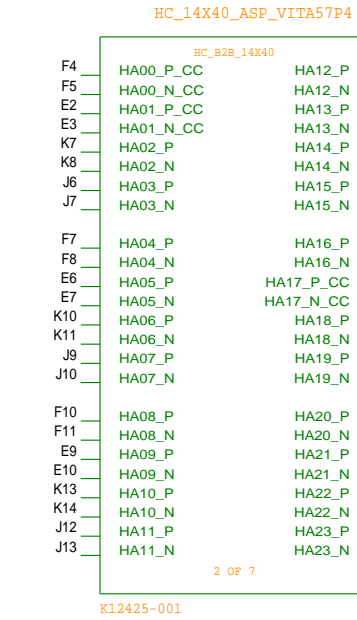
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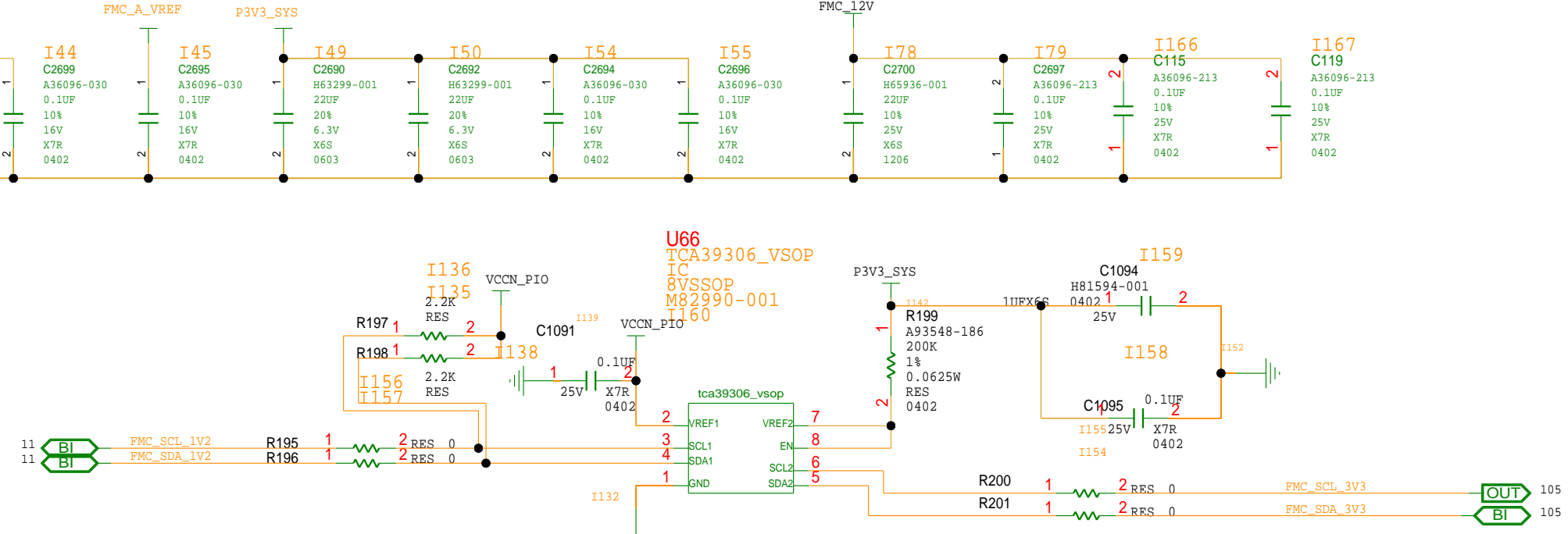
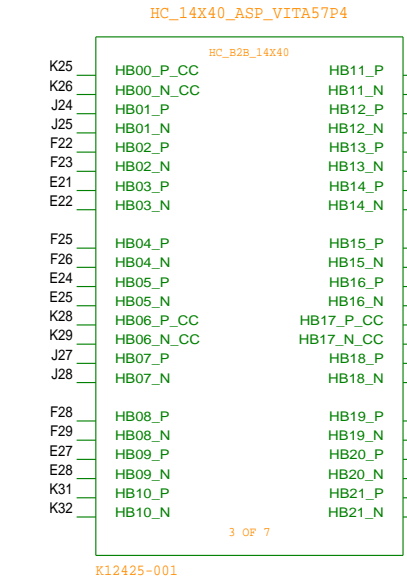
I109  
J34  
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I5  
J34  
SCOR



I6  
J34  
SCOR



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REV

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SHEET

106 OF 111



B



SHEET 107 OF 111

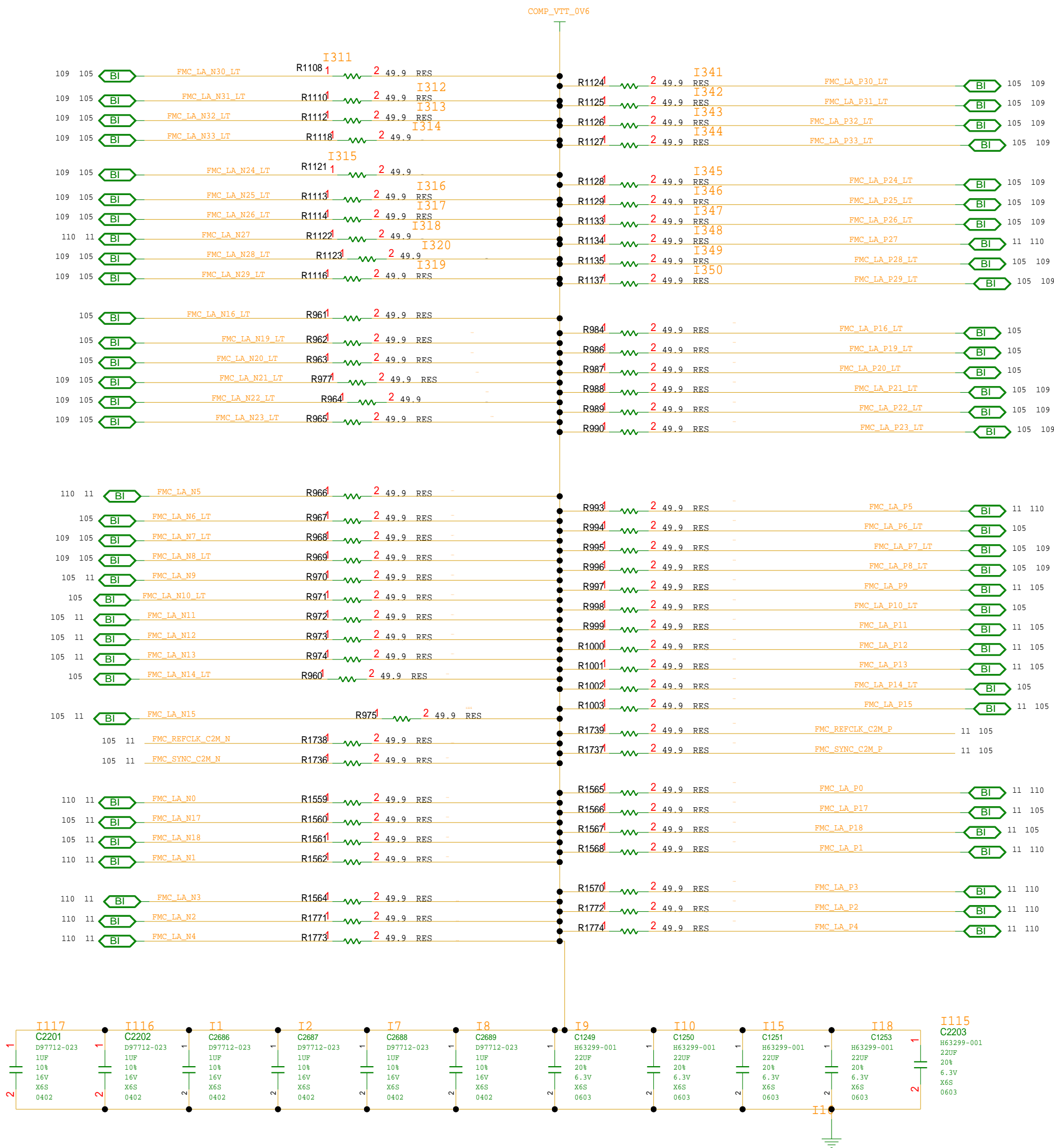
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DOCUMENT NUMBER

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SHEET

108 OF 111

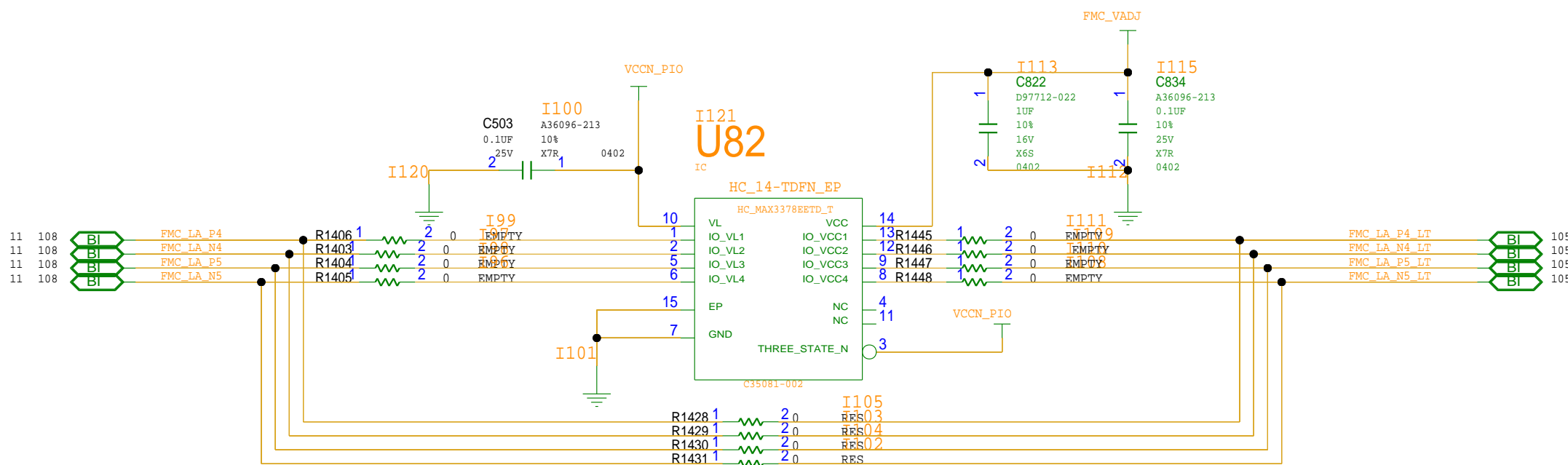
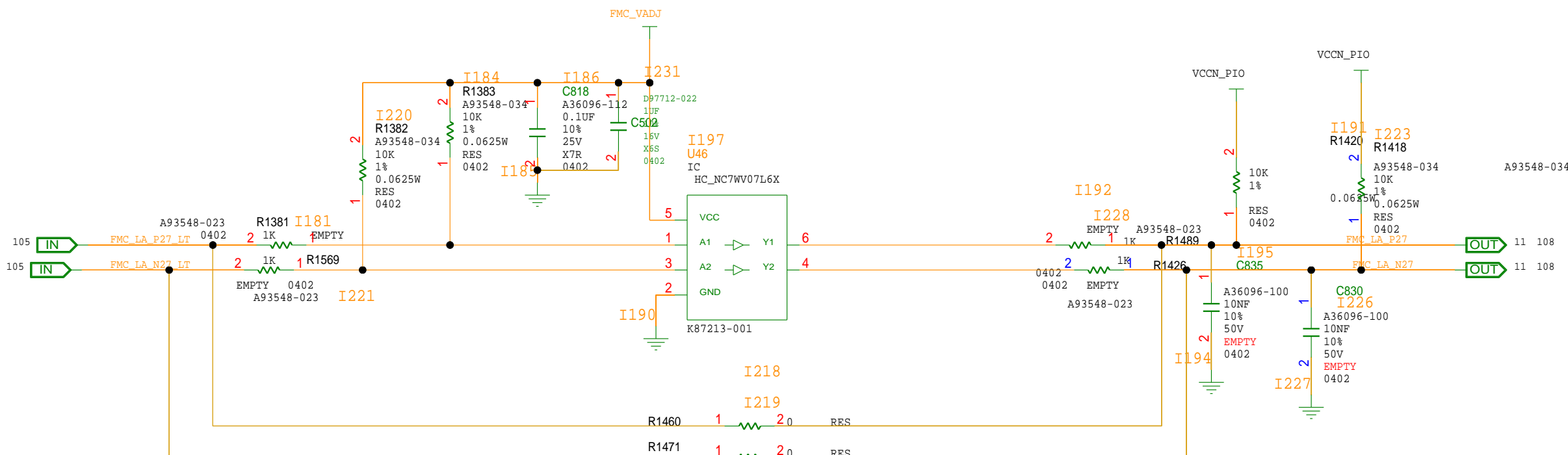
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FMC VT

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UNKNOWN	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	SCALE:		DO NOT SCALE DRAWING	SHEET 109 OF 111

CAD Note:

# VOLTAGE TRANSLATOR



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4

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B

B

## CHANGE LOG

REV A TO REV B VERSION

1)CHANGE THE PACKAGE ON I2C VT

2)CHANGE THE PACKAGE ON THE VT OF GPIO

3) FIXED 3 WIRE ON BOARD

A

A

Tue Aug 22 23:41:07 2023

REVISION HISTORY

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