

# Agilex<sup>™</sup> 7 FPGA M-Series HBM2e Development Kit User Guide



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**2024.05.14**

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## 1. Overview

The Agilex™ 7 FPGA M-Series HBM2e Development Kit FPGA M-Series HBM2e Development Kit is a complete design environment that includes both hardware and software you need to develop Agilex 7 FPGA M-Series HBM2e designs. The board provides a wide range of peripherals and memory interfaces to facilitate the development of Agilex 7 FPGA M-Series HBM2e designs.

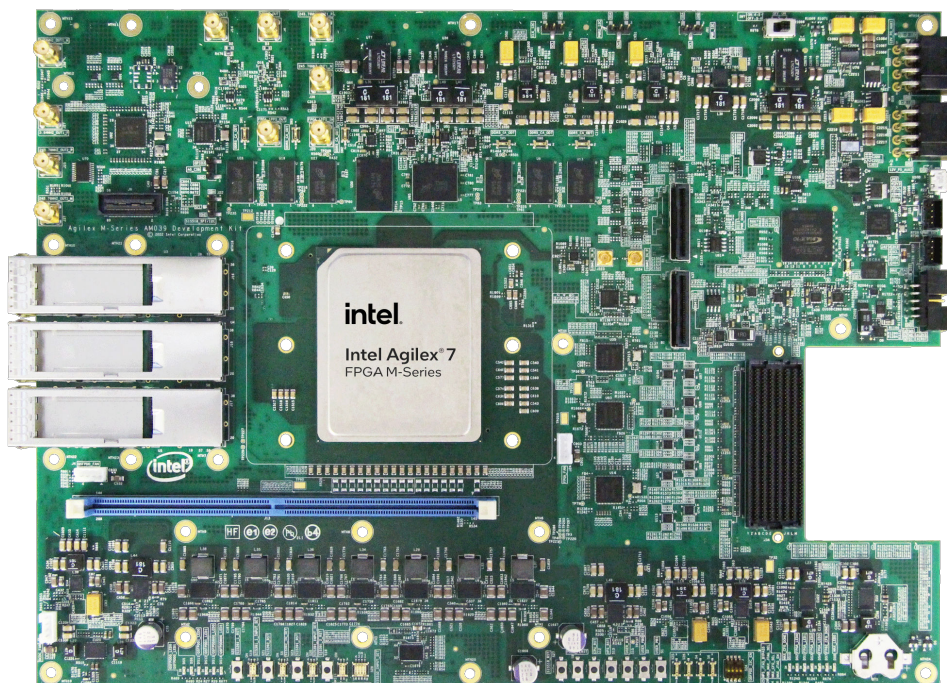
**Table 1. Ordering Information**

Development Kit Version	Ordering Code	Device Part Number	Serial Number Identifier
Agilex 7 FPGA M-Series Development Kit - HBM2e Edition (ES1 3x F-Tile and 1x R-Tile)	DK-DEV-AGM039FES	AGMF039R47A1E2VR0	AGM82DK0000001
Agilex 7 FPGA M-Series Development Kit - HBM2e Edition (Production 1 3x F-Tile and 1x R-Tile)	DK-DEV-AGM039EA	AGMF039R47A1E2VB	AGM82DK0001001

For the board and FPGA capabilities, refer to the *Agilex 7 FPGA and SoC FPGA M-Series* page on the Intel® website.

For more information about the *Agilex 7 Device Errata Sheet and User Guidelines (ES-1069)* and *Agilex 7 Known Issue List*, contact Intel Premier Support and quote ID #15011992053.

**Figure 1. Agilex 7 FPGA M-Series HBM2e Development Kit Top**



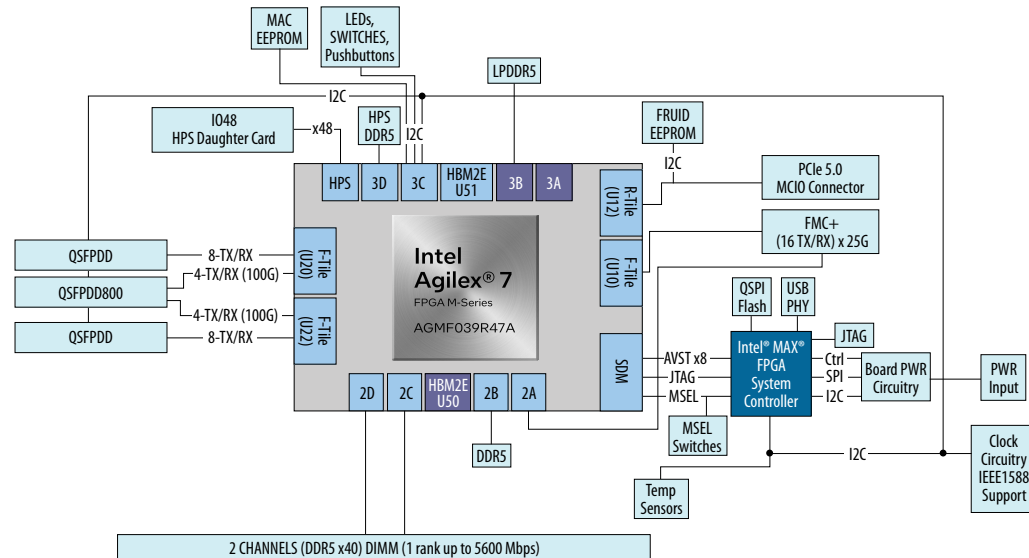
#### **Related Information**

[Agilex 7 FPGA and SoC FPGA M-Series Webpage](#)

## 1.1. Block Diagram

**Figure 2. Agilex 7 FPGA M-Series HBM2e Development Kit Block Diagram**

Note: Avalon® streaming interface x8 configuration mode (AVSTx8)



## 1.2. Feature Summary

- Agilex 7 FPGA M-Series (AGM039) device in 4700A BGA package
  - Quad-core 64-bit Arm Cortex-A53 hard processor (HPS)
  - 0.8 V VID-adjustable VCC core
  - F-Tile x3, R-Tile x1, and HBM2E
  - F-Tile 32G NRZ (58G PAM4) / High-Speed Transceiver 58G NRZ (116G PAM4) / R-Tile 32G PCIe\* (CXL) Lanes
  - 3.9M logic elements (LE)
  - 1.3M adaptive logic modules (ALM)
  - 12.3K digital signal processing (DSP) blocks
- FPGA configuration
  - Avalon streaming interface x8 configuration mode support
  - 2 Gb flash for Avalon streaming interface x8 configuration mode
  - JTAG header for device programming
  - Built-in Intel FPGA Download Cable II for device programming
- Programmable clock sources

- Transceiver interfaces
  - PCI Express\* (PCIe) x16 interface supporting Gen 5 endpoint connected to a MCIO connector
  - 2x QSFPDD optical module interface connected to F-Tile transceiver
  - 1x QSFPDD 800 optical module interface connected to F-Tile transceiver
  - 16 F-Tile transceiver connect to FMC+ connector
- Memory interfaces
  - 2 x40 DIMM sockets supporting DDR5-5600
  - 1 x40 DDR5-5600 component interface for HPS processor memory
  - 1 x40 DDR5-5600 component interface for fabric I/O memory
  - 2 X 16 LPDDR5 component, 2 channels and each is 16 bit data line interface
- Communication ports
  - JTAG header
  - Micro USB on-board Intel FPGA Download Cable II
  - System I2C header
- Buttons, switches, and LEDs
  - CPU reset push button
  - PCIe reset push button
  - CXL reset push button
  - HPS reset push button
  - Four dedicated user LEDs
  - Board power good LED
  - BMC MAX<sup>®</sup> 10 configuration done LED
  - FPGA configuration done LED
- Heatsink and fan
  - Air-cooled heatsink assembly for FPGA
  - Air-cooled heatsink assembly for 1 port of QSFPDD-800 and 2 ports of QSFPDD and all 3 ports support class 8
  - Red over-temperature warning LED
- Power
  - PCIe input power including required 2x4 auxiliary power connector
  - Blue power-good status LED
  - On/Off slide power switch for benchtop operation
  - On-board power and temperature measurement circuitry
- Mechanical
  - 4.375" x 10.0" board size
- Operating environment
  - Maximum ambient temperature of 0°C–30°C

## 1.3. Box Contents

- Agilex 7 FPGA M-Series HBM2e Development Kit
- 1x DDR5 DIMM module
- 1x IO48 HPS daughter board
- USB 2.0 MicroUSB cable
- 240W power adapter and NA/EU/JP/UK cords

## 1.4. Recommended Operating Conditions

**Table 2. Recommended Operating Conditions**

Operating Condition	Range of Values
Ambient operating temperature range	0°C to 30°C
ICC load current	195 A
ICC load transient percentage	200 A/μs
FPGA maximum power supported by active heatsink/fan	410 W

When handling the board, it is important to observe static discharge precautions.

**Caution:** Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the development kit.

**Note:** This development kit should not be operated in a vibration environment.



## 2. Getting Started

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### 2.1. Quartus® Prime Software and Driver Installation

Quartus® Prime design software is a multiplatform design environment that easily adapts to your specific needs in all phases of FPGA, CPLD and SoC designs. The Quartus Prime software delivers the highest performance and productivity for Intel FPGAs, CPLDs, and SoCs. Quartus Prime Pro Edition software is optimized to support the advanced features in next-generation FPGAs and SoCs with the Agilex 7, Stratix® 10, Arria® 10, and Cyclone® 10 GX device families.

Agilex 7 FPGA M-Series HBM2e Development Kit includes on-board Intel FPGA Download Cable circuits for FPGA and system MAX 10 programming. However, for the host computer and board to communicate, you must install the Intel FPGA Download Cable driver on the host computer. Installation instructions for the Intel FPGA Download Cable driver for your operating system are available on the Intel website.

On the Intel website, navigate to the *Cable and Adapter Drivers Information* link to locate the table entry for your configuration and click the link to access the instructions.

The Intel SoC EDS is a comprehensive software tool suite for embedded software development on Intel SoC devices. It contains development tools, utility programs, run-time software, and application examples to expedite firmware and application software of SoC embedded systems.

As a part of the Intel SoC EDS, the Arm® Development Studio 5 (DS-5) Intel SoC FPGA Edition Toolkit provides a comprehensive set of embedded development tools for Intel's SoC FPGAs.

For more information and steps to install the Intel SoC EDS Tool Suite, refer to the links below.

#### Related Information

- [Quick-Start for Intel Quartus Prime Pro Edition Software](#)
- [Intel Quartus Prime Pro Edition User Guide: Getting Started](#)
- [Arm DS-5 Intel SoC FPGA Edition Toolkit](#)
- [Intel SoC FPGA Embedded Development Suite User Guide](#)
- [Cable and Adapter Drivers Information](#)

### 2.2. Design Examples

Unzip the install package which includes board design files, documents and examples directories. The table below lists the file directory names and a description of their contents.

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\*Other names and brands may be claimed as the property of others.

**Table 3. Installed Development Kit Directory Structure**

Directory Name	Description of Directory Contents
board_design_files	Contains schematics, layout, assembly and bill of material board design files. Use these files as a starting point for a new prototype board design
documents	Contains the development kit documentation – quick start guides and user guide
examples	Contains: <ul style="list-style-type: none"> <li>Board Test System: BTS GUI, Power GUI, and Clock GUI</li> <li>Golden Top project for pinout assignments management</li> <li>Design Examples: Memory, XCVR, GPIO</li> </ul>
factory_recovery	The original data programmed into flash U98 for Avalon streaming interface x8 configuration before shipment.

## 3. Development Kit Setup

The instructions in this chapter explain how to setup the Agilex 7 FPGA M-Series HBM2e Development Kit for specific use cases.

### 3.1. Default Settings

The Agilex 7 FPGA M-Series HBM2e Development Kit ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be correctly configured with the default settings, follow the instructions in the factory default switch settings table to return to its factory settings before proceeding ahead.

**Table 4. Factory Default Switch Settings**

*Note:* X refers to Don't Care in the table below.

*Note:* Do not set the switches when the power is on. Only set the switches after the power is off.

Switch	Default Position	Notes
S24[1:4]	OFF/OFF/OFF/ON	S24[1:3] Set MSEL mode: <ul style="list-style-type: none"> <li>111: JTAG</li> <li>011: Avalon streaming interface x8 configuration mode</li> </ul> S24[4]: <ul style="list-style-type: none"> <li>OFF-FPGA can access three QSPDD modules</li> <li>ON-system_info_0_slv_data_write_0[2] determines if FPGA can access three QSPDD modules or not. No access by default.</li> </ul>
S25	OFF	<ul style="list-style-type: none"> <li>OFF-HPS is not in the JTAG chain</li> <li>ON-HPS is in the JTAG chain</li> </ul>
S3	OFF	<ul style="list-style-type: none"> <li>OFF-FMC+ is not in the JTAG chain</li> <li>ON-FMC+ is in the JTAG chain</li> </ul>
S26	ON	<ul style="list-style-type: none"> <li>ON-MAX 10 programming via on-board Intel FPGA Download Cable</li> <li>OFF-MAX 10 programming via external Intel FPGA Download Cable</li> </ul>
	OFF	Using mini USB JTAG
S28[1:4]	OFF/ON/OFF/OFF	S28[1:2] Select the clock source for EU122:
continued...		

Switch	Default Position	Notes
		<ul style="list-style-type: none"> <li>ON:ON-disabled</li> <li>OFF:ON-internal crystal (default)</li> <li>ON:OFF-CLKIN2 (MCIO)</li> <li>OFF:OFF-CLKIN3 (SMP)</li> </ul> <p>S28[3:4] Set SSC:</p> <ul style="list-style-type: none"> <li>ON:X-disabled (default)</li> <li>OFF:X-AND OUT0</li> <li>X:ON-disabled (default)</li> <li>X:OFF-enable SS on N1 divider OUT6, OUT7</li> </ul>
SW6	OFF	<p>MAX 10 JTAG Enable switch when the JTAG pin sharing is enabled:</p> <ul style="list-style-type: none"> <li>ON-JTAG pins function as dual-purpose pins</li> <li>OFF-JTAG pins function as JTAG dedicated pins</li> </ul> <p>This switch can be set to either ON or OFF with the current MAX 10 design because the JTAG pin sharing is not enabled in the design.</p>
S4	ON	<p>Select configuration image in the dual-configuration images mode:</p> <ul style="list-style-type: none"> <li>ON-the first configuration image is <b>configuration image 0</b></li> <li>OFF-the first configuration image is <b>configuration image 1</b></li> </ul> <p>This switch can be set to either ON or OFF with the current MAX 10 design because single image mode is used in the design.</p>
S16	[1]/[0]	Controls the configuration for the U35 clock device
	OFF/OFF (default)	Input clock from XTAL
	OFF/ON	Input clock from SI5391
	ON/OFF	Input clock from FPGA
	ON/ON	Not connected
SW20	[1]/[0]	Controls the configuration for the U93 clock device
	OFF/OFF(default)	Input clock from XTAL
	OFF/ON	Input clock from SI5391
	ON/OFF	Input from FPGA
	ON/ON	Not connected

## 3.2. Powering Up the Development Kit

To power up the development kit, follow these steps:

1. Use the provided 300 W power adapter to supply power through **J12** and **J3**.
2. After the power adapter is plugged into **J12** and **J3**, and switch **S7** is set to the **ON** position, **DS15** LED illuminates, indicating that the board powered up successfully. If the LED (**DS15**) is not turned ON, it indicates that one of the voltage regulators is not turned on.

*Note:* All the QSPFDD and QSPFDD800 ports can support up to class 8, meaning each port consumes 18 W. Two power supplies are needed to provide sufficient power for peak performance.

The Agilex 7 FPGA M-Series HBM2e Development Kit can run the loop back test or memory test using only one power adapter connected to **J12**. Since one power adapter can provide 300 W maximum, the Agilex 7 FPGA M-Series HBM2e Development Kit can only run diagnostic tests.

## 3.3. Performing Board Restore

This development kit ships with `bts_config` design examples stored in the QSPI flash device. You can perform board restore by following the instructions below through the Quartus Prime Programmer GUI.

### 3.3.1. Restoring Board QSPI Flash with Default Factory Image

*Note:* The QSPI flash is pre-programmed with 4 pages of images. Follow the steps to overwrite the Avalon streaming interface x8 configuration mode image.

1. Ensure that MSEL[2:0] is OFF (JTAG mode) before powering up the board.
2. Open Quartus Prime Programmer GUI, detect JTAG chain.
3. Change VTAP10 to 10M50DAF256, attach flash device of QSPI\_2Gb.
4. Attach the Avalon streaming interface x8 configuration mode image to QSPI\_2Gb.
5. Select program/configure options and click **Start** button.
6. Power off the board after programming the flash successfully, set MSEL[2:0] OFF OFF ON (Avalon streaming interface x8 configuration mode).

## 4. Board Test System

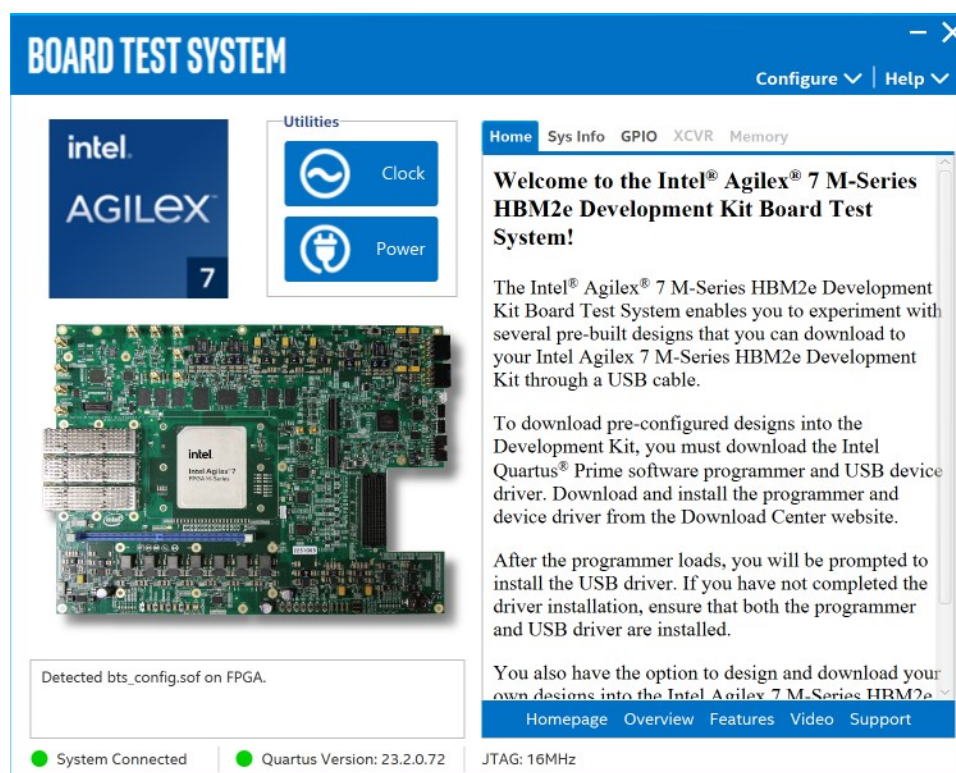
The Agilex 7 FPGA M-Series HBM2e Development Kit includes design examples and the board test system (BTS) GUI to test the functionality of this board. The BTS provides an easy-to-use interface to alter functional settings and observe results. You can use the BTS to test board components, modify functional parameters, observe performance, and measure power usage.

While using the BTS, you can reconfigure the FPGA several times with test designs specific to the functionality that you are testing. The BTS is also useful as a reference for designing systems. The BTS communicates over the JTAG bus to a test design running in the Agilex 7 FPGA.

The BTS checks for hardware faults before you can use the board. If one or more BTS test items fail, it implies either a wrong hardware setting or hardware fault on specific interface.

The following figure shows the graphical user interface (GUI) of a board that is in factory configuration.

**Figure 3. BTS GUI**



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## 4.1. Setting Up the BTS GUI Running Environment

You need to download and install **Java runtime environment** and Quartus Prime software on your systems to run the BTS GUI, including the Power Monitor and Clock Controller GUI. **Java runtime environment** includes **OpenJDK** and **OpenJFX**, whose installation is a one-time procedure. If you have completed it before, you do not need to do it again unless the Java version upgrade is needed.

### 4.1.1. Downloading OpenJDK

Follow these steps to download the Temurin OpenJDK:

1. Download the Temurin OpenJDK from the [Eclipse Temurin\\* Latest Releases](#) page.
2. Select Architecture x64, Package Type JRE, and Version 11.
3. For the **Windows** system option, choose the JRE .zip format file.
4. For the **Linux** system option, choose the JRE tar.gz format file.

*Note:* The JDK version may be updated, always download the latest version.

### 4.1.2. Downloading OpenJFX

Follow these steps to download the OpenJFX:

1. Download the OpenJFX from the [Gluon](#) page.
2. Select the JavaFX version 17.0.2.
3. For the **Windows** system option, download the JavaFX Windows x64 SDK.
4. For the **Linux** system option, download the JavaFX Linux x64 SDK.

### 4.1.3. Installing OpenJDK and OpenJFX

Follow these steps to install the downloaded zip files:

1. On the **Windows** system, Intel recommends that you unzip the files and put them in the following directory:
  - C:\Program Files\Java\jre
  - C:\Program Files\Java\jfx

*Note:* The unzipped folder name of JRE is jdk-11.0.xx+x-jre (for example, jdk-11.0.15+10-jre). Rename it to *jre*.

The unzipped folder name of JFX is javafx-sdk-17.0.2. Rename it to *jfx*.

2. On the **Linux** system, Intel recommends that you unzip the files and rename the folders using the following commands:

```
# unzip openjfx-17.0.2_linux-x64_bin-sdk.zip -d /opt/Java/  
# tar zxvf OpenJDK11U-jre_x64_linux_hotspot_11.0.15_10.tar.gz -C /opt/Java/  
# cd /opt/Java  
# mv javafx-sdk-17.0.2 jfx  
# mv jdk-11.0.15+10-jre jre
```

The following directories are on your **Linux** system:

- /opt/Java/jre
- /opt/Java/jfx

#### 4.1.4. Installing the Quartus Prime Software

You need to install the Quartus Prime software that can support the silicon on the development kit. The recommended version can be found in the `README.txt` file under `examples\board_test_system` directory. If you choose to install individual files, Agilex 7 Device Support is required to install.

The BTS communicates over JTAG to a test design running in the FPGA. The BTS shares the JTAG with other applications like the Nios® II JTAG Debug Module and the Signal Tap Logic Analyzer. Make sure to close other applications before you use the BTS, because the BTS is designed based on the Quartus Prime software.

The BTS relies on the Quartus Prime software's specific library. Before running the BTS, open the Quartus Prime software to automatically set the environment variable `QUARTUS_ROOTDIR`. You can also change it through **Environment Variables** in **System Properties** in Windows\*. The BTS uses this environment variable to locate the Quartus Prime library.

#### 4.1.5. Running the BTS GUI











With the power to the board off, follow these steps:

1. Connect the USB cable to your PC and the board.
2. Check that the development board switches and jumpers are set according to your preferences. Refer to the *Development Kit Setup* section. In most cases, BTS requires system MAX 10 and Agilex 7 FPGA on the JTAG chain while Clock Controller and Power Monitor require only the system MAX 10.
3. Check the external modules status: QSFPPD800/QSFPPD/FMC+/DIMM.
4. Turn on the board power switch.

**Note:** To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The BTS cannot run correctly unless the USB cable is attached, and the board is on.

To run the BTS, navigate to the `<package_dir>\examples\board_test_system` directory. The BTS release folder always includes the following files:

**Figure 4. BTS Folder**

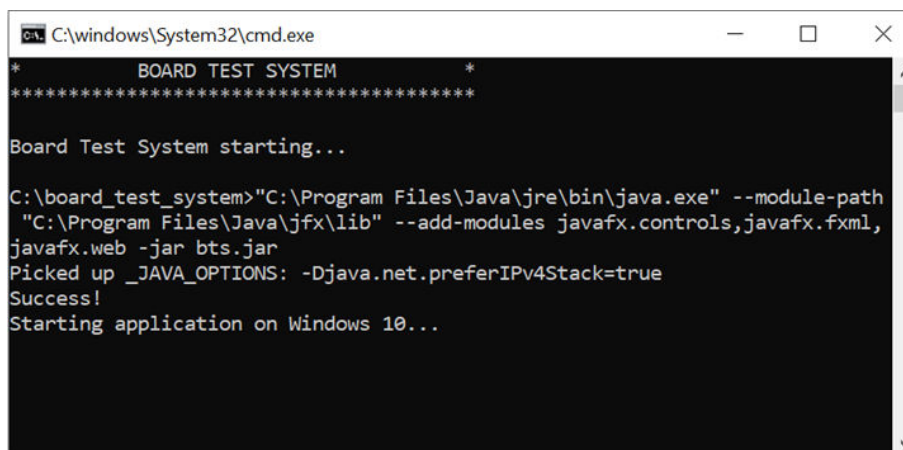
<input type="checkbox"/> Name	Type
 image	File folder
 lib	File folder
 BoardTestSystem.bat	Windows Batch File
 BoardTestSystem.sh	Shell Script
 bts.jar	JAR File
 ClockController.bat	Windows Batch File
 ClockController.sh	Shell Script
 PowerMonitor.bat	Windows Batch File
 PowerMonitor.sh	Shell Script
 README.TXT	TXT File



You can run BTS GUI with the following scripts:

1. On the **Windows** system, double-click the .bat files to run BTS, Clock Controller, or Power Monitor GUI.

**Figure 5. Windows Console**



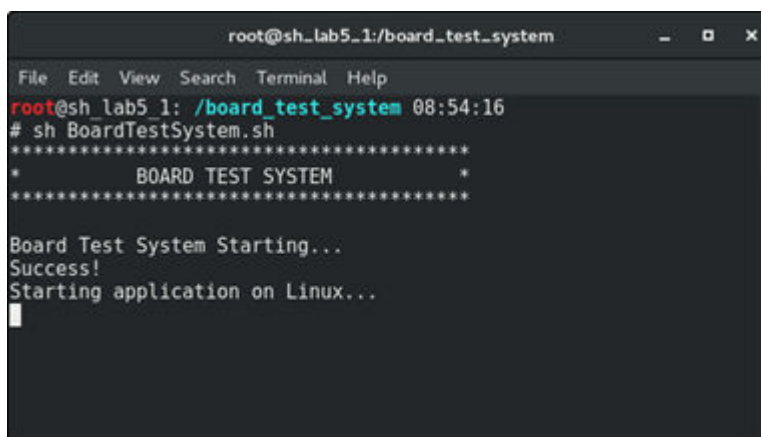
```
C:\windows\System32\cmd.exe
*      BOARD TEST SYSTEM      *
*****

Board Test System starting...

C:\board_test_system>"C:\Program Files\Java\jre\bin\java.exe" --module-path
"C:\Program Files\Java\jfx\lib" --add-modules javafx.controls,javafx.fxml,
javafx.web -jar bts.jar
Picked up _JAVA_OPTIONS: -Djava.net.preferIPv4Stack=true
Success!
Starting application on Windows 10...
```

2. On the **Linux** system, run the shell script with root privilege.

**Figure 6. Linux Console**



```
root@sh_lab5_1:/board_test_system
File Edit View Search Terminal Help
root@sh_lab5_1: /board_test_system 08:54:16
# sh BoardTestSystem.sh
*****
*      BOARD TEST SYSTEM      *
*****

Board Test System Starting...
Success!
Starting application on Linux...
```

*Note:* The .bat or shell script checks the Java environment settings, copies necessary files, and prompts if the environment is not set up correctly.

The GUI displays the application tab corresponding to the design running in the FPGA. If the design loaded in the FPGA is not supported by the BTS GUI, a message prompting you to configure your board with a valid BTS design appears. Refer to [The Configure Menu](#) on page 18.

#### Related Information

[Development Kit Setup](#) on page 11

## 4.2. Testing the Functionality of the Development Kit

This section describes each control in the BTS.

### 4.2.1. The Bottom Information Bar

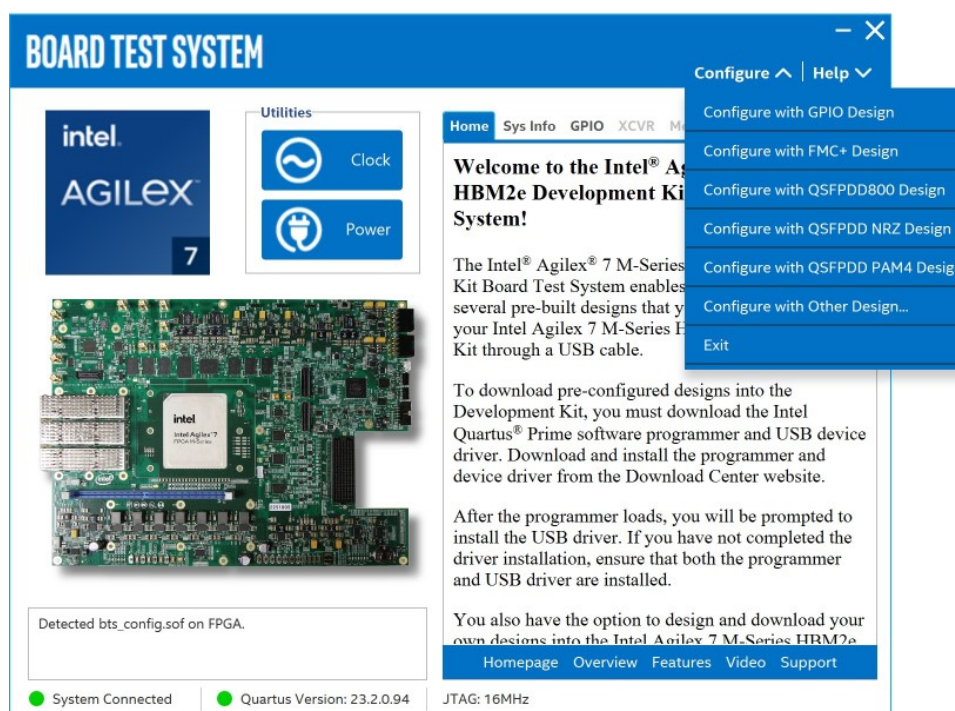
The bottom information bar shows the status of the system connection, Quartus Prime version, and the JTAG clock.

- **System Connected/Disconnected:** Shows if the board is connected to the system. The green sign turns gray if the board becomes disconnected.
- **Intel Quartus Prime Version:** Displays the current Quartus Prime version installed and active on your system. The text turns red if your version is older than the required version. Change the environment variable `QUARTUS_ROOTDIR` if you have installed the right version, but the active version does not meet the requirement.
- **JTAG:** Displays the JTAG clock frequency.

### 4.2.2. The Configure Menu

Use the **Configure** menu to select the design you want to use. Each design example tests different functionality that corresponds to different application tab.

Figure 7. The Configure Menu



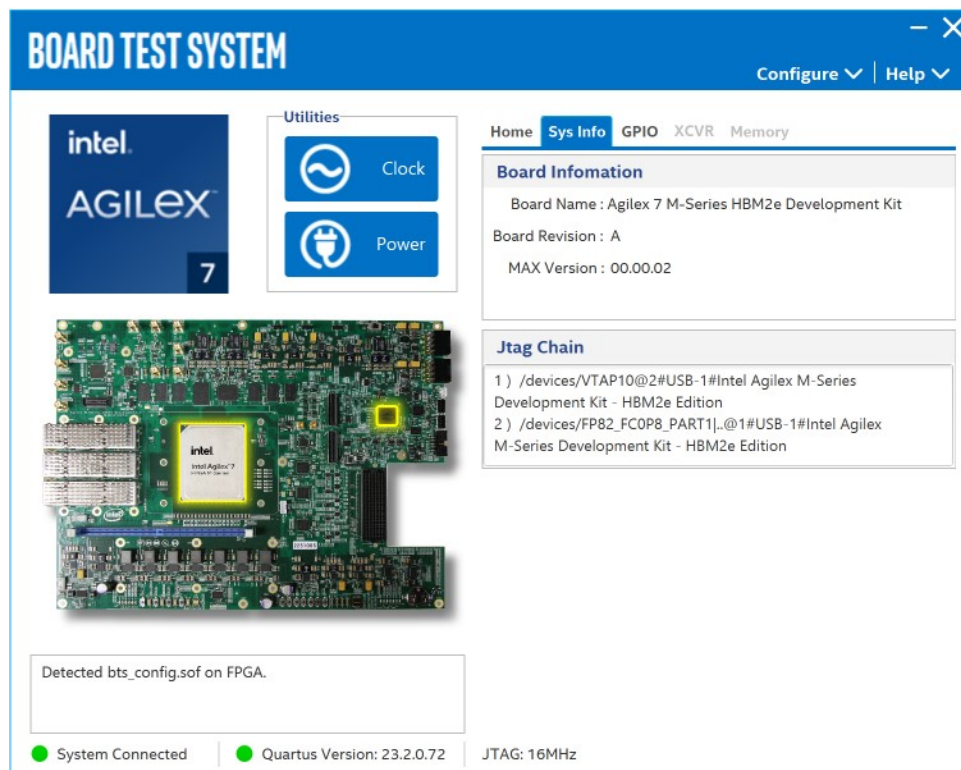
Follow these steps to configure the FPGA with a test system design:

1. On the **Configure** menu, click the **Configure** command that corresponds to the functionality you wish to test.
2. Click **Configure** in the dialog box that appears to download the corresponding design's SRAM Object File (.sof) to the FPGA. The download process usually takes less than a minute.
3. The design begins running in the FPGA after completion of the configuration. The corresponding GUI application tabs that interface with the design are now enabled. If you use the Quartus Prime Programmer for configuration, instead of the BTS GUI, you might need to restart the GUI.

### 4.2.3. The Sys Info Tab

The **Sys Info** tab shows information about the board's current configuration. The tab displays the board information, JTAG Chain devices, and other details stored on the board.

**Figure 8.** The Sys Info Tab



The following sections describe the controls on the **Sys Info** tab:

### Board Information

The board information control displays static information about your board.

- **Board Name:** Indicates the official name of the board given by the BTS.
- **Board Revision:** Indicates the revision of the board.
- **MAX Version:** Indicates the version of the System Intel MAX 10.

### JTAG Chain

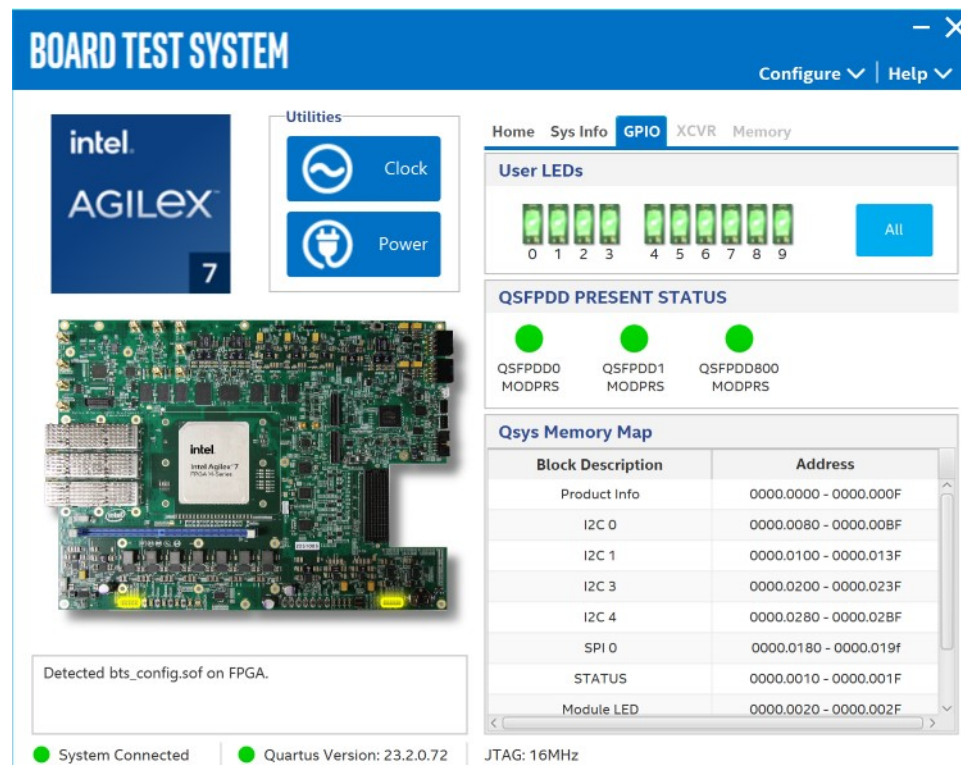
The JTAG chain control shows all the devices currently in the JTAG chain.

*Note:* Both of the systems, MAX 10 and the FPGA must be both in the JTAG chain when you are running the BTS GUI.

## 4.2.4. The GPIO Tab

The **GPIO** tab allows you to interact with the general-purpose user I/O components on your board. You can turn LEDs on or off and see the present status of the QSFPPD modules.

**Figure 9. The GPIO Tab**



The following sections describes the controls on the **GPIO** tab:

### User LEDs

The **User LEDs** control displays the current state of the user LEDs. Toggle the LED buttons to turn the board LEDs on and off. Click the **All** button to reverse the state of all the LEDs.

### QSFPDD PRESENT STATUS

The **QSFPDD PRESENT STATUS** control displays the present state of the QSFPDD modules.

### Qsys Memory Map

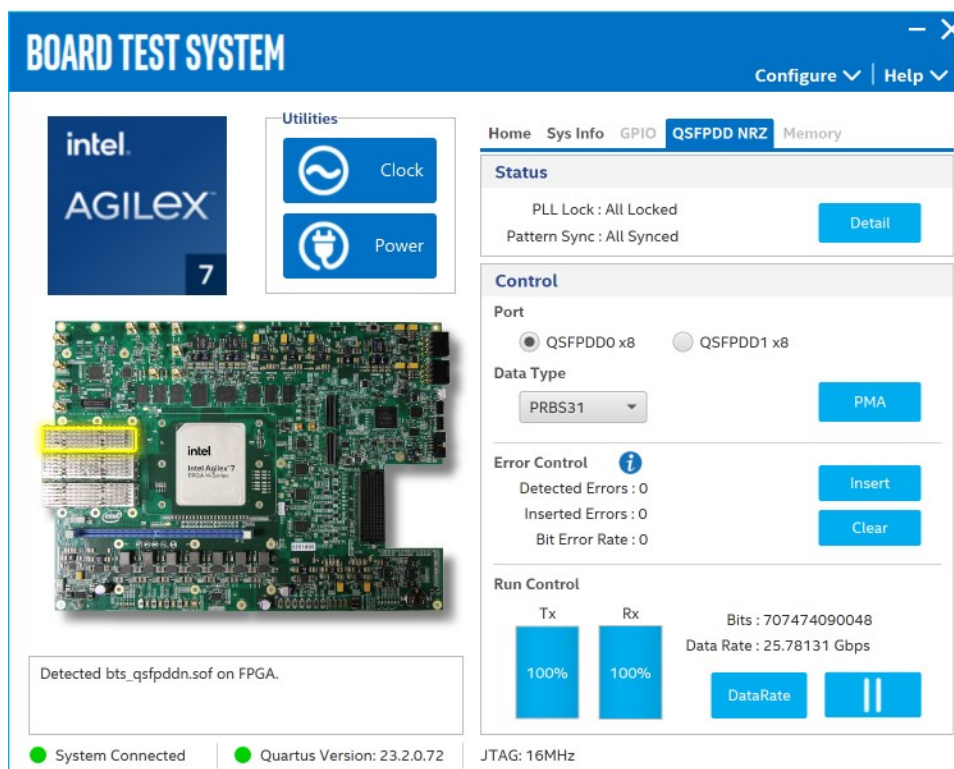
The **Qsys Memory Map** control shows the memory map of `bts_config.sof` design running on your board.

## 4.2.5. The XCVR Tab

The **XCVR** tab allows you to run transceiver tests on your board. You can run the test using either electrical loopback modules or optical fiber modules.

### 4.2.5.1. The QSFPDD NRZ Tab

Figure 10. The QSFPDD NRZ Tab



The following sections describe controls in the **QSFPDD NRZ** tab:

### Status

The **Status** control displays the following status information during the loopback test:

- **PLL Lock:** Shows the PLL locked or unlocked state.
- **Pattern Sync:** Shows the pattern synced or not state. The pattern is considered synced when the start of the data sequence is detected.
- **Detail:** Shows the PLL lock and pattern sync status. The number of the error bits of each channel can be found here.

**Figure 11. QSFPDD NRZ — PLL and Pattern Status**

PLL and Pattern Status				
Channel	PLL Lock Status	Pattern Sync Status	Errors	Error Rate
0	Locked	Synced	0	0
1	Locked	Synced	0	0
2	Locked	Synced	0	0
3	Locked	Synced	0	0
4	Locked	Synced	0	0
5	Locked	Synced	0	0
6	Locked	Synced	0	0
7	Locked	Synced	0	0

### Control

Use the following controls to select an interface to apply PMA settings, data type, and error control:

- **QSFPDD0x8**
- **QSFPDD1x8**



### PMA Setting

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback:** Displays the signal status between the transmitter and the receiver.
- **VOD:** Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap:**
  - Pre-tap 1: Specifies the amount of pre-emphasis on the first pre-tap of the transmitter buffer.
  - Pre-tap 2: Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
  - Post-tap 1: Specifies the amount of pre-emphasis on the post-tap of the transmitter buffer.

Figure 12. QSPD NRZ — PMA Setting

PMA SETTING
— ✕

		Serial Loopback	VOD	Pre-emphasis tap		
				Pre-tap 1	Pre-tap 2	Post-tap 1
<input type="checkbox"/>	All CH	<input type="checkbox"/>	19 ▾	11 ▾	0 ▾	0 ▾
<hr/>						
CH0	<input type="checkbox"/>	19 ▾	11 ▾	0 ▾	0 ▾	0 ▾
CH1	<input type="checkbox"/>	19 ▾	11 ▾	0 ▾	0 ▾	0 ▾
CH2	<input type="checkbox"/>	19 ▾	11 ▾	0 ▾	0 ▾	0 ▾
CH3	<input type="checkbox"/>	19 ▾	11 ▾	0 ▾	0 ▾	0 ▾
CH4	<input type="checkbox"/>	19 ▾	11 ▾	0 ▾	0 ▾	0 ▾
CH5	<input type="checkbox"/>	19 ▾	11 ▾	0 ▾	0 ▾	0 ▾
CH6	<input type="checkbox"/>	19 ▾	11 ▾	0 ▾	0 ▾	0 ▾
CH7	<input type="checkbox"/>	19 ▾	11 ▾	0 ▾	0 ▾	0 ▾

OK
Cancel
Apply

## Data Type

The **Data Type** control specifies the type of data pattern contained in the transactions. Select the following available data types for analysis:

- **PRBS7**: Pseudo-random 7-bit binary sequences.
- **PRBS15**: Pseudo-random 15-bit binary sequences.
- **PRBS23**: Pseudo-random 23-bit binary sequences.
- **PRBS31**: Pseudo-random 31-bit binary sequences (default).

## Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors**: Displays the number of data errors detected in the received bitstream.
- **Inserted Errors**: Displays the number of errors inserted into the transmit data stream.
- **Bit Error Rate**: Calculates the bit error rate of the transmit data stream.
- **Inserts**: Inserts a one-word error into the transmit data stream each time you click the button. Insert error is only enabled during transaction performance analysis.
- **Clear**: Resets the **Detected Errors** counter and **Inserted Errors** counter to zero.

## Run Control

- **TX and RX performance bars**: Show the percentage of the maximum theoretical data rate that the requested transactions are able to achieve.
- **Start**: Initiates the loopback tests.
- **Data Rate**: Displays the XCVR type and data rate of each channel.

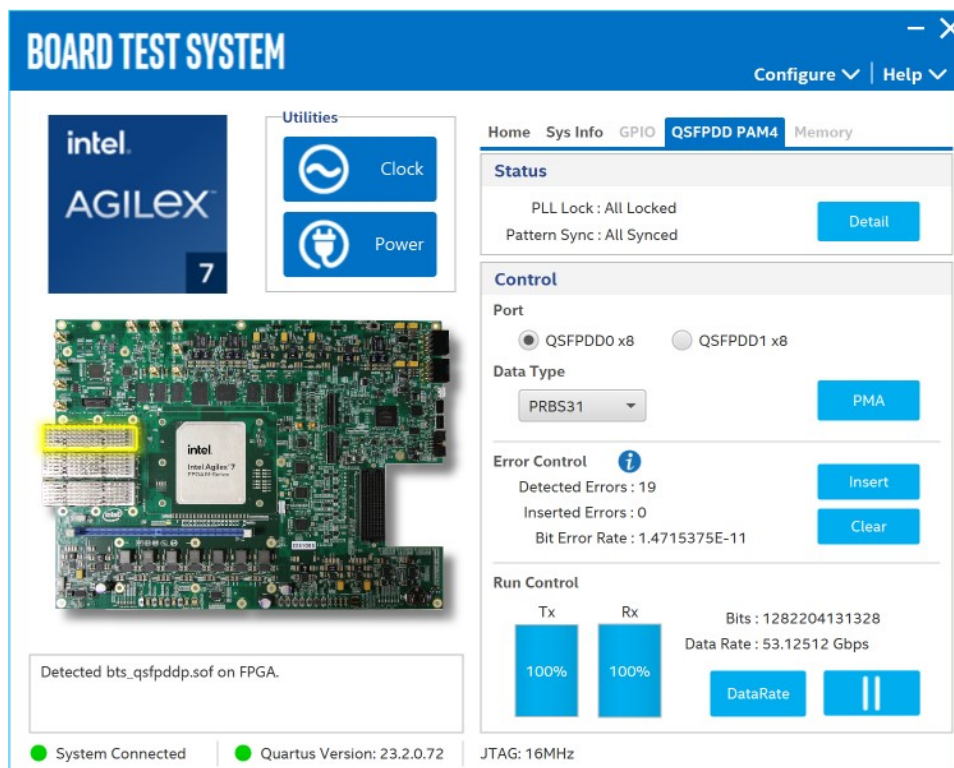
**Figure 13. QSFPDD NRZ — Data Rate**

Data Rate		
Channel	XCVR Type	Frequency
0	F-Tile FGT	25.78131 Gbps
1	F-Tile FGT	25.78131 Gbps
2	F-Tile FGT	25.78131 Gbps
3	F-Tile FGT	25.78131 Gbps
4	F-Tile FGT	25.78131 Gbps
5	F-Tile FGT	25.78131 Gbps
6	F-Tile FGT	25.78131 Gbps
7	F-Tile FGT	25.78131 Gbps



#### 4.2.5.2. The QSPD PAM4 Tab

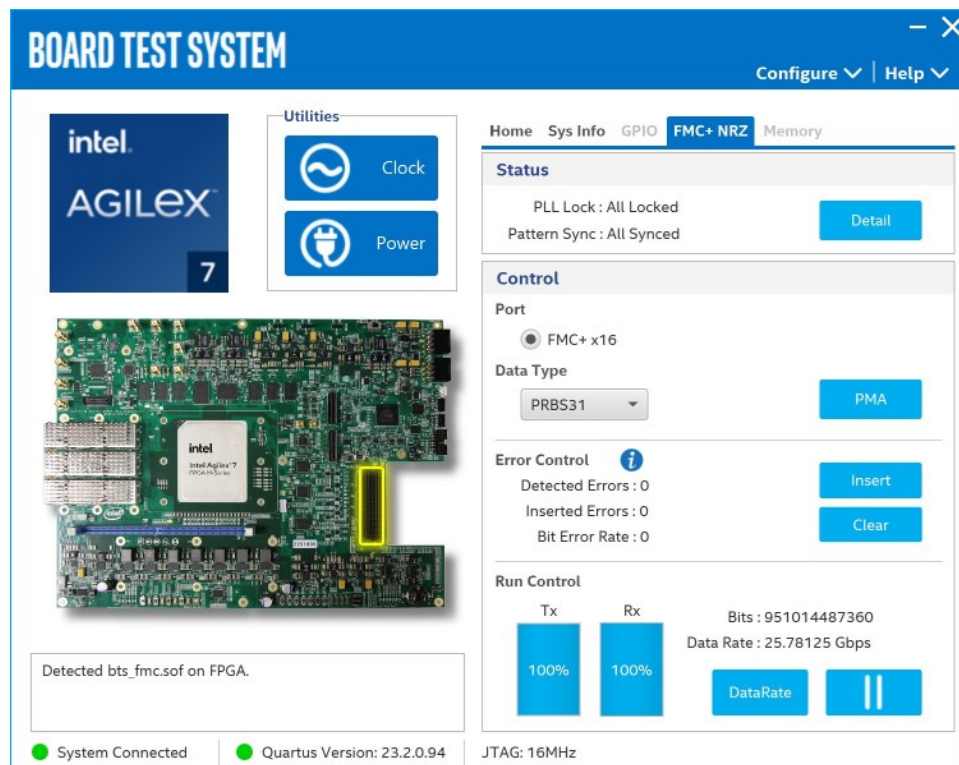
Figure 14. The QSPD PAM4 Tab



*Note:* This tab has similar control functions as the **QSPD NRZ** tab.

### 4.2.5.3. The FMC+ NRZ Tab

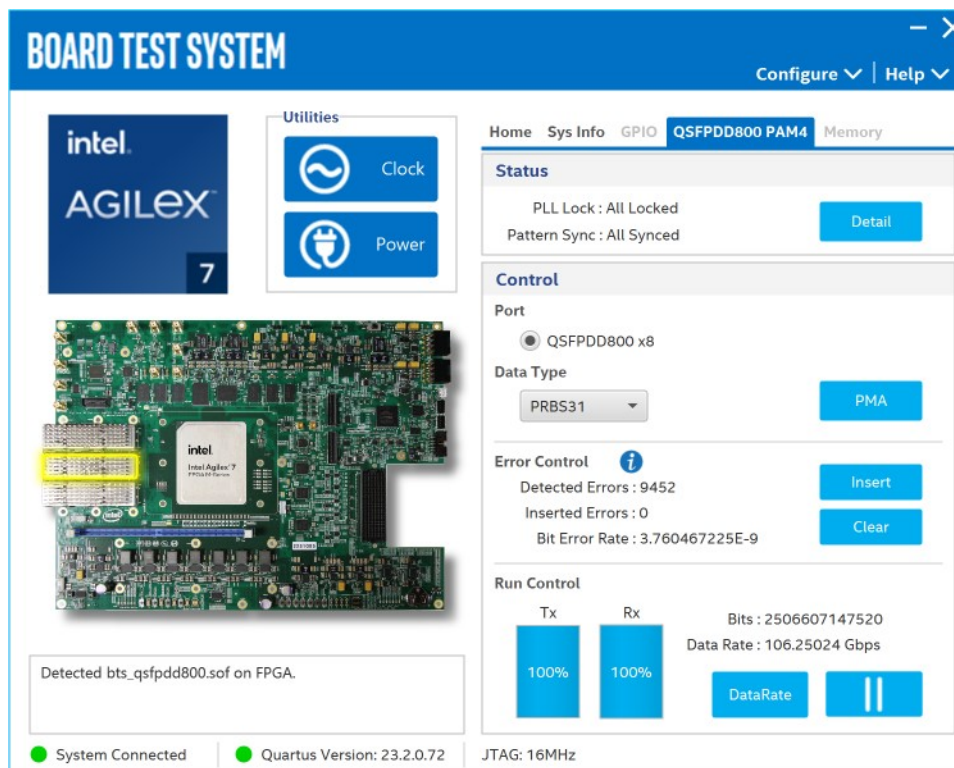
**Figure 15. The FMC+ Tab**



**Note:** This tab has similar control functions as the **QSPDD NRZ** tab.

#### 4.2.5.4. The QSPDD800 PAM4 Tab

Figure 16. The QSPDD800 PAM4 Tab



**Note:** This tab has similar control functions as the **QSPDD NRZ** tab.

#### PMA Setting

In addition to the PMA settings listed in [QSPDD NRZ — PMA Setting](#) figure, additional settings are available for the F-Tile FHT PMA. The PMA is set to the default values in the PAM4 designs.

- **Pre-emphasis tap:**
  - Post-tap 2: Specifies the amount of pre-emphasis on the second post-tap of the transmitter buffer.
  - Post-tap 3: Specifies the amount of pre-emphasis on the third post-tap of the transmitter buffer.
  - Post-tap 4: Specifies the amount of pre-emphasis on the fourth post-tap of the transmitter buffer.
  - Pre-tap 3: Specifies the amount of pre-emphasis on the third pre-tap of the transmitter buffer.

**Figure 17. QSPFDD800PAM4 Tab — PMA Setting**

Serial Loopback		VOD	Pre-emphasis tap						
			Pre-tap 1	Pre-tap 2	Post-tap 1	Post-tap 2	Post-tap 3	Post-tap 4	Pre-tap 3
<input checked="" type="checkbox"/>	All CH	22	-4	0	-2	-2	0	0	0
<input type="checkbox"/>	CH0	22	-4	0	-2	-2	0	0	0
<input type="checkbox"/>	CH1	22	-4	0	-2	-2	0	0	0
<input type="checkbox"/>	CH2	22	-4	0	-2	-2	0	0	0
<input type="checkbox"/>	CH3	22	-4	0	-2	-2	0	0	0
<input type="checkbox"/>	CH4	22	-4	0	-2	-2	0	0	0
<input type="checkbox"/>	CH5	22	-4	0	-2	-2	0	0	0
<input type="checkbox"/>	CH6	22	-4	0	-2	-2	0	0	0
<input type="checkbox"/>	CH7	22	-4	0	-2	-2	0	0	0

OK Cancel Apply

#### Related Information

The QSPFDD NRZ Tab on page 21

### 4.3. Controlling the On-board Clock through Clock Controller GUI

The Clock Controller GUI can control the outputs of on-board Si5391-1/Si5391-2/Si5392/ Si5395/Si5332/Si5518. The instructions to run Clock Controller GUI are stated in the [Running the BTS GUI](#) on page 16. You can also start it using the BTS GUI icon **Clock**.

The Clock Controller communicates with the System MAX 10 device through 10-pin JTAG header, **J7** or USB port, **J1**. Then, the System MAX 10 controls the programmable clock part through a 2-wire I<sup>2</sup>C bus.

**Note:** You cannot run the stand-alone Clock Controller GUI application when the BTS or Power Monitor GUI is running at the same time.

**Note:** Si5518 can be controlled only when a design in which the SPI interface is instantiated, such as the `bts_config.sof` under the `board_test_system\image\ES` folder that has been downloaded to the FPGA.

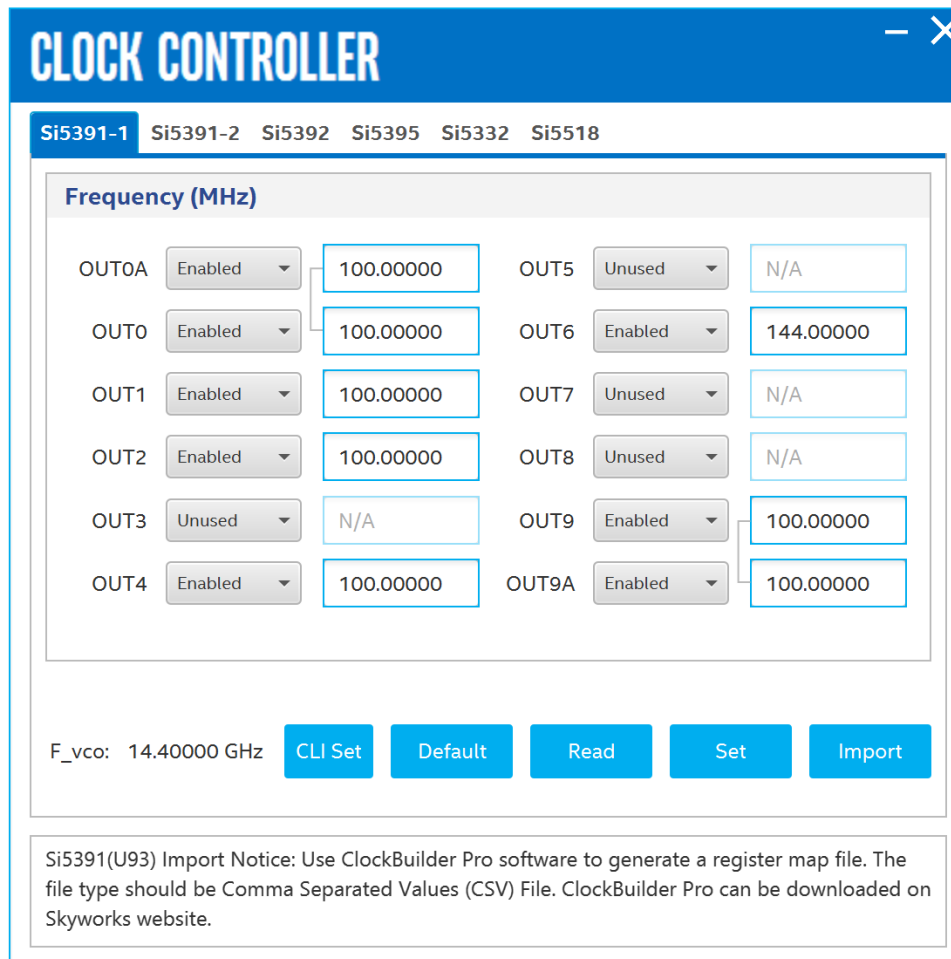
#### Related Information

[Skyworks Solution](#)

More information about the Clockbuilder Pro software.

### 4.3.1. Si5391-1

Figure 18. Si5391-1



**CLOCK CONTROLLER**

Si5391-1 Si5391-2 Si5392 Si5395 Si5332 Si5518

**Frequency (MHz)**

OUT0A	Enabled	100.00000	OUT5	Unused	N/A
OUT0	Enabled	100.00000	OUT6	Enabled	144.00000
OUT1	Enabled	100.00000	OUT7	Unused	N/A
OUT2	Enabled	100.00000	OUT8	Unused	N/A
OUT3	Unused	N/A	OUT9	Enabled	100.00000
OUT4	Enabled	100.00000	OUT9A	Enabled	100.00000

F\_vco: 14.40000 GHz CLI Set Default Read Set Import

Si5391(U93) Import Notice: Use ClockBuilder Pro software to generate a register map file. The file type should be Comma Separated Values (CSV) File. ClockBuilder Pro can be downloaded on Skyworks website.

The following sections describe the **Clock Controller** buttons.

#### Read

Reads the current frequency setting for the oscillator associated with the active tab.

#### Default

Sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.

#### Set

Sets the programmable oscillator frequency for the selected clock to the value in the OUTx output controls for Si5391. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Intel recommends resetting the FPGA logic after changing frequencies.

## Import

You can generate the register list from the *Clockbuilder Pro Software* tool and import it into Si5391 to update the settings of the output clocks. Register changes are volatile after power cycling.

### 4.3.2. Si5391-2

**Figure 19. Si5391-2**

The screenshot shows the 'CLOCK CONTROLLER' window for the Si5391-2 device. The interface includes a tabbed menu at the top with options: Si5391-1, **Si5391-2**, Si5392, Si5395, Si5332, and Si5518. The main section is titled 'Frequency (MHz)' and contains a table of output settings. Each output (OUT0A through OUT9A) has a status dropdown (Enabled or Unused) and a frequency input field. OUT0A through OUT4 are set to 100.00000 MHz and are Enabled. OUT5 is Unused (N/A). OUT6 is 144.00000 MHz and Enabled. OUT7 is 100.00000 MHz and Enabled. OUT8 is 125.00000 MHz and Enabled. OUT9 is 50.00000 MHz and Enabled. OUT9A is Unused (N/A). Below the table, the VCO frequency is set to 14.00000 GHz. At the bottom, there are buttons for 'CLI Set', 'Default', 'Read', 'Set', and 'Import'. A notice at the bottom states: 'Si5391(U35) Import Notice: Use ClockBuilder Pro software to generate a register map file. The file type should be Comma Separated Values (CSV) File. ClockBuilder Pro can be downloaded on Skyworks website.'

Output	Status	Frequency (MHz)
OUT0A	Enabled	100.00000
OUT0	Enabled	100.00000
OUT1	Enabled	100.00000
OUT2	Enabled	100.00000
OUT3	Enabled	100.00000
OUT4	Enabled	100.00000
OUT5	Unused	N/A
OUT6	Enabled	144.00000
OUT7	Enabled	100.00000
OUT8	Enabled	125.00000
OUT9	Enabled	50.00000
OUT9A	Unused	N/A

F\_vco: 14.00000 GHz

CLI Set Default Read Set Import

Si5391(U35) Import Notice: Use ClockBuilder Pro software to generate a register map file. The file type should be Comma Separated Values (CSV) File. ClockBuilder Pro can be downloaded on Skyworks website.

**Note:** This tab has similar control functions as the **Si5391-1** tab.

### 4.3.3. Si5392

Figure 20. Si5392

**CLOCK CONTROLLER**

Si5391-1 Si5391-2 **Si5392** Si5395 Si5332 Si5518

**Frequency (MHz)**

OUT0	Enabled	156.25000
OUT1	Unused	N/A

F\_vco: 13.75000 GHz

Default Read Set Import

Si5392 Import Notice: Use ClockBuilder Pro software to generate a register map file. The file type should be Comma Separated Values (CSV) File. ClockBuilder Pro can be downloaded on Skyworks website.

*Note:* This tab has similar control functions as the **Si5391-1** tab.

### 4.3.4. Si5395

**Figure 21. Si5395**

CLOCK CONTROLLER

Si5391-1

Si5391-2

Si5392

Si5395

Si5332

Si5518

Frequency (MHz)

OUT0A	Enabled	156.25000	OUT5	Enabled	156.25000
OUT0	Enabled	156.25000	OUT6	Enabled	156.25000
OUT1	Enabled	156.25000	OUT7	Enabled	156.25000
OUT2	Enabled	156.25000	OUT8	Enabled	96.00000
OUT3	Enabled	156.25000	OUT9	Enabled	96.00000
OUT4	Enabled	156.25000	OUT9A	Unused	N/A

F\_vco: 13.75000 GHz

Default

Read

Set

Import

Si5395 Import Notice: Use ClockBuilder Pro software to generate a register map file. The file type should be Comma Separated Values (CSV) File. ClockBuilder Pro can be downloaded on Skyworks website.

**Note:** This tab has similar control functions as the **Si5391-1** tab.



### 4.3.5. Si5332

Figure 22. Si5332

CLOCK CONTROLLER

Si5391-1

Si5391-2

Si5392

Si5395

Si5332

Si5518

Frequency (MHz)

OUT0	Enable	100.00000	OUT4	Enable	100.00000
OUT1	Enable	100.00000	OUT5	Disable	0.00000
OUT2	Enable	100.00000	OUT6	Enable	156.25000
OUT3	Enable	100.00000	OUT7	Enable	156.25000

F\_vco : 2500.000 MHz

Read

Set

Import

Si5332 Import Notice: Use ClockBuilder Pro software to generate a register map file. The file type should be Comma Separated Values (CSV) File. ClockBuilder Pro can be downloaded on Skyworks website.

**Note:** This tab has similar control functions as the **Si5391-1** tab. There is no default button for this clock but you can use **Import** or power cycle the board to get default clock frequencies.

### 4.3.6. Si5518

**Figure 23. Si5518**

CLOCK CONTROLLER

Si5391-1

Si5391-2

Si5392

Si5395

Si5332

Si5518

Frequency (MHz)

OUT0	Enabled	0.0000010	OUT9	Enabled	390.62500
OUT1	Enabled	312.50000	OUT10	Enabled	3.84000
OUT2	Enabled	156.25000	OUT11	Enabled	245.76000
OUT3	Enabled	0.0000010	OUT12	Enabled	245.76000
OUT4	Enabled	10.00000	OUT13	Enabled	245.76000
OUT5	Unused	--	OUT14	Enabled	245.76000
OUT6	Enabled	156.25000	OUT15	Enabled	245.76000
OUT7	Enabled	390.62500	OUT16	Enabled	390.62500
OUT8	Enabled	390.62500	OUT17	Enabled	390.62500

F\_vco: 11.05920 GHz

Default

Soft Reset

Import

Si5518 Import Notice: Use ClockBuilder Pro software to generate boot files and the design report. The boot file should be binary while the design report is text. ClockBuilder Pro can be downloaded on Skyworks website.

#### Import

You can generate the register list from the *Clockbuilder Pro Software* tool and import it into Si5518 to update the settings of RAM. Register changes are volatile after power cycling.

#### Default

Sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.

#### Soft Reset

Initiates a global soft reset. The global soft reset does not download the firmware and frequency plan from the NVM. Instead, it starts the firmware and frequency plan currently running on the device. The device behaves like it has been rebooted.

### Related Information

#### [Skyworks Solution](#)

More information about the Clockbuilder Pro software.

## 4.4. Monitoring On-Board Power Regulator through Power Monitor GUI

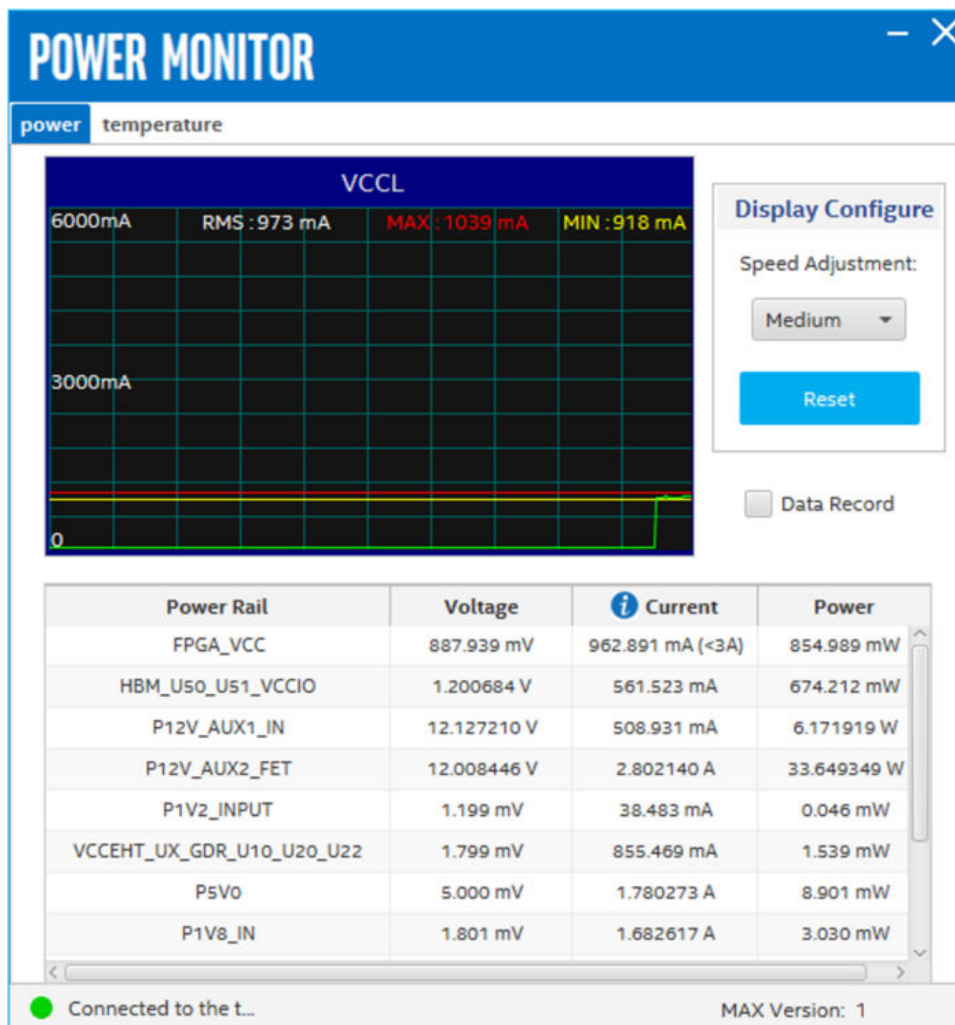
The Power Monitor GUI reports most power rails' voltage, current, and power information on the board. It also collects temperature from FPGA die, power modules, and diodes assembled on PCB.

The Power Monitor GUI communicates with System MAX 10 through a 10-pin JTAG header **J7** or USB port **J1**. System MAX 10 monitors and controls power regulator, temperature/voltage/current sensing chips through a 2-wire I<sup>2</sup>C bus.

The instructions to run Power Monitor GUI are stated in the *Running the BTS GUI* section. It can also be started with the BTS GUI icon **Power**.

**Note:** You cannot run the stand-alone Power Monitor GUI when the BTS or the Clock Controller GUI is running at the same time.

**Figure 24. Power Monitor GUI — The Power Tab**



The following sections describe the details of the Power Monitor GUI.

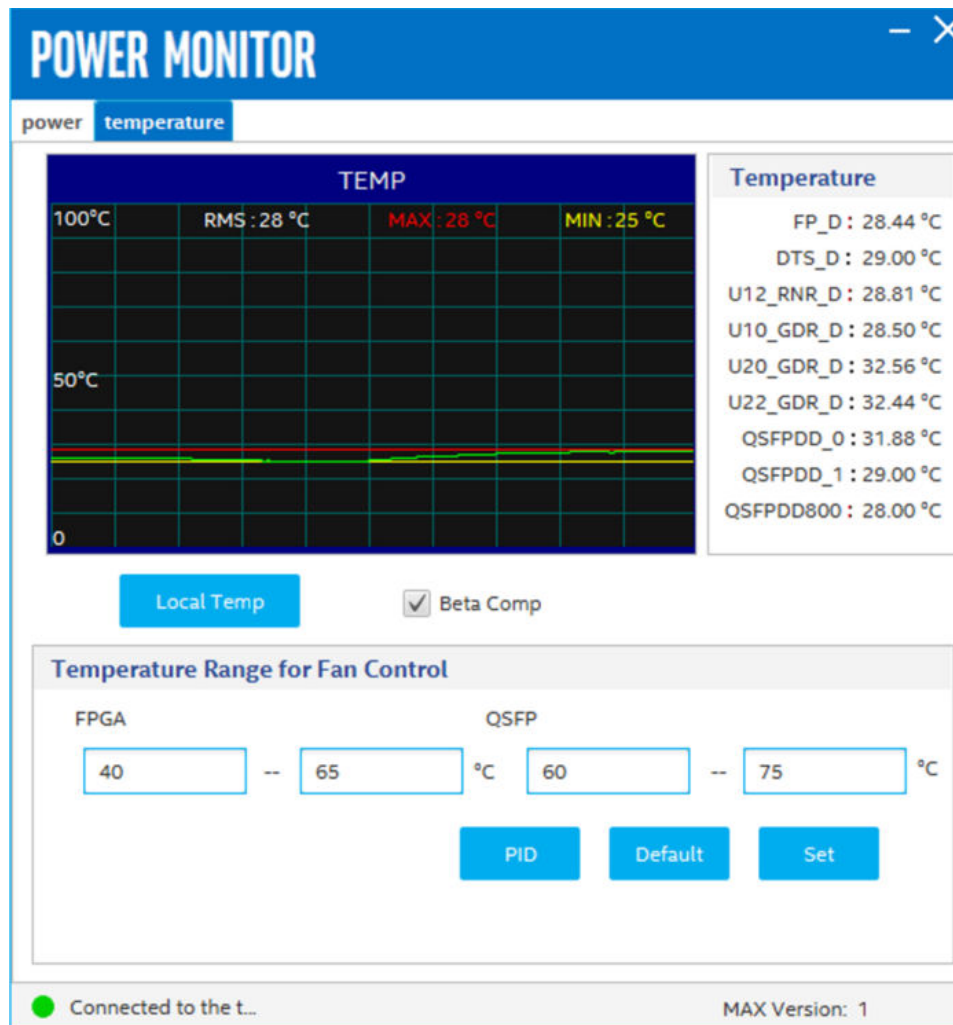
#### Display Configure

- **Speed Adjustment:** Adjusts the update rate of the current curve.
- **Reset:** Regenerates the graph.

#### Data Record

When the box is checked, the telemetry data of the selected power rail can be recorded. It saves the data into a .csv file in the log directory.

**Figure 25. Power Monitor GUI—The Temperature Tab**



### Temperature

Reads the temperature data from the FPGA die, diodes assembled on the PCB, and the QSFPDD modules.

### Local Temp

Shows the temperature comparison of the local and remote temperature sensors.

### Beta Comp

Enables Beta Compensation for the temperature sensing chips.

### Temperature Range for Fan Control

Sets and displays the temperature range for the fan control.

### **Related Information**

[Running the BTS GUI](#) on page 16

## **4.5. Identifying Test Pass or Fail-based on BTS GUI Test Status**

### **QSFPDD0/QSFPDD1**

Plug QSFPDD0/QSFPDD1 loopback module in **J16/J17** before you configure the QSFPDD NRZ/PAM4 example build through the BTS GUI.

### **QSFPDD800**

Plug QSFPDD800 loopback module in **J18** before you configure the QSFPDD800 PAM4 example build through the BTS GUI.

### **FMC+**

Plug FMC+ loopback module in **J34** before you configure the FMC+ NRZ example build through the BTS GUI.

### **DDR5 DIMM**

Plug the DIMM module, which is shipped alone with this development kit, in **J13**.

## 5. Development Kit Hardware and Configuration

The Agilex 7 FPGA M-Series HBM2e Development Kit can support multiple application scenarios and configuration modes. You need to change hardware setting for these cases.

**Table 5. Supported Configuration Modes**

S24 [1:4]	MSEL [2:0]	Configuration Mode
OFF/OFF/OFF/X	111	JTAG
ON/OFF/OFF/X	110	Avalon streaming interface x8 configuration mode

### 5.1. Configure FPGA and Access HPS Debug Access Port by JTAG

1. JTAG access does not rely on switch **S24** settings and system image.
2. Plug the USB cable to **J1** or Intel FPGA Download Cable to **J7 (set S26 on)**.
3. Open the Quartus Prime Programmer to configure the Agilex 7 FPGA
4. Open Arm Development Studio 5\* (DS-5\*) Intel SoC FPGA Edition to connect to and communicate with the HPS Debug Access Port (DAP) through the same JTAG interface.

### 5.2. Configure the FPGA Device Using the Avalon streaming interface x8 configuration Mode

1. Set S24 to Avalon streaming interface x8 configuration mode first.
2. Default MAX 10 image and hardware design supports the Avalon streaming interface x8 configuration mode only.
3. Power on the board, use push button S2 to choose page, and S1 to configure the FPGA.
4. Default page is 0.

### 5.3. Daughter Card

The Agilex 7 FPGA M-Series HBM2e Development Kit supports the HPS OOB daughter card. You can demonstrate HPS functions through these daughter card and cables.

### 5.3.1. HPS Out of Box Experience (OOBE) Daughter Card

1. Plug HPS OOBE daughter card in **J9**.
2. To test HPS Ethernet capability, connect OOBE's **RJ45** port **J3** to the Internet.
3. To test HPS USB 2.0 capability, connect OOBE's **J4** port to a USB cable.
4. To debug HPS from UART terminal applications, use a USB cable to connect to OOBE's **J7**.
5. OOBE's MicroSD card is pre-programmed with GSRD and OS.
6. General I/O access is provided by push buttons and LED indicators.



## 6. Custom Projects for the Development Kit

---

### 6.1. Add SmartVID Settings in the Quartus Prime QSF File

Agilex 7 silicon assembled on this development kit enables SmartVID feature by default. In order to avoid a Quartus Prime from generating an error due to incomplete SmartVID settings, you must put constraints outlined below into Quartus Prime project QSF file.

Open your Quartus Prime project QSF file, copy and paste the following constraint scripts into the file. Ensure there are no other similar settings with different values.

```
set_global_assignment -name PWRMGT_SLAVE_DEVICE_TYPE LTC3888
set_global_assignment -name PWRMGT_SLAVE_DEVICE0_ADDRESS 55
set_global_assignment -name PWRMGT_VOLTAGE_OUTPUT_FORMAT "LINEAR FORMAT"
set_global_assignment -name PWRMGT_LINEAR_FORMAT_N "-12"
set_global_assignment -name PWRMGT_PAGE_COMMAND_ENABLE ON
set_global_assignment -name PWRMGT_PAGE_COMMAND_PAYLOAD 0
set_global_assignment -name STRATIXV_CONFIGURATION_SCHEME "AVST X8"
set_global_assignment -name USE_PWRMGT_SCL SDM_IO0
set_global_assignment -name USE_PWRMGT_SDA SDM_IO16
set_global_assignment -name USE_CONF_DONE SDM_IO5
set_global_assignment -name USE_NCATTRIP SDM_IO7
set_global_assignment -name USE_HPS_COLD_RESET SDM_IO12
```

### 6.2. Golden Top

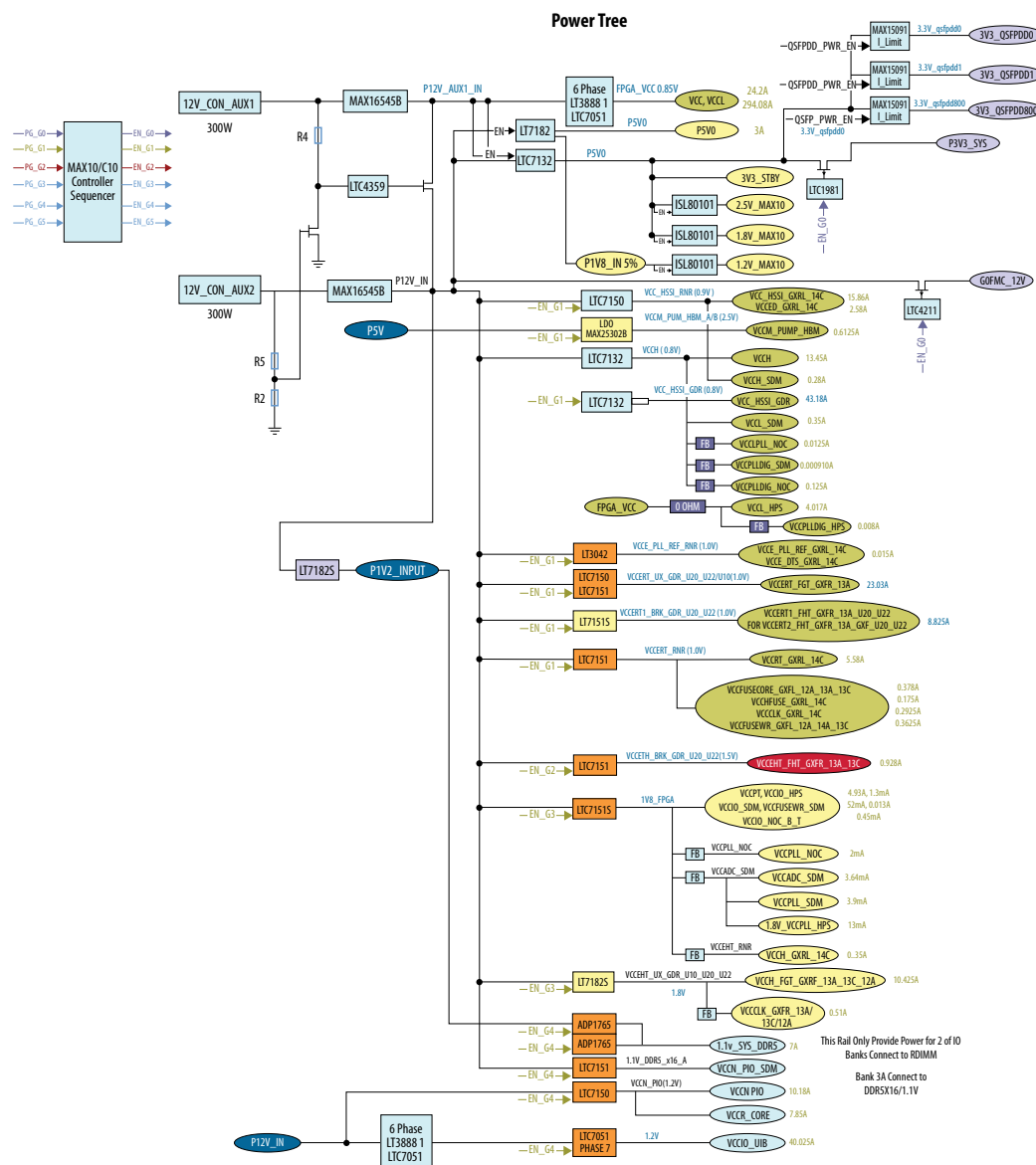
You can use the Golden Top project as the starting point for your designs. It comes loaded with constraints, pin locations, defined I/O standard, direction, and general termination.

## 7. Document Revision History for the Agilex 7 FPGA M-Series HBM2e Development Kit User Guide

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Document Version	Changes
2024.05.14	<ul style="list-style-type: none"><li>Retitled the document from <i>Agilex 7 M-Series HBM2e Development Kit User Guide</i> to <i>Agilex 7 FPGA M-Series HBM2e Development Kit User Guide</i>.</li><li>Removed mention of Agilex 9 from the document.</li><li>Removed information related to 256 MB QSPI flash daughter card in Appendix: <i>Daughter Cards</i>.</li><li>Updated document per latest branding standards.</li></ul>
2024.01.24	Updated Figure: <i>Agilex 7 FPGA M-Series HBM2e Development Kit Block Diagram</i> .
2023.11.03	Initial release.

### Figure 26. Power Tree



\*Other names and brands may be claimed as the property of others.

**ISO  
9001:2015  
Registered**

Onboard hot-plug circuit shuts down all power rails when the total power is over 360 W (30 A).

UB2/PWR MAX 10 shuts down significant power rails when one or more good power indicators is low due to a power fault.

UB2/PWR MAX 10 also shuts down significant power rails when temperature cross the acceptable range.

## A.2. Clocks

**Table 6. Default Clock Frequency**

Schematic Signal Name	Default Frequency (MHz)
SAMPLE_CLK_312_50MHZ_P/N	312.50
TOD_MASTER_156_25MHZ_P/N	156.25
1PPS_SI5518	100
SI5518_10MHZ_OUT	10
CLK_156_25MHZ_5391_P/N	156.25
CLK_390_625MHZ_1P/1N	390.625
CLK_390_625MHZ_2P/2N	390.625
CLK_390_625MHZ_3P/3N	390.625
CLK_3_84MHZ_SMA_P/N	3.84
CLK_245_76MHZ_SMA_P/N	245.76
CLK_245_76MHZ_1P/1N	245.76
CLK_245_76MHZ_2P/2N	245.76
CLK_245_76MHZ_3P/3N	245.76
CLK_245_76MHZ_4P/4N	245.76
CLK_390_625MHZ_4P/4N	390.625
CLK_390_625MHZ_5P/5N	390.625
CLK_156_25MHZ_U22_P/N	156.25
CLK_156_25MHZ_1_FMC_P/N	156.25
CLK_156_25MHZ_2_FMC_P/N	156.25
CLK_156_25MHZ_3_FMC_P/N	156.25
CLK_156_25MHZ_4_U22_P/N	156.25
CLK_156_25MHZ_5_U22_P/N	156.25
CLK_156_25MHZ_6_U20_P/N	156.25
CLK_156_25MHZ_7_U20_P/N	156.25
CLK_156_25MHZ_8_FMC_CON_P/N	156.25
CLK_156_25MHZ_SI5391_1_P/N	156.25
<i>continued...</i>	

Schematic Signal Name	Default Frequency (MHz)
CLK_156_25MHZ_SYNCE_DDR_P/N	156.25
CLK_156_25_MHZ_SI5392	156.25
CLK_UIB0_P/N	100
CLK_UIB0_FBR0_P/N	100
CLK_UIB0_FBR1_P/N	100
CLK_UIB1_P/N	100
FPGA_IO_CLK0_P/N	100
FPGA_IO_CLK5_P/N	100
CLK_UIB1_FBR0_P/N	100
CLK_UIB1_FBR1_P/N	100
CLK_100M_RP_0_P/N	100
CLK_100M_PCIE1_P/N	100
CLK_100M_PCIE0_P/N	100
CLK_100M_RP_1_P/N	100
CLK_100M_RP_2_P/N	100
CLK_SI5332_U10_IO_PLL_DP	100
CLK_SI5332_U20_IO_PLL_DP	100
CLK_SI5332_U22_IO_PLL_DP	100
CLK_DDR5_RDIMM_A0_DP/DN	100
CLK_DDR5_RDIMM_A1_DP/DN	100
CLK_DDR5_COM_DP/DN	100
CLK_DDR5_COM_HPS_DP/DN	100
CLK_LP5_B1_P/N	100
CLK_LP5_A1_P/N	100
FPGA_IO_CLK_2_P/N	100
CLK_NOC_PLL0	100
CLK_NOC_PLL1	100
FPGA_SDM_1V8_125M_CLK	125



Schematic Signal Name	Description
QFPDD_0_3V3_LED1/DS6	QSPDD PORT 0 LED1
QFPDD_1_3V3_LED0/DS11	QSPDD PORT 1 LED0
QFPDD_1_3V3_LED1/DS12	QSPDD PORT 1 LED1
QFPDD800_3V3_LED0/DS13	QSPDD800 LED0
QFPDD800_3V3_LED1/DS14	QSPDD800 LED1
MAX10_USER_LED0	Reserved
OVERTEMP_N/D10, D19	F-Tile die, R-Tile die, core die, board overtemp red LED is on
MAX_CONFIG_DONE/DS10	LED is on when MAX 10 configuration is done
S12	FPGA_RESETh
S13	HPS_COLD_RESETh
S9	PCIE_PERST_N
S15	USER RESETN
S2	MAX10 (USER_PB0)
S1	MAX10 (USER_PB1)
S21	CLK_SI5392_RST_R_N
S18	CLK_SI5391_2_RESET_N
S23	CLK_SI5391_RESET_N
SW7	Power recycle
QSPDD_I2C_3V3_EN_N	<ul style="list-style-type: none"> <li>0: MAX 10 access to QSPDD/QSPDD800 EEPROM</li> <li>1: Agilex 7 M-Series HBM2e access to QSPDD/QSPDD800 EEPROM</li> </ul>
MAX10_1V8__SI5391_1_RSTN	<ul style="list-style-type: none"> <li>0: SI5391 U14 RESETN mode</li> <li>1: Normal (default)</li> </ul>
HPS_RESETN	<ul style="list-style-type: none"> <li>0: HPS RESETN</li> <li>1: Normal (default)</li> </ul>
FMC_12v_EN	0: FMC_12V OFF 1: FMC_12V ON (DEFAULT)
SVID_I2C_EN	<ul style="list-style-type: none"> <li>Before power ok: 0</li> <li>After power ok: S_control_gui[1], =1 by default</li> </ul>
PWRGD_DDR5_MAX_RD	<ul style="list-style-type: none"> <li>Before power ok: 0</li> <li>After power ok: 1</li> </ul>
MAX10_SI5518_1V2_RSTN (control by FP8)	<ul style="list-style-type: none"> <li>Before power ok: 0</li> <li>After power ok: 1</li> </ul>
CLKMUX_OE_1V8_EN	Enable all the clocks on the development kit. It is always 0.
CLK_SI5392_RST_R_N	<ul style="list-style-type: none"> <li>Before power ok: 0</li> <li>After power ok: 1</li> </ul>
Clk_si5391_2_reset_n	<ul style="list-style-type: none"> <li>Before power ok: 0</li> <li>After power ok: 1</li> </ul>
<b>continued...</b>	

Schematic Signal Name	Description
usb_disablen	<ul style="list-style-type: none"> <li>0: external Intel FPGA Download Cable is inserted</li> <li>1: no external Intel FPGA Download Cable inserted</li> </ul>
Fx2_reseten	<ul style="list-style-type: none"> <li>0: On-board Intel FPGA Download Cable II is under reset</li> <li>1: 0: On-board Intel FPGA Download Cable II is out of reset</li> </ul>
BOARD_PWR_GOOD_LED/DS15	FPGA Power Good, Agilex 7 M-Series HBM2e power sequences are successful and all the power rails on board are good.
MAX_1V2_FPGA_SPARE[7:0]	Reserved GPIO between System MAX 10 and Agilex 7 M-Series HBM2e. All 8 signals have option pull up and pull down, all can be GPIO signals, I2C, SPI bus between MAX 10 and Agilex 7 M-Series HBM2e, or any status, alert, etc signals between MAX 10 and Agilex 7 M-Series HBM2e. By default all 8 signals have pull up 4.7K.

## A.4. Memory Interfaces

### FPGA Dedicated External Memory Interface (DDR5 RDIMM)

Agilex 7 M-Series HBM2e Development Kit supports 16 GB DDR5 RDIMM MTC10F1084S1RC56BG1. It is single slot. It targets up to 5600 Mbps.

### FPGA Dedicated External Memory Interface (DDR5 Component)

DDR5 component interface is a 40 bit, including 8-bit ECC support, single rank configuration based on x16 component. It targets up to 5600 Mbps. It targets up to 5600 Mbps. Three MT60B1G16HC-56B:G from Micron are soldered down on the development kit.

### FPGA and HPS Shared External Memory Interface (LPDDR5 Component)

LPDDR5 component interface is a 16 bit, two channels configuration. It targets up to 5600 Mbps. MT62F512M32D2DS-031 AUT:B from Micron is soldered down on the development kit.

### FPGA and HPS Shared External Memory Interface (DDR5 Component)

DDR5 component interface is a 40 bit, including 8-bit ECC support, single rank configuration based on x16 component. It targets up to 5600 Mbps. Three MT60B1G16HC-56B:G from Micron are soldered down on the development kit. Both Agilex 7 FPGA fabric and HPS can access this external memory interface. However, they cannot be accessed at the same time.

## A.5. Communication Interfaces

### MCIO Port

The MCIO slot is a PCIe Gen4 x4 port which fans out from Agilex 7 FPGA M-Series F-Tile. This port is designed to meet the standard MCIO pinout. PCIE1\_PERST0\_N signal can act as output and input respectively.



**Table 9. MCIO Port**

Schematic Signal Name	Description
PCIE_PERSTn_A	PCIe endpoint/root port reset
PCIE_ALERTn_A	PCIe Alert
PCIE_100M_REF_AP/AN	PCIe reference clock
PCIE_SCL_A/SDA_A	PCIe I <sup>2</sup> C bus
PCIE_TX_P/N[15:0]	Transceiver TX
PCIE_RX_P/N[15:0]	Transceiver RX

**2x MCIO x8 Connector**

The recommended MCIO cable to use with MCIO connector (Uxx) is not included as part of the development kit and must be acquired directly from third party supplier (Amphenol p/n = HMC74-0631).

**QSFPDD**

The Agilex 7 M-Series Development Kit supports 2x QSFPDD ports. The QSFPDD port fans out from Agilex 7 FPGA M-Series F-Tile (FGT). All 8 channels per QSFPDD can run up to 32G NRZ and 58G PAM4.

**QSFPDD800**

The Agilex 7 M-Series Development Kit supports 1X QSFPDD800 port. The QSFPDD800 port fans out from Agilex 7 FPGA M-Series F-Tile (FHT). All 8 channels per QSFPDD800 can run up to 32G NRZ, 58G PAM4, and 116G.

**Table 10. QSFPDD Connector 0 (J16)**

Schematic Signal Name	Description
QSFPDD0_3V3_MODPRS_L	Module present
QSFPDD0_3V3_RESET_L	Module reset
QSFPDD0_3V3_MODSEL_L	Mode select
QSFPDD0_3V3_LPMODE	Initial mode
QSFPDD0_3V3_INT_L	Interrupt
I2C_QSFPDD0_3V3_SCL	I <sup>2</sup> C clock
I2C_QSFPDD0_3V3_SDA	I <sup>2</sup> C data
QSFPDD0_TX_P/N[0:7]	Transceiver TX
QSFPDD0_RX_P/N[0:7]	Transceiver RX

**Table 11. QSFPDD Connector 1 (J17)**

Schematic Signal Name	Description
QSFPDD1_3V3_MODPRS_L	Module present
QSFPDD1_3V3_RESET_L	Module reset
<i>continued...</i>	

Schematic Signal Name	Description
QSFPDD1_3V3_MODSEL_L	Mode select
QSFPDD1_3V3_LPMODE	Initial mode
QSFPDD1_3V3_INT_L	Interrupt
I2C_QSFPDD1_3V3_SCL	I <sup>2</sup> C clock
I2C_QSFPDD1_3V3_SDA	I <sup>2</sup> C data
QSFPDD1_TX_P/N[0:7]	Transceiver TX
QSFPDD1_RX_P/N[0:7]	Transceiver RX

**Table 12. QSFPDD800 (J18)**

Schematic Signal Name	Description
QSFPDD800_3V3_MODPRS_L	Module present
QSFPDD800_3V3_RESET_L	Module reset
QSFPDD800_3V3_MODSEL_L	Mode select
QSFPDD800_3V3_LPMODE	Initial mode
QSFPDD800_3V3_INT_L	Interrupt
I2C_QSFPDD800_3V3_SCL	I <sup>2</sup> C clock
I2C_QSFPDD800_3V3_SDA	I <sup>2</sup> C data
QSFPDD800_TX_P/N[0:3]	Transceiver TX
QSFPDD800_RX_P/N[0:3]	Transceiver RX

### FMC+ Connector

The Agilex 7 M-Series Development Kit supports FMC+ slots for functional expandability. The x16 FGT lanes from bank 12A are terminated to the FMC+ (J34) connector and the 64 I/O signals from bank 2A connect to the FMC+ (J34) connector. Auxiliary signals are controlled by the system MAX 10.

### USB Type-C Connector

The Agilex 7 M-Series Development Kit has hardware support for the USB Type-C connector, which supports DP1.4 specification or USB 3.1 functionality through MUX (TUSB1146). This feature is yet to be validated and implemented.

### Serial Buses

The SDM I/Os (SDM\_IO16/0) and MAX 10 I/Os (VCCL\_SDA/SCL) share the same I<sup>2</sup>C bus which communicate with Agilex 7 FPGA core regulators. By default, SDM acts as SmartVID master and system MAX 10 act as Power GUI master in this chain.

The system MAX 10 I/Os (PMB\_SDA/SCL) manages the second I<sup>2</sup>C bus which access all I<sup>2</sup>C slave regulator except Agilex 7 FPGA core regulators.

The system MAX 10 supports I<sup>2</sup>C master dedicated to clock-related devices (CLK\_I2C\_SDA/SCL), which manages 3# clock devices and also connected to the HPS I/Os (HPS\_GPIO30/31) through level translator.

Another I<sup>2</sup>C master instance from the system MAX 10 (VCXO\_I2C\_SDA/SCL) controls the on board VCXO and Si5394 clock generator.

The Agilex 7 FPGA also manages QSFPDD800, 2x QSFPDD, 1 RDIMM DDR5 I<sup>2</sup>C buses, SDI transceivers, and ZL30733 clock synthesizer device.

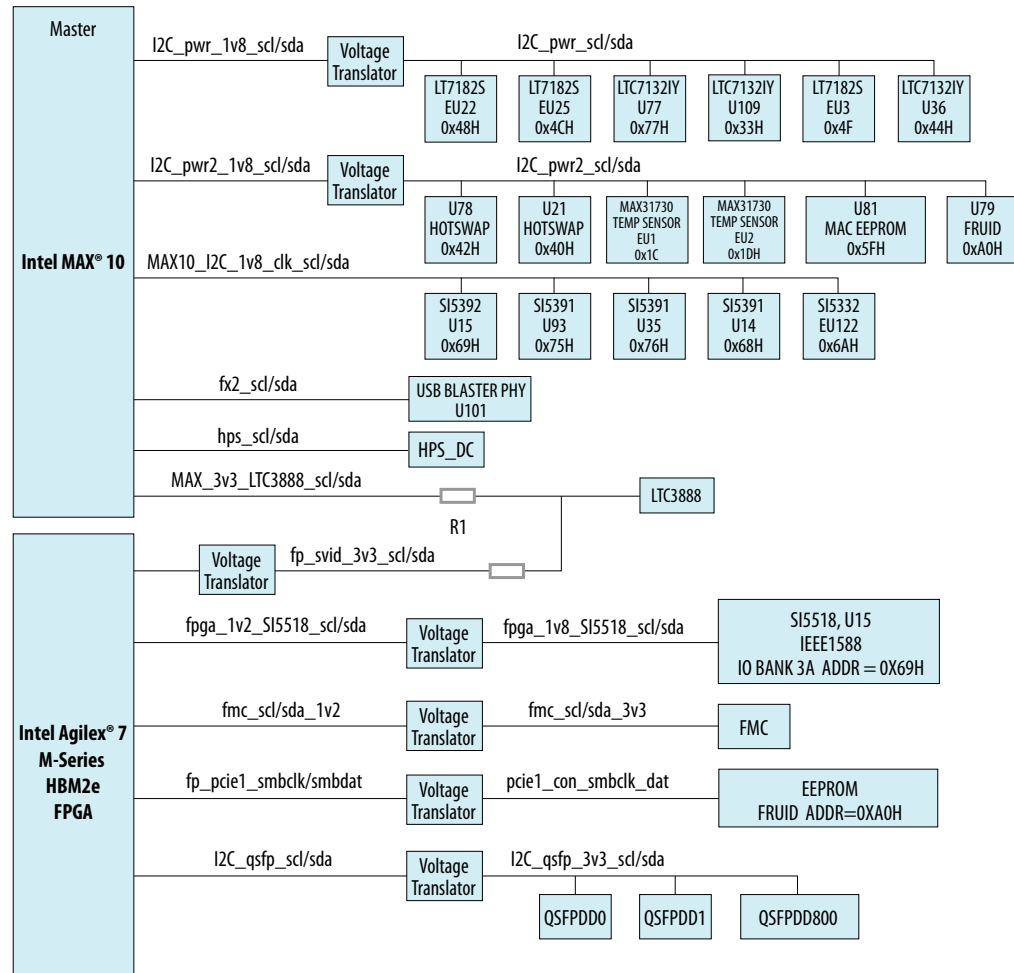
**Table 13. I<sup>2</sup>C Debug Headers**

Schematic Signal Name	Description
PMB_SCL/SDA	VRs I <sup>2</sup> C header <b>J5</b> and <b>J91</b>
CLK_I2C_SDA/SCL_3V3	All clock devices I <sup>2</sup> C header <b>J40</b>
HPS_SCL/HPS_SDA	HPS I <sup>2</sup> C interface MAX 10
FMC_SCL_1V2 FMC_SDA_1V2	FMC+ I <sup>2</sup> C interface Agilex 7 M-Series HBM2e
FP_I3C_2C_DIMM_SCL FP_I3C_2C_DIMM_SDA	DDR5_I3C_RDIMM interface Agilex 7 M-Series HBM2e
MAX10_I2C_2C_DIMM_SCL MAX10_I2C_2C_DIMM_SDA	DDR5_I3C_RDIMM interface Agilex 7 M-Series HBM2e
I2C_PWR2_SCL I2C_PWR2_SDA	Agilex 7 M-Series HBM2e R-Tile die, 3 F-Tile die, I/O core die board temperature sense, I <sup>2</sup> C interface MAX 10
FX2_SCL/FX2_SDA	USB PHY I <sup>2</sup> C interface MAX 10
MAX2237B_SCL/SDA	SI569_148.50 MHz interface MAX 10 can adjust the frequency for FMC+Video interface card

**Table 14. SPI Debug Headers for SI5518 Clocks**

Schematic Signal Name	Description
FPGA_SI5518_1V8_GPIO3	SI5518 SPI BUS, Debug connector <b>J22</b> and <b>J41</b>
FPGA_SI5518_A0_1V8_CSB	
I2C_1V8_CLK_GUI_SDA	
I2C_1V8_CLK_GUI_SCL	

**Figure 28. I<sup>2</sup>C Serial Bus**



## A.6. Daughter Card

### HPS IO48 OOB E Daughter Card

- 1x RGMII 10/100/1000 Mbps Ethernet port: Standard RJ-45
- 1x UART port: Standard USB Mini-B Receptacle
- 1x Micro SD Card Connector: Standard Micro SD Card Socket
- 1x USB 2.0 port: Standard USB Micro-AB Receptacle
- 1x Mictor 38-pin connector (JTAG only without Trace signals)
- HPS dedicated JTAG pins are connected with both mother board JTAG chain and Mictor 38-pin header

- I<sup>2</sup>C: HPS I<sup>2</sup>C port
- GPIO
  - 2x Push buttons
  - 3x LEDs
  - 1x Ethernet Interrupt from Ethernet PHY
  - 1x USB over-current indicator
- HPS Clock: 25 MHz oscillator

## A.7. Connectors and Cables

**Table 15. Connectors and Cables**

Connectors and Cables	Part Number	Switch Reference	Notes
QSFPDD loopback module	NLNAMB0001 (Amphenol)	<b>J16</b> <b>J17</b>	—
QSFP-DD800 loopback type 1	ML4062-LB-112 (Multilane)	<b>J18</b>	For 800 G usage, connect 85107421 at <b>J18</b>
MCIO cable	HMC74-0631 (Amphenol)	<b>J10</b> <b>J11</b>	—



## B. Additional Information

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### B.1. Safety and Regulatory Information



#### **ENGINEERING DEVELOPMENT PRODUCT - NOT FOR RESALE OR LEASE**

This development kit is intended for laboratory development and engineering use only.

This development kit is designed to allow:

- Product developers and system engineers to evaluate electronic components, circuits, or software associated with the development kit to determine whether to incorporate such items in a finished product.
- Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required Federal Communications Commission (FCC) equipment authorizations are first obtained.

Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference.

Unless the assembled kit is designed to operate under Part 15, Part 18 or Part 95 of the United States Code of Federal Regulations (CFR) Title 47, the operator of the kit must operate under the authority of an FCC licenseholder or must secure an experimental authorization under Part 5 of the United States CFR Title 47.

Safety Assessment and CE & UKCA mark requirements have been completed, however, other certifications that may be required for installation and operation in your region have not been obtained.

### B.1.1. Safety Warnings



#### Power Supply Hazardous Voltage

AC mains voltages are present within the power supply assembly. No user serviceable parts are present inside the power supply.

#### Power Connect and Disconnect

The AC power supply cord is the primary disconnect device from mains (AC power) and used to remove all DC power from the board/system. The socket outlet must be installed near the equipment and must be readily accessible.

	<b>WARNING</b>	
<b>RISK OF ELECTRIC SHOCK</b>		
Connect only to a properly earth grounded outlet. Apparaten skall anslutas till jordat uttag när den ansluts till ett nätverk.		

#### System Grounding (Earthing)

To avoid shock, you must ensure that the power cord is connected to a properly wired and grounded receptacle. Ensure that any equipment to which this product is attached to is also connected to properly wired and grounded receptacles.

	<b>WARNING</b>	
<b>RISK OF ELECTRIC SHOCK</b>		
Do not attempt to modify or use the supplied AC power cord if it is not the exact type and rating required.		

### Power Cord Requirements

The plug on the power cord must be a grounding-type male plug designed for use in your region. It must have certification marks showing certification by an agency in your region. The connector that plugs into the appliance inlet of the power supply must be an IEC 320, sheet C13, female connector. If the power cord supplied with the system does not meet requirements for use in your region, discard the cord, and do not use it with adapters. Use only certified power supply cord with appropriate gauge, designed for use in your region.



### Lightning/Electrical Storm

Do not connect/disconnect any cables or perform installation/maintenance of this product during an electrical storm.

### Risk of Fire

To reduce the risk of fire, keep all flammable materials a safe distance away from the boards and power supply. You must configure the development kit on a flame retardant surface.

## B.1.2. Safety Cautions

	<b>CAUTION</b>	
	<b>Hot Surfaces and Sharp Edges</b>	
<p><b>Integrated Circuits and heat sinks may be hot if the system has been running. Also, there might be sharp pins and edges on some boards. Contact should be avoided.</b></p>		

### Thermal and Mechanical Injury

Certain components such as heat sinks, power regulators, and processors may be hot. Heatsink fans are not guarded. Power supply fan may be accessible through guard. Care should be taken to avoid contact with these components.





### **Cooling Requirements**

Maintain a minimum clearance area of 5 centimeters (2 inches) around the side, front and back of the board for cooling purposes. Do not block power supply ventilation holes and fan.

### **Electro-Magnetic Interference (EMI)**

This equipment has not been tested for compliance with emission limits of FCC and similar international regulations. Use of this equipment in a residential location is prohibited. This equipment generates, uses and can radiate radio frequency energy which may result in harmful interference to radio communications. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment on and off, you are required to take measures to eliminate this interference.

### **Telecommunications Port Restrictions**

The wireline telecommunications ports (modem, xDSL, T1/E1) on this product must not be connected to the Public Switched Telecommunication Network (PSTN) as it might result in disruption of the network. No formal telecommunication certification to FCC, R&TTE Directive, or other national requirements have been obtained.



### Electrostatic Discharge (ESD) Warning

A properly grounded ESD wrist strap must be worn during operation/installation of the boards, connection of cables, or during installation or removal of daughter cards. Failure to use wrist straps can damage components within the system.

**Attention:** Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of this product in unsorted municipal waste.

### Lithium Ion Battery Warnings



**Lithium Battery:** Risk of explosion if the lithium battery is replaced by an incorrect type. Risk of fire, explosion, or chemical burn if the battery is mistreated (punctured or crushed). Do not attempt to disassemble. Do not incinerate. Observe proper polarity when replacing battery. Do not dispose—the battery is intended to be serviced and disposed by qualified Intel service personnel only.

**Perchlorate Material:** Special handling may apply. For more details, refer to [www.dtsc.ca.gov/hazardouswaste/perchlorate](http://www.dtsc.ca.gov/hazardouswaste/perchlorate). This notice is required by California Code of Regulations, Title 22, Division 4.5, Chapter 33: Best Management Practices for Perchlorate Materials. This product includes a battery which contains perchlorate material.

### Taiwan battery recycling:



廢電池請回收

(Translation - please recycle batteries)

**Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of product in unsorted municipal waste.**

## B.2. Compliance Information

### CE EMI Conformity Caution

This development board is delivered conforming to relevant standards mandated by Directive 2014/30/EU. Because of the nature of programmable logic devices, it is possible for the user to modify the development kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as a result of modifications to the delivered material is the responsibility of the user of this development kit.

