



# Clock Jitter Tool

## User Guide

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*April 2025*

**Revision 6.0.2**



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# Revision History

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Revision Number	Description	Date
6.0.2	<ul style="list-style-type: none"> <li>Update to address tool error when loading waveform files</li> </ul>	April 2025
6.0.1	<ul style="list-style-type: none"> <li>Update to support PCI Express 6.0</li> <li>MATLAB* Runtime installer removed from the Clock Jitter Tool package</li> </ul>	December 2024
5.0.1	<ul style="list-style-type: none"> <li>Update for the Clock Jitter Tool</li> </ul>	August 2021

# 1 Introduction and Quick Start

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## 1.1 Introduction

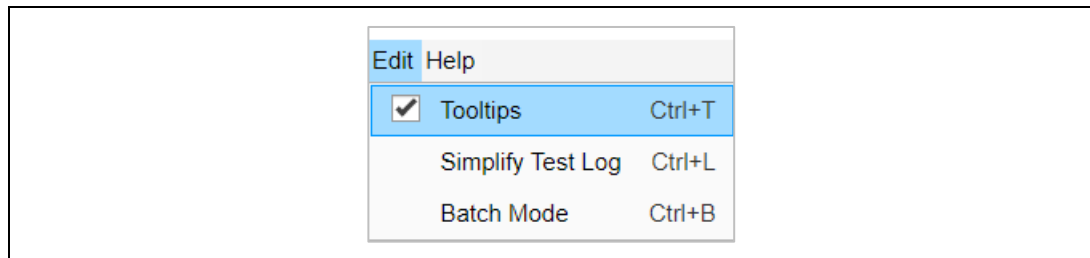
The Clock Jitter Tool is a jitter analysis tool for PCI Express\* (PCIe\*) reference clock ("refclk").

## 1.2 Quick Start

### 1.2.1 Tooltips

Tooltips can show a brief introduction to each function and configuration. If this is the first time using this version of the Clock Jitter Tool, enable **Tooltips** as shown in [Figure 1-1](#).

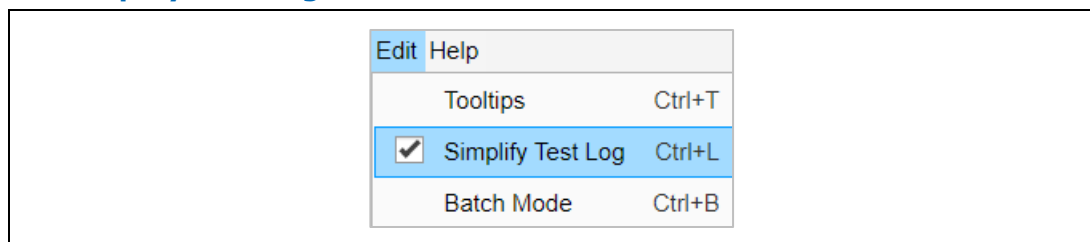
**Figure 1-1. Tooltips in the Edit Menu**



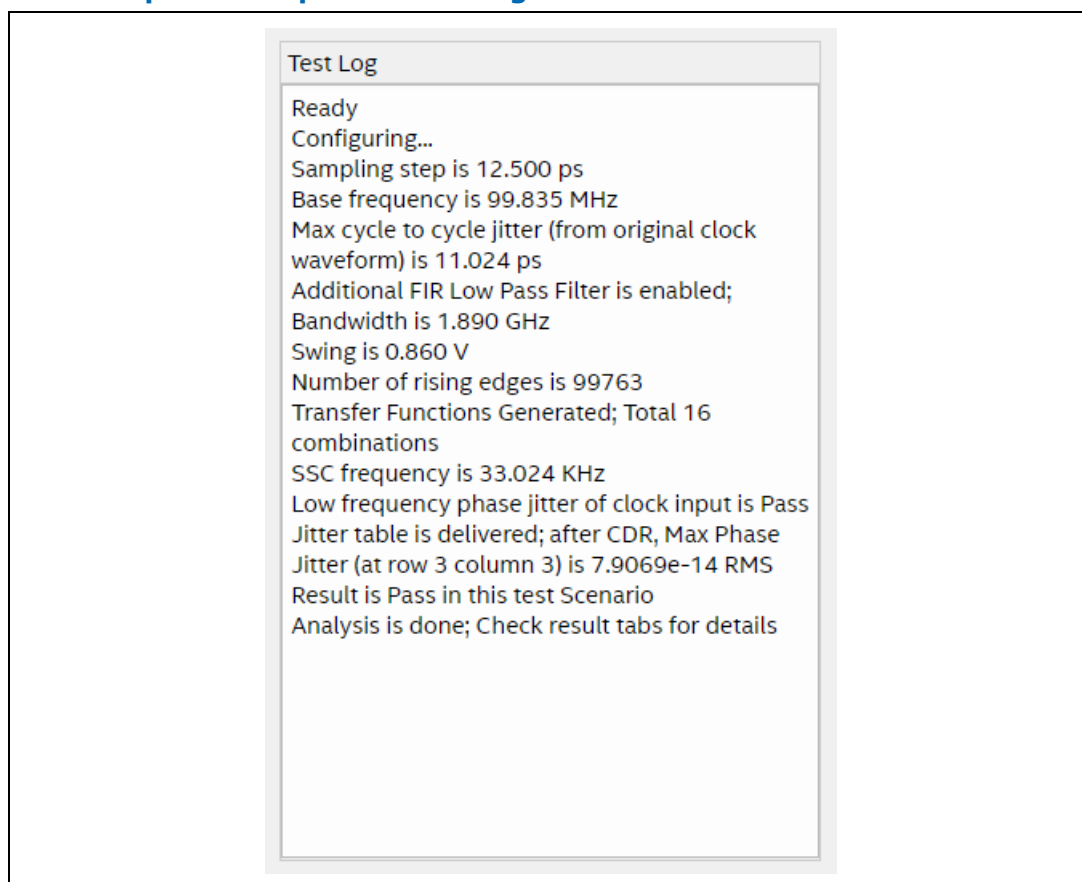
### 1.2.2 Simplify Test Log

The test log can be simplified by selecting the checkbox shown in [Figure 1-2](#). After enabling this option, only key parameters (without a step description) are kept in the test log. [Figure 1-3](#) shows an example.

**Figure 1-2. Simplify Test Log in the Edit Menu**



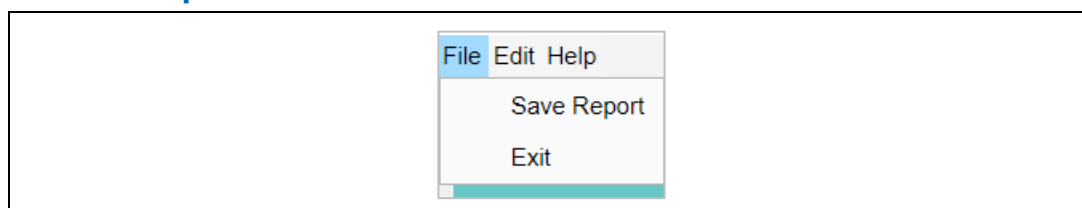
**Figure 1-3. Example as Simplified Test Log**



### 1.2.3 Save Report

After a successful simulation, a .pdf or HTML report, including all the analysis details, can be generated. After clicking the **Save** button, wait for a while (about 20 seconds) until the .pdf report pops out automatically. While the Clock Jitter Tool saves the report, the user should not attempt any other operations, to avoid potential tool crashes.

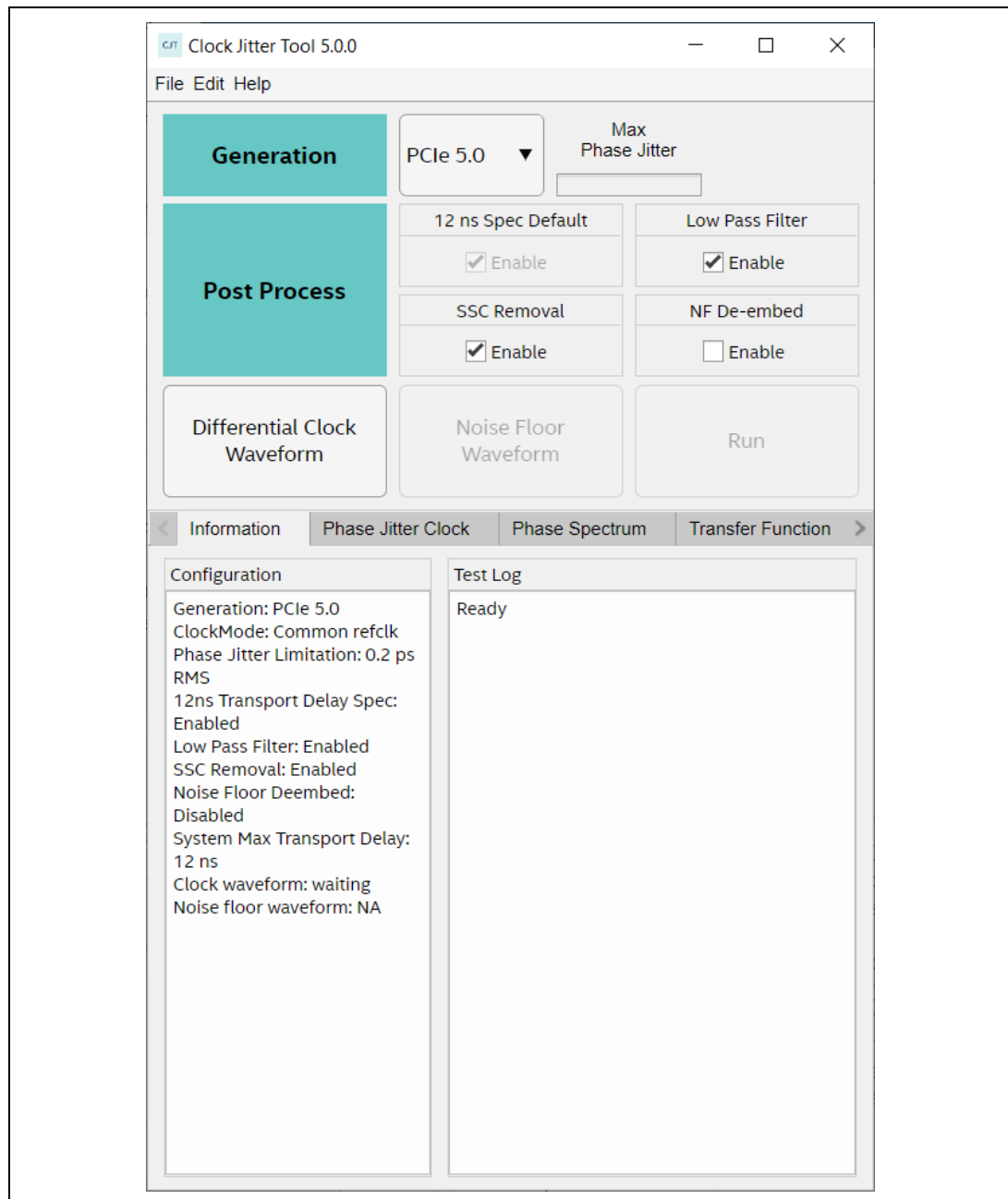
**Figure 1-4. Save Report in the File Menu**



## 2 *Clock Jitter Tool Settings in the Main Window*

As the default interface, the main window includes the complete Clock Jitter Tool configurations.

**Figure 2-1. Clock Jitter Tool GUI Main Window**

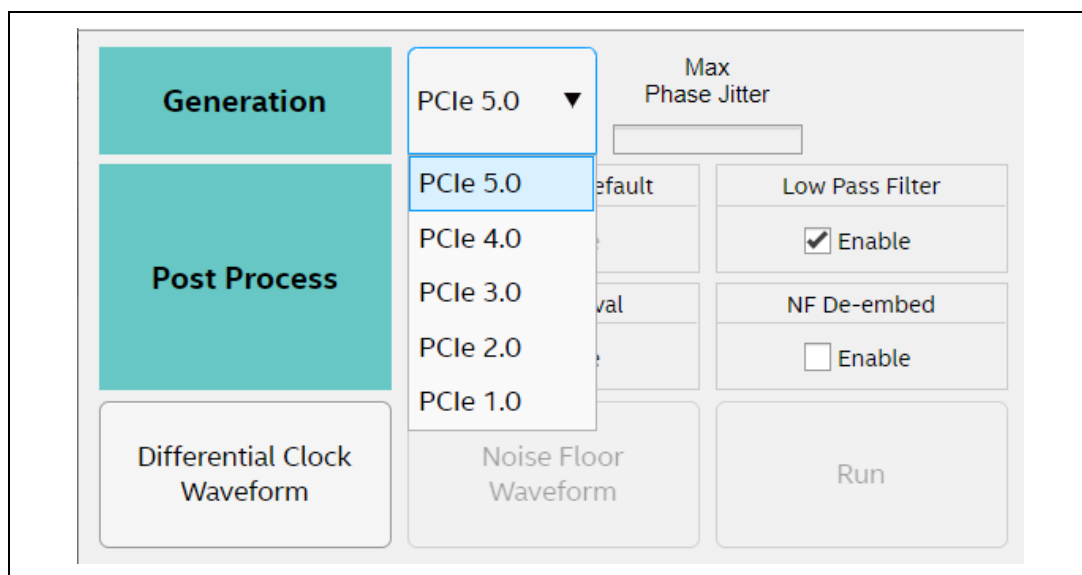




## 2.1 Generation

The Clock Jitter Tool can support a total of six PCIe\* generations in the **Generation** dropdown menu. An example view of the dropdown menu can be seen in [Figure 2-2](#).

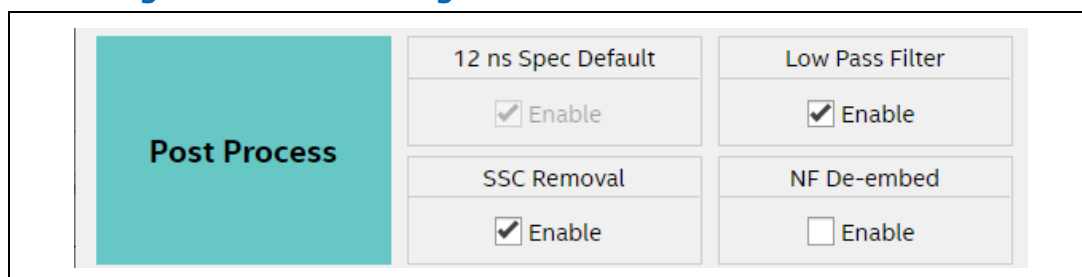
**Figure 2-2. List of Generations**



## 2.2 Post-Process and New Algorithms

There are four post-process configurations in the Clock Jitter Tool: **12 ns Spec Default** (transport delay), **Low Pass Filter**, **SSC Removal**, and **NF De-embed**, as shown in [Figure 2-3](#).

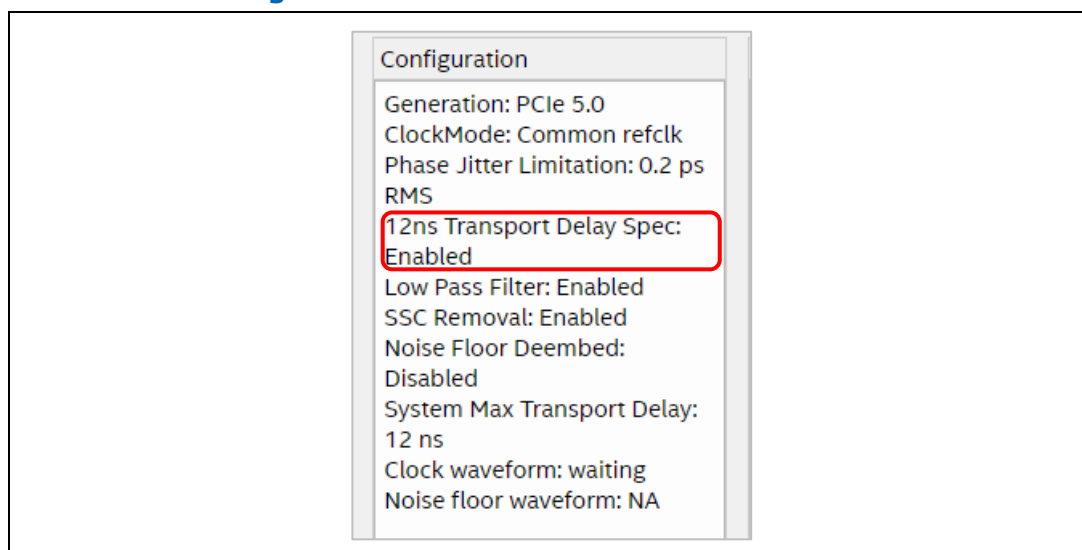
**Figure 2-3. Configurations of New Algorithms**



### 2.2.1 12 ns Spec Default (Transport Delay)

This function is designed for the PCIe\* compliance test: The system transport delay is fixed as 12 ns in the specification, instead of the flight time calculation for channels in the actual system. The status of this function can also be found in the **Configuration** text, as shown in [Figure 2-4](#). In the Clock Jitter Tool, this configuration is fixed for the compliance test.

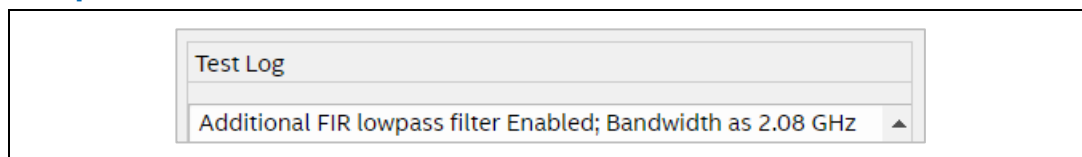
**Figure 2-4. 12 ns in Configuration Text**



## 2.2.2 Low Pass Filter

This function is designed per the *PCI Express\* Base Specification 6.0*, as the purpose of “The first, edge filtering, minimizes the measurement-induced jitter due to the finite sampling rate of the test equipment.” Since there is no specific value for bandwidth in the PCIe\* 6.0 specification, the Clock Jitter Tool uses a dynamic low pass filter controlled by the effective 3 dB frequency of the clock input waveforms. [Figure 2-5](#) shows an example.

**Figure 2-5. Example for Bandwidth of Additional Finite Impulse Response (FIR) Lowpass Filter**



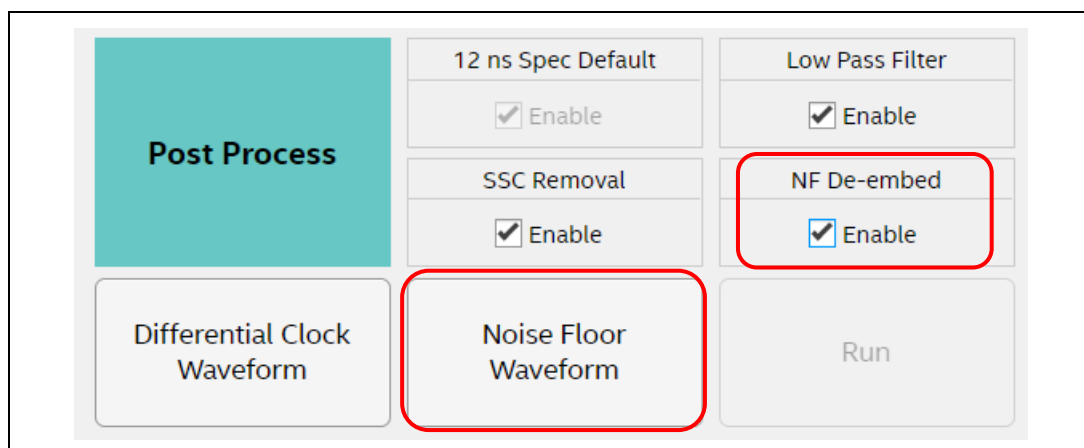
## 2.2.3 Spread-Spectrum Clocking (SSC) Removal

SSC removal is requested for PCIe\* 4.0 and onwards, as indicated in note 3 of the “Jitter Limits for Common Clock Architecture” table in the *PCI Express Base Specification 6.0*, version 1.0.

## 2.2.4 Noise Floor (NF) De-embed

This feature is an Intel new algorithm to remove the additional jitter brought by an oscilloscope (and probes) NF. When enabled, as in [Figure 2-6](#), the waveform of the NF is a must (see the step-by-step NF measurement process in [Capture NF Waveform](#)).

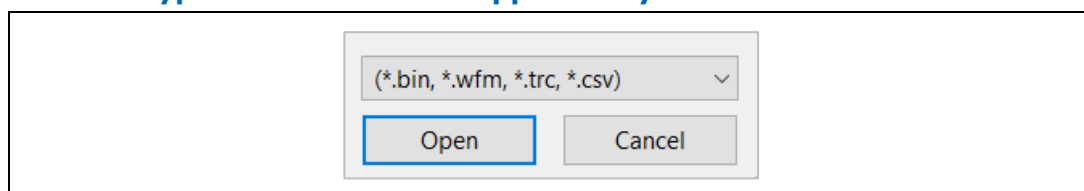
**Figure 2-6. NF Waveform Button when Function Enabled**



## 2.3 Waveform Import

As shown in [Figure 2-7](#), four types of differential waveforms can be imported to the Clock Jitter Tool: .bin, .wfm, .trc, and .csv.

**Figure 2-7. Four Types of Waveforms Supported by the Clock Jitter Tool**



### 2.3.1 Differential Clock Waveform

The clock waveform for Clock Jitter Tool 6.0.1 should be a differential toggle signal with a reasonable voltage swing. The number of clock cycles should be at least 160K. Oscilloscope configuration details can be found in [Capture the Clock Waveform](#).

### 2.3.2 Differential NF Waveform

When the NF De-embed function is enabled, the differential NF waveform is necessary for the measurement, as shown in [Figure 2-6](#). See the step-by-step NF measurement process in [Capture NF Waveform](#).

## 2.4 Information and Result Panel

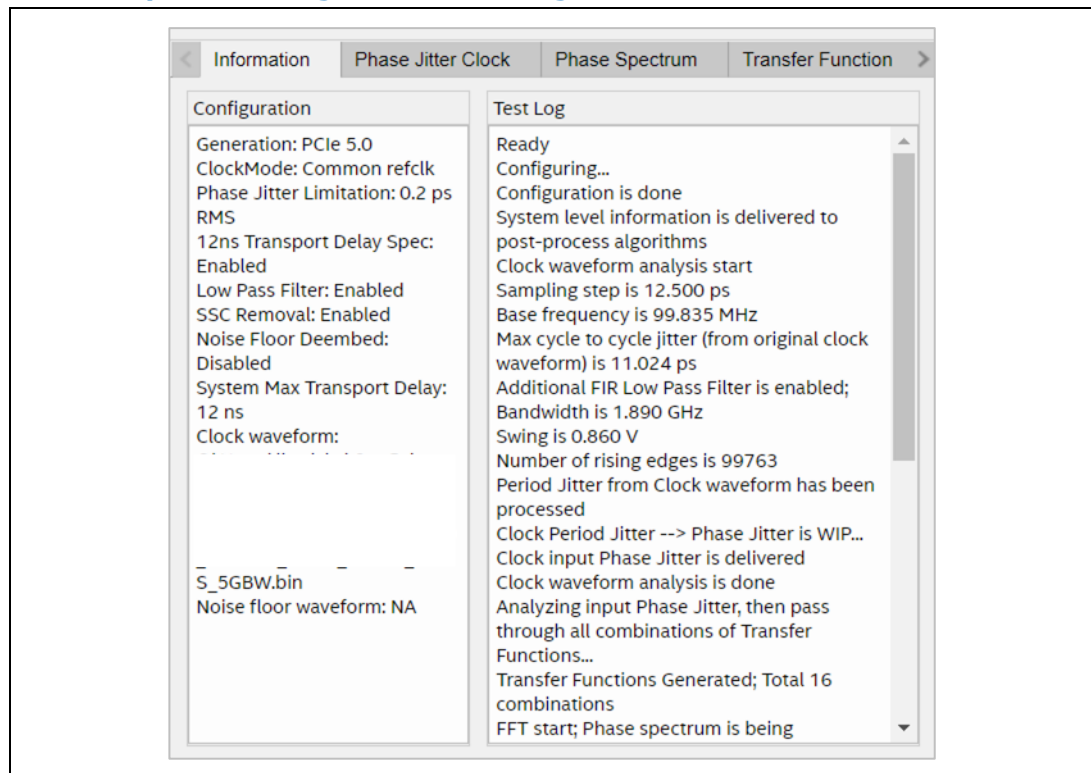
### 2.4.1 Configuration and Log

The configuration includes all the information from system-level clock configurations, such as generation, clock mode (fixed as "Common refclk" for the compliance test), function/status, transport delay, and waveform file paths.

After clicking the **Run** button, the **Test Log** area updates the information of critical steps until the simulation is done.

To speed up the analysis, the Clock Jitter Tool uses partial waveforms to calculate some parameters that are not critical for the final phase jitter results. Take the base frequency as an example: This parameter is selected as the maximum spike from the spectrum of 3030 clock cycles (equals almost one SSC cycle), so the value may have a tiny difference from the one shown by the oscilloscope.

**Figure 2-8. Example of Configuration and Log**



## 2.4.2 Phase Jitter Table Tabs

In the **Phase Jitter Clock** tab, a table shows the phase jitter from the clock waveform in Root-Mean-Square (RMS) (or in ps for PCIe\* 1.0 peak-to-peak jitter). The total number of combinations is relative to the generation in the specification. For example, there are 16 combinations for PCIe\* 6.0 refclk, as shown in [Figure 2-9](#). The PCIe\* Base Specification provides more details about the TX/RX PLL types and combinations.

Per the *PCI Express\* Card Electromechanical Specification 6.0*, the Clock Jitter Tool uses 200 fs RMS for PCIe\* 6.0 refclk phase jitter pass/fail judgment.

**Figure 2-9. Example of Phase Jitter Table**

< Information	Phase Jitter Clock	Phase Jitter Deembed	Phase Spectrum	Transfer Function >
	BW0p5MHz_PK0p01dB	BW0p5MHz_PK2dB	BW1p8MHz_PK0p01dB	BW1p8MHz_PK2dB
Delay+BW0p5MHz_PK0p01dB	3.2346e-14	3.0215e-14	9.5832e-14	6.9870e-14
Delay+BW0p5MHz_PK2dB	3.1080e-14	2.2661e-14	9.7662e-14	7.2827e-14
Delay+BW1p8MHz_PK0p01dB	9.1801e-14	9.4111e-14	1.1585e-13	9.7932e-14
Delay+BW1p8MHz_PK2dB	6.9094e-14	7.1455e-14	1.0575e-13	8.1583e-14

Another table is attached in the **Phase Jitter De-embed** tab if the **NF De-embed** function is enabled. It shows the phase jitter results after de-embedding the impact from the oscilloscope NF. [Figure 2-10](#) shows an example.

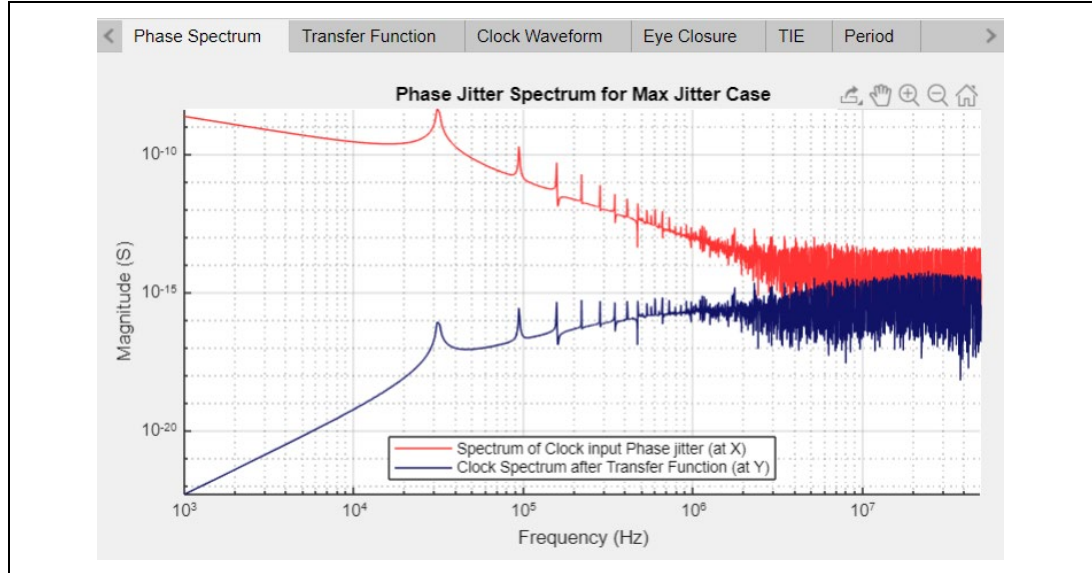
**Figure 2-10. Example of Phase Jitter Table after De-embedding**

< Information	Phase Jitter Clock	Phase Jitter Deembed	Phase Spectrum	Transfer Function >
	BW0p5MHz_PK0p01dB	BW0p5MHz_PK2dB	BW1p8MHz_PK0p01dB	BW1p8MHz_PK2dB
Delay+BW0p5MHz_PK0p01dB	3.0295e-14	2.8596e-14	9.0569e-14	6.6152e-14
Delay+BW0p5MHz_PK2dB	2.9453e-14	2.1225e-14	9.2616e-14	6.9392e-14
Delay+BW1p8MHz_PK0p01dB	8.6668e-14	8.9181e-14	1.0848e-13	9.1728e-14
Delay+BW1p8MHz_PK2dB	6.5384e-14	6.8047e-14	9.9330e-14	7.6412e-14

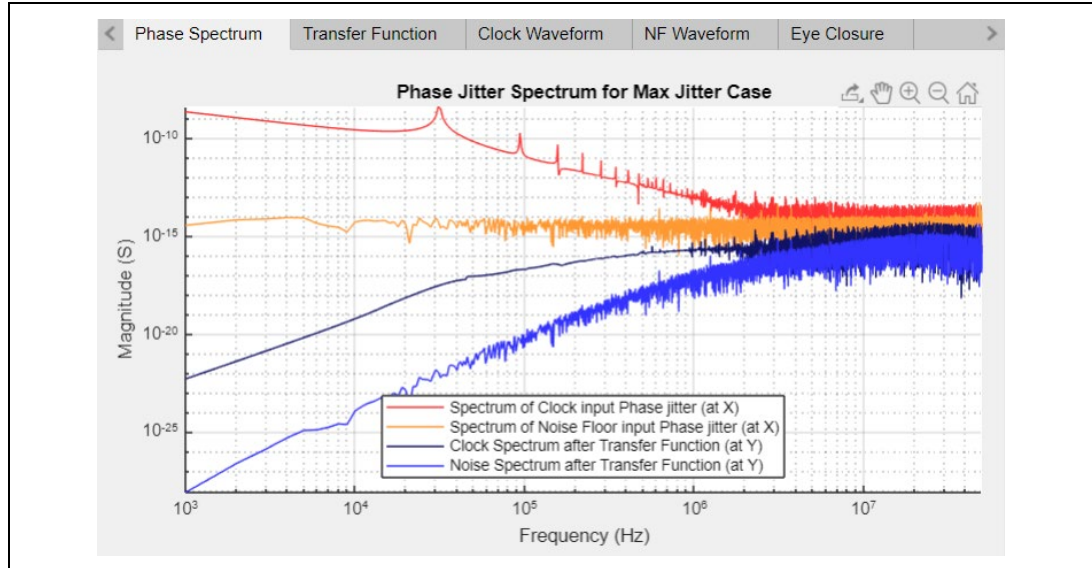
## 2.4.3 Figure Tabs

### 2.4.3.1 Phase Spectrum of Worst Jitter Combination

**Figure 2-11. NF De-embed Disabled and SSC Removal Disabled**



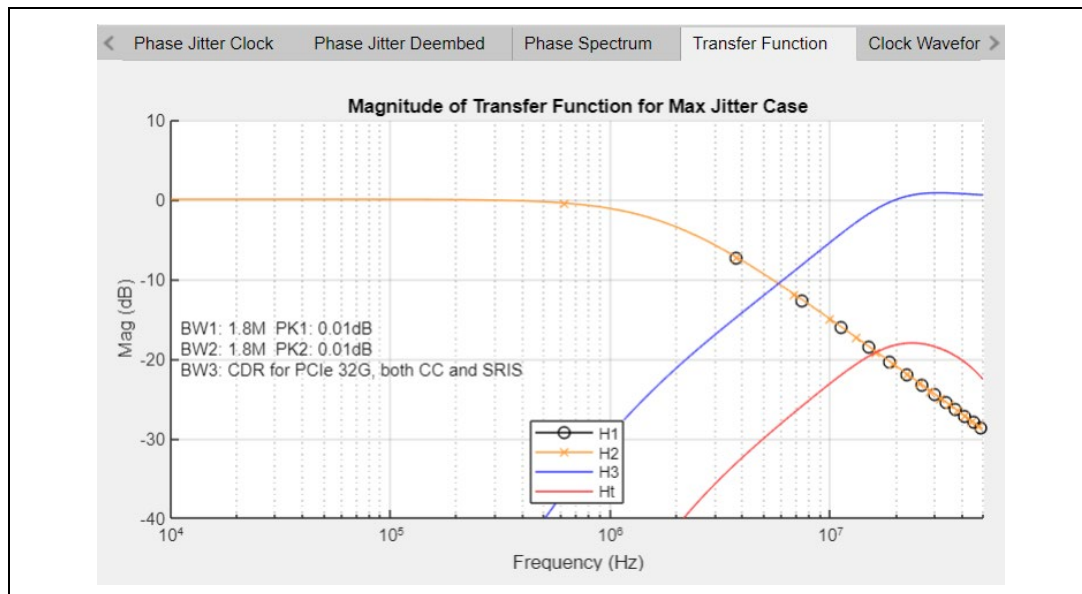
**Figure 2-12. NF De-embed Enabled and SSC Removal Enabled**



### 2.4.3.2 Transfer Function of Worst Jitter Combination

The figure in this tab shows the set of H1H2H3 transfer functions for the maximum phase jitter combination. [Figure 2-13](#) shows an example.

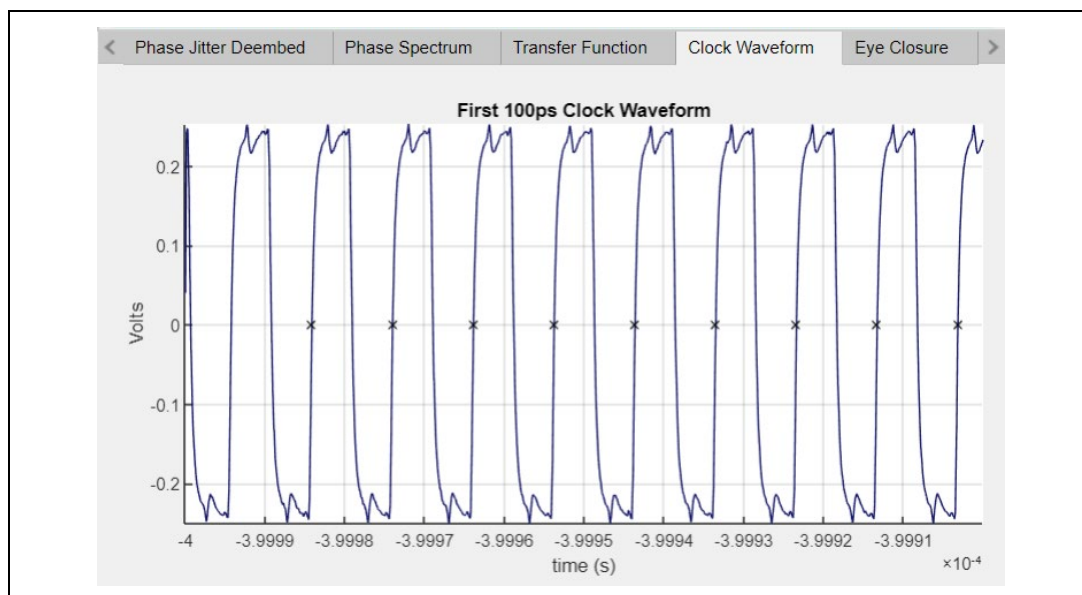
**Figure 2-13. H1, H2, H3, and Ht**



### 2.4.3.3 Clock Waveform of First 100 ps

Ten clock cycles are shown in this tab, with crossing points between rising edges and the 0V threshold voltage. [Figure 2-14](#) shows an example.

**Figure 2-14. Clock Waveform**

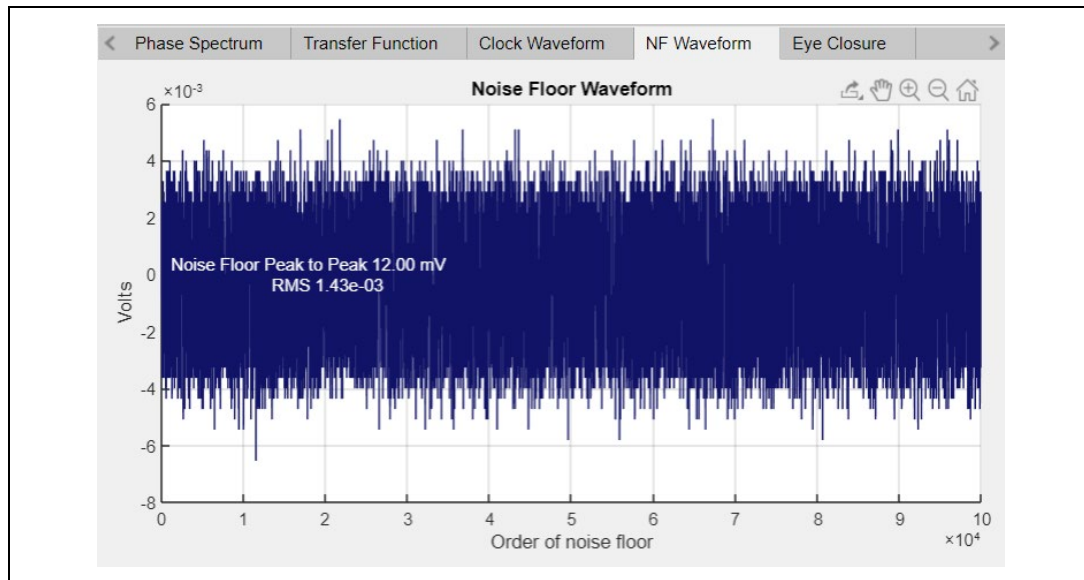




### 2.4.3.4 NF Waveform

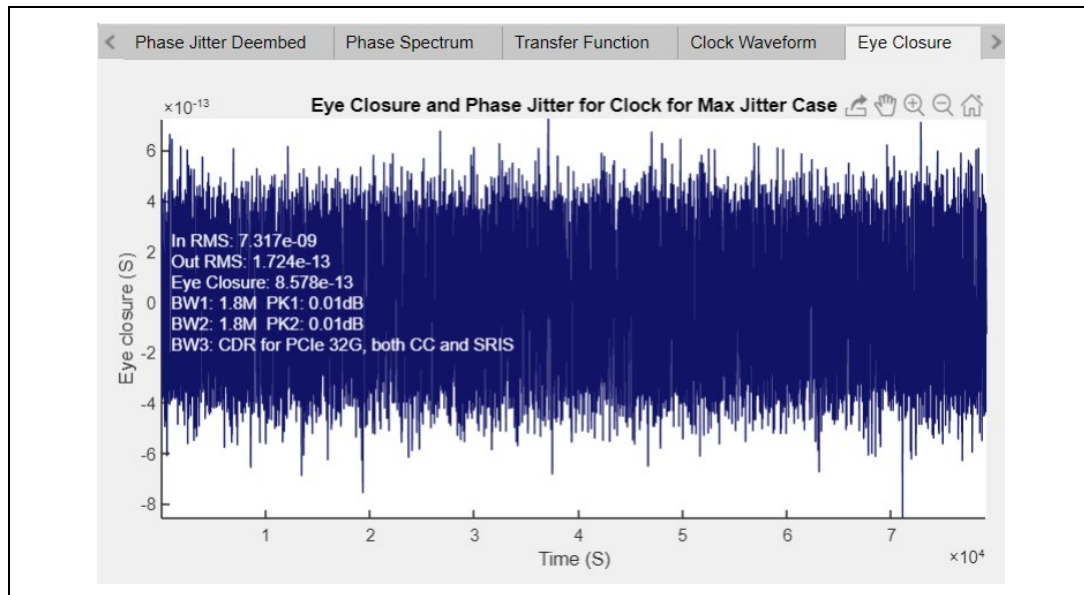
When **NF De-embed** is enabled, a new tab is generated to show the waveform of the NF. This figure can also be used to double-check the quality of the NF when debugging.

**Figure 2-15. NF Waveform**



### 2.4.3.5 Eye Closure of Each Cycle

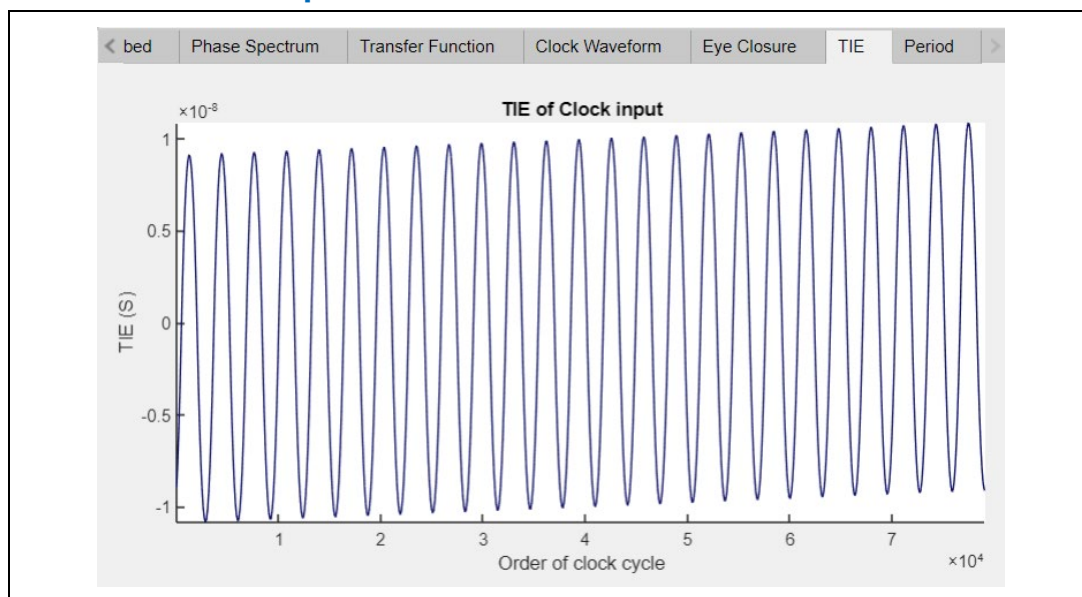
**Figure 2-16. Eye Closure Figure and Key Information**





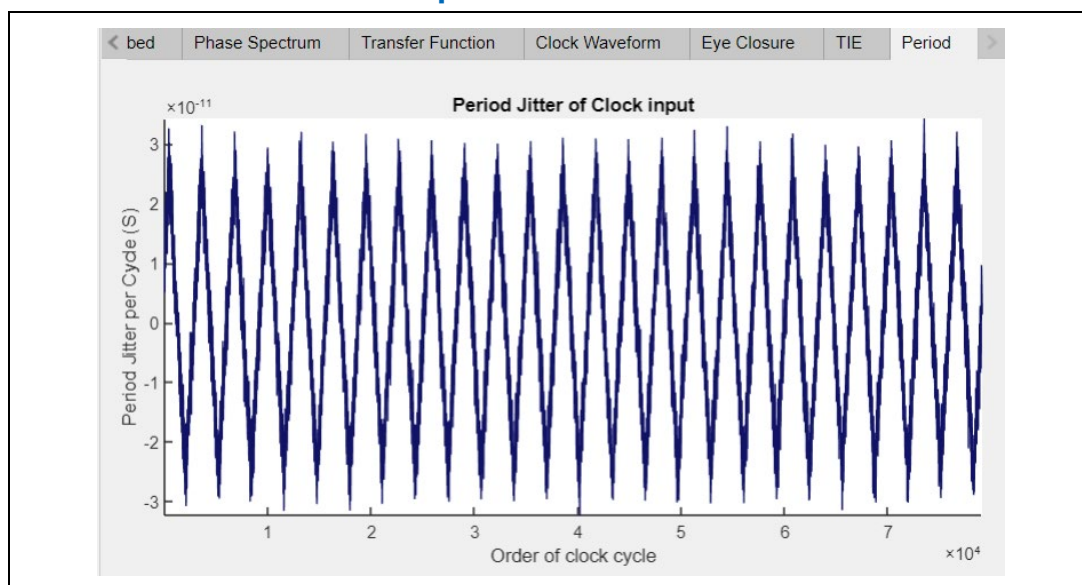
### 2.4.3.6 Time Interval Error (TIE)

**Figure 2-17. TIE of Clock Input**



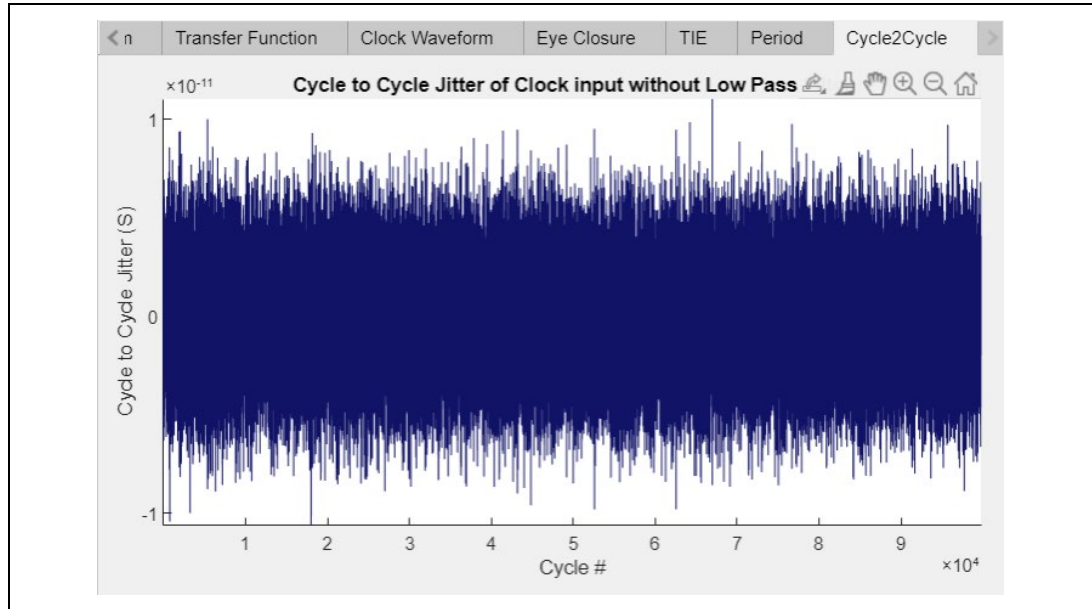
### 2.4.3.7 Period Jitter

**Figure 2-18. Period Jitter of Clock Input**



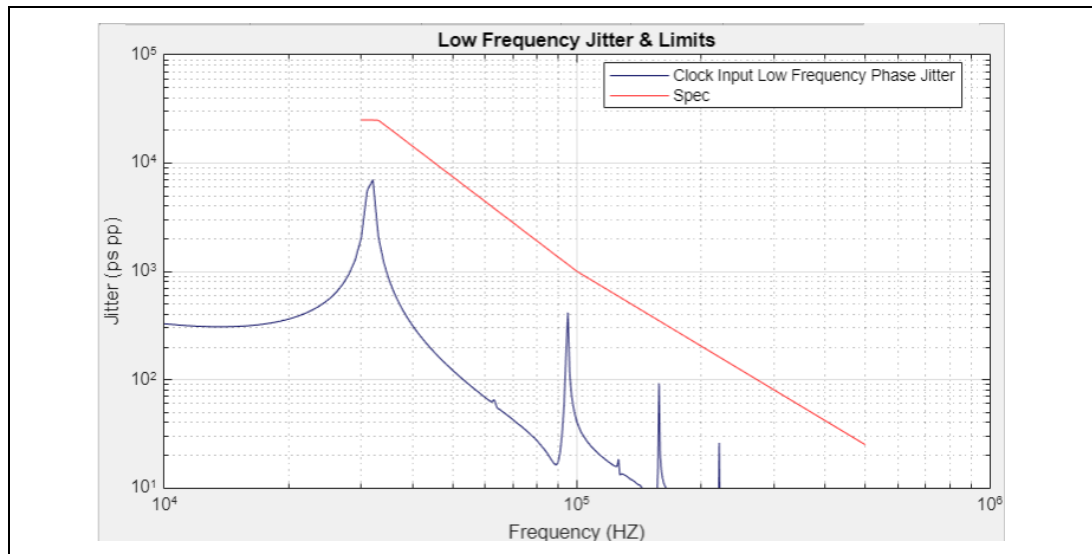
### 2.4.3.8 Cycle-to-Cycle Jitter

Figure 2-19. Cycle-to-Cycle Jitter of Clock Input



### 2.4.3.9 Low Frequency Phase Jitter

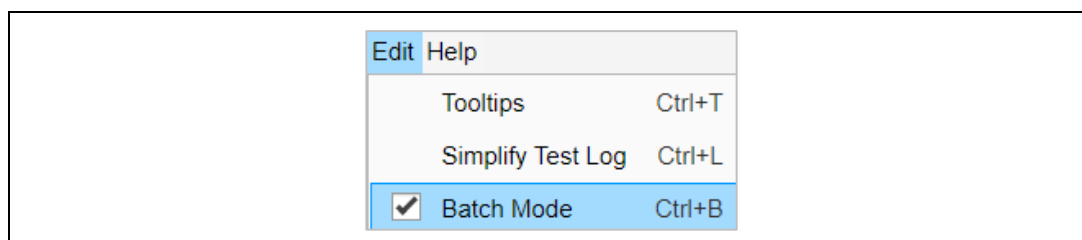
Figure 2-20. Low Frequency Phase Jitter and Limitation in the Specification



## 3 Batch Mode for High Volume Test

The batch mode can be switched into by enabling the **Batch Mode** in the **Edit** menu or **Ctrl + B**.

**Figure 3-1. Enabled Batch Mode**



### 3.1 Batch Mode Table

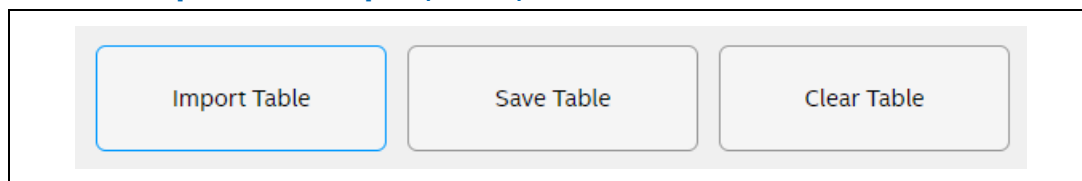
By default, there is a one-row table shown in the batch mode GUI after this mode is enabled. All the information and configurations in this one-row table are generated automatically from the configuration in the main GUI. It can be used as a demo to check the variables.

**Figure 3-2. One-Row Table after Batch Mode Selected**

Batch Mode by Table											
BMRReady	JitterLimitation	MaxPhaseJitter	PassFail	Generation	LowPassFilter	SSCRemoval	NFDeembed	ClockWaveform	NFWaveform	CJTVersion	CJTsimDate
TBD	0.2 ps RMS			PCIe 5.0	Enabled	Enabled	Disabled	C:\Users\jliwetzha\OneDrive - Intel Corporation\Docu...	NA		

The batch mode table has three operation modes: **Import Table**, **Save Table**, and **Clear Table**. The following figure shows the buttons:

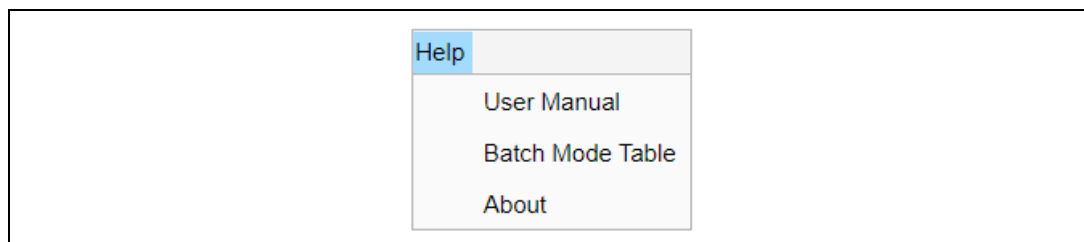
**Figure 3-3. Table Operation: Import, Save, and Clear**



#### 3.1.1 Import Table

The batch mode uses an Excel\* table (.xls) to define the system configurations and waveform paths. A demo .xls table can be checked in the **Help** menu, as shown in Figure 3-4. Copy the demo table into a new .xls file before changing it. Update the waveform paths (path for clock waveform, or paths for both clock and NF when the **NF De-embed** feature is enabled).

**Figure 3-4. Demo Table for Batch Mode**



### 3.1.2 Save Table

The .xls table can be saved from the Clock Jitter Tool to an Excel\* file. After the batch run, the final table with simulation results can be restored for a later check.

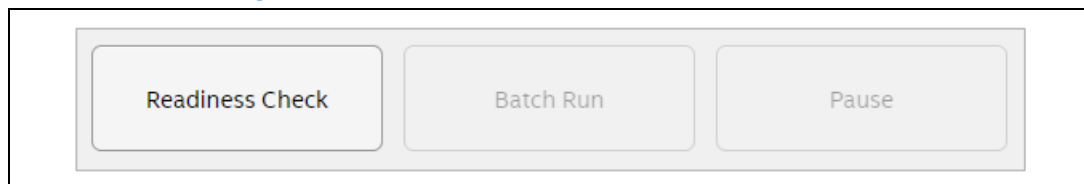
### 3.1.3 Clear Table

If a wrong table is imported, it can be cleared by clicking the **Clear Table** button. The default one-row table will appear again automatically instead of the previous imported table.

## 3.2 Batch Run Operation

The batch simulation has three operation modes: **Readiness Check**, **Batch Run**, and **Pause**. The following figure shows the buttons:

**Figure 3-5. Simulation Operation: Readiness Check, Batch Run, and Pause**



### 3.2.1 Readiness Check

Readiness Check is a must step before the batch simulation. In this step, the tool checks the configurations of each row to ensure the configurations are correct for the simulation. After doing the Readiness Check, the buttons **Batch Run** and **Pause** will be enabled.

If the configurations are correct, the status of **BMReady** is updated to **Yes**. If the configurations are not correct, the relative error is shown for debugging. Figure 3-6 shows examples of the BMReady status.

**Figure 3-6. Batch Mode Readiness Status**

BMReady
Yes
Yes
Wrong NF setting
Yes
Yes
Yes
Cannot find NF waveform
Wrong SSC setting

## 3.2.2 Batch Run

After the Readiness Check, the tool will run simulations one by one for the correct configured decks.

## 3.2.3 Pause

While analyzing in the batch mode, the **Pause** button can be used to pause for a while. Click this button again to continue.

## 3.3 Batch Run Result

After doing the Batch simulation, the results are shown in the table, including the maximum phase jitter number, pass/fail, Clock Jitter Tool version, and simulation date and time.

**Figure 3-7. Batch Mode Result**

Batch Mode by Table											
BMReady	JitterLimitation	MaxPhaseJitter	Pass/Fail	Generation	LowPassFilter	SSCRemoval	NFDeembed	ClockWaveform	NFWaveform	CJTversion	CJTsimDate
Yes	0.2 ps RMS	7.9069e-14	Pass	PCIe 5.0	Enabled	Enabled	Disabled		NA	CJT 5.0.0	15-May-2021 00:06...
Yes	0.5 ps RMS	2.3414e-13	Pass	PCIe 4.0	Enabled	Enabled	Disabled		NA	CJT 5.0.0	15-May-2021 00:06...
Yes	1 ps RMS	4.7337e-13	Pass	PCIe 3.0	Enabled	Disabled	Disabled		NA	CJT 5.0.0	15-May-2021 00:06...
Yes	3.1 ps RMS	6.2039e-13	Pass	PCIe 2.0	Enabled	Disabled	Disabled		NA	CJT 5.0.0	15-May-2021 00:06...
Yes	86 ps pkpk	3.9325e-12	Pass	PCIe 1.0	Enabled	Disabled	Disabled		NA	CJT 5.0.0	15-May-2021 00:06...
Yes	0.2 ps RMS	7.9069e-14	Pass	PCIe 5.0	Enabled	Enabled	Disabled		NA	CJT 5.0.0	15-May-2021 00:06...
Yes	0.2 ps RMS	7.9069e-14	Pass	PCIe 5.0	Enabled	Enabled	Disabled		NA	CJT 5.0.0	15-May-2021 00:07...


## 4 Command Line

---

### 4.1 Open Command Prompt

To open the Command Prompt, click the Windows\* OS button, type in "cmd" and then press **Enter**. Then, navigate to the directory where the Clock Jitter Tool is installed.

**Figure 4-1. Command Prompt and Folder of Application**



```
cmd: Command Prompt
Microsoft Windows [Version 10.0.18363.1679]
(c) 2019 Microsoft Corporation. All rights reserved.

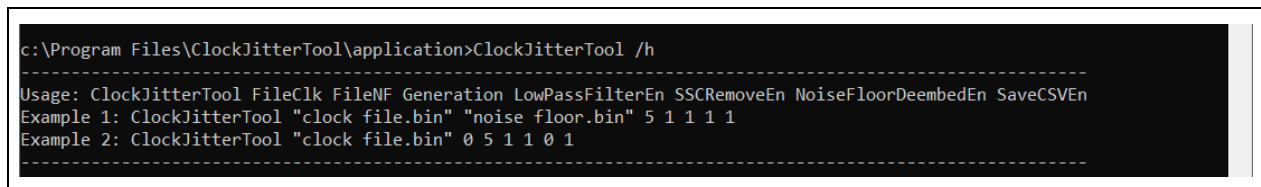
C:\Users\>cd "c:\Program Files\ClockJitterTool\application"

c:\Program Files\ClockJitterTool\application>
```

### 4.2 Clock Jitter Tool Help

Use "ClockJitterTool -h" or "ClockJitterTool /h" to check the help and some examples for this tool.

**Figure 4-2. Command Line Usages and Examples**



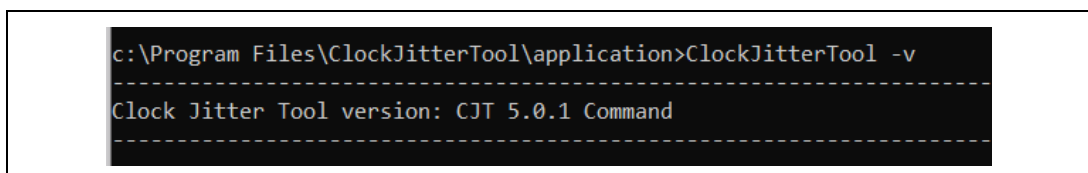
```
c:\Program Files\ClockJitterTool\application>ClockJitterTool /h

-----
Usage: ClockJitterTool FileClk FileNF Generation LowPassFilterEn SSCTimeEn NoiseFloorDeembedEn SaveCSVEn
Example 1: ClockJitterTool "clock file.bin" "noise floor.bin" 5 1 1 1 1
Example 2: ClockJitterTool "clock file.bin" 0 5 1 1 0 1
-----
```

### 4.3 Clock Jitter Tool Version

Use "ClockJitterTool -v" or "ClockJitterTool /v" to show the tool version without running a simulation.

**Figure 4-3. Clock Jitter Tool Version**



```
c:\Program Files\ClockJitterTool\application>ClockJitterTool -v

-----
Clock Jitter Tool version: CJT 5.0.1 Command
-----
```

## 4.4 Clock Jitter Tool Arguments

A total of seven arguments are used for the `ClockJitterTool` command. Arguments must be in the following sequence:

1. **FileClk**: File of clock waveform (path included). This argument is a must to run the command.
2. **FileNF**: File of NF waveform (path included). This argument is a must when the NF De-embed feature is enabled.
3. **Generation**: Type the order of PCIe\* generation to call the specific transfer functions, for example "5" means PCIe\* 5.0.
4. **LowPassFilterEn**: When this argument is set as 1, an additional low pass filter is enabled. "0" stands for disable.
5. **SSCRemoveEn**: When this argument is set as "1", SSC spikes will be removed from the phase jitter spectrum. Per the *PCI Express Base Specification 6.0*, this feature must be enabled for PCIe\* 4.0 and onwards. "0" stands for disable.
6. **NoiseFloorDeembedEn**: When this argument is set as "1", the NF waveform will be analyzed to remove the phase jitter impacts from the test environment. "0" stands for disable.
7. **SaveCSVEn**: When this argument is set as "1", a .csv file is generated to record the results. This file is saved with the same name as FileClk and in the same folder of FileClk. "0" stands for no .csv saved. [Figure 4-4](#) shows an example of .csv.

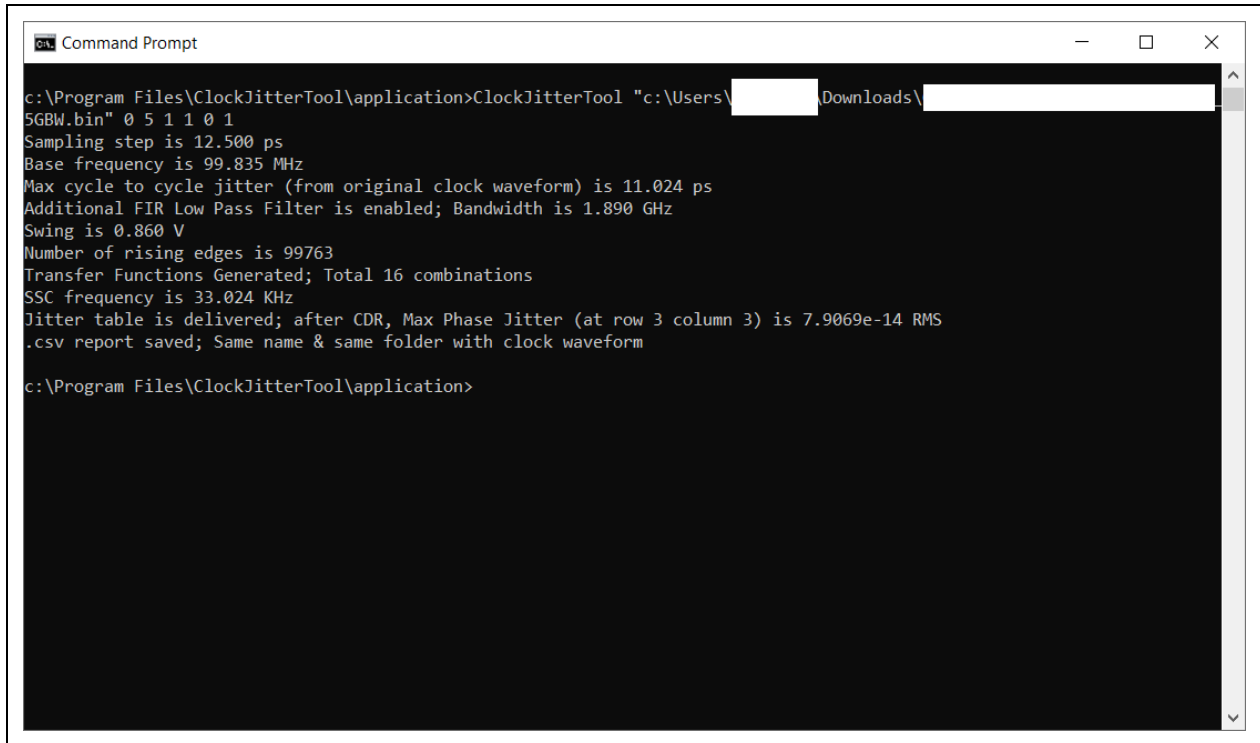
**Figure 4-4. ClockJitterTool Command .csv Report**

	A	B
1	FileClk	C:\Users\ \Doc
2	FileNF	0
3	Interface	PCIE
4	Generation	5
5	LowPassFilterEn	1
6	SSCRemoveEn	1
7	NoiseFloorDeembedEn	0
8	JitterSpec	2.00E-13
9	PassFail	Pass
10	rmsMax	7.91E-14
11	ToolVersion	CJT 5.0.1 Command
12	Date	8/6/2021 11:12

## 4.5 Clock Jitter Tool Command and Information

With the corrected configuration, the result and information are shown in [Figure 4-5](#).

**Figure 4-5. Command Line Usages and Examples**



```

c:\Program Files\ClockJitterTool\application>ClockJitterTool "c:\Users\[redacted]\Downloads\[redacted]\
5GBW.bin" 0 5 1 1 0 1
Sampling step is 12.500 ps
Base frequency is 99.835 MHz
Max cycle to cycle jitter (from original clock waveform) is 11.024 ps
Additional FIR Low Pass Filter is enabled; Bandwidth is 1.890 GHz
Swing is 0.860 V
Number of rising edges is 99763
Transfer Functions Generated; Total 16 combinations
SSC frequency is 33.024 KHz
Jitter table is delivered; after CDR, Max Phase Jitter (at row 3 column 3) is 7.9069e-14 RMS
.csv report saved; Same name & same folder with clock waveform

c:\Program Files\ClockJitterTool\application>

```



# A Tips for Measurement with Real-Time Oscilloscopes

## A.1 Recommended Test Probes and Fixtures for Phase Jitter Measurement

**Table A-1. Recommended Test Cables**

REFCLK	SubMiniature Push-on (SMP) Cables <sup>1, 2, 3</sup>
PCIe* 6.0 <sup>4</sup>	Yes
PCIe* 5.0 <sup>4</sup>	Yes
PCIe* 4.0	Yes
PCIe* 3.0	Yes
PCIe* 2.0	Yes
PCIe* 1.0	Yes

**Notes:**

1. In this connection, the clock swing will be almost half of the values measured by active probes, which is caused by the 50-ohm termination in the oscilloscope.
2. The Clock Jitter Tool 6.0.1 is mainly to validate the PCIe\* 6.0 REFCLK. SMP cables are recommended for all generation testing.
3. See "System Board Reference Clock (100 MHz) Jitter Test" in the *PCI Express Architecture PHY Test Specification Revision 6.0* for low-loss cable requirements (<https://members.pcisig.com/wg/PCI-SIG/document/16189>).
4. Low-loss cables are recommended for REFCLK tests for these versions. The active probe is strongly not recommended for clock tests for these versions.
  - a. The jitter of the active probe itself increases the measurement error, which may cause the result to fail.
  - b. When the jitter from the active probe is significant (compared with the jitter from the clock source), the process of the de-embedding NF would not be feasible mathematically, which may cause invalid test results.

**Table A-2. Recommended Fixture**

PCIe* Interface	Fixture
PCIe* Card Electromechanical (CEM) Slot	PCIe* CEM Compliance Load Board (CLB)

## A.2 Oscilloscope Requirements and Setting

Keep the same oscilloscope setting for clock phase jitter and NF waveform measurement.

Here are the supported formats:

- .bin
- .wfm
- .trc
- .csv

PCIe\* 6.0 clock waveforms are applicable to PCIe\* 6.0, 5.0, 4.0, 3.0, 2.0, or 1.0 phase jitter analysis.

**Table A-3. Recommended Measurement Settings**

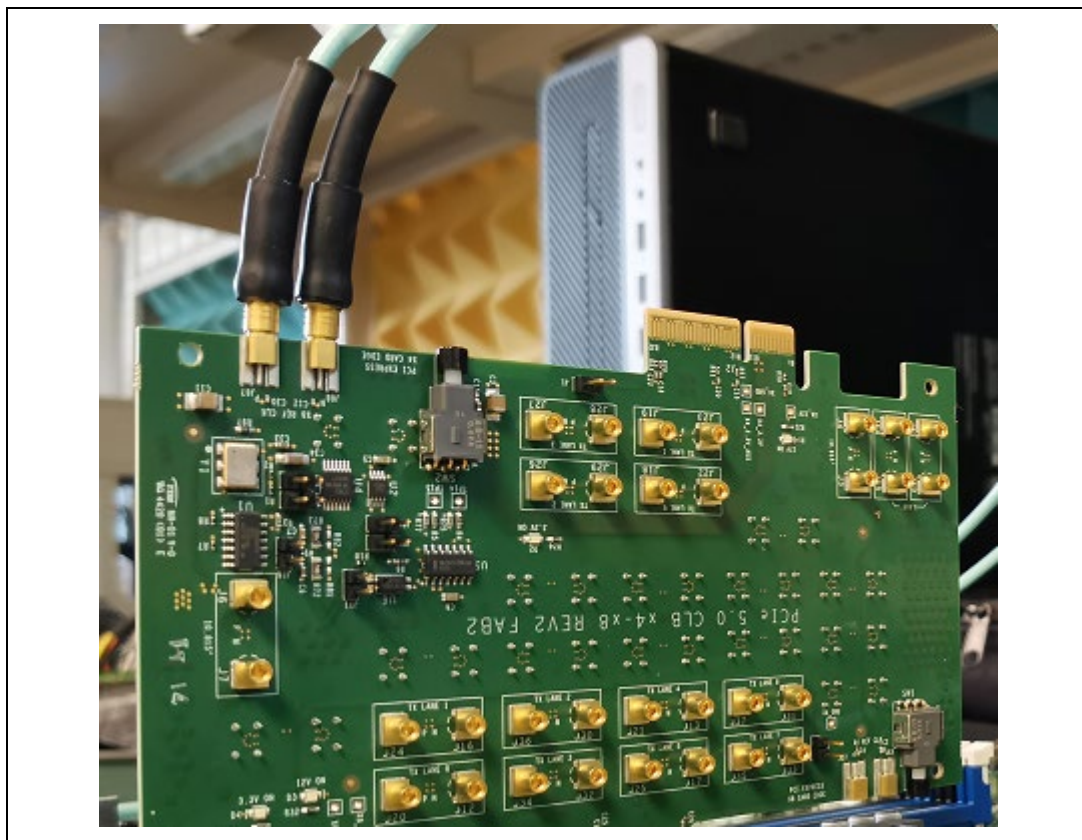
Oscilloscope Setting	Requirement	Notes
Bandwidth	5 GHz	Both oscilloscope and probes/cables need to meet the bandwidth limit.
Waveform length	80K clock cycles	A longer waveform will provide more accurate frequency steps after fast-Fourier transformations, and result in a better jitter resolution.
Minimum sampling rate (Maximum sampling step)	$\geq 20$ GSa/s ( $\leq 50$ ps per step)	Keep enough sampling points on the rising edge for the accurate crossing points.
Sampling mode	Real-time	N/A
Vertical scale	80 to 90% of the oscilloscope screen	Enable analog-digital converter precision with as many bits as possible.
No Clock-Data Recovery (CDR), interpolation, or other post-processes in the oscilloscope	Disable all post-processing of the oscilloscope	Decrease the additional jitter impact from the oscilloscope.

## A.3 Capture the Clock Waveform

Follow these steps:

1. Install the CLB to the PCIe\* slot on Unit under Test (UUT).
2. Connect the SMP cable from the oscilloscope to the CLB clock channels.
3. Capture the clock waveforms.

**Figure A-1. Clock - SMP Cable Connected to the CEM CLB Fixture**



## A.4 Capture NF Waveform

Follow these steps:

1. Detach the SMP cables from the CLB.
2. Terminate the SMP cables with 50 ohms.
3. Capture the NF waveform.

**Figure A-2. NF - SMP Cable Terminated with 50 ohms**

