An Introduction to Dynamic Temperature Range

White Paper

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Revision History

Date	Revision	Description
February 2024	1.0	Initial Release.

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1.0 Introduction

1.1 Purpose

The purpose of this document is to provide additional details on the Dynamic Temperature Range (DTR) specification for Intel® processors and chipsets.

1.2 Intended Audience

This document is targeted at the following audience:

- Original Equipment Manufacturers (OEMs)
- Original Design Manufacturers (ODMs)
- Independent Hardware Vendors (IHVs)
- System Integrators (SIs)

1.3 Acronyms and Terminology

Table 1. Acronyms and Terminology

Term	Description
°C	Degree Celsius
DTR	Dynamic Temperature Range
DTS	Digital Temperature Sensor
IHV	Independent Hardware Vendor
ODM	Original Design Manufacturer
OEM	Original Equipment Manufacturer
PCI	Peripheral Component Interconnect
PCIe*	PCI Express*
S0	ACPI System State S0
S5	ACPI Sleep State S5

Term	Description
SI	System Integrator
T_A	Ambient Temperature
T_{A_max}	Maximum Ambient Temperature
T_{BOOT}	Boot Temperature
T_C	Case Temperature
$T_{junction}$ / T_J	Silicon Junction Temperature
T_{J_max}	Maximum Silicon Junction Temperature
T_{J_min}	Minimum Silicon Junction Temperature

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2.0 Dynamic Temperature Range

2.1 Introduction

Dynamic Temperature Range (DTR) is the range of Junction Temperature (T_J) starting from boot (T_{BOOT}) and transitioning Cold-to-Hot (T_{BOOT} + DTR) and/or Hot-to-Cold (T_{BOOT} - DTR). For a single operational cycle, the processor executes at full data sheet performance across the full DTR without requiring a cold reset (S0 to S5 to S0 state transition) or power cycle.

No autonomous actions are taken by a processor or chipset based on the DTR. The DTR must be reset through a platform-initiated power cycle or cold reset.

Figure 1 shows different scenarios when DTR = ± 70 °C. The DTR is the worst case (smallest) when the processor boots at T_{J_min}. A processor that boots at Room Temperature has a wider DTR since it covers down to T_{J_min} and up-to T_{BOOT} + 70 °C. A processor that boots between (T_{J_max} – DTR) and maximum ambient temperature (T_{A_max}) is the best case (widest) DTR since it covers the entire T_J range.

Figure 1. DTR at Different Boot Temperatures: DTR = ±70 °C

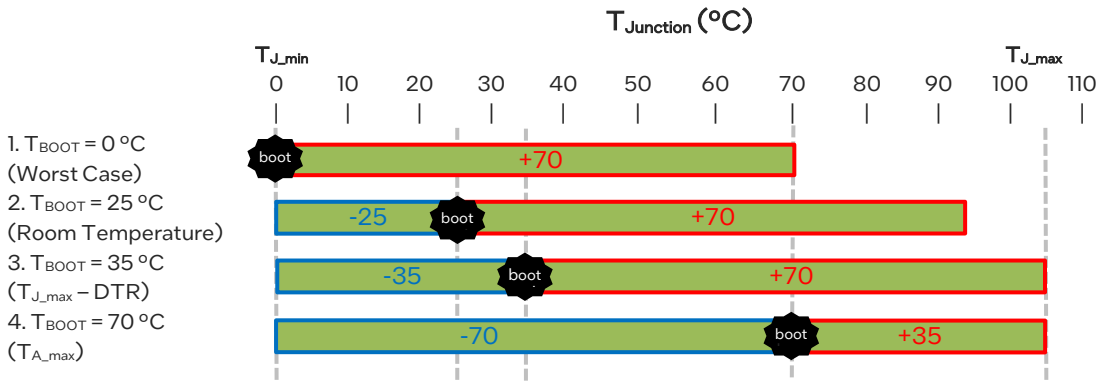
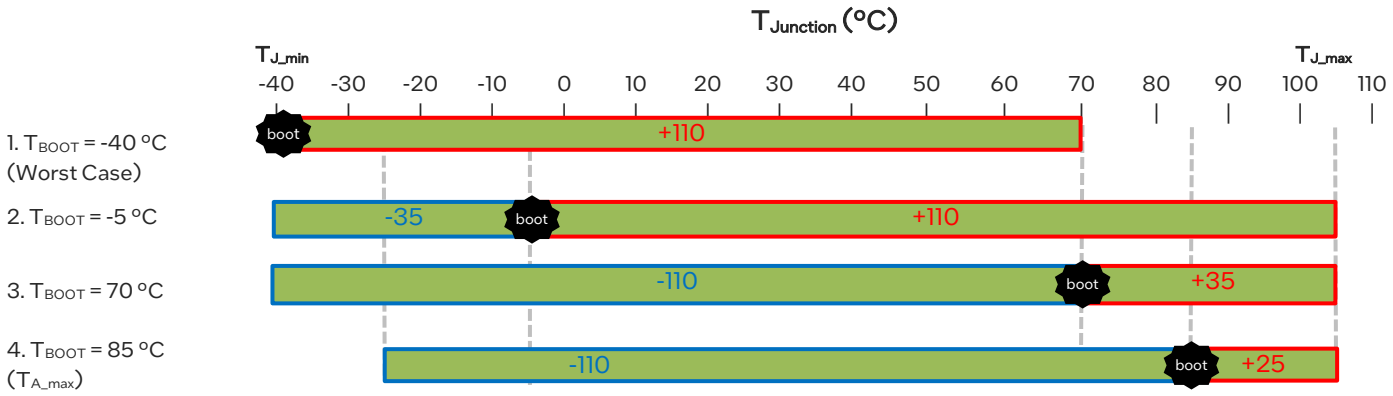


Figure 2, shows different scenarios when DTR = ± 110 °C. The DTR is the worst case (smallest) when the processor boots at T_{J_min}. A processor that boots between -5 °C and 70 °C has a best case (widest) DTR since it covers down to T_{J_min} and up-to T_{J_max}. A processor that boots at maximum ambient temperature (T_{A_max}) has a narrower DTR since it does not cover down to T_{J_min}.

Figure 2. DTR at Different Boot Temperatures: DTR = ±110 °C



2.2 DTR Specification

If a DTR specification exists for a processor or chipset, it may be available in the corresponding datasheet.

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3.0 Frequently Asked Questions (FAQs)

3.1 Will the processor or chipset start throttling if DTR is exceeded?

No autonomous actions are taken by the processor or chipset even if Dynamic Temperature Range (DTR) is exceeded.

3.2 What may happen when the DTR is exceeded?

When a processor or chipset violates the Dynamic Temperature Range (DTR) specification, the platform may exhibit unpredictable behavior. This behavior may include (but not limited to) a system hang, display corruption or High Speed I/O (PCI Express*, for example) link instability and may vary between different processors or between a cold reset/power cycle of the same processor.

3.3 What do I need to do if DTR is exceeded?

Intel recommends resetting the processor or chipset through a platform-initiated power cycle or cold reset.

3.4 How does resetting the processor or chipset solve DTR violation?

Once a platform-initiated power cycle or cold reset is performed, T_{BOOT} will be the new temperature at time of reset. This temperature is different from the previous T_{BOOT}, and hence the DTR is reset based on the new T_{BOOT} temperature.

3.5 Is DTR part of thermal design requirement?

DTR is not a thermal design requirement, meaning it is not mandatory to design a heatsink solution to meet DTR.

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