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INTEL AGILEX® 7 FPGA I-SERIES, AGI027 4 X F TILE TRANSEIVER -SOC DEVKIT

NOTES :

1. PROJECT DRAWING NUMBERS:

RAW PCB	100-0330690-C1
GERBER FILES	110-0330690-C1
PCB DESIGN FILES	120-0330690-C1
ASSEMBLY DRAWING	130-0330690-C1
FAB DRAWING	140-0330690-C1
SCHEMATIC DRAWING	150-0330690-C1
PCB FILM	160-0330690-C1
BILL OF MATERIALS	170-0330690-C1
SCHEMATIC DESIGN FILES	180-0330690-C1
FUNCTIONAL SPECIFICATION	210-0330690-C1
PCB LAYOUT GUIDELINES	220-0330690-C1
ASSEMBLY REWORK	320-0330690-C1

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04	04- CLOCK TREE DIAGRAM	54	54- CLOCK - ZL30733 -1
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29	29- DDR4 HPS COMP-1	79	79- PWR VCCL -3
30	30- DDR4 HPS COMP-2	80	80- PWR P0V8_G1
31	31- DDR4 HPS COMP-3	81	81- PWR VCC_HSSI_U1X_G1
32	32- DDR4 DIMM-2A	82	82- PWR VCC_HSSI_U2X_G1
33	33- DDR4 DIMM-2B	83	83- PWR VCERT1_13A/13C
34	34- DIMM PWR FLT	84	84- PWR VCERT2_U20/U22
35	35- USB3.X/DP MUX	85	85- PWR VCERT_UX_GDR
36	36- SDI BNC	86	86- PWR P1V5_G2/P2V5_G2
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39	39- QSFP-DD CONN 1	89	89- PWR P1V2_IO
40	40- QSFP-DD-800 CONN	90	90- PWR P1V8_G3
41	41- FMC+_A -1	91	91- PWR VCCH_SDM/P1V0_G2
42	42- FMC+_A -2	92	92- PWR LOAD SWITCHES
43	43- FMC+_B-1	93	93- PWR DDR4 VTT
44	44- FMC+_B-2	94	94- PD CONTROLLER
45	45- USB2.0	95	95- BLANK PAGE
46	46 - SMA		
47	47- PWR MAX10 -1		
48	48- PWR MAX10 -2		
49	49- SYS MAX10 -1		
50	50- SYS MAX10 -2		

REVISION HISTORY

[illegible]

LEVEL	MMID	99CA2X
0	TA	N22854-001
1	ASSY	N24091-200
2	PB	M77505-001
3	ALL ADD ON BOARDS AND ACCESSORIES	NA

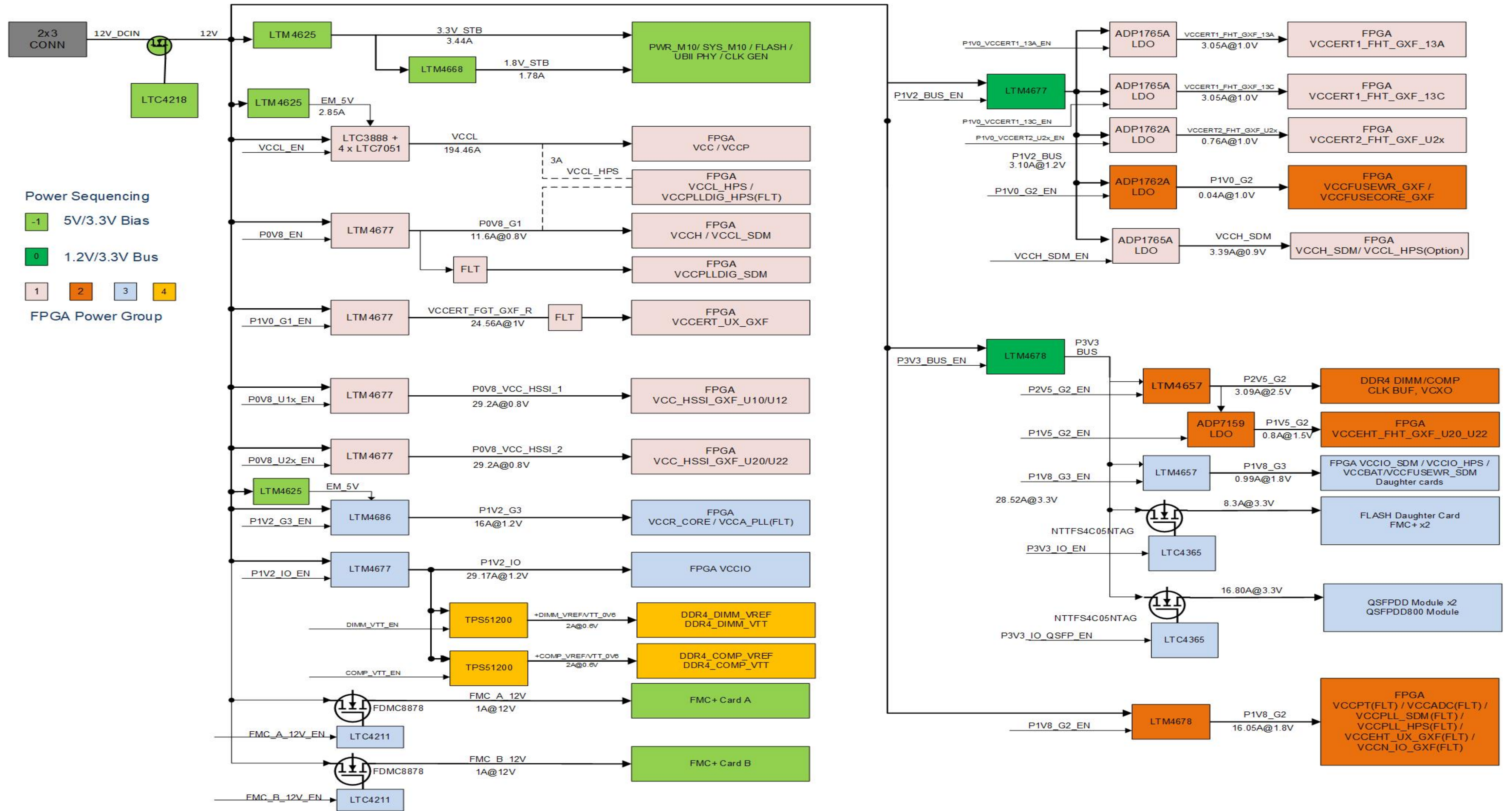
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A

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POWER TREE



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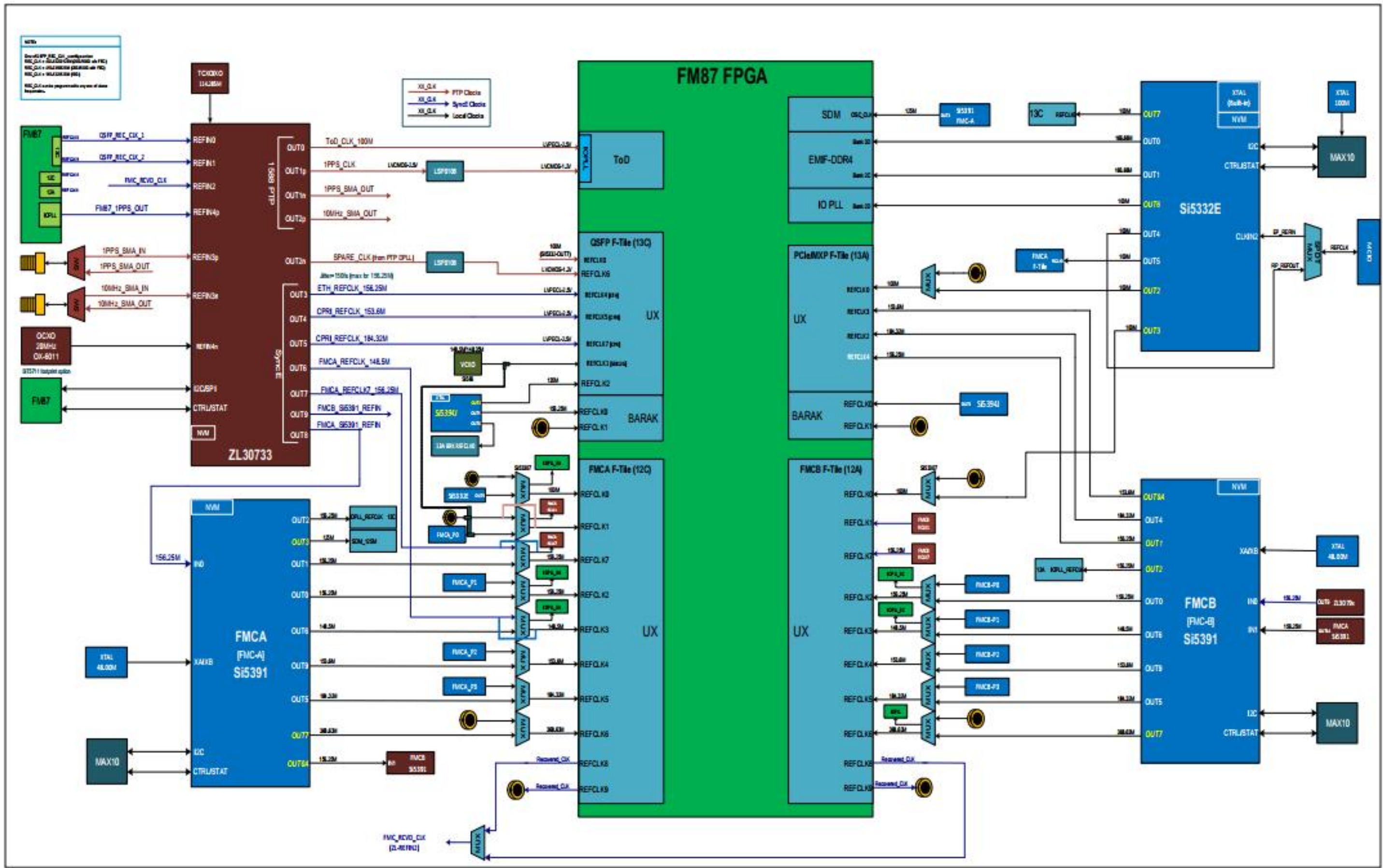
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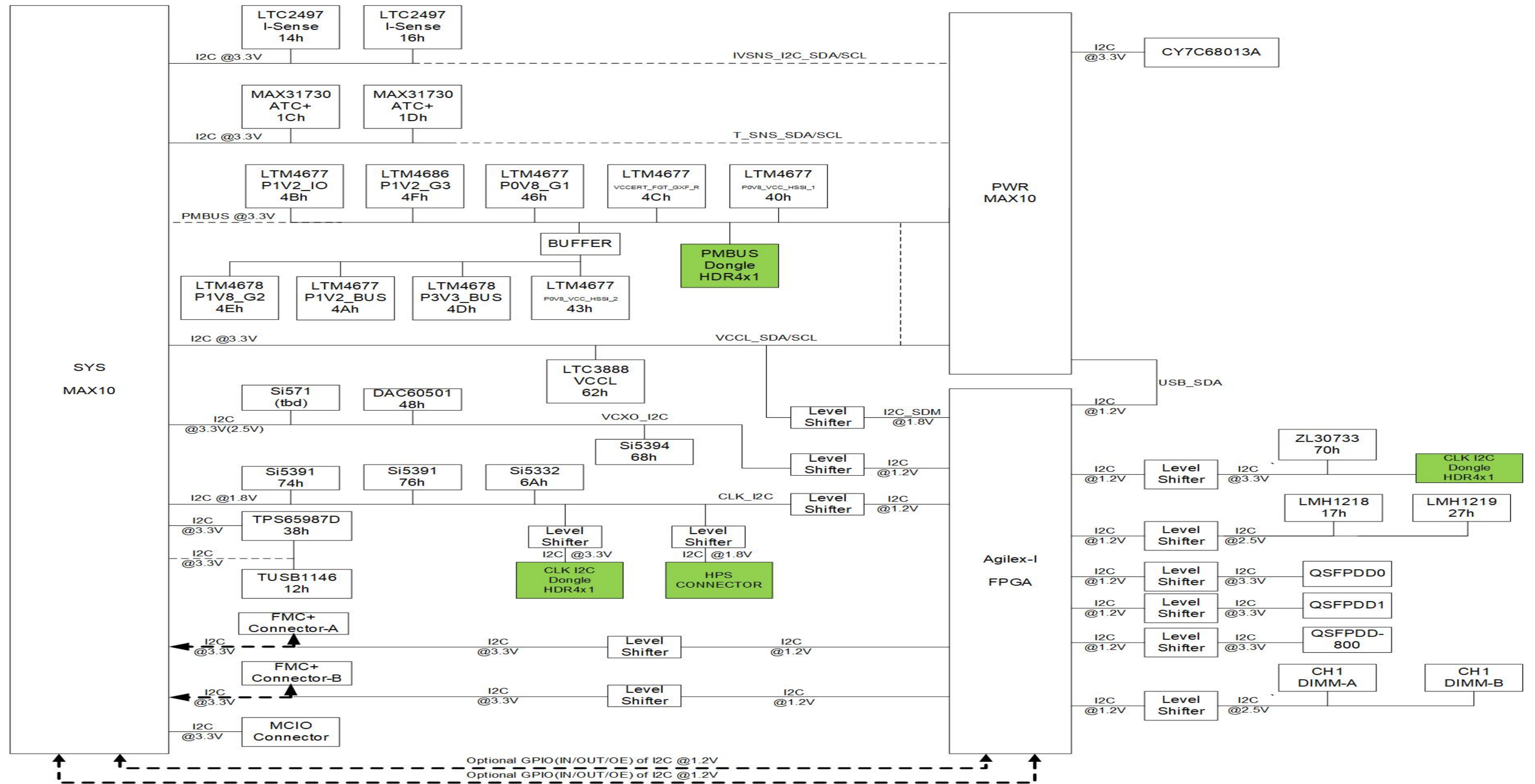
CLOCK TREE



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I2C TREE

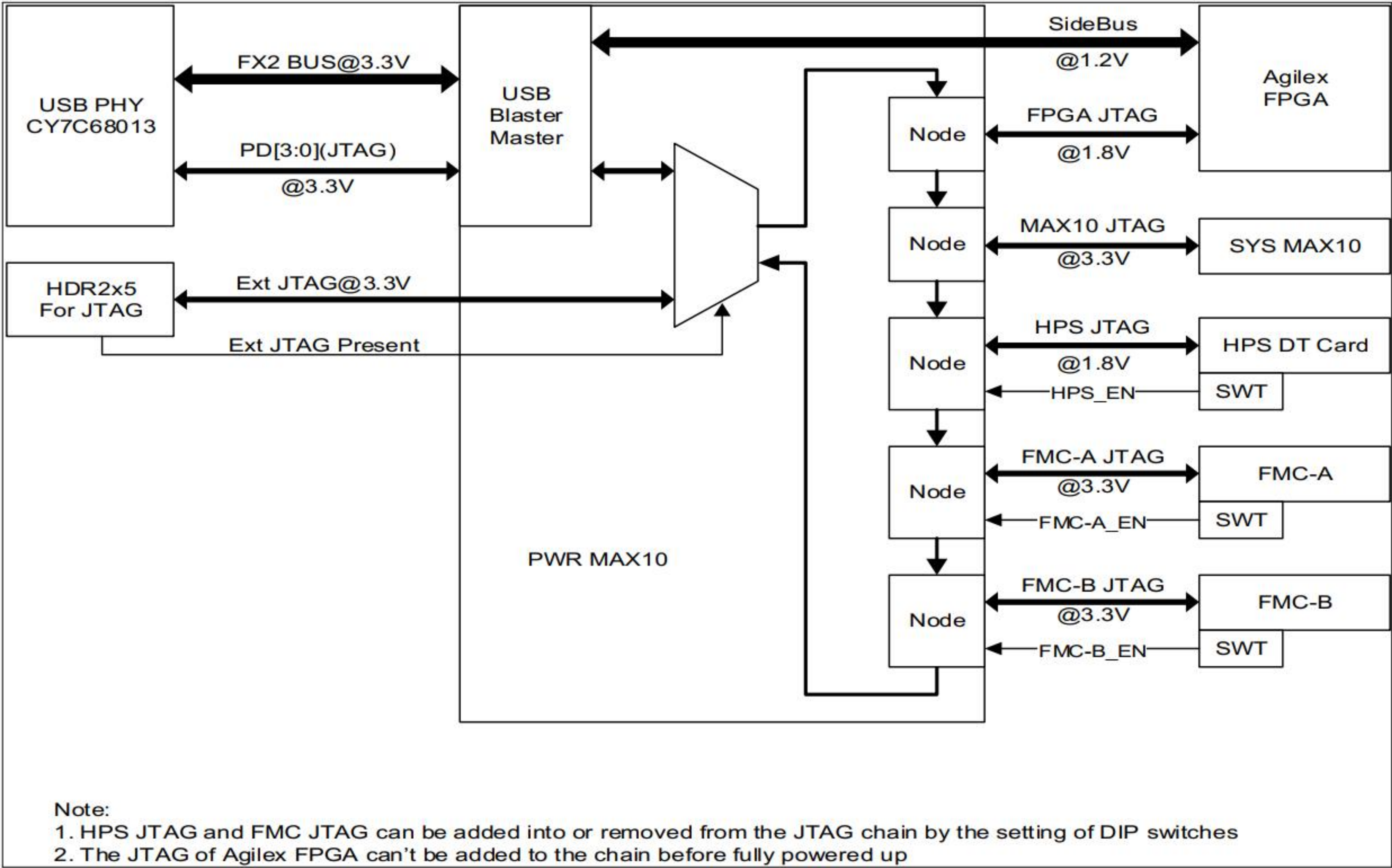


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JTAG TOPOLOGY



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SDM IO MAPPING

CONFIGURATION MODE		MSEL[2:0]
PASSIVE	AVSTX32	000
	AVSTX16	101
	AVSTX8	110
	JTAG	111
	CVP	001
ACTIVE	AS - FAST	001
	AS - NORMAL	011

SDM PINS	MSEL FUNCTIONS	CONFIGURATION SOURCE FUNCTION			
		AVSTX8	AS	AVSTX16	AVSTX32
SDM_IO0		PWR_SCL	PWR_SCL	PWR_SCL	PWR_SCL
SDM_IO1		DATA2	DATA1		
SDM_IO2		DATA0	CLK		
SDM_IO3		DATA3	DATA2		
SDM_IO4		DATA1	DATA0		
SDM_IO5	MSEL0	HPS_CRSTN	NCS00		
SDM_IO6		DATA4	DATA3		
SDM_IO7	MSEL1		NCS02		
SDM_IO8		READY	NCS03		
SDM_IO9	MSEL2		NCS01		
SDM_IO10		DATA7			
SDM_IO11		VALID	HPS_CRSTN	HPS_CRSTN	HPS_CRSTN
SDM_IO12		PWR_SDA		PWR_SDA	PWR_SDA
SDM_IO13		DATA5			
SDM_IO14		CLK			
SDM_IO15		DATA6	RESETN		
SDM_IO16		CFG_DONE	CFG_DONE	CFG_DONE	CFG_DONE

SYSTEM MAX IS THE SOURCE OF HPS_CRSTN FUNCTION

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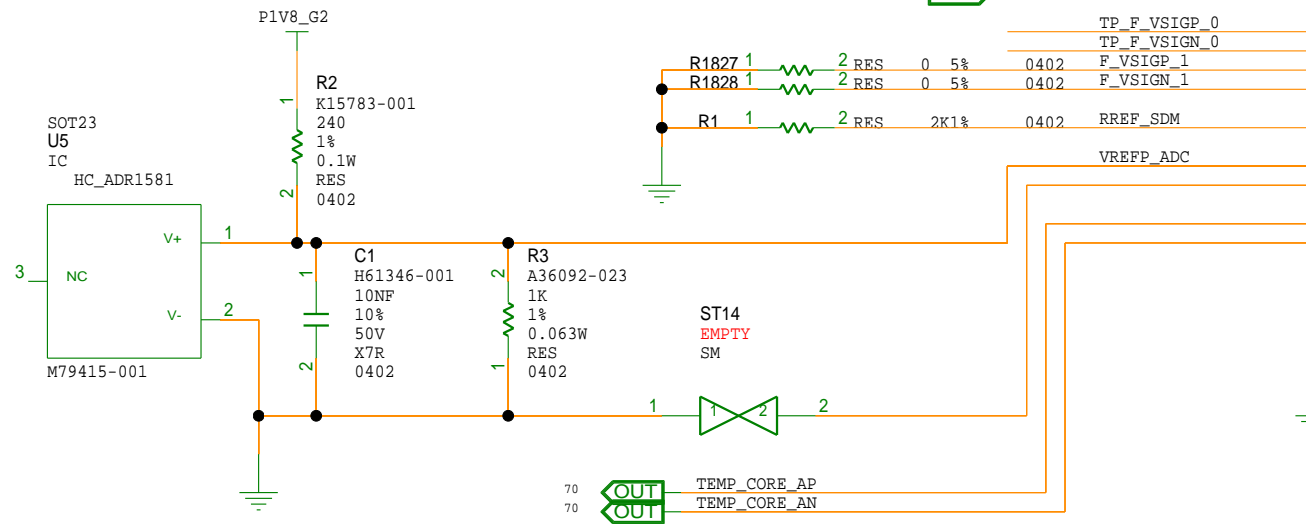
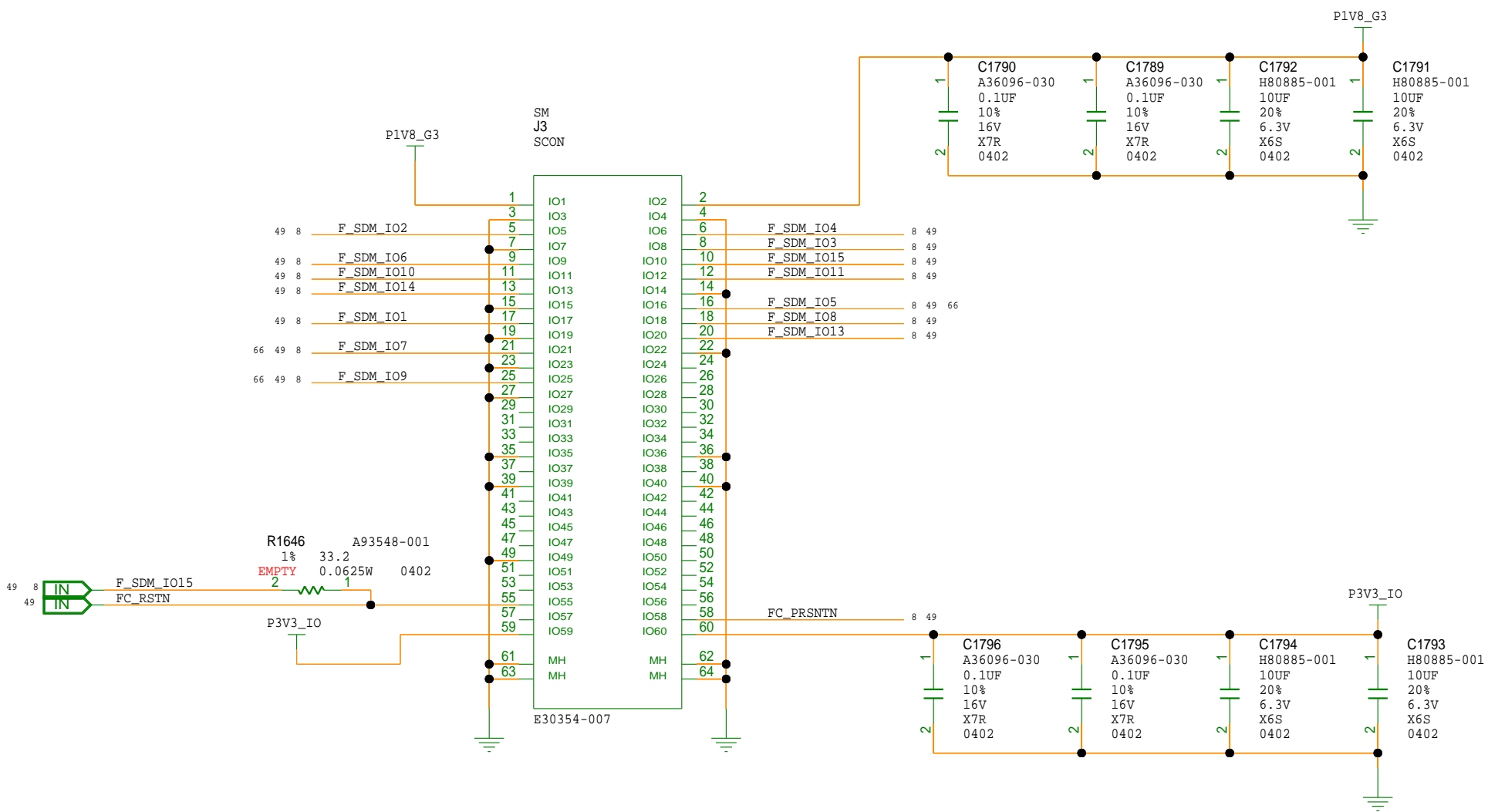
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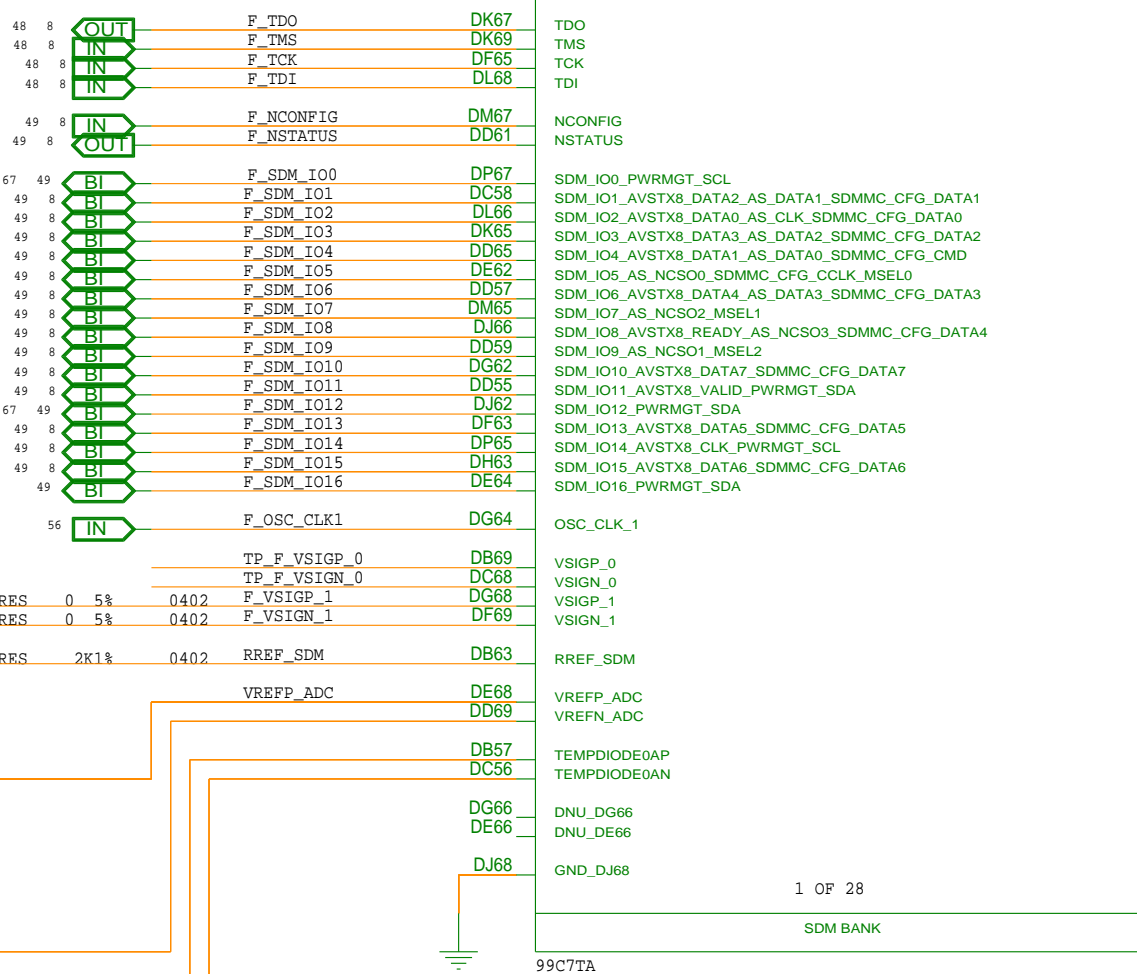


FPGA SDM

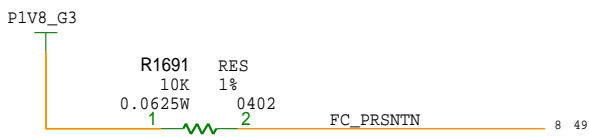
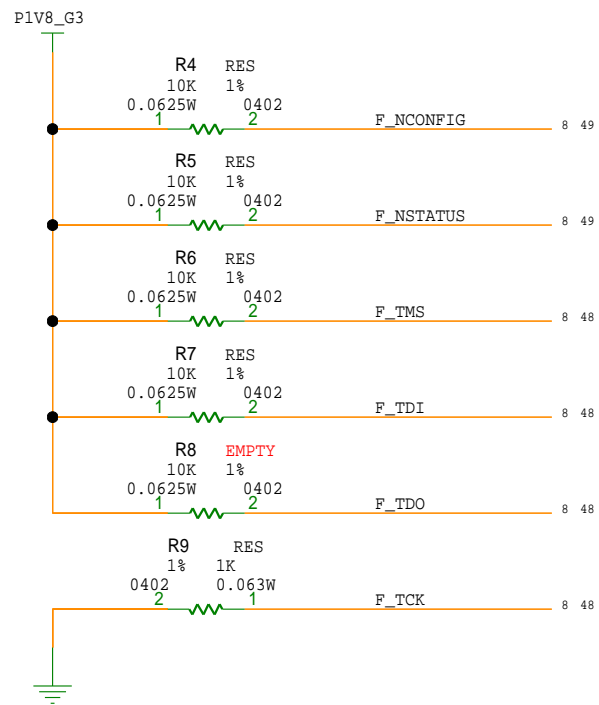
U1

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HC_FM87_3184B_FHBE



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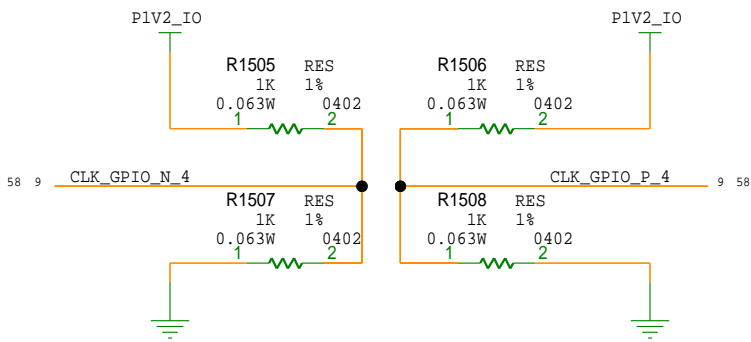
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BIT-SWAPPINGS ALLOWED WITHIN A BYTE.
BYTE-SWAPPING IS ALLOWED WITH PRIOR APPROVAL
FROM DESIGN ENGINEER

FPGA BANK 2D

U1
EMPTY

HC_FM87_3184B_PHB



CAD NOTE:
PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA

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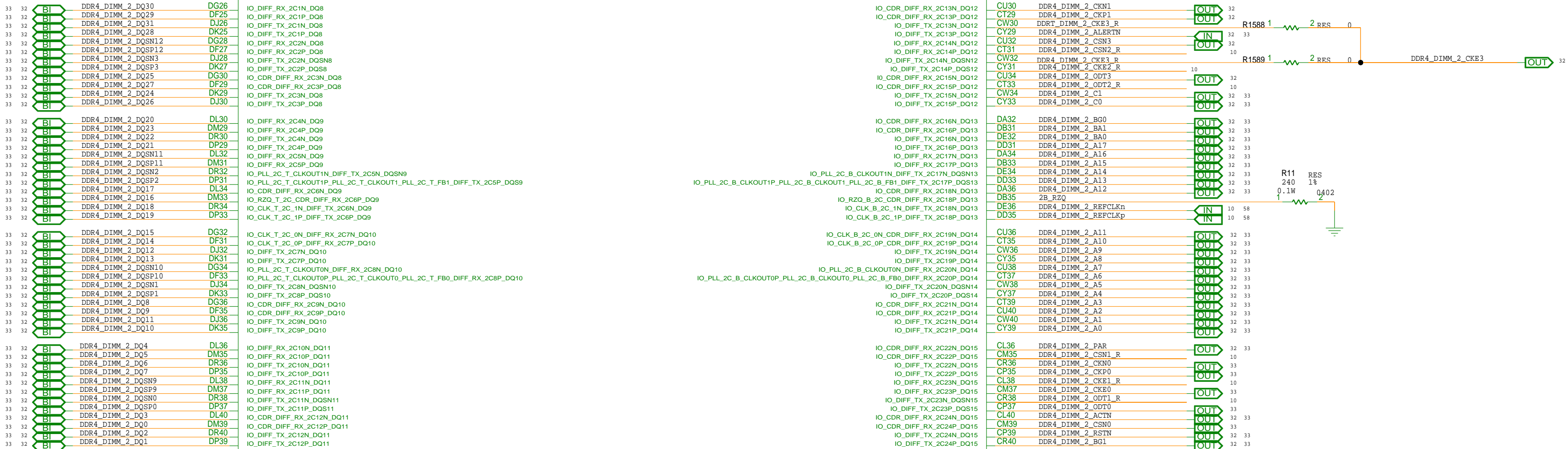
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FPGA BANK 2C

U1
EMPTY

HC_FM87_3184B_PHB6



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FPGA BANK 2F

U1

EMPTY

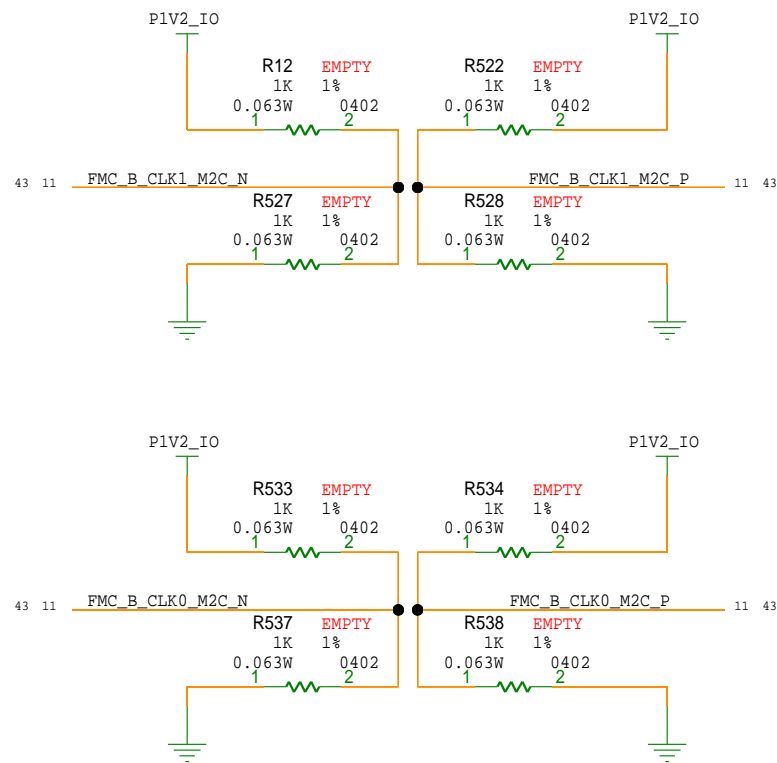
HC_PM87_3184B_PHB6

43	[BI]	FMC_B_LA_N12	DG38	IO_DIFF_RX_2F1N_DQ16
43	[BI]	FMC_B_LA_P12	DF37	IO_DIFF_RX_2F1P_DQ16
43	[BI]	FMC_B_LA_N7	DJ38	IO_DIFF_TX_2F1N_DQ16
43	[BI]	FMC_B_LA_P7	DK37	IO_DIFF_TX_2F1P_DQ16
43	[BI]	FMC_B_LA_N11	DC40	IO_DIFF_RX_2F1N_DQ20
43	[BI]	FMC_B_LA_P11	DF39	IO_DIFF_RX_2F2P_DQ16
43	[BI]	FMC_B_LA_N8	DJ40	IO_DIFF_TX_2F2N_DQS16
43	[BI]	FMC_B_LA_P8	DK39	IO_DIFF_TX_2F2P_DQS16
43	[BI]	FMC_B_LA_N5	DG42	IO_CDR_DIFF_RX_2F3N_DQ16
43	[BI]	FMC_B_LA_P5	DF41	IO_CDR_DIFF_RX_2F3P_DQ16
43	[BI]	FMC_B_LA_N22	DJ42	IO_DIFF_TX_2F3N_DQ16
43	[BI]	FMC_B_LA_P22	DK41	IO_DIFF_TX_2F3P_DQ16
43	[BI]	FMC_B_LA_N23	DL42	IO_DIFF_RX_2F4N_DQ17
43	[BI]	FMC_B_LA_P23	DM41	IO_DIFF_RX_2F4P_DQ17
43	[BI]	FMC_B_LA_N13	DR42	IO_DIFF_TX_2F4N_DQ17
43	[BI]	FMC_B_LA_P13	DP41	IO_DIFF_TX_2F4P_DQ17
43	[BI]	FMC_B_LA_N10	DL44	IO_DIFF_RX_2F5N_DQ17
43	[BI]	FMC_B_LA_P10	DM43	IO_DIFF_RX_2F5P_DQ17
43	[BI]	FMC_B_LA_N9	DR44	IO_PLL_2F_T_CLKOUT1N_DIFF_TX_2F5N_DQS17
43	[BI]	FMC_B_LA_P9	DP43	IO_PLL_2F_T_CLKOUT1P_PLL_2F_T_CLKOUT1P_PLL_2F_T_FB1_DIFF_TX_2F5P_DQS17
43	[BI]	FMC_B_LA_N14	DL46	IO_CDR_DIFF_RX_2F6N_DQ17
43	[BI]	FMC_B_LA_P14	DM45	IO_R2Q_2F_2F_CDR_DIFF_RX_2F6P_DQ17
43	[BI]	FMC_B_CLK2_M2C_N	DR46	IO_CLK_B_2F_1N_DIFF_TX_2F6N_DQ17
43	[IN]	FMC_B_CLK2_M2C_P	DP45	IO_CLK_B_2F_1P_DIFF_TX_2F6P_DQ17
43	[IN]	FMC_B_CLK0_M2C_N	DG44	IO_CLK_T_2F_0N_DIFF_RX_2F7N_DQ18
43	[IN]	FMC_B_CLK0_M2C_P	DF43	IO_CLK_T_2F_0P_DIFF_RX_2F7P_DQ18
43	[IN]	FMC_B_SYNC_M2C_N	DK43	IO_DIFF_TX_2F7N_DQ18
43	[IN]	FMC_B_SYNC_M2C_P	DJ44	IO_DIFF_TX_2F7P_DQ18
43	[OUT]	FMC_B_REFCLK_C2M_N	DG46	IO_PLL_2F_T_CLKOUT0N_DIFF_RX_2F8N_DQ18
43	[OUT]	FMC_B_REFCLK_C2M_P	DF45	IO_PLL_2F_T_CLKOUT0P_PLL_2F_T_CLKOUT0_PLL_2F_T_FB0_DIFF_RX_2F8P_DQ18
43	[OUT]	FMC_B_SYNC_C2M_N	DJ46	IO_DIFF_TX_2F8N_DQS18
43	[OUT]	FMC_B_SYNC_C2M_P	DK45	IO_DIFF_TX_2F8P_DQS18
43	[OUT]	FMC_B_LA_N25	DG48	IO_CDR_DIFF_RX_2F9N_DQ18
43	[BI]	FMC_B_LA_P25	DF47	IO_CDR_DIFF_RX_2F9P_DQ18
			DJ48	IO_DIFF_TX_2F9N_DQ18
			DK47	IO_DIFF_TX_2F9P_DQ18
			DL48	IO_DIFF_RX_2F10N_DQ19
			DM47	IO_DIFF_RX_2F10P_DQ19
			DR48	IO_DIFF_TX_2F10N_DQ19
			DP47	IO_DIFF_TX_2F10P_DQ19
			DL50	IO_DIFF_RX_2F11N_DQ19
			DM49	IO_DIFF_RX_2F11P_DQ19
			DR50	IO_DIFF_TX_2F11N_DQS19
			DP49	IO_DIFF_TX_2F11P_DQS19
			DL52	IO_CDR_DIFF_RX_2F12N_DQ19
			DM51	IO_CDR_DIFF_RX_2F12P_DQ19
			DR52	IO_DIFF_TX_2F12N_DQ19
			DP51	IO_DIFF_TX_2F12P_DQ19

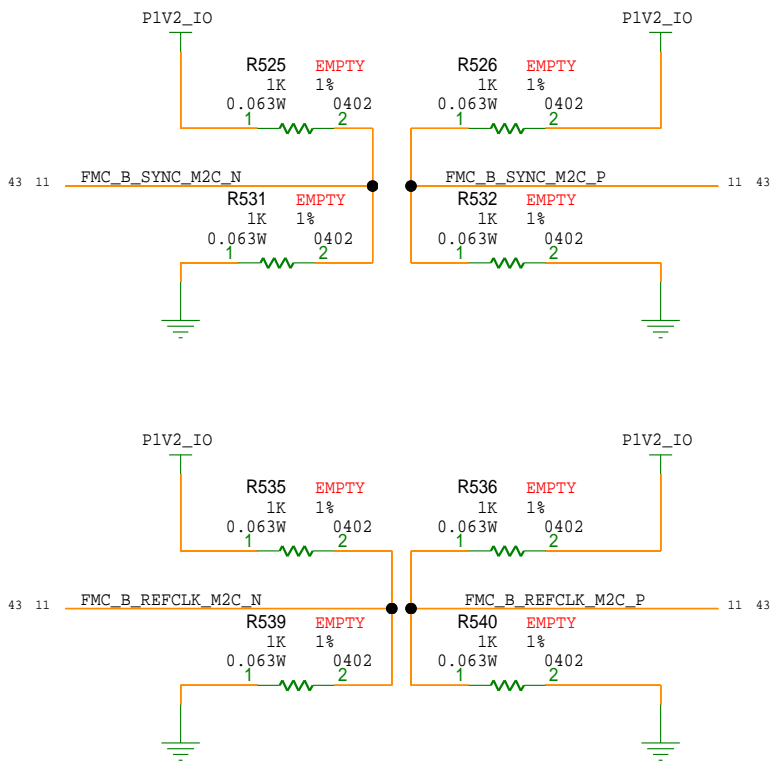
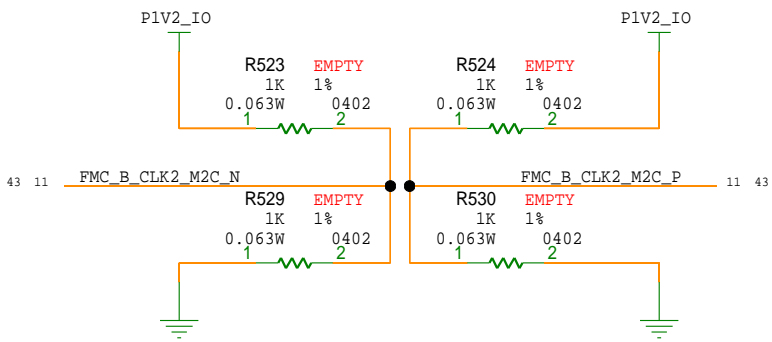
99C7TA

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IO BANK 2F



CAD NOTE:
PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA



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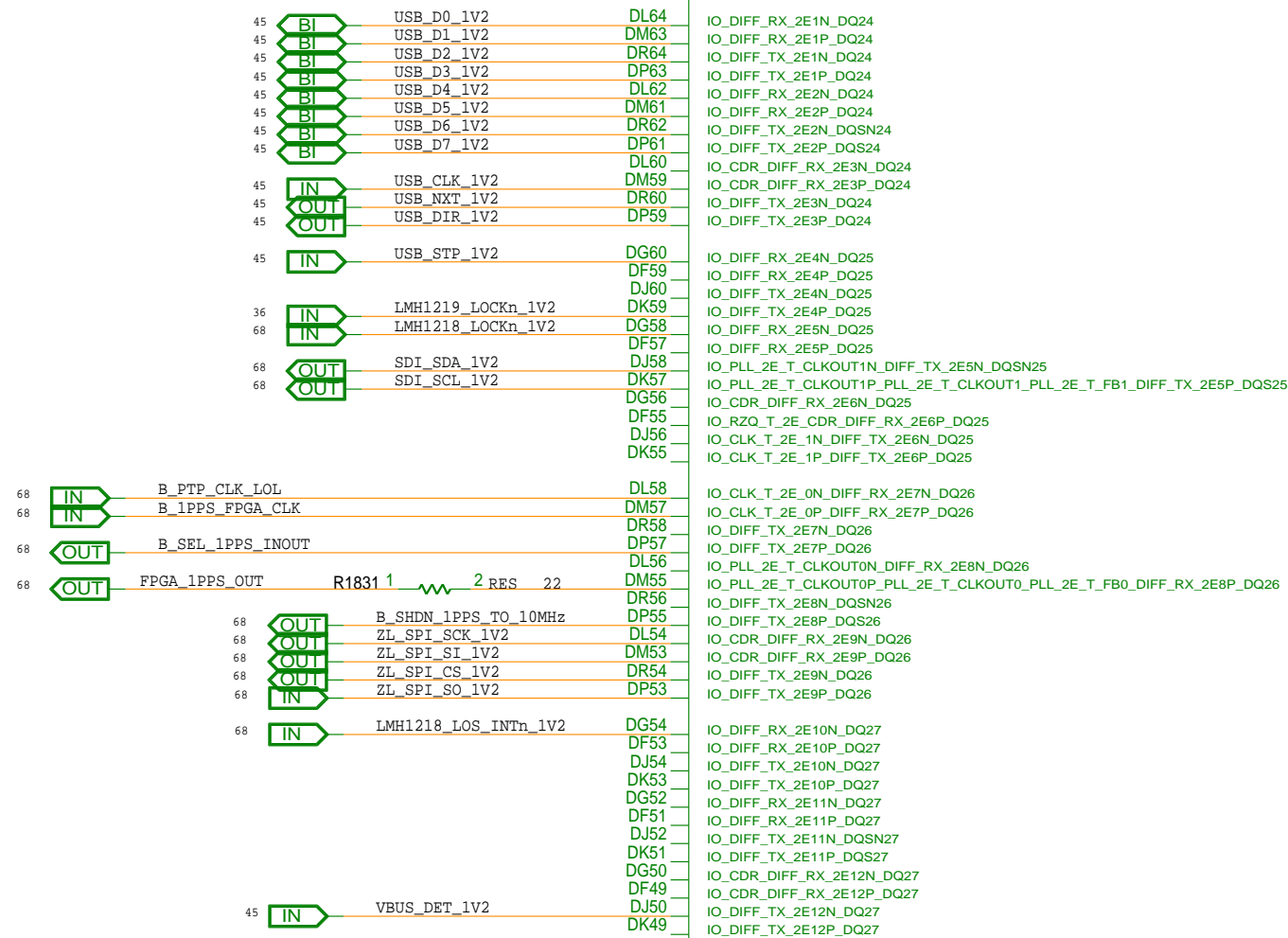
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FPGA BANK 2E

U1
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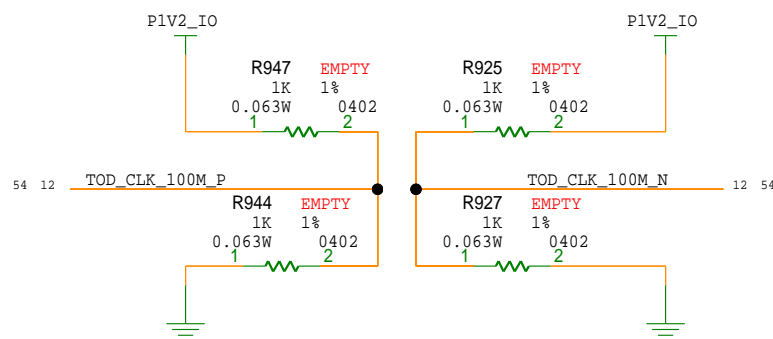
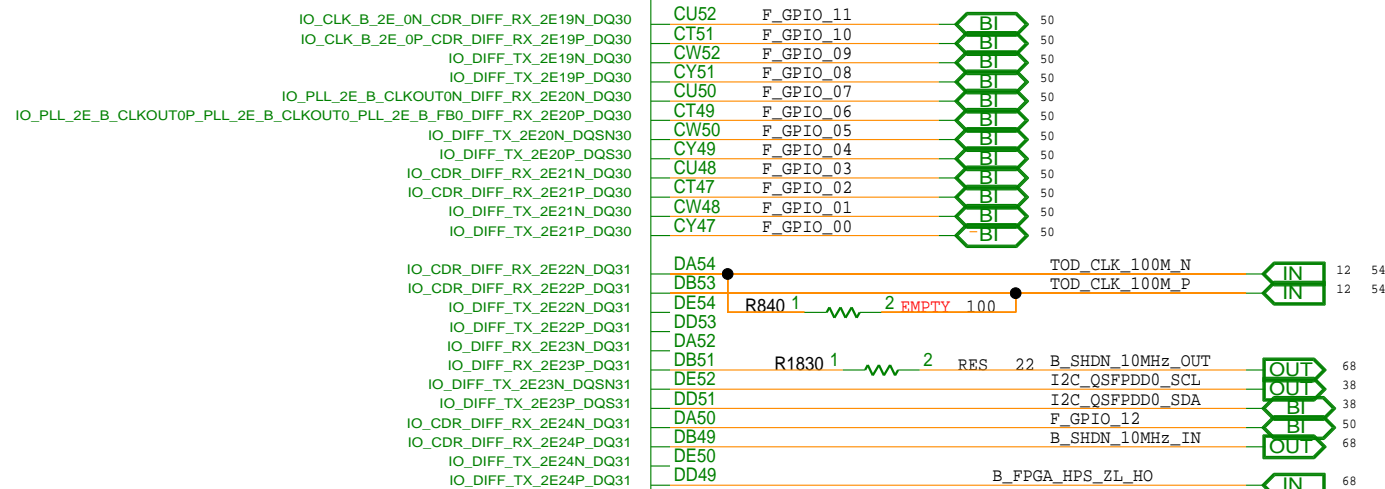
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IO BANK 2E

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DNU_CV53

CV53



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FPGA BANK 3D

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BIT-SWAPPINGS ALLOWED WITHIN A BYTE.

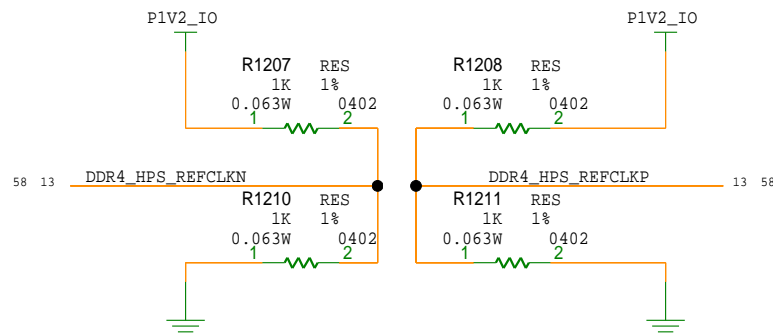
BYTE-SWAPPINGS IS ALLOWED WITH PRIOR APPROVAL

FROM DESIGN ENGINEER (EXCEPT ECC)

U1

EMPTY

HC_FM87_3184B_PHB8



CAD NOTE:

PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA

PLACE TE PAD ON THE TRACE

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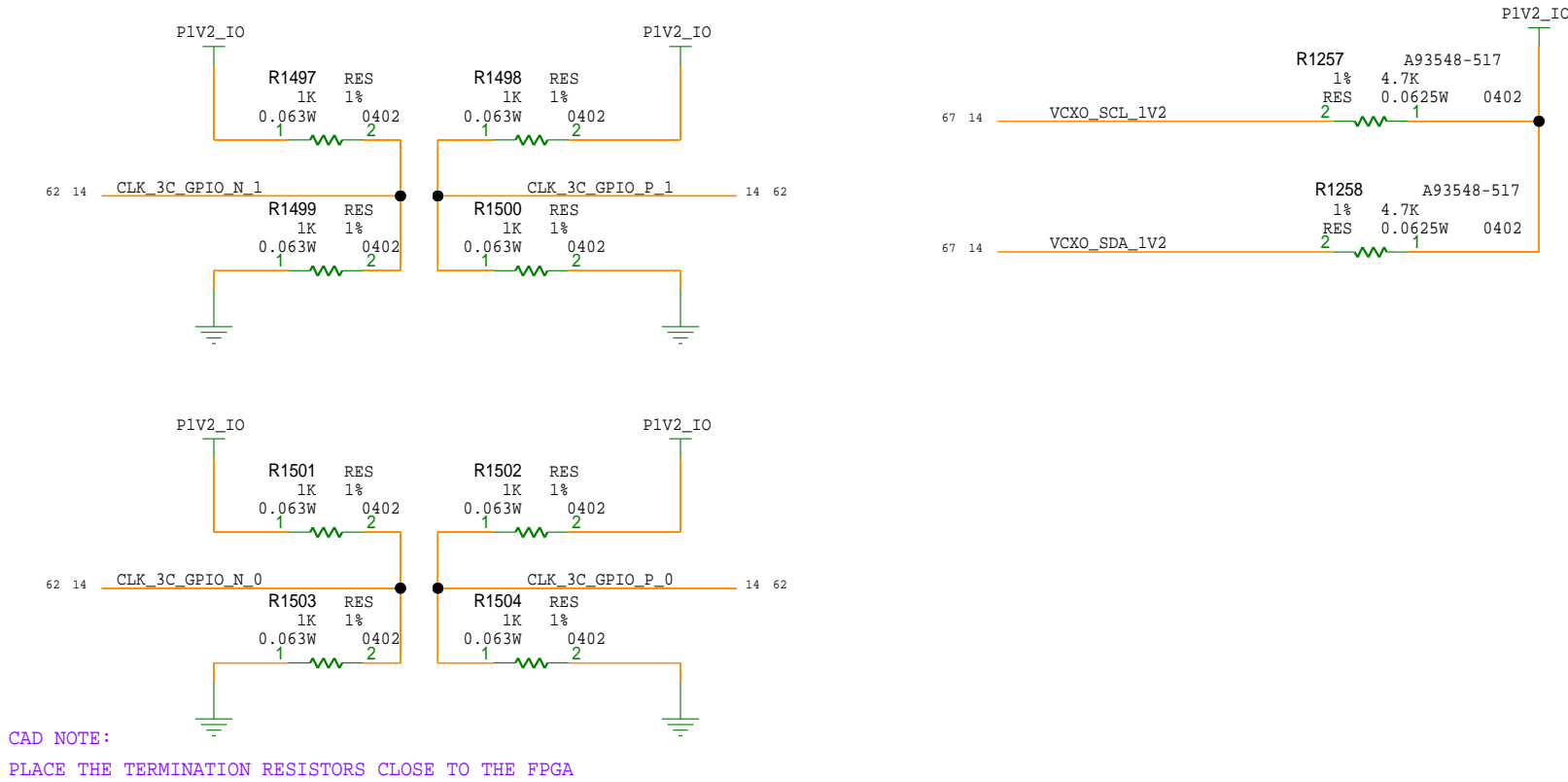
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FPGA BANK 3C

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EMPTY

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SCALE:

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FPGA BANK 3B

U1
EMPTY

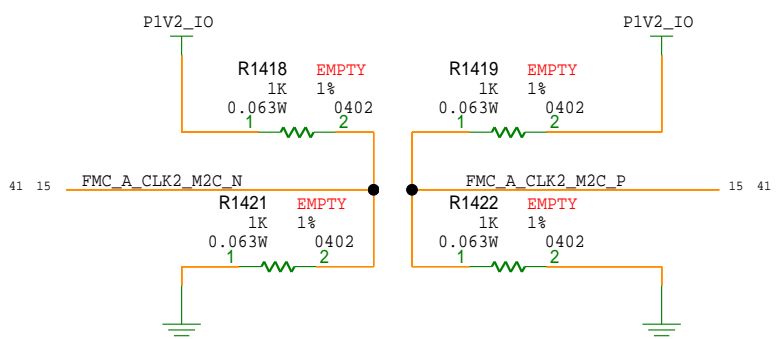
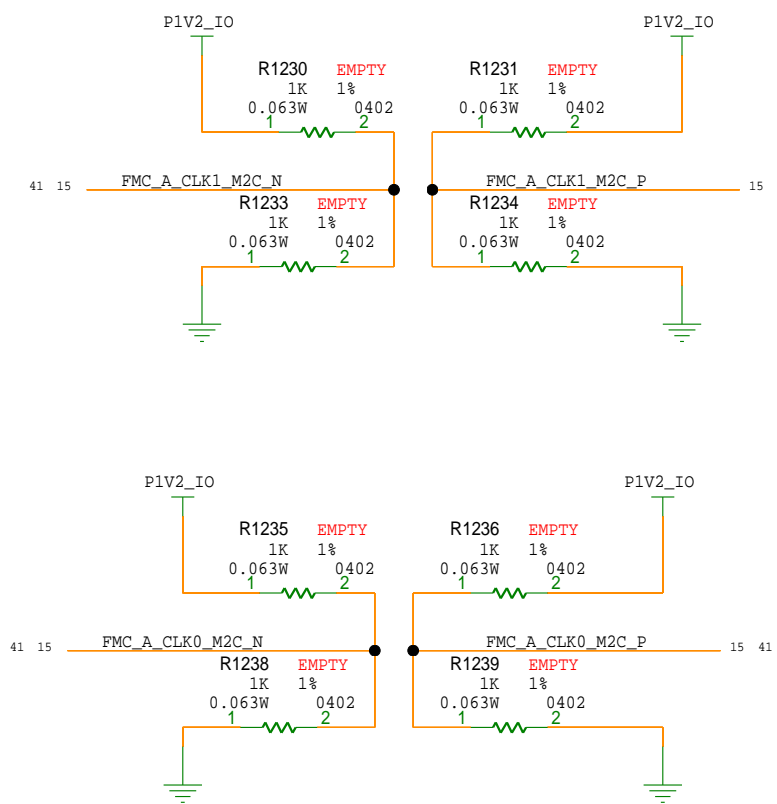
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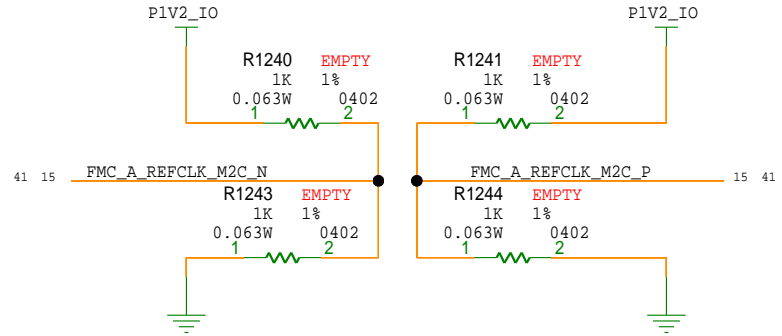
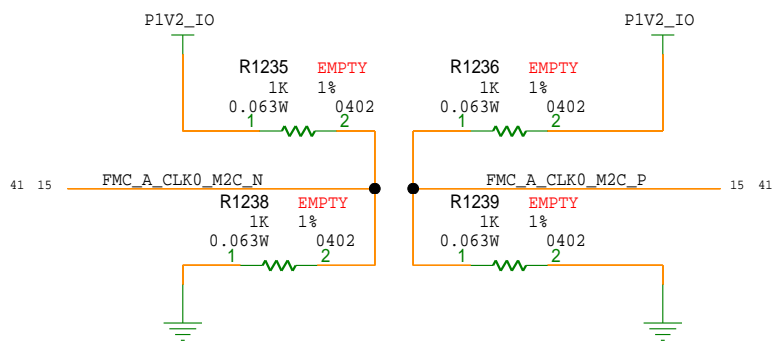
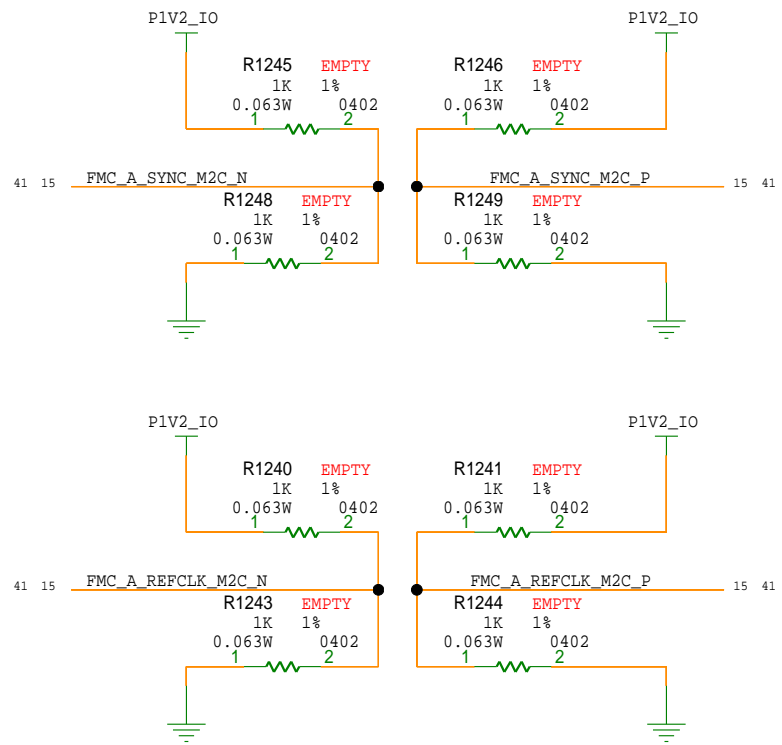
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IO BANK 3B

99C7TA



CAD NOTE:
PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA



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SCALE:

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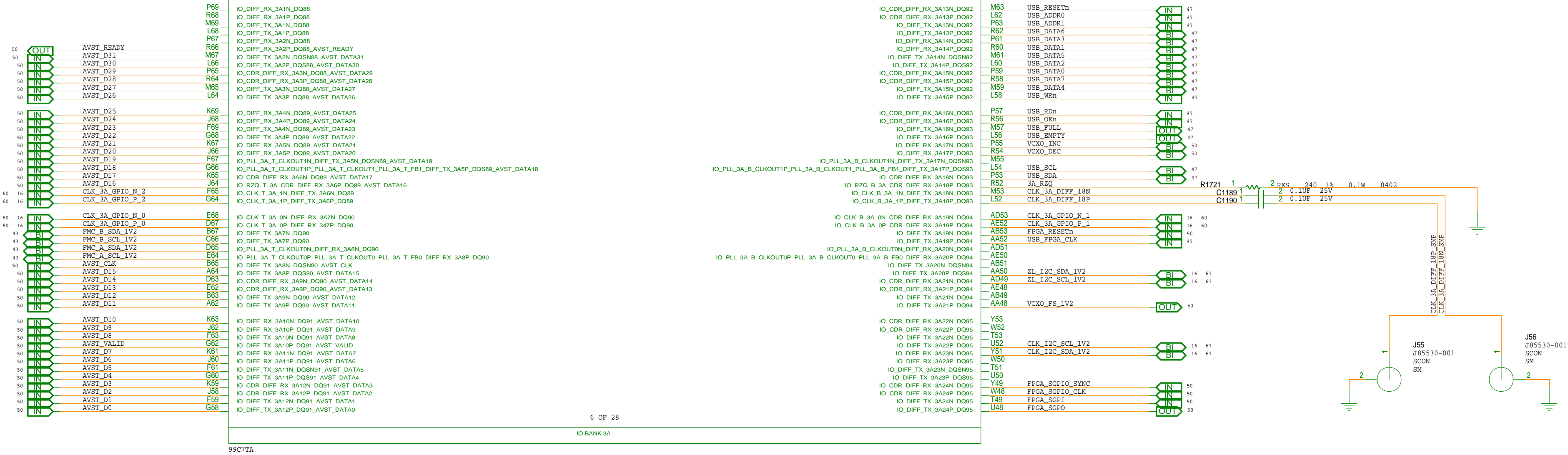
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FPGA NAME: 3A

U1

EMPTY

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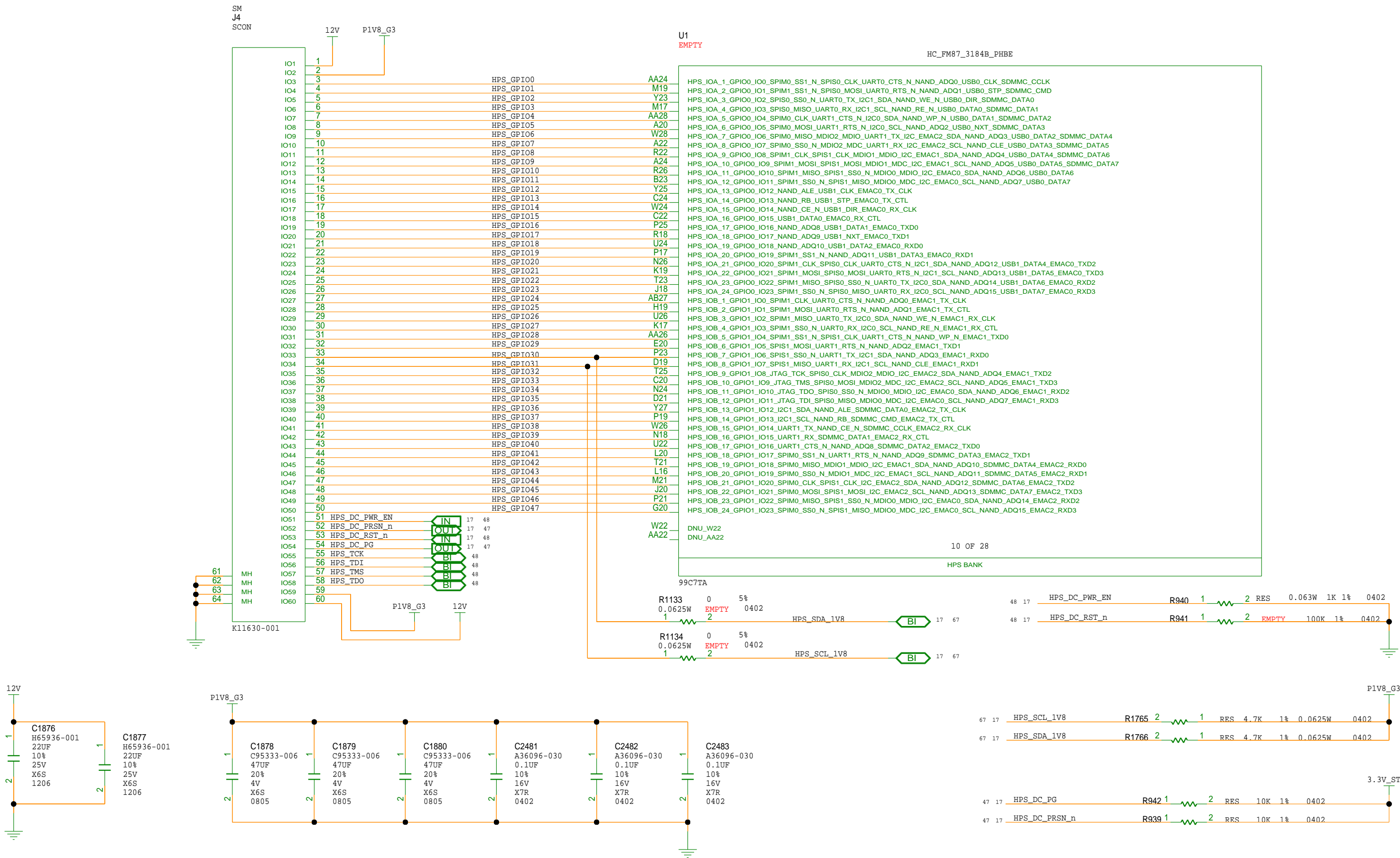
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HPS DAUGHTER CARD CONNECTOR



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Wed Feb 28 11:37:52 2024

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SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-C1

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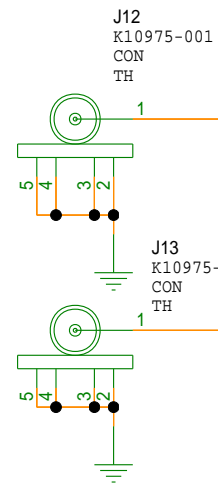
INTEL CONFIDENTIAL

CAD NOTE:
PLACE THESE 100-OHM RES RIGHT BELOW FPGA BALLS
ON THE BREAKOUT VIAS.



CAD NOTE: PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS.
FMC_A_RX*

CAD NOTE:
BREAK-OUT EVERY TP* NETS TO AN
EXPOSED PAD ON THE BOTTOM SIDE.



4

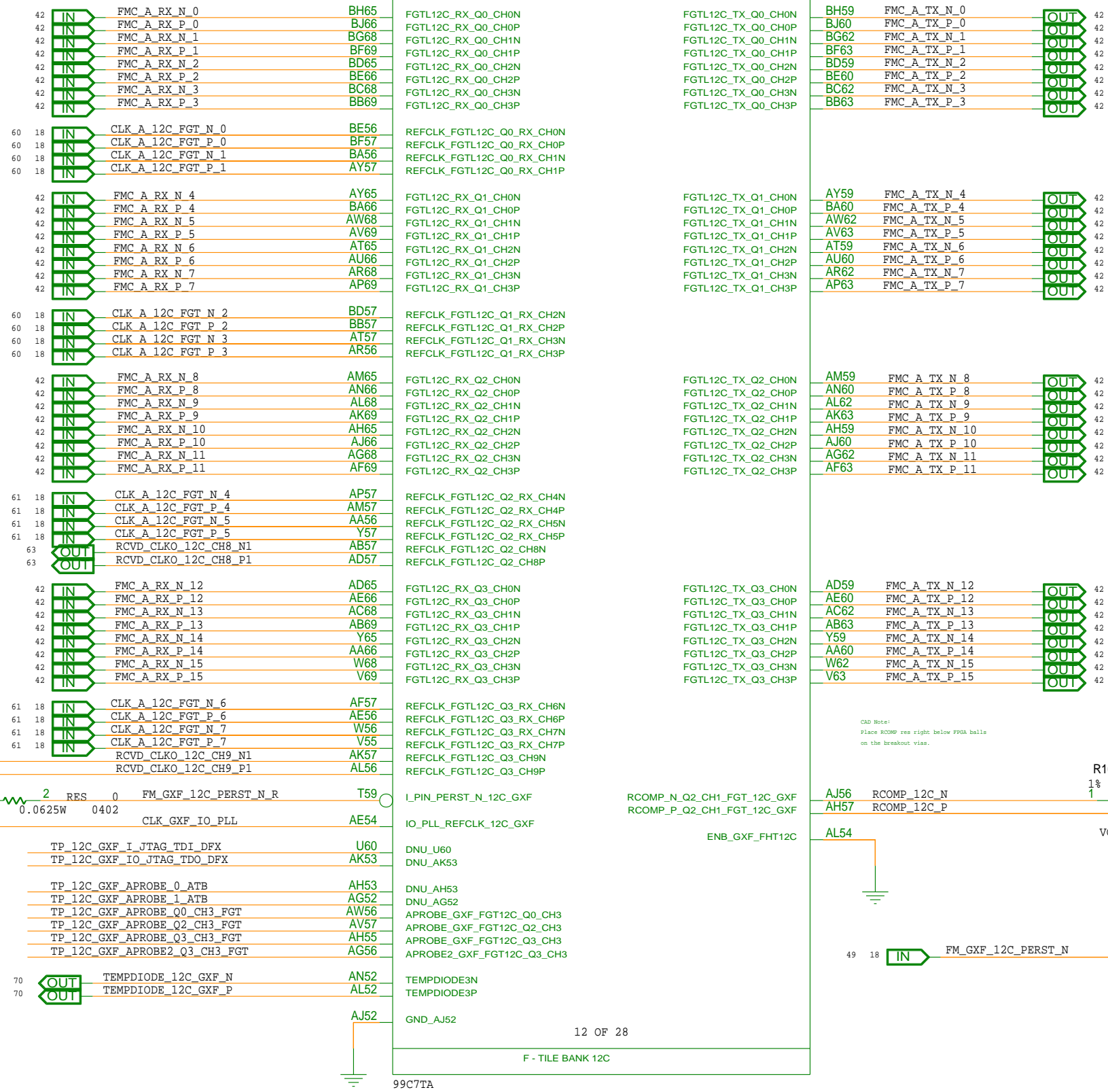
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FPGA BANK 12C

U1
EMPTY



CAD NOTE: PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS.

FMC_A_TX*

CAD Note:

Please follow the right below FPGA balls
on the breakout vias.

RCOMP_N_Q2_CH1_FGT_12C_GXF
RCOMP_P_Q2_CH1_FGT_12C_GXF

ENB_GXF_FHT12C

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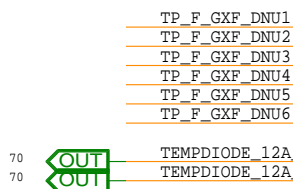
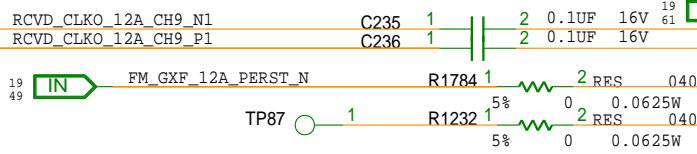
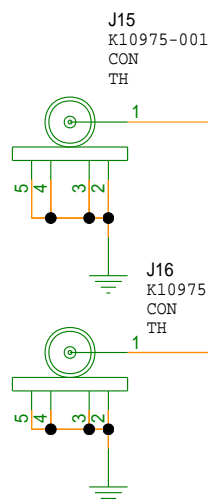
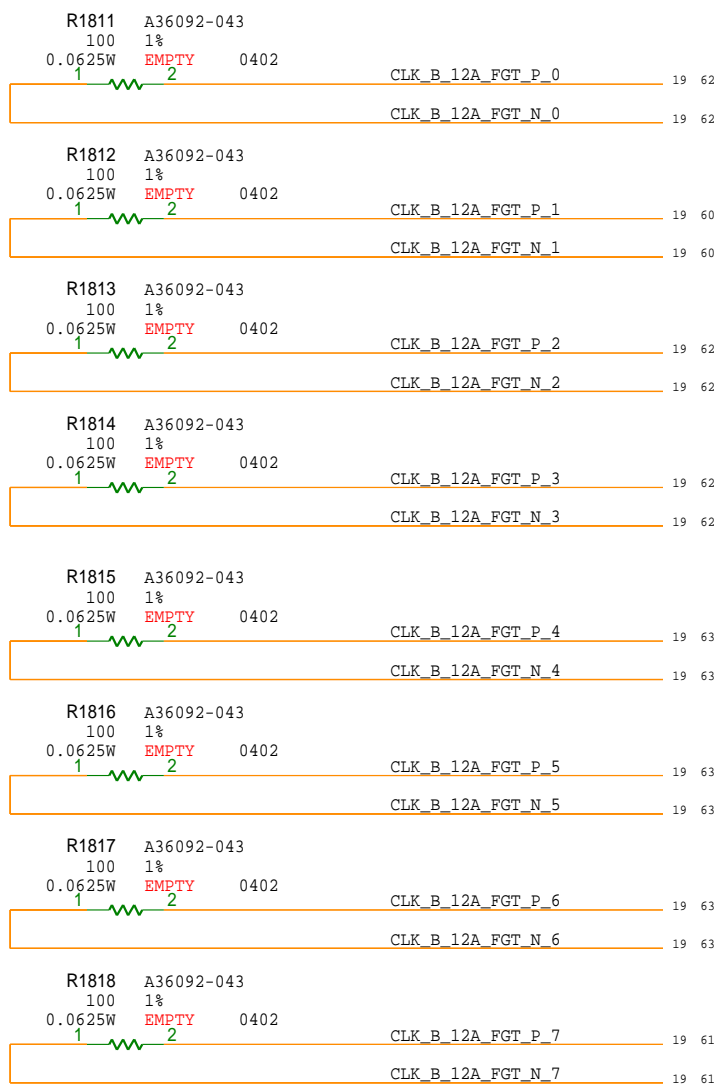
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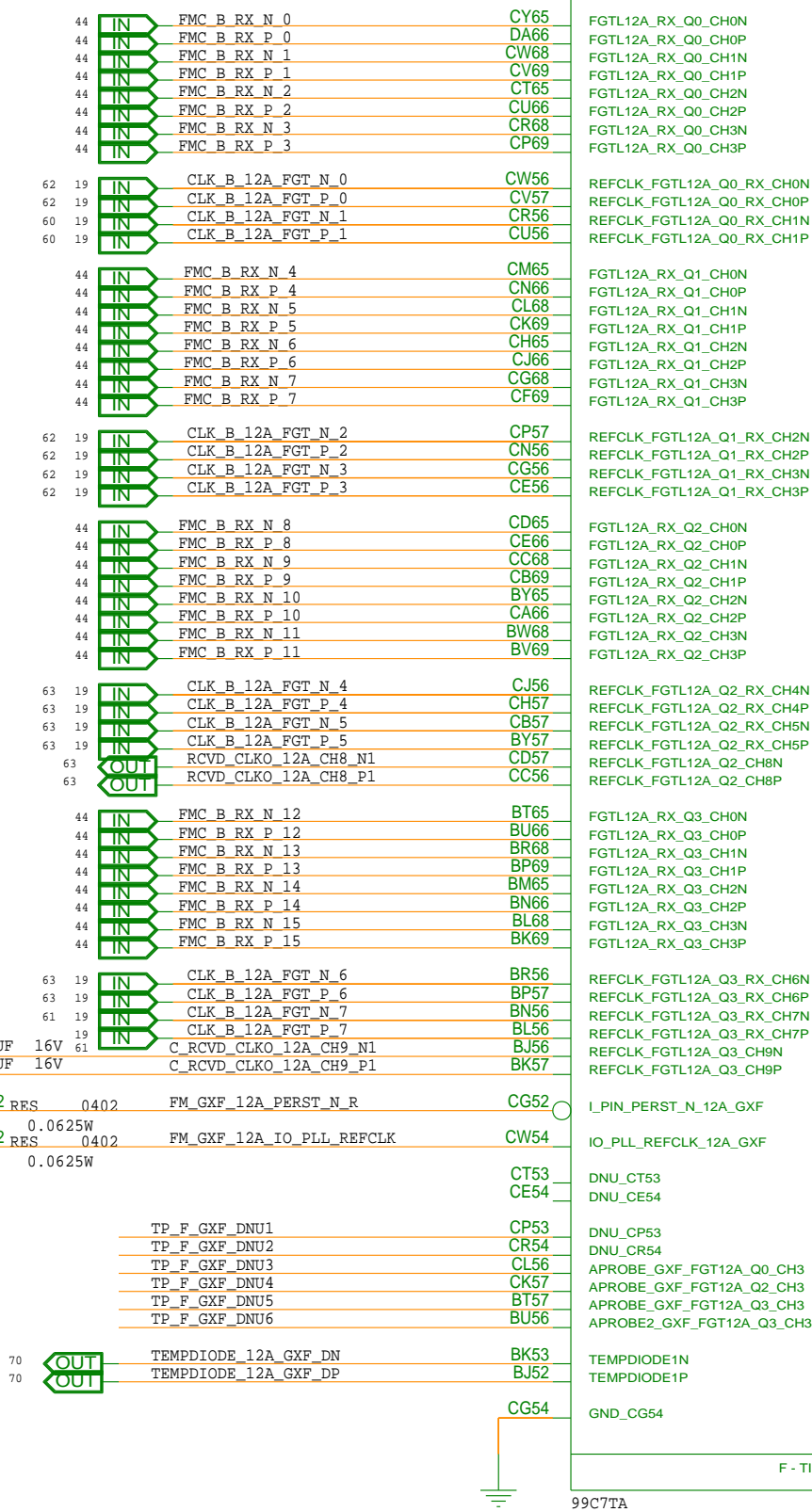
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CAD NOTE:
PLACE THESE 100-OHM RES RIGHT BELOW FPGA BALLS
ON THE BREAKOUT VIAS.



CAD NOTE: PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS

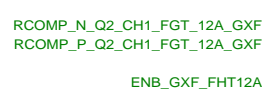
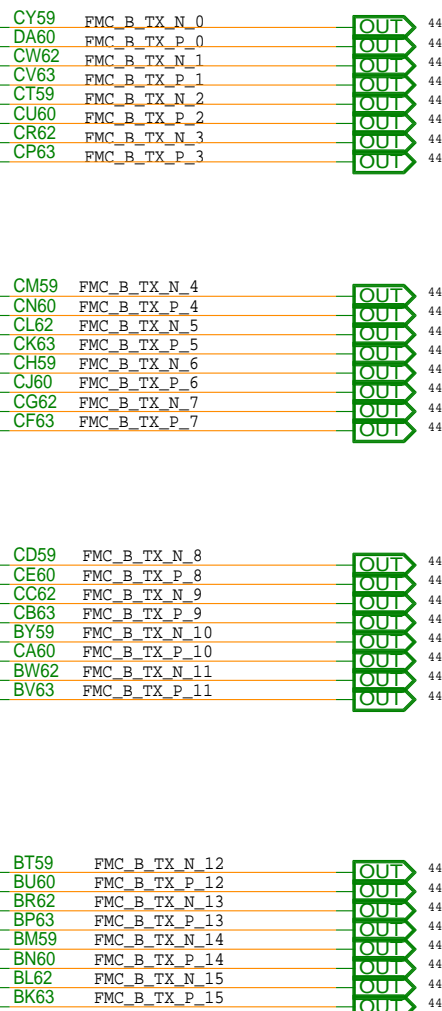
FMC_B_RX*



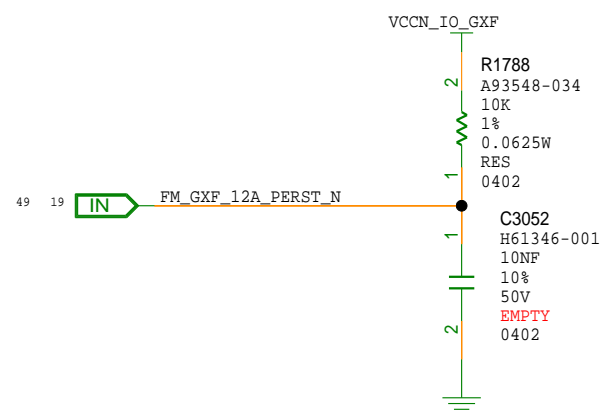
U1
EMPTY

CAD NOTE: PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS

FMC_B_TX*



CAD Note:
Place resistor one right below FPGA balls
on the breakout vias



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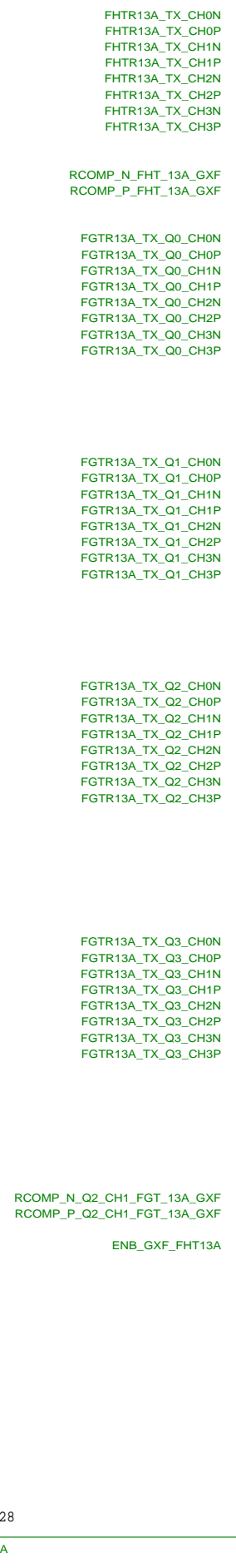
FPGA BANK 13A

CAD NOTE: PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS

U1
EMPTY

HC_FW87_3184B_PHB8

PM97 BANK 13A



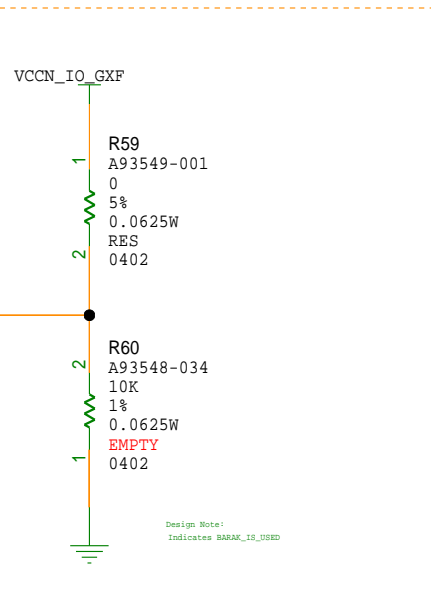
13 OF 28

F - TILE BANK 13A

99C7TA

2

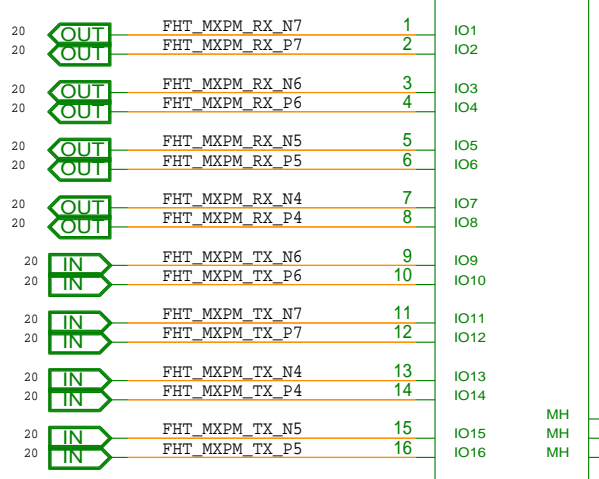
CAD NOTE:
TRANSCEIVER PAIRS MAY BE SWAPPED
TO OPTIMIZE LAYOUT (EXCEPT UX CH0).



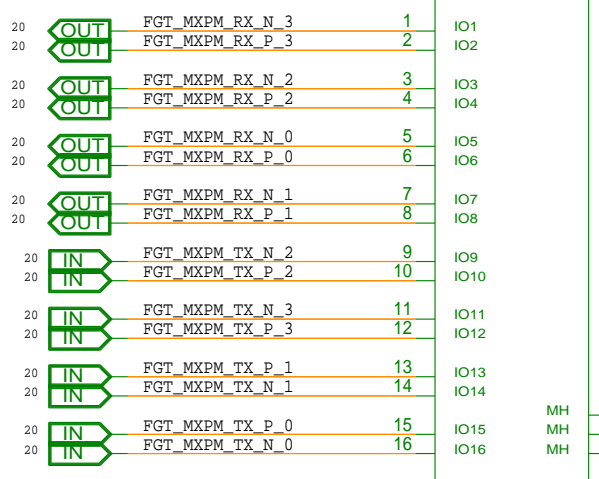
Design Note:
Add a 10K resistor to the VCCN_IO_GXF pin.

1

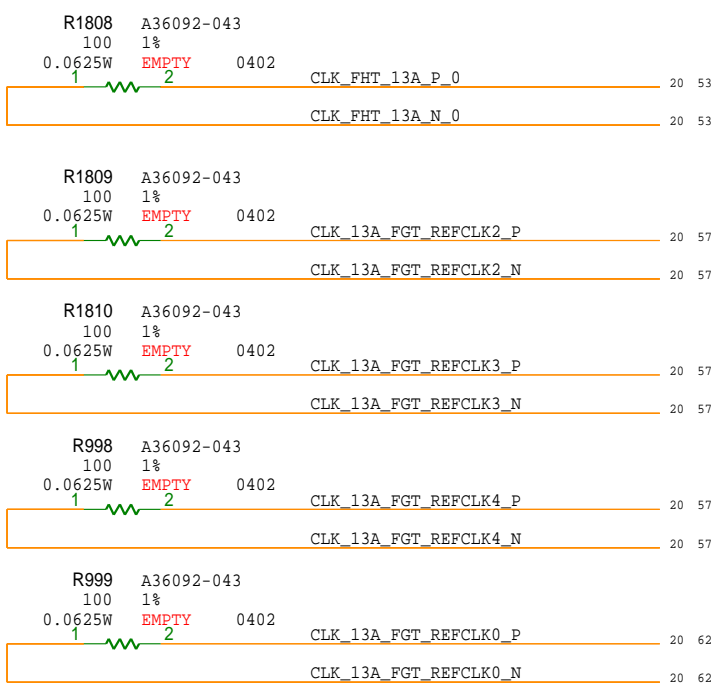
SM
J2
SCON



SM
J28
SCON



CAD NOTE:
PLACE THESE 100-OHM RES RIGHT BELOW FPGA BALLS
ON THE BREAKOUT VIAS.



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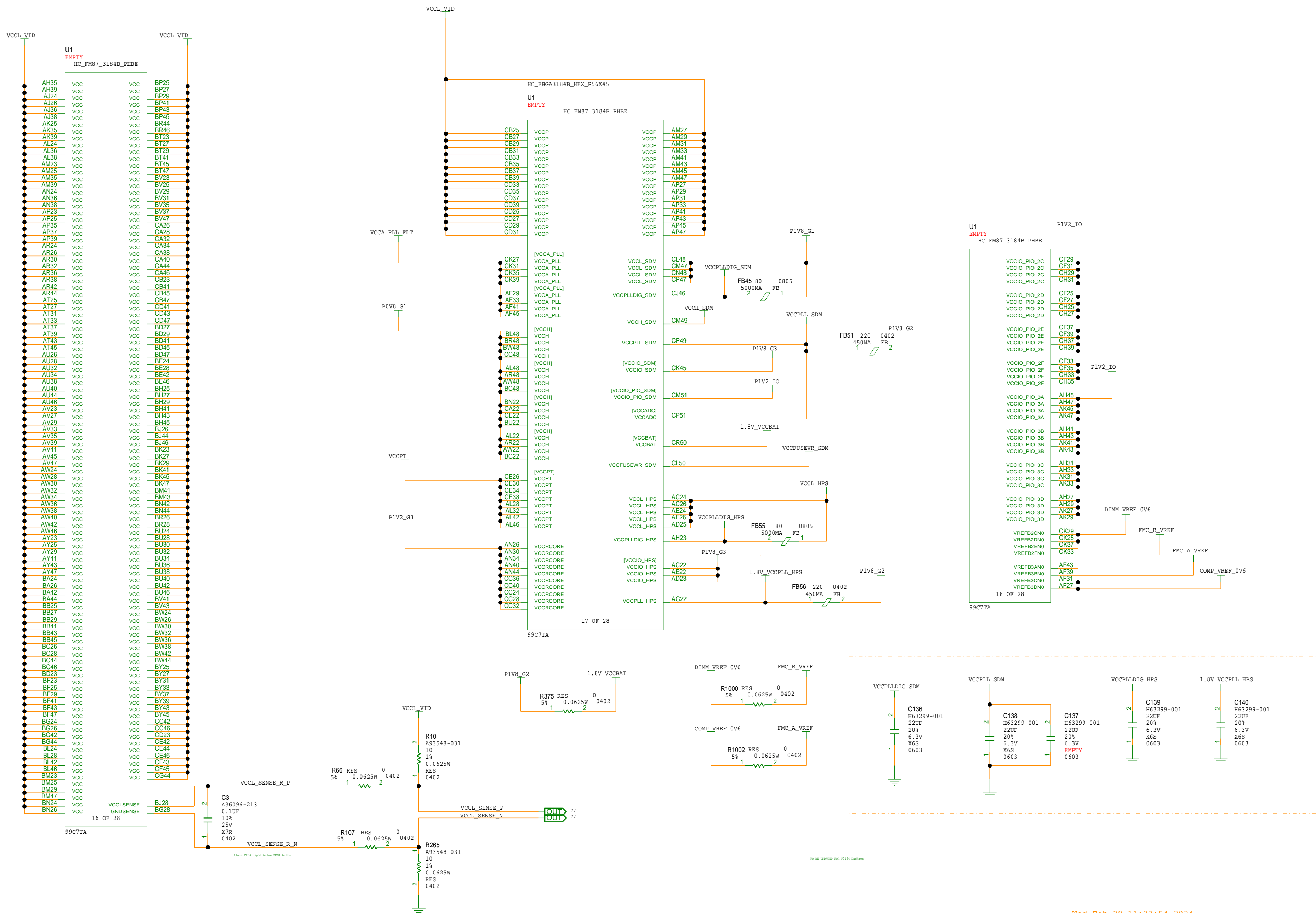
CAD NOTE:
PLACE THESE 100-OHM RES RIGHT BELOW FPGA BALLS
ON THE BREAKOUT VIAS.

CAD NOTE: PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS.

DESIGN NOTE:
INDICATES BARAK_IS_USED

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DOCUMENT NUMBER

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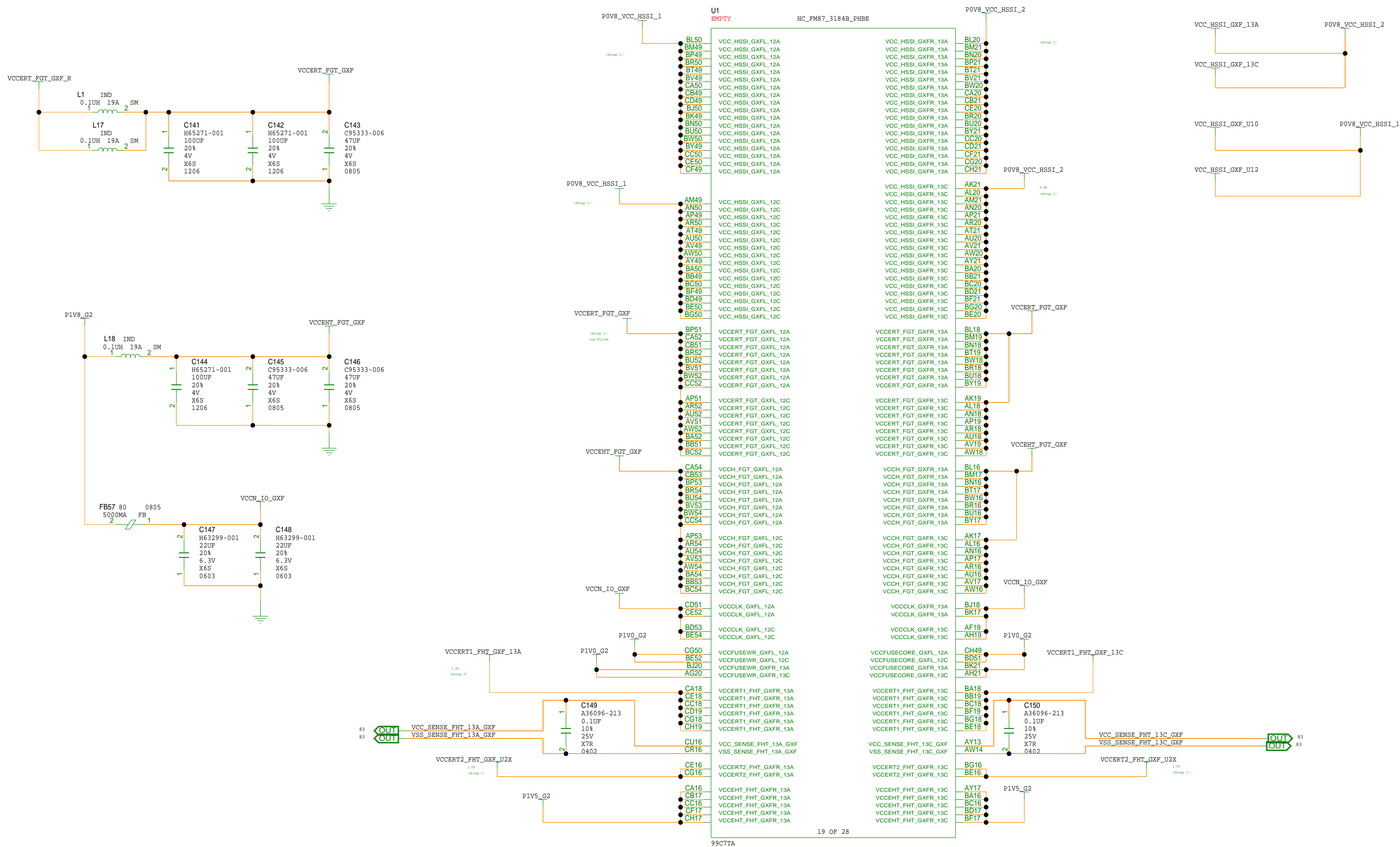
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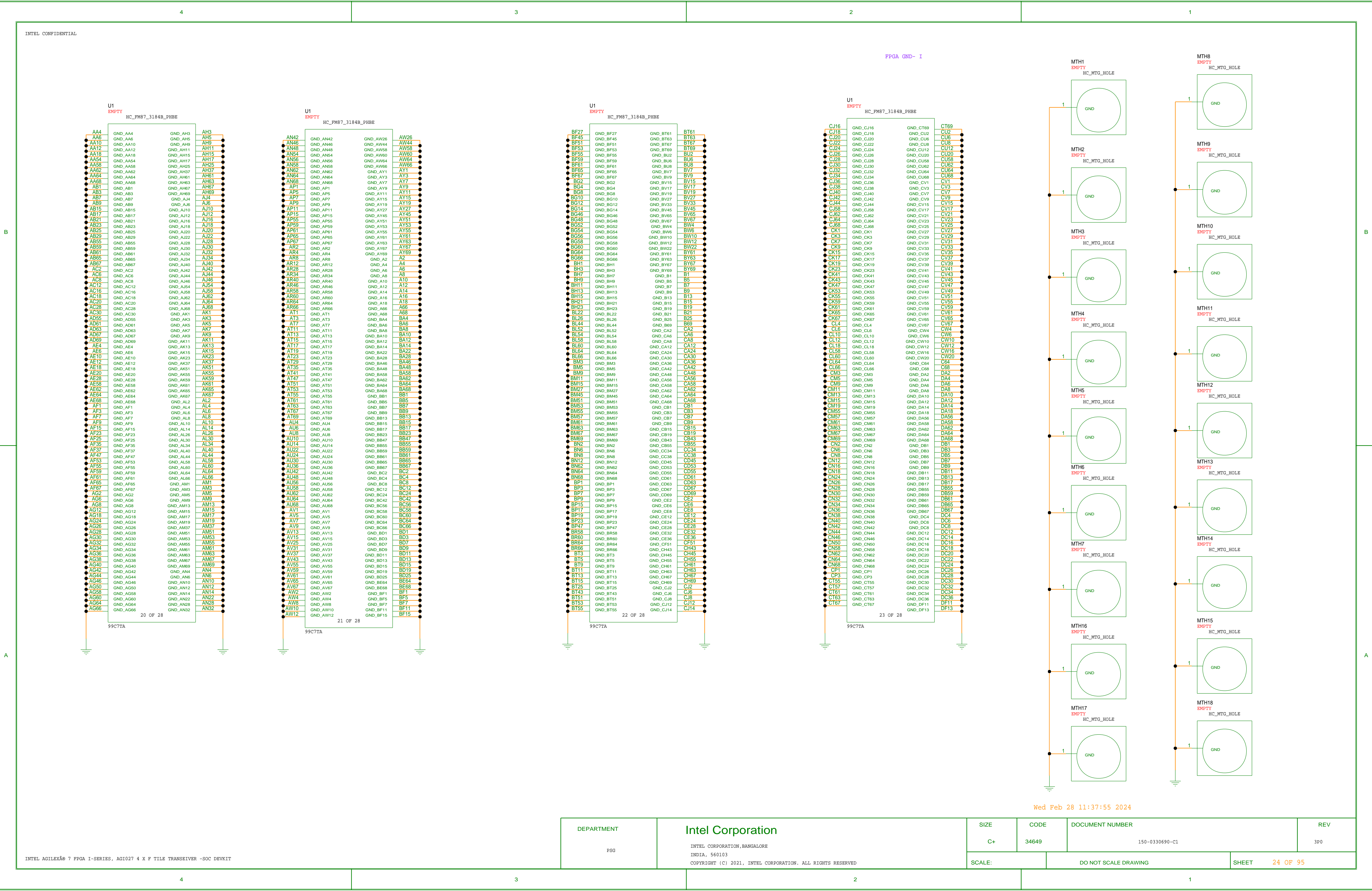
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150-0330690-01

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24 OF 95

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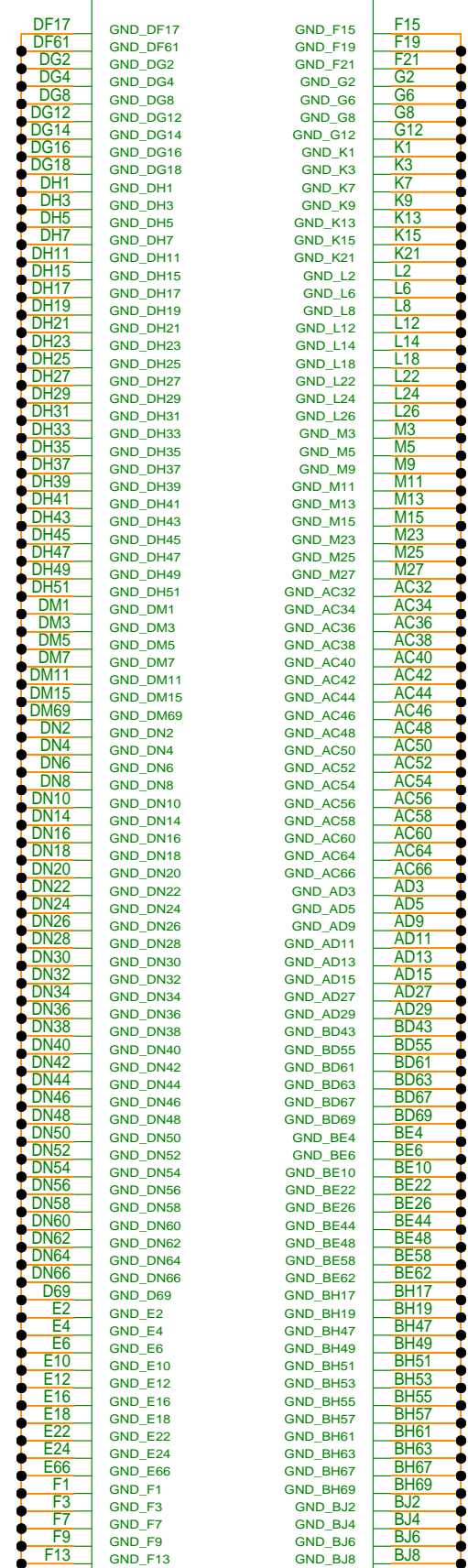
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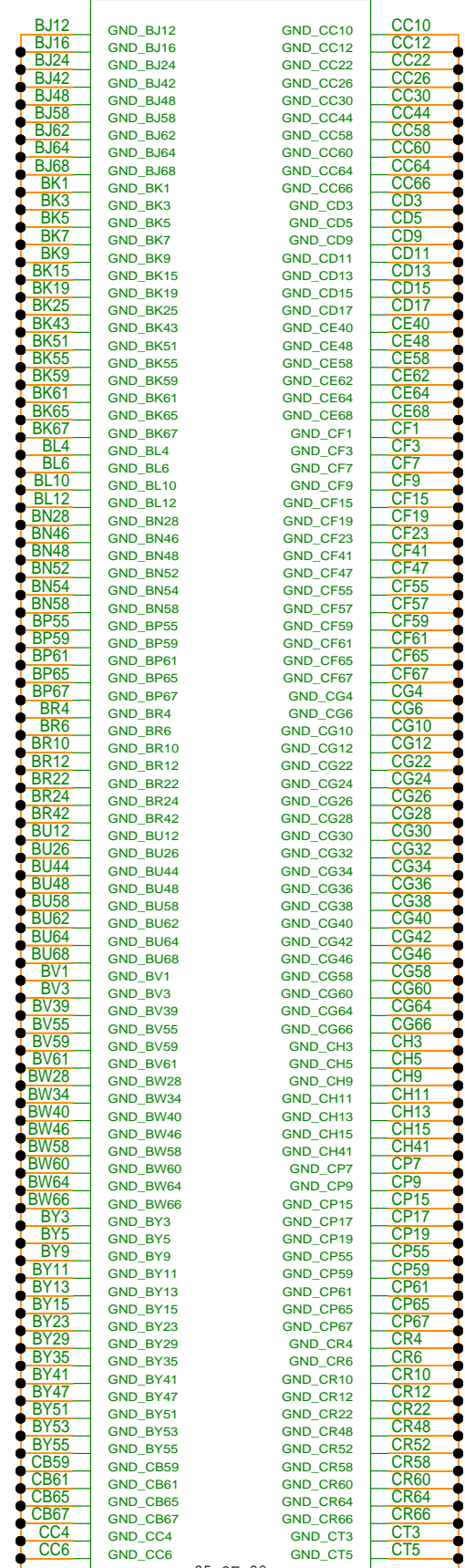
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FPGA GND- II

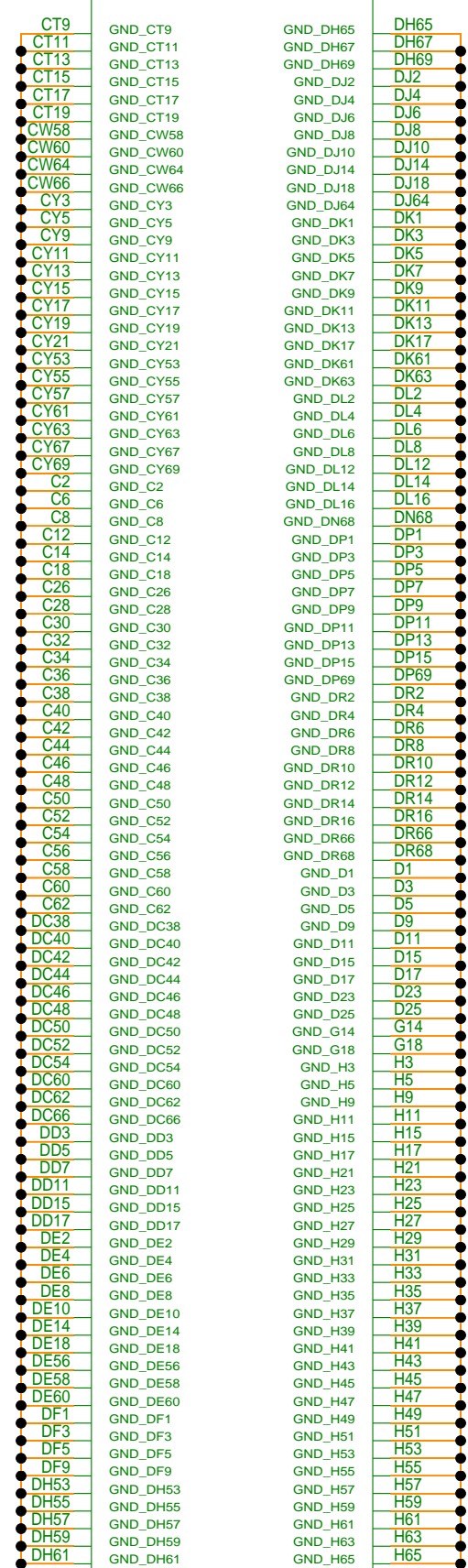
U1
EMPTY
HC_FM87_3184B_PHB8



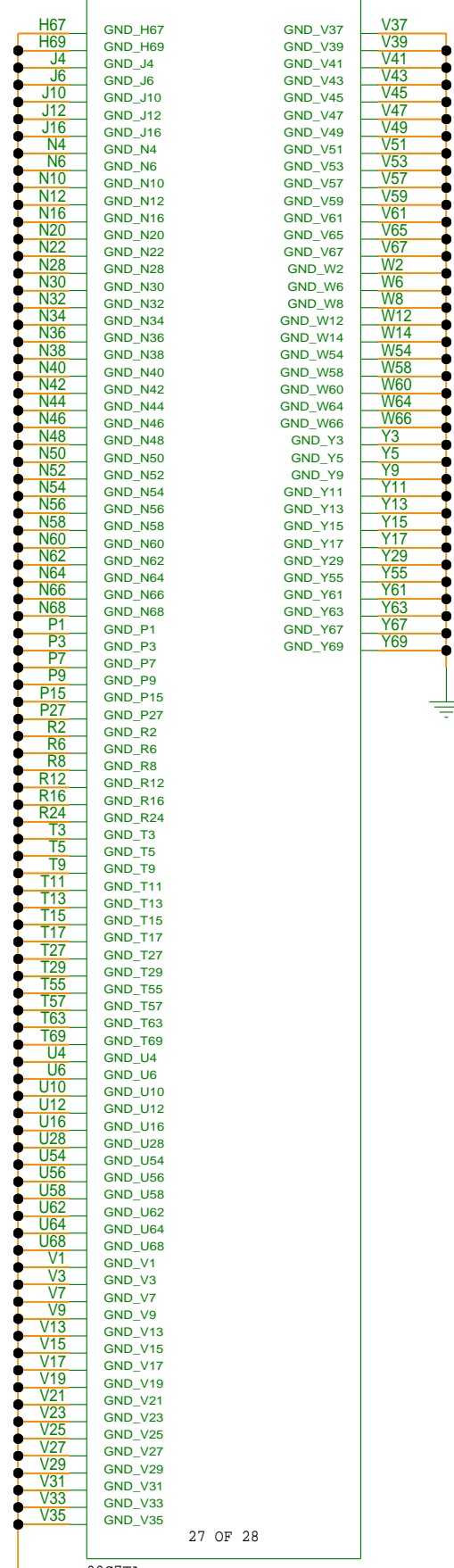
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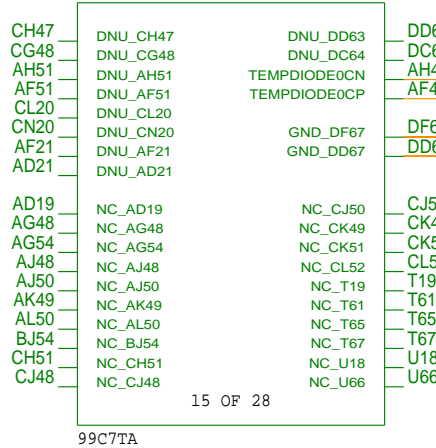
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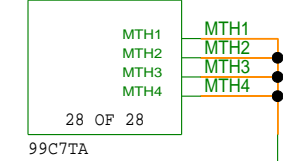
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HC_FM87_3184B_PHB8



U1
EMPTY
HC_FM87_3184B_PHB8



U1
EMPTY
HC_FM87_3184B_PHB8



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FPGA DECOUPLING - I

VCCL_VID

BOTTOM FPGA CAVITY

BOTTOM FPGA

PERIPHERAL SURROUNDING FPGA

POV8_G1

16 VCCB BALLS

PERIPHERAL SURROUNDING FPGA

VCCH

PERIPHERAL SURROUNDING FPGA

POV8_G1

VCCH

BOTTOM FPGA

POV8_G1

VCCL_SDM

PERIPHERAL SURROUNDING FPGA

BOTTOM FPGA

VCCLLDIG_SDM

BOTTOM FPGA

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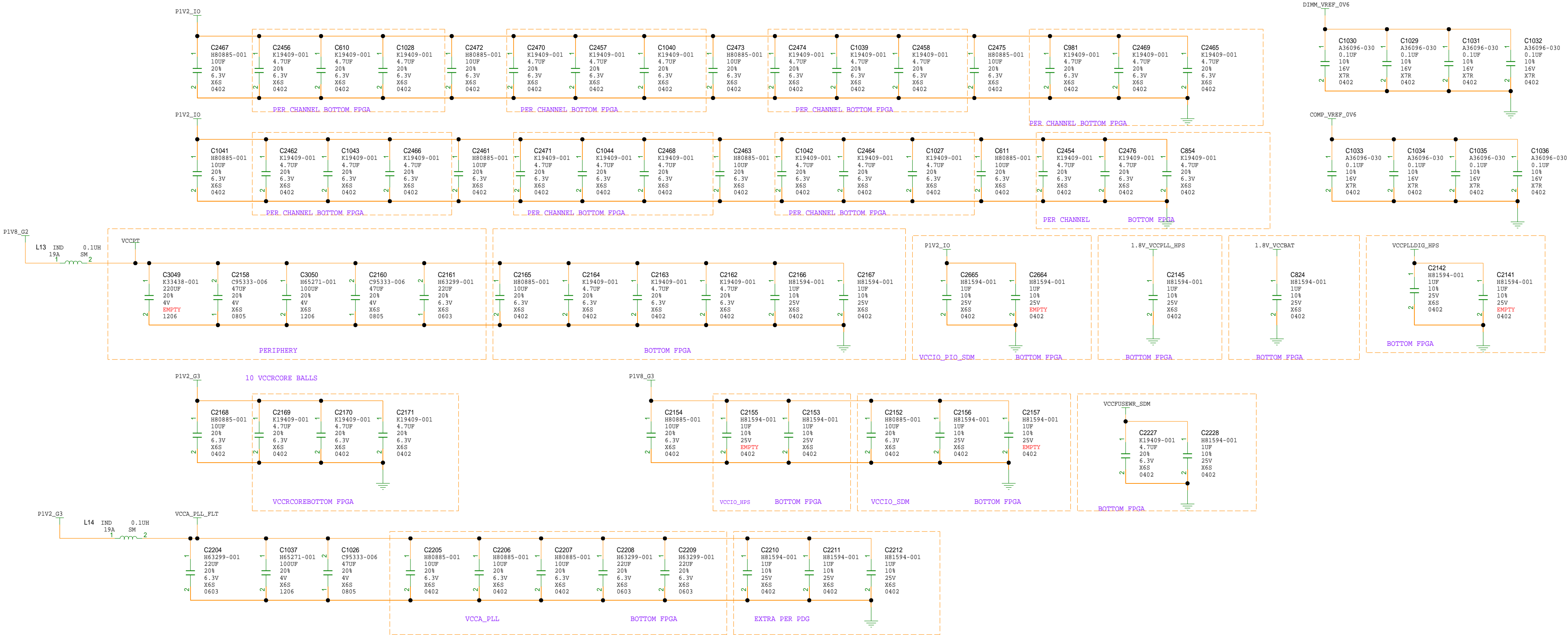
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FPGA DECOUPLING - II



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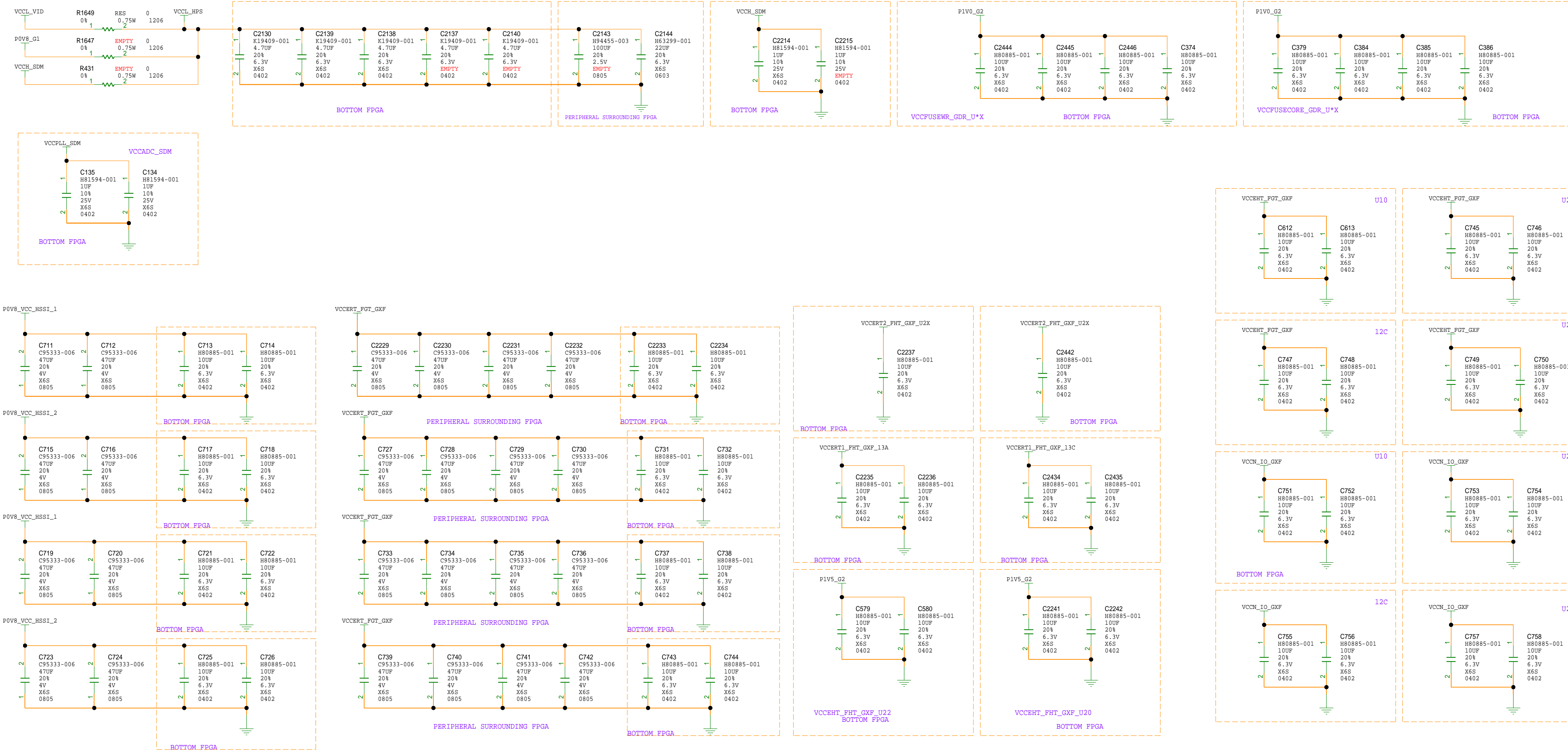
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FPGA DECOUPLING - III



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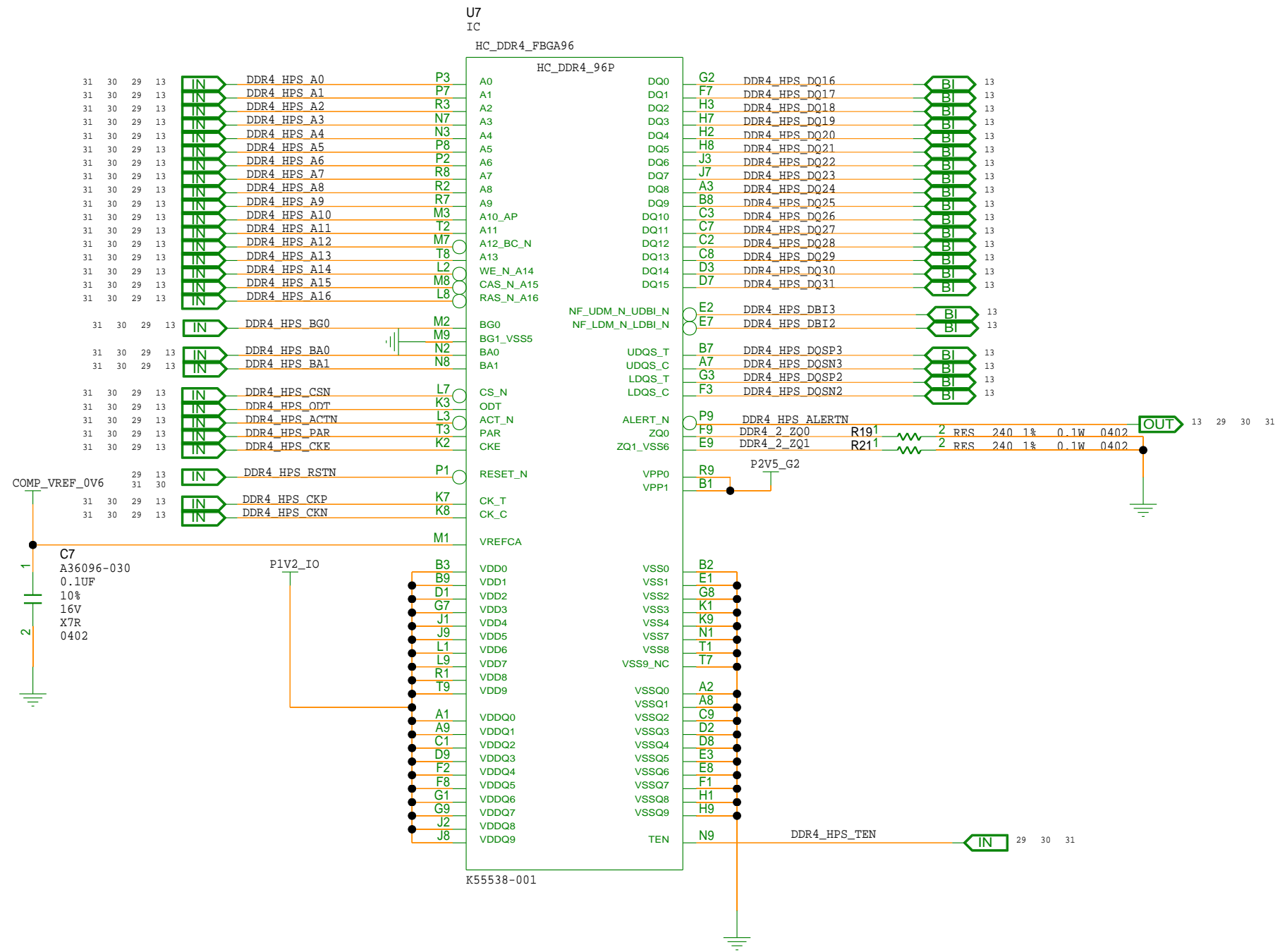
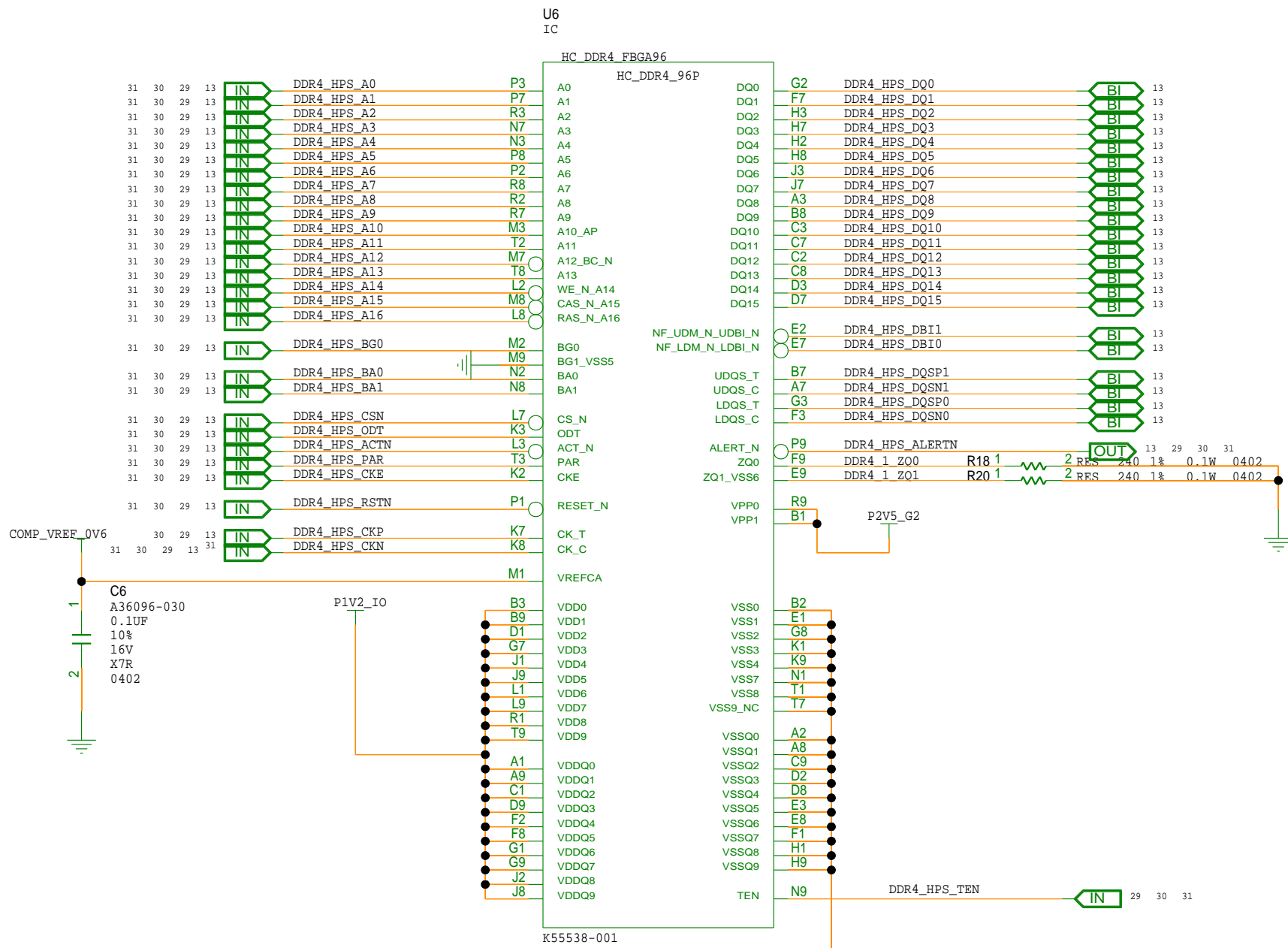
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DDR4 COMPONENT-I



DESIGN NOTE:
DDR4 COMPONENT SUPPORT FOR 1G16 CONFIGURATION ONLY.
PIN M9 OF THE DDR4 COMPONENT IS VSS FOR THE 96-BALL X16 BALL PACKAGE

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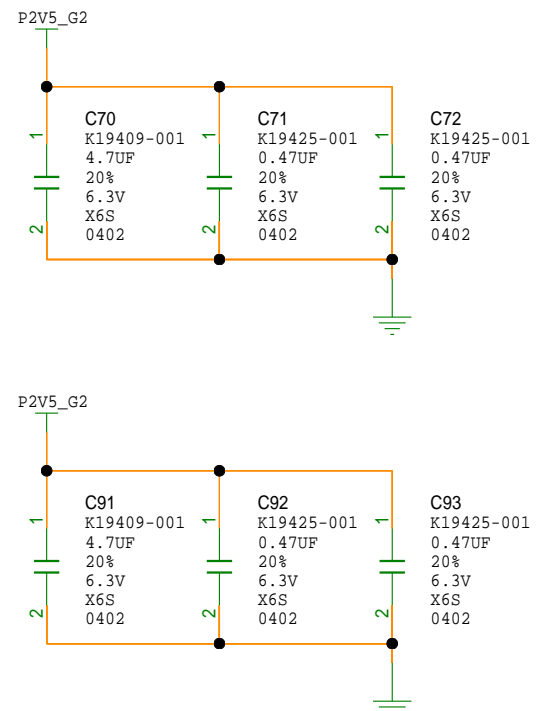
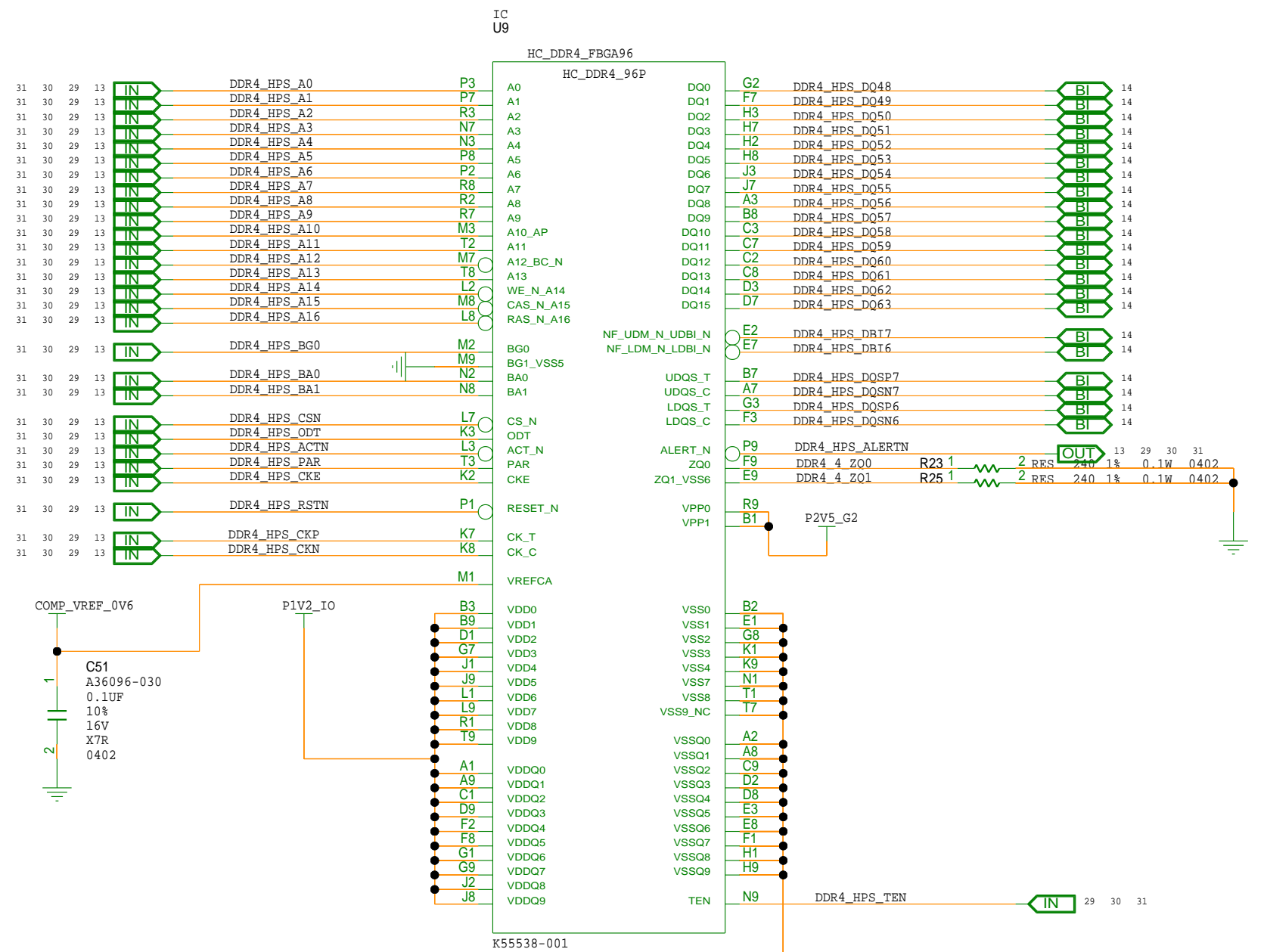
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SHEET 30 OF 95

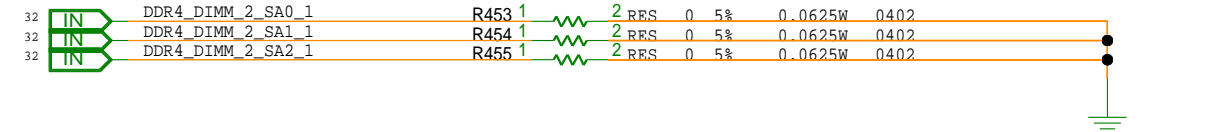
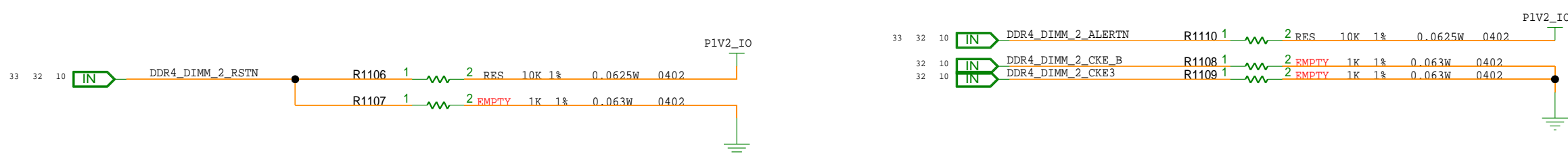
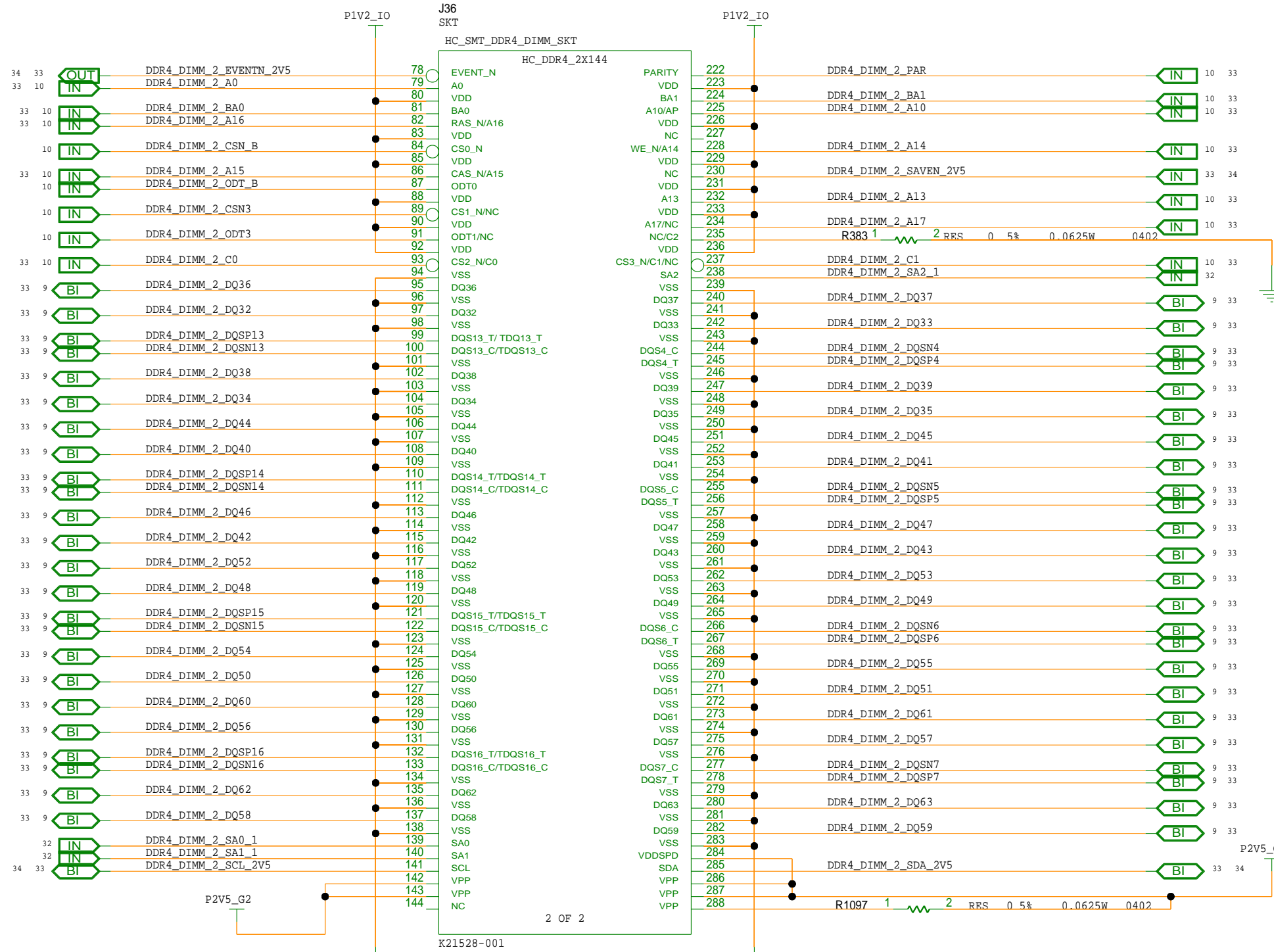
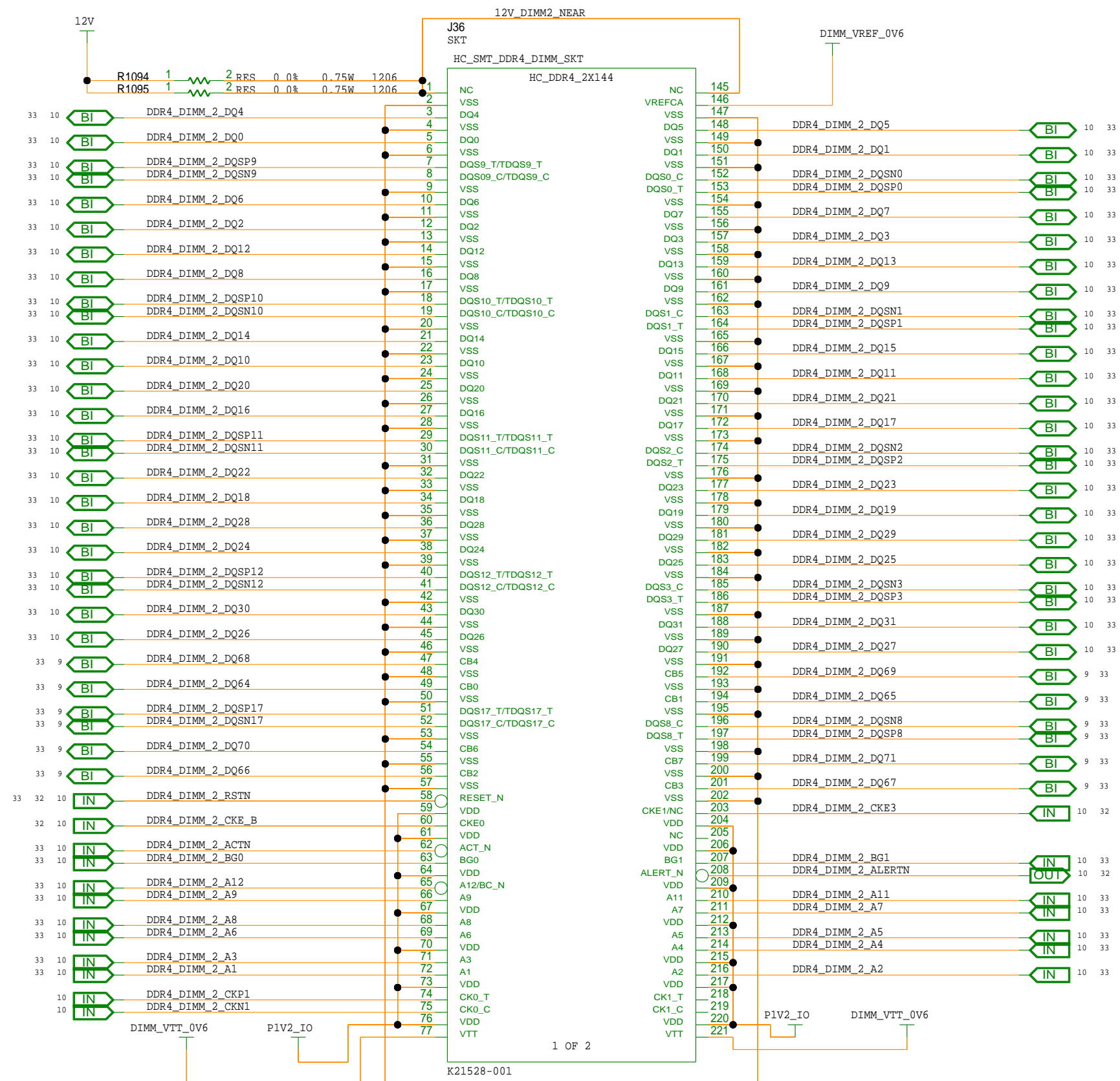
DDR4 COMPONENT-III



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2DPC DIMM-I



SIMULATION BASED ON
MTA18ASF2G72PZ-3G2E2 16GB SRX4 DDR4-3200
MTA36ASF4G72PZ-2G6E1 32GB DRX4 DDR4-2666

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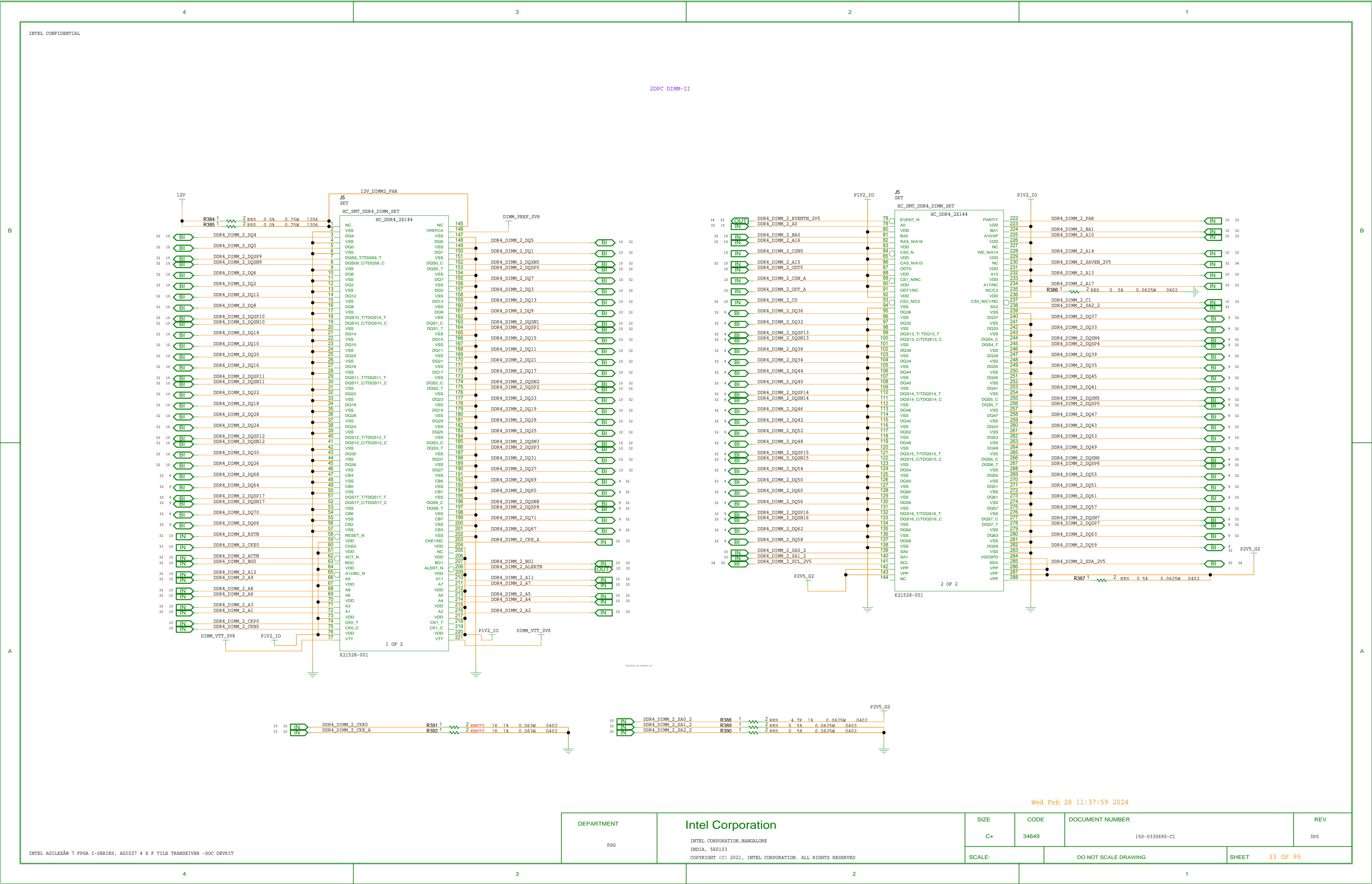
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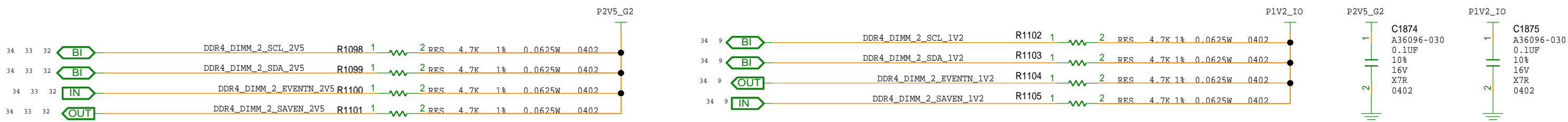
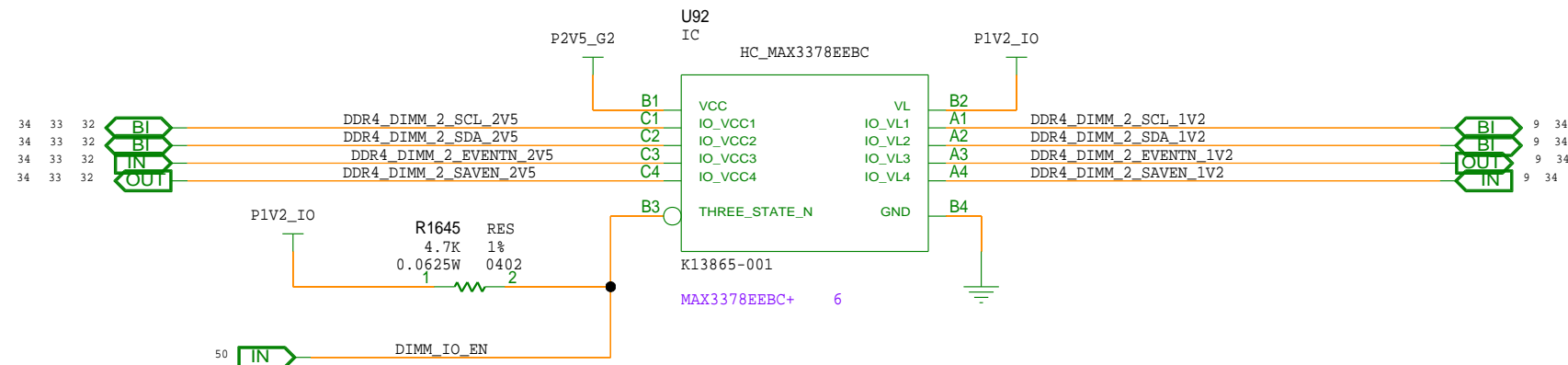
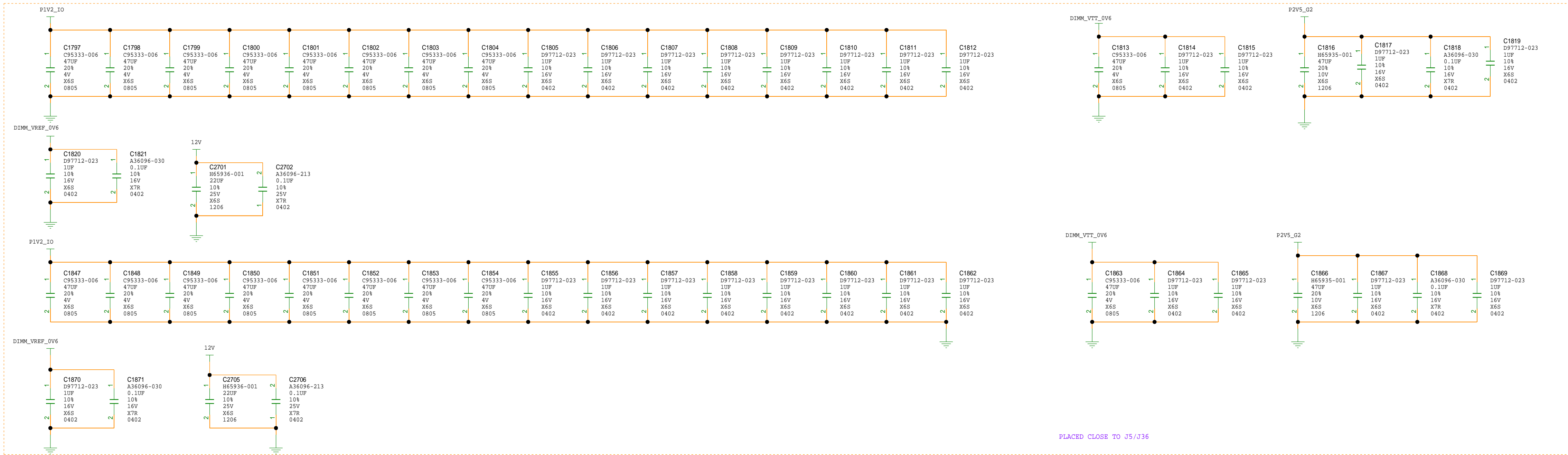
SHEET

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2DPC DIMM-FILTER AND LVL SHIFTER



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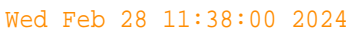
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USB3.X/DP1.4 ALTMODE MUX

INTEL AGILEX® 7 FPGA I-SERIES, AGI027 4 X F TILE TRANSEIVER -SOC DEVKIT

4

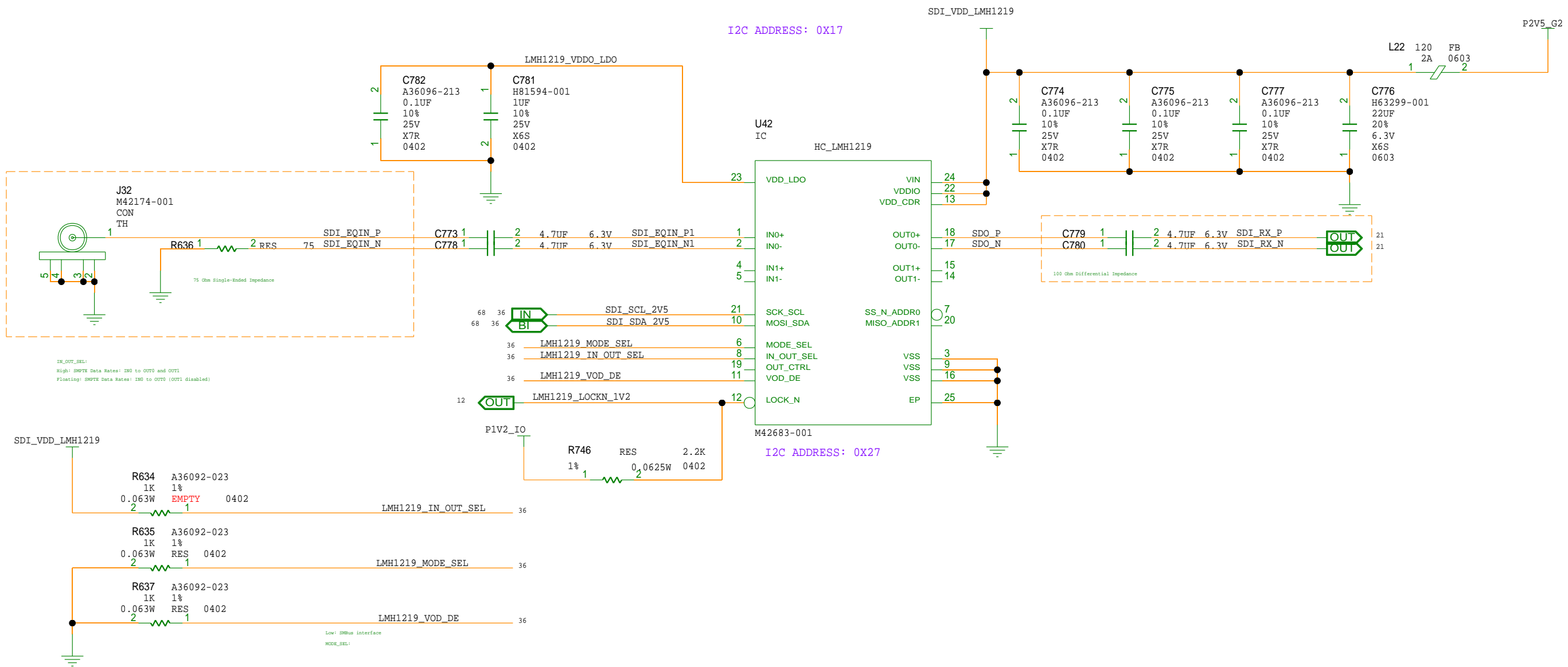
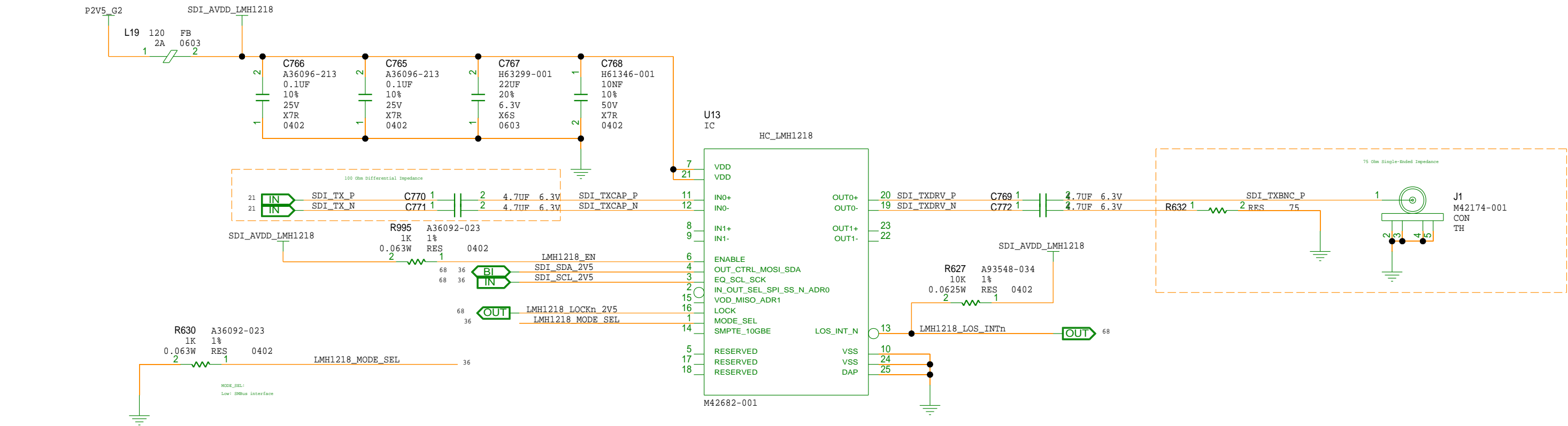
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SDI CABLE DRIVER, EQUALIZER, BNC



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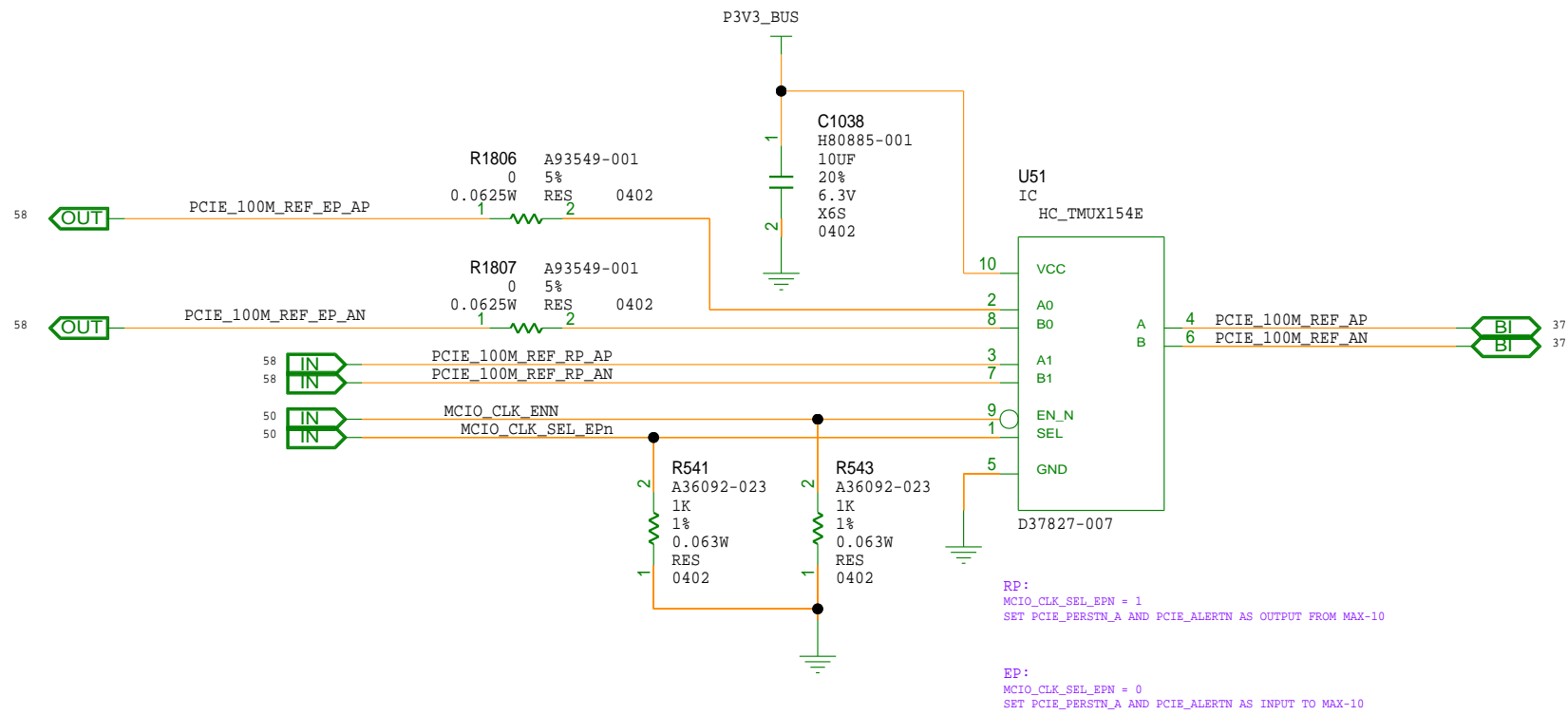
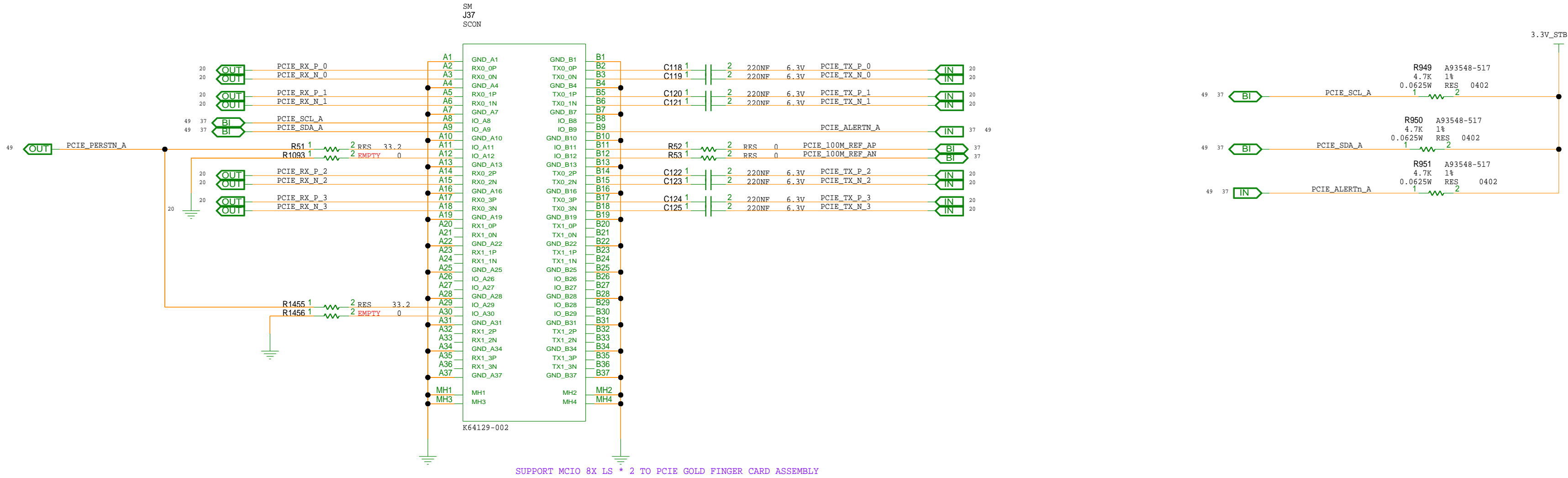
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MCIO



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DESIGN NOTE: CHANNELS MAY BE SWAPPED
WITHIN EACH UX BLOCK TO OPTIMIZE ROUTINGS.
LANE 0 & 4 MAY NOT BE SWAPPED.
(TX1/RX1 & TX4/RX4 ON CONN)

INTEL AGILEX® 7 FPGA I-SERIES, AGI027 4 X F TILE TRANSEIVER -SOC DEVKIT

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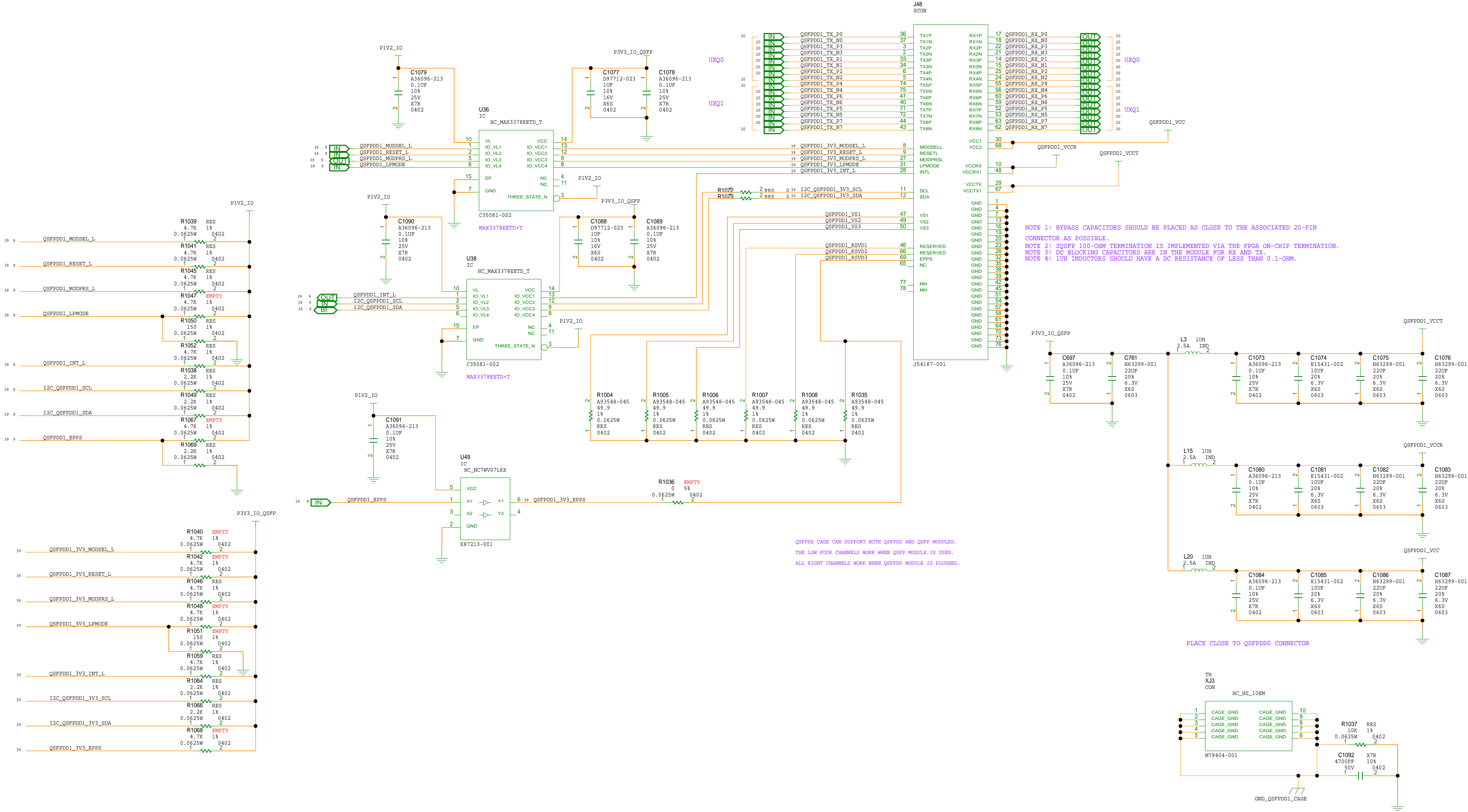
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QSFP-DD CONN #1 (56G ETHERNET)

DESIGN NOTE: CHANNELS MAY BE SWAPPED
WITHIN EACH UX BLOCK TO OPTIMIZE ROUTINGS.
LANE 0 & 4 MAY NOT BE SWAPPED.
(TX1/RX1 & TX4/RX4 ON CONN)



NOTE 1: BYPASS CAPACITORS SHOULD BE PLACED AS CLOSE TO THE ASSOCIATED 20-PIN CONNECTOR AS POSSIBLE.
NOTE 2: ZQSFP 100-OHM TERMINATION IS IMPLEMENTED VIA THE FPGA ON-CHIP TERMINATION.
NOTE 3: DC BLOCKING CAPACITORS ARE IN THE MODULE FOR RX AND TX.
NOTE 4: 1UH INDUCTORS SHOULD HAVE A DC RESISTANCE OF LESS THAN 0.1-OHM.

QSFPDD CAGE CAN SUPPORT BOTH QSFPDD AND QSFP MODULES.
THE LOW FOUR CHANNELS WORK WHEN QSFP MODULE IS USED.
ALL EIGHT CHANNELS WORK WHEN QSFPDD MODULE IS PLUGGED.

PLACE CLOSE TO QSFPDD0 CONNECTOR

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SCALE:

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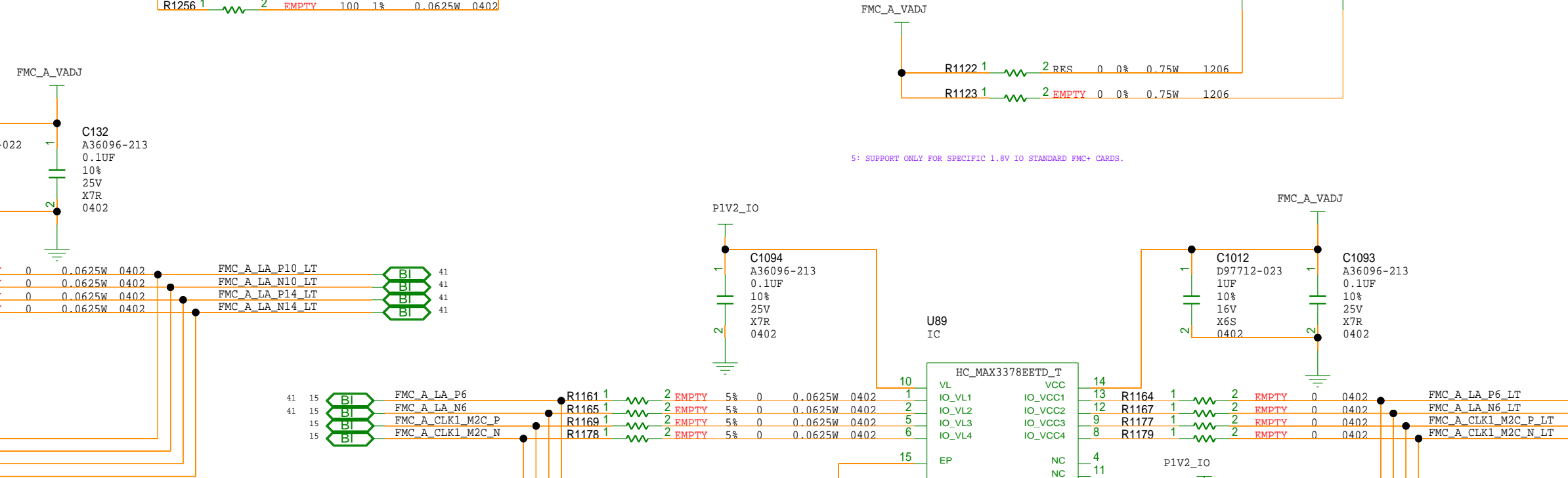
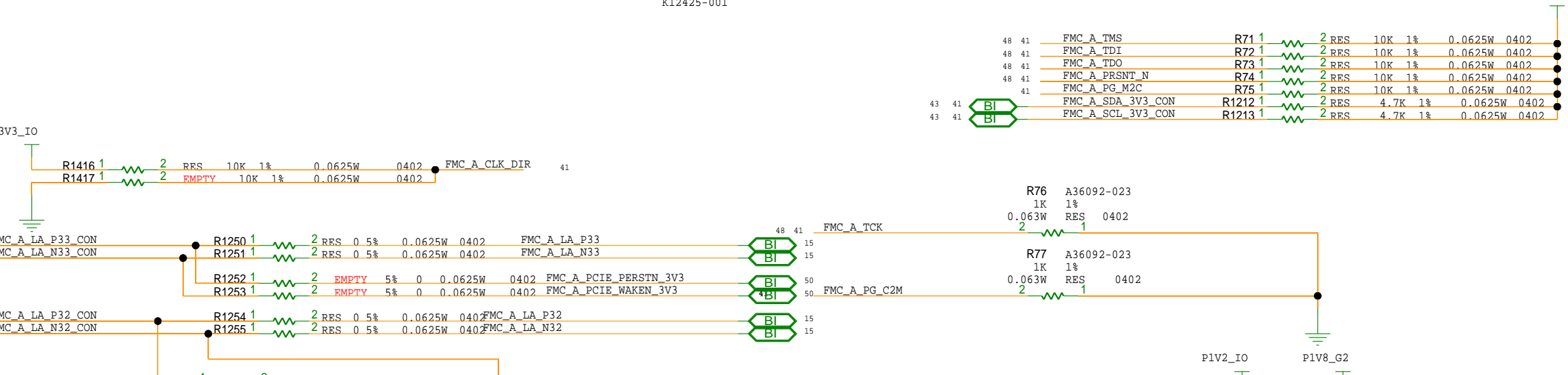
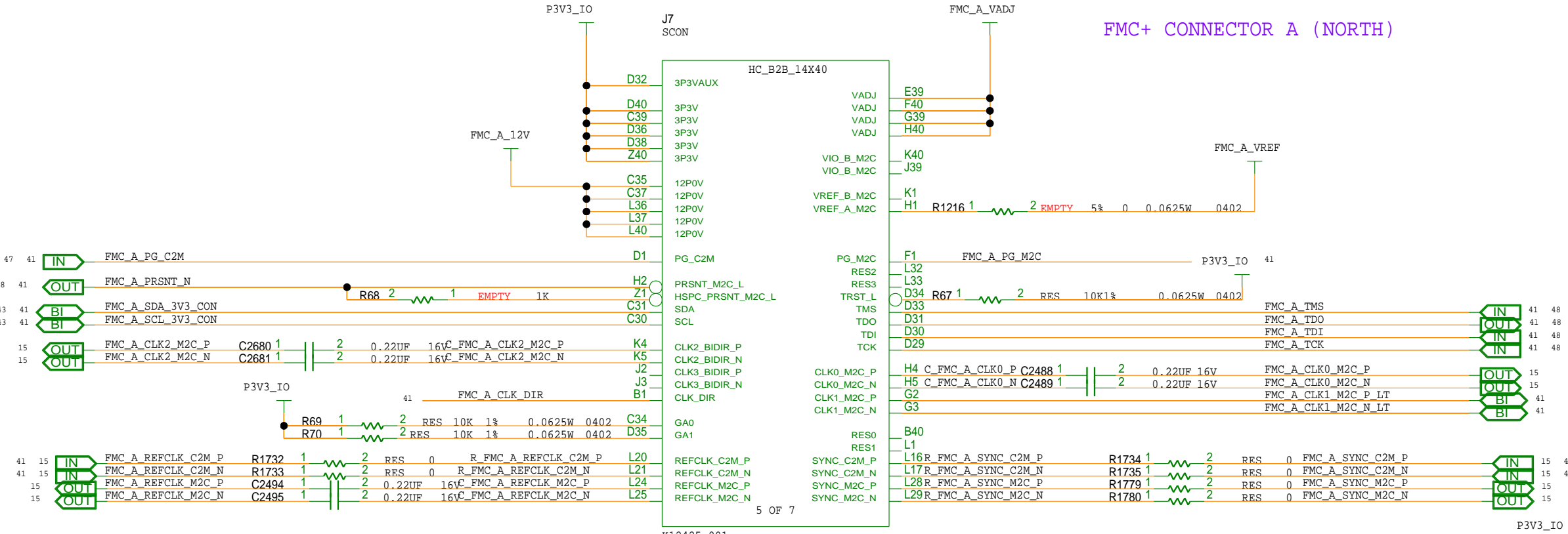
3

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```
3: CHANGE RESISTOR OPTIONS AND ROUTE LA_P/N/32/33 TO SYSTEM
    MAXIO WHEN THESE PINS RUN 3.3V SIGNALS
    [ INTEL BUILT FMC+ TO PCIE GOLD FINGER CABLE, SAMTEC]

4: NOT GUARANTEE SUPPORT OTHER FMC CARDS IF:
    FMC DAUGHTER CARD'S ON-BOARD LEVEL SHIFTER DOESN'T SUPPORT 1.2V
    THE REQUIREMENT OF FMC DIFFERENTIAL SIGNAL IS NOT COMPLIANT
    WITH AGILEX 1.2V IO
```



SUPPORT ONLY FOR SPECIFIC 1.8V IO STANDARD FMC+ CARDS

Wed Feb 28 11:38:03 2024

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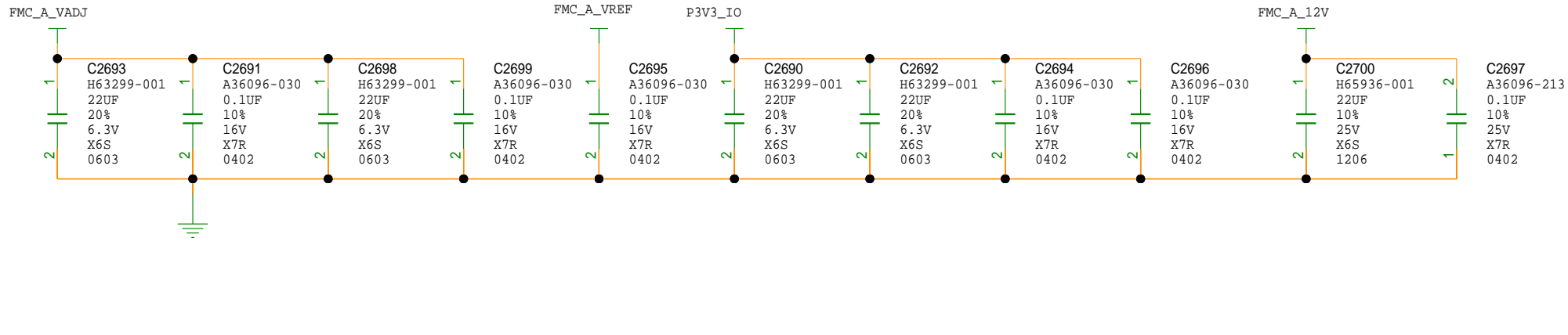
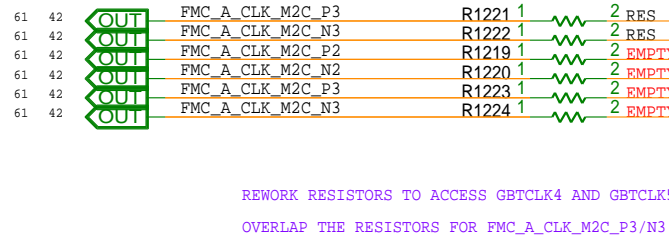
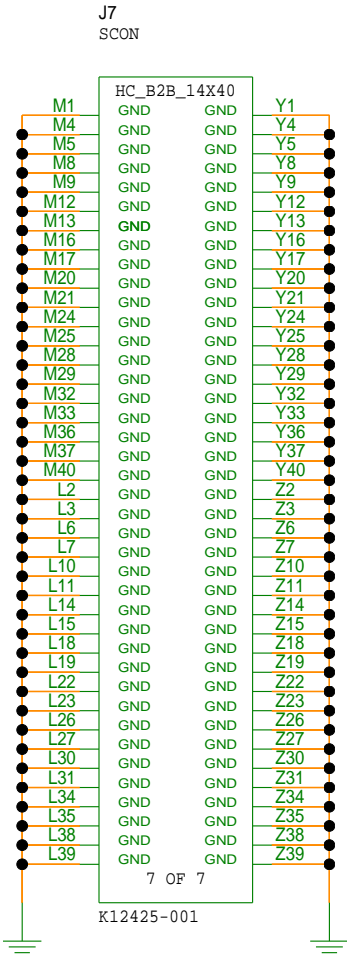
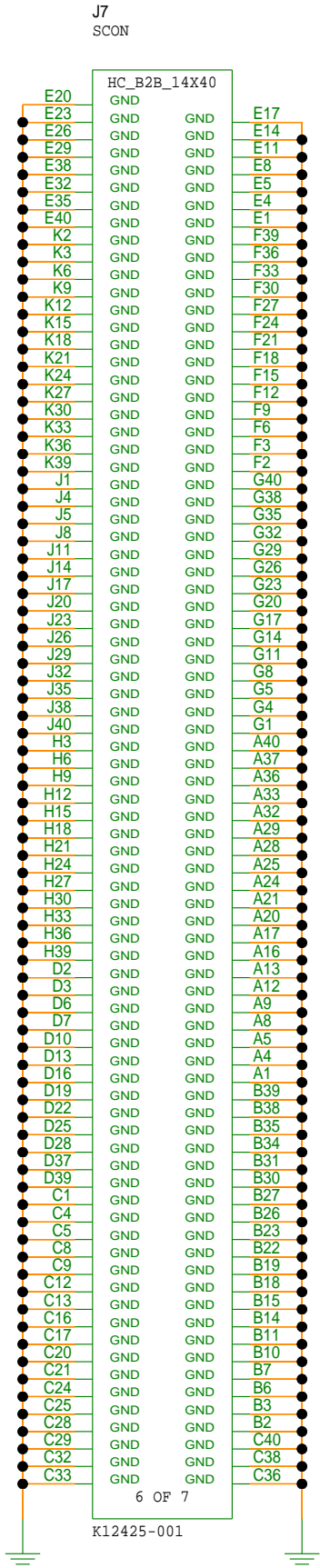
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FMC+ CONNECTOR A (NORTH)



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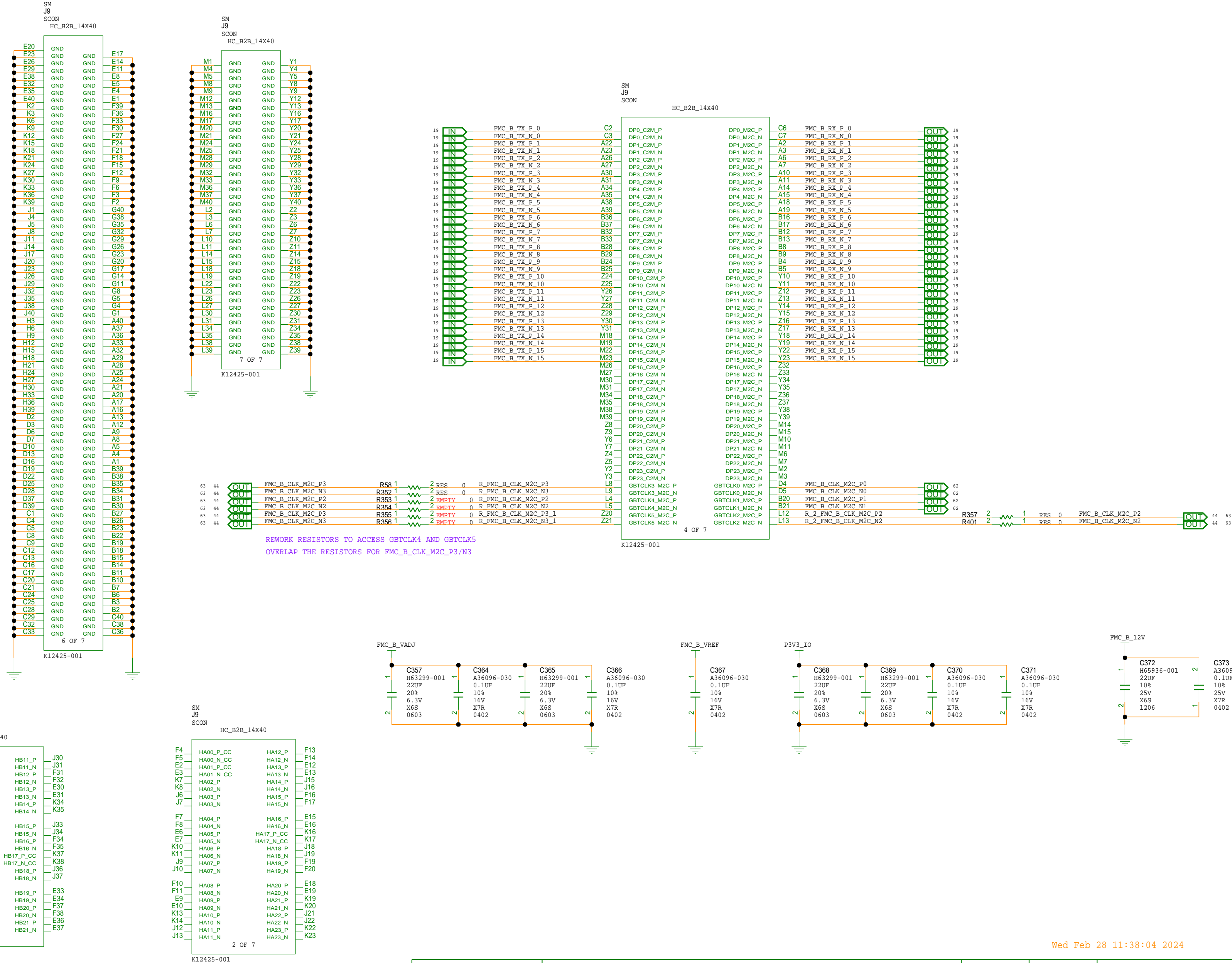
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FMC+ CONNECTOR B (EAST)



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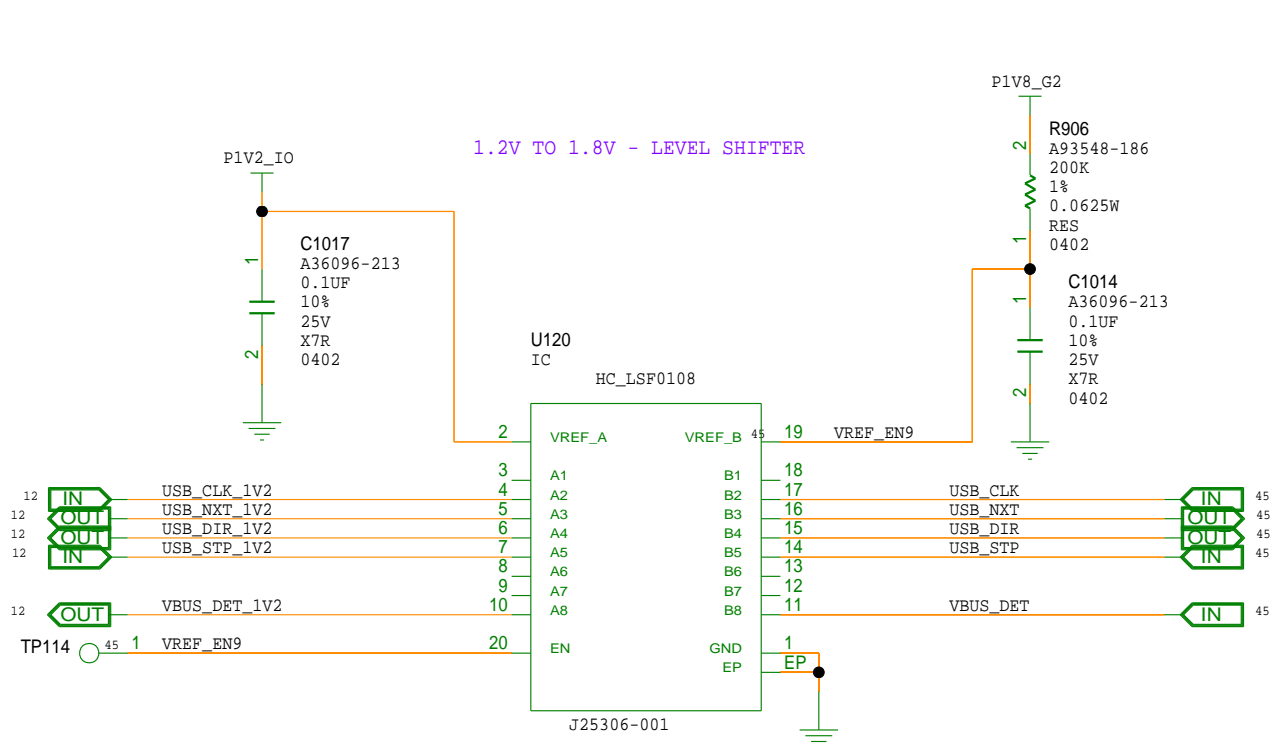
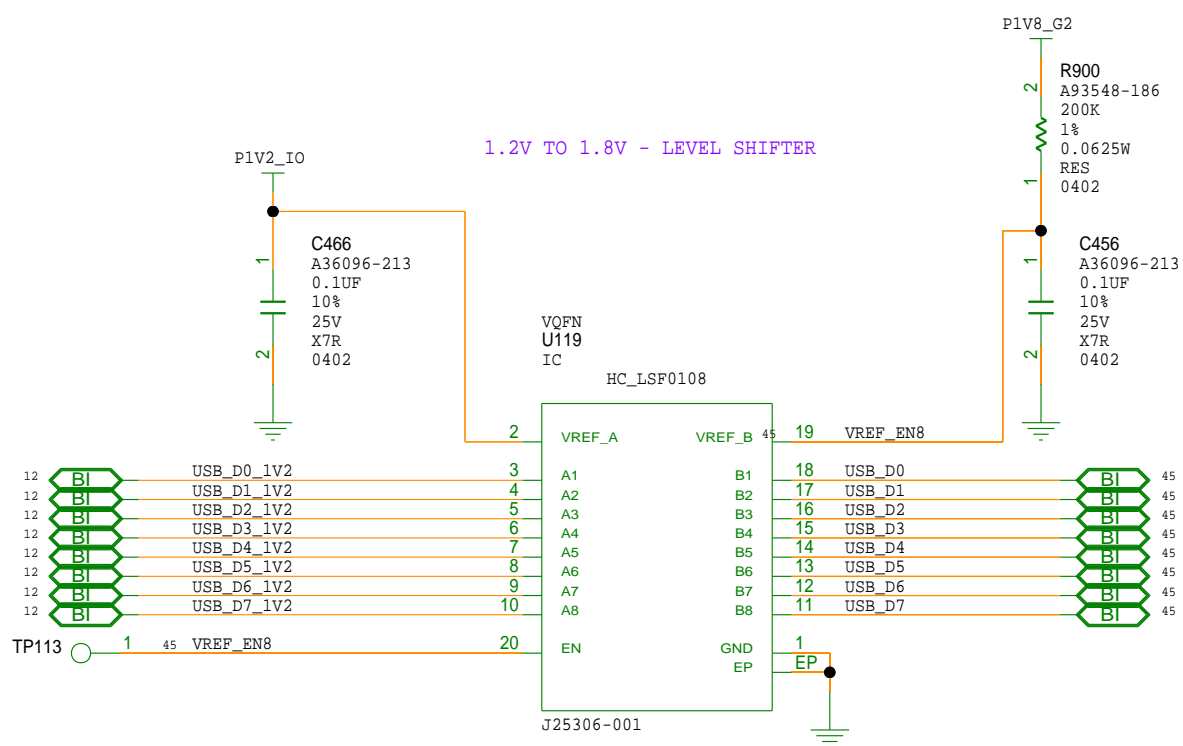
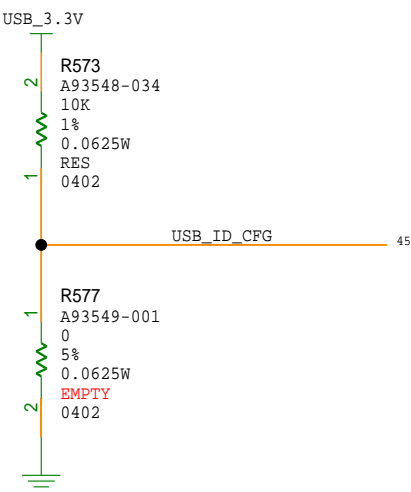
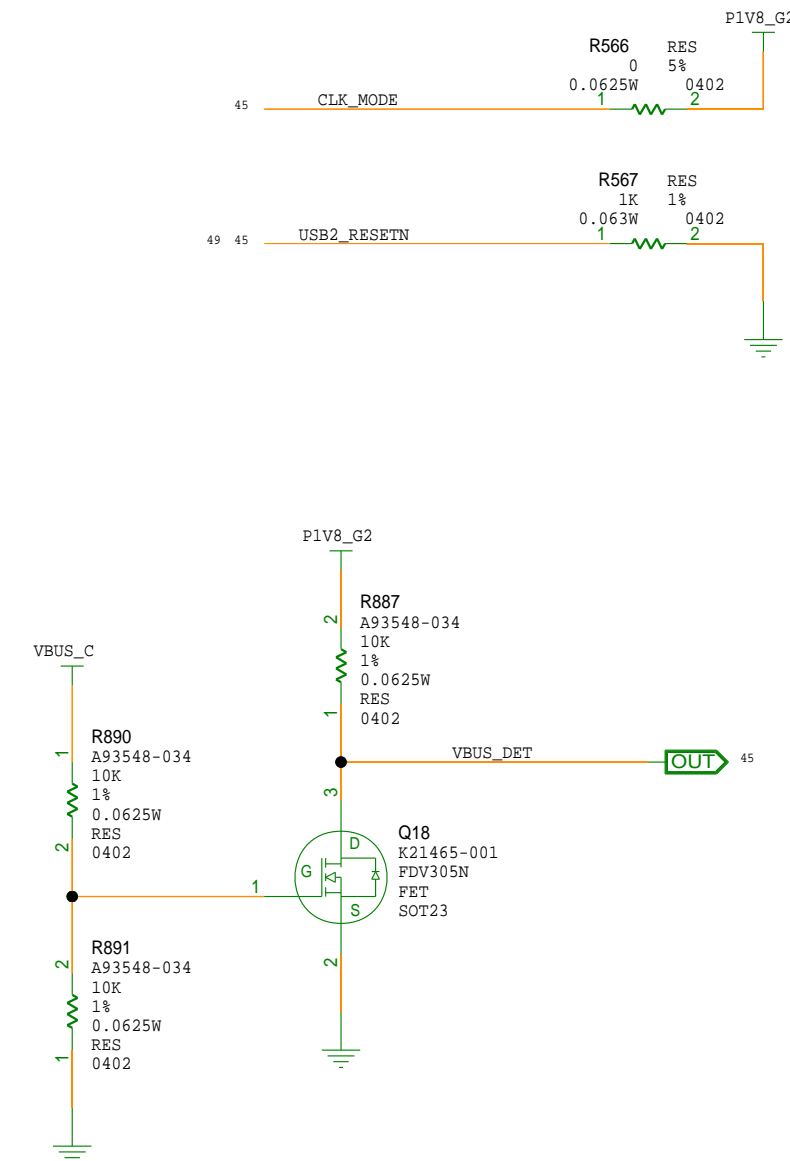
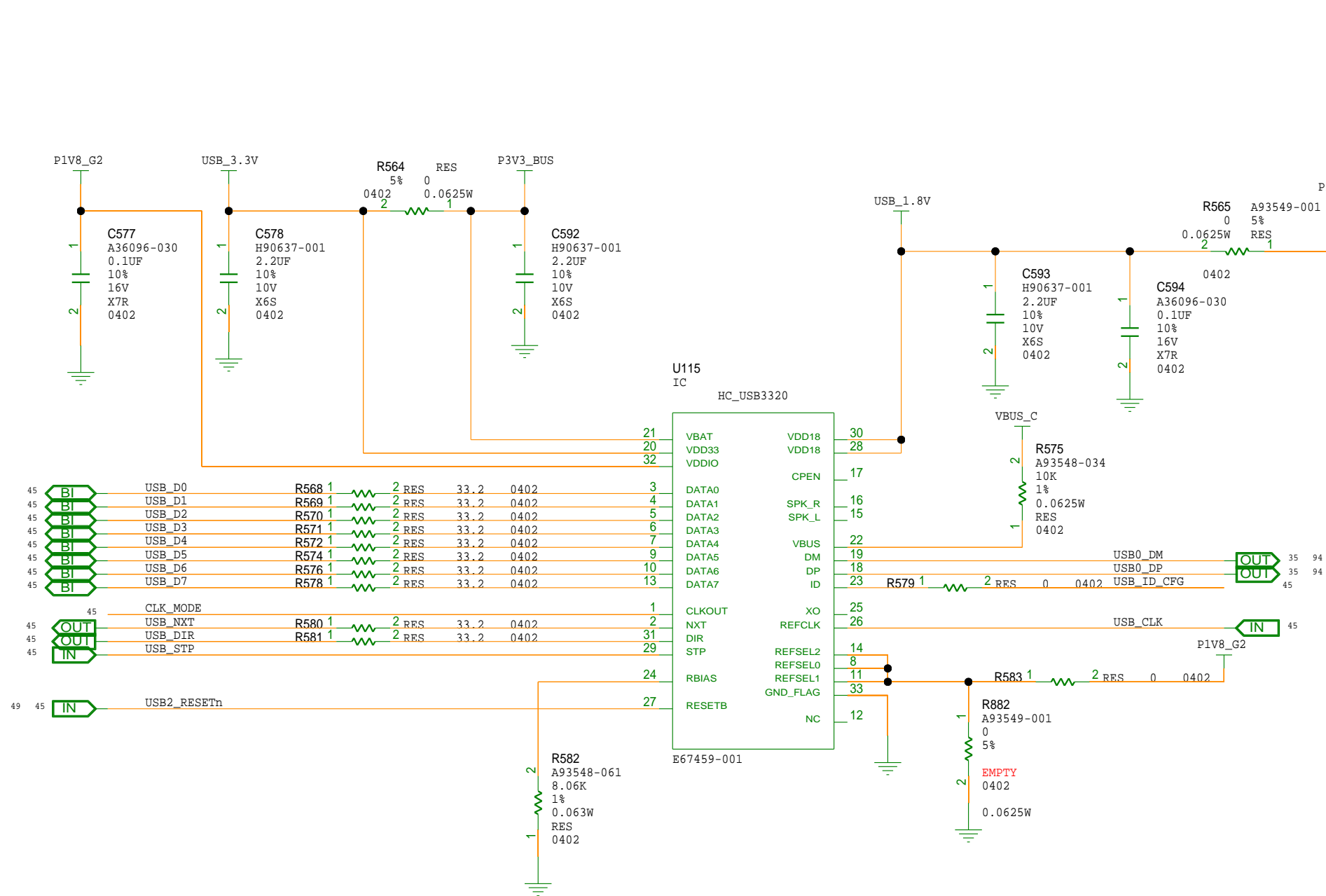
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USB2.0



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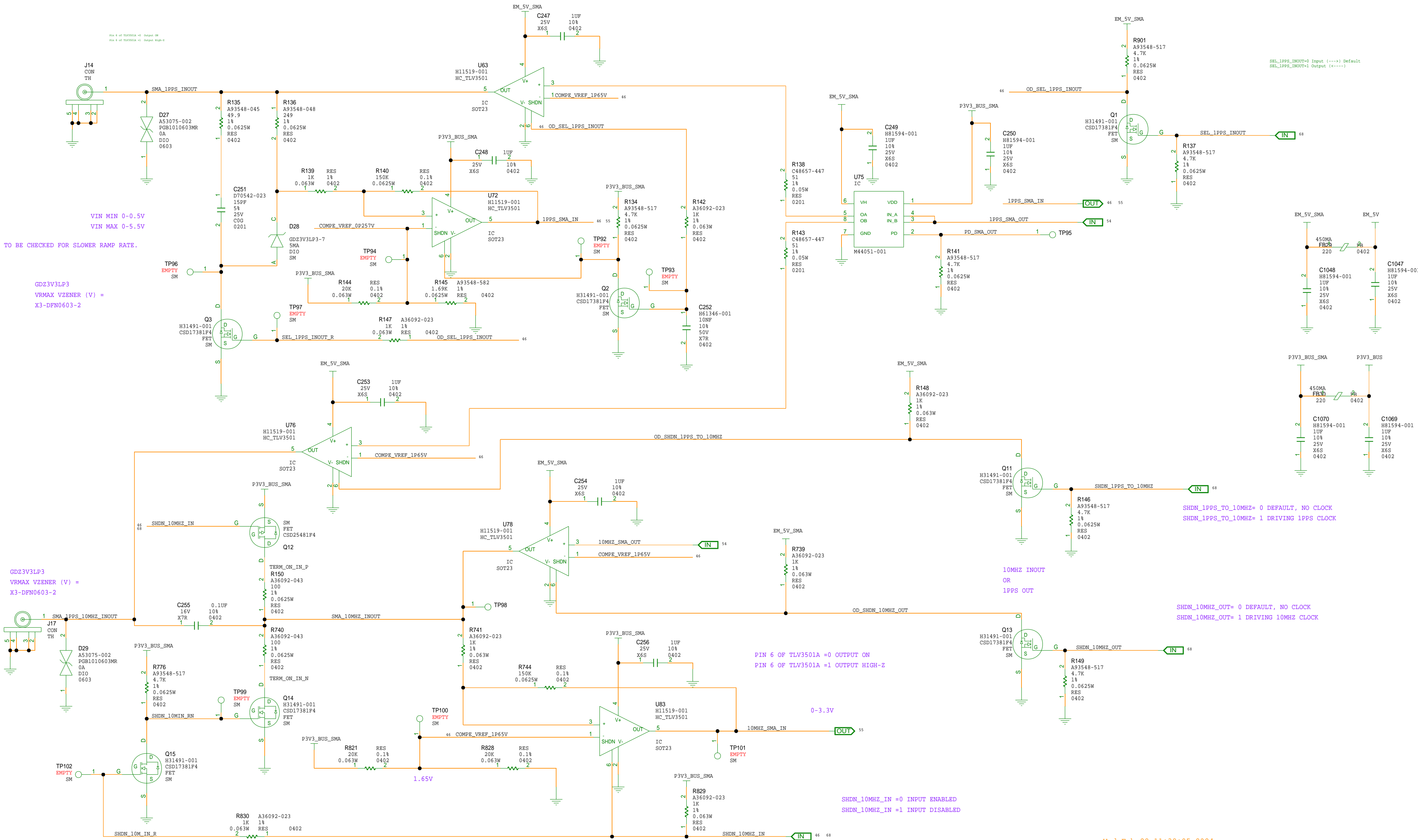
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1PPS INOUT



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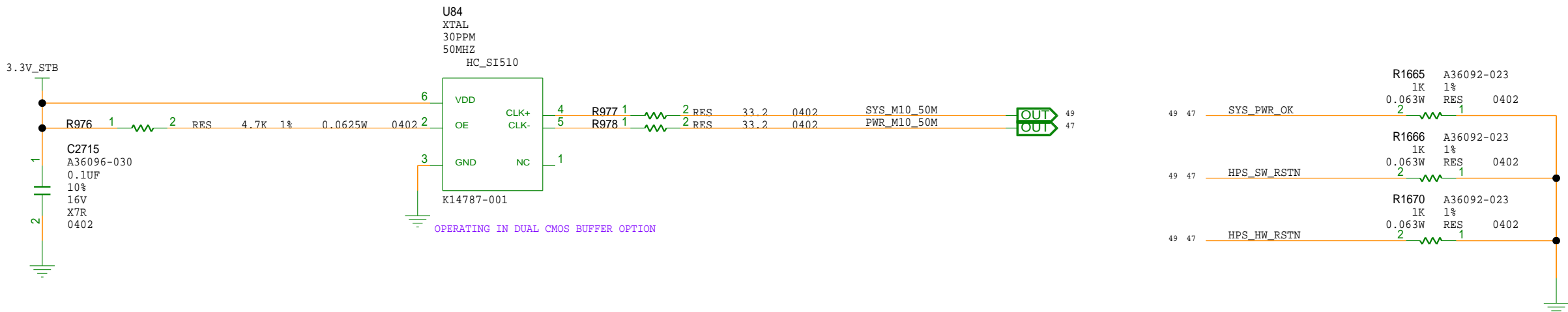
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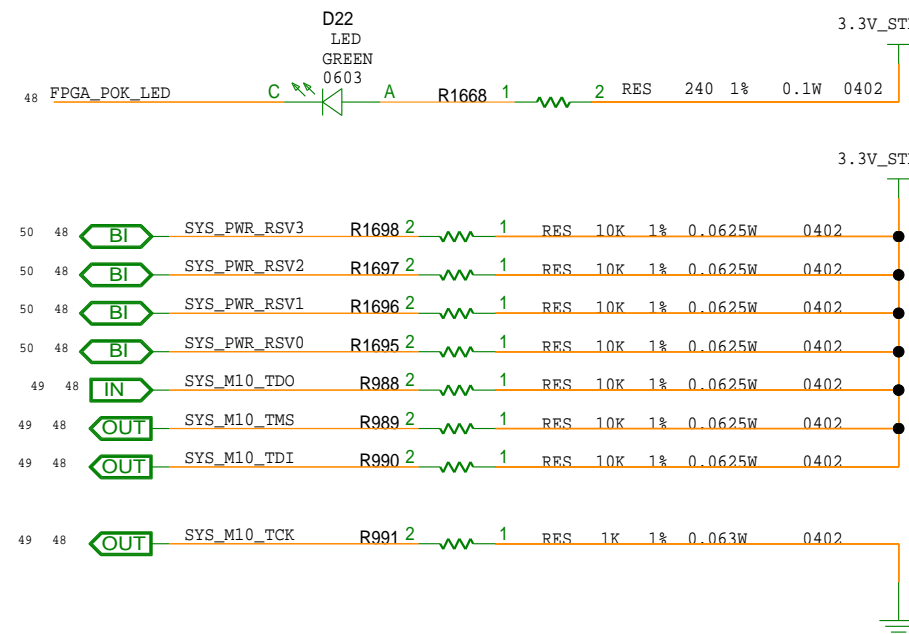
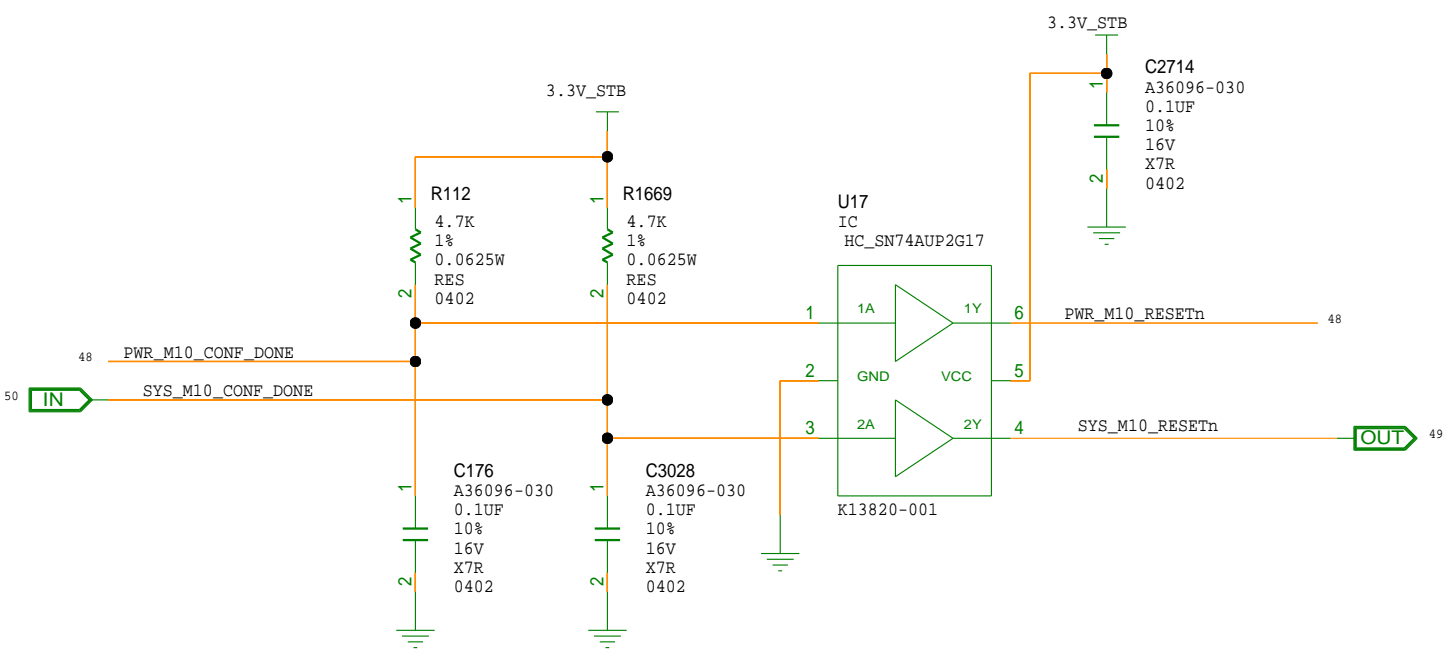
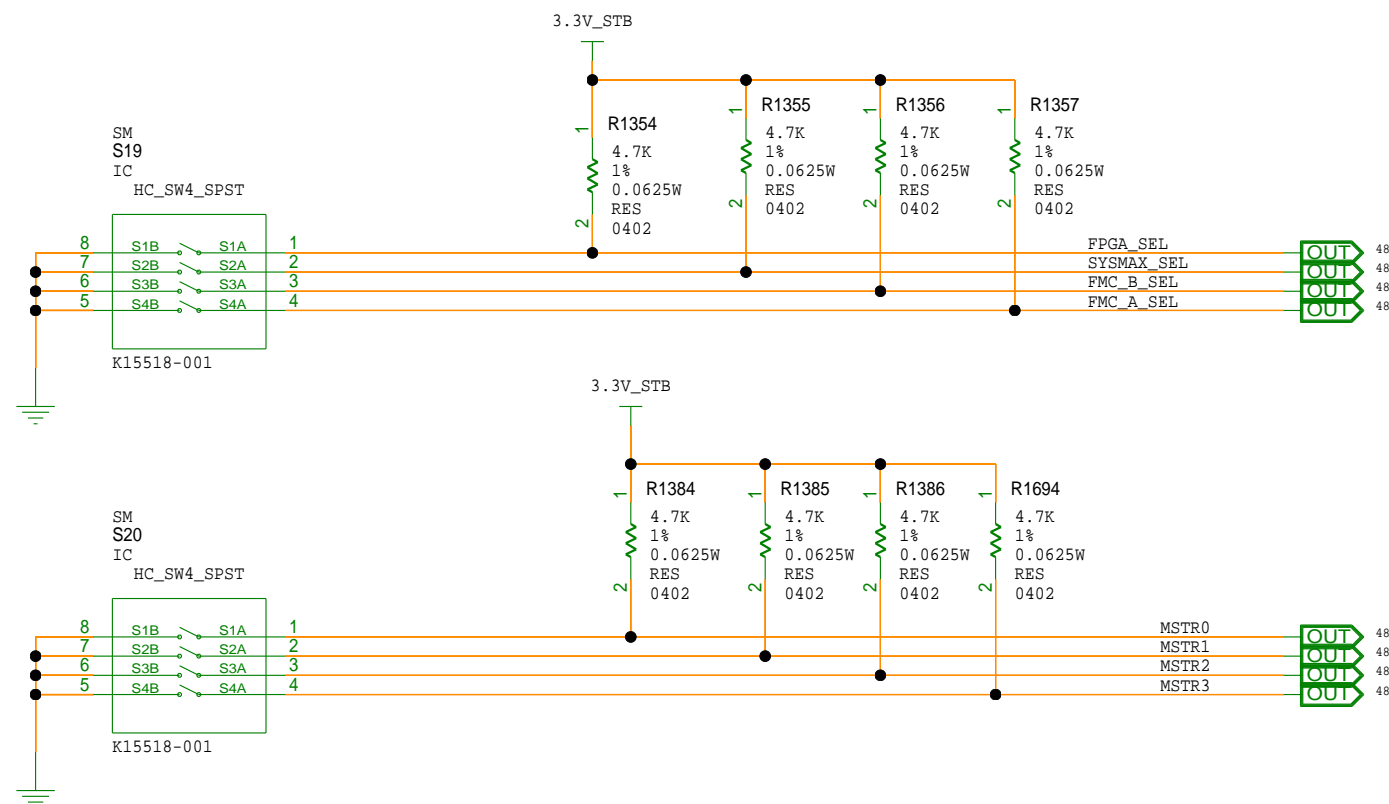
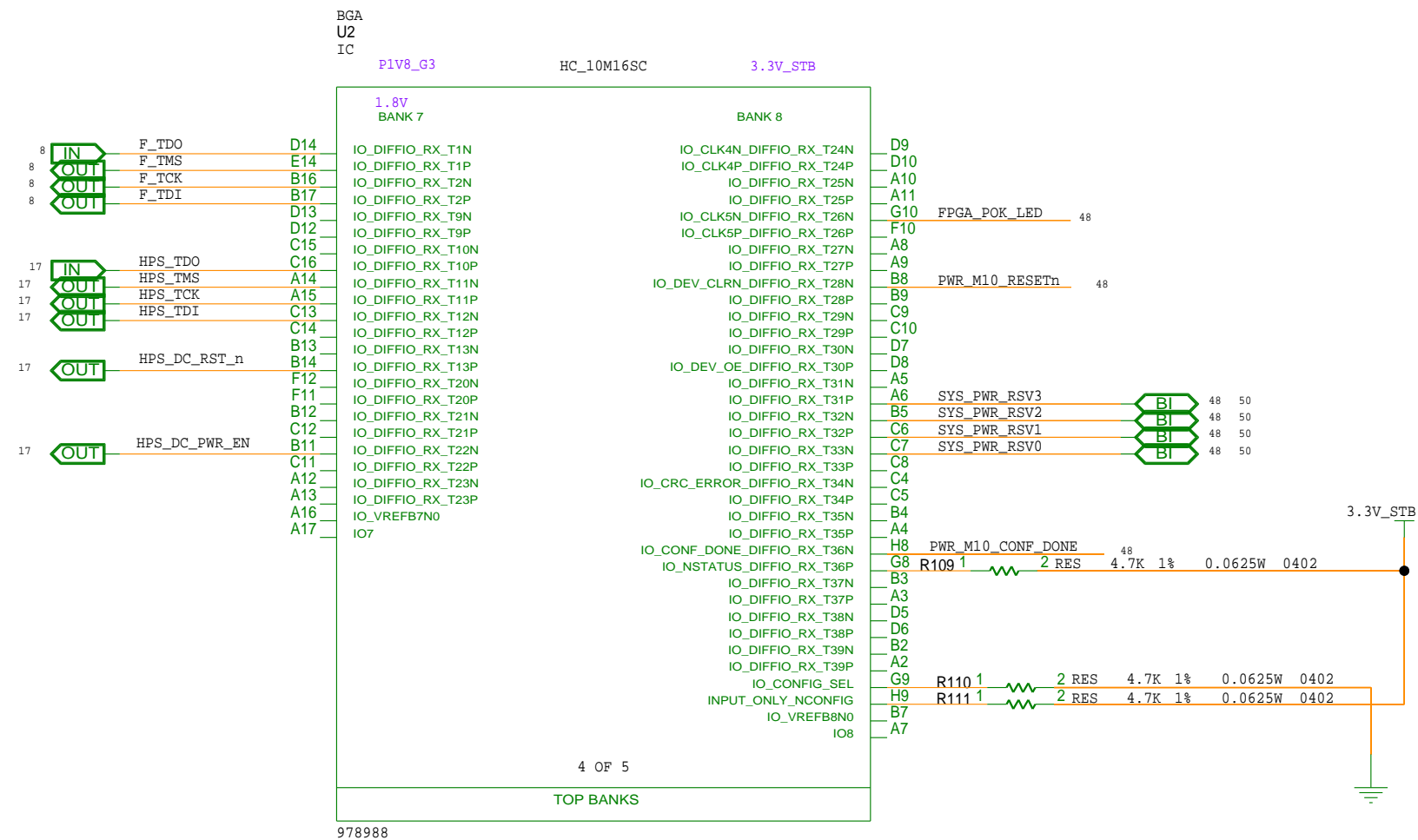
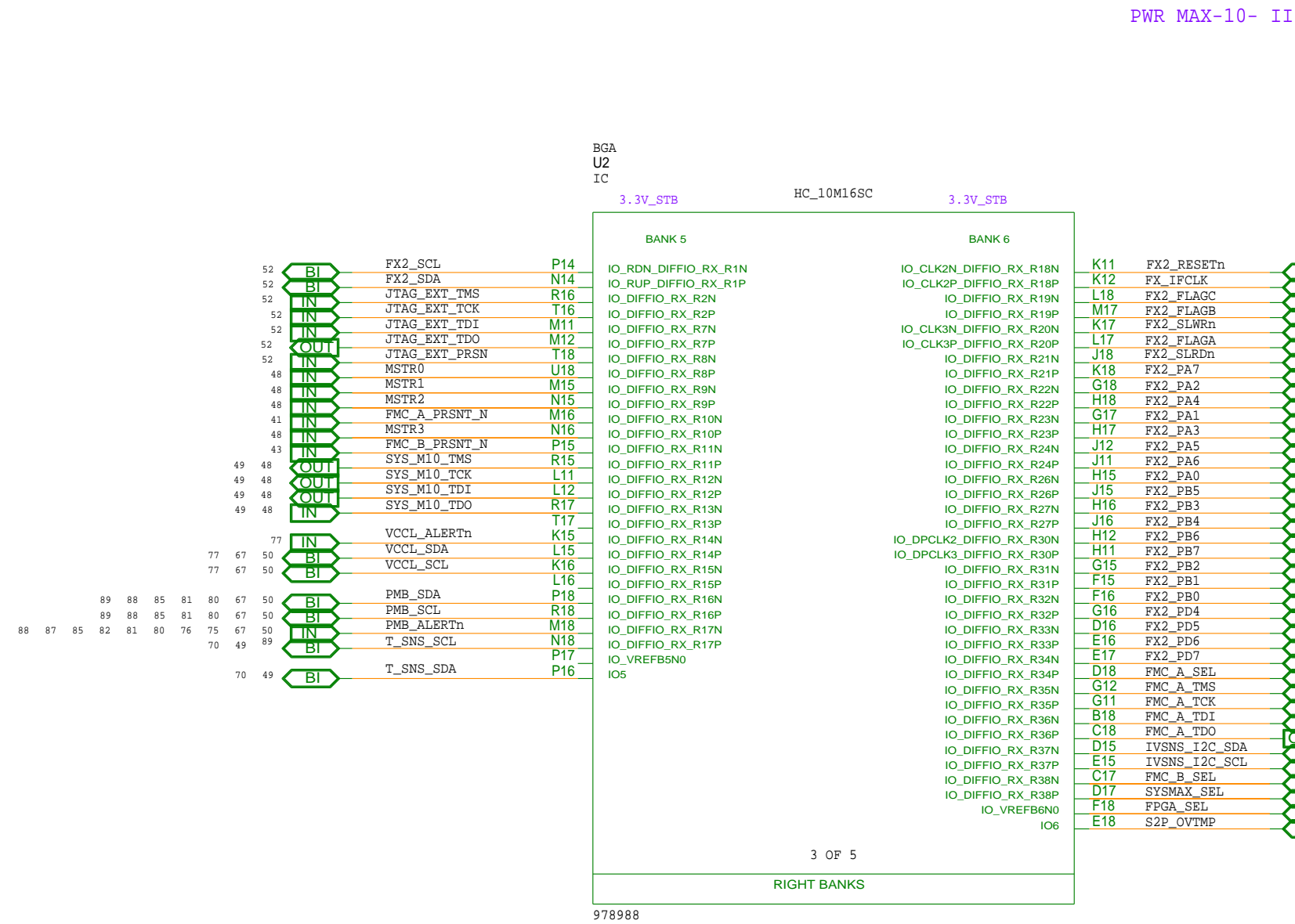
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PWR MAX-10- I



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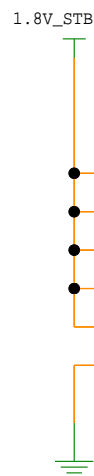
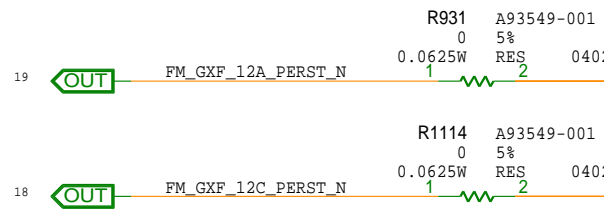
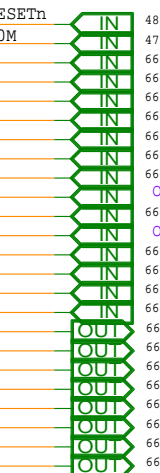
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SYS MAX-10- I



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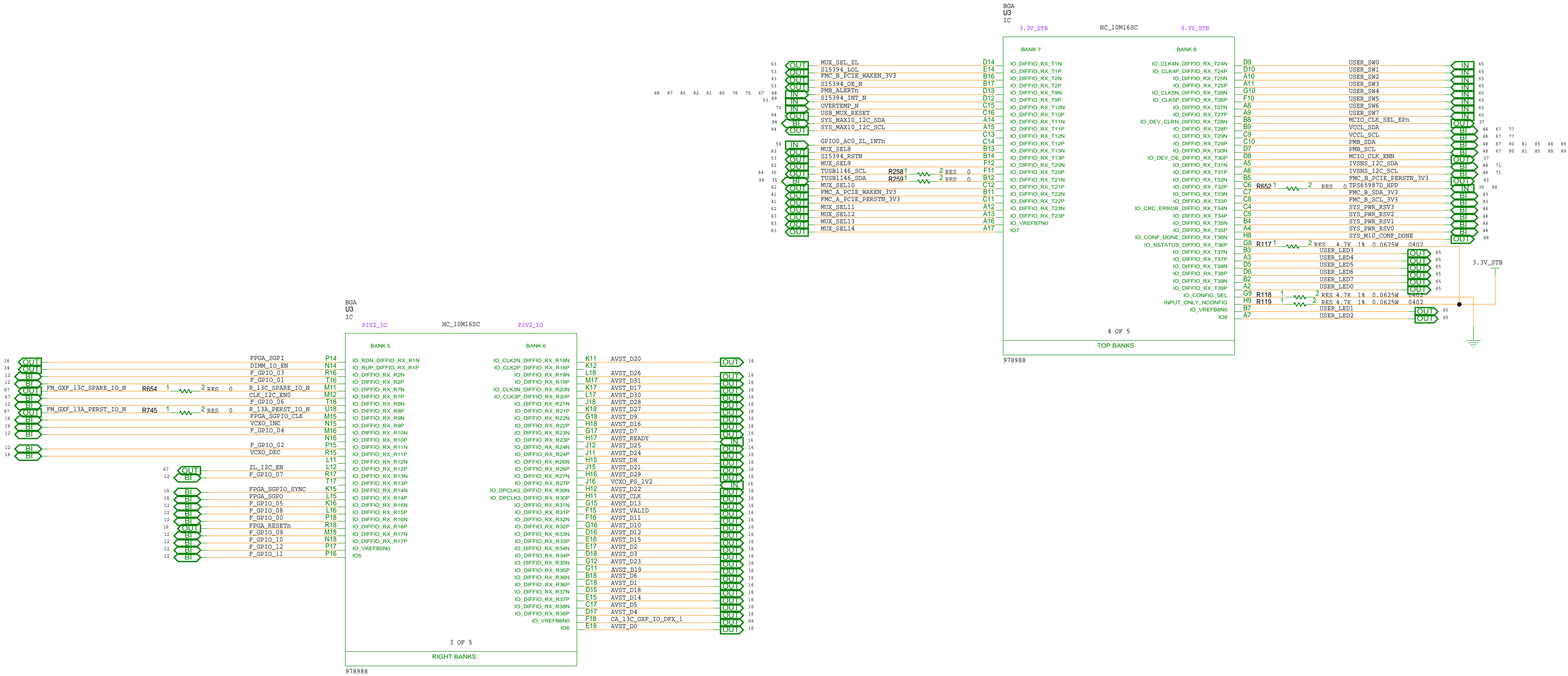
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SYS MAX-10- II



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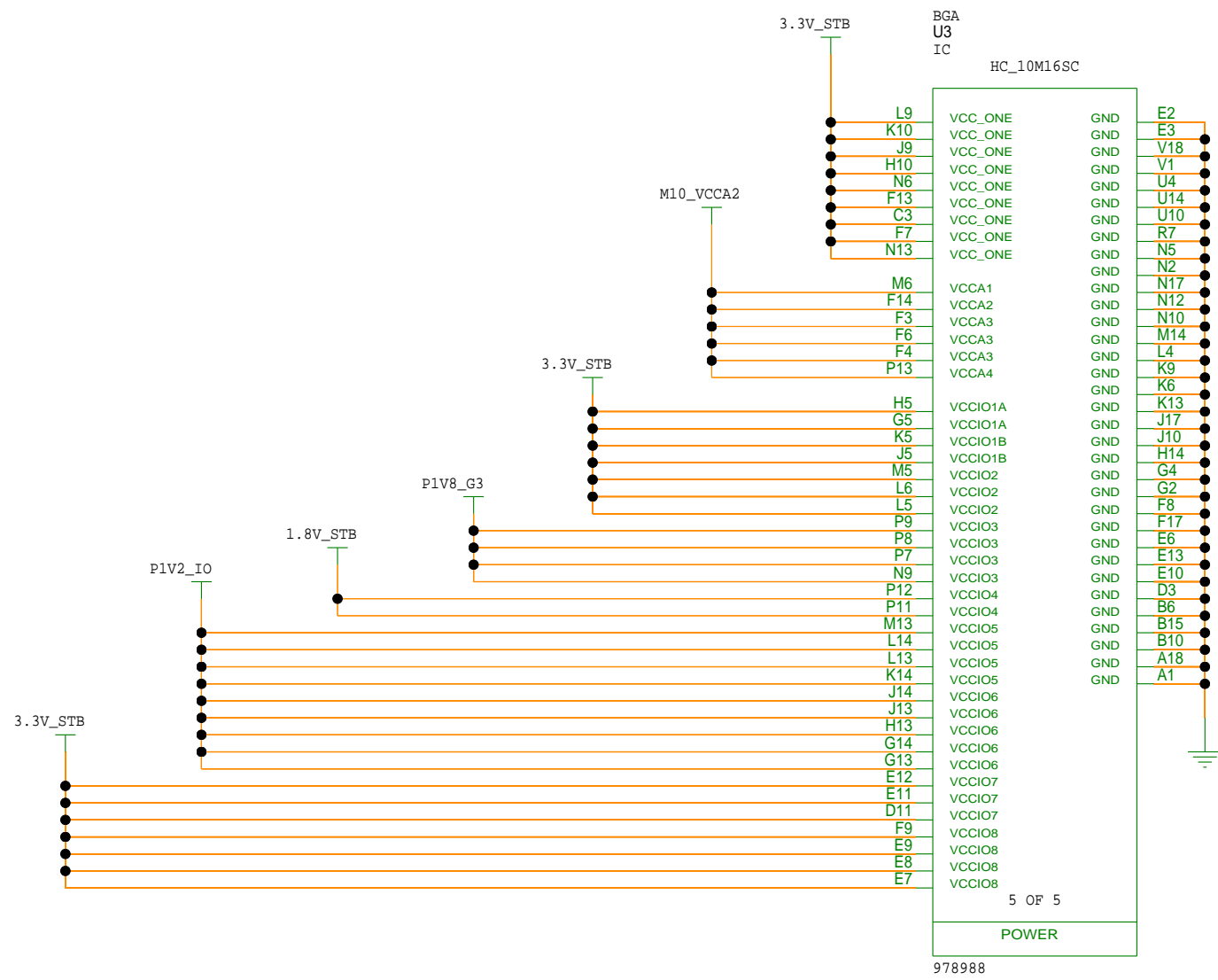
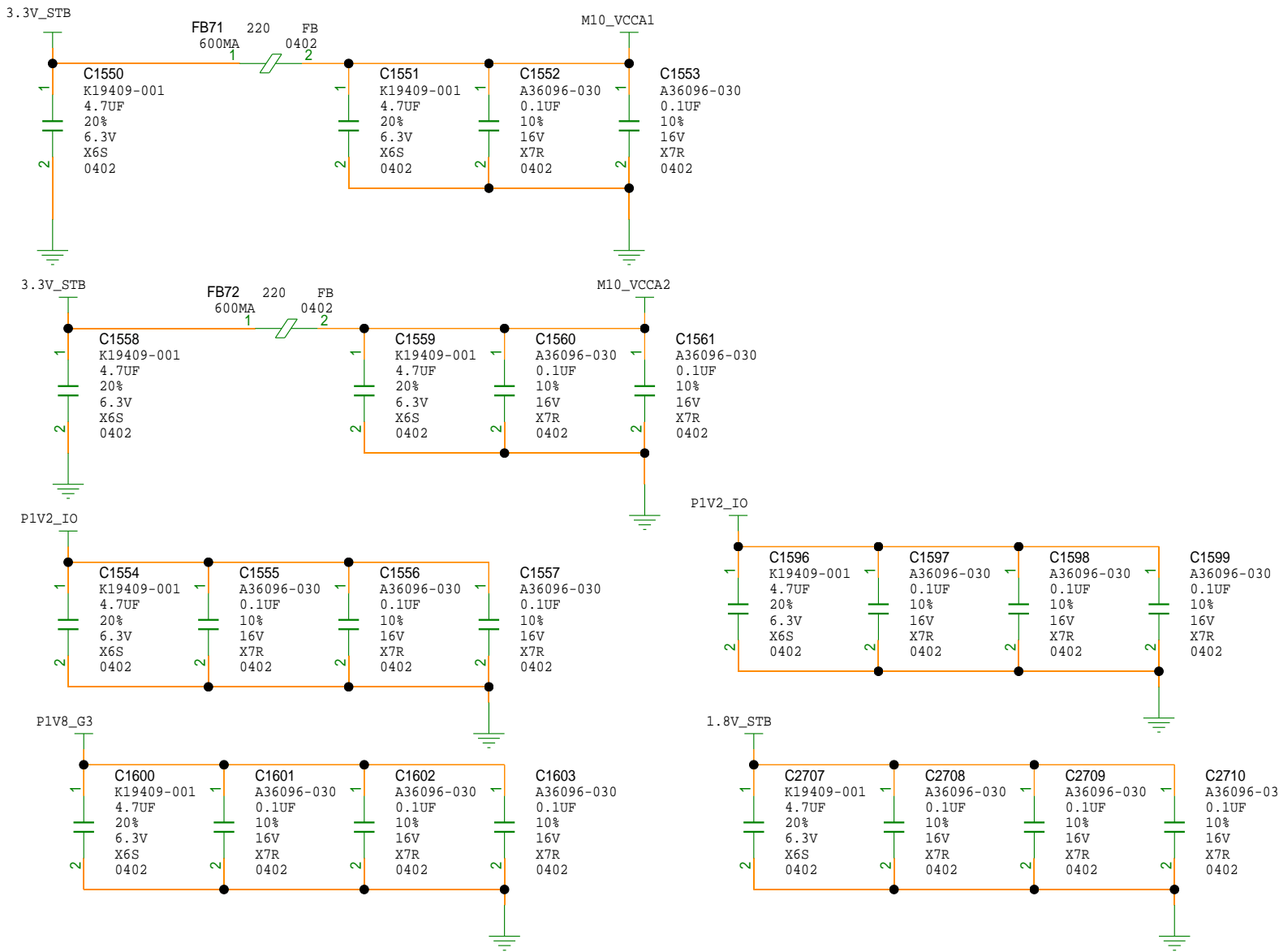
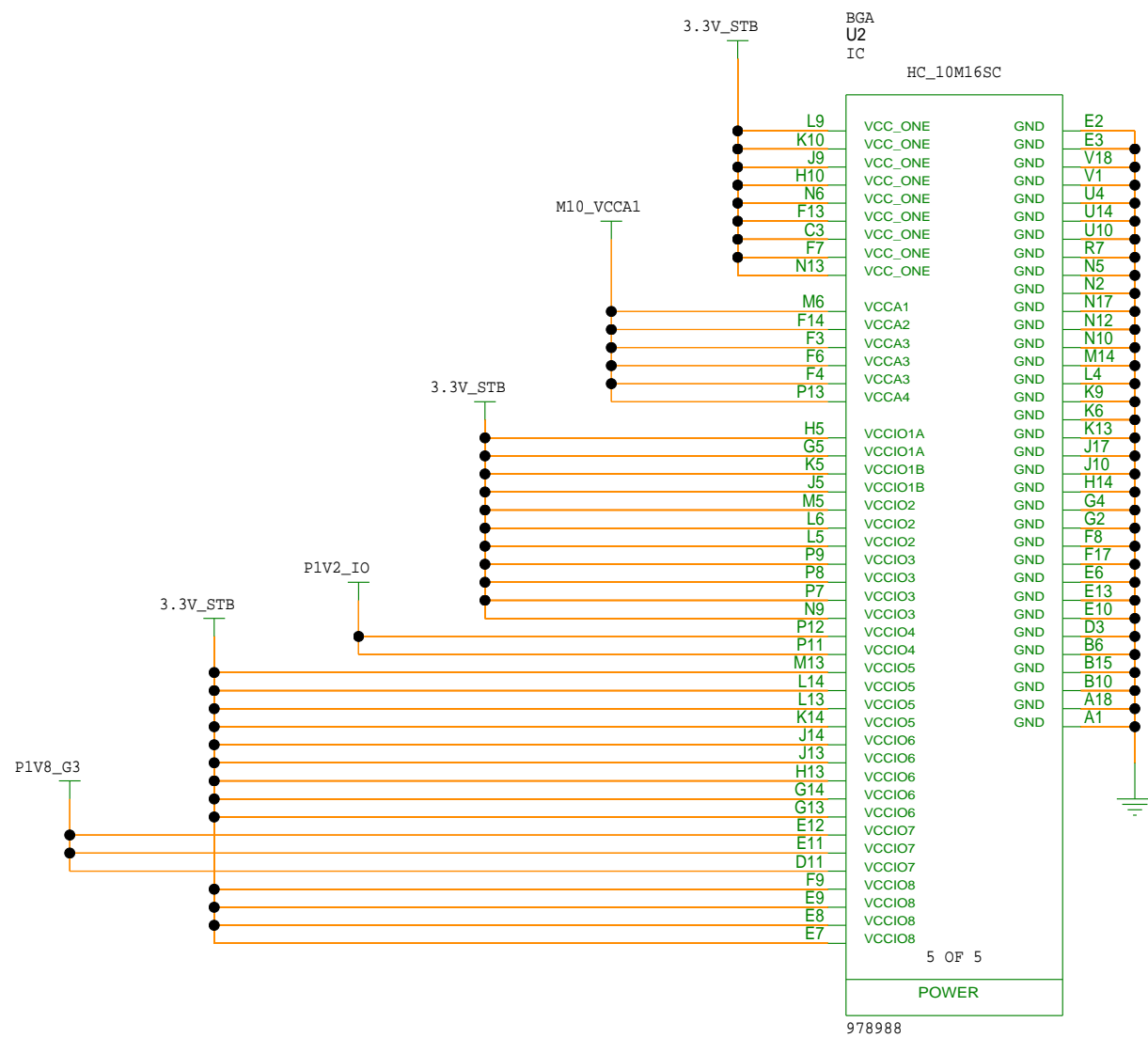
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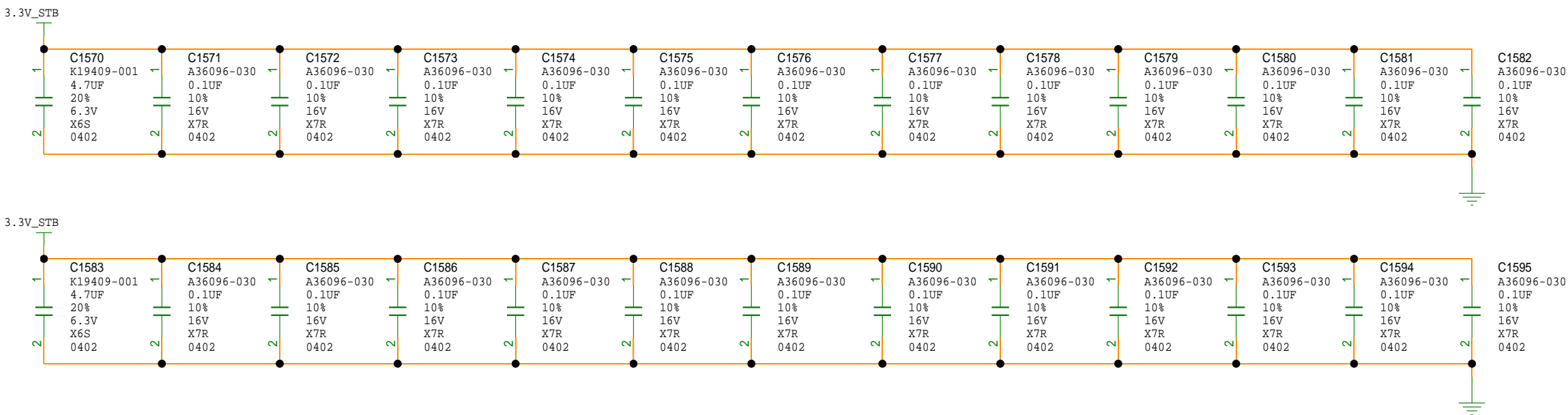
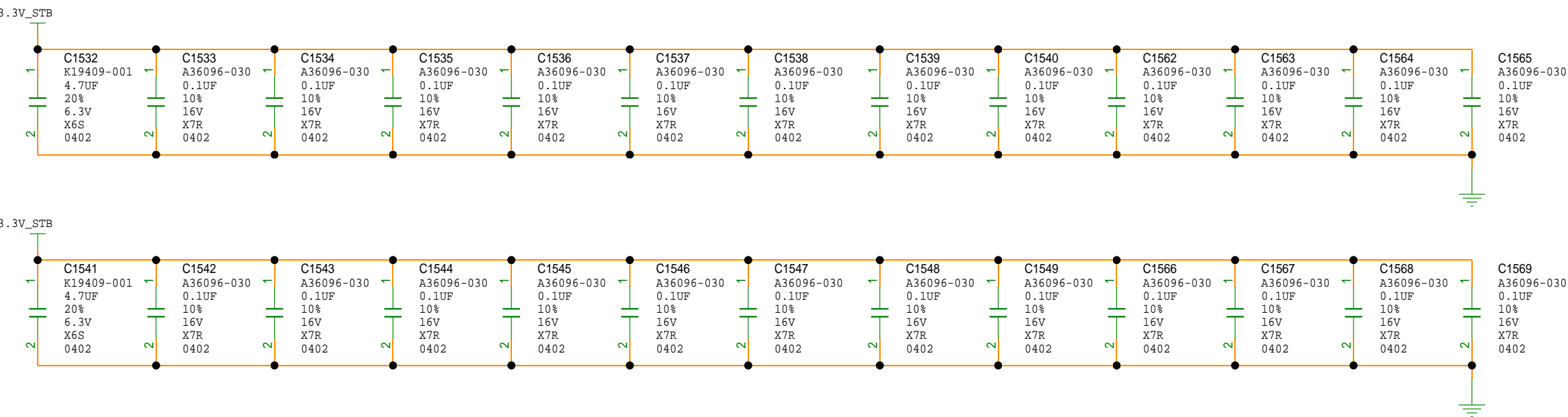
MAX-10 POWER

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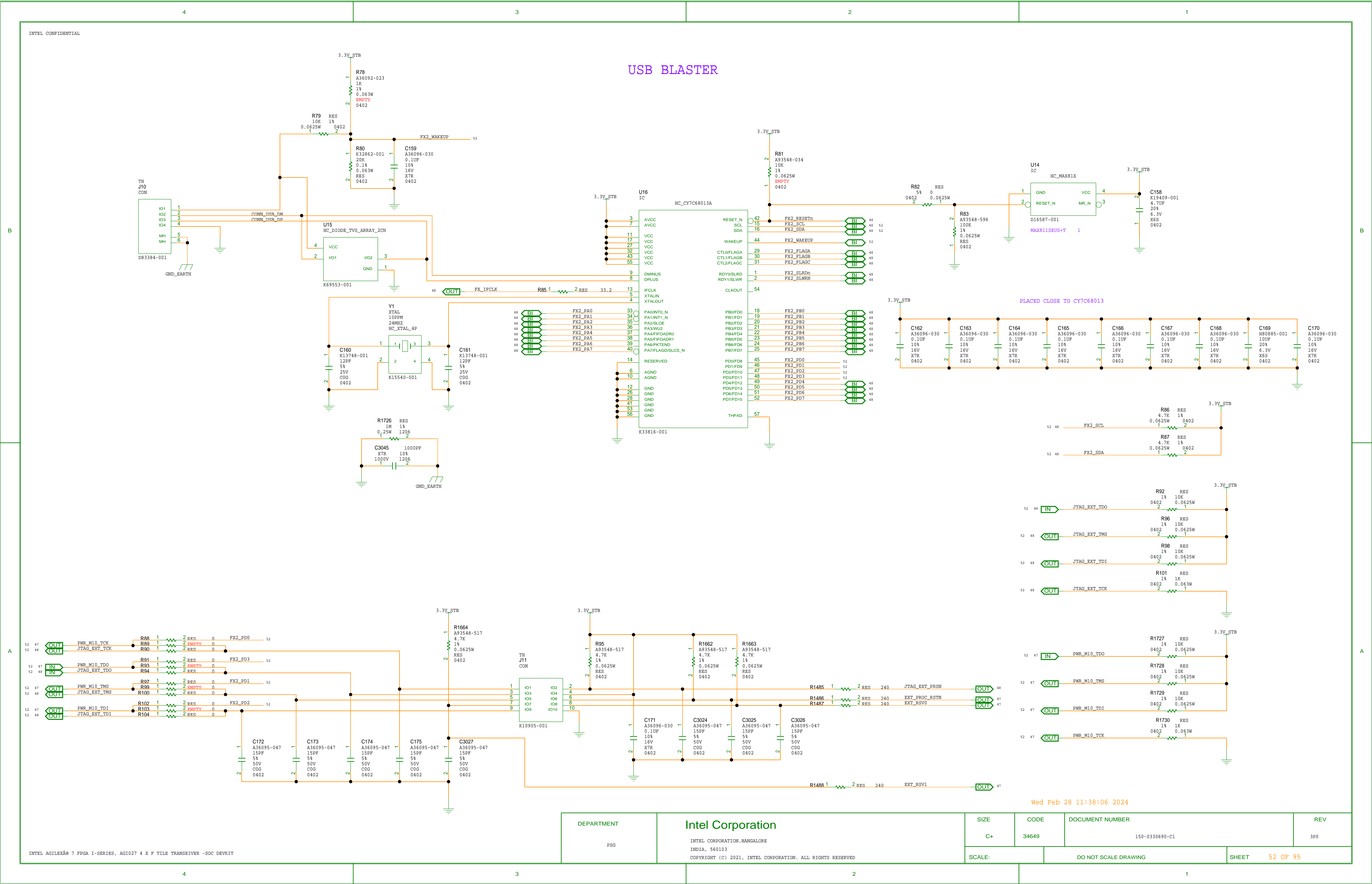
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USB BLASTER



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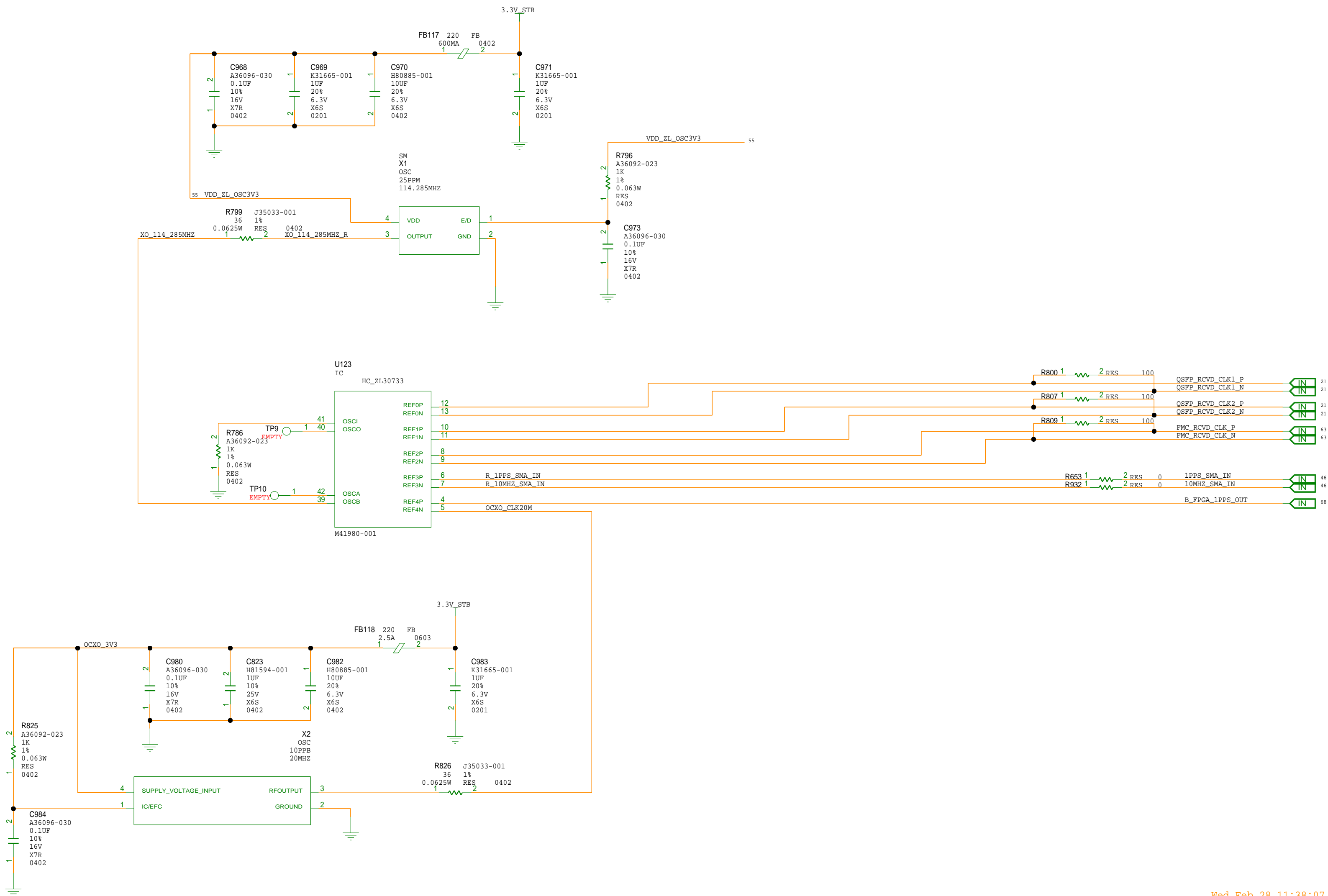
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SI5394 CLOCK GENERATOR



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ZL30733 PLL CLOCK GENERATOR-2



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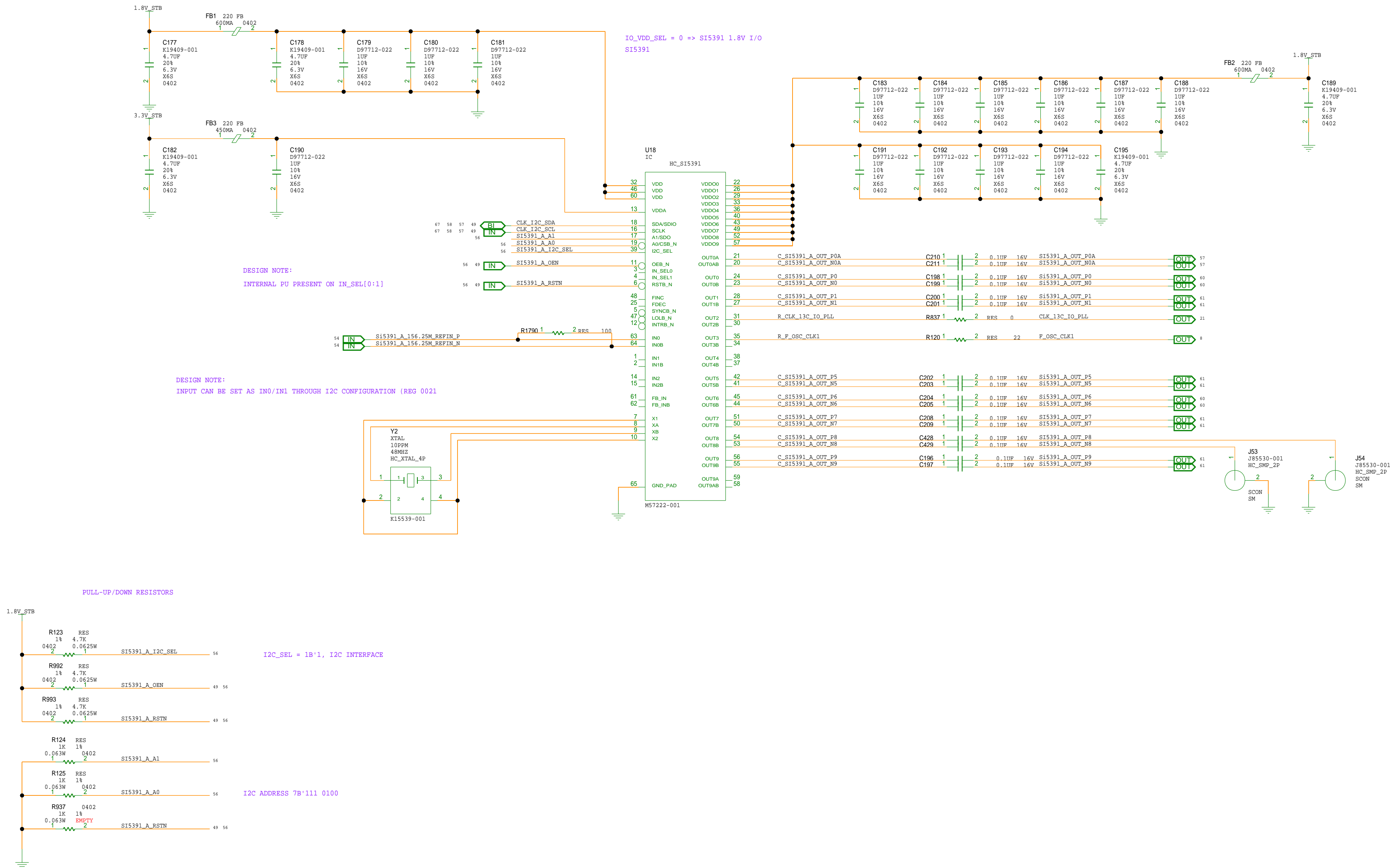
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SI5391 CLOCK GENERATOR-I



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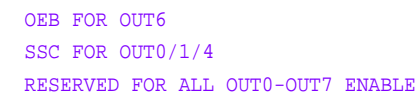
56 OF 95

SI5391 CLOCK GENERATOR-II



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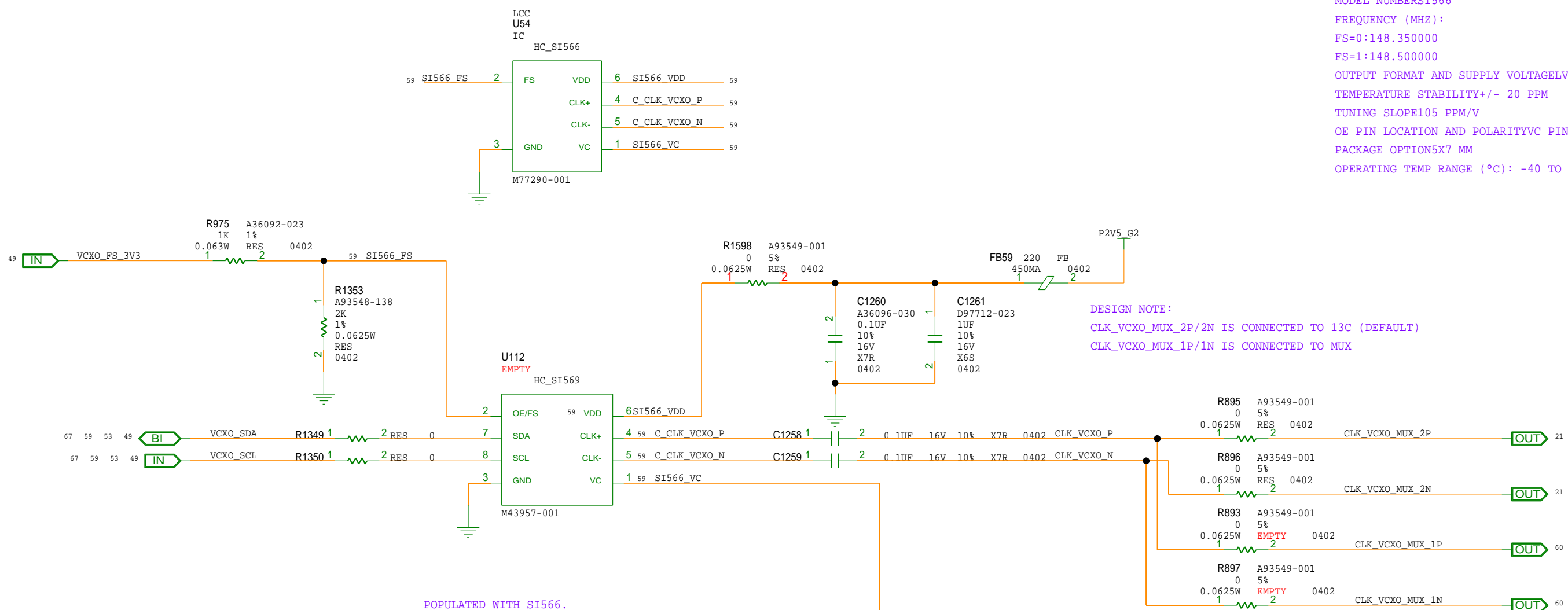
SI5332 CLOCK GENERATOR



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VCXO

DESIGN NOTE:
CLK_VC XO_MUX_2P/2N IS CONNECTED TO 13C (DEFAULT)
CLK_VC XO_MUX_1P/1N IS CONNECTED TO MUX

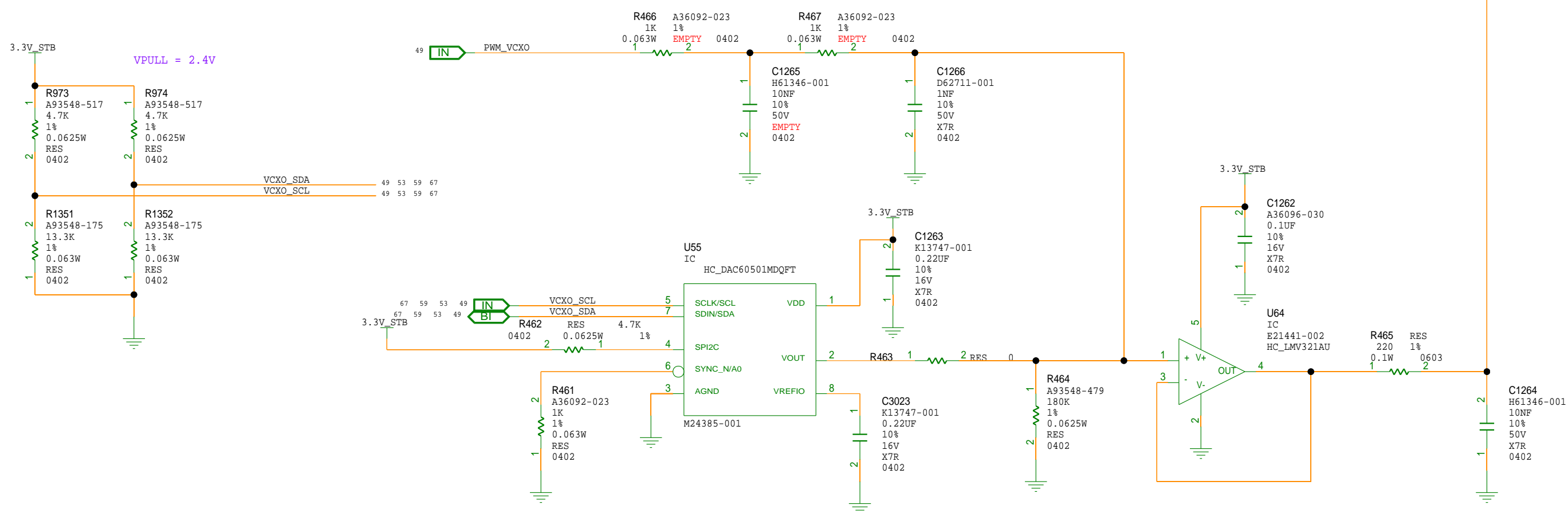


```

POPULATED WITH SI566.
FS CONTROL BY MAX10
FS=0: 148.35MHZ
FS=1: 148.50MHZ
I2C ONLY AVAILABLE IF SI569 IS POPULATED.

```

DESIGN NOTE:
CLK_VCXO_MUX_2P/2N IS CONNECTED TO 13C (DEFAULT)
CLK_VCXO_MUX_1P/1N IS CONNECTED TO MUX



I2C ADDRESS 7B'100_1000

DEFAULT MIDRANG, $2.5V/2$, NO OFFSET FROM THE $VDD/2$ OF THE VCXO INPUT

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CLOCK MUX-I

CAD NOTE:

PLACE AS FOUR-PAD RESISTOR, TO AVOID ANY STUB

CAD NOTE:

PLACE AS TRI-PAD WITH AC_CAP TO AVOID ANY STUB

CAD NOTE:

PLACE AS TRI-PAD RESISTOR, TO AVOID ANY STUB

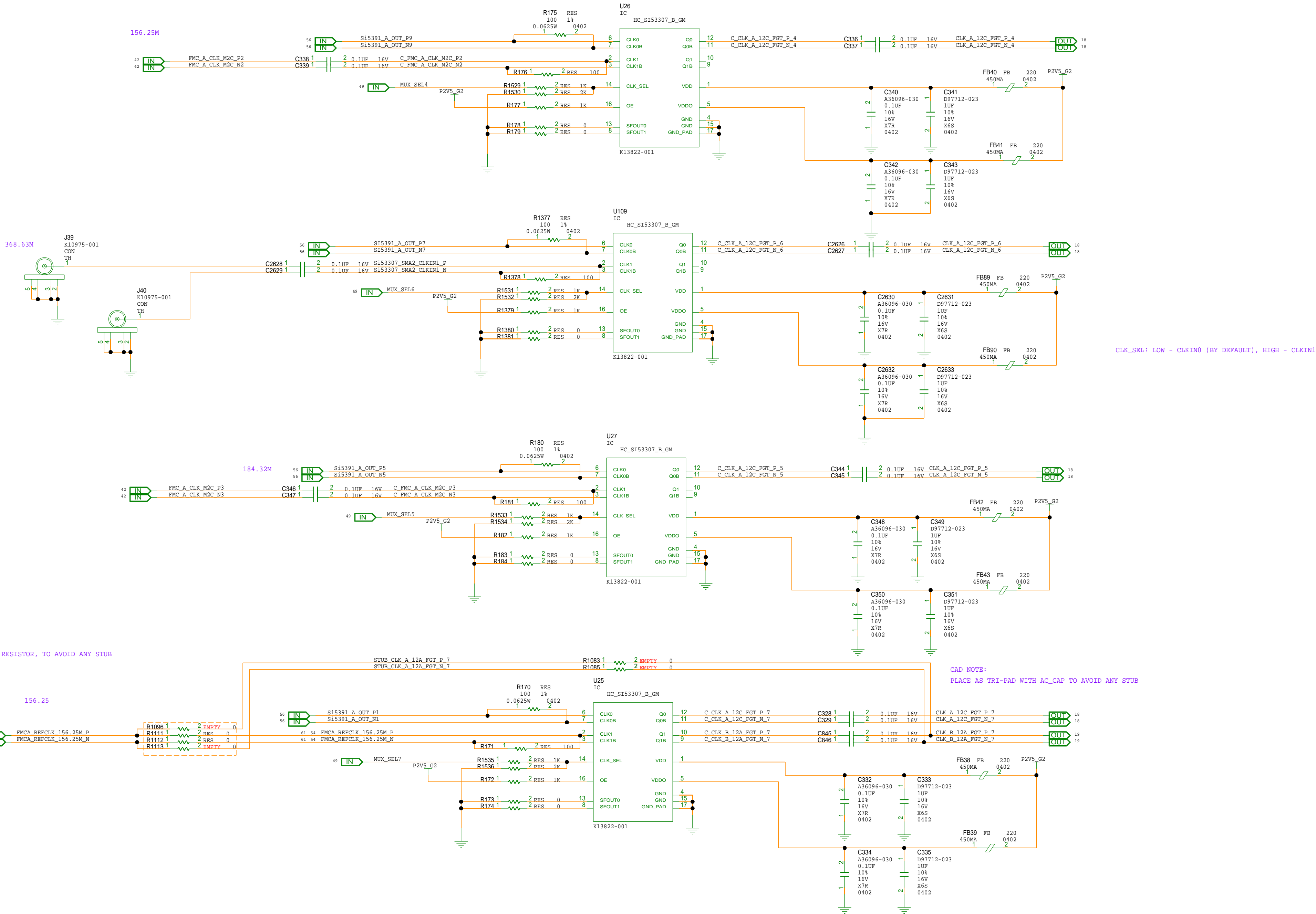
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CLOCK MUX-II



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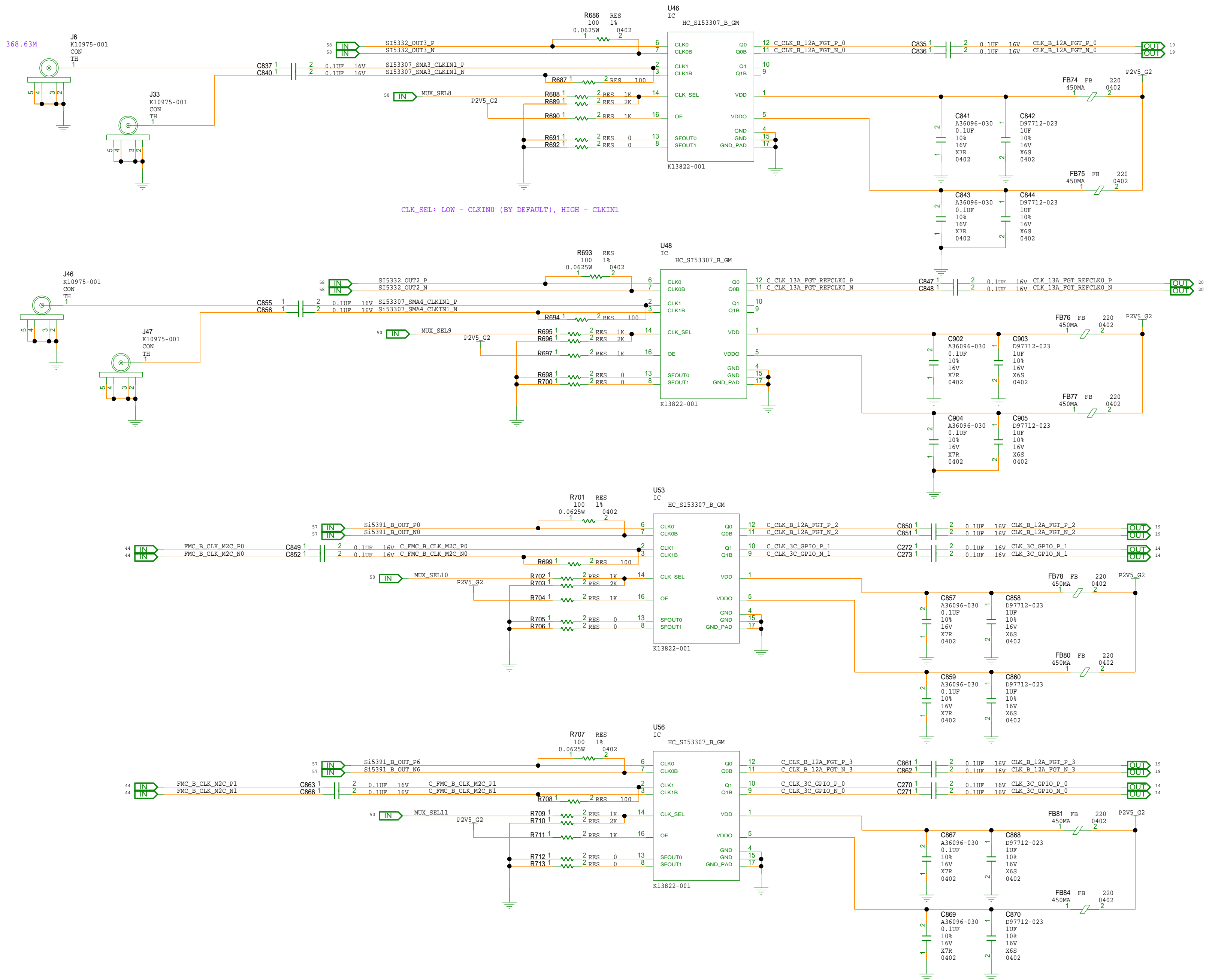
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CLOCK MUX-III



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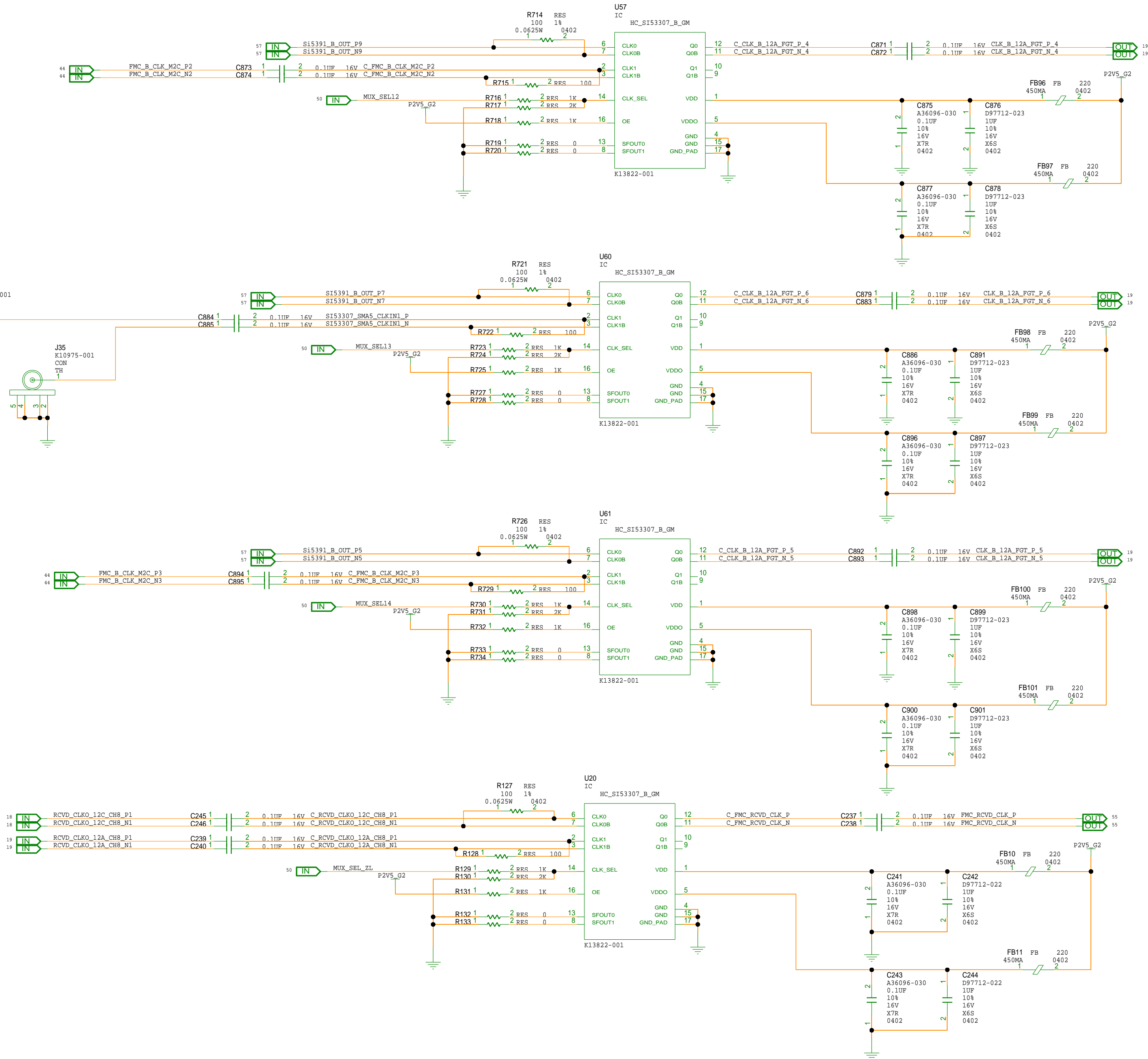
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CLOCK MUX-IV

CLK_SEL: LOW - CLKINO (BY DEFAULT), HIGH - CLKINI



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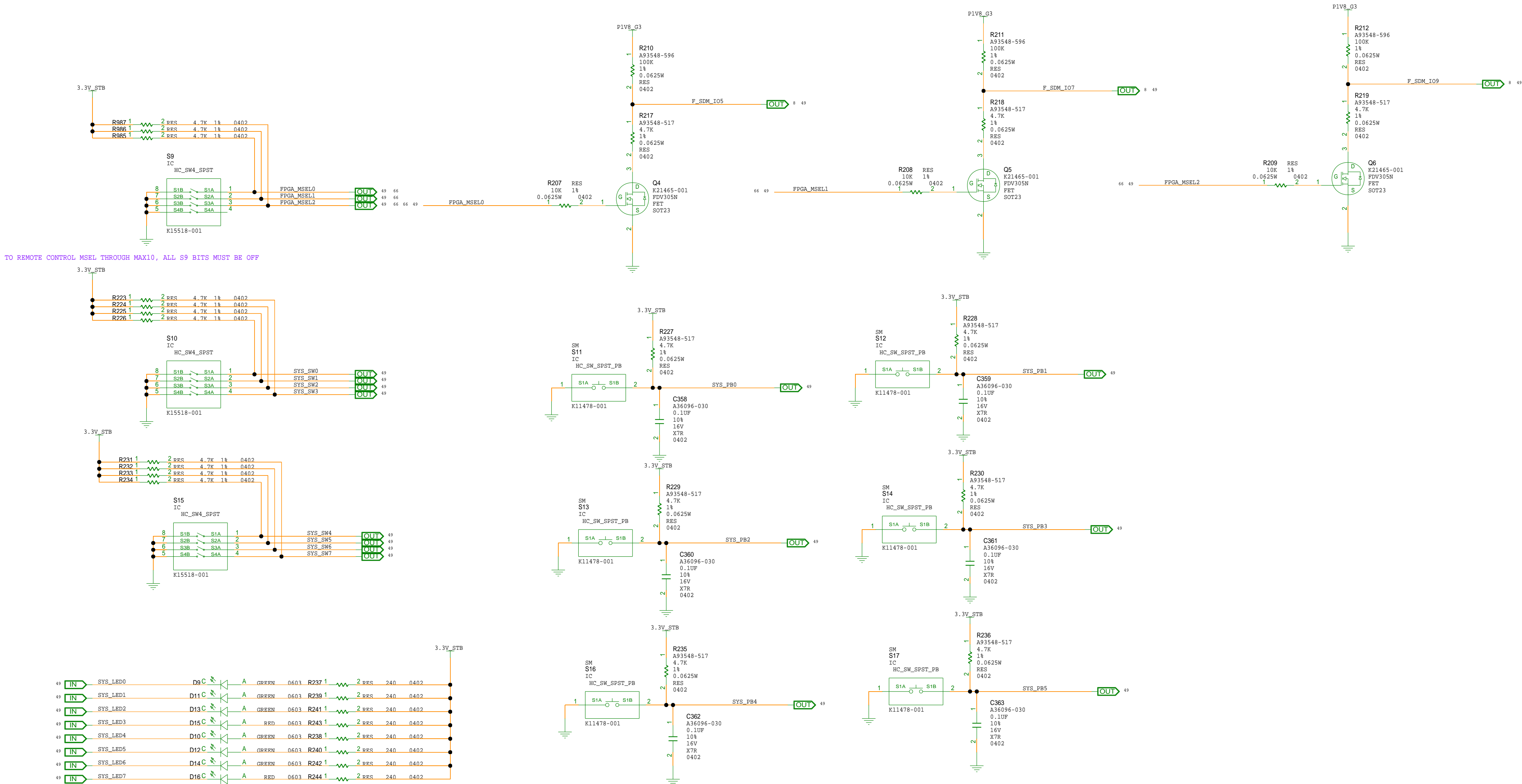
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DIP SWITCH, LEDS



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LVL SHIFTER-I

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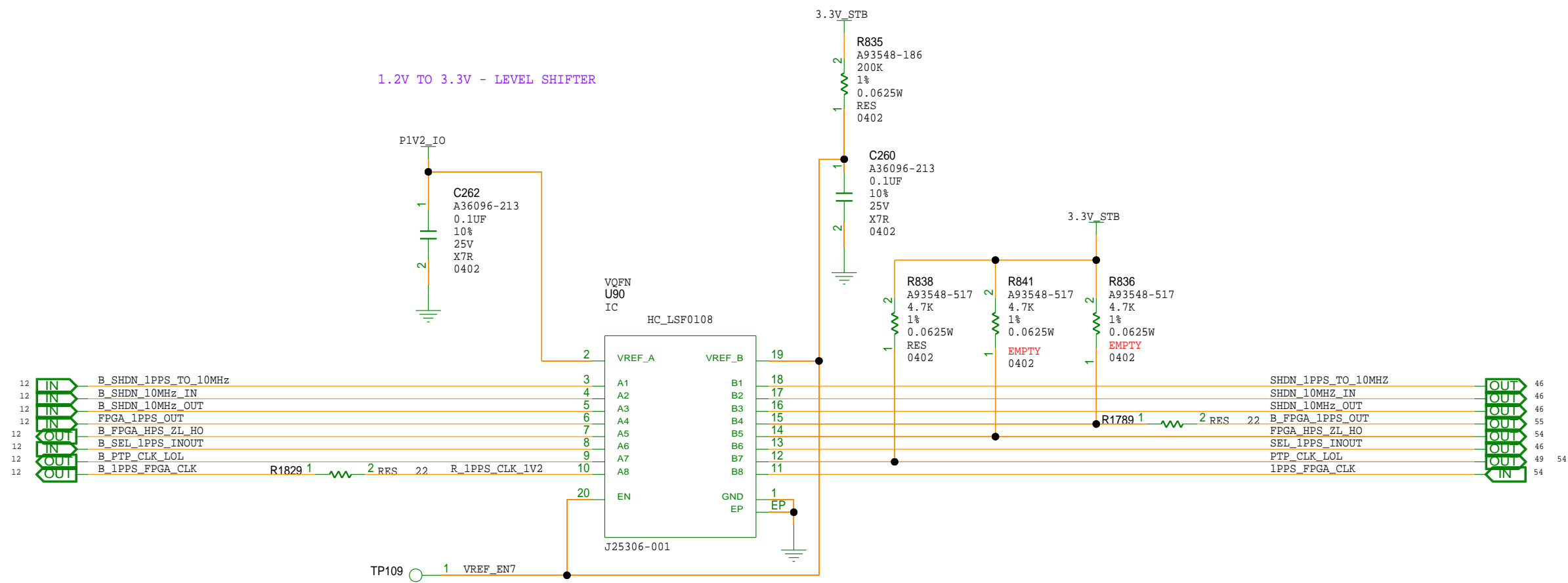
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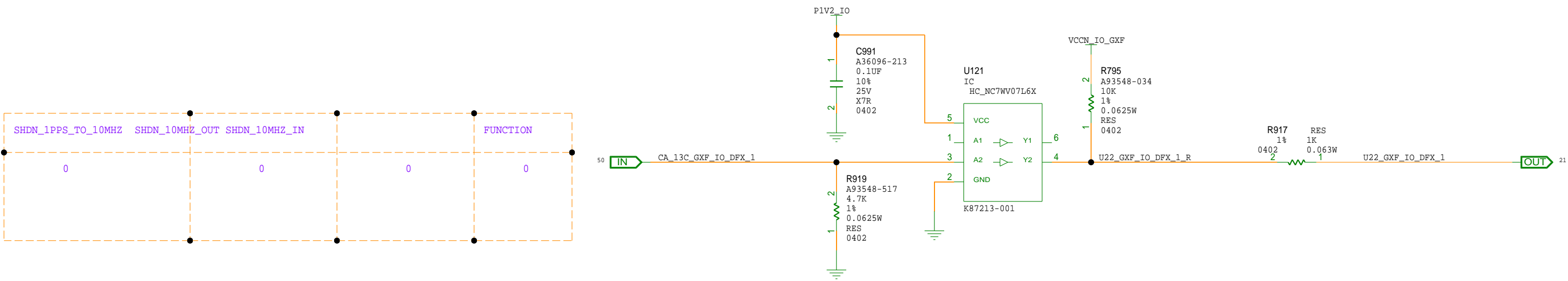
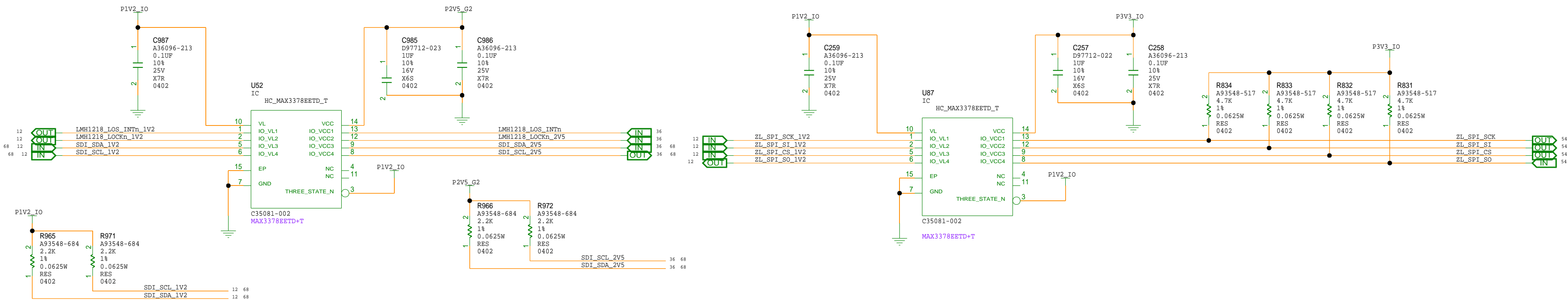
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LVL SHIFTER-II



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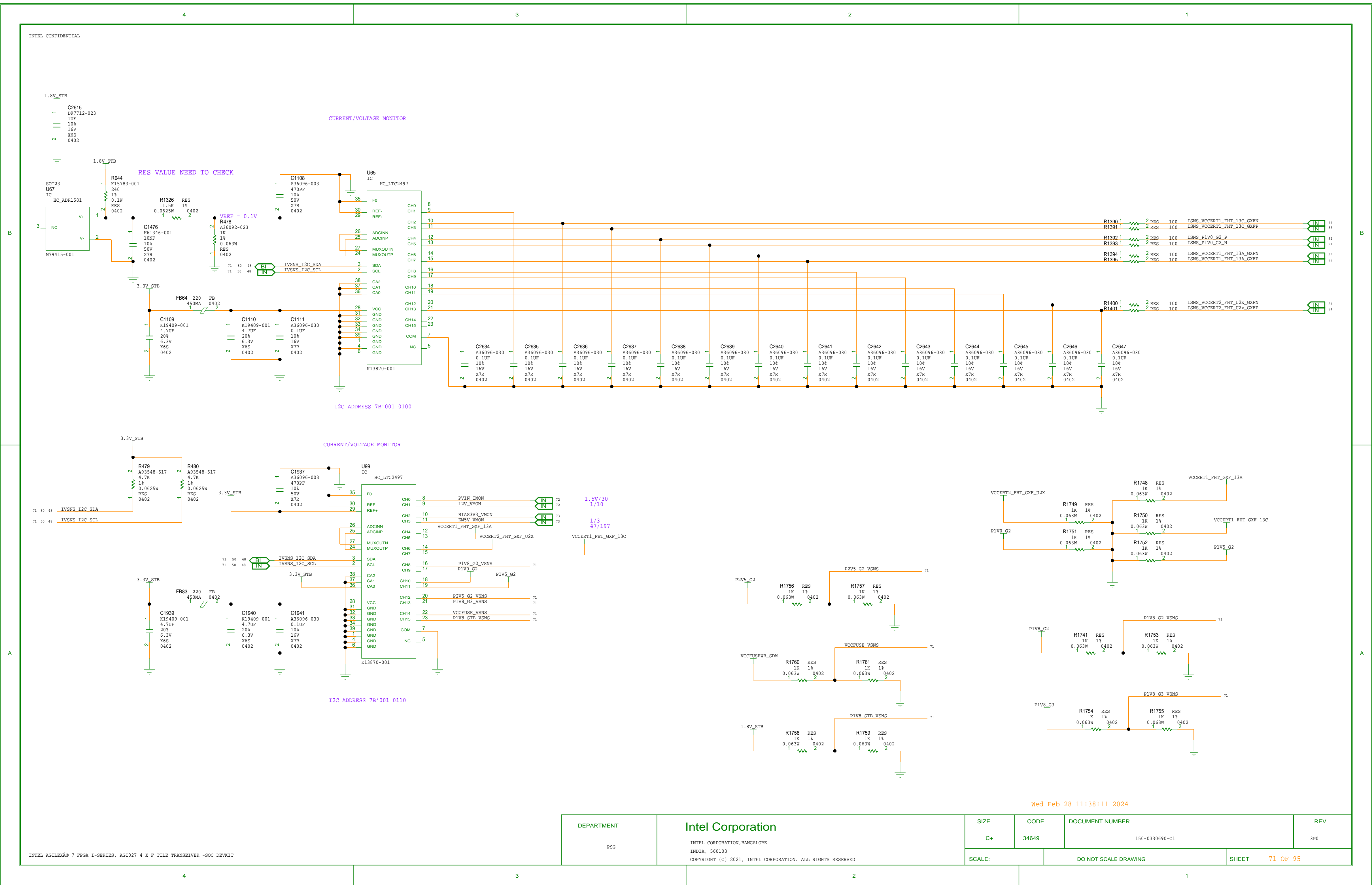
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BOARD TEMP SENSORS

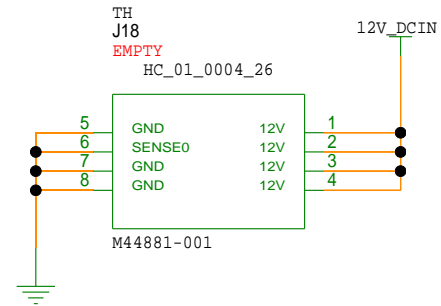
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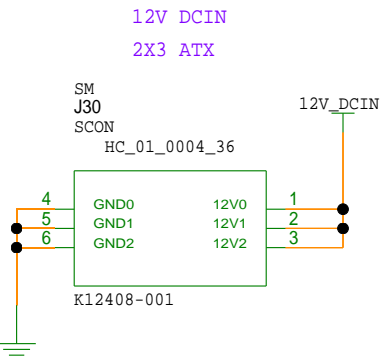
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POWER INPUT



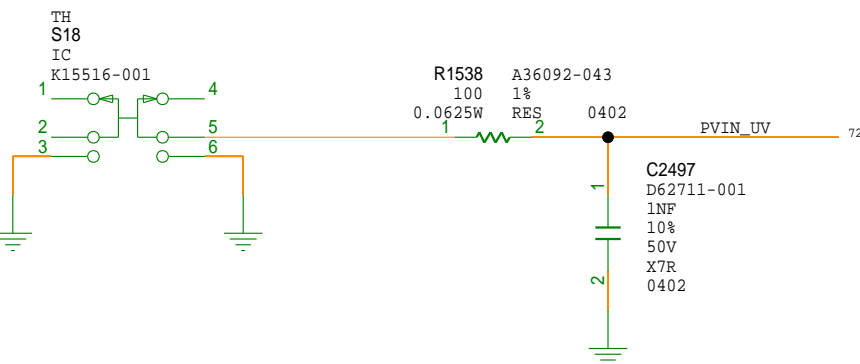
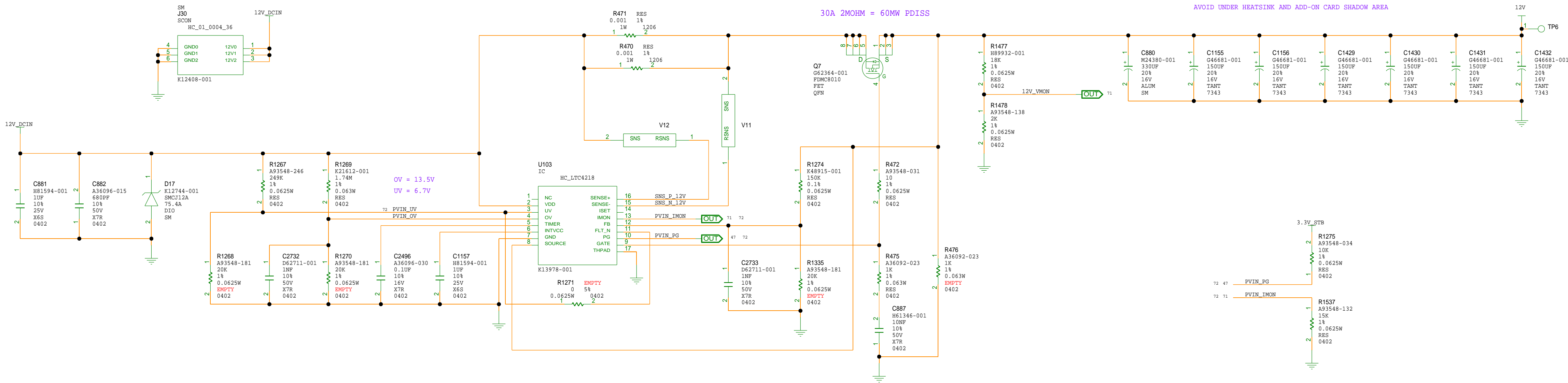
OVERLAP 2X3 CONNECTOR
WITH 2X4 CONNECTOR
FOR FUTURE USE IF ANY



30A CURRENT LIMIT
INRUSH: ~5A/5MS

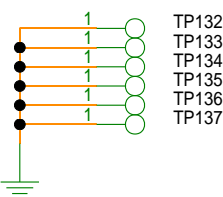
30A 2MOHM = 60MW PDISS

CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA



REVIEW NOTES:
1. ADDED 2X4 ATX CONNECTOR OPTION FOR FUTURE USE. (FP OVERLAP)

CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA
SPREAD THE GND TEST POINTS ACROSS THE PCB AREA. PROVIDE GND SYMBOL SILK



VCC_12V	STATUS	OUTA	OUTB
10.46-13.77V 1	NORMAL	1	1
<10.46V	UV	0	1
>13.77V	OV	1	0

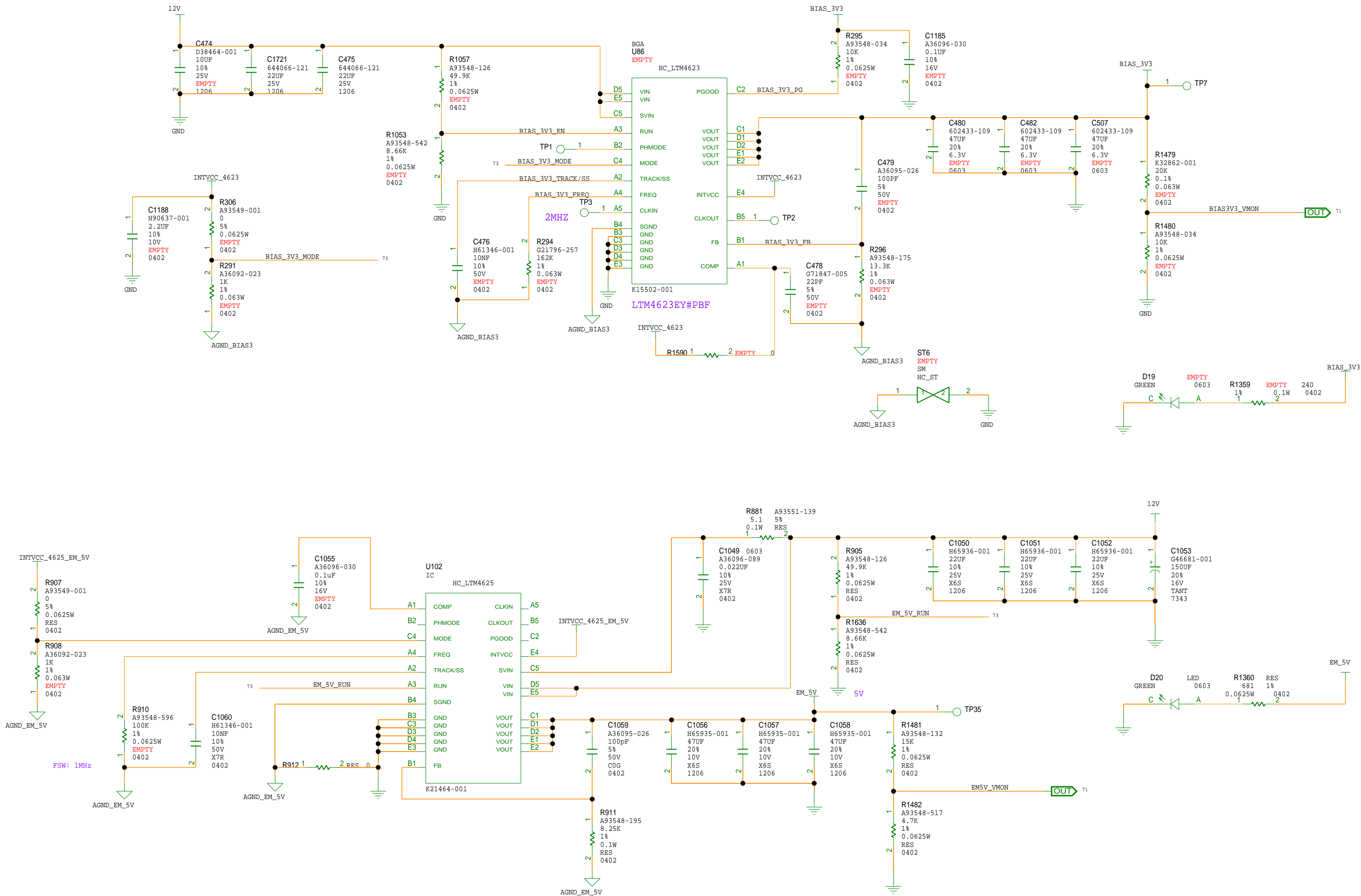
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POWER BIAS

CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

MAX CURRENT = 3A
LOAD CURRENT = 0.5A
VO = 3.3V
SWITCHING FREQ= 2 MHZ
RIPPLE = 5mV
TSS = 3MSEC



CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

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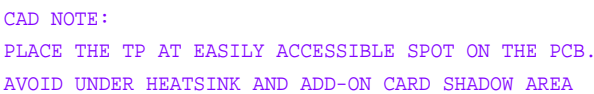
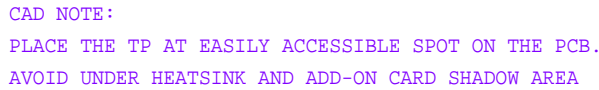
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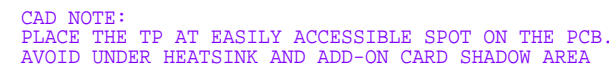
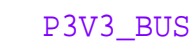
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3.3V_STB & 1.8V_STB



P3V3_BUS



NEED CONFIC
Rht0 20k
gm0: 3.69m

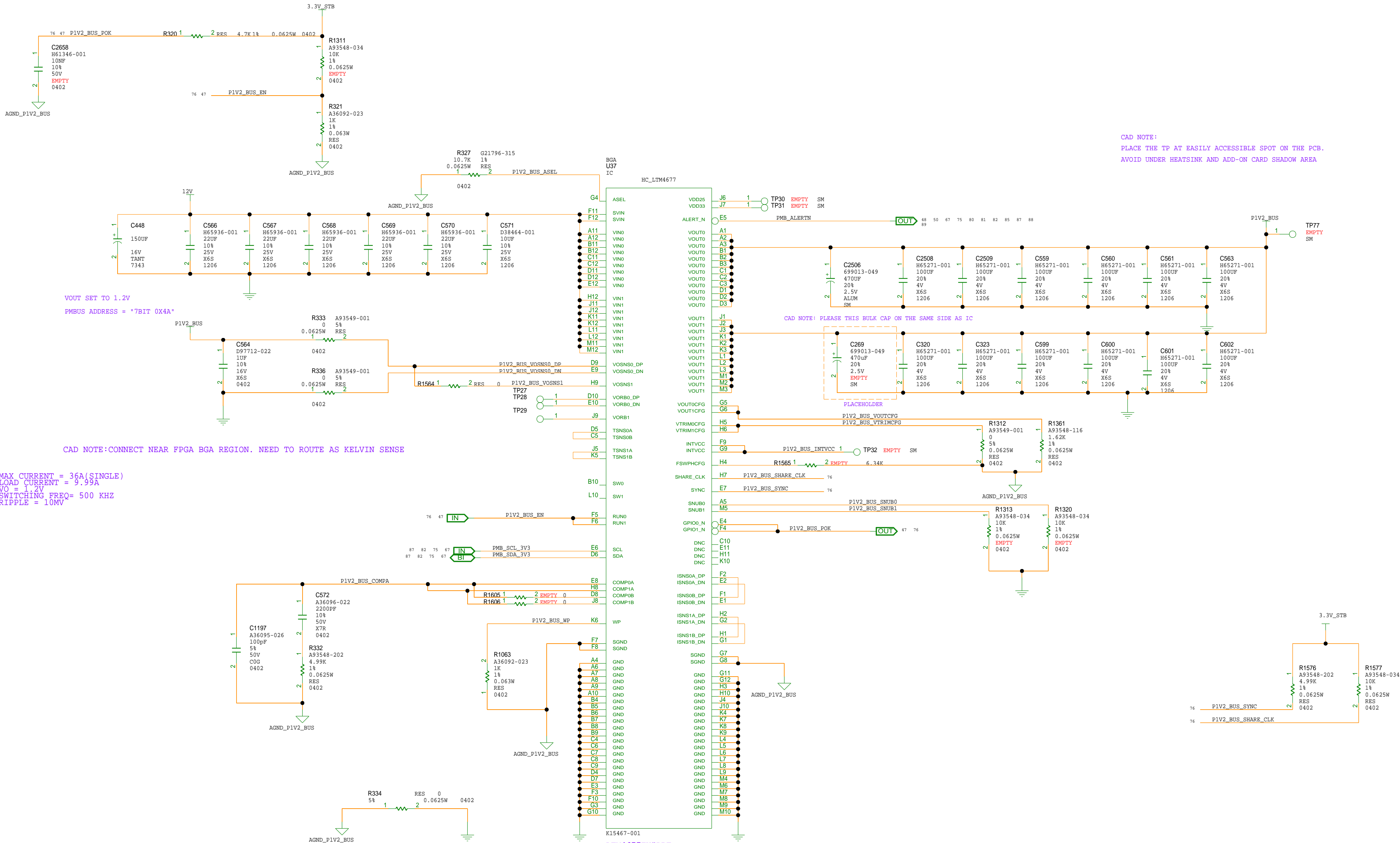


LTM4678EY#PBF

Wed Feb 28 11:38:11 2024

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PIV2_BUS



Wed Feb 28 11:38:12 2024

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CODE

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DOCUMENT NUMBER

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REV

3P0

SCALE:

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SHEET

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VCCL CONTROLLER

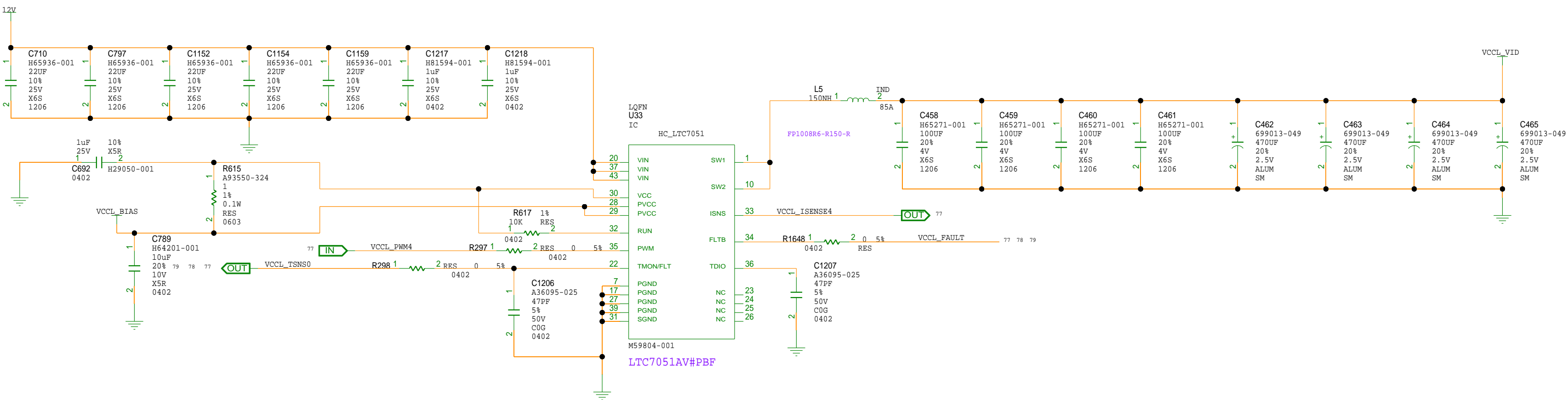
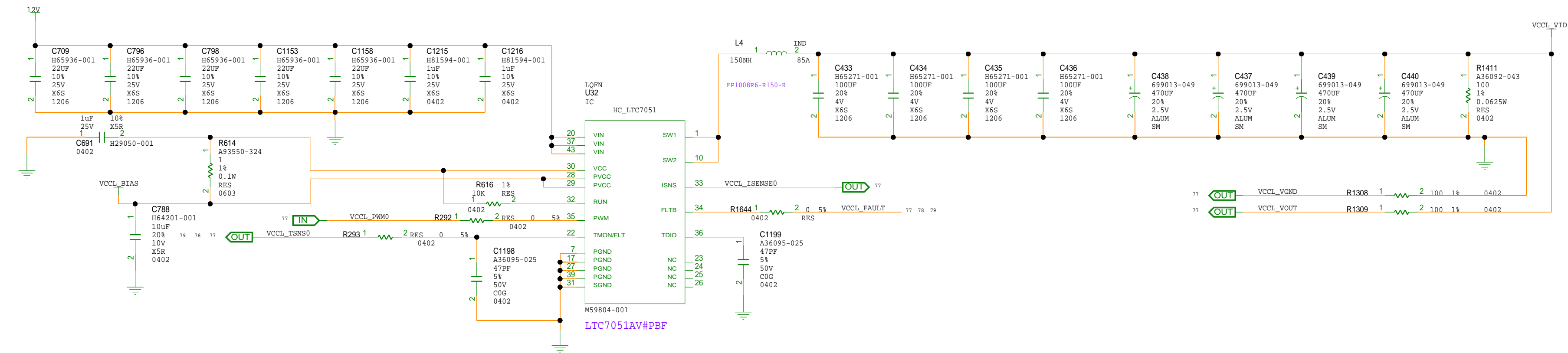


-MODIFIED FOR 5V

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CORE FETS



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DOCUMENT NUMBER

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REV

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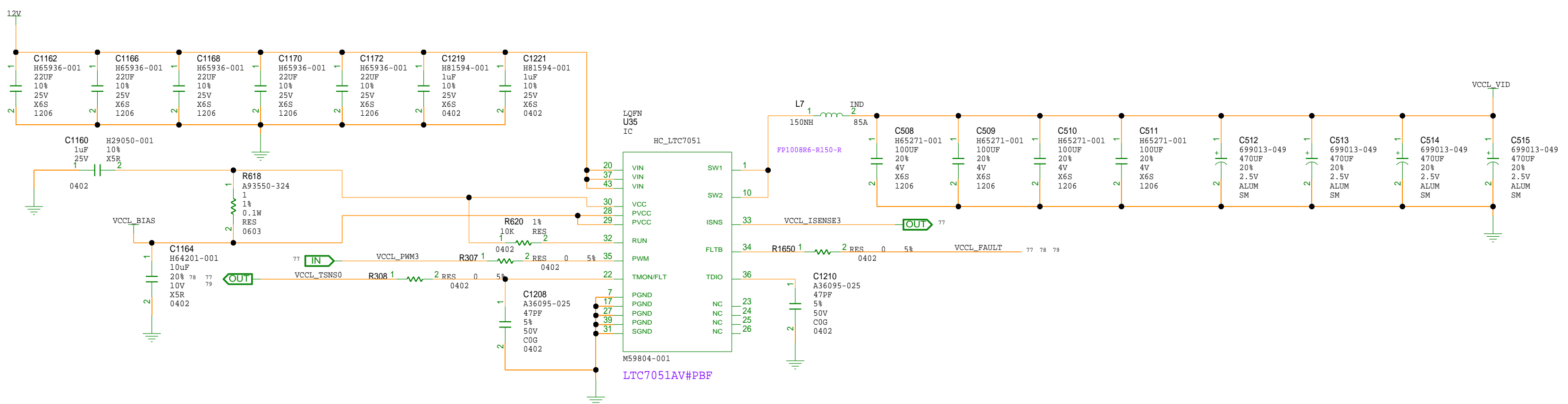
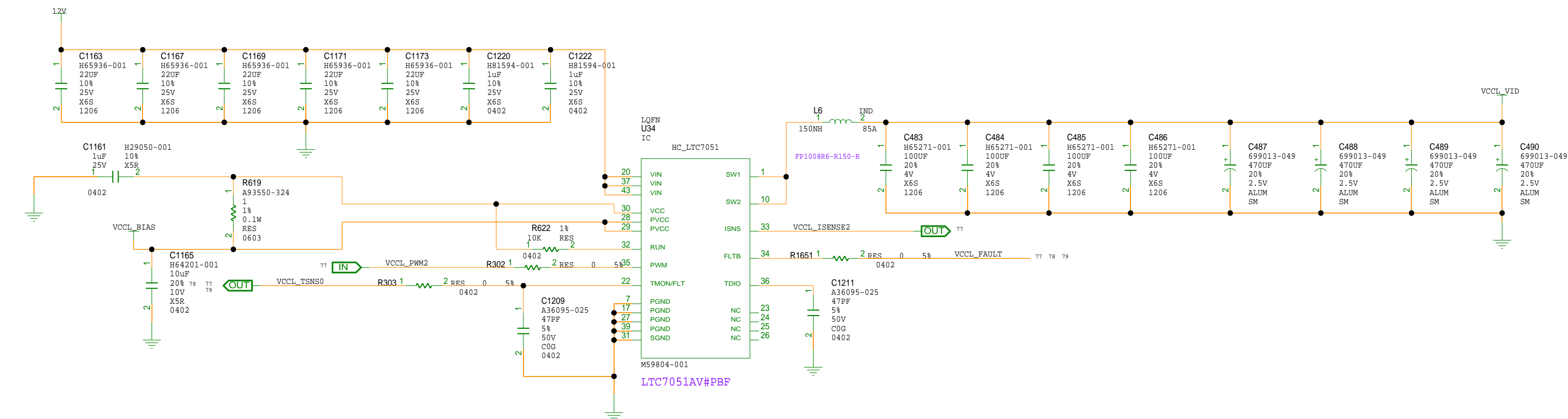
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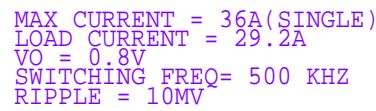
CORE FETS



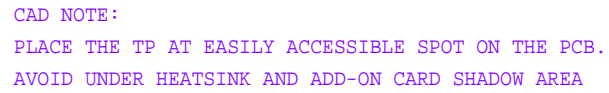
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		SCALE:		DO NOT SCALE DRAWING	SHEET 79 OF 95

P0V8_VCC_HSSI_1



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CAD NOTE: PLEASE THIS BULK CAP ON THE SAME SIDE AS IC

PLACEHOLDER

PLACED UNDER FPGA

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PWR_VCCERT1_13A/13C

VCCERT1_BRK_GDR_U20
VCCERT1_BRK_GDR_U22

CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

CAD NOTE: ROUTE AS DIFFERENTIAL SENSE.

CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

CAD NOTE: ROUTE AS DIFFERENTIAL SENSE.

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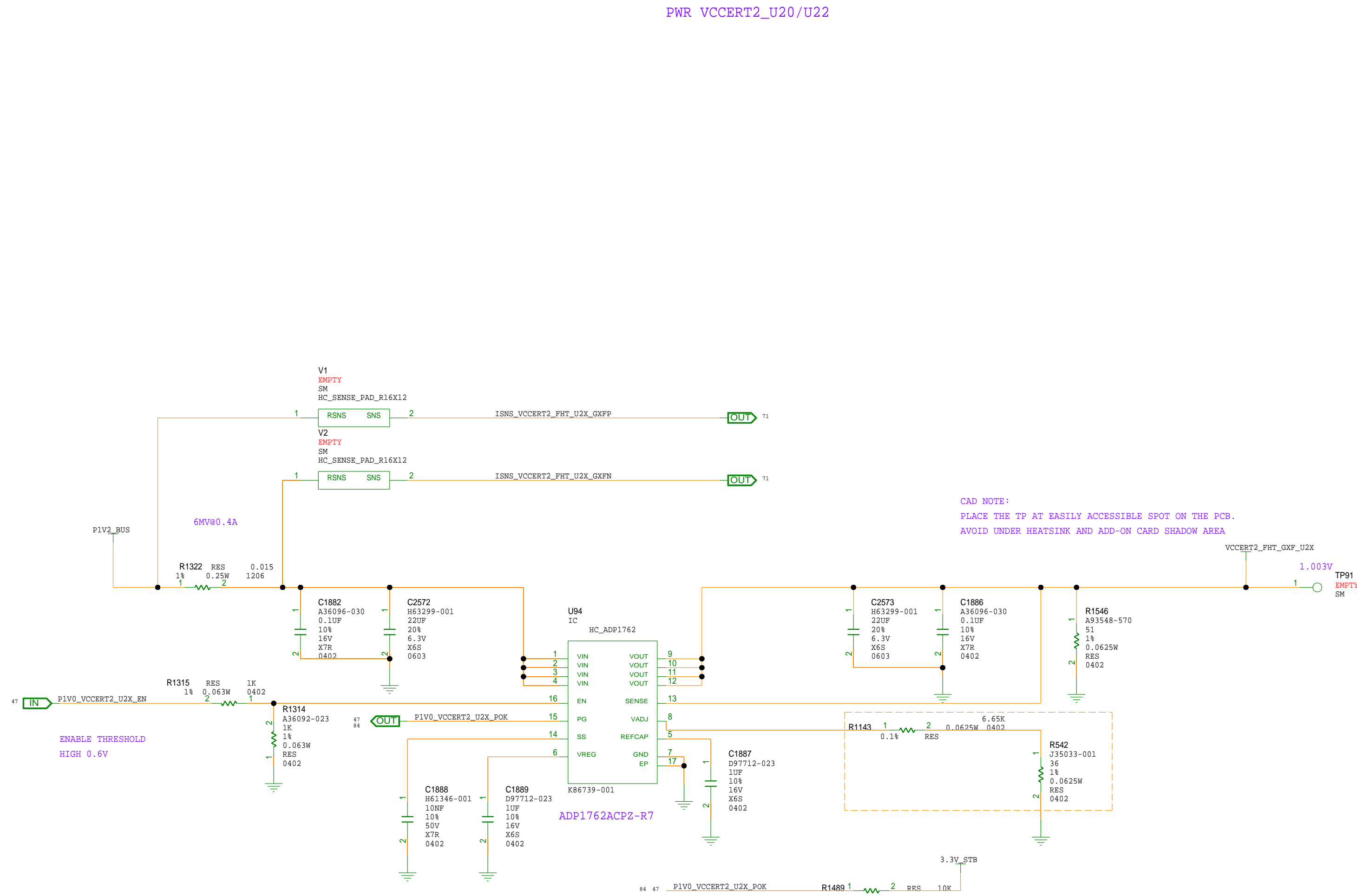
SCALE:

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		SCALE:	DO NOT SCALE DRAWING		SHEET 84 OF 95

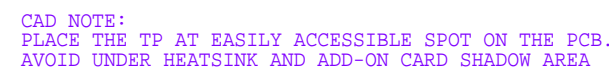
B



P1V5_G2



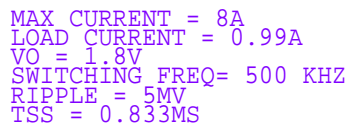
P1V8_G2



```
NEED CONFIG
Rht0 20k
gm0: 3.69m
```


LTM4677EY#PBF

P1V8_G3



CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA.

S->8.33MS

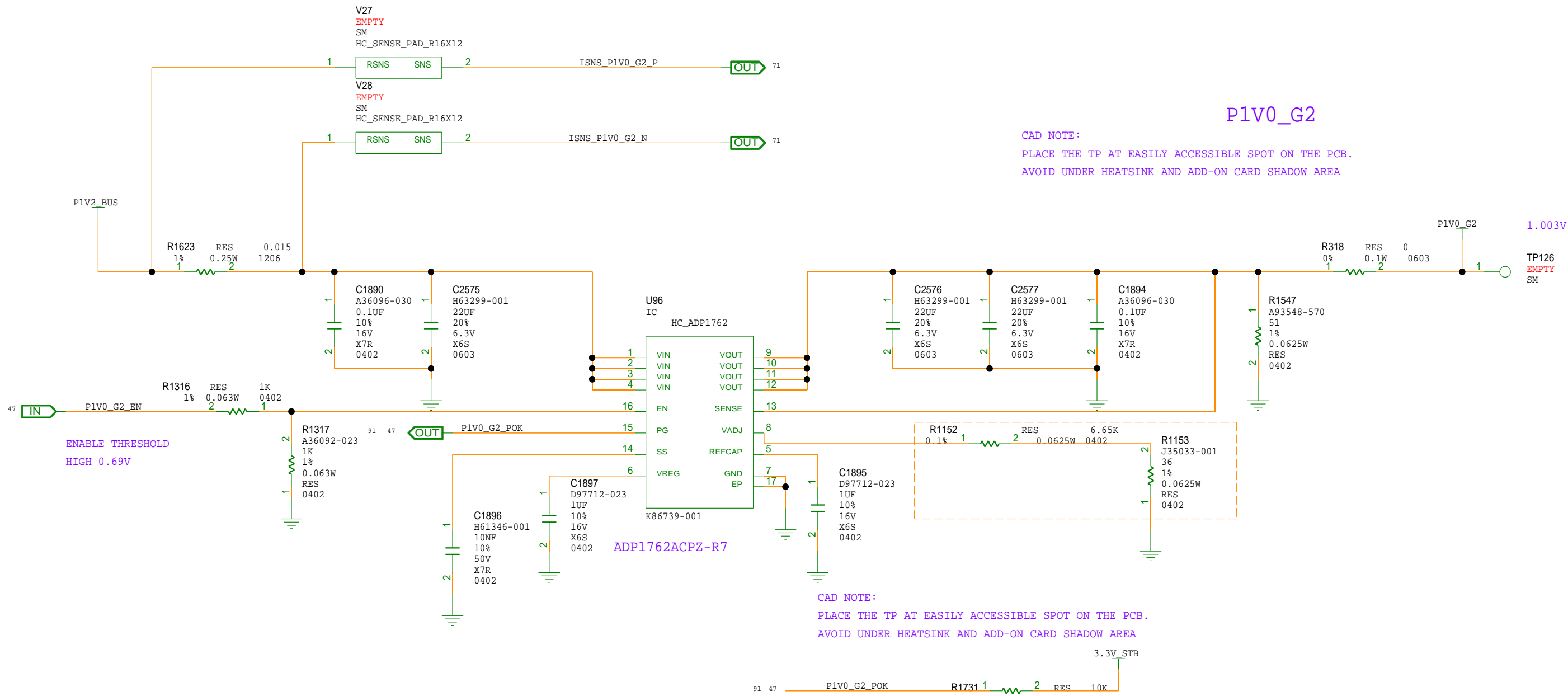
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VCCFUSEWR_SDM

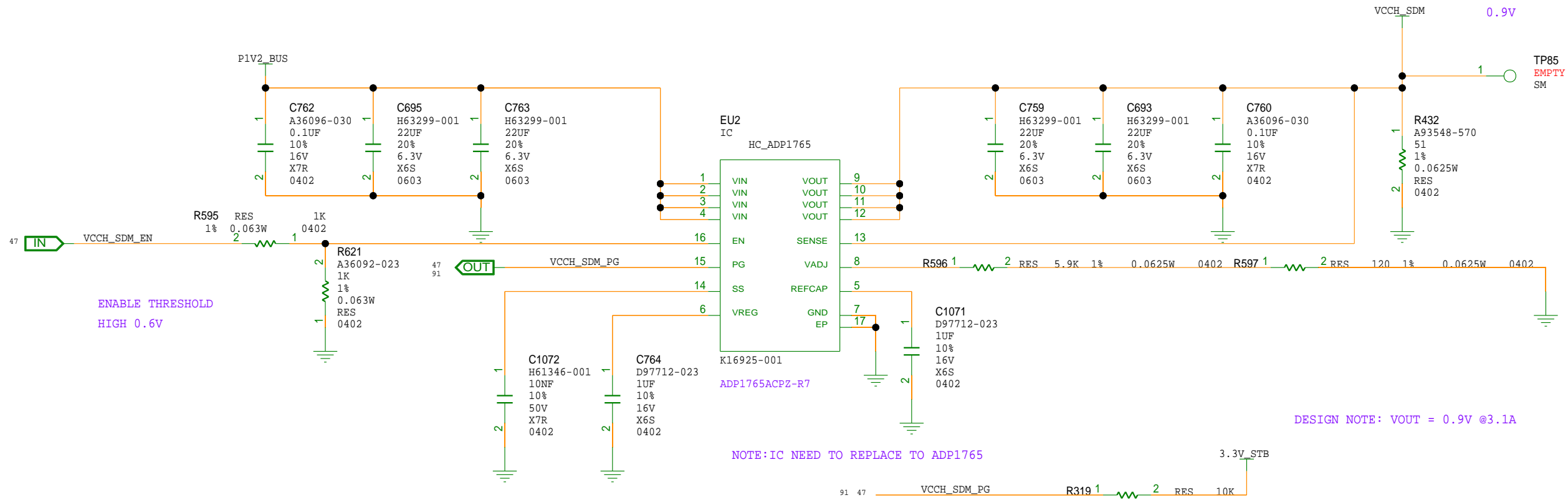
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PWR_VCCH_SDM/P1V0_G2



VCCH_SDM



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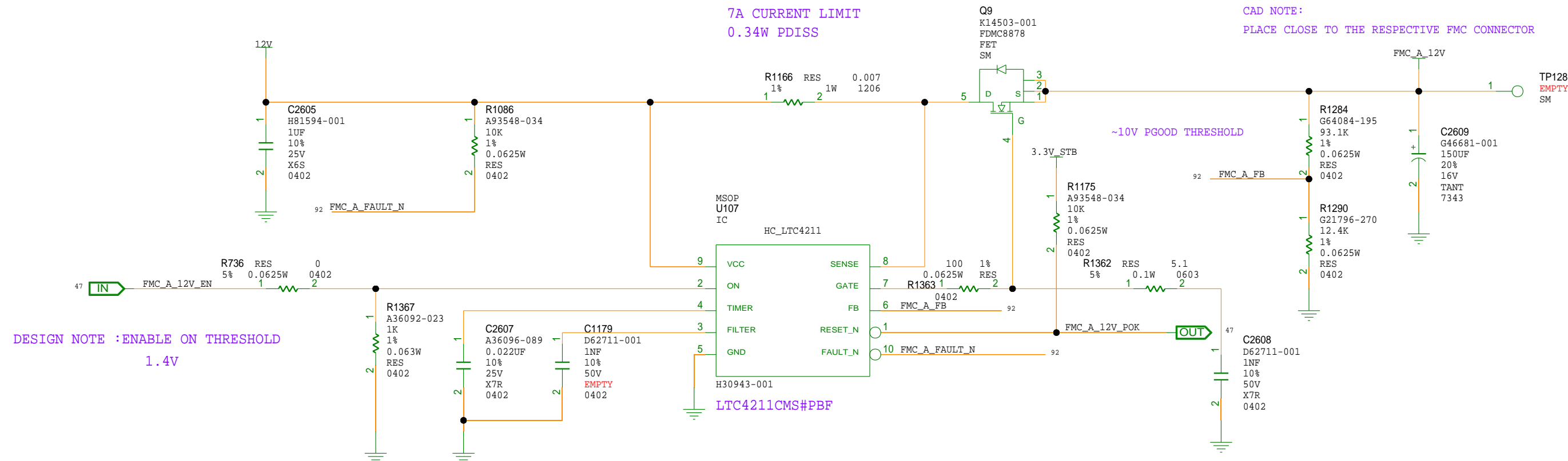
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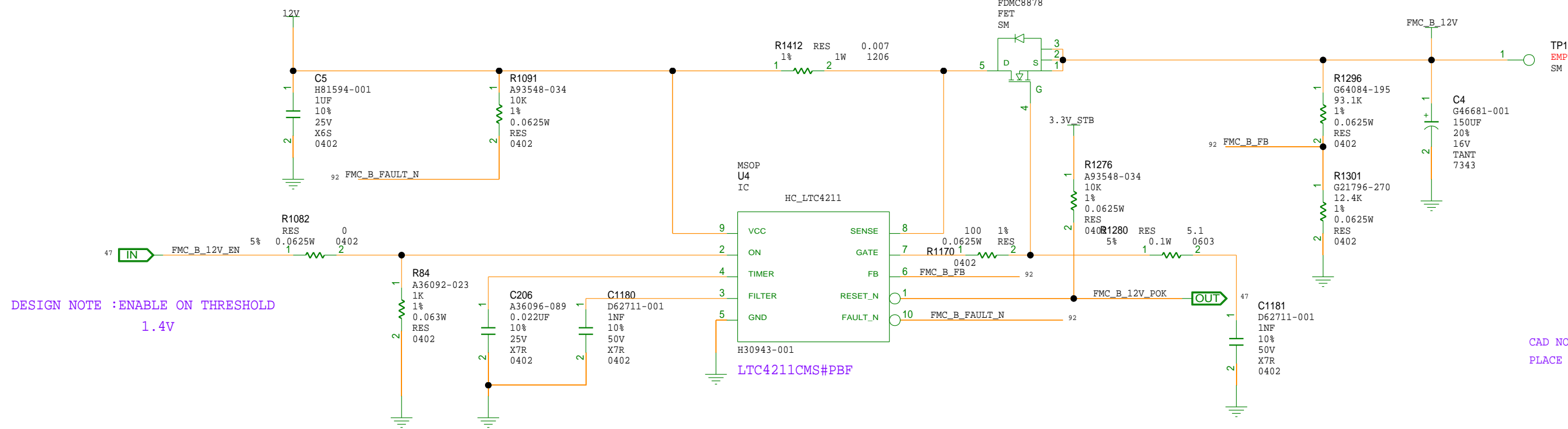
SHEET

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PWR LOAD SWITCHES

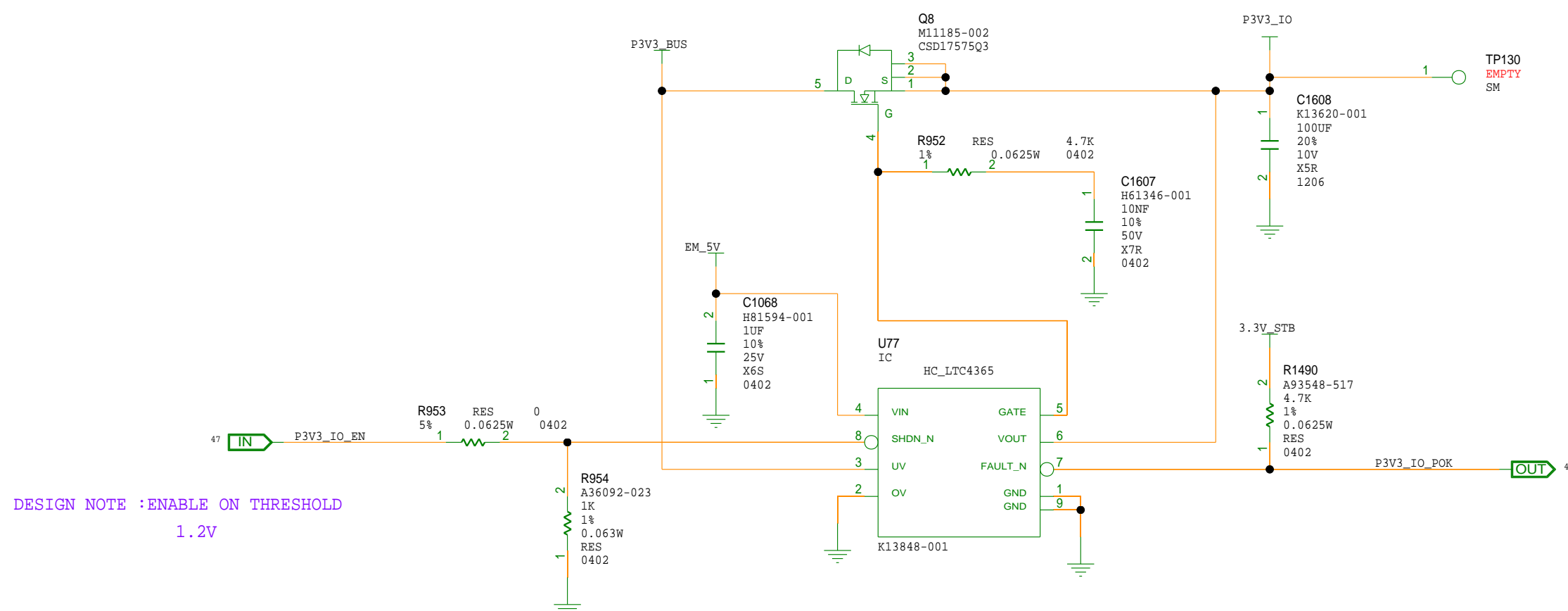


CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA



CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

CAD NOTE:
PLACE CLOSE TO THE RESPECTIVE FMC CONNECTOR



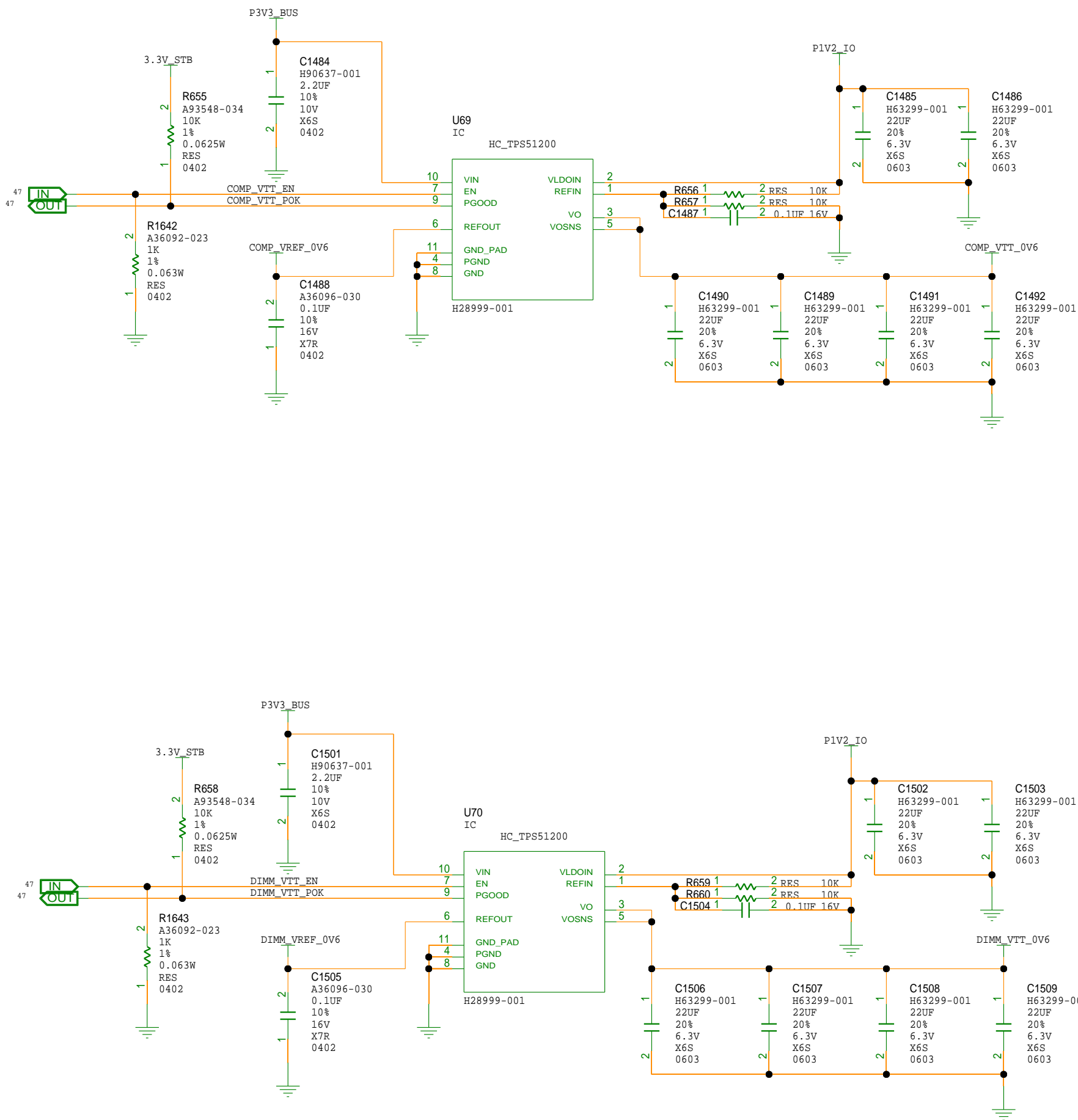
CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

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VTT REGULATORS



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USB PD CONTROLLER

CAD NOTE:

NO STUB ON USB_DP/DM CONNECTING TO THE ZERO OHM

DESIGN NOTE:

I2C2 ACTS AS A SLAVE. MAX-10 COMMUNICATES WITH PD CONTROLLER AS A MASTER
I2C ADDRESS: 0X18

DESIGN NOTE:
I2C1 ACTS AS A MASTER AND COMMUNICATES WITH THE TUSB1146 SS MUX CONTROLLER

VALUE TO BE CHECKED.

PROGRAMMING OF THE FLASH NEED TO BE CLARIFIED WITH FW TEAM

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B												B							
A												A							