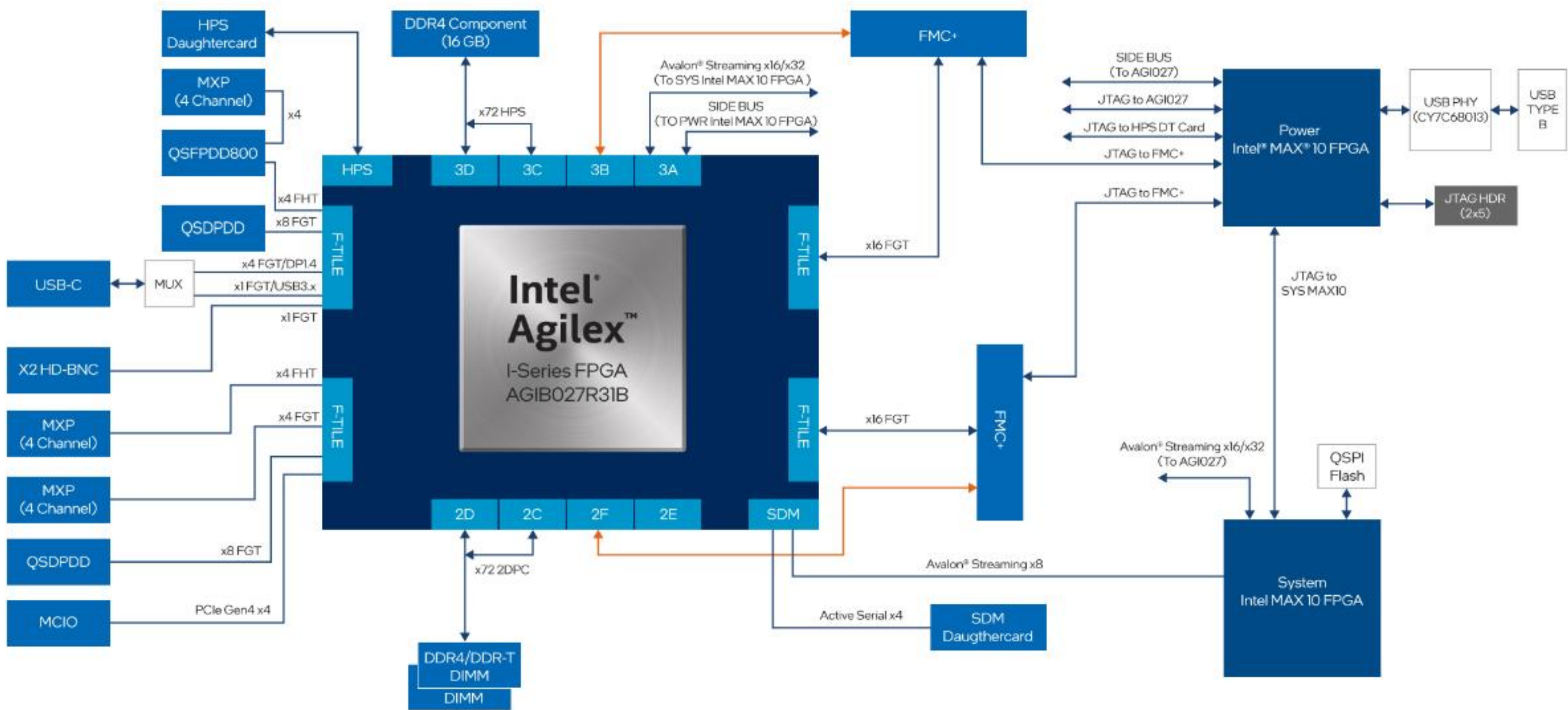
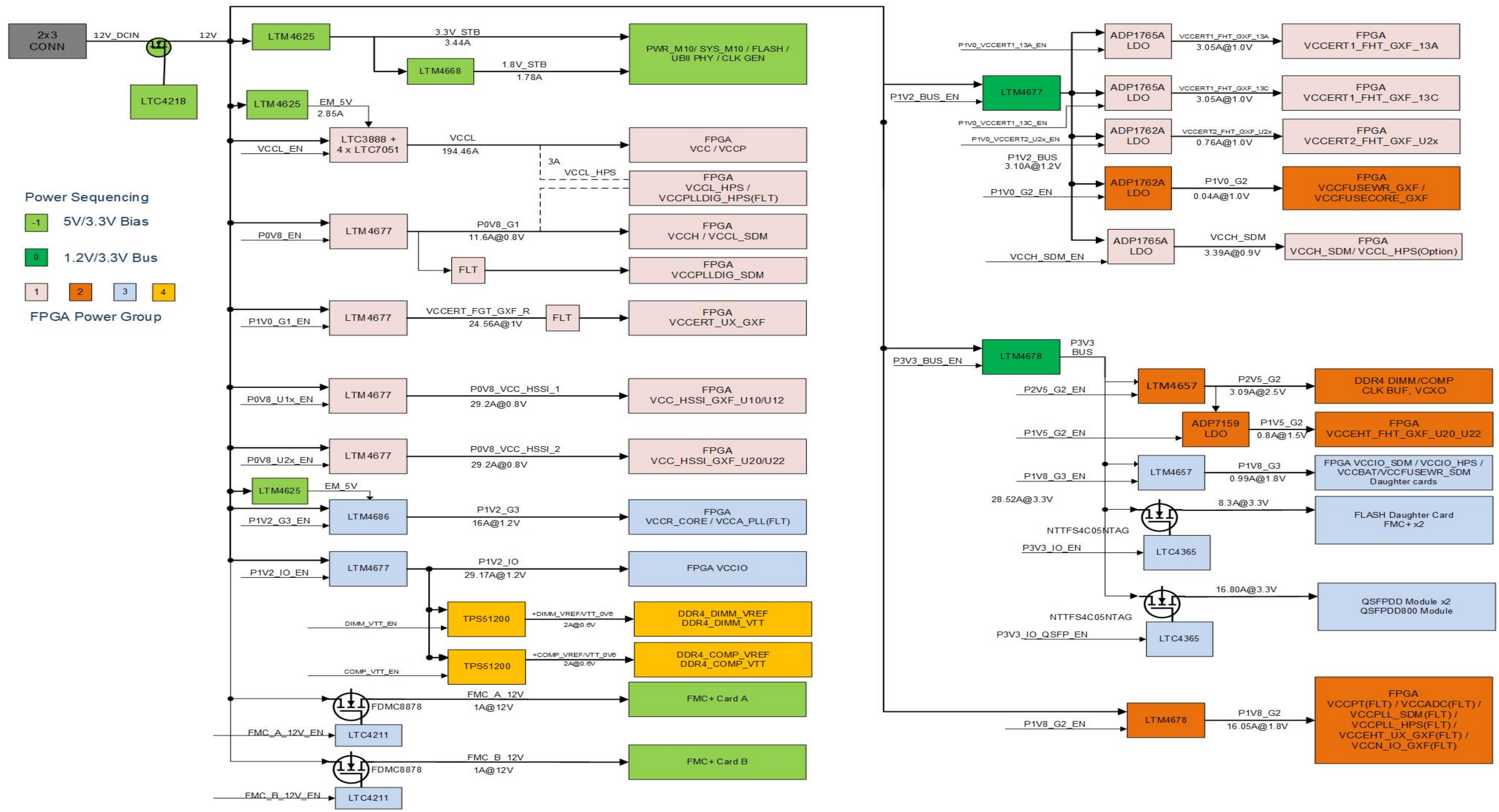


BLOCK DIAGRAM



Thu Feb 27 11:00:51 2025

POWER TREE



Thu Feb 27 11:00:52 2025

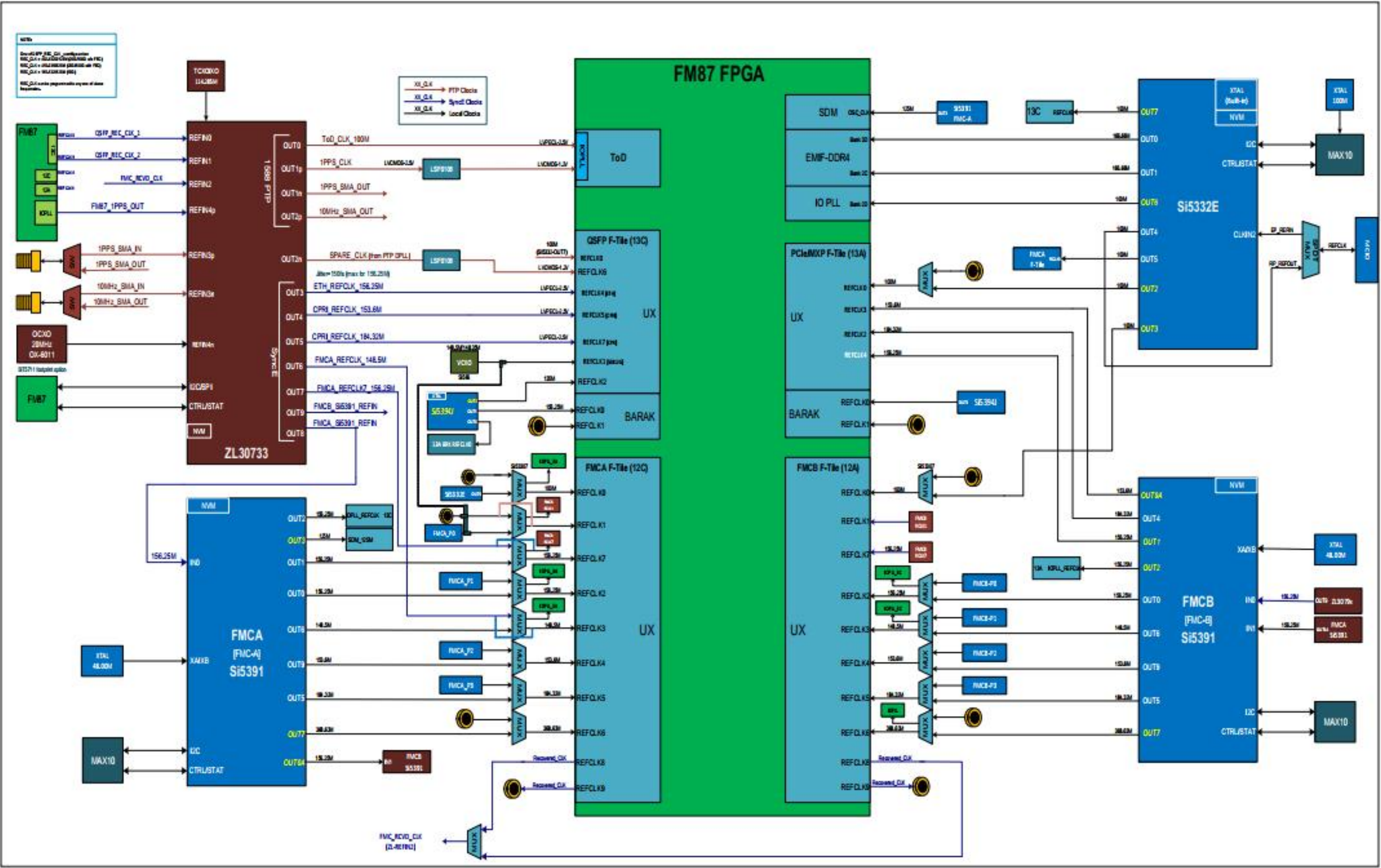
B

A


B

A

CLOCK TREE



Thu Feb 27 11:00:53 2025

DEPARTMENT	 An Intel Company	SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330690-C1	REV 3P0
SCALE:		DO NOT SCALE DRAWING		SHEET 4 OF 95	

4	3	2	1
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A

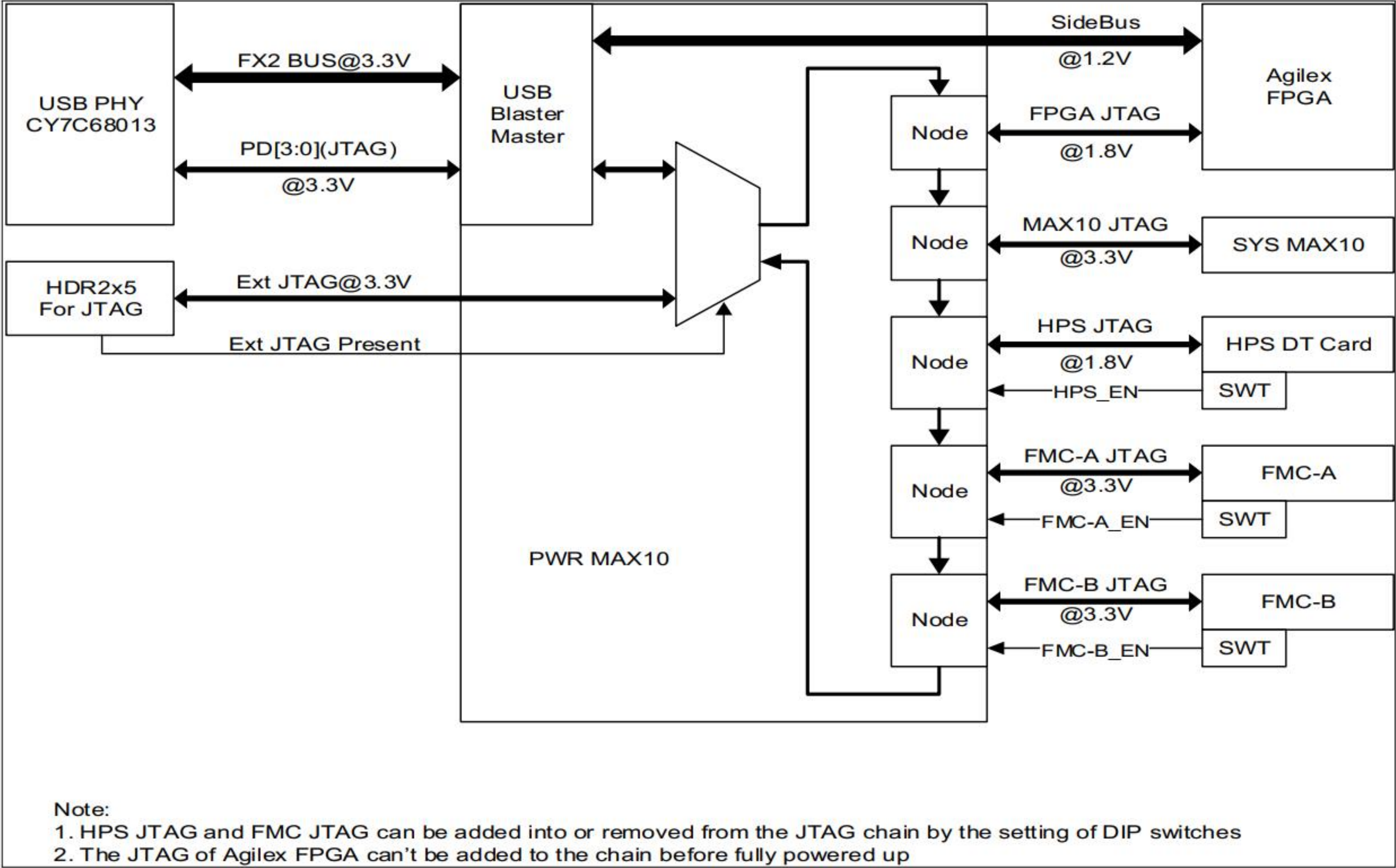
JTAG TOPOLOGY

B

A

B

A



Thu Feb 27 11:00:54 2025

SDM IO MAPPING

CONFIGURATION MODE		MSEL[2:0]
PASSIVE	AVSTX32	000
	AVSTX16	101
	AVSTX8	110
	JTAG	111
	CVP	001
ACTIVE	AS - FAST	001
	AS - NORMAL	011

SDM PINS	MSEL FUNCTIONS	CONFIGURATION SOURCE FUNCTION			
		AVSTX8	AS	AVSTX16	AVSTX32
SDM_IO0		PWR_SCL	PWR_SCL	PWR_SCL	PWR_SCL
SDM_IO1		DATA2	DATA1		
SDM_IO2		DATA0	CLK		
SDM_IO3		DATA3	DATA2		
SDM_IO4		DATA1	DATA0		
SDM_IO5	MSEL0	HPS_CRSTN	NCS00		
SDM_IO6		DATA4	DATA3		
SDM_IO7	MSEL1		NCS02		
SDM_IO8		READY	NCS03		
SDM_IO9	MSEL2		NCS01		
SDM_IO10		DATA7			
SDM_IO11		VALID	HPS_CRSTN	HPS_CRSTN	HPS_CRSTN
SDM_IO12		PWR_SDA		PWR_SDA	PWR_SDA
SDM_IO13		DATA5			
SDM_IO14		CLK			
SDM_IO15		DATA6	RESETN		
SDM_IO16		CFG_DONE	CFG_DONE	CFG_DONE	CFG_DONE

SYSTEM MAX IS THE SOURCE OF HPS_CRSTN FUNCTION

Thu Feb 27 11:00:55 2025

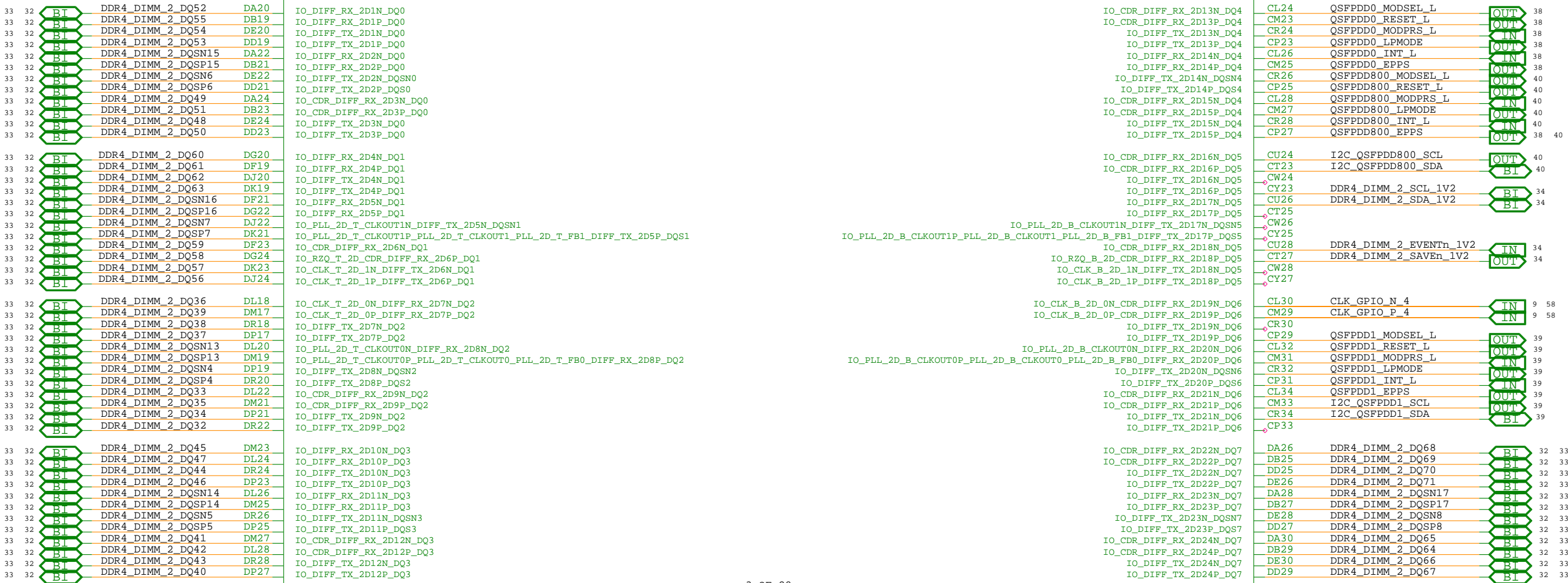
CAD NOTE:
BIT-SWAPPINGS ALLOWED WITHIN A BYTE.
BYTE-SWAPPING IS ALLOWED WITH PRIOR APPROVAL
FROM DESIGN ENGINEER

FPGA BANK 2D

U1

EMPTY

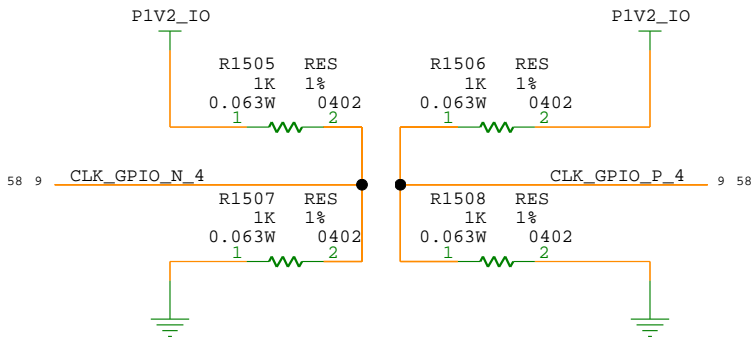
HC_FM87_3184B_PHB8



3 OF 28

IO BANK 2D

99C77A



CAD NOTE:
PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA

Thu Apr 10 09:49:10 2025

DEPARTMENT



SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-C1

REV

3P0

SCALE:

DO NOT SCALE DRAWING

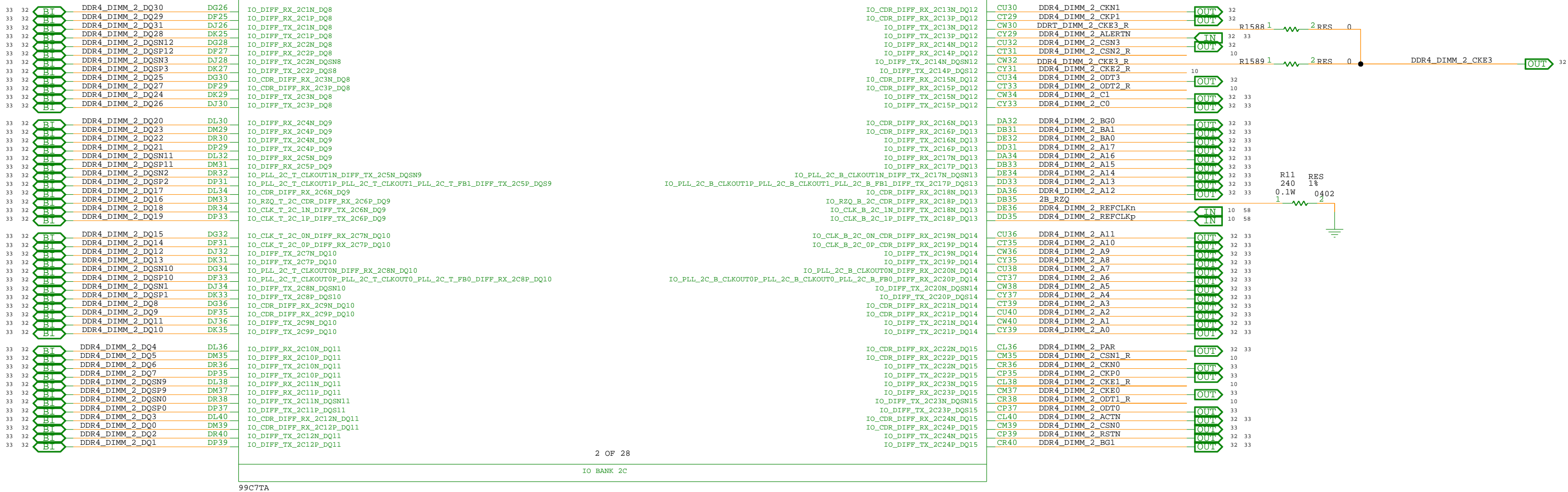
SHEET

9 OF 95

FPGA BANK 2C

U1
EMPTY

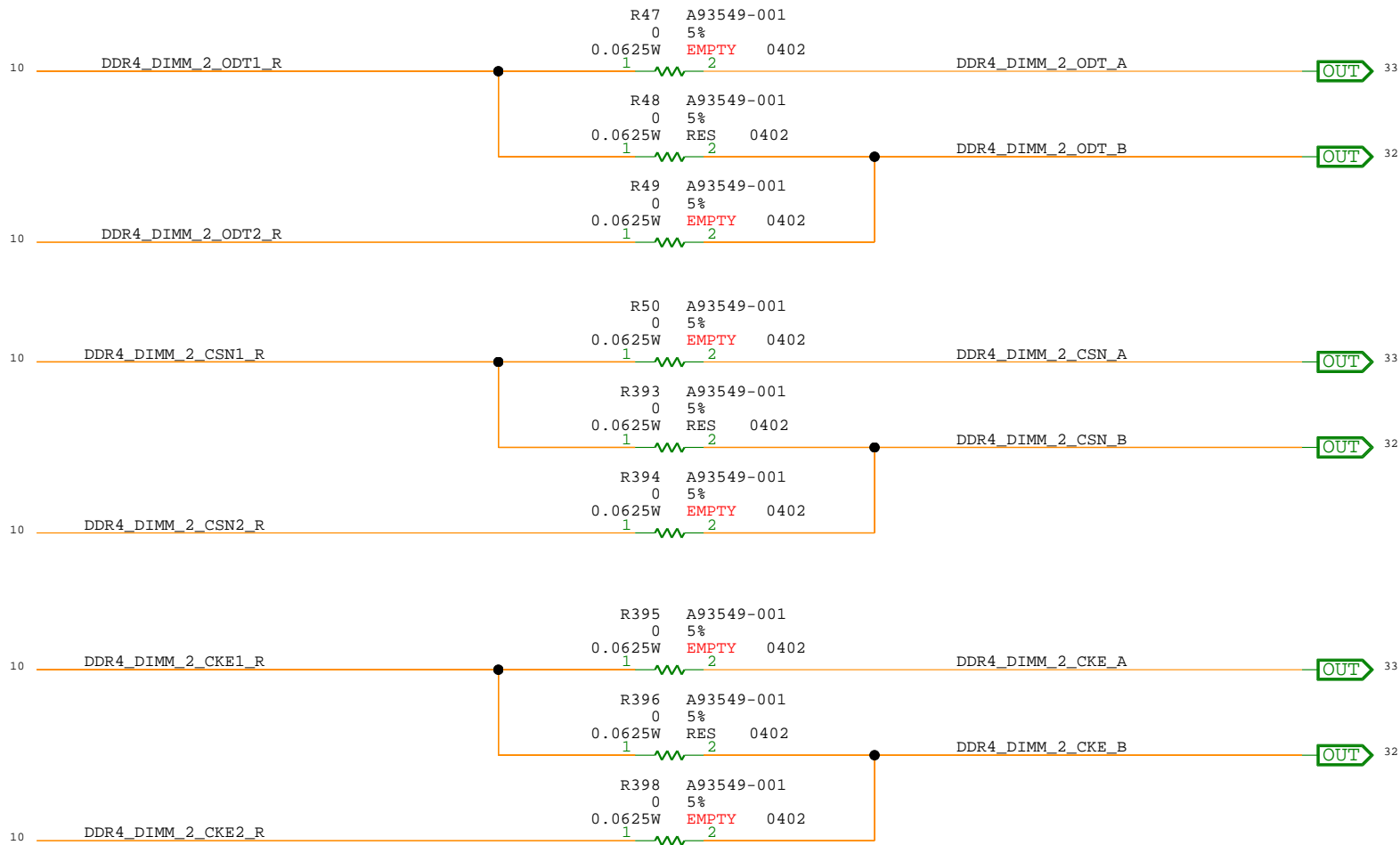
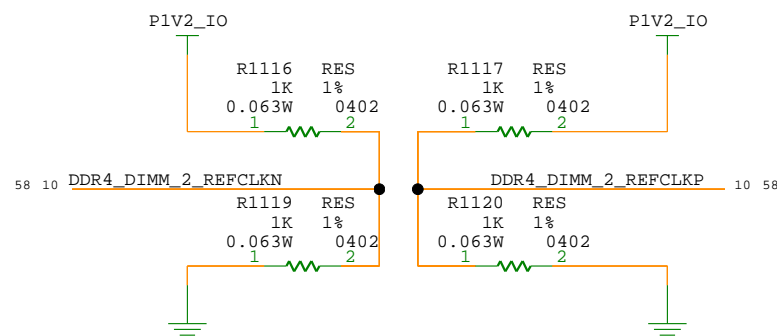
HC_FW87_3184B_PHBE



2 OF 28

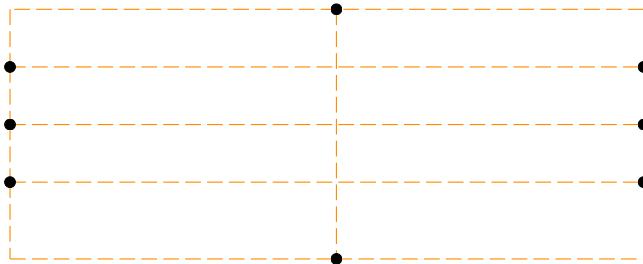
IO BANK 2C

99C7TA



MTA18ASF2G72PZ-3G2E2 16GB SRX4 DDR4-3200

DIMM-B : J36 (NEAR)



Thu Apr 10 09:49:12 2025

DEPARTMENT



SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-C1

REV

3P0

SCALE:

DO NOT SCALE DRAWING

SHEET

10 OF 95

B

B

A

A

FPGA BANK 2F

U1
EMPTY

HC_FM87_3184B_PHBE

43	B1	FMC_B_LA_N12	DG38
43	B1	FMC_B_LA_P12	DF37
43	B1	FMC_B_LA_N7	DJ38
43	B1	FMC_B_LA_P7	DK37
43	B1	FMC_B_LA_N11	DQ40
43	B1	FMC_B_LA_P11	DF39
43	B1	FMC_B_LA_N8	DJ40
43	B1	FMC_B_LA_P8	DK39
43	B1	FMC_B_LA_N5	DQ42
43	B1	FMC_B_LA_P5	DF41
43	B1	FMC_B_LA_N22	DJ42
43	B1	FMC_B_LA_P22	DK41
43	B1	FMC_B_LA_N23	DL42
43	B1	FMC_B_LA_P23	DM41
43	B1	FMC_B_LA_N13	DR42
43	B1	FMC_B_LA_P13	DP41
43	B1	FMC_B_LA_N10	DL44
43	B1	FMC_B_LA_P10	DM43
43	B1	FMC_B_LA_N9	DR44
43	B1	FMC_B_LA_P9	DP43
43	B1	FMC_B_LA_N14	DL46
43	B1	FMC_B_LA_P14	DM45
43	B1	FMC_B_CLK2_M2C_N	DR46
43	B1	FMC_B_CLK2_M2C_P	DE45
43	1N	FMC_B_CLK0_M2C_N	DG44
43	1N	FMC_B_CLK0_M2C_P	DF43
43	1N	FMC_B_SYNC_M2C_N	DK43
43	1N	FMC_B_SYNC_M2C_P	DJ44
43	0400	FMC_B_REFCLK_C2M_N	DG46
43	0400	FMC_B_REFCLK_C2M_P	DF45
43	0400	FMC_B_SYNC_C2M_N	DJ46
43	0400	FMC_B_SYNC_C2M_P	DK45
43	0400	FMC_B_LA_N25	DG48
43	B1	FMC_B_LA_P25	DF47
			DJ48
			DK47
			DL48
			DM47
			DR48
			DP47
			DL50
			DM49
			DR50
			DP49
			DL52
			DM51
			DR52
			DP51

IO_DIFF_RX_2F1N_DQ16	
IO_DIFF_RX_2F1P_DQ16	
IO_DIFF_TX_2F1N_DQ16	
IO_DIFF_TX_2F1P_DQ16	
IO_DIFF_RX_2F2N_DQ16	
IO_DIFF_TX_2F2N_DQ16	
IO_CDR_DIFF_RX_2F3N_DQ16	
IO_CDR_DIFF_RX_2F3P_DQ16	
IO_DIFF_TX_2F3N_DQ16	
IO_DIFF_TX_2F3P_DQ16	
IO_DIFF_RX_2F4N_DQ17	
IO_DIFF_RX_2F4P_DQ17	
IO_DIFF_TX_2F4N_DQ17	
IO_DIFF_TX_2F4P_DQ17	
IO_DIFF_RX_2F5N_DQ17	
IO_DIFF_RX_2F5P_DQ17	
IO_PLD_2F_T_CLKOUT1N_DIFF_TX_2F5N_DQSN17	
IO_PLD_2F_T_CLKOUT1P_PLD_2F_T_CLKOUT1_PLD_2F_T_FB1_DIFF_TX_2F5P_DQSN17	
IO_CDR_DIFF_RX_2F6N_DQ17	
IO_RZQ_B_2F_CDR_DIFF_RX_2F6P_DQ17	
IO_CLK_T_2F_1N_DIFF_TX_2F6N_DQ17	
IO_CLK_T_2F_1P_DIFF_TX_2F6P_DQ17	
IO_CLK_T_2F_0N_DIFF_RX_2F7N_DQ18	
IO_CLK_T_2F_0P_DIFF_RX_2F7P_DQ18	
IO_DIFF_TX_2F7N_DQ18	
IO_DIFF_TX_2F7P_DQ18	
IO_PLD_2F_T_CLKOUT0N_DIFF_RX_2F8N_DQ18	
IO_PLD_2F_T_CLKOUT0P_PLD_2F_T_CLKOUT0_PLD_2F_T_FB0_DIFF_RX_2F8P_DQ18	
IO_DIFF_TX_2F8N_DQSN18	
IO_DIFF_TX_2F8P_DQSN18	
IO_CDR_DIFF_RX_2F9N_DQ18	
IO_CDR_DIFF_RX_2F9P_DQ18	
IO_DIFF_TX_2F9N_DQ18	
IO_DIFF_TX_2F9P_DQ18	
IO_DIFF_RX_2F10N_DQ19	
IO_DIFF_RX_2F10P_DQ19	
IO_DIFF_TX_2F10N_DQ19	
IO_DIFF_TX_2F10P_DQ19	
IO_DIFF_RX_2F11N_DQ19	
IO_DIFF_RX_2F11P_DQ19	
IO_DIFF_TX_2F11N_DQSN19	
IO_DIFF_TX_2F11P_DQSN19	
IO_CDR_DIFF_RX_2F12N_DQ19	
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IO_DIFF_TX_2F12N_DQ19	
IO_DIFF_TX_2F12P_DQ19	

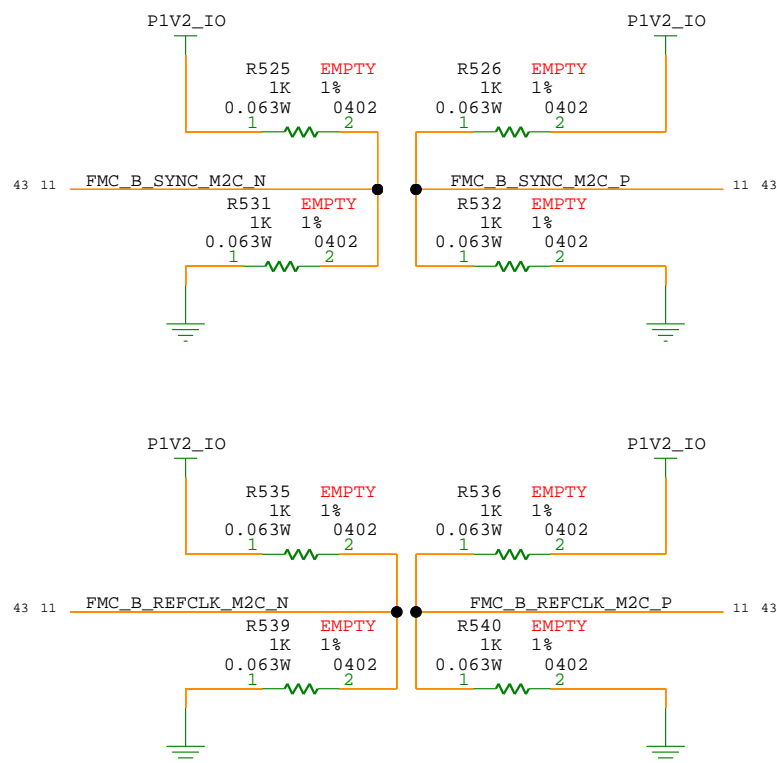
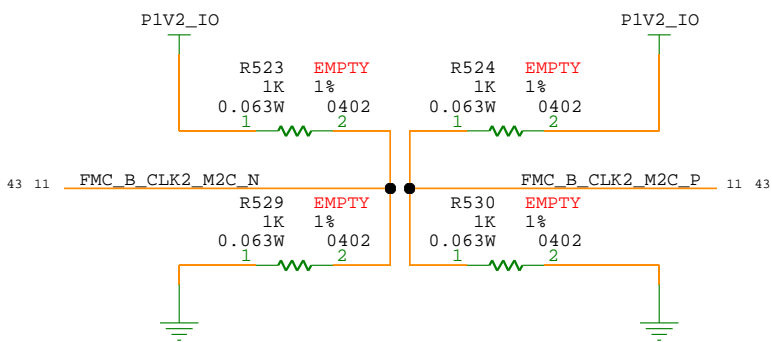
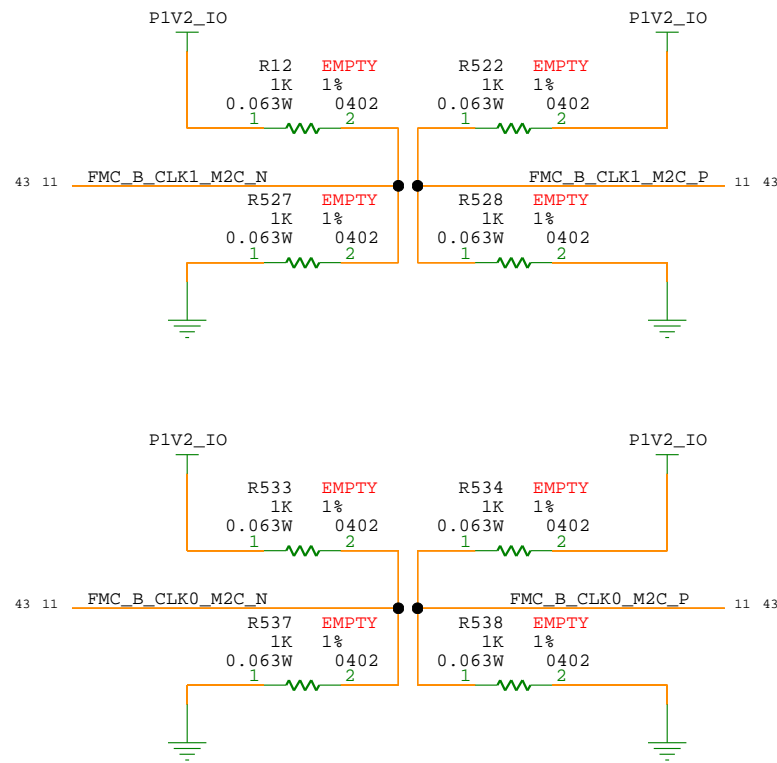
5 OF 28

IO BANK 2F

99C7TA

IO_CDR_DIFF_RX_2F13N_DQ20	
IO_CDR_DIFF_RX_2F13P_DQ20	
IO_DIFF_TX_2F13N_DQ20	
IO_DIFF_TX_2F13P_DQ20	
IO_DIFF_RX_2F14N_DQ20	
IO_DIFF_RX_2F14P_DQ20	
IO_DIFF_TX_2F14N_DQSN20	
IO_DIFF_TX_2F14P_DQSN20	
IO_CDR_DIFF_RX_2F15N_DQ20	
IO_CDR_DIFF_RX_2F15P_DQ20	
IO_DIFF_TX_2F15N_DQ20	
IO_DIFF_TX_2F15P_DQ20	
IO_CDR_DIFF_RX_2F16N_DQ21	
IO_CDR_DIFF_RX_2F16P_DQ21	
IO_DIFF_TX_2F16N_DQ21	
IO_DIFF_TX_2F16P_DQ21	
IO_DIFF_RX_2F17N_DQ21	
IO_DIFF_RX_2F17P_DQ21	
IO_PLD_2F_B_CLKOUT1N_DIFF_TX_2F17N_DQSN21	
IO_PLD_2F_B_CLKOUT1P_PLD_2F_B_CLKOUT1_PLD_2F_B_FB1_DIFF_TX_2F17P_DQSN21	
IO_CDR_DIFF_RX_2F18N_DQ21	
IO_RZQ_B_2F_CDR_DIFF_RX_2F18P_DQ21	
IO_CLK_B_2F_1N_DIFF_TX_2F18N_DQ21	
IO_CLK_B_2F_1P_DIFF_TX_2F18P_DQ21	
IO_CLK_B_2F_0N_CDR_DIFF_RX_2F19N_DQ22	
IO_CLK_B_2F_0P_CDR_DIFF_RX_2F19P_DQ22	
IO_DIFF_TX_2F19N_DQ22	
IO_DIFF_TX_2F19P_DQ22	
IO_PLD_2F_B_CLKOUT0N_DIFF_RX_2F20N_DQ22	
IO_PLD_2F_B_CLKOUT0P_PLD_2F_B_CLKOUT0_PLD_2F_B_FB0_DIFF_RX_2F20P_DQ22	
IO_DIFF_TX_2F20N_DQSN22	
IO_DIFF_TX_2F20P_DQSN22	
IO_CDR_DIFF_RX_2F21N_DQ22	
IO_CDR_DIFF_RX_2F21P_DQ22	
IO_DIFF_TX_2F21N_DQ22	
IO_DIFF_TX_2F21P_DQ22	
IO_CDR_DIFF_RX_2F22N_DQ23	
IO_CDR_DIFF_RX_2F22P_DQ23	
IO_DIFF_TX_2F22N_DQ23	
IO_DIFF_TX_2F22P_DQ23	
IO_DIFF_RX_2F23N_DQ23	
IO_DIFF_RX_2F23P_DQ23	
IO_DIFF_TX_2F23N_DQSN23	
IO_DIFF_TX_2F23P_DQSN23	
IO_CDR_DIFF_RX_2F24N_DQ23	
IO_CDR_DIFF_RX_2F24P_DQ23	
IO_DIFF_TX_2F24N_DQ23	
IO_DIFF_TX_2F24P_DQ23	

DA38	FMC_B_LA_N6	B1	43
DB37	FMC_B_LA_P6	B1	43
DE38	FMC_B_LA_N2	B1	43
DD37	FMC_B_LA_P2	B1	43
DA40	FMC_B_LA_N15	B1	43
DB39	FMC_B_LA_P15	B1	43
DE40	FMC_B_LA_N4	B1	43
DD39	FMC_B_LA_P4	B1	43
DA42	FMC_B_LA_N20	B1	43
DB41	FMC_B_LA_P20	B1	43
DE42	FMC_B_LA_N21	B1	43
DD41	FMC_B_LA_P21	B1	43
DA44	FMC_B_LA_N32	B1	43
DB43	FMC_B_LA_P32	B1	43
DE44	FMC_B_LA_N26	B1	43
DA43	FMC_B_LA_P26	B1	43
DE46	FMC_B_LA_N24	B1	43
DB45	FMC_B_LA_P24	B1	43
DE46	FMC_B_LA_N0	B1	43
DA45	FMC_B_LA_P0	B1	43
DA48	FMC_B_LA_N3	B1	43
DB47	FMC_B_LA_P3	B1	43
DE48	FMC_B_CLK1_M2C_N	1N	11 43
DD47	FMC_B_CLK1_M2C_P	1N	11 43
CT41	FMC_B_REFCLK_M2C_N	1N	11 43
CU42	FMC_B_REFCLK_M2C_P	1N	11 43
CY41	FMC_B_LA_N33	B1	43
CW42	FMC_B_LA_P33	B1	43
CU44	FMC_B_LA_N19	B1	43
CT43	FMC_B_LA_P19	B1	43
CW44	FMC_B_LA_N28	B1	43
CY43	FMC_B_LA_P28	B1	43
CU46	FMC_B_LA_N1	B1	43
CT45	FMC_B_LA_P1	B1	43
CY45	FMC_B_LA_N29	B1	43
CW46	FMC_B_LA_P29	B1	43
CM41	FMC_B_LA_N18	B1	43
CL42	FMC_B_LA_P18	B1	43
CP42	FMC_B_LA_N17	B1	43
CP41	FMC_B_LA_P17	B1	43
CL44	FMC_B_LA_N16	B1	43
CM43	FMC_B_LA_P16	B1	43
CR44	FMC_B_LA_N27	B1	43
CP43	FMC_B_LA_P27	B1	43
CM45	FMC_B_LA_N30	B1	43
CL46	FMC_B_LA_P30	B1	43
CP45	FMC_B_LA_N31	B1	43
CR46	FMC_B_LA_P31	B1	43



CAD NOTE:
PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA

Thu Apr 10 09:49:14 2025

DEPARTMENT



SIZE
C+

CODE
34649

DOCUMENT NUMBER

150-0330690-C1

REV

3P0

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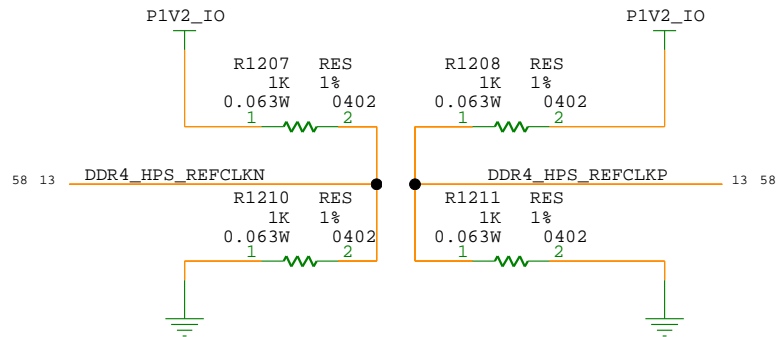
DO NOT SCALE DRAWING

SHEET

11 OF 95

FPGA BANK 3D

CAD NOTE:
BIT-SWAPPINGS ALLOWED WITHIN A BYTE.
BYTE-SWAPPING IS ALLOWED WITH PRIOR APPROVAL
FROM DESIGN ENGINEER (EXCEPT ECC)



CAD NOTE:
PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA
PLACE TE PAD ON THE TRACE

Thu Apr 10 09:49:19 2025

DEPARTMENT



SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-C1

REV

3P0

SCALE:

DO NOT SCALE DRAWING

SHEET

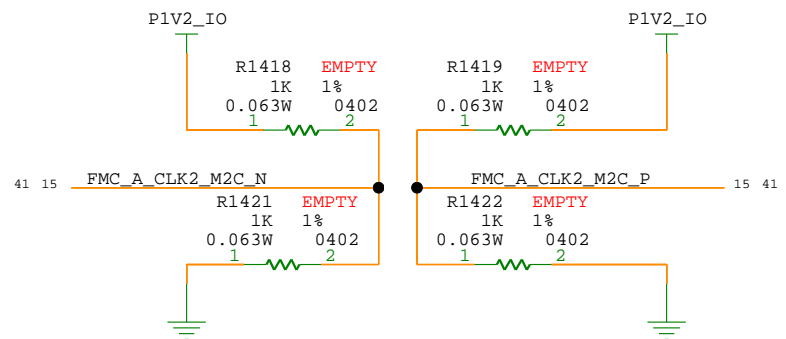
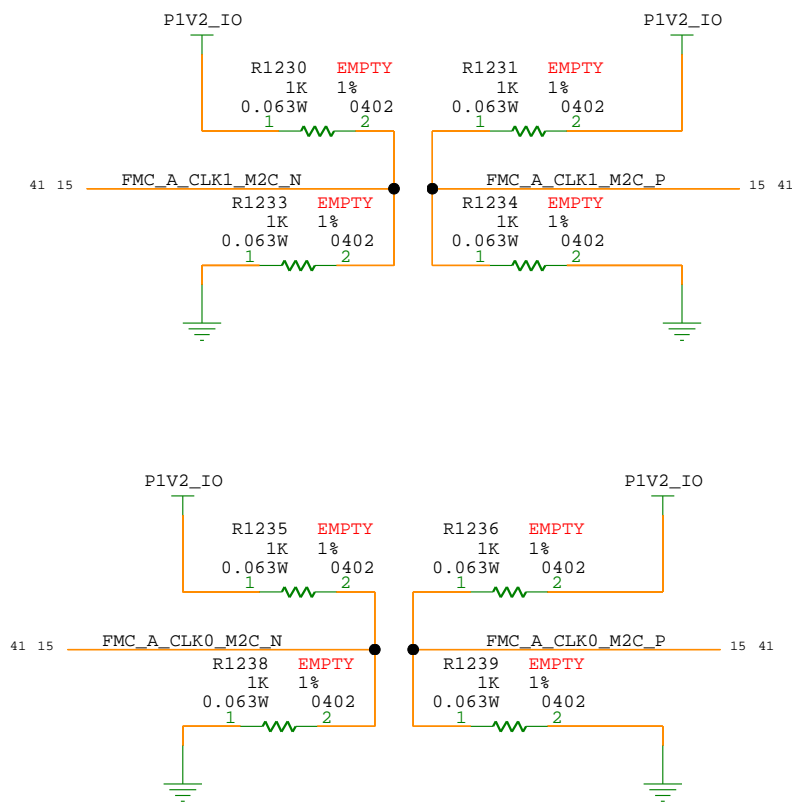
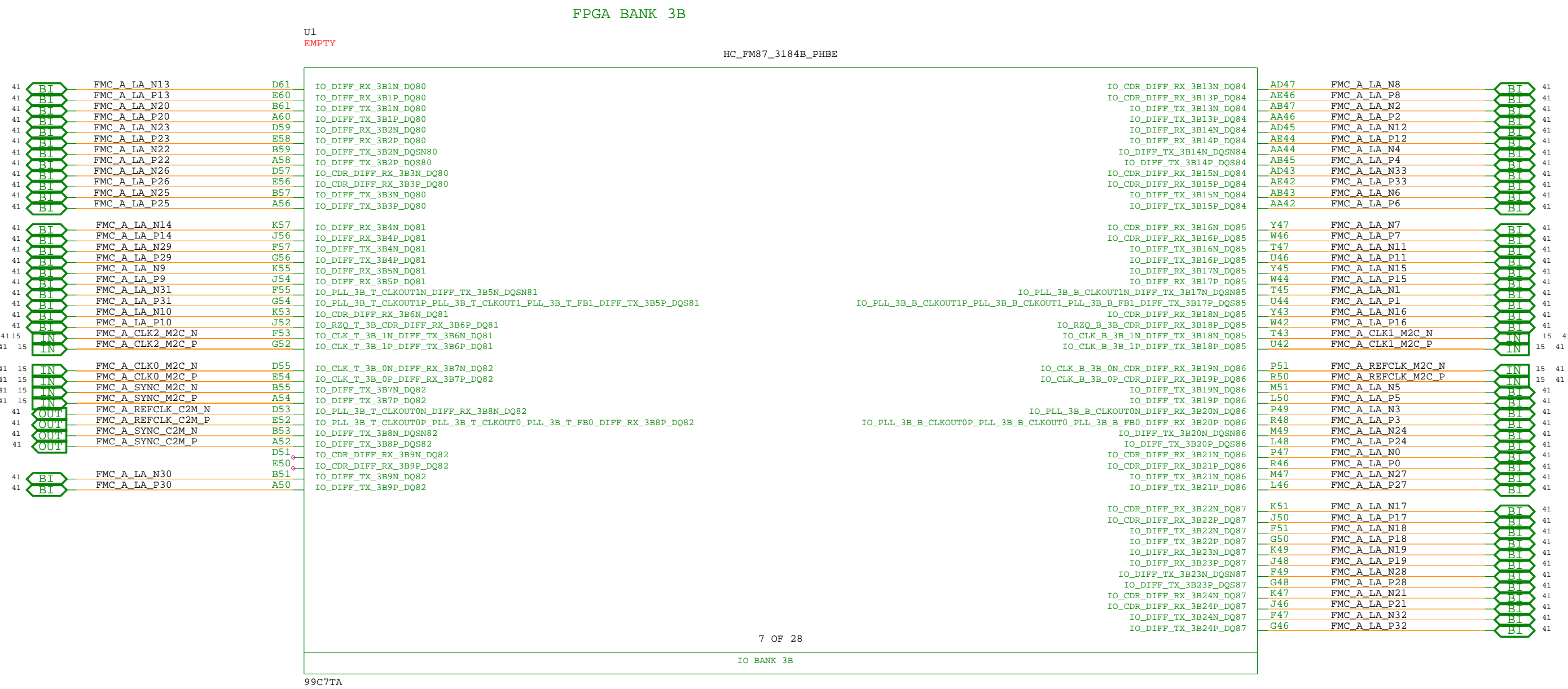
13 OF 95

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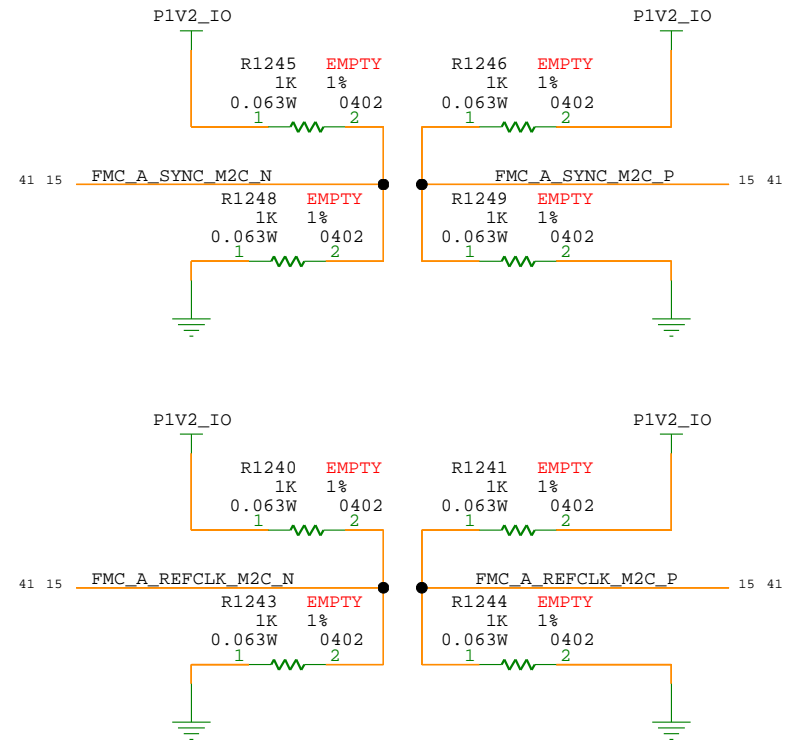
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CAD NOTE:
PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA



Thu Apr 10 09:49:24 2025

DEPARTMENT



SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-C1

REV

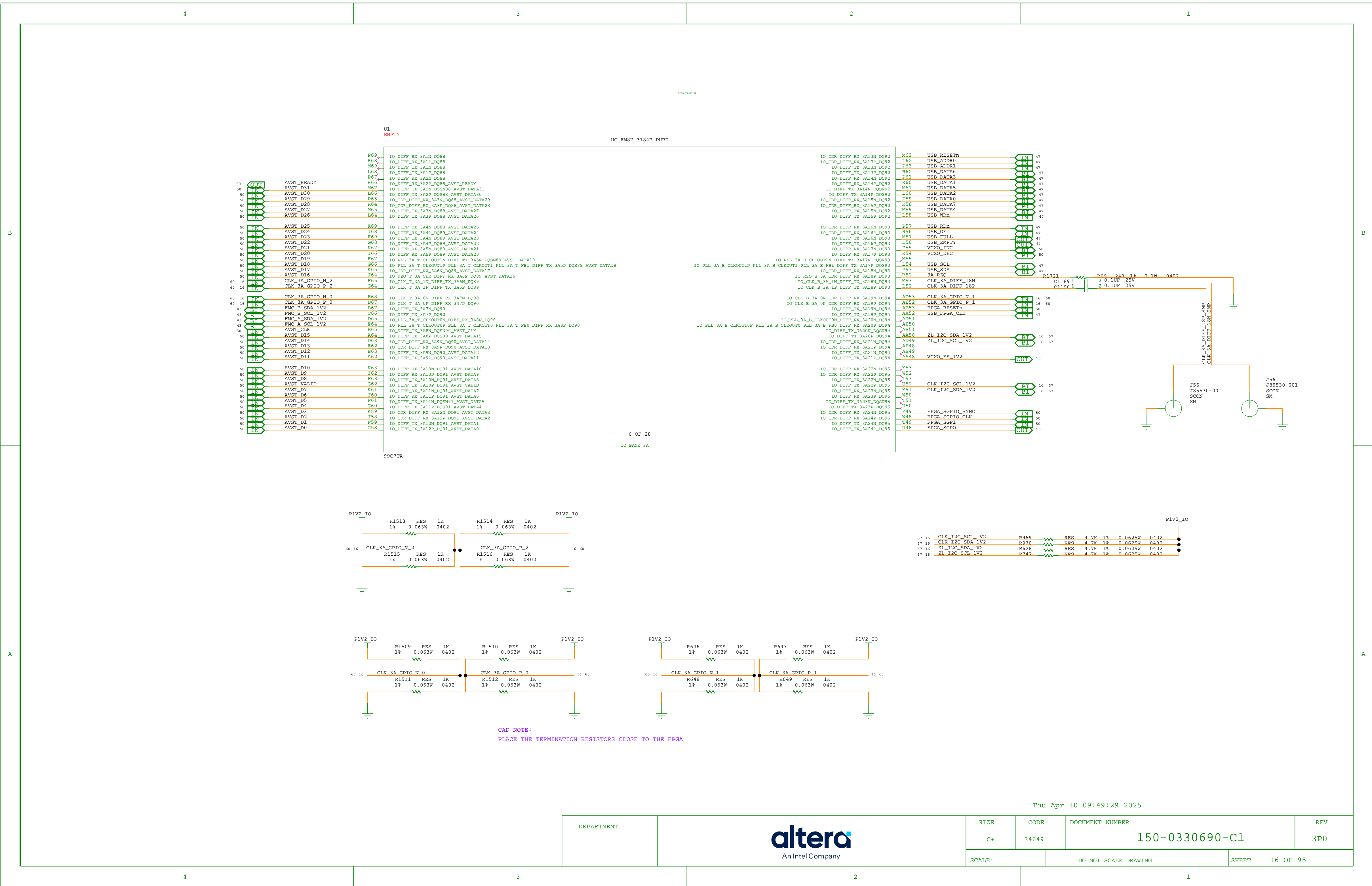
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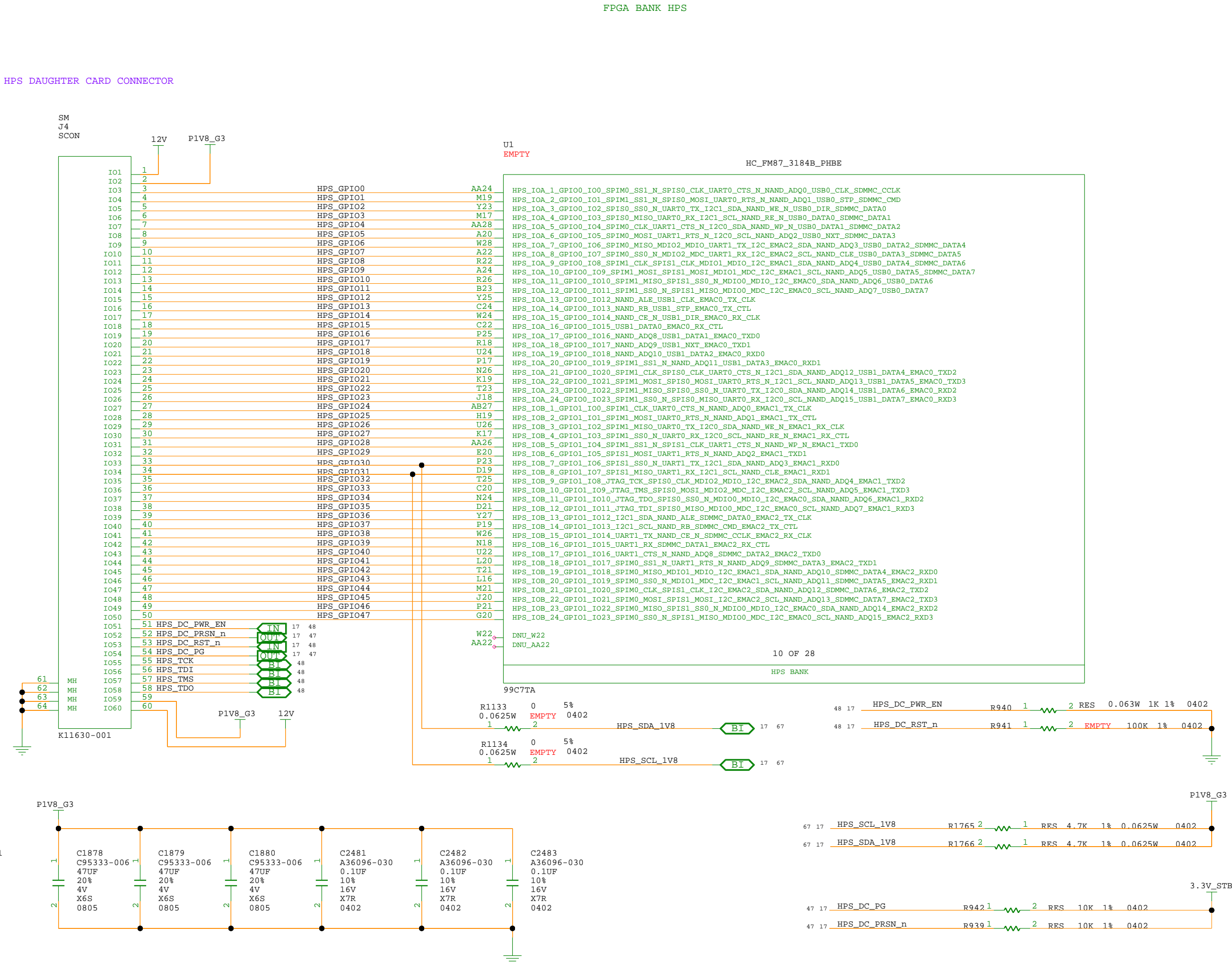
SHEET

15 OF 95



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B

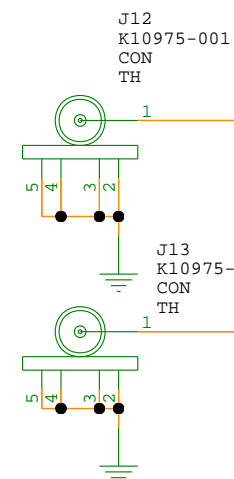
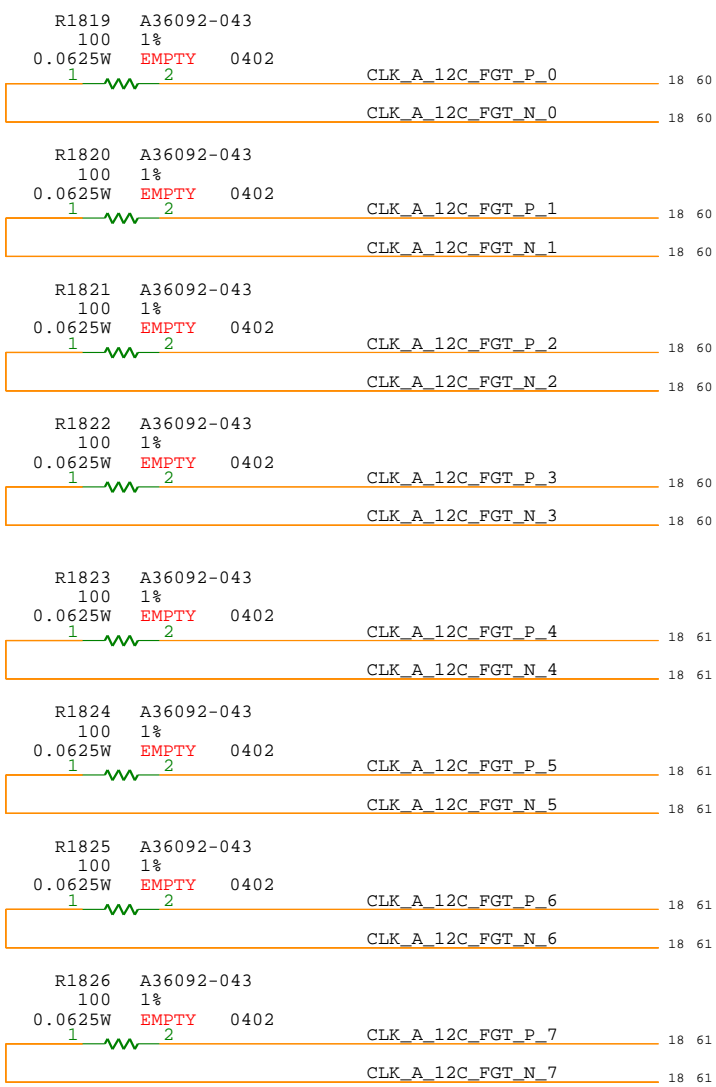


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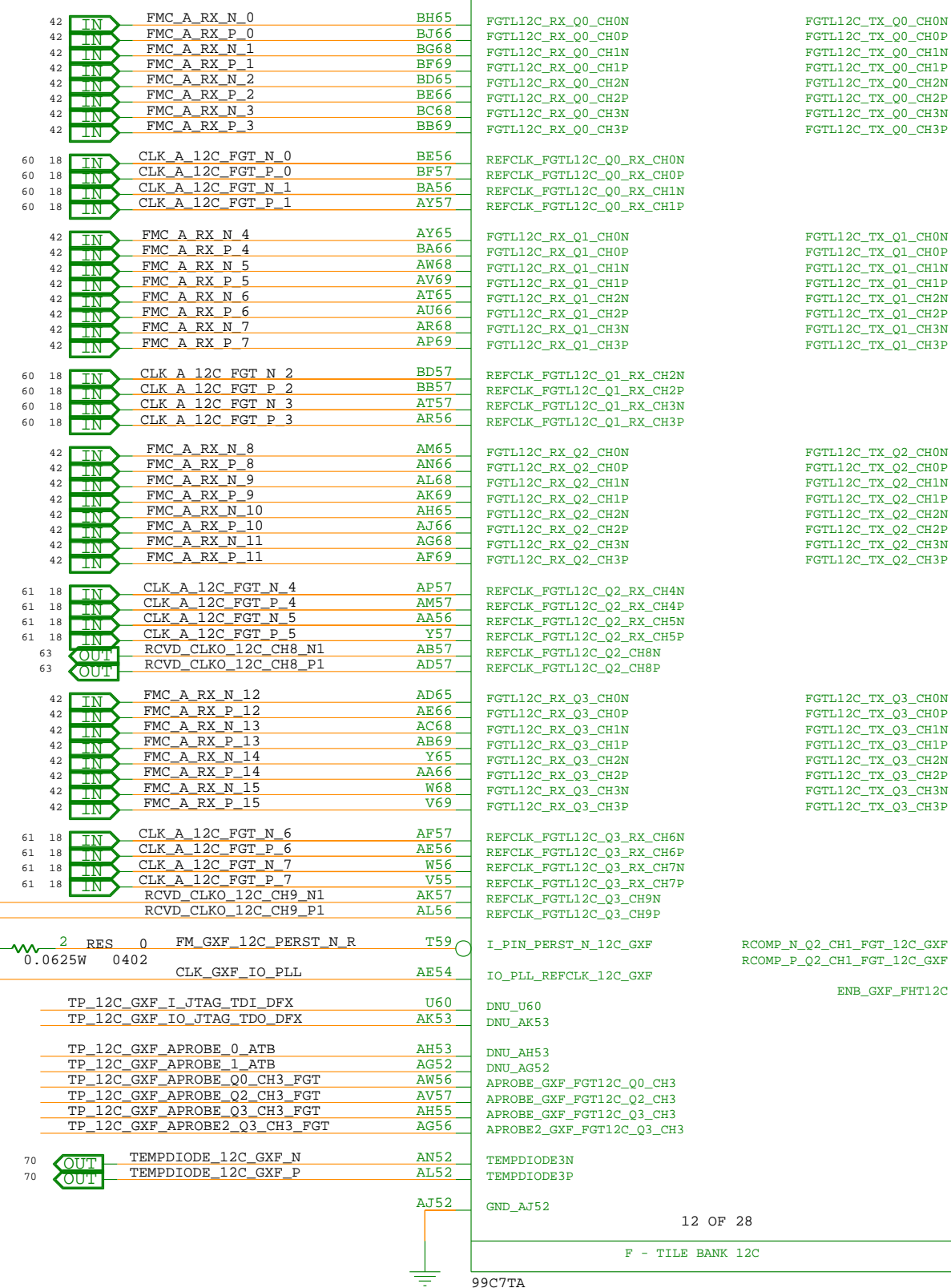
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Thu Apr 10 09:49:32 2025

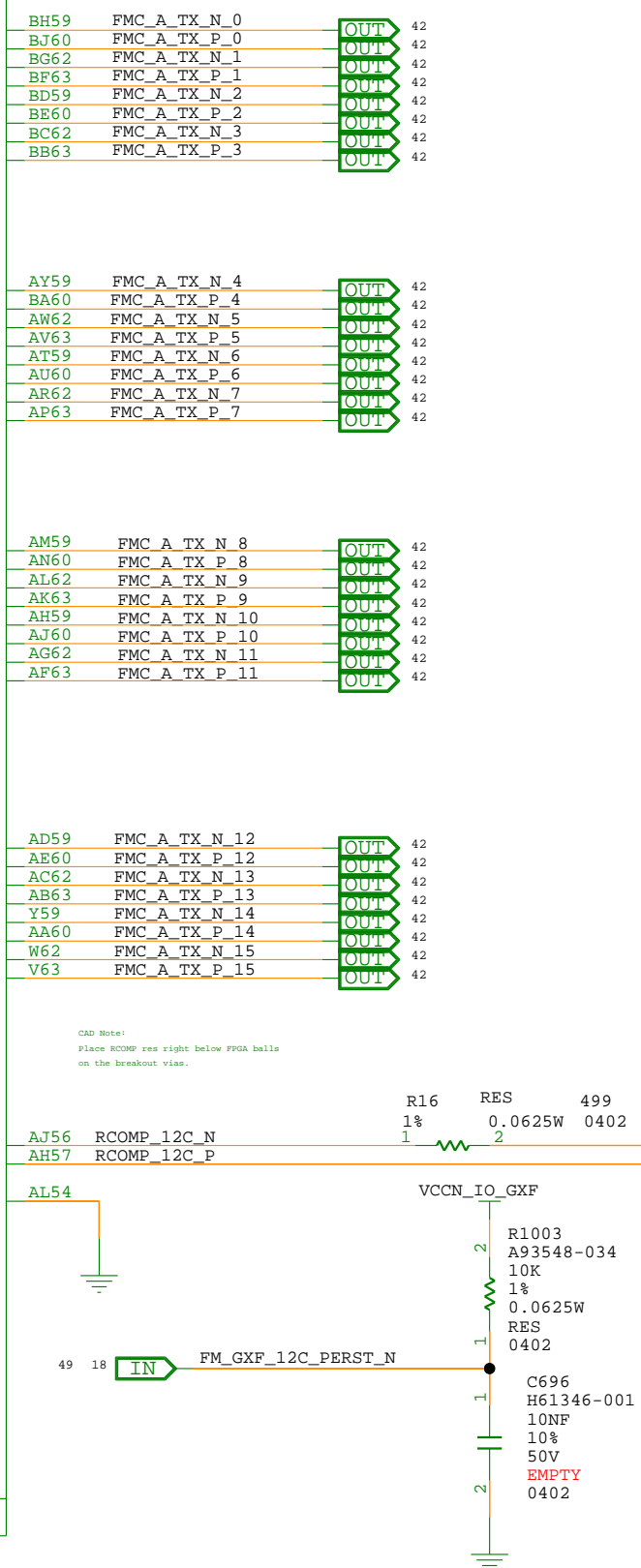
DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330690-C1	3P0
SCALE:		DO NOT SCALE DRAWING		SHEET	17 OF 95



CAD NOTE:
BREAK-OUT EVERY TP* NETS TO AN
EXPOSED PAD ON THE BOTTOM SIDE.



CAD NOTE: PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS.



DEPARTMENT



SIZE

CODE

DOCUMENT NUMBER

REV

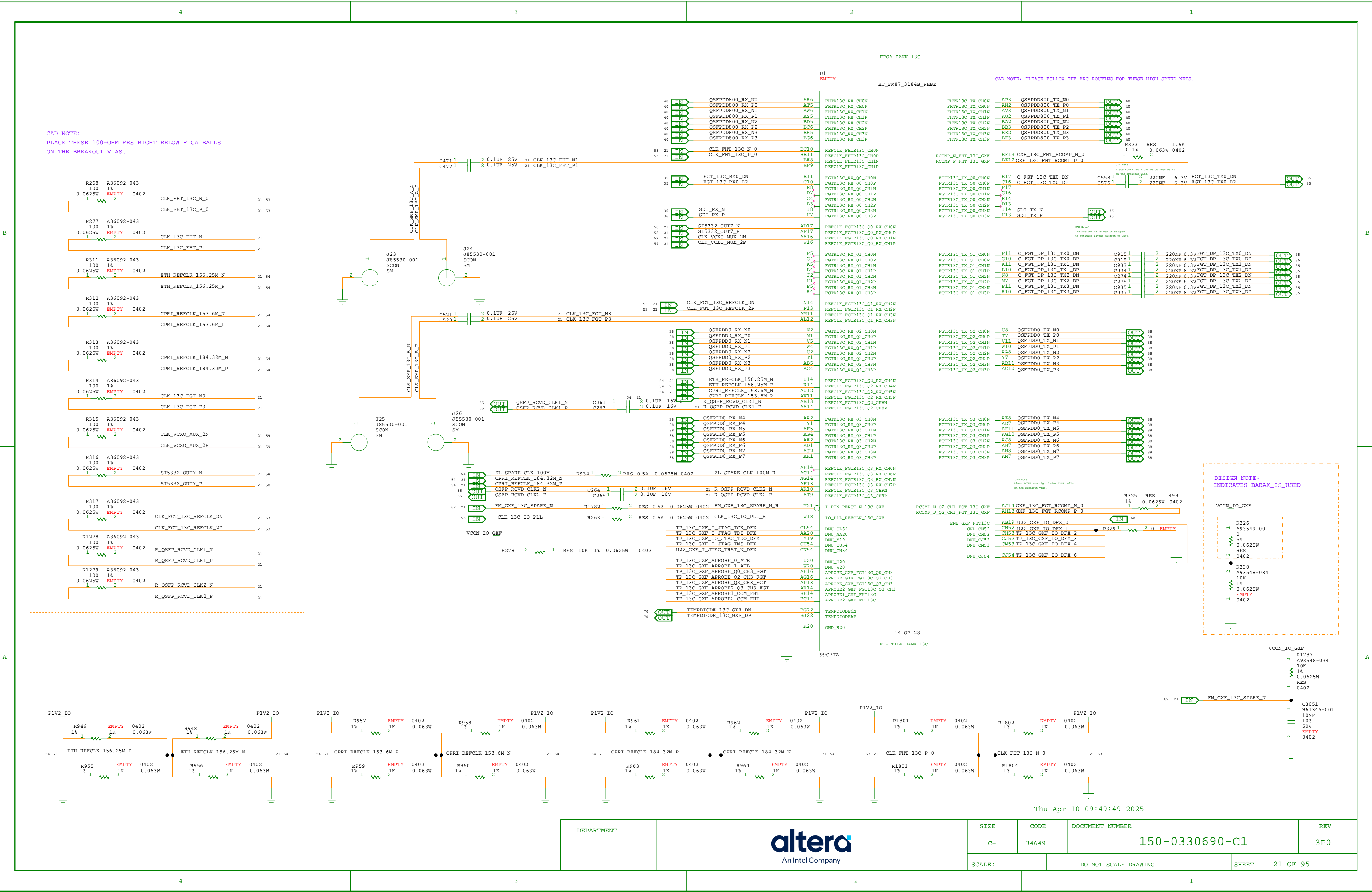
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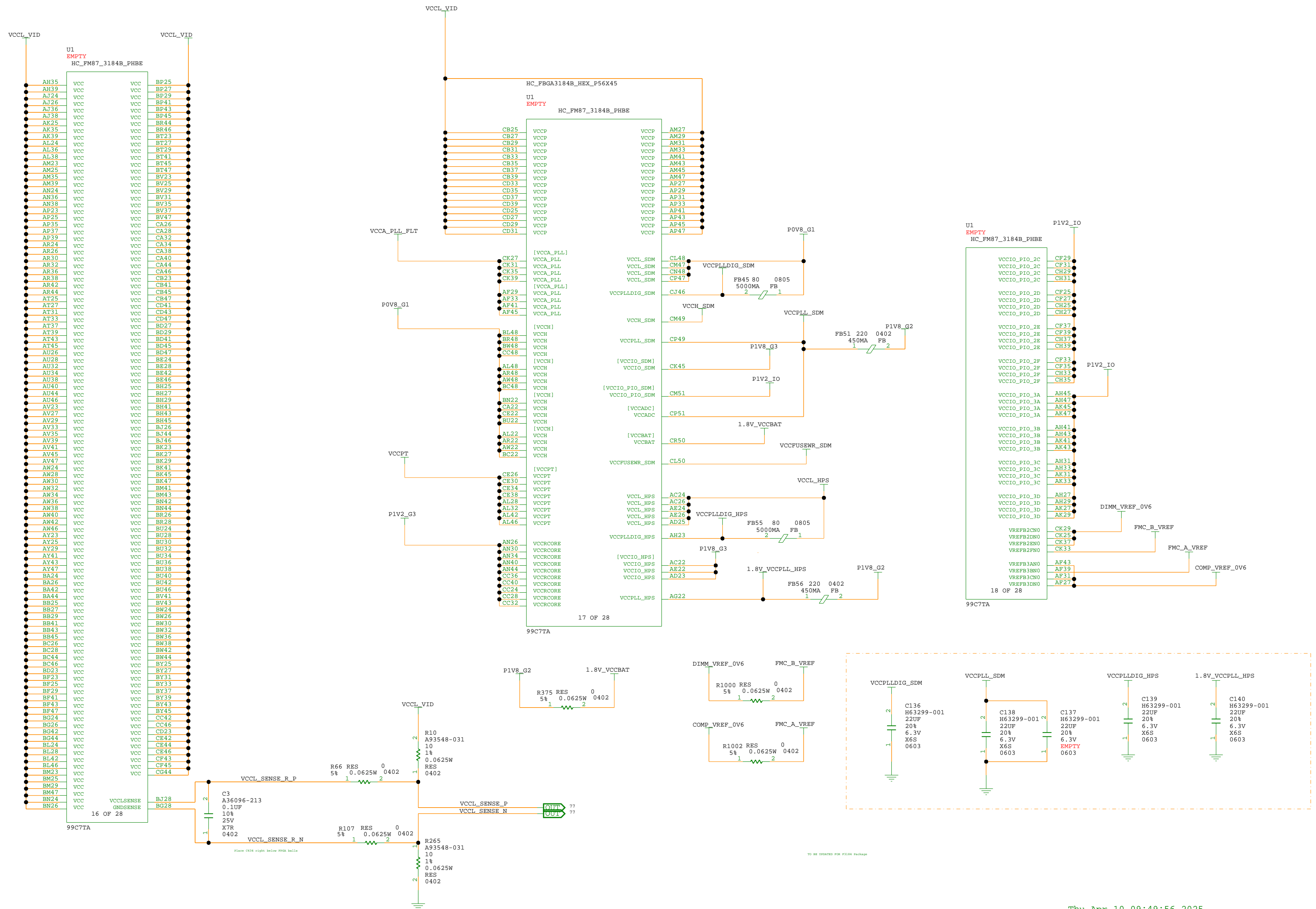
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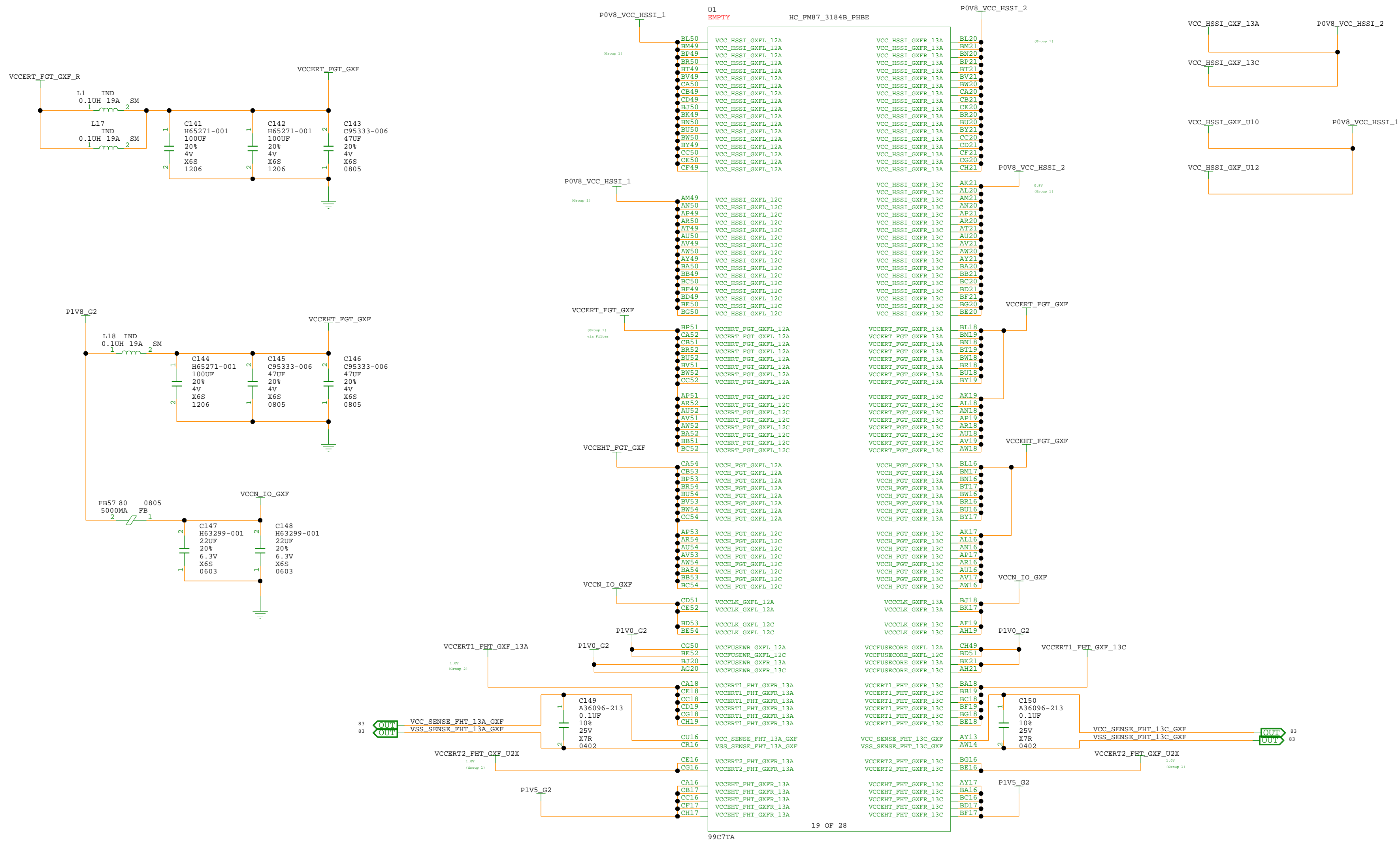
SHEET 18 OF 95





Thu Apr 10 09:49:56 2025

DEPARTMENT	<div> An Intel Company</div>	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330690-C1	3P0
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Thu Apr 10 09:50:00 2025

DEPARTMENT

altera
An Intel Company

SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-C1

REV

3P0

SCALE:

DO NOT SCALE DRAWING

SHEET

23 OF 95

B

A

B

A

FPGA GND- I

U1
EMPTY
HC_FM87_3184B_PHB8

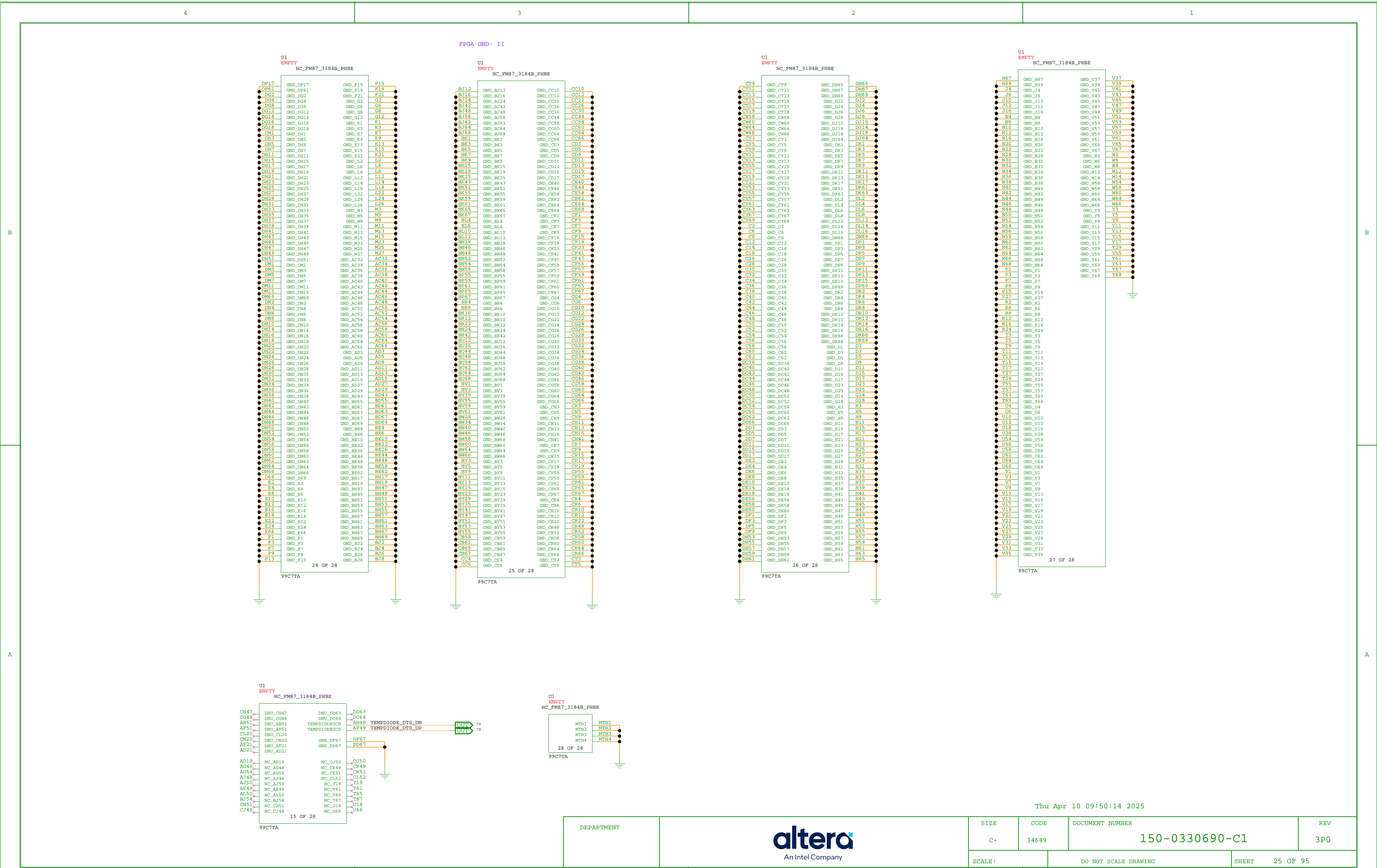
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AA64 GND_AA64
AA68 GND_AA68
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AB3 GND_AB3
AB7 GND_AB7
AB9 GND_AB9
AB15 GND_AB15
AB17 GND_AB17
AB21 GND_AB21
AB23 GND_AB23
AB25 GND_AB25
AB29 GND_AB29
AB55 GND_AB55
AB59 GND_AB59
AB61 GND_AB61
AB65 GND_AB65
AB67 GND_AB67
AC2 GND_AC2
AC6 GND_AC6
AC8 GND_AC8
AC12 GND_AC12
AC16 GND_AC16
AC18 GND_AC18
AC20 GND_AC20
AC28 GND_AC28
AC30 GND_AC30
AD55 GND_AD55
AD61 GND_AD61
AD63 GND_AD63
AD67 GND_AD67
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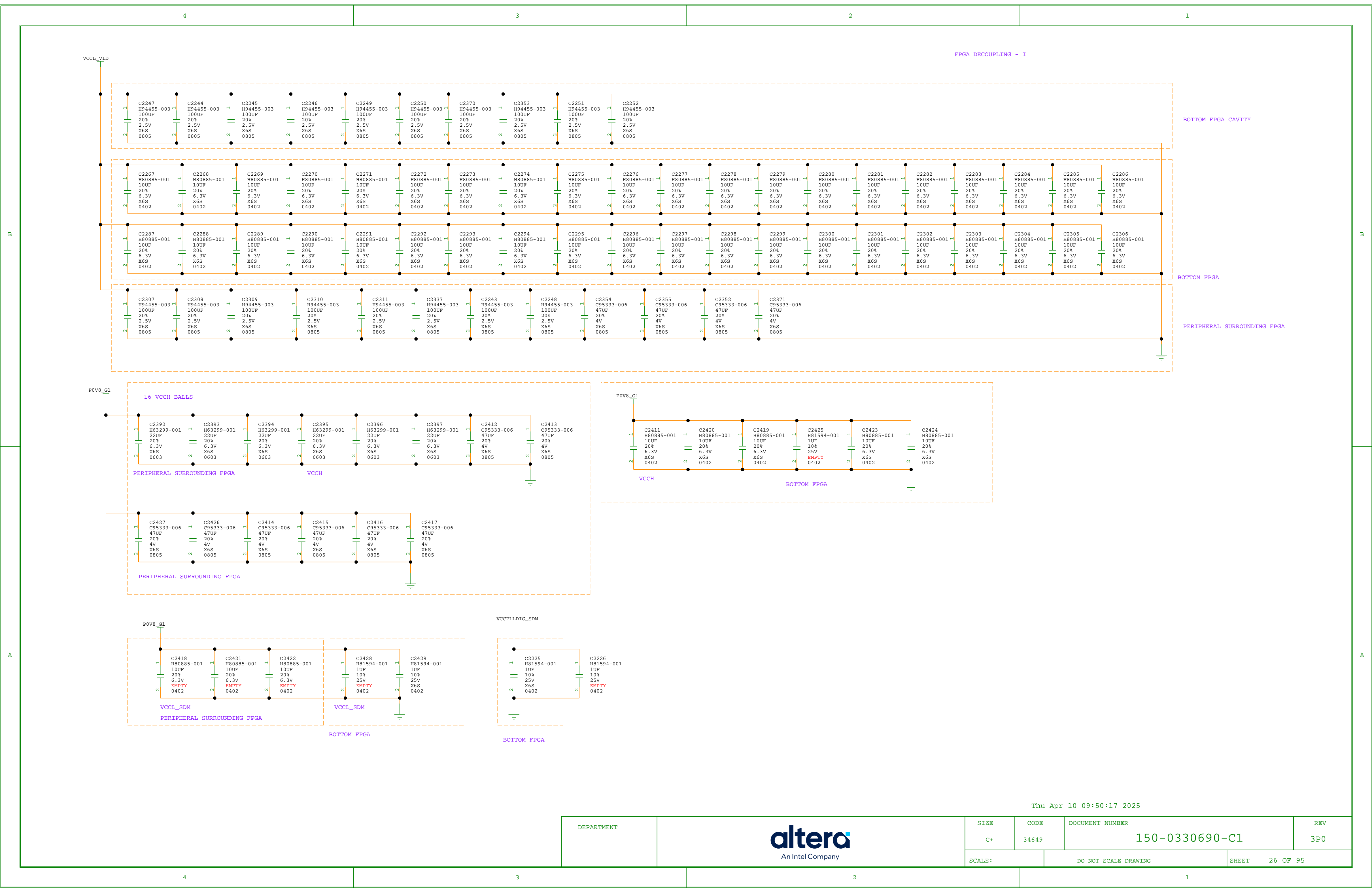
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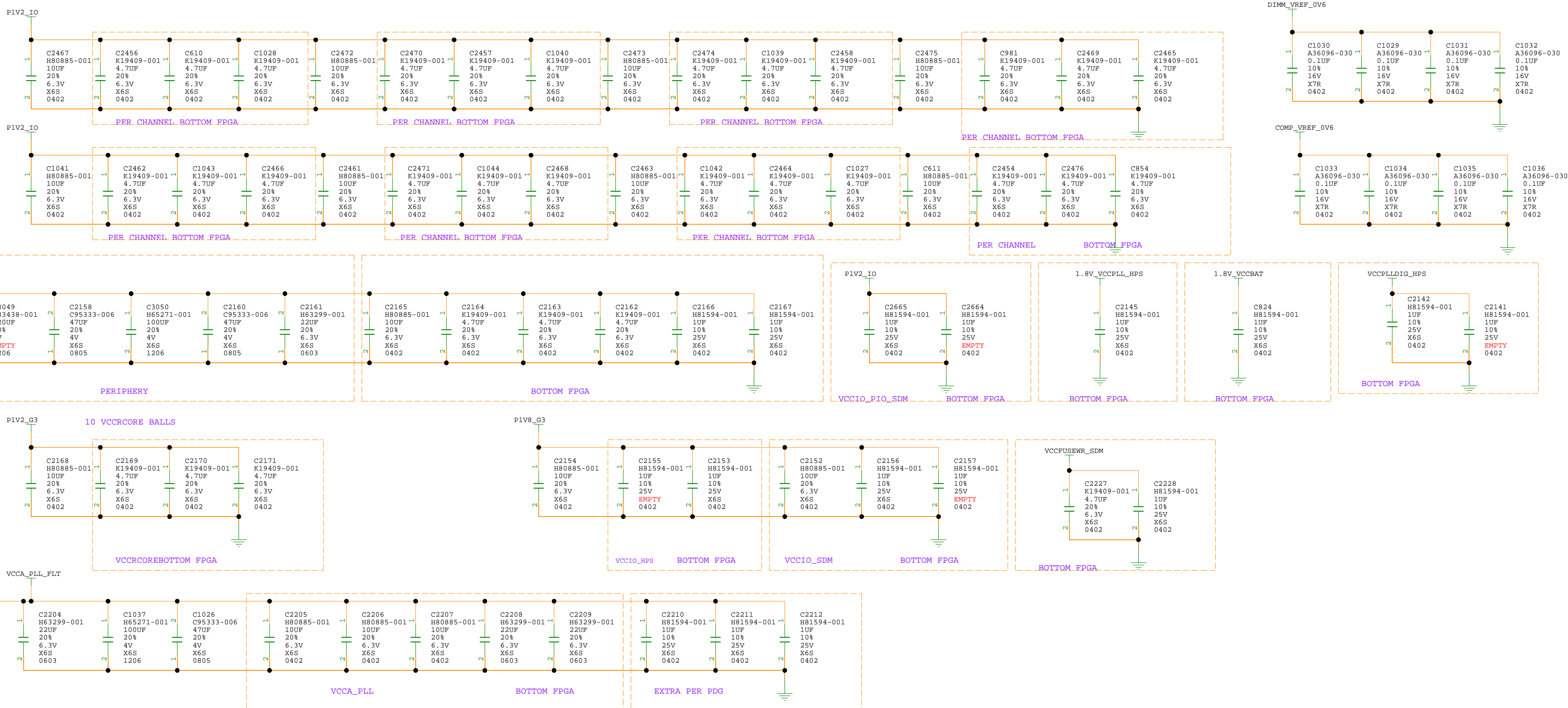
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BB1224 GND_BB1224
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BB1230 GND_BB1230
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BB1440 GND_BB1440
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BB1448 GND_BB1448
BB1450 GND_BB1450




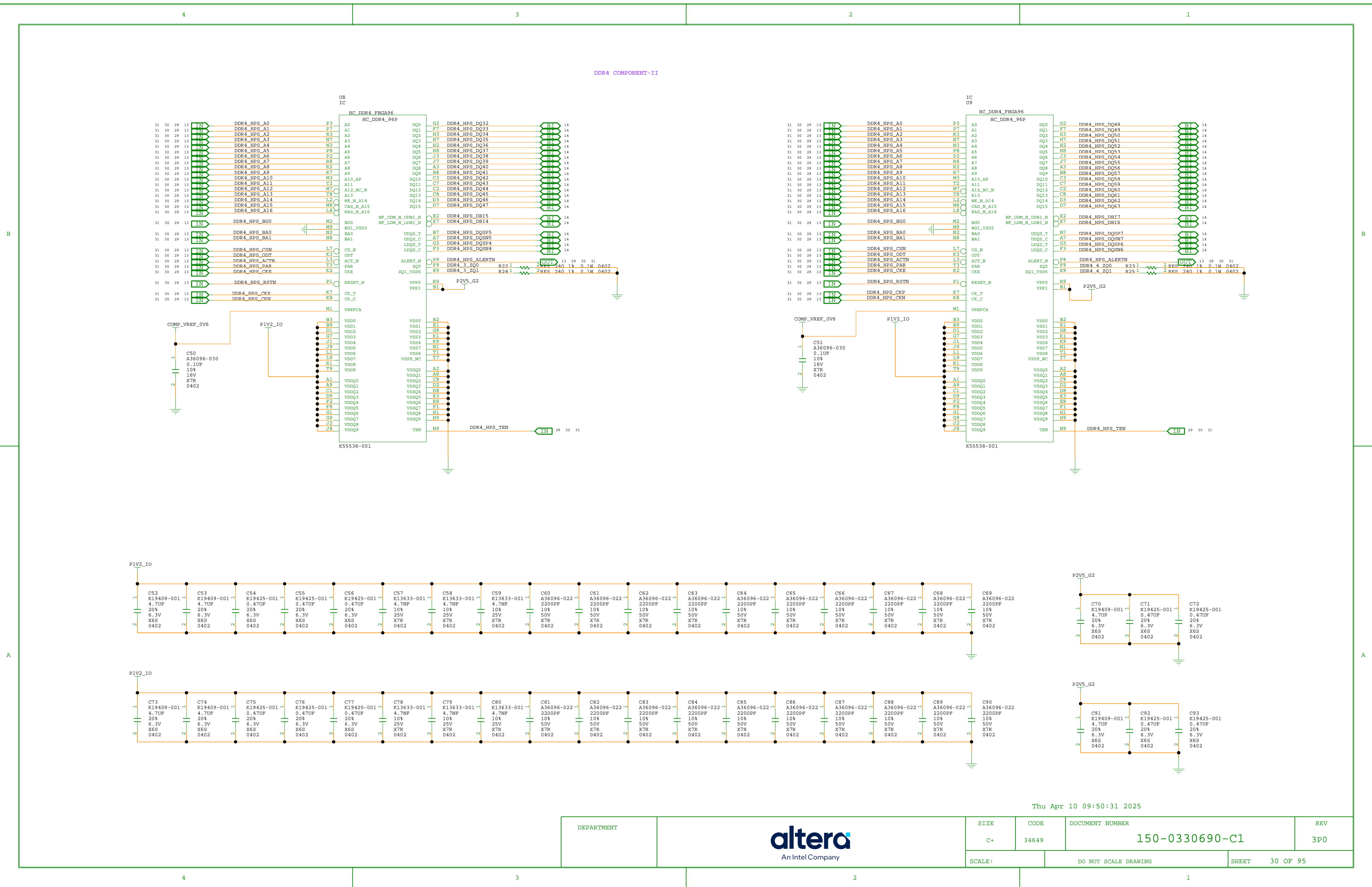


Thu Apr 10 09:50:17 2025

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330690-C1	3P0
		SCALE:	DO NOT SCALE DRAWING		SHEET 26 OF 95



DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330690-C1	3P0
		SCALE:	DO NOT SCALE DRAWING		SHEET 27 OF 95



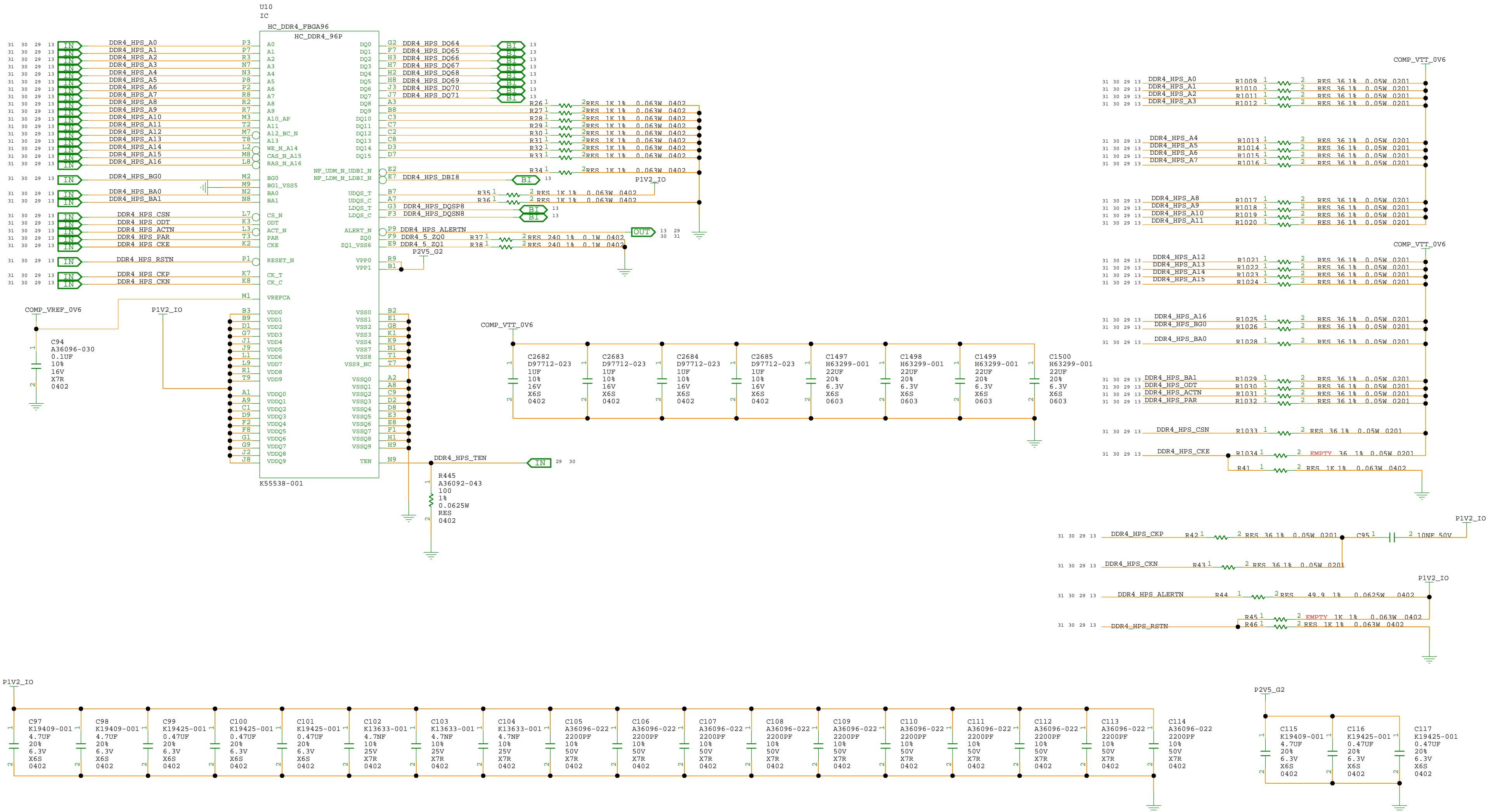
B

B


A

A

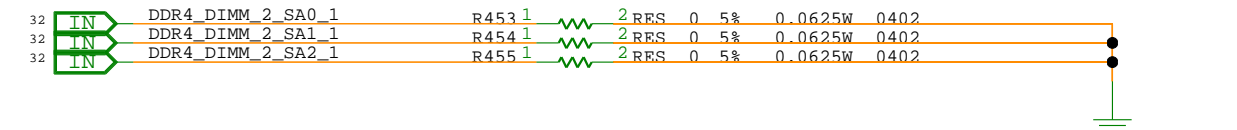
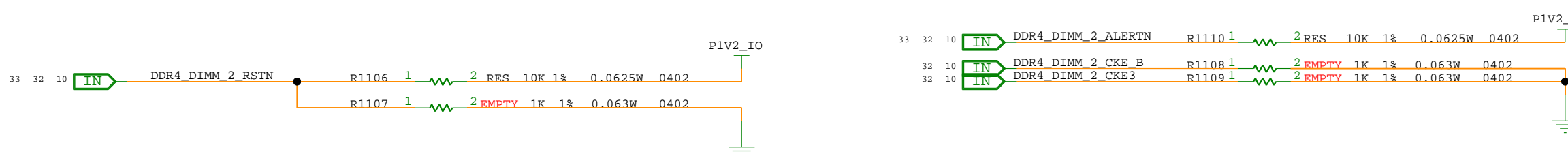
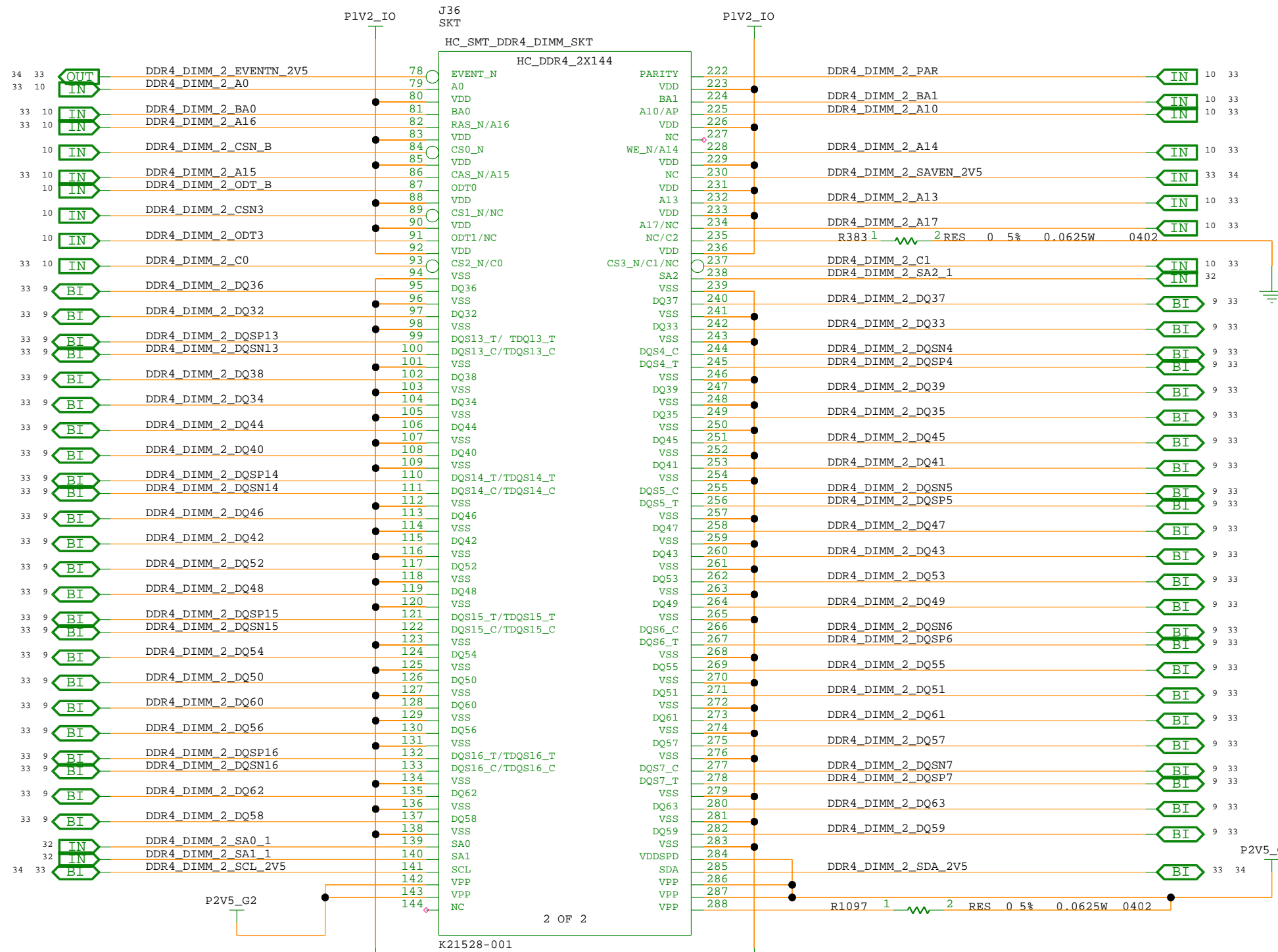
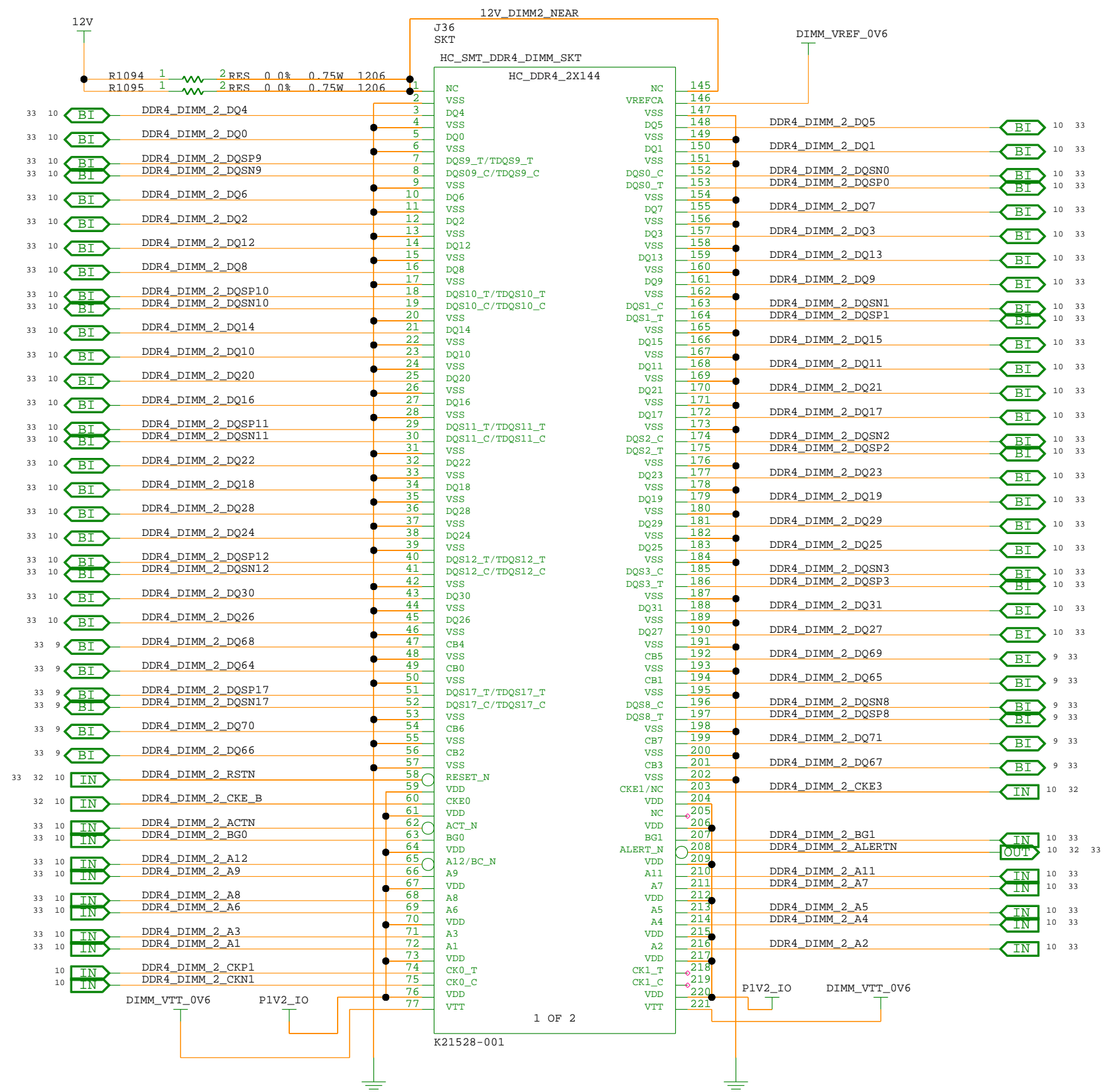
DDR4 COMPONENT-III



Thu Apr 10 09:50:34 2025

DEPARTMENT	<div> An Intel Company</div>	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330690-C1	3P0
		SCALE:		DO NOT SCALE DRAWING	SHEET 31 OF 95

2DPC DIMM-I



SIMULATION BASED ON
MTA18ASF2G72P2-3G2E2 16GB SRX4 DDR4-3200
MTA36ASF4G72P2-2G6E1 32GB DRX4 DDR4-2666

Thu Apr 10 09:50:41 2025

DEPARTMENT



SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-C1

REV

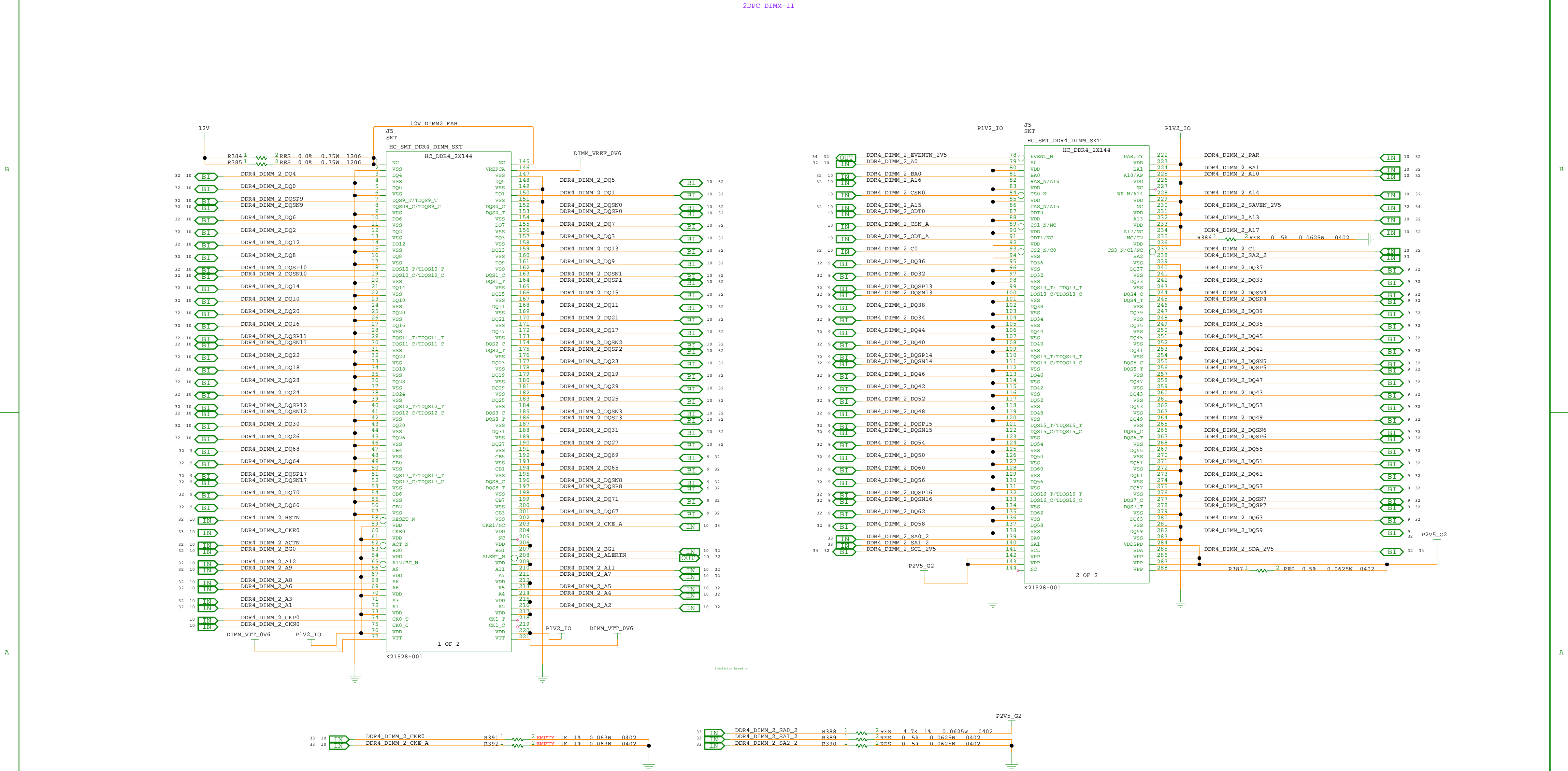
3P0

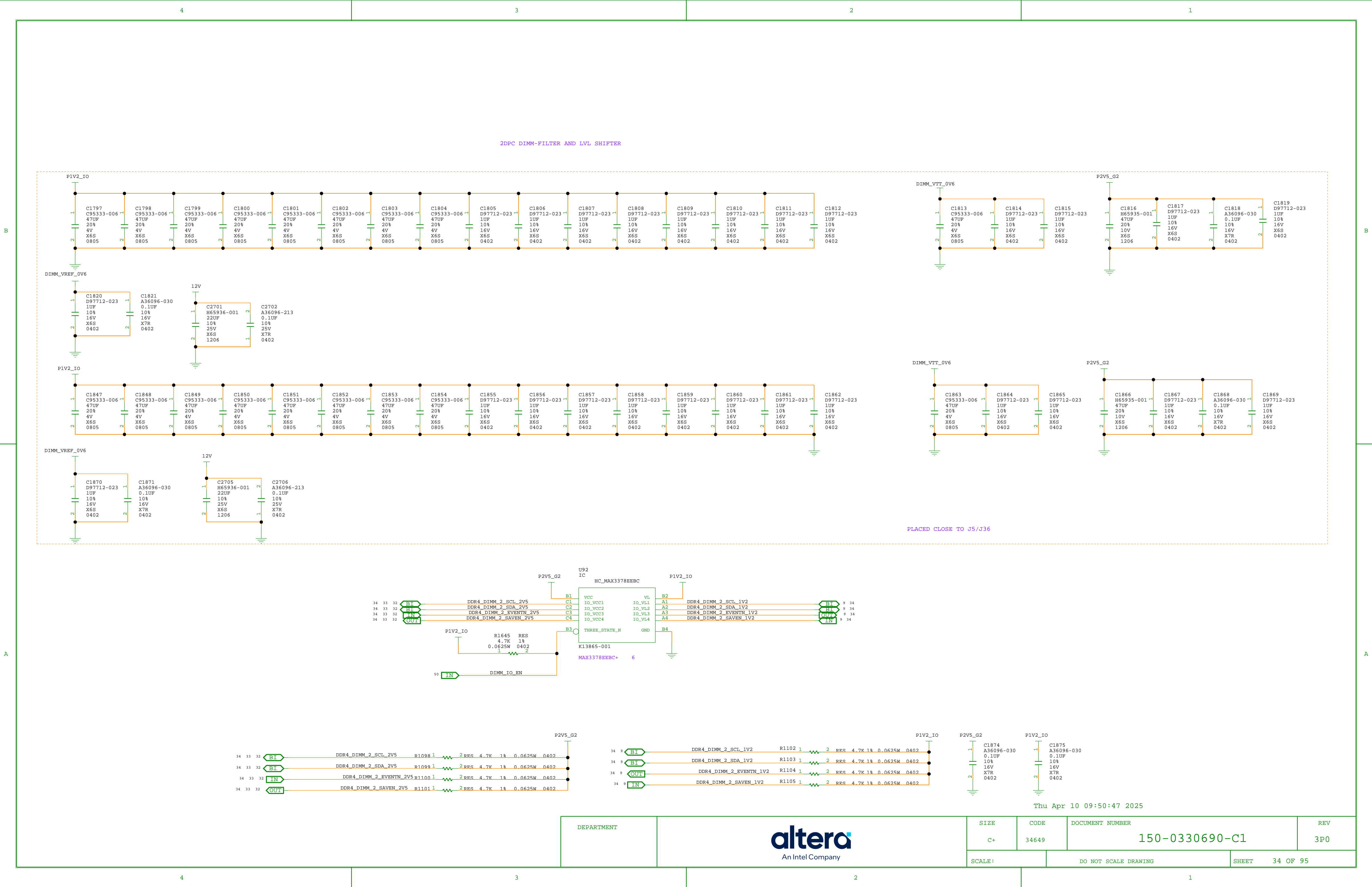
SCALE:

DO NOT SCALE DRAWING

SHEET

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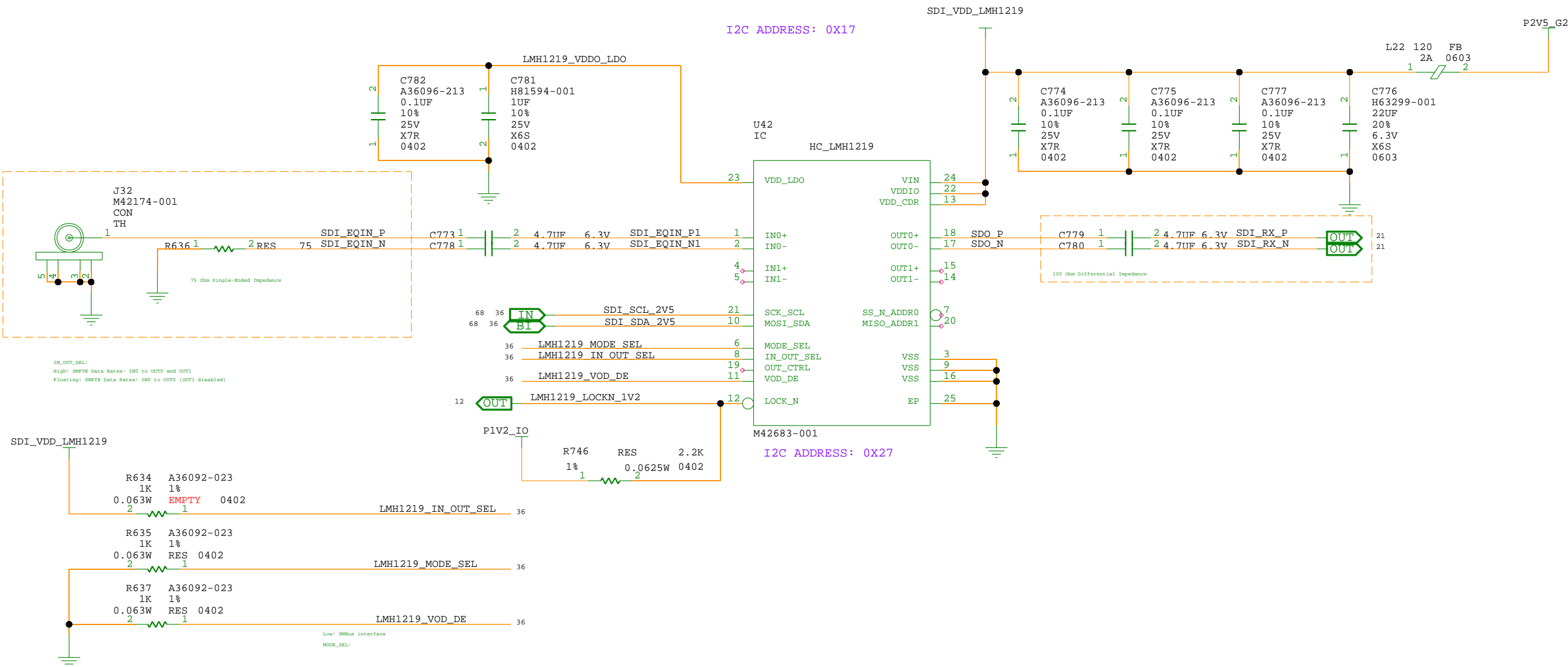
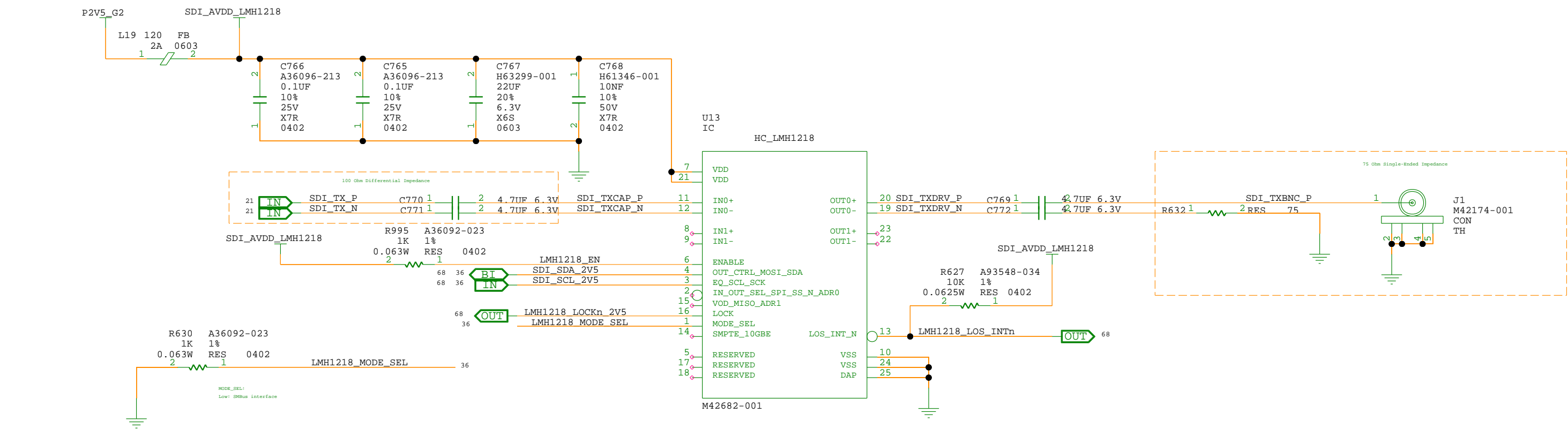


4



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SDI CABLE DRIVER, EQUALIZER, BNC



Thu Apr 10 09:50:56 2025

DEPARTMENT



SIZE

CODE

DOCUMENT NUMBER

REV

C+

34649

150-0330690-C1

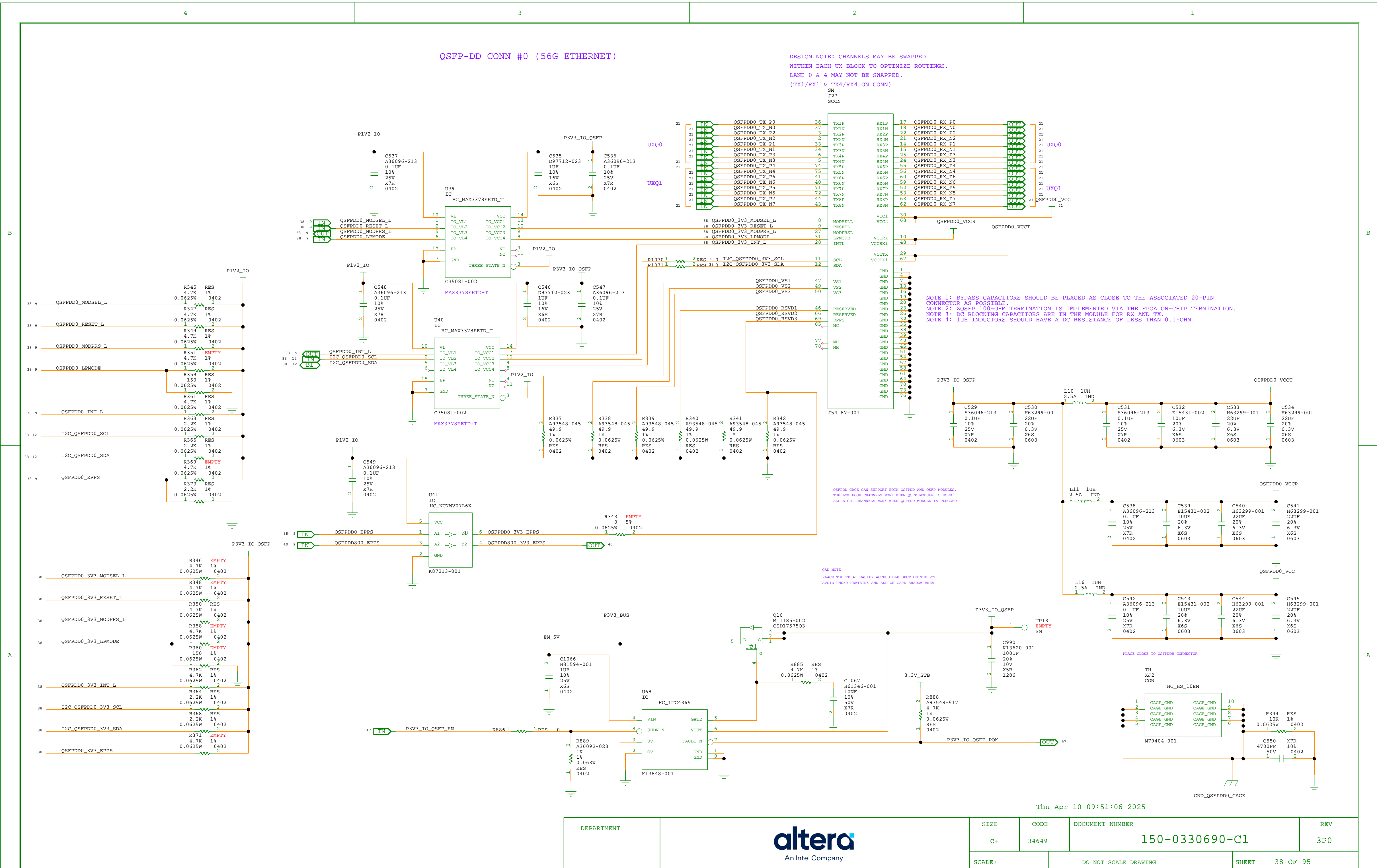
3P0

SCALE:

DO NOT SCALE DRAWING

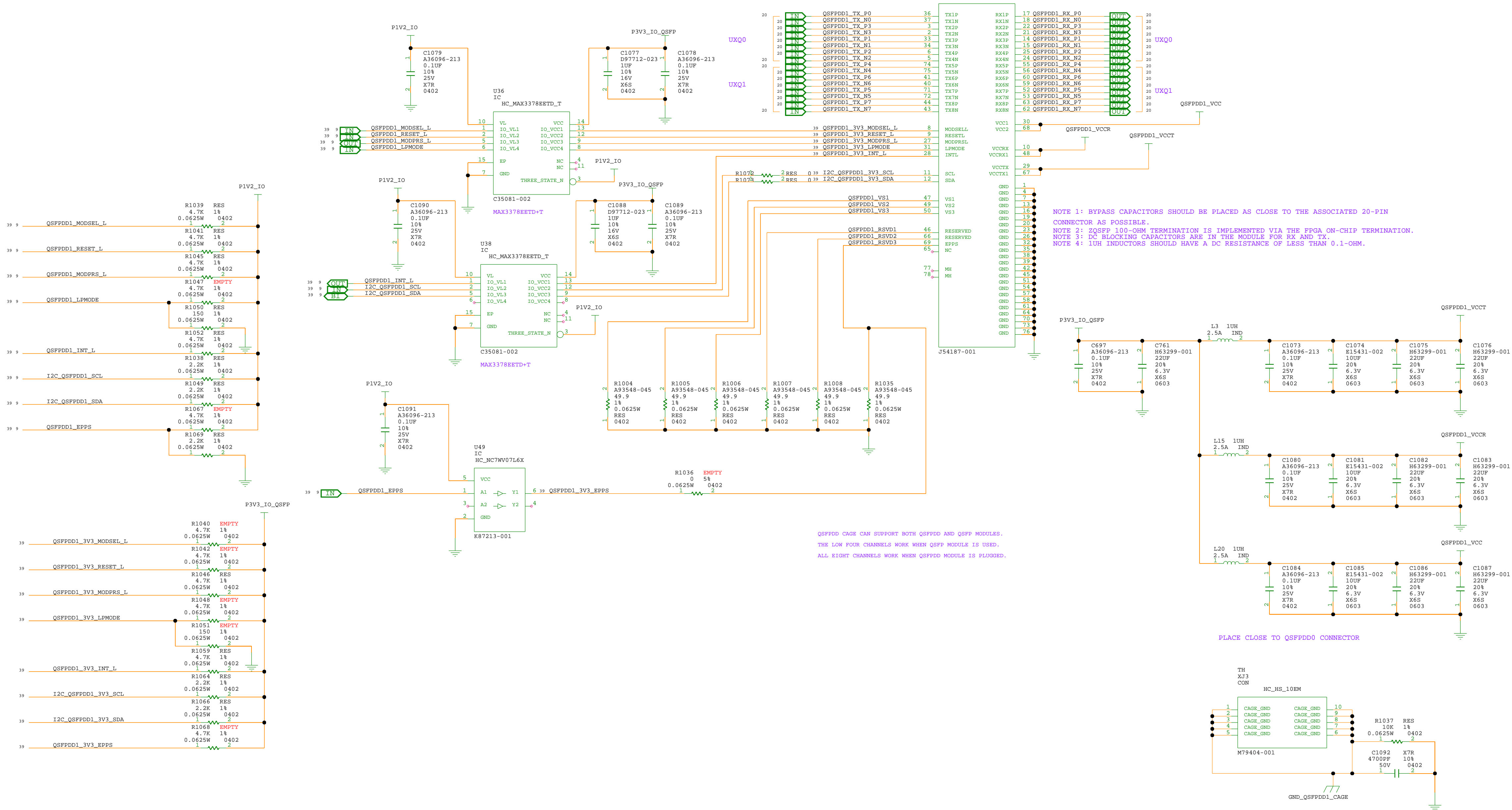
SHEET

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QSFP-DD CONN #1 (56G ETHERNET)

DESIGN NOTE: CHANNELS MAY BE SWAPPED
WITHIN EACH UX BLOCK TO OPTIMIZE ROUTINGS.
LANE 0 & 4 MAY NOT BE SWAPPED.
(TX1/RX1 & TX4/RX4 ON CONN)



Thu Apr 10 09:51:09 2025

DEPARTMENT

altera
An Intel Company

SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-C1

REV

3P0

SCALE:

DO NOT SCALE DRAWING

SHEET

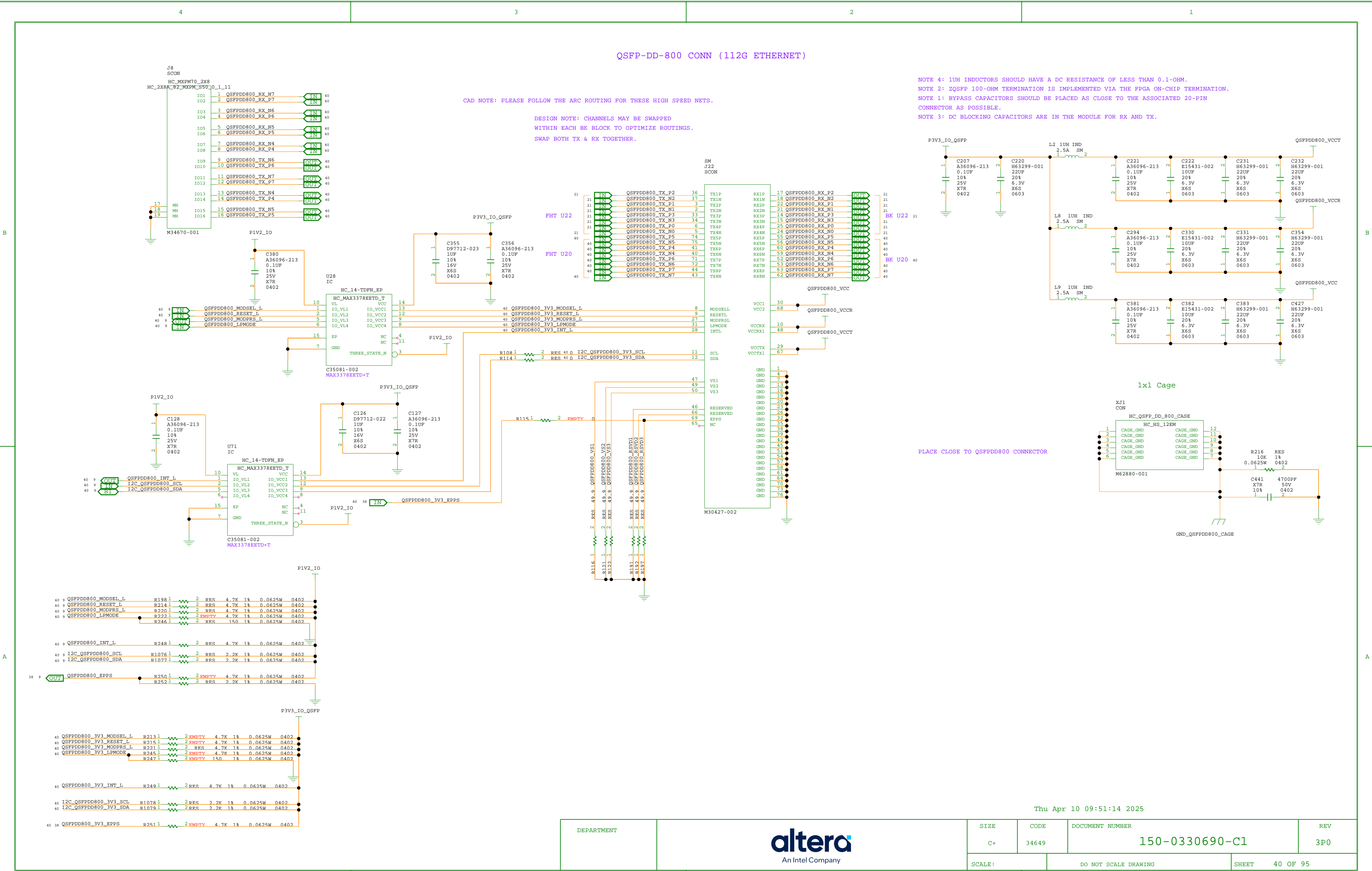
39 OF 95

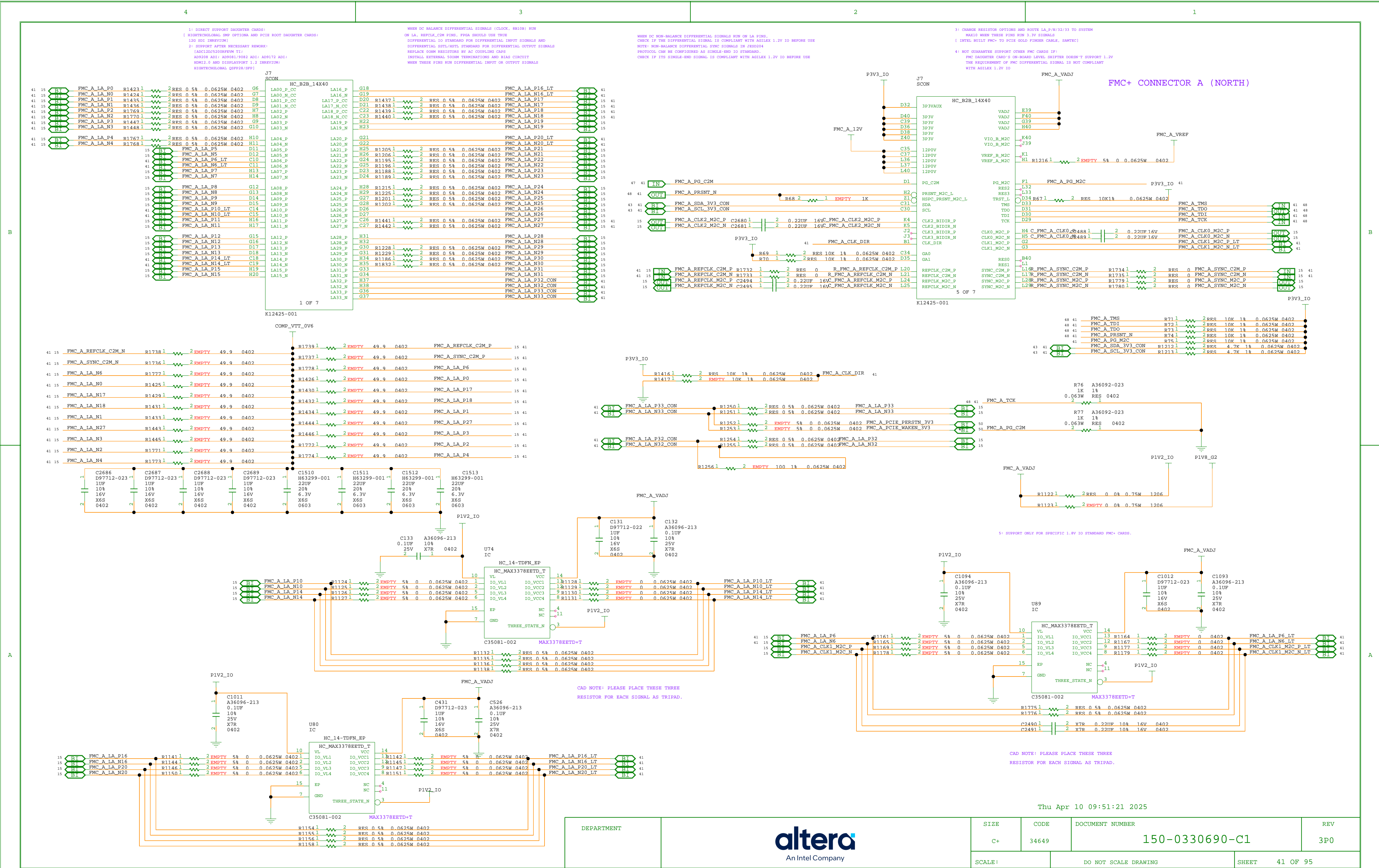
QSFP-DD-800 CONN (112G ETHERNET)

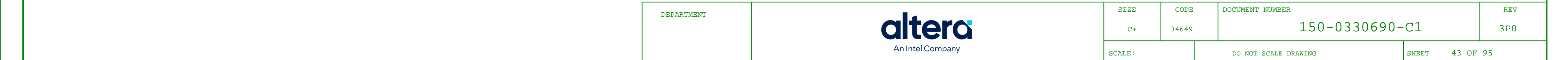
CAD NOTE: PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS.

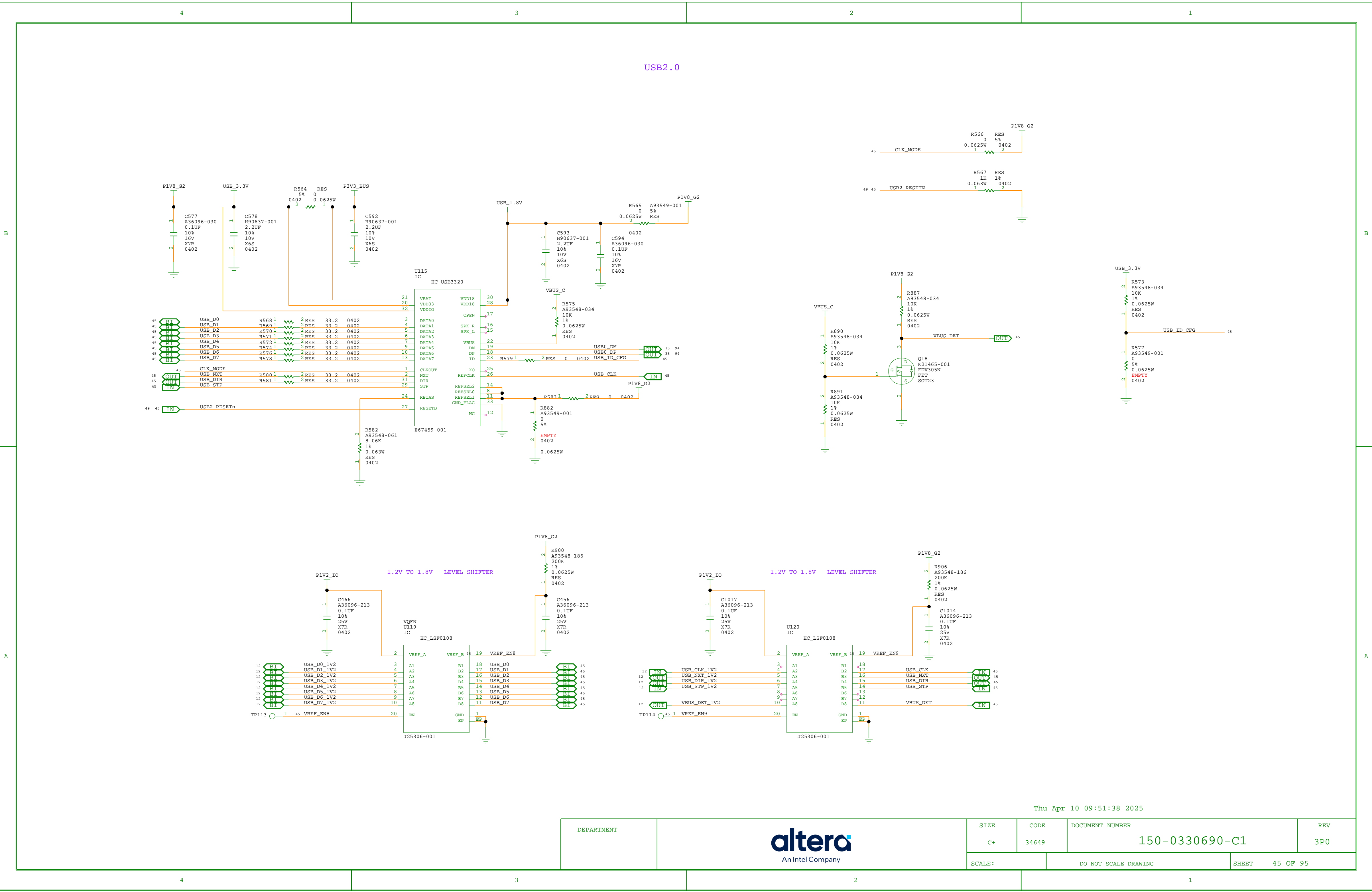
DESIGN NOTE: CHANNELS MAY BE SWAPPED
WITHIN EACH BK BLOCK TO OPTIMIZE ROUTINGS.
SWAP BOTH TX & RX TOGETHER.

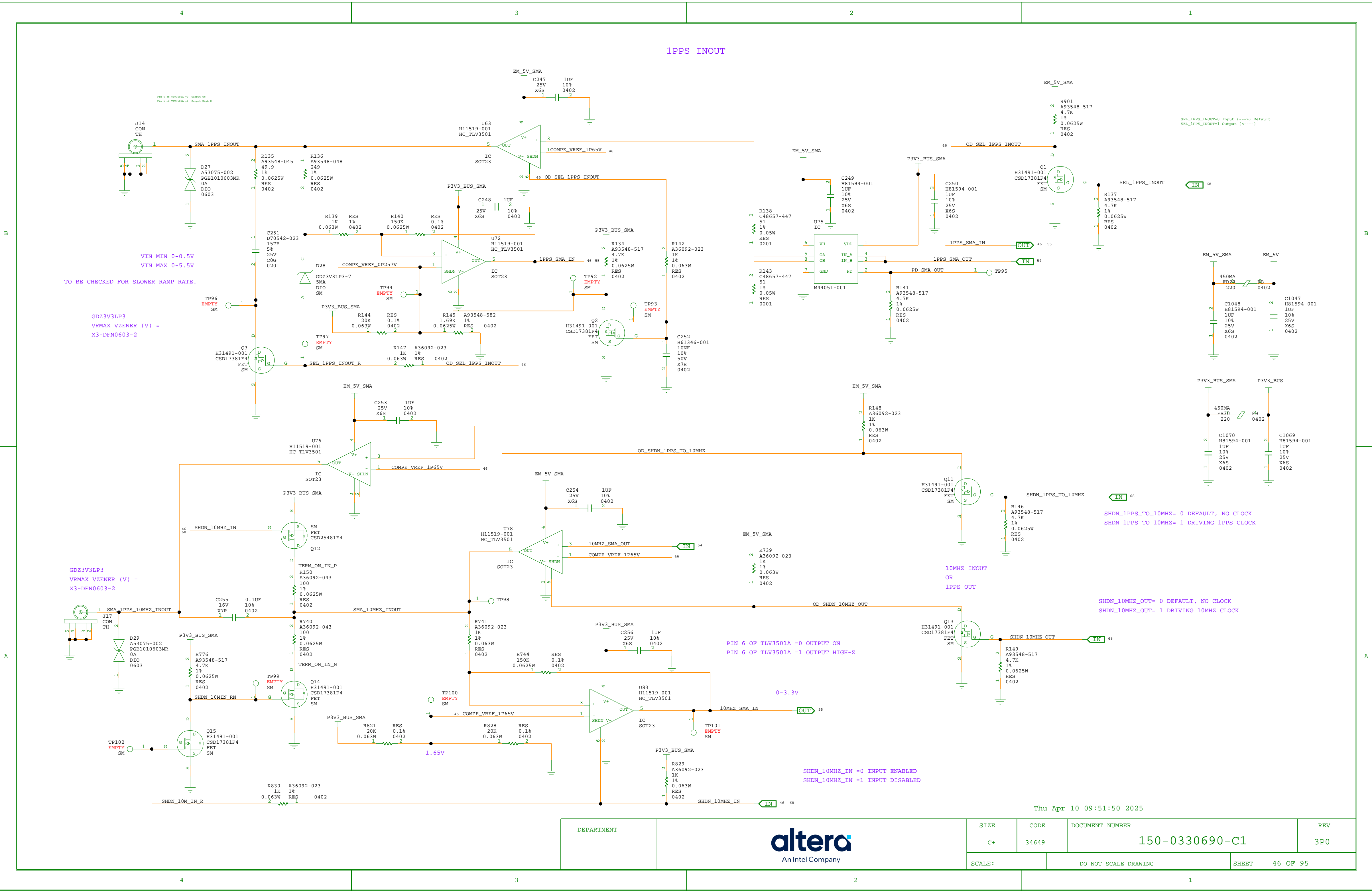
NOTE 4: 1UH INDUCTORS SHOULD HAVE A DC RESISTANCE OF LESS THAN 0.1-OHM.
NOTE 2: ZQSFP 100-OHM TERMINATION IS IMPLEMENTED VIA THE FPGA ON-CHIP TERMINATION.
NOTE 1: BYPASS CAPACITORS SHOULD BE PLACED AS CLOSE TO THE ASSOCIATED 20-PIN
CONNECTOR AS POSSIBLE.
NOTE 3: DC BLOCKING CAPACITORS ARE IN THE MODULE FOR RX AND TX.



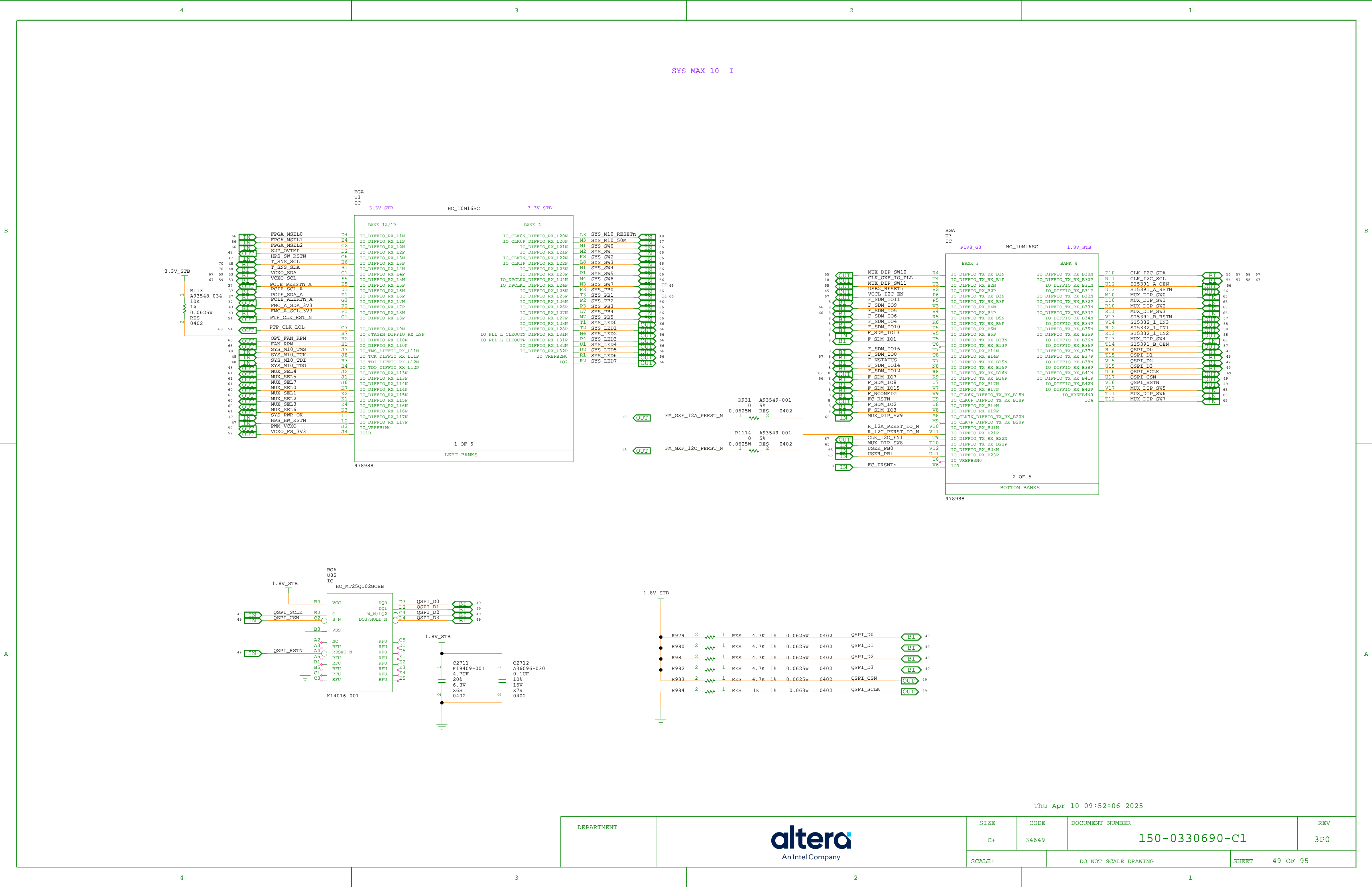




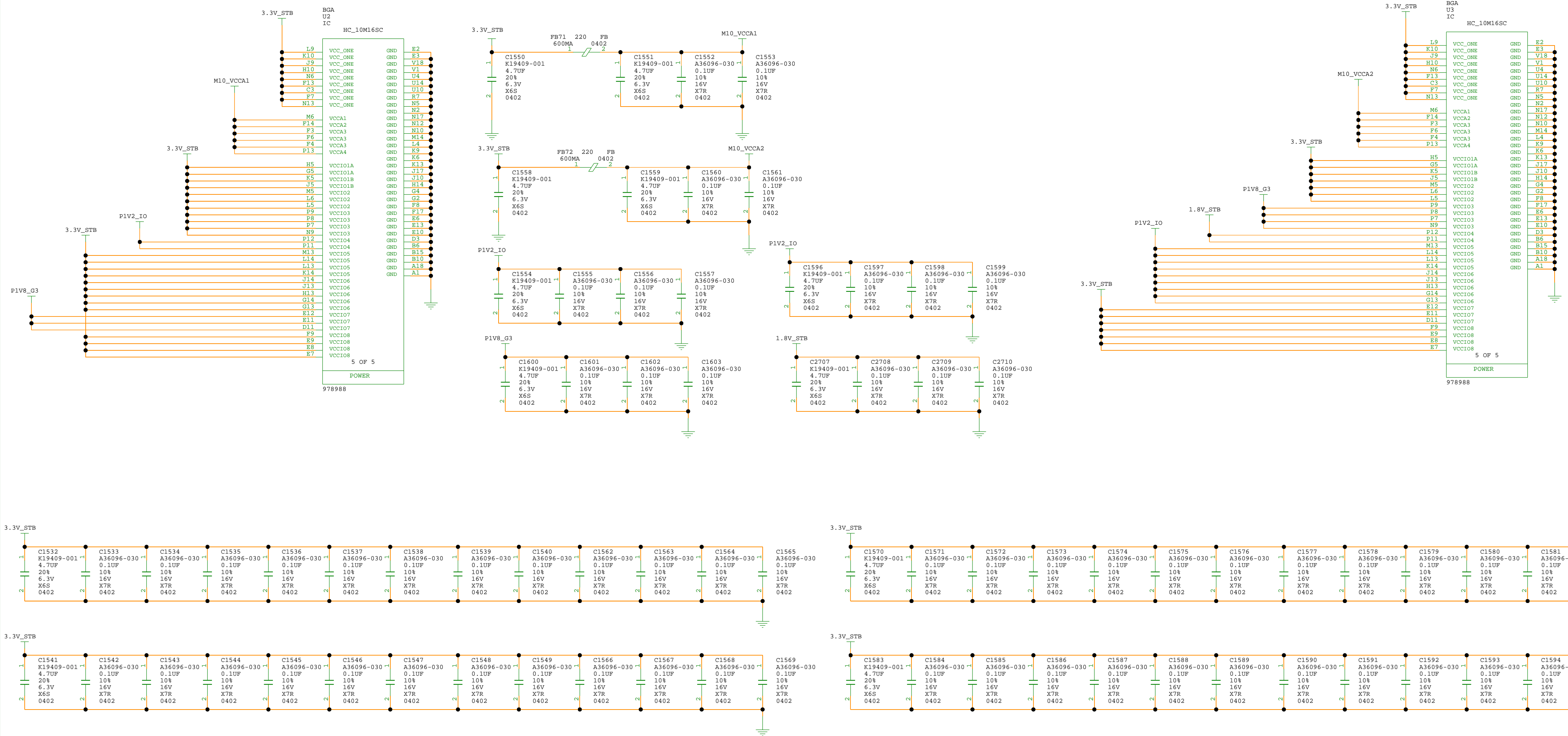







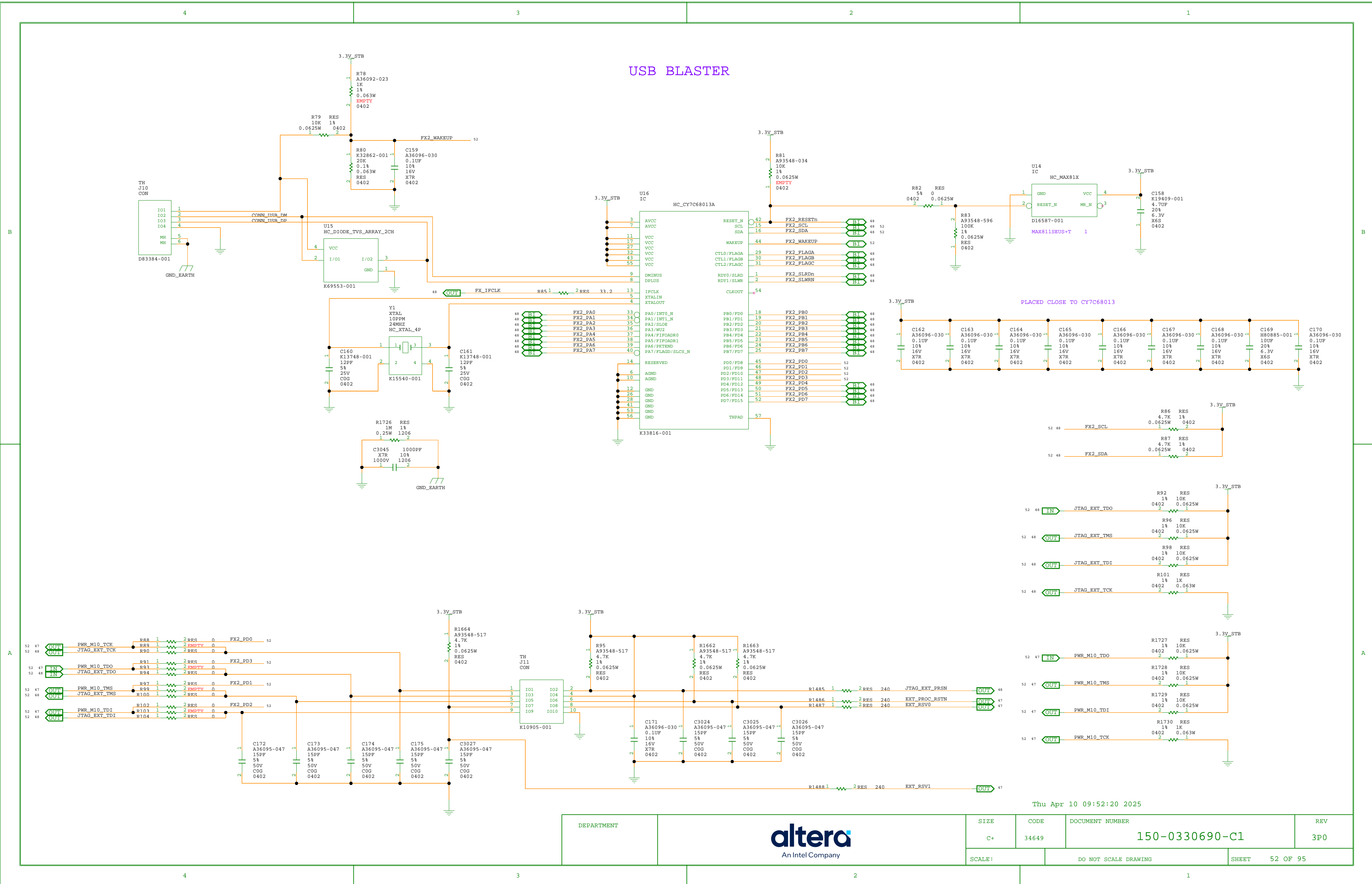


MAX-10 POWER



Thu Apr 10 09:52:11 202

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330690-C1	3P0
		SCALE:	DO NOT SCALE DRAWING		SHEET 51 OF 95



SI5394 CLOCK GENERATOR

X1 156MHZ XO SELECTED IN CASE IF RFCLK NOT PRESENT

**I2C ADDRESS 7-BIT 0X68
SLAVE ADDRESS 7-BIT - 1 1 0 1 0 A1 A0**

**IO_VDD_SEL = 0 (DEFAULT)
CHANGE IO_VDD_SEL = 1 FOR 3.3V OPERATION**

DP [100MHZ, 135MHZ, 150MHZ]

Thu Apr 10 09:52:25 2025

DEPARTMENT	altera An Intel Company	SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330690-C1	REV 3P0
		SCALE:	DO NOT SCALE DRAWING		SHEET 53 OF 95

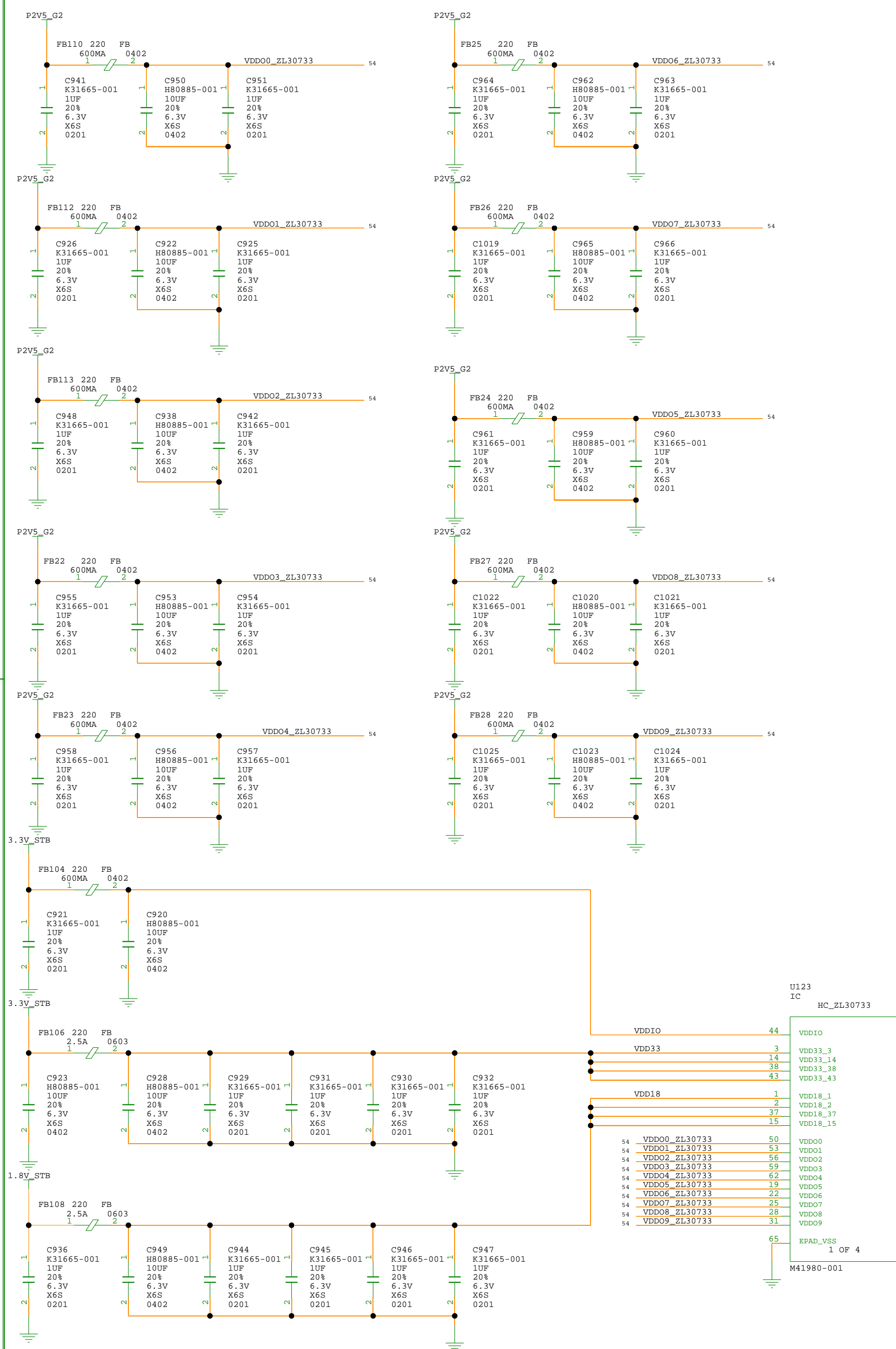
[illegible]

B

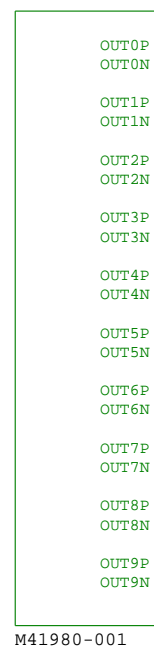
B

A

A

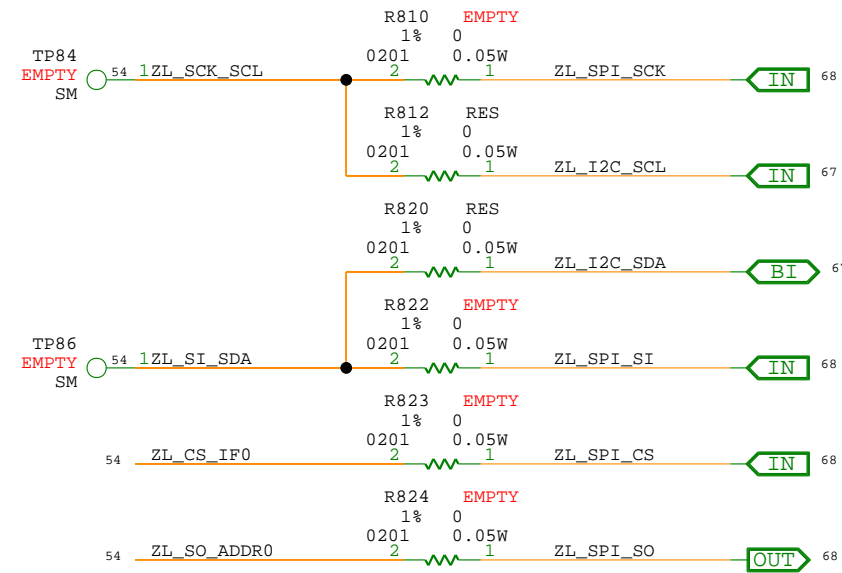
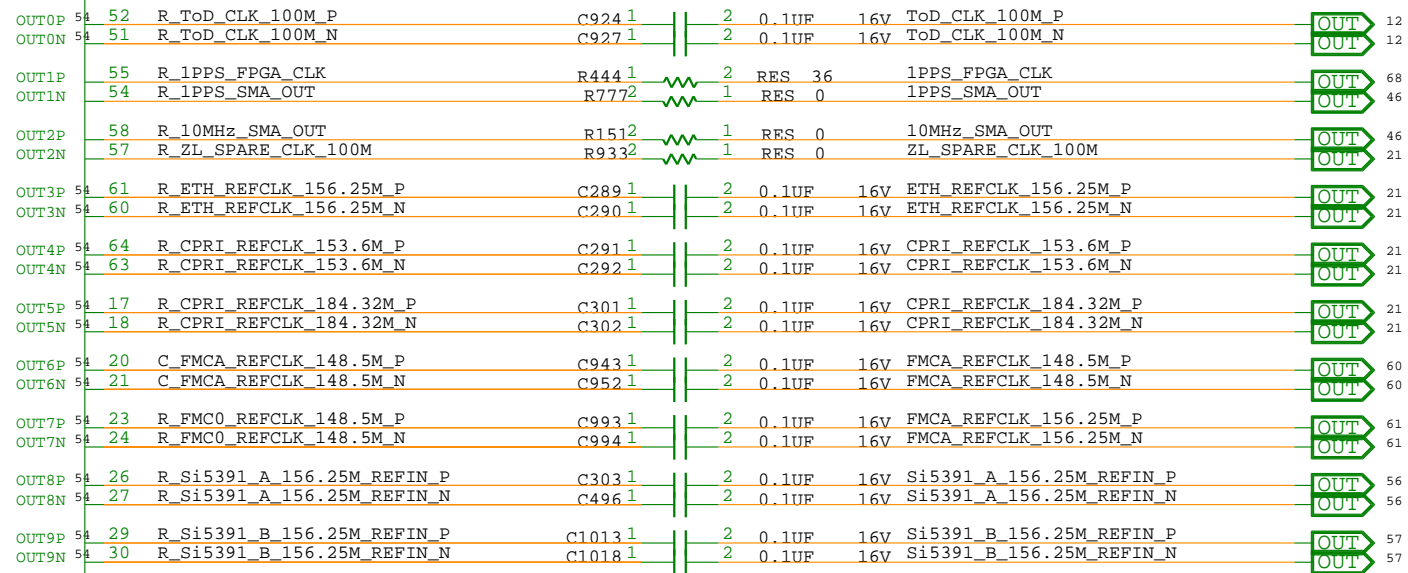


U123
IC
HC_ZL30733



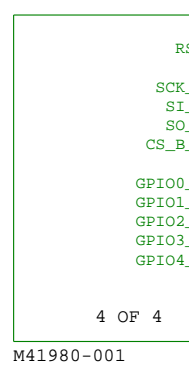
M41980-001

ZL30733 PLL CLOCK GENERATOR-1



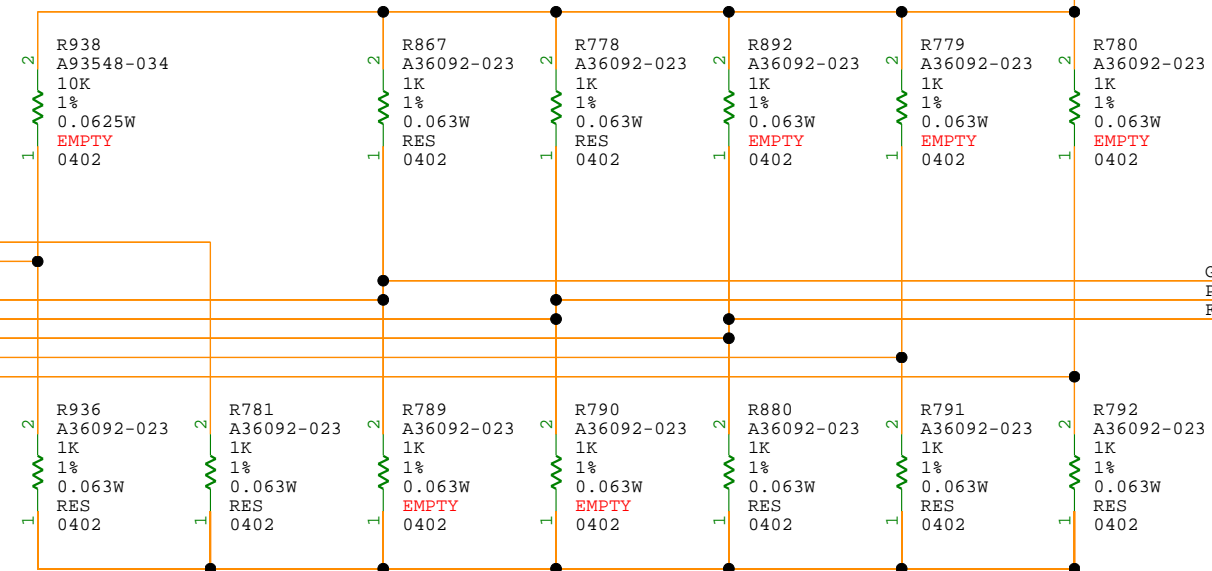
CONNECT TO DEBUG CONNECTOR

U123
IC
HC_ZL30733



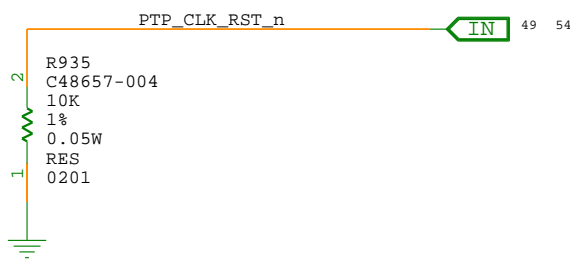
ZL_CS_IF0=0: I2C (DEFAULT)
ZL_CS_IF0=1: SPI

M41980-001

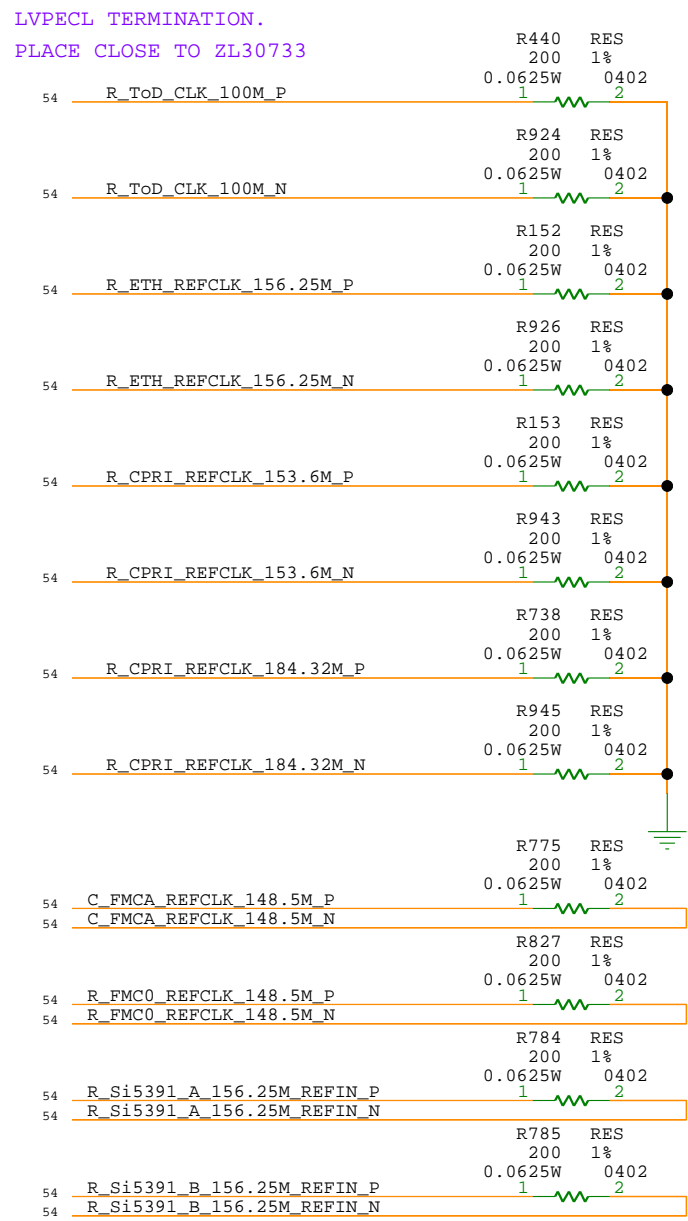


ZL_SO_ADDR0=0: FOR 550MS SETS I2C INTERFACE

I2C ADDRESS = 70H



LVPECL TERMINATION.
PLACE CLOSE TO ZL30733



LVDS TERMINATION.
PLACE CLOSE TO ZL30733

Thu Apr 10 09:52:25 2025

DEPARTMENT

altera
An Intel Company

SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-C1

REV

3P0

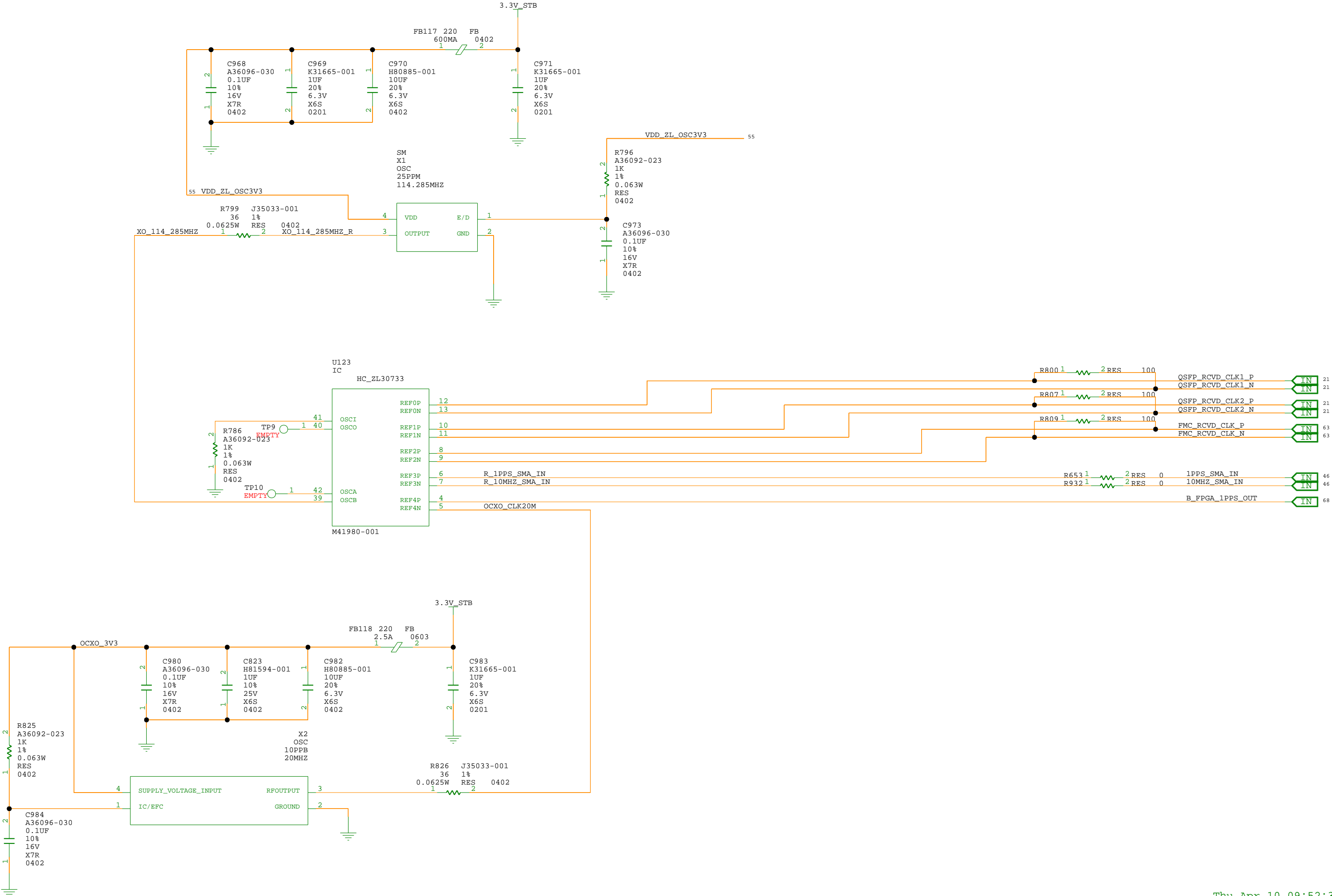
SCALE:

DO NOT SCALE DRAWING

SHEET

54 OF 95

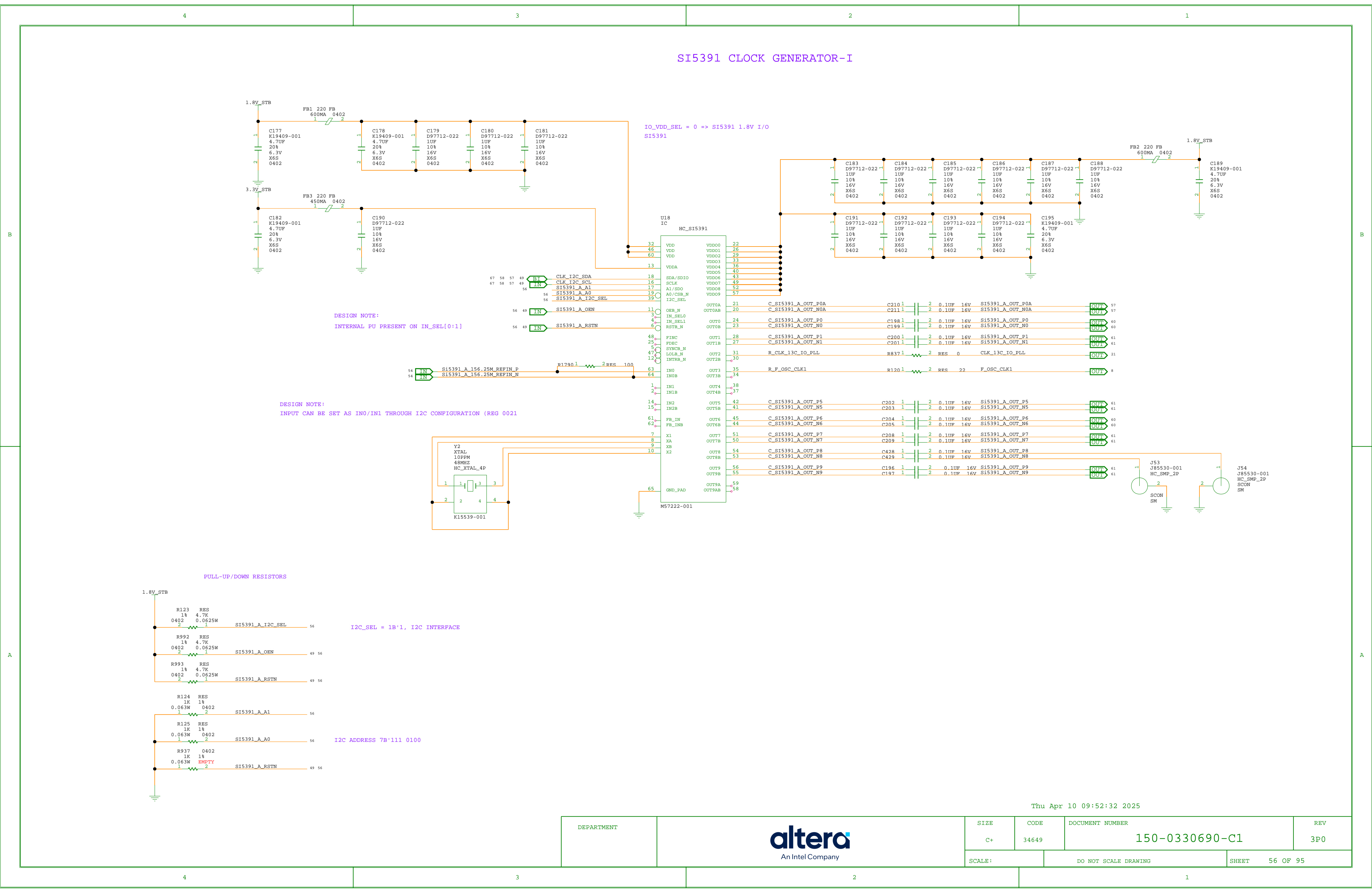
ZL30733 PLL CLOCK GENERATOR-2



Thu Apr 10 09:52:30 2025

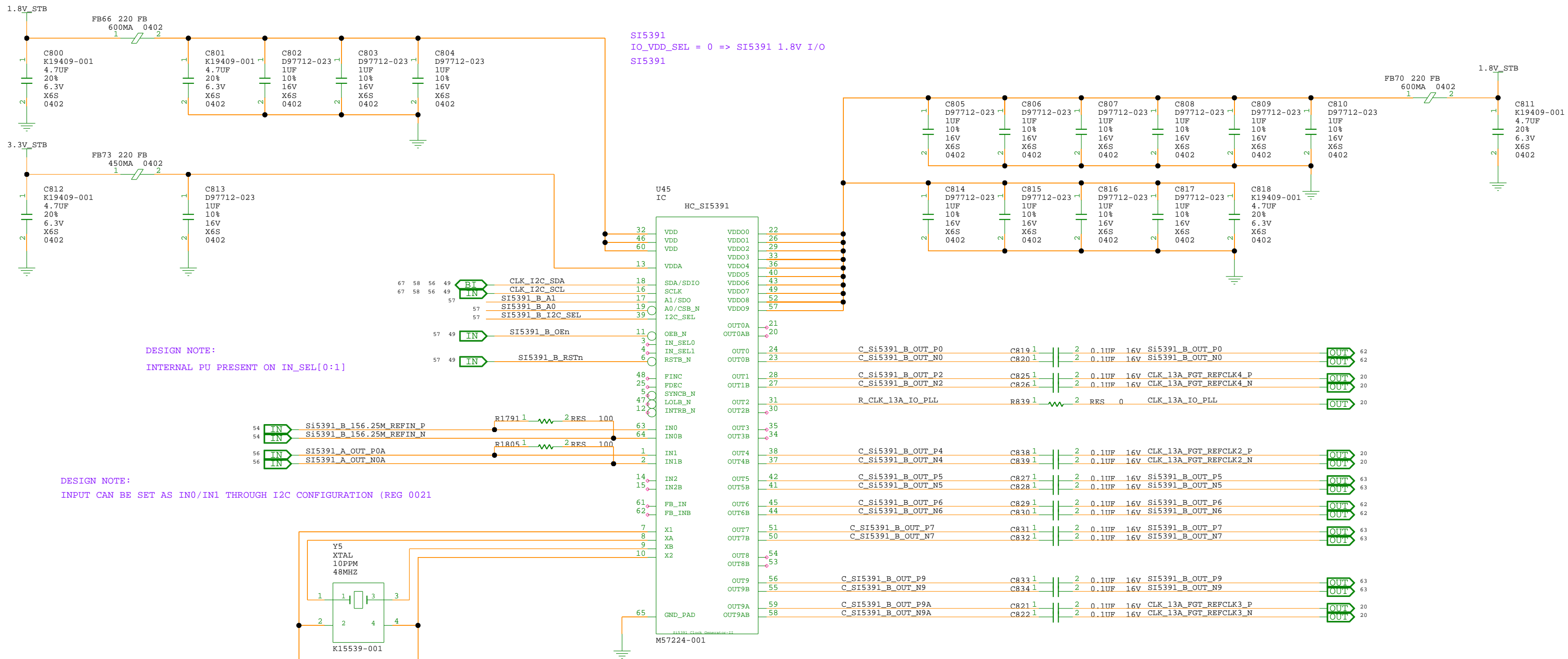
DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330690-C1	3P0
		SCALE:	DO NOT SCALE DRAWING		SHEET 55 OF 95

SI5391 CLOCK GENERATOR-I



Thu Apr 10 09:52:32 2025

SI5391 CLOCK GENERATOR-II

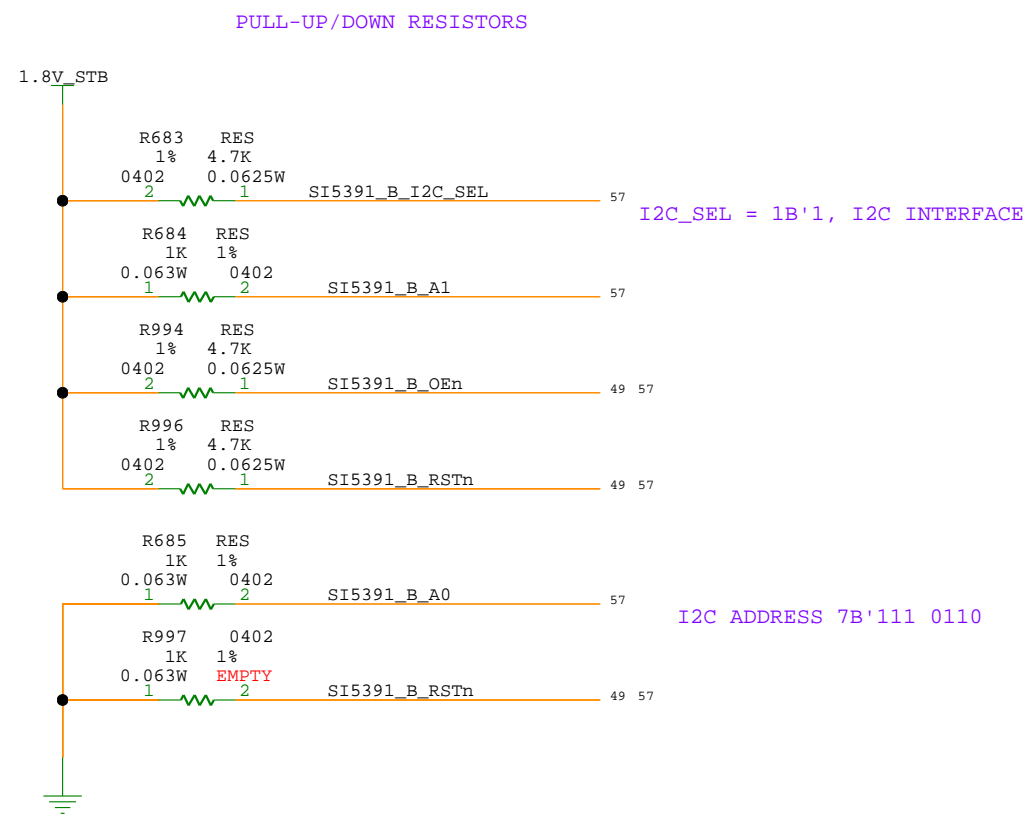


DESIGN NOTE:


INTERNAL PU PRESENT ON IN_SEL[0:1]

DESIGN NOTE

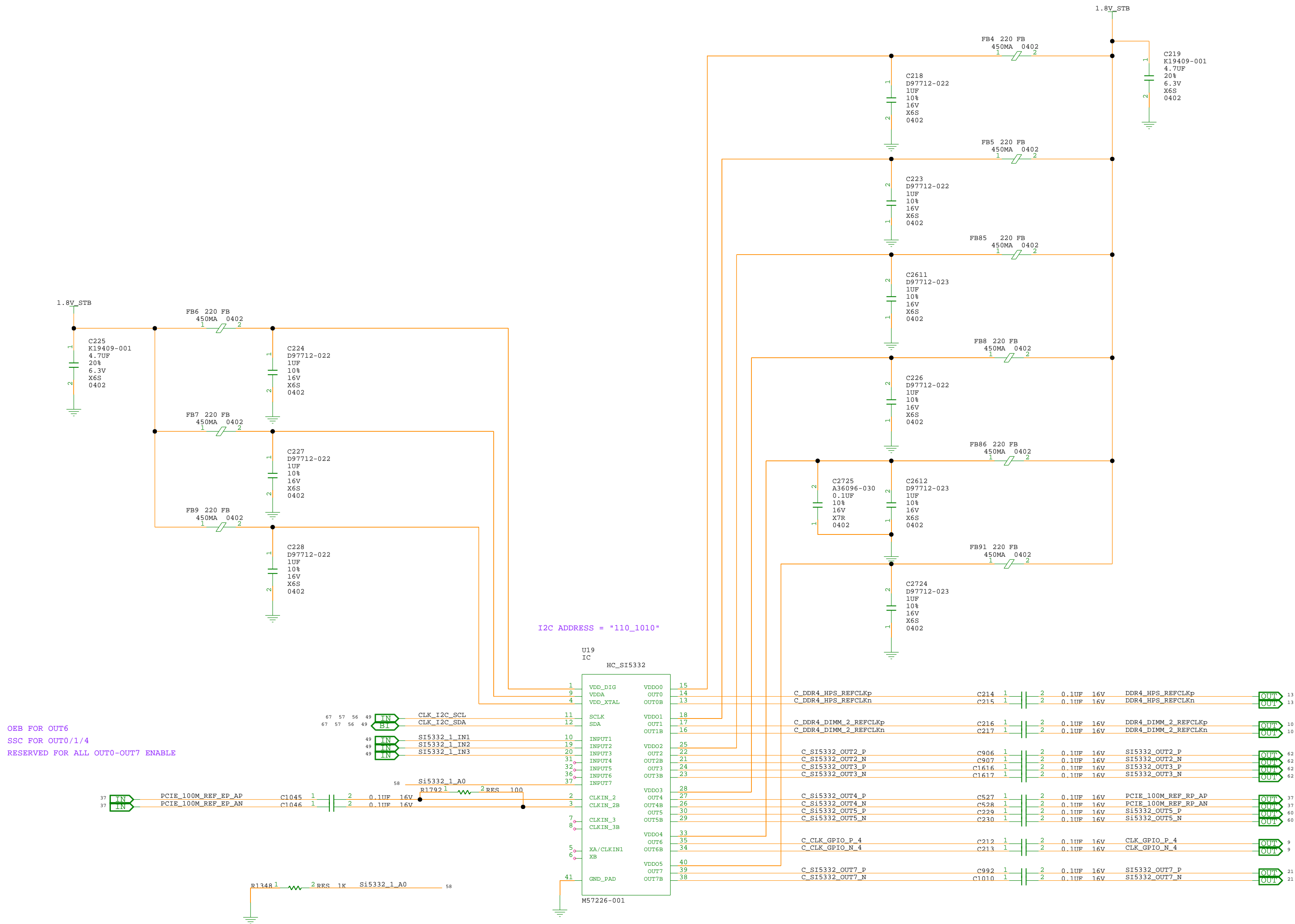
INPUT CAN BE SET AS IN0/IN1 THROUGH I2C CONFIGURATION (REG 0021)



Thu Apr 10 09:52:34 2025


DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330690-C1	3P0
		SCALE:	DO NOT SCALE DRAWING		SHEET 57 OF 95

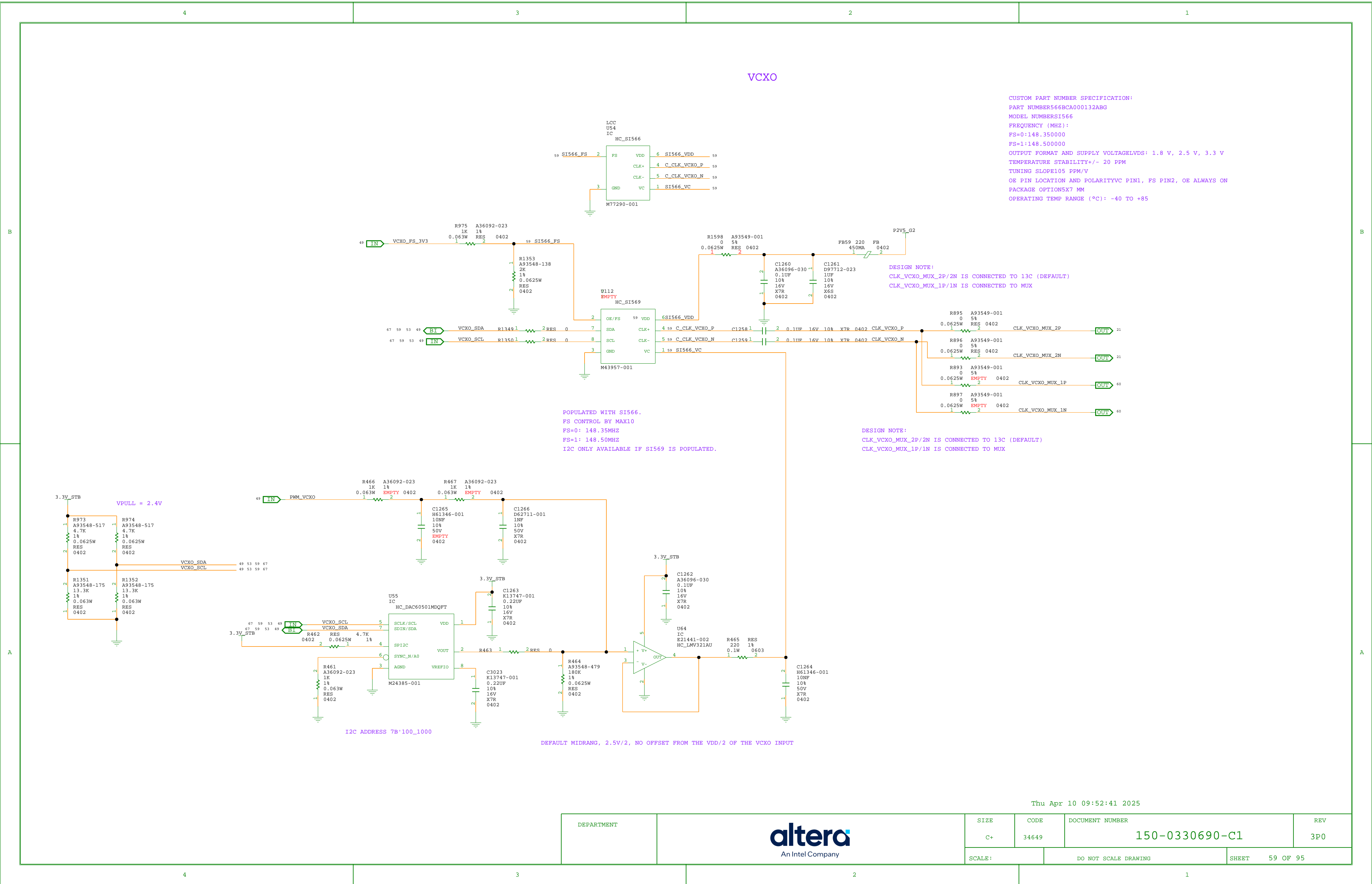
SI5332 CLOCK GENERATOR




OEB FOR OUT6
SSC FOR OUT0/1/4
RESERVED FOR ALL OUT0-OUT7 ENABLE

Thu Apr 10 09:52:36 2025

DEPARTMENT	 An Intel Company	SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330690-C1	REV 3P0
		SCALE:	DO NOT SCALE DRAWING		SHEET 58 OF 95





DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330690-C1	3P0
		SCALE:	DO NOT SCALE DRAWING		SHEET 60 OF 95

CLOCK MUX-II

156.25M

368.63M

184.32M

156.25

CAD NOTE:
PLACE AS TRI-PAD RESISTOR, TO AVOID ANY STUB

CAD NOTE:
PLACE AS TRI-PAD WITH AC_CAP TO AVOID ANY STUB

Thu Apr 10 09:52:46 2025

DEPARTMENT



SIZE
C+

CODE
34649

DOCUMENT NUMBER

150-0330690-C1

REV

3P0

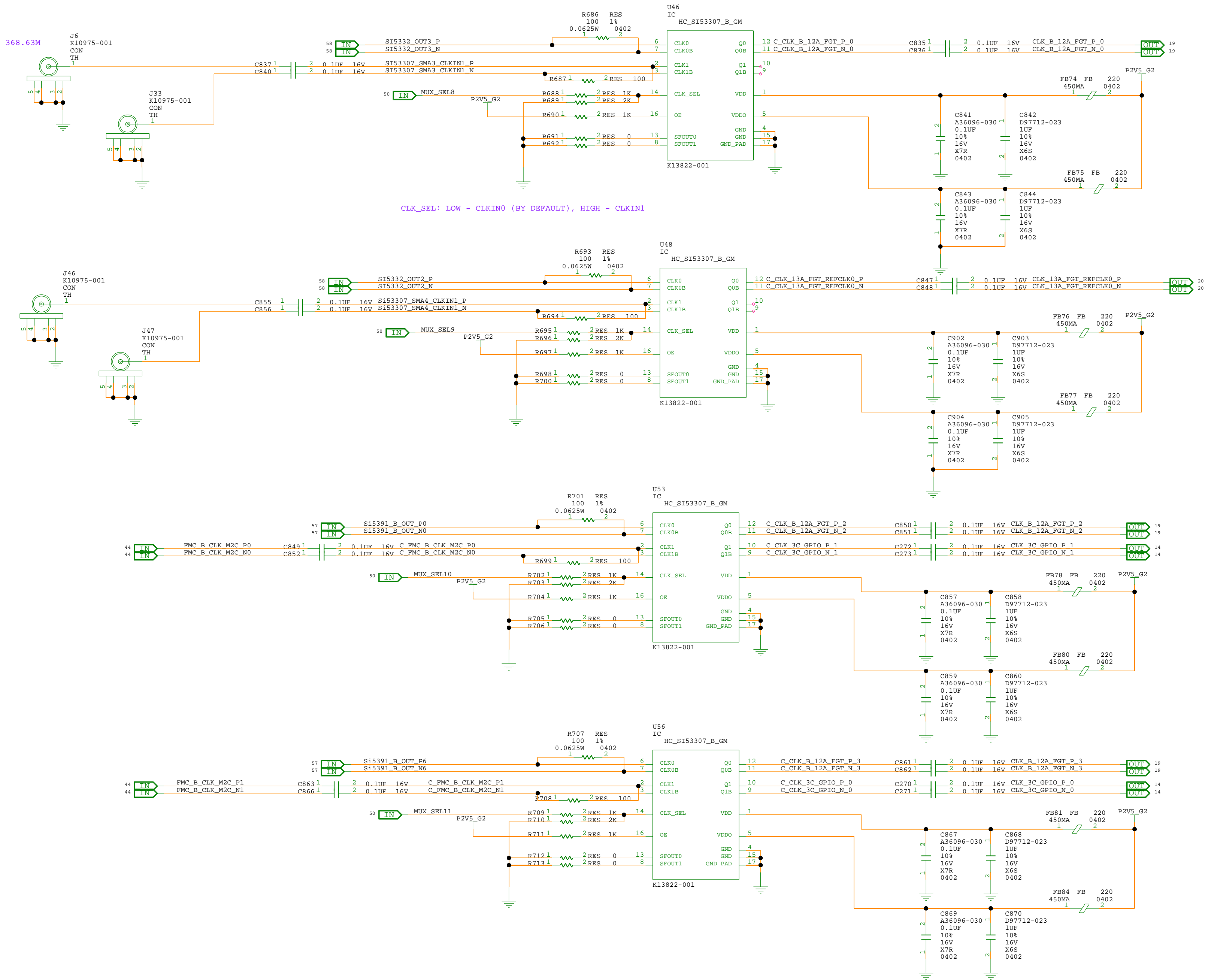
SCALE:

DO NOT SCALE DRAWING

SHEET

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CLOCK MUX-III



Thu Apr 10 09:52:48 2025

DEPARTMENT



SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-C1

REV

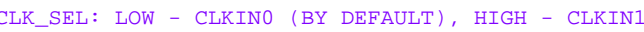
3P0

SCALE:

DO NOT SCALE DRAWING

SHEET

62 OF 95



DEPARTMENT



SIZE

CODE

DOCUMENT NUMBER

REV

150-0330690-C1

SCALE =

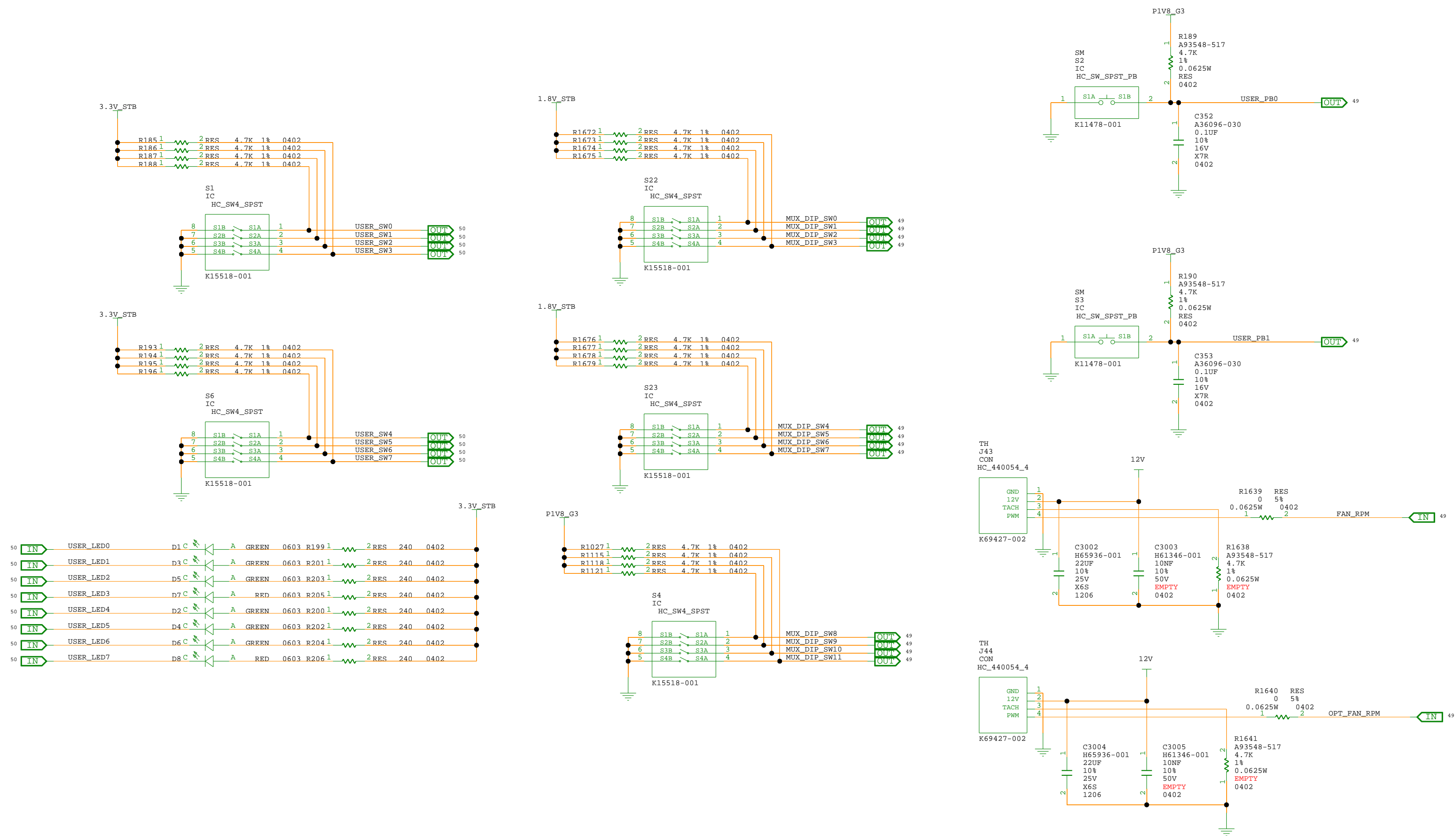
DO NOT SCALE DRAWING

SHEET

53 OF 95

4		3		2		1	
B							
A							

DIP SWITCH, LEDS



Thu Apr 10 09:52:58 2025

DEPARTMENT

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An Intel Company

SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-C1

REV

3P0

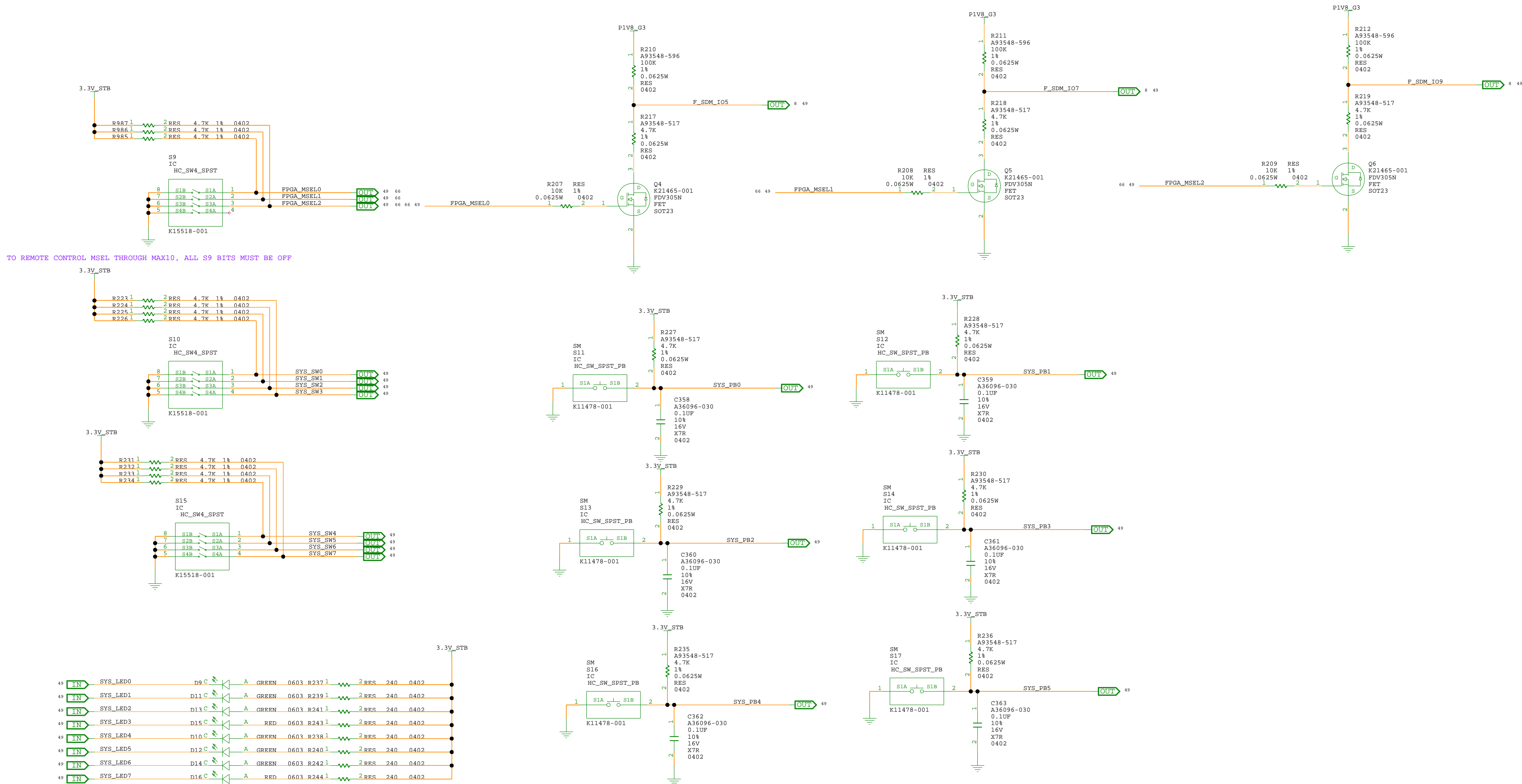
SCALE:

DO NOT SCALE DRAWING

SHEET

65 OF 95

DIP SWITCH, LEDS



TO REMOTE CONTROL MSEL THROUGH MAX10, ALL S9 BITS MUST BE OFF

Thu Apr 10 09:53:02 2025

DEPARTMENT



SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-C1

REV

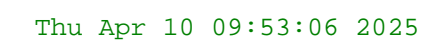
3P0

SCALE:

DO NOT SCALE DRAWING

SHEET

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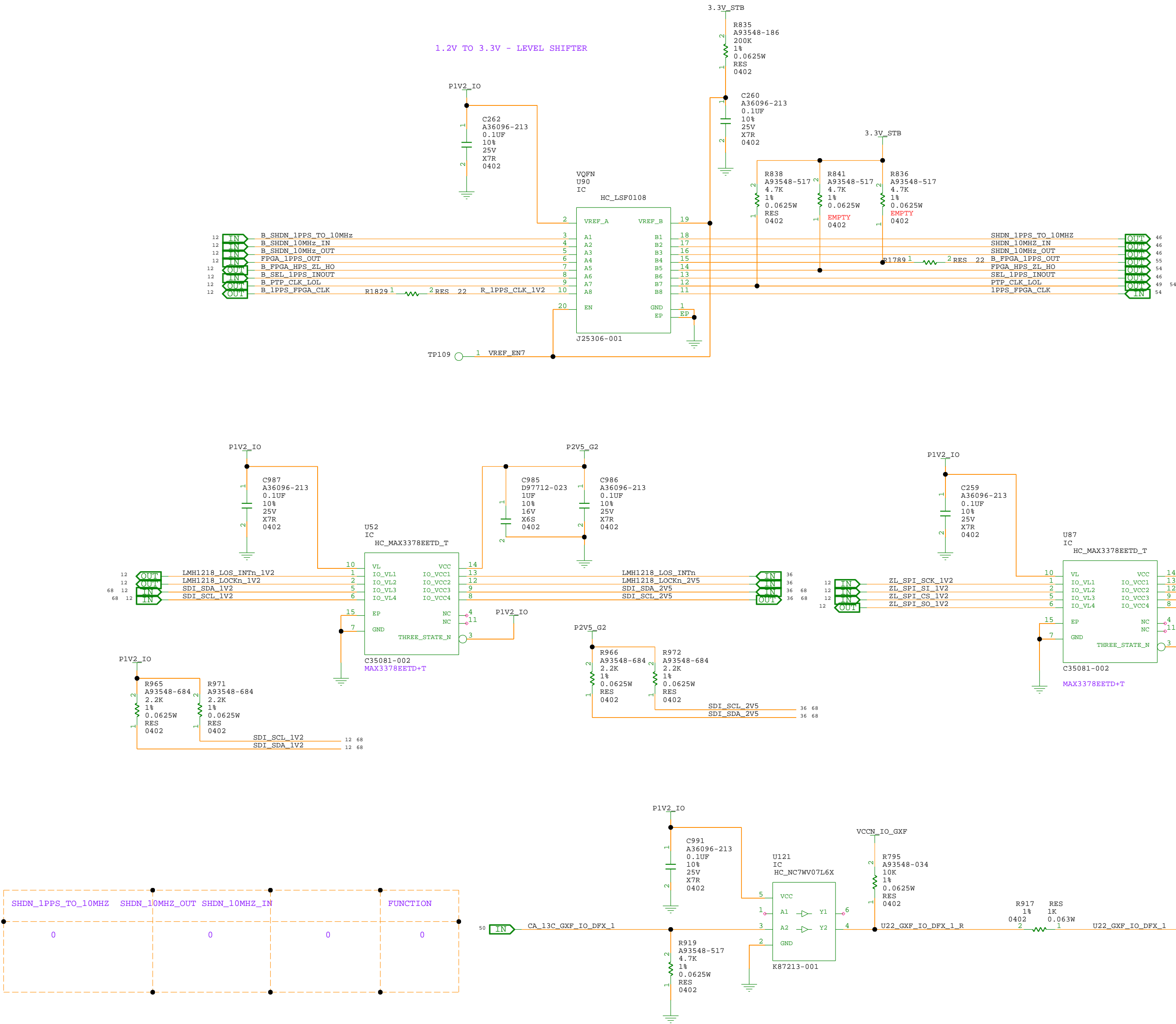
B

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LVL SHIFTER-II



Thu Apr 10 09:53:08 2025

4				3				2				1			
RESERVED															
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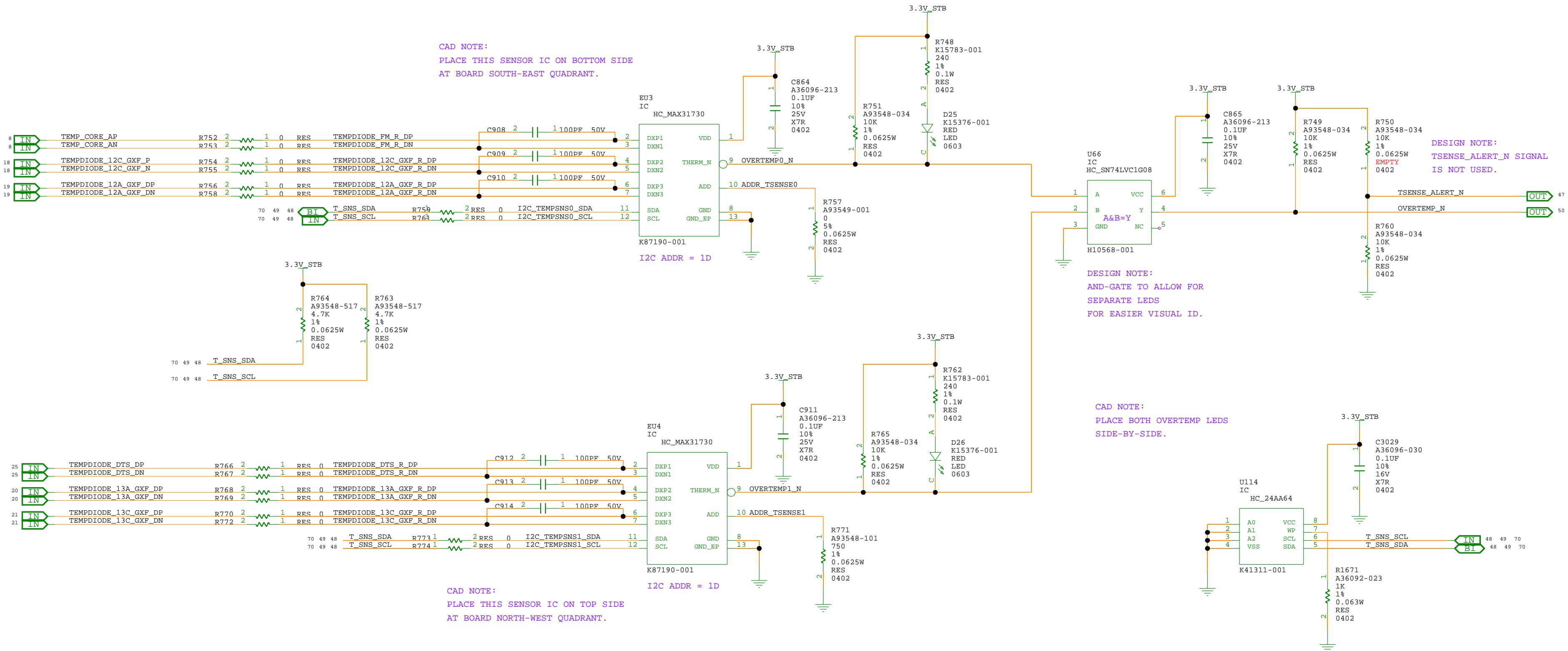
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Thu Feb 27 11:01:57 2025

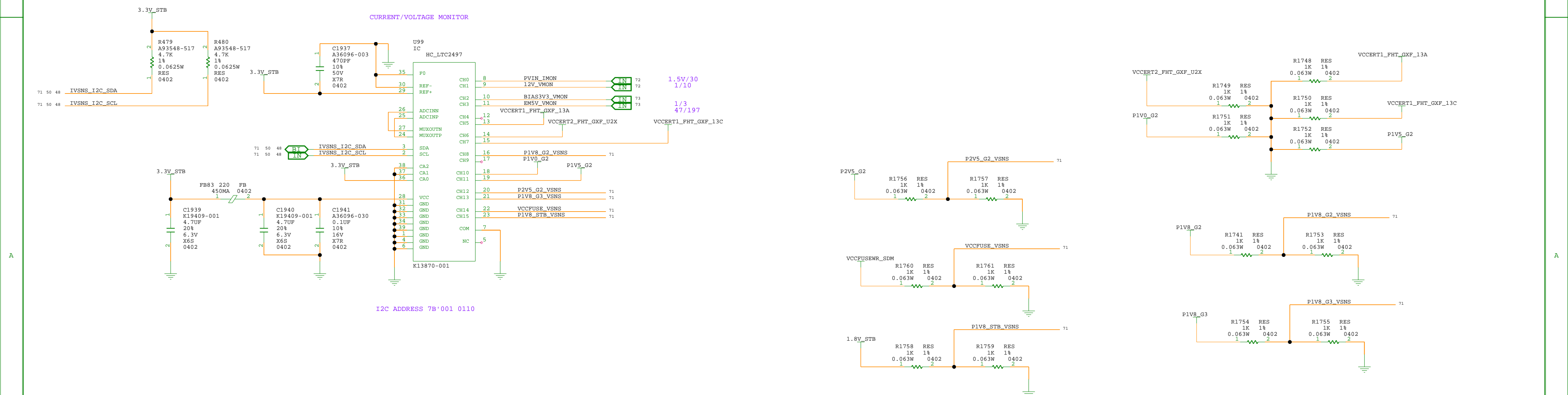
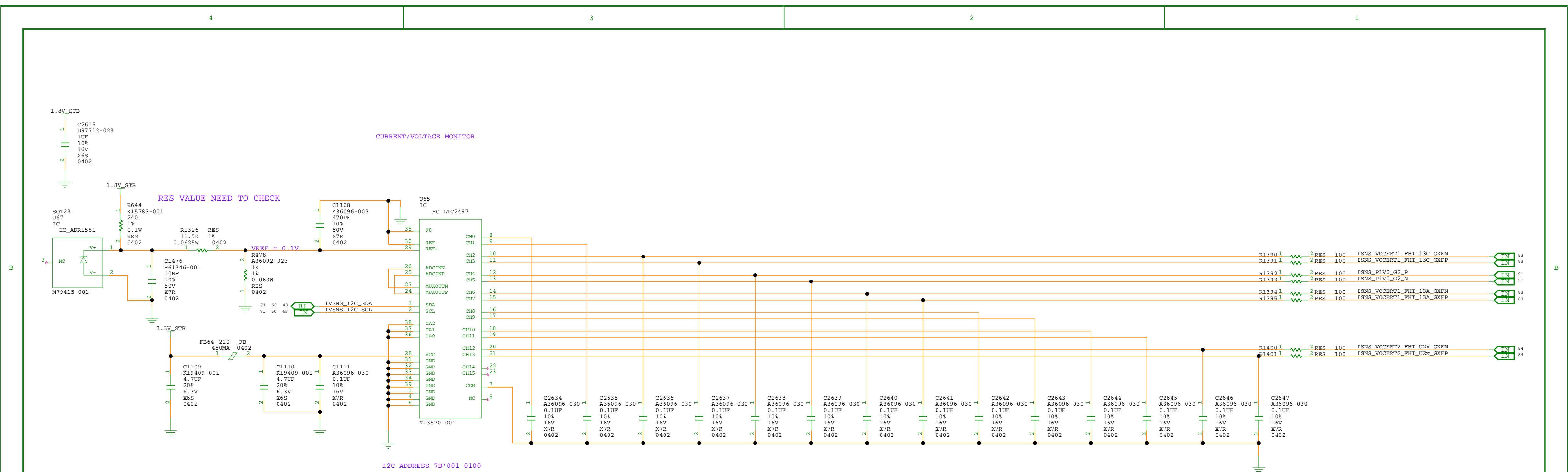
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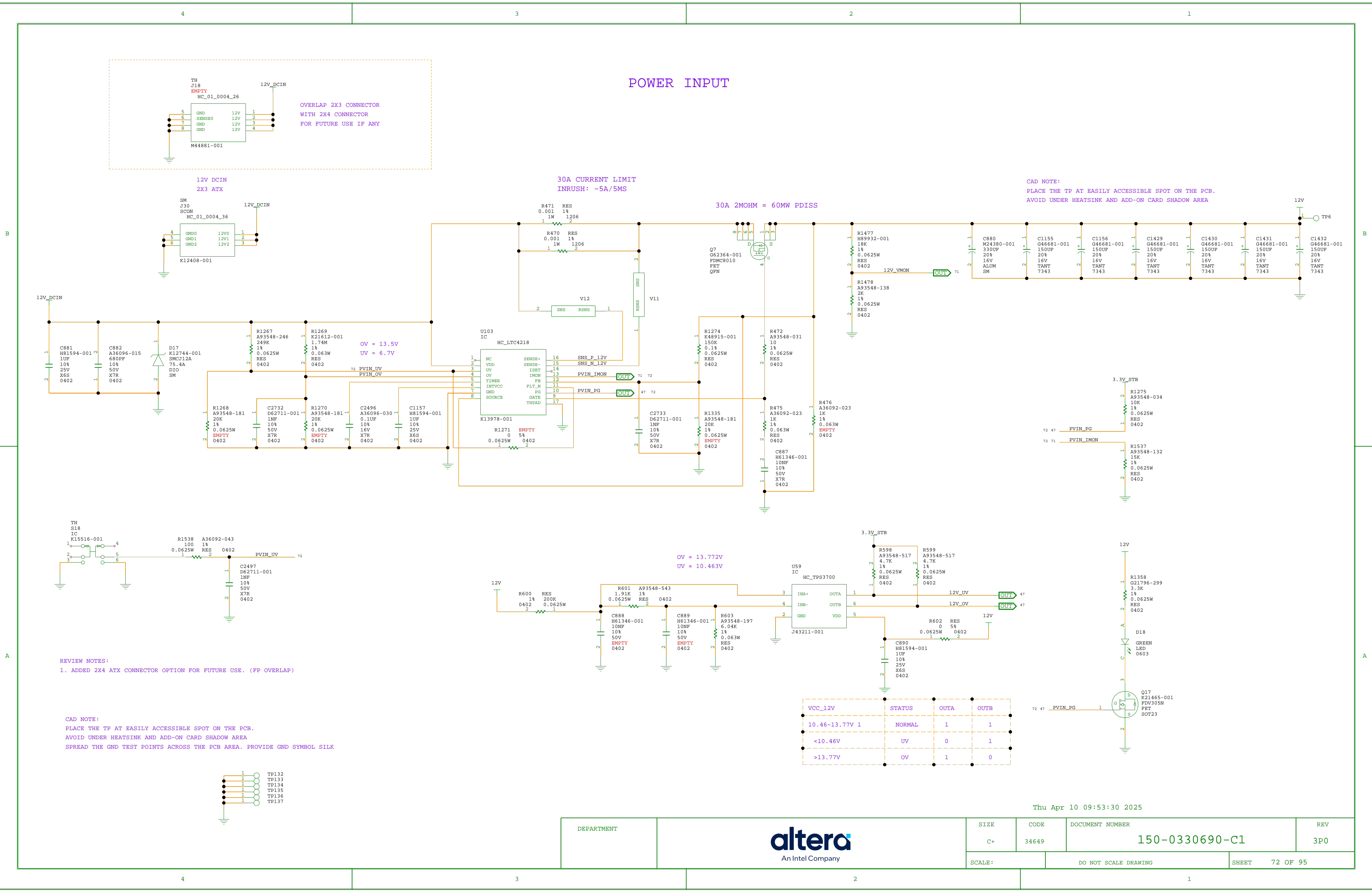
BOARD TEMP SENSORS



Thu Apr 10 09:53:15 2025

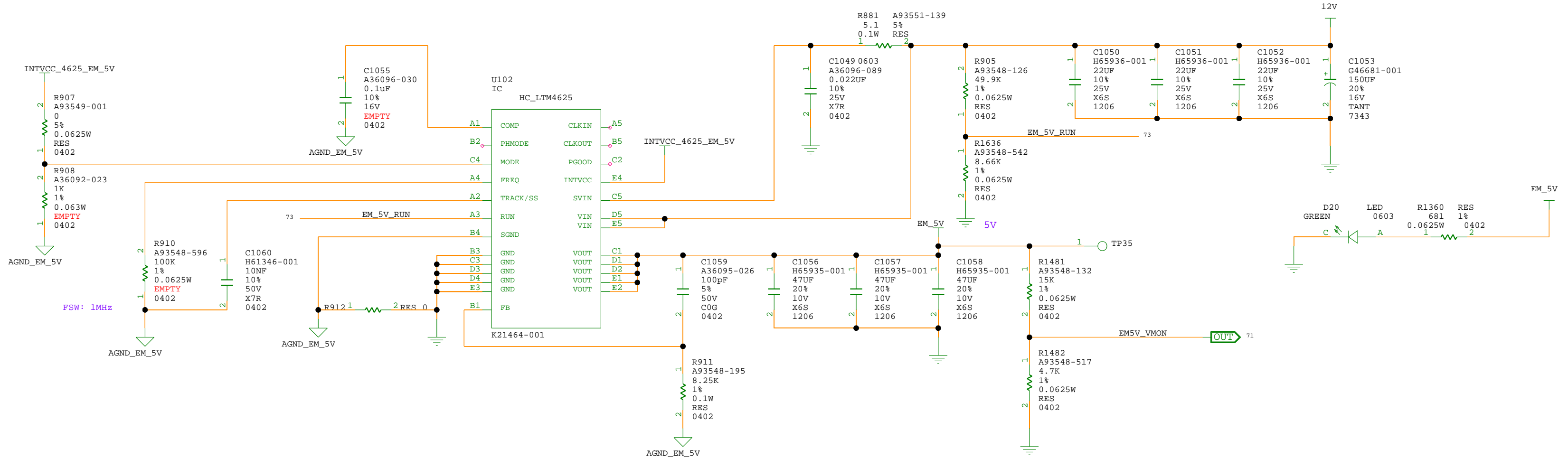
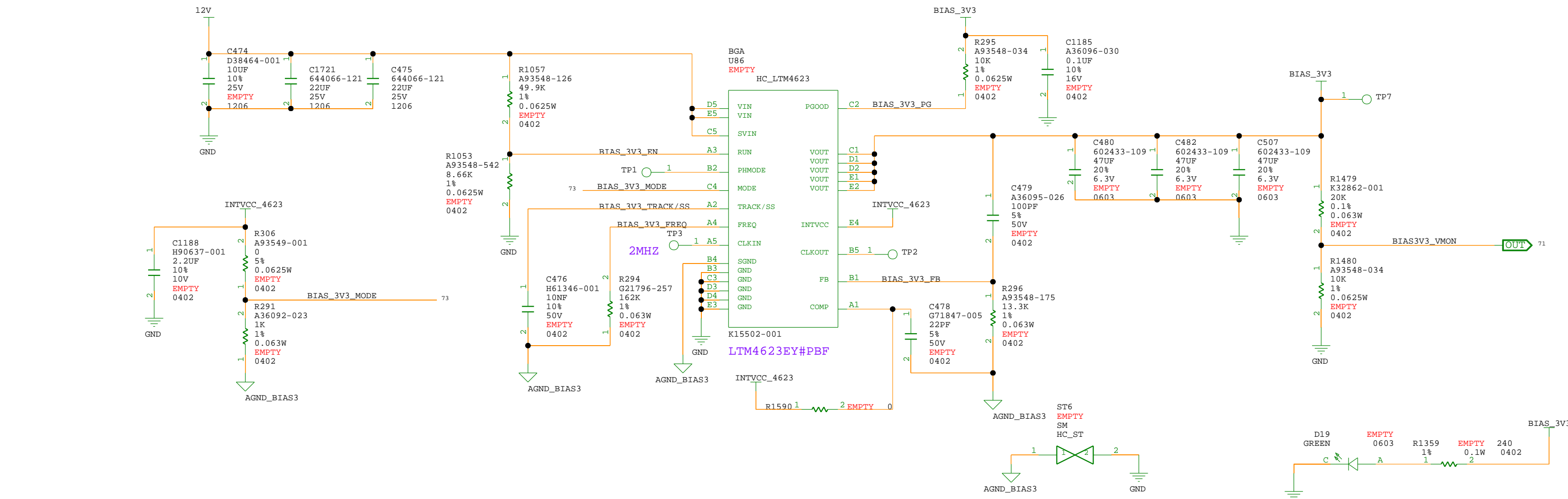
DEPARTMENT	 An Intel Company	SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330690-C1	REV 3P0
SCALE:		DO NOT SCALE DRAWING		SHEET 70 OF 95	





POWER BIAS


CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA



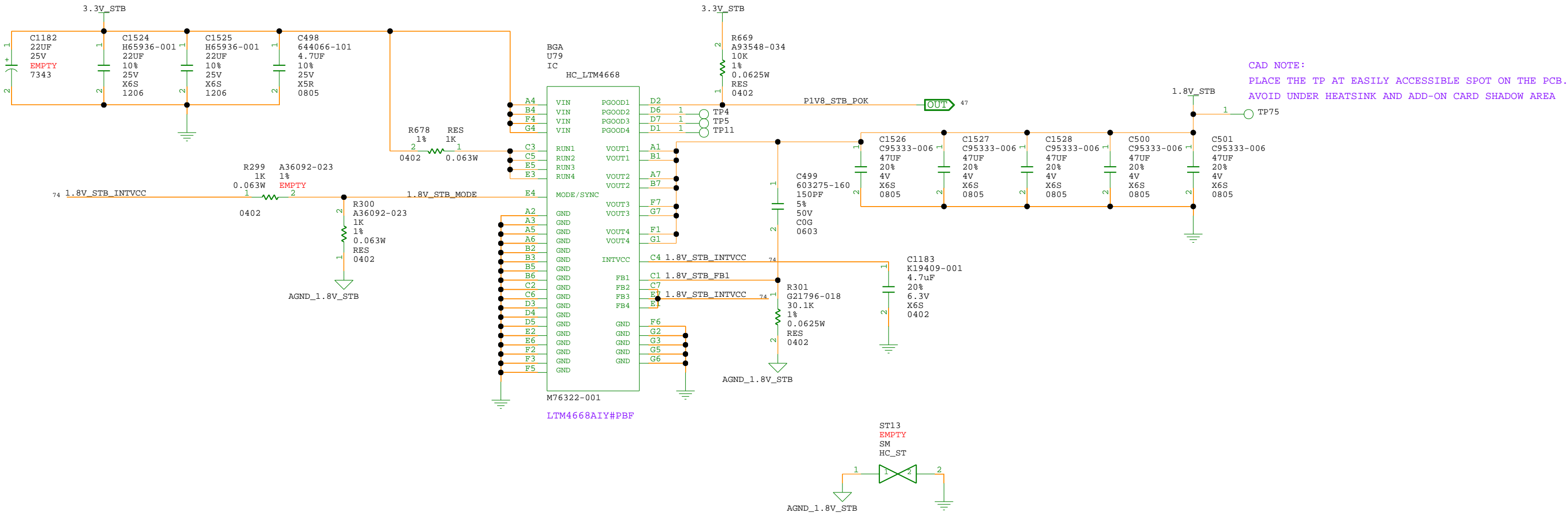
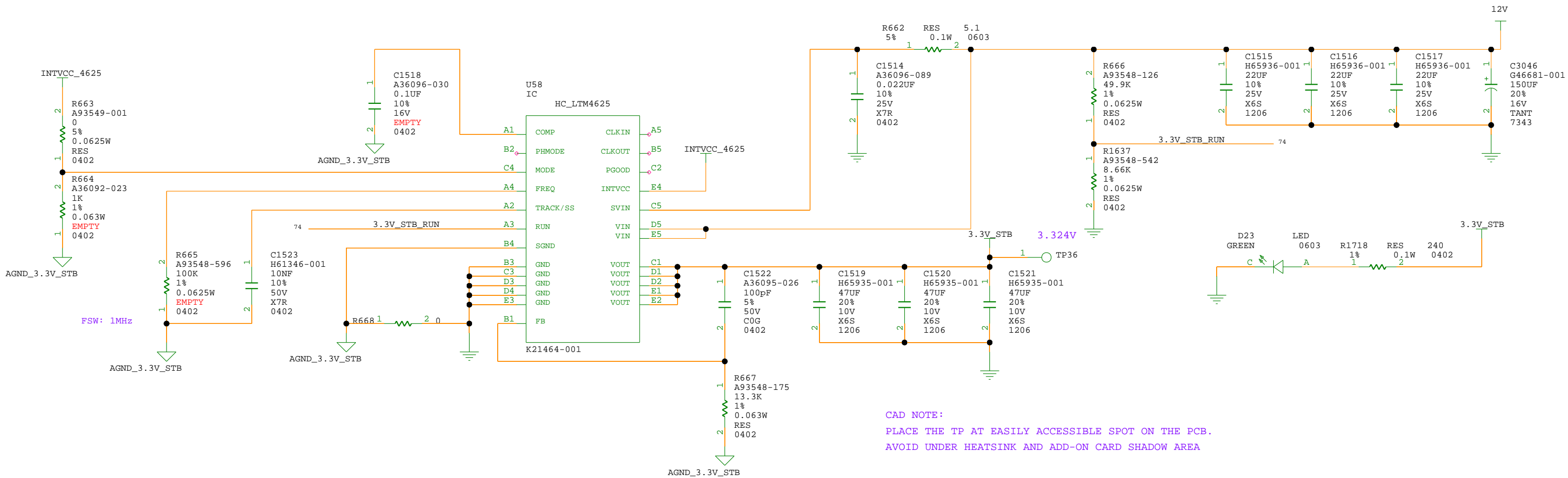
CAD NOTE:

PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

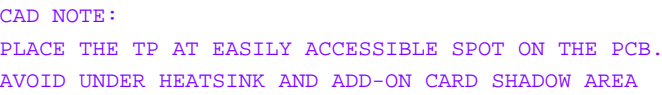
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DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330690-C1	3P0
		SCALE:	DO NOT SCALE DRAWING		SHEET 73 OF 95

3.3V_STB & 1.8V_STB



Thu Apr 10 09:53:41 2025



CAD NOTE: PLEASE THIS BULK CAP

PLACEHOLDER

P1V2_BUS_VOUTCFG
P1V2_BUS_VTRIMCFG

P1V2_BUS_INTVCC TP32 EMPTY SM

565 1 2 EMPTY 6.34K

76

P1V2_BUS_SNUB0

P1V2_BUS_POK  47 70

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2. BIIS

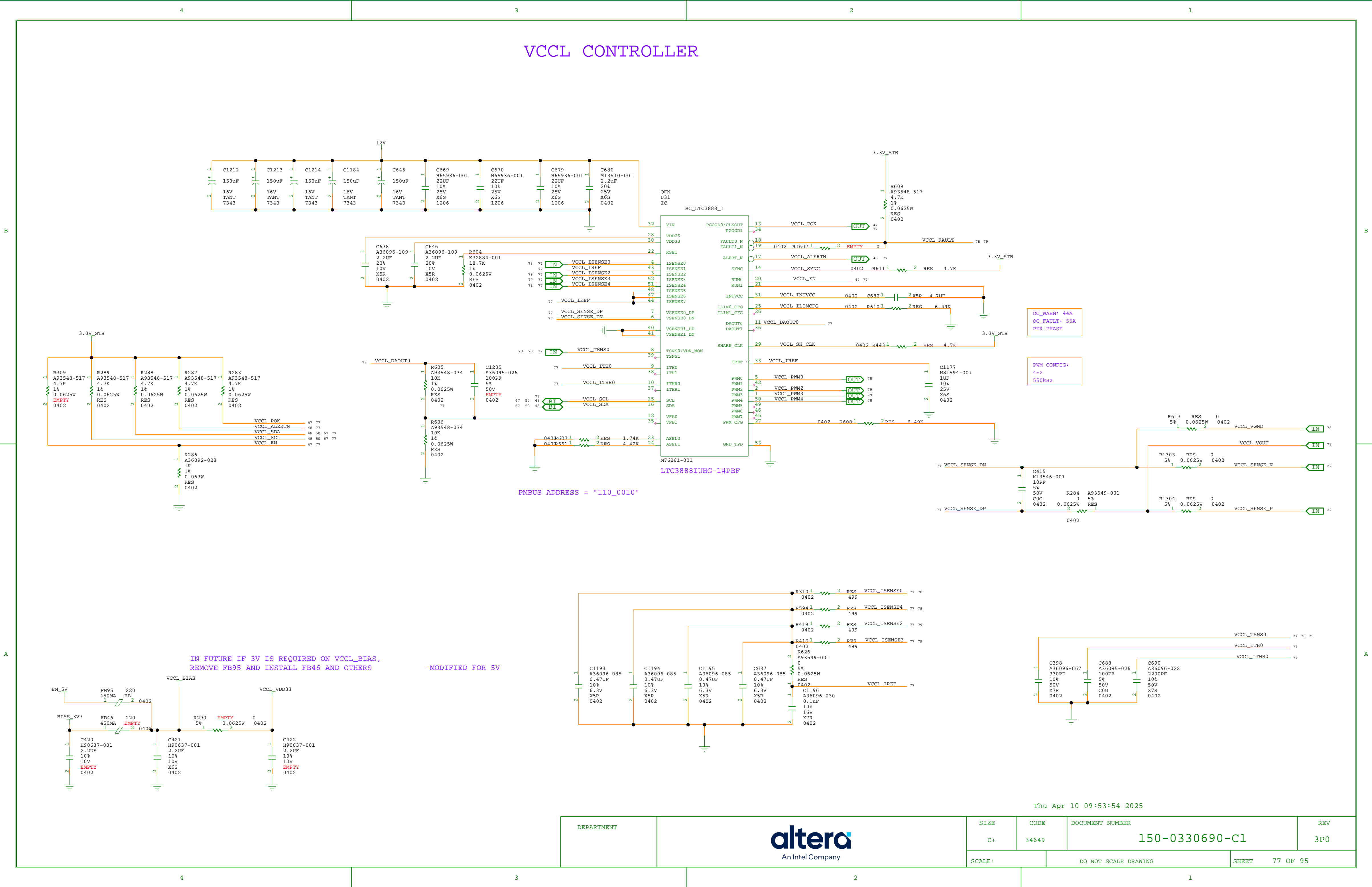
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Am. Inst. of Certified Financial Planners

Thu Apr 10 09:53:47 2025

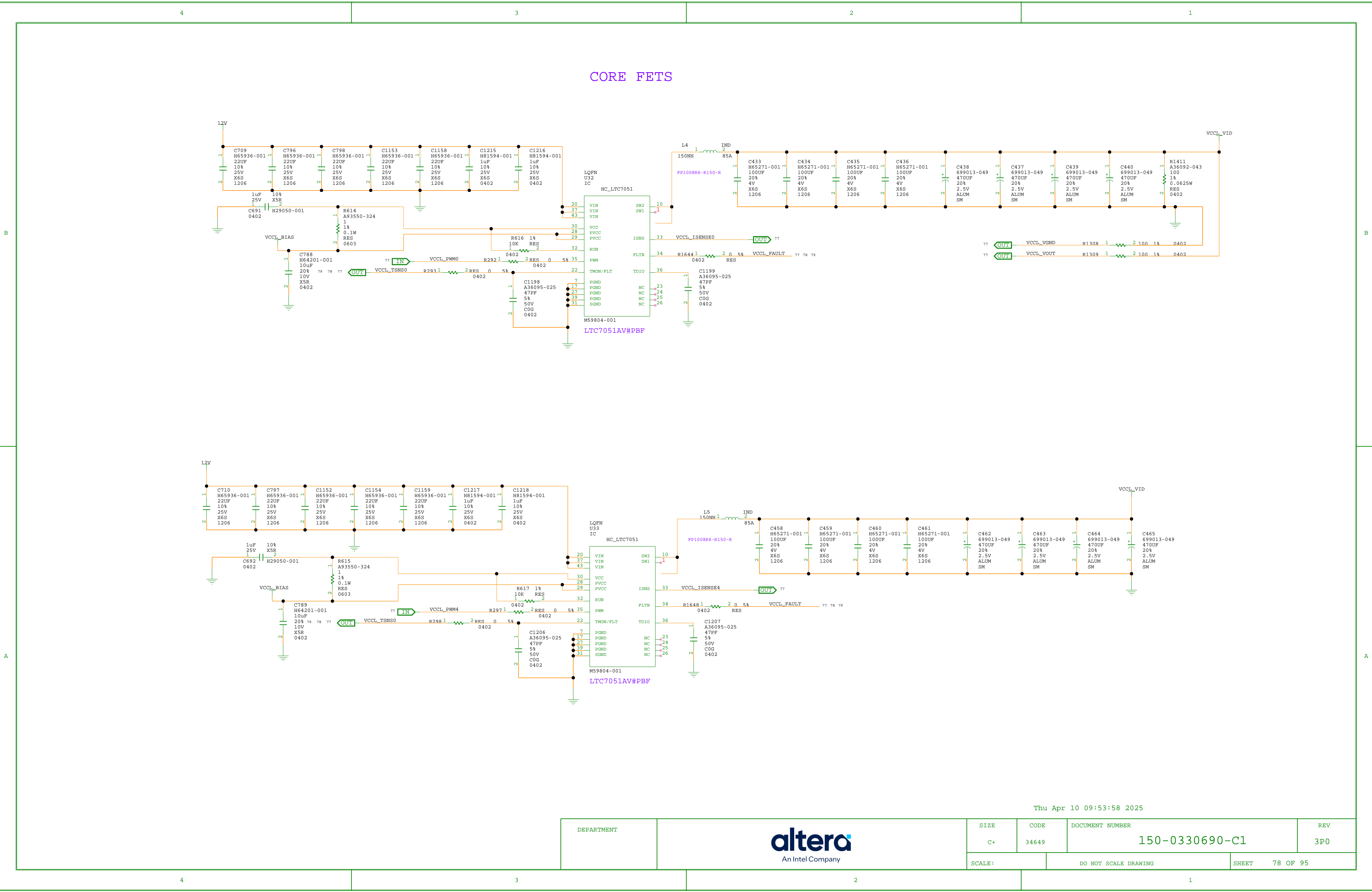
SCALE:	DO NOT SCALE DRAWING	SHEET	76 OF 95
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VCCL CONTROLLER

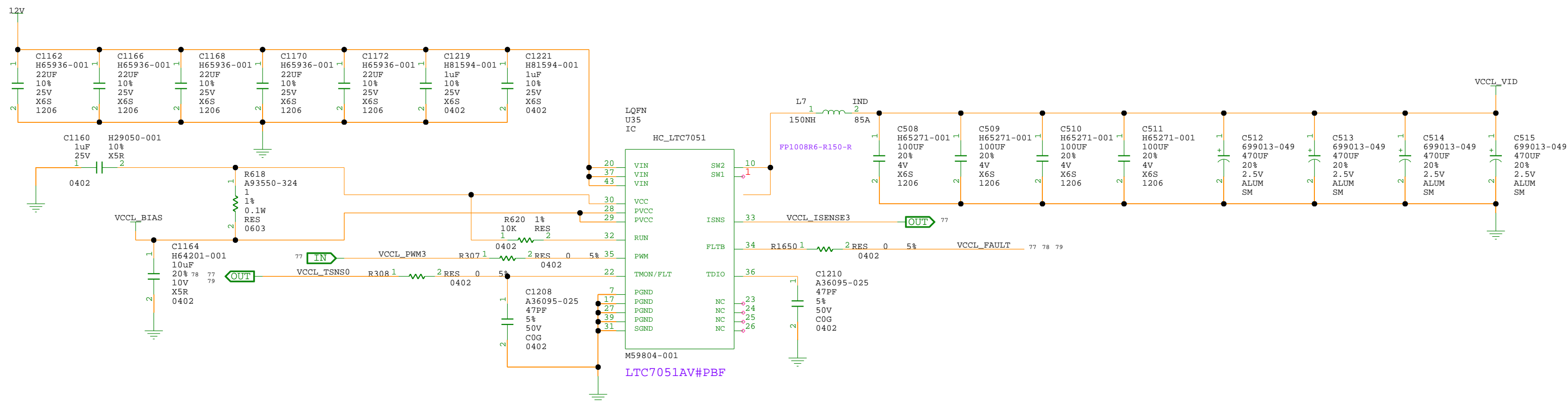
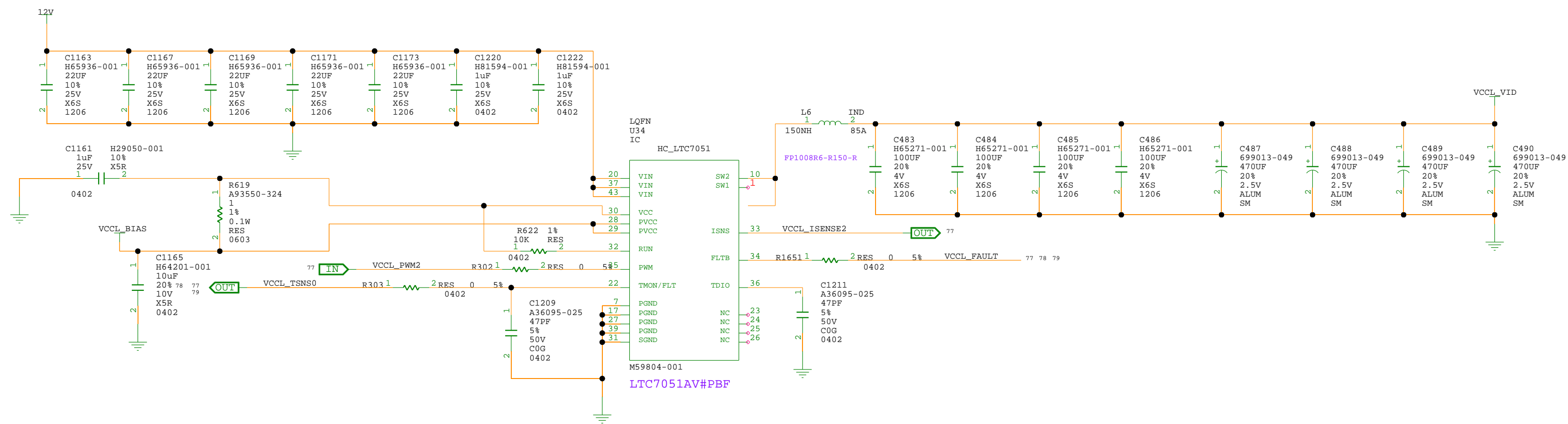


Thu Apr 10 09:53:54 2025


DEPARTMENT	SIZE	CODE	DOCUMENT NUMBER	REV
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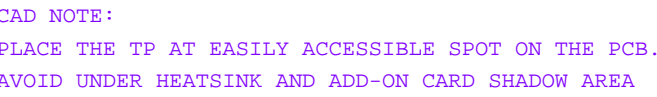


CORE FETS



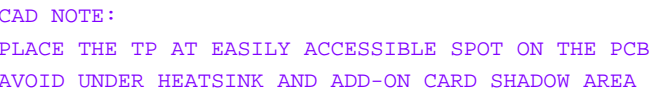
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DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
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		SCALE:	DO NOT SCALE DRAWING		SHEET 79 OF 95



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SIZE	CODE	DOCUMENT NUMBER	REV
C+	34649	150-0330690-C1	3P0
SCALE:	DO NOT SCALE DRAWING		SHEET 80 OF 95




PLACED UNDER FPGA

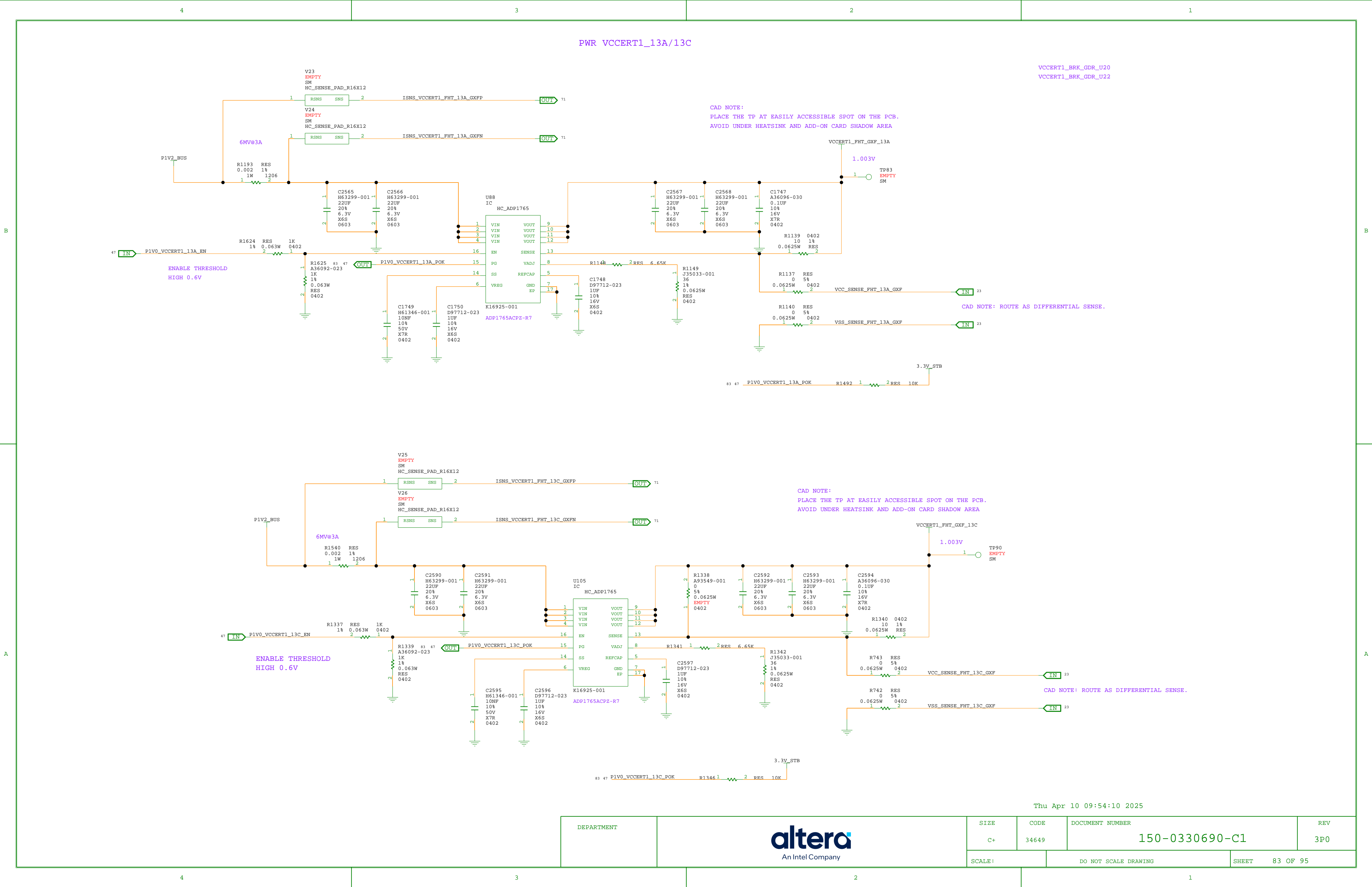
```
MAX CURRENT = 36A(SINGLE)
LOAD CURRENT = 29.2A
VO = 0.8V
SWITCHING FREQ= 500 KHZ
RIPPLE = 10MV
```

CAD NOTE:CONNECT NEAR FPGA BGA REGION. NEED TO ROUTE AS KELVIN SENSE

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An Intel Company

Thu Apr 10 09:54:07 2025

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
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		SCALE:	DO NOT SCALE DRAWING		SHEET 82 OF 95



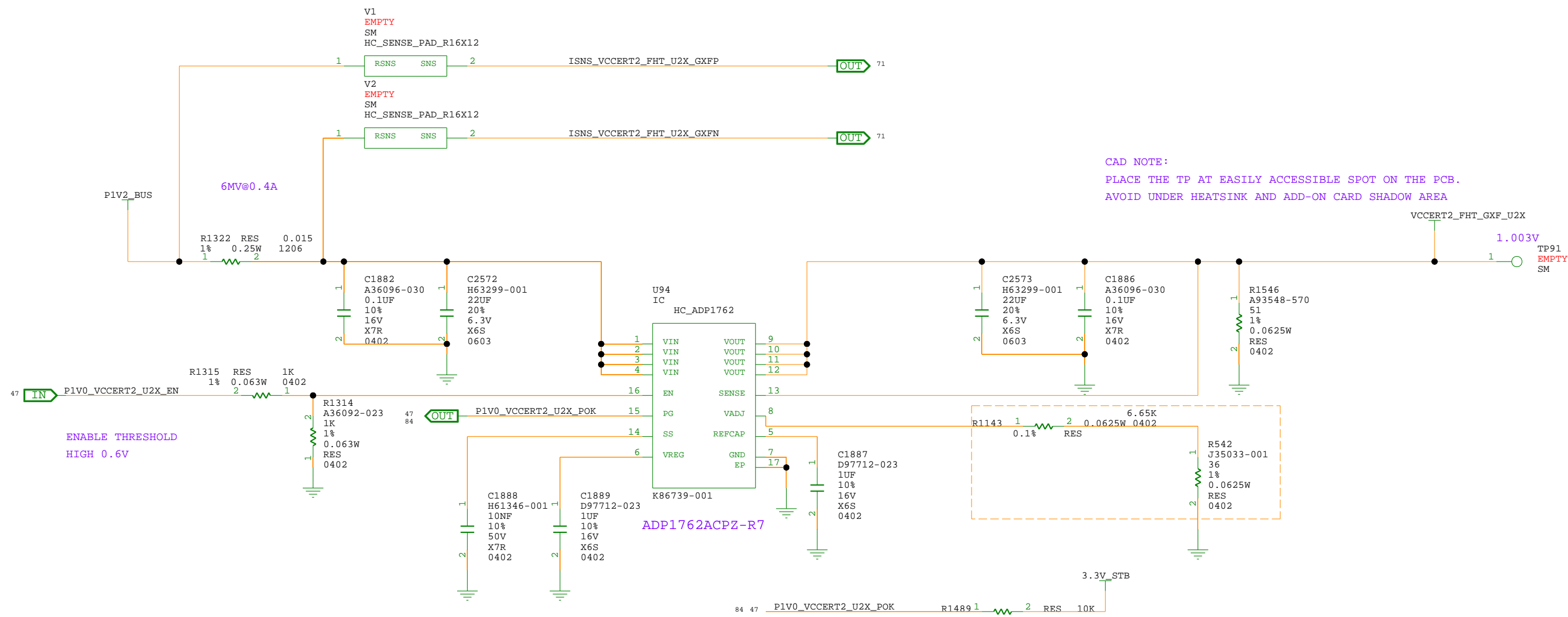
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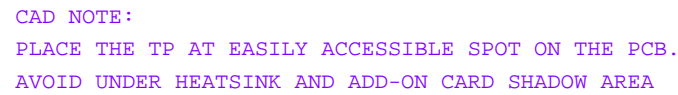
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PWR_VCCERT2_U20/U22

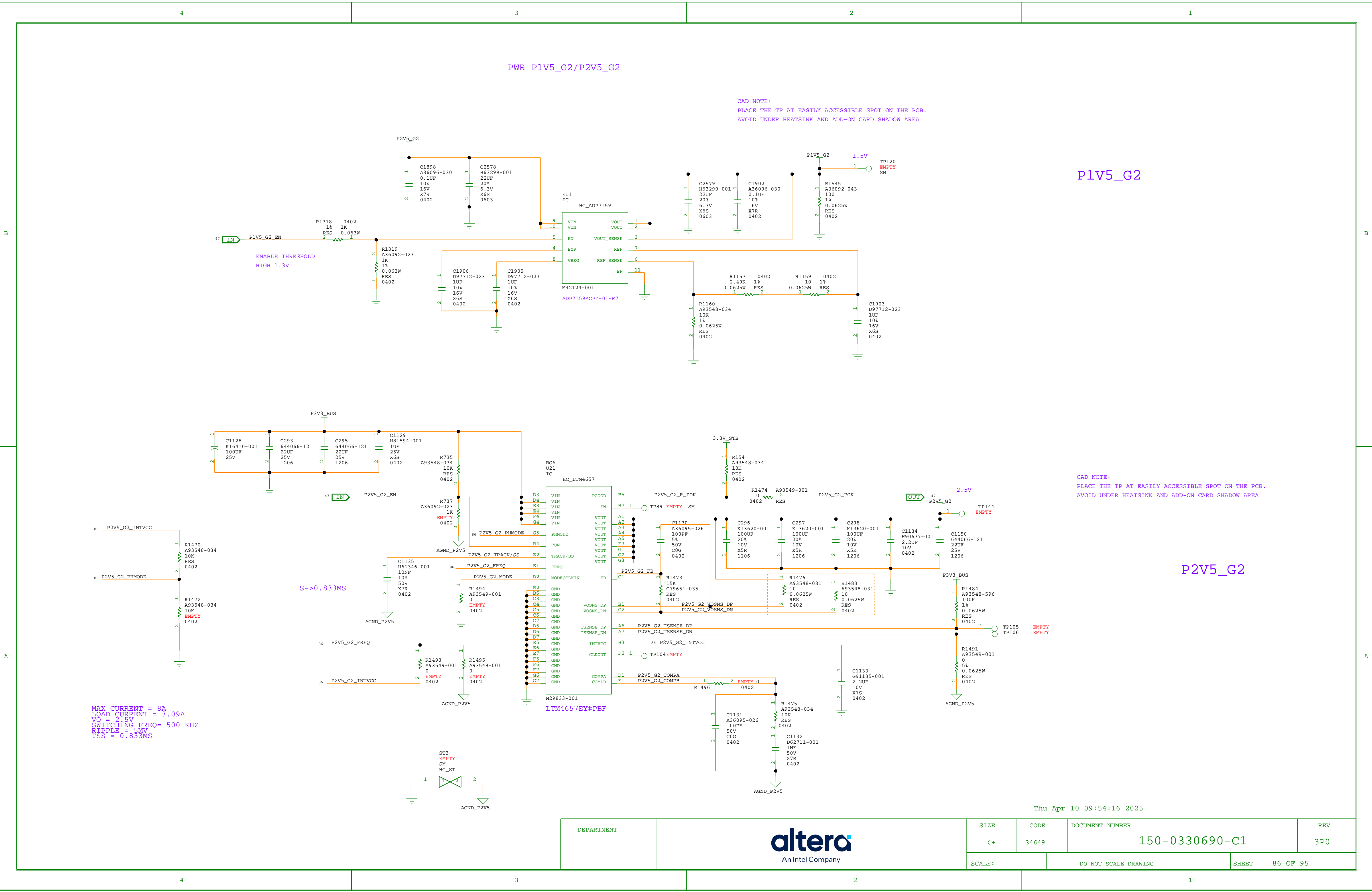


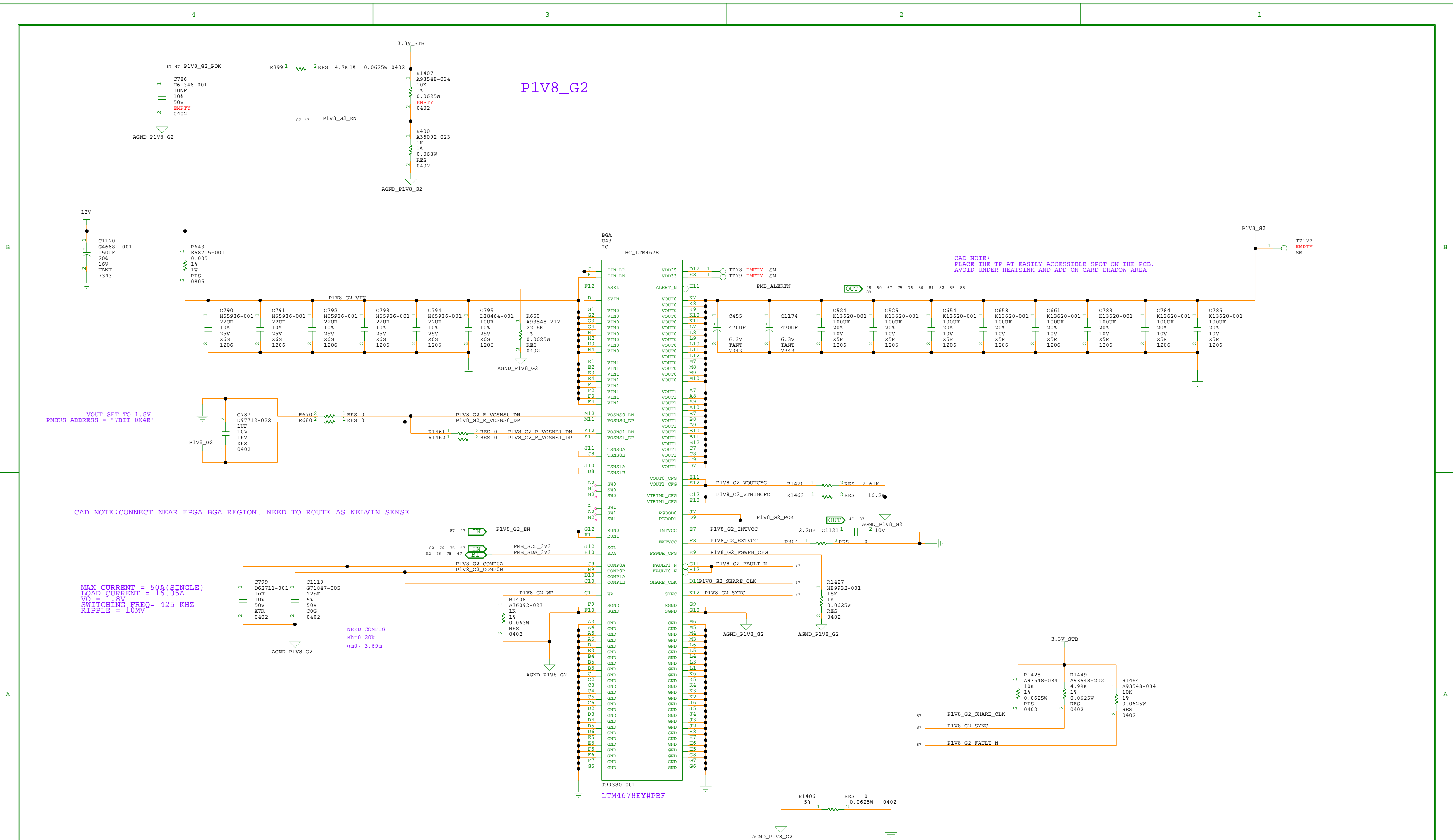
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DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
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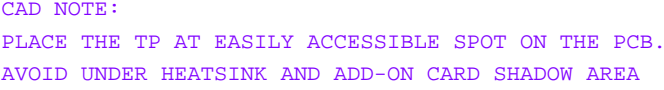


SIZE	CODE	DOCUMENT NUMBER	REV
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SCALE:	DO NOT SCALE DRAWING		SHEET 85 OF 95



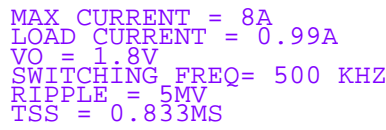


DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
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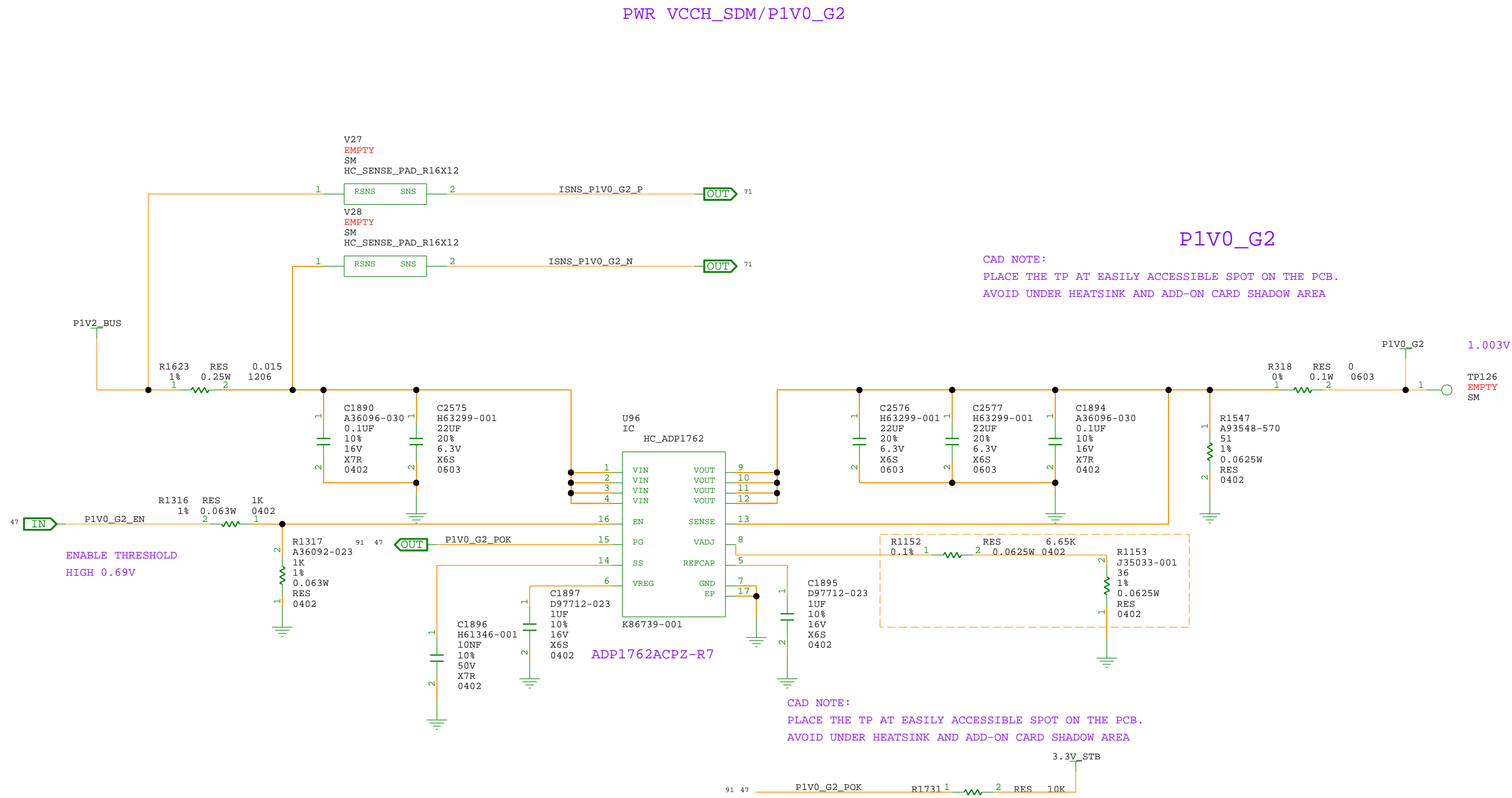
CAD NOTE:CONNECT NEAR FPGA BGA REGION. NEED TO ROUTE AS KELVIN SENSE

```
MAX CURRENT = 36A(SINGLE)
LOAD CURRENT = 29.17A
VO = 1.2V
SWITCHING FREQ= 500 KHZ
RIPPLE = 10MV
```



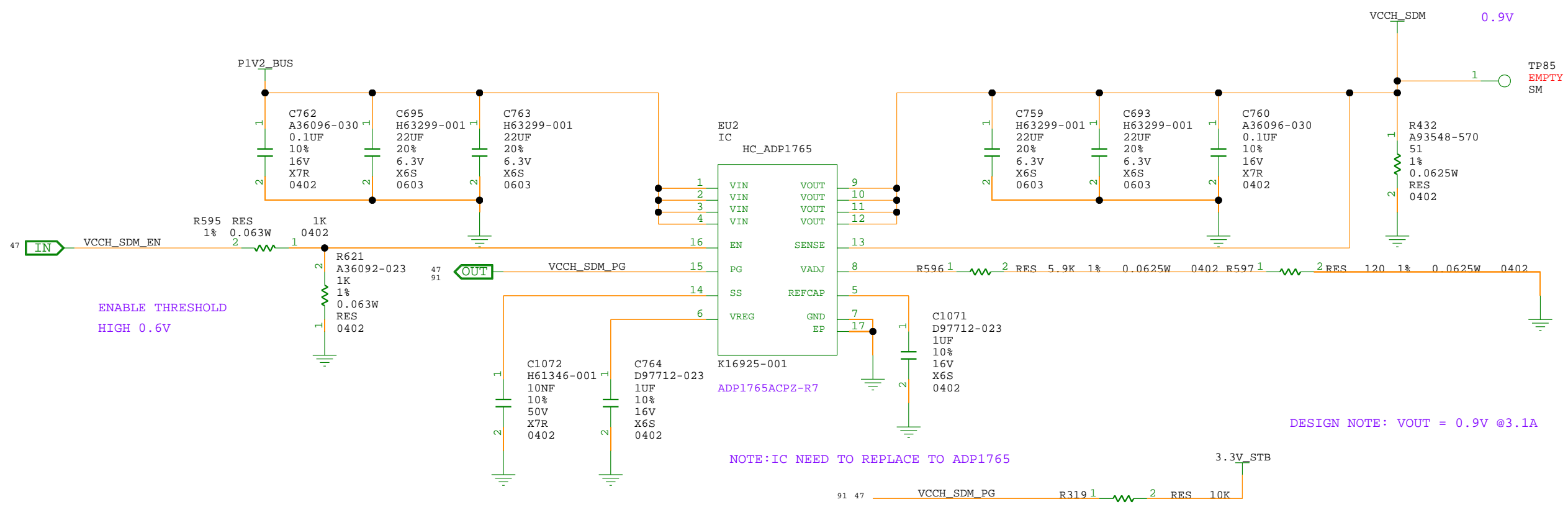
VCCFUSEWR_SDM

B




B

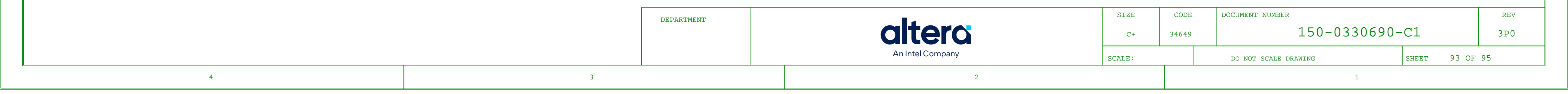
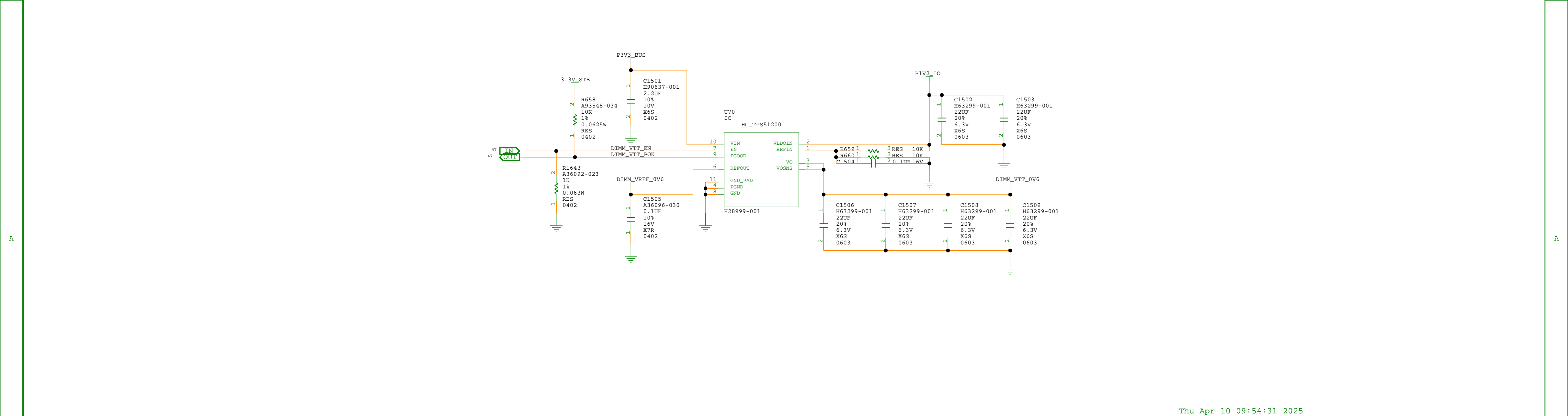
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		SCALE:		DO NOT SCALE DRAWING	SHEET 91 OF 95



USB PD CONTROLLER

CAD NOTE:
NO STUB ON USB0_DP/DM CONNECTING TO THE ZERO OHM

DESIGN NOTE:
I2C2 ACTS AS A SLAVE. MAX-10 COMMUNICATES WITH PD CONTROLLER AS A MASTER
I2C ADDRESS: 0X38

VALUE TO BE CHECKED.

I2C ADDRESS:

PROGRAMMING OF THE FLASH NEED TO BE CLARIFIED WITH FW TEAM

Thu Apr 10 09:54:35 2025

DEPARTMENT



SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-C1

REV

3P0

SCALE:

DO NOT SCALE DRAWING

SHEET

94 OF 95

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