

AGILEX® 7 FPGA I-SERIES, AGI027 4 X F TILE TRANSEIVER -SOC DEVKIT

NOTES :

1. PROJECT DRAWING NUMBERS:

RAW PCB	100-0330690-C1
GERBER FILES	110-0330690-C1
PCB DESIGN FILES	120-0330690-C1
ASSEMBLY DRAWING	130-0330690-C1
FAB DRAWING	140-0330690-C1
SCHEMATIC DRAWING	150-0330690-C1
PCB FILM	160-0330690-C1
BILL OF MATERIALS	170-0330690-C1
SCHEMATIC DESIGN FILES	180-0330690-C1
FUNCTIONAL SPECIFICATION	210-0330690-C1
PCB LAYOUT GUIDELINES	220-0330690-C1
ASSEMBLY REWORK	320-0330690-C1

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30	30- DDR4 HPS COMP-2	80	80- PWR P0V8_G1
31	31- DDR4 HPS COMP-3	81	81- PWR VCC_HSSI_U1X_G1
32	32- DDR4 DIMM-2A	82	82- PWR VCC_HSSI_U2X_G1
33	33- DDR4 DIMM-2B	83	83- PWR VCCERT1_13A/13C
34	34- DIMM PWR FLT	84	84- PWR VCCERT2_U20/U22
35	35- USB3.X/DP MUX	85	85- PWR VCCERT_UX_GDR
36	36- SDI BNC	86	86- PWR P1V5_G2/P2V5_G2
37	37- PCIE MCIO	87	87- PWR P1V8_G2
38	38- QSFP-DD CONN 0	88	88- PWR P1V2_G3
39	39- QSFP-DD CONN 1	89	89- PWR P1V2_IO
40	40- QSFP-DD-800 CONN	90	90- PWR P1V8_G3
41	41- FMC+_A -1	91	91- PWR VCCH_SDM/P1V0_G2
42	42- FMC+_A -2	92	92- PWR LOAD SWITCHES
43	43- FMC+_B-1	93	93- PWR DDR4 VTT
44	44- FMC+_B-2	94	94- PD CONTROLLER
45	45- USB2.0	95	95- BLANK PAGE
46	46 - SMA		
47	47- PWR MAX10 -1		
48	48- PWR MAX10 -2		
49	49- SYS MAX10 -1		
50	50- SYS MAX10 -2		

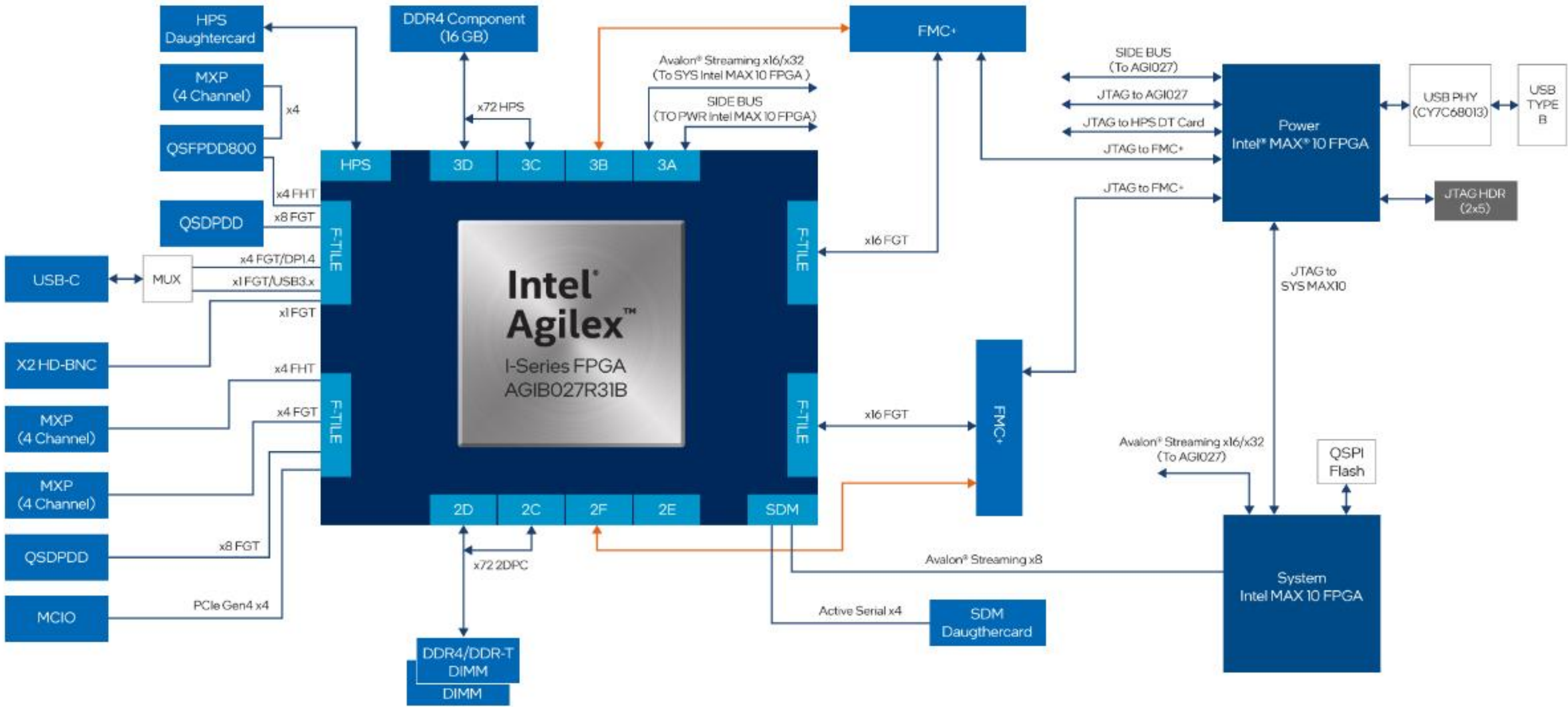
REVISION HISTORY

REV	DATE	PAGES	DESCRIPTION
0P00	31-JANUARY-2022	ALL	RECEIVED BASE FILE SCHEMATIC FOR VR UPDATE
1P0	19-APRIL-2022	ALL	REPLACED ALL THE ENPIRION VR, UPDATED CLOCKS WITH ALTERNATE PART NUMBER.. MADE I2C CONNECTION FROM FPGA TO FMC CONNECTOR.
	07-NOV-2022		REMOVED PG SHORTS AT U79, UPDATED FP FOR CORE SUPPLY INDUCTORS, CORRECTED NETNAME AT P1V8_G3 SUPPLY RAIL
	16-NOV-2022		REPLACED U94,U96 WITH ADP1762ACPZ-R7
3P0	27-FEB-2025		UPDATED THE DESIGN WITH FPGA IPN 99C7TA AND MMID 99CA2X

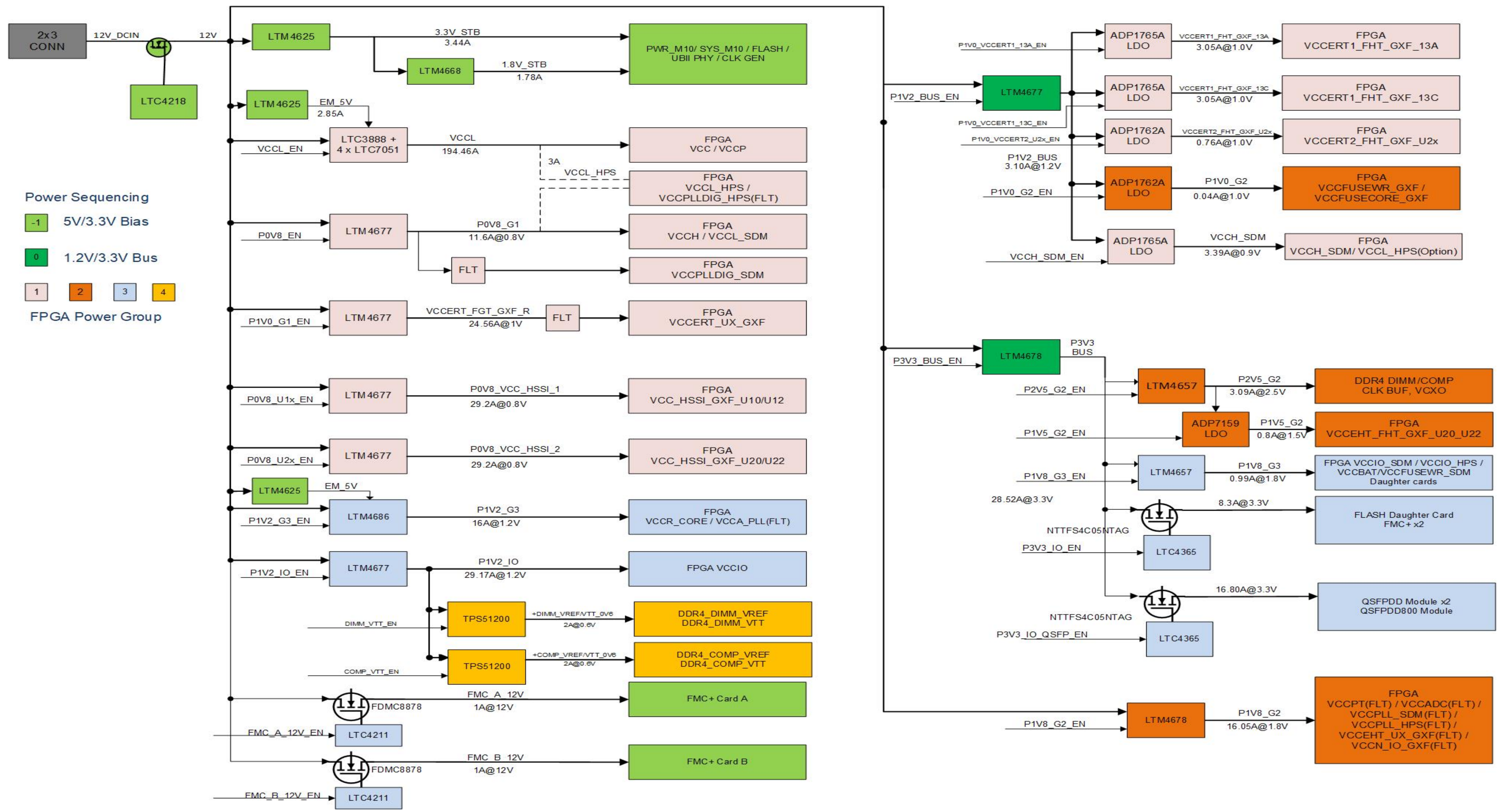
LEVEL	MMID	99CA2X
0	TA	N22854-001
1	ASSY	N24091-200
2	PB	M77505-001
3	ALL ADD ON BOARDS AND ACCESSORIES	NA

Thu Feb 27 10:50:47 2025

BLOCK DIAGRAM

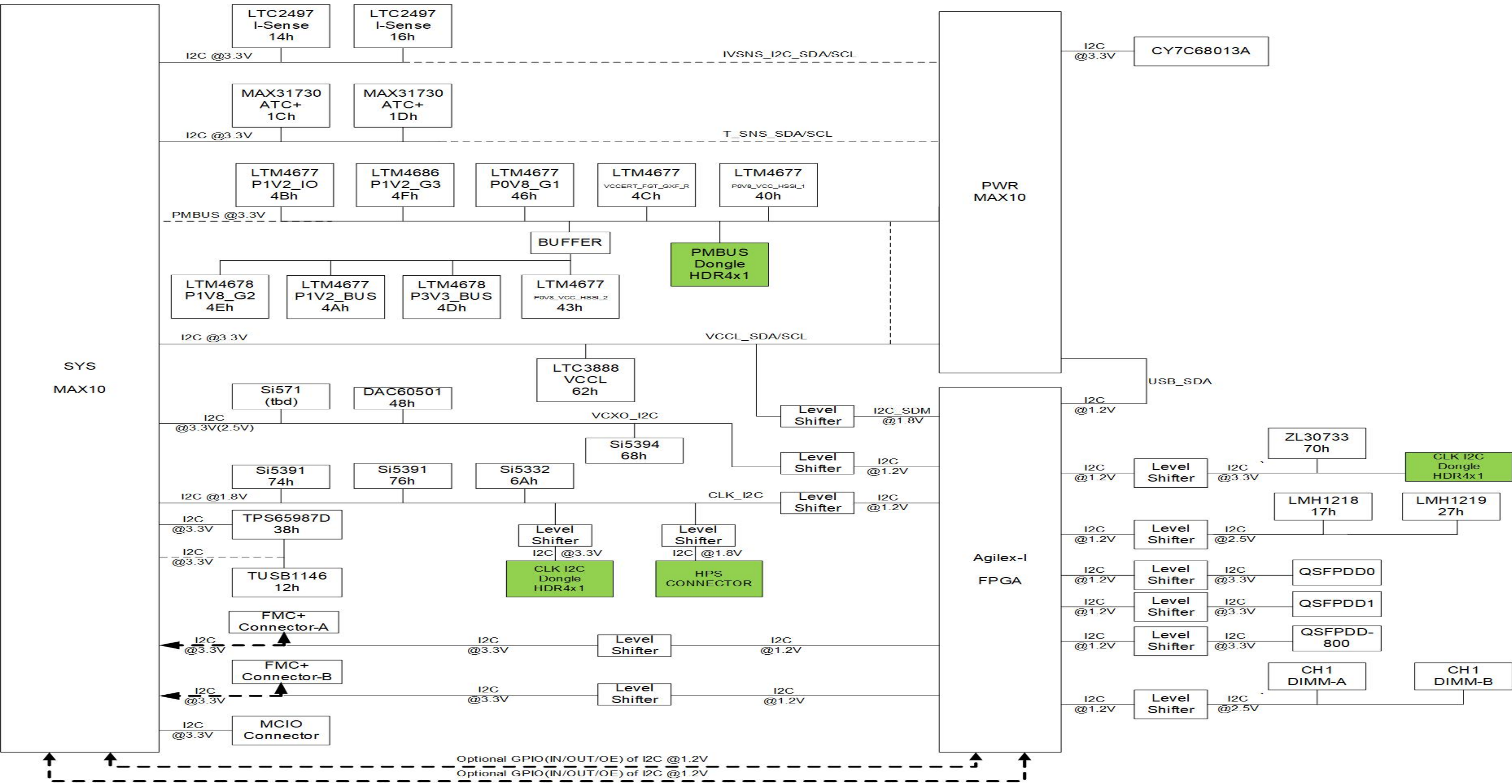


POWER TREE



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I2C TREE



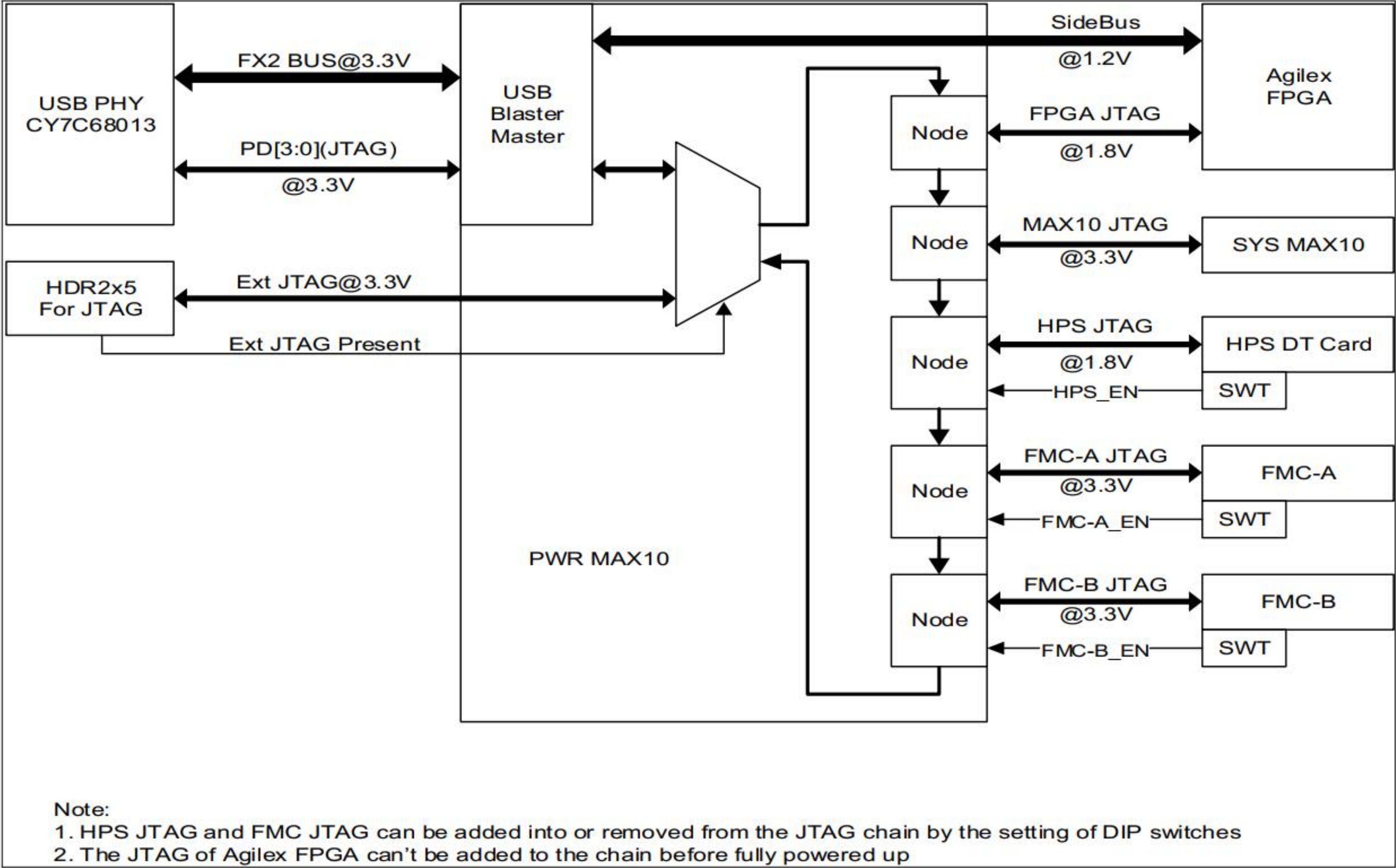
JTAG TOPOLOGY

B

A

B

A



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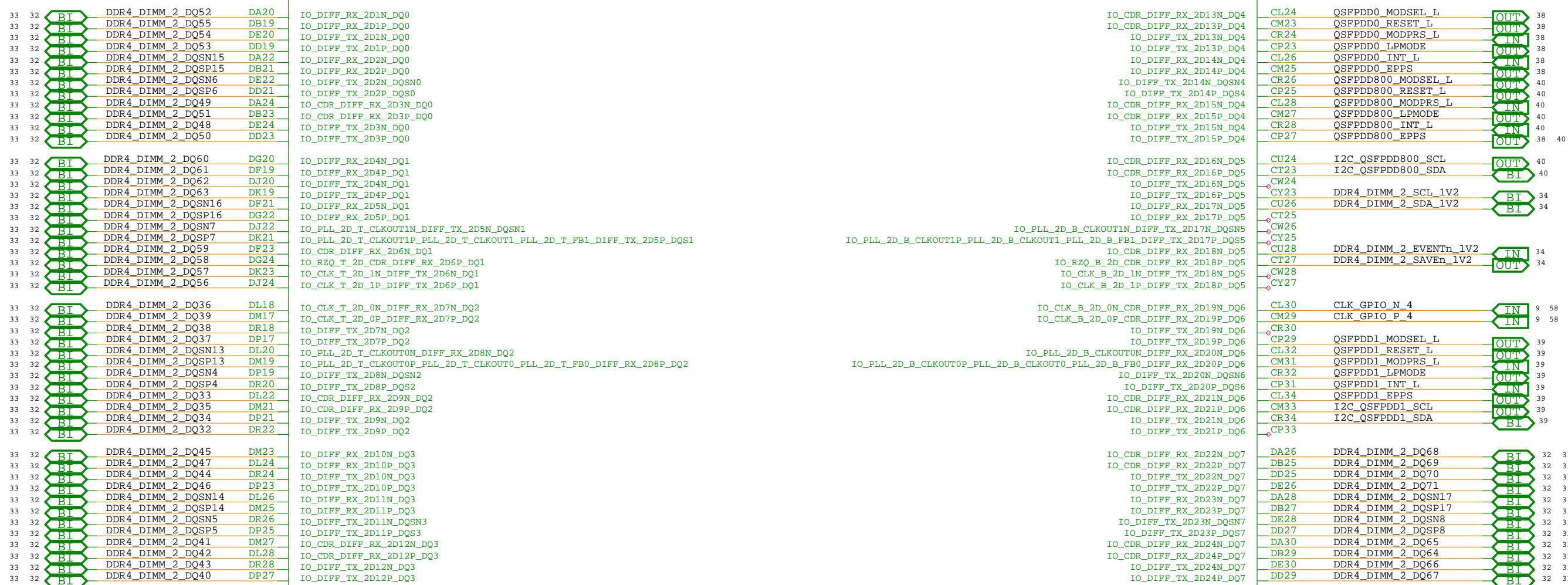


CAD NOTE:
BIT-SWAPPINGS ALLOWED WITHIN A BYTE.
BYTE-SWAPPING IS ALLOWED WITH PRIOR APPROVAL
FROM DESIGN ENGINEER

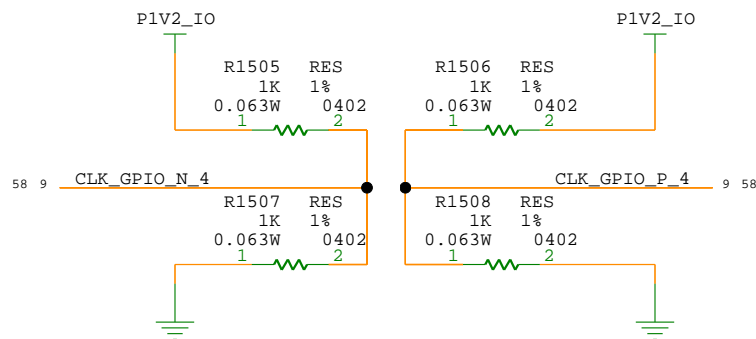
FPGA BANK 2D

U1
EMPTY

HC_FM87_3184B_PHB



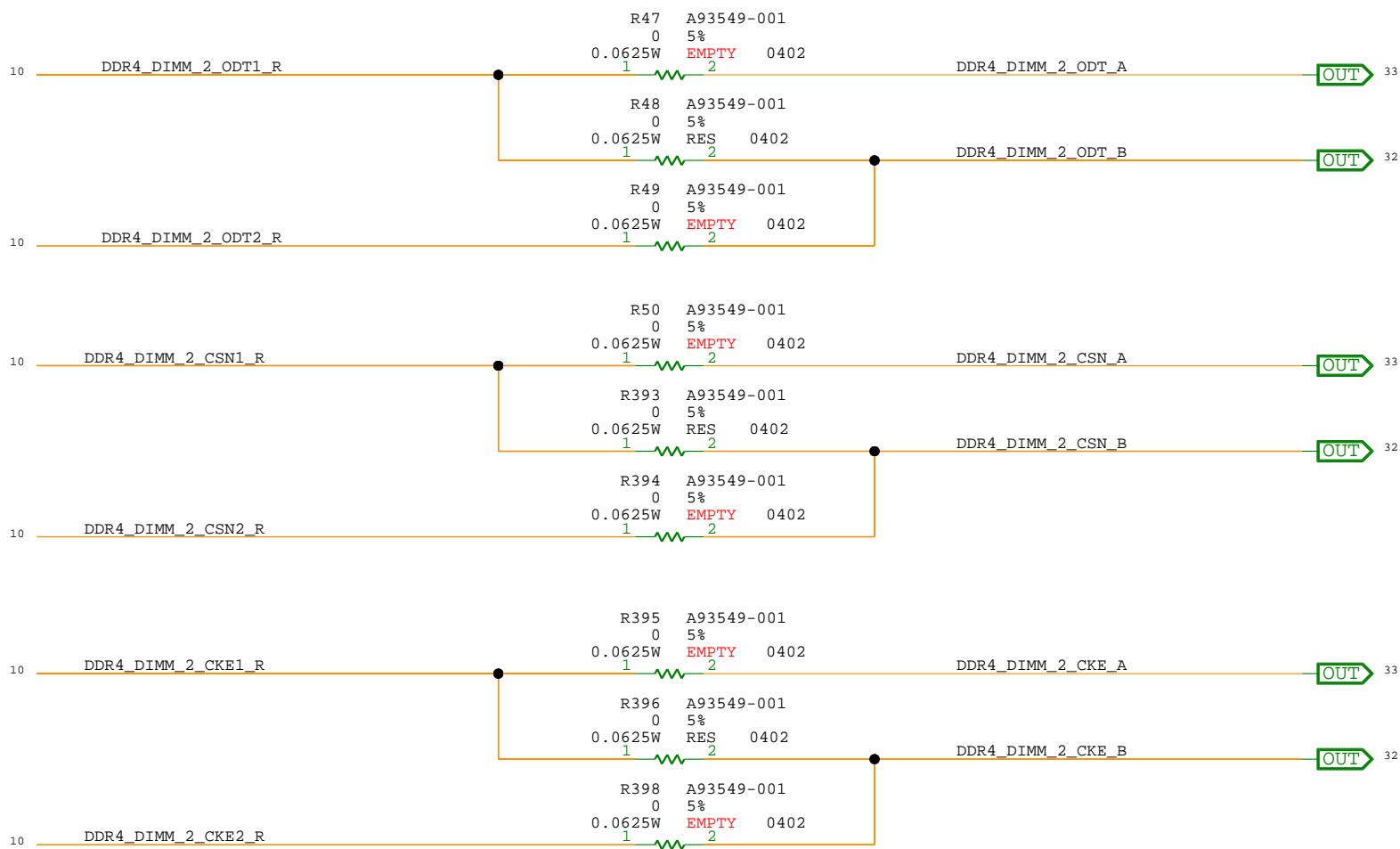
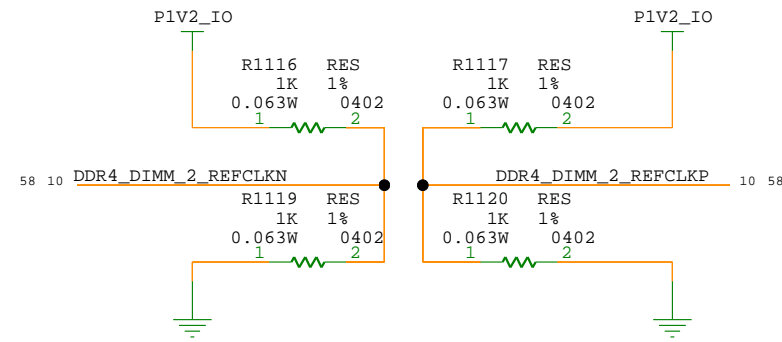
99C7TA



CAD NOTE:
PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA

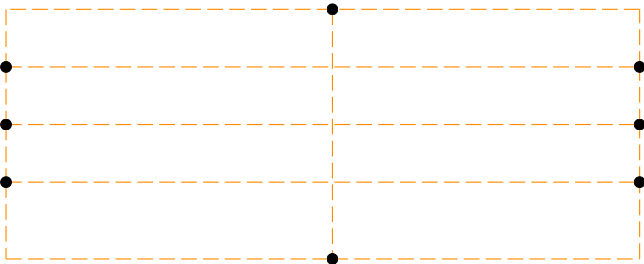
FPGA BANK 2C

U1
EMPTY
HC_FW87_3184B_PHBE



MTA18ASF2G72PZ-3G2E2 16GB SRX4 DDR4-3200

DIMM-B : J36 (NEAR)



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DEPARTMENT



SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-C1

REV

3P0

SCALE:

DO NOT SCALE DRAWING

SHEET

10 OF 95

B

B

A

A

FPGA BANK 2F

U1
EMPTY

HC_FM87_3184B_PHBE

43	B1	FMC_B_LA_N12	DG38
43	B1	FMC_B_LA_P12	DF37
43	B1	FMC_B_LA_N7	DJ38
43	B1	FMC_B_LA_P7	DK37
43	B1	FMC_B_LA_N11	DQ40
43	B1	FMC_B_LA_P11	DF39
43	B1	FMC_B_LA_N8	DJ40
43	B1	FMC_B_LA_P8	DK39
43	B1	FMC_B_LA_N5	DQ42
43	B1	FMC_B_LA_P5	DF41
43	B1	FMC_B_LA_N22	DJ42
43	B1	FMC_B_LA_P22	DK41
43	B1	FMC_B_LA_N23	DL42
43	B1	FMC_B_LA_P23	DM41
43	B1	FMC_B_LA_N13	DR42
43	B1	FMC_B_LA_P13	DP41
43	B1	FMC_B_LA_N10	DL44
43	B1	FMC_B_LA_P10	DM43
43	B1	FMC_B_LA_N9	DR44
43	B1	FMC_B_LA_P9	DP43
43	B1	FMC_B_LA_N14	DL46
43	B1	FMC_B_LA_P14	DM45
43	B1	FMC_B_CLK2_M2C_N	DR46
43	B1	FMC_B_CLK2_M2C_P	DE45
43	1N	FMC_B_CLK0_M2C_N	DG44
43	1N	FMC_B_CLK0_M2C_P	DF43
43	1N	FMC_B_SYNC_M2C_N	DK43
43	1N	FMC_B_SYNC_M2C_P	DJ44
43	0400	FMC_B_REFCLK_C2M_N	DG46
43	0400	FMC_B_REFCLK_C2M_P	DF45
43	0400	FMC_B_SYNC_C2M_N	DJ46
43	0400	FMC_B_SYNC_C2M_P	DK45
43	0400	FMC_B_LA_N25	DG48
43	B1	FMC_B_LA_P25	DF47
			DJ48
			DK47
			DL48
			DM47
			DR48
			DP47
			DL50
			DM49
			DR50
			DP49
			DL52
			DM51
			DR52
			DP51

IO_DIFF_RX_2F1N_DQ16	
IO_DIFF_RX_2F1P_DQ16	
IO_DIFF_TX_2F1N_DQ16	
IO_DIFF_TX_2F1P_DQ16	
IO_DIFF_RX_2F2N_DQ16	
IO_DIFF_TX_2F2P_DQ16	
IO_CDR_DIFF_RX_2F3N_DQ16	
IO_CDR_DIFF_RX_2F3P_DQ16	
IO_DIFF_TX_2F3N_DQ16	
IO_DIFF_TX_2F3P_DQ16	
IO_DIFF_RX_2F4N_DQ17	
IO_DIFF_RX_2F4P_DQ17	
IO_DIFF_TX_2F4N_DQ17	
IO_DIFF_TX_2F4P_DQ17	
IO_DIFF_RX_2F5N_DQ17	
IO_DIFF_RX_2F5P_DQ17	
IO_PLD_2F_T_CLKOUT1N_DIFF_TX_2F5N_DQSN17	
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IO_CDR_DIFF_RX_2F6N_DQ17	
IO_RZQ_B_2F_CDR_DIFF_RX_2F6P_DQ17	
IO_CLK_T_2F_1N_DIFF_TX_2F6N_DQ17	
IO_CLK_T_2F_1P_DIFF_TX_2F6P_DQ17	
IO_CLK_T_2F_0N_DIFF_RX_2F7N_DQ18	
IO_CLK_T_2F_0P_DIFF_RX_2F7P_DQ18	
IO_DIFF_TX_2F7N_DQ18	
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IO_DIFF_TX_2F8N_DQSN18	
IO_DIFF_TX_2F8P_DQSN18	
IO_CDR_DIFF_RX_2F9N_DQ18	
IO_CDR_DIFF_RX_2F9P_DQ18	
IO_DIFF_TX_2F9N_DQ18	
IO_DIFF_TX_2F9P_DQ18	
IO_DIFF_RX_2F10N_DQ19	
IO_DIFF_RX_2F10P_DQ19	
IO_DIFF_TX_2F10N_DQ19	
IO_DIFF_TX_2F10P_DQ19	
IO_DIFF_RX_2F11N_DQ19	
IO_DIFF_RX_2F11P_DQ19	
IO_DIFF_TX_2F11N_DQSN19	
IO_DIFF_TX_2F11P_DQSN19	
IO_CDR_DIFF_RX_2F12N_DQ19	
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IO_DIFF_TX_2F12N_DQ19	
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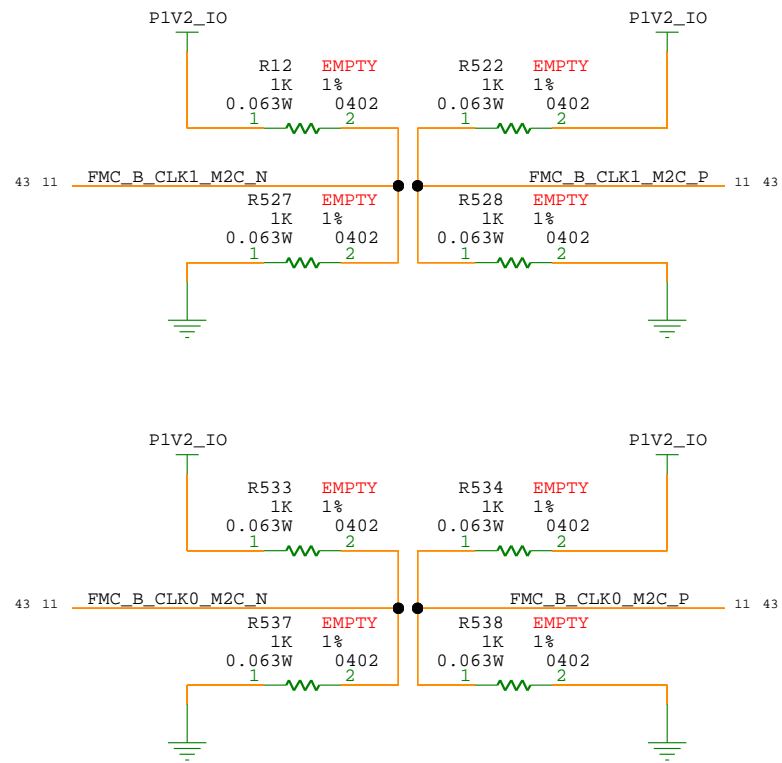
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IO BANK 2F

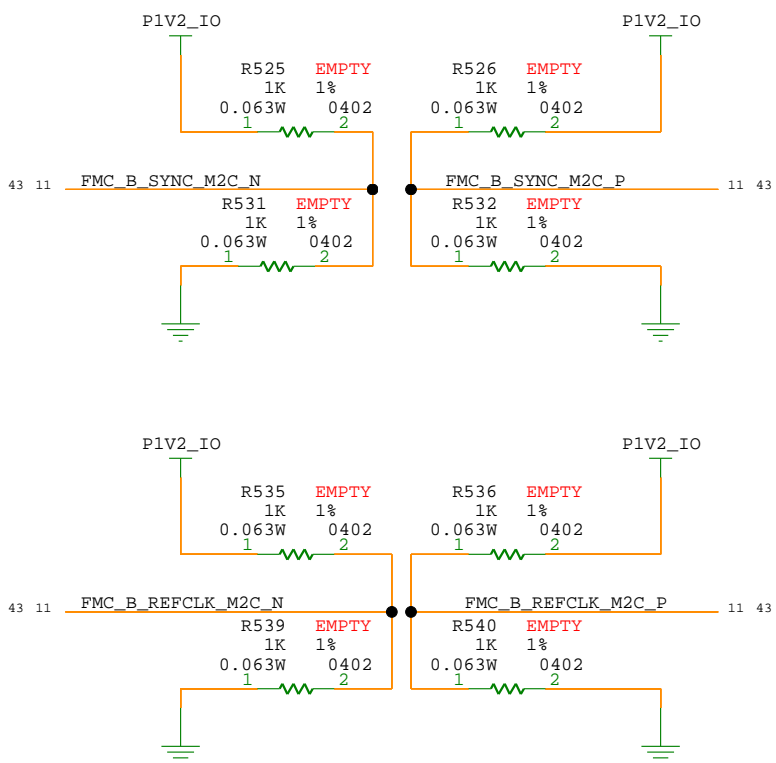
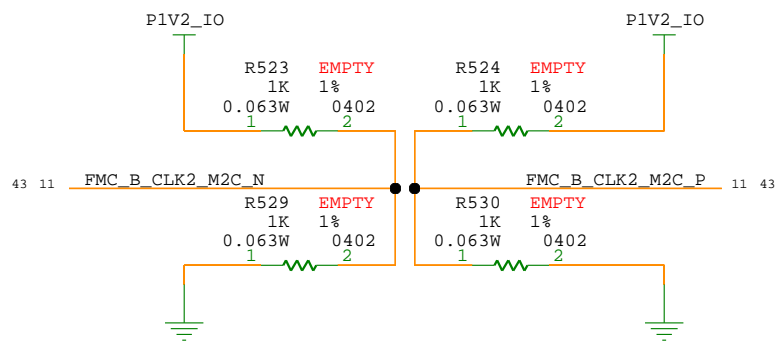
99C7TA

IO_CDR_DIFF_RX_2F13N_DQ20	
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IO_DIFF_TX_2F13N_DQ20	
IO_DIFF_TX_2F13P_DQ20	
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IO_DIFF_TX_2F15P_DQ20	
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IO_DIFF_TX_2F16P_DQ21	
IO_DIFF_RX_2F17N_DQ21	
IO_DIFF_RX_2F17P_DQ21	
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IO_CDR_DIFF_RX_2F18N_DQ21	
IO_RZQ_B_2F_CDR_DIFF_RX_2F18P_DQ21	
IO_CLK_B_2F_1N_DIFF_TX_2F18N_DQ21	
IO_CLK_B_2F_1P_DIFF_TX_2F18P_DQ21	
IO_CLK_B_2F_0N_CDR_DIFF_RX_2F19N_DQ22	
IO_CLK_B_2F_0P_CDR_DIFF_RX_2F19P_DQ22	
IO_DIFF_TX_2F19N_DQ22	
IO_DIFF_TX_2F19P_DQ22	
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IO_DIFF_TX_2F20P_DQSN22	
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IO_DIFF_TX_2F21N_DQ22	
IO_DIFF_TX_2F21P_DQ22	
IO_CDR_DIFF_RX_2F22N_DQ23	
IO_CDR_DIFF_RX_2F22P_DQ23	
IO_DIFF_TX_2F22N_DQ23	
IO_DIFF_TX_2F22P_DQ23	
IO_DIFF_RX_2F23N_DQ23	
IO_DIFF_RX_2F23P_DQ23	
IO_DIFF_TX_2F23N_DQSN23	
IO_DIFF_TX_2F23P_DQSN23	
IO_CDR_DIFF_RX_2F24N_DQ23	
IO_CDR_DIFF_RX_2F24P_DQ23	
IO_DIFF_TX_2F24N_DQ23	
IO_DIFF_TX_2F24P_DQ23	

DA38	FMC_B_LA_N6	B1	43
DB37	FMC_B_LA_P6	B1	43
DE38	FMC_B_LA_N2	B1	43
DD37	FMC_B_LA_P2	B1	43
DA40	FMC_B_LA_N15	B1	43
DB39	FMC_B_LA_P15	B1	43
DE40	FMC_B_LA_N4	B1	43
DD39	FMC_B_LA_P4	B1	43
DA42	FMC_B_LA_N20	B1	43
DB41	FMC_B_LA_P20	B1	43
DE42	FMC_B_LA_N21	B1	43
DD41	FMC_B_LA_P21	B1	43
DA44	FMC_B_LA_N32	B1	43
DB43	FMC_B_LA_P32	B1	43
DE44	FMC_B_LA_N26	B1	43
DA43	FMC_B_LA_P26	B1	43
DE46	FMC_B_LA_N24	B1	43
DB45	FMC_B_LA_P24	B1	43
DE46	FMC_B_LA_N0	B1	43
DA45	FMC_B_LA_P0	B1	43
DA48	FMC_B_LA_N3	B1	43
DB47	FMC_B_LA_P3	B1	43
DE48	FMC_B_CLK1_M2C_N	1N	11 43
DD47	FMC_B_CLK1_M2C_P	1N	11 43
CT41	FMC_B_REFCLK_M2C_N	1N	11 43
CU42	FMC_B_REFCLK_M2C_P	1N	11 43
CY41	FMC_B_LA_N33	B1	43
CW42	FMC_B_LA_P33	B1	43
CU44	FMC_B_LA_N19	B1	43
CT43	FMC_B_LA_P19	B1	43
CW44	FMC_B_LA_N28	B1	43
CY43	FMC_B_LA_P28	B1	43
CU46	FMC_B_LA_N1	B1	43
CT45	FMC_B_LA_P1	B1	43
CY45	FMC_B_LA_N29	B1	43
CW46	FMC_B_LA_P29	B1	43
CM41	FMC_B_LA_N18	B1	43
CL42	FMC_B_LA_P18	B1	43
CP42	FMC_B_LA_N17	B1	43
CP41	FMC_B_LA_P17	B1	43
CL44	FMC_B_LA_N16	B1	43
CM43	FMC_B_LA_P16	B1	43
CB44	FMC_B_LA_N27	B1	43
CP43	FMC_B_LA_P27	B1	43
CM45	FMC_B_LA_N30	B1	43
CL46	FMC_B_LA_P30	B1	43
CP45	FMC_B_LA_N31	B1	43
CR46	FMC_B_LA_P31	B1	43



CAD NOTE:
PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA



CAD NOTE:
PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA

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DEPARTMENT



SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-C1

REV

3P0

SCALE:

DO NOT SCALE DRAWING

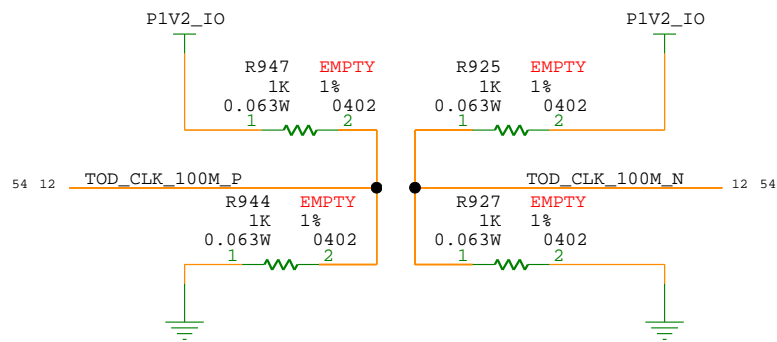
SHEET

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FPGA BANK 2E

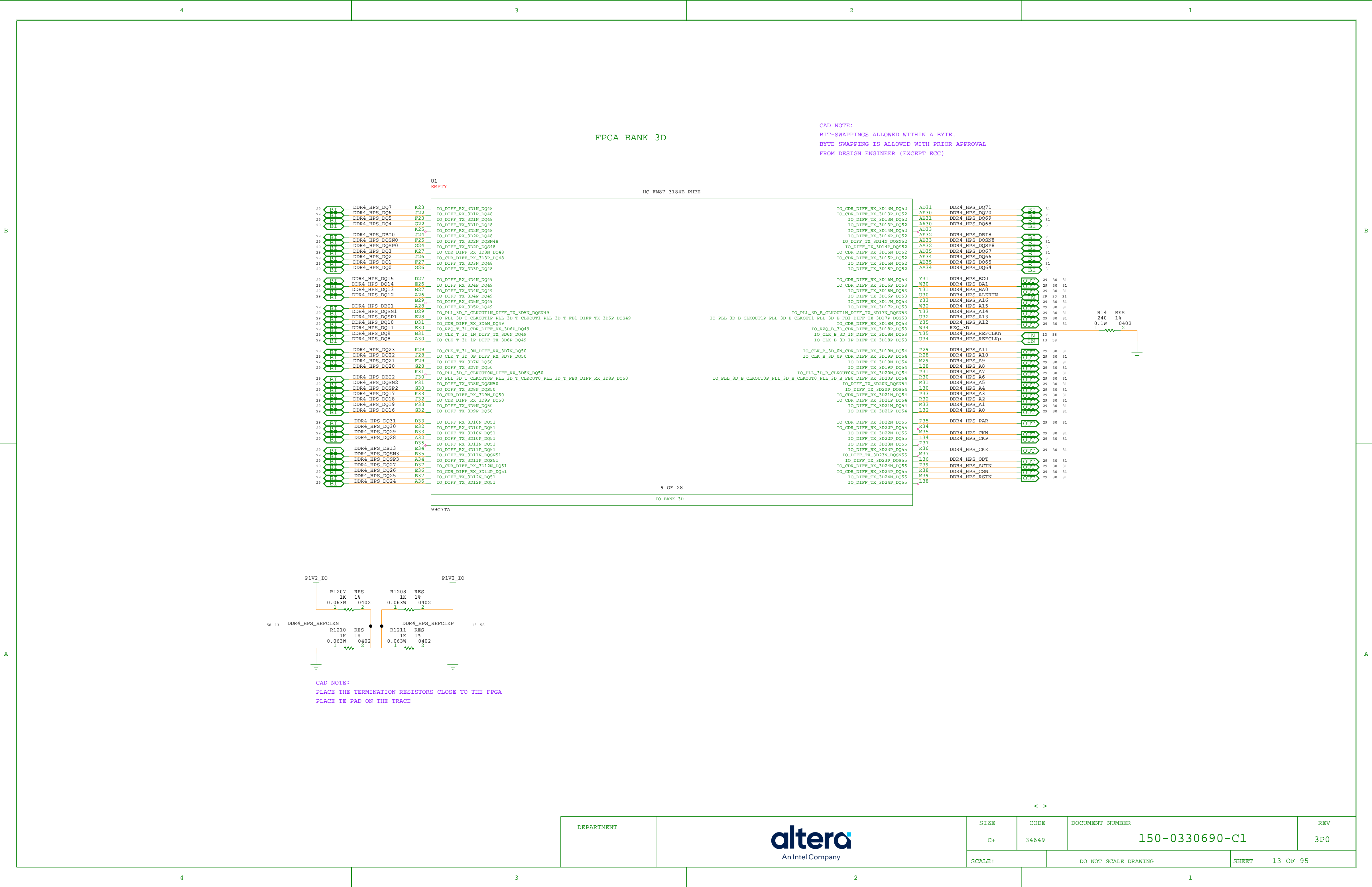
U1
EMPTY

HC_FM87_3184B_PHBE



CAD NOTE:
PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330690-C1	3P0
		SCALE:	DO NOT SCALE DRAWING		SHEET 12 OF 95



FPGA BANK 3C

U1
EMPTY

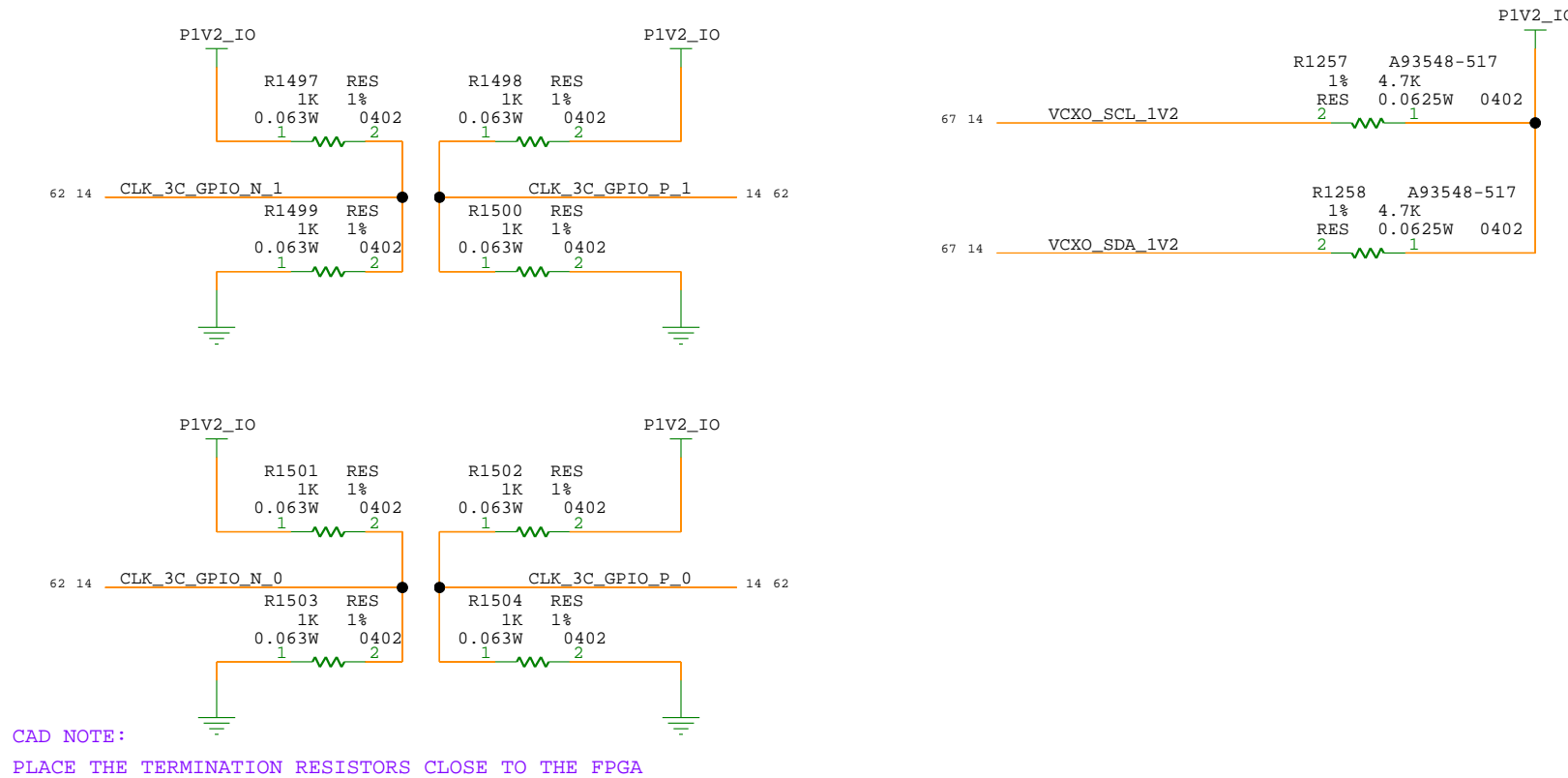
HC_FM87_3184B_PHBDE



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IO BANK 3C

99C77A



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DEPARTMENT

altera
An Intel Company

SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-C1

REV

3P0

SCALE:

DO NOT SCALE DRAWING

SHEET

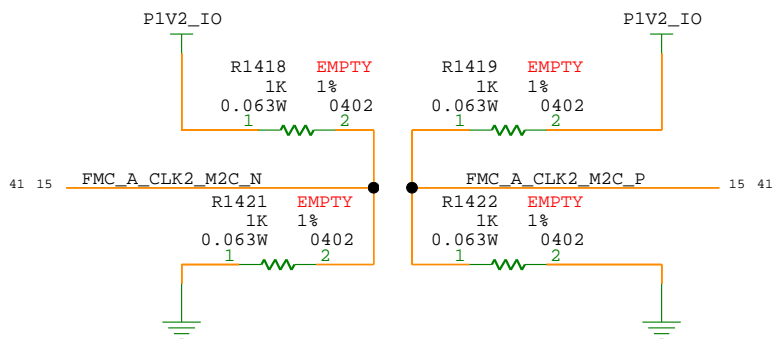
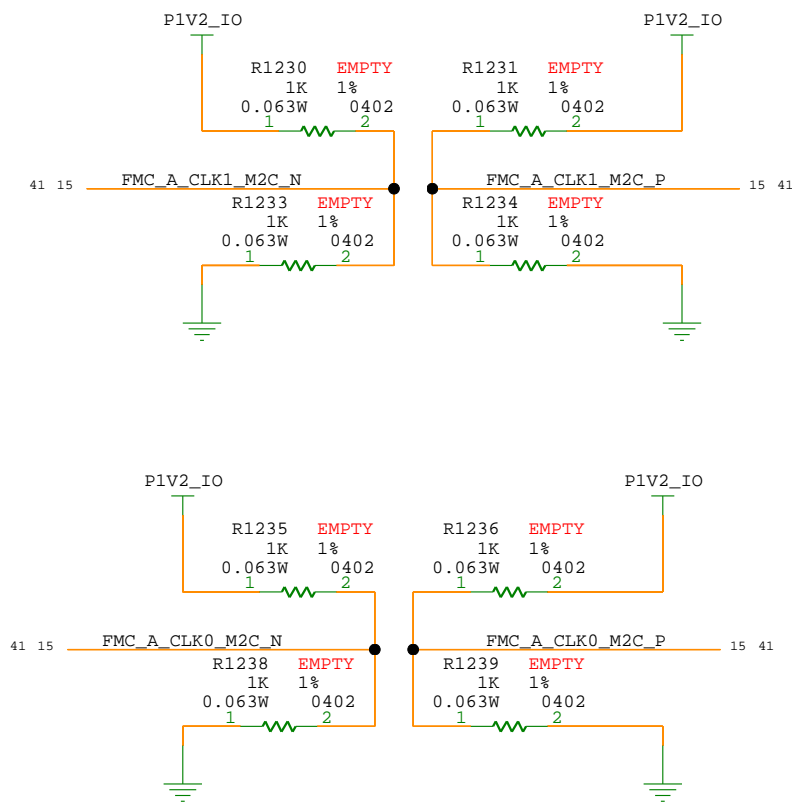
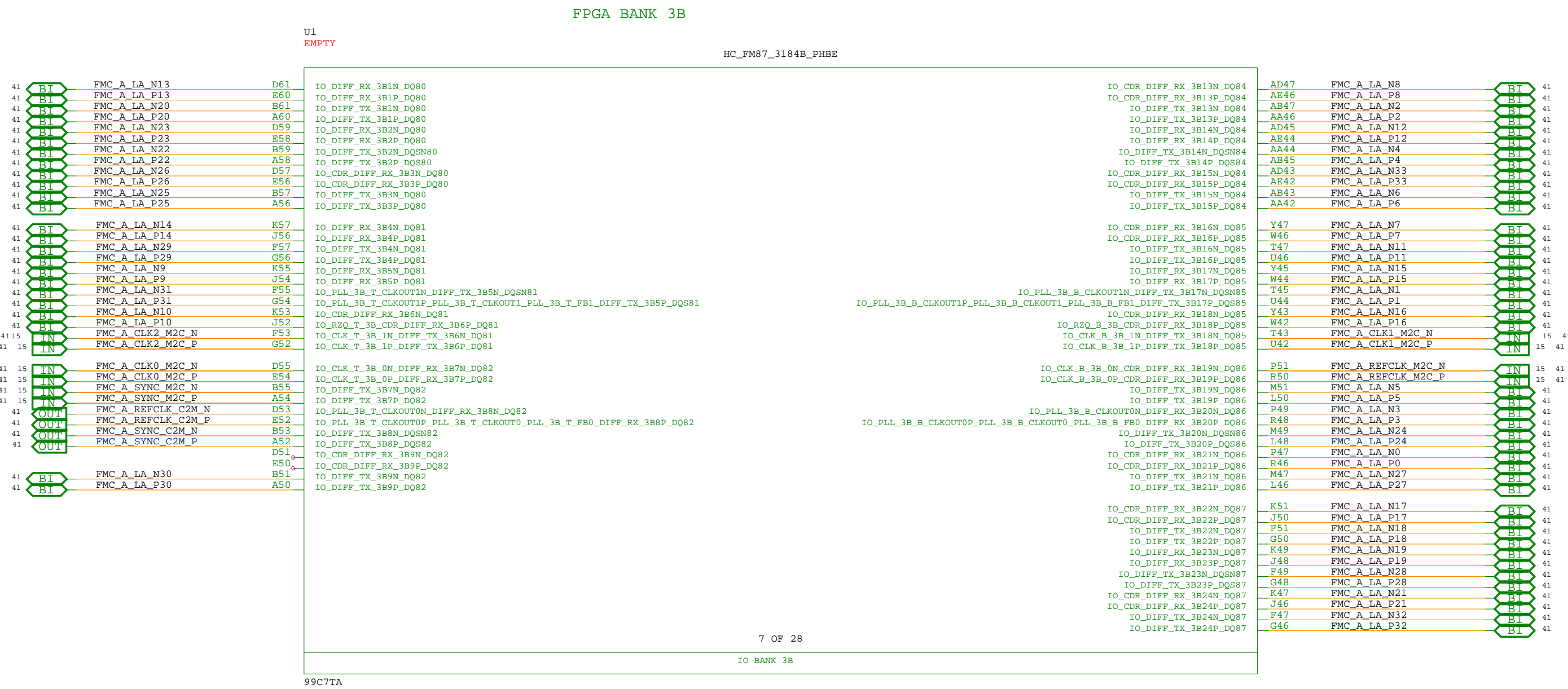
14 OF 95

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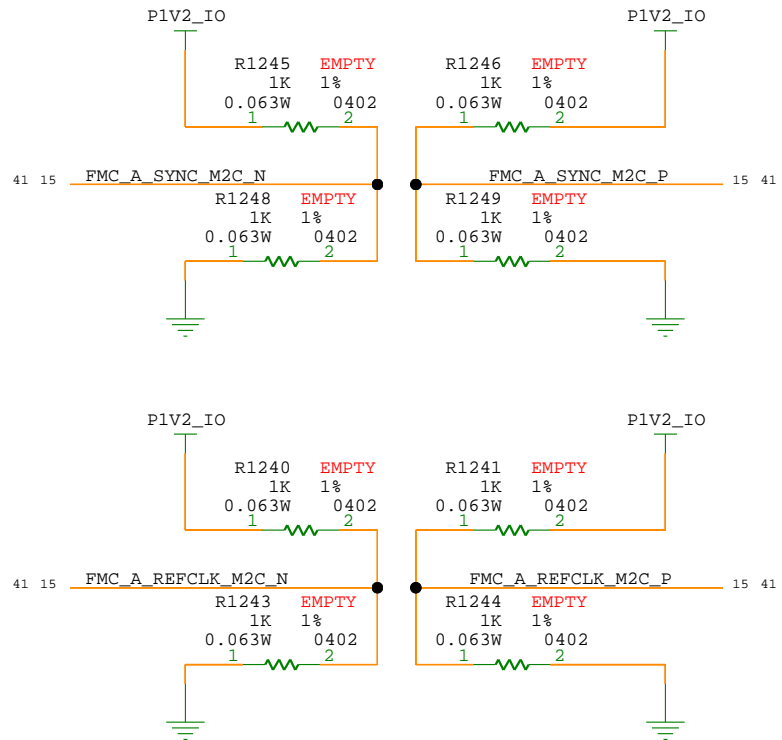
B

A

A



CAD NOTE:
PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA



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DEPARTMENT



SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-C1

REV

3P0

SCALE:

DO NOT SCALE DRAWING

SHEET

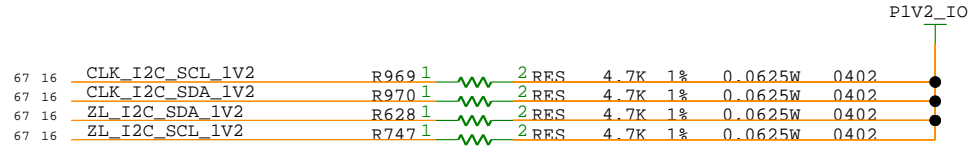
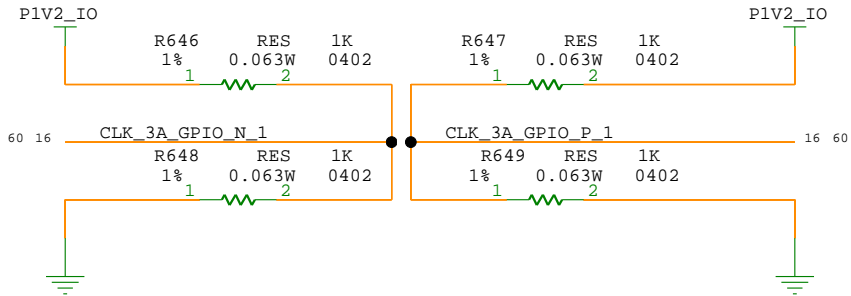
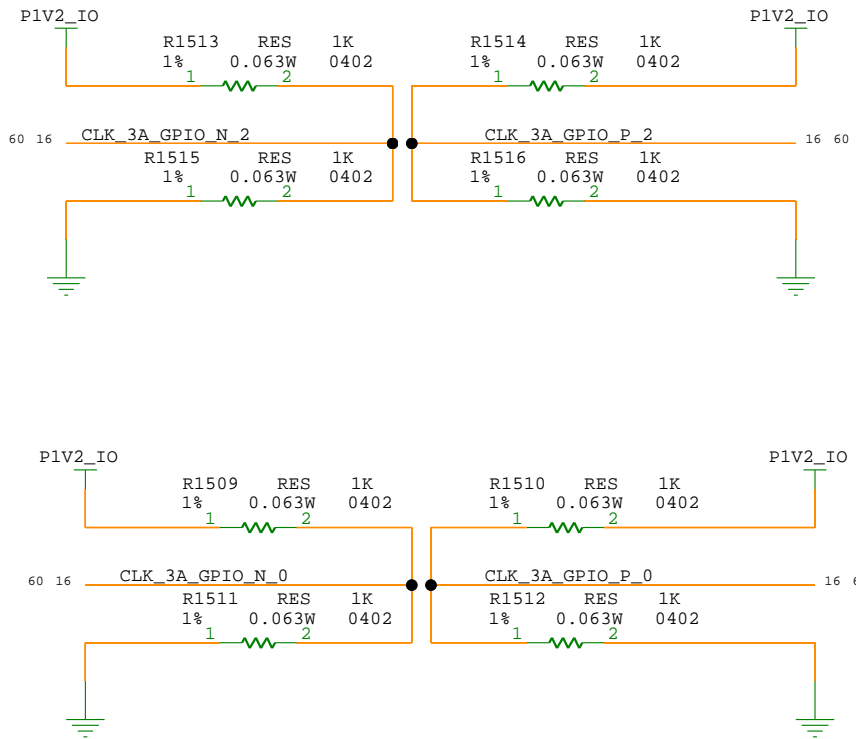
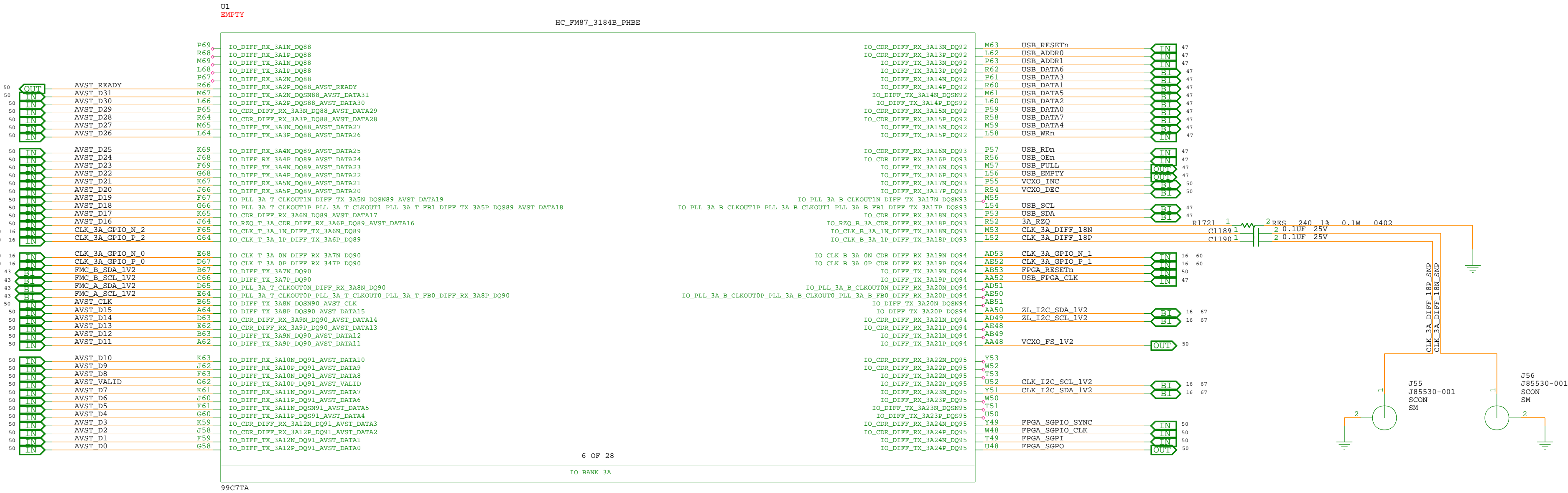
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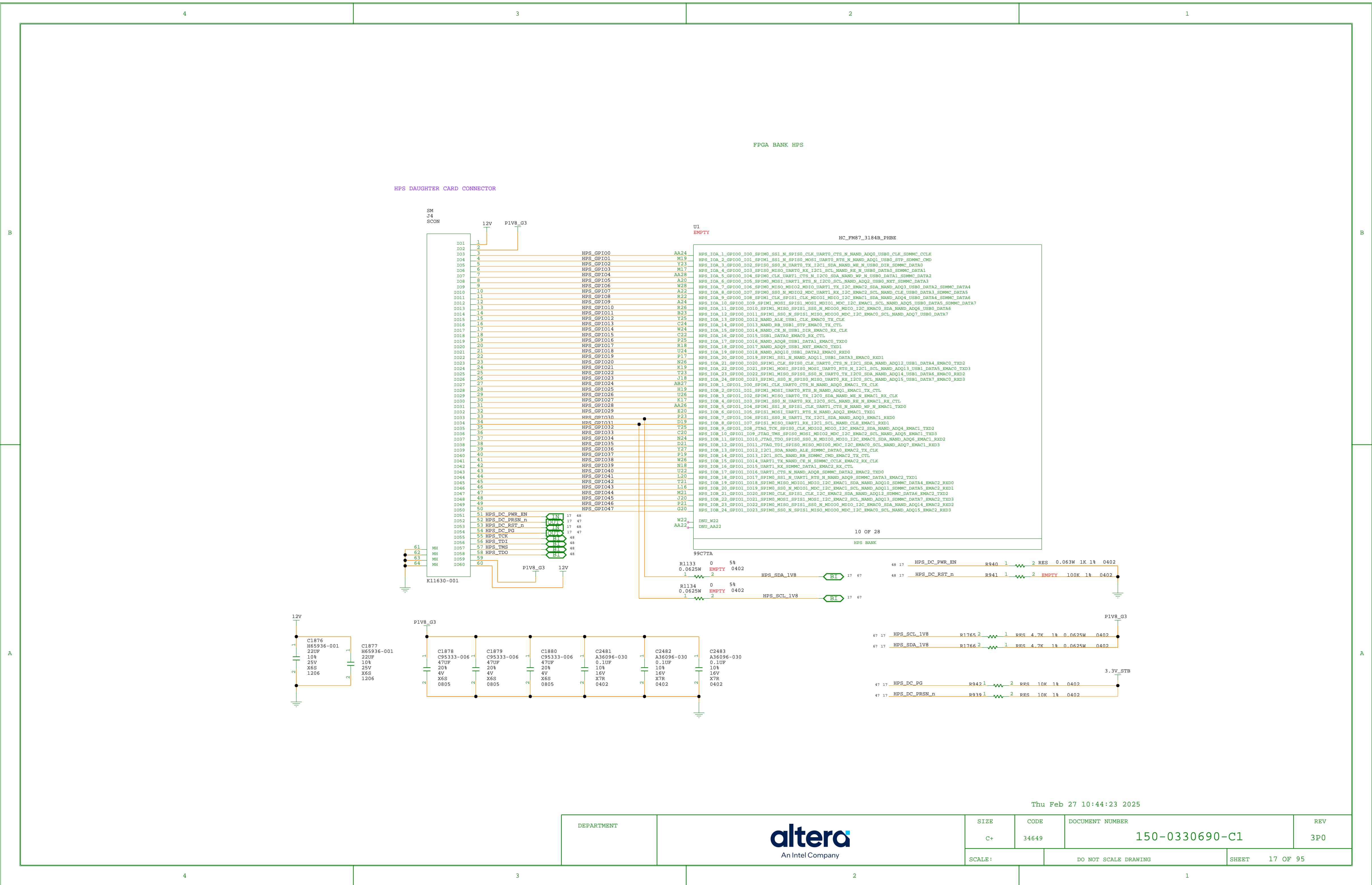
A

A

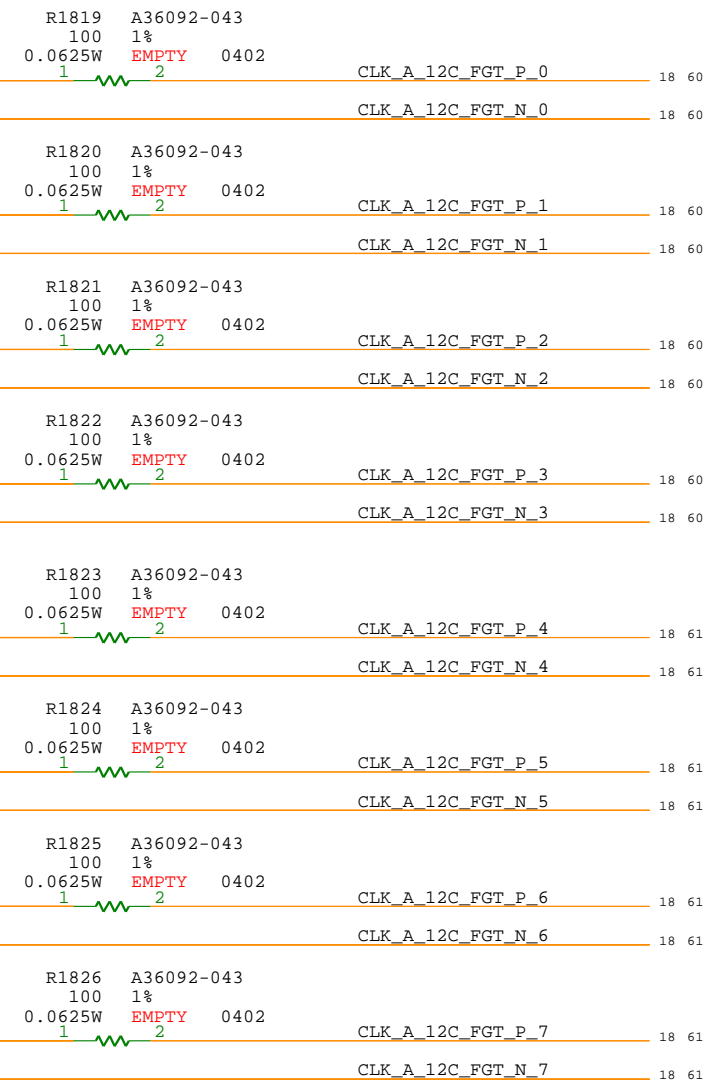


CAD NOTE:
PLACE THE TERMINATION RESISTORS CLOSE TO THE FPGA

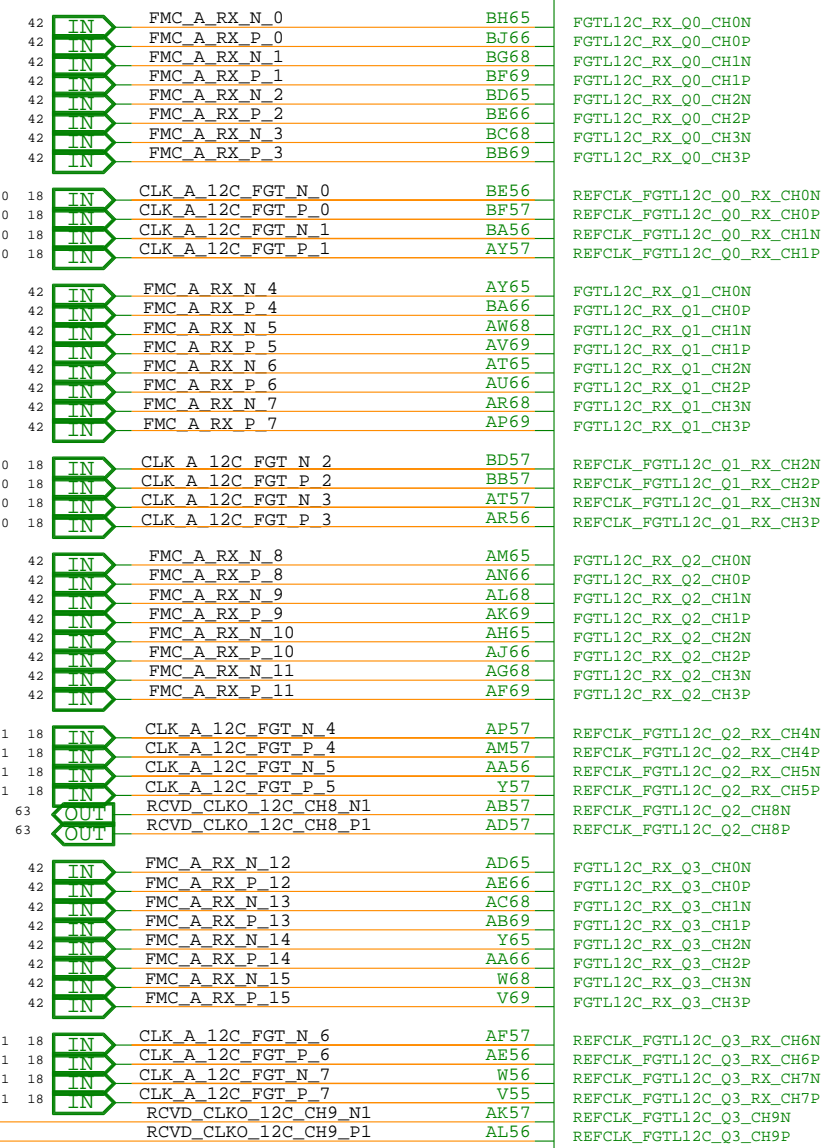
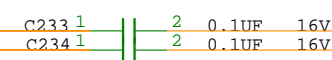
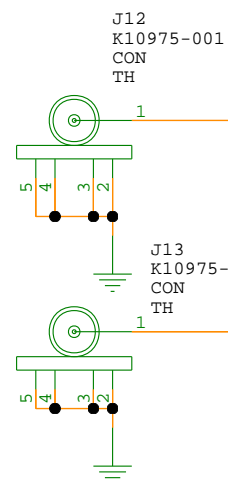
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CAD NOTE:

PLACE THESE 100-OHM RES RIGHT BELOW FPGA BALLS
ON THE BREAKOUT VIAS.CAD NOTE: PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS.
FMC_A_RX*

CAD NOTE:

BREAK-OUT EVERY TP* NETS TO AN
EXPOSED PAD ON THE BOTTOM SIDE.

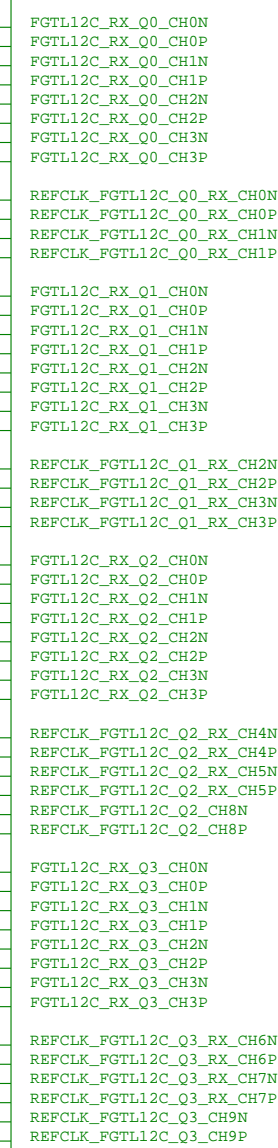
FPGA BANK 12C

U1

EMPTY

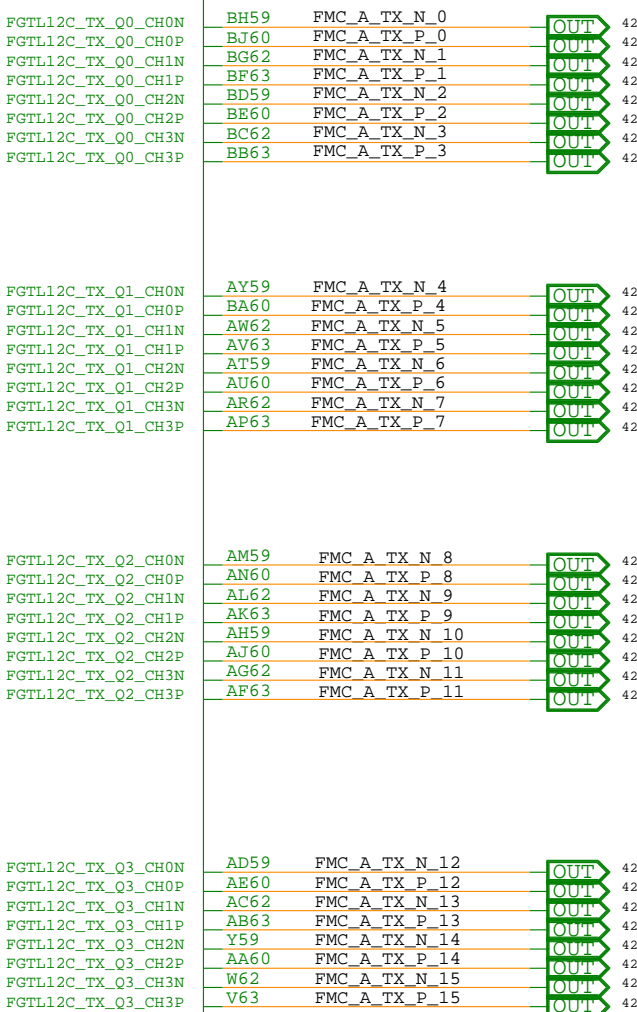
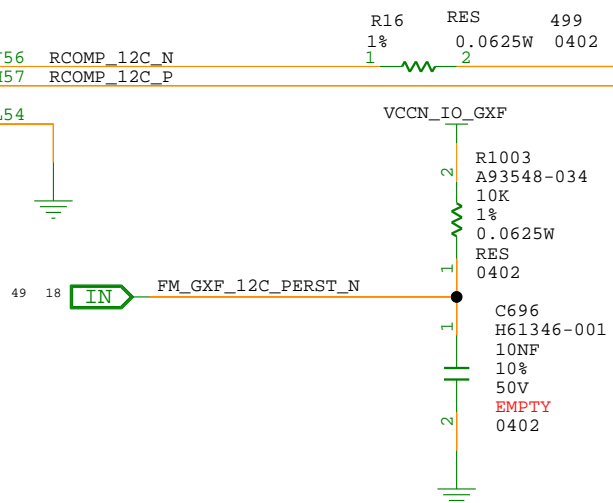
HC_FM87_3184B_PHBE

FMC + : A



CAD NOTE: PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS.

FMC_A_TX*

CAD Note:
Please place 100-ohm res right below FPGA balls
on the breakout vias.

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DEPARTMENT

altera
An Intel Company

SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-C1

REV

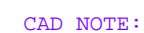
3P0

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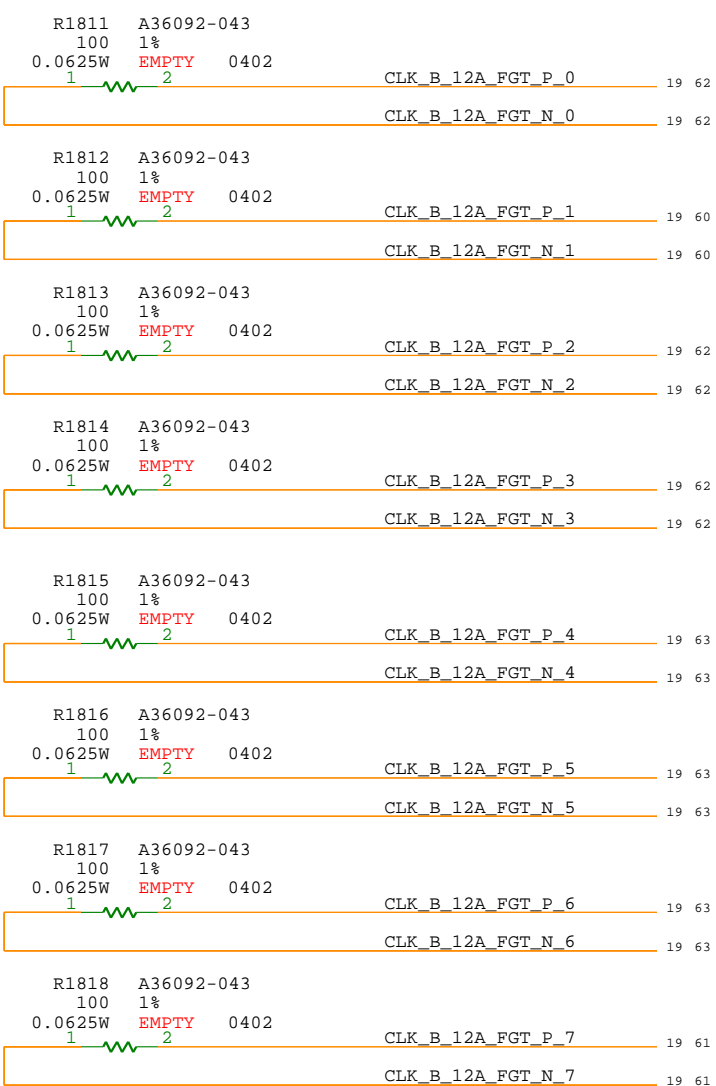
DO NOT SCALE DRAWING

SHEET

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PLACE THESE 100-OHM RES RIGHT BELOW FPGA BALLS
ON THE BREAKOUT VIAS.



CAD NOTE: PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS

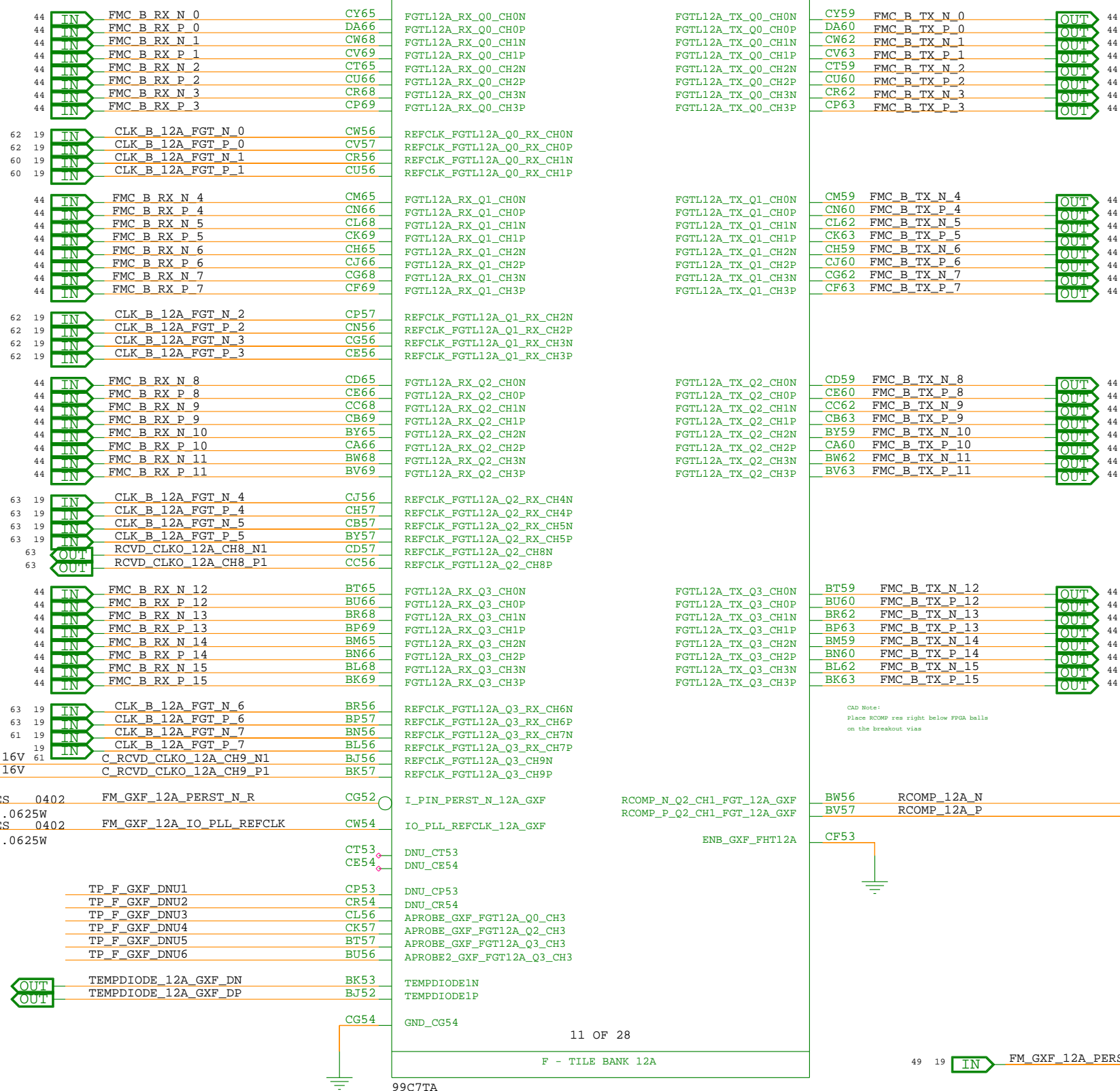
FMC_B_RX*

U1
EMPTY

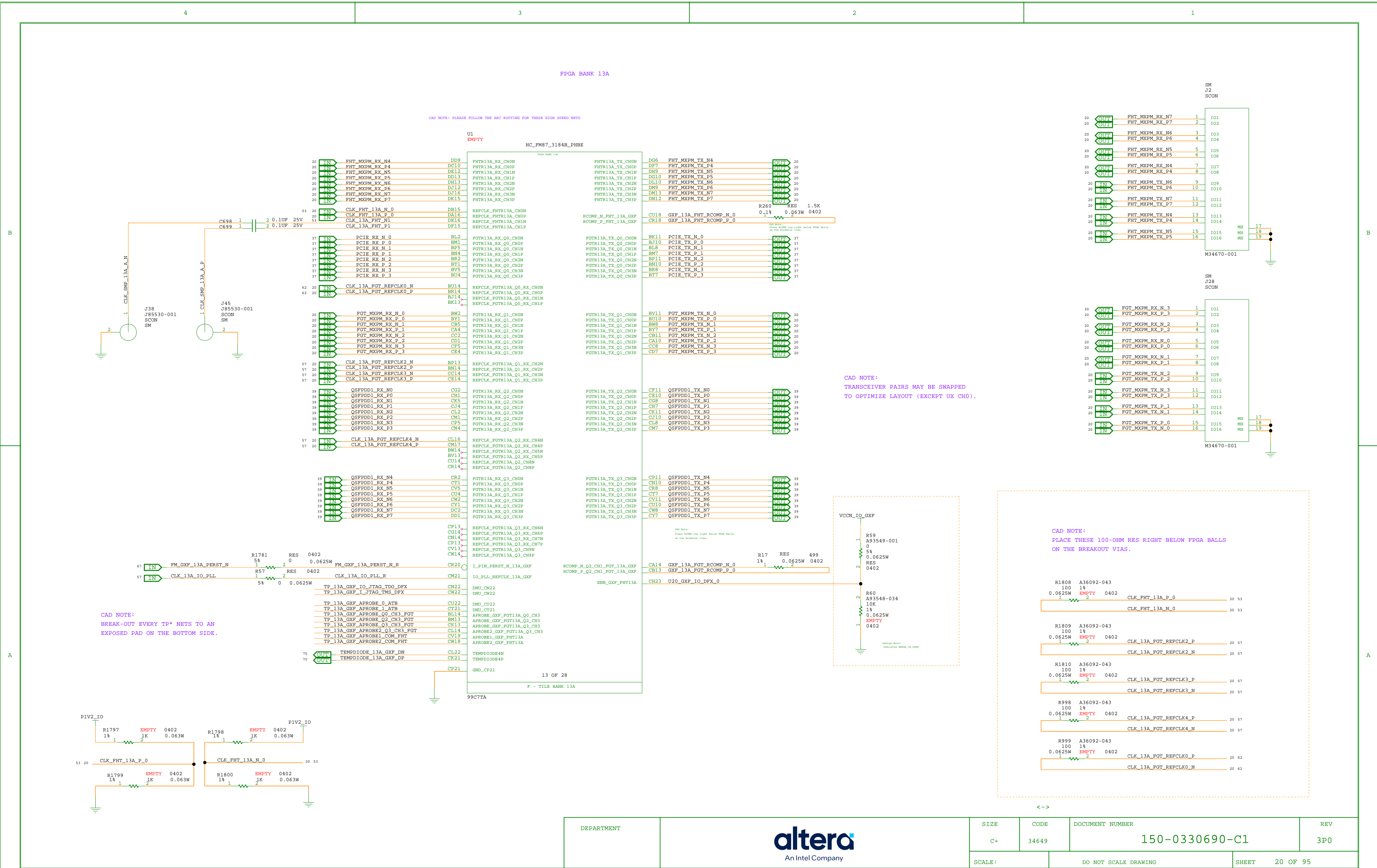
FPGA BANK 12A

CAD NOTE: PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS

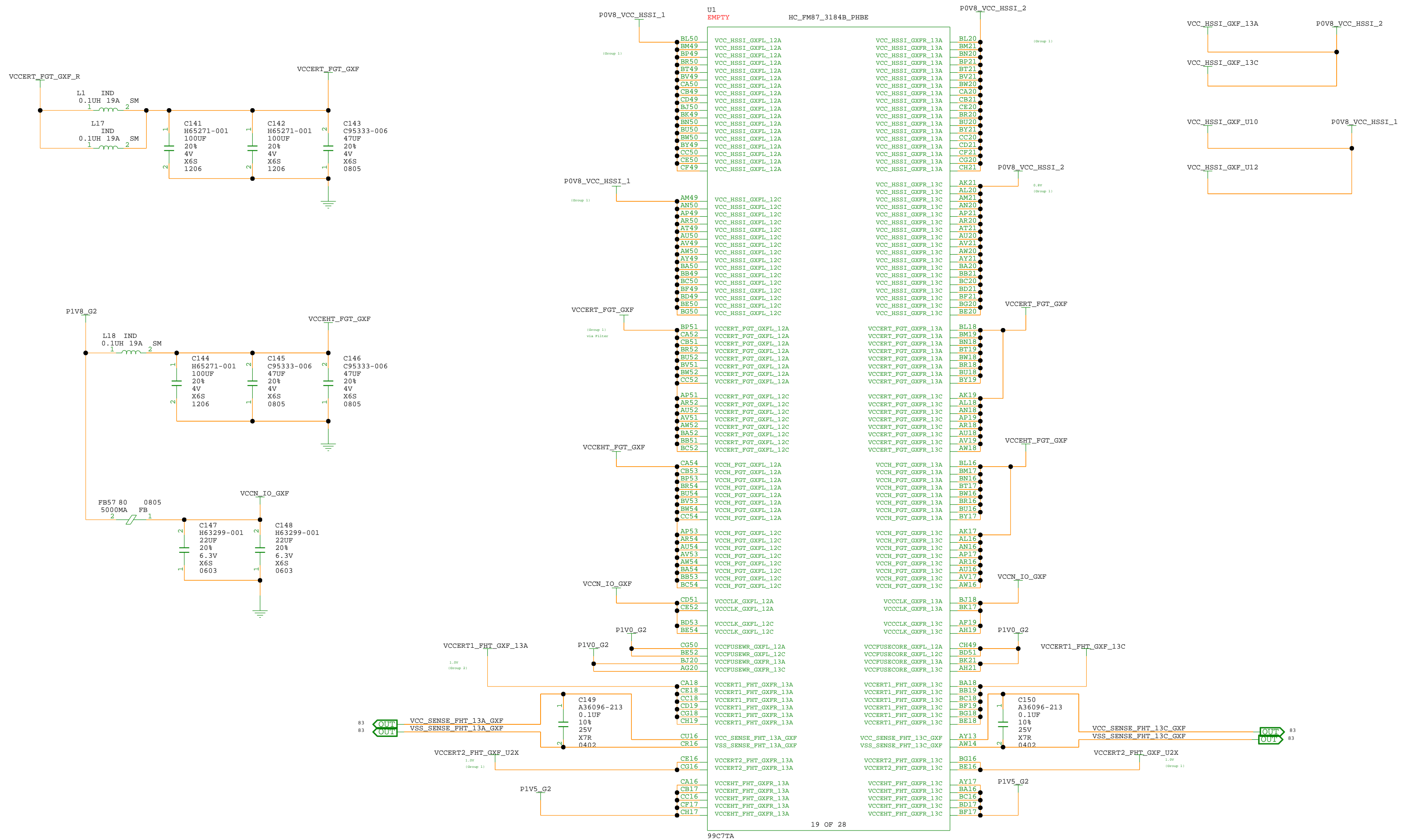
FMC_B_TX*



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99C7TA

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DEPARTMENT

altera
An Intel Company

SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-C1

REV

3P0

SCALE:

DO NOT SCALE DRAWING

SHEET

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B

B

A

A

FPGA GND- I

<->

DEPARTMENT

altera
An Intel Company

SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-C1

REV

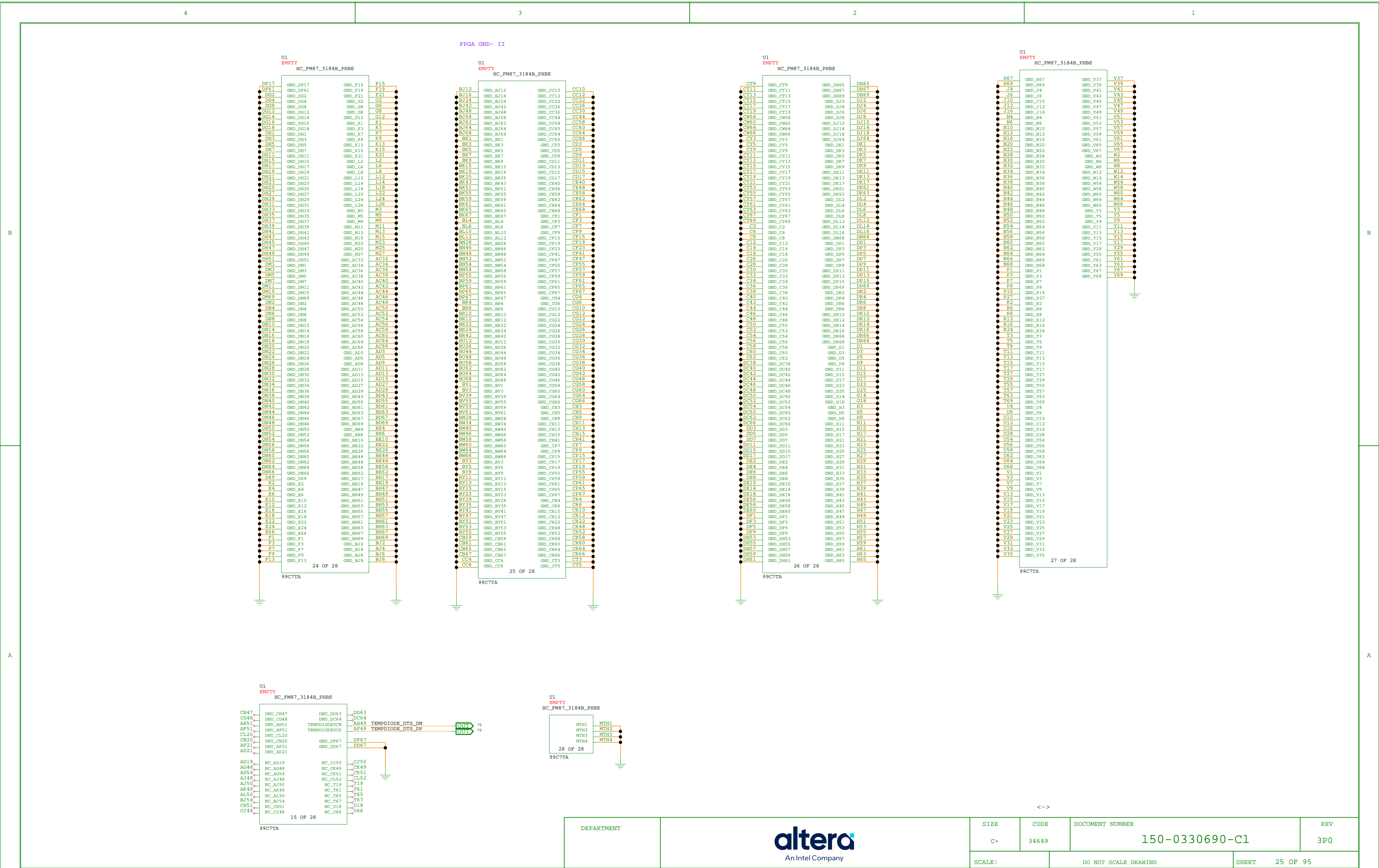
3P0

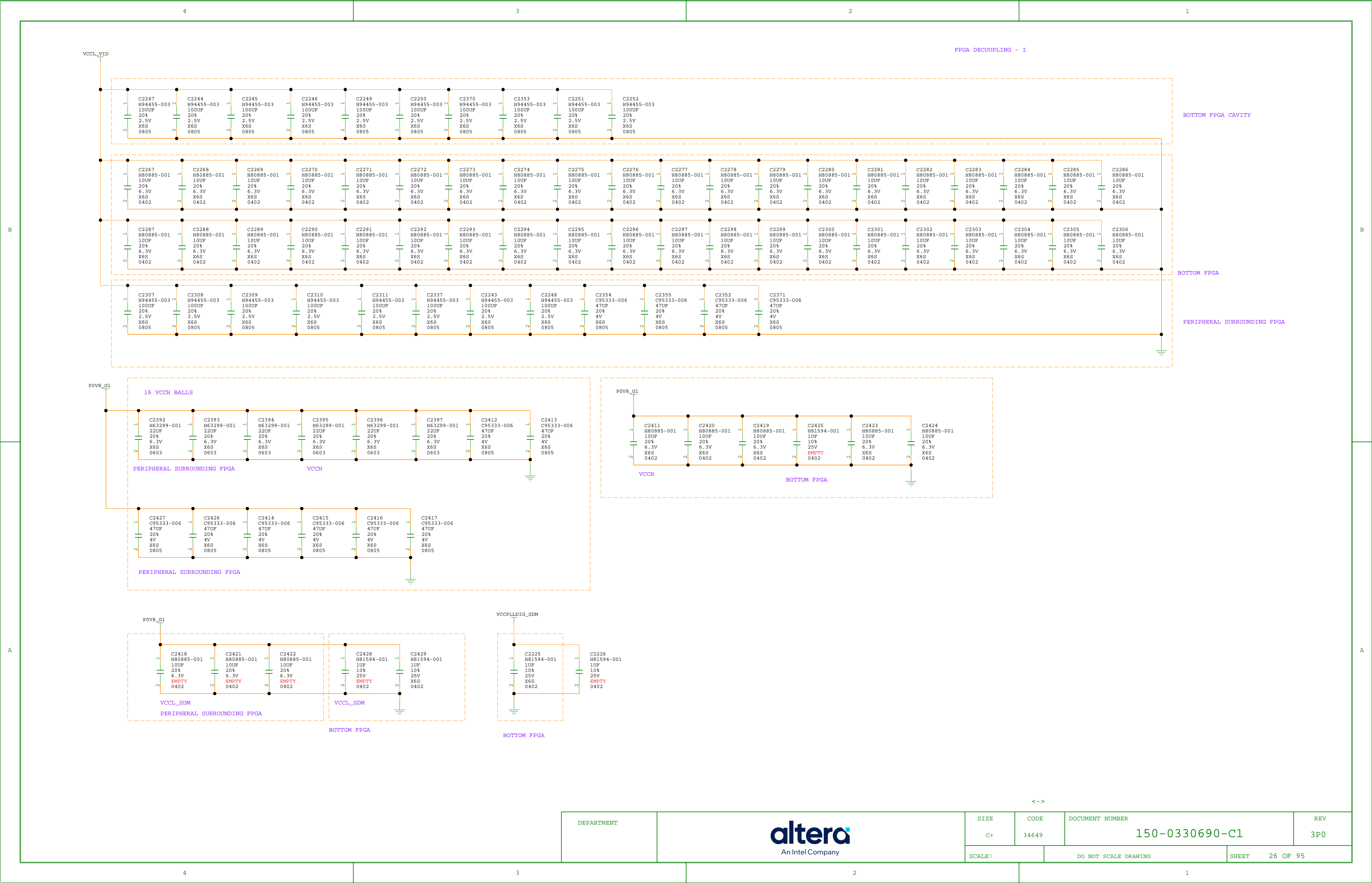
SCALE :


DO NOT SCALE DRAWING

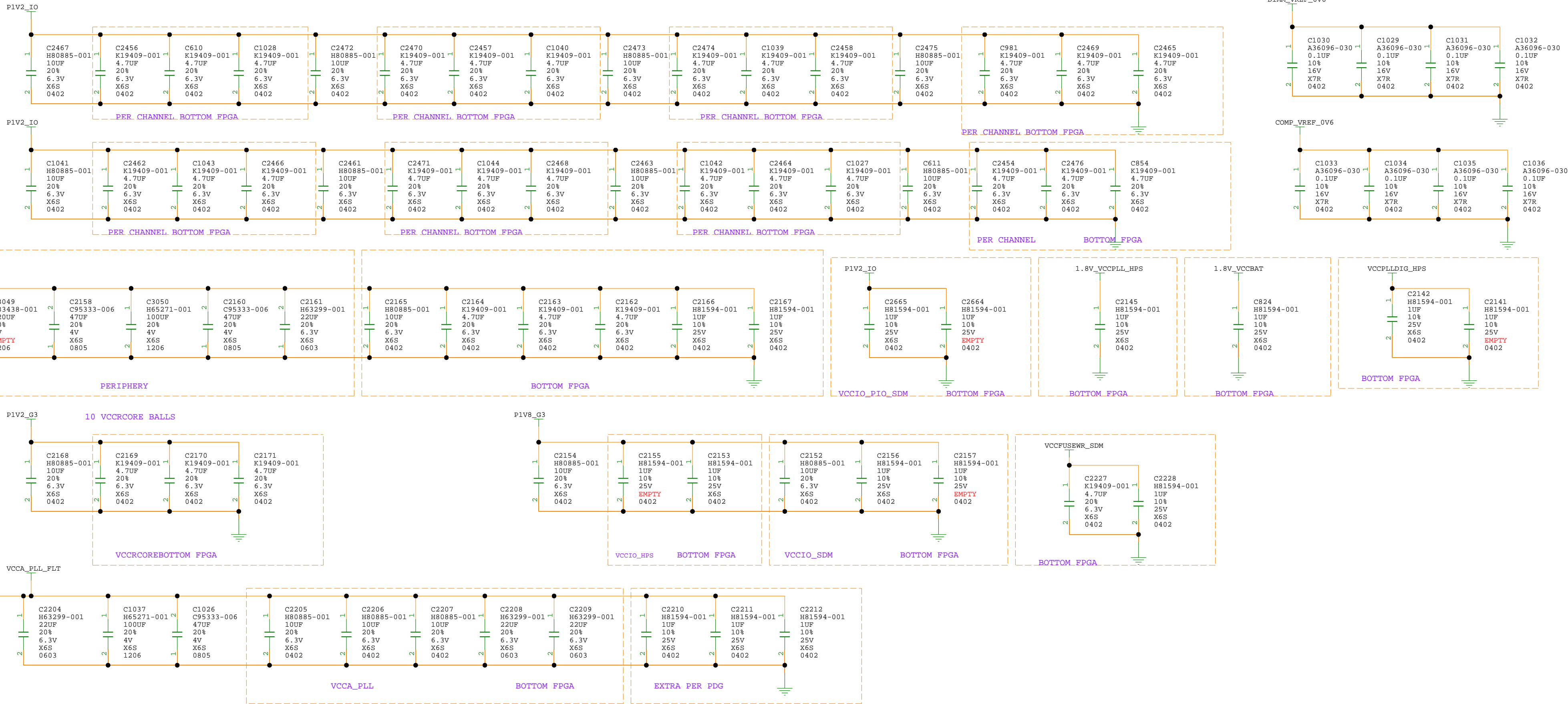
SHEET

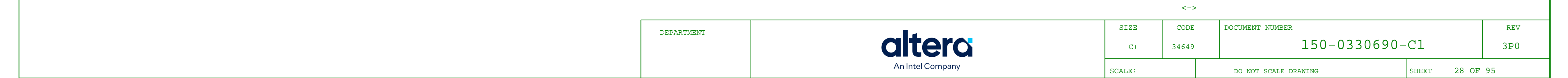
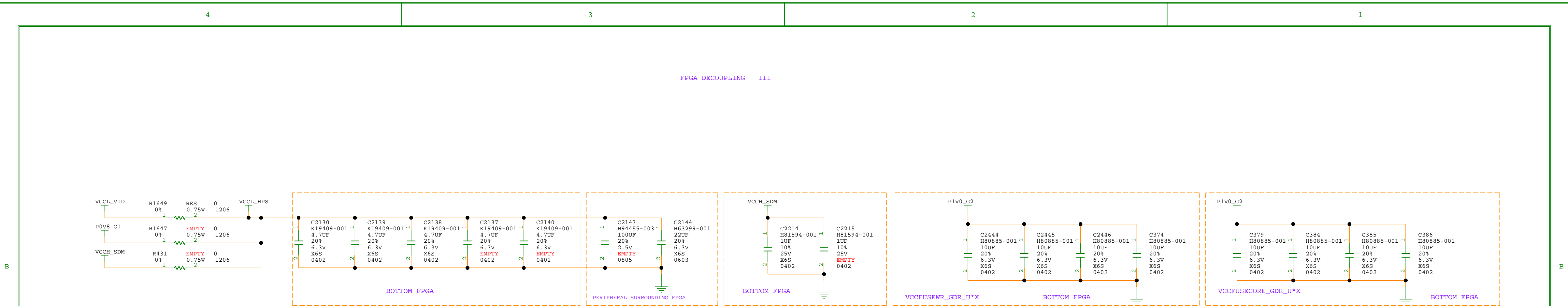
24 OF 95



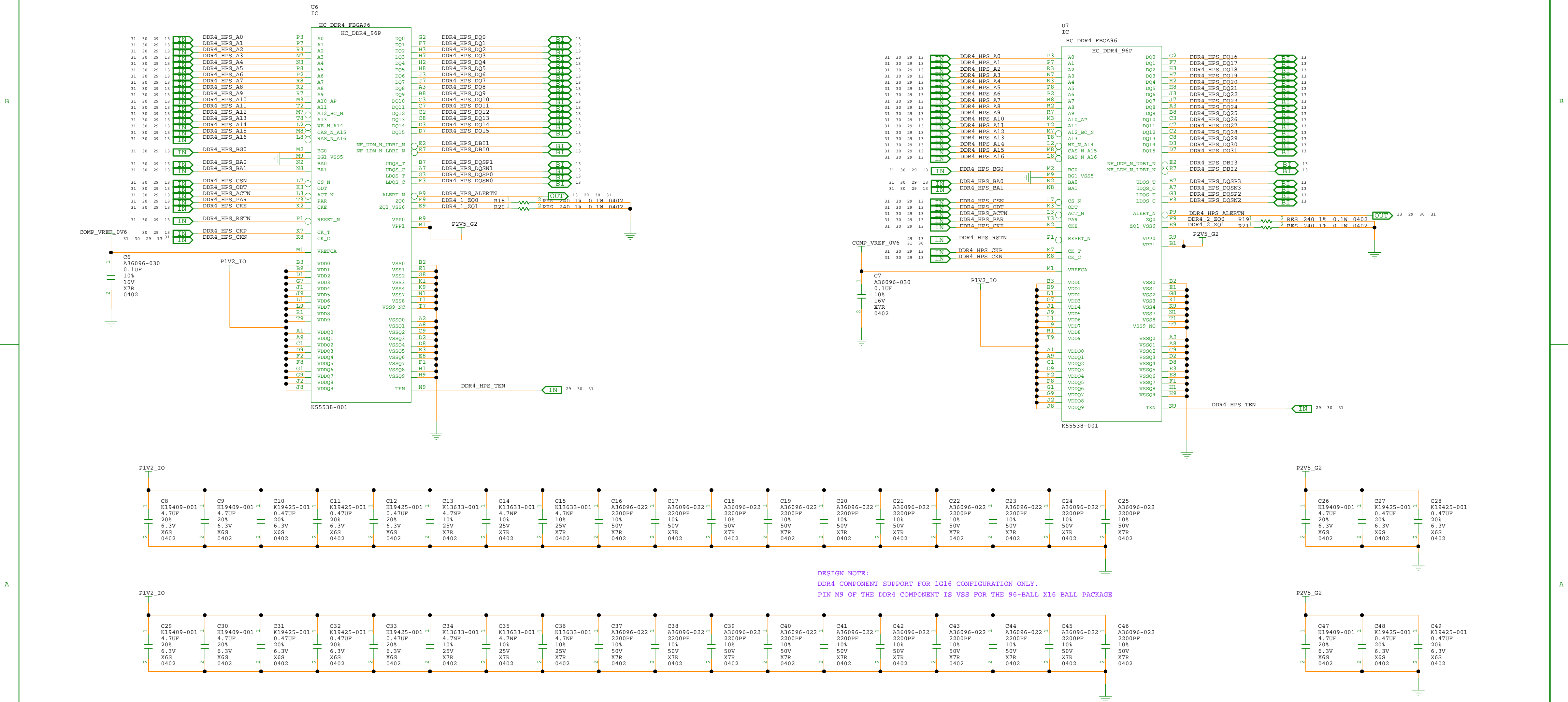


DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330690-C1	3P0
		SCALE:	DO NOT SCALE DRAWING		SHEET 26 OF 95





DDR4 COMPONENT-1



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DEPARTMENT

altera
An Intel Company

SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-C1

REV

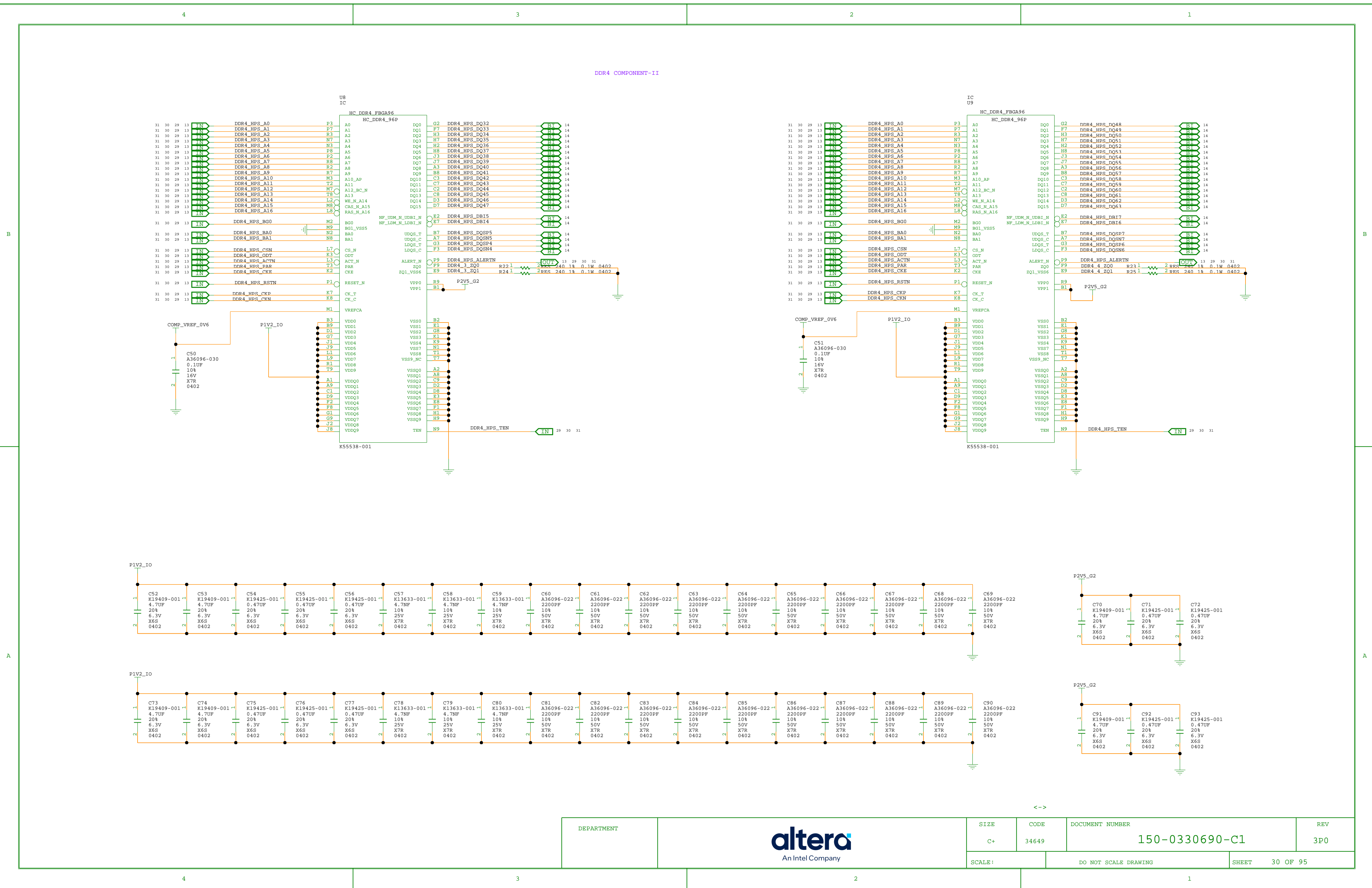
3P0

SCALE:

DO NOT SCALE DRAWING

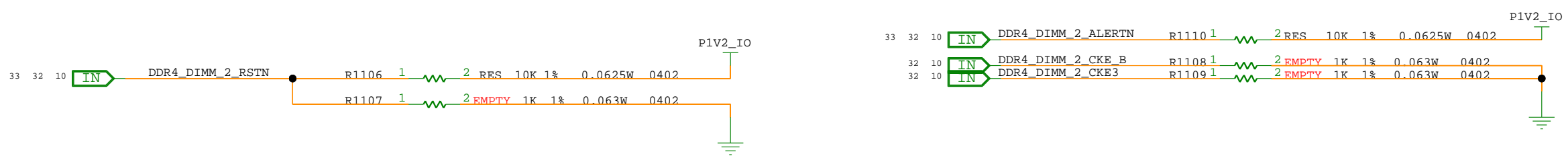
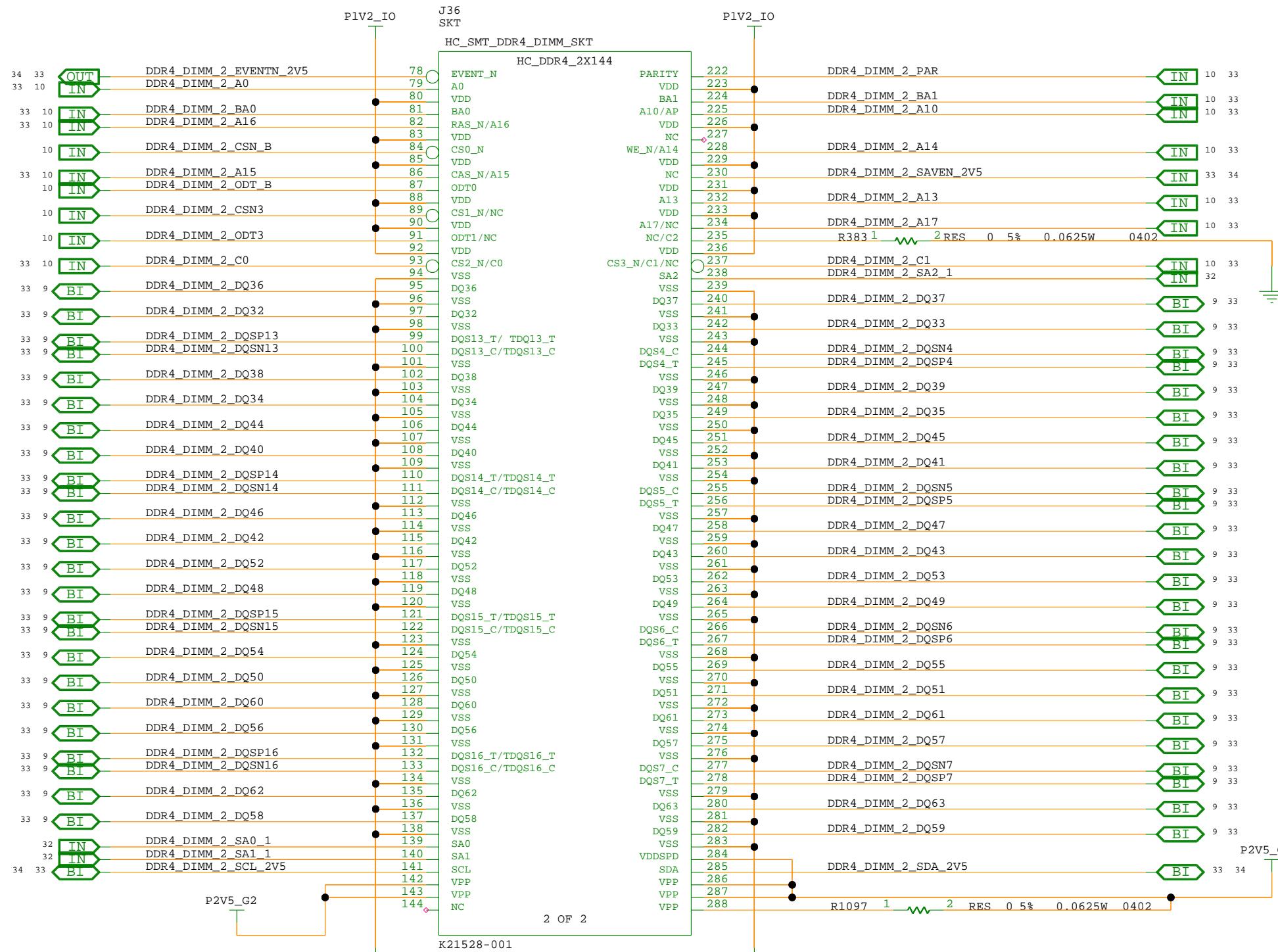
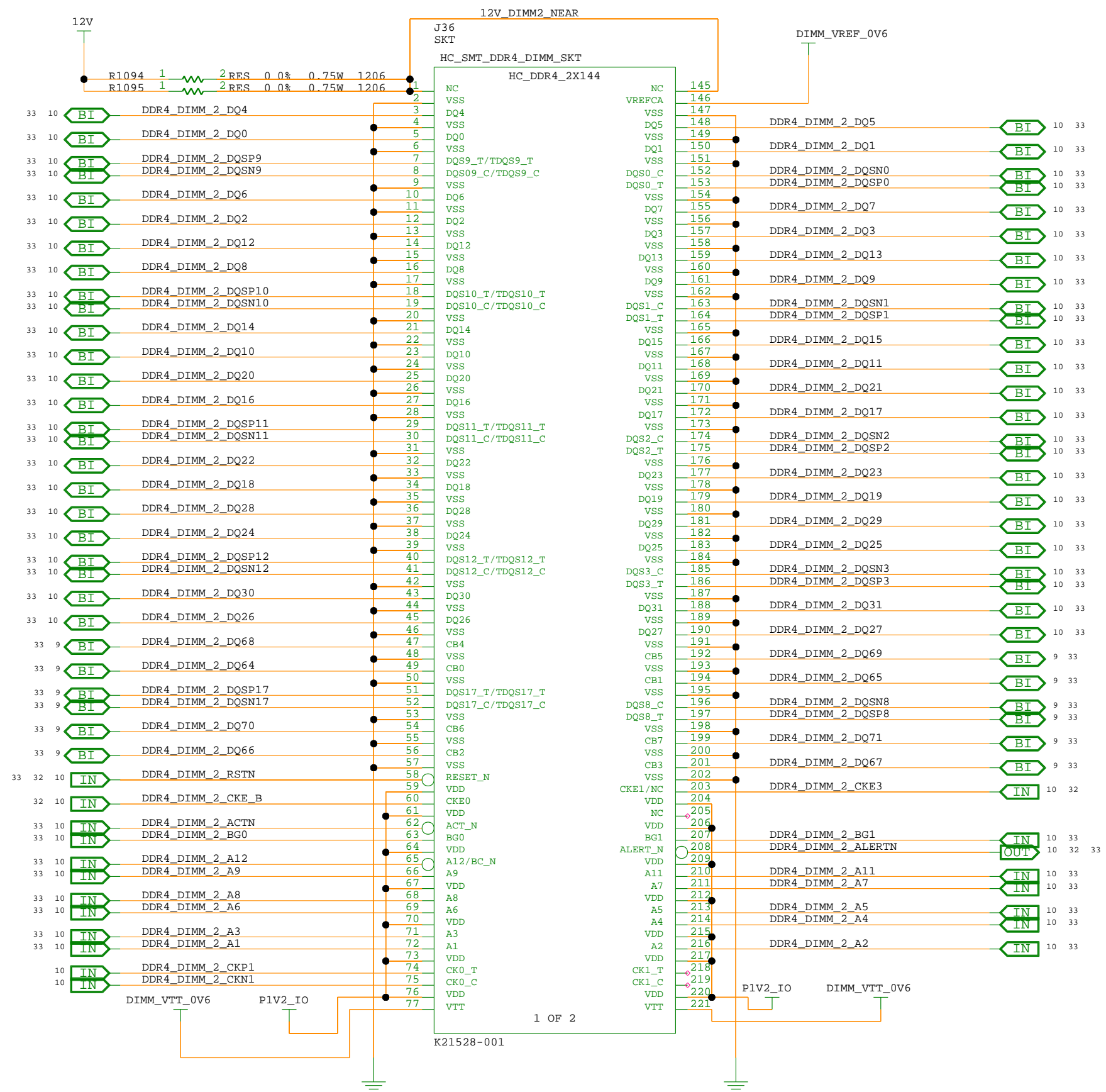
SHEET

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2DPC DIMM-I



SIMULATION BASED ON

MTA18ASF2G72PZ-3G2E2	16GB	SRX4	DDR4-3200
MTA36ASF4G72PZ-2G6E1	32GB	DRX4	DDR4-2666



SIZE

C+

34649

DOCUMENT NUMBER

150-0330690-C1

REV

3P0

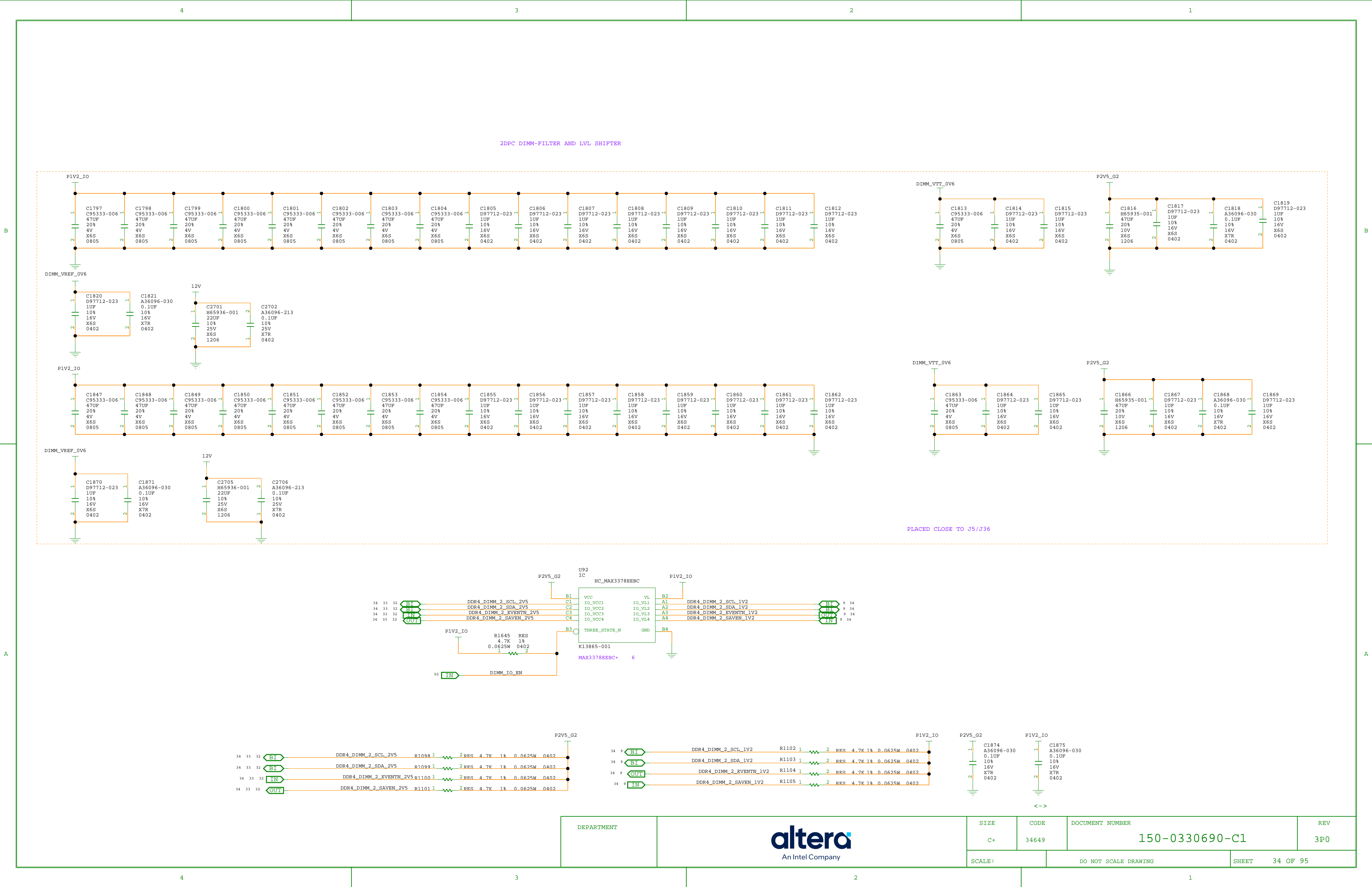
SCALE :

DO NOT SCALE DRAWING

SHEET

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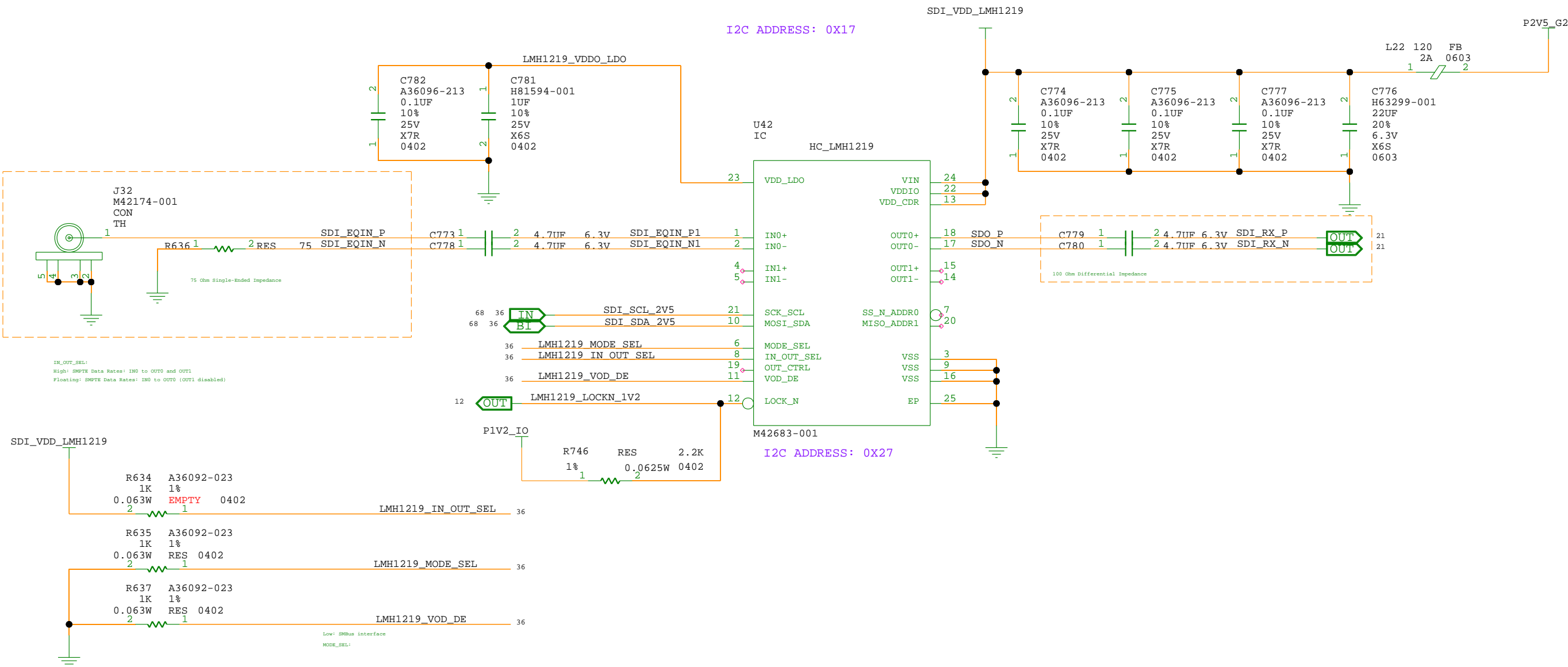
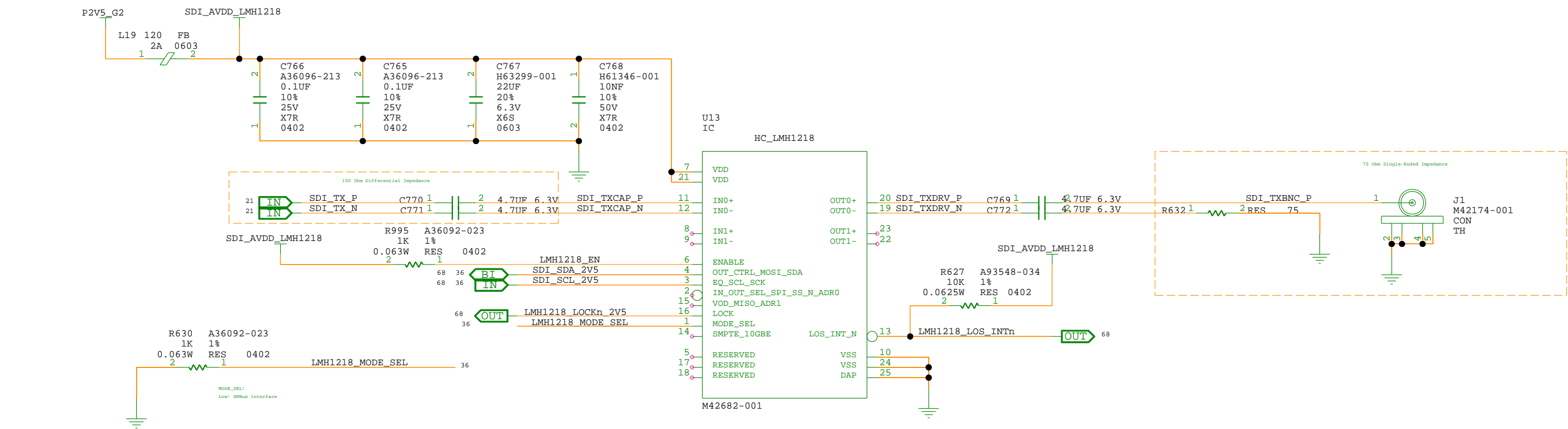


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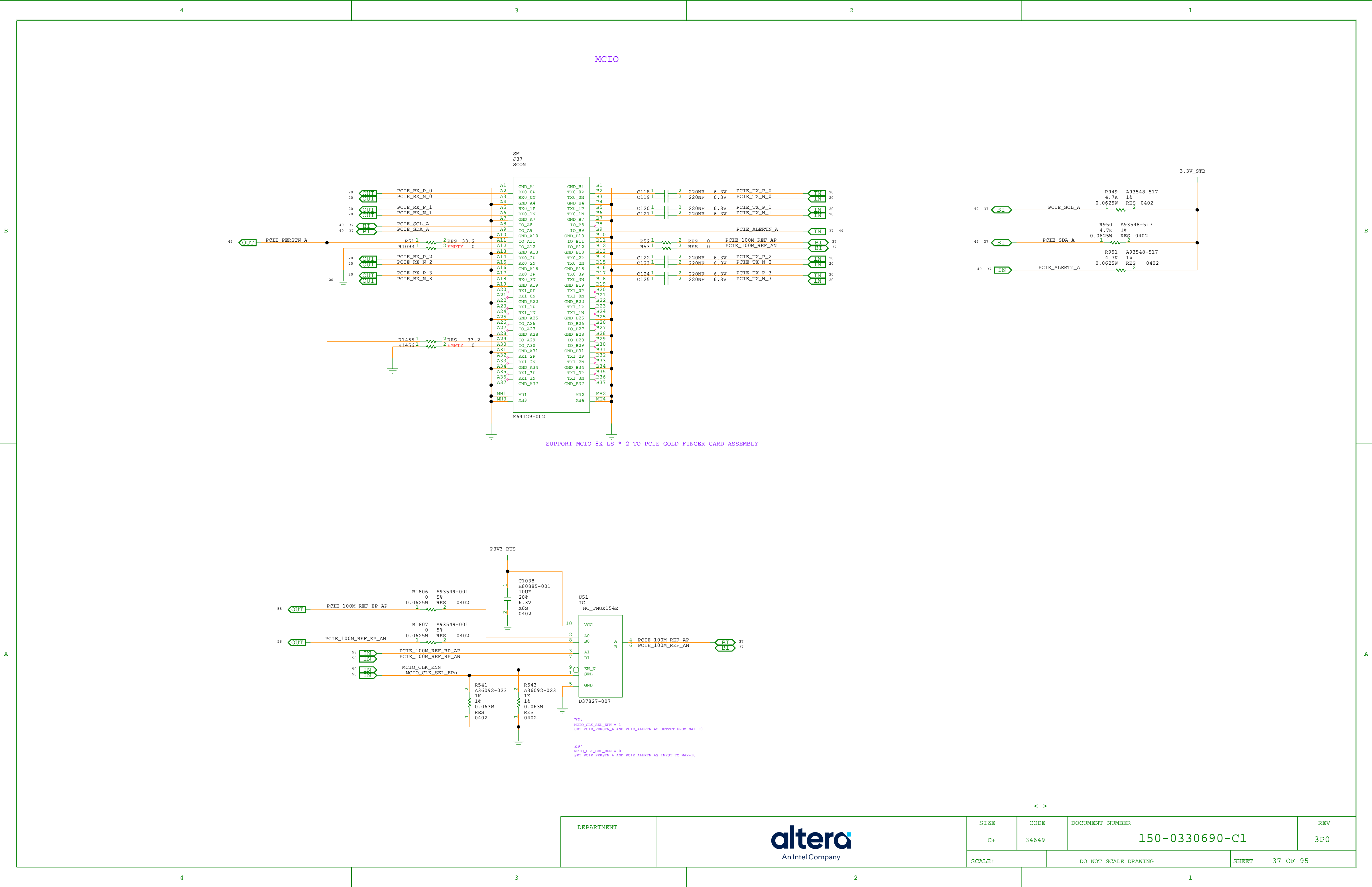
35 OF 95

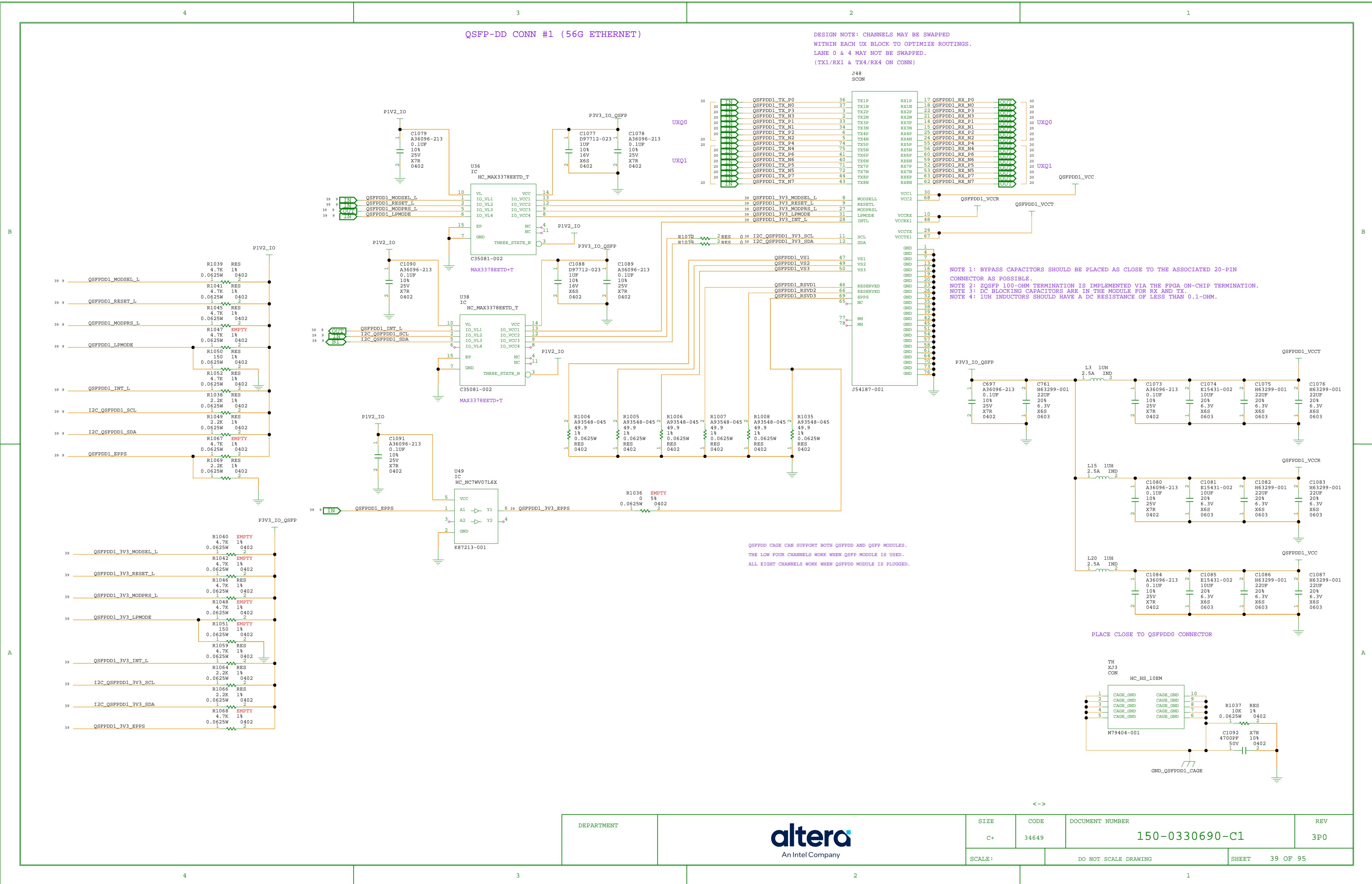
SDI CABLE DRIVER, EQUALIZER, BNC



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DEPARTMENT	 An Intel Company	SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330690-C1	REV 3P0
SCALE:		DO NOT SCALE DRAWING			SHEET 36 OF 95



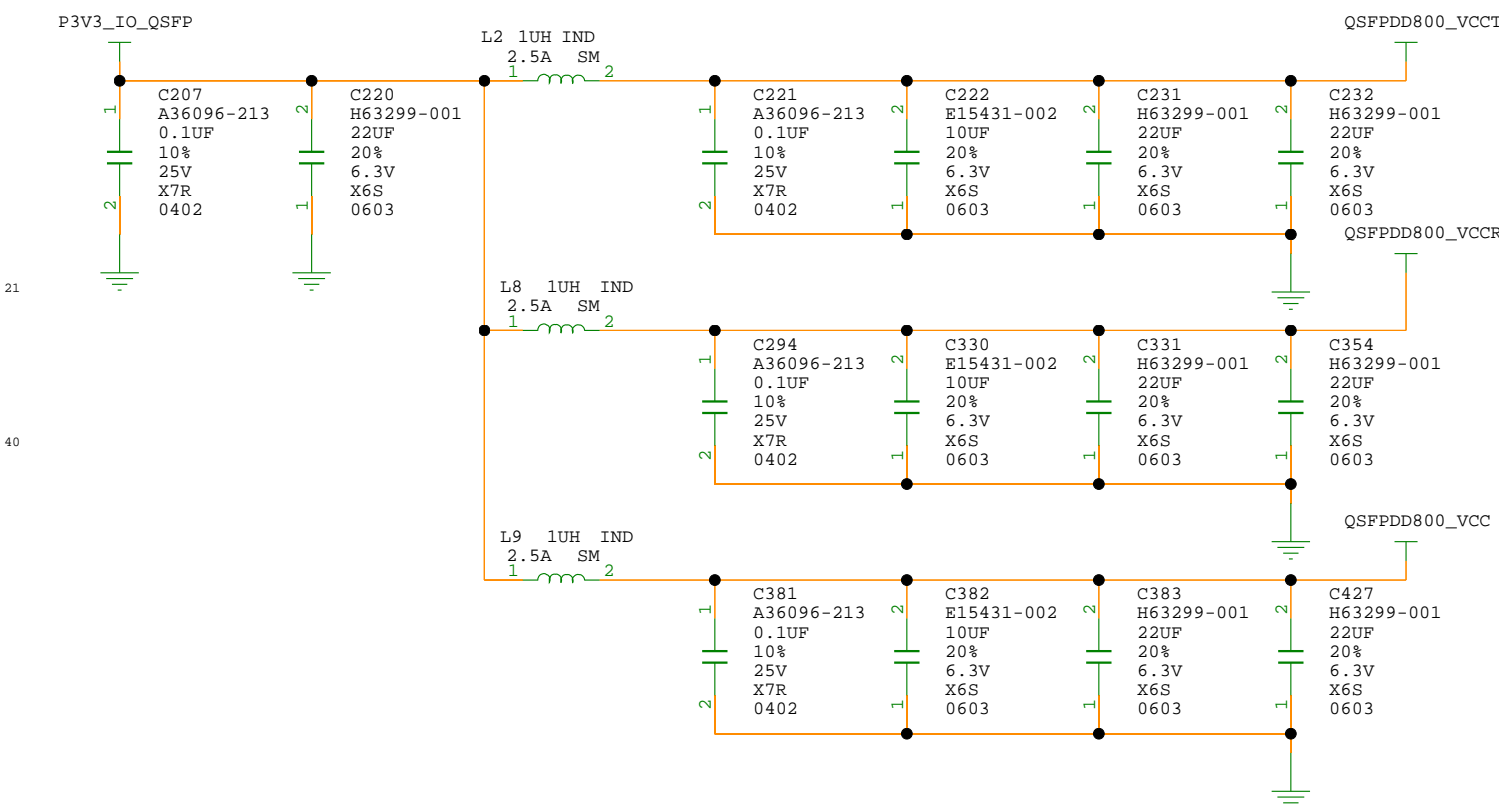


QSFP-DD-800 CONN (112G ETHERNET)

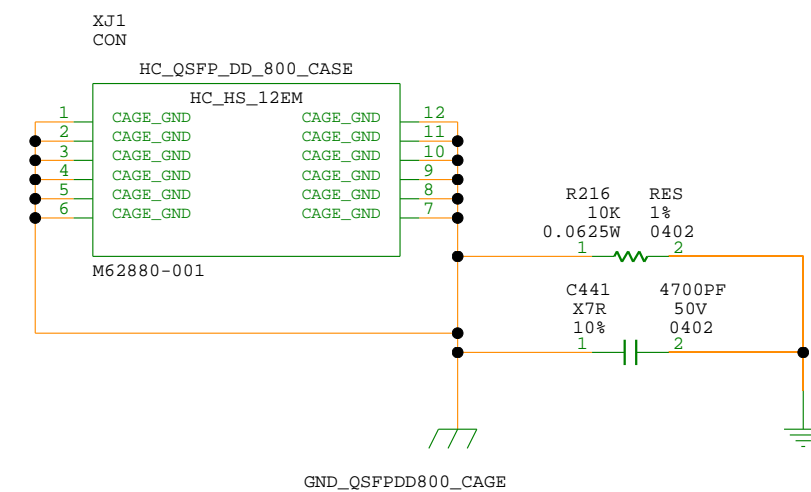
CAD NOTE: PLEASE FOLLOW THE ARC ROUTING FOR THESE HIGH SPEED NETS.

DESIGN NOTE: CHANNELS MAY BE SWAPPED
WITHIN EACH BK BLOCK TO OPTIMIZE ROUTINGS.
SWAP BOTH TX & RX TOGETHER.

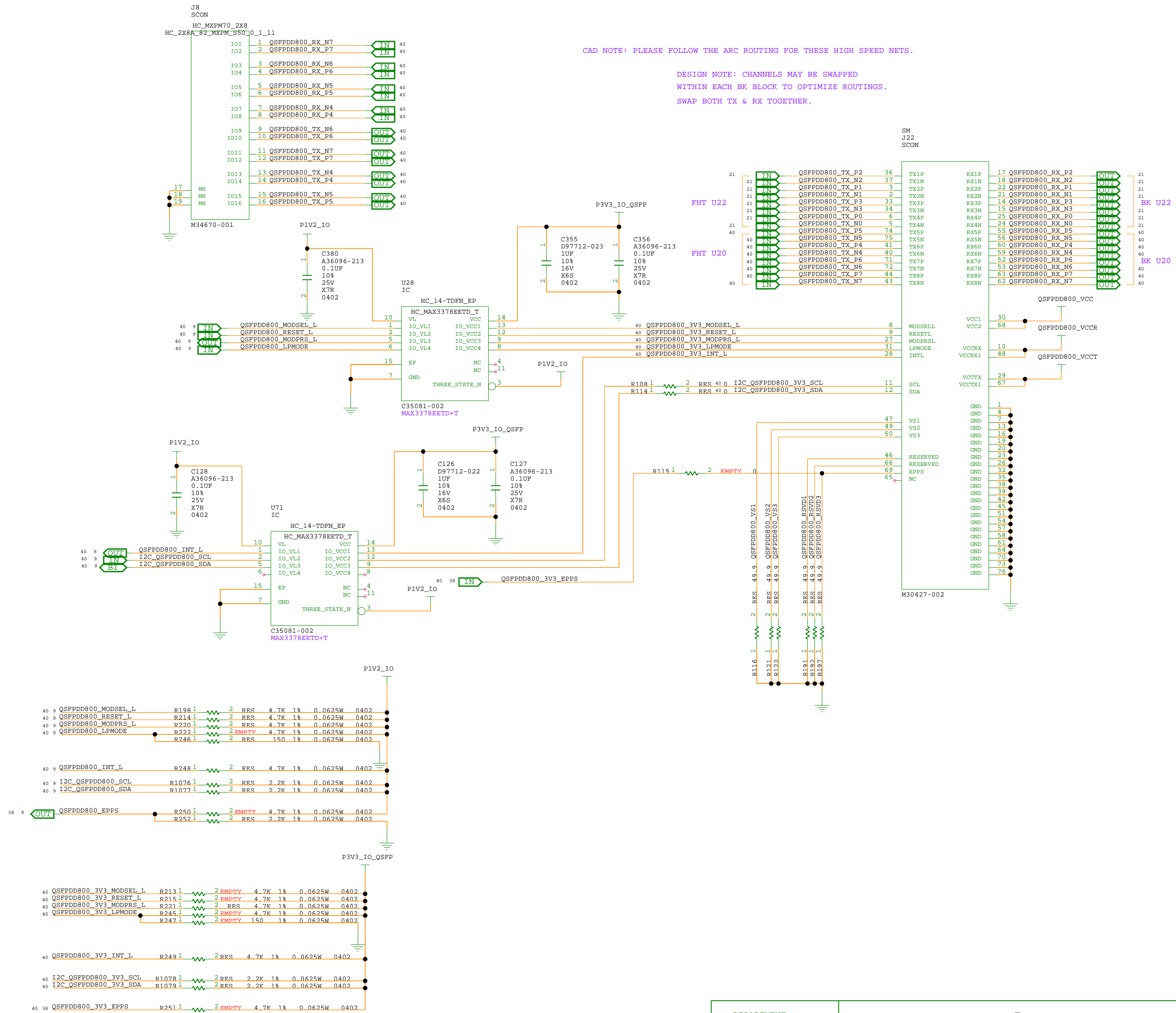
NOTE 4: 1UH INDUCTORS SHOULD HAVE A DC RESISTANCE OF LESS THAN 0.1-OHM.
NOTE 2: ZQSFP 100-OHM TERMINATION IS IMPLEMENTED VIA THE FPGA ON-CHIP TERMINATION.
NOTE 1: BYPASS CAPACITORS SHOULD BE PLACED AS CLOSE TO THE ASSOCIATED 20-PIN CONNECTOR AS POSSIBLE.
NOTE 3: DC BLOCKING CAPACITORS ARE IN THE MODULE FOR RX AND TX.




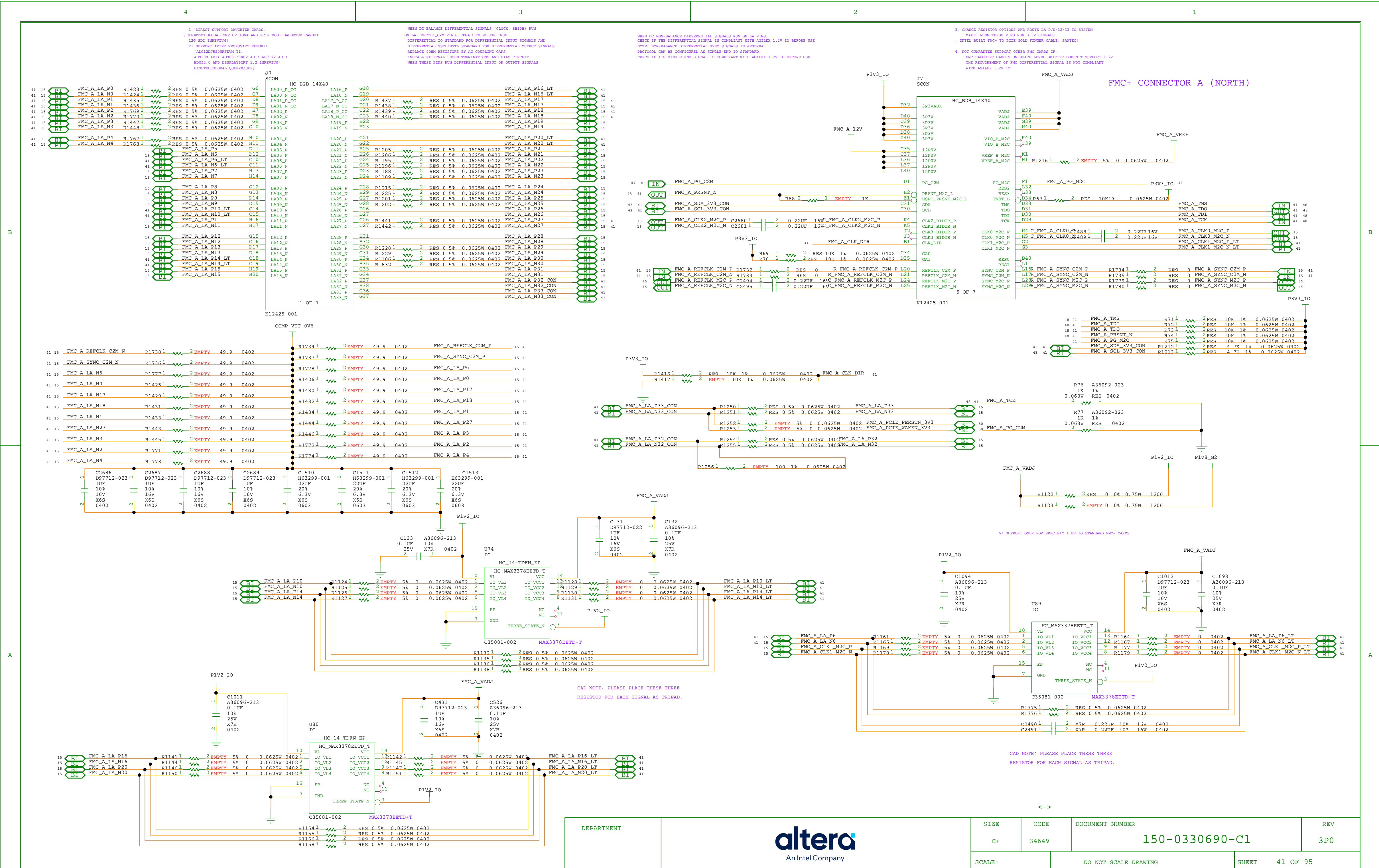
1x1 Cage



PLACE CLOSE TO QSFPDD800 CONNECTOR

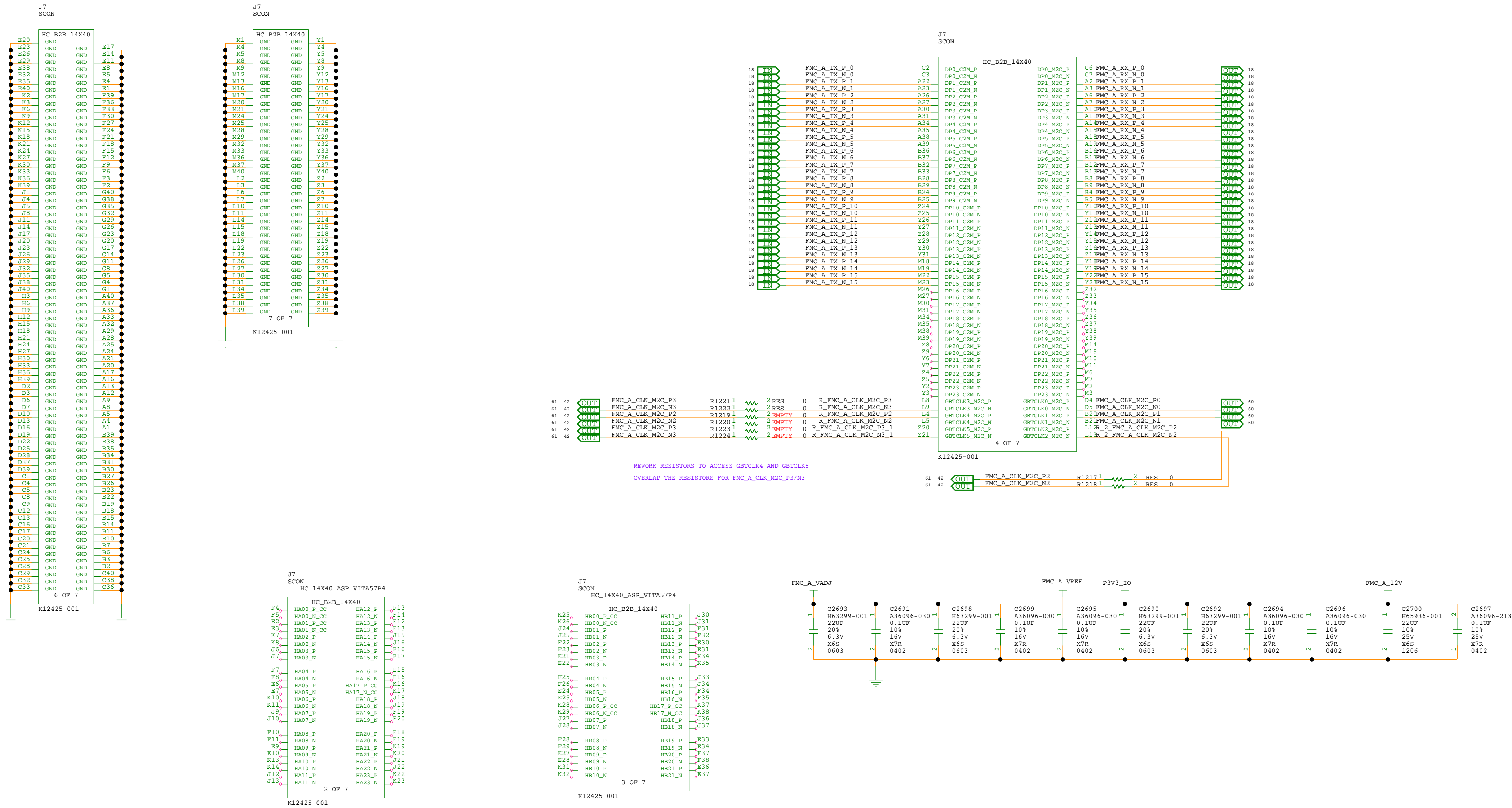


DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330690-C1	3P0
		SCALE :	DO NOT SCALE DRAWING		SHEET 40 OF 95

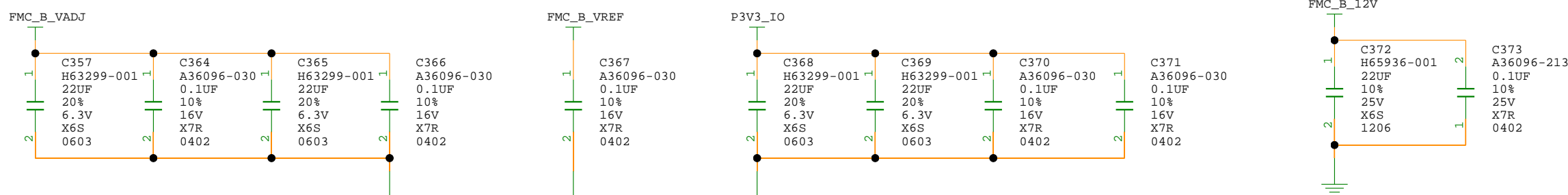
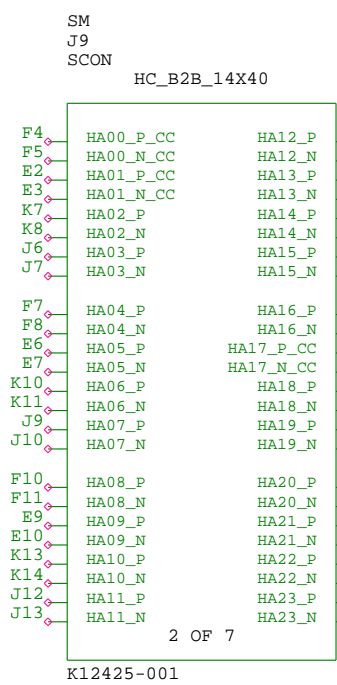
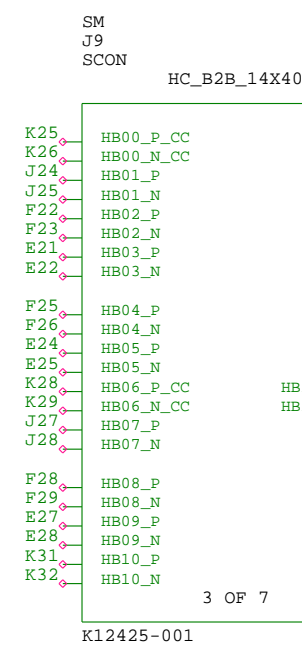
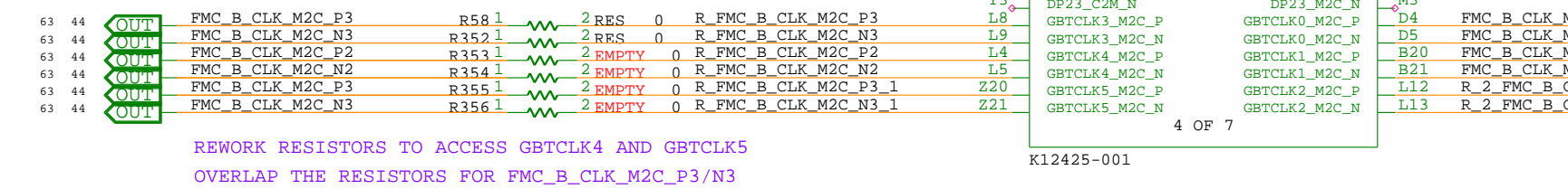
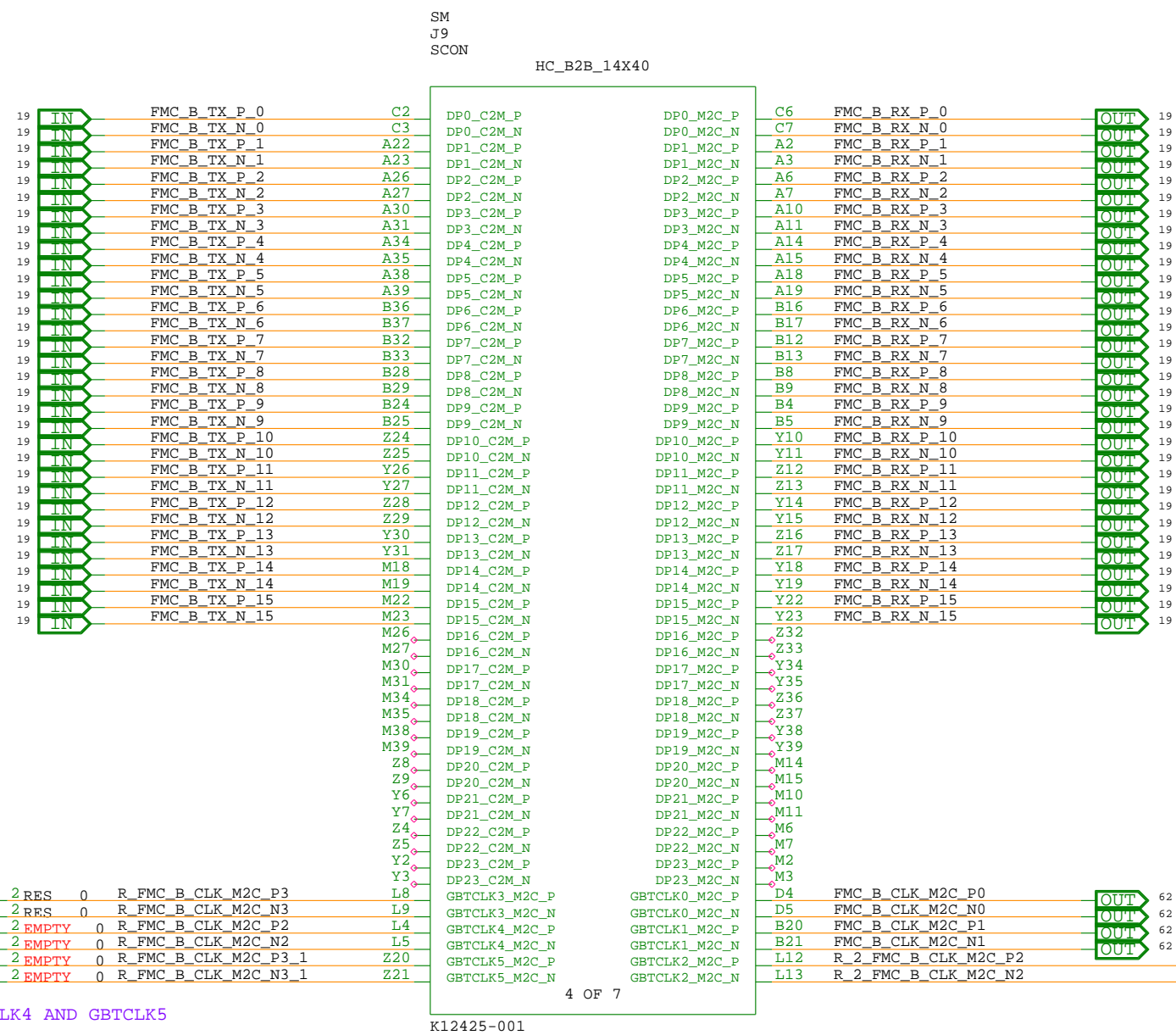
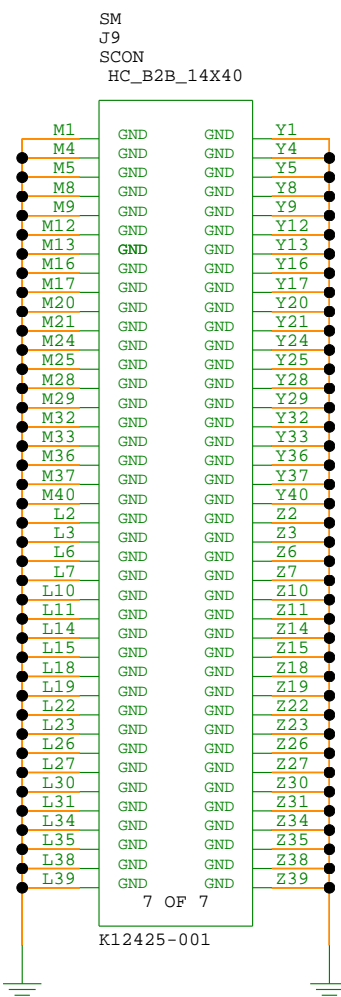
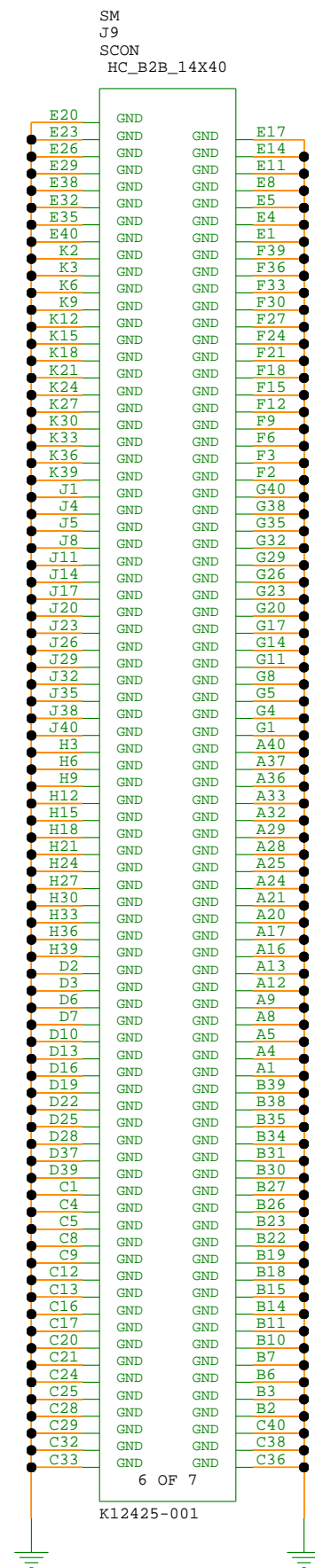


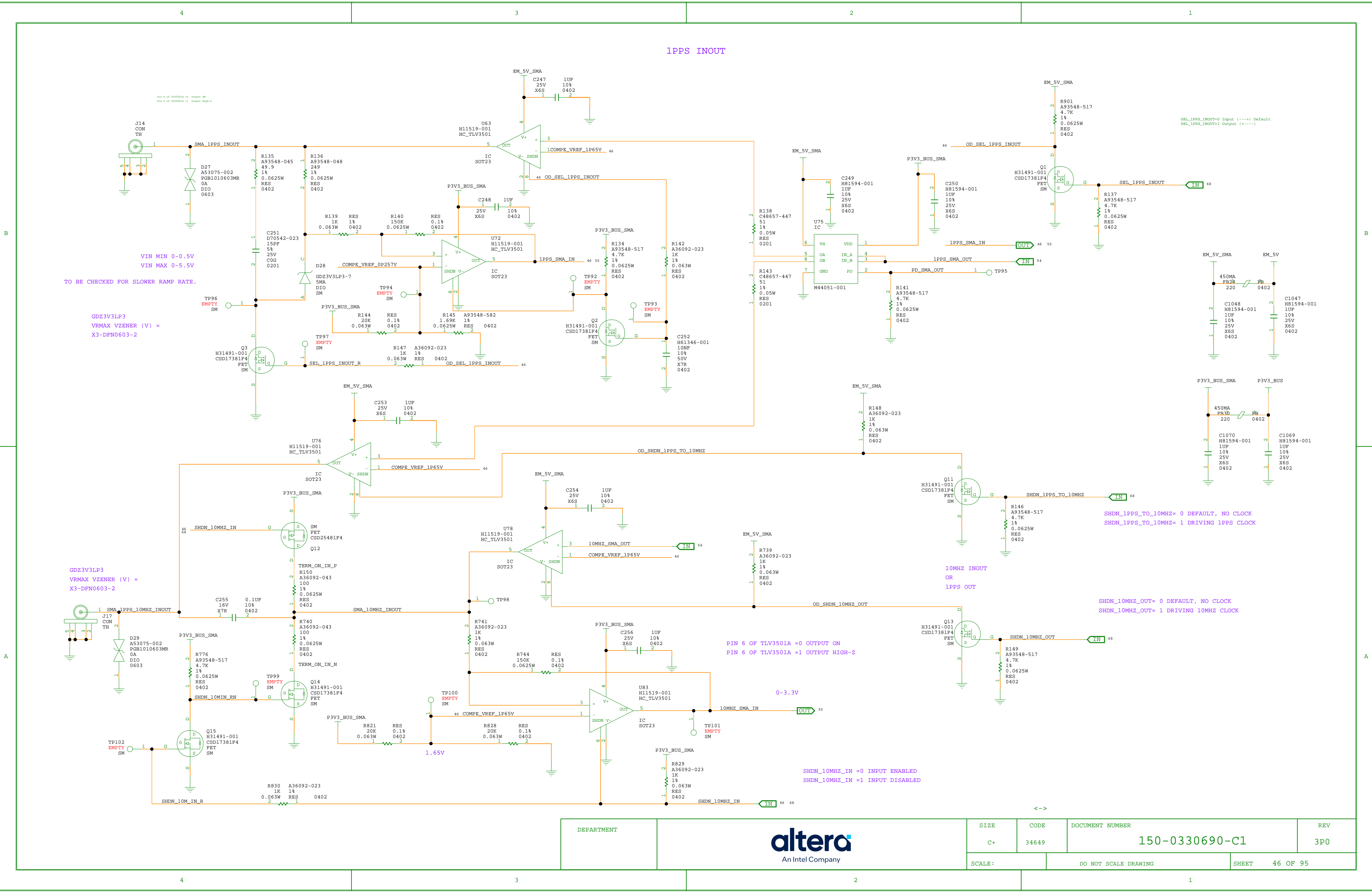
SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330690-C1	REV 3P0
SCALE:	DO NOT SCALE DRAWING	SHEET	41 OF 95

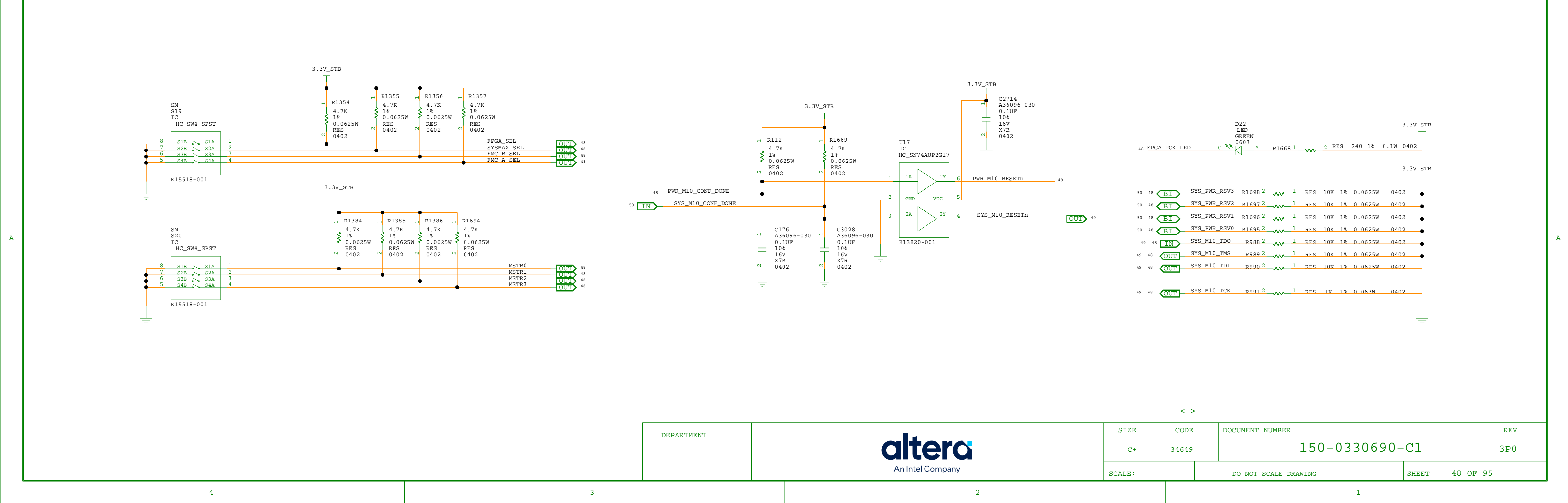
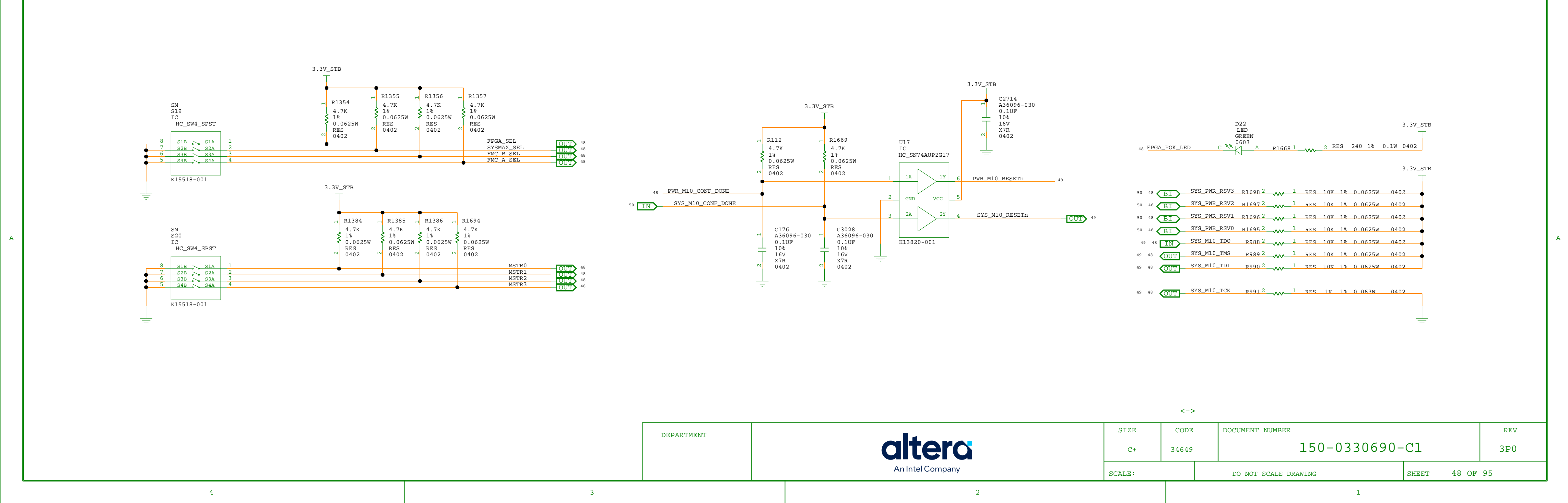
FMC+ CONNECTOR A (NORTH)



FMC+ CONNECTOR B (EAST)

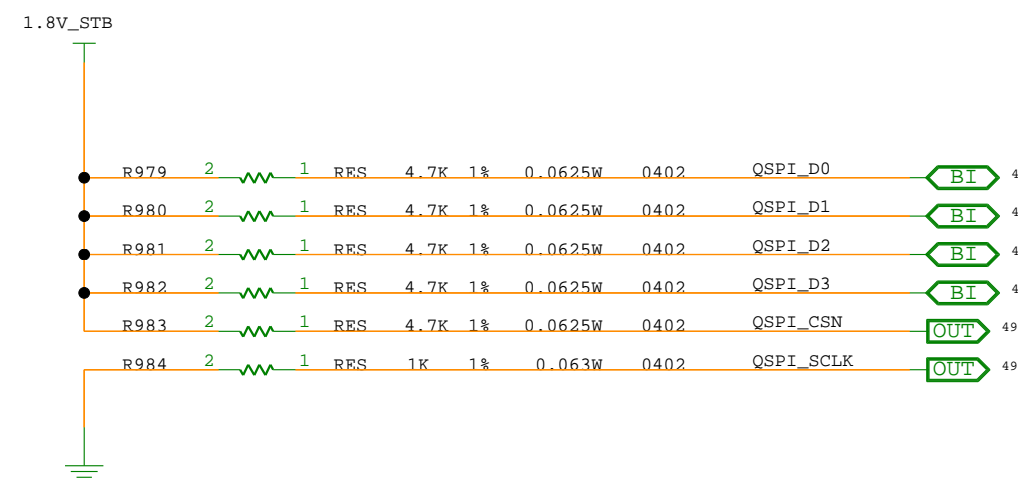
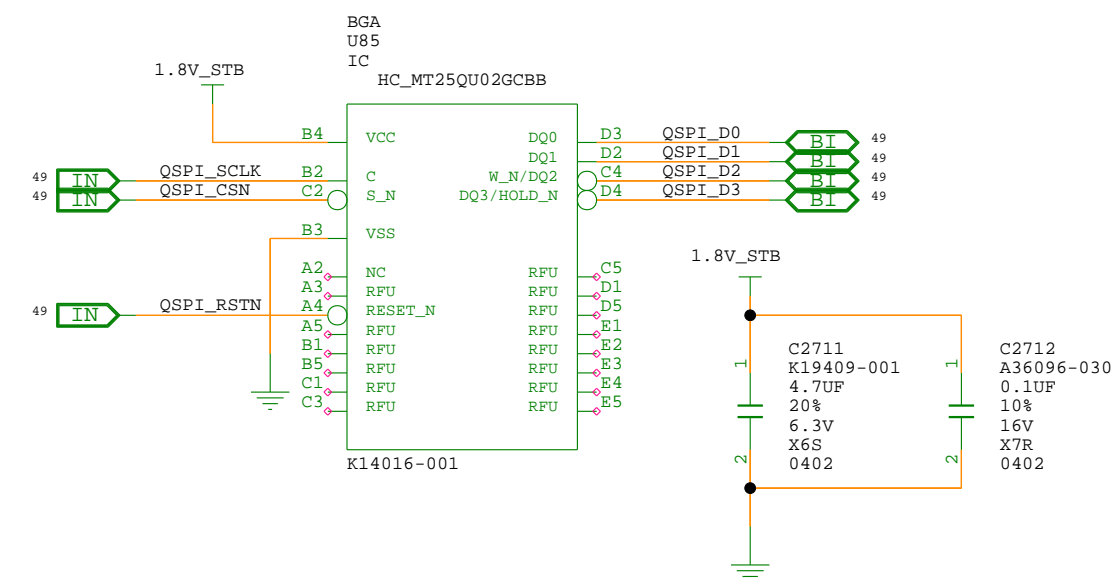
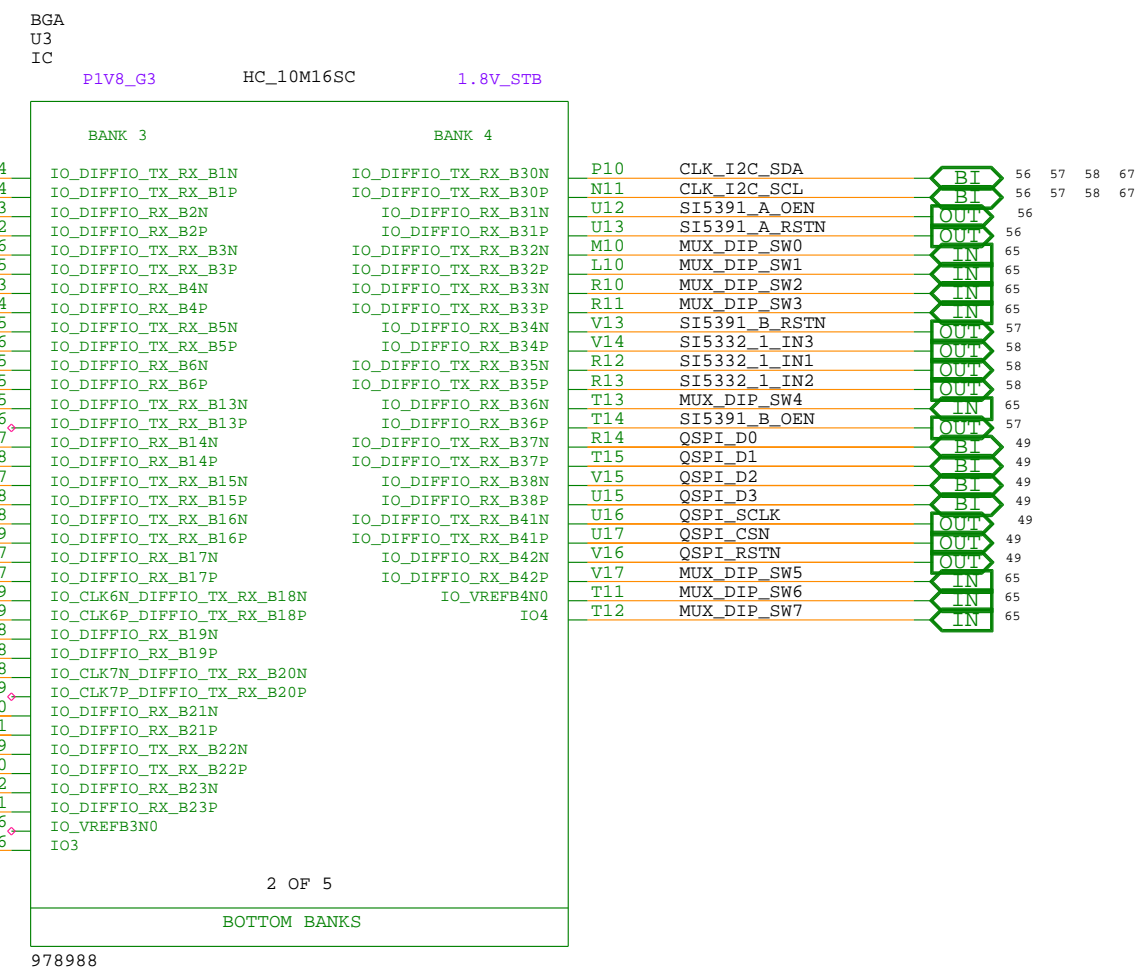
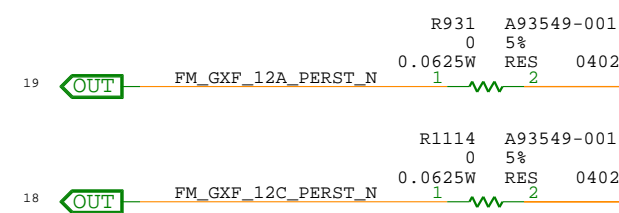
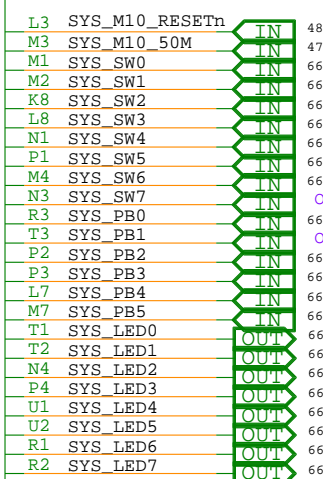









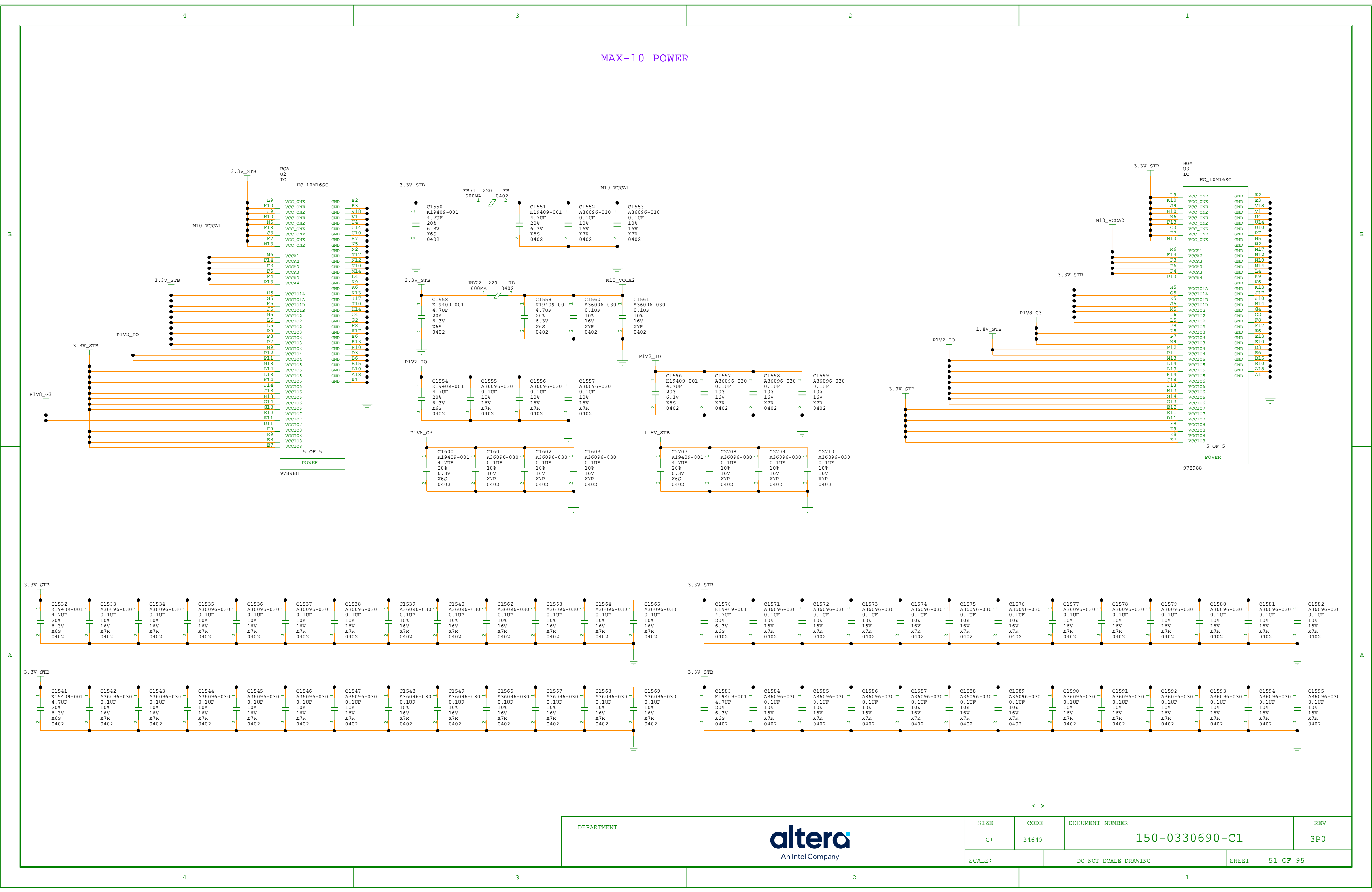
SYS MAX-10- I



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DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330690-C1	3P0
		SCALE:	DO NOT SCALE DRAWING		SHEET 49 OF 95

MAX-10 POWER



DEPARTMENT



SIZE

CODE

DOCUMENT NUMBER

REV

C+

34649

150-0330690-C1

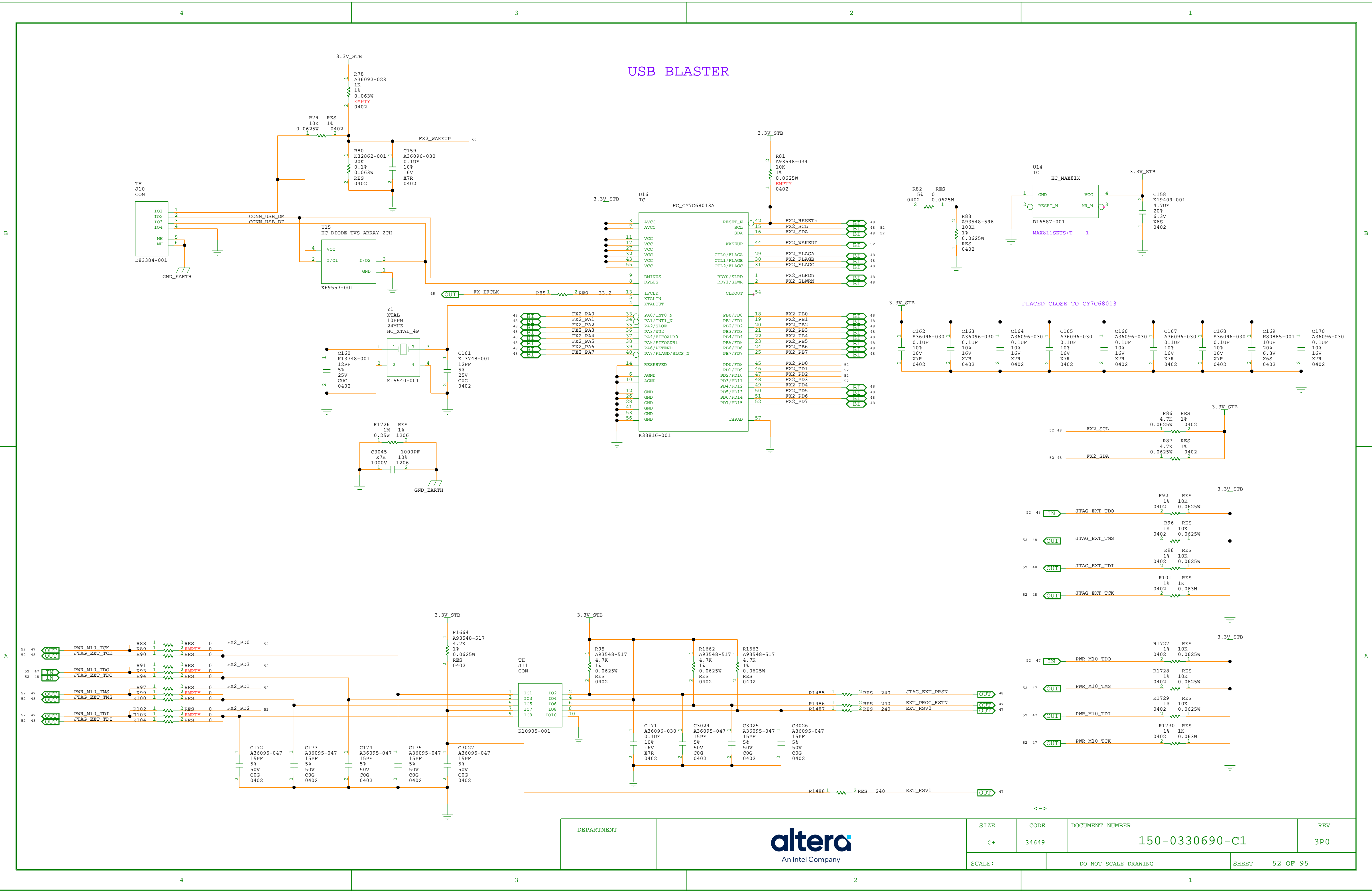
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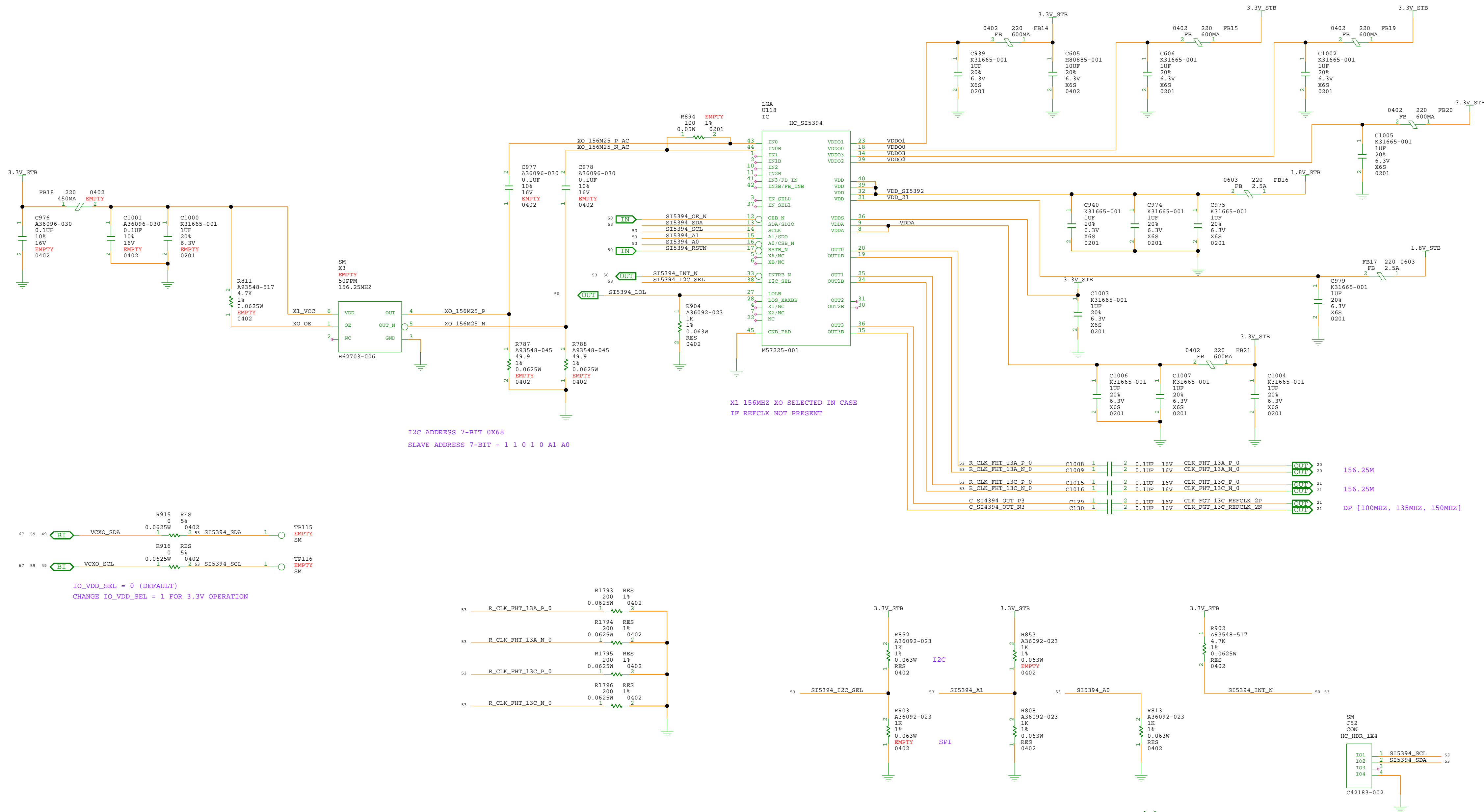
DO NOT SCALE DRAWING


SHEET

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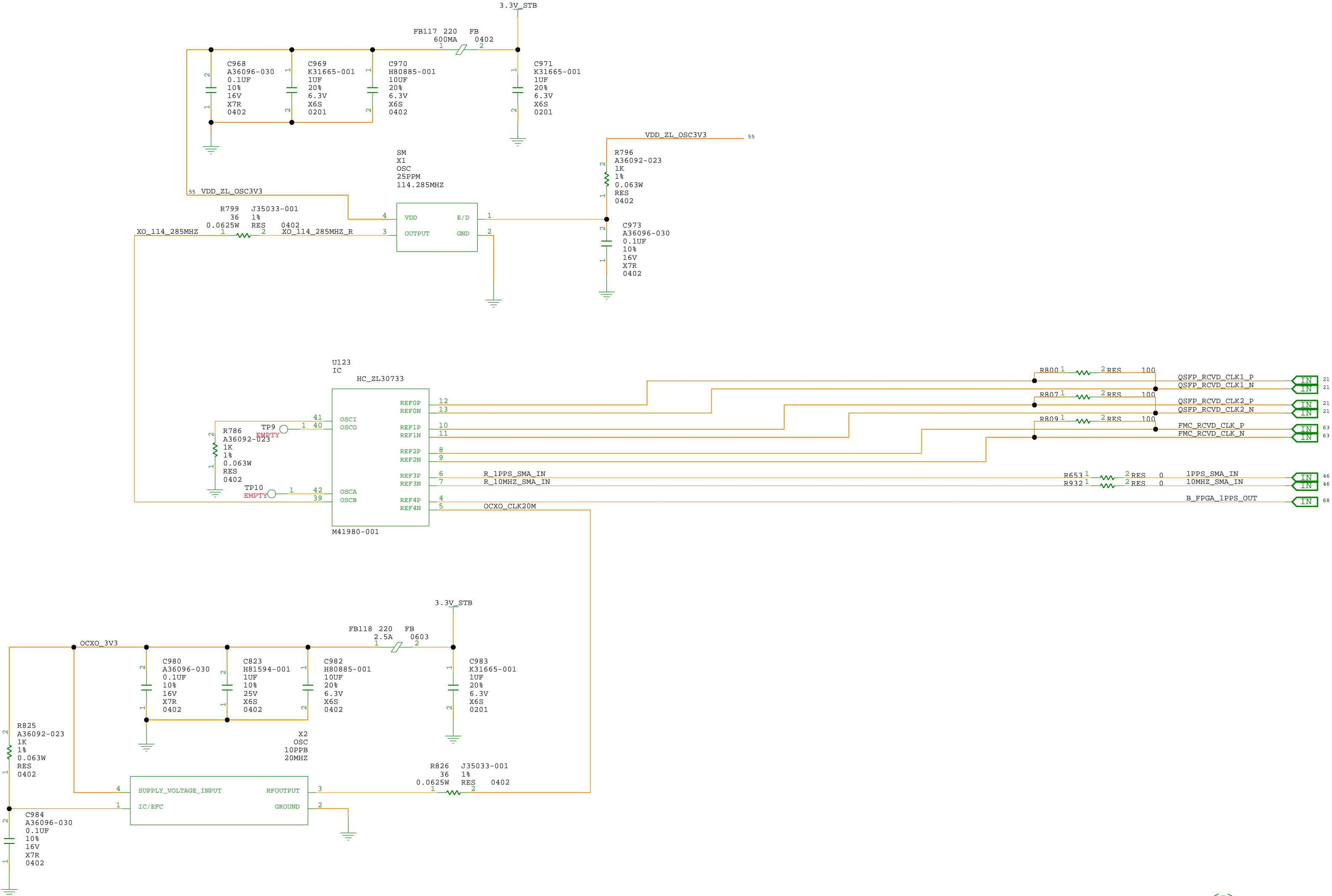


SI5394 CLOCK GENERATOR




DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
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		SCALE:	DO NOT SCALE DRAWING		SHEET 53 OF 95

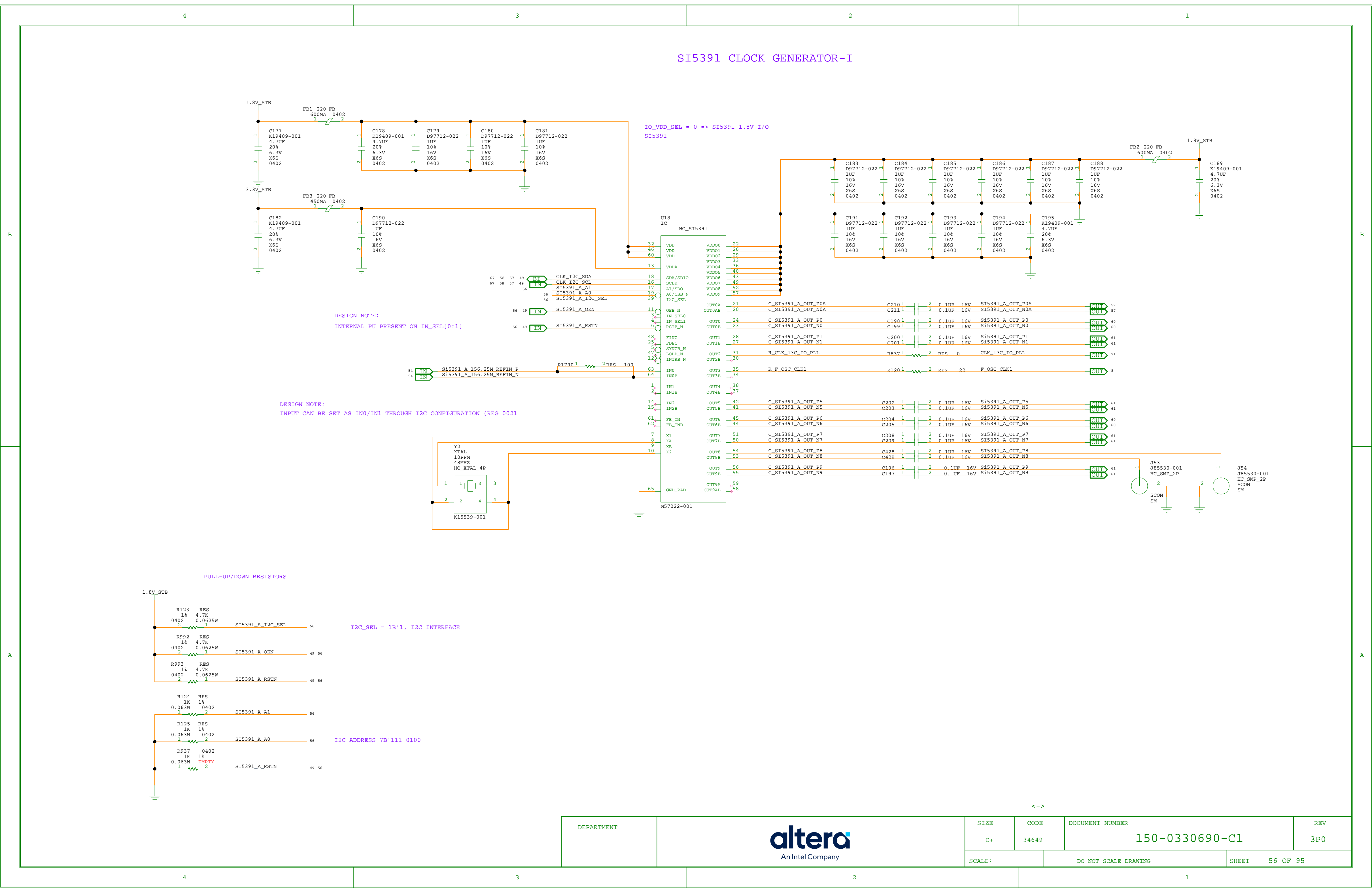
ZL30733 PLL CLOCK GENERATOR-2



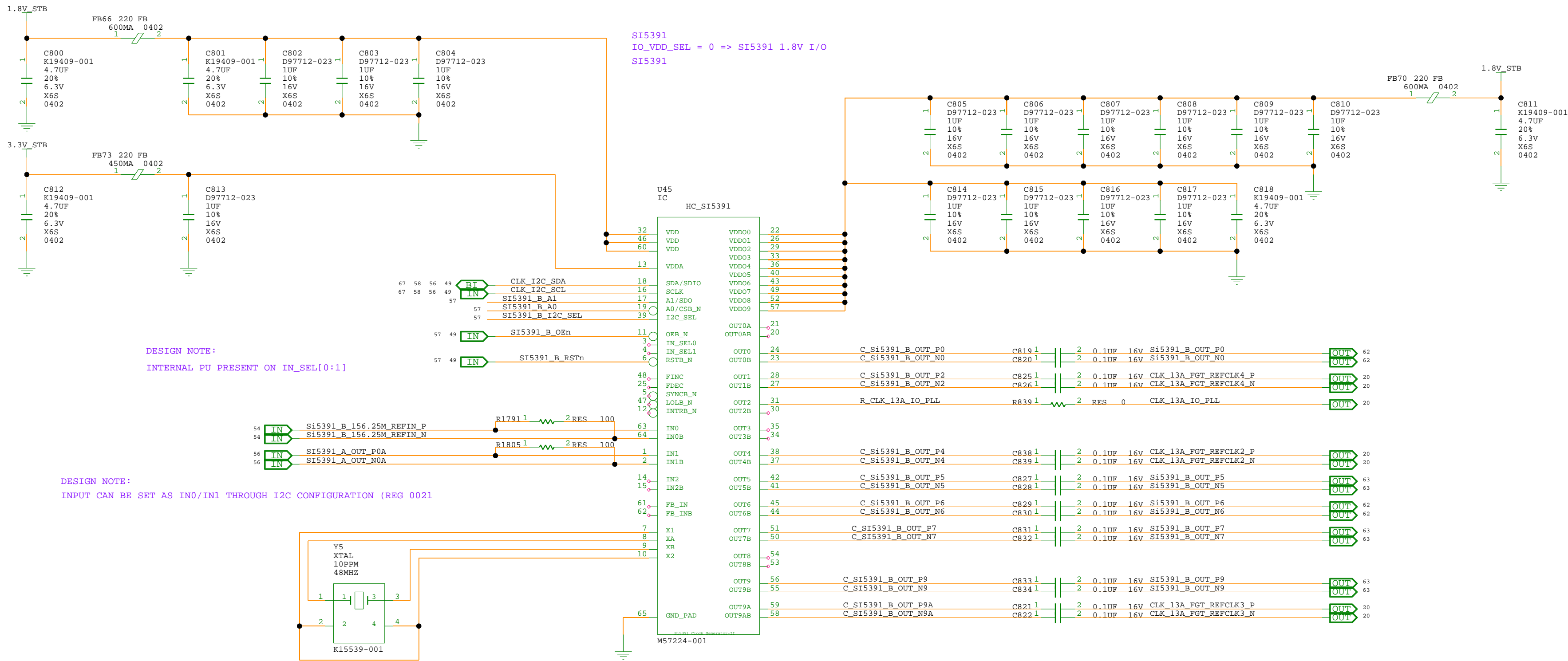
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DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
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		SCALE:	DO NOT SCALE DRAWING		SHEET 55 OF 95

SI5391 CLOCK GENERATOR-I



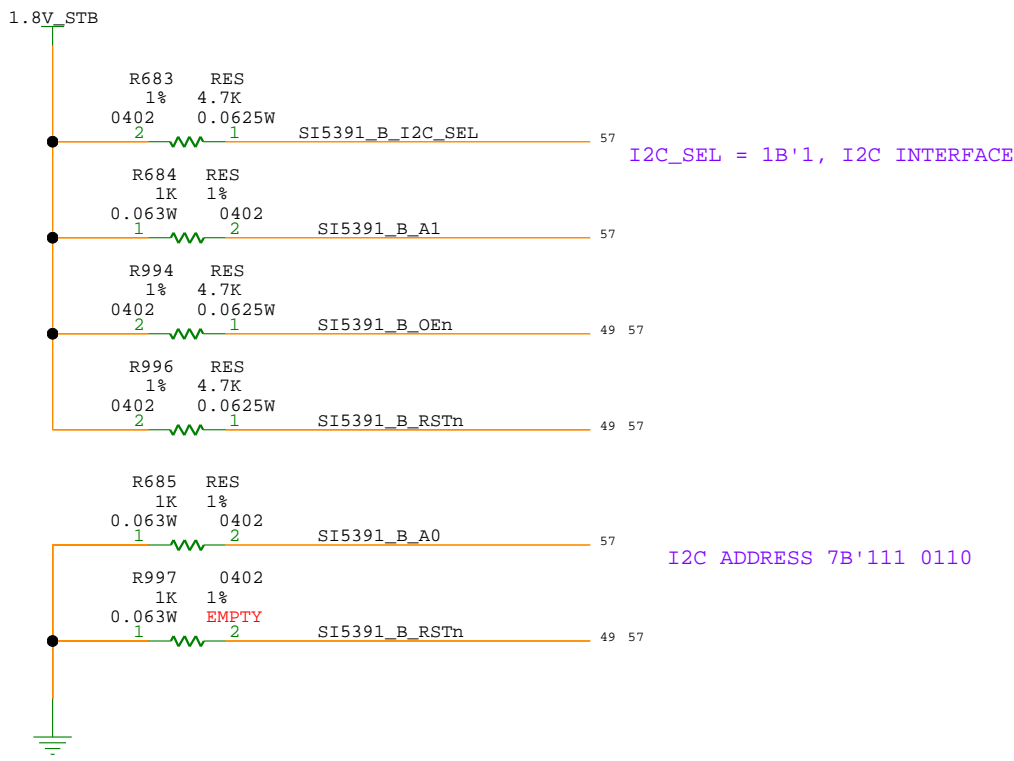
SI5391 CLOCK GENERATOR-II



DESIGN NOTE:
INTERNAL PU PRESENT ON IN_SEL[0:1]

DESIGN NOTE:
INPUT CAN BE SET AS IN0/IN1 THROUGH I2C CONFIGURATION (REG 0021)

PULL-UP/DOWN RESISTORS



DEPARTMENT



SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-C1

REV

3P0

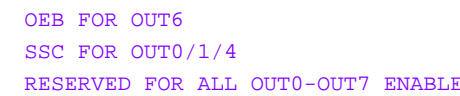
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DO NOT SCALE DRAWING

SHEET

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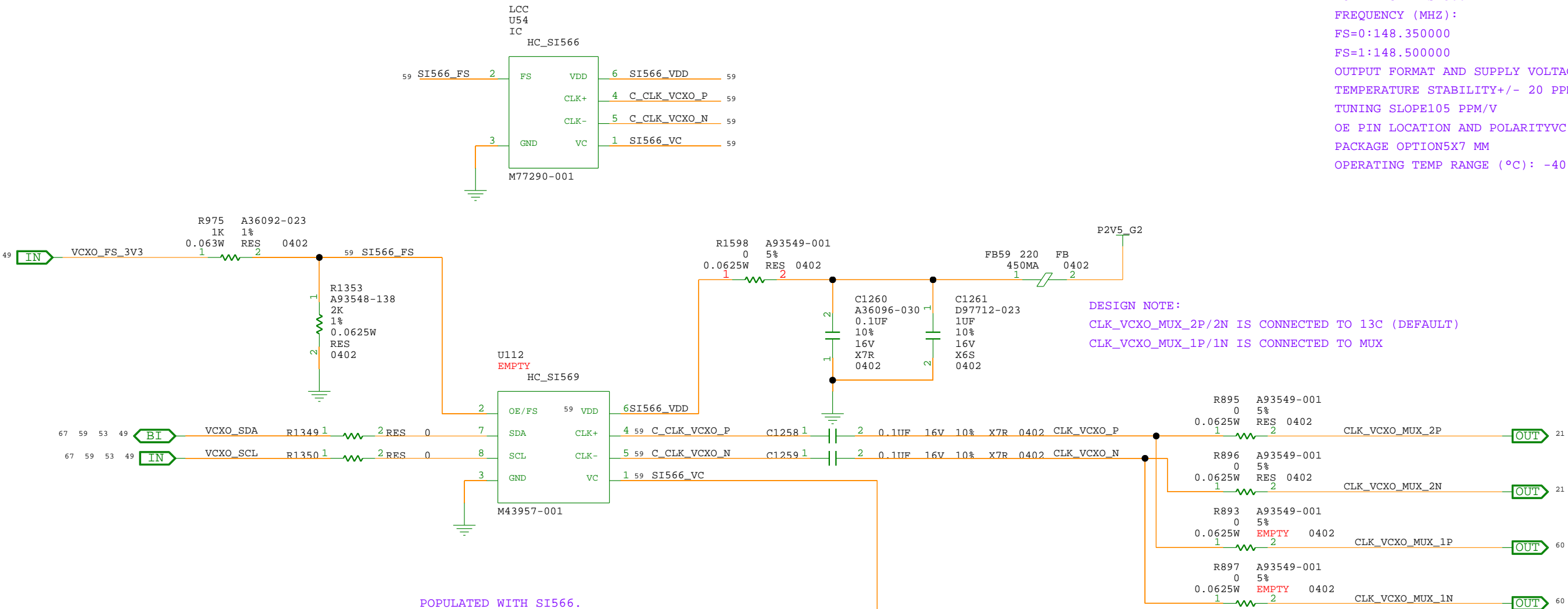
B

A

A

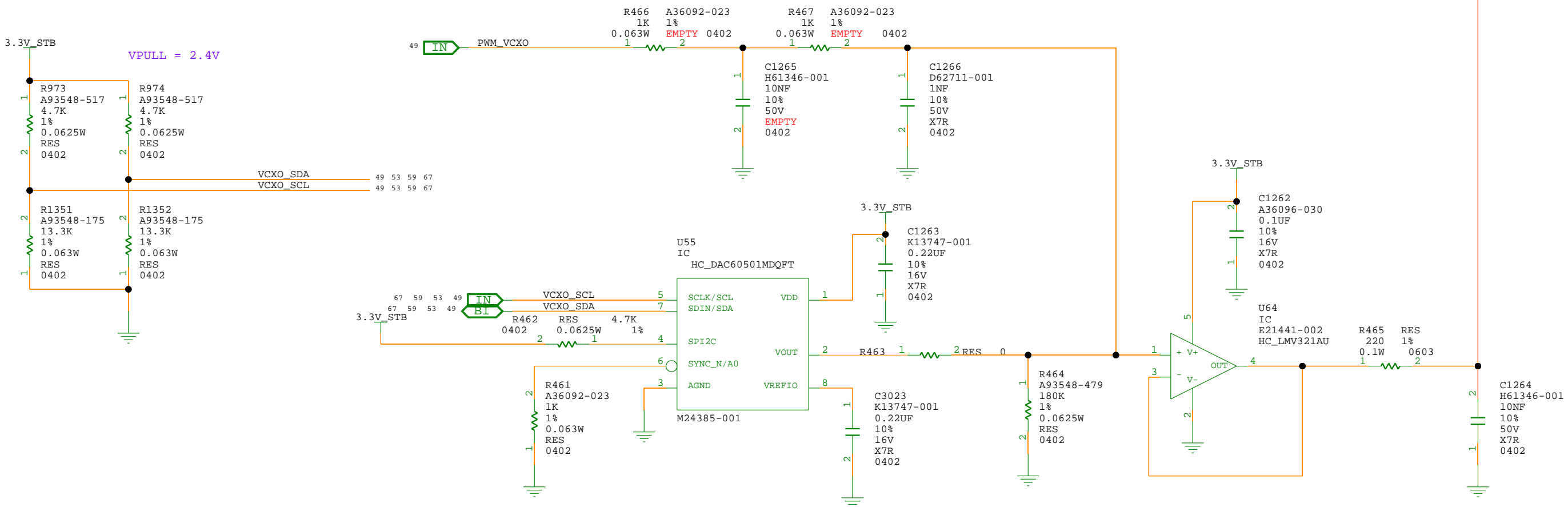
VCXO

CUSTOM PART NUMBER SPECIFICATION:
PART NUMBER56BCA000132ABG
MODEL NUMBERSI566
FREQUENCY (MHZ):
FS=0:148.350000
FS=1:148.500000
OUTPUT FORMAT AND SUPPLY VOLTAGELVDS: 1.8 V, 2.5 V, 3.3 V
TEMPERATURE STABILITY+/- 20 PPM
TUNING SLOPE105 PPM/V
OE PIN LOCATION AND POLARITYVC PIN1, FS PIN2, OE ALWAYS ON
PACKAGE OPTION5X7 MM
OPERATING TEMP RANGE (°C): -40 TO +85



POPULATED WITH SI566.
FS CONTROL BY MAX10
FS=0: 148.35MHZ
FS=1: 148.50MHZ
I2C ONLY AVAILABLE IF SI569 IS POPULATED.

DESIGN NOTE:
CLK_VCXO_MUX_2P/2N IS CONNECTED TO 13C (DEFAULT)
CLK_VCXO_MUX_1P/1N IS CONNECTED TO MUX




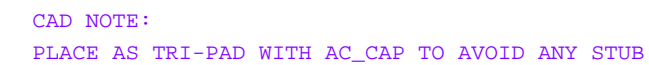
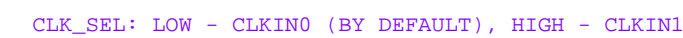
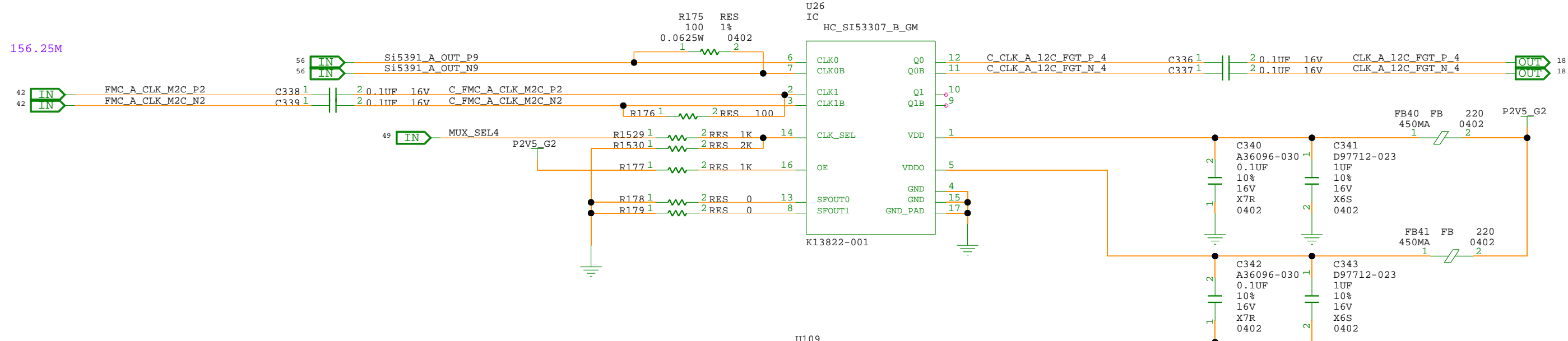
I2C ADDRESS 7B'100_1000

DEFAULT MIDRANG, 2.5V/2, NO OFFSET FROM THE VDD/2 OF THE VCXO INPUT

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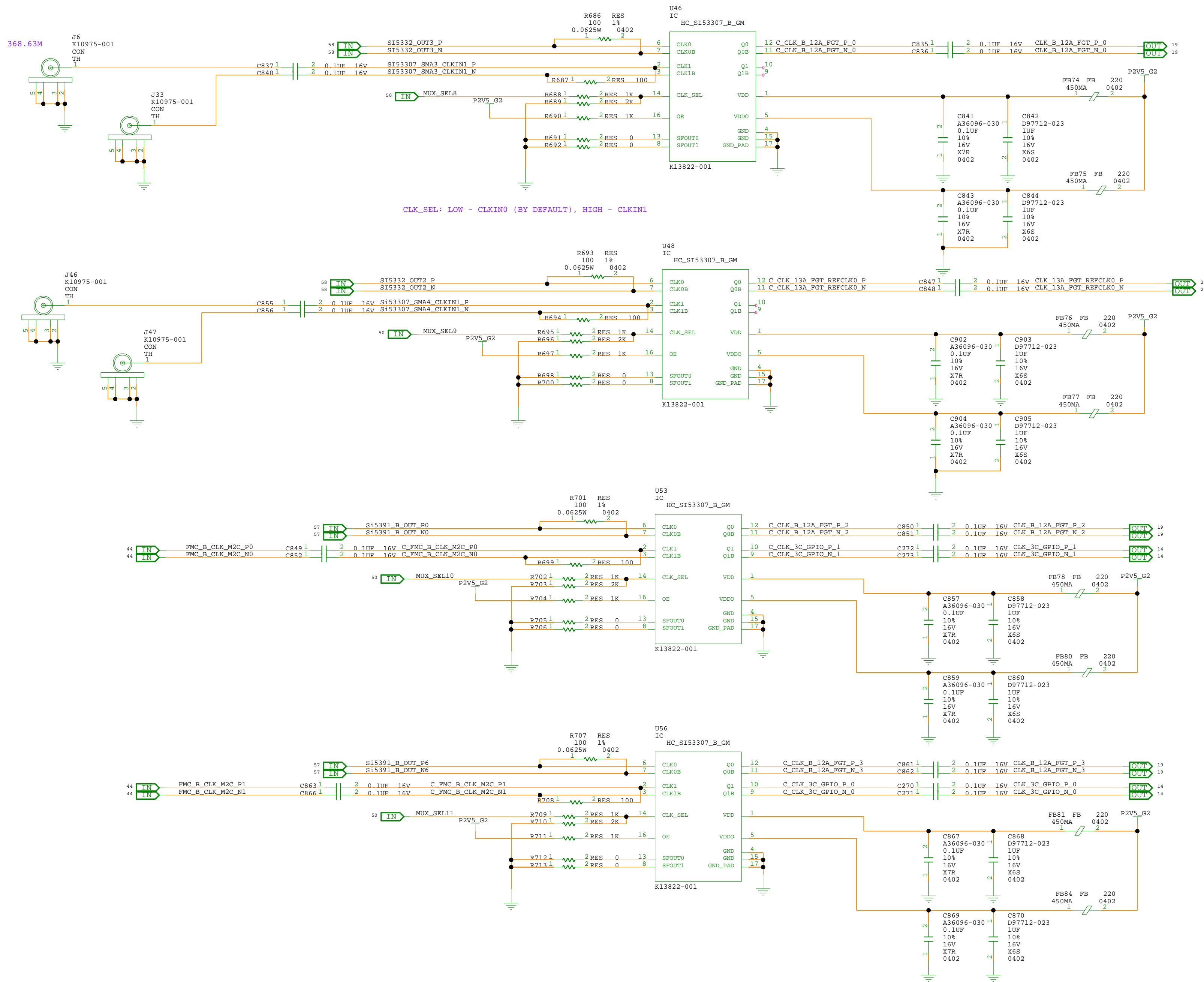
DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330690-C1	3P0
		SCALE:	DO NOT SCALE DRAWING		SHEET 60 OF 95



156.25



CLOCK MUX-III



CLK_SEL: LOW - CLKIN0 (BY DEFAULT), HIGH - CLKIN1

<->

DEPARTMENT



SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330690-C1

REV

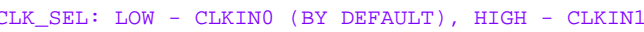
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SCALE:

DO NOT SCALE DRAWING

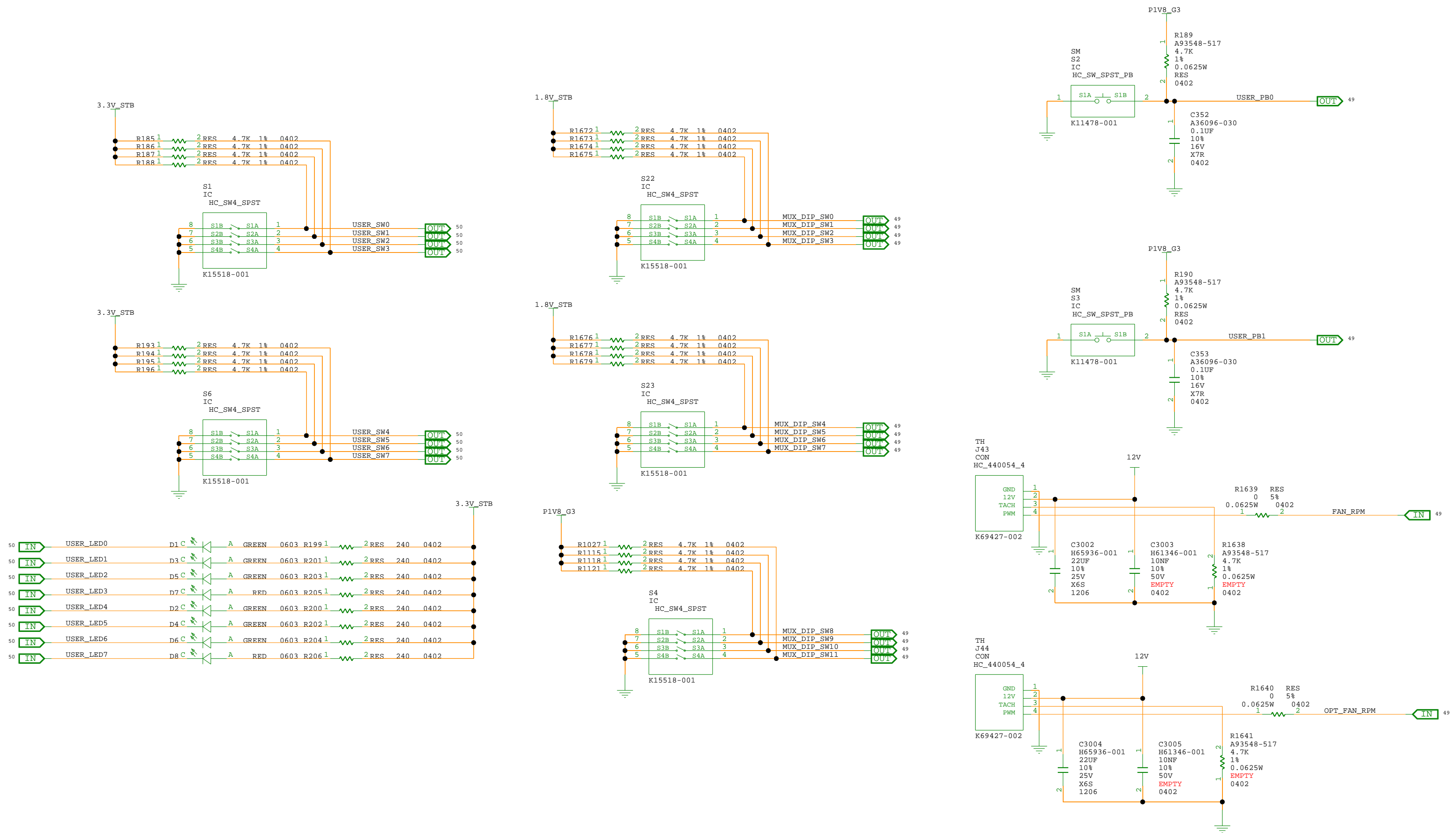
SHEET

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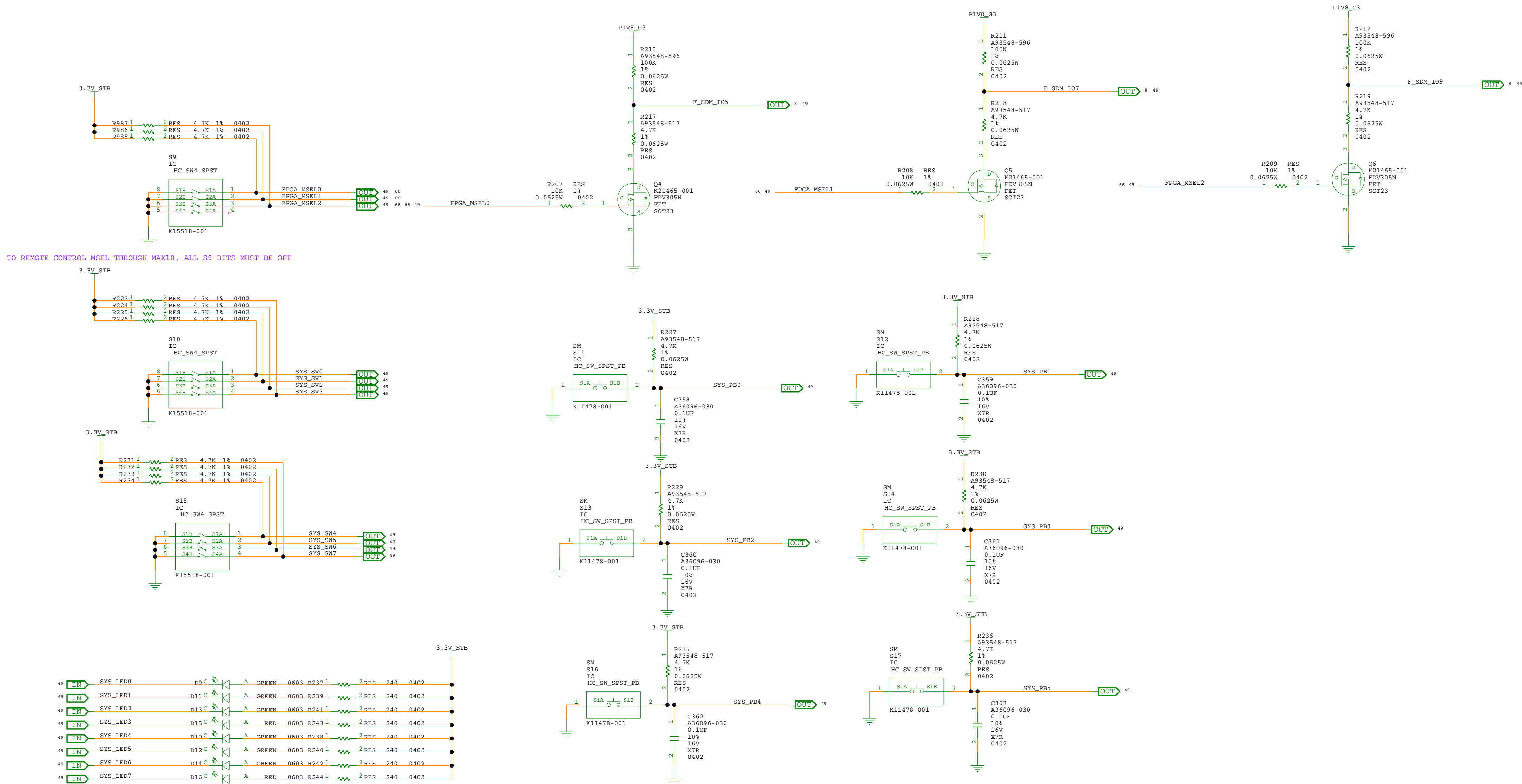


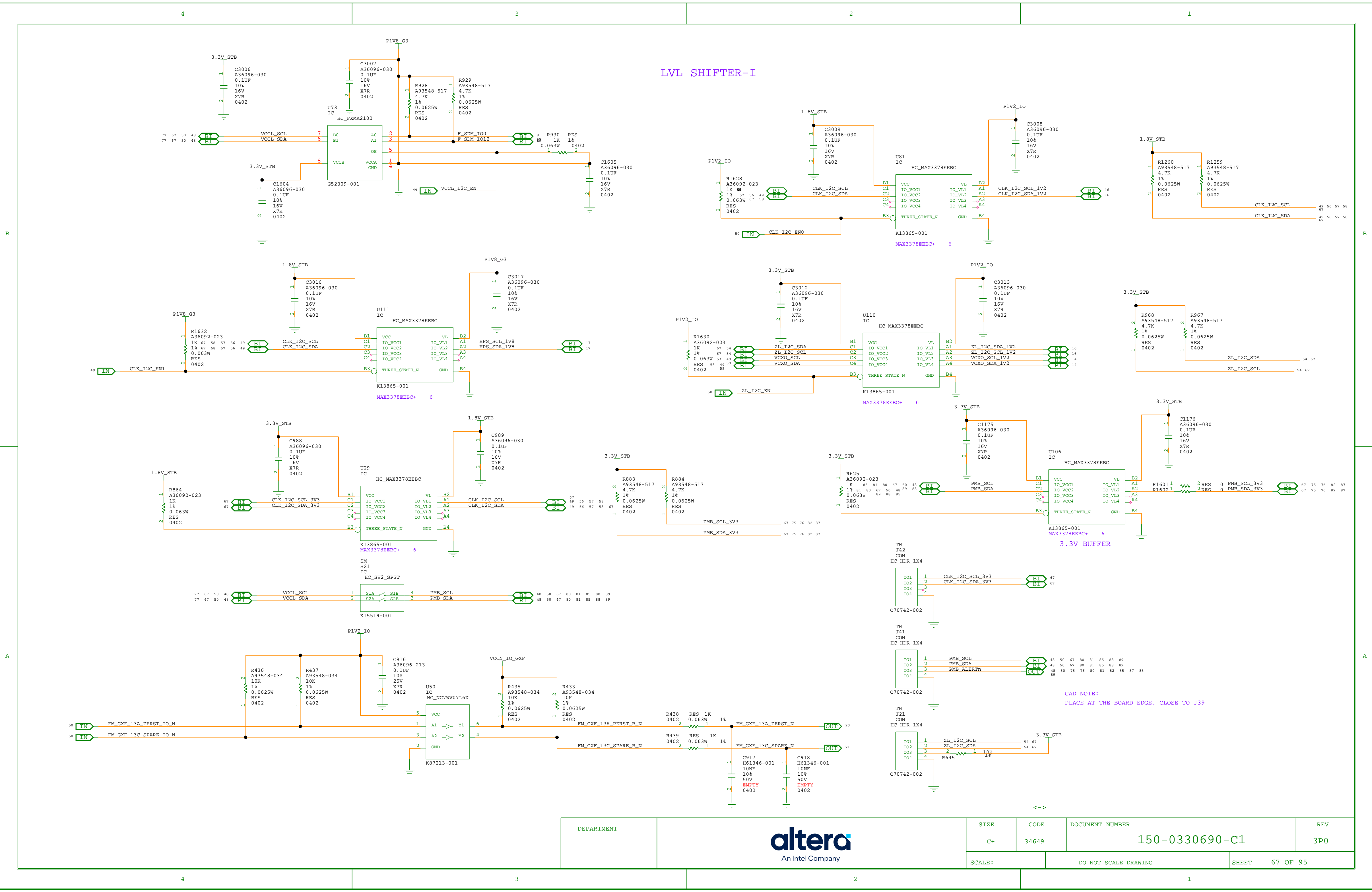
4		3		2		1			
RESERVED									
4		3		2		1			
		DEPARTMENT		altera An Intel Company		SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330690-C1	REV 3P0
						SCALE:		DO NOT SCALE DRAWING	SHEET 64 OF 95

DIP SWITCH, LEDS



DIP SWITCH, LEDS





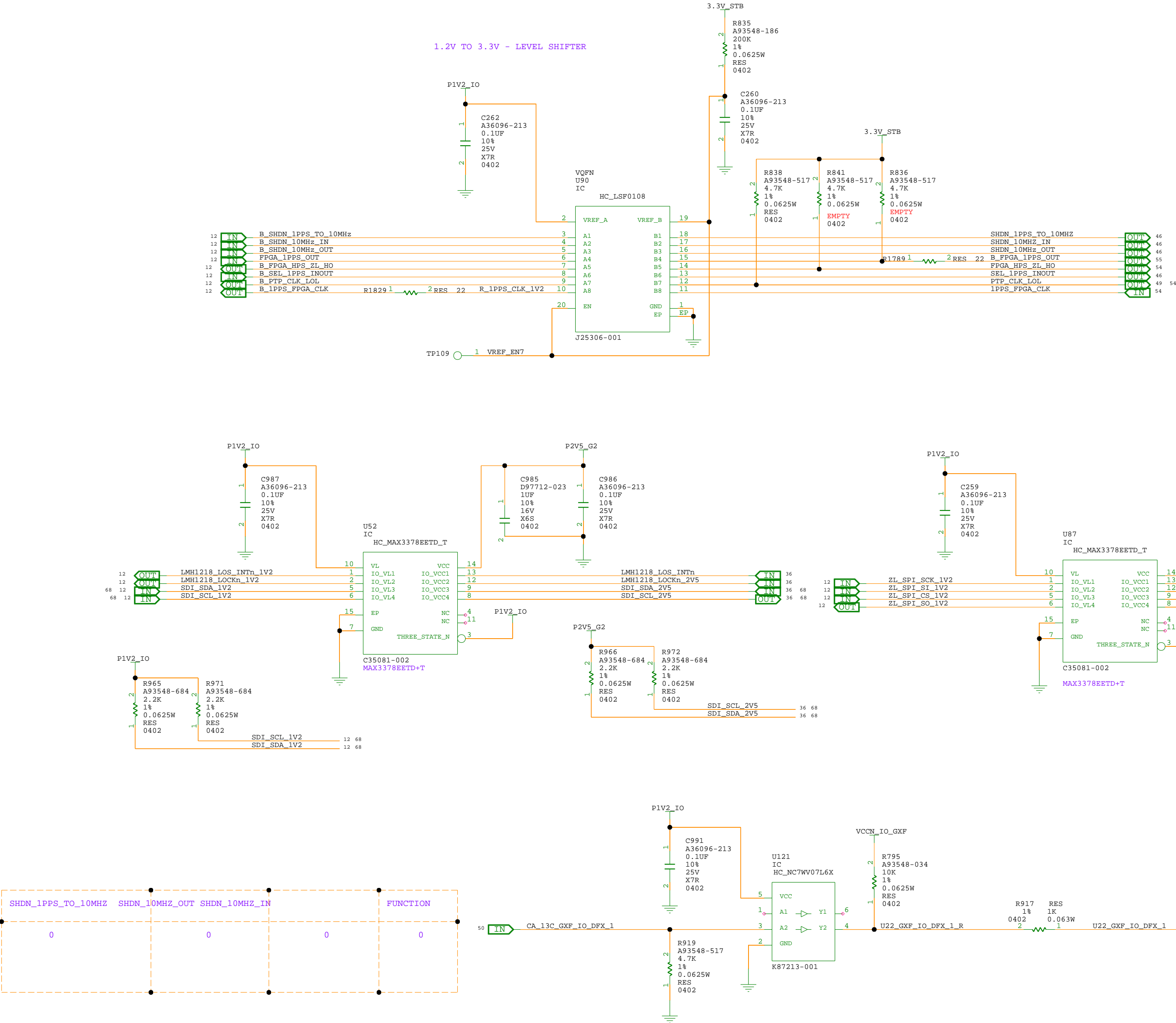
B

B

A

A

LVL SHIFTER-II



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4				3				2				1			
RESERVED															
4				3				2				1			

4				3				2				1			
A				B				A				B			

4				3				2				1			
A				B				A				B			

4				3				2				1			
A				B				A				B			

4				3				2				1			
A				B				A				B			

4				3				2				1			
A				B				A				B			

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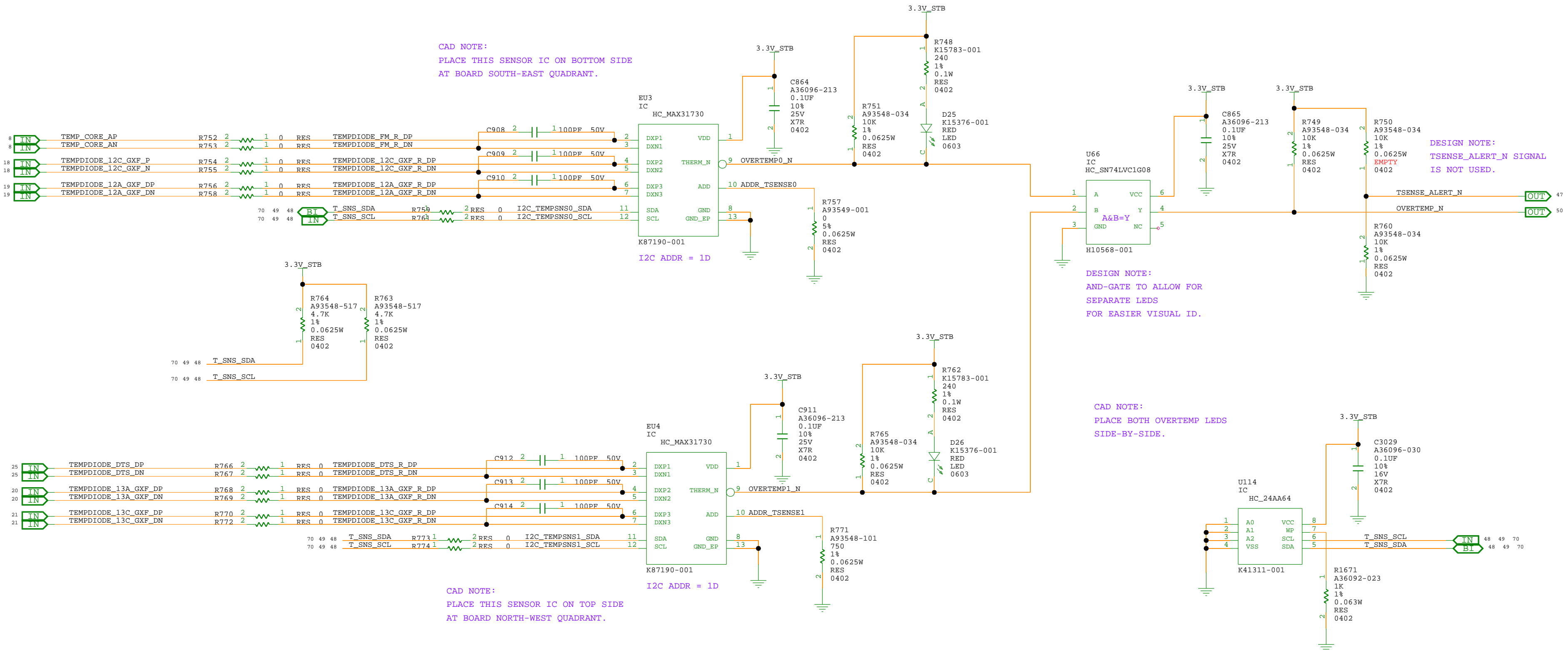
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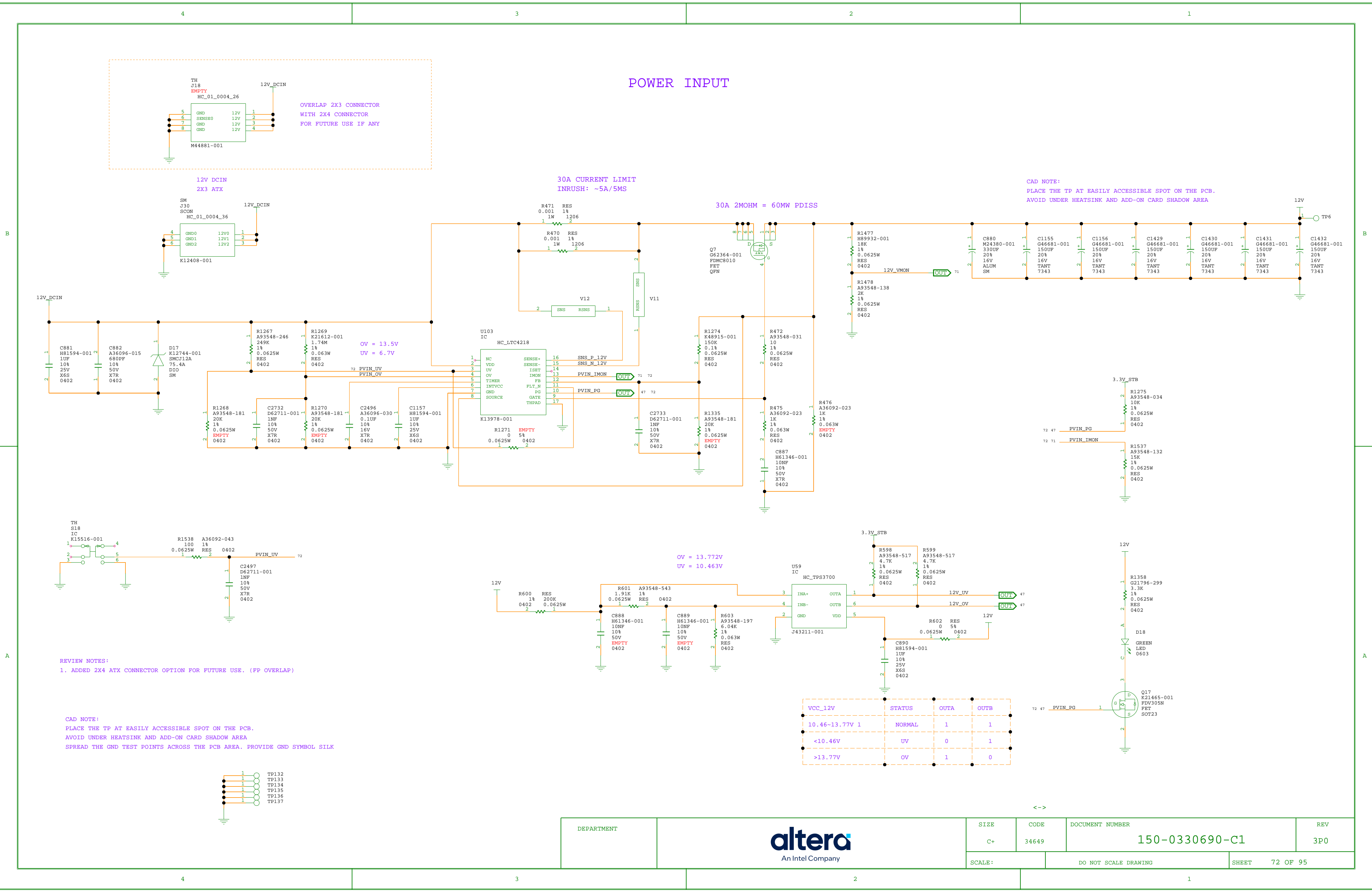
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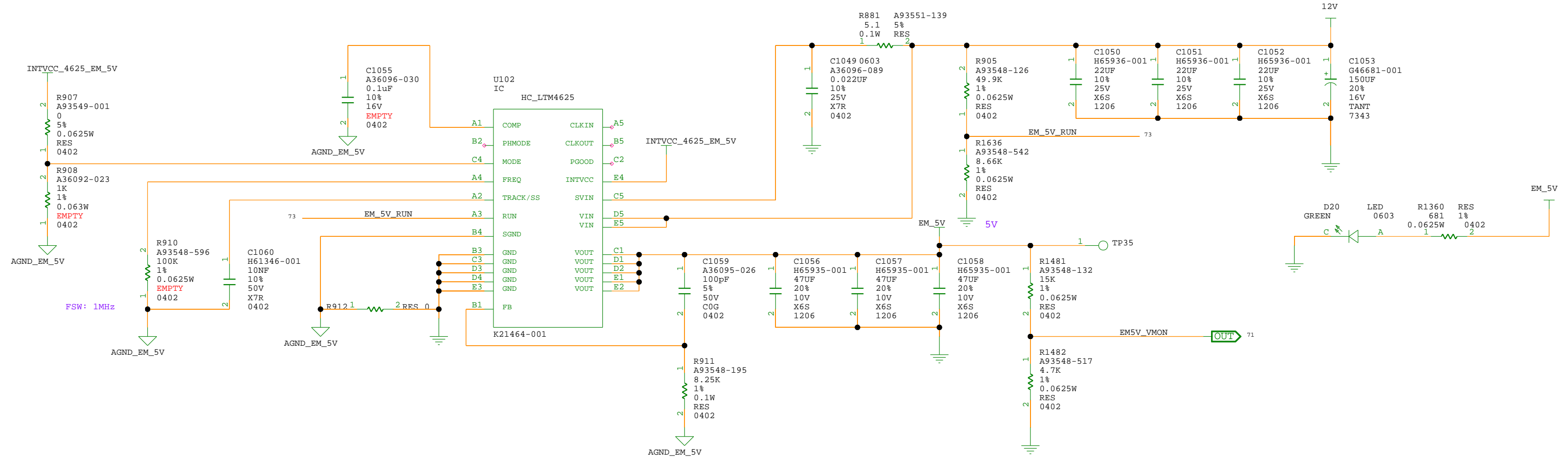
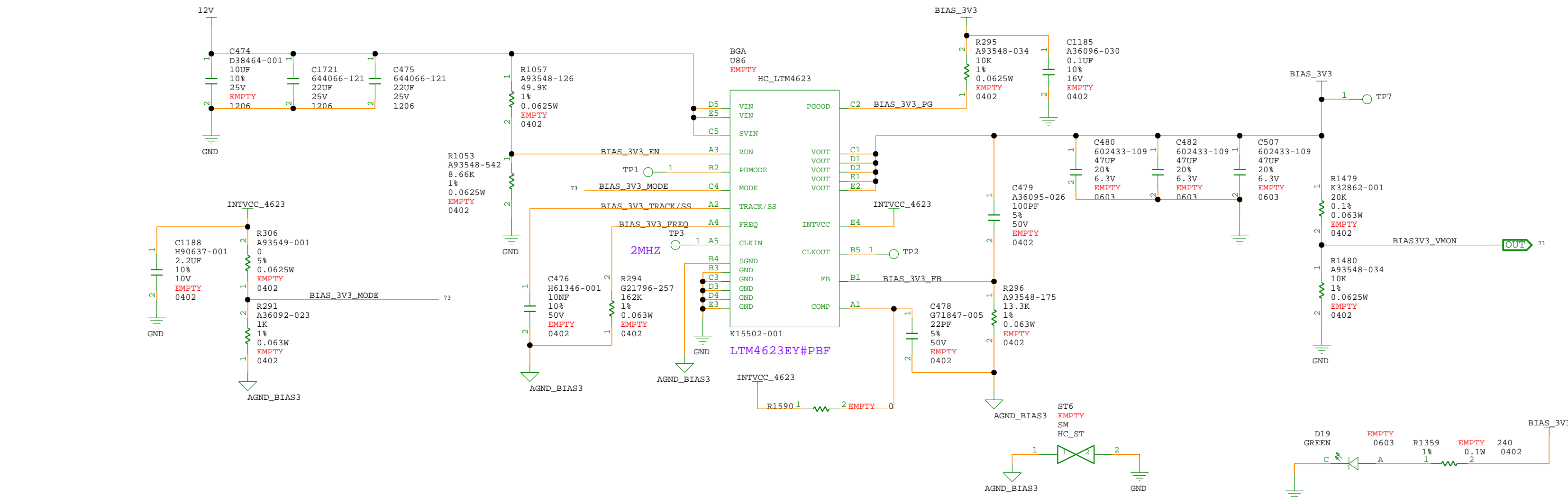
BOARD TEMP SENSORS





POWER BIAS


CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA



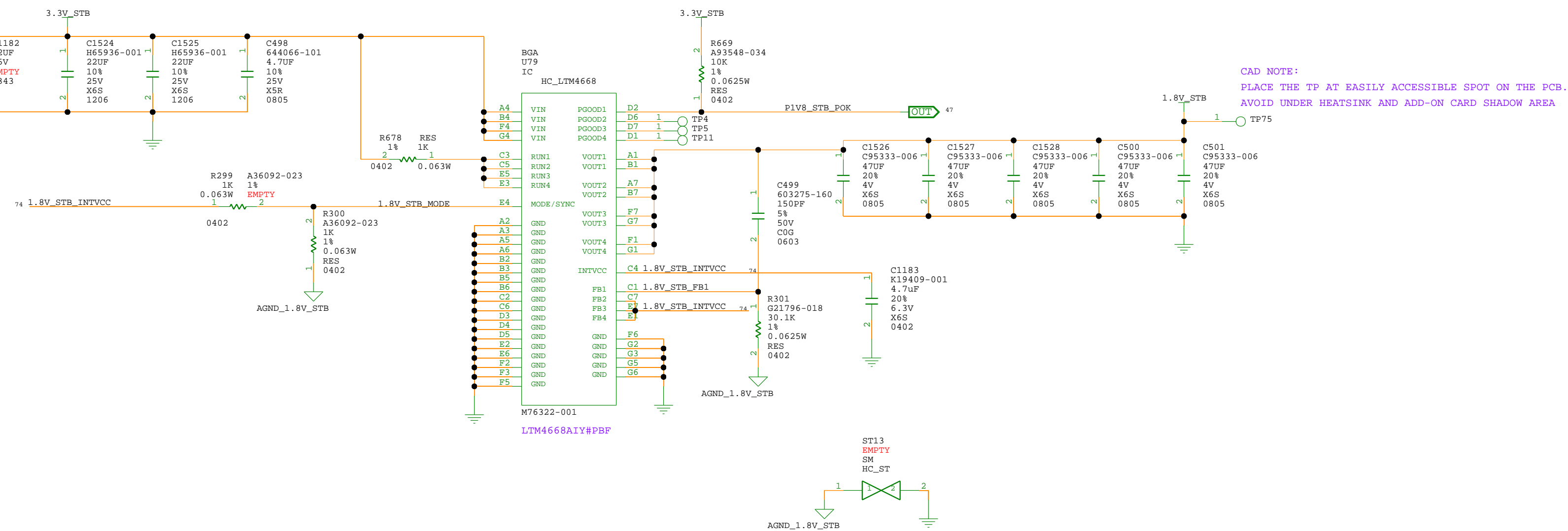
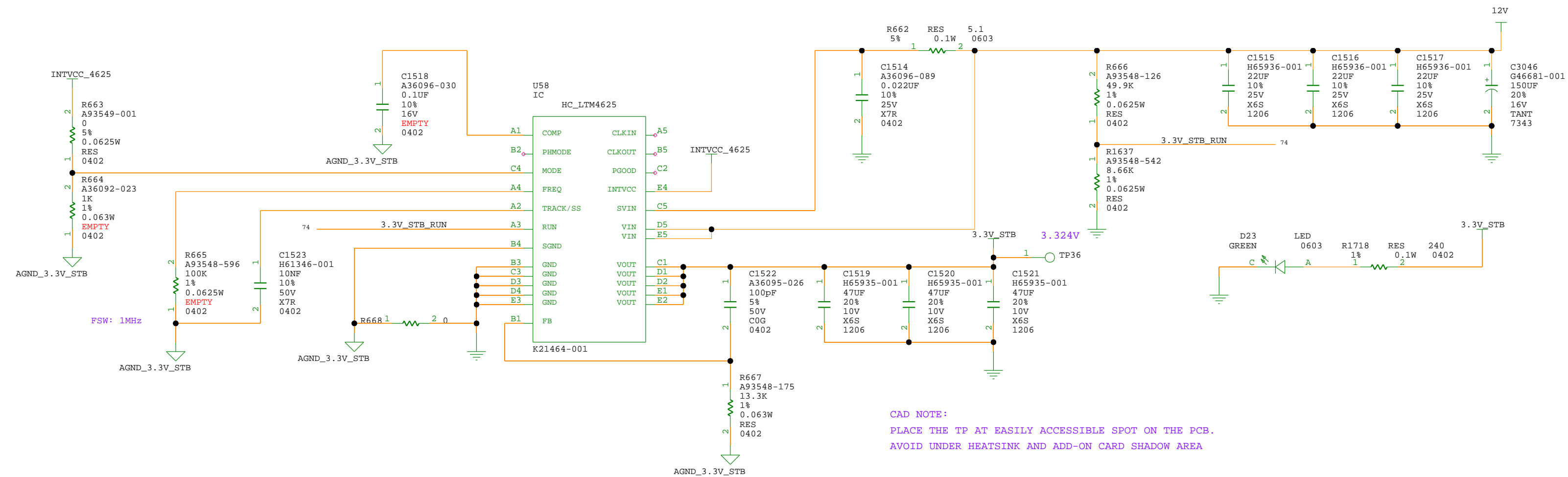
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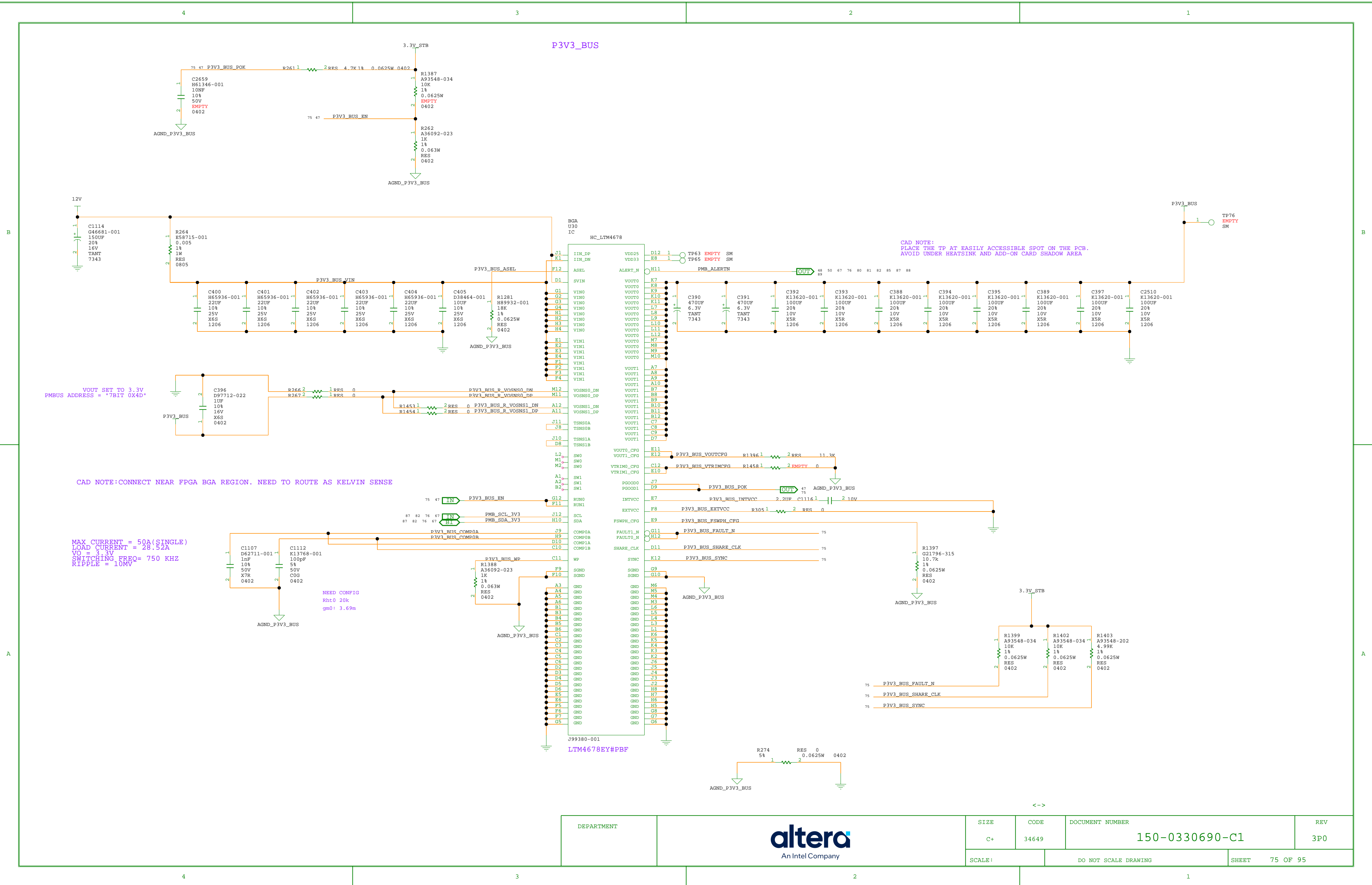
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

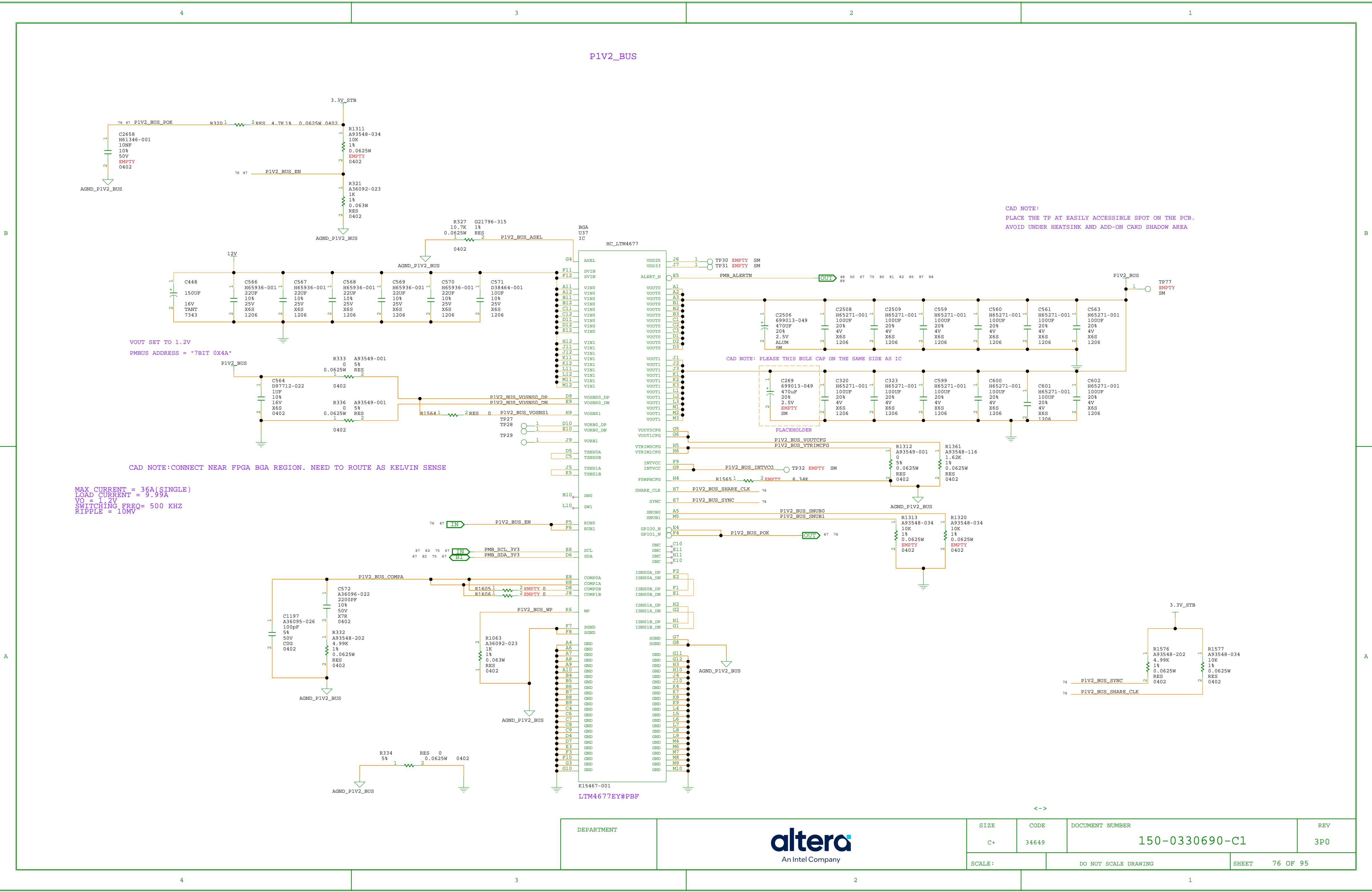
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DEPARTMENT <div>  <div> An Intel Company </div> </div>	SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330690-C1	REV 3P0
	SCALE:		DO NOT SCALE DRAWING	SHEET 73 OF 95

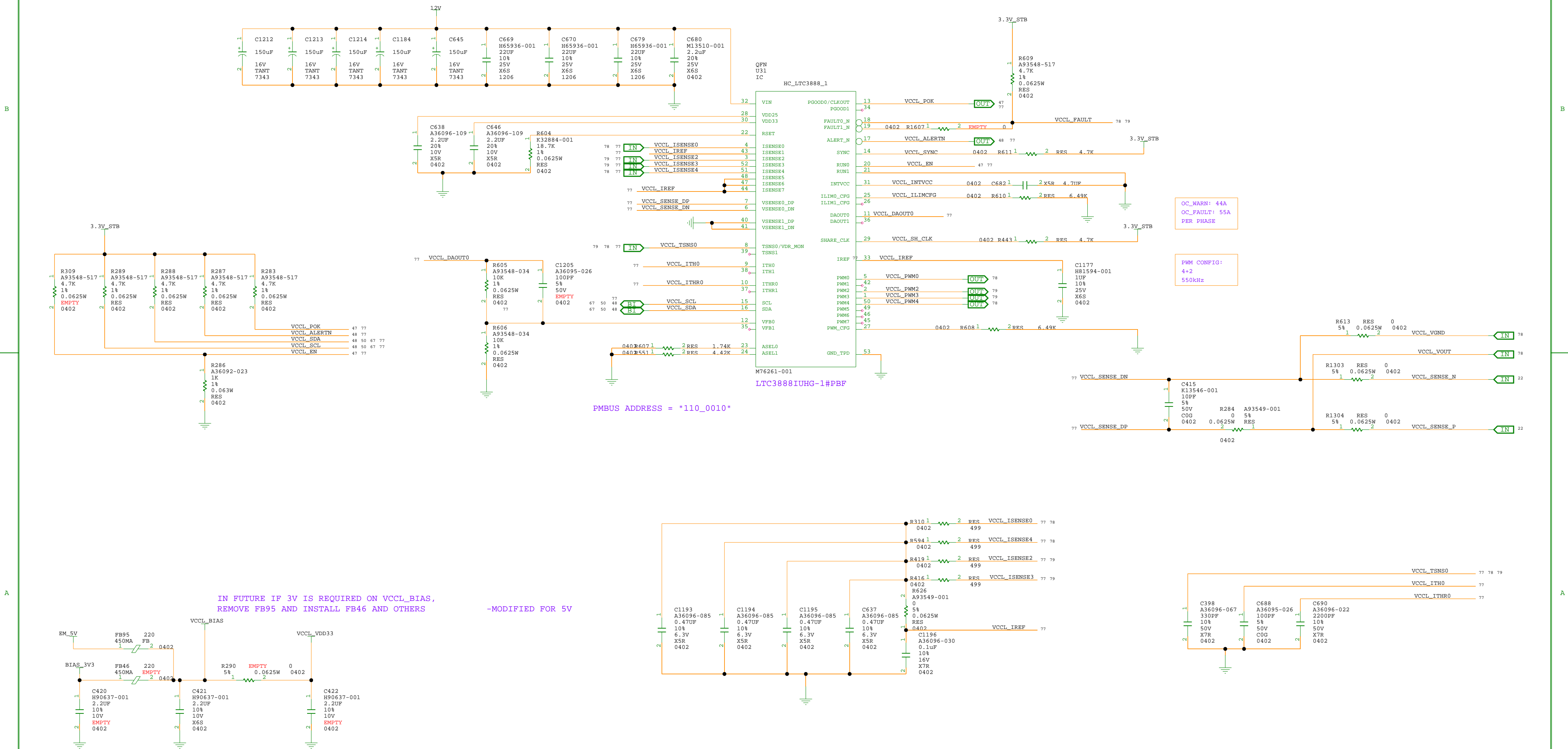
3.3V_STB & 1.8V_STB



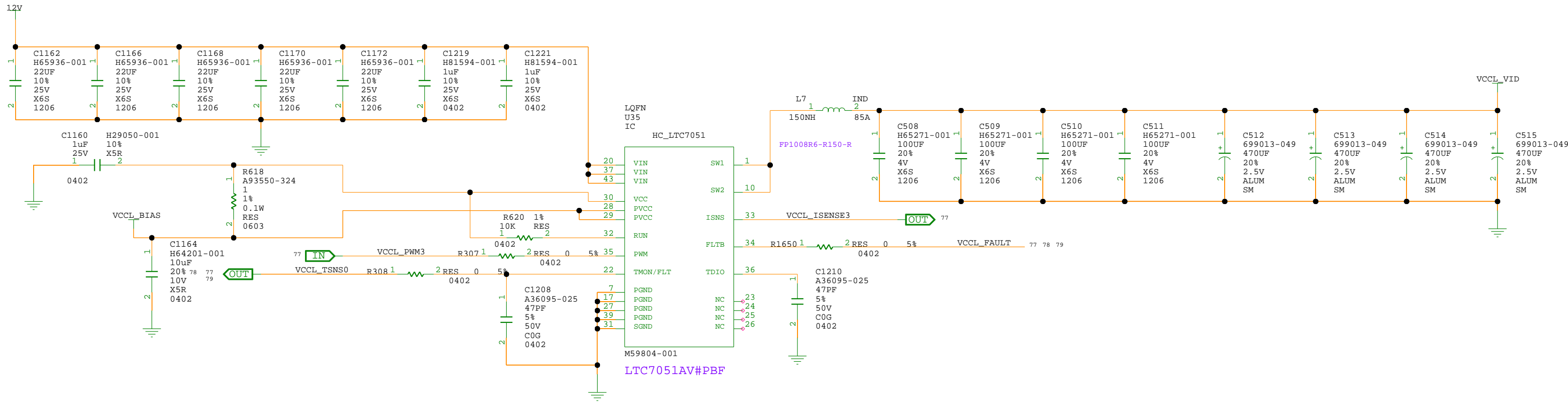
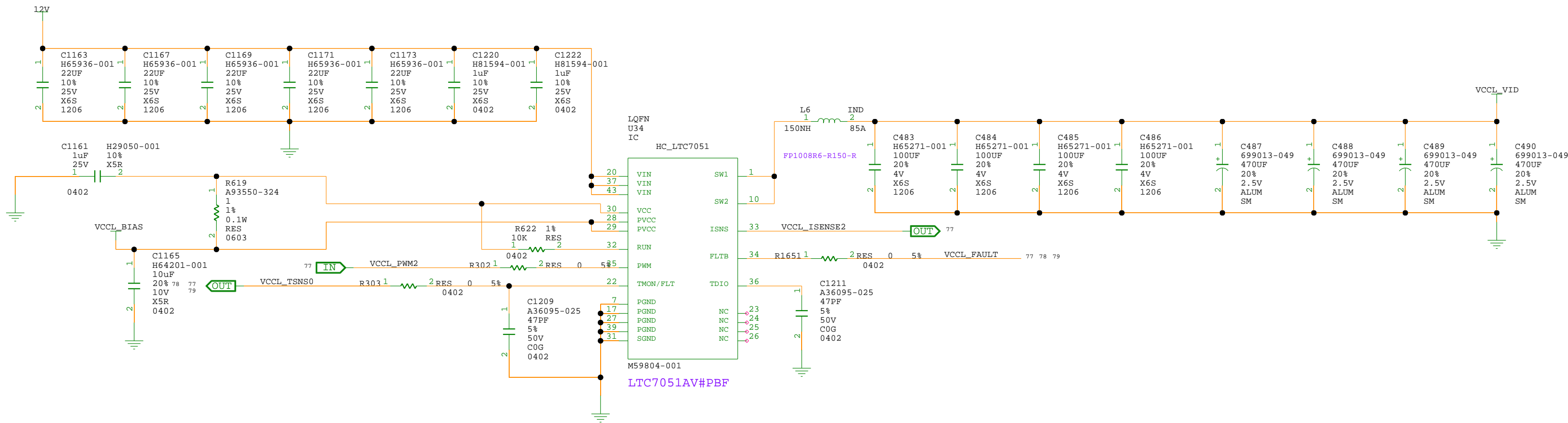




VCCL CONTROLLER



CORE FETS



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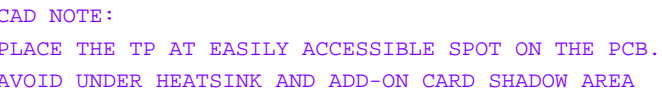
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Altera logo: The word "altera" in a bold, lowercase, sans-serif font, with a small blue square above the "a". Below it, the text "An Intel Company" in a smaller, lowercase, sans-serif font.

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B

B

VOUT SET TO 0.8V
PMBUS ADDRESS = "7BIT 0X40"

CAD NOTE:
PLACE THE TP AT EASILY ACCESSIBLE SPOT ON THE PCB.
AVOID UNDER HEATSINK AND ADD-ON CARD SHADOW AREA

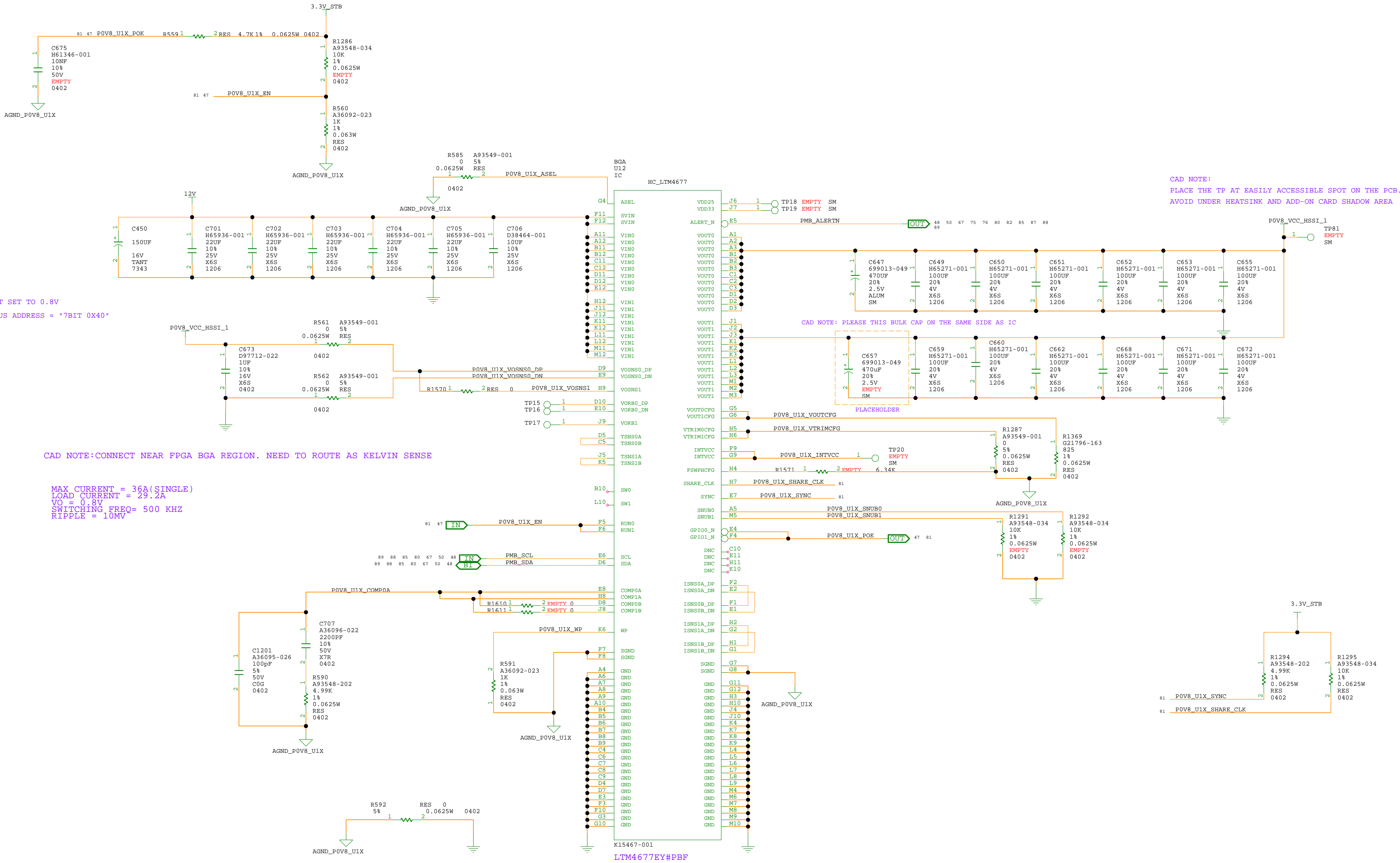
CAD NOTE:CONNECT NEAR FPGA BGA REGION. NEED TO ROUTE AS KELVIN SENSE

MAX CURRENT = 36A(SINGLE)
LOAD CURRENT = 29.2A
VO = 0.8V
SWITCHING FREQ= 500 KHZ
RIPPLE = 10MV

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P0V8_VCC_HSSI_1



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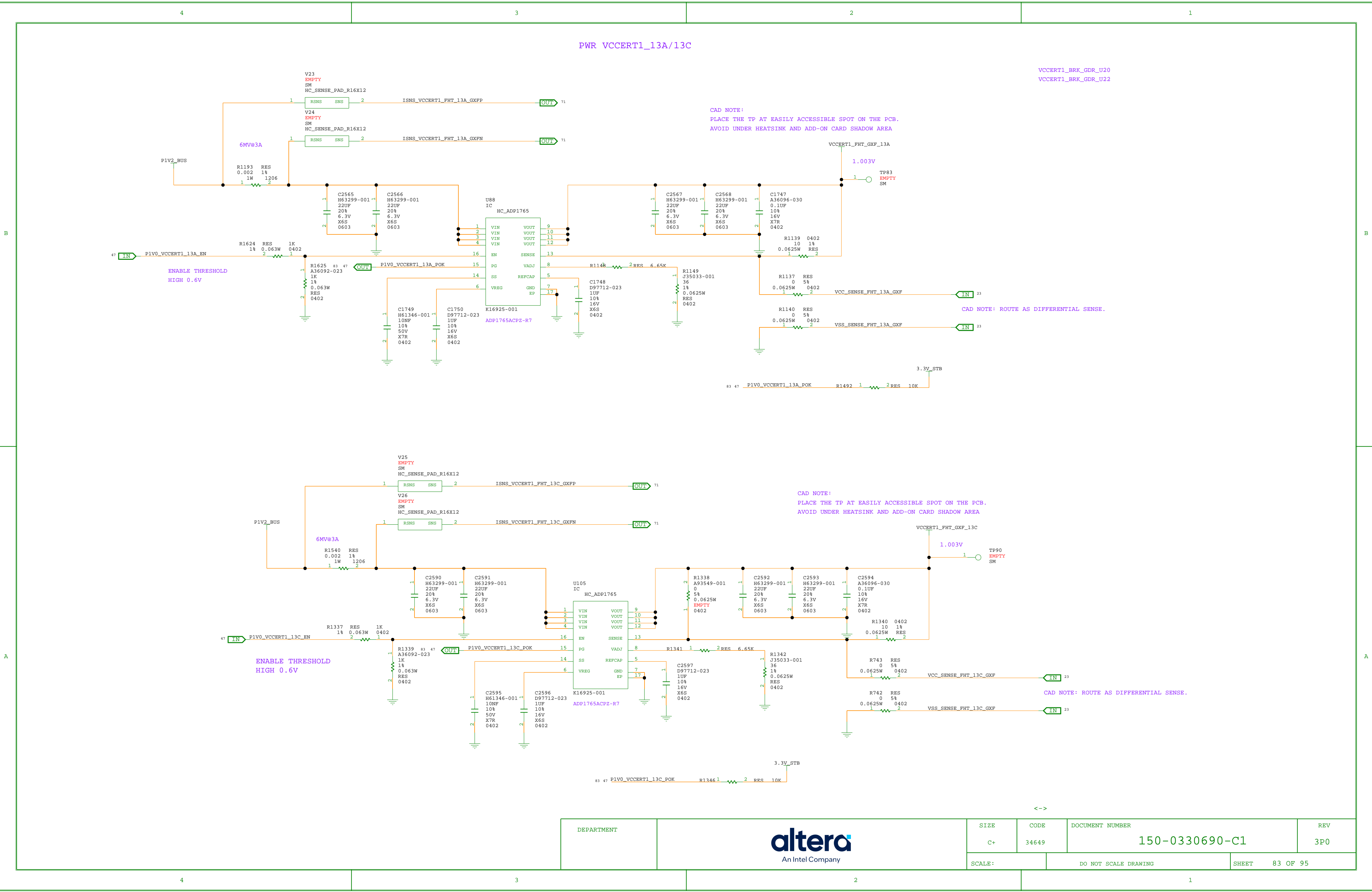
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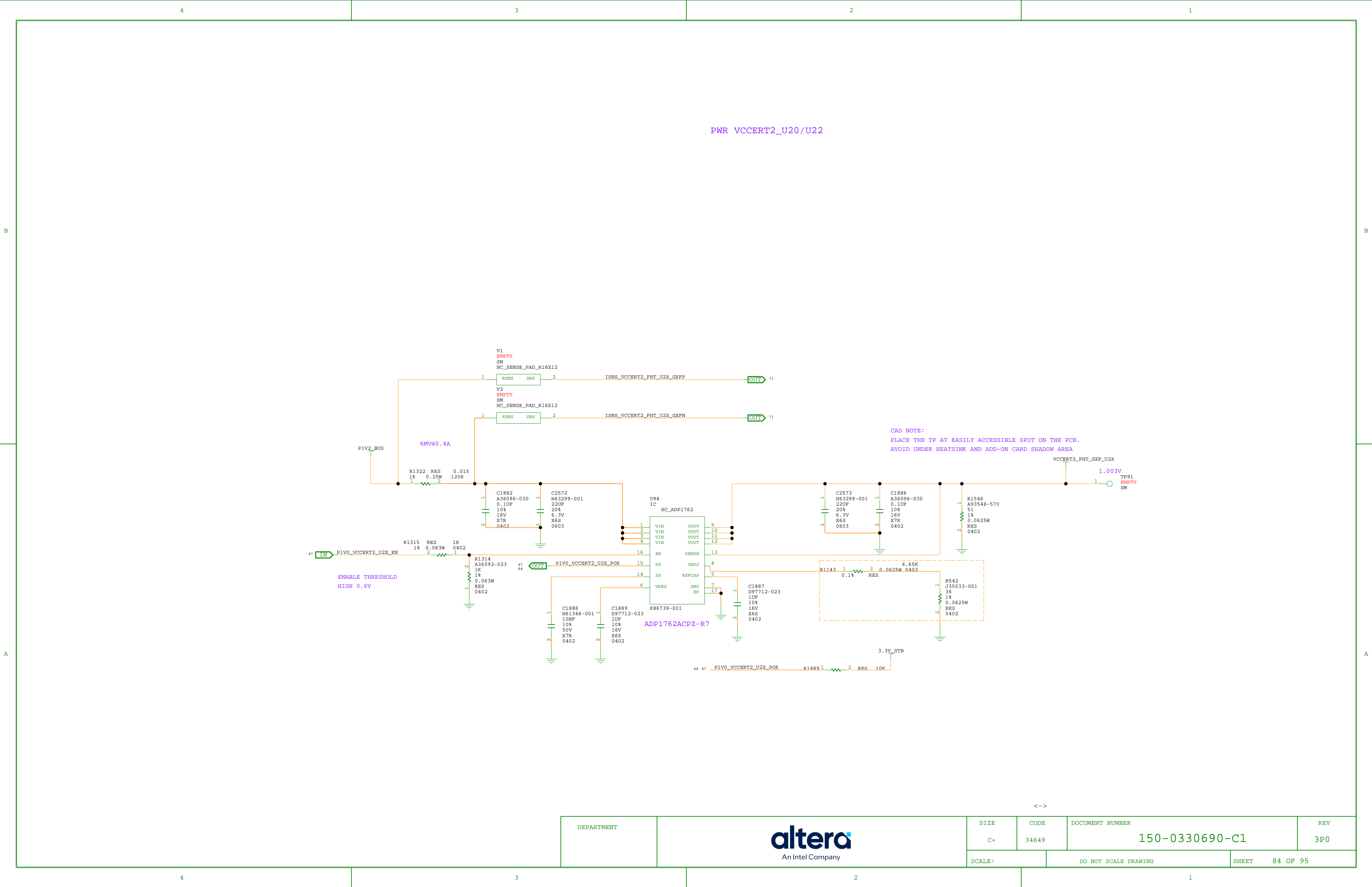
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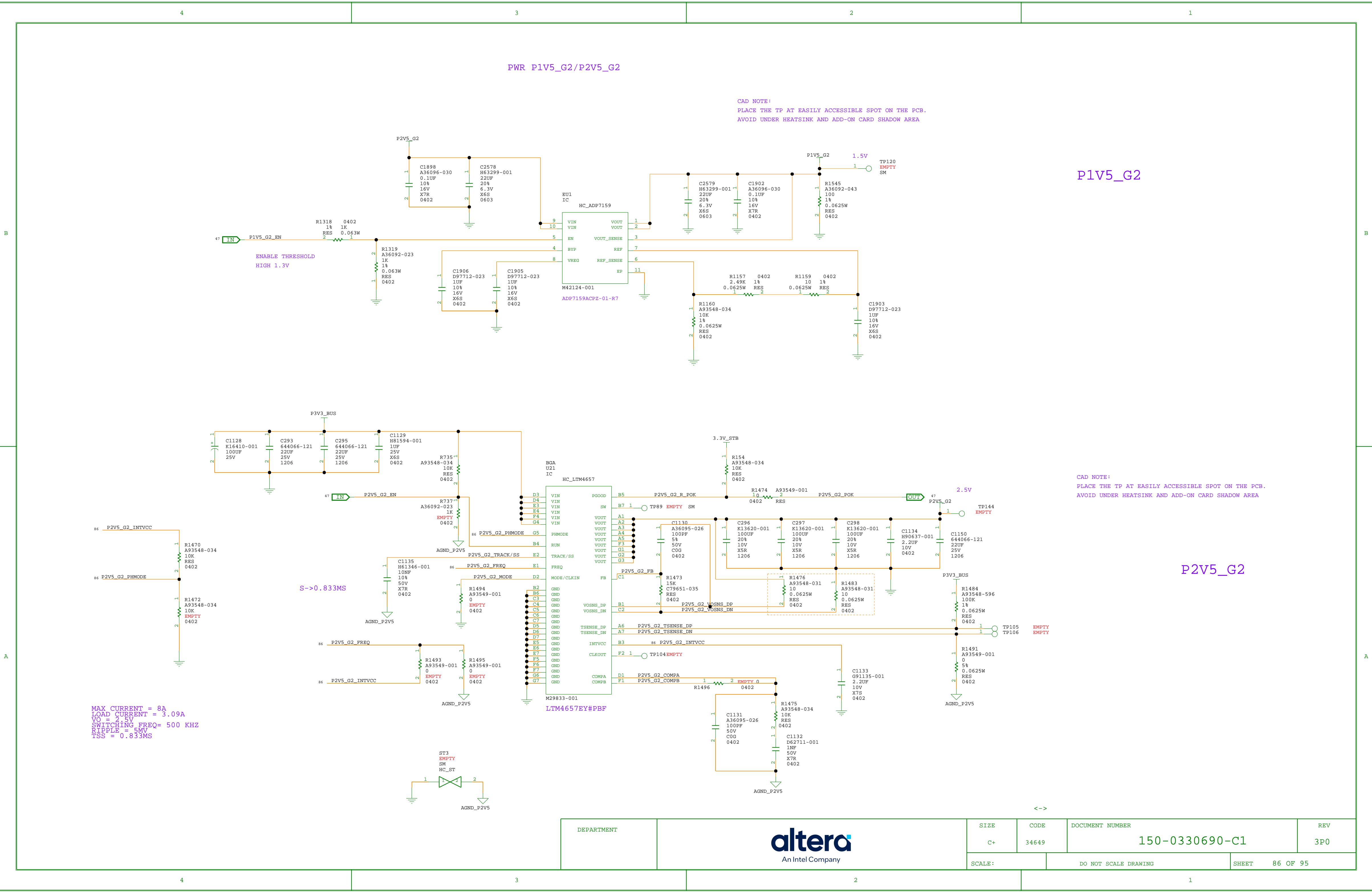
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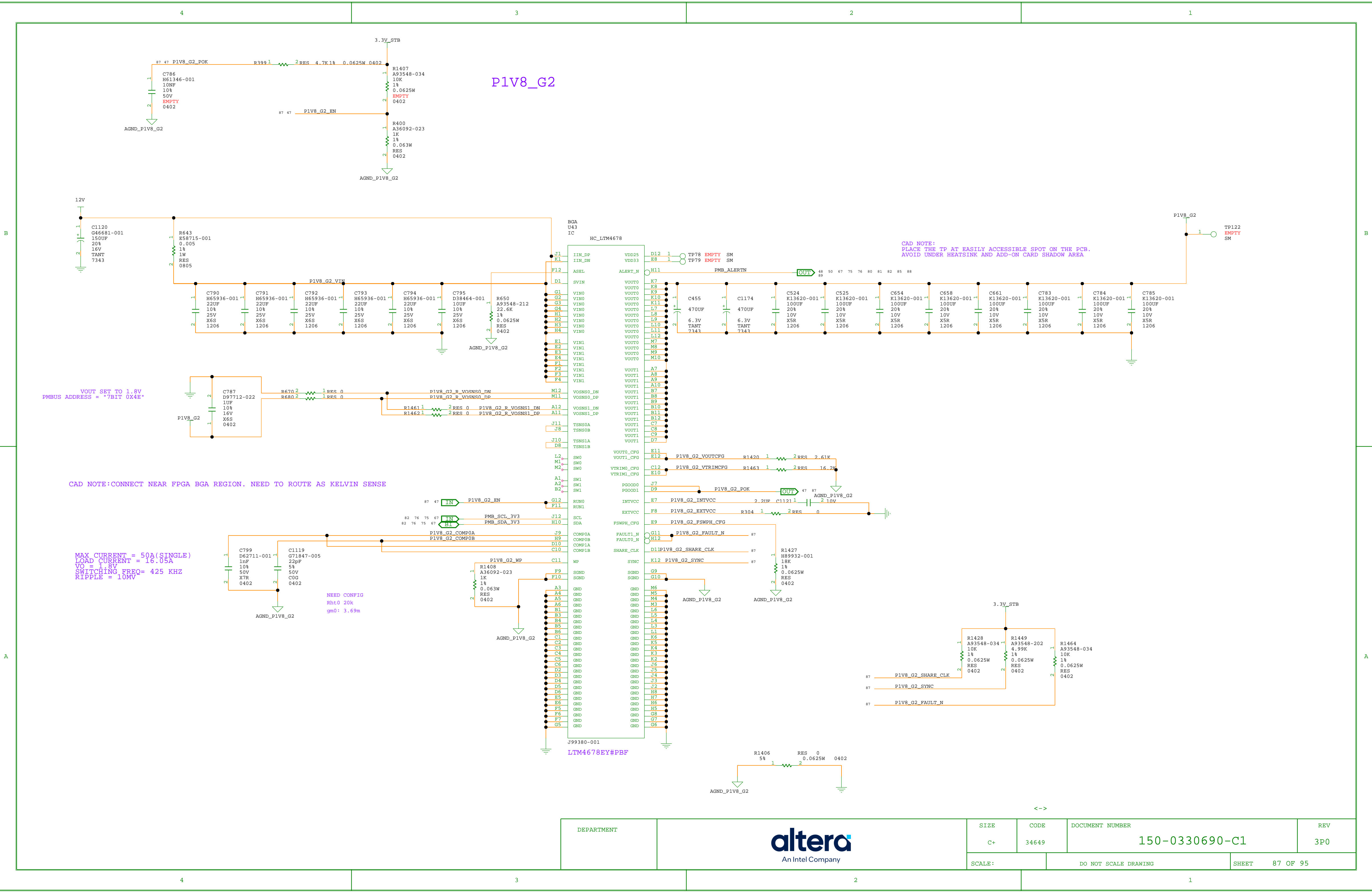
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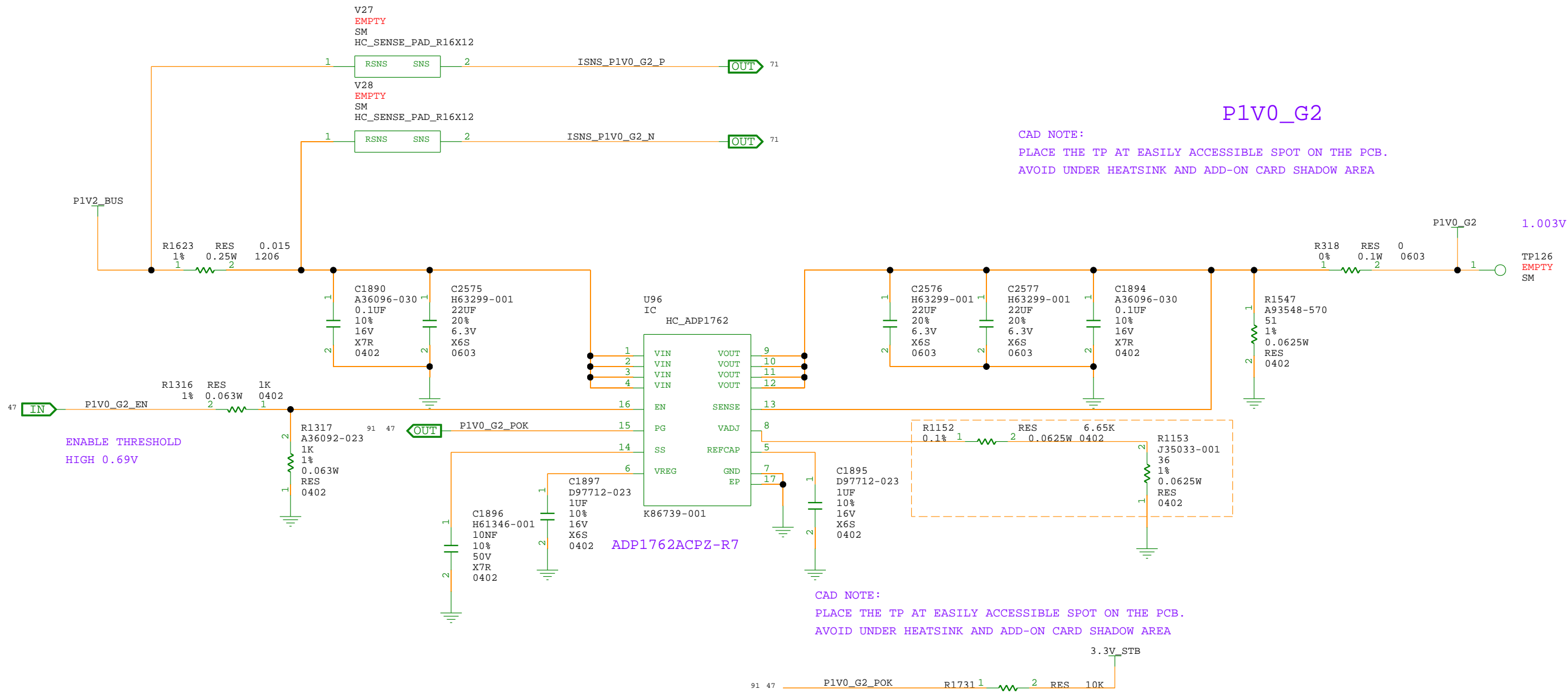
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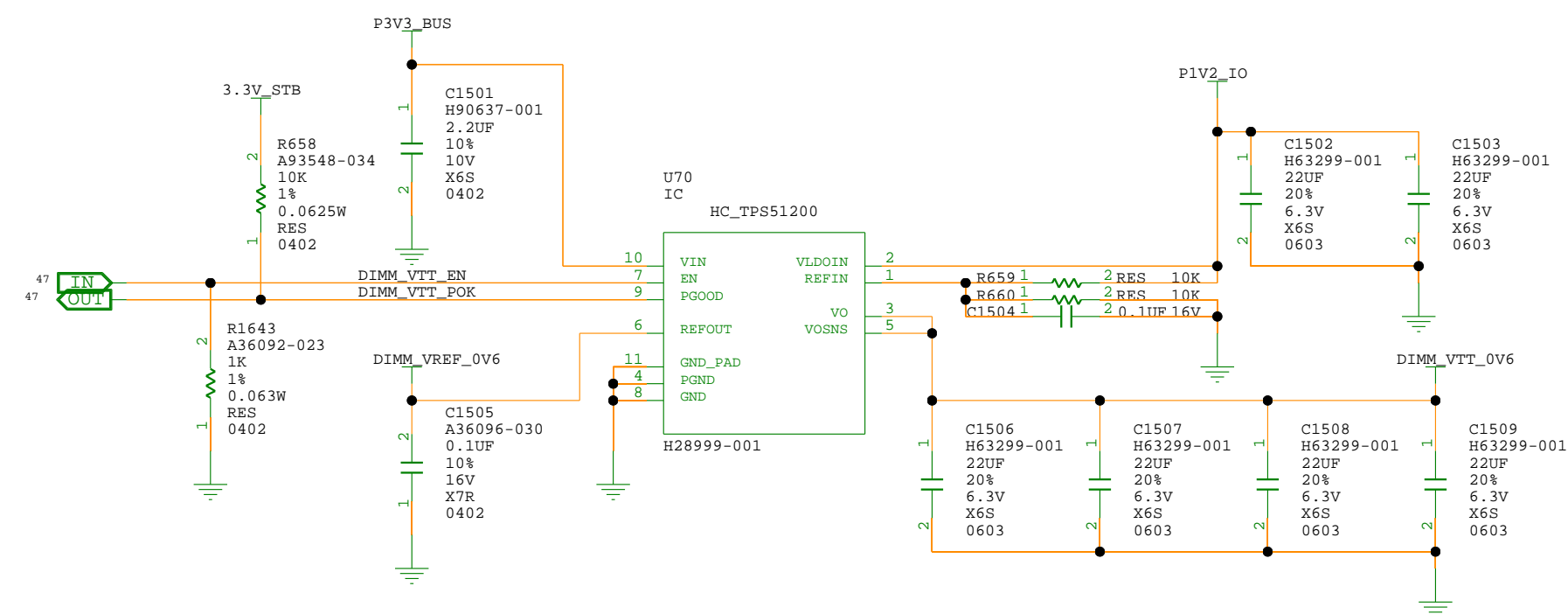
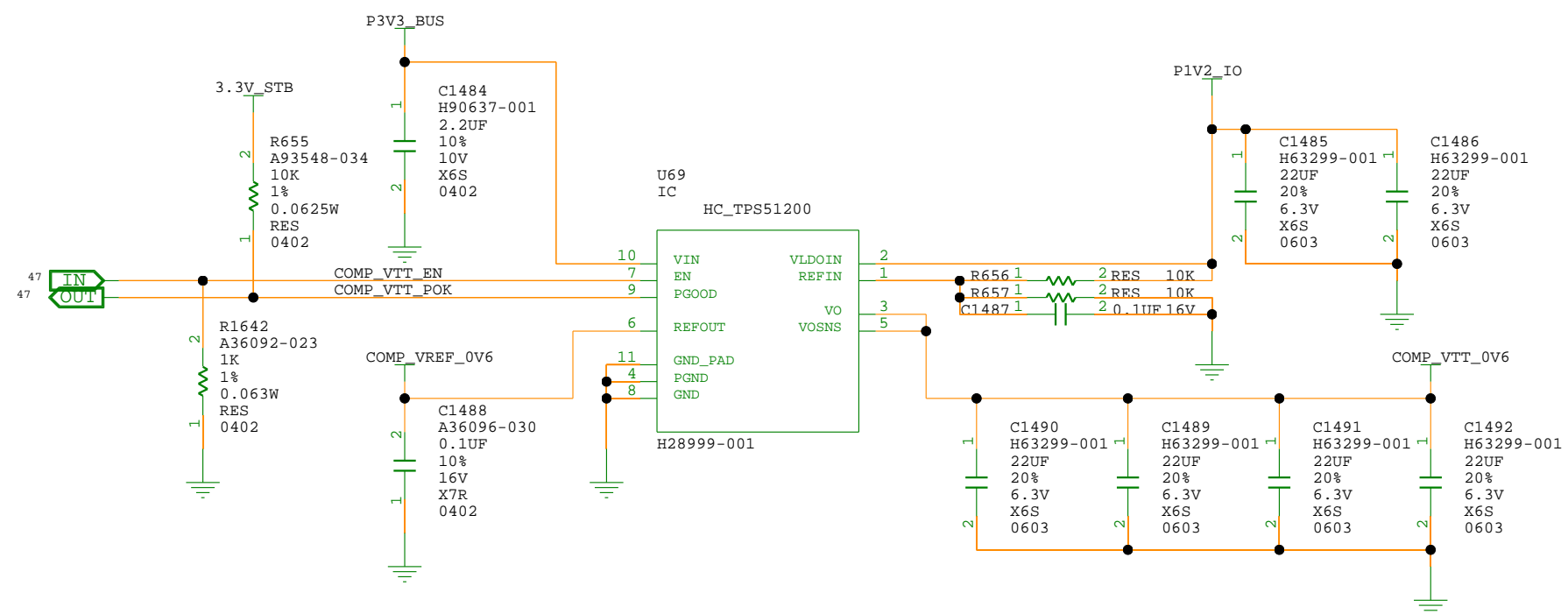
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PWR VCCH_SDM/P1V0_G2




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VTT REGULATORS



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USB PD CONTROLLER

CAD NOTE:
NO STUB ON USB0_DP/DM CONNECTING TO THE ZERO OHM

DESIGN NOTE:
I2C2 ACTS AS A SLAVE. MAX-10 COMMUNICATES WITH PD CONTROLLER AS A MASTER
I2C ADDRESS: 0X38

DESIGN NOTE:
I2C1 ACTS AS A MASTER AND COMMUNICATES WITH THE TUSB1146 SS MUX CONTROLLER

VALUE TO BE CHECKED.

I2C ADDRESS:

PROGRAMMING OF THE FLASH NEED TO BE CLARIFIED WITH FW TEAM

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