

# **Agilex<sup>™</sup> 7 FPGA I-Series Transceiver- SoC Development Kit User Guide**

## Contents

---

<b>1. Overview.....</b>	<b>4</b>
1.1. Block Diagram.....	6
1.2. Feature Summary.....	6
1.3. Box Contents.....	7
1.4. Recommended Operating Conditions.....	7
<b>2. Getting Started.....</b>	<b>8</b>
2.1. Before You Begin.....	8
2.2. Handling the Board.....	8
2.3. Software and Driver Installation.....	8
2.3.1. Installing the Quartus Prime Pro Edition Software.....	8
2.3.2. Installing the Intel SoC EDS.....	9
2.3.3. Installing the Development Kit.....	9
2.3.4. Installing the Intel FPGA Download Cable Driver.....	10
<b>3. Development Kit Setup.....</b>	<b>11</b>
3.1. Default Settings.....	11
3.2. Powering Up the Development Kit.....	12
3.3. Performing Board Restore.....	12
3.3.1. Restoring Board System MAX 10 with Default Factory Image.....	13
3.3.2. Restoring Board QSPI Flash with Default Factory Image.....	13
<b>4. Board Test System.....</b>	<b>14</b>
4.1. Set Up BTS GUI Running Environment.....	15
4.1.1. Downloading OpenJDK.....	15
4.1.2. Downloading OpenJFX.....	16
4.1.3. Installing OpenJDK and OpenJFX.....	16
4.1.4. Setting Up the Quartus Prime Software for BTS Operation.....	16
4.1.5. Running BTS GUI.....	17
4.2. Test the Functionality of the Development Kit.....	18
4.2.1. The Bottom Info Bar.....	18
4.2.2. The Configure Menu.....	18
4.2.3. The Sys Info Tab.....	19
4.2.4. The GPIO Tab.....	20
4.2.5. The XCVR Tab.....	22
4.2.6. The Memory Tab.....	31
4.3. Control On-Board Clock through Clock Controller GUI.....	34
4.4. Monitor On-Board Power Regulator through Power Monitor GUI.....	38
4.5. BTS Test Areas.....	39
4.6. Identify Test Pass or Fail based on BTS GUI Test Status.....	39
<b>5. Development Kit Hardware and Configuration.....</b>	<b>40</b>
5.1. Configure FPGA and Access HPS Debug Access Port by JTAG.....	40
5.2. Configure the FPGA Device Using the AS Mode (Default Mode).....	40
5.3. Configure the FPGA Device Using the Avalon-ST Mode.....	40
5.4. Daughter Cards.....	41
5.4.1. HPS Out of Box Experience (OOBE) Daughter Card.....	41

<b>6. Custom Projects for the Development Kit.....</b>	<b>42</b>
6.1. Add SmartVID Settings in the Quartus Prime QSF File.....	42
6.2. Golden Top.....	42
<b>7. Document Revision History for the Agilex 7 FPGA I-Series Transceiver-SoC Development Kit User Guide.....</b>	<b>43</b>
<b>A. Development Kit Components.....</b>	<b>45</b>
A.1. System Management.....	45
A.2. Power.....	47
A.3. Clocks.....	50
A.4. General Input/Output.....	52
A.5. Memory Interfaces.....	56
A.6. Communication Interfaces.....	56
A.7. Daughter Cards.....	60
A.8. Connectors and Cables.....	61
<b>B. Developer Resources.....</b>	<b>62</b>
<b>C. Safety and Regulatory Compliance Information.....</b>	<b>63</b>
C.1. Safety and Regulatory Information.....	63
C.1.1. Safety Warnings.....	64
C.1.2. Safety Cautions.....	65
C.2. Compliance Information.....	68

## 1. Overview

Agilex™ 7 FPGA I-Series Transceiver-SoC Development Kit is a complete design environment that includes both hardware and software you need to develop Agilex 7 FPGA I-Series designs. The board provides a wide range of peripherals and memory interfaces to facilitate the development of Agilex 7 I-Series Transceiver-SoC designs.

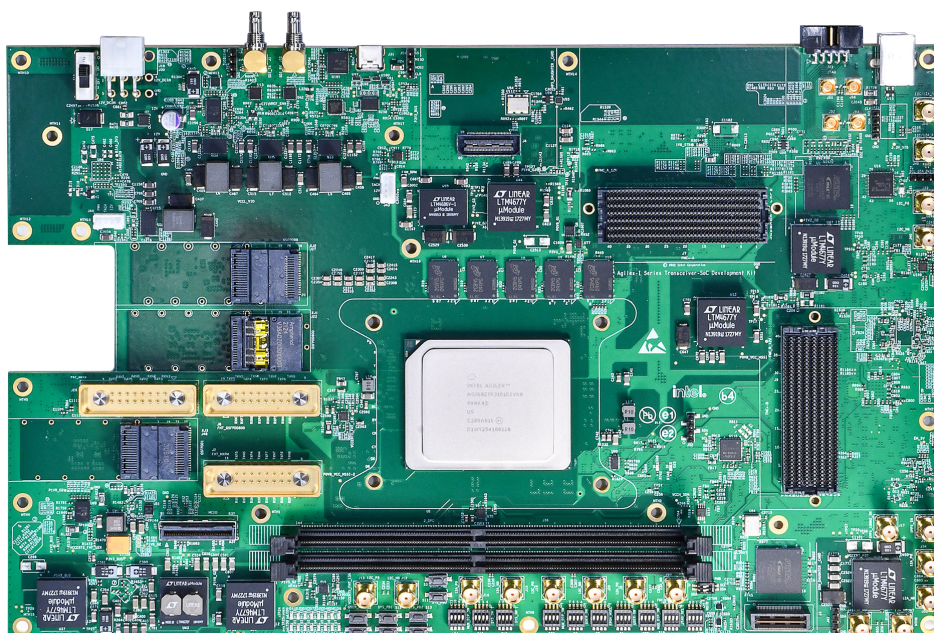
**Table 1. Ordering Information**

Development Kit Version	Ordering Code	Device Part Number	Serial Number Identifier
Agilex 7 FPGA I-Series Transceiver-SoC Development Kit (Production 2 4x F-Tile) (Power Solution 2)	DK-SI-AGI027FC	AGIB027R31B1E1VB	3000001
Agilex 7 FPGA I-Series Transceiver-SoC Development Kit (Production 1 4x F-Tile) (Power Solution 2)	DK-SI-AGI027FA	AGIB027R31B1E1V	2000001
Agilex 7 FPGA I-Series Transceiver-SoC Development Kit (ES1 4x F-Tile) (Power Solution 1)	DK-SI-AGI027FB	AGIB027R31B1E1VAA	0001001
Agilex 7 FPGA I-Series Transceiver-SoC Development Kit (ES 4x F-Tile) (Power Solution 1)	DK-SI-AGI027FES	AGIB027R31B1E2VR0	0000001

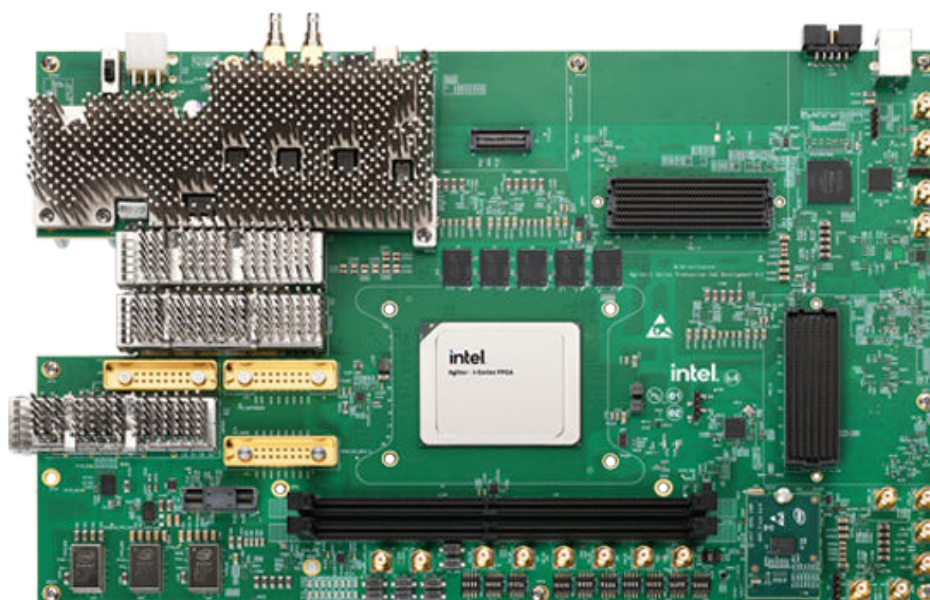
For the board and FPGA capabilities, refer to the *Agilex 7 FPGA and SoC FPGA I-Series* page on the Intel website.

For more information about the *Agilex 7 Device Errata Sheet and User Guidelines (ES-1069)*, contact Intel® Premier Support and quote ID #15011992053.

**Figure 1. Agilex 7 FPGA I-Series Transceiver-SoC Development Kit (Power Solution 2 Board) —Top View**



**Figure 2. Agilex 7 FPGA I-Series Transceiver-SoC Development Kit (Power Solution 1 Board)—Top View**



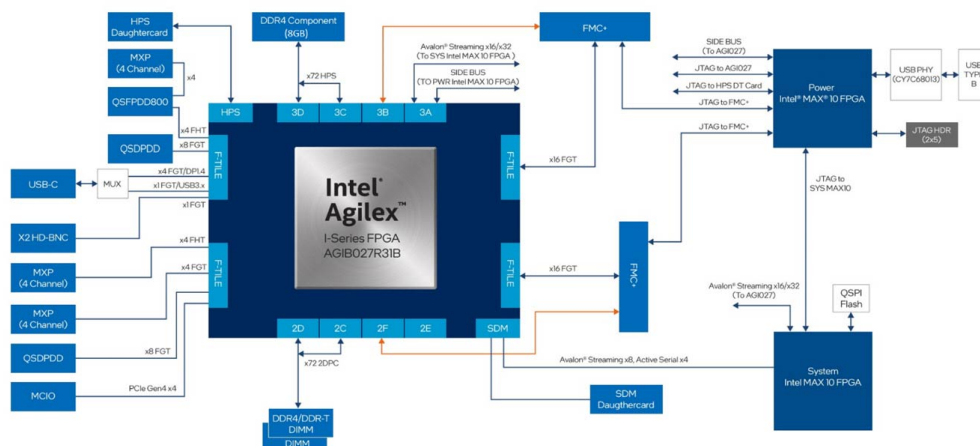
Refer to the *Appendix A—Development Kit Components* section for more details about the components on the Agilex 7 FPGA I-Series Transceiver-SoC Development Kit.

## Related Information

- [Development Kit Components](#) on page 45
- [Agilex 7 FPGA and SoC FPGA I-Series](#)
- [Agilex 7 F-Series and I-Series Known Issue List](#)

### 1.1. Block Diagram

**Figure 3.     Agilex 7 FPGA I-Series Transceiver-SoC Development Kit Block Diagram**



## 1.2. Feature Summary

- Agilix 7 FPGA I-Series, 2.7M LE, 3184B package
- F-Tile 1 (13C)
  - 4 FHT transceiver channels fan out to Quad Small Form Factor Double Density 800 (QSFPDD800)
  - 8 FGT transceiver channels to Quad Small Form Factor Double Density connector
  - 2 FGT transceiver channels to HD-BNC for SDI
  - 4 FGT transceiver as DP2.0<sup>(1)</sup>
  - 1FGT transceiver for USB3.2<sup>(1)</sup>
- F-Tile 2 (13A)
  - 4 FHT transceiver channels (116G) to MXPM
  - 8 FGT transceiver channels (56G) to MXPM
  - 8 FGT transceiver channels to Quad Small Form Factor Double Density connector
  - 4 FGT transceiver channels to MCIO (PCIe\*)

(1) Preliminary

- F-Tile 3 (12C)
  - 16 FGT channels to FMC+
- F-Tile 4 (12A)
  - 16 FGT channels to FMC+
- SR DDR4 2666 (x72 w/ ECC), 16GB
- 8GB SR DDR4-2666 (x72 w/ ECC) component down (HPS)
- IO48 interface for HPS Out of Box Experience (OOBE) daughter cards

### 1.3. Box Contents

- Agilix 7 FPGA I-Series Transceiver-SoC Development Kit
- Single-rank DDR4 DIMM module
- QSPI flash daughter card
- HPS IO48 OOBE daughter card
- NAND daughter card
- USB 2.0 Type B cable
- Ethernet cable
- 240W power adapter and NA/EU/JP/UK cords
- ATX power convert cable - 24 pin to 6 pin

#### Related Information

[Agilix 7 FPGA I-Series Transceiver-SoC Development Kit \(4x F-Tile\) Webpage](#)

### 1.4. Recommended Operating Conditions

**Table 2. Recommended Operating Conditions**

Operating Condition	Range of Values
Ambient operating temperature range	0°C to 30°C
ICC load current	195 A
ICC load transient percentage	200 A/μs
FPGA maximum power supported by active heatsink/fan	160 W <sup>(2)</sup>

#### Related Information

[Handling the Board](#) on page 8

---

<sup>(2)</sup> 160 W for core and 60 W for FGT transceiver.



## 2. Getting Started

---

### 2.1. Before You Begin

You must check the kit contents and inspect the boards to verify that you received all of the items in the box before using the kit of installing the software.

In case any of the items are missing, you must contact Altera before you proceed.

**Important:** Read the [Appendix C.1—Safety and Regulatory Information](#) for safe operation and regulatory adherence.

### 2.2. Handling the Board

When handling the board, it is important to observe static discharge precautions.

**Caution:** Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

**Caution:** This development kit should not be operated in a vibration environment.

### 2.3. Software and Driver Installation

This section explains how to install the following software and driver:

- Quartus® Prime Standard Edition software
- Intel SoC FPGA Embedded Development Software (EDS)
- Agilex 7 FPGA I-Series Transceiver-SoC Development Kit software
- Intel FPGA Download Cable driver

#### 2.3.1. Installing the Quartus Prime Pro Edition Software

1. Download the Quartus Prime Pro Edition software from the [FPGA Software Download Center](#) webpage of the Intel website.
2. Follow the on-screen instructions to complete the installation process. Choose an installation directory that is relative to the Quartus Prime Pro Edition software installation directory.

If you have difficulty installing the Quartus Prime software, refer to the *Altera® FPGA Software Installation and Licensing*.

#### Related Information

- [Quartus Prime Pro Edition User Guide: Getting Started](#)
- [Altera FPGA Software Installation and Licensing](#)



## 2.3.2. Installing the Intel SoC EDS

The Intel SoC FPGA Embedded Development Suite (SoC EDS) is a comprehensive software tool suite for embedded software development on Altera system-on-chip (SoC) devices. It contains development tools, utility programs, run-time software, and application examples to expedite firmware and application software of SoC embedded systems.

As a part of the Intel SoC EDS, the Arm\* Development Studio 5 (DS-5) Intel SoC FPGA Edition Toolkit provides a comprehensive set of embedded development tools for Altera's SoC FPGAs.

**Note:** Use the Quartus Prime Pro Edition software version 19.4 or later for this development kit test and debug.

For more information and steps to install the Intel SoC EDS Tool Suite, refer to the links below.

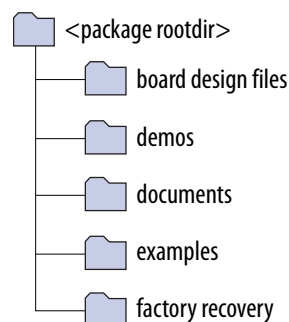
### Related Information

- [Intel SoC FPGA Embedded Development Suite \(SoC EDS\) User Guide](#)
- [Arm\\* Development Studio for Intel SoC FPGA](#)

## 2.3.3. Installing the Development Kit

1. Download the Agilex 7 FPGA I-Series Transceiver-SoC Development Kit installer package from the [Agilex 7 FPGA I-Series Transceiver-SoC Development Kit \(4x F-Tile\)](#) webpage on the Intel website.
2. Unzip the Agilex 7 FPGA I-Series Transceiver-SoC Development Kit installer package. The package creates the directory structure shown in the figure below.

**Figure 4. Agilex 7 FPGA I-Series Transceiver-SoC Development Kit Directory Structure**



3. For the latest issues and release notes, Altera recommends that you review the `readme.txt` located in the root directory of the kit installation.

**Table 3. Installed Development Kit Directory Description**

Directory Name	Description of Directory Contents
board_design_files	Contains schematic, layout, assembly, and Bill of Material (BOM) board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications when available.
<i>continued...</i>	

Directory Name	Description of Directory Contents
documents	Contains the development kit documentation.
examples	Contains the sample design files for the Agilex 7 FPGA I-Series Transceiver-SoC Development Kit: <ul style="list-style-type: none"> <li>Board Test System (BTS): BTS GUI, Clock GUI, and Power GUI</li> <li>Golden Top project for pinout assignments management</li> <li>Design Examples: Memory, XCVR, and GPIO</li> </ul>
factory_recovery	Contains the original image/binary programmed onto the board before shipment. Use this image to restore the board with its original factory content.

### 2.3.4. Installing the Intel FPGA Download Cable Driver

The Agilex 7 FPGA I-Series Transceiver-SoC Development Kit includes onboard Intel FPGA Download Cable circuits for FPGA and system MAX<sup>®</sup> 10 programming. However, for the host computer and board to communicate, you must install the Intel FPGA Download Cable driver on the host computer.

Installation instructions for the Intel FPGA Download Cable driver for your operating system are available on the Intel website.

On the Intel website, navigate to the *Cable and Adapter Drivers Information* link to locate the table entry for your configuration and click the link to access the instructions.

#### Related Information

- [Cable and Adapter Drivers Information](#)
- [Intel FPGA Download Cable User Guide](#)

## 3. Development Kit Setup

The instructions in this chapter explain how to setup the Agilex 7 FPGA I-Series Transceiver-SoC Development Kit for specific use cases.

### 3.1. Default Settings

The Agilex 7 FPGA I-Series Transceiver-SoC Development Kit ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be correctly configured with the default settings, follow the instructions in the factory default switch settings table to return to its factory settings before proceeding ahead.

**Note:** "X" refers to Don't Care in the table below.

**Note:** Do not set the switches when the power is on. Only set the switches after the power is off.

**Table 4. Factory Default Switch Settings**

Switch	Default Position	Default Function
S19[1:4]	OFF/OFF/ON/ON	System MAX 10 and FPGA selected in the JTAG chain.
S20[1:4]	ON/ON/ON/ON	Mode 1: On-board Intel download circuit act as the only JTAG master. Chained HPS with SDM nodes internally.
S9[1:4]	ON/OFF/OFF/X	Configuration mode setting bits: AS - Fast mode
S10[1:4]	ON/ON/ON/ON	SYS_SW[0:3] <ul style="list-style-type: none"> <li>• SYS_SW[0]—Factory Loadn</li> <li>• '0'—Load image from Page 0 of the QSPI</li> <li>• SYS_SW[1]—MUX_SEL1</li> <li>• SYS_SW[2]—MUX_SEL7</li> <li>• SYS_SW[3]—MUX_SEL9</li> </ul>
<i>continued...</i>		

Switch	Default Position	Default Function
S15[1:4]	ON/ON/ON/OFF	SYS_SW[4:7] <ul style="list-style-type: none"> <li>• SYS_SW[4]—MUX_SEL_ZL</li> <li>• SYS_SW[5]—FMC-A PCIe RP/EP Select               <ul style="list-style-type: none"> <li>— "0": RP (Default)</li> <li>— "1": EP</li> </ul> </li> <li>• SYS_SW[6]—FMC-B PCIe RP/EP Select               <ul style="list-style-type: none"> <li>— "0": RP (Default)</li> <li>— "1": EP</li> </ul> </li> <li>• SYS_SW[7]—MCIO PCIe RP/EP Select               <ul style="list-style-type: none"> <li>— "0": RP</li> <li>— "1": EP (Default)</li> </ul> </li> </ul>
S1[1:4]	OFF/OFF/OFF/OFF	User Switch [0:3]
S6[1:4]	OFF/OFF/OFF/OFF	User Switch [4:7]
S22[1:4]	ON/ON/ON/ON	MUX_DIP_SW[0:3] <ul style="list-style-type: none"> <li>• MUX_DIP_SW0—MUX_SEL2</li> <li>• MUX_DIP_SW1—MUX_SEL3</li> <li>• MUX_DIP_SW2—MUX_SEL4</li> <li>• MUX_DIP_SW3—MUX_SEL5</li> </ul> Set to "ON" by default to select on-board clock as input.
S23[1:4]	ON/ON/ON/ON	MUX_DIP_SW[4:7] <ul style="list-style-type: none"> <li>• MUX_DIP_SW4—MUX_SEL10</li> <li>• MUX_DIP_SW5—MUX_SEL11</li> <li>• MUX_DIP_SW6—MUX_SEL12</li> <li>• MUX_DIP_SW7—MUX_SEL14</li> </ul> Set "0"/closed by default for on-board clock as input.
S4[1:4]	ON/ON/ON/ON	MUX_DIP_SW[8:11] <ul style="list-style-type: none"> <li>• MUX_DIP_SW8—MUX_SEL13</li> <li>• MUX_DIP_SW9—MUX_SEL6</li> <li>• MUX_DIP_SW10—MUX_SEL0</li> <li>• MUX_DIP_SW11—MUX_SEL8</li> </ul> Set "0"/closed by default for on-board clock as input.

## 3.2. Powering Up the Development Kit

1. Use the provided 240 W power adapter to supply power through J30.
2. After power adapter is plugged into J30 and switch S18 is set to the **ON** position, the LED D22 illuminates, indicating that the board power up successfully. If the LED D22 is not turned **ON**, it indicates that one or more power supply is incorrect.

## 3.3. Performing Board Restore

This development kit ships with bts\_config design examples stored in the QSPI flash device. You can perform board restore by following the instructions below through the Quartus Prime Programmer GUI.

### 3.3.1. Restoring Board System MAX 10 with Default Factory Image

1. Open the Quartus Prime Programmer GUI, and detect the JTAG chain after the system MAX 10 is restored.
2. Attach the system MAX 10 image on the system MAX 10 part.
3. Select programming options and click program button.

*Note:* Once you plug Intel FPGA Download Cable between J11 and PC, the Intel on-board download cable circuit is disabled automatically.

### 3.3.2. Restoring Board QSPI Flash with Default Factory Image

*Note:* The QSPI flash is pre-programmed with 4 pages of images. Follow the steps to overwrite the Avalon® streaming interface x8 configuration mode image.

1. Ensure that MSEL[2:0] is OFF (JTAG mode) before powering up the board.
2. Open Quartus Prime Programmer GUI, detect JTAG chain.
3. Change VTAP10 to 10M50DAF256, attach flash device of QSPI\_2Gb.
4. Attach the Avalon streaming interface x8 configuration mode image to QSPI\_2Gb.
5. Select program/configure options and click **Start** button.
6. Power off the board after programming the flash successfully, set MSEL[2:0] OFF OFF ON (Avalon streaming interface x8 configuration mode).

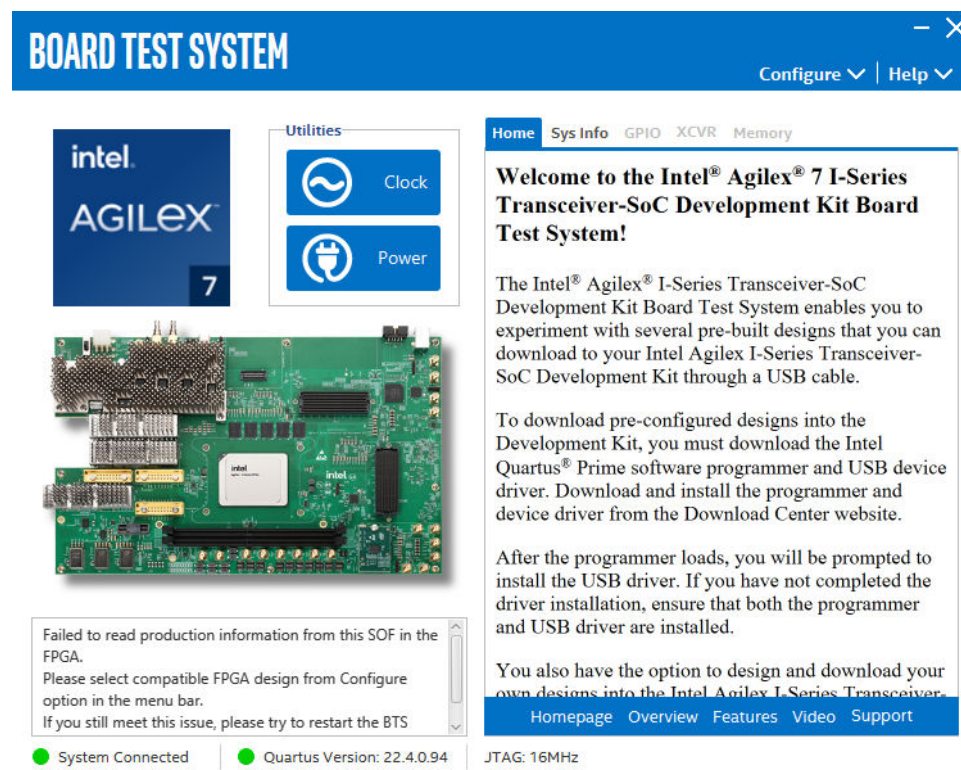
## 4. Board Test System

The Agilex 7 FPGA I-Series Transceiver-SoC Development Kit includes design examples and the board test system (BTS) GUI to test the functionality of this board. The BTS provides an easy-to-use interface to alter functional settings and observe results. You can use the BTS to test board components, modify functional parameters, observe performance, and measure power usage.

While using the BTS, you reconfigure the FPGA several times with test designs specific to the functionality that you are testing. The BTS is also useful as a reference for designing systems. The BTS communicates over the JTAG bus to a test design running in the Agilex 7 FPGA I-Series.

The following figure shows the graphical user interface (GUI) of a board that is in factory configuration.

**Figure 5. BTS GUI (Intel Enpirion®) DK-SI-AGI027FB and DK-SI-AGI027FES**

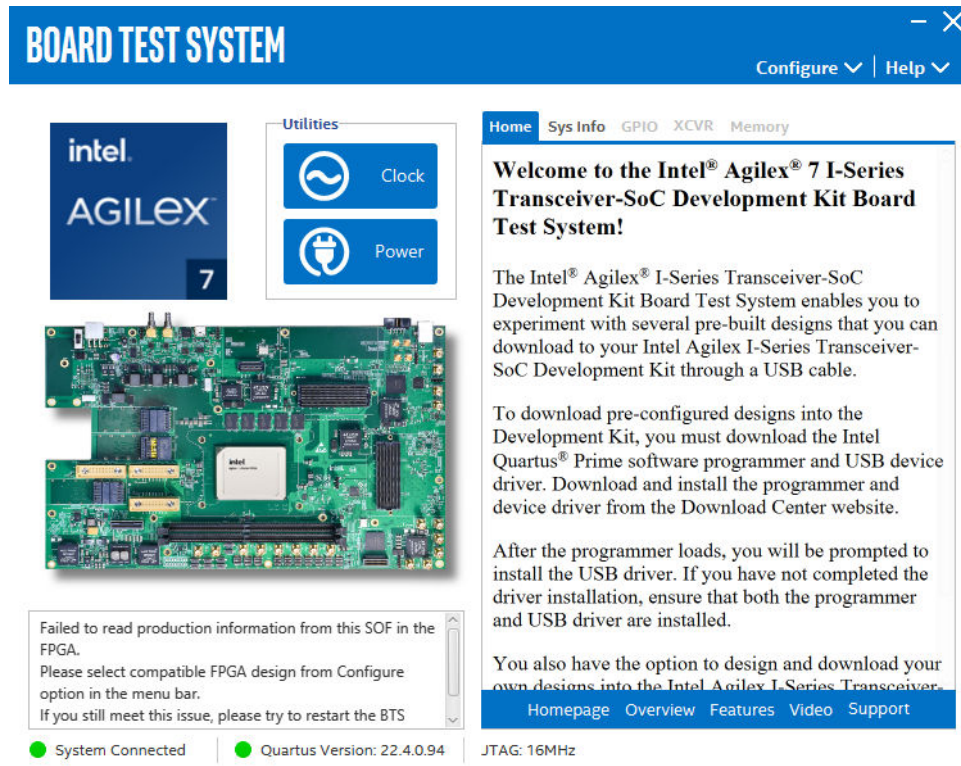


© Altera Corporation. Altera, the Altera logo, the 'a' logo, and other Altera marks are trademarks of Altera Corporation. Altera and Intel warrant performance of its FPGA and semiconductor products to current specifications in accordance with Altera's or Intel's standard warranty as applicable, but reserves the right to make changes to any products and services at any time without notice. Altera and Intel assume no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera or Intel. Altera and Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

\*Other names and brands may be claimed as the property of others.

**ISO  
9001:2015  
Registered**

Figure 6. BTS GUI (Not Intel Enpirion®) DK-SI-AGI027FA and DK-SI-AGI027FC



## 4.1. Set Up BTS GUI Running Environment

To run BTS GUI, including Power Monitor and Clock Controller GUI, you need to download and install Java runtime including OpenJDK and OpenJFX on your systems and set up the running environment. This is a one-time procedure, so if you have already completed it before, you do not need to do it again unless the Java version upgrade is needed.

### 4.1.1. Downloading OpenJDK

1. Download the Temurin\* OpenJDK. Refer to the related information for the download link.
2. Select Architecture x64, Package Type JRE, and Version 11.
  - a. For the **Windows** system, choose the `JRE.zip` format file.
  - b. For the **Linux** system, choose the `JRE.tar.gz` format file.

*Note:* Download the latest version to update the JDK version. The following version was tested: 11.0.21+9

#### Related Information

[Temurin\\* OpenJDK](#)



### 4.1.2. Downloading OpenJFX

1. Download the Gluon\* OpenJFX. Refer to the related information for the download link.
2. Select JavaFX version 17.0.2.
  - a. For the **Windows** system, download the JavaFX Windows x64 SDK.
  - b. For the **Linux** system, download the JavaFX Linux x64 SDK.

#### Related Information

[Gluon\\* OpenJFX](#)

### 4.1.3. Installing OpenJDK and OpenJFX

You have two downloaded compressed files. Follow these steps to install them.

Follow these steps to install the downloaded zip files:

1. On **Windows** system, Altera recommends you to unzip the files and put them in the following directory:

- C:\Program Files\Java\jre
- C:\Program Files\Java\jfx

*Note:* The unzipped folder name of JRE is `jdk-11.0.xx+x-jre` (for example, `jdk-11.0.15+10-jre`). Rename it to `jre`.

The unzipped folder name of JFX is `javafx-sdk-17.0.2`. Rename it to `jfx`.

2. On the **Linux** system, Altera recommends that you unzip the files and rename the folders using the following commands:

```
# unzip openjfx-17.0.2_linux-x64_bin-sdk.zip -d /opt/Java/
# tar zxvf OpenJDK11U-jre_x64_linux_hotspot_11.0.15_10.tar.gz -C /opt/Java/
# cd /opt/Java
# mv javafx-sdk-17.0.2 jfx
# mv jdk-11.0.15+10-jre jre
```

You have the following two directories on your **Linux** system:

- /opt/Java/jre
- /opt/Java/jfx

### 4.1.4. Setting Up the Quartus Prime Software for BTS Operation

You must install the Quartus Prime software to support the silicon on the development kit. The recommended version is located in the `README.txt` file in the `examples\board_test_system` directory. If you choose to install individual files, you must install Agilex 7 Device Support.

The BTS communicates over JTAG to a test design running in the FPGA. The BTS shares the JTAG with other applications such as the Nios® II JTAG Debug Module and the Signal Tap Logic Analyzer. Altera recommends closing other applications before using BTS, as the GUI is designed based on the Quartus Prime software.

The BTS relies on the Quartus Prime software's specific library. Before running the BTS, open the Quartus Prime software to automatically set the environment variable `QUARTUS_ROOTDIR`. You can also change it through **Environment Variables** in the **System Properties** in Windows\*. The BTS uses this environment variable to locate the Quartus Prime library.

#### 4.1.5. Running BTS GUI

With the power to the board off, follow these steps:

1. Connect the USB cable to your PC and the board.
2. Check the development board switches and jumpers are set according to your preferences. Refer to [Development Kit Setup](#) section. In most cases, BTS requires the system MAX 10 and Agilex 7 FPGA on the JTAG chain while the Clock Controller and Power Monitor require only the system MAX 10.
3. Check the external modules status: MXPM cable/QSFP/QSFPDD/FMC/DIMM.
4. Turn on the board power switch.

**Note:** To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. You must attach the USB cable and power on the board for BTS to run correctly.

Navigate to the `<packagedir>\examples\board_test_system` directory to run BTS. The BTS release folder always includes the following files.

**Figure 7. BTS Folder**

<input type="checkbox"/> Name	Type
image	File folder
lib	File folder
BoardTestSystem.bat	Windows Batch File
BoardTestSystem.sh	Shell Script
bts.jar	JAR File
ClockController.bat	Windows Batch File
ClockController.sh	Shell Script
PowerMonitor.bat	Windows Batch File
PowerMonitor.sh	Shell Script
README.TXT	TXT File

You can run BTS GUI easily with the following scripts.

1. On **Windows** system, double click the `.bat` files to run BTS, Clock Controller, or Power Monitor GUI.

**Figure 8. Windows Console**

```

C:\windows\System32\cmd.exe
*****
*      BOARD TEST SYSTEM      *
*****

Board Test System Starting...

D:\board_test_system>"C:\Program Files\Java\jre\bin\java.exe" --module-path
"C:\Program Files\Java\jfx\lib" --add-modules javafx.controls,javafx.fxml,
javafx.web -jar bts.jar
Success!
Starting application on Windows 10...

```

2. On **Linux** system, you need to run the shell script with root privilege.

**Figure 9. Linux Console**

```

root@sh_lab5_1:/board_test_system
File Edit View Search Terminal Help
root@sh_lab5_1: /board_test_system 08:54:16
# sh BoardTestSystem.sh
*****
*      BOARD TEST SYSTEM      *
*****

Board Test System Starting...
Success!
Starting application on Linux...

```

*Note:* The .bat or shell script checks the Java environment settings, copies necessary files, and gives some prompts if the environment is not set up correctly.

The GUI displays the application tab corresponding to the design running in the FPGA. If the design loaded in the FPGA is not supported, it prompts a message to configure your board with a valid BTS design. Refer to [The Configure Menu](#).

## 4.2. Test the Functionality of the Development Kit

This section describes each control in the BTS.

### 4.2.1. The Bottom Info Bar

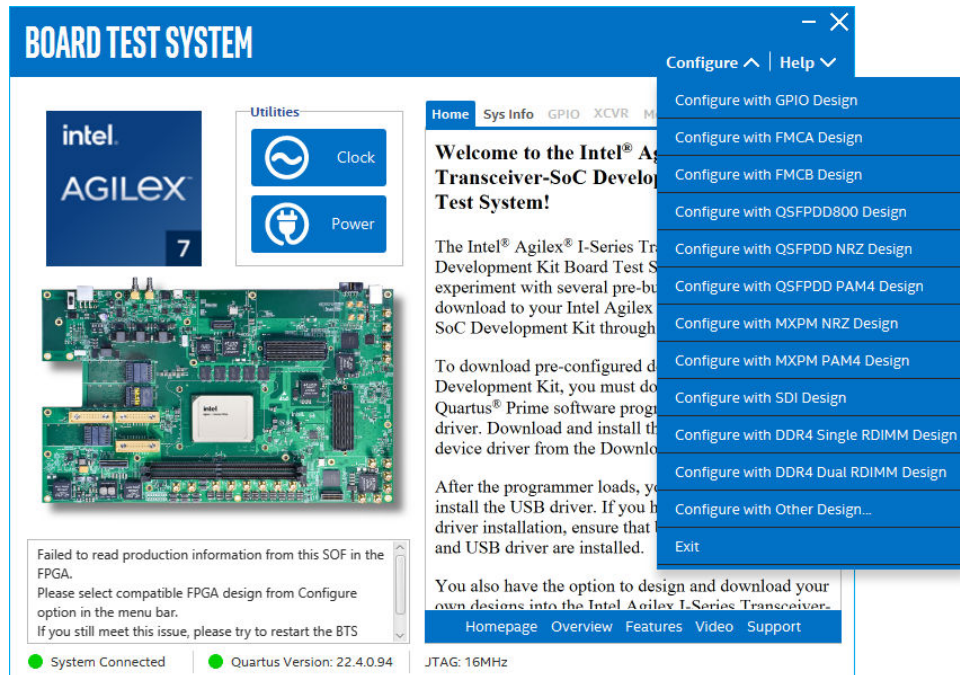
The bottom information bar shows the status of the system connection, the Quartus Prime version and the JTAG clock.

- **System Connected/Disconnected:** Shows if the board is connected to the system. The green sign turns gray if the board becomes disconnected.
- **Quartus Prime Version:** Displays the current Quartus Prime version installed and active on your system. The text turns red if your version is older than the required version. Change the QUARTUS\_ROOTDIR environment variable if you have installed the right version but the active version does not meet the requirement.
- **JTAG:** Displays the JTAG clock frequency.

### 4.2.2. The Configure Menu

Use the Configure Menu to select the design you want to use. Each design example tests different functionality that corresponds to one or more application tabs.

Figure 10. The Configure Menu



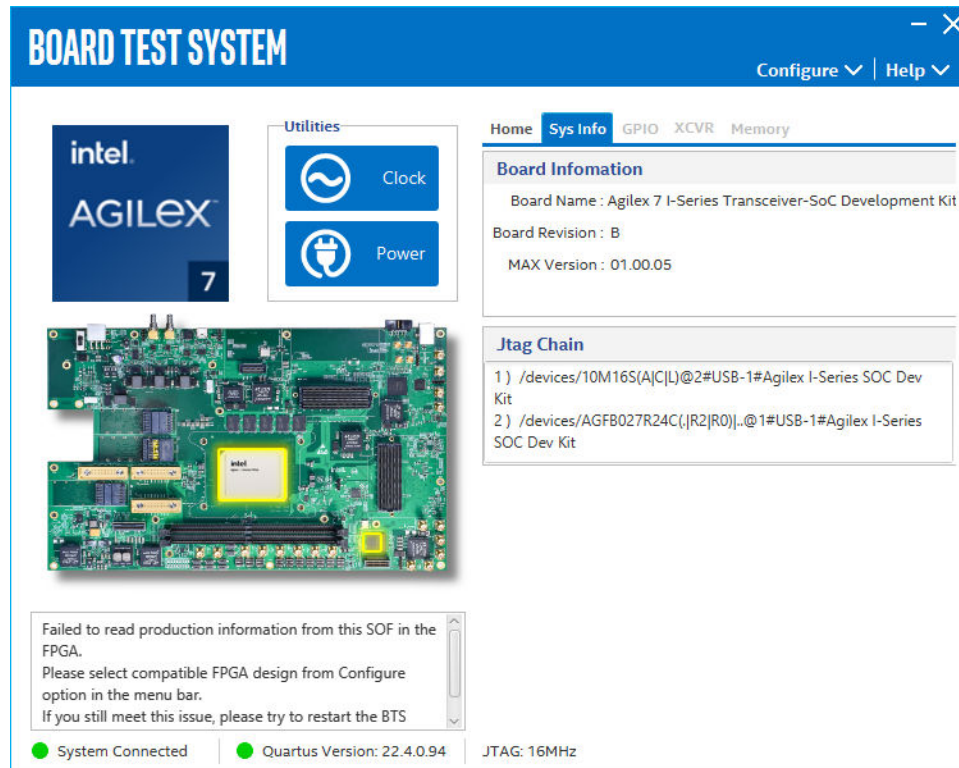
To configure the FPGA with a test system design, follow these steps:

1. On the **Configure** menu, click the **Configure** command that corresponds to the functionality you want to test.
2. In the dialog box that appears, click **Configure** to download the corresponding design's SRAM Object File (.sof) to the FPGA. The download process usually takes less than a minute.
3. When configuration finishes, the design begins running in the FPGA. The corresponding GUI application tabs that interface with the design are now enabled. If you use the Quartus Prime Programmer for configuration, instead of the BTS GUI, you might need to restart the GUI.

#### 4.2.3. The Sys Info Tab

The **Sys Info** tab shows information about the board's current configuration. The tab displays the board information, JTAG Chain devices and other details stored on the board.

**Figure 11. The Sys Info Tab**



The following sections describe the controls on the System Info tab.

### Board Information

The board information control displays static information about your board.

- **Board Name:** Indicates the official name of the board given by the BTS.
- **Board Revision:** Indicates the revision of the board.
- **MAX Version:** Indicates the version of the system MAX 10.

### JTAG Chain

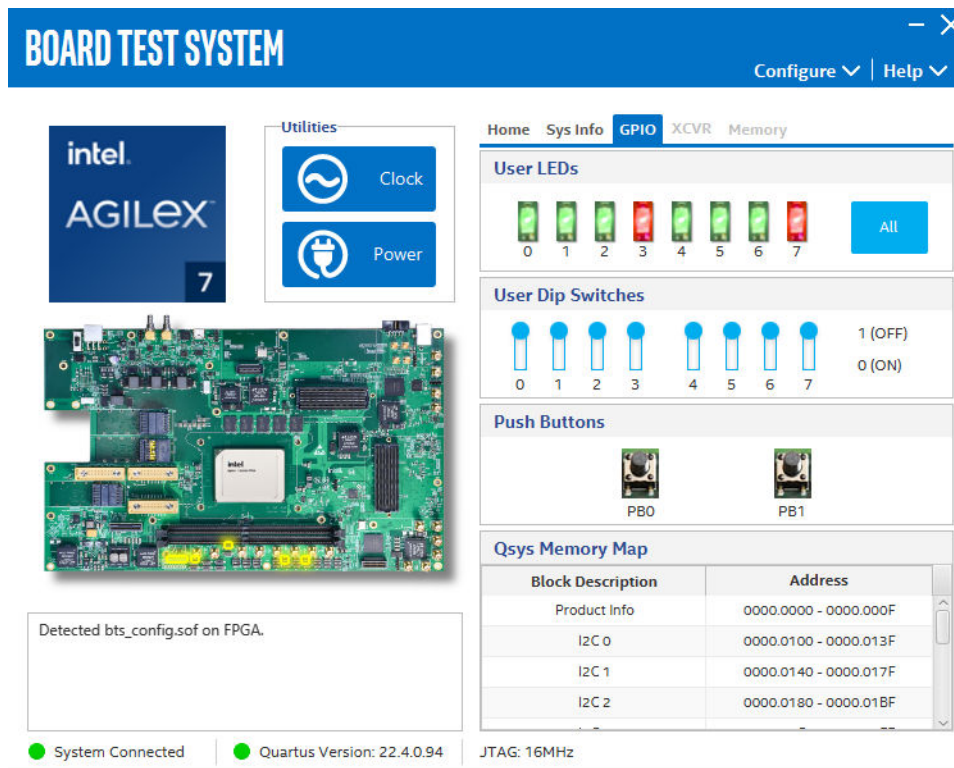
The JTAG chain control shows all the devices currently in the JTAG chain.

**Note:** You should place the system MAX 10 and FPGA in the JTAG chain when running the BTS GUI.

## 4.2.4. The GPIO Tab

The **GPIO** tab allows you to interact with all the general-purpose user I/O components on your board. You can turn LEDs on or off and see the status of push buttons and dip switches.

Figure 12. The GPIO Tab



The following sections describe the controls on the **GPIO** tab.

### User LEDs

The User LEDs control displays the current state of the user LEDs. Toggle the LED buttons to turn the board LEDs on and off. Click the All button to reverse the state of all the LEDs.

### User Dip Switches

The User Dip Switches control display the status of the USER\_SW[0:3] (S1) and USER\_SW[4:7] (S6).

### Push Buttons

The Push Button control shows the status of PB0 and PB1.

### Qsys Memory Map

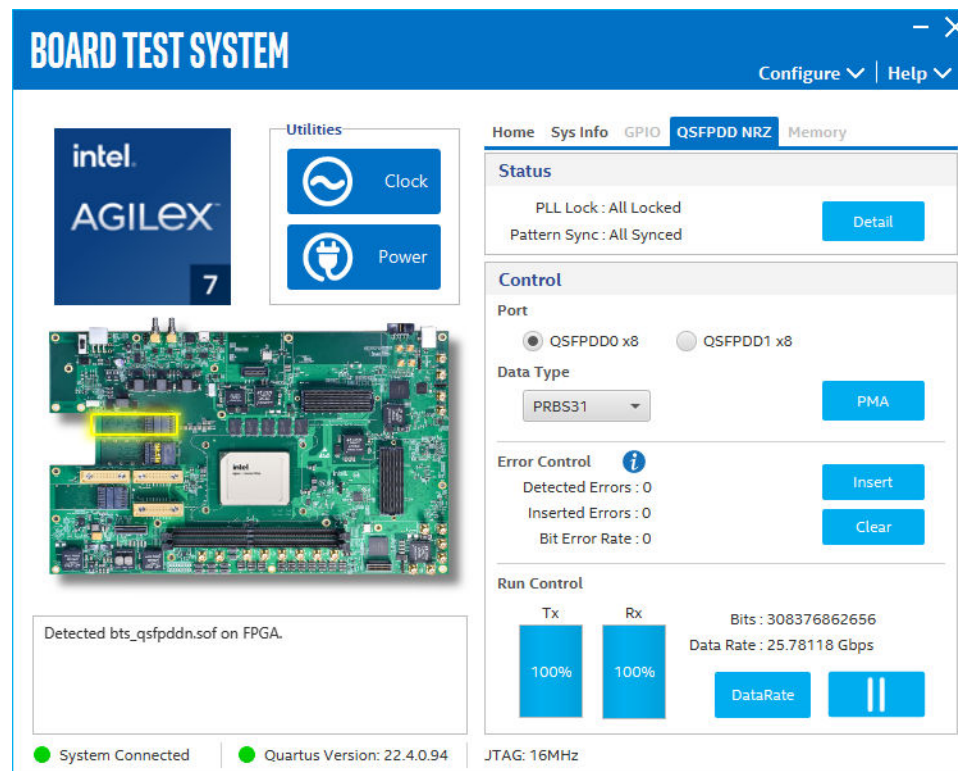
The Qsys Memory Map control shows the memory map of `bts_config.sof` design running on your board.

## 4.2.5. The XCVR Tab

The **XCVR** tab allows you to run transceiver tests on your board. You can run the test using either electrical loopback modules or optical fiber modules.

### 4.2.5.1. The QSFPDD NRZ Tab

**Figure 13.** The QSFPDD NRZ Tab



The following sections describe controls in the **QSFPDD NRZ** tab.

#### Status

The Status control displays the following status information during the loopback test:

- **PLL lock:** Shows the PLL locked or unlocked state.
- **Pattern Sync:** Shows the pattern synced or not state. The pattern is considered synced when the start of the data sequence is detected.
- **Detail:** Shows the PLL lock and pattern sync status of each channel. The number of the error bits of each channel can be found here.



**Figure 14. QSFPDD NRZ - PLL and Pattern Status**

Channel	PLL Lock Status	Pattern Sync Status	Errors	Error Rate
0	Locked	Synced	0	0
1	Locked	Synced	0	0
2	Locked	Synced	0	0
3	Locked	Synced	0	0
4	Locked	Synced	0	0
5	Locked	Synced	0	0
6	Locked	Synced	0	0
7	Locked	Synced	0	0

### Control

Use the following controls to select an interface to apply PMA settings, data type, and error control:

- **QSFPDD0 x8**
- **QSFPDD1 x8**

### PMA Setting

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback:** Displays the signal status between the transmitter and the receiver.
- **VOD:** Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap:**
  - **Pre-tap 1:** Specifies the amount of pre-emphasis on the first pre-tap of the transmitter buffer.
  - **Pre-tap 2:** Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
  - **Post-tap 1:** Specifies the amount of pre-emphasis on the post-tap of the transmitter buffer.

**Figure 15. QSFPDD NRZ-PMA Setting**

### Data Type

The Data Type control specifies the type of data pattern contained in the transactions. Select the following available data types for analysis:

- **PRBS7**: Pseudo-random 7-bit binary sequences
- **PRBS15**: Pseudo-random 15-bit binary sequences
- **PRBS23**: Pseudo-random 23-bit binary sequences
- **PRBS31**: Pseudo-random 31-bit binary sequences (default)

### Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors**: Displays the number of data errors detected in the received bit stream.
- **Inserted Errors**: Displays the number of errors inserted into the transmit data stream.
- **Bit Error Rate**: Calculates the bit error rate of the transmit data stream.
- **Insert**: Insert a one-word error into the transmit data stream each time you click the button. **Insert** Error is only enabled during transaction performance analysis.
- **Clear**: Resets the **Detected Errors** counter and **Inserted Errors** counter to zeros.

### Run Control

- **TX and RX performance bars**: Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Start**: This control initiates the loopback tests.
- **Data Rate**: Displays the XCVR type and data rate of each channel.

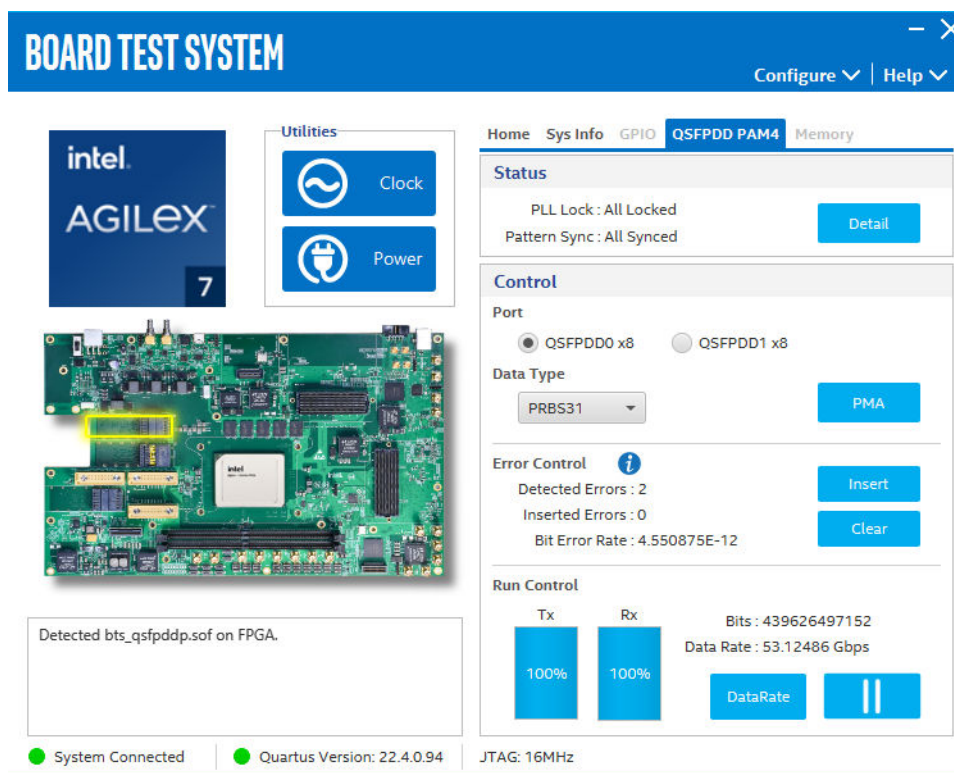
**Figure 16. QSFPDD NRZ - Data Rate**

Data Rate		
Channel	XCVR Type	Frequency
0	F-Tile FGT	24.99994 Gbps
1	F-Tile FGT	24.99994 Gbps
2	F-Tile FGT	24.99994 Gbps
3	F-Tile FGT	24.99994 Gbps
4	F-Tile FGT	24.99994 Gbps
5	F-Tile FGT	24.99994 Gbps
6	F-Tile FGT	24.99994 Gbps
7	F-Tile FGT	24.99994 Gbps

#### 4.2.5.2. The QSFPDD PAM4 Tab

Similar control functions with the **QSFPDD NRZ** tab.

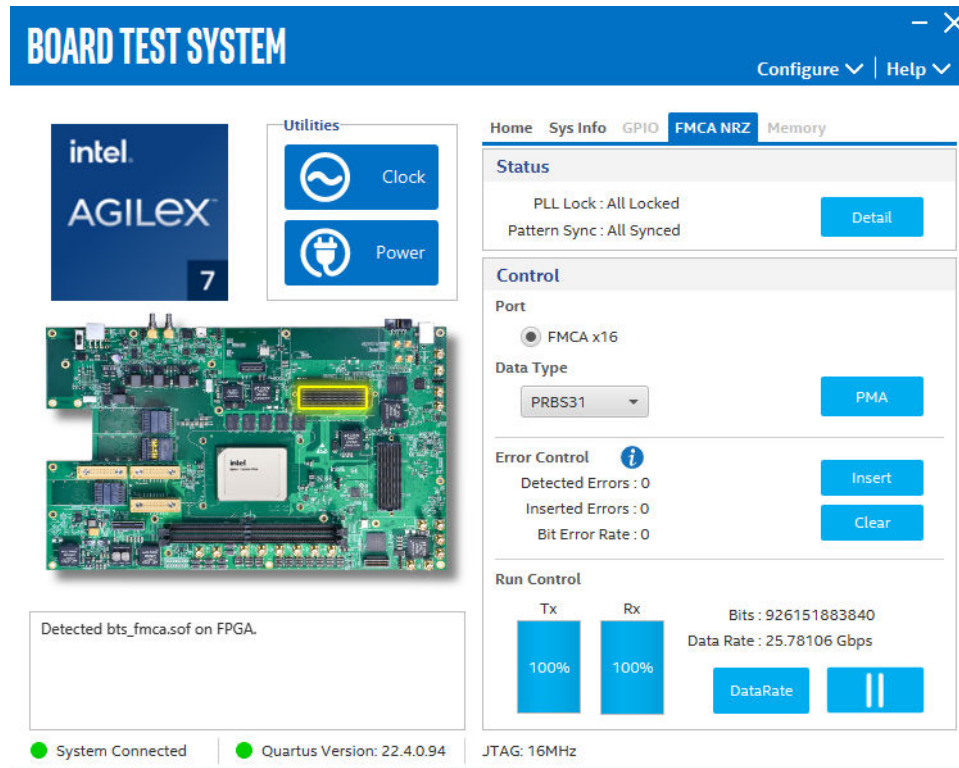
Figure 17. The QSFDD PAM4 Tab



#### 4.2.5.3. The FMCA NRZ Tab

Similar control functions with the **QSFDD NRZ** tab except for the port selection.

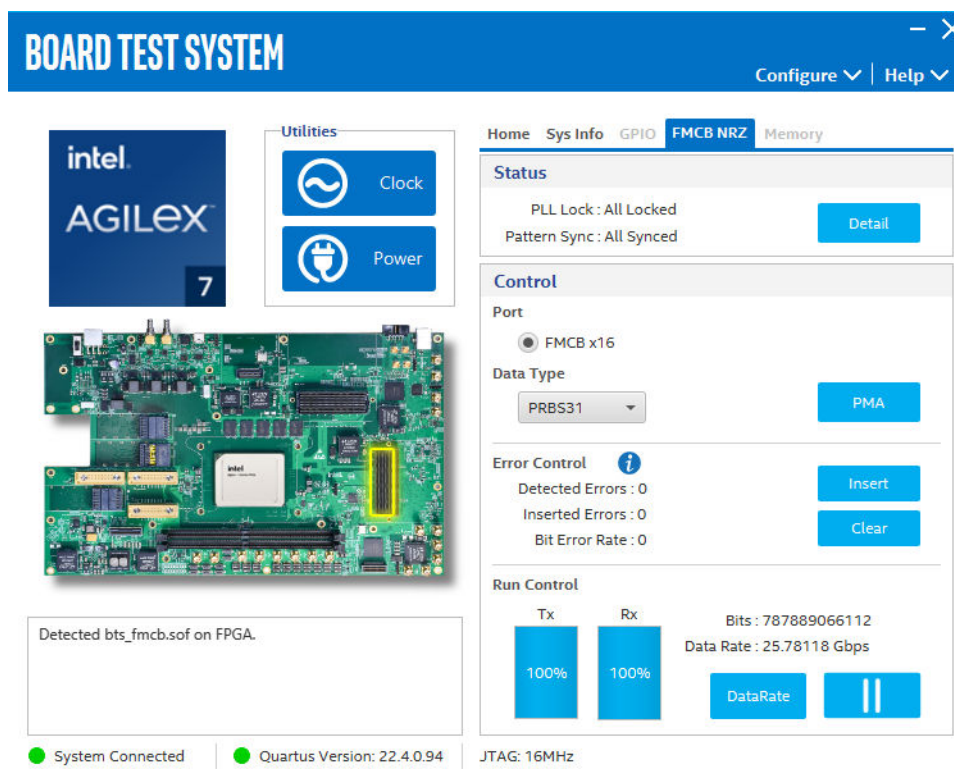
**Figure 18. The FMCA NRZ Tab**



#### 4.2.5.4. The FMCB NRZ Tab

Similar control functions with the **QSPDD NRZ** tab except for the port selection.

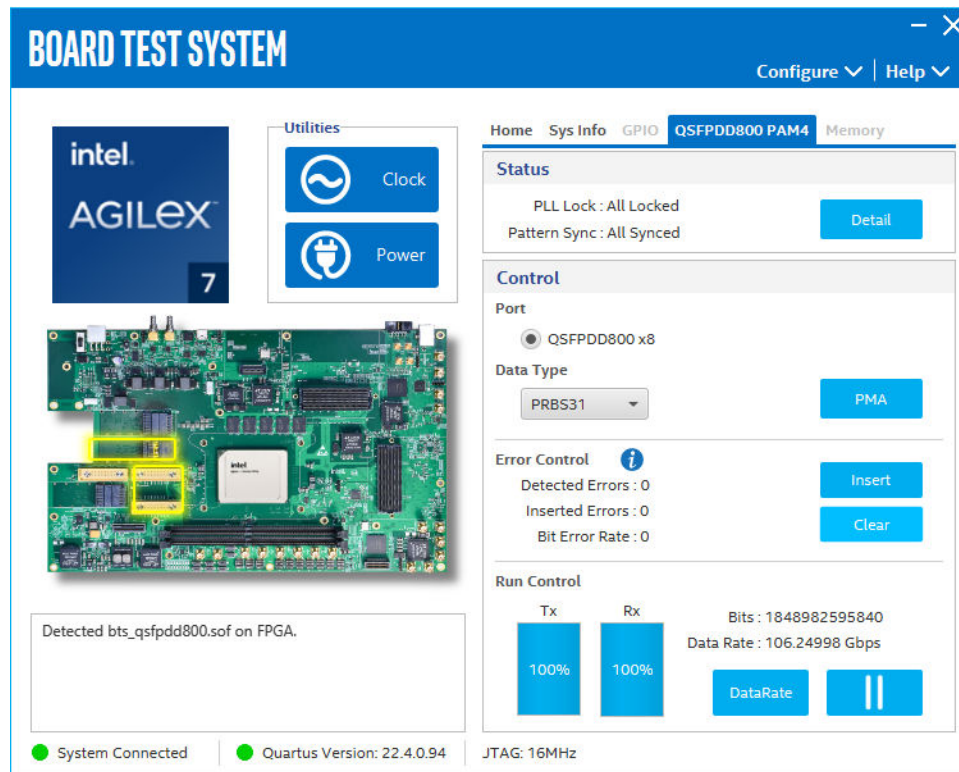
Figure 19. The FMCB NRZ Tab



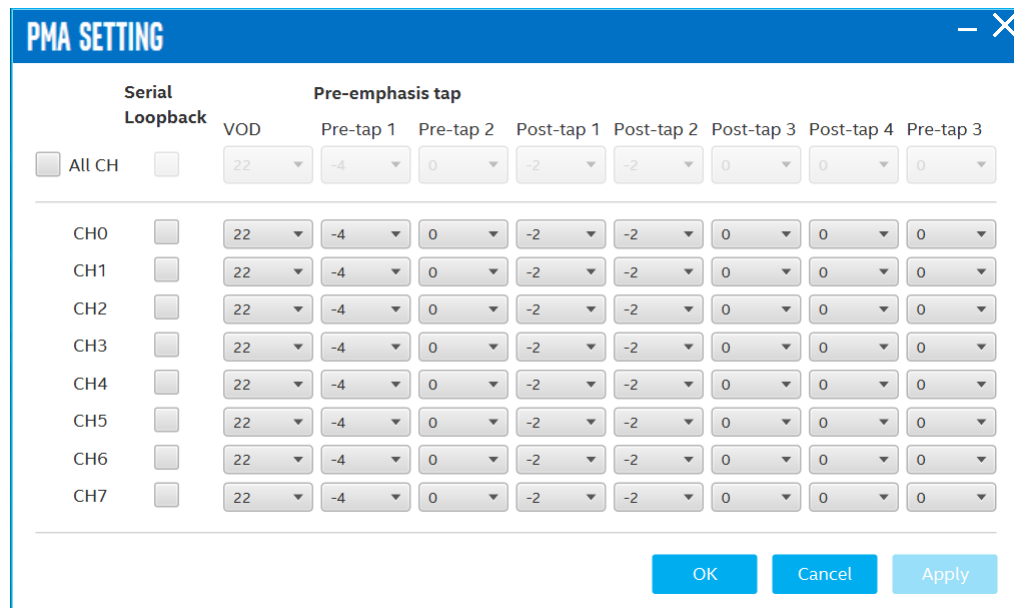
#### 4.2.5.5. The QSPDD800 PAM4 Tab

Similar control functions with the **QSPDD NRZ** tab.

**Figure 20. The QSFDD800 PAM4 Tab**



**Figure 21. The QSFDD800 PAM4 Tab - PMA Setting**



### PMA Setting

In addition to the PMA settings listed in Figure: *QSFPDD NRZ-PMA Setting*, additional settings are available for the F-Tile FHT PMA. The PMA is set to the default values in the PAM4 designs.

- **Pre-emphasis tap:**
  - **Post-tap 2:** Specifies the amount of pre-emphasis on the second post-tap of the transmitter buffer.
  - **Post-tap 3:** Specifies the amount of pre-emphasis on the third post-tap of the transmitter buffer.
  - **Post-tap 4:** Specifies the amount of pre-emphasis on the fourth post-tap of the transmitter buffer.
  - **Pre-tap 3:** Specifies the amount of pre-emphasis on the third pre-tap of the transmitter buffer.

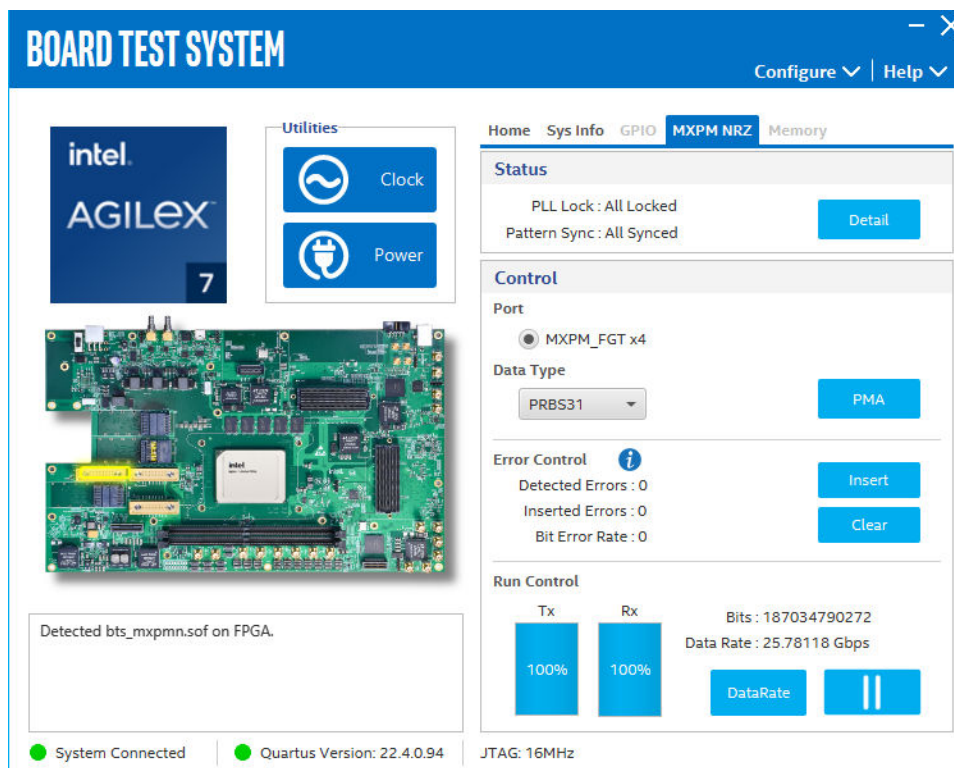
### Related Information

The QSFPDD NRZ Tab on page 22

#### 4.2.5.6. The MXPM NRZ Tab

Similar control functions with the **QSFPDD NRZ** tab except for the port selection.

**Figure 22. The MXPM NRZ Tab**

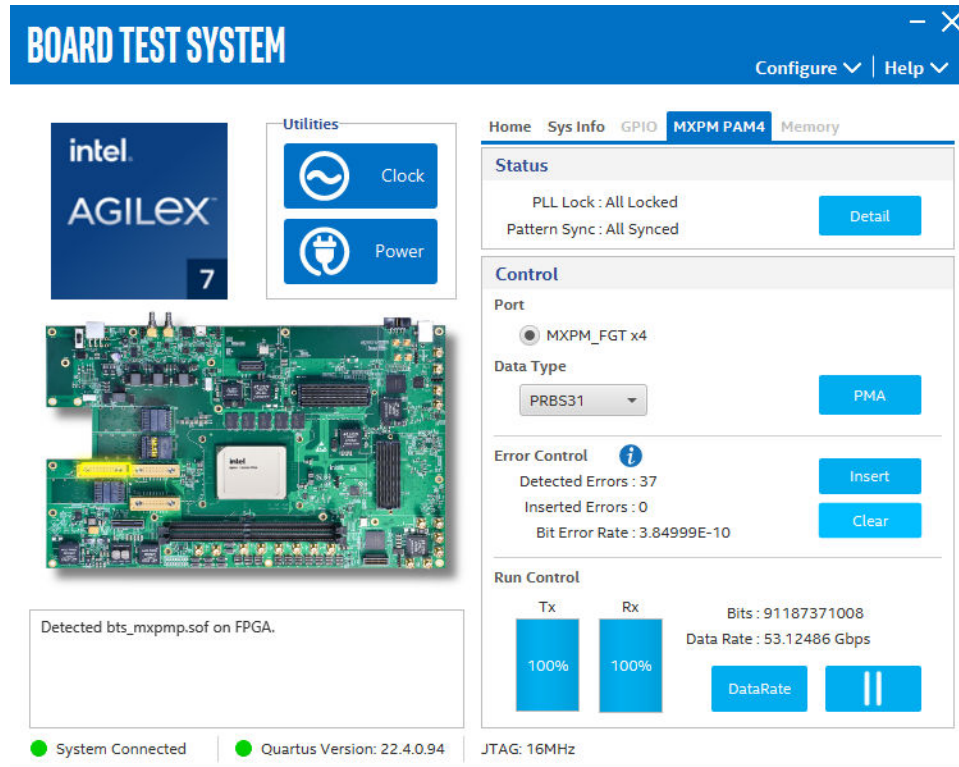




#### 4.2.5.7. The MXPM PAM4 Tab

Similar control functions with the **QSFPDD NRZ** tab.

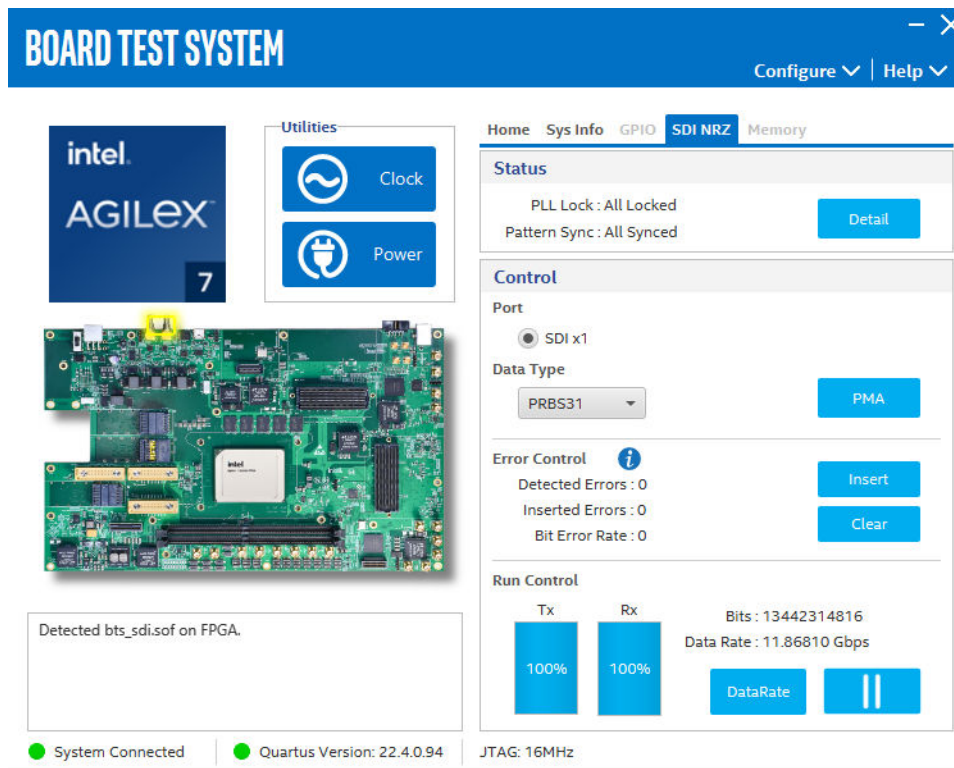
**Figure 23. The MXPM PAM4 Tab**



#### 4.2.5.8. The SDI Tab

Similar control functions with the **QSFPDD NRZ** tab.

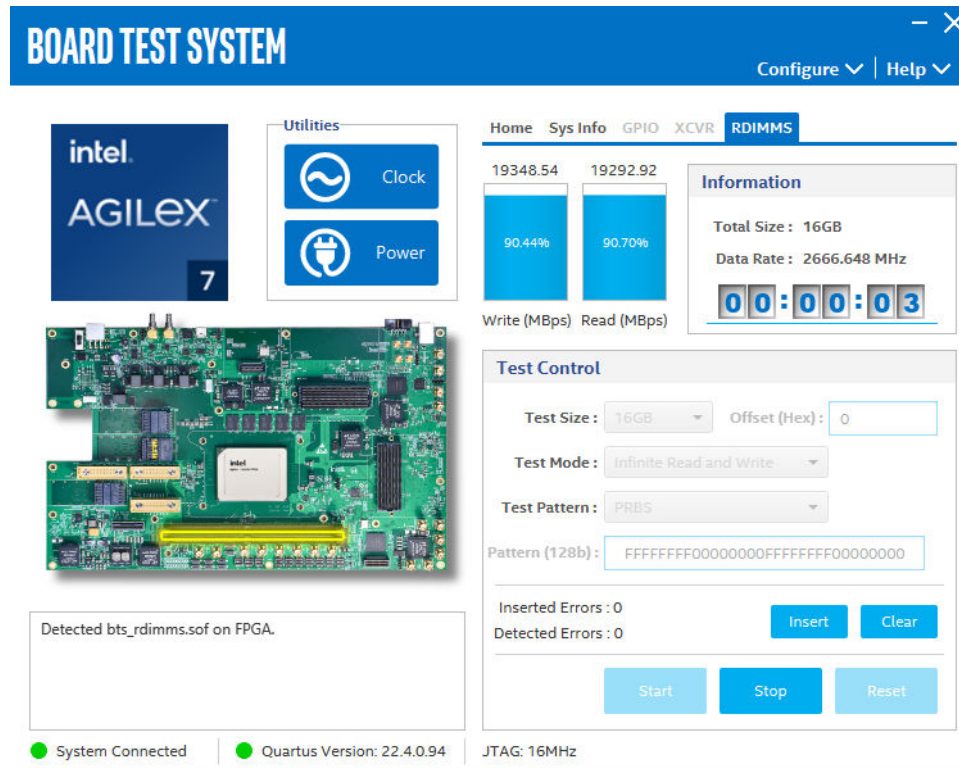
Figure 24. The SDI Tab



#### 4.2.6. The Memory Tab

This tab allows you to read and write DDR4 DIMM-2A (DIMM-I) and DDR4 DIMM-2B (DIMM-II) memory on your board. RDIMMS only tests DIMM-II while RDIMMD tests DIMM-I and DIMM-II. Download the design through the **Configure** menu.

**Figure 25. The RDIMMS Tab**



The following sections describe controls on this tab.

### Start

Initiates DDR4 memory transaction performance analysis.

### Stop

Terminates transaction performance analysis.

### Reset

Resets transaction performance analysis.

### Performance Indicators

These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **Write and Read performance bars:** Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Write (MBps) and Read (MBps):** Show the number of bytes analyzed per second.
- **Data Bus:** 72 bits (8 bits ECC) wide, reference clock is 166.666 MHz, and the frequency is 1333.33 MHz double data rate 2666.66 MT/s.

### Test Control

- **Test Size:** You can choose the size of the memory to test. The available options are 64 KB, 256 KB, 1 MB, 16 MB, 64 MB, 256 MB, 1 GB, 4 GB, 8 GB, and 16GB (default).
- **Offset (Hex):** You can define the memory start address to test.
- **Test Mode:** Infinite Read and Write (default), Single Read and Write.
- **Test Pattern:** PRBS (default), User Defined Constant, Walking '0', Walking '1'.

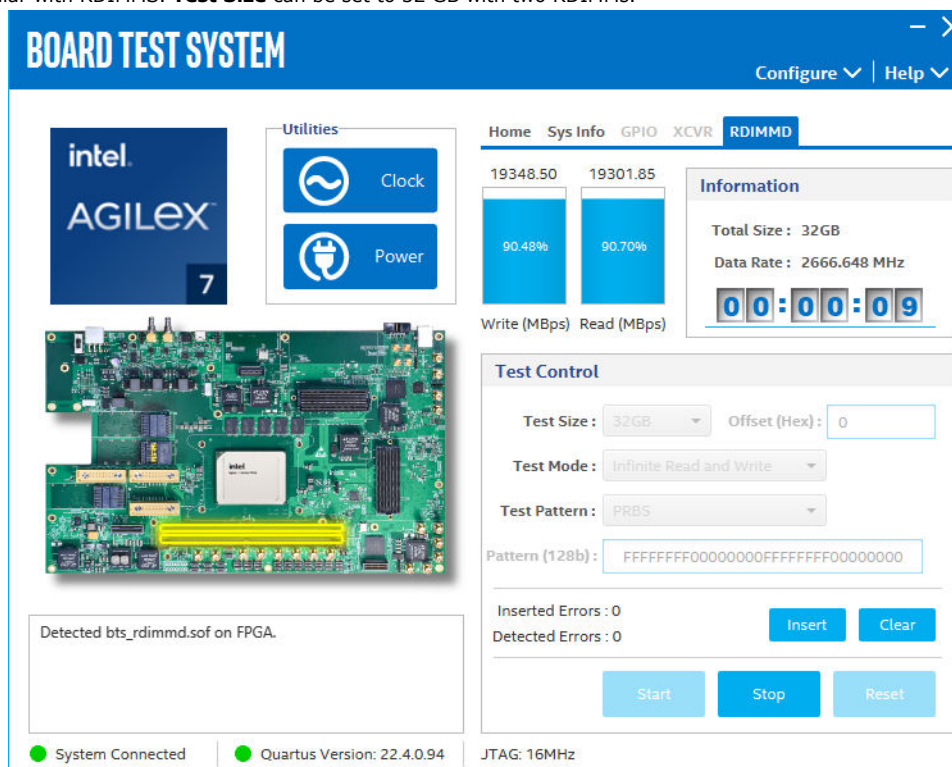
### Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors:** Displays the number of data errors detected in the hardware.
- **Inserted Errors:** Displays the number of errors inserted into the transaction stream.
- **Insert:** Insert a one-word error into the transaction stream each time you click the button. Insert error is only enabled during transaction performance analysis.
- **Clear:** Resets the Detected Errors counter and Inserted Errors counter to zeros.

**Figure 26. The RDIMMD Tab**

Similar with RDIMMS. **Test Size** can be set to 32 GB with two RDIMMs.



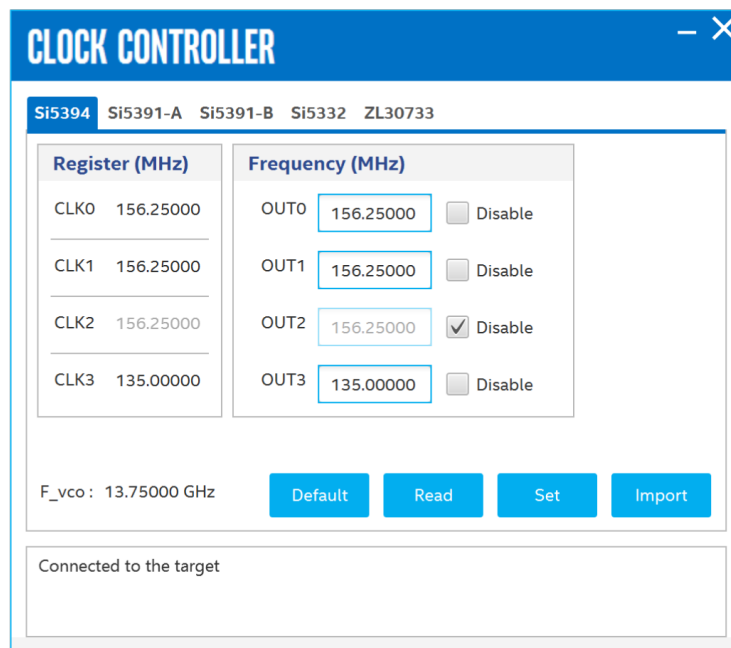
### 4.3. Control On-Board Clock through Clock Controller GUI

The **Clock Controller** communicates with the system MAX 10/Agilex 7 device through a 10-pin JTAG header J11 or USB port J10. The system MAX 10 controls Si5394/Si5391-A/Si5391-B/Si5332, and Agilex 7 device controls ZL30733 through the I<sup>2</sup>C bus.

The instructions to run the **Clock Controller** GUI are stated in the [Running the BTS GUI](#) section. Alternatively, you can start using the Clock Controller feature by selecting the **Clock** icon on the BTS GUI.

**Note:** You cannot run the stand-alone **Clock Controller** GUI application when the BTS or **Power Monitor** GUI is running at the same time. ZL30733 can be controlled only when a design in which the I<sup>2</sup>C interface is instantiated, such as the `bts_config.sof` under the `board_test_system\image\ES` folder has been downloaded to the FPGA.

**Figure 27. Si5394**



The following sections describe the **Clock Controller** GUI buttons.

#### Read

Reads the current frequency setting for the oscillator associated with the active tab.

#### Default

Sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.

## Set

Sets the programmable oscillator frequency for the selected clock to the value in the OUT<sub>x</sub> output controls for Si5394. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Altera recommends resetting the FPGA logic after changing frequencies.

## Import

Si5394 has a two-time rewritable non-volatile memory (NVM). You can generate the register list from the Clockbuilder Pro tool and import it into Si5394 to update the settings of the RAM. Register changes are volatile after power cycling.

**Figure 28. Si5391-A**

Similar control functions with Si5394.

**CLOCK CONTROLLER**

Si5394 **Si5391-A** Si5391-B Si5332 ZL30733

**Frequency (MHz)**

OUT0A	Enable	156.25000	OUT5	Enable	184.32000
OUT0	Enable	156.25000	OUT6	Enable	148.50000
OUT1	Enable	156.25000	OUT7	Enable	368.63000
OUT2	Enable	156.25000	OUT8	Disable	625.00000
OUT3	Enable	125.00000	OUT9	Enable	153.60000
OUT4	Disable	625.00000	OUT9A	Disable	625.00000

F<sub>vco</sub>: 13.75000 GHz    **Default**    **Read**    **Set**    **Import**

Connected to the target

**Figure 29. Si5391-B**

Same with Si5391-A.

CLOCK CONTROLLER

Si5394

Si5391-A

Si5391-B

Si5332

ZL30733

Frequency (MHz)

OUT0A	Disable	156.25000	OUT5	Enable	184.32000
OUT0	Enable	156.25000	OUT6	Enable	148.50000
OUT1	Enable	156.25000	OUT7	Enable	368.63000
OUT2	Enable	156.25000	OUT8	Disable	156.25000
OUT3	Disable	156.25000	OUT9	Enable	153.60000
OUT4	Enable	184.32000	OUT9A	Enable	153.60000

F\_vco : 13.75000 GHz

Default

Read

Set

Import

Connected to the target



**Figure 30. Si5332**

Similar control functions with Si5394. There is no default button for this clock but you can use Import or power cycle the board to get default clock frequencies.

**Figure 31. ZL30733**

Similar control functions with Si5394.

The output frequency of ZL30733 is from 0.5 Hz to 750 MHz. It can generate up to 10 differential outputs with a total of 5 output frequency families.

### Import

ZL30733 has a multiple time writable non-volatile memory (NVM). You can generate the register list with the following format:

- **Register Write Command Link:** X, <register\_address>, <data\_bytes>, <register\_address> and <data\_bytes>, where prefix must be "0x" are in hexadecimal
- **Wait Command Line:** W, <time\_microseconds>

Import it into ZL30733 to update the RAM settings. Register changes are volatile after power cycling. For more details, refer to ZL30733 on the Microchip website.

### Related Information

#### [Skyworks Solution](#)

More information about the ClockBuilder Pro software.

## 4.4. Monitor On-Board Power Regulator through Power Monitor GUI

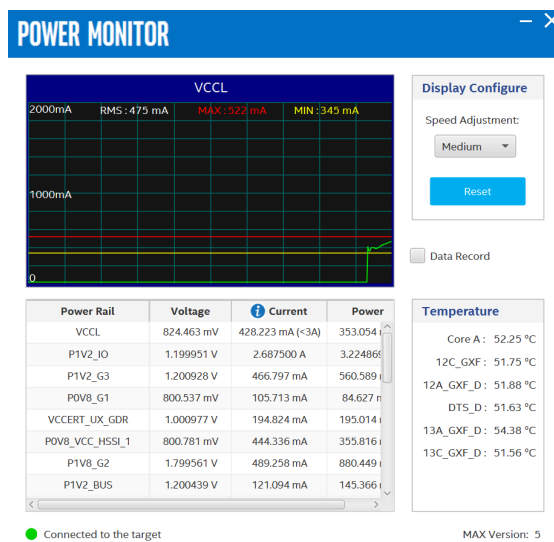
The **Power Monitor** GUI reports most power rails' voltage, current, and power information on the board. It also collects temperature from FPGA die, power modules, and diodes assembled on PCB.

The **Power Monitor** GUI communicates with the system MAX 10 through a 10-pin JTAG header J11 or USB port J10. The system MAX 10 monitors and controls power regulator, temperature/voltage/current sensing chips through a 2-wire I<sup>2</sup>C bus.

The instructions to run the **Power Monitor** GUI are stated in the [Running the BTS GUI](#) section. Alternatively, you can start using the Power Monitor feature by selecting the **Power** icon on the BTS GUI.

**Note:** You cannot run the stand-alone **Power Monitor** GUI when the BTS or the **Clock Controller** GUI is running at the same time.

**Figure 32. Power Monitor GUI**



The following sections describe the details of the **Power Monitor** GUI.

### Display Configure

- **Speed Adjustment:** Adjusts the update rate of the current curve.
- **Reset:** Regenerates the graph.

### Data Record

When the box is checked, the telemetry data of the selected power rail can be recorded. It saves the data into a .csv file in the log directory.

### Temperature

Reads the temperature data from FPGA die internal temperature sense diodes.

## 4.5. BTS Test Areas

BTS checks for hardware fault before you can use the board. If one or more BTS test items fail, it implies either a wrong hardware setting or hardware fault on specific interface.

## 4.6. Identify Test Pass or Fail based on BTS GUI Test Status

### QSFPDD0/QSFPDD1

Plug QSFPDD0/QSFPDD1 loopback module in J27/J48 before you configure QSFPDD NRZ/PAM4 example build through the BTS GUI.

### QSFPDD800

Plug QSFPDD800 loopback module in J22 and use the MXPM cable between MXPM\_FHT connector J2 and J8 before you configure QSFPDD800 PAM4 example build through the BTS GUI.

### FMCA/FMCB

Plug FMCA/FMCB loopback module in J7/J9 before you configure FMCA/FMCB NRZ example build through the BTS GUI.

### MXPM\_FGT

Plug MXPM\_FGT loopback module in J28 before you configure MXPM NRZ/PAM4 example build through the BTS GUI.

### DDR4 DIMM

Plug the DIMM-I/II module, which is shipped alone with this development kit, in J5. The BTS GUI only supports fabric memory interfaces, namely DDR4 DIMM-2A (DIMM-I) and DDR4 DIMM-2B (DIMM-II).

## 5. Development Kit Hardware and Configuration

The Agilex 7 FPGA I-Series Transceiver-SoC Development Kit can support multiple application scenarios and configuration modes. You need to change hardware setting and/or re-program system images for these cases.

**Table 5. Supported Configuration Modes**

S9 [1:4]	MSEL [2:0]	Configuration Mode
ON/OFF/OFF/X	001	AS – Fast mode (Default setting)
ON/ON/OFF/X	011	AS – Normal mode
ON/ON/ON/X	111	JTAG
OFF/ON/ON/X	110	Avalon-ST x8
ON/OFF/ON/X	101	Avalon-ST x16
OFF/OFF/OFF/X	000	Avalon-ST x32

### 5.1. Configure FPGA and Access HPS Debug Access Port by JTAG

1. JTAG access does not rely on switch S9 settings and system image.
2. Plug the USB cable to J10 or Intel FPGA Download Cable to J11.
3. Open the Quartus Prime Programmer, system console to configuration Agilex 7 FPGA SDM, system MAX 10 and FMC JTAG nodes.
4. Open Arm Development Studio 5\* (DS-5\*) Intel SoC FPGA Edition to connect to and communicate with the HPS Debug Access Port (DAP) through the same JTAG interface.

### 5.2. Configure the FPGA Device Using the AS Mode (Default Mode)

1. Default S9 setting and system MAX 10 image support the active serial (AS) configuration mode.
2. Plug pre-programmed SDM QSPI flash daughter into J3.
3. Power on and observe FPGA user LED behavior.

### 5.3. Configure the FPGA Device Using the Avalon-ST Mode

© Altera Corporation. Altera, the Altera logo, the 'a' logo, and other Altera marks are trademarks of Altera Corporation. Altera and Intel warrant performance of its FPGA and semiconductor products to current specifications in accordance with Altera's or Intel's standard warranty as applicable, but reserves the right to make changes to any products and services at any time without notice. Altera and Intel assume no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera or Intel. Altera and Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

\*Other names and brands may be claimed as the property of others.

1. Set S9 to Avalon-ST x32 mode first.
2. Default system MAX 10 image support the Avalon-ST x32 mode only. You should build a corresponding .POF image if you select Avalon-ST x8 or Avalon-ST x16 configuration mode.
3. Power on the board, use push button S16 to choose page, and S17 to configure the FPGA.
4. Default page depends on the setting of S10.1.

**Table 6. Avalon-ST x32 LED Behavior**

LED	Page0	Page1	Page2	Page3
LED_D9	ON	OFF	OFF	OFF
LED_D11	OFF	ON	OFF	ON
LED_D13	OFF	OFF	ON	ON
USER_LED0_D1	Blinking	Blinking	Blinking	Blinking
USER_LED1_D3	ON	ON	ON	ON
USER_LED2_D5	Blinking reversed	Blinking	Blinking	Blinking
USER_LED3_D7	ON	ON	ON	ON
USER_LED4_D2	ON	ON	Blinking reversed	Blinking
USER_LED5_D4	ON	Blinking reversed	Blinking	Blinking
USER_LED6_D6	ON	ON	ON	Blinking reversed
USER_LED7_D8	ON	ON	ON	ON

## 5.4. Daughter Cards

The Agilex 7 FPGA I-Series Transceiver-SoC Development Kit supports HPS OOB daughter card. You can demonstrate HPS functions through these daughter cards and cables.

### 5.4.1. HPS Out of Box Experience (OOBE) Daughter Card

1. Plug HPS OOB daughter card in J4.
2. To test HPS Ethernet capability, connect OOB's RJ45 port J3 to internet.
3. To test HPS USB 2.0 capability, connect OOB's J4 port to USB cable.
4. To debug HPS from UART terminal applications, use USB cable to connect to OOB's J7.
5. OOB's MicroSD card is pre-programmed with GSRD and OS.
6. General I/O access is provided by push buttons and LED indicators.

## 6. Custom Projects for the Development Kit

### 6.1. Add SmartVID Settings in the Quartus Prime QSF File

Agilex 7 silicon assembled on this development kit enables SmartVID feature by default. In order to avoid a Quartus Prime from generating an error due to incomplete SmartVID settings, you must put constraints outlined below into Quartus Prime project QSF file. These constraints are designed for Intel Enpirion® ED8401 core circuit.

#### DK-SI-AGI027FA and DK-SI-AGI027FC (Not Intel Enpirion)

Open your Quartus Prime project QSF file, copy and paste the following constraint scripts into the file. Ensure there are no other similar settings with different values.

```
set_global_assignment -name USE_PWRMGT_SCL SDM_IO0
set_global_assignment -name USE_PWRMGT_SDA SDM_IO12
set_global_assignment -name USE_CONF_DONE SDM_IO16
set_global_assignment -name VID_OPERATION_MODE "PMBUS MASTER"
set_global_assignment -name PWRMGT_BUS_SPEED_MODE "100 KHZ"
set_global_assignment -name PWRMGT_SLAVE_DEVICE_TYPE LTC3888
set_global_assignment -name NUMBER_OF_SLAVE_DEVICE 1
set_global_assignment -name PWRMGT_SLAVE_DEVICE0_ADDRESS 62
set_global_assignment -name PWRMGT_VOLTAGE_OUTPUT_FORMAT "LINEAR FORMAT"
set_global_assignment -name PWRMGT_LINEAR_FORMAT_N "-12"
set_global_assignment -name PWRMGT_TRANSLATED_VOLTAGE_VALUE_UNIT VOLTS
```

#### DK-SI-AGI027FB and DK-SI-AGI027FES (Intel Enpirion)

Open your Quartus Prime project QSF file, copy and paste the following constraint scripts into the file. Ensure there are no other similar settings with different values.

```
set_global_assignment -name USE_PWRMGT_SCL SDM_IO0
set_global_assignment -name USE_PWRMGT_SDA SDM_IO12
set_global_assignment -name USE_CONF_DONE SDM_IO16
set_global_assignment -name VID_OPERATION_MODE "PMBUS MASTER"
set_global_assignment -name PWRMGT_BUS_SPEED_MODE "100 KHZ"
set_global_assignment -name PWRMGT_SLAVE_DEVICE_TYPE ED8401
set_global_assignment -name NUMBER_OF_SLAVE_DEVICE 1
set_global_assignment -name PWRMGT_SLAVE_DEVICE0_ADDRESS 62
set_global_assignment -name PWRMGT_VOLTAGE_OUTPUT_FORMAT "LINEAR FORMAT"
set_global_assignment -name PWRMGT_LINEAR_FORMAT_N "-13"
set_global_assignment -name PWRMGT_TRANSLATED_VOLTAGE_VALUE_UNIT VOLTS
```

### 6.2. Golden Top

You can use the Golden Top project as the starting point for your designs. It comes loaded with constraints, pin locations, defined I/O standard, direction, and general termination. The DDR4 pin termination settings are not included. Refer DDR4 example designs for details.

## 7. Document Revision History for the Agilex 7 FPGA I-Series Transceiver-SoC Development Kit User Guide

Document Version	Changes
2025.02.28	<ul style="list-style-type: none"> <li>Updated the Overview chapter: <ul style="list-style-type: none"> <li>Updated the following topics: <ul style="list-style-type: none"> <li>Recommended Operating Conditions</li> </ul> </li> </ul> </li> <li>Updated the Getting Started chapter: <ul style="list-style-type: none"> <li>Added new topics: <ul style="list-style-type: none"> <li>Before You Begin</li> <li>Handling the Board</li> <li>Installing the Quartus Prime Pro Edition Software</li> <li>Installing the Intel SoC EDS</li> <li>Installing the Development Kit</li> <li>Installing the Intel FPGA Download Cable Driver</li> </ul> </li> <li>Updated and retitled topic <i>Quartus Prime Software and Driver Installation</i> to <i>Software and Driver Installation</i>.</li> <li>Removed the <i>Design Examples</i> topic.</li> </ul> </li> <li>Updated and retitled chapter <i>Power Up the Development Kit</i> to <i>Development Kit Setup</i>: <ul style="list-style-type: none"> <li>Retitled topic <i>Power Up</i> to <i>Powering Up the Development Kit</i>.</li> <li>Retitled topic <i>Restore Board System MAX 10 with Default Factory Image</i> to <i>Restoring Board System MAX 10 with Default Factory Image</i>.</li> </ul> </li> <li>Updated the Board Test System chapter: <ul style="list-style-type: none"> <li>Retitled topic <i>Download OpenJDK</i> to <i>Downloading OpenJDK</i>.</li> <li>Retitled topic <i>Download OpenJFX</i> to <i>Downloading OpenJFX</i>.</li> <li>Retitled topic <i>Download OpenJDK and OpenJFX</i> to <i>Downloading OpenJDK and OpenJFX</i>.</li> <li>Retitled topic <i>Install Quartus Prime Software</i> to <i>Setting Up the Quartus Prime Software for BTS Operation</i>.</li> <li>Retitled topic <i>Run BTS GUI</i> to <i>Running the BTS GUI</i>.</li> <li>Updated the <i>Control On-Board Clock through Clock Controller GUI</i> topic.</li> </ul> </li> <li>Added new appendix chapter—<i>Developer Resources</i>.</li> <li>Restructured the document to improve clarity and for ease of reference.</li> <li>Updated the document for the latest branding standards.</li> </ul>
2024.05.31	<ul style="list-style-type: none"> <li>Updated the description of Development Kit Version in Table: <i>Ordering Information</i>.</li> </ul>
2023.04.10	<ul style="list-style-type: none"> <li>Updated Ordering Information in Overview section.</li> <li>Added Figure: <i>Agilex 7 FPGA I-Series Transceiver-SoC Development Kit Board Image - DK-SI-AGI027FB and DK-SI-AGI027FES (Intel Enpirion)</i> and Figure: <i>Agilex 7 FPGA I-Series Transceiver-SoC Development Kit Board Image - DK-SI-AGI027FA and DK-SI-AGI027FC (Not Intel Enpirion)</i> in Overview section.</li> <li>Updated list in <i>Box Contents</i> section.</li> <li>Updated the FPGA maximum power supported by active heatsink/fan in <i>Recommended Operating Conditions</i>.</li> <li>Updated <i>Restore Board QSPI Flash with the Default Factory Image</i> section.</li> <li>Added <i>Control On-board Clock through Clock Controller GUI</i> section.</li> <li>Added <i>Control On-board Power Regulator through Power Monitor GUI</i> section.</li> <li>Added Post-tap 2 setting in <i>The QSPFDD800 PAM4 Tab</i> section.</li> </ul>

continued...

© Altera Corporation. Altera, the Altera logo, the 'a' logo, and other Altera marks are trademarks of Altera Corporation. Altera and Intel warrant performance of its FPGA and semiconductor products to current specifications in accordance with Altera's or Intel's standard warranty as applicable, but reserves the right to make changes to any products and services at any time without notice. Altera and Intel assume no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera or Intel. Altera and Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

\*Other names and brands may be claimed as the property of others.

ISO  
9001:2015  
Registered



Document Version	Changes
	<ul style="list-style-type: none"> <li>Added <i>The SDI Tab</i> section.</li> <li>Added description for Reset button in <i>The Memory Tab</i> section.</li> <li>Updated description for <i>Custom Projects for the Development Kit</i>.</li> <li>Updated Figure: <i>BTS GUI</i>.</li> <li>Updated Figure: <i>The Sys Info Tab</i>.</li> <li>Updated Figure: <i>The Configure Menu</i>.</li> <li>Updated Figure: <i>The Sys Info Tab</i>.</li> <li>Updated Figure: <i>The GPIO Tab</i>.</li> <li>Updated Figure: <i>The QSPDD NRZ Tab</i>.</li> <li>Updated Figure: <i>QSPDD NRZ – PLL and Pattern Status</i>.</li> <li>Updated Figure: <i>QSPDD NRZ - PMA Setting</i>.</li> <li>Updated Figure: <i>QSPDD NRZ - Data Rate</i>.</li> <li>Updated Figure: <i>The QSPDD PAM4 Tab</i>.</li> <li>Updated Figure: <i>The FMCA NRZ Tab</i>.</li> <li>Updated Figure: <i>The FMCB NRZ Tab</i>.</li> <li>Updated Figure: <i>The QSPDD800 PAM4 Tab</i>.</li> <li>Updated Figure: <i>The MXPM NRZ Tab</i>.</li> <li>Updated Figure: <i>The MXPM PAM4 Tab</i>.</li> <li>Updated Figure: <i>The RDIMMS Tab</i>.</li> <li>Updated Figure: <i>The RDIMMD Tab</i>.</li> <li>Updated Figure: <i>ZL30733</i>.</li> <li>Updated Figure: <i>Power Monitor GUI</i>.</li> <li>Added constraint scripts for DK-SI-AGI027FA and DK-SI-AGI027FC, DK-SI-AGI027FB and DK-SI-AGI027FES in <i>Add SmartVID Settings in the Intel Quartus Prime QSF File</i> section.</li> <li>Added Figure: <i>Power Tree (Not Intel Enpirion) DK-SI-AGI027FA and DK-SI-AGI027FC</i>.</li> <li>Added Figure: <i>I<sup>2</sup>C Serial Bus (Not Intel Enpirion) DK-SI-AGI027FA and DK-SI-AGI027FC</i>.</li> <li>Updated product family name to "Intel Agilex® 7".</li> </ul>
2023.03.02	Updated the MXMP breakout cable and MCIO cable part number details in Table: <i>Connectors and Cables</i> .
2022.09.30	<ul style="list-style-type: none"> <li>Added UKCA in the <i>Safety and Regulatory Information and Compliance Information</i> sections.</li> <li>Added the <i>Lithium Ion Battery Warnings</i> section.</li> <li>Updated Table: <i>Ordering Information</i>.</li> <li>Updated the <i>Perform Board Restore</i> section.</li> <li>Updated step 3 in the <i>Restore Board QSPI Flash with Default Factory Image</i> section.</li> <li>Updated the <i>Control On-Board Clock through Clock Controller GUI</i> section.</li> <li>Updated step 1 and step 3 in the <i>Configure FPGA and Access HPS Debug Access Port by JTAG</i> section.</li> <li>Updated the <i>System Management</i> section.</li> <li>Updated the <i>Power Cord Requirements</i> section.</li> <li>Updated the <i>Safety Cautions</i> section.</li> </ul>
2022.04.07	Initial release.

## A. Development Kit Components

### A.1. System Management

Two MAX 10 FPGAs (10M16SCU324C8G) are used for system management. The system MAX 10 acts as a system controller. It handles the FPGA Avalon-ST configuration, I<sup>2</sup>C bus access, fan speed control, and system reset functions. The UB2/PWR MAX 10 acts as the Power Manager and on-board JTAG controller. Refer to the following description for each function:

- **Power management:** Control systems and FPGA power-up and optional power-down sequence (PDS), supervise power regulators/switches status and manage power faults, supervise temperature analog-to-digital converter (ADC) interrupt signals and manage temperature faults.
- **JTAG controller:** Manage the JTAG chain topology, JTAG master source and JTAG slaves using S19/S20.

**Table 7. JTAG Master Sources**

Schematic Signal Name	Description
EXT_JTAG_TCK/TDO/TMS/TDI	JTAG header J11 for Intel FPGA Download Cable
FX2_Dp/n	Input port J10 for on-board Intel download circuit
HPS_GPIO[32:35]	Mictor 38-pin header on the OOB daughter card

Agilex 7 HPS JTAG can be accessed from either SDM dedicated JTAG pins or HPS dedicated I/Os. When it is accessed from SDM JTAG pins (FPGA\_JTAG\_TCK/TDO/TMS/TDI), SDM is chained with HPS inside FPGA. When it is accessed from HPS dedicated I/Os (HPS\_GPIO[32:35]), HPS is chained externally by PCB traces.

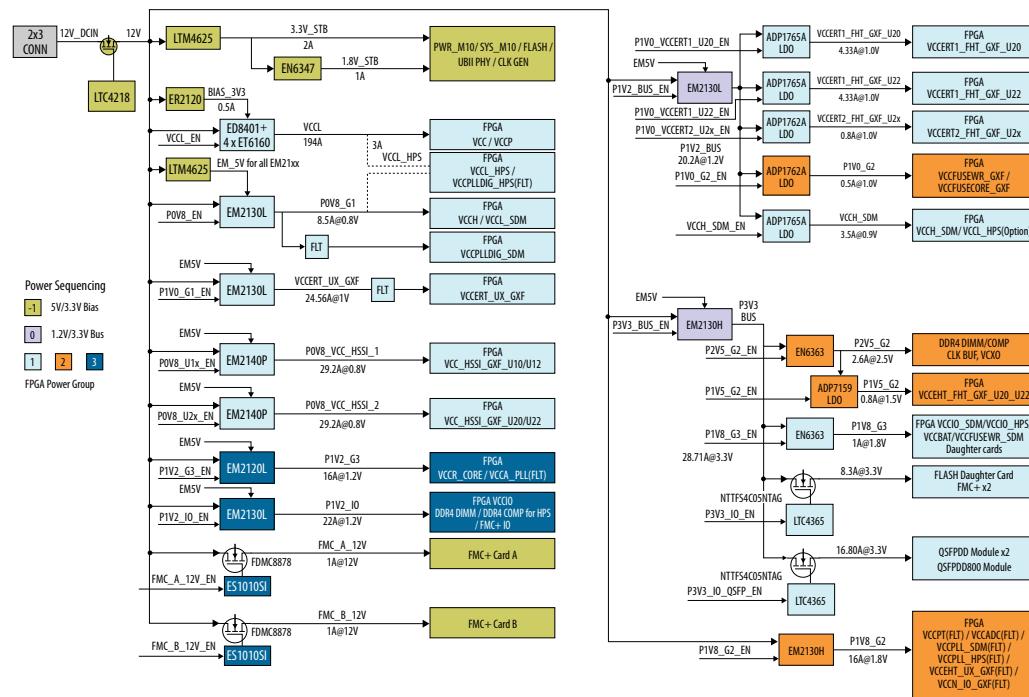
**Table 8. JTAG Chain Topology Settings**

Mode	S20 [4:2]	S19 [4] [3] [2] [1] ON: Bypass from chain OFF: Enable in chain	Function
000	ON/ON/ON (Default)	S19.1 (SDM+HPS) S19.2 (System MAX 10) S19.3 (FMC_B) S19.4 (FMC_A)	Mode 1: On-board Intel download circuit act as the only JTAG Master. Chained HPS with SDM nodes <b>internally</b> .
continued...			

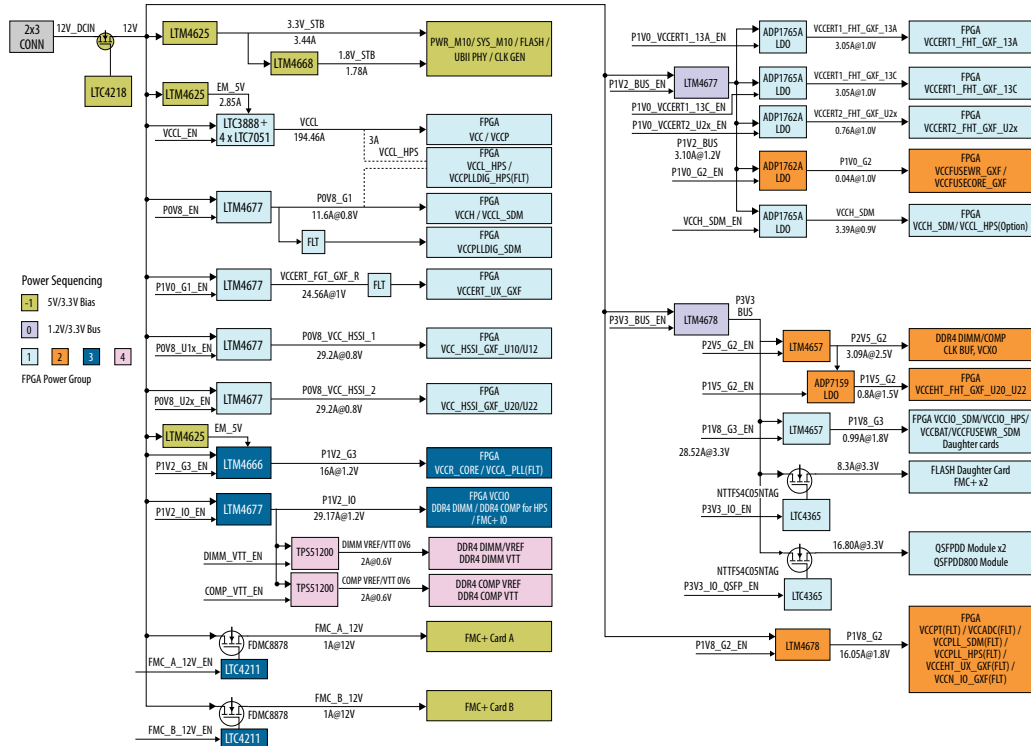
Mode	S20 [4:2]	S19 [4] [3] [2] [1] ON: Bypass from chain OFF: Enable in chain	Function
			Mode 3: External Intel FPGA Download Cable act as the only JTAG Master. Chained HPS with SDM nodes <b>internally</b> .
001	ON/ON/OFF	SDM is always enabled in the JTAG chain. S19.1 (HPS) S19.2 (System MAX 10) S19.3 (FMC_B) S19.4 (FMC_A)	Mode 2: On-board Intel download circuit act as the only JTAG Master. Chained HPS with SDM nodes <b>externally</b> . Mode 4: External Intel FPGA Download Cable act as the only JTAG Master. Chained HPS with SDM node <b>externally</b> .
100	OFF/ON/ON	S19.1 (SDM) S19.2 (System MAX 10) S19.3 (FMC_B) S19.4 (FMC_A)	Mode 7: Both on-board Intel download circuit and OOBEE act as JTAG Masters. Separated HPS and SDM JTAG <b>chains, OOBEE only drive HPS</b> . Mode 8: Both external Intel FPGA Download Cable and OOBEE JTAG act as JTAG Masters. Separated HPS and SDM JTAG <b>chains, OOBEE only drive HPS</b> .
Others	N/A	N/A	Reserved

## A.2. Power

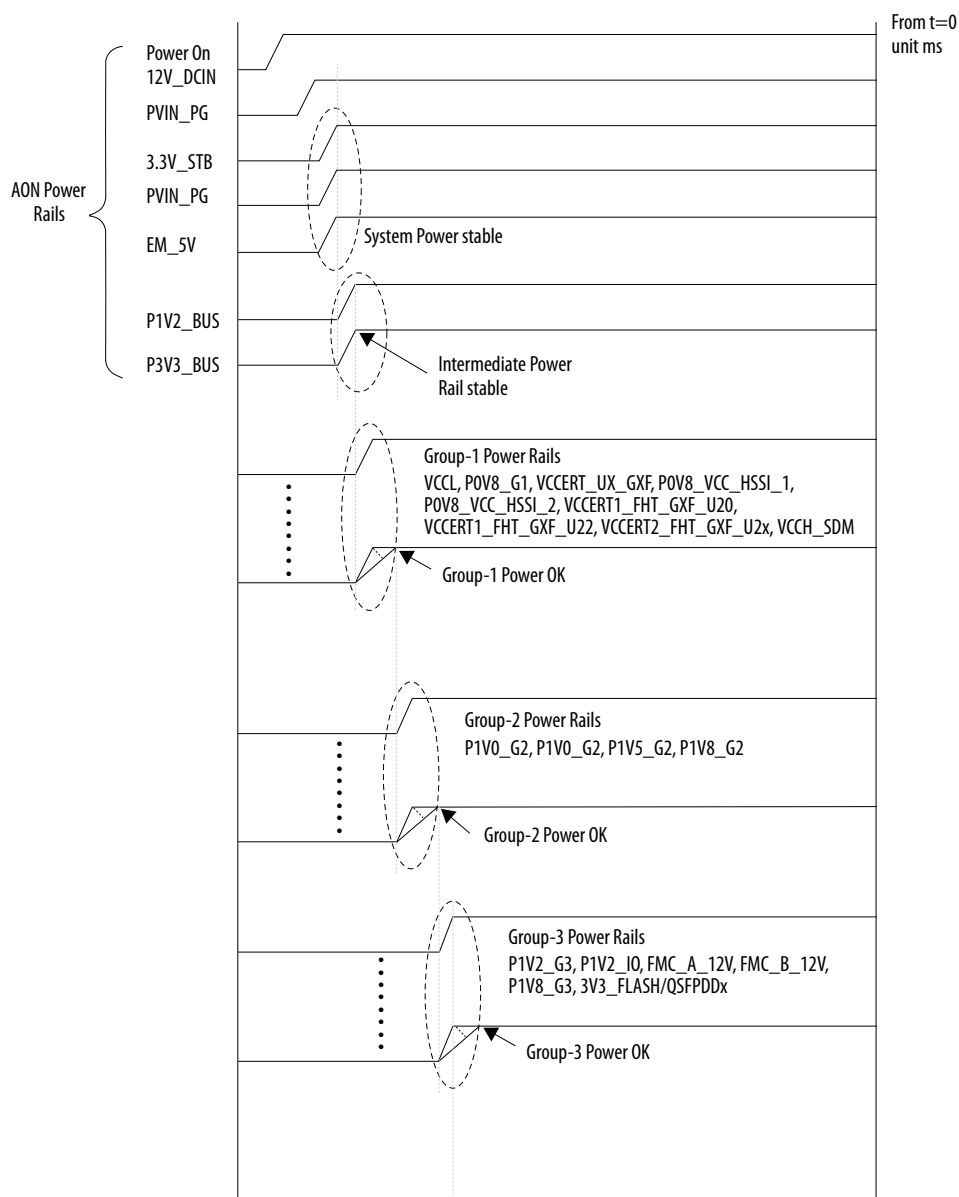
**Figure 33. Power Tree (Intel Enpirion) DK-SI-AGI027FB and DK-SI-AGI027FES**



**Figure 34. Power Tree (Not Intel Enpirion) DK-SI-AGI027FA and DK-SI-AGI027FC**



**Figure 35. Power Sequence**



Onboard hot-plug circuit shuts down all power rails when the total power is over 360 W (30 A).

UB2/PWR MAX 10 shuts down significant power rails when one or more good power indicators is low due to a power fault.

UB2/PWR MAX 10 also shuts down significant power rails when temperature cross the acceptable range.

## A.3. Clocks

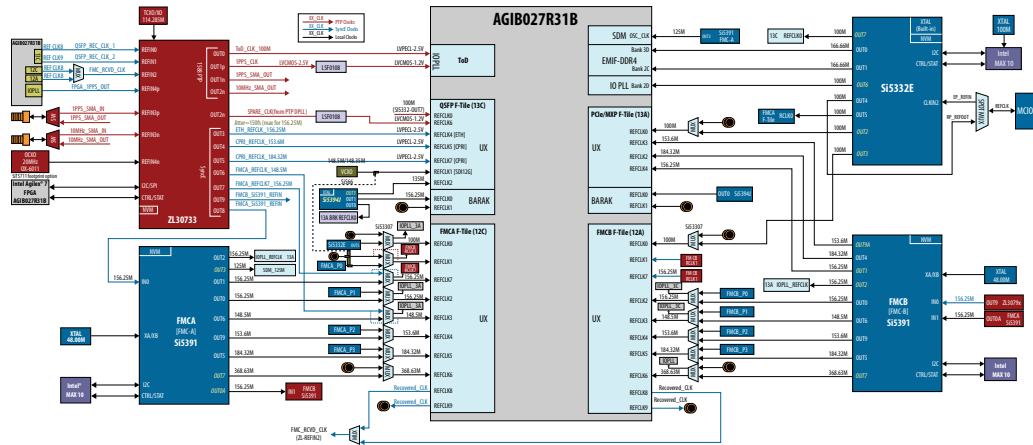
**Table 9. Default Clock Frequency**

Schematic Signal Name	Default Frequency
DDR4_HPS_REFCLKp/n	166.6M
DDR4_DIMM_2_REFCLKp/n	166.6M
Si5332_OUT2_P/N	100M
Si5332_OUT3_P/N	100M
PCIE_100M_REF_RP_AP/N	100M
Si5332_OUT5_P/N	100M
CLK_GPIO_P_4/N_4	100M
Si5332_OUT7_P/N	100M
Si5391_A_OUT_P0A/N0A	156.25M
Si5391_A_OUT_P0/N0	156.25M
Si5391_A_OUT_P1/N1	156.25M
Si5391_A_OUT_P5/N5	184.32M
Si5391_A_OUT_P6/N6	148.5M
Si5391_A_OUT_P7/N7	368.63M
Si5391_A_OUT_P9/N9	153.6M
Si5391_B_OUT_P0/N0	156.25M
CLK_13A_FGT_REFCLK4_P/N	156.25M
CLK_13A_FGT_REFCLK2_P/N	184.32M
Si5391_B_OUT_P5/N	184.32M
Si5391_B_OUT_P6/N6	148.5M
Si5391_B_OUT_P7/N7	368.63M
Si5391_B_OUT_P9/N9	153.6M
CLK_13A_FGT_REFCLK3_P/N	153.6M
CLK_FHT_13A_P_0/N_0	156.25M
CLK_FHT_13C_P_0/N_0	156.25M
CLK_FGT_13C_REFCLK_2P/N	135M
CLK_A_12C_FGT_P_0/N_0	100M
CLK_3A_GPIO_P_0/N_0	100M
CLK_A_12C_FGT_P_3/N_3	148.5M
CLK_3A_GPIO_P_2/N_2	148.5M
CLK_A_12C_FGT_P_2/N_2	156.25M
CLK_3A_GPIO_P_1/N_1	156.25M
<i>continued...</i>	



Schematic Signal Name	Default Frequency
CLK_A_12C_FGT_P_4/N_4	156.25M
CLK_A_12C_FGT_P_6/N_6	368.63M
CLK_A_12C_FGT_P_5/N_5	184.32M
CLK_B_12A_FGT_P_0/N_0	100M
CLK_13A_FGT_REFCLK0_P/N	100M
CLK_B_12A_FGT_P_2/N_2	156.25M
CLK_3C_GPIO_P_1/N_1	156.25M
CLK_B_12A_FGT_P_3/N_3	148.5M
CLK_3C_GPIO_P_0/N_0	148.5M
CLK_B_12A_FGT_P_4	156.25M
CLK_B_12A_FGT_P_5	184.32M
CLK_B_12A_FGT_P_6	368.63M
ToD_CLK_100M_P/N	100M
ETH_REFCLK_156.25M_P/N	156.25M
CPRI_REFCLK_153.6M_P/N	153.6M
CPRI_REFCLK_184.32M_P/N	184.32M
FMCA_REFCLK_148.5M_P/N	148.5M
FMCA_REFCLK_156.25M_P/N	156.25M
Si5391_A_156.25M_REFIN_P/N	156.25M
Si5391_B_156.25M_REFIN_P/N	156.25M
CLK_3C_GPIO_P_1/N_1	156.25M
CLK_B_12A_FGT_P_3/N_3	148.5M
CLK_3C_GPIO_P_0/N_0	148.5M
1PPS_FPGA_CLK	1PPS
1PPS_SMA_OUT	1PPS
10MHz_SMA_OUT	10M
ZL_SPARE_CLK_100M	100M

**Figure 36. Clock Tree**



## A.4. General Input/Output

**Table 10. MAX 10 and FPGA**

Schematic Signal Name	Description
F_GPIO0	The value of filtered user_pb[0]
F_GPIO1	The value of filtered user_pb[1]
F_GPIO2	MCIO_PERST in RP mode
F_GPIO3	FMC_A_PERST in RP mode
F_GPIO4	FMC_B_PERST in RP mode
F_GPIO5	Status of SYS_SW3 from MAX 10
F_GPIO6	Reserved
F_GPIO7	Reserved
F_GPIO8	Reserved
F_GPIO9	Reserved
F_GPIO10	Reserved
F_GPIO11	Reserved
F_GPIO12	Reserved

**Table 11. System MAX 10**

Schematic Signal Name	Description
SYS_LED0/D9	PGM_LED0 for Avalon-ST configuration
SYS_LED1/D11	PGM_LED1 for Avalon-ST configuration
SYS_LED2/D13	PGM_LED2 for Avalon-ST configuration
SYS_LED3/D15	MAX_ERROR for Avalon-ST configuration
SYS_LED4/D10	MAX_LOAD for Avalon-ST configuration
<i>continued...</i>	

Schematic Signal Name	Description
SYS_LED5/D12	MAX_CONF_DONE for Avalon-ST configuration
SYS_LED6/D14	Reserved
SYS_LED7/D16	Reserved
SYS_PB0/S11	MAX_RESETh
SYS_PB1/S12	FPGA_RESETh
SYS_PB2/S13	HPS_COLD_RESETh
SYS_PB3/S14	Power recycle
SYS_PB4/S16	PGM_SEL for Avalon-ST configuration
SYS_PB5/S17	PGM_CFG for Avalon-ST configuration
clk_i2c_en0	Before power ok: 0 After power ok: S_control_gui[2], =1 by default
clk_i2c_en1	Stuck at GND
VCCL_I2C_EN	Before power ok: 0 After power ok: S_control_gui[1], =1 by default
dimm_io_en	Before power ok: 0 After power ok: 1
zl_i2c_en	Before power ok: 0 After power ok: S_control_gui[3], =0 by default
si5394_rstn	When input globe resetn active: 0 When input globe resetn release: S_control_gui[13], =1 by default
si5394_oe_n	Before power ok: 1 After power ok: S_control_gui[14], =0 by default
si5391_rstn	When input globe resetn active: 0 When input globe resetn release: S_control_gui[9], =1 by default
si5394_lo1	Store in status_gui bit3
si5394_int_n	Store in status_gui bit2
si5391_oen	Before power ok: 1 After power ok: S_control_gui[10], =0 by default
si5391_b_rstn	When input globe resetn active: 0 When input globe resetn release: S_control_gui[11], =1 by default
si5391_b_oen	Before power ok: 1 After power ok: S_control_gui[12], =0 by default
usb2_resetn	Before power ok: 0 After power ok: S_control_gui[15], =1 by default
usb_mux_reset	Before power ok: 1 After power ok: S_control_gui[16], =0 by default
mux_sel0	system_info_slv_data_write_0[0]=1 : controlled by system_info_slv_data_write_1[0]
continued...	

Schematic Signal Name	Description
	system_info_slv_data_write_0[0]=0 : controlled by MUX_DIP_SW10
mux_sel1	system_info_slv_data_write_0[1]=1 : controlled by system_info_slv_data_write_1[1] system_info_slv_data_write_0[1]=0 : controlled by SYS_SW1
mux_sel2	system_info_slv_data_write_0[2]=1 : controlled by system_info_slv_data_write_1[2] system_info_slv_data_write_0[2]=0 : controlled by MUX_DIP_SW0
mux_sel3	system_info_slv_data_write_0[3]=1 : controlled by system_info_slv_data_write_1[3] system_info_slv_data_write_0[3]=0 : controlled by MUX_DIP_SW1
mux_sel4	system_info_slv_data_write_0[4]=1 : controlled by system_info_slv_data_write_1[4] system_info_slv_data_write_0[4]=0 : controlled by MUX_DIP_SW2
mux_sel5	system_info_slv_data_write_0[5]=1 : controlled by system_info_slv_data_write_1[5] system_info_slv_data_write_0[5]=0 : controlled by MUX_DIP_SW3
mux_sel6	system_info_slv_data_write_0[6]=1 : controlled by system_info_slv_data_write_1[6] system_info_slv_data_write_0[6]=0 : controlled by MUX_DIP_SW9
mux_sel7	system_info_slv_data_write_0[7]=1 : controlled by system_info_slv_data_write_1[7] system_info_slv_data_write_0[7]=0 : controlled by SYS_SW2
mux_sel8	system_info_slv_data_write_0[8]=1 : controlled by system_info_slv_data_write_1[8] system_info_slv_data_write_0[8]=0 : controlled by MUX_DIP_SW11
mux_sel9	system_info_slv_data_write_0[9]=1 : controlled by system_info_slv_data_write_1[9] system_info_slv_data_write_0[9]=0 : controlled by SYS_SW3
mux_sel10	system_info_slv_data_write_0[10]=1 : controlled by system_info_slv_data_write_1[10] system_info_slv_data_write_0[10]=0 : controlled by MUX_DIP_SW4
mux_sel11	system_info_slv_data_write_0[11]=1 : controlled by system_info_slv_data_write_1[11] system_info_slv_data_write_0[11]=0 : controlled by MUX_DIP_SW5
mux_sel12	system_info_slv_data_write_0[12]=1 : controlled by system_info_slv_data_write_1[12]
<b>continued...</b>	

Schematic Signal Name	Description
	system_info_slv_data_write_0[12]=0 : controlled by MUX_DIP_SW6
mux_sel13	system_info_slv_data_write_0[13]=1 : controlled by system_info_slv_data_write_1[13] system_info_slv_data_write_0[13]=0 : controlled by MUX_DIP_SW8
mux_sel14	system_info_slv_data_write_0[14]=1 : controlled by system_info_slv_data_write_1[14] system_info_slv_data_write_0[14]=0 : controlled by MUX_DIP_SW7
mux_sel_z1	system_info_slv_data_write_0[15]=1 : controlled by system_info_slv_data_write_1[15] system_info_slv_data_write_0[15]=0 : controlled by SYS_SW4
mcio_clk_enn	Before power ok: 1 After power ok: S_control_gui[7], =0 by default
mcio_clk_sel_epn	system_info_slv_data_write_0[16]=1 : controlled by S_control_gui[8], =0 by default system_info_slv_data_write_0[16]=0 : <ul style="list-style-type: none"> <li>=0 when AGIB027R31B is Endpoint</li> <li>=1 when AGIB027R31B is Root port</li> </ul>
si5332_1_in[1:0]	S_control_gui[5:4], =00 by default
si5332_1_in[2]	1'bZ
PTP_CLK_RST_n	Before power ok: 0 After power ok: S_control_gui[6], =1 by default
PTP_CLK_LOL	Store in status_gui bit1
gpio0_ac0_z1_intn	Store in status_gui bit0

**Table 12. UB2/PWR MAX 10**

Schematic Signal Name	Description
FPGA_POK_LED	FPGA Power Good
SYS_PWR_RSV0	Reserved GPIO between the system MAX 10 and the power MAX 10. Used as I <sup>2</sup> C clock.
SYS_PWR_RSV1	Reserved GPIO between the system MAX 10 and the power MAX 10. Used as I <sup>2</sup> C data.
SYS_PWR_RSV2	Reserved GPIO between the system MAX 10 and the power MAX 10. It is the status of SYS_PB3.
SYS_PWR_RSV3	Reserved GPIO between the system MAX 10 and the power MAX 10.

## A.5. Memory Interfaces

### FPGA Dedicated External Memory Interface (2DPC DDR4)

Agilex 7 FPGA I-Series Transceiver-SoC Development Kit supports 32 GB 2DPC DDR4 with ECC support (x72). Mechanically, the development kit provides 2 dual-in memory module slots for the same. This development kit also supports 16 GB 1DPC DDR4 with ECC support (x72). Mechanically, install one RDIMM module on J5.

### FPGA and HPS Shared External Memory Interface (DDR4)

DDR4 component interface is a 72 bit, single rank configuration based on x16 component. It runs at 2666 Mbps. MT40A1G16RC-062E:B from Micron is soldered down on the development kit. Both Agilex 7 FPGA fabric and HPS can access this external memory interface. However, they cannot be accessed at the same time.

## A.6. Communication Interfaces

### MCIO Port

The MCIO slot is a PCIe 4.0 x4 port which fans out from Agilex 7 FPGA I-Series F-Tile. This port is designed to meet the standard MCIO pinout. The system MAX 10 acts as the board management controller (BMC) of the development kit. It manages power-up reset for both PCIe root port and PCIe endpoint. PCIE\_PERSTn\_A signal can act as output and input respectively.

**Table 13. MCIO Port**

Schematic Signal Name	Description
PCIE_PERSTn_A	PCIe endpoint/root port reset
PCIE_ALERTn_A	PCIe Alert
PCIE_100M_REF_AP/AN	PCIe reference clock
PCIE_SCL_A/SDA_A	PCIe I <sup>2</sup> C bus
PCIE_TX_P/N[0:3]	Transceiver TX
PCIE_RX_P/N[0:3]	Transceiver RX

### MCIO x4 Connector

The recommended MCIO cable to use with MCIO connector (Uxx) is NOT included as part of the development kit and must be acquired directly from third party supplier (Amphenol p/n = HMC74-0631).

### QSFPDD

Agilex 7 FPGA I-Series Transceiver-SoC Development Kit supports 2x QSFPDD ports. QSFPDD port fans out from Agilex 7 FPGA I-Series F-Tile (FGT). All 8 channels per QSFPDD can run up to 32G NRZ and 58G PAM4.

**Table 14. QSFPDD Connector 0 (13C/J27)**

Schematic Signal Name	Description
QSFPDD0_3V3_MODPRS_L	Module present
QSFPDD0_3V3_RESET_L	Module reset
QSFPDD0_3V3_MODSEL_L	Mode select
QSFPDD0_3V3_LPMODE	Initial mode
QSFPDD0_3V3_INT_L	Interrupt
I2C_QSFPDD0_3V3_SCL	I <sup>2</sup> C clock
I2C_QSFPDD0_3V3_SDA	I <sup>2</sup> C data
QSFPDD0_TX_P/N[0:7]	Transceiver TX
QSFPDD0_RX_P/N[0:7]	Transceiver RX

**Table 15. QSFPDD Connector 1 (13A/J48)**

Schematic Signal Name	Description
QSFPDD1_3V3_MODPRS_L	Module present
QSFPDD1_3V3_RESET_L	Module reset
QSFPDD1_3V3_MODSEL_L	Mode select
QSFPDD1_3V3_LPMODE	Initial mode
QSFPDD1_3V3_INT_L	Interrupt
I2C_QSFPDD1_3V3_SCL	I <sup>2</sup> C clock
I2C_QSFPDD1_3V3_SDA	I <sup>2</sup> C data
QSFPDD1_TX_P/N[0:7]	Transceiver TX
QSFPDD1_RX_P/N[0:7]	Transceiver RX

### QSFPDD800/MXP

Agilex 7 FPGA I-Series Transceiver-SoC Development Kit supports 1x QSFPDD800 port. QSFPDD800 port fans out from Agilex 7 FPGA I-Series F-Tile (FHT). The FHT tile from bank 13A and 13C can run up to 116G PAM4. 4 FHT lanes from bank 13C is terminated directly to QSFPDD800 connector lanes [0:3] (J22).

**Table 16. QSFPDD800 (13A)**

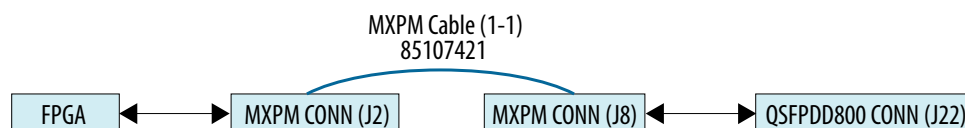
Schematic Signal Name	Description
QSFPDD800_3V3_MODPRS_L	Module present
QSFPDD800_3V3_RESET_L	Module reset
QSFPDD800_3V3_MODSEL_L	Mode select
QSFPDD800_3V3_LPMODE	Initial mode
QSFPDD800_3V3_INT_L	Interrupt
I2C_QSFPDD800_3V3_SCL	I <sup>2</sup> C clock
<i>continued...</i>	



Schematic Signal Name	Description
I2C_QSFPDD800_3V3_SDA	I <sup>2</sup> C data
QSFPDD800_TX_P/N[0:3]	Transceiver TX
QSFPDD800_RX_P/N[0:3]	Transceiver RX

Four FHT lanes from bank 13A are terminated to MXPM connector (J2). Other lanes [4:7] of QSFPDD800 connector is terminated to MXPM connector (J8). For x8 QSFPDD800 topology, 1-1 cable between J2 and J8 need to be used.

**Figure 37. MXPM Cable**



### MXP

MXP port fan out from Agilex 7 FPGA I-Series F-Tile (13A). All four channels can run up to 32G NRZ and 58G PAM4.

**Table 17. MXP**

Schematic Signal Name	Description
FGT_MXPM_TX_P/N[0:3]	Transceiver TX
FGT_MXPM_RX_P/N[0:3]	Transceiver RX

### FMC+ Connector

Agilex 7 FPGA I-Series Transceiver-SoC Development Kit supports 2x FMC+ slots for functional expandability. The x16 FGT lanes from bank 12C and 12A are terminated to FMC-A (J7) and FMC-B (J9) connectors, respectively. Auxiliary signals are controlled by the system MAX 10.

### SDI Connector

1x FGT channel (13C/Q0/CH3) been terminated to the HD-BNC TX (J1) and RX (J32) connectors to support up to 12G SDI. The system MAX 10 acts as an I<sup>2</sup>C master for both SDI driver and receiver, along with control signals.

### USB Type-C Connector

Agilex 7 FPGA I-Series Transceiver-SoC Development Kit has hardware support for the USB Type-C connector, which supports DP1.4 specification or USB 3.1 functionality through MUX (TUSB1146). This feature is yet to be validated and implemented.

### Serial Buses

SDM I/Os (SDM\_IO0/12) and MAX 10 I/Os (VCCL\_SDA/SCL) share the same I<sup>2</sup>C bus which communicate with Agilex 7 FPGA core regulators. By default, SDM acts as SmartVID master and the system MAX 10 act as Power GUI master in this chain.

The system MAX 10 I/Os (PMB\_SDA/SCL) manages the second I<sup>2</sup>C bus which access all I<sup>2</sup>C slave regulator except Agilex 7 FPGA core regulators.

The system MAX 10 supports I<sup>2</sup>C master dedicated to clock-related devices (CLK\_I2C\_SDA/SCL), which manages 3# clock devices and also connected to the HPS I/Os (HPS\_GPIO30/31) through level translator.

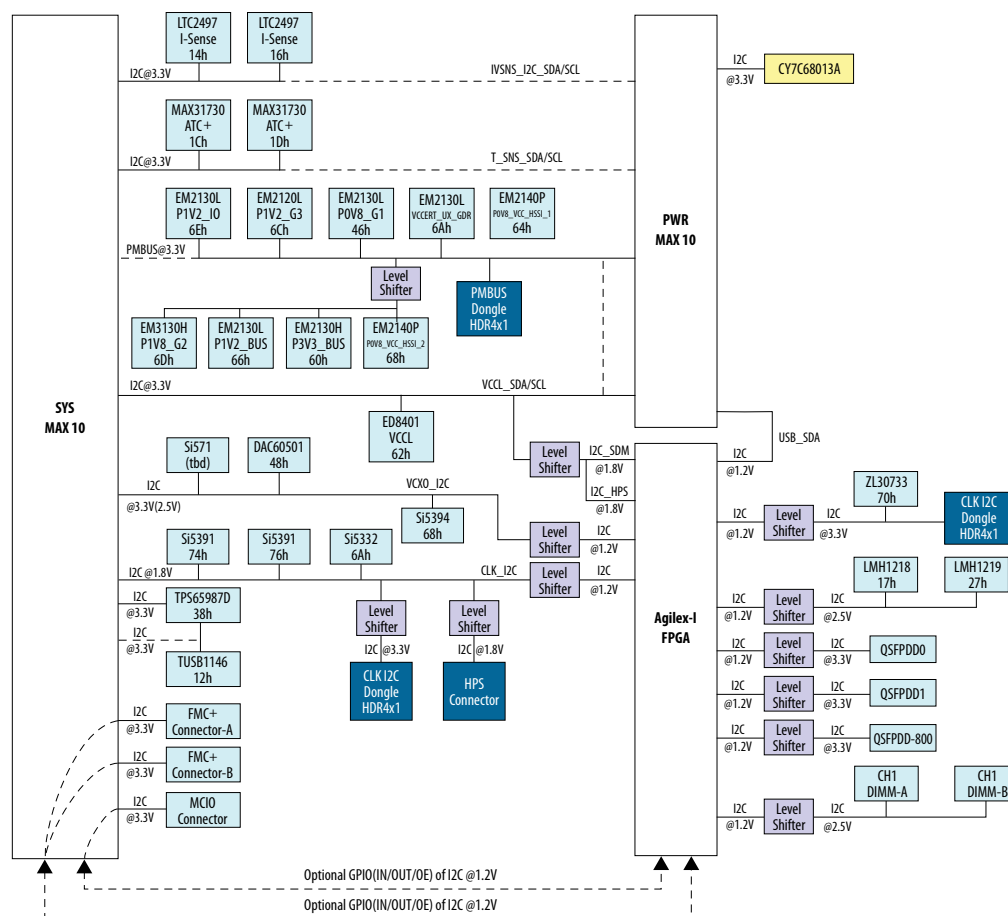
Another I<sup>2</sup>C master instance from the system MAX 10 (VCXO\_I2C\_SDA/SCL) controls the on board VCXO and Si5394 clock generator.

Agilex 7 FPGA also manages QSFPPD800, 2x QSFPPD, 2DPC DIMM I<sup>2</sup>C buses, SDI transceivers, and ZL30733 clock synthesizer device.

**Table 18. I<sup>2</sup>C Debug Headers**

Schematic Signal Name	Description
PMB_SCL/SDA	VRs I <sup>2</sup> C header J41
CLK_I2C_SDA/SCL_3V3	System MAX 10 clock I <sup>2</sup> C bus header J42
ZL_I2C_SDA/SCL	ZL30733 I <sup>2</sup> C access header J21

**Figure 38. I<sup>2</sup>C Serial Bus (Intel Enpirion) DK-SI-AGI027FB and DK-SI-AGI027FES**



## HPS IO48 OOB Daughter Card

- 1x RGMII 10/100/1000 Mbps Ethernet port: Standard RJ-45
- 1x UART port: Standard USB Mini-B Receptacle
- 1x Micro SD Card Connector: Standard Micro SD Card Socket
- 1x USB 2.0 port: Standard USB Micro-AB Receptacle
- 1x Mictor 38-pin connector (JTAG only without Trace signals)
- HPS dedicated JTAG pins are connected with both mother board JTAG chain and Mictor 38-pin header

- I<sup>2</sup>C: HPS I<sup>2</sup>C port
- GPIO
  - 2x Push buttons
  - 3x LEDs
  - 1x Ethernet Interrupt from Ethernet PHY
  - 1x USB over-current indicator
- HPS Clock: 25 MHz oscillator

### 256 MB QSPI Flash Daughter Card

This daughter card is pre-programmed with GHRD for AS configuration. It can be re-programmed by customer image. The part number is MT25QU02GCBB8E12-0SIT.

## A.8. Connectors and Cables

**Table 19. Connectors and Cables**

Connectors and Cables	Part Number	Switch Reference	Notes
QSFPDD loopback module	NLNAMB0001 (Amphenol)	J27 J48 J22 (for use up to 400 G)	—
QSFP-DD800 loopback type 1	ML4062-LB-112 (Multilane)	J22	For 800 G usage, connect 85107421 at J2 and J8
MXMP breakout cable	85107421 (Huber + Suhner)	J2–J8	Connect between J2 and J8
MCIO cable	HMC74-0631 (Amphenol)	J37	—
HD-BNC Straight Plug to HD-BNC Straight Plug	095-850-214M100 (Amphenol)	J1 J32	SDI loopback between J1 and J32

## B. Developer Resources

Use the following links to check the Intel website for other related information.

**Table 20.     Agilex 7 FPGA I-Series Transceiver-SoC Development Kit References**

Reference	Description
<a href="#">Agilex 7 FPGA I-Series Transceiver-SoC Development Kit page</a>	Latest board design files, reference designs, and kit installation for Windows* and Linux*.
<a href="#">Agilex 7 FPGA Board Design Guided Journey</a>	The interactive FPGA Board Guided Journey provides step-by-step guidance for developing printed circuit boards (PCBs) using Agilex 7 devices.
<a href="#">AN 958: Board Design Guidelines</a>	Board design-related resources for Altera devices. Its goal is to help you implement successful high-speed PCBs that integrate device(s) and other elements.
<a href="#">Agilex 7 Power Management User Guide</a>	Describes the Agilex 7 devices power-optimization features, power-up and power-down sequences, power distribution network, voltage and temperature monitoring systems with a design example to read the TSDs, and power optimization techniques.
<a href="#">Agilex 7 Power Distribution Network Design Guidelines</a>	Provides information for the Agilex 7 device family power distribution network (PDN) design guidelines.
<a href="#">FPGA SmartVID</a>	SmartVID is a feature on select Altera FPGAs where the device identifies the optimal voltage that it should be operated at, and provides this information to the power regulator via the PMBus. The term represents Smart Voltage Identification (SmartVID).
<a href="#">SmartVID Debug Checklist and Voltage Regulator Guidelines</a>	Provides the checklist to assist you to rule out the possible causes of configuration failure due to SmartVID.
<a href="#">Agilex 7 Configuration User Guide</a>	Provides the configuration process, the device pins required for configuration, the available configuration schemes, remote system updates, and debugging. This user guide also provides an overview of the secure device manager (SDM) which manages security for the configuration bitstream.
<a href="#">Documentation: Agilex 7</a>	Agilex 7 device documentation.
<a href="#">Cadence* Capture CIS Schematic Symbols</a>	Agilex 7 OrCAD symbols.



## C. Safety and Regulatory Compliance Information

---

### C.1. Safety and Regulatory Information



#### **ENGINEERING DEVELOPMENT PRODUCT - NOT FOR RESALE OR LEASE**

This development kit is intended for laboratory development and engineering use only.

This development kit is designed to allow:

- Product developers and system engineers to evaluate electronic components, circuits, or software associated with the development kit to determine whether to incorporate such items in a finished product.
- Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required Federal Communications Commission (FCC) equipment authorizations are first obtained.

Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference.

Unless the assembled kit is designed to operate under Part 15, Part 18 or Part 95 of the United States Code of Federal Regulations (CFR) Title 47, the operator of the kit must operate under the authority of an FCC licenseholder or must secure an experimental authorization under Part 5 of the United States CFR Title 47.

Safety Assessment and CE & UKCA mark requirements have been completed, however, other certifications that may be required for installation and operation in your region have not been obtained.

### C.1.1. Safety Warnings





#### Power Supply Hazardous Voltage

AC mains voltages are present within the power supply assembly. No user serviceable parts are present inside the power supply.


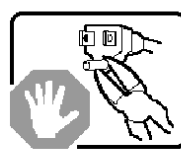
#### Power Connect and Disconnect

The AC power supply cord is the primary disconnect device from mains (AC power) and used to remove all DC power from the board/system. The socket outlet must be installed near the equipment and must be readily accessible.

	<b>WARNING</b>	
<b>RISK OF ELECTRIC SHOCK</b>		
<p>Connect only to a properly earth grounded outlet.          Apparaten skall anslutas till jordat uttag när den ansluts till ett nätverk.</p>		

#### System Grounding (Earthing)

To avoid shock, you must ensure that the power cord is connected to a properly wired and grounded receptacle. Ensure that any equipment to which this product is attached to is also connected to properly wired and grounded receptacles.

	<b>WARNING</b>	
<b>RISK OF ELECTRIC SHOCK</b>		
<p>Do not attempt to modify or use the supplied AC power cord if it is not the exact type and rating required.</p>		

### Power Cord Requirements

The plug on the power cord must be a grounding-type male plug designed for use in your region. It must have certification marks showing certification by an agency in your region. The connector that plugs into the appliance inlet of the power supply must be an IEC 320, sheet C13, female connector. If the power cord supplied with the system does not meet requirements for use in your region, discard the cord, and do not use it with adapters. Use only certified power supply cord with appropriate gauge, designed for use in your region.



### Lightning/Electrical Storm

Do not connect/disconnect any cables or perform installation/maintenance of this product during an electrical storm.

### Risk of Fire

To reduce the risk of fire, keep all flammable materials a safe distance away from the boards and power supply. You must configure the development kit on a flame retardant surface.

## C.1.2. Safety Cautions

	CAUTION	
	Hot Surfaces and Sharp Edges	
Integrated Circuits and heat sinks may be hot if the system has been running. Also, there might be sharp pins and edges on some boards. Contact should be avoided.		

### Thermal and Mechanical Injury

Certain components such as heat sinks, power regulators, and processors may be hot. Heatsink fans are not guarded. Power supply fan may be accessible through guard. Care should be taken to avoid contact with these components.





### **Cooling Requirements**

Maintain a minimum clearance area of 5 centimeters (2 inches) around the side, front and back of the board for cooling purposes. Do not block power supply ventilation holes and fan.

### **Electro-Magnetic Interference (EMI)**

This equipment has not been tested for compliance with emission limits of FCC and similar international regulations. Use of this equipment in a residential location is prohibited. This equipment generates, uses and can radiate radio frequency energy which may result in harmful interference to radio communications. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment on and off, you are required to take measures to eliminate this interference.

### **Telecommunications Port Restrictions**

The wireline telecommunications ports (modem, xDSL, T1/E1) on this product must not be connected to the Public Switched Telecommunication Network (PSTN) as it might result in disruption of the network. No formal telecommunication certification to FCC, R&TTE Directive, or other national requirements have been obtained.



### Electrostatic Discharge (ESD) Warning

A properly grounded ESD wrist strap must be worn during operation/installation of the boards, connection of cables, or during installation or removal of daughter cards. Failure to use wrist straps can damage components within the system.

**Attention:** Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of this product in unsorted municipal waste.

### Lithium Ion Battery Warnings



**Lithium Battery:** Risk of explosion if the lithium battery is replaced by an incorrect type. Risk of fire, explosion, or chemical burn if the battery is mistreated (punctured or crushed). Do not attempt to disassemble. Do not incinerate. Observe proper polarity when replacing battery. Do not dispose—the battery is intended to be serviced and disposed by qualified Intel service personnel only.

**Perchlorate Material:** Special handling may apply. For more details, refer to [www.dtsc.ca.gov/hazardouswaste/perchlorate](http://www.dtsc.ca.gov/hazardouswaste/perchlorate). This notice is required by California Code of Regulations, Title 22, Division 4.5, Chapter 33: Best Management Practices for Perchlorate Materials. This product includes a battery which contains perchlorate material.

### Taiwan battery recycling:



廢電池請回收

(Translation - please recycle batteries)

**Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of product in unsorted municipal waste.**

## C.2. Compliance Information

### CE EMI Conformity Caution

This development board is delivered conforming to relevant standards mandated by Directive 2014/30/EU. Because of the nature of programmable logic devices, it is possible for the user to modify the development kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as a result of modifications to the delivered material is the responsibility of the user of this development kit.

