Intel Agilex® 5 Device HSIO IBIS Models User Guide

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1.0 INTRODUCTION

Intel Agilex® 5 device HSIO IBIS models model the operation of the HSIO buffers across different process, voltage, and temperature conditions. The IBIS file has been tested and verified using commercial tools.

This document explains how to use the IBIS models in simulations and contains a list of all IBIS models that the existing version of the Intel Agilex® 5 device HSIO IBIS models support.

For proper termination schemes, please refer to HSIO Termination topic in Intel Agilex® 5 General-Purpose I/O User Guide. Please also refer to the user guide for default settings (e.g., pre-emphasis, OCT, etc.…) of each I/O standard. The user guide can be obtained from Intel Website when available.

Please note that IBIS model is intended to target extreme operating conditions of the Intel devices. Therefore, Min and Max corner settings in the IBIS model might defer from datasheet to consider package, die IR drop, and functional max value to avoid running into hold-time violations in simulation.

2.0 IBIS FILE INSTRUCTION

The IBIS file is currently using IBIS Specification v5.0. There are additional keywords that are supported in v5.0 but not in previous versions. Users are advised to use Visual IBIS Editor with IBIS specification of 5.0 onwards. This is to prevent any error which might be prompted from IBIS checker on updated keywords which are available in IBIS Specification v5.0 but are not backward compatible.

Package resistance, inductance, and capacitance (RLC) values that are currently defined under [Package] section in the IBIS file contains lumped RLC value for A5ED065BB32A package. For other packages model values, please refer to the **intel-agilex-5-device-pkg-rlc.xlsx** excel sheet which contains all supported packages for Intel Agilex® 5 device. The excel sheet can be obtained from Intel Website when available.

The IBIS file contains multiple models. Please refer to section 3.0 below for details on models naming conventions.

3.0 NAMING NOMENCLATURE

All models follow naming method below:
<I/O standard>_<I/O>_<Feature1>_<Feature2>

where,

<I/O Standard> refers to:

lv13	-	1.3 V LVCMOS
lv12	-	1.2 V LVCMOS
lv11	-	1.1 V LVCMOS
lv105	-	1.05 V LVCMOS
lv10	-	1.0 V LVCMOS
sstl12	-	SSTL-12
hstl12	-	HSTL-12
hsul12	-	HSUL-12
pod12	-	POD12
pod11	-	POD11
lvstl11	-	LVSTL11
lvstl105	-	LVSTL105
lvstl700_105v	-	LVSTL700 1.05 V
dsstl12	-	Differential SSTL-12
dhstl12	-	Differential HSTL-12
dhsul12	-	Differential HSUL-12
dpod12	-	Differential POD12
dpod11	-	Differential POD11
dlvstl11	-	Differential LVSTL11
dlvstl105	-	Differential LVSTL105
dlvstl700_105v	-	Differential LVSTL700 1.05 V
slvs400_dphyhs_12v	-	SLVS-400/DPHY HS 1.2 V
slvs400_dphyhs_11v	-	SLVS-400/DPHY HS 1.1 V
dphylp_12v	-	DPHY LP 1.2 V
dphylp_11v	-	DPHY LP 1.1 V
tds13	-	True Differential Signaling 1.3 V

<I/O> refers to:

in	-	Input pin
io	-	Bidirectional I/O
out	-	Output pin

<Feature1> or ***<Feature2>*** refers to:

wpu	-	weak pull-up resistor
us0	-	uncompensated slow slew rate
us1	-	uncompensated medium slew rate
us2	-	uncompensated fast slew rate
cs0	-	compensated slow slew rate
cs1	-	compensated medium slew rate
cs2	-	compensated fast slew rate

s3	-	fastest slew rate
r34	-	34ohm series on-chip termination without calibration
r40	-	40ohm series on-chip termination without calibration
r110	-	110ohm series on-chip termination without calibration
r34c	-	34ohm series on-chip termination with calibration
r40c	-	40ohm series on-chip termination with calibration
r45c	-	45ohm series on-chip termination with calibration
doff	-	disabled de-emphasis
dl	-	low de-emphasis
dm	-	medium de-emphasis
dh	-	high de-emphasis
dlc	-	low constant impedance de-emphasis
dmc	-	medium constant impedance de-emphasis
dhc	-	high constant impedance de-emphasis
poff	-	disabled pre-emphasis
pon	-	enabled pre-emphasis
vlow	-	low differential output voltage
vmlow	-	medium low differential output voltage
vmhigh	-	medium high differential output voltage
vhigh	-	high differential output voltage

Example: dpod12_io_cs2r40c_doff refers to Differential POD12 I/O standard with compensated fast slew rate, 40ohm series on-chip termination with calibration, and de-emphasis disabled.

4.0 LIST OF INTEL AGILEX® 5 DEVICE HSIO IBIS MODELS

HSIO_Model_List worksheet in **intel-agilex-5-device-model-list.xlsx** excel sheet contains all supported models for the Intel Agilex® 5 device HSIO IBIS models version 1.0. The excel sheet can be obtained from Intel Website when available.

5.0 INTEL AGILEX® 5 DEVICE HSIO IBIS FILE REVISION HISTORY

Date	Version	Description
March 2024	1.0	Preliminary release. Subject to change.

6.0 INTEL AGILEX® 5 DEVICE HSIO IBIS MODELS USER GUIDE REVISION HISTORY

Date	Version	Description
March 2024	1.0	Initial release of Intel Agilex® 5 Device HSIO IBIS Models User Guide