Intel Agilex® 5 Device HVIO IBIS Models User Guide

Contents

1.0 INTRODUCTION

Intel Agilex® 5 device HVIO IBIS models model the operation of the HVIO buffers across different process, voltage, and temperature conditions. The IBIS file has been tested and verified using commercial tools.

This document explains how to use the IBIS models in simulations and contains a list of all IBIS models that the existing version of the Intel Agilex® 5 device HVIO IBIS models support.

Please refer to Intel Agilex® 5 General-Purpose I/O User Guide for default settings (e.g., current strength, weak pull-up/pull-down, etc…) for each I/O standard. The user guide can be obtained from Intel Website when available.

Please note that IBIS model is intended to target extreme operating conditions of Intel devices. Therefore, Min and Max corner settings in the IBIS model might defer from datasheet to consider package, die IR drop, and functional max value to avoid running into hold-time violations in simulation.

2.0 IBIS FILE INSTRUCTION

The IBIS file is currently using IBIS Specification v5.0. There are additional keywords that are supported in v5.0 but not in previous versions. Users are advised to use Visual IBIS Editor with IBIS specification of 5.0 onwards. This is to prevent any error which might be prompted from IBIS checker on updated keywords which are available in IBIS Specification v5.0 but are not backward compatible.

Package resistance, inductance, and capacitance (RLC) values that are currently defined under [Package] section in the IBIS file contains lumped RLC value for A5ED065BB32A package. For other packages model values, please refer to the **intel-agilex-5-device-pkg-rlc.xlsx** excel sheet which contains all supported packages for Intel Agilex® 5 device. The excel sheet can be obtained from Intel Website when available.

The IBIS file contains multiple models. Please refer to section 3.0 below for details on models naming conventions.

3.0 NAMING NOMENCLATURE

All models follow naming method below:
<I/O standard>_<I/O>_<Feature1>_<Feature2>

where,

<I/O Standard> refers to:

lv33	-	3.3 V LVCMOS/LVTTL
lv25	-	2.5 V LVCMOS/LVTTL
lv18	-	1.8 V LVCMOS/LVTTL

<I/O> refers to:

in	-	Input pin
io	-	Bidirectional I/O

<Feature1> or ***<Feature2>*** refers to:

20wpu	-	weak pull-up with 20 kohm resistor
20wpd	-	weak pull-down with 20 kohm resistor
od	-	enabled open-drain output
d3	-	3 mA current strength
d6	-	6 mA current strength
d9	-	9 mA current strength
d12	-	12 mA current strength

Example: lv33_io_od_d12 refers to 3.3 V LVCMOS/LVTTL I/O standard with 12 mA current strength and open-drain output enabled.

4.0 LIST OF INTEL AGILEX® 5 DEVICE HVIO IBIS MODELS

HVIO_Model_List worksheet in **intel-agilex-5-device-model-list.xlsx** excel sheet contains all supported models for the Intel Agilex® 5 device HVIO IBIS models version 1.0. The excel sheet can be obtained from Intel Website when available.

5.0 INTEL AGILEX® 5 DEVICE HVIO IBIS FILE REVISION HISTORY

Date	Version	Description
March 2024	1.0	Preliminary release. Subject to change.

6.0 INTEL AGILEX® 5 DEVICE HVIO IBIS MODELS USER GUIDE REVISION HISTORY

Date	Version	Description
March 2024	1.0	Initial release of Intel Agilex® 5 Device HVIO IBIS Models User Guide