

Agilex[™] 7 FPGA I-Series Development Kit User Guide



Online Version

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UG-20338

683288

2024.05.31

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1. Overview

This user guide describes the design features and the usage of the Agilex™ 7 FPGA I-Series Development Kit (2x R-Tile & 1x F-Tile) board.

Table 1. Agilex 7 FPGA I-Series Development Kit Ordering Information

Development Kit Version	Ordering Code	Device Part Number	Starting Serial Number and Range
Agilex 7 FPGA I-Series Development Kit (Production 2x R-Tile & 1x F-Tile) (Power Solution 2)	DK-DEV-AGI027-RA	AGIB027R29A1E1VB	8100505
Agilex 7 FPGA I-Series Development Kit (ES2 2x R-Tile & 1x F-Tile) (Power Solution 2)	DK-DEV-AGI027RBES	AGIB027R29A1E2VR3	8020001
Agilex 7 FPGA I-Series Development Kit (ES1 2x R-Tile & 1x F-Tile) (Power Solution 1)	DK-DEV-AGI027R1BES	AGIB027R29A1E2VR3	8000311 – 8010000 8100000 – 8100242
Agilex 7 FPGA I-Series Development Kit (ES 2x R-Tile & 1x F-Tile) (Power Solution 1)	DK-DEV-AGI027RES	AGIB027R29A1E2VR0	8000001

For more details on Agilex 7 I-Series FPGAs, refer to the *Agilex FPGA Portfolio* page on the Intel website.

For more information about the *Agilex 7 Device Errata Sheet and User Guidelines (ES-1069)* and *Agilex 7 Known Issue List*, contact Intel Premier Support and quote ID #15011992053.

Related Information

[Agilex 7 FPGA and SoC FPGA I-Series](#)

1.1. Block Diagram

The demonstration board showcases the features of the Agilex 7 FPGA I-Series device in the F2957 FBGA package. These devices feature R-Tile transceivers with PCIe* Gen5 x16 and CXL⁽¹⁾ interfaces and F-Tile transceivers with 28G x8 or 56G x8 QSFPDD interfaces. The board supports two on-board DDR4 x72 with ECC channels. The board also features DDR4 DIMM support. Refer to the block diagrams for variations between board versions.

- ⁽¹⁾ To activate the CXL hard IP and receive CXL soft R-Tile Wrapper and Soft Support logic, purchase or activation of a separate CXL IP license is required for proper use with the Quartus® Prime Design Software. Contact your local Altera sales representative for pricing details. To activate a free-of-charge 30- or 60-days trial IP license, contact your local Altera sales representative.

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*Other names and brands may be claimed as the property of others.

Figure 1. Agilex 7 FPGA I-Series Development Kit Board Diagram

This diagram applies to DK-DEV-AGI027RES and DK-DEV-AGI027R1BES.

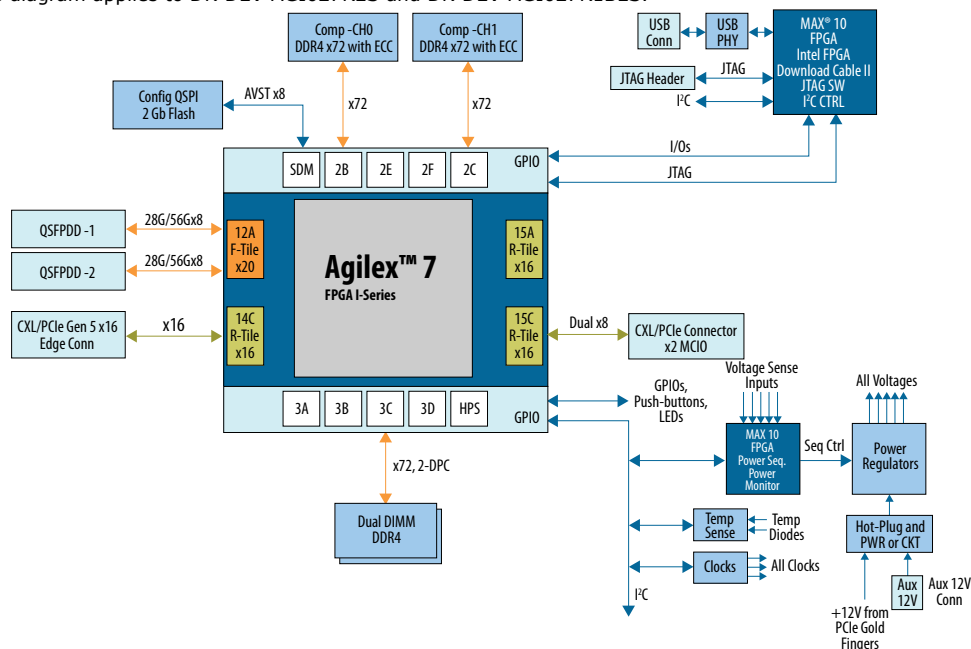
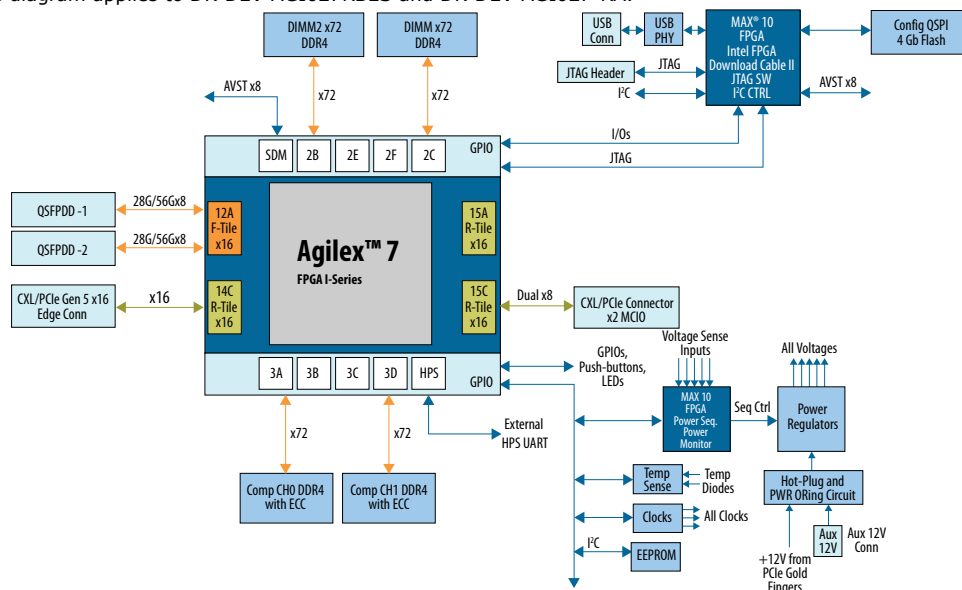


Figure 2. Agilex 7 FPGA I-Series Development Kit Board Diagram

This diagram applies to DK-DEV-AGI027RBES and DK-DEV-AGI027-RA.



Feature Summary

- Agilex 7 FPGA I-Series (AGIB027) device in the 2957A BGA package
 - 0.8 VID-adjustable VCC core
 - R-Tile transceivers supporting PCIe Gen5/CXL⁽¹⁾
 - F-Tile transceivers supporting 56 Gbps NRZ
- FPGA configuration
 - Partial reconfiguration support
 - Configuration via Protocol (CvP) configuration support
 - Storage for two configuration images in flash (factory and user)
 - JTAG header for device programming
 - Built-in Intel® FPGA Download Cable II for device programming
- Programmable clock sources
 - 156.25 MHz differential LVDS for F-Tile (QSFPDD)
 - 100.000 MHz HCSL for PCIe and CXL (R-Tile)
 - 33.33 MHz differential LVDS for memory
 - 125 MHz configuration clock
 - 100 MHz differential LVDS for I/O banks
- Transceiver interfaces
 - PCIe/CXL x16 interface supporting the Gen5 end-point mode connected to a x16 PCIe edge connector (gold edge fingers)
 - 2x standard QSFPDD optical module interfaces connected to the F-Tile transceivers
 - 1x PCIe/CXL⁽¹⁾ interface supporting CXL x16 or PCIe x16 at 32 Gbps via MCIO connectors
- Memory interfaces
 - Two on-board independent single rank DDR4 x72 (ECC) channels operating at 1333 MHz (DDR4-2666)
 - Two DIMM sockets which are either on a single memory channels (last two OPNs in Table 1) or each on independent channels (first two OPNs in Table 1). The DIMM supports DDR4 x72 (ECC) and can operate up to DDR-3200 (depending on the speed of the FPGA used).
- Communication ports
 - 2x QSFPDD optical interface port
 - JTAG header
 - USB (Micro USB) on-board Intel FPGA Download Cable II
 - System I2C header

- Buttons, switches, and LEDs
 - System reset push button
 - CPU reset push button
 - PCIe reset push button
 - Four dedicated user LEDs
 - Link LED of each QSFP28 port to indicate the link and data transceiver
 - Two dedicated configuration status LEDs
- Heatsink and Fan
 - Air-cooled heatsink assembly
 - Red over-temperature warning LED indicator
- Power
 - PCIe input power including required 2x4 auxiliary power connector
 - Blue power-on LED
 - On/off slide power switch for benchtop operation
 - On board power and temperature measurement circuitry
- Mechanical
 - PCIe standard height form factor (full height, 3/4 length, dual-width)
 - 4.376" x 10.0" board size
 - 2 slots height with heatsink
- Operating environment
 - Maximum ambient temperature of 0–35°C
- HPS dedicated interfaces (only available on selected board variants, see Figure 2)
 - JTAG connected to MAX10
 - I²C
 - UART connected to 3-Pin header

1.2. Box Contents

- Agilex 7 FPGA I-Series development board
- DDR4 DIMM module
- USB2.0 Micro-USB cable
- 240 W power adapter
- NA/EU/JP/UK cords

Note: Altera provides only one DIMM module Micron 16GB RDIMM (MTA18ASF2G72PZ-3G2J3) with each development kit.

1.3. Operating Conditions

Table 2. Recommended Operating Conditions

Operating Condition	Range
Recommended ambient operating temperature range	0°C to 35°C
Maximum ICC load current	198 A
Maximum ICC load transient percentage	30%
Maximum FPGA power supported by the supplied heatsink/fan	180 W

Handling Precautions

When handling the board, observe static discharge precautions.

Caution: Without proper anti static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

Caution: This development kit should not be operated in a vibration environment.



2. Getting Started

2.1. About Quartus Prime Software

The new Quartus Prime Design Suite design software includes everything needed to design for Altera FPGAs, SoCs, and CPLDs from design entry and synthesis to optimization, verification, and simulation. The Quartus Prime Design Suite software includes an additional Spectra-Q® engine that is optimized for Agilex 7 devices. The Spectra-Q engine enables new levels of design productivity for next generation programmable devices with a set of faster and more scalable algorithms, a hierarchical database infrastructure, and a unified compiler technology.

The Agilex 7 FPGA I-Series Development Kit is supported by the Quartus Prime Pro Edition.

The Quartus Prime Pro Edition is optimized to support the advanced features in Altera's next generation FPGAs and SoCs, starting with the Arria® 10 device family and requires a paid license.

Included in the Quartus Prime Pro Edition are the Quartus Prime software, Nios® II EDS, and the Altera FPGA IP Library. To install Altera's development tools, download the Quartus Prime Pro Edition software from the Quartus Prime Pro Edition page in the [Download Center](#) of Intel's website.

2.1.1. Activating Your License

Before using the Quartus Prime software, you must activate your license, identify specific users and computers, and obtain and install license file. If you already have a licensed version of the Quartus Prime Standard Edition or Quartus Prime Pro Edition, you can use that license file with this kit. If not, follow these steps:

1. Log on at the [My Intel Account Sign In](#) web page and click **Sign In**.
2. On the My Intel Home web page, click the [Self-Service Licensing Center](#) link.
3. Locate the serial number printed on the side of the development kit box below the bottom bar code. The number consists of alphanumeric characters and does not contain hyphens.
4. On the Self-Service Licensing Center web page, click the **Find it with your License Activation Code** link.
5. In the **Find/Activate Products** dialog box, enter your development kit serial number and click **Search**.

2.2. Development Board Package

Download the Agilex 7 FPGA I-Series Development Kit package from the [Agilex 7 FPGA I-Series Development Kit page](#) of the Intel website.

Unzip the Agilex 7 FPGA I-Series Development Kit package.

Figure 3. Installed Development Kit Directory Structure

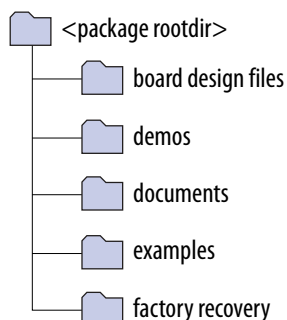


Table 3. Installed Development Kit Directory Description

Directory Name	Description of Directory Contents
board_design_files	Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications when available.
documents	Contains documentation.
examples	Contains sample design files for this board.
factory_recovery	Contains the original image/binary programmed onto the board before shipment. Use this image to restore the board with its original factory content.

Related Information

[Agilex 7 FPGA I-Series Development Kit](#)

2.3. Installing the Intel FPGA Download Cable II Driver

The development board includes integrated Intel FPGA Download Cable II circuits for FPGA programming. However, for the host computer and board to communicate, you must install the on-board Intel FPGA Download Cable II driver on the host computer.

Installation instructions for the on-board Intel FPGA Download Cable II driver for your operating system are available on the [Intel website](#).

On the [Cable and Adapter Drivers Information](#) web page of the Intel website, locate the table entry for Intel FPGA Download Cable II and click the link to access the instructions.

3. Development Board Setup

This chapter describes how to apply power to the development board and provides default switch and jumper settings.

3.1. Applying Power to the Development Board

This development kit is designed to operate in two modes:

As a PCIe Add-In Card

When operating the add-in card as a PCIe end-point, insert the add-in card into an available PCIe slot and connect a 2x4 pin PCIe power cable from the system to power connectors at **J11** of the board.

Note: When operating as a PCIe add-in card, the board does not power on unless power is supplied to **J11**.

In Bench-Top Mode

In bench-top mode, you must supply the board with the provided 240 W power supply connected to the power connector **J11**. The following describes the operation in bench-top mode.

This development board ships with its switches preconfigured to support the design examples in the kit.

If you suspect that your board may not be correctly configured with the default settings, follow the instructions in the [Default Switch Settings](#) on page 12.

1. Connect the supplied power supply to an outlet and the DC Power Jack (**J11**) on the FPGA board.

Note: Use only the supplied power supply. Power regulation circuits on the board can be damaged by power supplies with greater voltage.

2. Set the power switch (**SW6**) to the **ON** position.

When the board powers up, the blue power LED illuminates and the board is ready for use.

The blue LED (**D6**) illuminates to indicate that all the power rails on the board are good. If the POWER GOOD LED (**D6**) is not illuminated, it indicates that the power supply malfunctioned, and the board does not power up.

Caution: Standby powers are always present as soon as the Aux power is applied to **J11**. Use power switch **SW6** to start the board.

3.2. Default Switch Settings

This section describes the functionality and default settings for the switches on the board.

3.2.1. Default Settings

The Agilex 7 FPGA I-Series Development Kit ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be correctly configured with the default settings, follow the instructions in the tables below to return to the factory settings before proceeding.

Table 4. Factory Default Switch Settings for DK-DEV-AGI027RES and DK-DEV-AGI027R1BES

Note: X refers to Don't Care in this table.

For more information, refer to [Board Overview](#) on page 47.

Switch	Default Position	Function				
SW1[1:4]	ON/OFF/OFF/OFF	PCIe PRSNT x1/x4/x8/x16 settings. Default = x16.				
		PCIe PRSNT x16	PCIe PRSNT x8	PCIe PRSNT x4	PCIe PRSNT x1	
		ON	OFF	OFF	OFF	
SW2[1:4]	ON/OFF/OFF/X	Configuration mode setting bits.				
		Mode	MSEL0	MSEL1	MSEL2	Reserved
		JTAG	OFF	OFF	OFF	X
		AVST x8	ON	OFF	OFF	X
SW3[1:4]	OFF/ON/ON/OFF	Type	ON (Close)		OFF (Open)	
		1: Si5391 Clock Enable	Disable all clocks		Enable all Clocks	
		2: CXL REFCLK Select	CLK from CXL Connector		On-board REFCLK	
		3: PCIe REFCLK Select	CLK from PCIe Connector		On-board REFCLK	
		4: Si52204 Clock Enable	Disable all clocks		Enable all Clocks	
SW4	OFF/OFF/OFF/OFF	Type	ON (Close)		OFF (Open)	
		1: FPGA I2C Enable	MAIN I2C bus disable		MAIN_I2C bus enable	
continued...						

Switch	Default Position	Function		
		2: FPGA I2C_2 Enable	I2C2 Bus disable	I2C2 Bus enable
		3: Main PMBUS Enable	CORE PMBUS disable	CORE PMBUS enable
		4: FPGA PMBUS Enable	SDM_I2C Bus disable	SDM_I2C Bus enable
SW5[1:4]	OFF/OFF/OFF/X	On-board Intel FPGA Download Cable II is the JTAG host when the external JTAG header (J10) is unoccupied.		
		Type	ON	OFF
		1: JTAG input source	PCIe EP Edge connector	On-Board Intel FPGA Download Cable II
		2: FPGA Bypass	Bypass FPGA	FPGA in JTAG chain
		3: MAX® 10 JTAG Select	MAX 10 JTAG Enable	MAX 10 JTAG Disable
		4: Not used	X	X
SW6	ON/OFF	When the board is not in a PCIe slot, it must be powered by an external power supply. The SW6 switch turns on the power of the board when it is at the ON position and turns off the power when it is at the OFF position.		
		When the board is in a PCIe slot, the external and auxiliary power supplies must still be connected. The SW6 switch can be left at either the ON or OFF position. The board can only be powered on when both power sources are present.		

Table 5. Factory Default Switch Settings for DK-DEV-AGI027RBES and DK-DEV-AGI027-RA

Note: X refers to Don't Care in this table.

For more information, refer to [Board Overview](#) on page 47.

Switch	Default Position	Function				
SW1[1:4]	ON/OFF/OFF/OFF	PCIe PRSNT x1/x4/x8/x16 settings. Default = x16.				
		PCIe PRSNT x16	PCIe PRSNT x8	PCIe PRSNT x4	PCIe PRSNT x1	
		ON	OFF	OFF	OFF	
SW2[1:4]	ON/OFF/OFF/X	Configuration mode setting bits.				
		Mode	MSEL0	MSEL1	MSEL2	Reserved
		JTAG	OFF	OFF	OFF	X
		AVST x8	ON	OFF	OFF	X
SW3[1:4]	OFF/OFF/OFF/OFF	Type	ON (Close)		OFF (Open)	
		1: Si5391 Clock Enable	Disable all clocks		Enable all Clocks	
continued...						

Switch	Default Position	Function		
		2: CXL REFCLK Select	CLK from CXL Connector	On-board REFCLK
		3: PCIe REFCLK Select	CLK from PCIe Connector	On-board REFCLK
		4: Si52204 Clock Enable	Disable all clocks	Enable all Clocks
SW4[1:4]	OFF/OFF/ON/OFF	Type	ON (Close)	OFF (Open)
		1: FPGA I2C Enable	MAIN I2C bus disable	MAIN_I2C bus enable
		2: FPGA I2C_2 Enable	I2C2 Bus disable	I2C2 Bus enable
		3: Main PMBUS Enable	CORE PMBUS disable	CORE PMBUS enable
		4: FPGA PMBUS Enable	SDM_I2C Bus disable	SDM_I2C Bus enable
SW8[1:4]	OFF/OFF/OFF/X	On-board Intel FPGA Download Cable II is the JTAG host when the external JTAG header (J10) is unoccupied.		
		Type	ON	OFF
		1: JTAG input source	PCIe EP Edge connector	On-Board Intel FPGA Download Cable II
		2: FPGA Bypass	Bypass FPGA	FPGA in JTAG chain
		3: MAX 10 JTAG Select	MAX 10 JTAG Enable	MAX 10 JTAG Disable
		4: Not used	X	X
SW6	ON/OFF	<p>When the board is not in a PCIe slot, it must be powered by an external power supply. The SW6 switch turns on the power of the board when it is at the ON position and turns off the power when it is at the OFF position.</p> <p>When the board is in a PCIe slot, the external and auxiliary power supplies must still be connected. The SW6 switch can be left at either the ON or OFF position. The board can only be powered on when both power sources are present.</p>		

Figure 4. SW1[1:4] Switch Setting

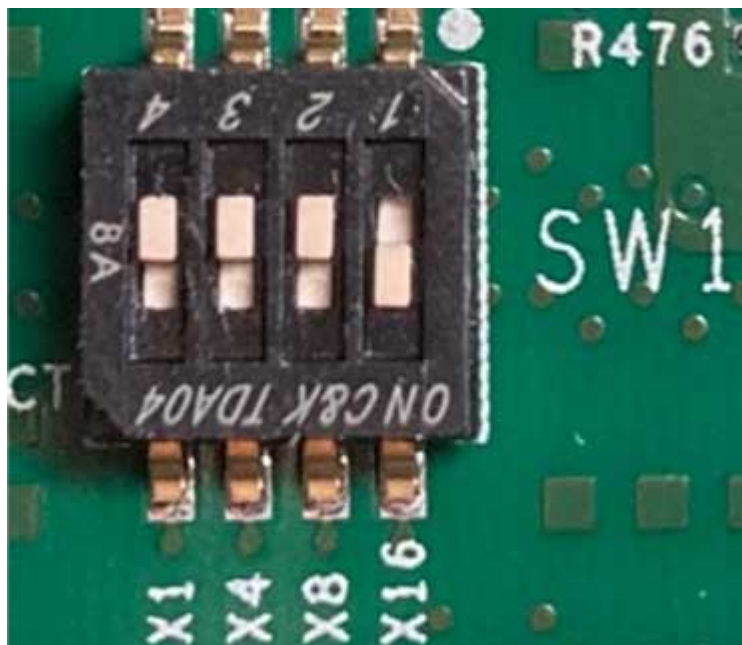


Figure 5. SW2[1:4] Switch Setting

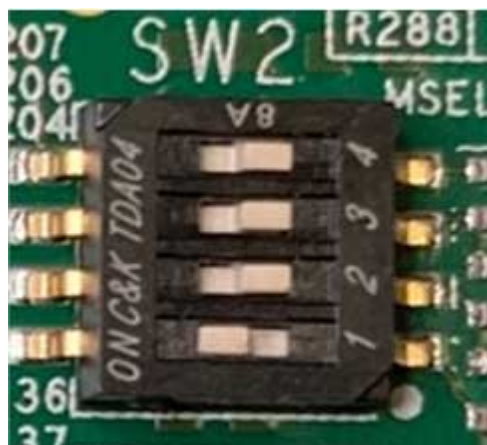


Figure 6. SW3[1:4] Switch Setting

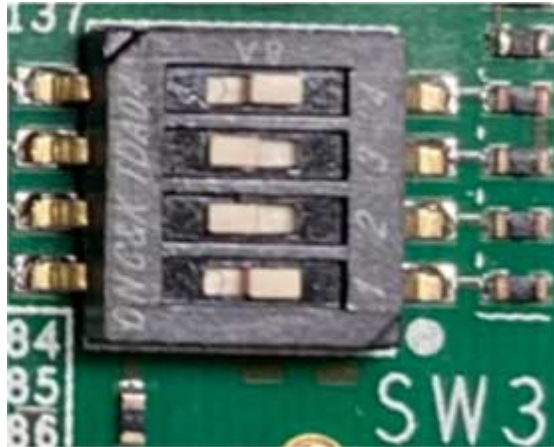


Figure 7. SW4[1:4] Switch Setting

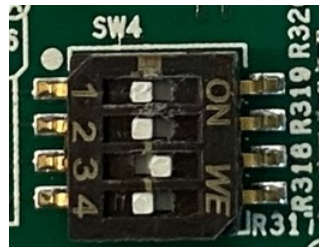


Figure 8. SW5[1:4] Switch Setting



Figure 9. SW8[1:4] Switch Setting

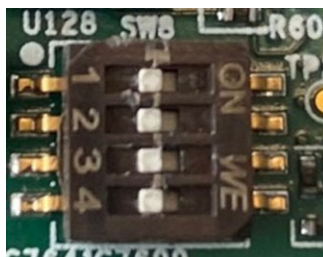


Table 6. Connectors on the Development Kit

Board Reference	Type	Description
J11	Auxiliary power connector	For the external 12V auxiliary power supply or power adapter
J12	I2C/PMBus connector	For accessing core power controller
J13	I2C connector	For accessing to the main I2C1 bus
J3	QSFPDD_0 connector	—
J4	QSFPDD_1 connector	—
J8	USB connector	For programming the FPGA using on-board Intel FPGA Download Cable II
J10	External JTAG header	For use with the external download cable
J1	DIMM A connector	DDR4 Dual DIMM A
J2	DIMM B connector	DDR4 Dual DIMM B
J5	PCIe x16 Gold Finger	—
J6, J7	CXL/PCIe connectors	For connecting the external CXL/PCIe MCIO cables
J24	Fan connector	For connecting to the heatsink cooling fan

Table 7. LEDs on the Development Kit

Board Reference	Type	Description
D1	QSFPDD_0 Link/Activity LED	Green LED - User defined
D2	QSFPDD_0 Link/Activity LED (Dual color)	Yellow LED - User defined Green LED - User defined
D3	QSFPDD_1 Link/Activity LED	Green LED - User defined
D4	QSFPDD_1 Link/Activity LED (Dual color)	Yellow LED - User defined Green LED - User defined
D5	USER LED 0	Green LED for USER LED 0
D7	USER LED 1	Green LED for USER LED 1
D8	USER LED 2	Green LED for USER LED 2
D10	USER LED 3	Green LED for USER LED 3

continued...

Board Reference	Type	Description
D6	POWER GOOD LED	Blue LED: <ul style="list-style-type: none"> ON: All powers are good. OFF: Power failure
D11	CONFIG DONE LED	Green LED: <ul style="list-style-type: none"> ON: FPGA configuration successful OFF: FPGA configuration failed
D9	Over Temp LED	Red LED: <ul style="list-style-type: none"> ON: FPGA over temperature condition

Table 8. Push-Buttons on the Development Kit

Board Reference	Type	Description
S1	CPU Reset	Push to reset FPGA
S2	PCIe Reset	Push to reset PCIe bus on MCIO connectors (J6 and J7)
S3	CXL Reset	Push to reset CXL bus on MCIO connectors (J6 and J7)
S4	USB PHY Reset	Push to reset on-board USB PHY
S5	QSFPDD_1 Reset	Push to reset F-tile for QSFPDD_1 port

3.2.2. Perform Board Restore through Quartus Prime Programmer

The development kit ships with FPGA design examples stored in the QSPI flash device and the MAX 10 pre-programmed. If you want to restore the QSPI flash with the factory default image, follow these steps:

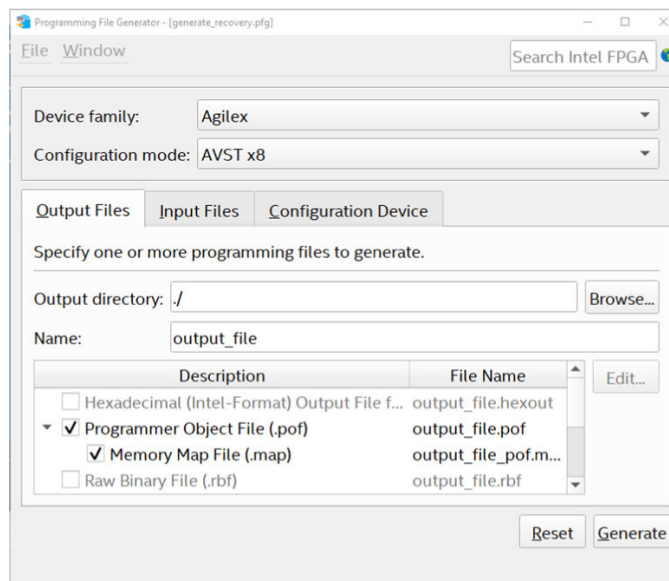
1. Connect the USB cable between the **J8** USB connector and your computer.
2. Open the Quartus Prime Programmer GUI, detect the JTAG chain, and attach the factory default image to the MAX 10 device.
3. Select programming options and click the program button.

3.3. How to Generate a POF Image to Program the Flash

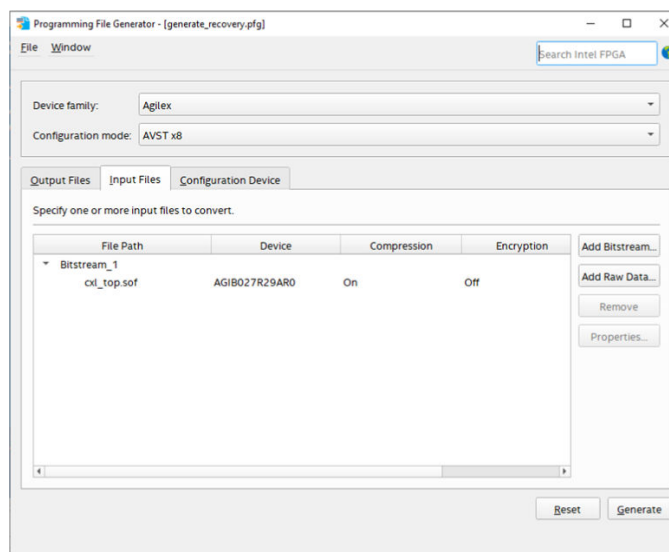
Note: If you already have a Programmer Object File (.pof), you can skip this section.

To generate a POF image to program the flash on the development kit, follow these steps:

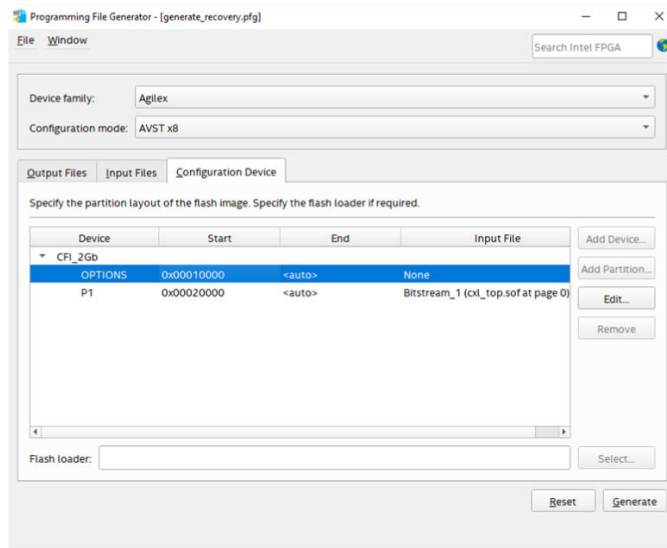
1. Open the Quartus Prime Pro Edition software and click on **File > Programming File Generator** to launch the **Programming File Generator** too.
2. In the **Device family** list, select **Agilex 7**, and in the **Configuration mode** list, select **AVST x8** to specify the device and configuration mode.
3. In the **Output directory** tab, click **Browse** to specify the output directory for .pof file.
4. In the **Description** column, select the **Programmer Object File (.pof)** and **Memory Map File (.map)** options.



5. Click on the **Input Files > Add Bitstream** tab to specify a .sof that contains the configuration bitstream.



6. Click on the **Configuration Device > Add Device** to specify the flash device. In the **Device** list of the pop-up window, select **CFI_2Gb** for the configuration flash device.
7. Click on the **OPTIONS** row, and then click on the **Edit** option to modify the start address. In the **Address Mode** list of the pop-up window, select **Start**. In the **Start address** list, input **0x00010000**.
8. Click on the **CFI_2Gb** row, and then click the **Add Partition** option. In the **Input file** list of pop-up window, select **Bitstream (input_sof_file.sof)**. In the **Address Mode** list of pop-up window, select **Start**. In the **Start address** list, input **0x00020000**.

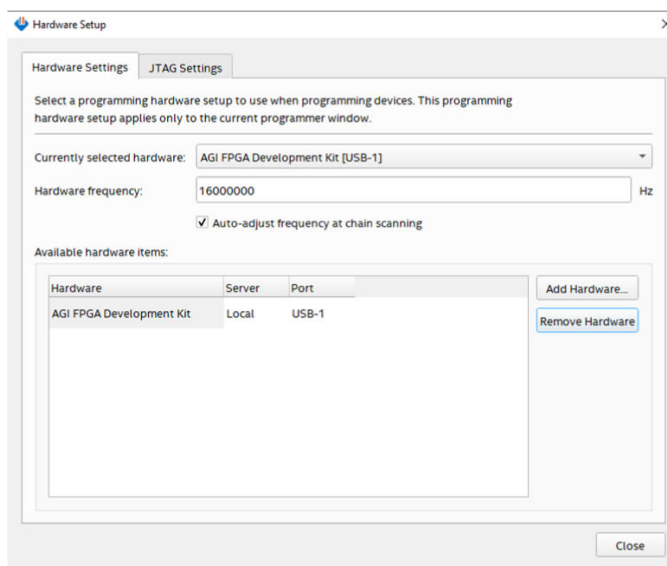


9. Click **Generate** to generate the .pof file.

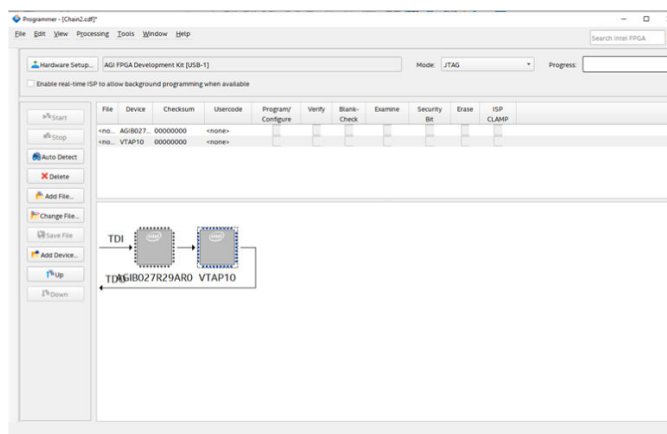
3.4. How to Program the Generated POF Image

To program the generated POF image, follow these steps:

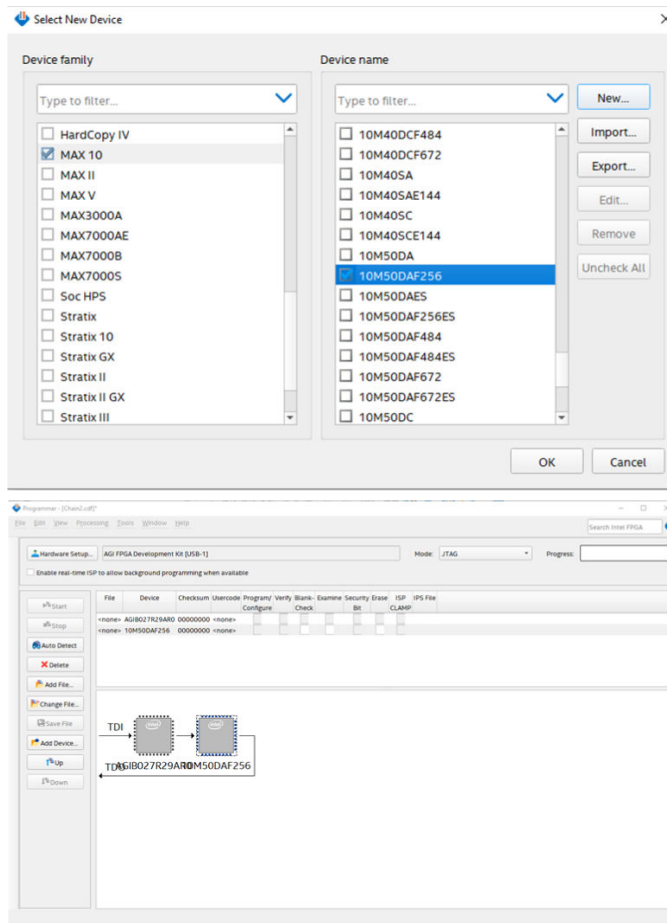
1. Plug in the USB cable to the USB port **J8** (when using J10, DIPSWITCH SW5.3 (DK-DEV-AGI027RES and DK-DEV-AGI027R1BES) and SW8.3 (DK-DEV-AGI027RB and DK-DEV-AGI027-RA) should be off).
2. Set the DIPSWITCH SW2 to [on:off:off:X] (the 4th bit is don't care).
3. Power on the board.
4. Open the Quartus Prime Pro Edition software and click on **Tools > Programmer** to launch the **Programmer** tool.
5. In the **Hardware Setup** page, select **AGI FPGA Development Kit**, and in the **Hardware frequency** column, input **16000000 Hz**.



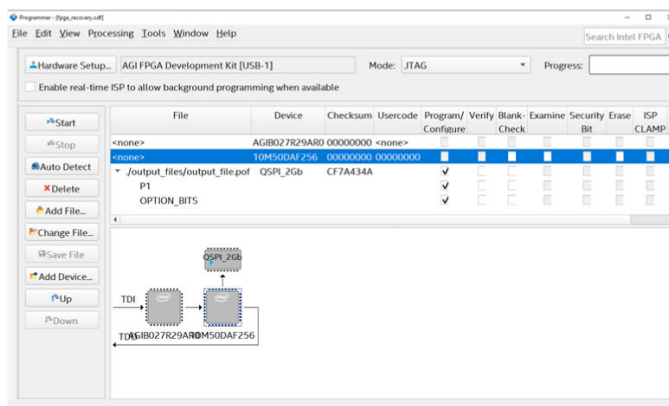
6. In the **Programmer** page, click **Auto Detect** to scan the JTAG devices.



7. Right click the **VTAP10** device, **Edit > Change Device**, change it to **MAX 10 > 10M50DAF256**.



8. Right click the **10M50DAF256** device, **Edit > Attach Flash Device**, select **Quad SPI Flash Memory QSPI_2Gb**.
9. In the **Programmer** page, click **QSPI_2Gb > Change File** to select the **.pof** file.



10. Start the **Programmer**.

3.5. The Required SmartVID QSF Assignments to Compile a Design

If you are creating your own design and want to generate a programming SRAM object file (.sof), you must add the correct SmartVID setting into the Quartus Prime project for the Agilex 7 FPGA development kit to configure successfully. Before you add the following SmartVID setting into the Quartus settings file (.qsf), you must change the configuration scheme to Avalon® streaming interface x8 (AVST x8) for your project. You can also extract the SmartVID setting from the Golden Top file.

Figure 10. Selecting the Configuration Scheme

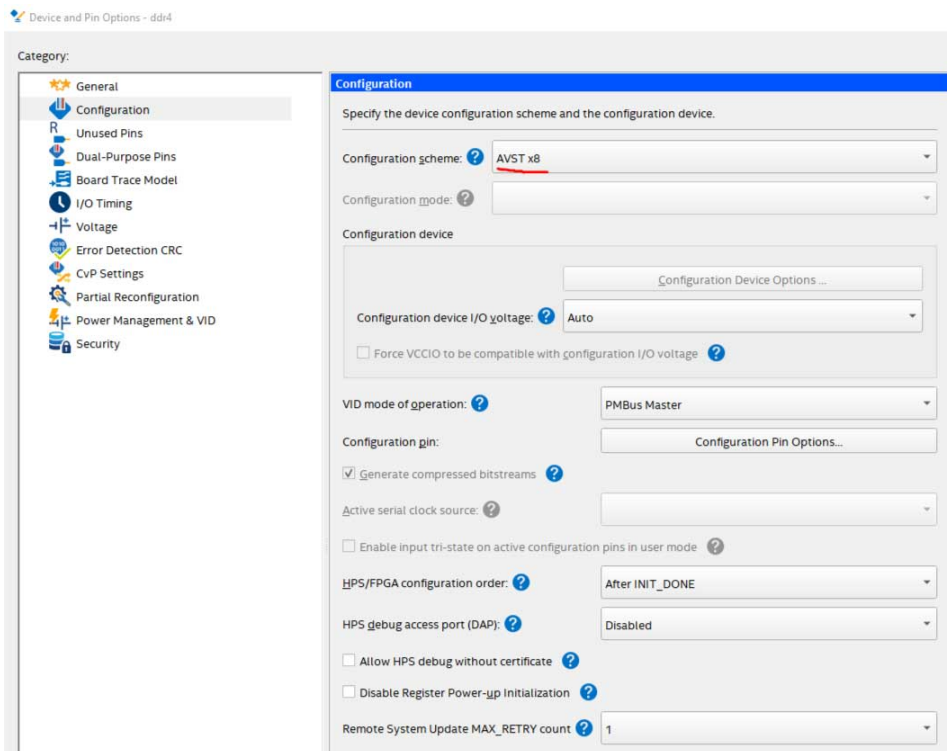


Figure 11. Power Management & VID Settings

This applies to DK-DEV-AGI027RES and DK-DEV-AGI027R1BES.

Device and Pin Options - ddi4

Category:

- General
- Configuration
- Unused Pins
- Dual-Purpose Pins
- Board Trace Model
- I/O Timing
- Voltage
- Error Detection CRC
- CvP Settings
- Partial Reconfiguration
- Power Management & VID**
- Security

Power Management & VID

Specify power management and VID settings.

Name	Value
Bus speed mode ?	100 KHz
Slave device type ?	ED8401
Device address in PMBus Slave mode ?	00
PMBus device 0 slave address ?	47
PMBus device 1 slave address ?	00
PMBus device 2 slave address ?	00
PMBus device 3 slave address ?	00
PMBus device 4 slave address ?	00
PMBus device 5 slave address ?	00
PMBus device 6 slave address ?	00
PMBus device 7 slave address ?	00
Voltage output format ?	Linear format
Direct format coefficient m ?	0
Direct format coefficient b ?	0
Direct format coefficient R ?	0
Linear format N ?	-13
Translated voltage value unit ?	Volts

```
set_global_assignment -name VID_OPERATION_MODE "PMBUS MASTER"
set_global_assignment -name USE_PWRMGT_SCL SDM_IO0
set_global_assignment -name USE_PWRMGT_SDA SDM_IO12
set_global_assignment -name USE_CONF_DONE SDM_IO16
set_global_assignment -name PWRMGT_BUS_SPEED_MODE "100 KHZ"
set_global_assignment -name PWRMGT_SLAVE_DEVICE_TYPE ED8401
set_global_assignment -name PWRMGT_SLAVE_DEVICE0_ADDRESS 47
set_global_assignment -name PWRMGT_SLAVE_DEVICE1_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE2_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE3_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE4_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE5_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE6_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE7_ADDRESS 00
set_global_assignment -name PWRMGT_TRANSLATED_VOLTAGE_VALUE_UNIT VOLTS
set_global_assignment -name PWRMGT_PAGE_COMMAND_ENABLE OFF
```


Figure 12. Power Management & VID Settings

This diagram applies to DK-DEV-AGI027RBES and DK-DEV-AGI027-RA.

Category:

- General
- Configuration
- Unused Pins
- Dual-Purpose Pins
- Board Trace Model
- I/O Timing
- Voltage
- Error Detection CRC
- CvP Settings
- Partial Reconfiguration
- Power Management & VID**
- Security

Power Management & VID

Specify power management and VID settings.

Name	Value
Bus speed mode	100 KHz
Slave device type	Other
Device address in PMBus Slave mode	00
Number of slave devices	1
PMBus device 0 slave address	47
PMBus device 1 slave address	00
PMBus device 2 slave address	00
PMBus device 3 slave address	00
PMBus device 4 slave address	00
PMBus device 5 slave address	00
PMBus device 6 slave address	00
PMBus device 7 slave address	00
Voltage output format	Linear format
Direct format coefficient m	0
Direct format coefficient b	0
Direct format coefficient R	0
Linear format N	-12
Translated voltage value unit	Volts

```

set_global_assignment -name VID_OPERATION_MODE "PMBUS MASTER"
set_global_assignment -name USE_PWRMGT_SCL SDM_IO0
set_global_assignment -name USE_PWRMGT_SDA SDM_IO12
set_global_assignment -name USE_CONF_DONE SDM_IO16
set_global_assignment -name PWRMGT_BUS_SPEED_MODE "100 KHZ"
set_global_assignment -name PWRMGT_SLAVE_DEVICE_TYPE OTHER
set_global_assignment -name PWRMGT_SLAVE_DEVICE0_ADDRESS 47
set_global_assignment -name PWRMGT_SLAVE_DEVICE1_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE2_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE3_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE4_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE5_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE6_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE7_ADDRESS 00
set_global_assignment -name PWRMGT_TRANSLATED_VOLTAGE_VALUE_UNIT VOLTS
set_global_assignment -name PWRMGT_PAGE_COMMAND_ENABLE OFF

```

4. Board Test System

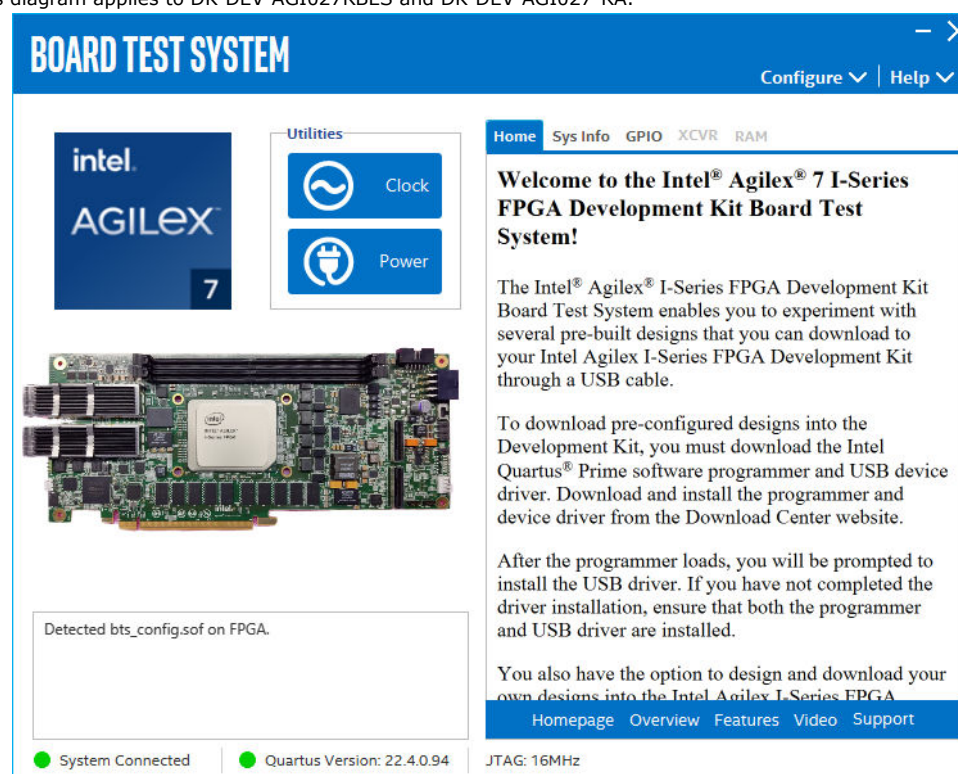
The Agilex 7 FPGA I-Series Development Kit includes design examples and the board test system (BTS) GUI to test the functionality of this board. The BTS provides an easy-to-use interface to alter functional settings and observe results. You can use the BTS to test board components, modify functional parameters, observe performance, and measure power usage.

While using the BTS, you reconfigure the FPGA several times with test designs specific to the functionality that you are testing. The BTS is also useful as a reference for designing systems. The BTS communicates over the JTAG bus to a test design running in the Agilex 7 FPGA I-Series device.

The figures below show the graphical user interface (GUI) of a board that is in factory configuration.

Figure 13. BTS GUI (Power Solution 2)

This diagram applies to DK-DEV-AGI027RBES and DK-DEV-AGI027-RA.



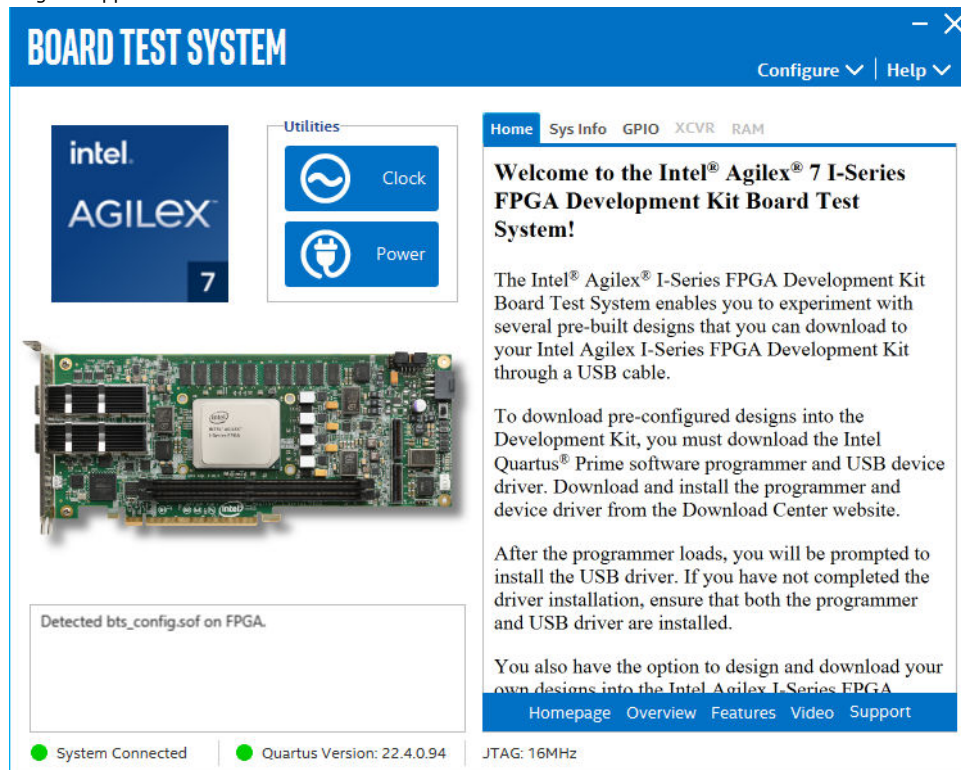
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Registered

Figure 14. BTS GUI (Power Solution 1)

This diagram applies to DK-DEV-AGI027RES and DK-DEV-AGI027R1BES.



4.1. Set Up BTS GUI Running Environment

To run the BTS GUI, including the Power Monitor and Clock Controller GUIs, you need to download and install Java runtime including OpenJDK and OpenJFX on your system and set up the environment. This is a one-time procedure, so if you have already completed it before, you do not need to do it again unless a Java version upgrade is needed.

4.1.1. Download OpenJDK

To download the Temurin OpenJDK, follow these steps:

1. Download the Temurin OpenJDK using this link: <https://adoptium.net/releases.html>.
2. Select Architecture x64, package type JRE, and version 11.
3. On **Windows** systems, choose the JRE zip format file.
4. On **Linux** systems, choose the JRE tar.gz format file.

Note: The JDK version can be updated, by downloading the latest version.

4.1.2. Download OpenJFX

To download the OpenJFX, follow these steps:

1. Download the OpenJFX using this link: <https://gluonhq.com/products/javafx/>.
2. Select the JavaFX version 17.0.2.
3. For **Windows** systems, download the JavaFX Windows x64 SDK.
4. For **Linux** systems, download the JavaFX Linux x64 SDK.

4.1.3. Install OpenJDK and OpenJFX

You have two downloaded compressed files. Follow these steps to install them.

1. On **Windows** systems, Altera recommend that you to unzip the files and put them in the following directories:

- C:\Program Files\Java\jre
- C:\Program Files\Java\jfx

Note: The unzipped folder name of JRE is jdk-11.0.xx+x-jre (for example jdk-11.0.15+10-jre), and you must rename it to jre. The unzipped folder name of JFX is javafx-sdk-17.0.2, and you must rename it to jfx.

2. On **Linux** systems, Altera recommend that you to unzip the files and rename the folders using the following commands:

```
# unzip openjfx-17.0.2_linux-x64_bin-sdk.zip -d /opt/Java/
# tar zxvf OpenJDK11U-jre_x64_linux_hotspot_11.0.15_10.tar.gz -C /opt/Java/
# cd /opt/Java
# mv javafx-sdk-17.0.2 jfx
# mv jdk-11.0.15+10-jre jre
```

You have the following two directories on your **Linux** system:

- /opt/Java/jre
- /opt/Java/jfx

4.1.4. Run BTS GUI

The BTS release folder always include the following files.

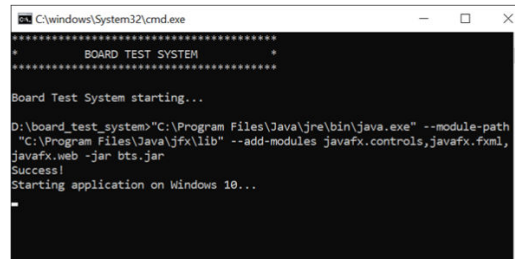
Figure 15. BTS Folder

Name	Type
image	File folder
lib	File folder
BoardTestSystem.bat	Windows Batch File
BoardTestSystem.sh	Shell Script
bts.jar	Executable Jar File
ClockController.bat	Windows Batch File
ClockController.sh	Shell Script
PowerMonitor.bat	Windows Batch File
PowerMonitor.sh	Shell Script
README.TXT	Text Document

You can run the BTS GUI easily with the following scripts.

1. On **Windows** systems, double click the .bat files to run BTS, Clock Controller, or Power Monitor GUIs.

Figure 16. Windows Console



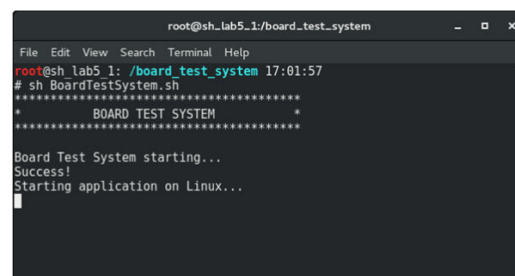
```
C:\windows\System32\cmd.exe
*****
*          BOARD TEST SYSTEM          *
*****

Board Test System starting...

D:\board_test_system>"C:\Program Files\Java\jre\bin\java.exe" --module-path
"C:\Program Files\Java\jfx\lib" --add-modules javafx.controls,javafx.fxml,
javafx.web -jar bts.jar
Success!
Starting application on Windows 10...
```

2. On **Linux** systems, you need to run the shell script with root privilege.

Figure 17. Linux Console



```
root@sh_lab5_1:/board_test_system
File Edit View Search Terminal Help
root@sh_lab5_1: /board_test_system 17:01:57
# sh BoardTestSystem.sh
*****
*          BOARD TEST SYSTEM          *
*****

Board Test System starting...
Success!
Starting application on Linux...
```

Note: The .bat or shell script checks the Java environment settings, copies necessary files, and gives some prompts if the environment is not set up correctly.

4.2. Test the Functionality of the Development Kit

This section describes each control in the BTS.

4.2.1. The Bottom Info Bar

The bottom information bar shows the status of the system connection, Quartus Prime version, and the JTAG clock speed.

- **System Connected/Disconnected:** Shows if the board is connected to the system. The green sign turns gray if the board becomes disconnected.
- **Quartus Prime Version:** Displays the current Quartus Prime version installed and active on your system. The text turns red if your version is older than the required version. Change the QUARTUS_ROOTDIR environment variable if you have installed the right version but the active version does not meet the requirement.
- **JTAG:** Displays the JTAG clock frequency.

4.2.2. The Configure Menu

Use the Configure Menu to select the design you want to use. Each design example tests different functionality that corresponds to one or more application tabs.

Figure 18. The Configure Menu (Power Solution 2)

This diagram applies to DK-DEV-AGI027RBES and DK-DEV-AGI027-RA.

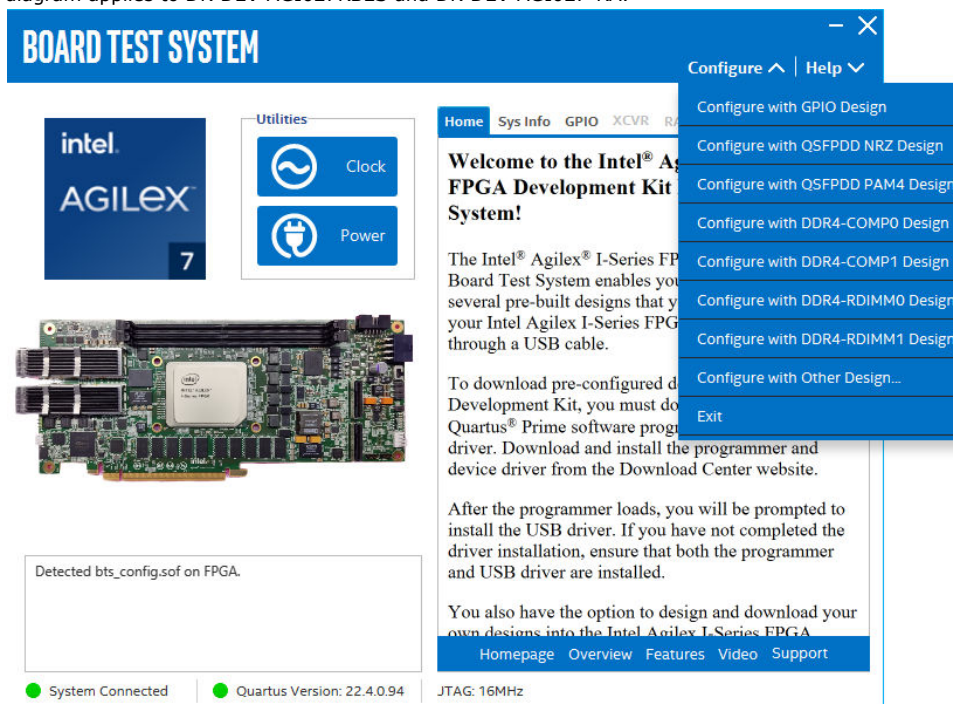
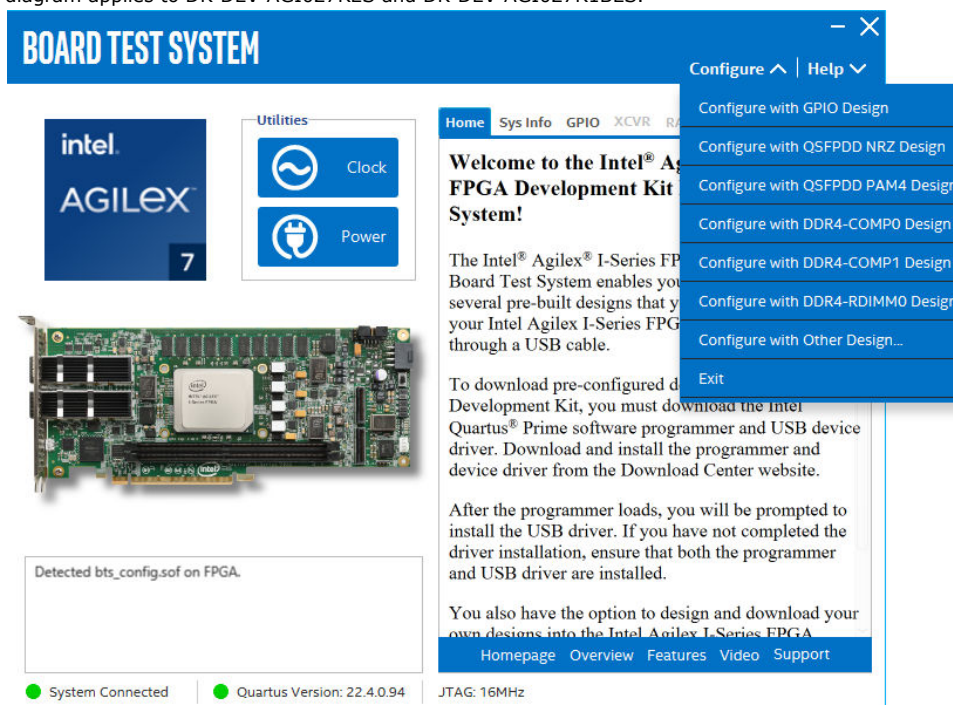


Figure 19. The Configure Menu (Power Solution 1)

This diagram applies to DK-DEV-AGI027RES and DK-DEV-AGI027R1BES.



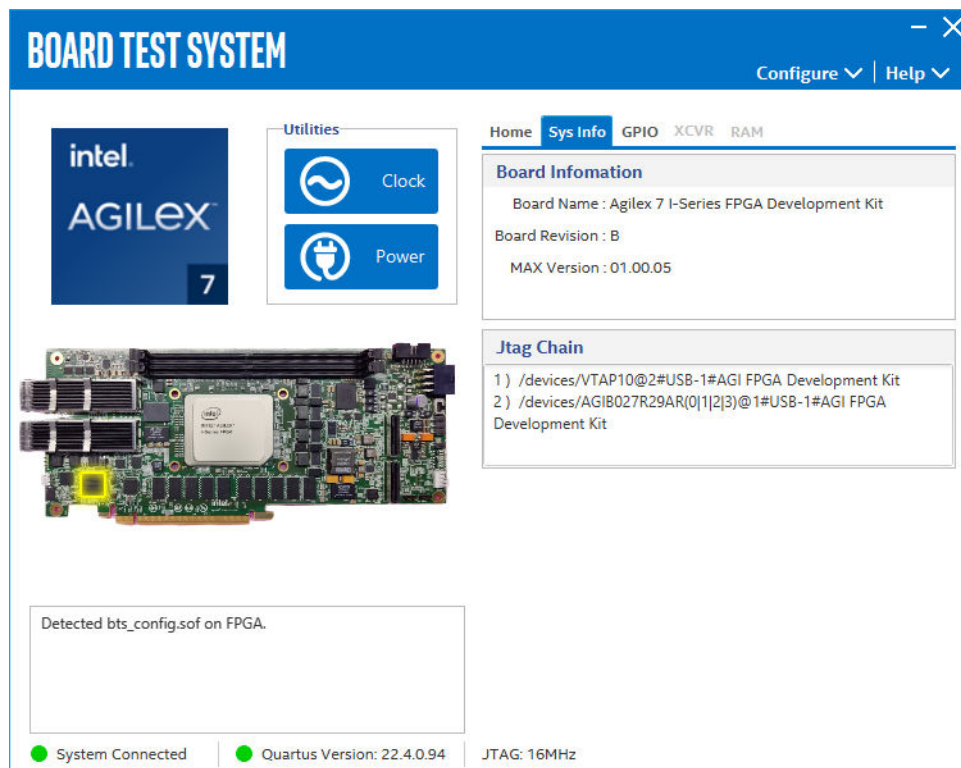
To configure the FPGA with a test system design, follow these steps:

1. On the **Configure** menu, click the **Configure** command that corresponds to the functionality you wish to test.
2. In the dialog box that appears, click **Configure** to download the corresponding design's SRAM Object File (.sof) to the FPGA. The download process usually takes less than a minute.
3. When configuration finishes, the design begins running in the FPGA. The corresponding GUI application tabs that interface with the design are now enabled. If you use the Quartus Prime Programmer for configuration, instead of the BTS GUI, you might need to restart the GUI.

4.2.3. The Sys Info Tab

The **Sys Info** tab shows information about the board's current configuration. The tab displays the board information, JTAG Chain devices, and other details stored on the board.

Figure 20. The Sys Info Tab



The following sections describe the controls on the System Info tab.

Board Information

The board information control displays static information about your board.

- **Board Name:** Indicates the official name of the board given by the BTS.
- **Board Revision:** Indicates the revision of the board.
- **MAX Version:** Indicates the version of the MAX 10 FPGA image.

JTAG Chain

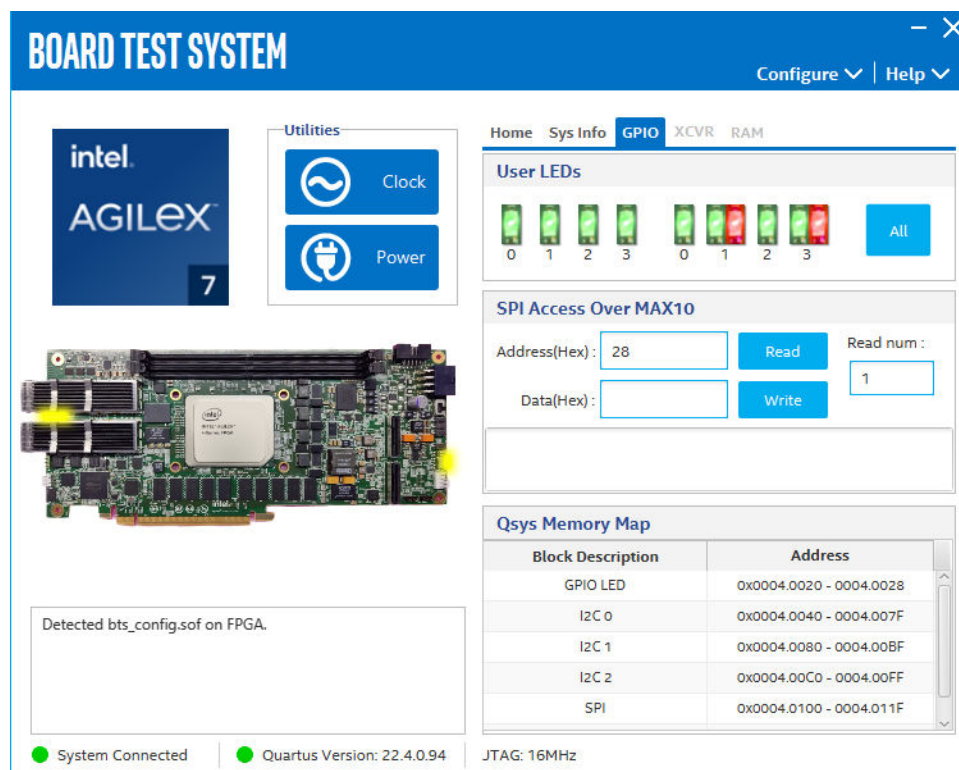
The JTAG chain control shows all the devices currently in the JTAG chain.

Note: The system MAX 10 and Agilex 7 FPGA should all be in the JTAG chain using the BTS GUI.

4.2.4. The GPIO Tab

The **GPIO** tab allows you to interact with all the general-purpose user I/O components on your board. You can turn LEDs on or off and read or write data with SPI access.

Figure 21. The GPIO Tab



The following sections describe the controls on the GPIO tab.

User LEDs

The User LEDs control displays the current state of the user LEDs. Toggle the LED buttons to turn the board LEDs on and off.

SPI Access Over MAX10

SPI Access Over MAX10 allows you to read and write the data at the address you specify.

Qsys Memory Map

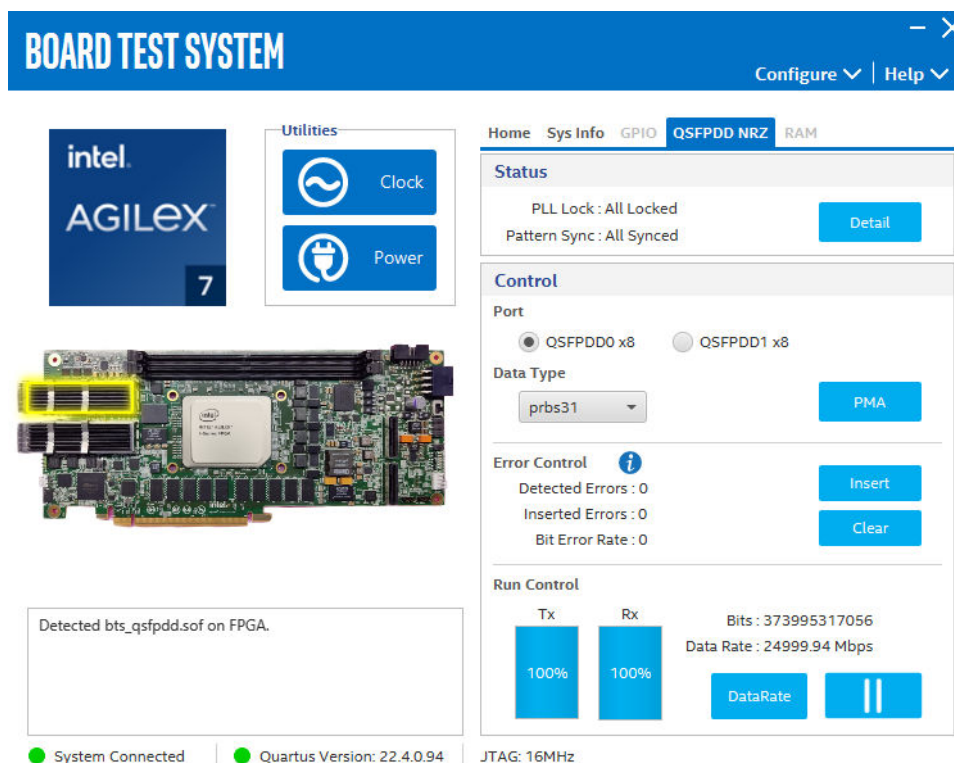
The Qsys Memory Map control shows the memory map of **bts_config.sof** design running on your board.

4.2.5. The XCVR Tab

The **XCVR** tab allows you to run transceivers tests on your board. You can run the QSFDD test using optical fiber modules.

4.2.5.1. The QSFDD NRZ Tab

Figure 22. The QSFDD NRZ Tab



The following sections describe controls in the QSFDD NRZ tab.

Status

The Status control displays the following status information during the loopback test:

- **PLL Lock:** Shows the PLL locked or unlocked state.
- **Pattern Sync:** Shows the pattern synced or not state. The pattern is considered synced when the start of the data sequence is detected.
- **Detail:** Shows the PLL lock and pattern sync status.

Control

Use the following controls to select an interface to apply PMA settings, data type, and error control:

- **QSFPDD0 x8**
- **QSFPDD1 x8**

PMA Setting

PMA allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback:** Displays the signal status between the transmitter and the receiver.
- **VOD:** Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap:**
 - Pre-tap 1: Specifies the amount of pre-emphasis on the first pre-tap of the transmitter buffer.
 - Pre-tap 2: Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
 - Post-tap 1: Specifies the amount of pre-emphasis on the post-tap of the transmitter buffer.

Figure 23. QSFPDD-PMA Setting

Serial Loopback		Pre-emphasis tap			
		VOD	Pre-tap 1	Pre-tap 2	Post-tap 1
<input type="checkbox"/> All CH	<input type="checkbox"/>	0	0	0	0
CH0	<input type="checkbox"/>	0	0	0	0
CH1	<input type="checkbox"/>	0	0	0	0
CH2	<input type="checkbox"/>	0	0	0	0
CH3	<input type="checkbox"/>	0	0	0	0
CH4	<input type="checkbox"/>	0	0	0	0
CH5	<input type="checkbox"/>	0	0	0	0
CH6	<input type="checkbox"/>	0	0	0	0
CH7	<input type="checkbox"/>	0	0	0	0

OK Cancel Apply

Data Type

The Data Type control specifies the type of data pattern contained in the transactions. Select the following available data types for analysis:

- **PRBS7**: Pseudo-random 7-bit sequences.
- **PRBS15**: Pseudo-random 15-bit sequences.
- **PRBS23**: Pseudo-random 23-bit sequences.
- **PRBS31**: Pseudo-random 31-bit sequences (default).
- **High_freq**: Selects the highest frequency divided-by-2 data pattern 10101010.
- **Low_freq**: Selects the lowest frequency divided-by-33 data pattern.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors**: Displays the number of data errors detected in the received bitstream.
- **Inserted Errors**: Displays the number of errors inserted into the transmit datastream.
- **Bit Error Rate**: Calculates the bit error rate of the transmit data stream.
- **Insert**: Insert a one-word error into the transmit data stream each time you click the button. Insert error is only enabled during transaction performance analysis.
- **Clear**: Resets the Detected Errors counter and Inserted Errors counter to zeros.

Run Control

- **TX and RX performance bars**: Show the percentage of the maximum theoretical data rate that the requested transactions are able to achieve.
- **Start**: This control initiates the loopback tests.
- **Data Rate**: Displays the XCVR type and data rate of each channel.

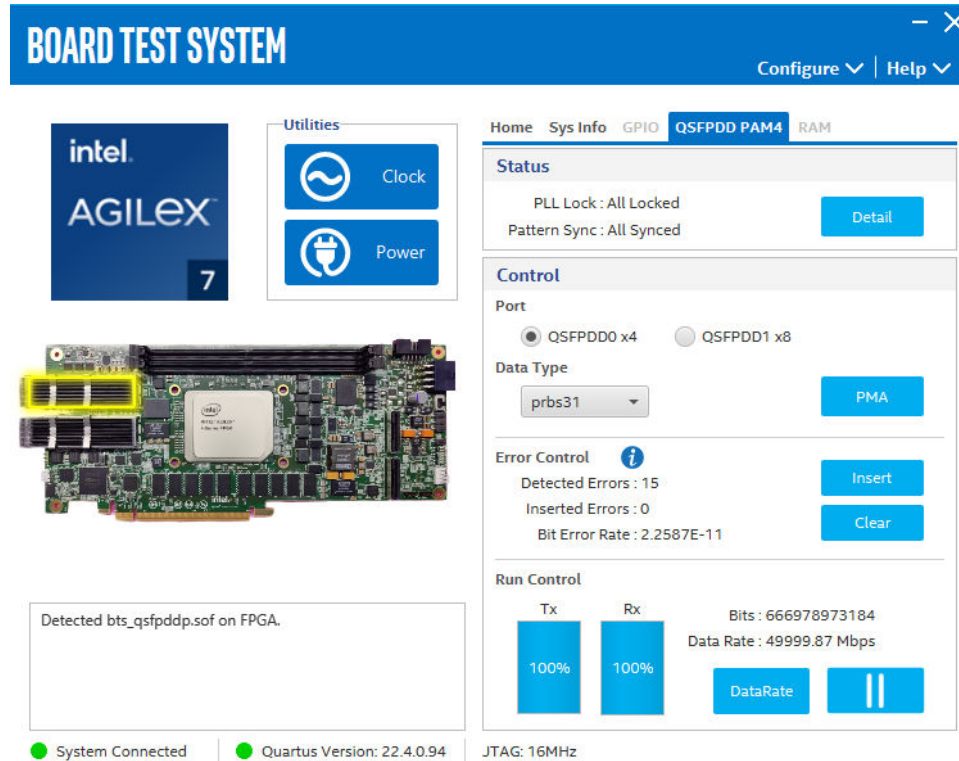
Figure 24. XCVR-Data Rate

Data Rate		
Channel	XCVR Type	Frequency
0	F-Tile FGT	24999.94 Mbps
1	F-Tile FGT	24999.94 Mbps
2	F-Tile FGT	24999.87 Mbps
3	F-Tile FGT	24999.94 Mbps
4	F-Tile FGT	24999.94 Mbps
5	F-Tile FGT	24999.94 Mbps
6	F-Tile FGT	24999.94 Mbps
7	F-Tile FGT	24999.94 Mbps

4.2.5.2. The QSFDD PAM4 Tab

Figure 25. The QSFDD PAM4 Tab

Similar control functions with the QSFDD NRZ tab.

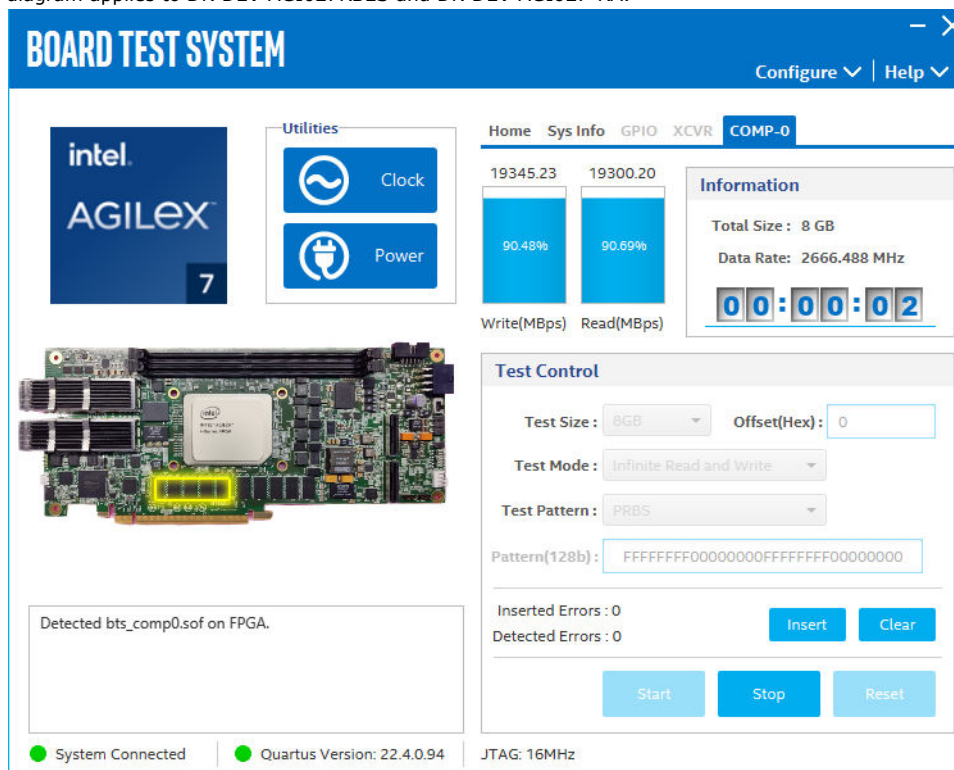


4.2.6. The RAM Tab

This tab allows you to read and write DDR4-COMP0, DDR4-COMP1, DDR4-RDIMM0, and DDR4-RDIMM1 memory on your board.

Figure 26. The COMP-O Tab

This diagram applies to DK-DEV-AGI027RBES and DK-DEV-AGI027-RA.



The following sections describe controls on this tab.

Start

Initiates DDR4 memory transaction performance analysis.

Stop

Terminates transaction performance analysis.

Performance Indicators

These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **Write and Read performance bars:** Show the percentage of the maximum theoretical data rate that the requested transactions are able to achieve.
- **Write (MBps) and Read (MBps):** Show the number of bytes analyzed per second.
- **Data Bus:** 72 bits (8 bits ECC) wide, reference clock is 33.33 MHz, and the frequency is 1333.33 MHz double data rate 2666.66 MT/s.

Test Control

- **Test Size:** You can choose the size of the memory to test. The available options are 64 KB, 256 KB, 1 MB, 4 MB, 16 MB, 64 MB, 256 MB, 1 GB, 4 GB, and 8 GB (default).
- **Offset (Hex):** You can define the memory start address to test.
- **Test Mode:** Infinite Read and Write (default), Single Read and Write.
- **Test Pattern:** PRBS (default), User Defined Constant, Walking '0', Walking '1'.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors:** Displays the number of data errors detected in the hardware.
- **Inserted Errors:** Displays the number of errors inserted into the transaction stream.
- **Insert:** Insert a one-word error into the transaction stream each time you click the button. Insert error is only enabled during transaction performance analysis.
- **Clear:** Resets the Detected Errors counter and Inserted Errors counter to zeros.

Figure 27. The COMP-1 Tab

This diagram applies to DK-DEV-AGI027RBES and DK-DEV-AGI027-RA. Same as DDR4-COMP0.

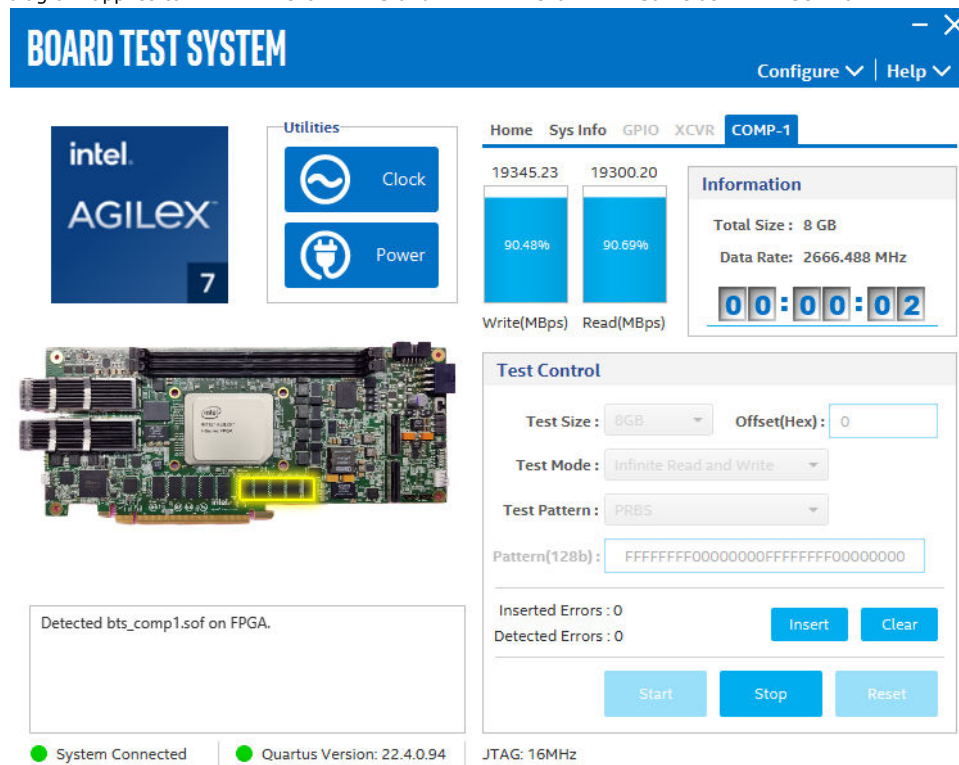


Figure 28. The RDIMM-0 Tab

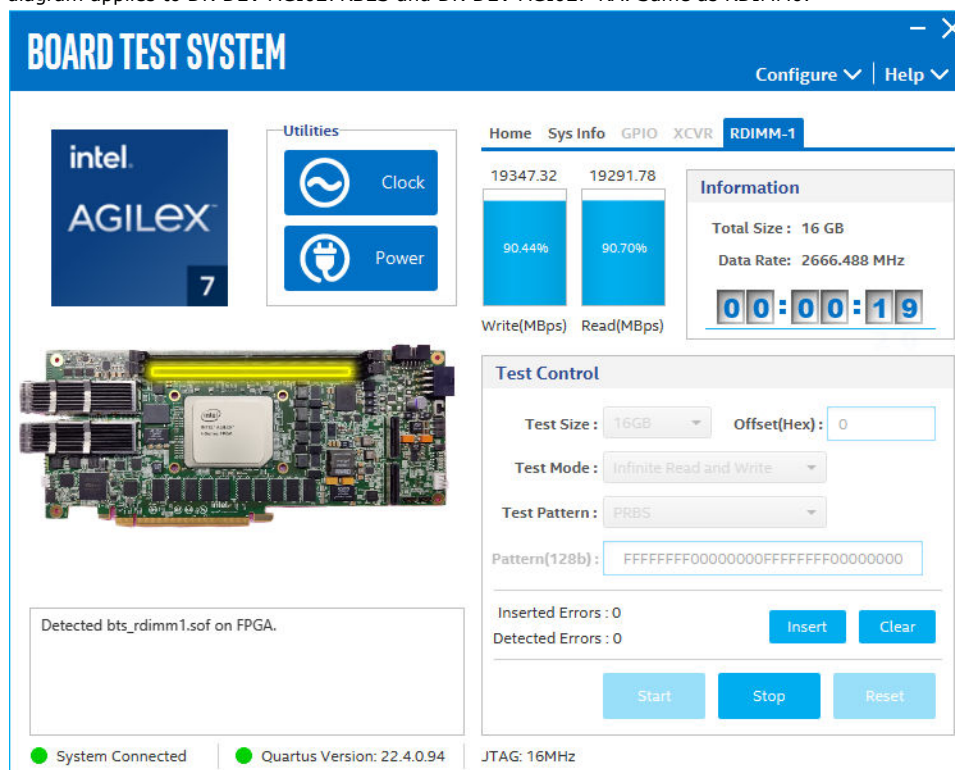
This diagram applies to DK-DEV-AGI027RBES and DK-DEV-AGI027-RA. Similar control functions to the DDR4-COMP0 tab, the total size is 16 GB.

The screenshot displays the BOARD TEST SYSTEM interface for the RDIMM-0 tab. The interface is divided into several sections:

- Header:** BOARD TEST SYSTEM with a blue background and a close button (X).
- Navigation:** Home, Sys Info, GPIO, XCVR, and RDIMM-0 (selected).
- System Information:**
 - Intel Agilex 7 logo.
 - Utilities: Clock and Power buttons.
 - Performance metrics: Write (19347.39 MBps) and Read (19291.78 MBps) speeds, both at 90.44% and 90.70% respectively.
 - Information: Total Size: 16 GB, Data Rate: 2666.488 MHz, and a digital display showing 00:00:29.
- Test Control:**
 - Test Size: 16GB (dropdown).
 - Offset(Hex): 0 (input field).
 - Test Mode: Infinite Read and Write (dropdown).
 - Test Pattern: PRBS (dropdown).
 - Pattern(128b): FFFFFFFF00000000FFFFFFFF00000000 (input field).
 - Inserted Errors: 0, Detected Errors: 0.
 - Buttons: Insert, Clear, Start, Stop, and Reset.
- Footer:**
 - Detected bts_rdim. sof on FPGA.
 - System Connected (green dot).
 - Quartus Version: 22.4.0.94 (green dot).
 - JTAG: 16MHz.

Figure 29. The RDIMM-1 Tab

This diagram applies to DK-DEV-AGI027RBES and DK-DEV-AGI027-RA. Same as RDIMM0.



4.3. Control On-board Clock through Clock Controller GUI

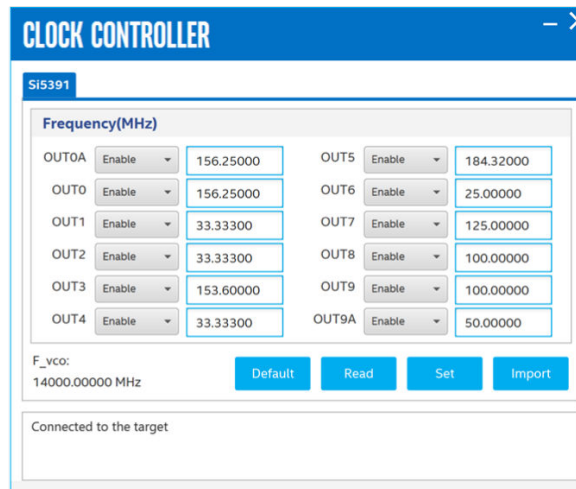
The Clock Controller GUI can change the on-board Si5391 programmable PLLs to any customized frequency between 100 Hz and 712.5 MHz.

The instructions to run the Clock Controller GUI are stated in the [Run BTS GUI](#) on page 28. It can also be started with the BTS GUI icon "Clock".

The Clock Controller communicates with the MAX 10 device through either USB port **J8** or 10-pin JTAG header **J10**. The MAX 10 controls these programmable clock parts through a 2-wire I²C bus.

Note: You cannot run the stand-alone Clock Controller GUI application when the BTS or Power Monitor GUI is running at the same time.

Figure 30. Clock Controller GUI



The following sections describe the Clock Controller buttons.

Read

Reads the current frequency setting for the oscillator associated with the active tab.

Default

Sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.

Set

Sets the programmable oscillator frequency for the selected clock to the value in the OUT_x output controls for the Si5391. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Altera recommends resetting the FPGA logic after changing frequencies.

Import

You can generate the register list from the Skyworks* Clockbuilder Pro tool and import it into the Si5391 to update the settings of the RAM. Register changes are volatile after power cycling.

Related Information

[Skyworks Solution](#)

More information about the Clockbuilder Pro software.

4.4. Monitor On-board Power through Power Monitor GUI

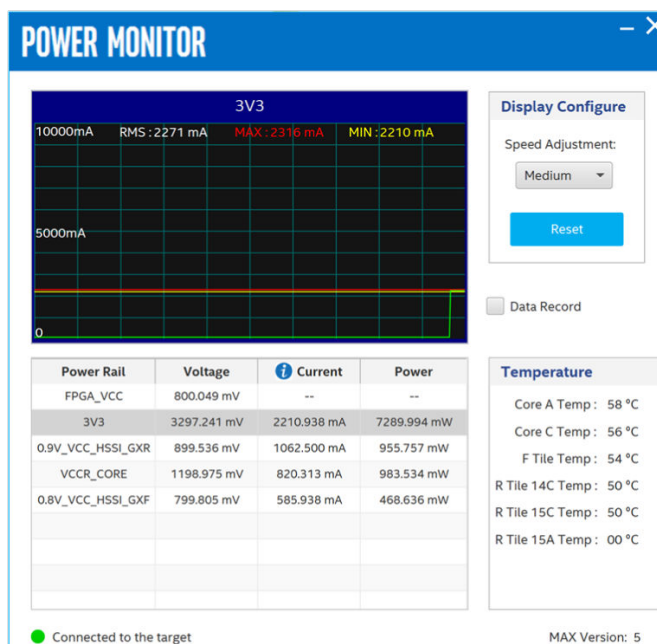
The Power Monitor GUI reports most power rails' voltage, current, and power information on the board. It also collects temperature from FPGA die, power modules, and diodes assembled on PCB.

The Power Monitor GUI communicates with System MAX 10 through either USB port **J8** or 10-pin JTAG header **J10**. The MAX 10 monitors and controls power regulators, and temperature/voltage/current sensing chips through a 2-wire I²C bus.

The instructions to run the Power Monitor GUI are stated in the [Run BTS GUI](#) on page 28. It can also be started with the BTS GUI icon “Power”.

Note: You cannot run the stand-alone Power Monitor GUI when the BTS or the Clock Controller GUI is running at the same time.

Figure 31. Power Monitor GUI



The following sections describe the details of the Power Monitor GUI.

Display Configure

- Speed Adjustment: Adjusts the update rate of the current curve.
- Reset: Regenerates the graph.

Data Record

When the box is checked, the telemetry data of the selected power rail can be recorded. The data is saved into a .csv file in the log directory.

Temperature

Core A Temp/Core C Temp/F Tile Temp/R Tile 14C Temp/R Tile 15C Temp/R Tile 15A Temp: FPGA die internal temperature sense diodes.

4.5. BTS Test Areas

BTS checks for hardware faults before you can use the board. If one or more BTS test items fail, it implies either a wrong hardware setting or hardware fault on specific interface.

4.6. Identify Test Pass or Fail-based on BTS GUI Test Status

DDR4 DIMMs

Plug the DDR4 DIMM module which is shipped with this development kit in **J1/J2**.

QSFPDD0/QSFPDD1

Plug QSFPDD0/QSFPDD1 loopback module in **J3/J4** before you configure the QSFPDD NRZ/PAM4 example build through BTS GUI.

5. Document Revision History for the Agilex 7 FPGA I-Series Development Kit User Guide

Document Version	Changes
2024.05.31	<ul style="list-style-type: none"> Updated the serial numbers for the following development kit versions in Table: <i>Agilex 7 FPGA I-Series Development Kit Ordering Information</i>: <ul style="list-style-type: none"> Agilex 7 FPGA I-Series Development Kit (Production 2x R-Tile & 1x F-Tile) Agilex 7 FPGA I-Series Development Kit (ES1 2x R-Tile & 1x F-Tile) Made editorial edits throughout the document.
2024.04.05	Added DDR4 DIMM density support information in the <i>Memory Interfaces</i> section.
2024.02.05	Removed <i>Hard Processing System</i> from the <i>Development Kits Components</i> chapter.
2024.01.09	Updated the DIMM supported frequency in the <i>Memory Interfaces</i> section.
2023.10.04	Updated the <i>Hard Processing System</i> section.
2023.04.21	<ul style="list-style-type: none"> Added Ordering Codes and Device Part Numbers for development kits. Added Figure: <i>Agilex 7 FPGA I-Series Development Kit board diagram</i> for DK-DEV-AGI027RBES and DK-DEV-AGI027-RA. Added Table: <i>Factory Default Switch Settings for DK-DEV-AGI027RBES and DK-DEV-AGI027-RA</i> and in <i>Default Switch Settings</i> section. Updated Figure: <i>SW4[1:4] Switch Setting</i>. Added Figure: <i>SW8[1:4] Switch Setting</i>. Added <i>Power Management and VID Settings for DK-DEV-AGI027RBES and DK-DEV-AGI027-RA</i> in <i>The Required SmartVID QSF Assignments to Compile a Design</i>. Updated Figure: <i>BTS GUI</i>. Updated the <i>Download Open JDK</i> and <i>Download OpenJFX</i> sections. Updated Figure: <i>The Configure Menu</i>. Updated Figure: <i>The Sys Info Tab</i>. Updated Figure: <i>The GPIO Tab</i>. Updated Figure: <i>The QSPDD NRZ Tab</i>. Updated Figure: <i>The QSPDD PAM4 Tab</i>. Updated Figure: <i>The COMP-0 Tab</i>. Updated Figure: <i>The COMP-1 Tab</i>. Updated Figure: <i>The RDIMM-1 Tab</i>. Updated note in <i>The Sys Info Tab</i> to change the settings of SW8. Added the <i>DDR4-RDIMM0</i> and <i>DDR4-RDIMM1</i> tabs in <i>The RAM Tab</i>. Removed <i>Bit Error Rate</i> from the <i>Error Control</i> list. Updated the description for <i>Import</i> section of Clock Controller button. Updated the description for <i>DDR4 DIMMs</i> and <i>QSPDD0/QSPDD1</i> in <i>Identify Test Pass or Fail-based on BTS GUI Test Status</i> section. Updated Figure: <i>Intel Agilex 7 FPGA I-Series Development Board Image—Front</i> for DK-DEV-AGI027RES and DK-DEV-AGI027R1BES, and DK-DEV-AGI027RBES and DK-DEV-AGI027-RA. Updated Figure: <i>Intel Agilex 7 FPGA I-Series Development Board Image—Back</i> for DK-DEV-AGI027RES and DK-DEV-AGI027R1BES, and DK-DEV-AGI027RBES and DK-DEV-AGI027-RA. Updated Figure: <i>MCIO Connector Circuit</i>. Updated Figure: <i>F-Tile Bank 12A Circuit</i>. Updated Figure: <i>Port Controller Circuit</i>.

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*Other names and brands may be claimed as the property of others.

Document Version	Changes
	<ul style="list-style-type: none"> Added the memory information for DK-DEV-AGI027RBES and DK-DEV-AGI027-RA in <i>Memory Interfaces</i>. Updated Table: <i>I2C Device Address</i> and Figure: <i>I2C Chain</i>. Updated Figure: <i>Clock Connection Diagram</i>. Updated Figures: <i>Powering Board Using Standard PCIe-Compliant System</i> and <i>Powering Board Using Included Power Supply</i> in <i>Power Guidelines</i>. Updated Figure: <i>Power Tree Diagram</i> in <i>Power Distribution System</i>. Added the description for DK-DEV-AGI027RBES and DK-DEV-AGI027-RA in <i>Power Measurement</i> section. Updated Figure: <i>Board Temperature Measurement Circuit</i>. Updated Figure: <i>Air-Cooled Heatsink Assembly</i>. Added the <i>Hard Processing System</i> section. Updated product family name to "Intel Agilex® 7". Updated development kit name to Intel Agilex 7 FPGA I-Series Development Kit. Retitled the document from <i>Intel Agilex I-Series FPGA Development Kit User Guide</i> to <i>Intel Agilex® 7 FPGA I-Series Development Kit User Guide</i>.
2023.02.27	Updated the supported DDR4 speed for memory interfaces in the <i>Feature Summary</i> section.
2022.09.22	<ul style="list-style-type: none"> Added the <i>Additional Information</i> section. Added <i>The XCVR Tab</i> section. Added <i>The QSFPDD PAM4 Tab</i> section. Added Figure: <i>The QSFPDD PAM4 Tab</i>. Updated the <i>Overview</i> section. Updated the <i>Block Diagram</i> section to include details about the CXL IP license. Updated the <i>About Quartus Prime Software</i> section. Updated the section title from <i>Perform Board Restore through Board Test System (BTS) GUI to Perform Board Restore through Quartus Prime Programmer</i>. Updated the <i>Download OpenJDK</i> section. Updated the <i>Download OpenJFX</i> section. Updated the <i>Install OpenJDK and OpenJFX</i> section. Updated <i>The Sys Info Tab</i> section. Updated <i>The QSFPDD NRZ Tab</i> section. Updated the <i>Intel Agilex I-Series FPGA</i> section. Updated the <i>PCIe and CXL Interfaces</i> section. Updated step 8 in the <i>How to Generate a POF Image to Program the Flash</i> section. Updated the description of J6 and J7 in Table: <i>Connectors on the Development Kit</i>. Updated the description of S2 and S3 in Table: <i>Push-Buttons on the Development Kit</i>. Updated Figure: <i>BTS GUI</i>. Updated Figure: <i>OpenJDK Version</i>. Updated Figure: <i>JavaFX Version</i>. Updated Figure: <i>BTS Folder</i>. Updated Figure: <i>Windows Console</i>. Updated Figure: <i>Linux Console</i>. Updated Figure: <i>The Configure Menu</i>. Updated Figure: <i>The Sys Info Tab</i>. Updated Figure: <i>The QSFPDD NRZ Tab</i>. Updated Figure: <i>QSFPDD-PMA Setting</i>. Updated Figure: <i>XCVR-Data Rate</i>. Updated Figure: <i>The COMP-O Tab</i>. Updated Figure: <i>The COMP-1 Tab</i>. Updated Figure: <i>The DDR4-RDIMM Tab</i>. Updated Figure: <i>Clock Controller GUI</i>. Updated Figure: <i>Power Monitor GUI</i>.

continued...

Document Version	Changes
	<ul style="list-style-type: none"> Removed Figure: <i>Windows OpenJDK Version</i>. Removed Figure: <i>Linux OpenJDK Version</i>. Removed support for Intel Optane™.
2022.03.30	Updated the <i>MCIO Cable Assembly Information</i> section.
2022.02.11	<ul style="list-style-type: none"> Added the <i>Board Test System</i> section. Added the <i>How to Generate a POF Image to Program the Flash</i> section. Added the <i>How to Program the Generated POF Image</i> section. Added <i>The Required SmartVID QSF Assignments to Compile a Design</i> section. Added Figure: <i>SW1[1:4] Switch Setting</i>. Added Figure: <i>SW2[1:4] Switch Setting</i>. Added Figure: <i>SW3[1:4] Switch Setting</i>. Added Figure: <i>SW4 Switch Setting</i>. Added Figure: <i>SW5[1:4] Switch Setting</i>. Updated the <i>PCIe and CXL Interfaces</i> section. Updated Figure: <i>Intel Agilex I-Series FPGA Development Board Image—Front</i>. Updated the header of Table: <i>Intel Agilex I-Series FPGA Development Kit Ordering Information</i>. Updated Table: <i>Factory Default Switch Settings</i>. Removed the <i>Factory Reset</i> section. Minor editorial updates.
2021.11.17	Updated the PCIe REFCLK Select function in the SW3[1:4] switch row in Table: <i>Factory Default Switch Settings</i> .
2021.09.24	Initial release.

A. Development Kits Components

This chapter introduces all the major components on the development board. A complete set of schematics, a physical layout database, and GERBER files for the development board reside in the development kit documents directory.

A.1. Board Overview

Images of the Agilex 7 FPGA I-Series development board are shown below.

Figure 32. Agilex 7 FPGA I-Series Development Board Image—Front

For DK-DEV-AGI027RES and DK-DEV-AGI027R1BES.

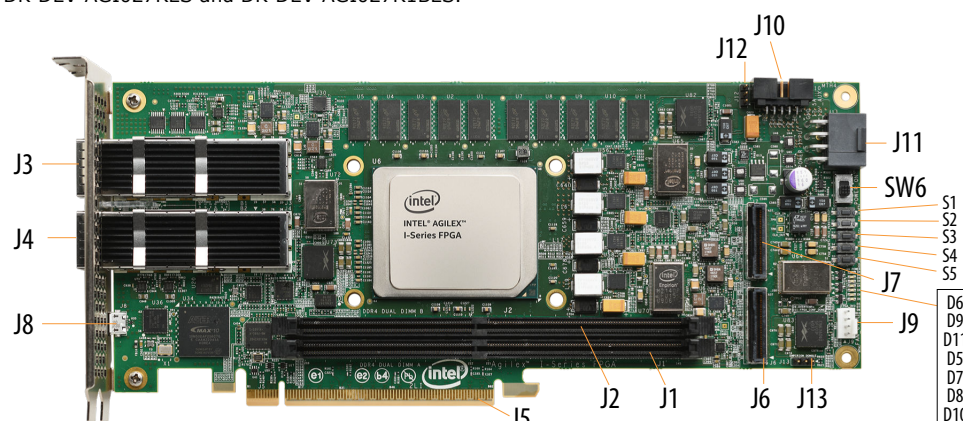
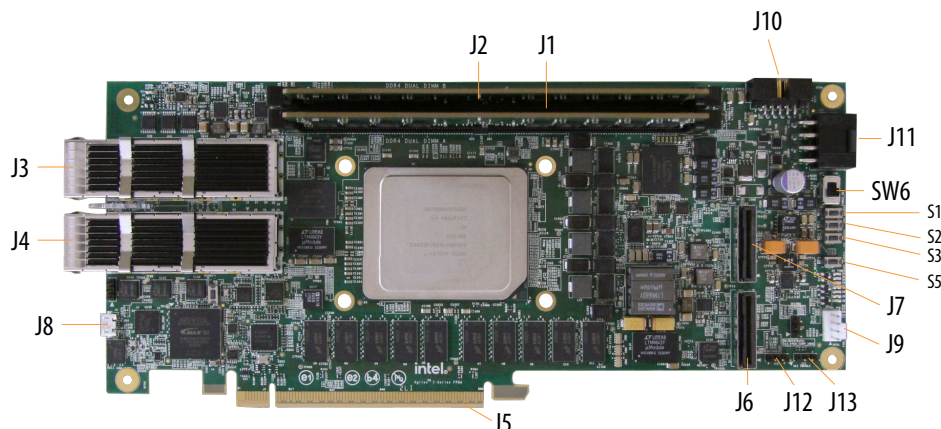


Figure 33. Agilex 7 FPGA I-Series Development Board Image—Front

For DK-DEV-AGI027RBES and DK-DEV-AGI027-RA.



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Figure 34. Agilex 7 FPGA I-Series Development Board Image—Back

For DK-DEV-AGI027RES and DK-DEV-AGI027R1BES

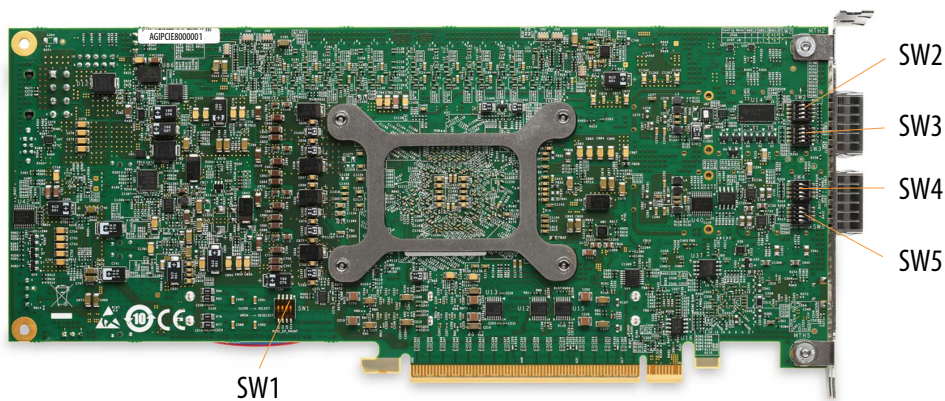
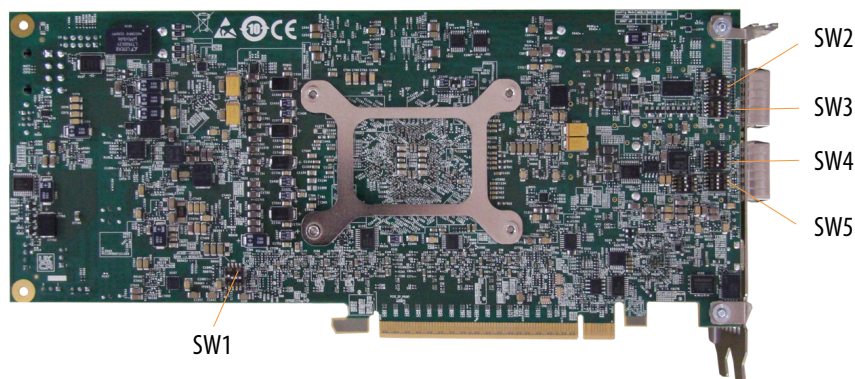


Figure 35. Agilex 7 FPGA I-Series Development Board Image—Back

For DK-DEV-AGI027RBES and DK-DEV-AGI027-RA.



A.2. Agilex 7 FPGA I-Series

Agilex 7 FPGA I-Series 56 mm x 45 mm package:

- Part Number: AGIB027R29A1E2VR0, AGIB027R29A1E2VR3, or AGIB027R29A1E1VB
- 2957-Ball FBGA Package
- 2.7M LEs
- 8528 digital signal processing (DSP) blocks
- 17056 18x19 Multipliers
- LVDS pairs supporting 1.6 Gbps
- 3x R-tile supporting PCIe Gen5 x16 (32Gb/s) or CXL⁽²⁾ x16
- 1x F tile transceiver supporting 56Gbps NRZ
- Multiple channels to connect to external DDR4 memories

A.3. PCIe and CXL Interfaces

The Agilex 7 FPGA I-Series Development Kit supports two PCIe/CXL Gen5 x16 interfaces using two out of the FPGA's three R-tiles, refer to [Board Diagram](#).

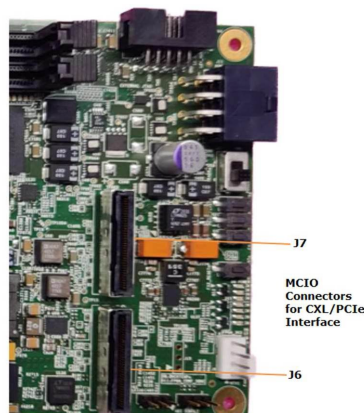
1. One R-tile (14C) supports PCIe/CXL x16 connecting to the development kit's PCIe edge connector. This interface supports x1, x4, x8, and x16 PCIe Endpoint or CXL Endpoint.
2. One R-tile (15C) connects to two 74-pin MCIO connectors that can be used as a CXL or PCIe x16 interface in the Endpoint or Root Port mode. The MCIO connectors also carry SMBus/I2C, clock, and GPIO signals.

Note: To activate the CXL hard IP and receive CXL soft R-Tile Wrapper and Soft Support logic, purchase or activation of a separate CXL IP license is required for proper use with the Quartus Prime Design Software. Contact your local Intel sales representative for pricing details. To activate a free-of-charge 30- or 60-days trial IP license, please contact your local Intel sales representative.

A.4. MCIO Connector

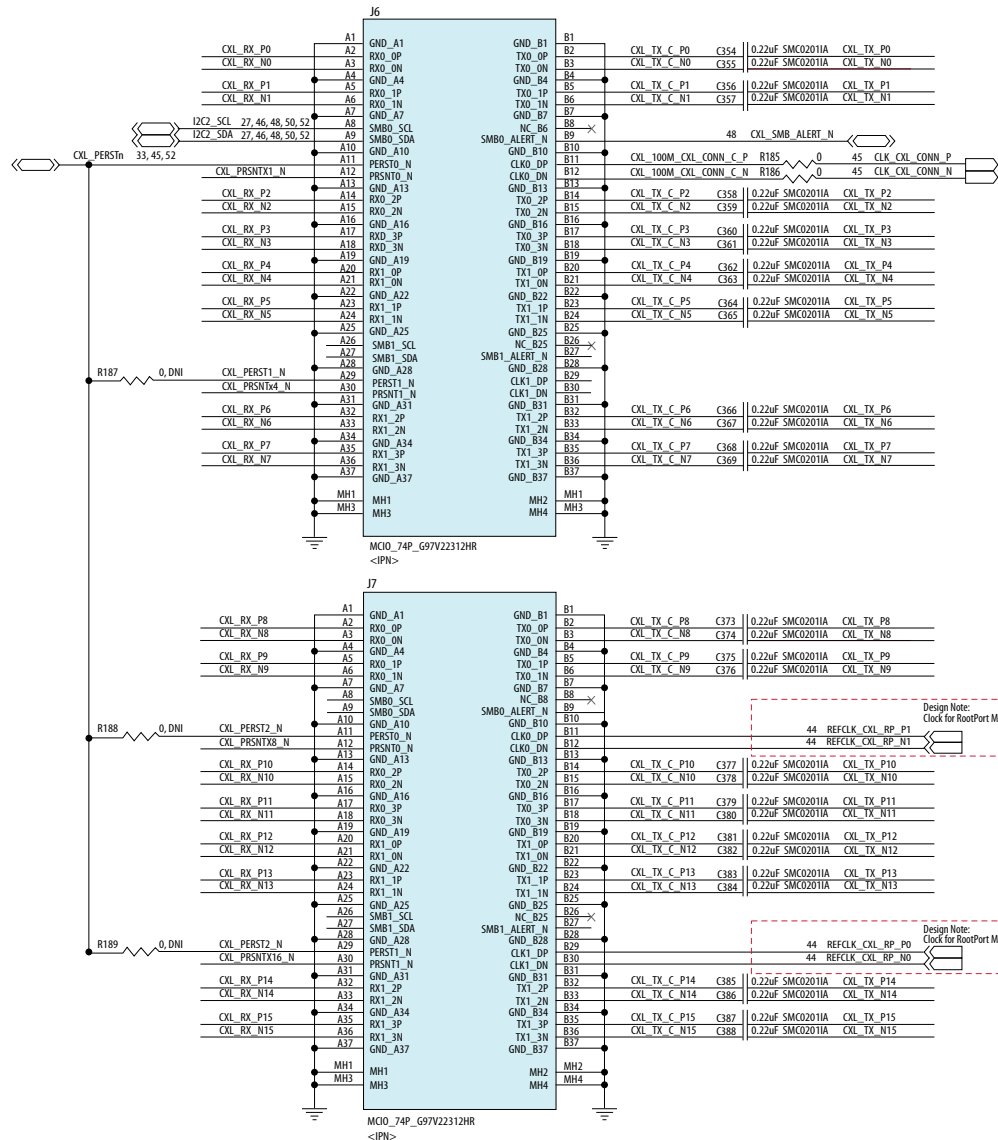
The CXL or PCIe interface is connected to two 74-pin MCIO connectors for 16 channels of transmit and receive signals of the R-tile (15C). Cables are used to connect this CXL or PCIe link from the development kit to the host board or application-specific daughter cards.

Figure 36. MCIO Connector



-
- (2) To activate the CXL hard IP and receive CXL soft R-Tile Wrapper and Soft Support logic, purchase or activation of a separate CXL IP license is required for proper use with the Quartus Prime Design Software. Contact your local Intel sales representative for pricing details. To activate a free-of-charge 30- or 60-days trial IP license, please contact your local Intel sales representative.

Figure 37. MCIO Connector Circuit



A.5. MCIO Cable Assembly Information

The cable is not provided with the development kit. For more information, contact Intel Premier Support and quote ID #14016163317.

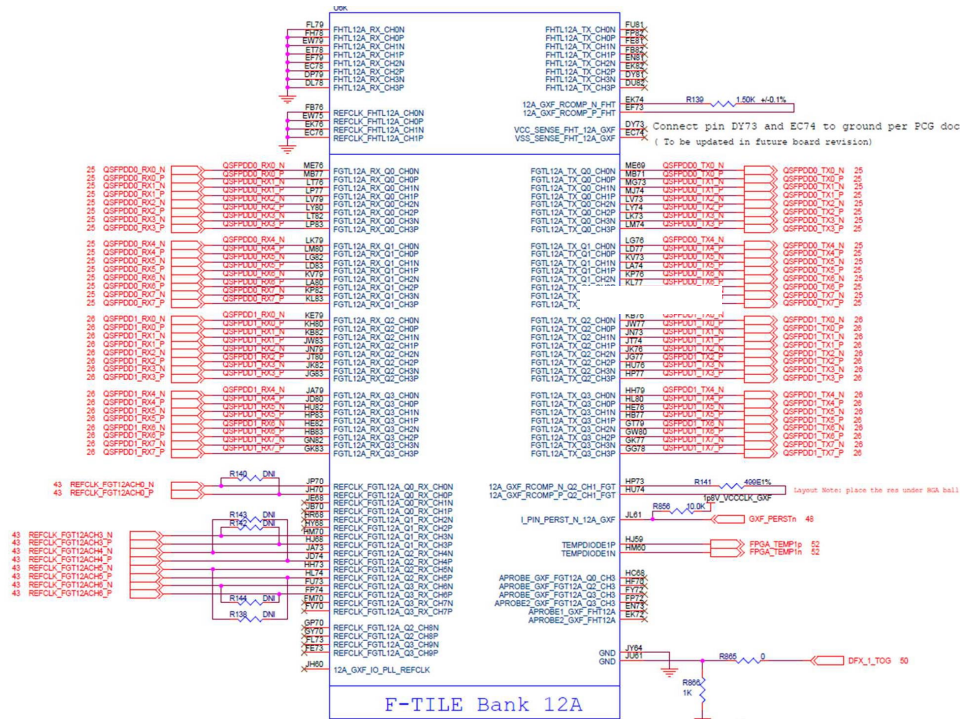
A.6. Network Interfaces

The development kit supports two QSFPDD connectors each, connecting to the Agilex 7's F-tile (12A) transceivers. Each port can operate at 4x 58G or 8x 28G. These two ports support ZQSFP56 SR optical modules as well as the 3M DAC electrical cables. A Texas Instruments FPC202 dual-port controller serves as the low-speed signal

aggregator that makes up the Dual 100Gbps Ethernet interfaces. The FPC202 aggregates all low speed and I2C signals across two ports and presents it as a single management interface to the host.

The F-tile (12A) of the FPGA provides 16 general-purpose (FGT) transceiver channels, each 8-channel group is routed to one QSFPDD. The transceiver bank requires 156.25 MHz clocks for the 28 Gbps NRZ and 325.50 MHz clocks for the 56 Gbps PAM4. These clocks must have RPM jitter <250fs.

Figure 38. F-Tile Bank 12A Circuit



[illegible]

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Programming the FPGA over Intel FPGA Download Cable II

[Supported Configuration Modes](#) shows the high-level conceptual block diagram for programming the FPGA over the embedded Intel FPGA Download Cable II or external download cable.

A.9. Supported Configuration Modes

- The development board supports two configuration modes: Avalon-ST (AVST) x8 and JTAG.
- The default configuration is AVST x8 using a 2 Gb QSPI flash device.
- JTAG configuration is supported by using either the embedded Intel FPGA Download Cable II or the Intel FPGA Download Cable II dongle.

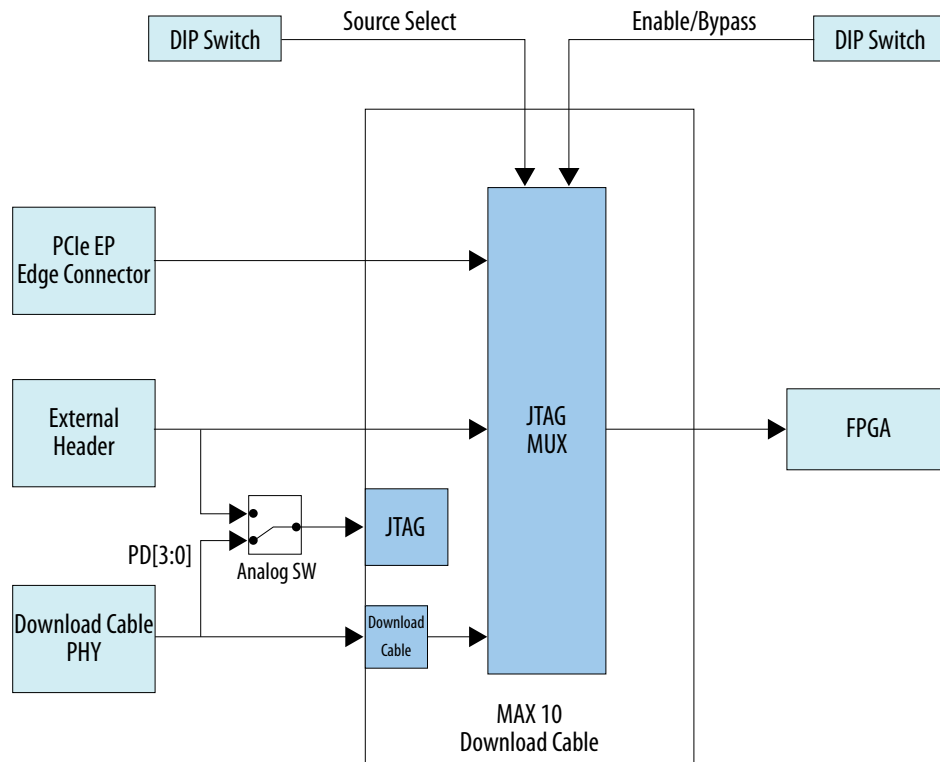
Avalon-ST (AVST) x8 Mode

The SDM block in the Agilex 7 device controls the configuration process and interface. The MAX 10 System Controller (U34) interfaces to the Agilex 7 FPGA in the AVST x8 mode. The MAX 10 also interfaces to the QSPI flash in the active serial (AS) x4 mode. For the AS x4 mode, `MSEL[2:0]` configuration pin strapping (SW2) must be set to [110]. The flash device is Micron Technology 1.8 V core, 1.8V I/O 2 Gigabit CFI NOR-type device (P/N: MT25QL02GBB8E12-0).

JTAG Configuration Mode

The JTAG switch implemented in the MAX 10 System Controller (U34) allows the selection of devices to be included in the JTAG chain. It is done by the settings of the DIP switch SW8. The embedded Intel FPGA Download Cable II (or external download cable) or PCIe JTAG can be selected as the source for programming the devices on the chain. The embedded Intel FPGA Download Cable II is the default setting for this configuration mode.

Figure 40. JTAG Block Diagram



The on-board Intel FPGA Download Cable II is implemented in a MAX 10 device. A micro-USB connector connects to a CY7C68013A USB2 PHY provides the data to MAX 10. This allows configuration of the FPGA using a USB cable directly connected to a PC running the Quartus Prime software without requiring the external download cable dongle. An external download cable dongle can also be used on J10 to configure the FPGA.

A.10. Memory Interfaces

This memory information applies to DK-DEV-AGI027RES and DK-DEV-AGI027R1BES.

Three independent memory interfaces are supported: Two independent on-board DDR4 and one dual DIMM sockets for DDR4.

- The on-board DDR4 uses five 16 Gb DDR4 single rank devices connecting to Bank 2B, 2E for memory component channel 0 and bank 2C, 2F for memory component channel 1. The total memory size of each channel is 16 GB running at 1200 MHz.
- The two 288-pin DIMM sockets interface to bank 3C, 3D for Dual DIMM memory. These sockets accept DDR4 module. These DIMM support dual rank at frequency 1333 MHz 16 GB per channel, and single rank at 1333 MHz 8 GB per channel.
 - Some board re-work is required for using DIMM sockets in 2-DPC configuration or different kinds of DDR4 modules. For more details of the resistor connections required to be present for the type of configuration used, refer to board schematic table.
- The 1.2 V DDR power supply is designed to support up to 12 A currents to the two DIMM slots. This is sufficient to support 64 GB DIMMs in both slots (128 GB in total). If higher capacity DIMM has to be supported, the DDR power supply design must be updated to use a higher rated 1.2 V voltage regulator based on the current requirement of the DIMMs.

This memory information applies to DK-DEV-AGI027RBES and DK-DEV-AGI027-RA.

- The on-board DDR4 uses five 16 Gb DDR4 single rank devices connecting to Bank 3A, 3B for memory component channel 0 and bank 3C, 3D for memory component channel 1. The total memory size of each channel is 16 GB running at 1200 MHz.
- The two 288-pin DIMM sockets interface to bank 2B, 2E for Dual DIMM memory channel 2 and bank 2F, 2C for Dual DIMM memory channel 1. These sockets accept DDR4 modules. These DIMM support dual rank at frequency 1200 MHz 16 GB per channel, and single rank at 1200 MHz 8 GB per channel.
- The 1.2 V DDR power supply is designed to support up to 12 A currents to the two DIMM slots. This is sufficient to support 64 GB DIMMs in both slots (128 GB in total). If higher capacity DIMM has to be supported, the DDR power supply design must be updated to use a higher rated 1.2 V voltage regulator based on the current requirement of the DIMMs.

A.11. I2C

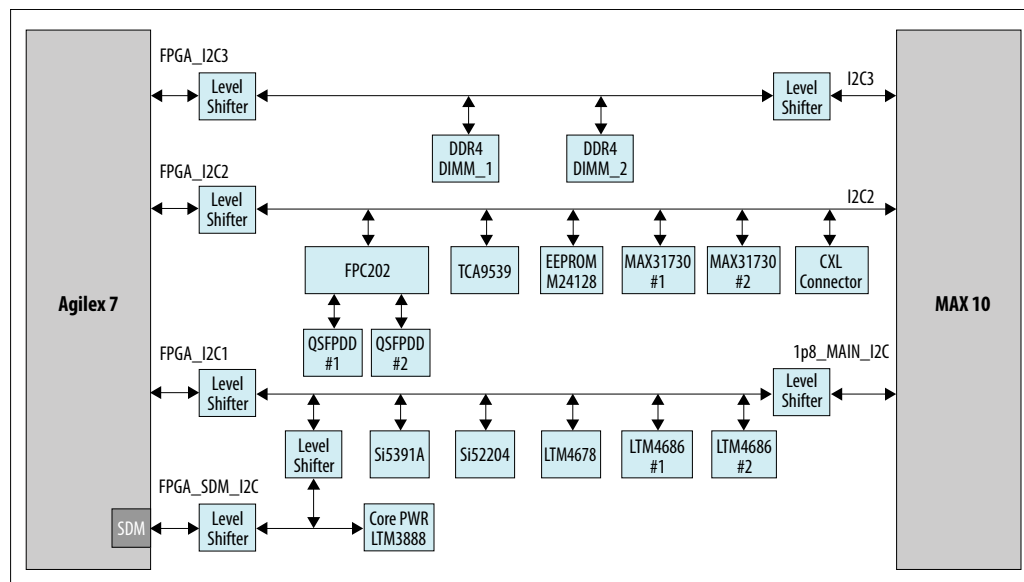
I2C supports communication between integrated circuits on a board. It is a simple two-wire bus that consists of a serial data line (SDA) and a serial clock (SCL). The MAX 10 and the Agilex 7 devices use the I2C for reading and writing to the various components on the board such as programmable clock generators, VID regulators, analog-to-digital converters (ADC), and temperature sensors.

You can use the Agilex 7 or MAX 10 as the I2C host to access these devices, change clock frequencies or get status information of the board such as voltage and temperature readings.

Table 9. I2C Device Address

Type	Bus	Address	Device
FPGA/MAX 10 I2C Address	I2C1	0x74	Si5391
		0x6A	Si52204
		0x42	LTM4678/LTM4680
		0x45	LTM4686
		0x46	LTM4686
	I2C2	0x1E	FPC202
		0x57/0x5F	M24128
		0x38	MAX31730
		0x3A	MAX31730
		0xA0	QSFPDD_0
		0xA0	QSFPDD_1
		0x74	TCA9539
	I2C3	0xA1	DDR4_DIMM
		0xA0	DDR4_DIMM2
MAX 10 I2C Address	AVS_I2C	0x47	LTC3888

Figure 41. I2C Chain

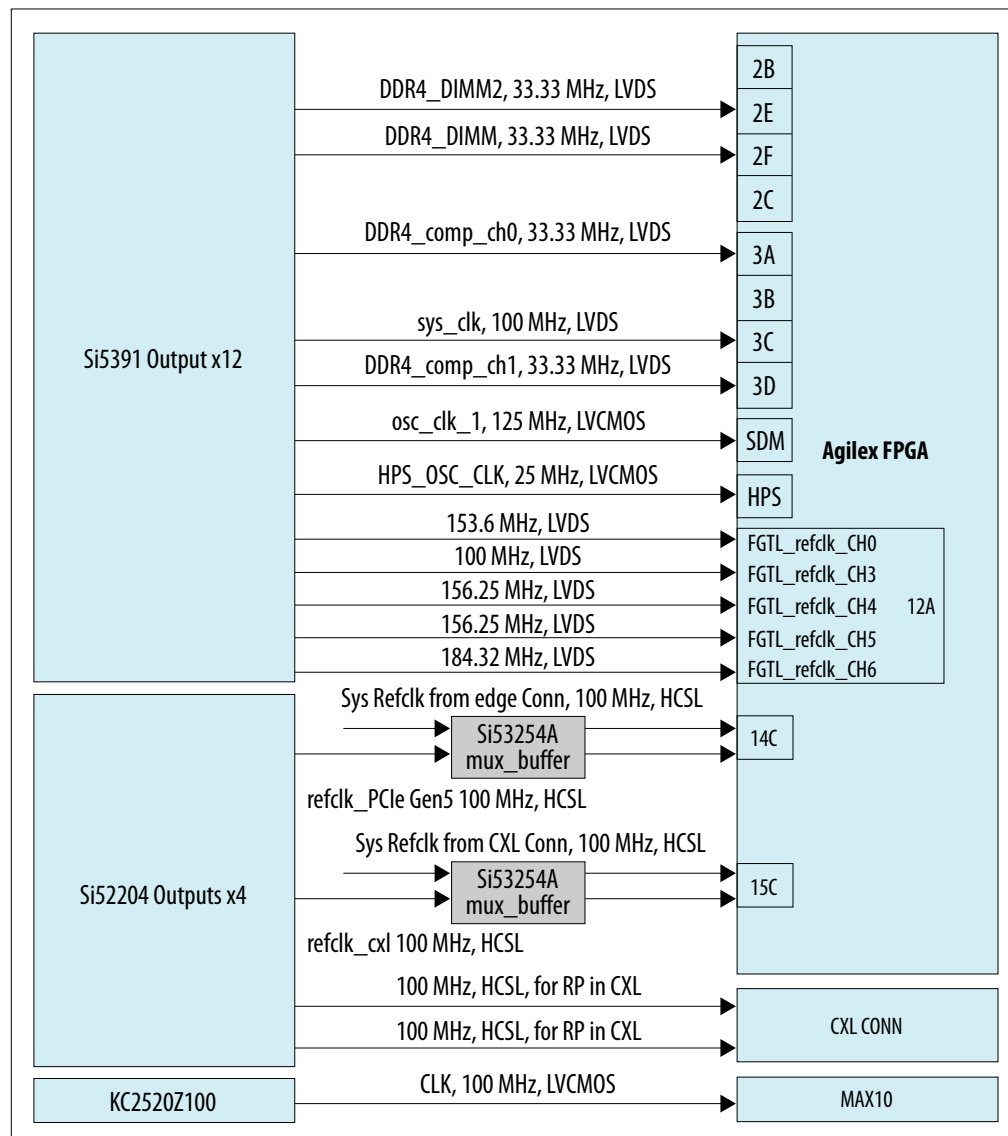


A.12. Clock Circuits

All clocks are supplied by three on-board low-jitter programmable clock generator circuits. The following is the clock connection diagram to the Agilex 7 FPGA. For detailed clock connections, refer to the schematic.

- Si5391 provides most of the clocks to the Agilex 7 FPGA I-Series including reference clocks for memory interfaces, QSFP_DD, and the FPGA SDM/fabric core.
- Si52204 provides the dedicated reference clock as a local clock option for PCIe Gen5 by selecting the inputs of a clock multiplex/buffer Si53254A. Another input of the clock buffer is from PCIe Edge connector as a system clock of PCIe Gen5.
- Si510 provides a 50MHz clock to System MAX 10 and power MAX 10 devices.

Figure 42. Clock Connection Diagram



A.13. System Power

This section describes the Agilex 7 FPGA I-Series development board's power supply.

A laptop style DC power supply is provided with the development kit. Use only the supplied power supply. The power supply has an auto sensing input voltage of 100 ~ 240 V AC power and output 12 V DC power at 20 A to the development board. The 12 V DC input power is then stepped down to various power rails used by the board components.

An on-board multi-channel analog-to-digital converter (ADC) measures both the voltage and current for several specific board rails. The power utilization is displayed on a graphical user interface (GUI) that can graph power consumption versus time.

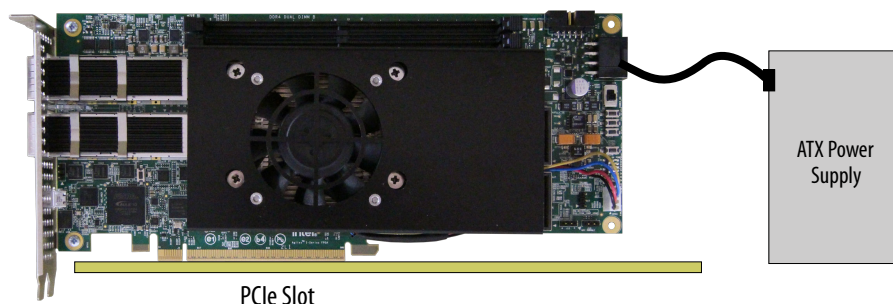
A.13.1. Power Guidelines

The Agilex 7 FPGA I-Series Development Kit has two modes of operation as described below.

In a Standard PCIe-Compliant System

In this mode, plug the board into an available PCI Express* slot and connect the standard 2x4 power cords available from the PC's ATX power supply to **J11** on the board. The PCIe slot together with the auxiliary PCIe power cords are required to power the entire board. If you do not connect the 2x4 auxiliary power connection, it prevents the board from powering on.

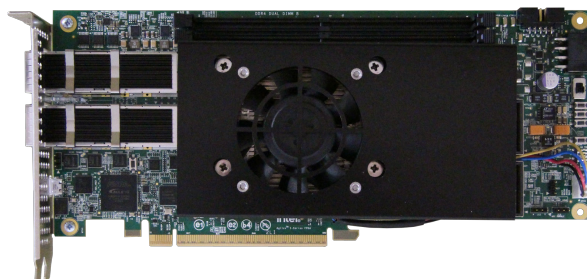
Figure 43. Powering Board Using Standard PCIe-Compliant System



As a Standalone Evaluation Board Powered by Included Power Supply

In this mode, plug the included power supply into the 2x4 pin connector (J11) and the AC power cord of the power supply into a power outlet. This power supply provides the entire power to the board without the need to obtain power from the PCIe slot. The power switch SW6 controls powering of the board.

Figure 44. Powering Board Using Included Power Supply

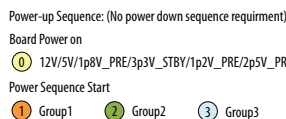


Included Power

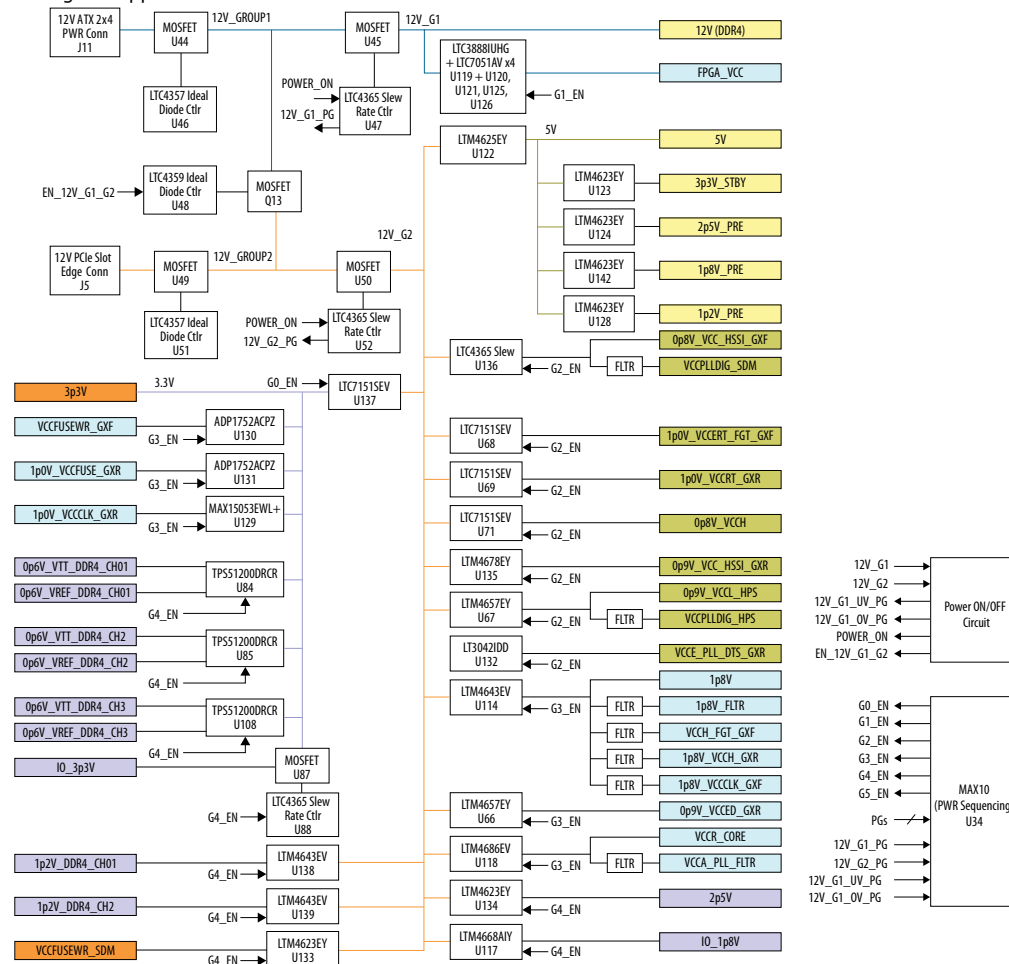
A.13.2. Power Distribution System

The following figure below shows the power distribution system on the Agilex 7 FPGA I-Series development board.

This diagram applies to DK-DEV-AGI027RES and DK-DEV-AGI027R1BES.

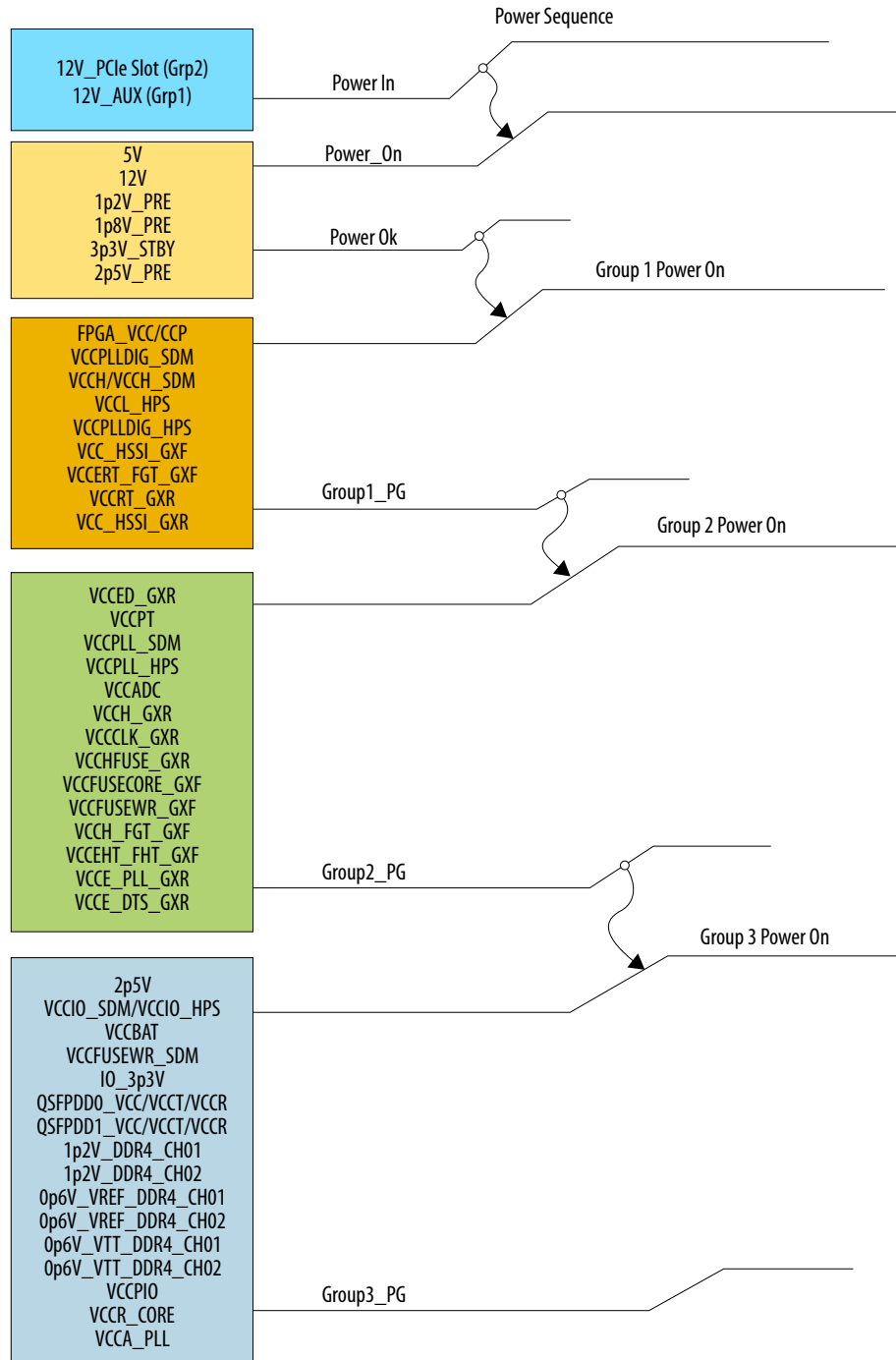


This diagram applies to DK-DEV-AGI027RBES and DK-DEV-AGI027-RA.



For more information on the connection guidelines, refer to the [Agilex 7 Device Family Pin Connection Guidelines](#).

Figure 47. Power Sequence



A.13.4. Power Measurement

Power measurements are provided for six FPGA power rails by reading the power value of various power regulators via their I2C connection.

For DK-DEV-AGI027RES and DK-DEV-AGI027R1BES, the following power rails are monitored:

1. VCC, VCCP (Power sensing by I2C on ED8401)
2. 0.8V (Power sensing by I2C on EM2120L (U72))
3. 1.2V (Power sensing by I2C on EM2120L (U65))
4. 0.9V (Power sensing by I2C on EN2340L (U70))
5. 3.3V (Power sensing by I2C on EM2130H (U64))

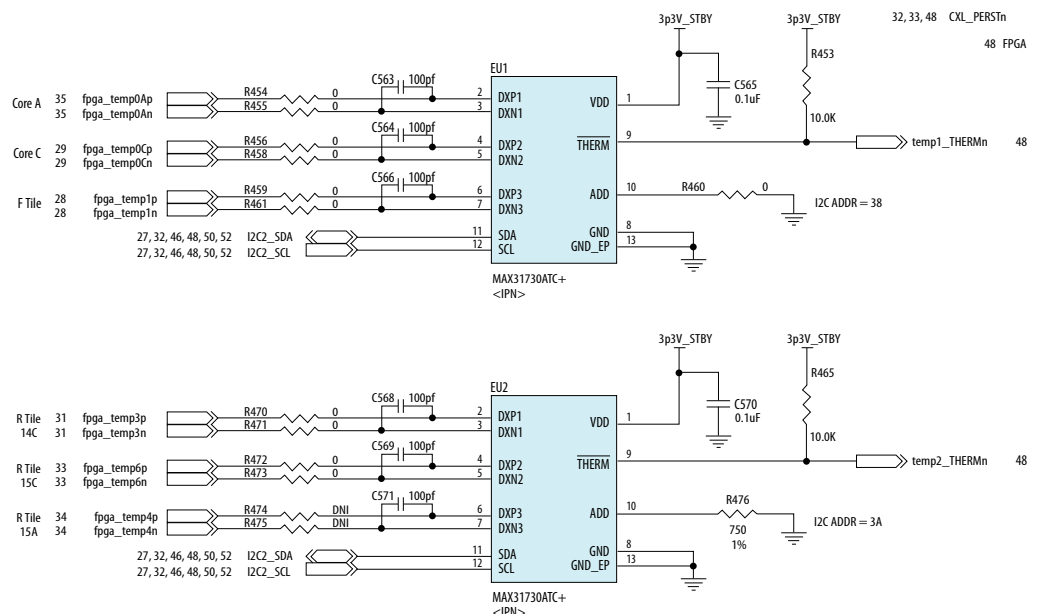
For DK-DEV-AGI027RBES and DK-DEVI-AGI027RA, the following power rails are monitored:

1. VCC, VCCP (Power sensing by I2C on LTC3888 (U119))
2. 0.8V (Power sensing by I2C on LTM4686EV (U136))
3. 1.2V (Power sensing by I2C on LTM4686EV (U118))
4. 0.9V (Power sensing by I2C on LTM4678EY (U135))

A.14. Temperature Monitoring

Temperature monitoring of the Agilex 7 FPGA device is done by a pair of MAX31730ATC+ temperature sense devices. The Agilex 7 FPGA device has 6 die temperature diodes that can be monitored via external temperature sensing devices. The MAX31730ATC+ senses these diodes and convert the signals to digital form for the MAX 10 to read via a I2C bus. Additionally, the `THERMn` signal from the MAX31730ATC+ are brought to the MAX 10 to allow it to immediately sense a temperature fault condition. An over temperature warning LED D9 (Red-colored) is controlled by the MAX 10 device to indicate an over temperature warning. Temperature fault set points can be programmed into the temperature sensing device.

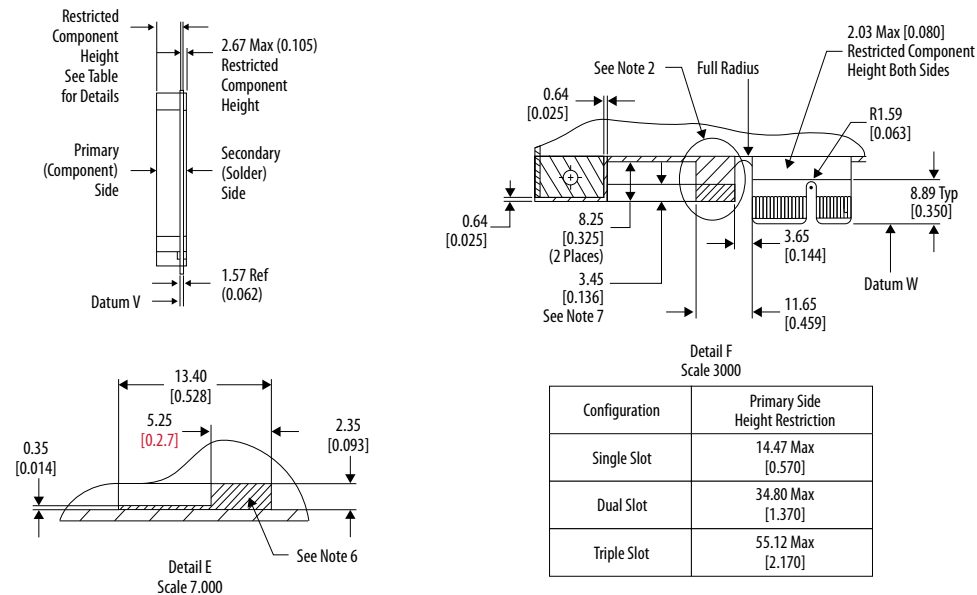
Figure 48. Board Temperature Measurement Circuit



A.15. Mechanical Requirements

The board is a PCIe standard-height (4.376 in tall), 10" long, dual-slot (1.37 in high above the top surface of the PCB) form factor as defined by the PCIe CEM specification Revision 3.0.

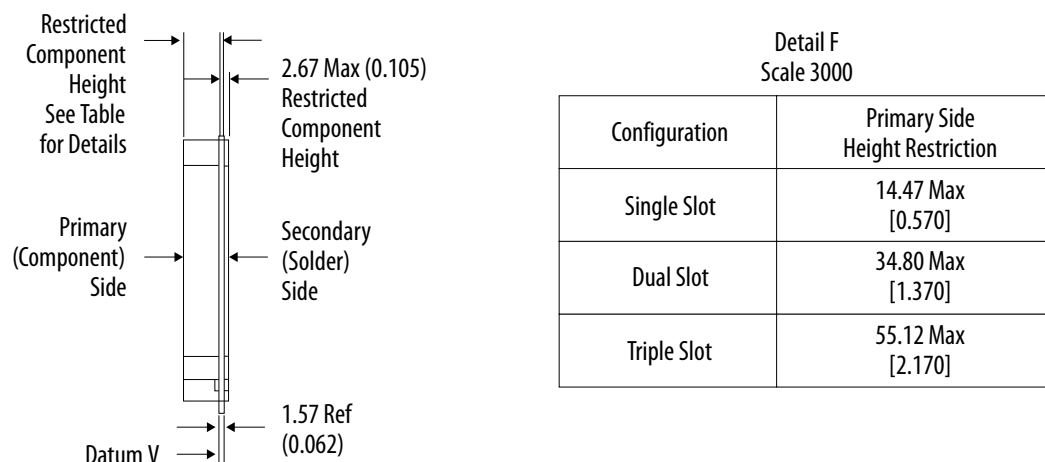
Figure 49. Mechanical Requirements



A.16. Board Thermal Requirements

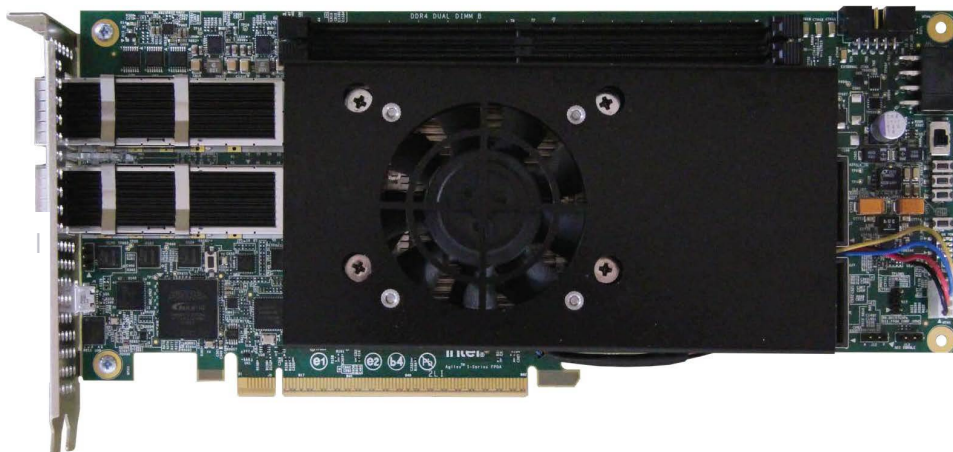
A thermal solution is designed to cool up to 250W total power of the board. An active cooling design is used. The heatsink is designed to meet the height constraints of a 2-slot PCIe card form-factor as defined by the PCIe CEM specification revision 3.0.

Figure 50. Board Thermal Requirements



The heatsink is securely mounted to the board using screws for easy assembly and removal. A thermal material is also used between the FPGA and heatsink to ensure good thermal contact.

Figure 51. Air-Cooled Heatsink Assembly



A.17. Board Operating Conditions

The board should be designed to operate within the below conditions while keeping the FPGA die temperature within its recommended operating T_J as defined in the *Agilex 7 Device Data Sheet* (usually 100°C).

Table 10. Board Operating Conditions

Operating Condition	Range
Maximum power dissipation	250W
Maximum ambient temperature	0°C to 35°C
FPGA junction temperature	85°C

A.18. Over Temperature Warning LED

A red colored LED (D9) is connected to the MAX 10 to indicate when an over temperature fault condition has been detected. The MAX 10 can turn on this LED to indicate an over temperature warning.



B. Additional Information

B.1. Safety and Regulatory Information



ENGINEERING DEVELOPMENT PRODUCT - NOT FOR RESALE OR LEASE

This development kit is intended for laboratory development and engineering use only.

This development kit is designed to allow:

- Product developers and system engineers to evaluate electronic components, circuits, or software associated with the development kit to determine whether to incorporate such items in a finished product.
- Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required Federal Communications Commission (FCC) equipment authorizations are first obtained.

Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference.

Unless the assembled kit is designed to operate under Part 15, Part 18 or Part 95 of the United States Code of Federal Regulations (CFR) Title 47, the operator of the kit must operate under the authority of an FCC licenseholder or must secure an experimental authorization under Part 5 of the United States CFR Title 47.

Safety Assessment and CE & UKCA mark requirements have been completed, however, other certifications that may be required for installation and operation in your region have not been obtained.

B.1.1. Safety Warnings



Power Supply Hazardous Voltage

AC mains voltages are present within the power supply assembly. No user serviceable parts are present inside the power supply.

Power Connect and Disconnect

The AC power supply cord is the primary disconnect device from mains (AC power) and used to remove all DC power from the board/system. The socket outlet must be installed near the equipment and must be readily accessible.

	WARNING	
RISK OF ELECTRIC SHOCK		
Connect only to a properly earth grounded outlet. Apparaten skall anslutas till jordat uttag när den ansluts till ett nätverk.		

System Grounding (Earthing)

To avoid shock, you must ensure that the power cord is connected to a properly wired and grounded receptacle. Ensure that any equipment to which this product is attached to is also connected to properly wired and grounded receptacles.

	WARNING	
RISK OF ELECTRIC SHOCK		
Do not attempt to modify or use the supplied AC power cord if it is not the exact type and rating required.		

Power Cord Requirements

The plug on the power cord must be a grounding-type male plug designed for use in your region. It must have certification marks showing certification by an agency in your region. The connector that plugs into the appliance inlet of the power supply must be an IEC 320, sheet C13, female connector. If the power cord supplied with the system does not meet requirements for use in your region, discard the cord, and do not use it with adapters. Use only certified power supply cord with appropriate gauge, designed for use in your region.



Lightning/Electrical Storm

Do not connect/disconnect any cables or perform installation/maintenance of this product during an electrical storm.

Risk of Fire

To reduce the risk of fire, keep all flammable materials a safe distance away from the boards and power supply. You must configure the development kit on a flame retardant surface.

B.1.2. Safety Cautions

	CAUTION	
	Hot Surfaces and Sharp Edges	
<p>Integrated Circuits and heat sinks may be hot if the system has been running. Also, there might be sharp pins and edges on some boards. Contact should be avoided.</p>		

Thermal and Mechanical Injury

Certain components such as heat sinks, power regulators, and processors may be hot. Heatsink fans are not guarded. Power supply fan may be accessible through guard. Care should be taken to avoid contact with these components.



Cooling Requirements

Maintain a minimum clearance area of 5 centimeters (2 inches) around the side, front and back of the board for cooling purposes. Do not block power supply ventilation holes and fan.

Electro-Magnetic Interference (EMI)

This equipment has not been tested for compliance with emission limits of FCC and similar international regulations. Use of this equipment in a residential location is prohibited. This equipment generates, uses and can radiate radio frequency energy which may result in harmful interference to radio communications. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment on and off, you are required to take measures to eliminate this interference.

Telecommunications Port Restrictions

The wireline telecommunications ports (modem, xDSL, T1/E1) on this product must not be connected to the Public Switched Telecommunication Network (PSTN) as it might result in disruption of the network. No formal telecommunication certification to FCC, R&TTE Directive, or other national requirements have been obtained.



Electrostatic Discharge (ESD) Warning

A properly grounded ESD wrist strap must be worn during operation/installation of the boards, connection of cables, or during installation or removal of daughter cards. Failure to use wrist straps can damage components within the system.

Attention: Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of this product in unsorted municipal waste.

Lithium Ion Battery Warnings



Lithium Battery: Risk of explosion if the lithium battery is replaced by an incorrect type. Risk of fire, explosion, or chemical burn if the battery is mistreated (punctured or crushed). Do not attempt to disassemble. Do not incinerate. Observe proper polarity when replacing battery. Do not dispose—the battery is intended to be serviced and disposed by qualified Intel service personnel only.

Perchlorate Material: Special handling may apply. For more details, refer to www.dtsc.ca.gov/hazardouswaste/perchlorate. This notice is required by California Code of Regulations, Title 22, Division 4.5, Chapter 33: Best Management Practices for Perchlorate Materials. This product includes a battery which contains perchlorate material.

Taiwan battery recycling:



廢電池請回收

(Translation - please recycle batteries)

Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of product in unsorted municipal waste.

B.2. Compliance Information

CE EMI Conformity Caution

This development board is delivered conforming to relevant standards mandated by Directive 2014/30/EU. Because of the nature of programmable logic devices, it is possible for the user to modify the development kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as a result of modifications to the delivered material is the responsibility of the user of this development kit.

