Solution Brief

An Intel Company

MVDR Adaptive Beamformer for Stratix® 10 AX FPGAs Design Example

Description

Stratix® 10 AX FPGAs provide unprecedented technological capabilities that allow wideband and size, weight, and power (SWaP)-sensitive systems. Its unrivaled analog/digital sampling capabilities can be a key enabler in many applications. The enormous computational capabilities of Stratix 10 FPGAs can be a basis for integrated and high-performance processing platforms.

Given such a capable computational platform and its capacity to implement very complex systems, development time and productivity are becoming ever more important for developers.

Altera has developed a variety of high-level design (HLD) flows, targeting different design entry points and types of applications. The SYCL* high-level synthesis (HLS) flow is a C-like entry point, developed around the Data Parallel C++ (DPC++) language. It enables developers to write their implementation using a modern abstracted language while taking advantage of all the verification, debugging, and rich integrated development environments (IDEs) developed for this language. The SYCL HLS compiler can translate this design into FPGA-synthesizable code that can be integrated into the FPGA pipeline.

To showcase how the SYCL HLS flow can be a significant productivity enabler for complex computational systems, Altera developed a minimum variance distortionless response (MVDR) adaptive beamformer design example.

In this example, real-time data is sampled using an array of integrated analog/digital converters and processed using intellectual property (IP) developed using the DPC++ language.

In this design example, the MVDR algorithm is implemented. The MVDR adaptive beamforming uses sample-matrix inversion (SMI) methods, which determine the antenna array weights directly from observation. The adaptive solution is found using a QR decomposition liner solver implemented in floating-point mathematics on the FPGA.

Features

- MVDR adaptive beamformer
- Supports an array of eight elements
- SYCL HLS flow
- Stratix 10 AX FPGA Development kit

Applications

- Radar and electronic countermeasures
- Communication systems

For more information about Altera® design examples, Contact Altera® representative.