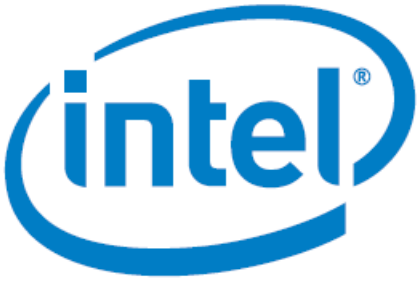

Intel® FPGA Triple-Speed Ethernet and On-Board PHY Chip Reference Design for Agilex® 7 Devices

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Contents

1. Intel® FPGA Triple-Speed Ethernet and On-Board PHY Chip Reference Design for Intel® Agilex® 7 Devices

The Intel® Agilex® 7 FPGA Triple-Speed Ethernet and on-board PHY chip reference design demonstrates Ethernet operation between the Triple-Speed Ethernet Intel FPGA IP core and on-board Marvell 88E1111 PHY chip in Intel® Agilex® 7 F-Series Transceiver-SoC Development Kit. In this reference design, the Triple-Speed Ethernet Intel FPGA IP core is connected to the on-board PHY chip through Serial Gigabit Media Independent Interface (SGMII).

1.1. Features

- Single-channel Triple-Speed Ethernet Intel FPGA IP core operating at data rate of 10/100/1000 Mbps.
- Implementation of the SGMII auto-negotiation feature in order to communicate with on-board PHY chip.
- Sequential random burst test is supported in the hardware test and users can configure the number of packets, payload-data pattern, packet length, source MAC address, and destination MAC address of each burst.
- Support for Ethernet packet transmission and reception through internal MAC/PHY loopback path or Avalon® Streaming reverse loopback path.
- Support for packet monitoring on both TX and RX data paths.
- Support for packet statistics report on both MAC transmitter (TX) and MAC receiver (RX).
- Support for System Console user interface. Users can make use of this TCL-based interface to dynamically configure and monitor any registers in this reference design.

1.2. Hardware and Software Requirements

Intel uses the following hardware and software to test the reference design :

- Intel Quartus® Prime Pro Edition software version 24.1.
- For hardware testing:
  - Intel Agilex 7 F-Series Transceiver SoC Development Kit (AGFB014R24B2E2V)
  - USB 2.0 Type-B cable
  - External Ethernet packet generator (for Avalon Streaming reverse loopback test only)
  - Ethernet Cat5e cable (for Avalon Streaming reverse loopback test only)

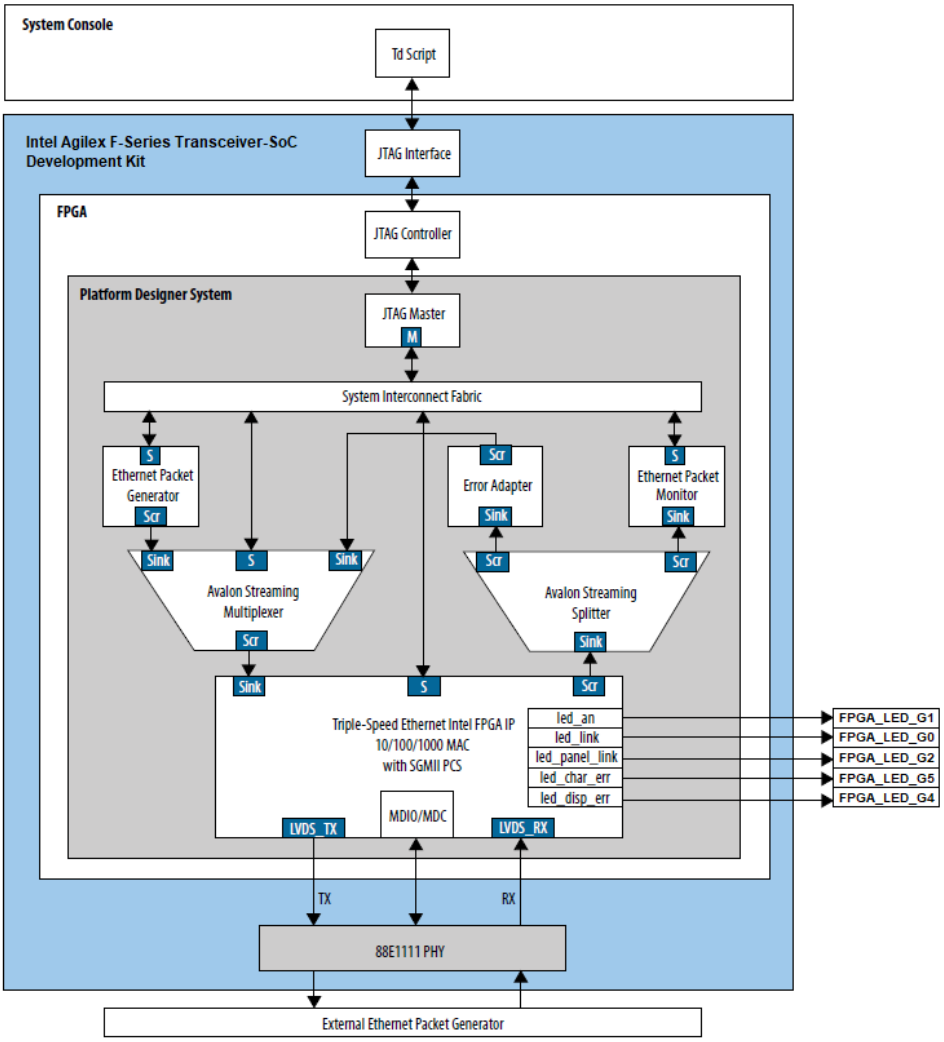
Related Information

- Getting Started with the Design Store
- Intel® Agilex® 7 F-series Transceiver-SoC Development Kit

1.3. Functional Description

The reference design consists of various design components. The following figure shows the design components and the top-level signals of the reference design. In general, the Tcl Script with users and IP configuration is sourced in the System Console to configure the Triple-Speed Ethernet Intel FPGA IP through the JTAG interface. The Ethernet packet traffic flow can be internally generated by an internal Ethernet Packet Generator or sourced from an external Ethernet packet generator to test the Triple-Speed Ethernet Intel FPGA IP. The on-board Marvell 88E1111 PHY chip handles the packet traffic flowing to and coming from the external device. An internal Ethernet Packet Monitor is available to monitor the flow of the packet traffic. Different LEDs are available to monitor the status of Triple-Speed Ethernet Intel FPGA IP for debug purpose. Table 1 in next section provide the details and roles of various design components in the system.

Figure 1. Block Diagram



Legend:
M = Avalon Memory-Mapped Master Port
S = Avalon Memory-Mapped Slave Port
Scr = Avalon Streaming Source Port
Sink = Avalon Streaming Sink Port

1.3.1. Design Components

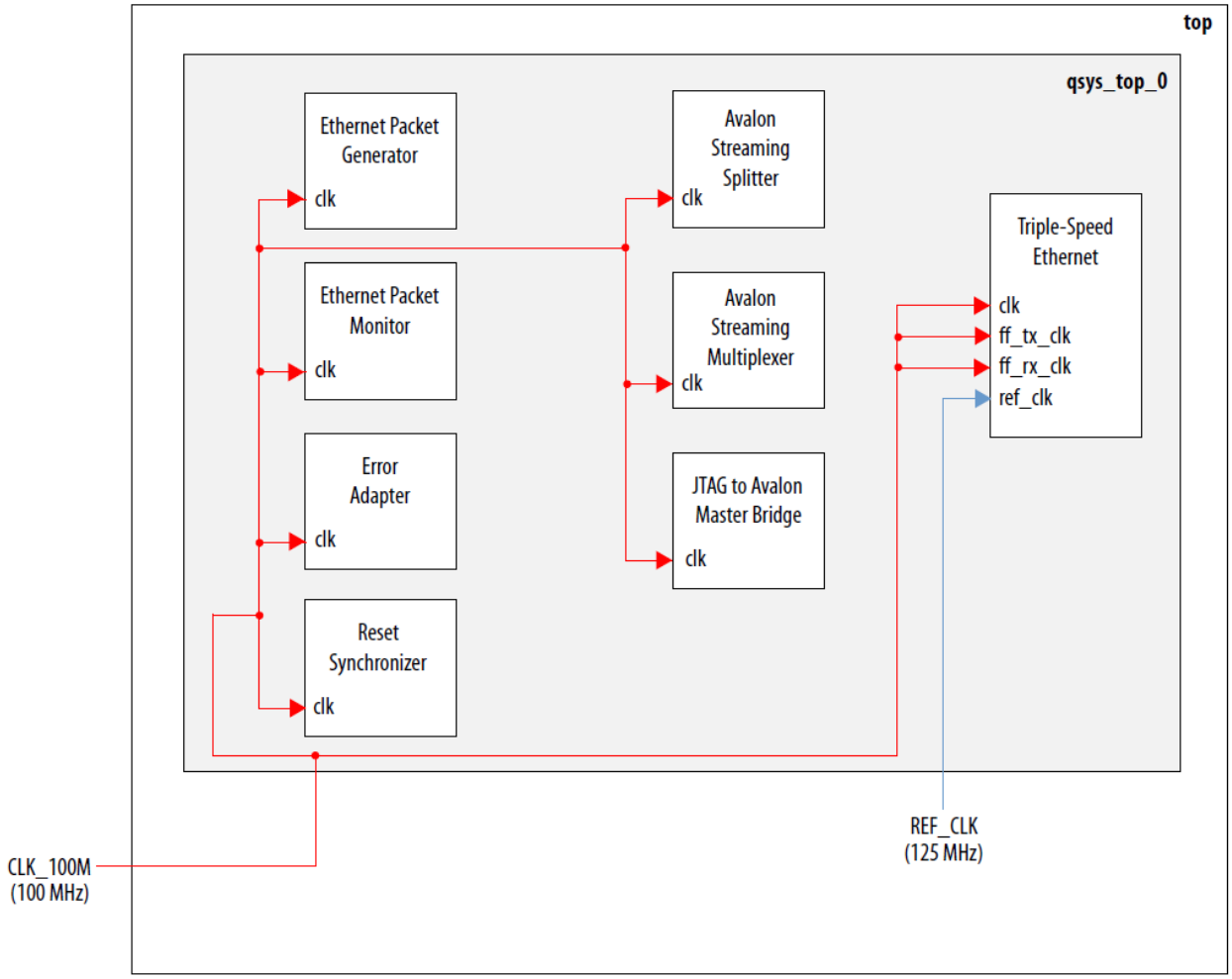
Table 1. Design Components

Component	Description
Triple-Speed Ethernet Intel FPGA IP core	• This IP core provides an integrated Ethernet MAC, PCS, and PMA solution for Ethernet applications. • During data transmission, the Triple-Speed Ethernet Intel FPGA IP core transmits Ethernet packets from Avalon Streaming interface to a 1.25-Gbps serial LVDS I/O interface and the Ethernet packets receiving operation is done with the opposite way.
Ethernet Packet Generator	• This module is a Platform Designer custom component that generates Ethernet packets. • It consists of sub-components such as Ethernet packet generation block, CRC generator, Avalon Memory-Mapped registers, and shift register.
Ethernet Packet Monitor	• This module is a Platform Designer custom component that verifies the payload of all received packets and collects the statistics of each received packet such as number of bytes received. • It consists of sub-components such as CRC checker and Avalon Memory-Mapped registers.
Error Adapter	• This adapter is a Platform Designer custom component that used to connect mismatched Avalon Streaming source and sink interface. • By using this adapter, data source and data sink with different bit width can be connected. For RX-to-TX Avalon Streaming reverse loopback in this reference design, `ff_tx_err` is a 1-bit error signal while `rx_err` is a 6-bit error signal. • This adapter can match the error conditions that are handled by the Avalon Streaming source and Avalon Streaming sink.
Avalon Streaming Multiplexer	• This multiplexer is a Platform Designer custom component that accepts data on its two Avalon Streaming sink interfaces and multiplexes the data for transmission on its Avalon Streaming source interface. • One of the Avalon Streaming sink interface is connected to the Avalon Streaming source interface of Ethernet Packet Generator (For forward MAC/PHY loopback) and another Avalon Streaming sink interface is connected to the Avalon Streaming source interface of Error Adapter (for reverse loopback). • The packets on Avalon Streaming source interface of this multiplexer will be transmitted to Triple-Speed Ethernet Intel FPGA IP core.
Avalon Streaming Splitter	• This splitter is a Platform Designer custom component that accepts data from Triple-Speed Ethernet Intel FPGA IP core through Avalon Streaming sink interface and splits the data on its two Avalon Streaming source interfaces. • One of its Avalon Streaming source interface is connected to the Avalon Streaming sink interface of Ethernet Packet Monitor (for forward MAC/PHY loopback) and another Avalon Streaming source interface is connected to the Avalon Streaming sink interface of Error Adapter (for reverse loopback).
JTAG to Avalon Master Bridge Intel FPGA IP core	• This IP core provides a connection between System Console and Platform Designer system through the physical interface. The System Console initiates Avalon Memory-Mapped transactions by sending encoded streams of bytes through Avalon Master Bridge physical interface.

1.3.2. Clocking Scheme

The figure below describes the clocks that are driving various of design components. Both the clocks are sourced directly from the on-board oscillators.

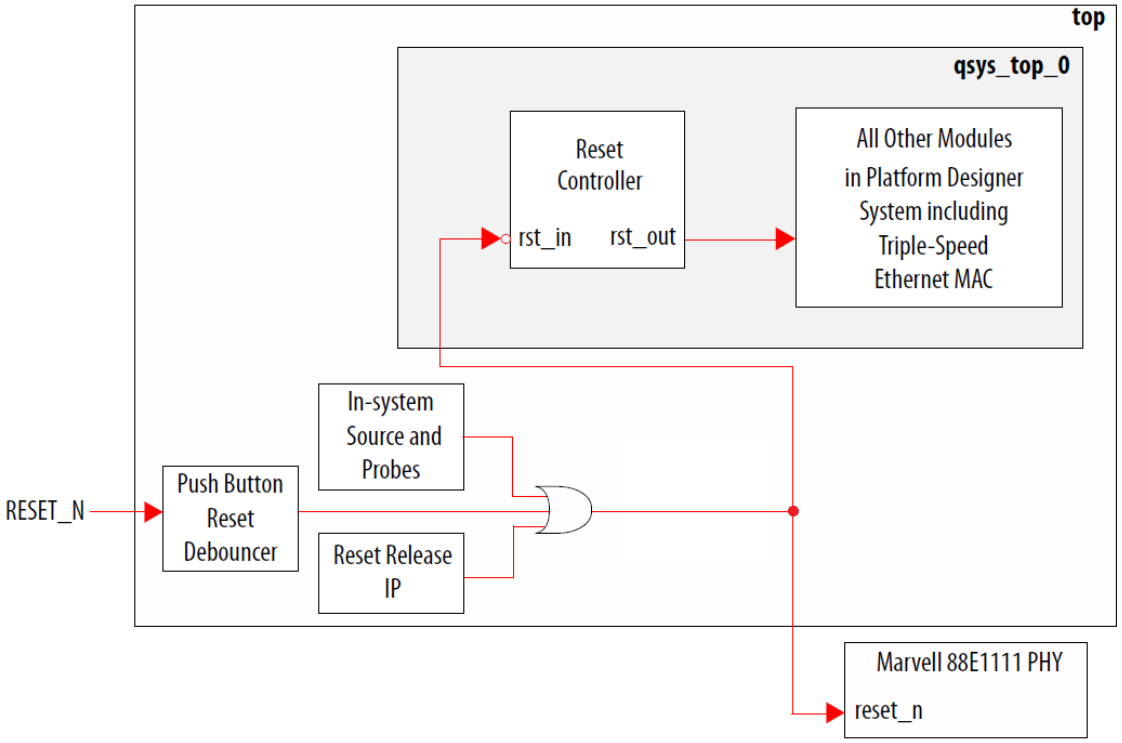
Figure 2. Clocking Scheme



1.3.3. Reset Scheme

The figure below describes the reset paths for various of design components. User can choose to reset the design through either the physical push button or the Quartus ISSP(In-system Source and Probes) which could be found from the tools menu.

Figure 3. Reset Scheme



1.4. TCL Script

Any text editor can be used to edit the TCL scripts which located in `project_directory/sc_tcl`. Please refer to the following sections to find out which TCL script requires changes to run the design while which TCL script can be used as provided without changes.

1.4.1. Configuration Script

The configuration script, `config.tcl` contains the settings and parameters that configure the Triple-Speed Ethernet MAC, Triple-Speed Ethernet PCS and Marvell PHY registers in this reference design.

- Triple-Speed Ethernet MAC configurations can be changed by configuring the MAC registers. For more information about Triple-Speed Ethernet MAC configuration register space, refer to Triple-Speed Ethernet Intel FPGA IP User Guide.
- Triple-Speed Ethernet PCS configurations can be changed by configuring the PCS registers. For more information about Triple-Speed Ethernet PCS configuration register space, refer to Triple-Speed Ethernet Intel FPGA IP User Guide.
- Marvell PHY configurations can be changed by configuring the on-board PHY chip register.

1.4.2. Ethernet Packet Generator Script

The Ethernet Packet Generator script, `eth_gen_start.tcl` contains the parameters and settings to configure the Ethernet Packet Generator registers in this reference design.

Table 2. Ethernet Packet Generator Script Parameters

Parameter	Description
`number_packet`	Sets the total number of packets to be generated by the packet generator.
`eth_gen`	Enables or disables the packet generator.
`length_sel`	Selects fixed or random packet length.
`pkt_length`	Sets the fixed packet length. The packet length can be a value between 24 to 9600 bytes.
`pattern_sel`	Selects the data pattern for the random packet length.
`rand_seed`	Sets the initial random seed for the PRBS generator. This parameter is only valid when you select random packet length.
`source_addr`	Sets the source MAC address.
`destination_addr`	Sets the destination MAC address.

1.4.3. Other Functional Script

The design can run without any modification to the following TCL scripts. Any attempt to make changes to the scripts may make the design malfunction due to these scripts are used to configure various functional blocks within the design such as the setup of Ethernet IP, generation and monitoring of Ethernet packet traffic.

- `tse_mac_config.tcl`
- `tse_pcs_config.tcl`
- `tse_marvel_phy.tcl`
- `eth_gen_mon.tcl`
- `tse_stat_read.tcl`

1.5. Critical Interface Signals

The following tables show the interface signals that are critical to get the design operates without error. If errors happen, the debug process can start from them. For more details about Triple-Speed Ethernet Intel FPGA IP that are not listed here, please refer to Triple-Speed Ethernet Intel FPGA IP User Guide.

Table 3. Clock and Reset Signals

Signal	Direction	Width	Description
clk_clk	Input	1	This is the reference design clock.
reset_reset	Input	1	A single reset signal that used to reset all logic in the reference design. This reset signal is connected to a push button (FPGA_PB1).
triple_speed_ethernet_0_pcs_ref_clk_clock_connection_clk	Input	1	The 125 MHz reference clock for the 1.25 Gbps serial LVDS I/O interface. This clock is sourced from a dedicated reference clock source, which is in the same IO bank as triple_speed_ethernet_0_serial_connection_txp_0 and triple_speed_ethernet_0_serial_connection_rxp_0 pins.

Table 4. 1.25 Gbps Serial Interface Signals

Signal	Direction	Width	Description
triple_speed_ethernet_0_serial_connection_txp_0	Output	1	SGMII serial differential transmit interface. Connect this interface to the on-board PHY chip.
triple_speed_ethernet_0_serial_connection_rxp_0	Input	1	SGMII serial differential receive interface. Connect this interface to the on-board PHY chip.

1.6. System Registers, Configuration Registers and Status Registers

The following tables show the parametric values of the registers used to map the base address of various design component in the system and the registers used to configure Ethernet Packet Generator and Ethernet Packet Monitor that enable traffic of packets being internaslly generated and monitored in the system. Status of the packet traffic flow is captured by certain registers as shown in Table 7. For more details about registers of Triple-Speed Ethernet Intel FPGA IP, please refer to Triple-Speed Ethernet Intel FPGA IP User Guide.

Table 5. System Register Map

Base Address	Block
0x00000000	Triple-Speed Ethernet Intel FPGA IP core
0x00000400	Avalon Streaming Multiplexer
0x00000800	Ethernet Packet Monitor
0x00000C00	Ethernet Packet Generator

Table 6. Avalon Streaming Multiplexer Configuration Registers Map

Byte Offset	Name	Width	R/W	HW Reset Value	Description
0x00	sel	1	RW	0x00	Used to select the Ethernet packet traffic source.

Table 7. Ethernet Packet Monitor Configuration Registers Map

Byte Offset	Name	Width	R/W	HW Reset Value	Description
0x00	number_packet	32	RO	0x00	Total number of packets that the monitor expects to receive.
0x04	packet_rx_ok	32	RO	0x00	Total number of received good packets.
0x08	packet_rx_error	32	RO	0x00	Total number of received packets with errors.
0x0C	byte_rx_count[31:0]	32	RO	0x00	• 64-bit counter that keeps track of the total number of bytes received. • byte_rx_count[31:0] represents the lower 32 bits. • byte_rx_count[63:32] represents the upper 32 bits. • Read byte_rx_count[31:0] followed by byte_rx_count[63:32] in the subsequent cycle to get an accurate count.
0x10	byte_rx_count[63:32]	32	RO	0x00	
0x14	cycle_rx_count[31:0]	32	RO	0x00	• 64-bit counter that keeps track of the total number of cycles the monitor takes to receive all packets. • cycle_rx_count[31:0] represents the lower 32 bits. • cycle_rx_count[63:32] represents the upper 32 bits. • Read byte_rx_count[31:0] followed by byte_rx_count[63:32] in the subsequent cycle to get an accurate count.
0x18	cycle_rx_count[63:32]	32	RO	0x00	
0x1C	receive_ctrl_status	32	RW/RO	0x00	• Bit 0—Set this bit to 1 to trigger packets reception. This bit clears after packet reception is started. • Bit 1—Set this bit to 1 to stop packet reception. This bit clears when packet reception starts. • Bit 2—A value of 1 indicates that the packet monitor has received the total number of packets specified in the number_packet register. • Bit 3—A value of 1 indicates that the current packet received by monitor has CRC error. • Bits [9:4]—Receive error status. The behavior of rx_err signal in Triple-Speed Ethernet Intel FPGA IP core is mapped to this register. • Bits [31:10]—Reserved.

Table 8. Ethernet Packet Generator Configuration Registers Map

Byte Offset	Name	Width	R/W	HW Reset Value	Description
0x00	number_packet	32	RW	0x00	Used to specify the number of packets to be generated.
0x04	config_setting	32	RW	0x00	• Bit 0 — 0: Fixed packet length — 1: Random packet length • Bits [14:1]—Specifies the fixed packet length and the valid values are between 24 to 9600 bytes. It is applicable only when you set bit 0 to 0. • Bit 15—Specifies the data pattern for random packet length. Set this bit to 0 for incremental data pattern. For random data pattern, set this bit to 1. • Bits [31:16]—Reserved.
0x08	rand_seed0	32	RW	0x00	• The lower 32 bits of the random seed. • Occupies bits 31:0 of the PBRS generator when you set the data pattern to random (bit 15 of the configuration register).
0x0c	rand_seed1	32	RW	0x00	• The upper 32 bits of the random seed. • Occupies bits 63:32 of the PBRS generator when you set the data pattern to random (bit 15 of the configuration register).
0x10	source_addr0	32	RW	0x00	• Used to specify 6-bytes source/destination MAC address. • source_addr0/ destination_addr0 = last four bytes of the address • Bits [15:0] of source_ addr1/ destination_addr1 = first two bytes of the address • Bits [31:16] of source_ addr1/ destination_addr1 = unused • For example, if the source MAC address is 00-1C-23-17- 4A-CB, you get the following assignments: — source_addr0 = 0x17231C00 — source_addr1 = 0x0000CB4A
0x14	source_addr1	32	RW	0x00	
0x18	destination_addr0	32	RW	0x00	
0x1C	destination_addr1	32	RW	0x00	

continued...

Byte Offset	Name	Width	R/W	HW Reset Value	Description
0x20	operation	32	RW/RO	0x00	• Bit 0—Set this bit to 1 to trigger packet generation. This bit clears after the packet generation is started. • Bit 1—Set this bit to 1 to stop the packets generation. The generator will complete its current packet transmission 1st before terminates the packet generation. • Bit 2—A value of 1 indicates that the packet generator completes generating the total number of packets specified in the number_packet register. This bit clears each time packet generation triggers. • Bit [31:3]—Reserved.
0x24	packet_tx_count	32	RO	0x00	• This register will keep track the number of packets that the generator transmitted successfully. This register will clear if the packet generation is triggered.

Related Information

Triple-Speed Ethernet Intel® FPGA IP User Guide

1.7. Hardware Testing

There are two kind of hardware testings which users can perform. The first test case is Internal MAC/PHY Loopback whereby users can get the Ethernet packet traffic generated by the design internal Ethernet Packet Generator internally loopback within the MAC or PHY block. As for the second test case is Avalon Streaming Reverse Loopback whereby users can get the Ethernet packet traffic coming from an external Ethernet packet generator loopback through Avalon Streaming blocks.

1.7.1. Test Case—Internal MAC/PHY Loopback

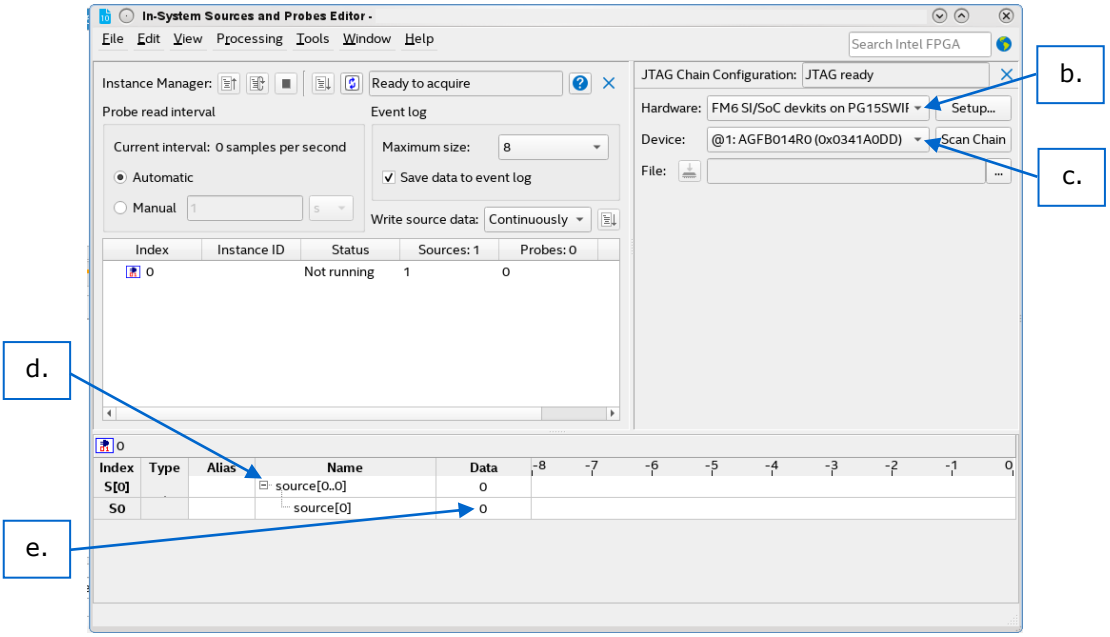
To run the hardware test case, follow these steps:

1. Download the reference design from Design Store and restore the design using Intel Quartus Prime software.
2. Launch the Intel Quartus Prime software and open the project file (top.qpf).
3. Click **Processing ➤ Start Compilation** to compile the design.
4. After the design is compiled successfully, a programming file (top.sof) will be generated and located in the project_directory/output_files directory.
5. Set up the Intel Agilex 7 F-Series Transceiver-SoC Development Kit.
   a. Connect the programming cable to the JTAG connection port (CN1).
   b. Connect the power adapter to the power supply input (J37).

6. In the Intel Quartus Prime software, select **Tools ➤ Programmer** to launch the programmer.
7. Download the generated programming file (`top.sof`) to the development kit using the **Programmer** application.
8. Reset the Ethernet design by either these methods:
   - Press the `FPGA_PB1` push button.
   - Toggle the In-System Source and Probes Editor bit source[0] from 0 to 1 and back to 0 according to Figure 4 below.
     a. In the Quartus, click **Tools ➤ In-System Sources and Probes Editor** to invoke the In-System Sources and Probes Editor.
     b. In the In-System Sources and Probes Editor, click **Hardware Dropdown ➤** Select the Intel Agilex 7 F-Series Transceiver SoC Development Kit name as seen in the **Programmer** application.
     c. In the In-System Sources and Probes Editor, click **Device Dropdown ➤** Select the Intel Agilex 7 Device name as seen in the **Programmer** application.
     d. Click the "**+**" at the side of ***source[0..0]*** to expand the bits list.
     e. Toggle the bit ***source[0]*** from 0 to 1 and back to 0.

Note: The design must be reset whenever you begin a new test. The reset must be asserted for at least 10ms because the `RESET_N` pin of the Marvell PHY needs to be kept low for 10 ms which is the minimum reset requirement of the Marvell PHY.

Figure 4. Reset Through In-System Sources and Probes Editor



9. Open the `config.tcl` script using text editor, which located in `project_directory/sc_tcl` directory. Please make sure the following parameters are set accordingly to achieve intended operating speed rate and mode. For more information, refer to Configuration Script on page 7.
    a. Selection of speed rate.
        i. For 10Mbps, set `ETH_SPEED` to 0 while to `ENA_10` to 1.
        ii. For 10/100/1000Mbps, set `ETH_SPEED` to 0 while to `ENA_10` to 0.
        iii. For 1000Mbps ONLY, set `ETH_SPEED` to 1 while to `ENA_10` to 0 or 1. This is not recommended as it will cause link failure if the PHY is running at 10/100Mbps ONLY.
    b. Mode enablement for MAC loopback or PHY loopback.
        i. For MAC loopback, set `LOOP_ENA` to 1 while `PHY_LOOPBACK` to 1 or 0.
        ii. For PHY loopback, set `LOOP_ENA` to 0 while `PHY_LOOPBACK` to 1.
10. In the Intel Quartus Prime software, select **Tools ➤ System Debugging Tools ➤ System Console** to launch the system console.
11. In the System Console command shell, change the directory to `project_directory/sc_tcl`.
12. Run the following command in the System Console command shell to start TSE MAC, TSE PCS, and on-board PHY chip configurations:

    ```
    source config.tcl
    ```

13. Run the following command in System Console command shell to start generating and monitoring Ethernet packets:

    ```
    source eth_gen_start.tcl
    ```

    Note: Open the `eth_gen_start.tcl` script which located in `project_directory/sc_tcl` directory to set to desired configurations. For more information, refer to Ethernet Packet Generator Script on page 8.

    The Avalon Streaming Multiplexer will be configured for forward MAC/PHY loopback when the Ethernet Packet Generator is started and the Ethernet Packet Monitor automatically starts after the Ethernet packet is generated. The System Console displays the number of packets with/without error received by the Ethernet Packet Monitor (refer to Figure 8 on page 18).
14. Run the following command to view the TSE MAC statistic counters:

    ```
    source tse_stat_read.tcl
    ```

Figure 5. Sample Output—MAC Configuration Summary

```
================================================================================
          Starting TSE MAC Configuration System Console
================================================================================


Info: Opened JTAG Master Service


Info: Configure TSE MAC


TSE MAC Rev                     = 0x00001304
TSE MAC write Scratch           = 0xaaaaaaaa
TSE MAC read Scratch            = 0xaaaaaaaa
Command Config(Value)           = 8033
Command Config(Pre-write)                = 0x00008030
Command Config(Post-write)               = 0x00008033
MAC Address 0                   = 0x22334450
MAC Address 1                   = 0x0000ee11
Frame Length                    = 0x000005ee
Pause Quanta                    = 0x0000ffff
RX Section Empty                = 0x00001ff0
RX Section Full                 = 0x00000010
TX Section Empty                = 0x00001ff0
TX Section Full                 = 0x00000010
RX Almost Empty                 = 0x00000008
RX Almost Full                  = 0x00000008
TX Almost Empty                 = 0x00000008
TX Almost Full                  = 0x00000003
MDIO Address 0                  = 0x00000000
MDIO Address 1                  = 0x00000000
Regiter Status                  = 0x00000000
TX IPG Length                   = 0x0000000c
TX Command Status               = 0x00000000
RX Command Status               = 0x00000000

Info: Closed JTAG Master Service
```

Figure 6. Sample Output—PCS Configuration Summary

```
================================================================================
          Starting TSE PCS Configuration System Console
================================================================================


Info: Opened JTAG Master Service


Info: Configure TSE PCS


TSE PCS rev                    = 0x00001304
TSE PCS write scratch          = 0x0000aaaa
TSE PCS read scratch           = 0x0000aaaa
TSE PCS if_mode                = 0x0000000b
TSE PCS control register       = 0x00001140
Waiting Link Up.....
Link is established!
Partner Ability:

Copper link interface is down.
Copper operating in Half Duplex mode.
Copper operating Speed 10Mbps

Info: Closed JTAG Master Service
```

Figure 7. Sample Output—On-Board PHY Chip Configuration Summary

```
================================================================================
          Starting Marvell PHY Configuration System Console
================================================================================


Info: Opened JTAG Master Service


Info: Configure On Board Ethernet PHY Chip


Configure PHY.
Set PHY SPEED to 1000Mbps
Enable PHY Auto-Negotiation
Enable PHY In Full Duplex Mode
PHY read Control Register                          = 0x00001140
Advertise PHY 100BASE-TX & 10BASE-TX Full Duplex
PHY read AN Advertisement Register                 = 0x00000141
Advertise PHY 1000BASE-T Full Duplex
PHY read 1000BASE-T Control Register               = 0x00000e00
Set PHY Synchronizing FIFO to maximum
Enable PHY MDIX crossover
Set PHY HWCFG_MODE for SGMII to Copper Without Clock
PHY read Extended PHY Specific Status Register     = 0x00008484
PHY Link Down!
PHY Speed and Duplex Resolve Failed!
PHY operating in Half Duplex mode.
PHY operating Speed 1000Mbps
PHY read Status Register                           = 0x00007949
PHY read Control Register               = 0x00001140

Info: Closed JTAG Master Service
```

Note :

1. If the RJ-45 port is not connected to an external device(eg. Tester or development kit), the "PHY Link Down!" message is normal.
2. The MAC internal loopback and PHY internal loopback could be performed without connecting the RJ-45 port to an external device.

Figure 8. Sample Output—Ethernet Packet Generator and Ethernet Packet Monitor Statistics

```
================================================================================
          Starting Ethernet Generator / Monitor System Console
================================================================================


Info: Opened JTAG Master Service


Use Ethernet Generator
Number of packets     = 10000
Configuration setting:
- Length              : Random
- Packets length      : 1500
- Pattern             : Random
Random seed 0                    = 0x56789abc
Random seed 1                    = 0x00001234
Source address 0                 = 0x22334450
Source address 1                 = 0x0000ee11
Destination address 0            = 0x22334450
Destination address 1            = 0x0000ee11
Start Ethernet Generator
Monitor receive done
Number of packets received OK             = 10000
Number of packets received error          = 0

Info: Closed JTAG Master Service
```

Figure 9. Sample Output—TX and RX MAC Statistic Counters

```
TSE MAC Statistics Counters Map

============================


Addr       Name                                Read Value
----       ----                                ----------
0x68       aFramesTransmittedOK                0x00002710
0x6c       aFramesReceivedOK                   0x00002710
0x70       aFrameCheckSequenceErrors           0x00000000
0x74       aAlignmentErrors                    0x00000000
0x78       aOctetsTransmittedOK                0x005f3b89
0x7c       aOctetsReceivedOK                   0x005f3b89
0x80       aTxPAUSEMACCtrlFrames               0x00000000
0x84       aRxPAUSEMACCtrlFrames               0x00000000
0x88       ifInErrors                          0x00000000
0x8c       ifOutErrors                         0x00000000
0x90       ifInUcastPkts                       0x00002710
0x94       ifInMulticastPkts                   0x00000000
0x98       ifInBroadcastPkts                   0x00000000
0x9c       ifOutDiscards                       0x00000000
0xa0       ifOutUcastPkts                      0x00002710
0xa4       ifOutMulticastPkts                  0x00000000
0xa8       ifOutBroadcastPkts                  0x00000000
0xac       etherStatsDropEvents                0x00000000
0xb0       etherStatsOctets                    0x0061faa9
0xb4       etherStatsPkts                      0x00002710
0xb8       etherStatsUndersizePkts             0x00000000
0xbc       etherStatsOversizePkts              0x00000000
0xc0       etherStatsPkts64Octets              0x000001a8
0xc4       etherStatsPkts65to127Octets         0x00000273
0xc8       etherStatsPkts128to255Octets        0x00000532
0xcc       etherStatsPkts256to511Octets        0x00000942
0xd0       etherStatsPkts512to1023Octets       0x00000b32
0xd4       etherStatsPkts1024to1518Octets      0x0000094f
0xd8       etherStatsPkts1519toXOctets         0x00000000
0xdc       etherStatsJabbers                   0x00000000
0xe0       etherStatsFragments                 0x00000000
```

Related Information

- Marvell 88E1111 PHY Configuration Steps

1.7.2. Test Case—Avalon Streaming Reverse Loopback

To run the hardware test case, follow these steps:

1. Download the reference design from Design Store and restore the design using Intel Quartus Prime software.
2. Launch the Intel Quartus Prime software and open the project file (`top.qpf`).
3. Click **Processing ➤ Start Compilation** to compile the design.
4. After the design is compiled successfully, a programming file (`top.sof`) will be generated and located in the `project_directory/output_files` directory.
5. Set up the Intel Agilex 7 F-Series Transceiver-SoC Development Kit.
   a. Connect the external packet generator to the RJ-45 port of the development kit (J15) by using Ethernet Cat5e cable.
   b. Connect the programming cable to the JTAG connection port (CN1).
   c. Connect the power adapter to the power supply input (J37).
6. In the Intel Quartus Prime software, select **Tools ➤ Programmer** to launch the programmer.
7. Download the generated programming file (`top.sof`) to the development kit using the **Programmer** application.
8. Reset the Ethernet design by either these methods:
   - Press the `FPGA_PB1` push button.
   - Toggle the In-System Source and Probes Editor bit source[0] from 0 to 1 and back to 0 according to Figure 4 on page 13.

   Note: The design must be reset whenever you begin a new test. The reset must be asserted for at least 10ms because the `RESET_N` pin of the Marvell PHY needs to be kept low for 10 ms which is the minimum reset requirement of the Marvell PHY.
9. Open the `config.tcl` script using text editor, which located in `project_directory/sc_tcl` directory. Please ensure the following parameters are set accordingly. For more information, refer to Configuration Script on page 7.
   a. Please make sure `ETH_SPEED` is set to 0 and `ENA_10` to 0 to ensure the MAC is not forced to operate at 1000Mbps ONLY so that the MAC could follow the speed rate of the PHY set in step 9.c below.
   b. If you wish to operate the MAC in 1000Mbps ONLY, you can set `ETH_SPEED` to 1. This is not recommended as it will cause link failure if the PHY is running at 10/100Mbps ONLY.
   c. Selection of speed rate.
      i. For 10Mbps ONLY, set `PHY_ETH_SPEED` to 10.
      ii. For 10/100Mbps ONLY, set `PHY_ETH_SPEED` to 100.
      iii. For 10/100/1000Mbps, set `PHY_ETH_SPEED` to 1000.
   d. Please make sure the `LOOP_ENA` and `PHY_LOOPBACK` parameter is set to 0 to ensure the MAC/PHY loopback mode or PHY loopback mode is disabled.
10. In the Intel Quartus Prime software, select **Tools ➤ System Debugging Tools ➤ System Console** to launch the System Console.
11. In the System Console command shell, change the directory to `project_directory/sc_tcl`.

12. Run the following command in the System Console command shell to start TSE MAC, TSE PCS, and on-board PHY chip configurations:

```
source config.tcl
```

    The System Console displays the copper link connection status and the resolved operating speed and duplex mode of on-board PHY Chip (refer to Figure 12 on page 23).

13. The Avalon Streaming Multiplexer is by default configured for reverse loopback after reset in step 8. Therefore, start to transmit the Ethernet packets from the external packet generator to the development kit. Verify the number of packets that successfully loop back to the external packet generator.
14. Run the following command to view the TSE MAC statistic counters:

```
source tse_stat_read.tcl
```

Figure 10. Sample Output—MAC Configuration Summary

```
Info: Opened JTAG Master Service


Info: Configure TSE MAC


TSE MAC Rev                     = 0x00001303
TSE MAC write Scratch           = 0xaaaaaaaa
TSE MAC read Scratch            = 0xaaaaaaaa
Command Config(Value)           = 33
Command Config(Pre-write)                 = 0x00000030
Command Config(Post-write)                = 0x00000033
MAC Address 0                   = 0x22334450
MAC Address 1                   = 0x0000ee11
Frame Length                    = 0x000005ee
Pause Quanta                    = 0x0000ffff
RX Section Empty                = 0x00001ff0
RX Section Full                 = 0x00000010
TX Section Empty                = 0x00001ff0
TX Section Full                 = 0x00000010
RX Almost Empty                 = 0x00000008
RX Almost Full                  = 0x00000008
TX Almost Empty                 = 0x00000008
TX Almost Full                  = 0x00000003
MDIO Address 0                  = 0x00000000
MDIO Address 1                  = 0x00000000
Regiter Status                  = 0x00000000
TX IPG Length                   = 0x0000000c
TX Command Status               = 0x00000000
RX Command Status               = 0x00000000

Info: Closed JTAG Master Service
```

Figure 11. Sample Output—PCS Configuration Summary

```
================================================================================
          Starting TSE PCS Configuration System Console
================================================================================


Info: Opened JTAG Master Service


Info: Configure TSE PCS


TSE PCS rev                    = 0x00001303
TSE PCS write scratch          = 0x0000aaaa
TSE PCS read scratch           = 0x0000aaaa
TSE PCS if_mode                = 0x0000000b
TSE PCS control register       = 0x00001140
Waiting Link Up.....
Link is established!
Partner Ability:

Copper link interface is up.
Copper operating in Full Duplex mode.
Copper operating Speed 1000Mbps

Info: Closed JTAG Master Service
```

Figure 12. Sample Output—On-Board PHY Chip Configurations

```
================================================================================
          Starting Marvell PHY Configuration System Console
================================================================================


Info: Opened JTAG Master Service


Info: Configure On Board Ethernet PHY Chip


Configure PHY.
Set PHY SPEED to 1000Mbps
Enable PHY Auto-Negotiation
Enable PHY In Full Duplex Mode
PHY read Control Register                              = 0x00001140
Advertise PHY 100BASE-TX & 10BASE-TX Full Duplex
PHY read AN Advertisement Register                     = 0x00000141
Advertise PHY 1000BASE-T Full Duplex
PHY read 1000BASE-T Control Register                   = 0x00000e00
Set PHY Synchronizing FIFO to maximum
Enable PHY MDIX crossover
Set PHY HWCFG_MODE for SGMII to Copper Without Clock
PHY read Extended PHY Specific Status Register         = 0x00008484
PHY Link Up.
PHY Speed and Duplex Resolved.
PHY operating in Full Duplex mode.
PHY operating Speed 1000Mbps
PHY read Status Register                               = 0x00007969
PHY read Control Register                 = 0x00001140

Info: Closed JTAG Master Service
```

Figure 13. Sample Output—TX and RX MAC Statistic Counters

```
TSE MAC Statistics Counters Map

============================


Addr       Name                                Read Value

----       ----                                ----------

0x68       aFramesTransmittedOK                0x00002710

0x6c       aFramesReceivedOK                   0x00002710

0x70       aFrameCheckSequenceErrors           0x00000000

0x74       aAlignmentErrors                    0x00000000

0x78       aOctetsTransmittedOK                0x005f3b89

0x7c       aOctetsReceivedOK                   0x005f3b89

0x80       aTxPAUSEMACCtrlFrames               0x00000000

0x84       aRxPAUSEMACCtrlFrames               0x00000000

0x88       ifInErrors                          0x00000000

0x8c       ifOutErrors                         0x00000000

0x90       ifInUcastPkts                       0x00002710

0x94       ifInMulticastPkts                   0x00000000

0x98       ifInBroadcastPkts                   0x00000000

0x9c       ifOutDiscards                       0x00000000

0xa0       ifOutUcastPkts                      0x00002710

0xa4       ifOutMulticastPkts                  0x00000000

0xa8       ifOutBroadcastPkts                  0x00000000

0xac       etherStatsDropEvents                0x00000000

0xb0       etherStatsOctets                    0x0061faa9

0xb4       etherStatsPkts                      0x00002710

0xb8       etherStatsUndersizePkts             0x00000000

0xbc       etherStatsOversizePkts              0x00000000

0xc0       etherStatsPkts64Octets              0x000001a8

0xc4       etherStatsPkts65to127Octets         0x00000273

0xc8       etherStatsPkts128to255Octets        0x00000532

0xcc       etherStatsPkts256to511Octets        0x00000942

0xd0       etherStatsPkts512to1023Octets       0x00000b32

0xd4       etherStatsPkts1024to1518Octets      0x0000094f

0xd8       etherStatsPkts1519toXOctets         0x00000000

0xdc       etherStatsJabbers                   0x00000000

0xe0       etherStatsFragments                 0x00000000
```

Related Information

- Marvell 88E1111 PHY Configuration Steps

1.8. Document Revision History : Intel FPGA Triple- Speed Ethernet and On-Board PHY Chip Reference Design for Intel Agilex 7 Devices

Date	Version	Changes
July 2020	2020.07.30	• Initial release
November 2022	2022.11.30	• Quartus version updated to 22.3 and beyond
July 2023	2023.07.05	• Update product name to Intel® Agilex® 7 per Intel® product trademark guideline.
October 2023	2023.10.02	• Migrated the design to Production board(Ordering Code: DK-SI-AGF014EA)
April 2024	2024.04.16	• Migrated the design from 23.3 to 24.1 Quartus version. • Updated Triple Speed Ethernet User guide links to latest version.