



# **Cyclone® V GT FPGA Development Kit User Guide**



**Online Version**



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## Contents

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<b>1. Kit Features.....</b>	<b>4</b>
1.1. Hardware.....	4
1.2. Software.....	4
1.2.1. Intel® Quartus® Prime Software.....	4
1.2.2. Cyclone V GT FPGA Development Kit Installer.....	5
<b>2. Getting Started.....</b>	<b>6</b>
2.1. Before You Begin.....	6
2.2. Inspecting the Boards.....	6
2.3. References for Getting Started.....	7
<b>3. Software Installation.....</b>	<b>8</b>
3.1. Installing the Intel Quartus Prime Subscription Edition Software.....	8
3.2. Activating Your License.....	8
3.3. Installing the Development Kit.....	9
3.4. Installing the Intel FPGA Download Cable II Driver.....	10
<b>4. Development Board Setup.....</b>	<b>11</b>
4.1. Setting Up the Board.....	11
4.2. Factory Default Switch and Jumper Settings.....	12
4.3. Configuring the MAX V Device to Program EPCQ.....	15
4.4. Restoring the MAX V CPLD to the Factory Settings.....	15
4.5. Restoring the Flash Device to the Factory Settings.....	16
4.6. Configuring the FPGA Using the Intel Quartus Prime Programmer.....	17
<b>5. Board Update Portal.....</b>	<b>18</b>
5.1. Connecting to the Board Update Portal Web Page.....	18
5.2. Using the Board Update Portal to Write User Designs.....	19
<b>6. Board Test System.....</b>	<b>20</b>
6.1. Preparing to Run the Board Test System.....	21
6.2. Running the Board Test System.....	21
6.3. Using the Board Test System.....	21
6.3.1. The Configure Menu.....	21
6.3.2. The System Info Tab.....	22
6.3.3. The GPIO Tab.....	26
6.3.4. The Flash Tab.....	28
6.3.5. The DDR3x40 and DDR3x64 Tabs.....	29
6.3.6. The HSMA Tab.....	32
6.3.7. The HSMB Tab.....	34
6.4. The Power Monitor.....	37
6.4.1. Power Monitor Features.....	37
6.4.2. Power Monitor Controls.....	38
6.5. The Clock Control.....	38
6.5.1. Clock Control Features.....	39
6.5.2. Clock Control Controls.....	39
<b>7. Document Revision History for Cyclone V GT FPGA Development Kit User Guide.....</b>	<b>41</b>

<b>A. Programming the Flash Memory Device.....</b>	<b>42</b>
A.1. CFI Flash Memory Map.....	42
A.2. Preparing Design Files for Flash Programming.....	43
A.3. Creating Flash Files Using the Nios II EDS.....	43
A.4. Converting Additional Files.....	44
A.5. Programming Flash Memory Using the Nios II EDS.....	44
A.6. Programming Flash Memory Using the Board Update Portal.....	45
<b>B. Additional Information.....</b>	<b>46</b>
B.1. Safety and Regulatory Information.....	46
B.1.1. Safety Warnings.....	47
B.1.2. Safety Cautions.....	48
B.2. Compliance Information.....	51

## 1. Kit Features

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This section briefly describes the Cyclone® V GT FPGA Development Kit contents.

### 1.1. Hardware

The Cyclone V GT FPGA Development Kit includes the following hardware:

- Cyclone V GT FPGA development board
- Debug Header Breakout Board HSMC
- Loopback Daughtercard HSMC
- Power supply and cables:
  - Power supply and AC adapters for North America/Japan, Europe, and the United Kingdom
  - USB cable
  - Ethernet cable
  - Mini SMB cable

**Table 1. Cyclone V GT FPGA Development Kit Ordering Information**

Development Kit Version	Ordering Code	Device Part Number
Cyclone V GT FPGA Development Kit (Version B) Power Solution 2	DK-DEV-5CGTD9N-B	5CGTFD9E5F35C7N

For a complete list of this kit's contents and capabilities, refer to the *Cyclone V GT FPGA Development Kit* page.

#### Related Information

[Cyclone V GT FPGA Development Kit](#)

### 1.2. Software

The software for this kit, described in the following sections, is available on the Intel website for immediate downloading. You can also request to have Intel mail the software to you on DVDs.

#### 1.2.1. Intel® Quartus® Prime Software

Your kit includes a license for the Development Kit Edition (DKE) of the Intel® Quartus® Prime software (Windows\* platform only). For one year, this license entitles you to most of the features of the Subscription Edition (excluding the IP Base Suite).

After tone the DKE license will not be valid and you will not be permitted to use this version of the Intel Quartus Prime software. To continue using the Intel Quartus Prime software, you should download the free Intel Quartus Prime Web edition or purchase a subscription to Intel Quartus Prime software. For more information, refer to the *Intel Quartus Prime Design Software* page of the Intel website.

The Intel Quartus Prime Development Kit Edition (DKE) software includes the following items:

- Intel Quartus Prime software—The Intel Quartus Prime software, including the Platform Designer (Standard) system integration tool, provides a comprehensive environment for network on a chip (NoC) design. The Intel Quartus Prime software integrates into nearly any design environment and provides interfaces to industry-standard EDA tools.
- Intel FPGA IP Library—A library that contains Intel FPGA IP functions. You can evaluate Intel FPGA IP functions by using the Intel FPGA IP Evaluation Mode feature to do the following:
  - Simulate behavior of an Intel FPGA IP function within your system.
  - Verify functionality of your design, and quickly and easily evaluate its size and speed.
  - Generate time-limited device programming files for designs that include Intel FPGA IP functions.
  - Program a device and verify your design in hardware.

The Intel FPGA IP Evaluation Mode hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use an Intel FPGA IP function in production.

For more information about the Intel FPGA IP Evaluation Mode, refer to *AN 320: Using Intel® FPGA IP Evaluation Mode*.

Nios® II Embedded Design Suite (EDS)—A full-featured set of tools that allows you to develop embedded software for the Nios II processor, which you can include in your Intel FPGA designs.

#### Related Information

- [Intel Quartus Prime Design Software](#)
- [AN 320: Using Intel FPGA IP Evaluation Mode](#)

### 1.2.2. Cyclone V GT FPGA Development Kit Installer

The license-free Cyclone V GT FPGA Development Kit installer includes all the documentation and design examples for the kit.

For information on installing the Development Kit Installer, refer to *Installing the Development Kit*.

#### Related Information

[Installing the Development Kit](#) on page 9



## 2. Getting Started

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This chapter provides the initial guidelines to get you started using the kit.

### 2.1. Before You Begin

You must check the kit contents and inspect the boards to verify that you received all of the items listed in *Kit Features* before using the kit or installing the software.

In case any of the items are missing, you must contact Intel before you proceed.

### 2.2. Inspecting the Boards

Following are the steps to inspect each board:

1. Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment. You may damage the board without proper anti-static handling.
2. Verify that components on the boards appear to be in place and intact.

In typical applications with the Cyclone V GT FPGA development board, a heat sink is not necessary. However, under extreme conditions or for engineering sample silicon, the board might require additional cooling to stay within operating temperature guidelines. The board has two holes near the FPGA that accommodate many different heat sinks, including the Dynatron CHR-152. You can perform power consumption and thermal modeling to determine whether your application requires additional cooling. For information about measuring board and FPGA power in real time. Refer to *The Power Monitor* section for more details.

For more information about power consumption and thermal modeling, refer to *AN 358: Thermal Management for FPGAs*.

#### Related Information

- [The Power Monitor](#) on page 37
- [Thermal Management for Intel FPGAs](#)

## 2.3. References for Getting Started

Use the following links to check the Intel website for other related information:

- For complete information about the FPGA development board hardware, refer to the *Cyclone V GT FPGA Development Board Reference Manual*.
- For the latest board design files and reference designs, refer to the *Cyclone V GT FPGA Development Kit* page.
- For additional daughter cards available for purchase, refer to the *Development Board Daughter cards* page.
- For the Cyclone V GT device documentation, refer to the *Cyclone V FPGA and SoC FPGA* page.
- For Cyclone V GT or CAD symbols, refer to the *Cyclone V CIS SYMBOLS* page.
- For Nios II 32-bit embedded processor solutions, refer to the *Cyclone V Embedded processing* page.

### Related Information

- [Cyclone V GT FPGA Development Board Reference Manual](#)
- [Cyclone V GT FPGA Development Kit](#)
- [Development Board Daughter Cards](#)
- [Cyclone V FPGA and SoC FPGAs](#)
- [Cyclone V CIS SYMBOLS](#)
- [Cyclone V Embedded Processing](#)

## 3. Software Installation

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This chapter explains how to install the following softwares:

- Intel Quartus Prime Subscription Edition software
- Cyclone V GT FPGA Development Kit software
- On-Board Intel FPGA Download Cable II driver

### 3.1. Installing the Intel Quartus Prime Subscription Edition Software

The following are included in Intel Quartus Prime Subscription Edition software:

- Intel Quartus Prime software (including Platform Designer (Standard))
- Nios II EDS
- Intel FPGA IP Library

Following are the steps to install the Intel development tools:

1. Download the Intel Quartus Prime Subscription Edition Software from the *Intel Quartus Prime Web Edition Design Software Version 13.1 for Windows* page of the Intel website. Alternatively, you can request a DVD from the *Intel Quartus Prime Design Software* page of the Intel website.
2. Follow the on-screen instructions to complete the installation process. Choose an installation directory that is relative to the Intel Quartus Prime software installation directory.

If you have difficulty installing the Intel Quartus Prime software, refer to the *Intel FPGA Software Installation and Licensing*.

#### Related Information

- [Intel Quartus Prime Web Edition Design Software Version 13.1 for Windows](#)
- [Intel Quartus Prime Design Software](#)
- [Intel FPGA Software Installation and Licensing](#)

### 3.2. Activating Your License

Purchasing this kit entitles you to a one-year license for the Development Kit Edition (DKE) of the Intel Quartus Prime software.

After one year, your DKE license will no longer be valid and you will not be permitted to use this version of the Intel Quartus Prime software. To continue using the Intel Quartus Prime software, you should download the free Intel Quartus Prime Web Edition or purchase a subscription to Intel Quartus Prime software.



Before using the Intel Quartus Prime software, you must activate your license, identify specific users and computers, and obtain and install a license file.

If you already have a licensed version of the subscription edition, you can use that license file with this kit. If not, follow these steps:

1. Log on at the [MyIntel Account Sign In](#) webpage, and click **Sign In**.
2. On the MyIntel Home web page, click the **Self-Service Licensing Center** link.
3. Locate the serial number printed on the side of the development kit box below the bottom bar code. The number consists of alphanumeric characters and does not contain hyphens: for example, 5xxxSoCxxxxxxx.
4. On the Self-Service Licensing Center web page, click the *Find it with your License Activation Code* link.
5. In the **Find/Activate Products** dialog box, enter your development kit serial number and click **Search**.
6. When your product appears, turn on the check box next to the product name.
7. Click **Activate Selected Products**, and click **Close**.
8. When licensing is complete, Intel emails a `license.dat` file to you. Store the file on your computer and use the **License Setup** page of the **Options** dialog box in the Intel Quartus Prime software to enable the software.

To license the Intel Quartus Prime software, you need your computer's network interface card (NIC) ID, a number that uniquely identifies your computer. On the computer you use to run the Intel Quartus Prime software, type `ipconfig/all` at a command prompt to determine the NIC ID. Your NIC ID is the 12-digit hexadecimal number on the **Physical Address** line.

For complete licensing details, refer to the *Intel FPGA Software Installation and Licensing*.

#### Related Information

[Intel FPGA Software Installation and Licensing](#)

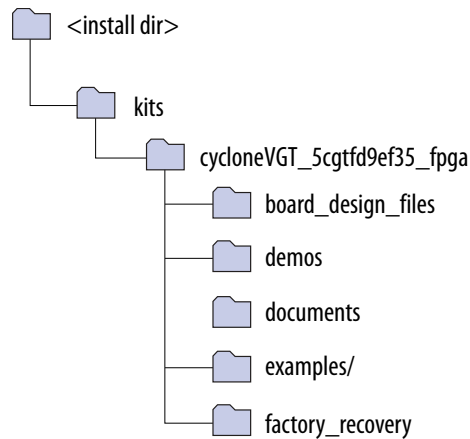
### 3.3. Installing the Development Kit

Following are the steps to install the development kit:

1. Download the Cyclone V GT FPGA Development Kit installer from the *Cyclone V GT FPGA Development Kit* page of the Intel website. Alternatively, you can request a development kit DVD from the Intel Kit Installations DVD Request Form page of the Intel website.
2. Unzip the installer package.

The installation program creates the **Cyclone V GT FPGA Development Kit** directory structure shown in the following figure.

**Figure 1. Cyclone V GT FPGA Development Kit Installed Directory Structure**  
(1)



The following table lists the file directory names and a description of their contents.

**Table 2. Installed Directory Contents**

Directory Name	Description of Contents
board_design_files	Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications.
documents	Contains the kit documentation.
examples	Contains the sample design files for the Cyclone V GT FPGA Development Kit.
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

#### Related Information

[Cyclone V GT FPGA Development Kit](#)

### 3.4. Installing the Intel FPGA Download Cable II Driver

The Cyclone V GT FPGA development board includes integrated Intel FPGA Download Cable circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the On-Board Intel FPGA Download Cable II driver on the host computer.

For installation instructions for the On-Board Intel FPGA Download Cable II driver, refer to the *Cable and Adapter Drivers Information* page of the Intel website.

#### Related Information

[Cable and Adapter Drivers Information](#)

(1) Early-release versions might have slightly different directory names.

## 4. Development Board Setup

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This chapter explains how to set up the Cyclone V GT FPGA development board and restore default settings.

### 4.1. Setting Up the Board

Following are the steps to configure and apply power to the board:

1. The FPGA development board ships with its board switches preconfigured to support the design examples in the kit. If your board might not be currently configured with the default settings, follow the instructions in *Factory Default Switch and Jumper Settings* before proceeding.
2. The FPGA development board ships with design examples stored in flash memory. Verify the SW4.3 DIP switch is set to the FACT ON (logic 0) position to load the design stored in the factory portion of flash memory.

The FPGA development board can be powered by the PCIe\* host adapter or the laptop power adapter. If you want to power the board by the PCIe host system, plug the FPGA development card into a standard PCIe connector. Alternatively, to power the FPGA development board using the laptop power adaptor, perform the following two steps:

1. Connect the +19 V (6.32 A) power supply to the DC Power Jack (J8) on the FPGA board and plug the cord into a power outlet.  
Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage, and a lower-rated power supply may not be able to provide enough power for the board.
2. Set the POWER switch (SW2) to the ON position. When power is supplied to the board, blue LED (D21) illuminates indicating that the board has power.

The MAX<sup>®</sup> V device on the board contains (among other things) a parallel flash loader (PFL) megafunction. When the board powers up, the PFL reads a design from flash memory and configures the FPGA. The SW4.3 DIP switch controls which design to load. When the switch is in the FACT ON (logic 0) position, the PFL loads the design from the factory portion of flash memory.

The MAX V design resides in the `<install_dir>\kits  
\cycloneVGT_5cgtfd9ef35_fpga\examples\max5` directory.

When configuration is complete, the Config Done LED (D7) illuminates, signaling that the Cyclone V GT device configured successfully.

For more information about the PFL megafunction, refer to the *Parallel Flash Loaded Megafunction User Guide*.

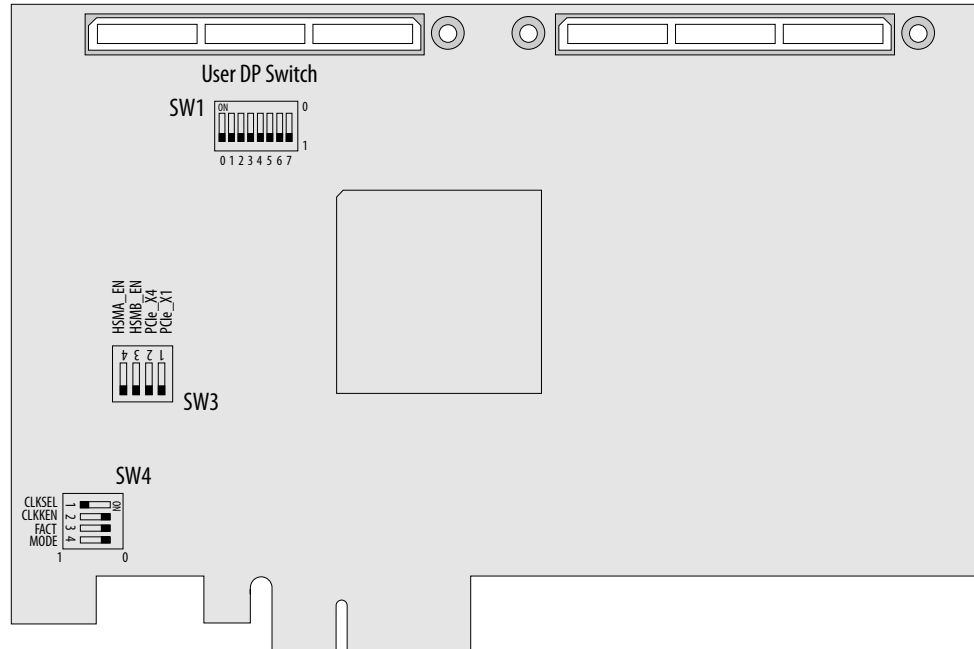
### Related Information

Factory Default Switch and Jumper Settings on page 12

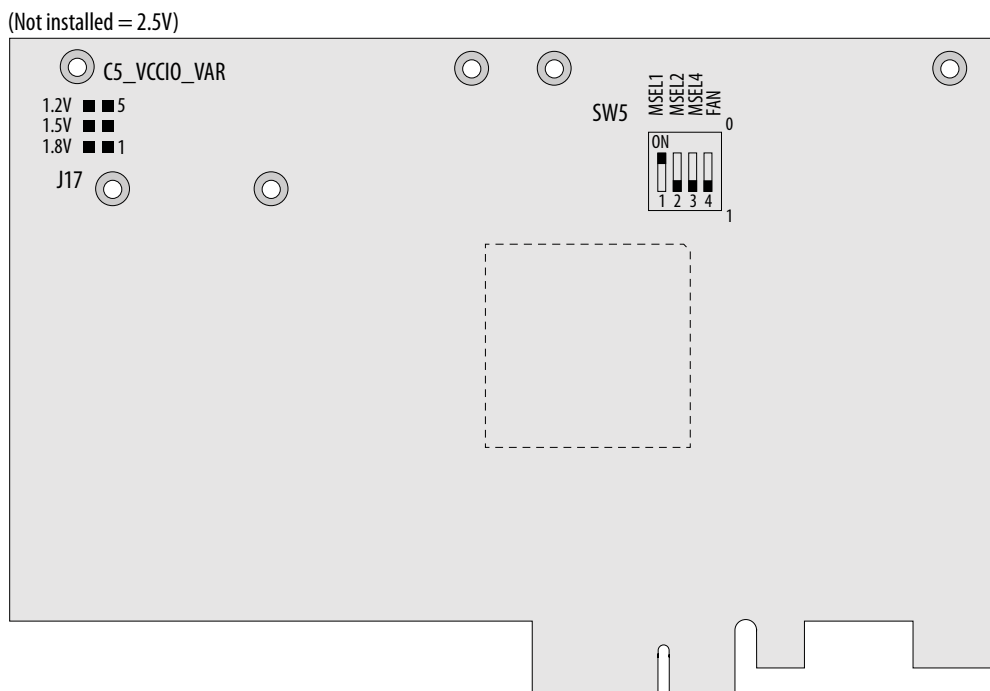
## 4.2. Factory Default Switch and Jumper Settings

The following figure shows the default switch settings for the top side of the Cyclone V GT FPGA development board.

**Figure 2. Default Switch Settings on the Board Top**



The following figure shows the default switch and jumper settings for the bottom side of the Cyclone V GT FPGA development board.

**Figure 3. Default Switch Settings on the Board Bottom**

**Note:** The following tables do not describe user DIP switches.

To restore the switches to the default settings, perform the following:

1. Set the DIP switch bank (SW3) to match *SW3 DIP Switch Settings* table and *Default Switch Settings on the Board Top* figure.

**Table 3. SW3 DIP Switch Settings**

Switch	Board Label	Function	Default Position
1	PCIe_X1	Switch1 has the following options: <ul style="list-style-type: none"> <li>ON (logical 0) = x1 presence detect is enabled.</li> <li>OFF (logical 1) = x1 presence detect is disabled.</li> </ul>	ON
2	PCIe_X4	Switch2 has the following options: <ul style="list-style-type: none"> <li>ON (logical 0) = x4 presence detect is enabled.</li> <li>OFF (logical 1) = x4 presence detect is disabled.</li> </ul>	ON
3	HSMB_EN	Switch 3 has the following options: <ul style="list-style-type: none"> <li>ON (logical 0) = HCMC Port B not in JTAG chain.</li> <li>OFF (logical 1) = Include HCMC Port B in the JTAG chain.</li> </ul>	ON
4	HSMA_EN	Switch 4 has the following options: <ul style="list-style-type: none"> <li>ON (logical 0) = HCMC Port A not in JTAG chain.</li> <li>OFF (logical 1) = Include HCMC Port A in the JTAG chain.</li> </ul>	ON

2. Set the DIP switch bank (SW4) to match *SW4 DIP Switch Settings* table and *Default Switch Settings on the Board Top* figure.

**Table 4. SW4 DIP Switch Settings**

Switch	Board Label	Function	Default Position
1	CLKSEL	Switch 1 has the following options: <ul style="list-style-type: none"> <li>ON (logical 0) = SMA input clock select.</li> <li>OFF (logical 1) = Programmable oscillator clock select.</li> </ul>	OFF
2	CLKEN	—	ON
3	FACT	Switch 3 has the following options: <ul style="list-style-type: none"> <li>ON (logical 0) = Load the factory design from flash at power up.</li> <li>OFF (logical 1) = Load the user design from flash at power up.</li> </ul>	ON
4	MODE	Switch 4 is an optional user switch setting. It is not currently defined in the MAX V system controller.	ON

- Set the DIP switch bank (SW5) to match *SW5 DIP Switch Settings* table and *Default Switch Settings on the Board Bottom* figure.

**Table 5. SW5 DIP Switch Settings**

Switch	Board Label	Function	Default Position
1	MSEL1	Switch 1 has the following options: <ul style="list-style-type: none"> <li>When ON, a logic 0 is selected.</li> <li>When OFF, a logic 1 is selected.</li> </ul>	ON
2	MSEL2	Switch 2 has the following options: <ul style="list-style-type: none"> <li>When ON, a logic 0 is selected.</li> <li>When OFF, a logic 1 is selected.</li> </ul>	OFF
3	MSEL4	Switch 3 has the following options: <ul style="list-style-type: none"> <li>When ON, a logic 0 is selected.</li> <li>When OFF, a logic 1 is selected.</li> </ul>	OFF
4	FAN	Switch 4 has is an optional user switch setting. It is not currently defined in the MAX V system controller.	OFF

For more information on the MSEL modes, refer to *Cyclone V Device Handbook: Volume 1: Device Interfaces and Integration*.

- Set the J17 jumper block to match *J17 Jumper Block* table and *Default Switch Settings on the Board Bottom* figure. The C5\_VCCIO\_VAR power rail provides the voltage to bank 7, which connects to the HSMB interface. By default this rail is 2.5 V. If needed, you can change the voltage level of this power supply by adding in a jumper wire between the pins of J17 as indicated in *J17 Jumper Block* table and *Default Switch Settings on the Board Bottom* figure.

**Table 6. J17 Jumper Block**

*Note:* Adding a single jumper between the pins sets the voltage as described in the table. Install only one jumper location at a time.

Jumper	C5_VCCIO_VAR	Default Position
Pins 1-2	1.8 V	Not installed
Pins 3-4	1.5 V	Not installed
Pins 5-6	1.2 V	Not installed

For more information about the FPGA board settings, refer to the *Cyclone V GT FPGA Development Board Reference Manual*.

#### Related Information

- [Cyclone V Device Handbook: Volume 1: Device Interfaces and Integration](#)
- [Cyclone V GT FPGA Development Board Reference Manual](#)

### 4.3. Configuring the MAX V Device to Program EPCQ

It is possible to configure the FPGA from the EPCQ device. However, the MAX V design provided with the Cyclone V GT FPGA development kit does not allow you to store a design in the EPCQ configuration device.

To enable FPGA configuration using the EPCQ device, reconfigure the MAX V device with the design file found at [How do I access the EPCQ configuration device on the Cyclone V GT FPGA Development Kit?](#).

### 4.4. Restoring the MAX V CPLD to the Factory Settings

This section describes how to restore the original factory contents to the MAX V CPLD on the FPGA development board. Make sure you have the Nios II EDS installed, and perform the following steps:

1. Set the board switches to the factory default settings described in *Factory Default Switch and Jumper Settings*.
2. Start the Intel Quartus Prime Programmer.
3. Click **Auto Detect**.
4. Click **Add File** for the 5M2210 MAX V device and select `<install_dir>\kits\cycloneVGT_5cgtfd9ef35_fpga\factory_recovery\max5.pof`.
5. Turn on the **Program/Configure** option for the added file.
6. Click **Start** to download the selected configuration file to the MAX V CPLD. Configuration is complete when the progress bar reaches 100%.

To ensure that you have the most up-to-date factory restore files and information about this product, refer to the *Cyclone V GT FPGA Development Kit* page of the Intel website.

#### Related Information

- [Factory Default Switch and Jumper Settings](#) on page 12
- [Cyclone V GT FPGA Development Kit](#)

## 4.5. Restoring the Flash Device to the Factory Settings

This section describes how to restore the original factory contents to the flash memory device on the FPGA development board. Make sure you have the Nios II EDS installed, and perform the following steps:

1. Set the board switches to the factory default settings described in *Factory Default Switch and Jumper Settings*.
2. Start the Intel Quartus Prime Programmer to configure the FPGA with a .sof capable of flash programming. For more information, refer to *Configuring the FPGA Using the Intel Quartus Prime Programmer*.
3. Click **Add File** and select <install\_dir>\kits\cycloneVGT\_5cgtfd9ef35\_fpga\factory\_recovery\c5gt\_fpga\_bup.sof.
4. Turn on the **Program/Configure** option for the added file.
5. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%. The Config Done LED (D7) illuminates indicating that the flash device is ready for programming.
6. On the Windows Start menu, click **All Programs > intelFPGAxxxxx > Nios II Command Shell**.
7. In the Nios II command shell, navigate to the <install\_dir>\kits\cycloneVGT\_5cgtfd9ef35\_fpga\factory\_recovery directory and type the following command to run the restore script:

```
./restore.sh
```

Restoring the flash memory might take several minutes. Follow any instructions that appear in the Nios II command shell.

8. After all flash programming completes, if powered by the laptop power adapter, cycle the POWER switch (SW2) off then on. If the FPGA development board is powered by PCIe host, cycle the host power.
9. Using the Intel Quartus Prime Programmer, click **Add File** and select <install\_dir>\kits\cycloneVGT\_5cgtfd9ef35\_fpga\factory\_recovery\c5gt\_fpga\_bup.sof.
10. Turn on the **Program/Configure** option for the added file.
11. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%. The Config Done LED (D7) illuminates indicating the flash memory device is now restored with the factory contents.
12. After all flash programming completes, if powered by the laptop power adapter, cycle the POWER switch (SW2) off then on. If the FPGA development board is powered by PCIe host, cycle the host power.
13. In the Nios II command shell, type the following Nios II EDS command:

```
./restore.sh
```

14. Do not remove board\_information and MAC address. The restore script cannot restore them. They can not be recovered if be removed.



To ensure that you have the most up-to-date factory restore files and information about this product, refer to the *Cyclone V GT FPGA Development Kit* page of the Intel website.

#### Related Information

- [Factory Default Switch and Jumper Settings](#) on page 12
- [Configuring the FPGA Using the Intel Quartus Prime Programmer](#) on page 17
- [Cyclone V GT FPGA Development Kit](#)

## 4.6. Configuring the FPGA Using the Intel Quartus Prime Programmer

You can use the Intel Quartus Prime Programmer to configure the FPGA with a specific SRAM Object File (.sof). Verify the following conditions, before configuring the FPGA:

- Intel Quartus Prime Programmer and the Intel FPGA Download Cable II driver are installed on the host computer.
- USB cable is connected to the FPGA development board.
- Power to the board is on.
- No other applications that use the JTAG chain are running.

To configure the Cyclone V GT FPGA, do the following:

1. Start the Intel Quartus Prime Programmer.
2. Click **Auto Detect** to display the devices in the JTAG chain.
3. Click **Add File** and select the path to the desired .sof.
4. Turn on the **Program/Configure** option for the added file.
5. Click **Start** to download the selected file to the FPGA. Configuration is complete when the progress bar reaches 100%.

Using the Intel Quartus Prime programmer to configure a device on the board causes other JTAG-based applications to lose their connection to the board. Restart those applications after configuration is complete.

If the Intel Quartus Prime programming window is already open and you power cycle the board, to detect the JTAG chain, do the following:

- Click **Hardware Setup** in the Intel Quartus Prime Programmer window.
- Reselect Intel FPGA Download Cable II.

## 5. Board Update Portal

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This chapter explains how you can connect to the Board Update Portal and use it to upload your own designs.

The Cyclone V GT FPGA Development Kit ships with the Board Update Portal design example stored in the factory portion of the flash memory on the board. The design consists of a Nios II embedded processor, an Ethernet MAC, and an HTML web server.

When you power up the board with the SW4.3 DIP switch in the FACT ON (logic 0) position, the FPGA configures with the Board Update Portal design example. The design can obtain an IP address from any DHCP server and serve a web page from the flash on your board to any host computer on the same network. The web page allows you to upload new FPGA designs to the user hardware 1 portion of flash memory and provides useful kit-specific links and design resources.

After successfully updating the user hardware 1 flash memory, you can load a design from flash memory into the FPGA. To do so, set the SW4.3 DIP switch to the FACT OFF (logic 1) position and power cycle the board.

The source code for the Board Update Portal design resides in the `<install_dir>\kits\cycloneVGT_5cgtfd9ef35_fpga\examples` directory.

### 5.1. Connecting to the Board Update Portal Web Page

To connect to the Board Update Portal web page, ensure that you have the following items setup and installed:

- A PC with a connection to a working Ethernet port on a DHCP enabled network.
- A separate working Ethernet port connected to the same network for the board.
- The Ethernet and power cables that are included in the kit.

To connect to the Board Update Portal web page, perform the following:

1. With the board powered down, set the SW4.3 DIP switch to the FACT ON (logic 0) position.
2. Attach the Ethernet cable from the board to your LAN.
3. Power up the board. The board connects to the LAN's gateway router and obtains an IP address. The LCD on the board displays the IP address.
4. Start a web browser on a PC that is connected to the same network, and enter the IP address from the LCD into the browser address bar. The Board Update Portal web page appears in the browser.

You can click *Cyclone V GT FPGA Development Kit* on the Board Update Portal web page to access the kit's home page for documentation updates and additional new designs.

You can also navigate directly to the *Cyclone V GT FPGA Development Kit* page of the Intel website to determine if you have the latest kit software.

#### Related Information

[Cyclone V GT FPGA Development Kit](#)

## 5.2. Using the Board Update Portal to Write User Designs

The Board Update Portal allows you to write new designs to the user hardware 1 portion of flash memory. Designs must be in the Nios II Flash Programmer File (.flash) format. However, if you have generated a SRAM Object File (.sof) that operates without a software design file, you can still use the Board Update Portal to upload your design. In this case, leave the **Software File Name** field blank.

Design files available from the *Cyclone V GT FPGA Development Kit* page include .flash files. You can also create .flash files from your own custom design. Refer to *Preparing to Run the Board Test System* for information about preparing your own design for upload.

To upload a design over the network into the user portion of flash memory on your board, do the following:

1. Perform the steps in *Connecting to the Board Update Portal Web Page* to access the Board Update Portal web page.
2. In the **Hardware File Name** field, specify the .flash file that you either downloaded from the Intel website or created on your own. If there is a software component to the design, specify it in the same manner using the **Software File Name** field. Otherwise, leave the **Software File Name** field blank.
3. Click **Upload** and then wait for the files to write to flash memory. A progress bar indicates the percent complete.
4. To configure the FPGA with the new design, set the SW4.3 DIP switch to the FACT OFF (logic 1) position and power cycle the board.

As long as you do not overwrite the factory image in the flash memory device, you can continue to use the Board Update Portal to write new designs to the user hardware 1 portion of flash memory. If you do overwrite the factory image, you can restore it by following the instructions in *Restoring the Flash Device to the Factory Settings*.

#### Related Information

- [Cyclone V GT FPGA Development Kit](#)
- [Preparing to Run the Board Test System](#) on page 21
- [Connecting to the Board Update Portal Web Page](#) on page 18
- [Restoring the Flash Device to the Factory Settings](#) on page 16

## 6. Board Test System

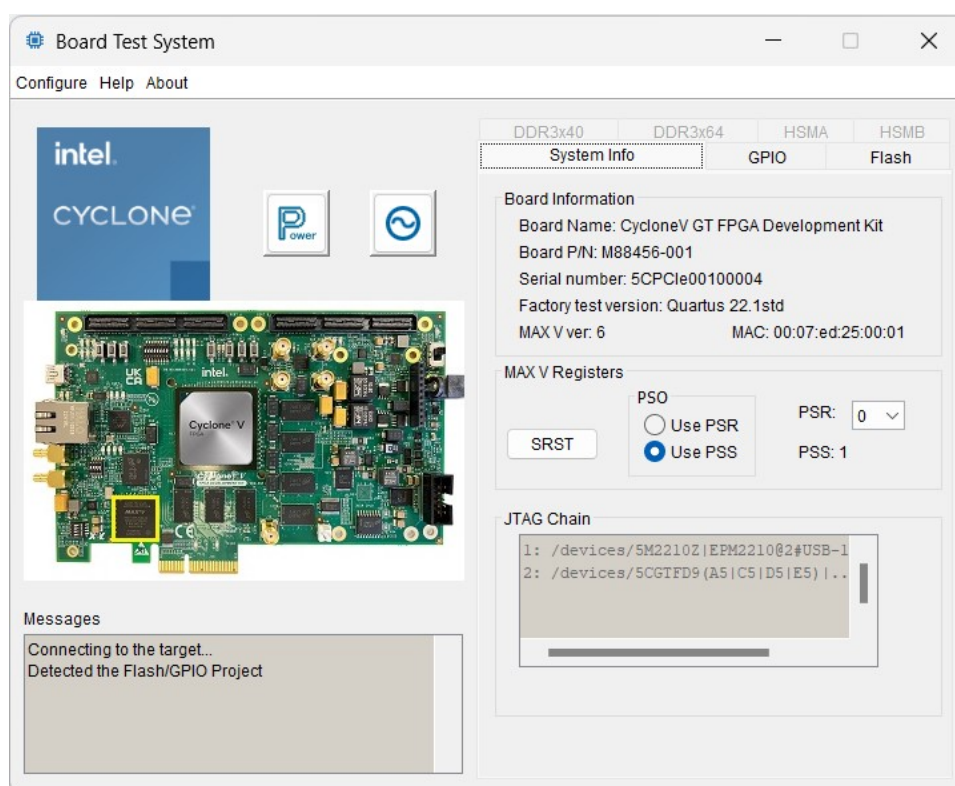
This chapter explains how you can use the Board Test System GUI to test board components, modify functional parameters, observe performance, and measure power usage.

Along with the Board Test System, the development kit includes related design examples. These designs are provided to test the major board features. Each design provides data for one or more tabs in the application. While using the Board Test System, you must reconfigure the FPGA several times with test designs specific to the functionality you are testing.

The Board Test System is also useful as a reference for designing systems.

The following figure shows the GUI and initial **System Info** tab for a board in the factory configuration.

**Figure 4. Board Test System GUI**



Highlights appear in the board picture around the corresponding components.

The Board Test System and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the Signal Tap II Embedded Logic Analyzer. As the Intel Quartus Prime programmer uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time out. You must ensure to close the other applications before attempting to reconfigure the FPGA using the Intel Quartus Prime Programmer.

## 6.1. Preparing to Run the Board Test System

With the power to the board off, perform the following steps:

1. Connect the USB cable to the board.
2. Ensure that the Ethernet patch cord is plugged into the RJ45 connector.
3. Ensure that the development board switches and jumpers are set to the default positions as shown in the *Factory Default Switch and Jumper Settings*.
4. Set the SW4.3 DIP switch to the FACT OFF (logic 1) position.
5. To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The application cannot run correctly unless the USB cable is attached and the board is on.

### Related Information

[Factory Default Switch and Jumper Settings](#) on page 12

## 6.2. Running the Board Test System

To run the Board Test System, make sure you have first installed the software. Follow the steps in *Installing the Development Kit*.

You can start the Board Test System with the following:

- The BoardTestSystem.exe application that resides in <install\_dir>\kits\cycloneVGT\_5cgtfd9ef35\_fpga\examples\board\_test\_system directory.

Once the Board Test System application GUI appears, it displays the application tab that corresponds to the design running in the FPGA. The board's flash memory ships preconfigured with the design that corresponds to the **System Info**, **GPIO**, **Flash** tabs.

### Related Information

[Installing the Development Kit](#) on page 9

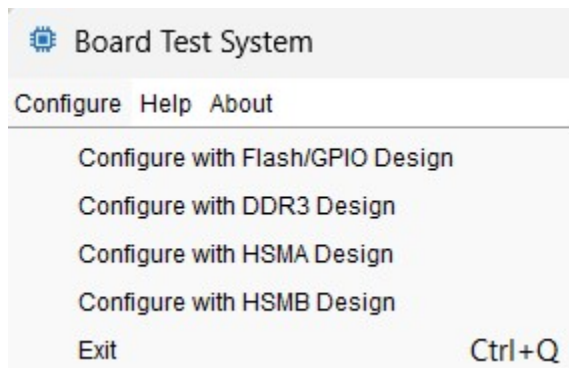
## 6.3. Using the Board Test System

This section describes the menus and controls on the Board Test System application.

### 6.3.1. The Configure Menu

Use the Configure menu as shown on the following figure to select the design you want to use. Each design example on this menu tests different board features that corresponds to one or more application tabs. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

**Figure 5. The Configure Menu**



To configure the FPGA with a test system design, perform the following:

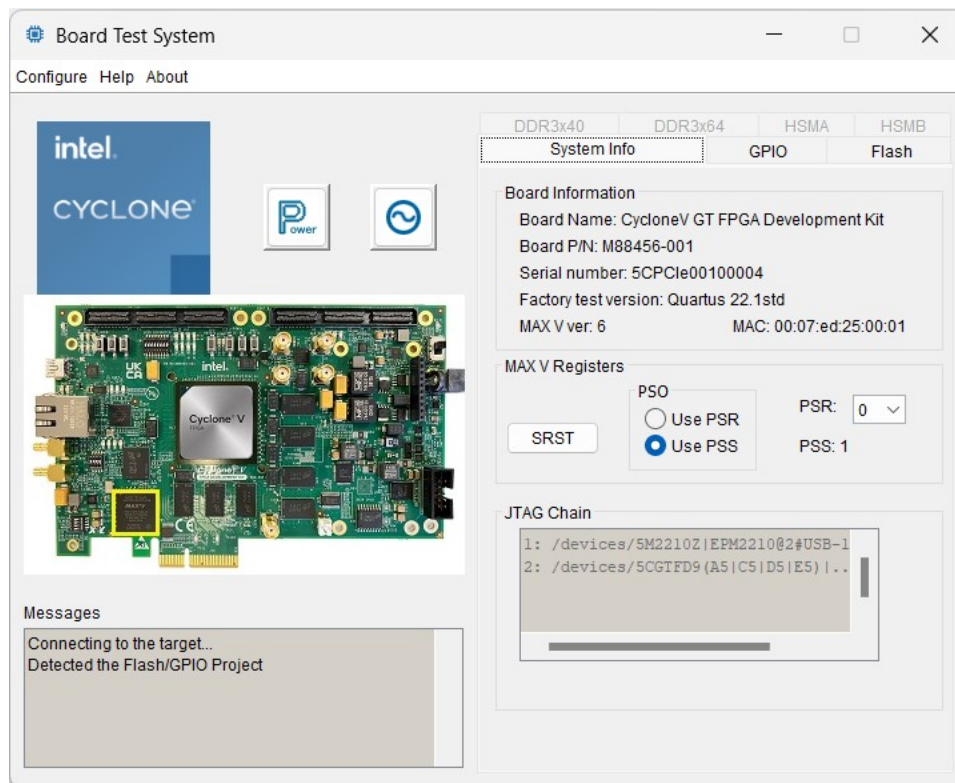
1. On the Configure menu, click the configure command that corresponds to the functionality you wish to test.
2. When configuration finishes, close the Intel Quartus Prime Programmer if open. The design begins running in the FPGA. The corresponding GUI application tabs that interface with the design are now enabled.

If the Board Test System application is open while you configure FPGAs with the Intel Quartus Prime Programmer, you may need to restart the Board Test System.

### 6.3.2. The System Info Tab

The **System Info** tab displays the board's current configuration and allows you to change MAX V register values. The following figure shows the **System Info** tab with the MAX V highlighted in the photograph.

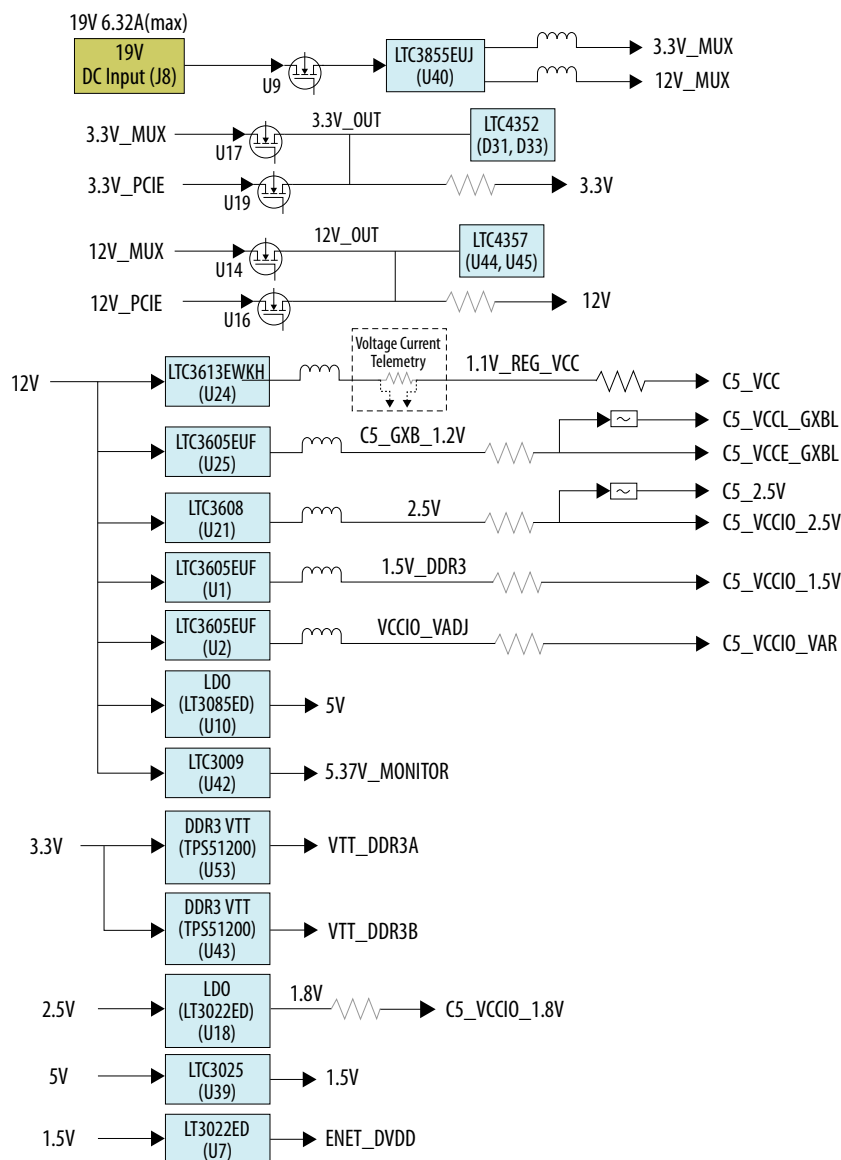
Figure 6. The System Info Tab



The following sections describe the controls on the **System Info** tab.

### 6.3.2.1. Power Tree

Figure 7. Power Tree Diagram (DK-DEV-5CGTD9N-B)



### 6.3.2.2. Power Monitor

Clicking this control starts the Power Monitor application that measures and reports current power information for the board. As the application communicates over the JTAG bus to the MAX V device, you can measure the power of any design in the FPGA, including your own designs. For more information, refer to *The Power Monitor* section.

#### Related Information

[The Power Monitor](#) on page 37



### 6.3.2.3. Board Information

This group control displays static information about your board:

- **Board name**—Indicates the official name of the board.
- **Board P/N**—Indicates the part number of the board.
- **Serial number**—Indicates the serial number of the board.
- **Factory test version**—Indicates the version of the Board Test System currently running on the board.
- **MAX V ver**—Indicates the version of MAX V code currently running on the board. The MAX V code resides in the `<install_dir>\kits\cycloneVGT_5cgtfd9ef35_fpga\examples` directory.  
Newer revisions of this code might be available on the *Cyclone V GT FPGA Development Kit* page of the Intel website.
- **MAC**—Indicates the MAC address of the board.

#### Related Information

[Cyclone V GT FPGA Development Kit](#)

### 6.3.2.4. MAX V Registers

The **MAX V registers** control allows you to view and change the current MAX V register values as described in the following table. Changes to the register values with the GUI take effect immediately. For example, writing a 0 to SRST resets the board.

**Table 7. MAX V Registers**

Register Name	Read/Write Capability	Description
System Reset (SRST)	Write only	Set to 0 to initiate an FPGA reconfiguration.
Page Select Register (PSR)	Read/Write	Determines which of the up to three (0-2) pages of flash memory to use for FPGA reconfiguration. The flash memory ships with pages 0 and 1 preconfigured.
Page Select Override (PSO)	Read/Write	When set to 0, the value in PSR determines the page of flash memory to use for FPGA reconfiguration. When set to 1, the value in PSS determines the page of flash memory to use for FPGA reconfiguration.
Page Select Switch (PSS)	Read only	Holds the current value of the illuminated PGM LED (D2-D4) based on the following encoding: <ul style="list-style-type: none"> <li>• 0 = PGM LED (D14) and corresponds to the flash memory page for the factory hardware design.</li> <li>• 1 = PGM LED (D13) and corresponds to the flash memory page for the user hardware 1 design.</li> <li>• 2 = PGM LED (D12) and corresponds to the flash memory page for the user hardware 2 design.</li> </ul>

- **PSO**—Sets the MAX V PSO register. The following options are available:
  - **Use PSR**—Allows the PSR to determine the page of flash memory to use for FPGA reconfiguration.
  - **Use PSS**—Allows the PSS to determine the page of flash memory to use for FPGA reconfiguration.
- **PSR**—Sets the MAX V PSR register. The numerical value in the list corresponds to the page of flash memory to load during FPGA reconfiguration. Refer to the *MAX V Registers* table above for more information.
- **PSS**—Displays the MAX V PSS register value. Refer to *MAX V Registers* table for the list of available options.
- **SRST**—Resets the system and reloads the FPGA with a design from flash memory based on the other MAX V register values. Refer to *MAX V Registers* table for more information.

As the **System Info** tab requires that a specific design is running in the FPGA at a specific clock speed, writing a 0 to SRST or changing the PSO value can cause the Board Test System to stop running.

### 6.3.2.5. JTAG Chain

This control shows all the devices currently in the JTAG chain. The Cyclone V GT device is always the first device in the chain. The JTAG chain is normally mastered by the On-board Intel FPGA Download Cable II.

If you plug in an external download cable to the JTAG header (J13), the On-Board Intel FPGA Download Cable II is disabled.

JTAG DIP switch bank (SW3) selects which interfaces are in the chain. Refer to [Table 3](#) on page 13 table for detailed settings.

For details on the JTAG chain, refer to the *Cyclone V GT FPGA Development Board Reference Manual*. For Intel FPGA Download Cable II configuration details, refer to the *On-Board Intel FPGA Download Cable II User Guide* page.

#### Related Information

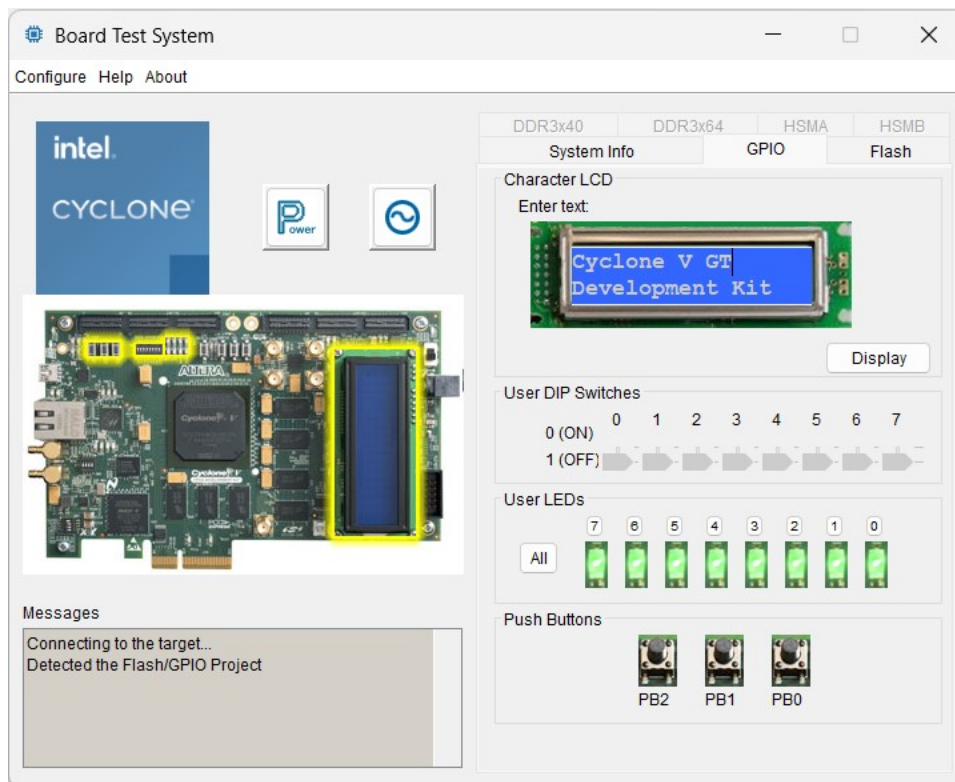
- [Cyclone V GT FPGA Development Board Reference Manual](#)
- [Intel FPGA Download Cable II User Guide](#)

### 6.3.3. The GPIO Tab

The **GPIO** tab allows you to interact with all the general purpose user I/O components on your board. You can write to the character LCD, read DIP switch settings, turn LEDs on or off, and detect push button presses. The following figure shows the **GPIO** tab.

**Figure 8. The GPIO Tab**

**Note:** The picture of the development kit is only a reference and might be different from the latest one.



The following sections describe the controls on the **GPIO** tab.

#### 6.3.3.1. Character LCD and Display

The **Character LCD** controls allow you to type in text strings that appear on the character LCD on your board after clicking **Display**.

If you exceed the 16 character display limit on either line, a warning message appears.

#### 6.3.3.2. User DIP Switches

This control displays the current positions of the switches in the user DIP switch bank. Change the switches on the board to see the graphical display change accordingly.

#### 6.3.3.3. User LEDs

This control displays the current state of the user LEDs. Click the graphical representation of the LEDs to turn the board LEDs on and off. Click **All** to turn on and off all of the user LEDs at once.

### 6.3.3.4. Push Buttons

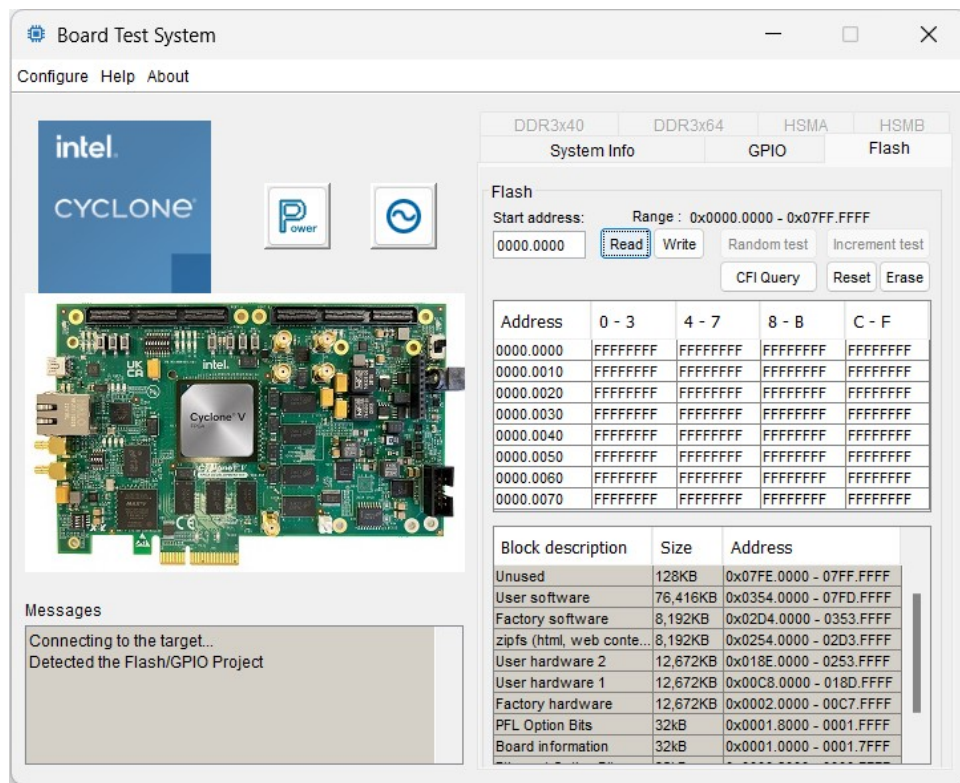
This control displays the current state of the board user push buttons. Press a push button on the board to see the graphical display change accordingly.

### 6.3.4. The Flash Tab

The **Flash** tab allows you to read and write flash memory on your board. The following figure shows the **Flash** tab.

**Figure 9. The Flash Tab**

*Note:* The picture of the development kit is only a reference and might be different from the latest one.



The following sections describe the controls on the **Flash** tab.

#### 6.3.4.1. Read and Start Address

The **Read** control reads the flash memory on your board. To see the flash memory contents, type a starting address in the **Start address** text box and click **Read**. Values starting at the specified address appear in the memory table on the **Flash** tab.

#### 6.3.4.2. Range

Range displays the entire range of the flash memory. If you enter an address outside of the flash memory address space, a warning message identifies the valid flash memory address range.

#### 6.3.4.3. Write

Writes the flash memory on your board. To update the flash memory contents:

- Type in values in the memory table cells.
- Press Enter, and click **Write**.

The application writes the new values to flash memory and then reads the values back to guarantee that the memory table accurately reflects the memory contents.

#### 6.3.4.4. CFI Query

Updates the memory table with the CFI ROM table contents from the flash memory.

#### 6.3.4.5. Reset

Starts the flash device's reset command and updates the memory table displayed on the **Flash** tab.

#### 6.3.4.6. Erase

Clears the `Unused` block of flash memory.

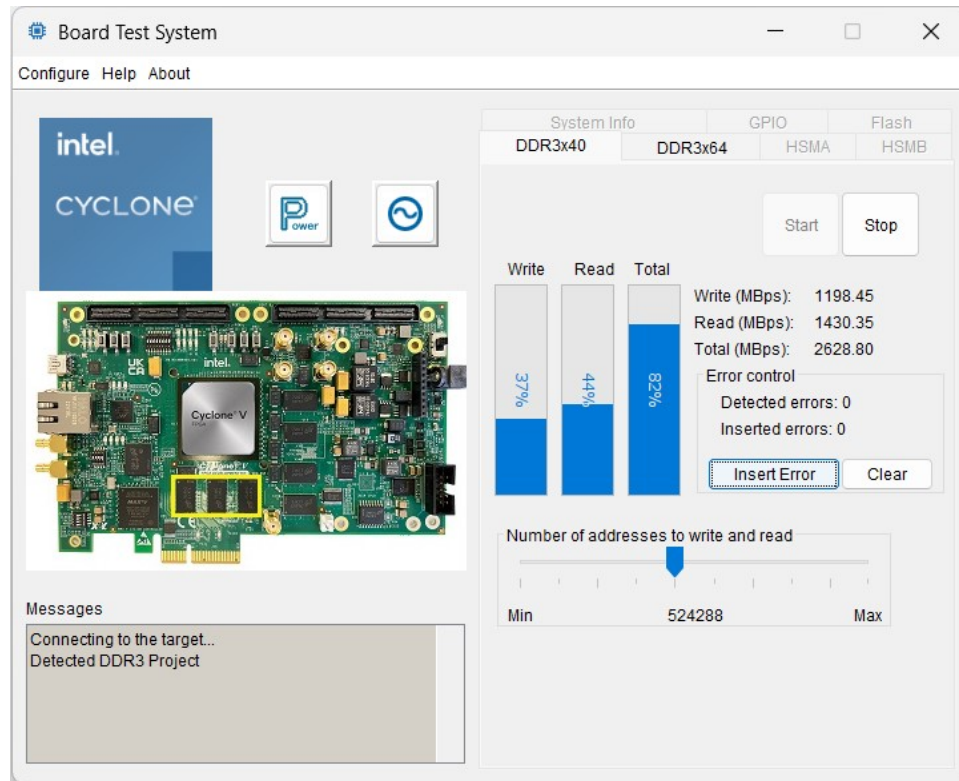
#### 6.3.4.7. Flash Memory Table and Flash Memory Map

The control starting with the **Address** column allows you to write data in each cell. The control underneath is read-only and displays the board's flash memory map.

### 6.3.5. The DDR3x40 and DDR3x64 Tabs

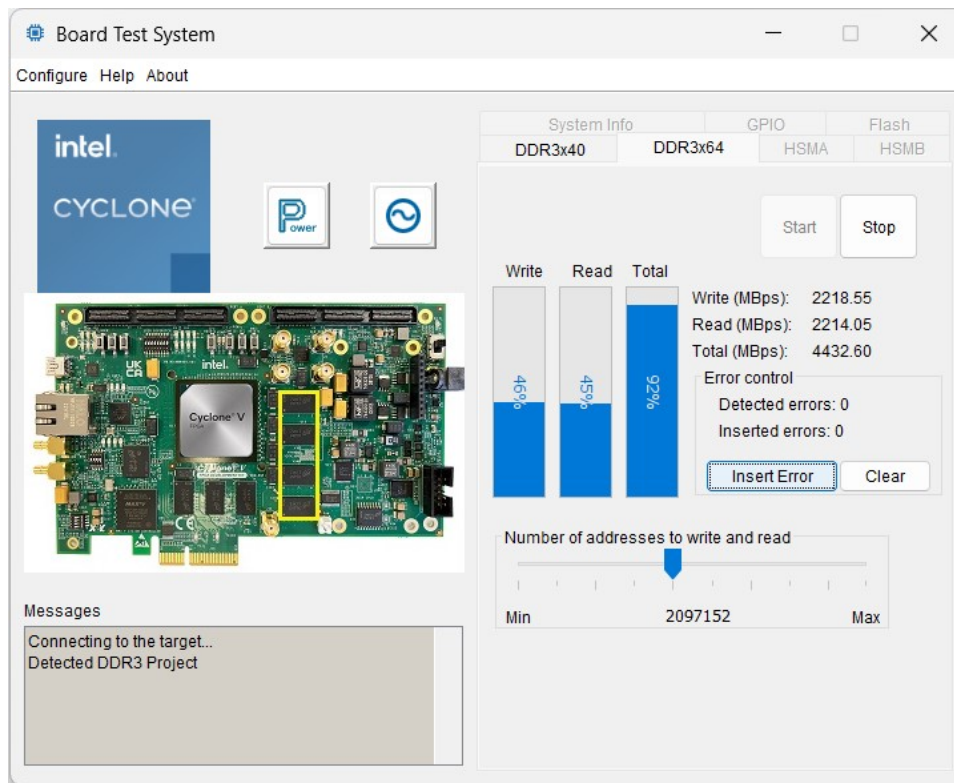
The **DDR3x40** and **DDR3x64** tabs allow you to read and write the DDR3 memory on your board. The following figure shows the **DDR3x40** tab.

Figure 10. The DDR3x40 Tab



The following figure shows the **DDR3x64** tab. Except for the tab name and photograph, this tab is identical to the **DDR3x40** tab.

Figure 11. The DDR3x64 Tab



The following sections describe the controls on the **DDR3x40** and **DDR3x64** tabs.

#### 6.3.5.1. Start

Initiates DDR3 memory transaction performance analysis.

#### 6.3.5.2. Stop

Terminates the transaction performance analysis.

#### 6.3.5.3. Performance Indicators

Display current transaction performance analysis information collected since you last clicked **Start**:

- **Write, Read, and Total** performance bars—Show the percentage of the maximum theoretical data rate that the requested transactions are able to achieve.
- **Write (MBps), Read (MBps), and Total (MBps)**—Show the number of bytes of data analyzed per second.
  - DDR3x40—The theoretical maximum bandwidth is 3200 MBps.
  - DDR3x64—The theoretical maximum bandwidth is 4800 MBps.



#### 6.3.5.4. Error Control

This group displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors**—Displays the number of data errors detected in the hardware.
- **Inserted Errors**—Displays the number of errors inserted into the transaction stream.
- **Insert Error**—Inserts a one-word error into the transaction stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.
- **Clear**—Resets the **Detected errors** and **Inserted errors** counters to zeros.

#### 6.3.5.5. Number of Addresses to Write and Read

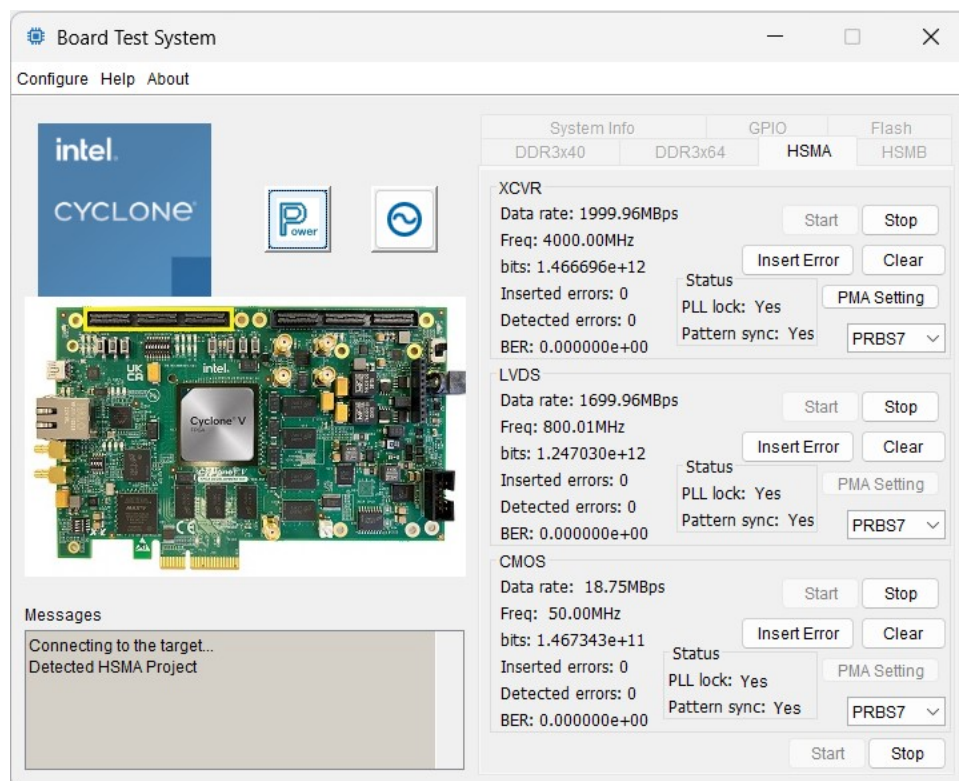
This control allows you to determine the number of addresses for each iteration of reads and writes.

#### 6.3.6. The HSMA Tab

**HSMA** stands for high-speed mezzanine card for Port A.

The **HSMA** tab as shown in the following figure allows you to perform loopback tests on the HSMA transceiver (XCVR), HSMA LVDS, and CMOS ports.

Figure 12. The HSMA Tab





You must have the loopback HSMA installed on the HSMC Port A connector for this test to work correctly.

The following sections describe the controls on the **HSMA** tab.

#### 6.3.6.1. Start, Stop

The **Start** and **Stop** controls at the bottom-right of this tab allow you to start and stop testing for all three ports.

#### 6.3.6.2. XCRV, LVDS, CMOS

The XCRV, LVDS, CMOS groups display the following status information during the loopback test:

**Data rate**—Displays the current data rate in megabytes per second (Mbps).

**Freq**—Displays the data rate frequency in MHz which is equivalent to Mbps.

**Bits**—Displays the number of bits transmitted since clicking **Start**.

**Inserted errors**—Displays the number of errors inserted by clicking **Insert Error** button.

**Detected errors**—Displays the number of bit errors detected by the error checking circuitry.

**BER**—Displays the bit error rate of the interface.

##### Status

- **PLL lock**—Displays Yes if the PLL is locked.
- **Pattern Sync**—Displays Yes if the receiver has detected the input data pattern.

**Start**—Starts the PRBS data test and begins to monitor and update screen with live test results.

**Stop**—Stops the PRBS data test.

**Insert Error**—Inserts an error into a data stream that is detected by the receiver when in loopback mode. With the **Insert Error**, there are differences among the three ports:

- **XCVR**—Inserts 4 errors at 1 click.
- **LVDS**—Inserts 3 errors at 1 click.
- **CMOS**—Inserts 1 error at 1 click.

**Clear**—Clears the **Detected errors** counter.

**PMA Setting**—Only available for the XCVR test. This control allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback**—Routes the selected TX output signal back to the RX input signal on-chip to verify operation without using an external loopback board.
- **VOD**—Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap**

- **Pre**—Not available.
  - **First post**—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
  - Second post**—Not available.
- **Equalizer**—Specifies the setting for the receiver equalizer.
- **DC gain**—Specifies the DC portion of the receiver equalizer.

**Data Type**—Specifies the type of data contained in the transactions. The following data types are available for analysis:

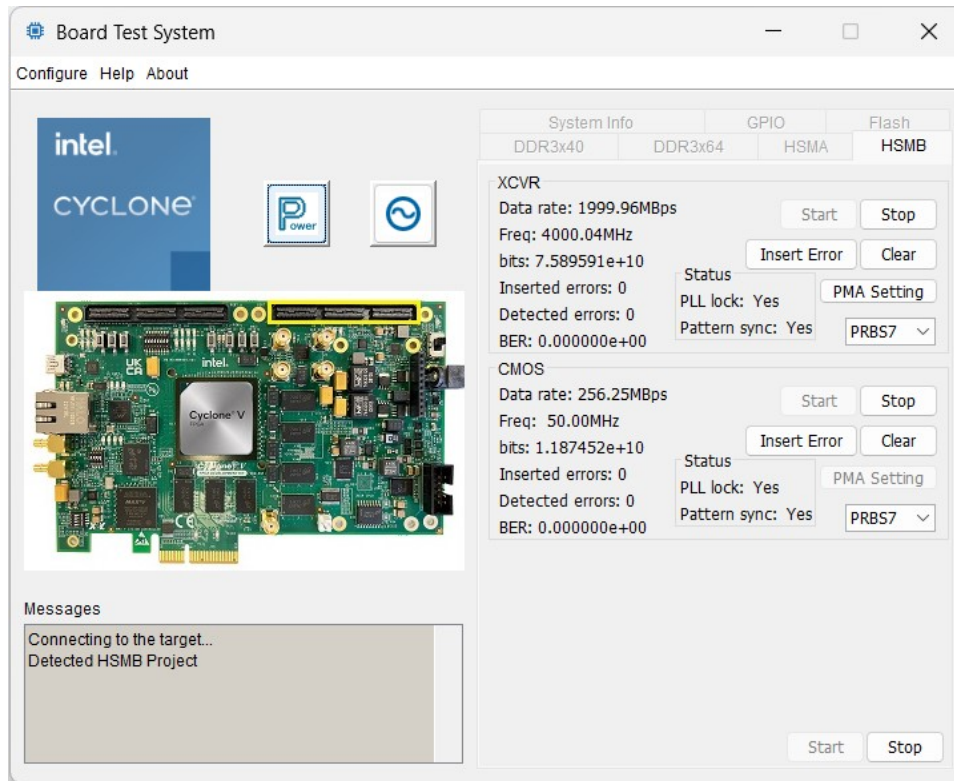
- **PRBS7**—Pseudo-random 7-bit sequences
- **PRBS15**—Pseudo-random 15-bit sequences
- **PRBS23**—Pseudo-random 23-bit sequences
- **PRBS31**—Pseudo-random 31-bit sequences
- **HF**—Highest frequency divide-by-4 data pattern 10101010
- **LF**—Lowest frequency divide-by-4 data pattern 11110000

### 6.3.7. The HSMB Tab

**HSMB** stands for high-speed mezzanine card for Port B.

The **HSMB** tab as shown in the following figure allows you to perform loopback tests on the HSMB transceiver (XCVR) and HSMB CMOS ports.

Figure 13. The HSMB Tab



You must have the loopback **HSMB** installed on the **HSMC** Port B connector for this test to work correctly.

The following sections describe the controls on the **HSMB** tab.

#### 6.3.7.1. Start, Stop

The **Start** and **Stop** controls at the bottom-right of this tab allow you to start and stop testing for all three ports.

#### 6.3.7.2. XCRV and CMOS

The XCRV and CMOS groups display the following status information during the loopback test:

**Data rate**—Displays the current data rate in megabytes per second (Mbps).

**Freq**—Displays the data rate frequency in MHz which is equivalent to Mbps.

**Bits**—Displays the number of bits transmitted since clicking **Start**.

**Inserted errors**—Displays the number of errors inserted by clicking **Insert Error** button.

**Detected errors**—Displays the number of bit errors detected by the error checking circuitry.

**BER**—Displays the bit error rate of the interface.

**Status**

- **PLL lock**—Displays Yes if the PLL is locked.
- **Pattern Sync**—Displays Yes if the receiver has detected the input data pattern.

**Start**—Starts the PRBS data test and begins to monitor and update screen with live test results.

**Stop**—Stops the PRBS data test.

**Insert Error**—Inserts an error into a data stream that is detected by the receiver when in loopback mode. With the **Insert Error**, there are differences among the three ports:

- **XCVR**—Inserts 4 errors at 1 click.
- **CMOS**—Inserts 1 error at 1 click.

**Clear**—Clears the **Detected errors** counter.

**PMA Setting**—Only available for the XCVR test. This control allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback**—Routes the selected TX output signal back to the RX input signal on-chip to verify operation without using an external loopback board.
- **VOD**—Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap**
- **Pre**—Not available.
  - **First post**—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
  - Second post**—Not available.
- **Equalizer**—Specifies the setting for the receiver equalizer.
- **DC gain**—Specifies the DC portion of the receiver equalizer.

**Data Type**—Specifies the type of data contained in the transactions. The following data types are available for analysis:

- **PRBS7**—Pseudo-random 7-bit sequences
- **PRBS15**—Pseudo-random 15-bit sequences
- **PRBS23**—Pseudo-random 23-bit sequences
- **PRBS31**—Pseudo-random 31-bit sequences
- **HF**—Highest frequency divide-by-4 data pattern 10101010
- **LF**—Lowest frequency divide-by-4 data pattern 11110000

## 6.4. The Power Monitor

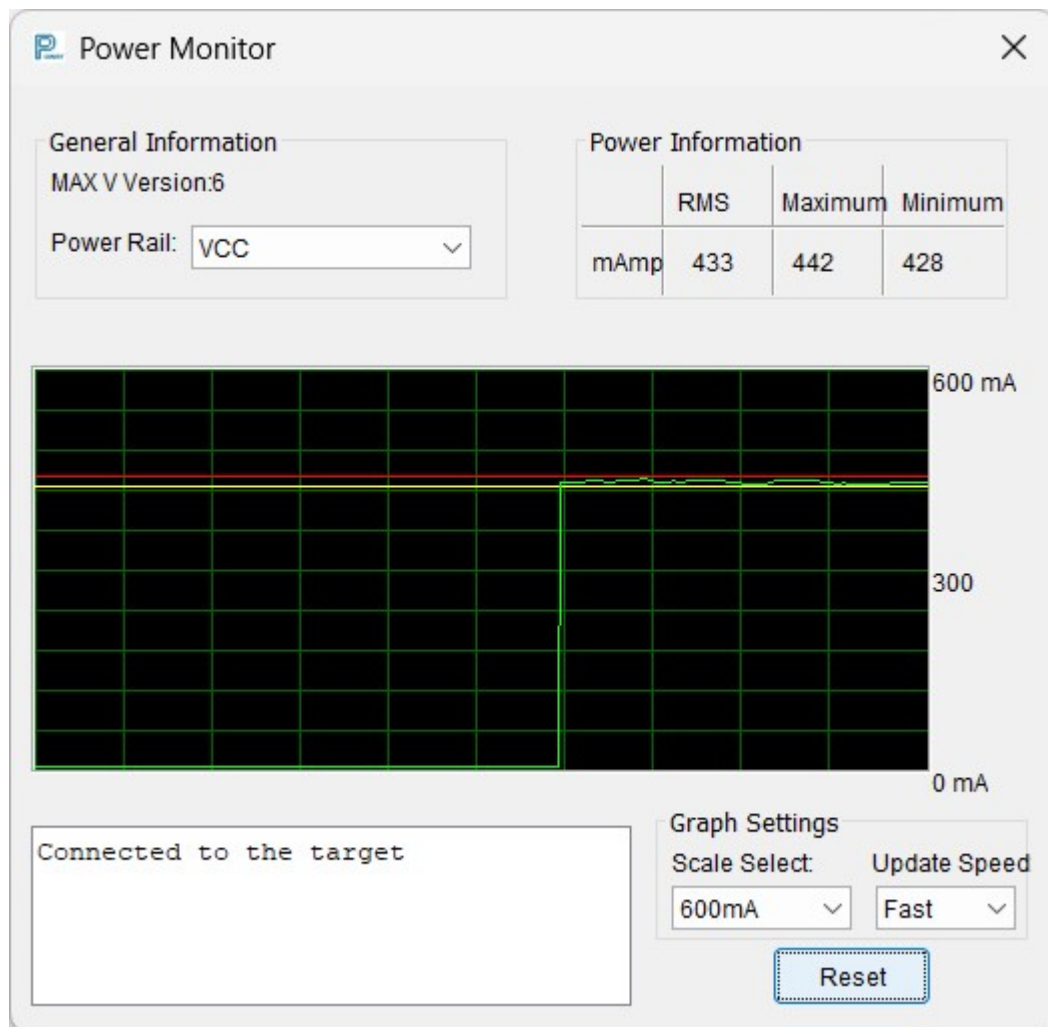
You can start the **Power Monitor** application with the following:

- The **Power Monitor** button on the Board Test System GUI.
- The **PowerMonitor.exe** application that resides in the <install\_dir>\kits\cycloneVGT\_5cgtfd9ef35\_fpga\examples\board\_test\_system directory.

### 6.4.1. Power Monitor Features

The Power Monitor measures and reports current power information and communicates with the MAX V device on the board through the JTAG bus. A power monitor circuit attached to the MAX V device allows you to measure the power that the Cyclone V GT FPGA is consuming. The following figure shows the Power Monitor.

Figure 14. The Power Monitor



## 6.4.2. Power Monitor Controls

The following sections describe the Power Monitor controls.

### 6.4.2.1. General Information

General Information displays the following information about the MAX V device:

- **MAX V version**—Indicates the version of MAX V code currently running on the board. The MAX V code resides in the <install\_dir>\kits\cycloneVGT\_5cgtfd9ef35\_fpga\examples\max5 directories.

Newer revisions of this code might be available on the *Cyclone V GT FPGA Development Kit* page of the Intel website.

- **Power rail**—Indicates the currently-selected power rail. After selecting the desired rail, click **Reset** to refresh the screen with updated board readings.

A table with the power rail information is available in the *Cyclone V GT FPGA Development Board Reference Manual*.

#### Related Information

- [Cyclone V GT FPGA Development Kit](#)
- [Cyclone V GT FPGA Development Board Reference Manual](#)

### 6.4.2.2. Power Information

Power information displays current, maximum, and minimum numerical power readings in mA.

### 6.4.2.3. Power Graph

Power Graph displays the mA power consumption of your board over time. The green line indicates the current value. The red line indicates the maximum value read since the last reset. The yellow line indicates the minimum value read since the last reset.

### 6.4.2.4. Graph Settings

The following controls allow you to define the look and feel of the power graph:

- **Scale select**—Specifies the amount to scale the power graph. Select a smaller number to zoom in to see finer detail. Select a larger number to zoom out to see the entire range of recorded values.
- **Update speed**—Specifies how often to refresh the graph.

### 6.4.2.5. Reset

Reset clears the graph, resets the minimum and maximum values, and restarts the Power Monitor.

## 6.5. The Clock Control

You can start the application with the following:

- The **ClockControl.exe** application that resides in the <install\_dir>\kits\cycloneVGT\_5cgtfd9ef35\_fpga\examples\board\_test\_system directory.

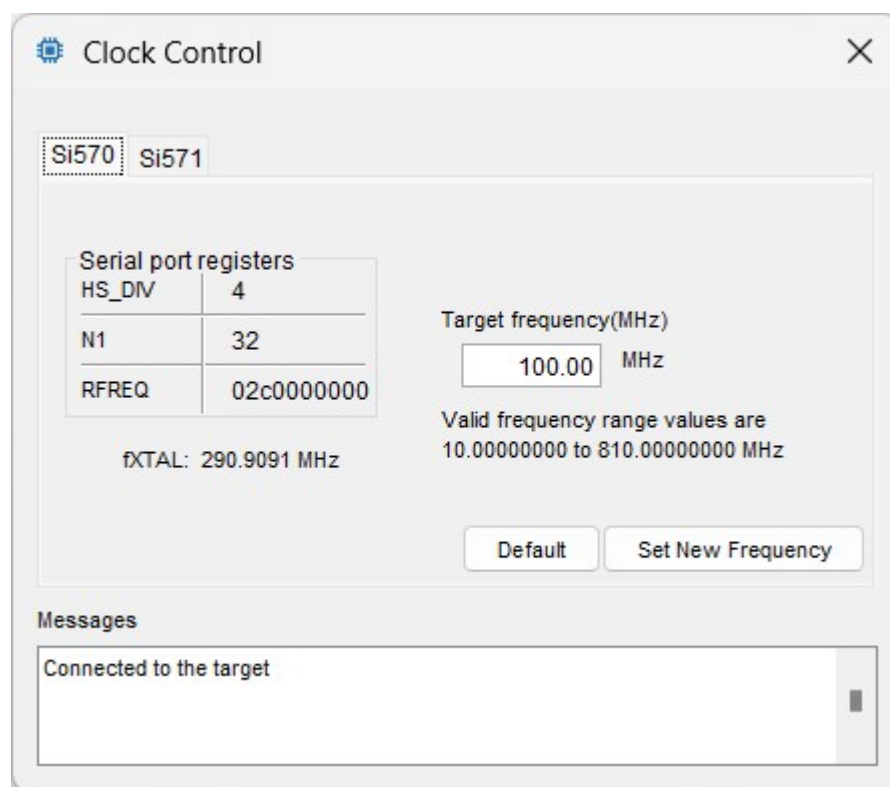
### 6.5.1. Clock Control Features

The Clock Control application sets the Si570 and Si571 programmable oscillators to any frequency between 10 MHz and 810 MHz.

- The Si570 (not the Si571) oscillator drives a 1-to-6 buffer that drives a copy of the clock to the following areas of the FPGA:
  - Top, bottom, and right edges
  - REFCLK0 and REFCLK3
- The 6th clock outputs to SMAs J4 and J7 on the board.
- The Clock Control communicates with the MAX V device on the board through the JTAG bus.
- The Si570 and Si571 programmable oscillators are connected to the MAX V device through a 2-wire serial bus.

The following figure shows the Clock Control Si570 tab, which has the same controls as the Si571 tab.

**Figure 15. The Clock Control - Si570 Tab**



### 6.5.2. Clock Control Controls

The following sections describe the Clock Control controls.

### 6.5.2.1. Serial Port Registers

This group shows the current values from the Si570 tab and Si571 tab registers.

For more information about the registers, refer to the *Si570/Si571* data sheet available on the Skyworks website.

#### Related Information

[Skyworks](#)

### 6.5.2.2. fXTAL

This control displays the calculated internal fixed-frequency crystal, based on the serial port register values.

For more information about the fXTAL value and how it is calculated, refer to the *Si570/Si571* data sheet available on the Skyworks website.

#### Related Information

[Skyworks](#)

### 6.5.2.3. Target Frequency

This control allows you to specify the frequency of the clock. Legal values are between 10–810 MHz with eight digits of precision to the right of the decimal point. For example, 421.31259873 is possible within 100 parts per million (ppm). The **Target frequency** control works in conjunction with the **Set New Frequency** control.

### 6.5.2.4. Clear

This control sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.

### 6.5.2.5. Set New Frequency

This control sets the programmable oscillator frequency for the selected clock to the value in the **Target frequency** control for the Si570 and Si571 oscillators. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Intel recommends resetting the FPGA logic after changing frequencies.

For more information about the *Si570/Si571* and the Cyclone V GT FPGA development board's clocking circuitry and clock input pins, refer to the *Cyclone V GT FPGA Development Board Reference Manual*.

#### Related Information

[Cyclone V GT FPGA Development Board Reference Manual](#)



## 7. Document Revision History for Cyclone V GT FPGA Development Kit User Guide

Document Version	Changes
2024.02.21	<ul style="list-style-type: none"> <li>Updated for latest branding standards.</li> <li>Added Table: <i>Cyclone V GT FPGA Development Kit Ordering Information</i>.</li> <li>Updated <i>Restoring the Flash Device to the Factory Settings</i> section.</li> <li>Updated <i>Preparing to Run the Board Test System</i> section.</li> <li>Updated figures in the following sections: <ul style="list-style-type: none"> <li>— <i>Board Test System</i></li> <li>— <i>The Configure Menu</i></li> <li>— <i>The System Info Tab</i></li> <li>— <i>The GPIO Tab</i></li> <li>— <i>The Flash Tab</i></li> <li>— <i>The DDR3x40 and DDR3x64 Tabs</i></li> <li>— <i>The HSMA Tab</i></li> <li>— <i>The HSMB Tab</i></li> <li>— <i>Power Monitor Features</i></li> <li>— <i>Clock Control Features</i></li> </ul> </li> <li>Added <i>Power Tree</i> section.</li> </ul>
2017.08.30	Added information about programming EPCQ.
2014.09.30	Additions for CE compliance: CE mark and statements.
2013.12.30	Initial release.

## A. Programming the Flash Memory Device

This appendix describes the pre-programmed contents of the common flash interface (CFI) flash memory device and how to reprogram the user portions of flash memory.

As you develop your own project using the Intel tools, you can program the flash memory device so that your own design loads from flash memory into the FPGA on power up. The FPGA development board ships with the flash memory preprogrammed with a default factory FPGA configuration. This configuration allows you to run the Board Update Portal design example and the Board Test System demonstration. There are several other factory software files written to the CFI flash device to support the Board Update Portal. These software files were created using the Nios II EDS, just as the hardware design was created using the Intel Quartus Prime software.

For more information about Intel development tools, refer to the *Intel Quartus Prime Software Suite and FPGA Development Tools* page of the Intel website.

### Related Information

- [Restoring the Flash Device to the Factory Settings](#) on page 16
- [Intel Quartus Prime Software Suite and FPGA Development Tools](#)

### A.1. CFI Flash Memory Map

The following table shows the default memory contents of the 1 Gb CFI flash device. For the Board Update Portal to run correctly and update designs in the user memory, this memory map must not be altered.

**Table 8. Byte Address Flash Memory Map**

Block Description	KB Size	Address Range
Unused	128	0x07FE.0000 – 0x07FF.FFFF
User software	76,416	0x0354.0000 – 0x07FD.FFFF
Factory software	8,192	0x02D4.0000 – 0x0353.FFFF
zipfs (html, web content)	8,192	0x0254.0000 – 0x02D3.FFFF
User hardware 2	12,672	0x018E.0000 – 0x0253.FFFF
User hardware 1	12,672	0x00C8.0000 – 0x018D.FFFF
Factory hardware	12,672	0x0002.0000 – 0x00C7.FFFF
PFL option bits	32	0x0001.8000 – 0x0001.FFFF
Board information	32	0x0001.0000 – 0x0001.7FFF
Ethernet option bits	32	0x0000.8000 – 0x0000.FFFF
User design reset vector	32	0x0000.0000 – 0x0000.7FFF

Intel recommends that you do not overwrite the factory hardware and factory software images unless you are an expert with the Intel tools. If you unintentionally overwrite the factory hardware or factory software image, refer to *Restoring the Flash Device to the Factory Settings*.

## A.2. Preparing Design Files for Flash Programming

The following sections use the following file types:

- Nios II Flash Programmer File (.flash)
- Executable and Linking Format File (.elf)
- SRAM Object File (.sof)
- S-Record File (.srec)

You can obtain designs containing prepared .flash files from the *Cyclone V GT FPGA Development Kit* page of the Intel website. You can also create .flash files from your own custom design.

The Nios II EDS sof2flash command line utility converts your Intel Quartus Prime-compiled .sof into the .flash format necessary for the flash device. Similarly, the Nios II EDS elf2flash command line utility converts your compiled and linked .elf software design to .flash.

For more information about Nios II EDS software tools and practices, refer to the *Embedded Software Developer Center* page of the Intel website.

### Related Information

- [Cyclone V GT FPGA Development Kit](#)
- [Embedded Software Developer Center](#)

## A.3. Creating Flash Files Using the Nios II EDS

If you have an FPGA design developed using the Intel Quartus Prime software, and software developed using the Nios II EDS, follow these instructions:

1. On the Windows Start menu, click **All Programs > Altera > Nios II EDS > Nios II Command Shell**.
2. In the Nios II command shell, navigate to the directory where your design files reside and type the following Nios II EDS commands:

- For Intel Quartus Prime .sof files:

```
sof2flash --input=<yourfile>_hw.sof --output=<yourfile>_hw.flash --  
offset=0xC80000  
--pfl --optionbit=0x00018000 --programmingmode=FPP
```

- For Nios II .elf files:

```
elf2flash --base=0x00000000 --end=0xFFFFFFFF --reset=0x3540000  
--input=<yourfile>_sw.elf --output=<yourfile>_sw.flash  
--boot=$SOPC_KIT_NIOS2/components/altera_nios2/boot_loader_cfi.srec
```

The resulting .flash files are ready for flash device programming.

The Board Update Portal standard `.flash` format conventionally uses either `<filename>_hw.flash` for hardware design files or `<filename>_sw.flash` for software design files.

## A.4. Converting Additional Files

If your design uses additional files such as image data or files used by the runtime program, you must first convert the files to `.flash` format. Once converted, concatenate them into one `.flash` file before using the Board Update Portal to upload them.

After your design files are in the `.flash` format, use one of the following to write the `.flash` files to the user software locations of the flash memory:

- Board Update Portal. Refer to *Using the Board Update Portal to Write User Designs* for more information.

Nios II EDS **nios2-flash-programmer** utility.

## A.5. Programming Flash Memory Using the Nios II EDS

The Nios II EDS offers a **nios2-flash-programmer** utility to program the flash memory directly. To program the `.flash` files or any compatible `.srec` file to the board using **nios2-flash-programmer**, do the following:

1. Set the SW4.3 DIP switch to the FACT ON (logic 0) to load the Board Update Portal design from flash memory on power up.
2. Attach the Intel FPGA Download Cable and power up the board.
3. If the board has powered up and the LCD displays either *Connecting...* or a valid IP address (such as 152.198.231.75), proceed to step 8. If no output appears on the LCD or if the Config Done LED (D7) does not illuminate, continue to step 4 to load the FPGA with a flash-writing design.
4. Run the Intel Quartus Prime Programmer to configure the FPGA with a `.sof` capable of flash programming. Refer to *Restoring the MAX V CPLD to the Factory Settings* for more information.
5. Click **Add File** and select `<install_dir>\kits  
\cycloneVGT_5cgtfd9ef35_fpga\factory_recovery  
\c5gt_fpga_bup.sof`.
6. Turn on the **Program/Configure** option for the added file.
7. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%. The Config Done LED (D7) illuminates indicating that the flash device is ready for programming.
8. In the Nios II command shell, navigate to the `<install_dir>\kits  
\cycloneVGT_5cgtfd9ef35_fpga\factory_recovery` directory.

You can also navigate to the directory of the `.flash` files you created in *Creating Flash Files Using the Nios II EDS*.

9. Type the following Nios II EDS command:

```
nios2-flash-programmer --base=0x00000000 <yourfile>_hw.flash
```

10. After programming completes, if you have a software file to program, type the following Nios II EDS command:

```
nios2-flash-programmer --base=0x00000000 <yourfile>_sw.flash
```

11. Set the SW4.3 DIP switch to the FACT OFF (logic 1) position and power cycle the board.

Programming the board is now complete.

To restore flash memory, refer to *Restoring the Flash Device to the Factory Settings*.

For more information about the **nios2-flash-programmer** utility, refer to the *Nios II Flash Programmer User Guide*.

#### Related Information

- [Restoring the MAX V CPLD to the Factory Settings](#) on page 15
- [Creating Flash Files Using the Nios II EDS](#) on page 43
- [Restoring the Flash Device to the Factory Settings](#) on page 16
- [Nios II Flash Programmer User Guide](#)

## A.6. Programming Flash Memory Using the Board Update Portal

Once you have the necessary `.flash` files, you can use the Board Update Portal to reprogram the flash memory. Refer to *Using the Board Update Portal to Write User Designs* for more information.

If you have generated a `.sof` that operates without a software design file, you can still use the Board Update Portal to upload your design. In this case, leave the **Software File Name** field blank.

#### Related Information

[Using the Board Update Portal to Write User Designs](#) on page 19

## B. Additional Information

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This chapter provides additional information about the document and Intel.

### B.1. Safety and Regulatory Information



#### **ENGINEERING DEVELOPMENT PRODUCT - NOT FOR RESALE OR LEASE**

This development kit is intended for laboratory development and engineering use only.

This development kit is designed to allow:

- Product developers and system engineers to evaluate electronic components, circuits, or software associated with the development kit to determine whether to incorporate such items in a finished product.
- Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required Federal Communications Commission (FCC) equipment authorizations are first obtained.

Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference.

Unless the assembled kit is designed to operate under Part 15, Part 18 or Part 95 of the United States Code of Federal Regulations (CFR) Title 47, the operator of the kit must operate under the authority of an FCC licenseholder or must secure an experimental authorization under Part 5 of the United States CFR Title 47.

Safety Assessment and CE & UKCA mark requirements have been completed, however, other certifications that may be required for installation and operation in your region have not been obtained.

### B.1.1. Safety Warnings





#### Power Supply Hazardous Voltage

AC mains voltages are present within the power supply assembly. No user serviceable parts are present inside the power supply.


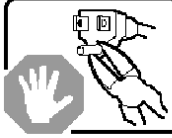
#### Power Connect and Disconnect

The AC power supply cord is the primary disconnect device from mains (AC power) and used to remove all DC power from the board/system. The socket outlet must be installed near the equipment and must be readily accessible.

	<b>WARNING</b>	
<b>RISK OF ELECTRIC SHOCK</b>		
Connect only to a properly earth grounded outlet. Apparaten skall anslutas till jordat uttag när den ansluts till ett nätverk.		

#### System Grounding (Earthing)

To avoid shock, you must ensure that the power cord is connected to a properly wired and grounded receptacle. Ensure that any equipment to which this product is attached to is also connected to properly wired and grounded receptacles.

	<b>WARNING</b>	
<b>RISK OF ELECTRIC SHOCK</b>		
Do not attempt to modify or use the supplied AC power cord if it is not the exact type and rating required.		

### Power Cord Requirements

The plug on the power cord must be a grounding-type male plug designed for use in your region. It must have certification marks showing certification by an agency in your region. The connector that plugs into the appliance inlet of the power supply must be an IEC 320, sheet C13, female connector. If the power cord supplied with the system does not meet requirements for use in your region, discard the cord, and do not use it with adapters. Use only certified power supply cord with appropriate gauge, designed for use in your region.



### Lightning/Electrical Storm

Do not connect/disconnect any cables or perform installation/maintenance of this product during an electrical storm.

### Risk of Fire

To reduce the risk of fire, keep all flammable materials a safe distance away from the boards and power supply. You must configure the development kit on a flame retardant surface.

## B.1.2. Safety Cautions

	<p><b>CAUTION</b></p>	
	<p><b>Hot Surfaces and Sharp Edges</b></p>	
<p><b>Integrated Circuits and heat sinks may be hot if the system has been running. Also, there might be sharp pins and edges on some boards. Contact should be avoided.</b></p>		

### Thermal and Mechanical Injury

Certain components such as heat sinks, power regulators, and processors may be hot. Heatsink fans are not guarded. Power supply fan may be accessible through guard. Care should be taken to avoid contact with these components.





### Cooling Requirements

Maintain a minimum clearance area of 5 centimeters (2 inches) around the side, front and back of the board for cooling purposes. Do not block power supply ventilation holes and fan.

### Electro-Magnetic Interference (EMI)

This equipment has not been tested for compliance with emission limits of FCC and similar international regulations. Use of this equipment in a residential location is prohibited. This equipment generates, uses and can radiate radio frequency energy which may result in harmful interference to radio communications. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment on and off, you are required to take measures to eliminate this interference.

### Telecommunications Port Restrictions

The wireline telecommunications ports (modem, xDSL, T1/E1) on this product must not be connected to the Public Switched Telecommunication Network (PSTN) as it might result in disruption of the network. No formal telecommunication certification to FCC, R&TTE Directive, or other national requirements have been obtained.



### Electrostatic Discharge (ESD) Warning

A properly grounded ESD wrist strap must be worn during operation/installation of the boards, connection of cables, or during installation or removal of daughter cards. Failure to use wrist straps can damage components within the system.

**Attention:** Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of this product in unsorted municipal waste.

### Lithium Ion Battery Warnings



**Lithium Battery:** Risk of explosion if the lithium battery is replaced by an incorrect type. Risk of fire, explosion, or chemical burn if the battery is mistreated (punctured or crushed). Do not attempt to disassemble. Do not incinerate. Observe proper polarity when replacing battery. Do not dispose—the battery is intended to be serviced and disposed by qualified Intel service personnel only.

**Perchlorate Material:** Special handling may apply. For more details, refer to [www.dtsc.ca.gov/hazardouswaste/perchlorate](http://www.dtsc.ca.gov/hazardouswaste/perchlorate). This notice is required by California Code of Regulations, Title 22, Division 4.5, Chapter 33: Best Management Practices for Perchlorate Materials. This product includes a battery which contains perchlorate material.

### Taiwan battery recycling:



廢電池請回收

(Translation - please recycle batteries)

**Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of product in unsorted municipal waste.**

## **B.2. Compliance Information**

### **CE EMI Conformity Caution**

This development board is delivered conforming to relevant standards mandated by Directive 2014/30/EU. Because of the nature of programmable logic devices, it is possible for the user to modify the development kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as a result of modifications to the delivered material is the responsibility of the user of this development kit.

